Compal confidential

Hamburg 10ADG

NALAE LA-6054P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

2009-02-04 Rev. 0.2

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: *SCHEMATIC,MB A6054*

Size: Custom	Document Number: *401871*	Rev: B
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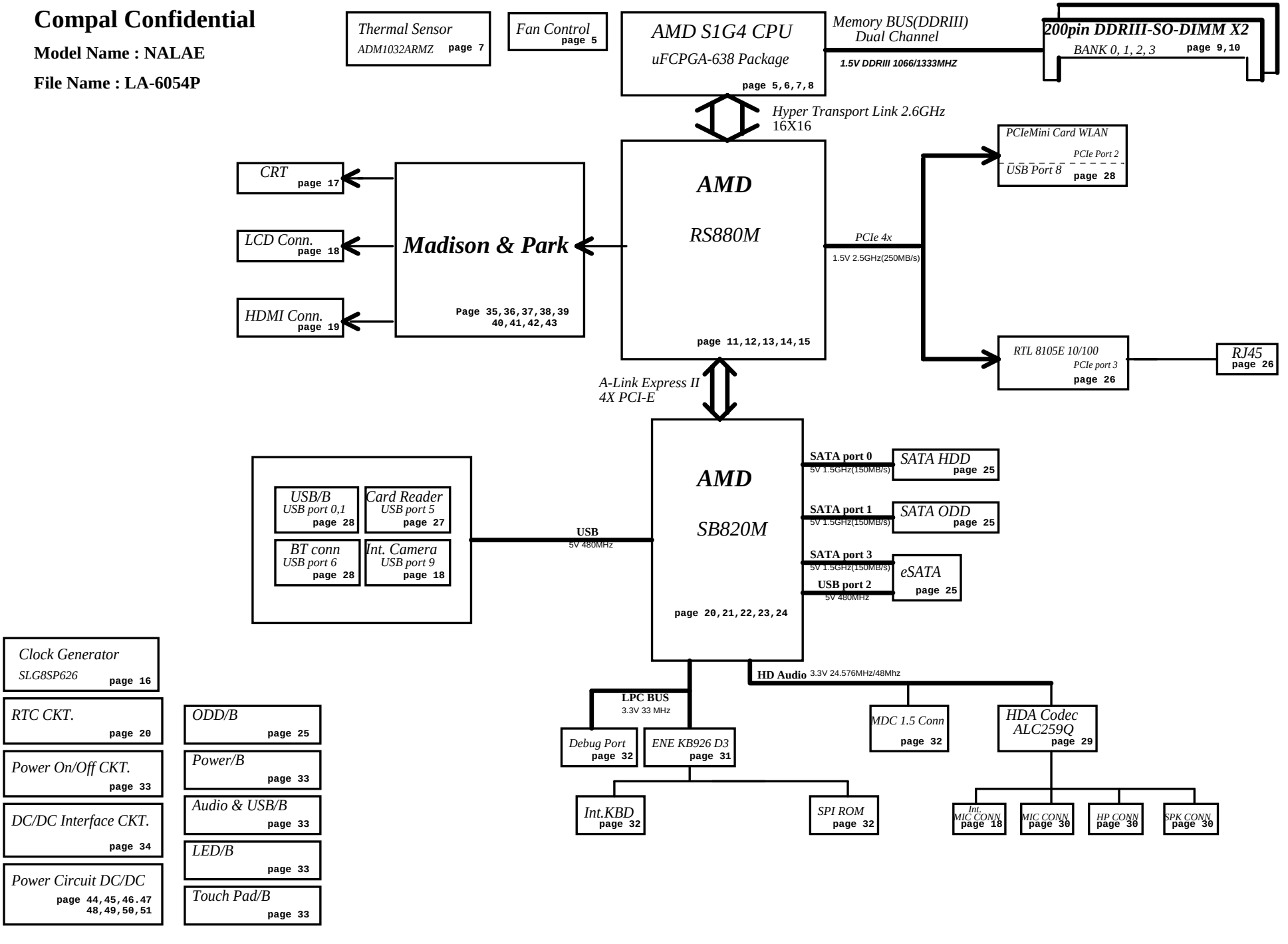
Compal Confidential

Model Name : NALAE

File Name : LA-6054P



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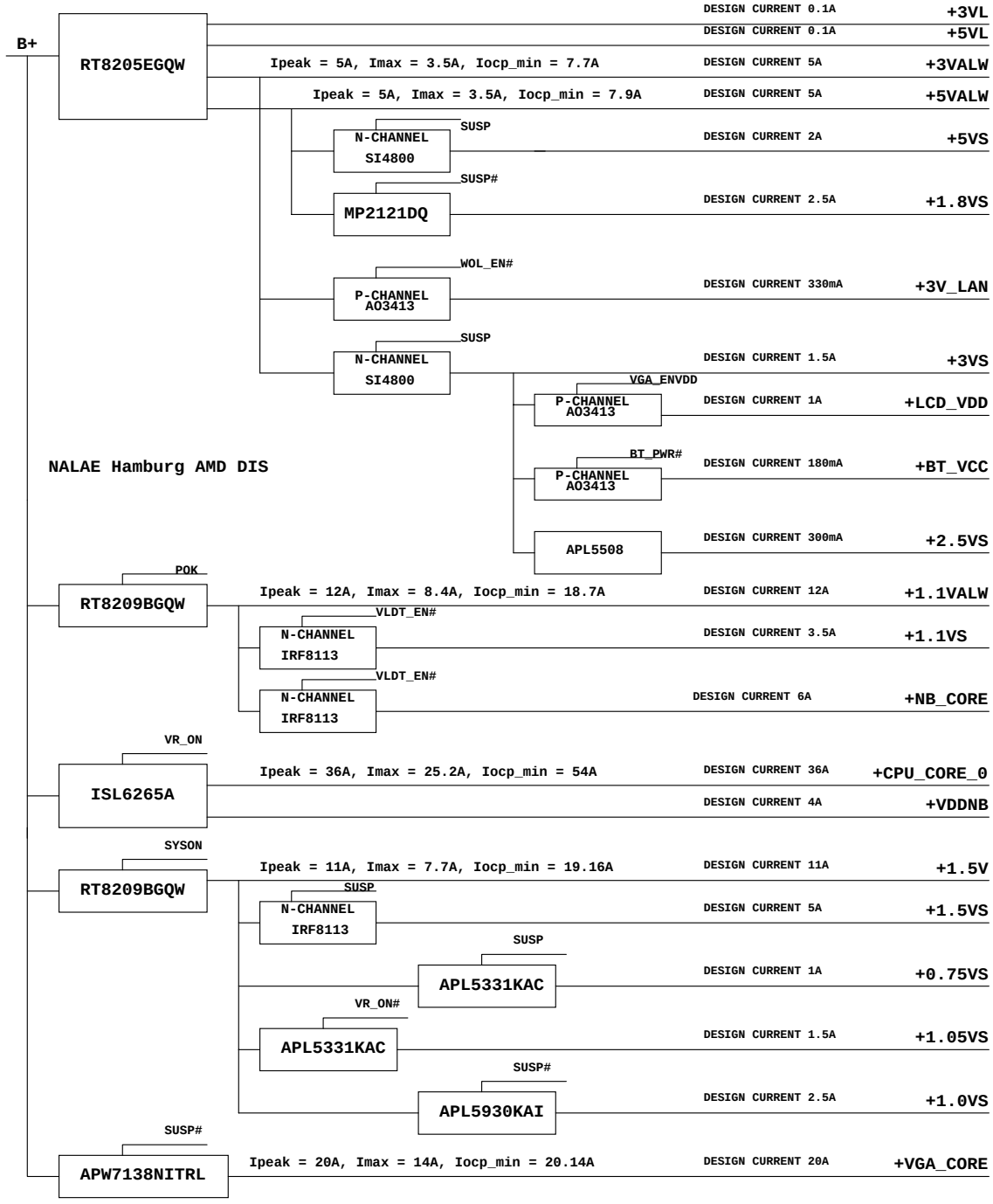

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Voltage Rails

O : ON
X : OFF

State \ power plane	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE +NB_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: Digital Ground

: Analog Ground

@ : just reserve , no build

GPU	CPU	NB	VGA	SB	Comment
Manhattan	S1G4	RS880M	MADISON	SB820M	Madison@ or PARK@ +4PCS or 8PCS
	S1G4	RS880M	PARK	SB820M	
M96/M92	S1G4	RS880M	M96	SB820M	M9X@+M96@ or M92@ +4PCS or 8PCS
	S1G4	RS880M	M92	SB820M	

Platform	CPU	NB	VGA	SB	Comment
Danube					
	S1G4	RS880M	NA	SB820M	

BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	(B)	(Y)				
Explain						
BTO	BT@	H@				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D3		

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+1.1VS

250 mil VLDT CAP. Near CPU Socket

C1 10U_0805_10V4Z | C2 10U_0805_10V4Z | C3 0.22U_0603_16V4Z | C4 0.22U_0603_16V4Z | C5 180P_0402_50V8J | C6 180P_0402_50V8J

<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]
H_CADOP[0..15] H_CADOP[0..15] <11>
H_CADON[0..15] H_CADON[0..15] <11>

+1.1VS

JCPUA

VLDT=500mA

HT LINK

D1	VLDT_A0	VLDT_B0	AE2	+VLDT_B	C7 10U_0805_10V4Z
D2	VLDT_A1	VLDT_B1	AE3		
D3	VLDT_A2	VLDT_B2	AE4		
D4	VLDT_A3	VLDT_B3	AE5		

< VLDT_A & VLDT_B : HyperTransport I/O ring power >

< From NB >

H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	E5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

< To NB >

<11> H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 <11>
<11> H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 <11>
<11> H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 <11>
<11> H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 <11>
<11> H_CTLIP0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 <11>
<11> H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 <11>
<11> H_CTLIP1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	H_CTLOP1 <11>
<11> H_CTLIN1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	H_CTLON1 <11>

FOX_PZ6382A-284S-41F_Champlian

< FAN Control Circuit : Vout = 1.6 x Vset >

+5VS

1A

+FAN1

C1120 10U_0805_10V4Z

C1119 10U_0805_10V4Z

U31

1	EN	GND	8
2	VIN	GND	7
3	VOUT	GND	6
4	VSET	GND	5

APL5607KI-TRG_SO8

<30> EN_DFAN1

@ C1121 1000P_0402_25V8J

JFAN

1	+FAN1	4	GND
2		5	GND
3			

@ACES_85204-0300N

+3VS

R795 10K_0402_5%

@ C1122 0.01U_0402_25V7K

FAN_SPEED1 <30>

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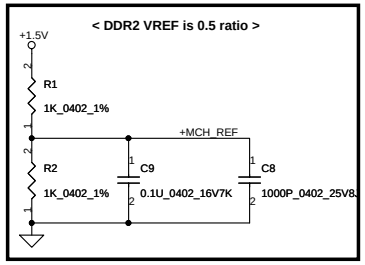
< DDR2 VREF is 0.5 ratio >



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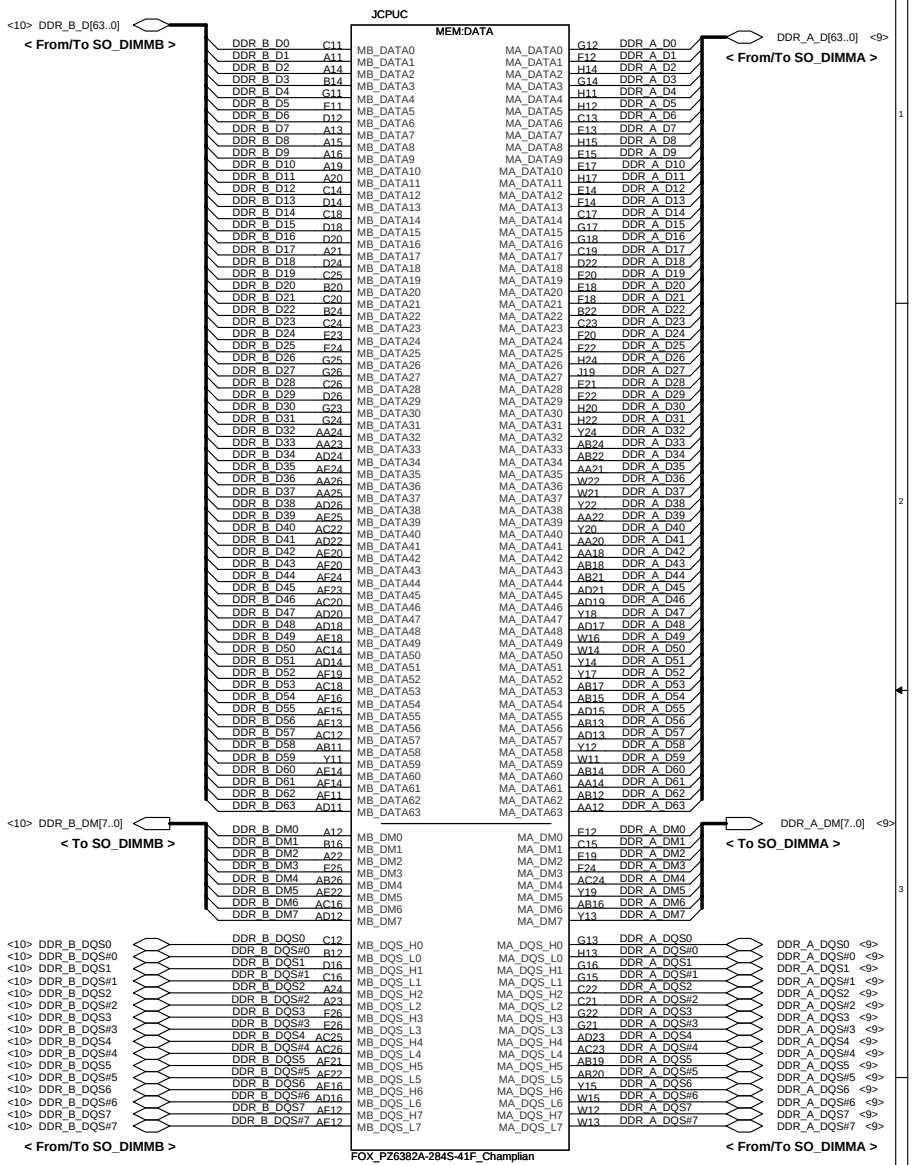

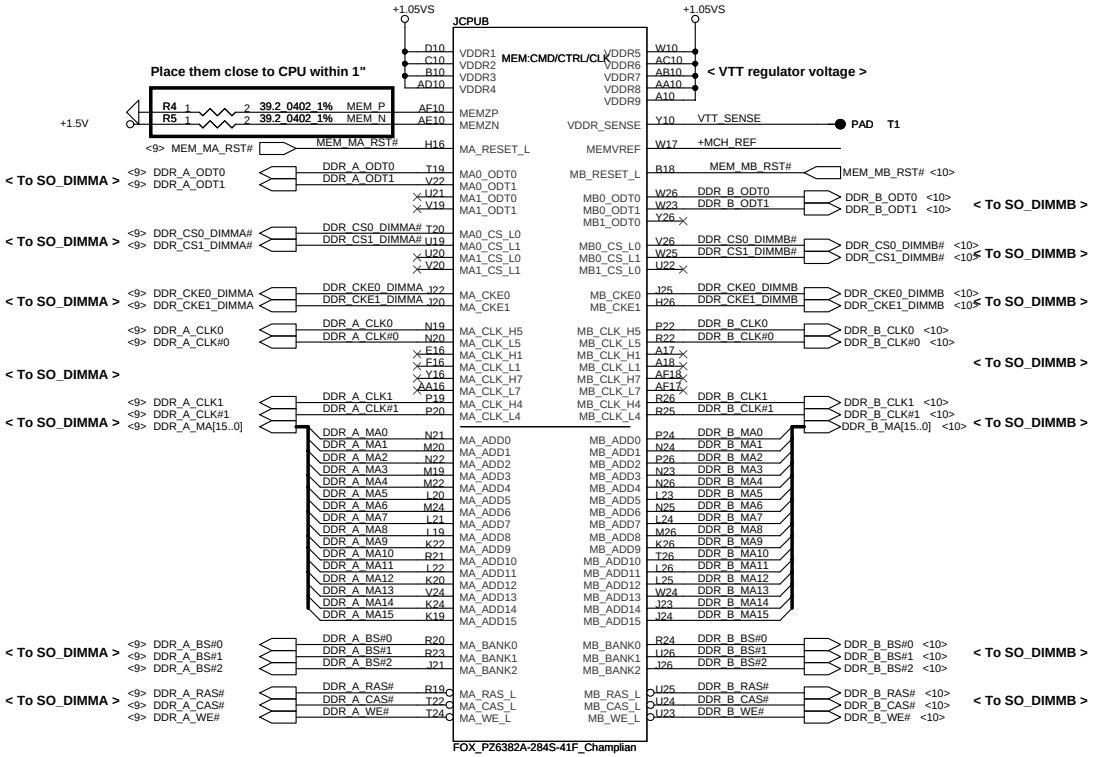

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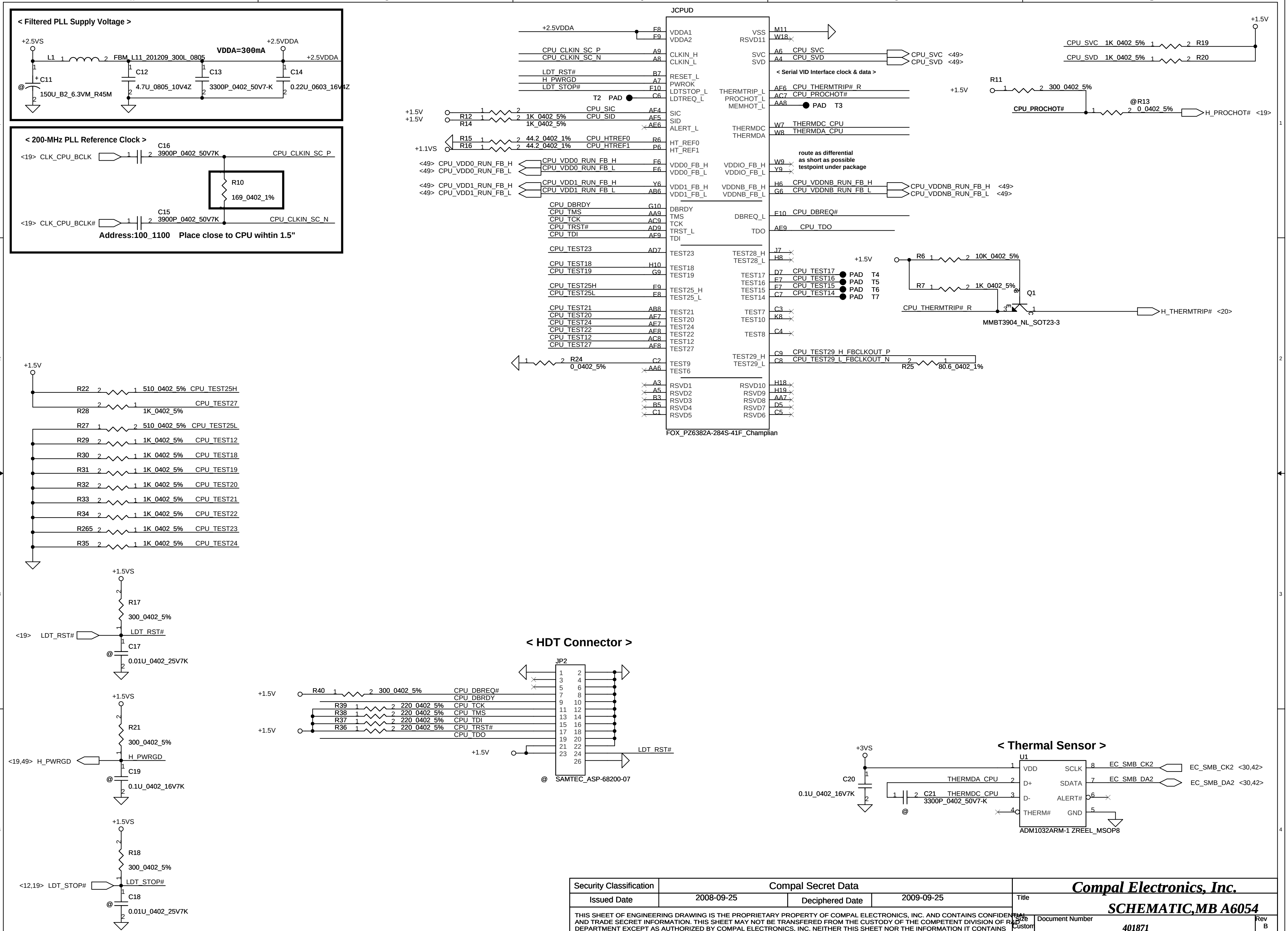

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VDD decoupling : +CPU_CORE

+CPU_CORE — C26 330U_X_2VM_R6M, C25 330U_X_2VM_R6M — Near CPU Socket

+CPU_CORE — C35, C34, C28, C29 22U_0805_6.3V6M — Under CPU Socket

+CPU_CORE — C36 0.22U_0603_16V4Z, C37 0.01U_0402_25V7K, C38 180P_0402_50V8J — Under CPU Socket

+CPU_CORE — @C23, C89, @C24, C90 330U_X_2VM_R6M / 330U_2.5V_M — Near CPU Socket

+CPU_CORE — C30, C31, C32, C33 22U_0805_6.3V6M — Under CPU Socket

+CPU_CORE — C39 0.22U_0603_16V4Z, C40 0.01U_0402_25V7K, C41 180P_0402_50V8J — Under CPU Socket

VDDIO decoupling : DDR SDRAM I/O ring power

+1.5V — C44, C45 22U_0805_6.3V6M; C46, C47 0.22U_0603_16V4Z; C48 180P_0402_50V8J; C50 180P_0402_50V8J — Under CPU Socket

+1.5V — C54, C51, C52, C53 0.22U_0603_16V4Z — Between CPU Socket and DIMM

+1.5V — C64, C65 0.01U_0402_25V7K — Between CPU Socket and DIMM

+1.5V — 180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch> — C66, C67, C68, C69 180P_0402_50V8J — Between CPU Socket and DIMM

C56 Co-layout with C75

+1.5V — C56 390U_2.5V_M_R10

+1.5V — C71, C72, C73, C74 4.7U_0805_10V4Z — Between CPU Socket and DIMM; @C75 330U_D2E_2.5VM_R6M

C1124 Co-layout with C1125

+1.05VS — C1124 390U_2.5V_M_R10

VDDR decoupling.

+1.05VS — C57, C58 4.7U_0805_10V4Z; C59, C60 0.22U_0603_16V4Z; C61 1000P_0402_25V8J; C62 1000P_0402_25V8J; C63 180P_0402_50V8J; C70 180P_0402_50V8J — Near CPU Socket Right side

+1.05VS — C76, C77 4.7U_0805_10V4Z; C78, C79 0.22U_0603_16V4Z; C80 1000P_0402_25V8J; C81 1000P_0402_25V8J; C82 180P_0402_50V8J; C83 180P_0402_50V8J — Near CPU Socket Left side

+1.05VS — @C1125 330U_D2E_2.5VM

+VDDNB decoupling : Northbridge power

+VDDNB — C42, C43 22U_0805_6.3V6M; C49 22U_0805_6.3V6M

+CPU_CORE — JCPUE — +CPU_CORE

G4	VDD0_1	VDD1_1	P8
H2	VDD0_2	VDD1_2	P10
J9	VDD0_3	VDD1_3	R4
J11	VDD0_4	VDD1_4	R7
J13	VDD0_5	VDD1_5	R9
J15	VDD0_6	VDD1_6	R11
K6	VDD0_7	VDD1_7	T2
K10	VDD0_8	VDD1_8	T6
K12	VDD0_9	VDD1_9	T8
K14	VDD0_10	VDD1_10	T10
L4	VDD0_11	VDD1_11	T12
L7	VDD0_12	VDD1_12	T14
L9	VDD0_13	VDD1_13	U7
L11	VDD0_14	VDD1_14	U9
L13	VDD0_15	VDD1_15	U11
L15	VDD0_16	VDD1_16	U13
M2	VDD0_17	VDD1_17	U15
M6	VDD0_18	VDD1_18	V6
M8	VDD0_19	VDD1_19	V8
M10	VDD0_20	VDD1_20	V10
N7	VDD0_21	VDD1_21	V12
N9	VDD0_22	VDD1_22	V14
N11	VDD0_23	VDD1_23	W4
		VDD1_24	Y2
K16	VDDNB_1	VDD1_25	AC4
M16	VDDNB_2	VDD1_26	AD2
P16	VDDNB_3		
T16	VDDNB_4	VDDIO27	Y25
V16	VDDNB_5	VDDIO26	V25
		VDDIO25	V23
H25	VDDIO1	VDDIO24	V21
J17	VDDIO2	VDDIO23	V18
K18	VDDIO3	VDDIO22	U17
K21	VDDIO4	VDDIO21	T25
K23	VDDIO5	VDDIO20	T23
K25	VDDIO6	VDDIO19	T21
L17	VDDIO7	VDDIO18	T18
M18	VDDIO8	VDDIO17	R17
M21	VDDIO9	VDDIO16	P25
M23	VDDIO10	VDDIO15	P23
M25	VDDIO11	VDDIO14	P21
N17	VDDIO12	VDDIO13	P18

+VDDNB — +1.5V — FOX_PZ6382A-284S-41F_Champlian

JCPUF

AA4	VSS1	VSS66	J6
AA11	VSS2	VSS67	J8
AA13	VSS3	VSS68	J10
AA15	VSS4	VSS69	J12
AA17	VSS5	VSS70	J14
AA19	VSS6	VSS71	J16
AB2	VSS7	VSS72	J18
AB7	VSS8	VSS73	K2
AB9	VSS9	VSS74	K7
AB23	VSS10	VSS75	K9
AB25	VSS11	VSS76	K11
AC11	VSS12	VSS77	K13
AC13	VSS13	VSS78	K15
AC15	VSS14	VSS79	K17
AC17	VSS15	VSS80	L6
AC19	VSS16	VSS81	L8
AC21	VSS17	VSS82	L10
AD6	VSS18	VSS83	L12
AD8	VSS19	VSS84	L14
AD25	VSS20	VSS85	L16
AE11	VSS21	VSS86	L18
AE13	VSS22	VSS87	M7
AE15	VSS23	VSS88	M9
AE17	VSS24	VSS89	AC6
AE19	VSS25	VSS90	M17
AE21	VSS26	VSS91	N4
AE23	VSS27	VSS92	N8
B4	VSS28	VSS93	N10
B6	VSS29	VSS94	N16
B8	VSS30	VSS95	N18
B9	VSS31	VSS96	P2
B11	VSS32	VSS97	P7
B13	VSS33	VSS98	P9
B15	VSS34	VSS99	P11
B17	VSS35	VSS100	P17
B19	VSS36	VSS101	R8
B21	VSS37	VSS102	R10
B23	VSS38	VSS103	R16
B25	VSS39	VSS104	R18
D6	VSS40	VSS105	T7
D8	VSS41	VSS106	T9
D9	VSS42	VSS107	T11
D11	VSS43	VSS108	T13
D13	VSS44	VSS109	T15
D15	VSS45	VSS110	T17
D17	VSS46	VSS111	U4
D19	VSS47	VSS112	U6
D21	VSS48	VSS113	U8
D23	VSS49	VSS114	U10
D25	VSS50	VSS115	U12
E4	VSS51	VSS116	U14
F2	VSS52	VSS117	U16
F11	VSS53	VSS118	U18
F13	VSS54	VSS119	V2
F15	VSS55	VSS120	V7
F17	VSS56	VSS121	V9
F19	VSS57	VSS122	V11
F21	VSS58	VSS123	V13
F23	VSS59	VSS124	V15
F25	VSS60	VSS125	V17
H7	VSS61	VSS126	W6
H9	VSS62	VSS127	Y21
H21	VSS63	VSS128	Y23
H23	VSS64	VSS129	N6
J4	VSS65		

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DIMM_A STD H:5.2 mm

<Address: 00>

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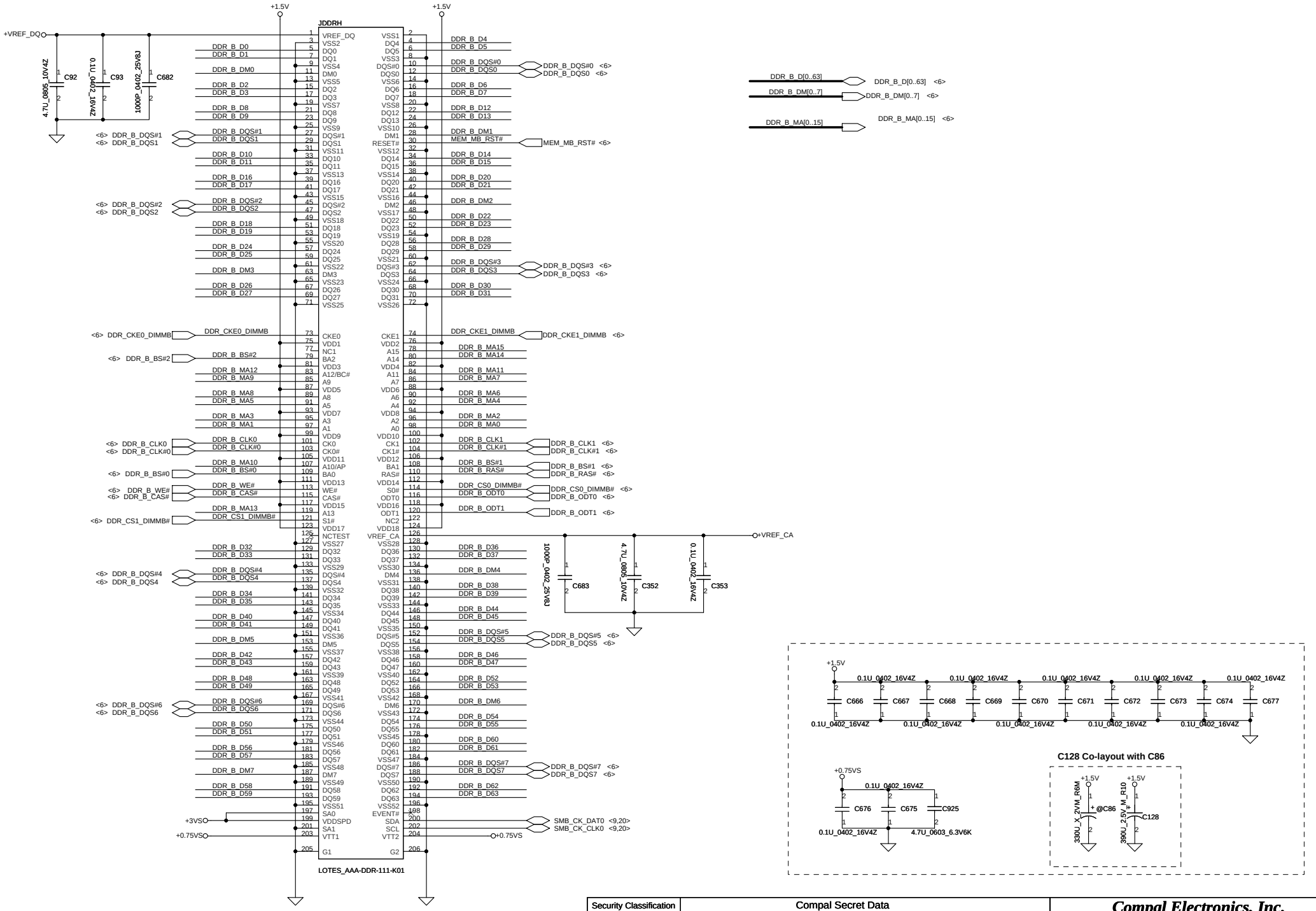

DIMM_B STD H:9.2 mm

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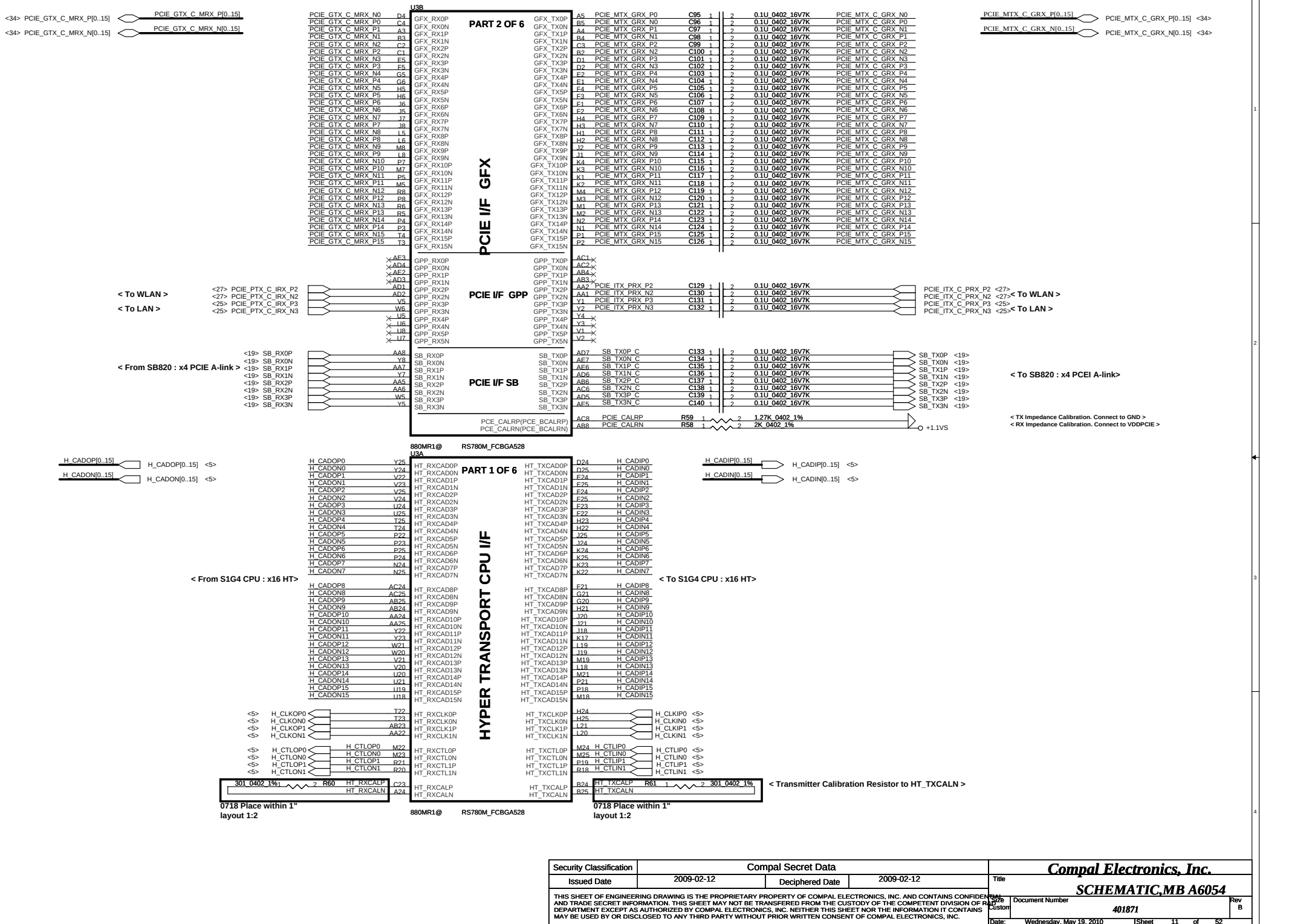

Security Classification	Compal Secret Data		
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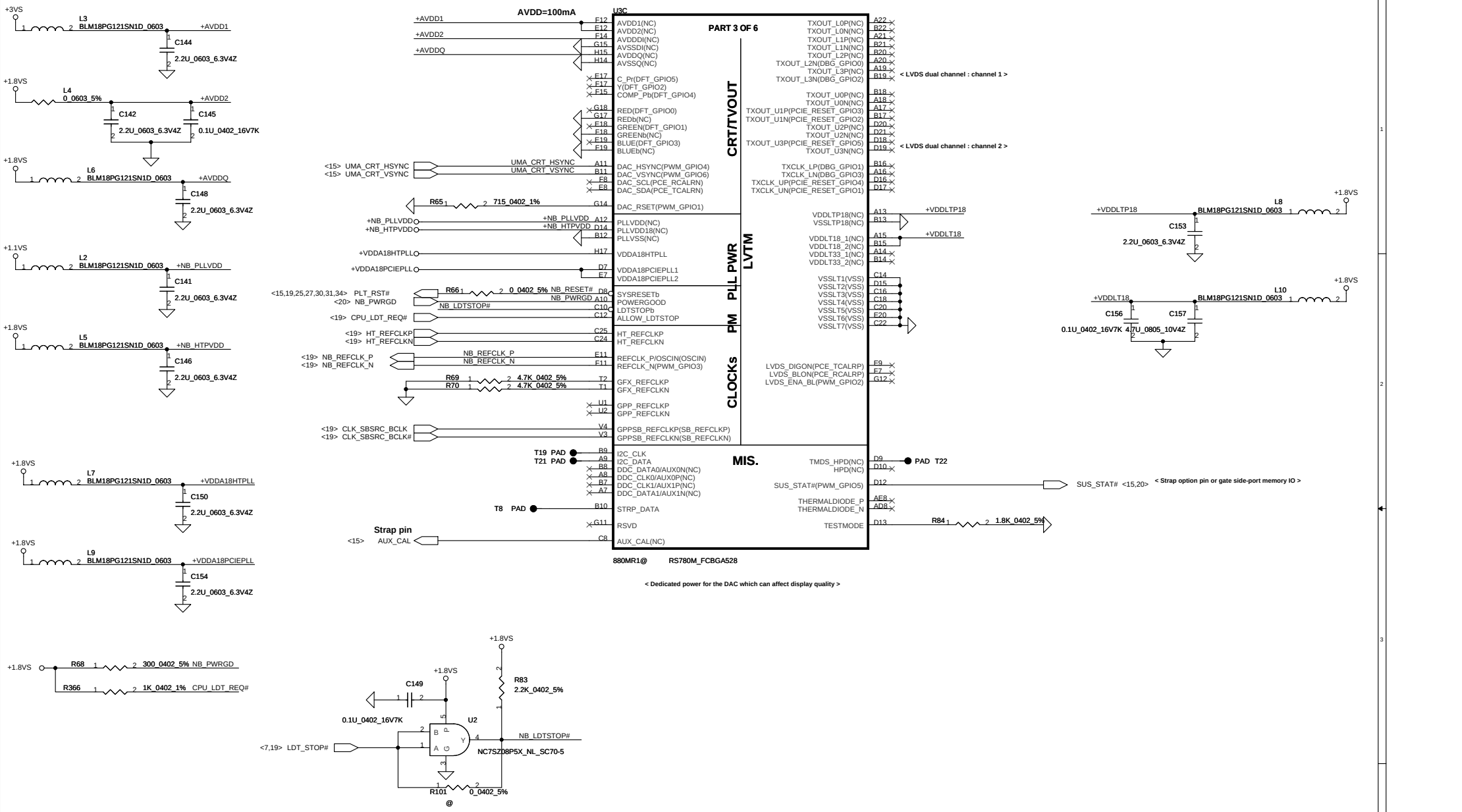

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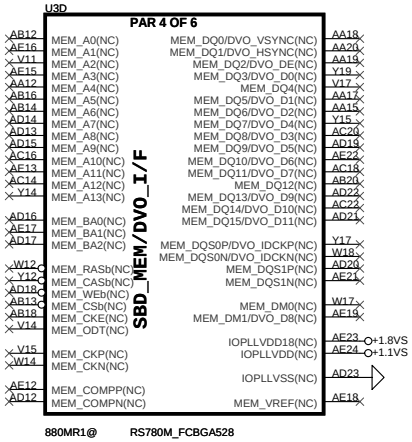

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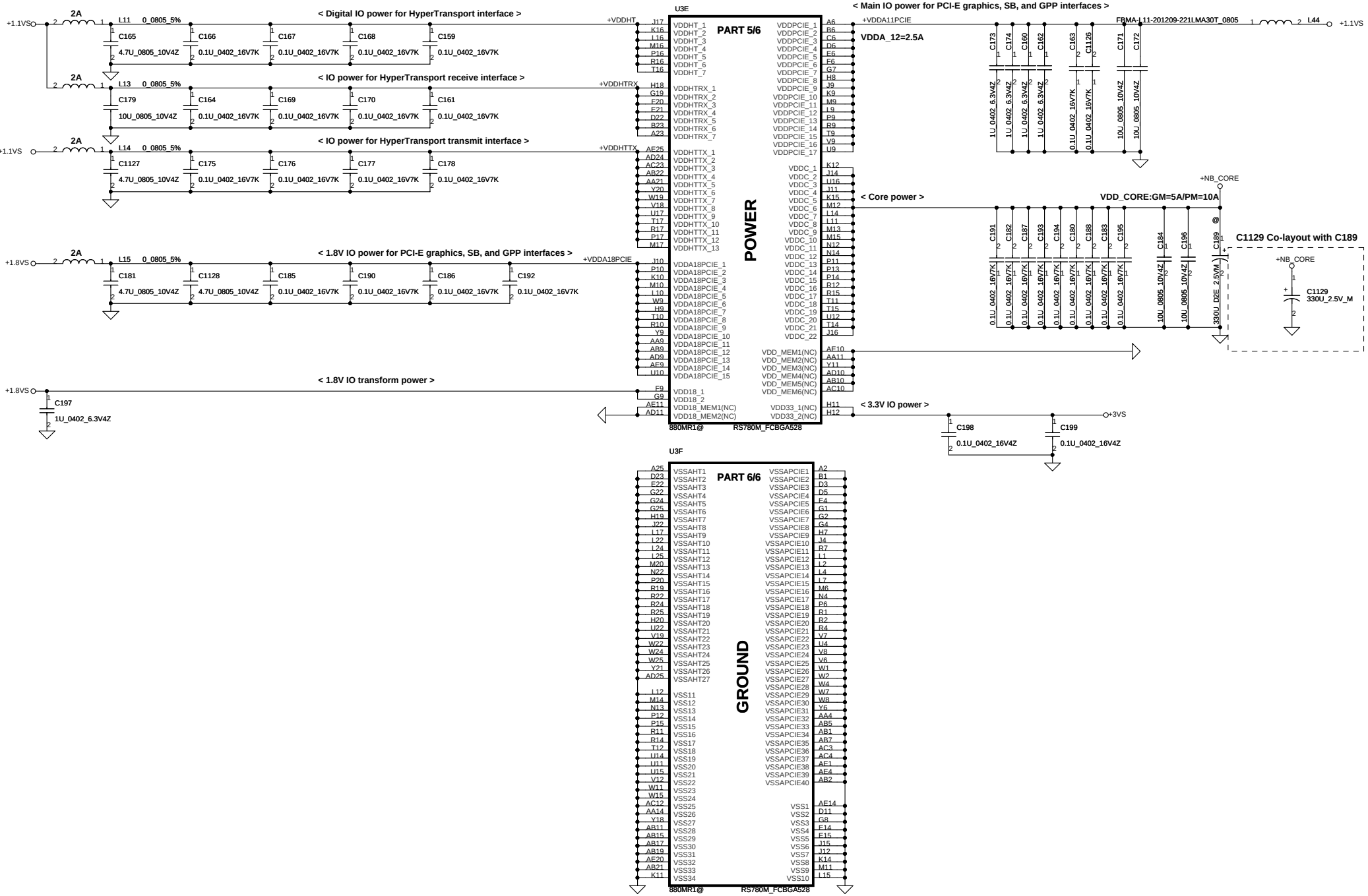

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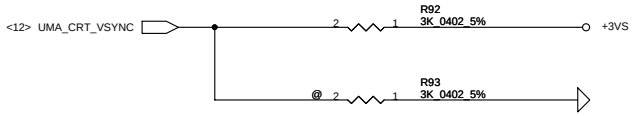
< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

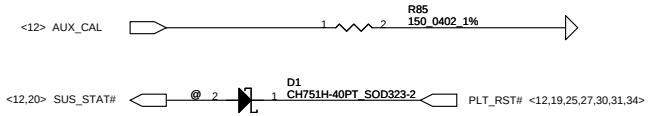
PIN: RS880--> VSYNC#

< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



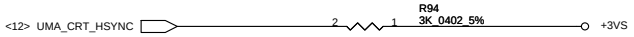
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

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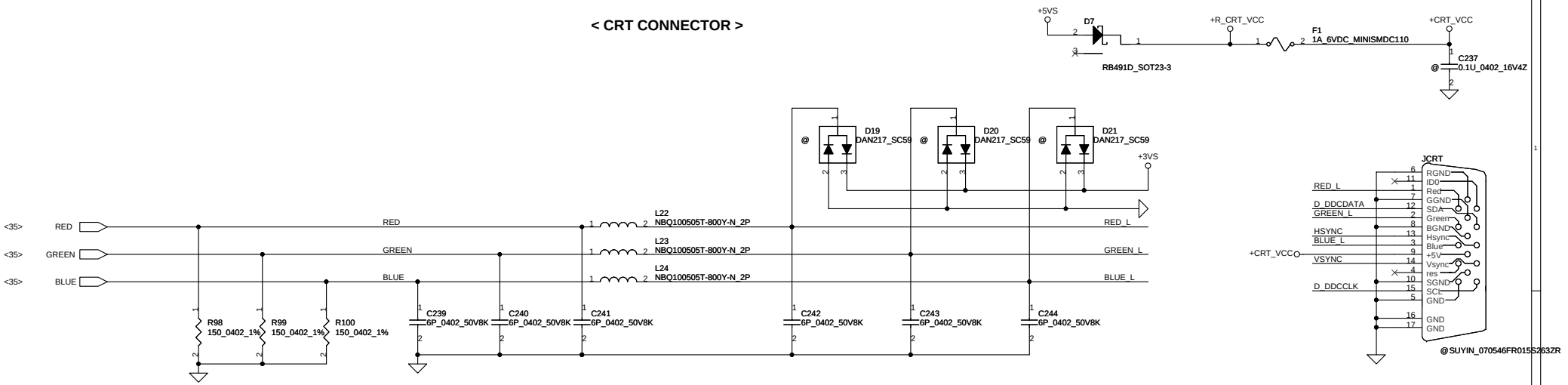
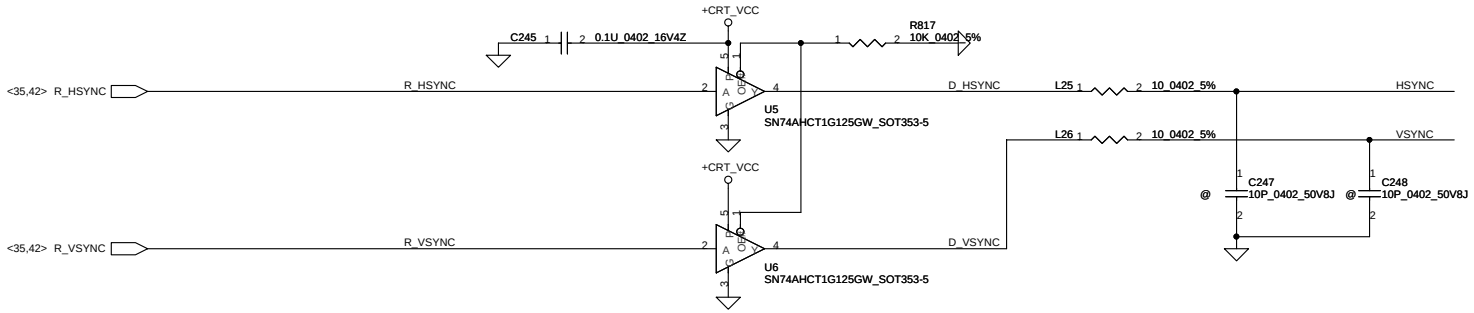
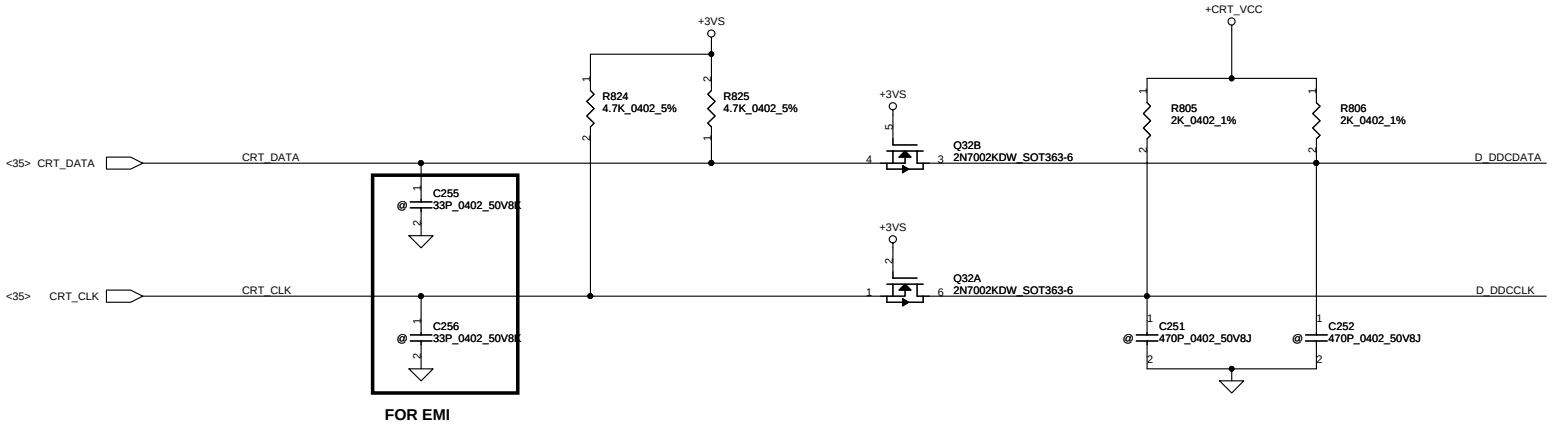
< CRT CONNECTOR >



< SYNC SIGNAL >



< Display Data Channel >



FOR EMI

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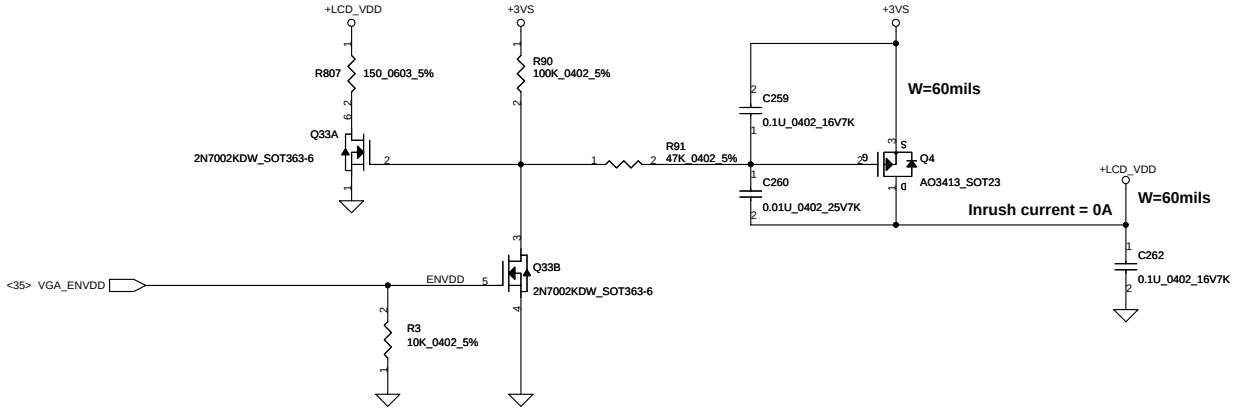
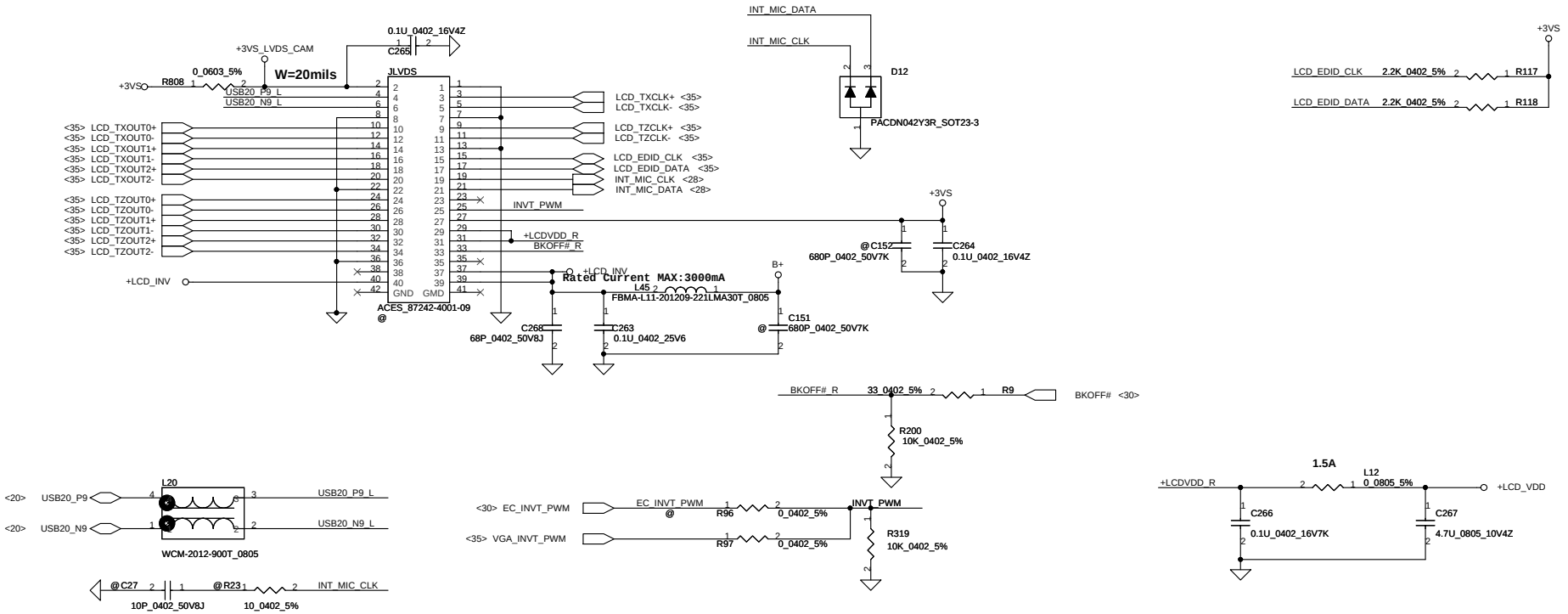
LCD/PANEL BD. Conn.



< LVDS Connector >



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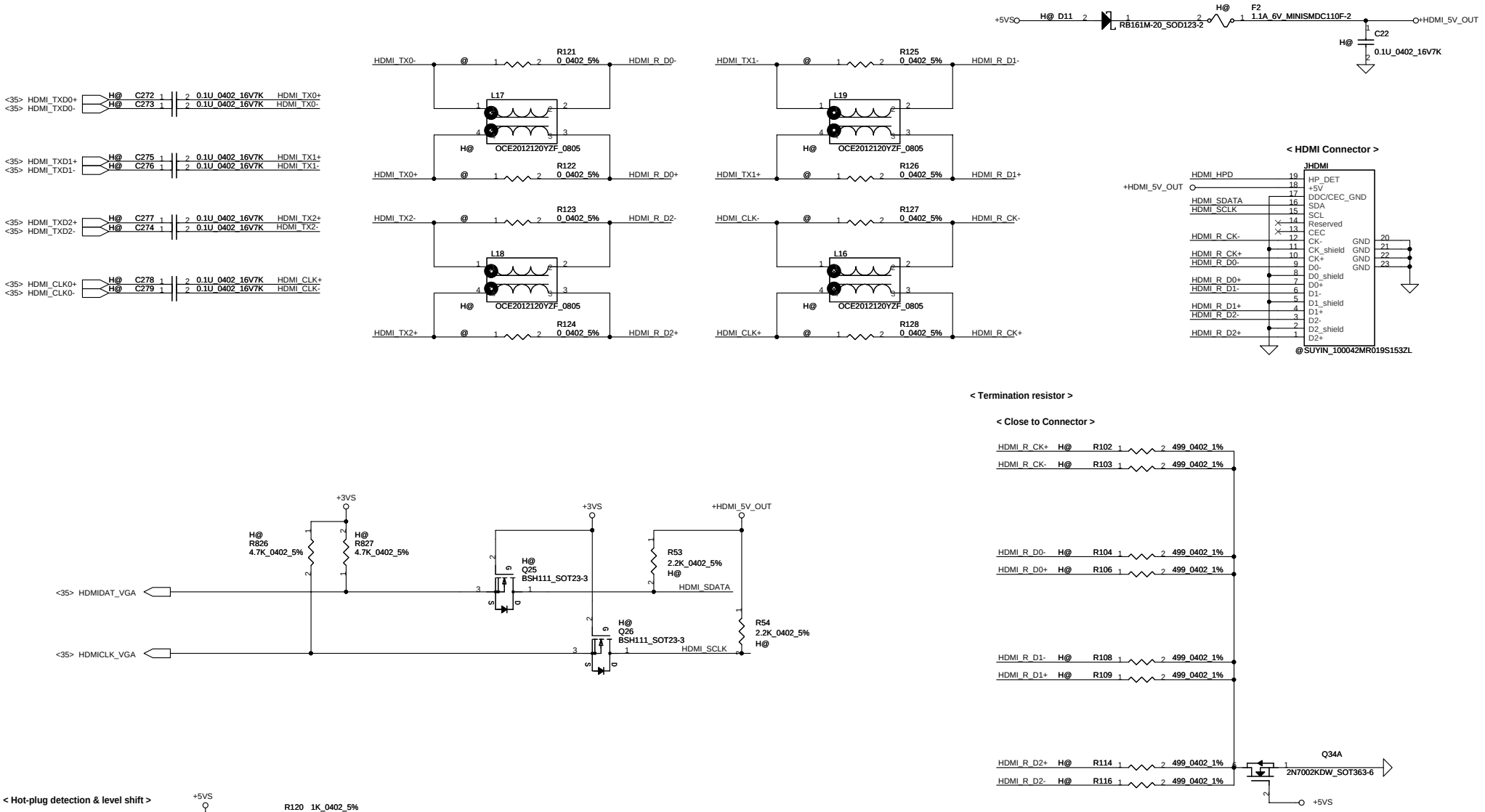

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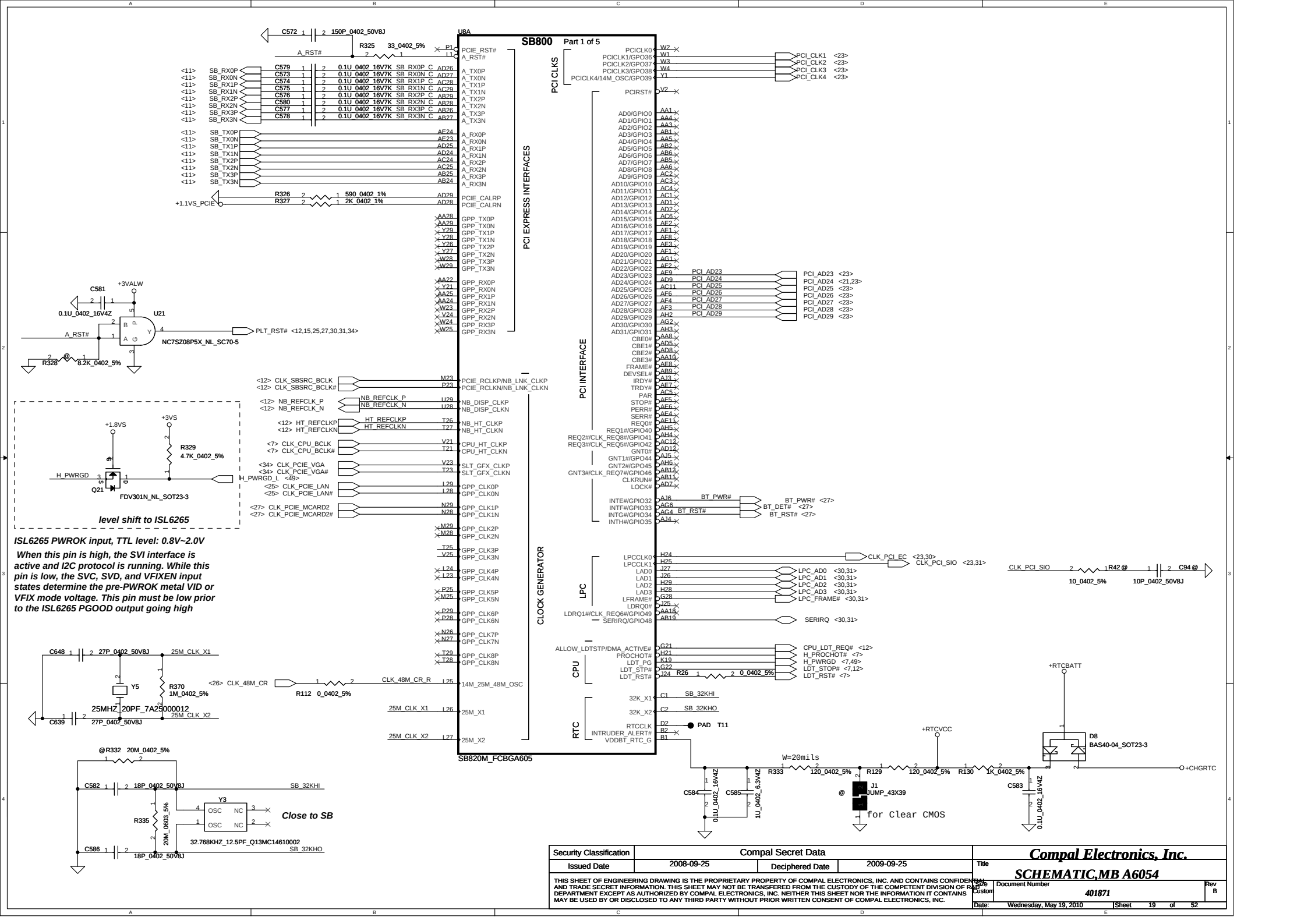

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Compal Electronics, Inc.

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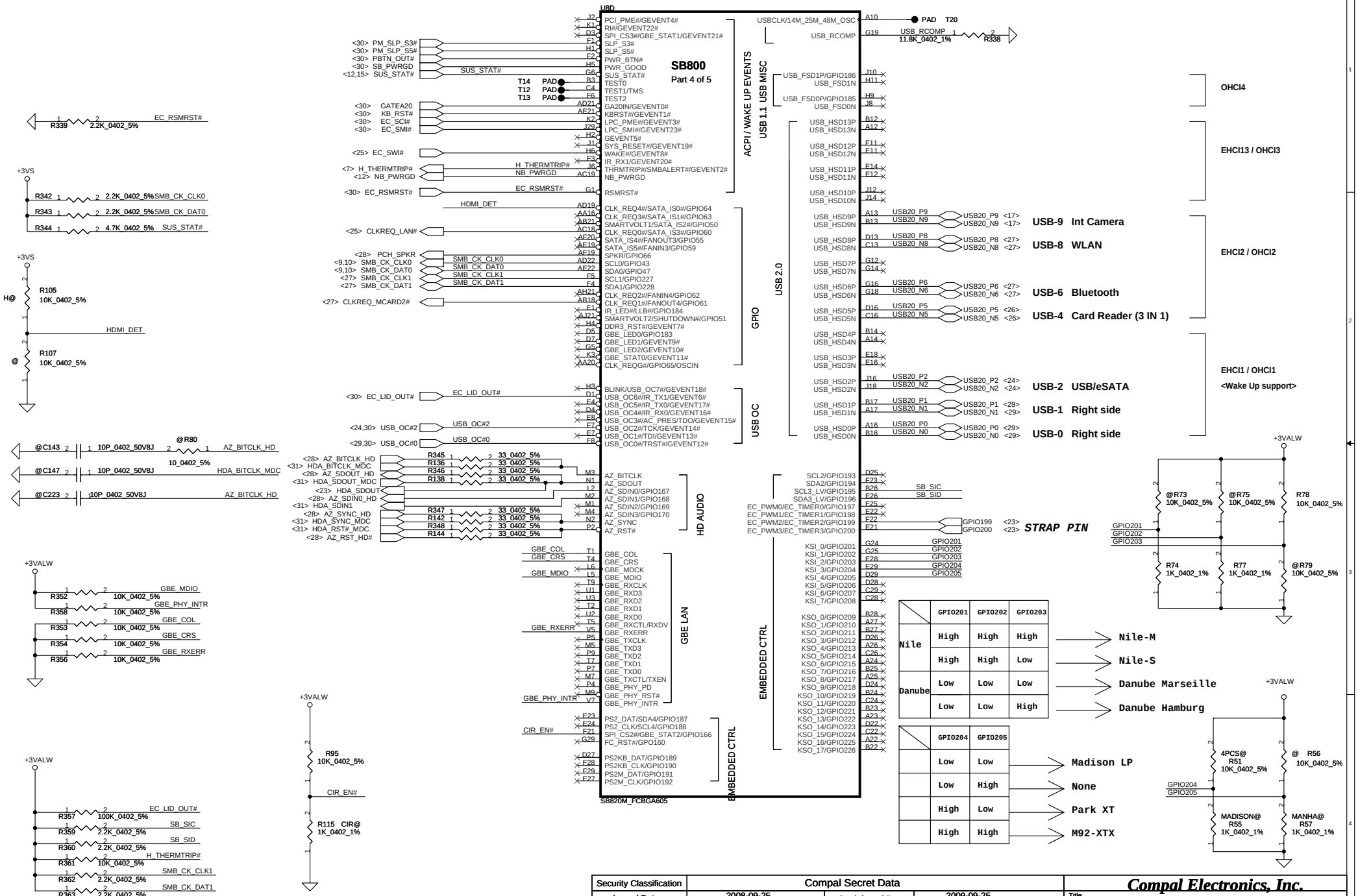

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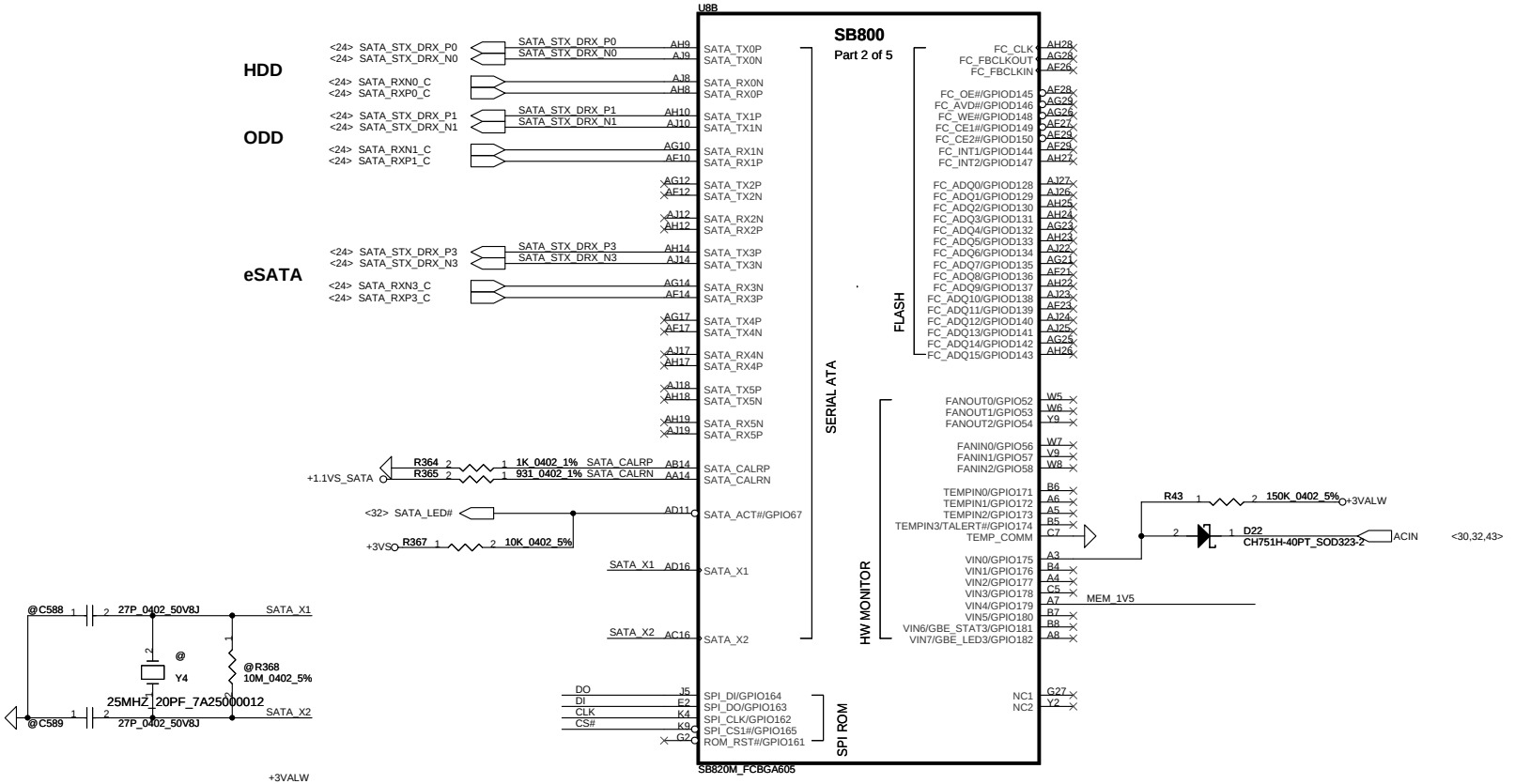

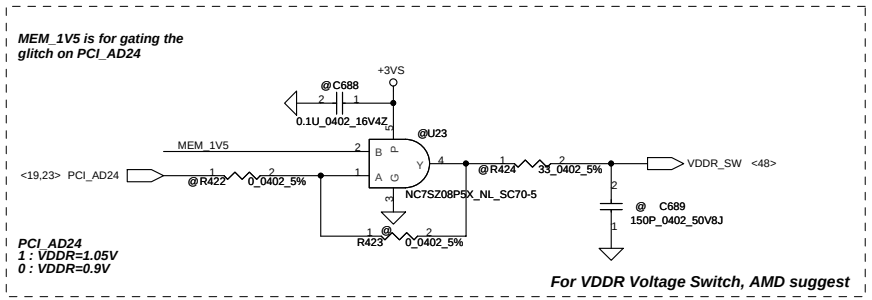

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Compal Electronics, Inc.			
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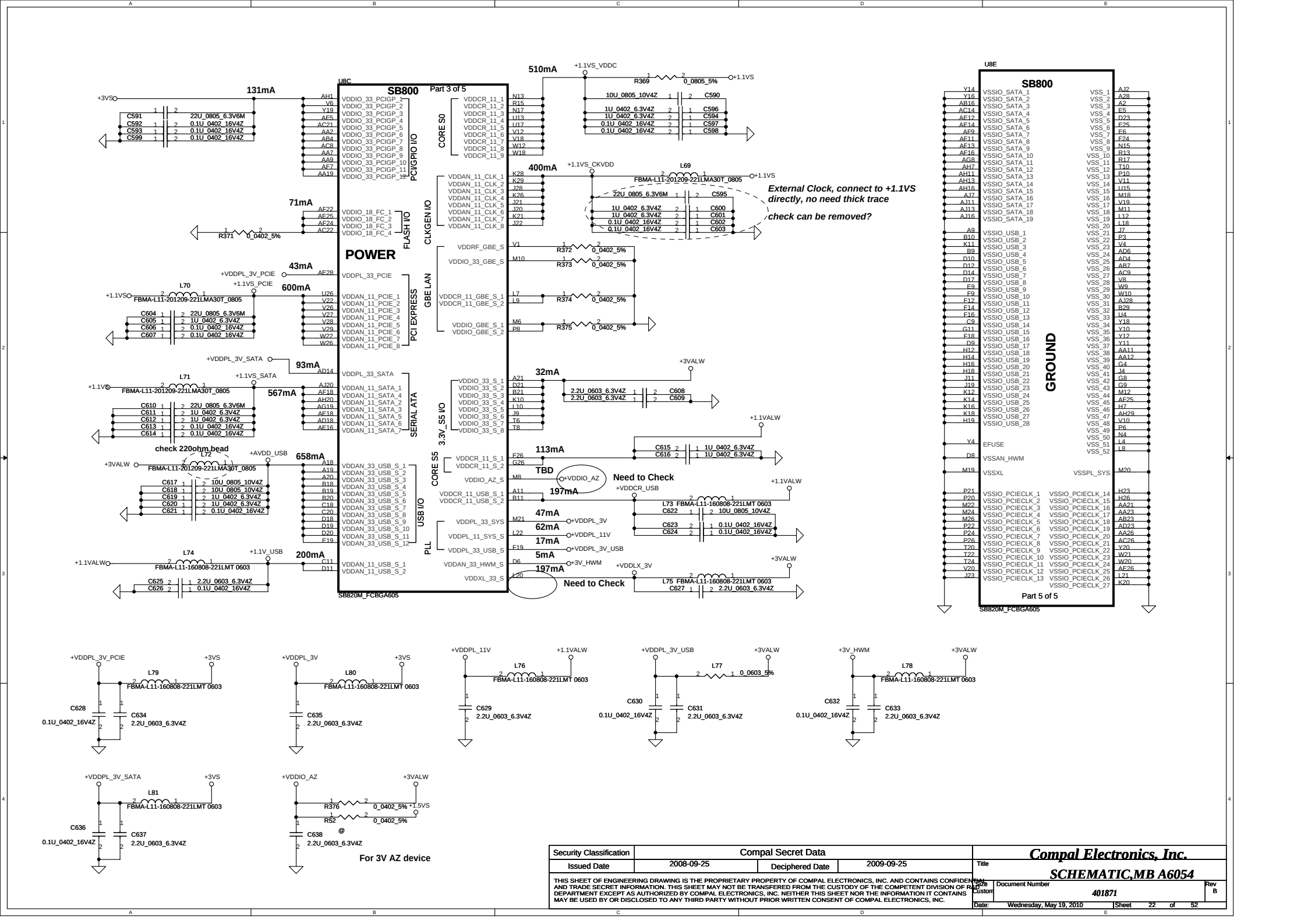

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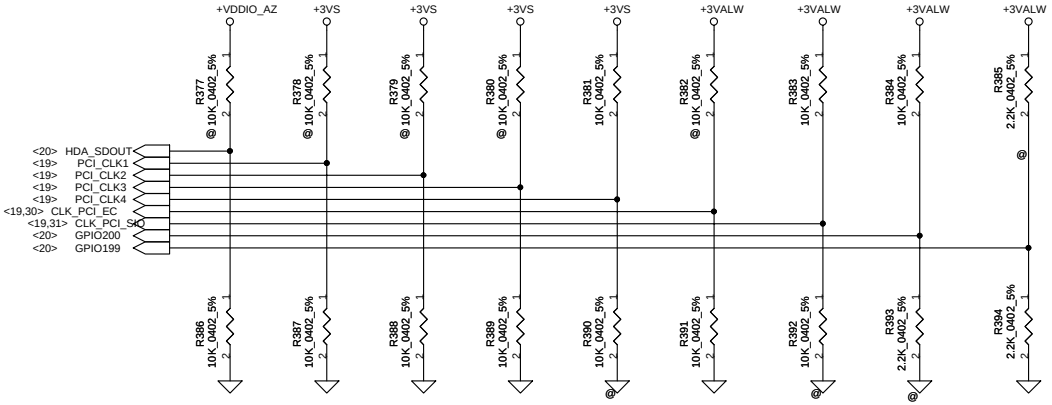
REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT		H,H = Reserved **H,L = SPI ROM (Default)** L,H = LPC ROM L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE		



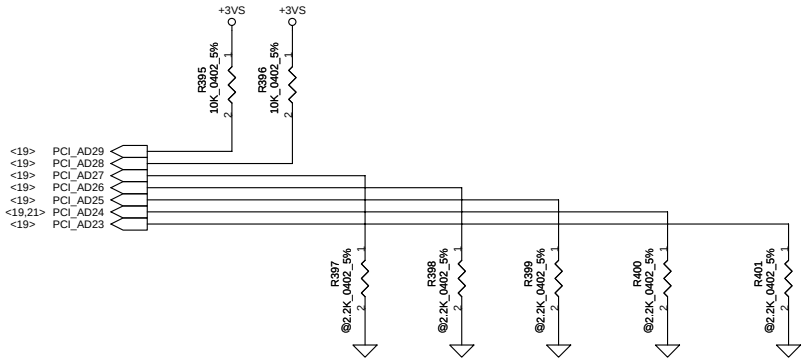
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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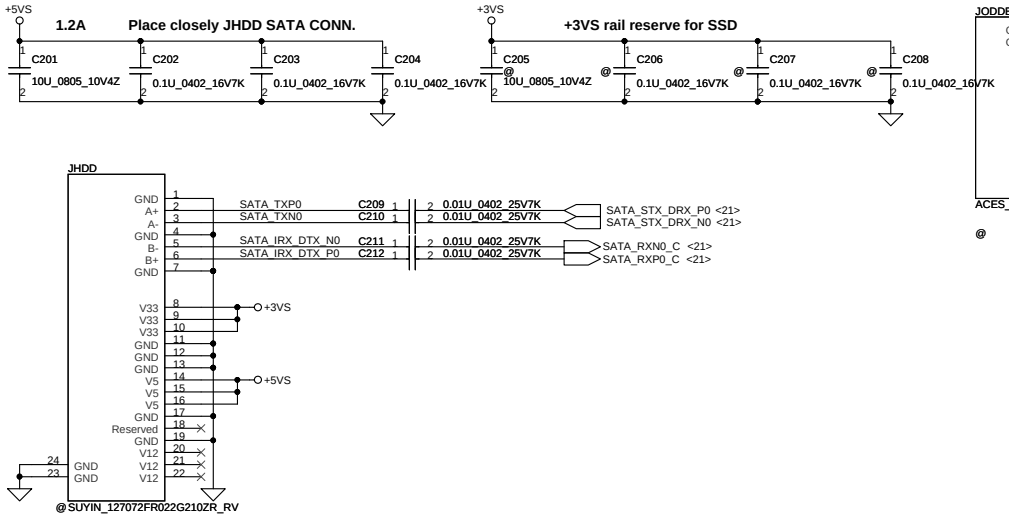
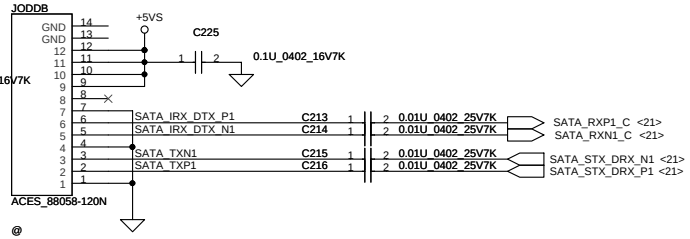
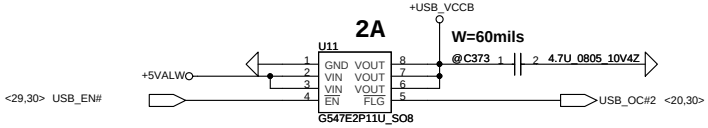
< SATA HDD Conn >

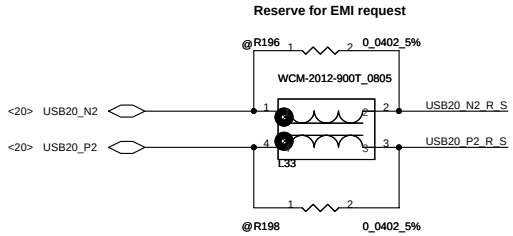


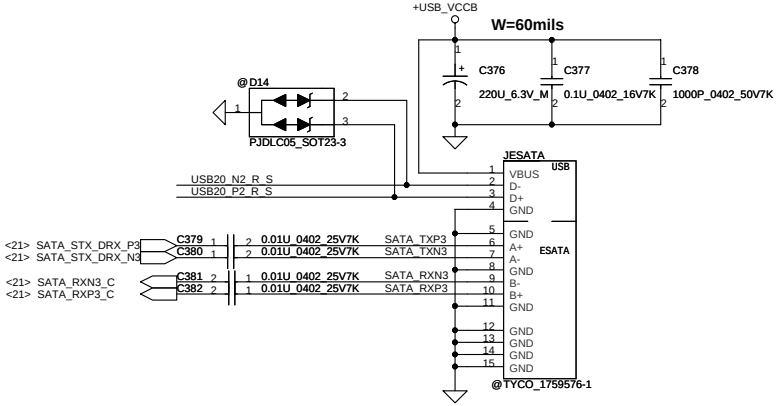
< SATA ODD Conn >



eSATA/USB Conn







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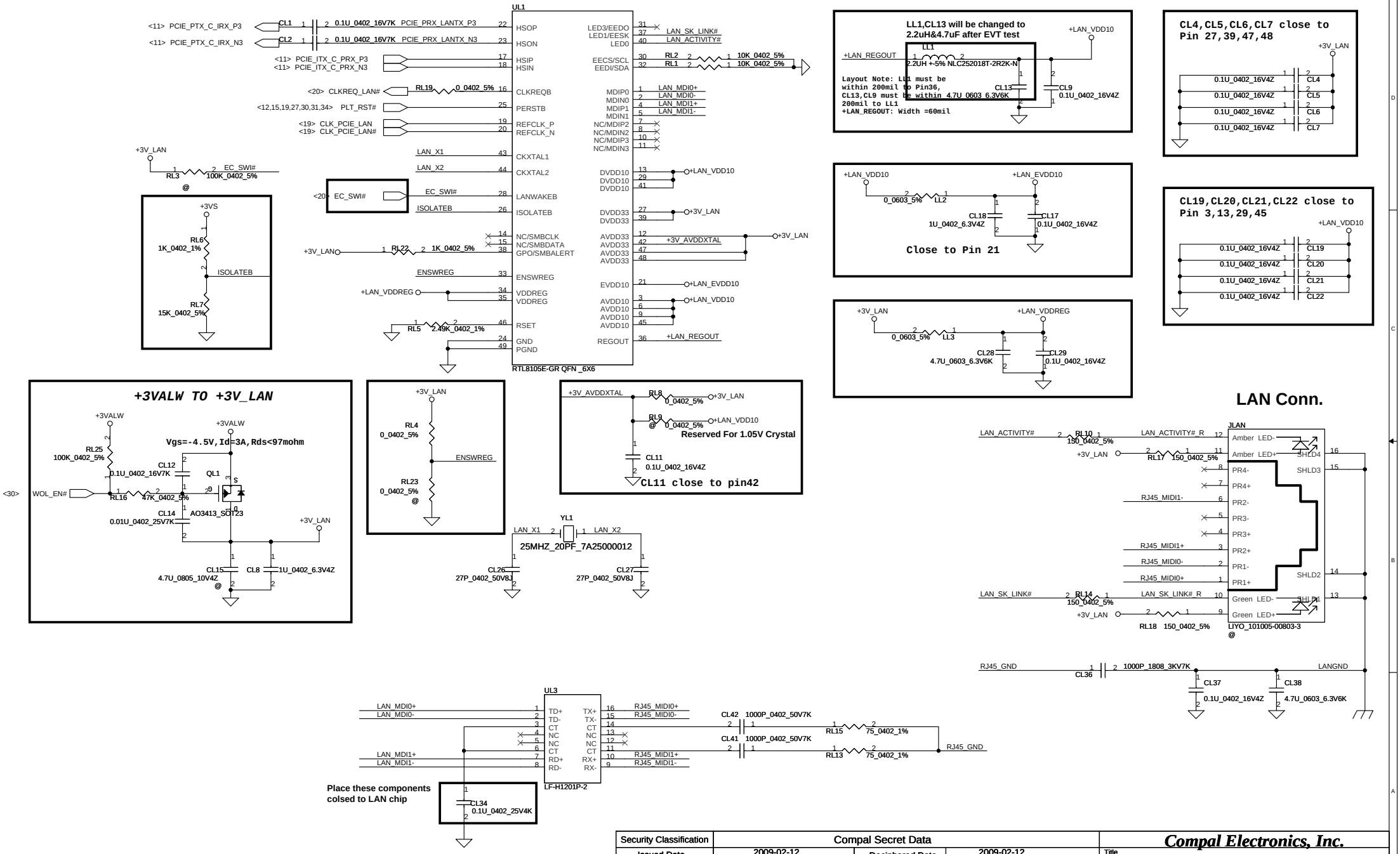
UL1
RTL8105E-GR QFN _6X6
LL1,CL13 will be changed to 2.2uH&4.7uF after EVT test
Layout Note: LL1 must be within 200mil to Pin36, CL13,CL9 must be within 200mil to LL1 +LAN_REGOUT: Width =60mil
CL4,CL5,CL6,CL7 close to Pin 27,39,47,48
CL19,CL20,CL21,CL22 close to Pin 3,13,29,45
Close to Pin 21
+3VALW TO +3V_LAN
Vgs=-4.5V,Id=3A,Rds<97mohm
Reserved For 1.05V Crystal
CL11 close to pin42
LAN Conn.
JLAN
LIYO_101005-00803-3
25MHZ_20PF_7A25000012
LF-H1201P-2
Place these components colsed to LAN chip
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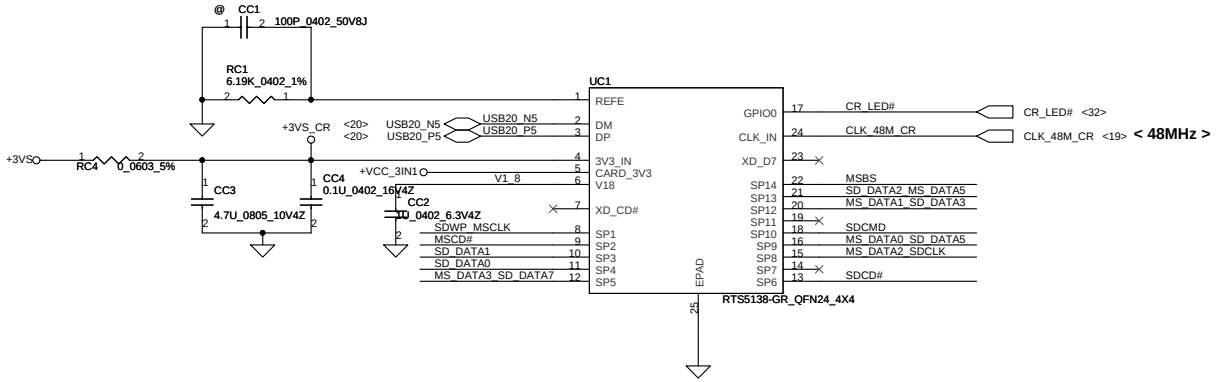
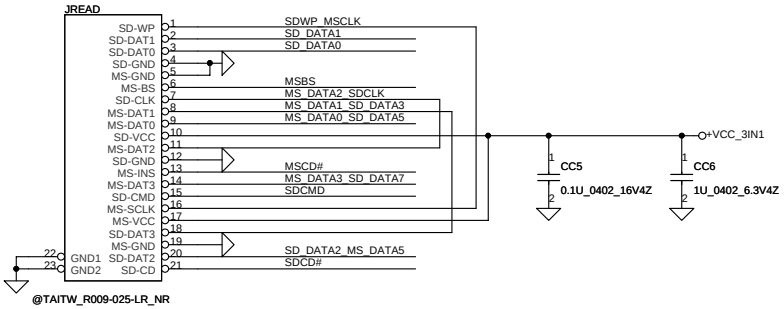
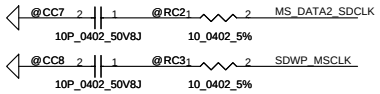


< 3 in 1 Card Reader >





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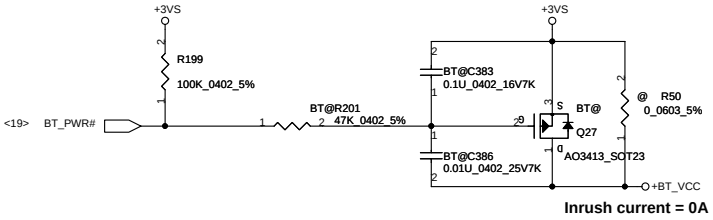
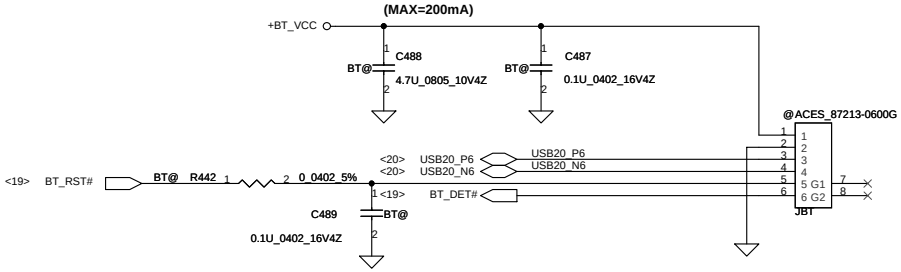
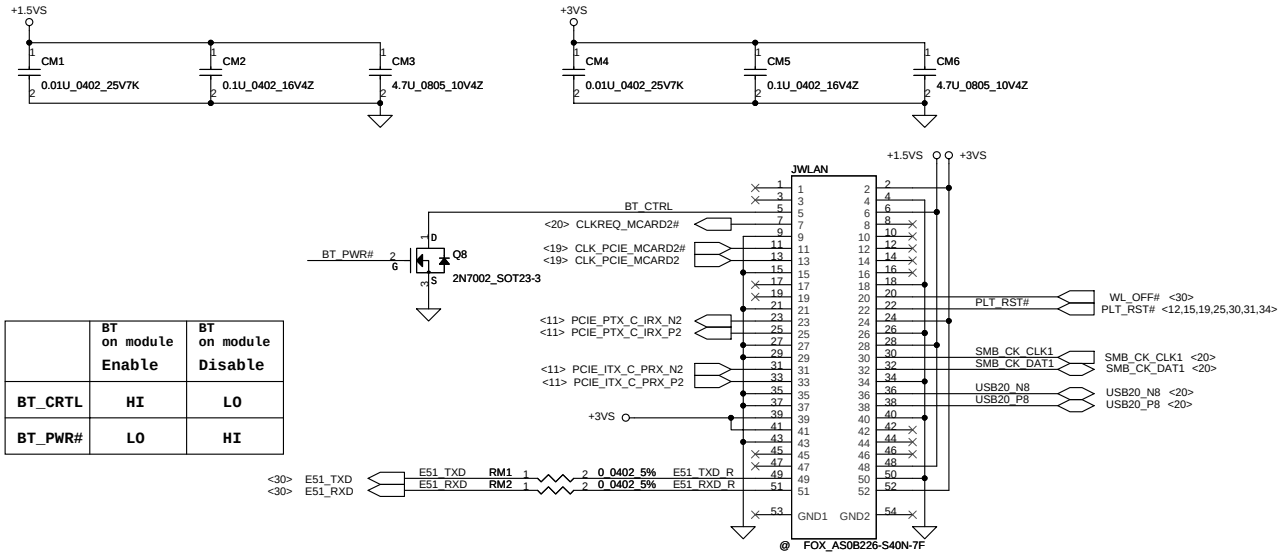
< BlueTooth Interface, USB port6 >



< Bluetooth Connector >



< PCIe Mini Card for WLAN >



	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

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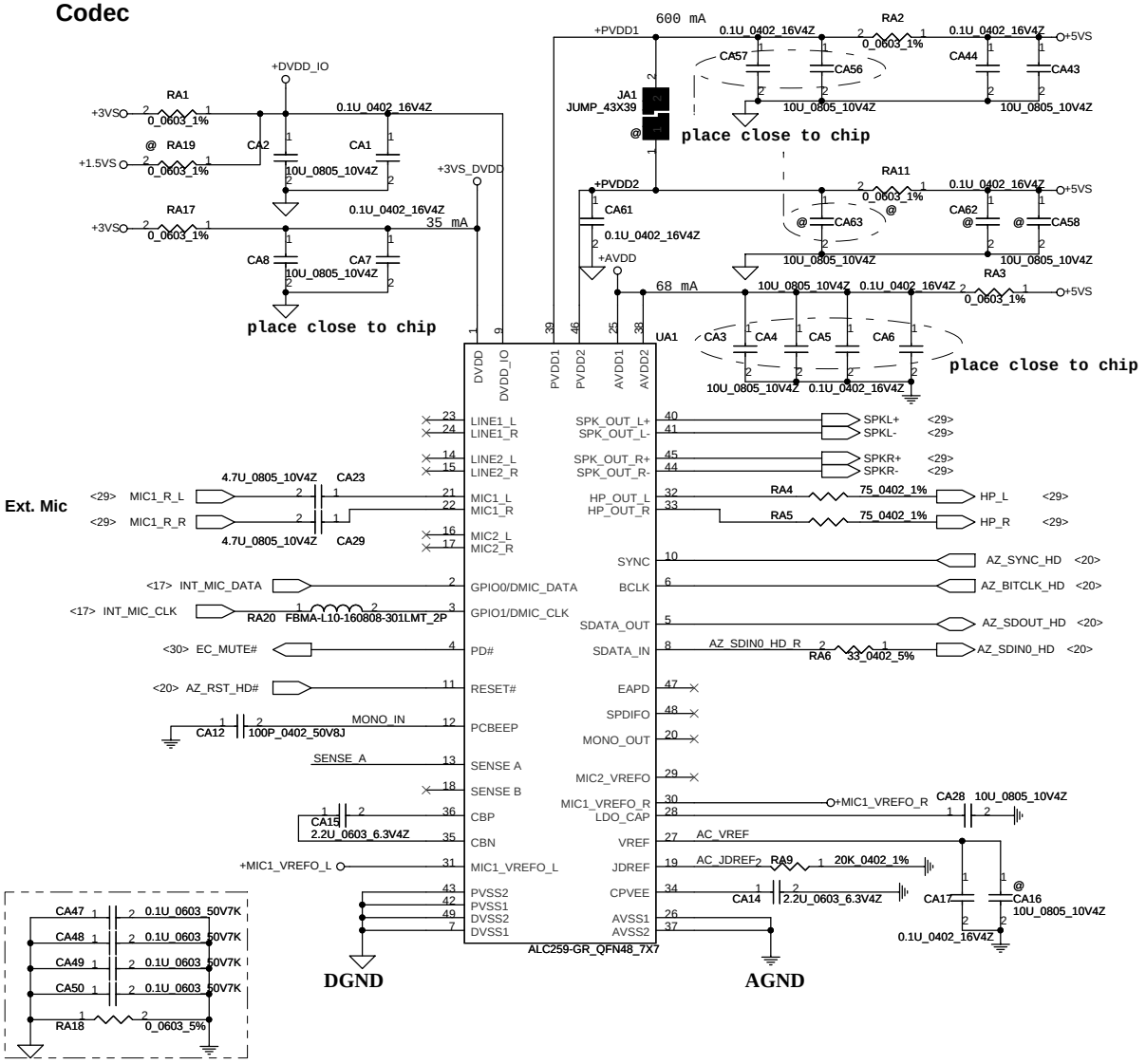
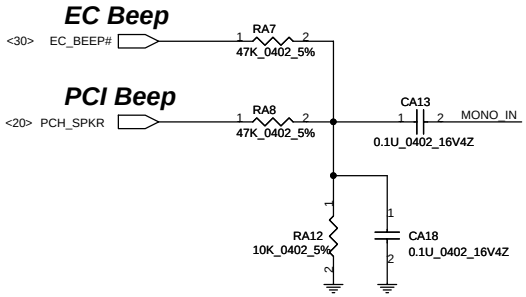
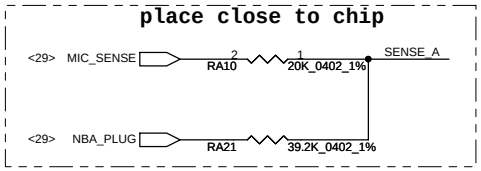
Codec



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



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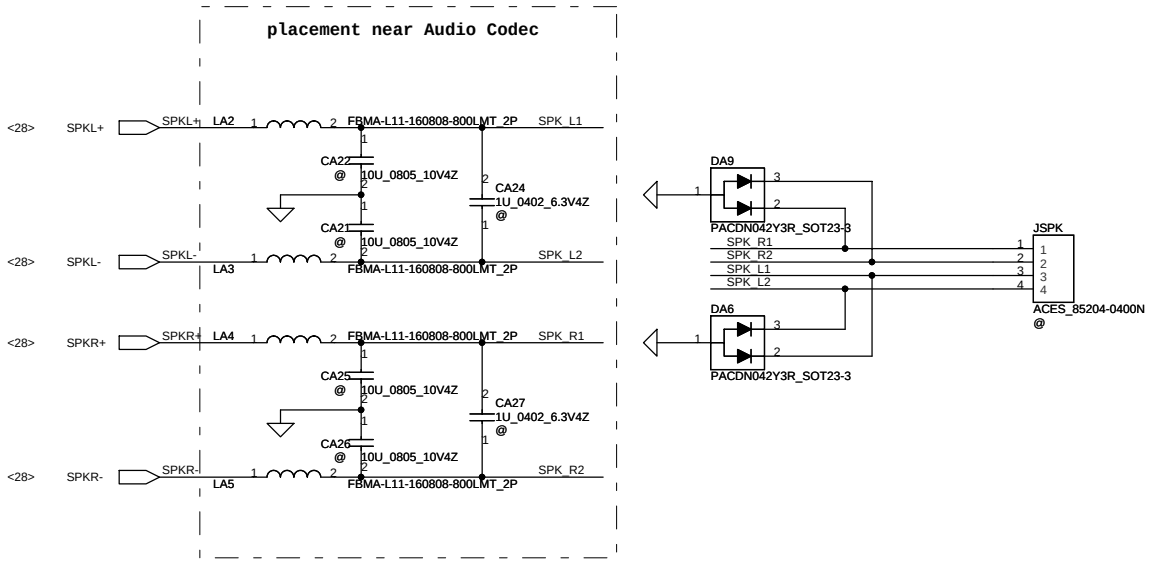
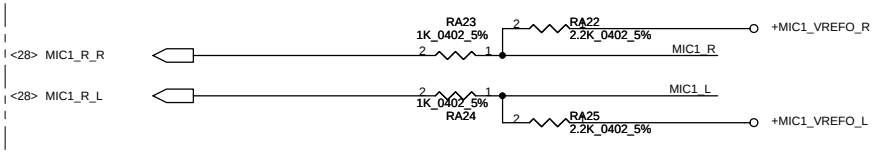
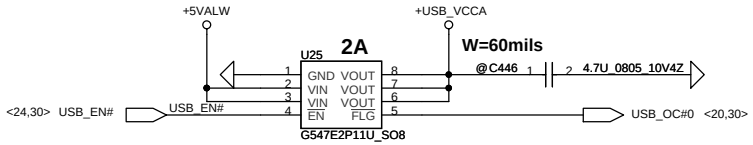
Speaker Connector

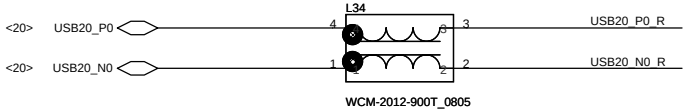


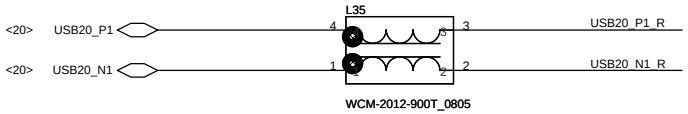
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK

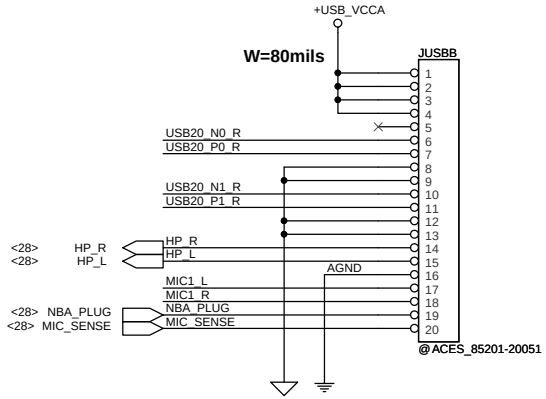








Audio & USB Sub-Board Conn.



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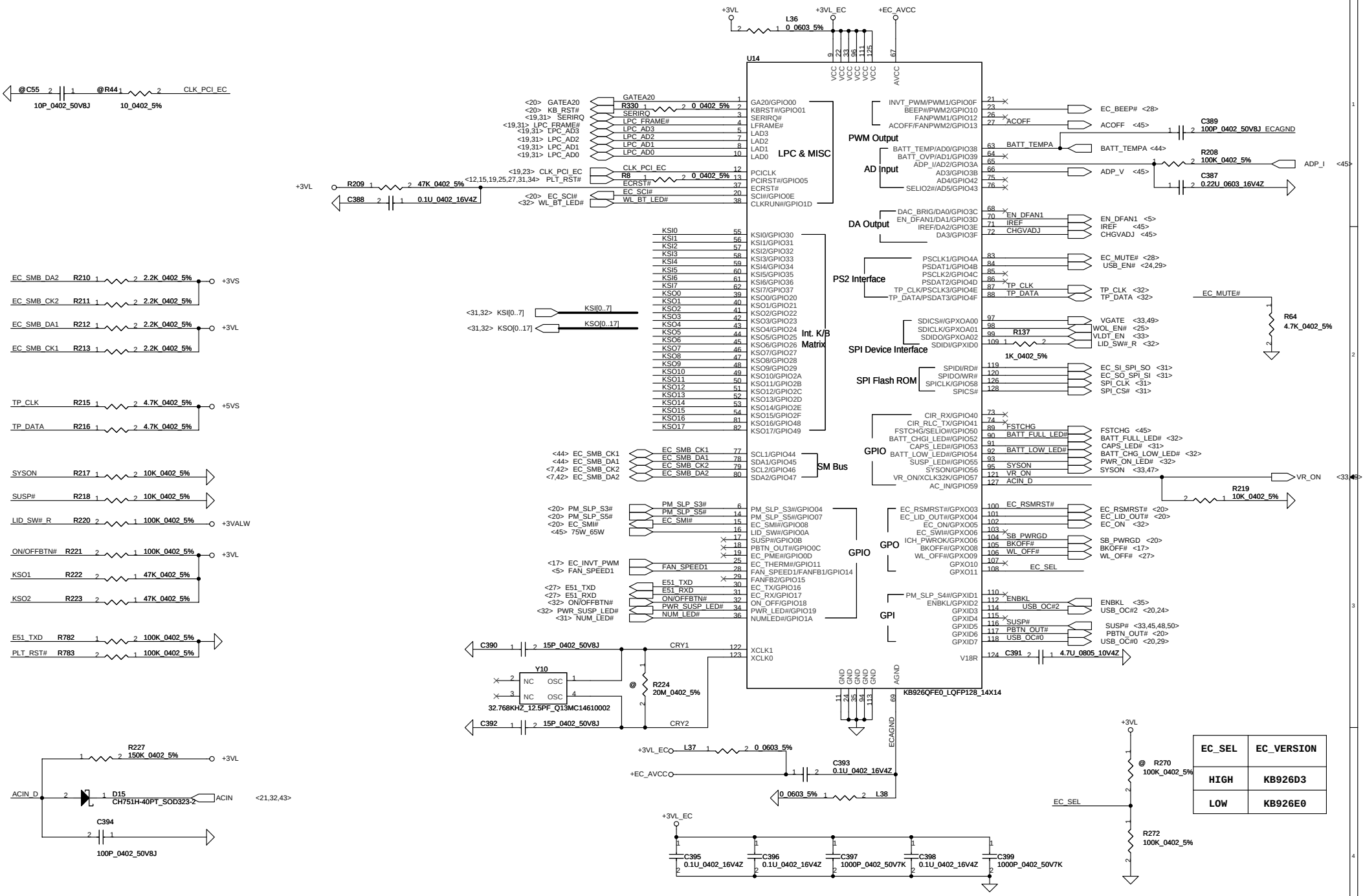

EC_SEL	EC_VERSION
HIGH	KB926D3
LOW	KB926E0

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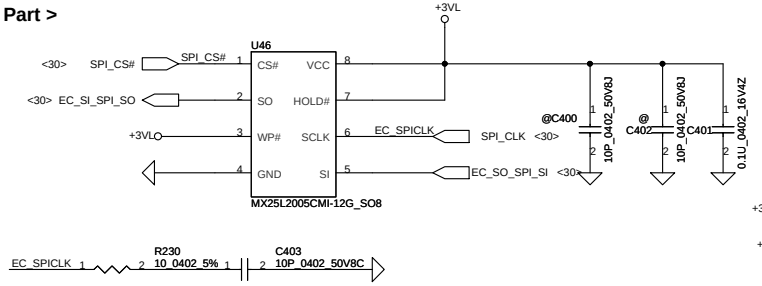
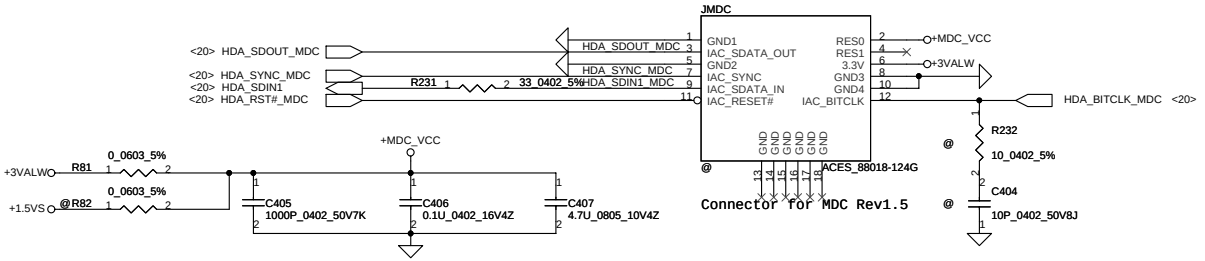
< ROM Part >

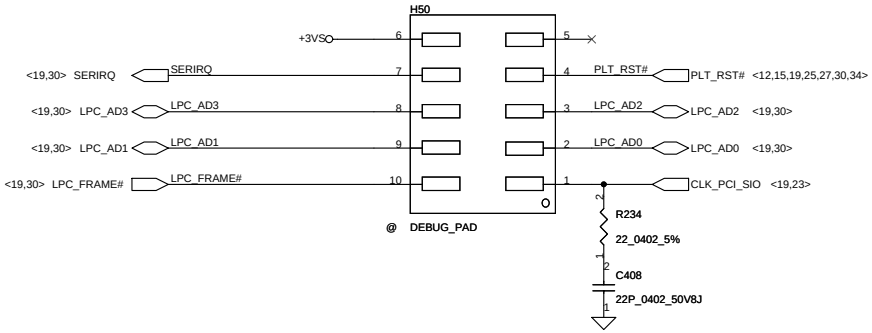


< MDC 1.5 Conn >



< LPC Debug Port >

Please place the PAD under DDR DIMM.



< KEYBOARD Conn >

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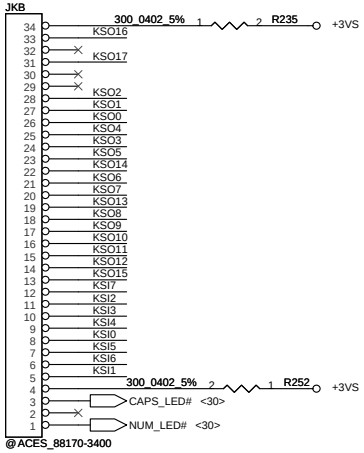
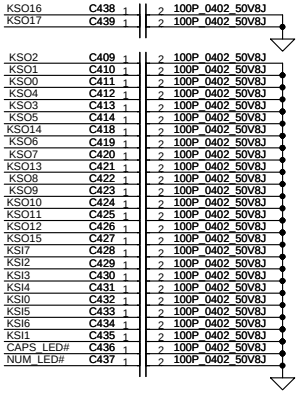
KSO[0..17] KSO[0..17] <30,32>



< For EMI >



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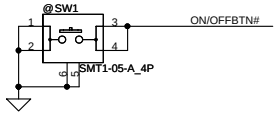
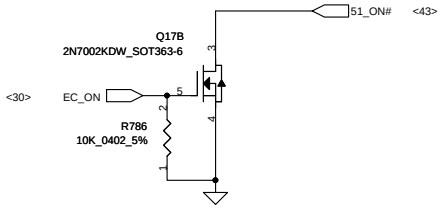
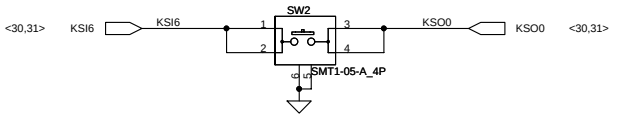
< Power Button for Debug >



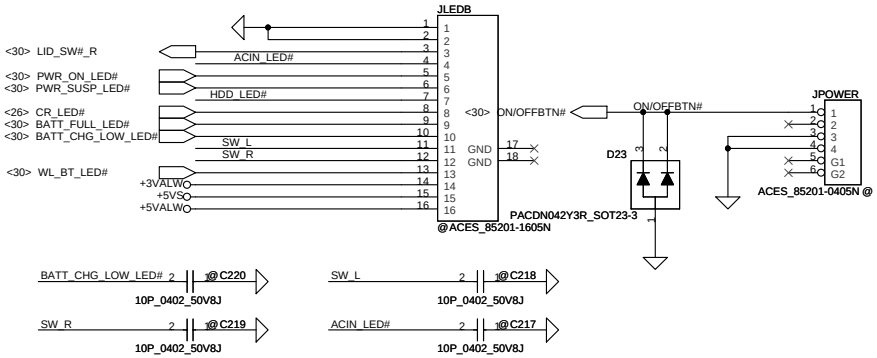
< Power Button Circuit >

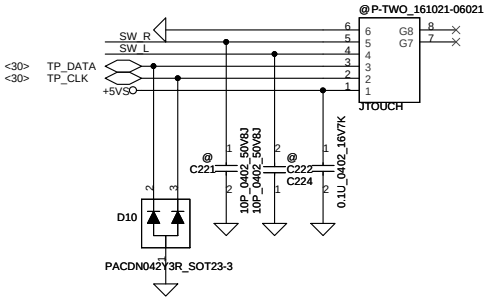


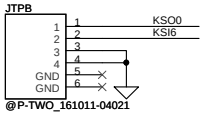
< TP on & off BTN on M/B>



Sub-B Connector

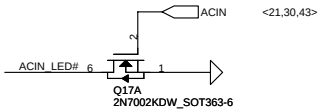




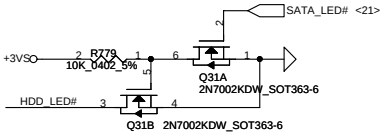


LED Circuit

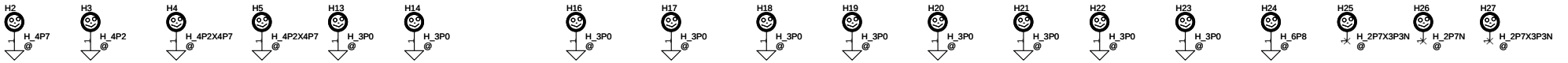
DC-IN LED

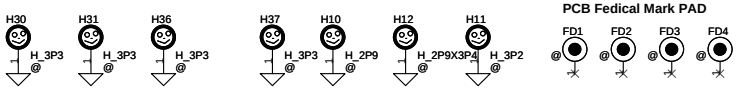


HDD LED



SCREW





PCB Fedical Mark PAD

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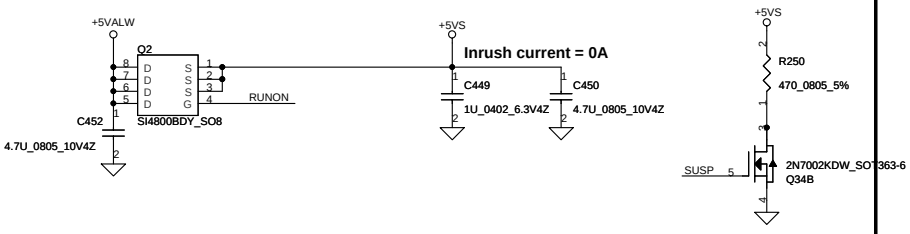
< +5VALW TO +5VS >



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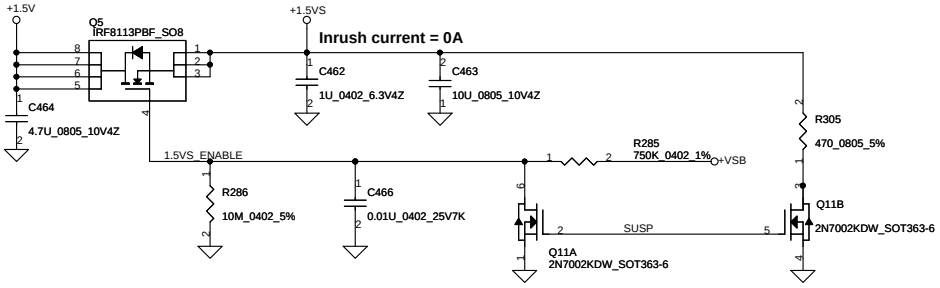

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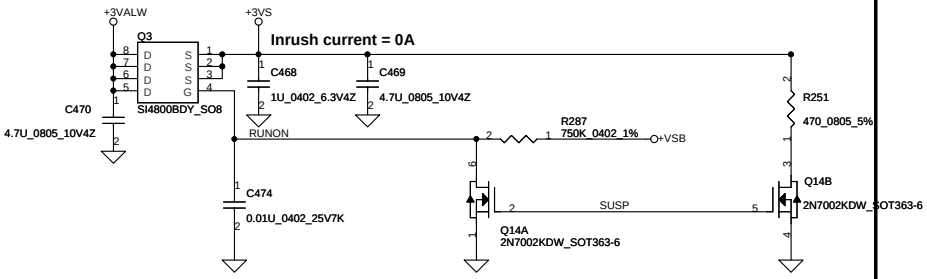

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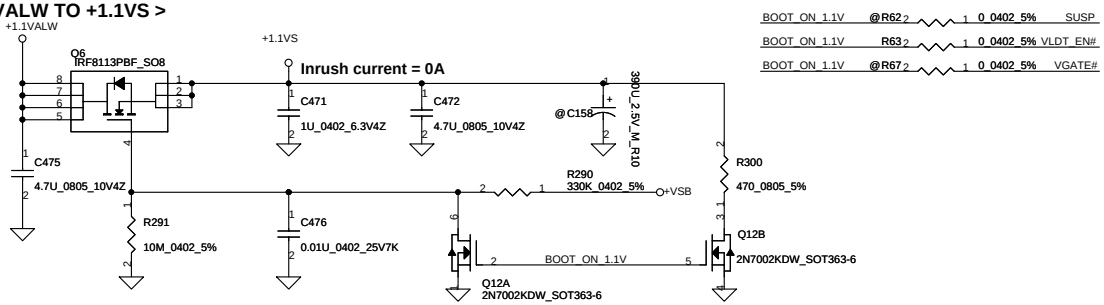
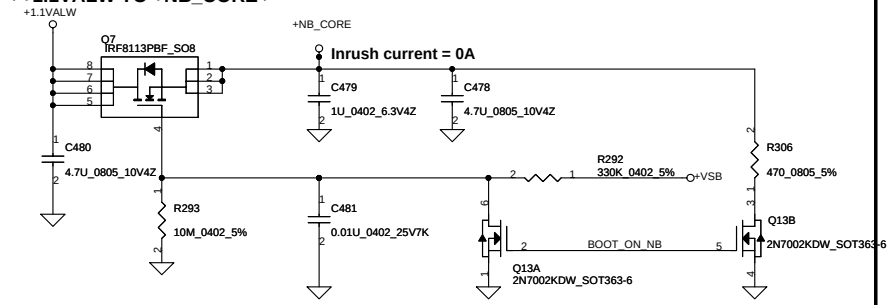
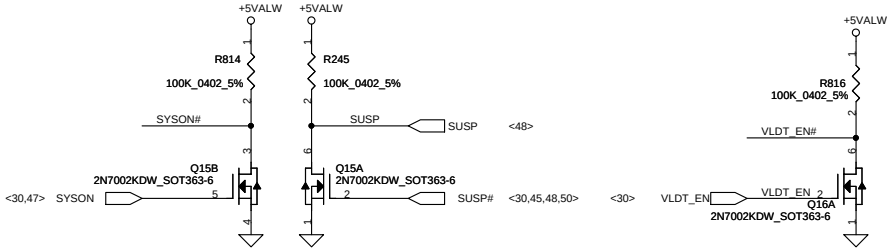
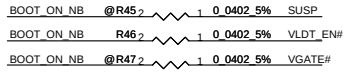


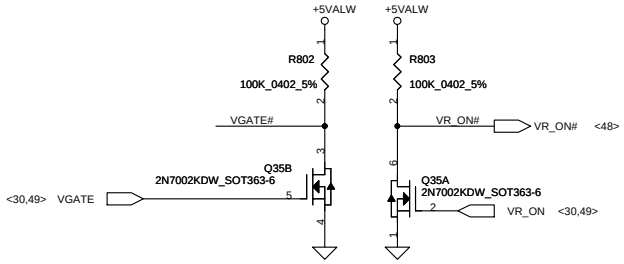
< +1.1VALW TO +NB_CORE >



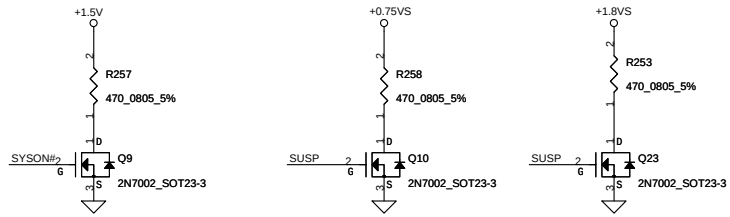
< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >







< Discharge circuit >



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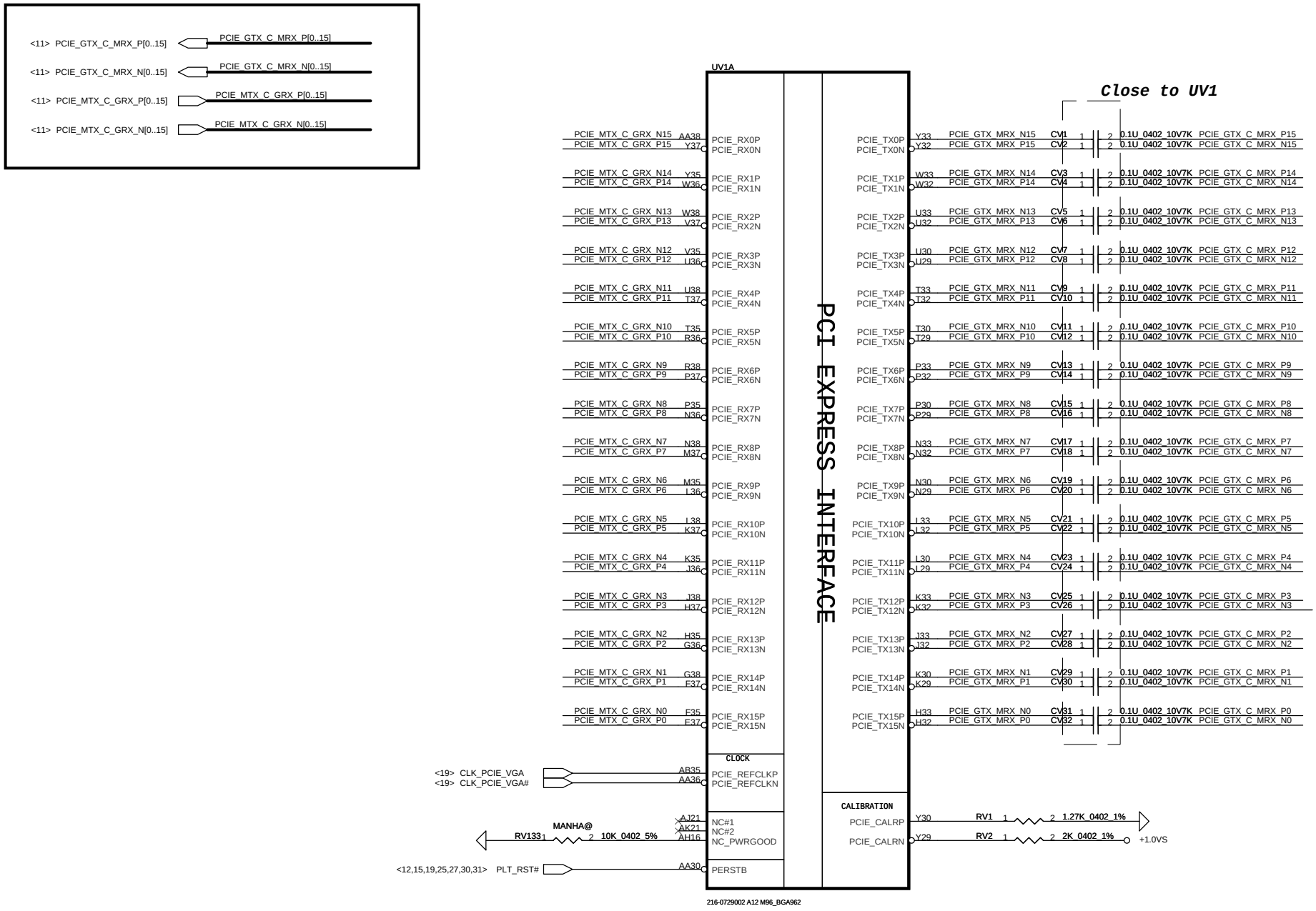

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Compal Electronics, Inc.			
Title: SCHEMATIC,MB A6054			
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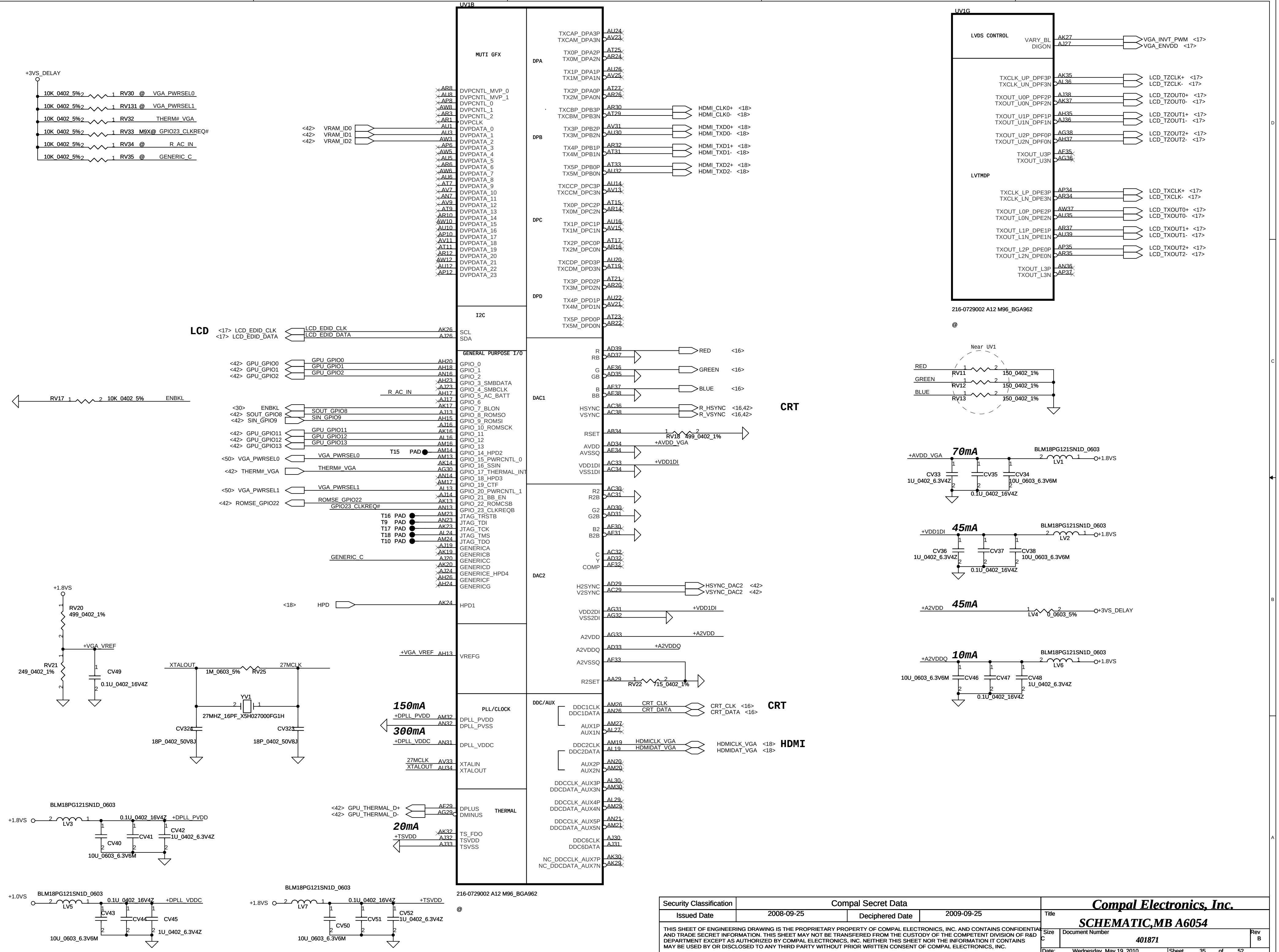

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Compal Electronics, Inc.

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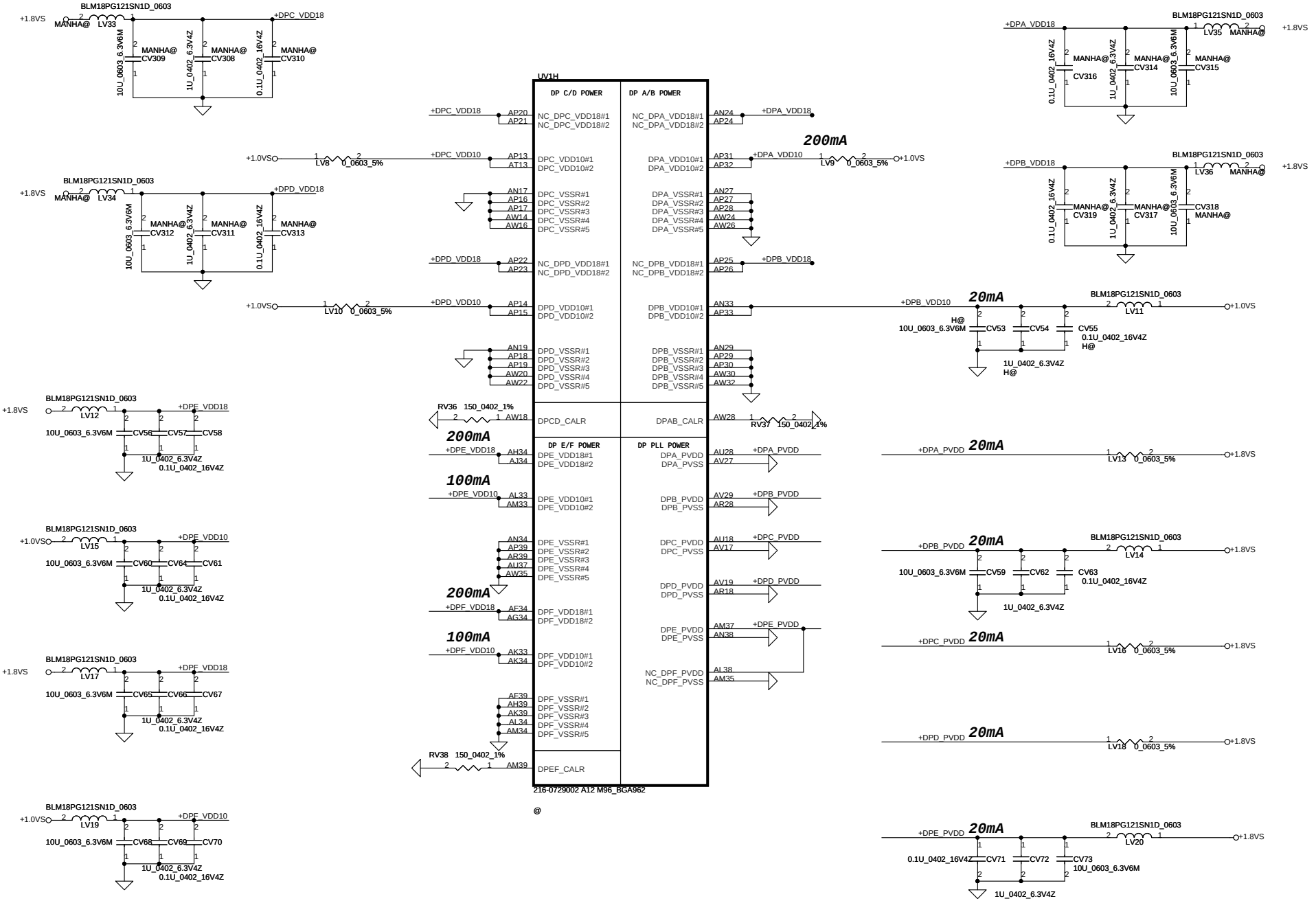

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

Title: **SCHEMATIC,MB A6054**

Size	Document Number	Rev
Custom	401871	B

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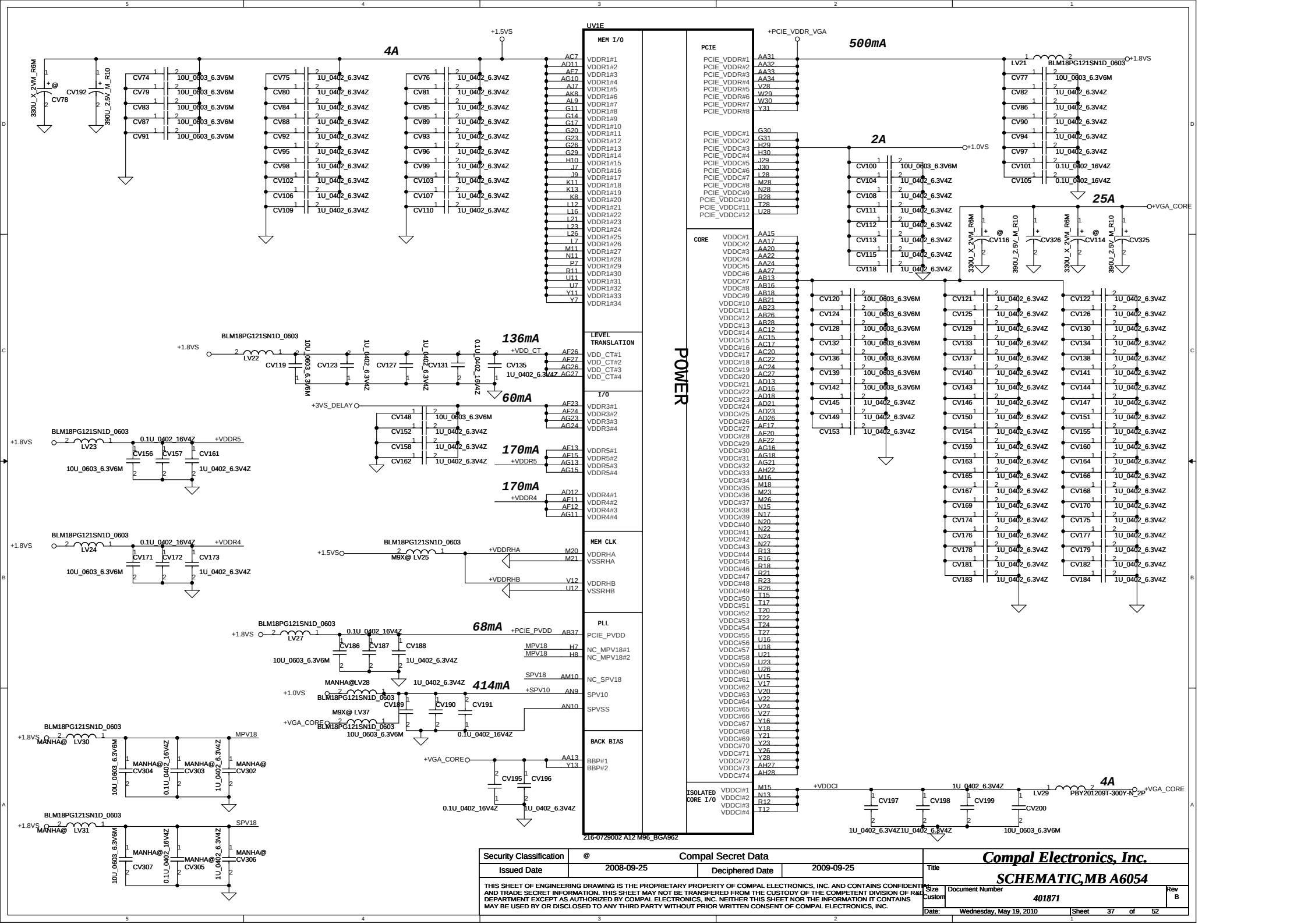

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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Title: **SCHEMATIC,MB A6054**

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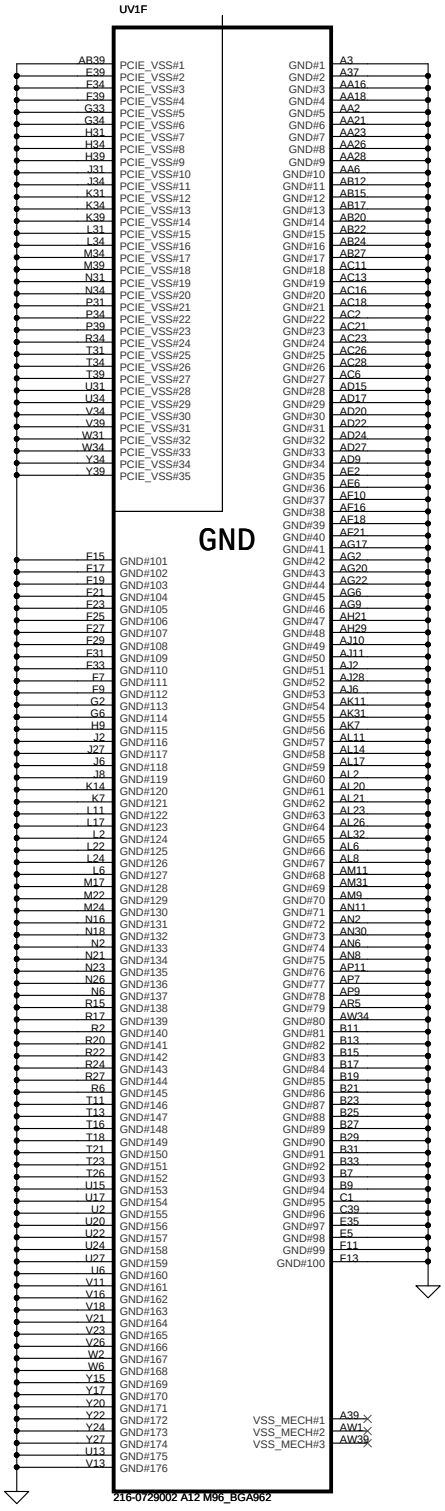

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

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MDA[0..63] → MDA[0..63] <40>

MDB[0..63] → MDB[0..63] <41>

Park uses memory group B only

UV1C

MEMORY INTERFACE A

MDA0	C37	DQA_0	MAA_0	G24	MAA0
MDA1	C35	DQA_1	MAA_1	J23	MAA1
MDA2	A35	DQA_2	MAA_2	H24	MAA2
MDA3	E34	DQA_3	MAA_3	J24	MAA3
MDA4	G32	DQA_4	MAA_4	H26	MAA4
MDA5	D33	DQA_5	MAA_5	J26	MAA5
MDA6	F32	DQA_6	MAA_6	H21	MAA6
MDA7	E32	DQA_7	MAA_7	G21	MAA7
MDA8	D31	DQA_8	MAA_8	H19	MAA8
MDA9	F30	DQA_9	MAA_9	H20	MAA9
MDA10	C30	DQA_10	MAA_10	L13	MAA10
MDA11	A30	DQA_11	MAA_11	G16	MAA11
MDA12	E28	DQA_12	MAA_12	J16	MAA12
MDA13	C28	DQA_13	MAA_13/BA2	H16	A_BA2
MDA14	A28	DQA_14	MAA_14/BA0	J17	A_BA0
MDA15	E28	DQA_15	MAA_15/BA1	H17	A_BA1
MDA16	D27	DQA_16			
MDA17	F26	DQA_17	DQMA_0	A32	DQMA#0
MDA18	C26	DQA_18	DQMA_1	C32	DQMA#1
MDA19	A26	DQA_19	DQMA_2	D23	DQMA#2
MDA20	E24	DQA_20	DQMA_3	E22	DQMA#3
MDA21	C24	DQA_21	DQMA_4	C14	DQMA#4
MDA22	A24	DQA_22	DQMA_5	A14	DQMA#5
MDA23	F24	DQA_23	DQMA_6	F10	DQMA#6
MDA24	C22	DQA_24	DQMA_7	D9	DQMA#7
MDA25	A22	DQA_25			
MDA26	F22	DQA_26	QSA_0/RDQSA_0	C34	QSA0
MDA27	D21	DQA_27	QSA_1/RDQSA_1	D29	QSA1
MDA28	A20	DQA_28	QSA_2/RDQSA_2	D25	QSA2
MDA29	F20	DQA_29	QSA_3/RDQSA_3	E20	QSA3
MDA30	D19	DQA_30	QSA_4/RDQSA_4	F16	QSA4
MDA31	E18	DQA_31	QSA_5/RDQSA_5	E12	QSA5
MDA32	C18	DQA_32	QSA_6/RDQSA_6	J10	QSA6
MDA33	A18	DQA_33	QSA_7/RDQSA_7	D7	QSA7
MDA34	F18	DQA_34			
MDA35	D17	DQA_35	QSA_0B/WDQSA_0	A34	QSA#0
MDA36	A16	DQA_36	QSA_1B/WDQSA_1	E30	QSA#1
MDA37	F16	DQA_37	QSA_2B/WDQSA_2	E26	QSA#2
MDA38	D15	DQA_38	QSA_3B/WDQSA_3	C20	QSA#3
MDA39	E14	DQA_39	QSA_4B/WDQSA_4	C16	QSA#4
MDA40	F14	DQA_40	QSA_5B/WDQSA_5	C12	QSA#5
MDA41	D13	DQA_41	QSA_6B/WDQSA_6	J11	QSA#6
MDA42	F12	DQA_42	QSA_7B/WDQSA_7	F8	QSA#7
MDA43	A12	DQA_43			
MDA44	D11	DQA_44	ODTA0	J21	ODTA0
MDA45	F10	DQA_45	ODTA1	G19	ODTA1
MDA46	A10	DQA_46			
MDA47	C10	DQA_47	CLKA0	H27	CLKA0
MDA48	G13	DQA_48	CLKA0B	G27	CLKA0#
MDA49	H13	DQA_49			
MDA50	J13	DQA_50	CLKA1	J14	CLKA1
MDA51	H11	DQA_51	CLKA1B	H14	CLKA1#
MDA52	G10	DQA_52			
MDA53	G8	DQA_53	RASA0B	K23	RASA0#
MDA54	K9	DQA_54	RASA1B	K19	RASA1#
MDA55	K10	DQA_55			
MDA56	G9	DQA_56	CASA0B	K20	CASA0#
MDA57	A8	DQA_57	CASA1B	K17	CASA1#
MDA58	C8	DQA_58			
MDA59	E8	DQA_59	CSA0B_0	K24	CSA0#_0
MDA60	A6	DQA_60	CSA0B_1	K27	
MDA61	C6	DQA_61			
MDA62	E6	DQA_62	CSA1B_0	M13	CSA1#_0
MDA63	A5	DQA_63	CSA1B_1	K16	
+MVREFDA	L18	MVREFDA	CKEA0	K21	CKEA0
+MVREFSA	L20	MVREFSA	CKEA1	J20	CKEA1
MANHA@ RV48	2 243_0402_1%	L27	WEA0B	K26	WEA0#
MANHA@ RV49	2 243_0402_1%	N12	WEA1B	L15	WEA1#
MANHA@ RV50	2 243_0402_1%	AG12			
RV51	2 243_0402_1%	M12	RSVD#1	AE28	
MANHA@ RV53	2 243_0402_1%	M27	RSVD#2	AG28	
MANHA@ RV55	2 243_0402_1%	AH12	RSVD#3	AL31	
NC_MEM_CALRN0			RSVD#5	H23	MAA13
NC_MEM_CALRN1			RSVD#6	J19	
NC_MEM_CALRN2					
			RSVD#9	T8	MAB13
MEM_CALRP1			RSVD#11	W8	
NC_MEM_CALRP0					
NC_MEM_CALRP2					

MAA[13..0] → MAA[13..0] <40>

A_BA[2..0] → A_BA[2..0] <40>

DQMA#[7..0] → DQMA#[7..0] <40>

QSA[7..0] → QSA[7..0] <40>

QSA#[7..0] → QSA#[7..0] <40>

ODTA0 → ODTA0 <40>

ODTA1 → ODTA1 <40>

CLKA0 → CLKA0 <40>

CLKA0# → CLKA0# <40>

CLKA1 → CLKA1 <40>

CLKA1# → CLKA1# <40>

RASA0# → RASA0# <40>

RASA1# → RASA1# <40>

CASA0# → CASA0# <40>

CASA1# → CASA1# <40>

CSA0#_0 → CSA0#_0 <40>

CSA1#_0 → CSA1#_0 <40>

CKEA0 → CKEA0 <40>

CKEA1 → CKEA1 <40>

WEA0# → WEA0# <40>

WEA1# → WEA1# <40>

216-0729002 A12 M96_BGA962

@

UV1D

MEMORY INTERFACE B

MDB0	C5	DQB_0	MAB_0	P8	MAB0
MDB1	C3	DQB_1	MAB_1	T9	MAB1
MDB2	E3	DQB_2	MAB_2	P9	MAB2
MDB3	E1	DQB_3	MAB_3	N7	MAB3
MDB4	F1	DQB_4	MAB_4	N8	MAB4
MDB5	F3	DQB_5	MAB_5	N9	MAB5
MDB6	F5	DQB_6	MAB_6	U9	MAB6
MDB7	G4	DQB_7	MAB_7	U8	MAB7
MDB8	H5	DQB_8	MAB_8	Y9	MAB8
MDB9	H6	DQB_9	MAB_9	W9	MAB9
MDB10	J4	DQB_10	MAB_10	AC8	MAB10
MDB11	K6	DQB_11	MAB_11	AC9	MAB11
MDB12	K5	DQB_12	MAB_12	AA7	MAB12
MDB13	L4	DQB_13	MAB_13/BA2	AA8	B_BA2
MDB14	M6	DQB_14	MAB_14/BA0	Y8	B_BA0
MDB15	M1	DQB_15	MAB_15/BA1	AA9	B_BA1
MDB16	M3	DQB_16			
MDB17	M5	DQB_17	DQMB_0	H3	DQMB#0
MDB18	N4	DQB_18	DQMB_1	H1	DQMB#1
MDB19	P6	DQB_19	DQMB_2	T3	DQMB#2
MDB20	P5	DQB_20	DQMB_3	T5	DQMB#3
MDB21	R4	DQB_21	DQMB_4	AE4	DQMB#4
MDB22	T6	DQB_22	DQMB_5	AF5	DQMB#5
MDB23	T1	DQB_23	DQMB_6	AK6	DQMB#6
MDB24	U4	DQB_24	DQMB_7	AK5	DQMB#7
MDB25	V6	DQB_25			
MDB26	V1	DQB_26	QSB_0/RDQSB_0	F6	QSB0
MDB27	V3	DQB_27	QSB_1/RDQSB_1	K3	QSB1
MDB28	Y6	DQB_28	QSB_2/RDQSB_2	P3	QSB2
MDB29	Y1	DQB_29	QSB_3/RDQSB_3	V5	QSB3
MDB30	Y3	DQB_30	QSB_4/RDQSB_4	AB5	QSB4
MDB31	Y5	DQB_31	QSB_5/RDQSB_5	AH1	QSB5
MDB32	AA4	DQB_32	QSB_6/RDQSB_6	AJ9	QSB6
MDB33	AB6	DQB_33	QSB_7/RDQSB_7	AM5	QSB7
MDB34	AB1	DQB_34			
MDB35	AB3	DQB_35	QSB_0B/WDQSB_0	G7	QSB#0
MDB36	AD6	DQB_36	QSB_1B/WDQSB_1	K1	QSB#1
MDB37	AD1	DQB_37	QSB_2B/WDQSB_2	P1	QSB#2
MDB38	AD3	DQB_38	QSB_3B/WDQSB_3	W4	QSB#3
MDB39	AD5	DQB_39	QSB_4B/WDQSB_4	AC4	QSB#4
MDB40	AF1	DQB_40	QSB_5B/WDQSB_5	AH3	QSB#5
MDB41	AF3	DQB_41	QSB_6B/WDQSB_6	AJ8	QSB#6
MDB42	AF6	DQB_42	QSB_7B/WDQSB_7	AM3	QSB#7
MDB43	AG4	DQB_43			
MDB44	AH5	DQB_44	ODTB0	T7	ODTB0
MDB45	AH6	DQB_45	ODTB1	W7	ODTB1
MDB46	AJ4	DQB_46			
MDB47	AK3	DQB_47	CLKB0	L9	CLKB0
MDB48	AF8	DQB_48	CLKB0B	L8	CLKB0#
MDB49	AF9	DQB_49			
MDB50	AG8	DQB_50	CLKB1	AD8	CLKB1
MDB51	AG7	DQB_51	CLKB1B	AD7	CLKB1#
MDB52	AK9	DQB_52			
MDB53	AL7	DQB_53	RASB0B	T10	RASB0#
MDB54	AM8	DQB_54	RASB1B	Y10	RASB1#
MDB55	AM7	DQB_55			
MDB56	AK1	DQB_56	CASB0B	W10	CASB0#
MDB57	AL4	DQB_57	CASB1B	AA10	CASB1#
MDB58	AM5	DQB_58			
MDB59	AM1	DQB_59	CSB0B_0	P10	CSB0#_0
MDB60	AN4	DQB_60	CSB0B_1	L10	
MDB61	AP3	DQB_61			
MDB62	AP1	DQB_62	CSB1B_0	AD10	CSB1#_0
MDB63	AP5	DQB_63	CSB1B_1	AC10	
+MVREFDB	Y12	MVREFDB	CKEB0	U10	CKEB0
+MVREFSB	AA12	MVREFSB	CKEB1	AA11	CKEB1
			WEB0B	N10	WEB0#
			WEB1B	AB11	WEB1#
TESTEN	AD28	TESTEN			
CLKTESTA	AK10	CLKTESTA			
CLKTESTB	AL10	CLKTESTB			
			DRAM_RST	AH11	

MAB[13..0] → MAB[13..0] <41>

B_BA[2..0] → B_BA[2..0] <41>

DQMB#[7..0] → DQMB#[7..0] <41>

QSB[7..0] → QSB[7..0] <41>

QSB#[7..0] → QSB#[7..0] <41>

ODTB0 → ODTB0 <41>

ODTB1 → ODTB1 <41>

CLKB0 → CLKB0 <41>

CLKB0# → CLKB0# <41>

CLKB1 → CLKB1 <41>

CLKB1# → CLKB1# <41>

RASB0# → RASB0# <41>

RASB1# → RASB1# <41>

CASB0# → CASB0# <41>

CASB1# → CASB1# <41>

CSB0#_0 → CSB0#_0 <41>

CSB1#_0 → CSB1#_0 <41>

CKEB0 → CKEB0 <41>

CKEB1 → CKEB1 <41>

WEB0# → WEB0# <41>

WEB1# → WEB1# <41>

DRAM_RST# <40,41>

216-0729002 A12 M96_BGA962

@

Close to pin L18

+1.5VS

MANHA@ RV41 40.2_0402_1% — RV41 100_0402_1% M9X@ — +MVREFDA

RV43 100_0402_1% — CV202 0.1U_0402_16V4Z

Close to pin L20

+1.5VS

MANHA@ RV45 40.2_0402_1% — RV45 100_0402_1% M9X@ — +MVREFSA

RV47 100_0402_1% — CV204 0.1U_0402_16V4Z

Close to pin Y12

+1.5VS

MANHA@ RV42 40.2_0402_1% — RV42 100_0402_1% M9X@ — +MVREFDB

RV44 100_0402_1% — CV203 0.1U_0402_16V4Z

Close to pin AA12

+1.5VS

MANHA@ RV46 40.2_0402_1% — RV46 100_0402_1% M9X@ — +MVREFSB

RV52 100_0402_1% — CV205 0.1U_0402_16V4Z

+3VS_DELAY

@ RV56 10K_0402_5% — TESTEN — M9X@ RV125 4.7K_0402_5% TESTA — M9X@ RV129 4.7K_0402_5% TESTB

RV23 10K_0402_5%

M9X@ RV54 4.7K_0402_5% — +1.5VS

M9X@ RV132 0_0402_5% — MANHA@ RV132 51_0402_5% — DRAM_RST# <40,41>

68P_0402_50V8J — MANHA@ CV206 — M9X@ CV206 0.01U_0402_25V7K

MANHA@ RV59 10K_0402_5%

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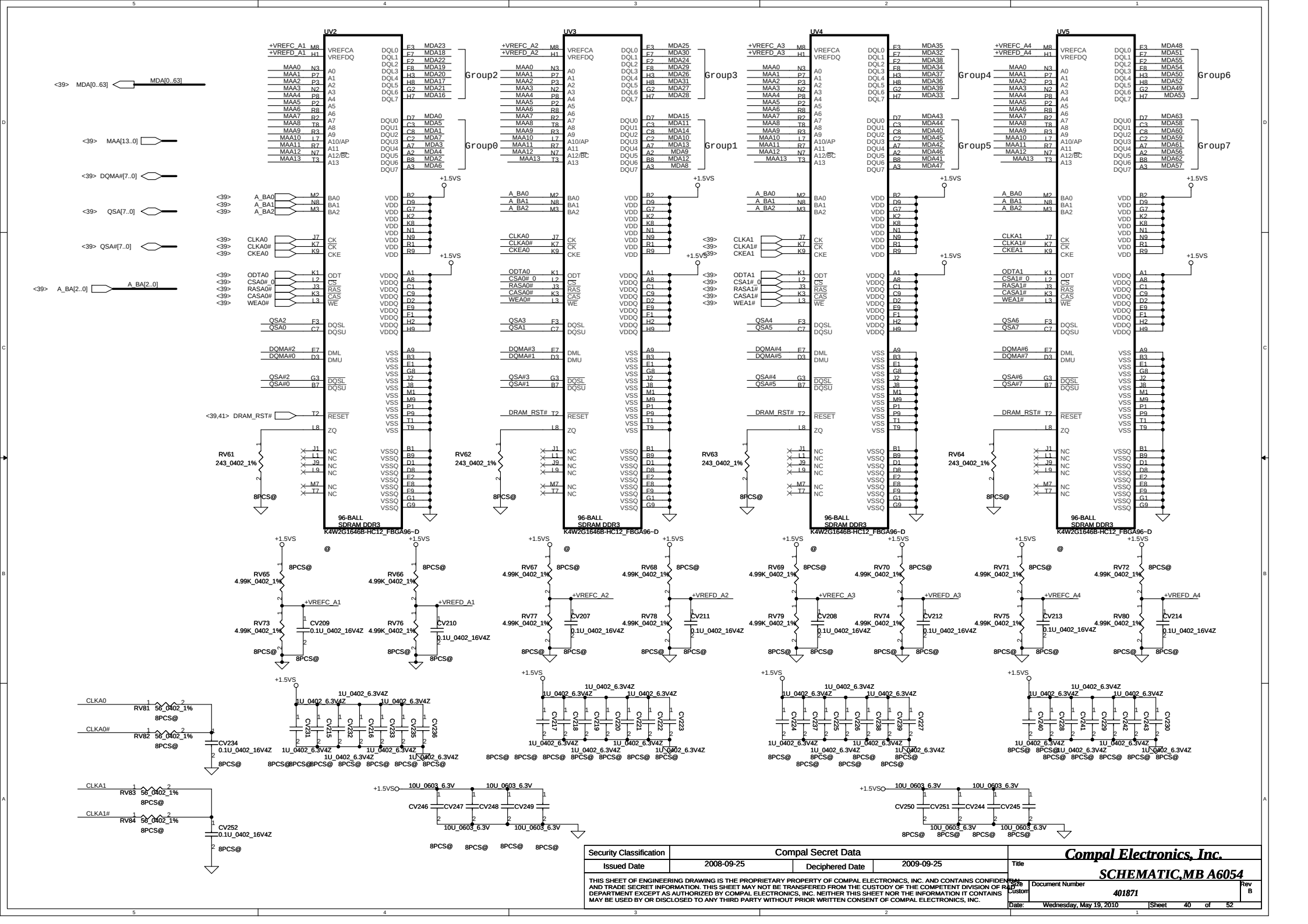

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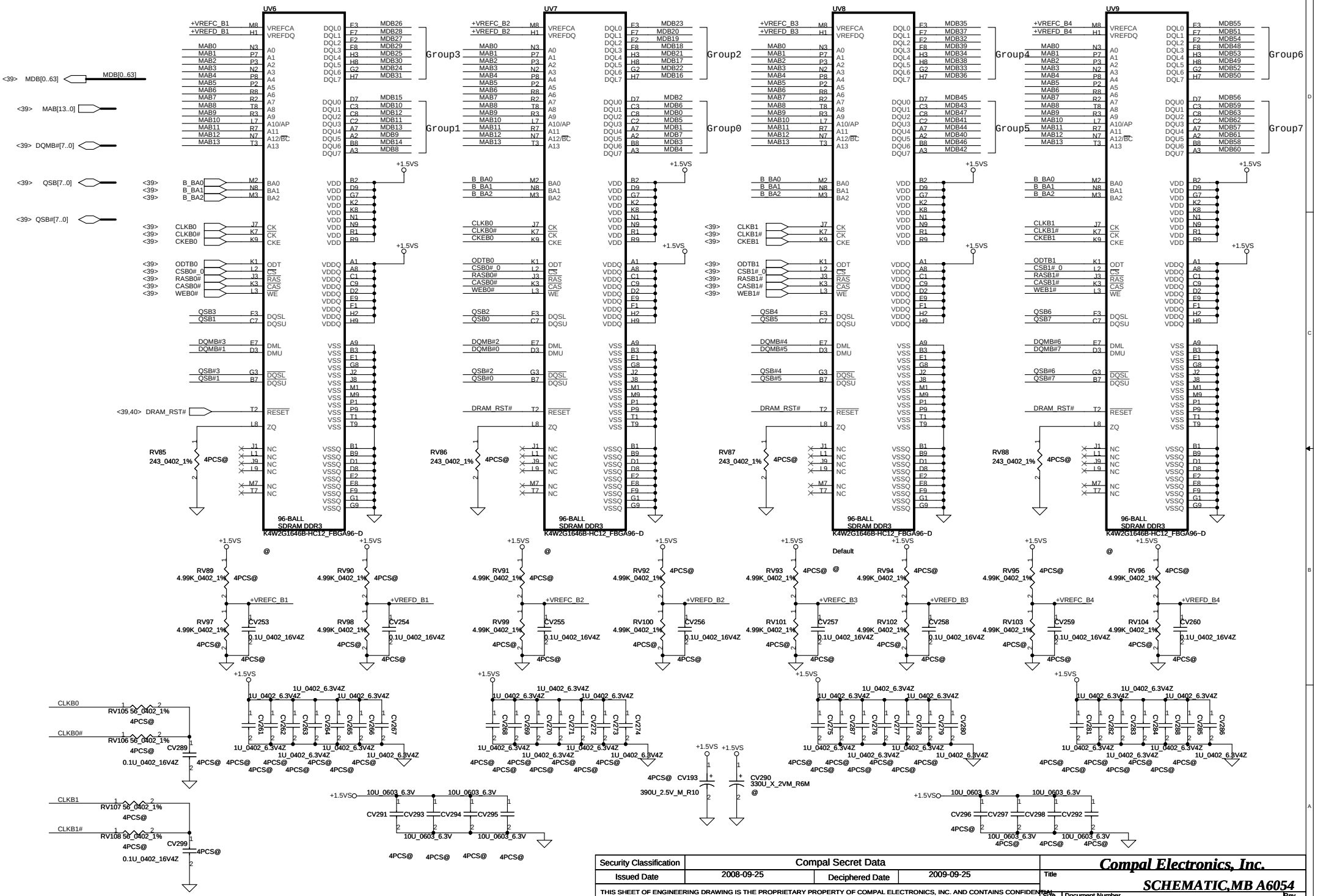

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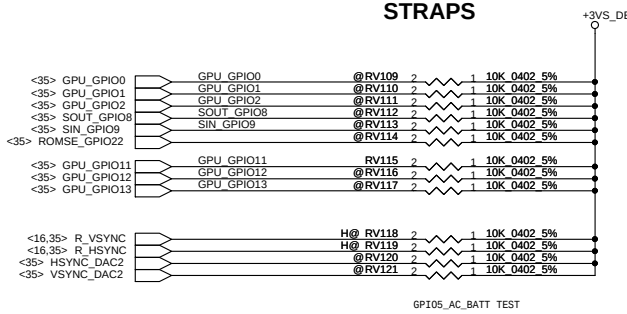
STRAPS

GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

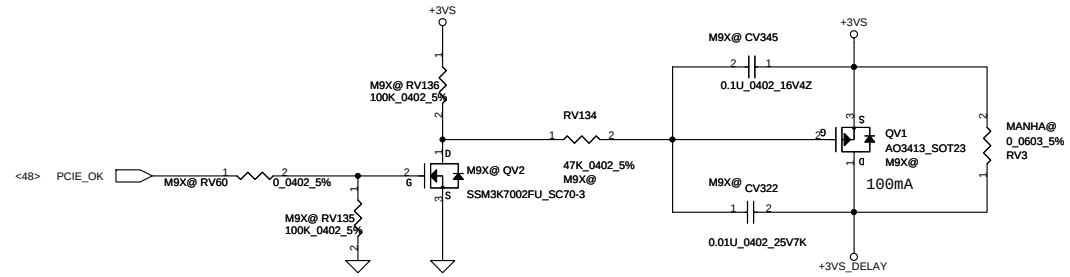
AMD RESERVED CONFIGURATION STRAPS

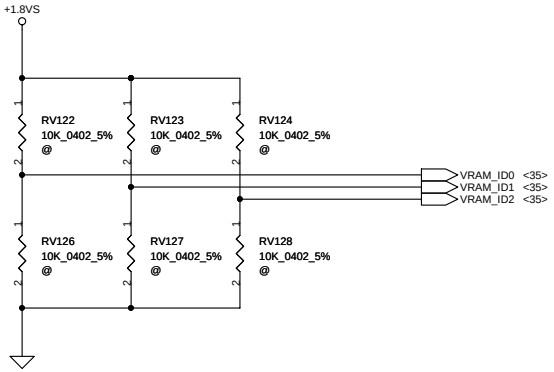
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2 GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

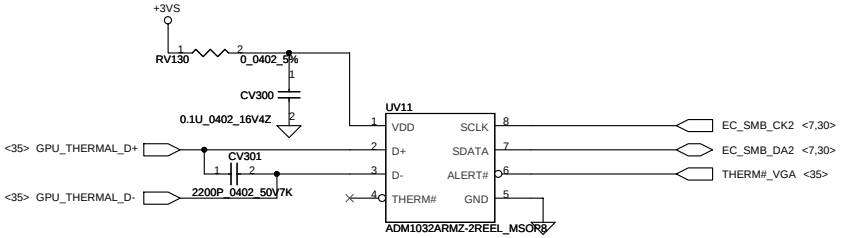
GPIO_28_TDO GPIO21_BB_EN





STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (2,1,0)	Park M2	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN		0 1 0 (Reserve)
			1G 128Mx16 (x4)	SAM K4W2G1646B-HC12	SA00003MQ00	0 1 1 (Reserve)
		Madison M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	1 0 0
			1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			2G 128Mx16 (x8)	HYN		1 1 0 (Reserve)
			2G 128Mx16 (x8)	SAM K4W2G1646B-HC12	SA00003MQ00	1 1 1 (Reserve)

External VGA Thermal Sensor



UV1 — M92 XTX, M92@

UV1 — Madison, MADISON@

UV1 — Park, PARK@

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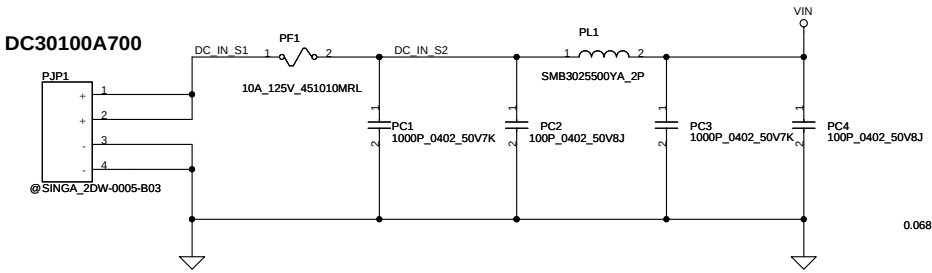
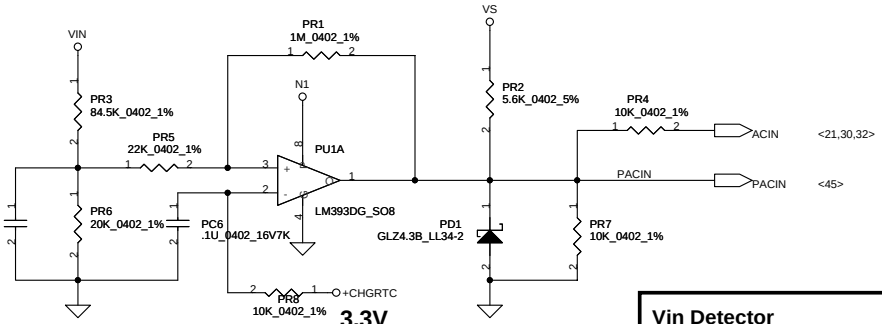
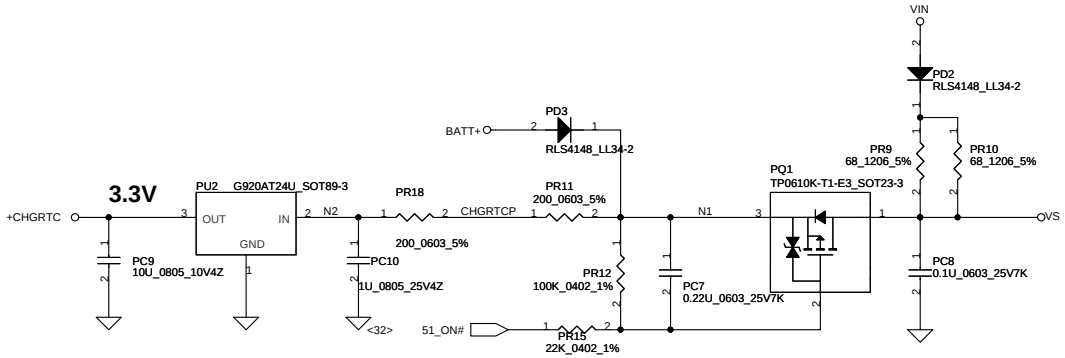


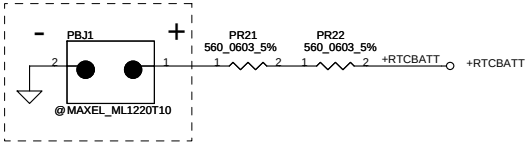


Vin Detector

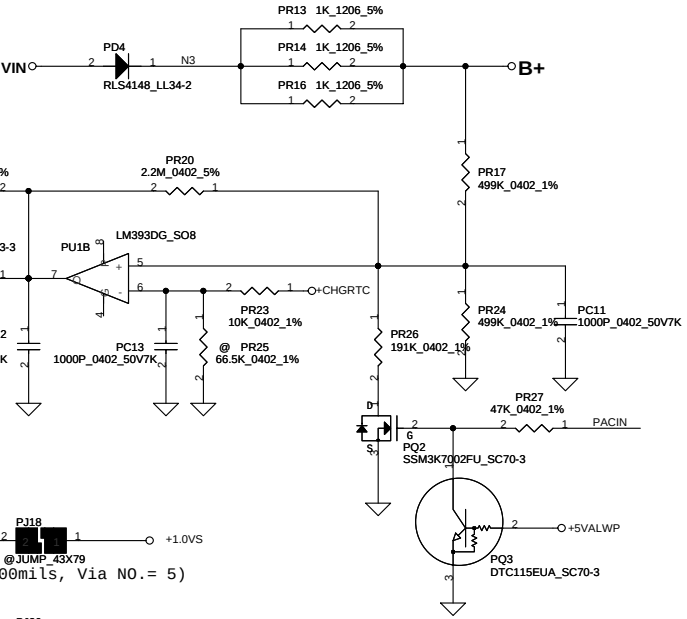
High	**18.384**	**17.901**	**17.430**
Low	**17.728**	**17.257**	**16.976**

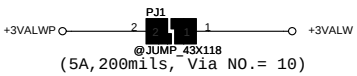


RTC Battery

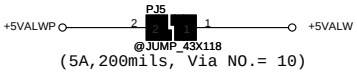


SP093MX0000

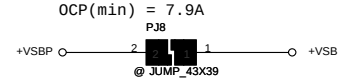




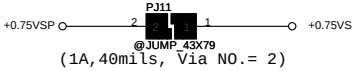
(5A,200mils, Via NO.= 10)
OCP(min) = 7.7A



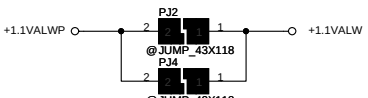
(5A,200mils, Via NO.= 10)
OCP(min) = 7.9A



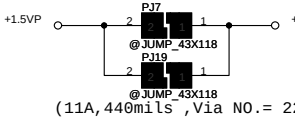
(120mA,40mils, Via NO.= 1)



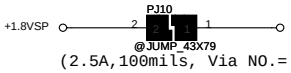
(1A,40mils, Via NO.= 2)



(12A,480mils, Via NO.= 24)
OCP(min) = 18.7A

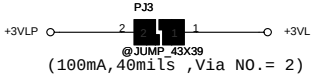


(11A,440mils ,Via NO.= 22)
OCP(min) = 19.16A

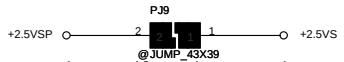


(2.5A,100mils, Via NO.= 5)

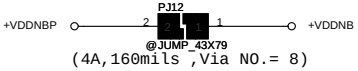
(1.5A,60mils, Via NO.= 3)



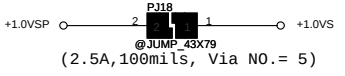
(100mA,40mils ,Via NO.= 2)



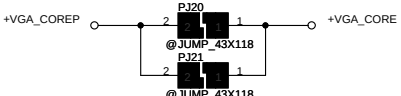
(1A,40mils ,Via NO.= 2)



(4A,160mils ,Via NO.= 8)



(2.5A,100mils, Via NO.= 5)



(20A,800mils ,Via NO.= 40)
OCP(min) = 20.14A

Precharge detector
15.97V/14.84V FOR ADAPTOR

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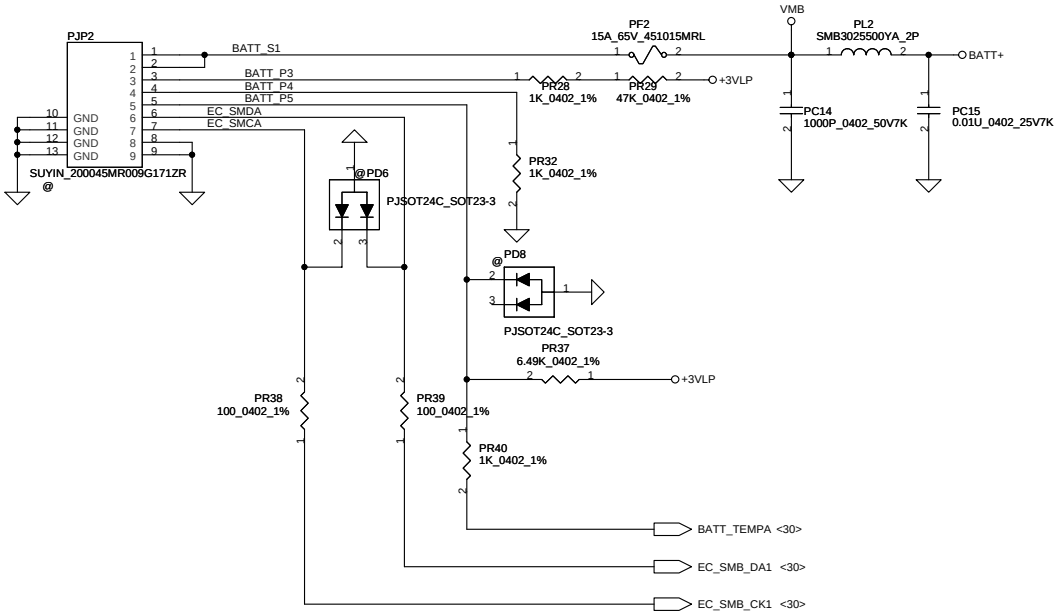
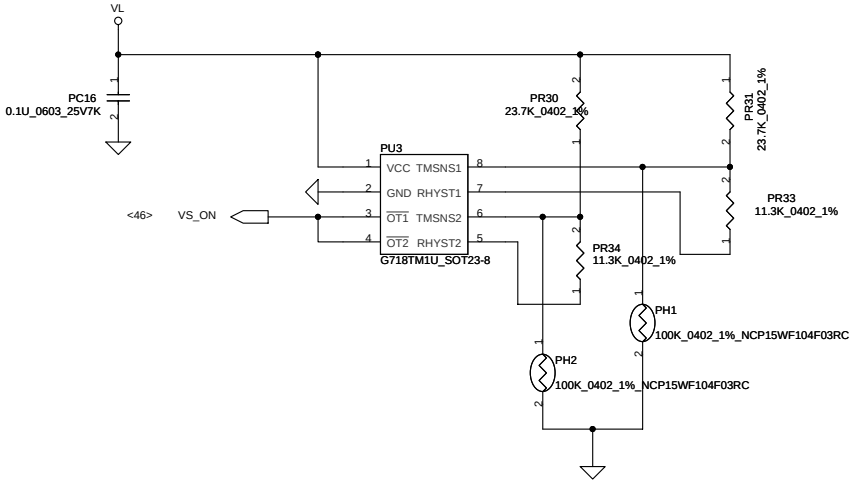
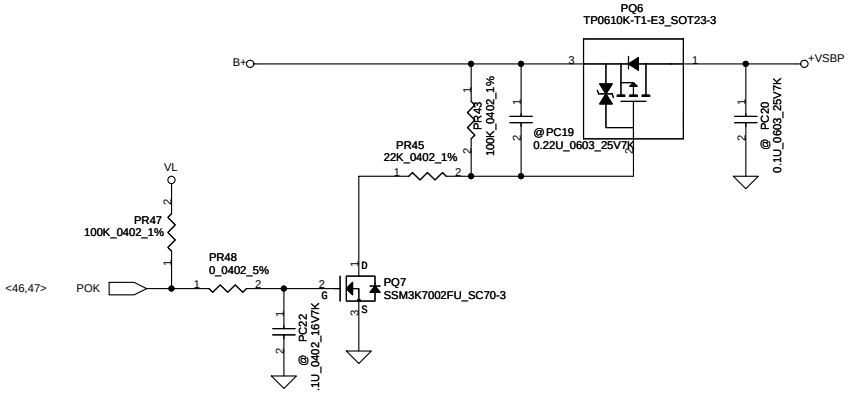


PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
Rset = 3 * 7.87K = 23.61K ==> 23.7K
Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 56 degree C

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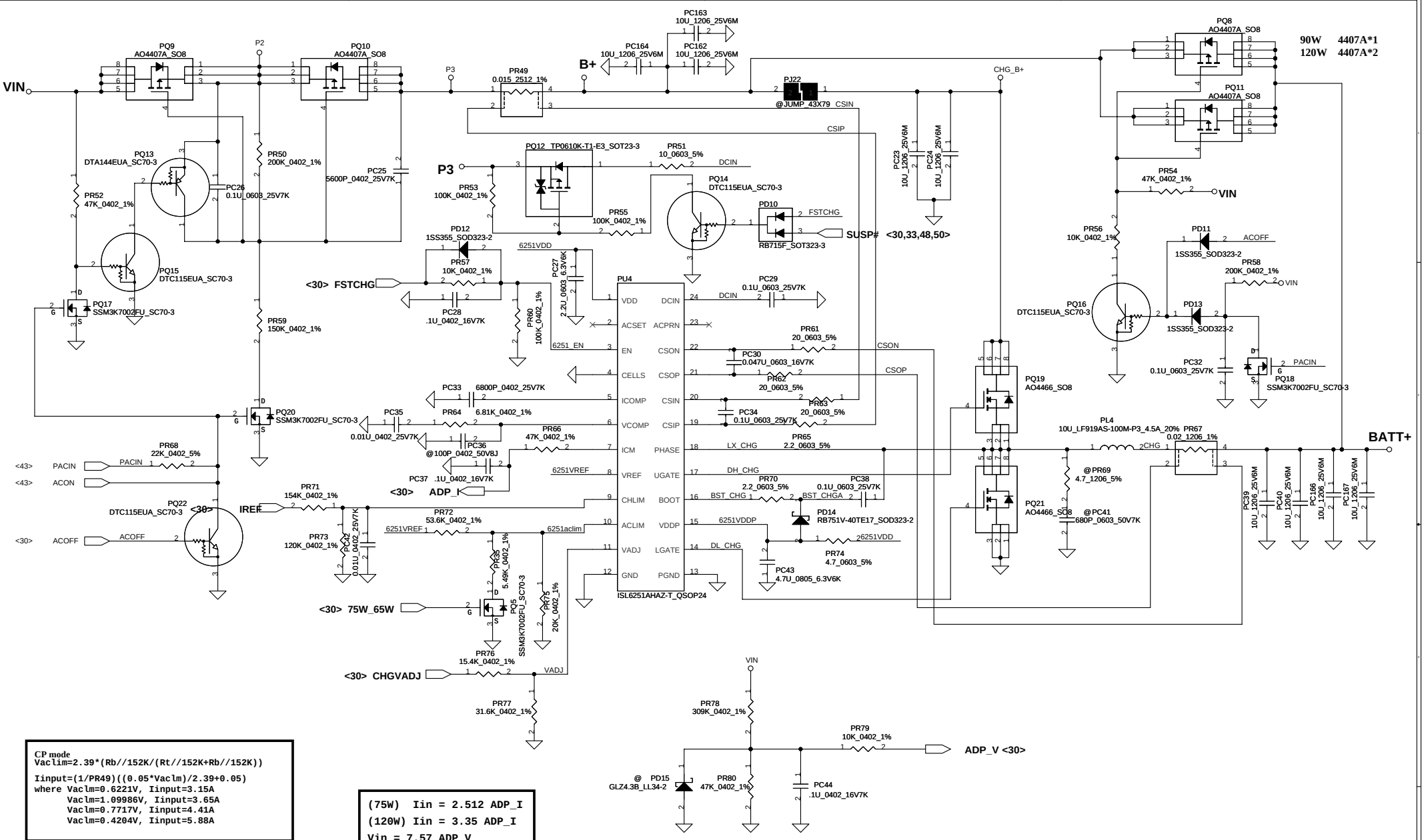

CP mode
Vaclim=2.39*(Rb//152K/(Rt//152K+Rb//152K))

Iinput=(1/PR49)((0.05*Vaclm)/2.39+0.05)
where Vaclm=0.6221V, Iinput=3.15A
Vaclm=1.09986V, Iinput=3.65A
Vaclm=0.7717V, Iinput=4.41A
Vaclm=0.4204V, Iinput=5.88A

(75W) Iin = 2.512 ADP_I
(120W) Iin = 3.35 ADP_I
Vin = 7.57 ADP_V

CC=0.25A~3.6A
IREF=0.9133*Icharge
IREF=0.228V~3.29V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

CELLS	VDD	GND	Float
CELL number	4	3	2

Iada=0~3.421A(65W) CP=3.15A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=high
Iada=0~3.947A(75W) CP=3.63A PR49=0.02, PR72=24k, PR75=20k, PR35=11.5K, 75W_65W=low
Iada=0~4.737A(90W) CP=4.36A PR49=0.015, PR72=53.6k, PR75=20k, PR35=unpop, PQ5=unpop
Iada=0~6.316A(120W) CP=5.81A PR49=0.015, PR72=8.25k, PR75=26.7k, PR35=unpop, PQ5=unpop
CP= 92%*Iada

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Issued Date	2008/9/25	Deciphered Date	2009/9/25

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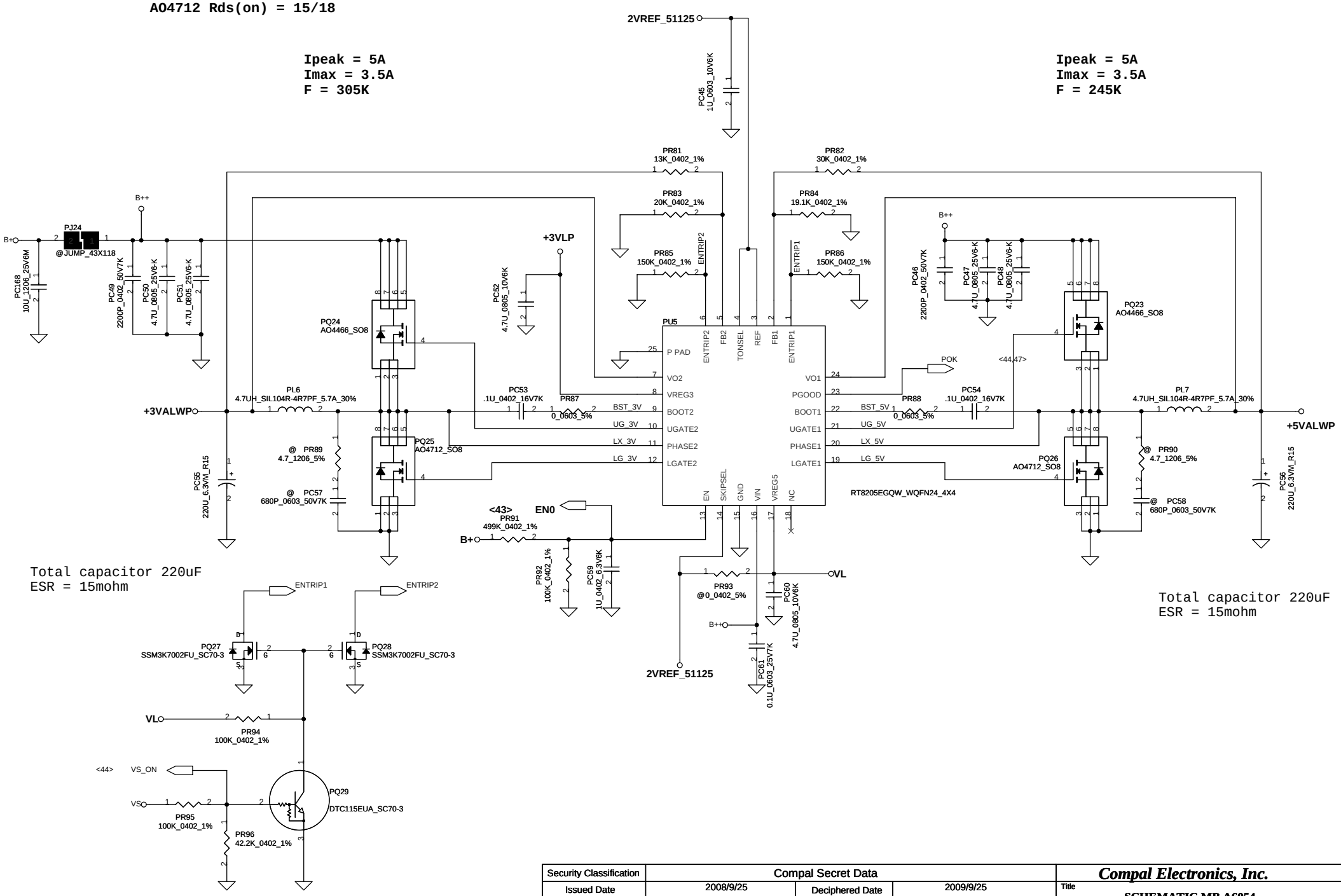

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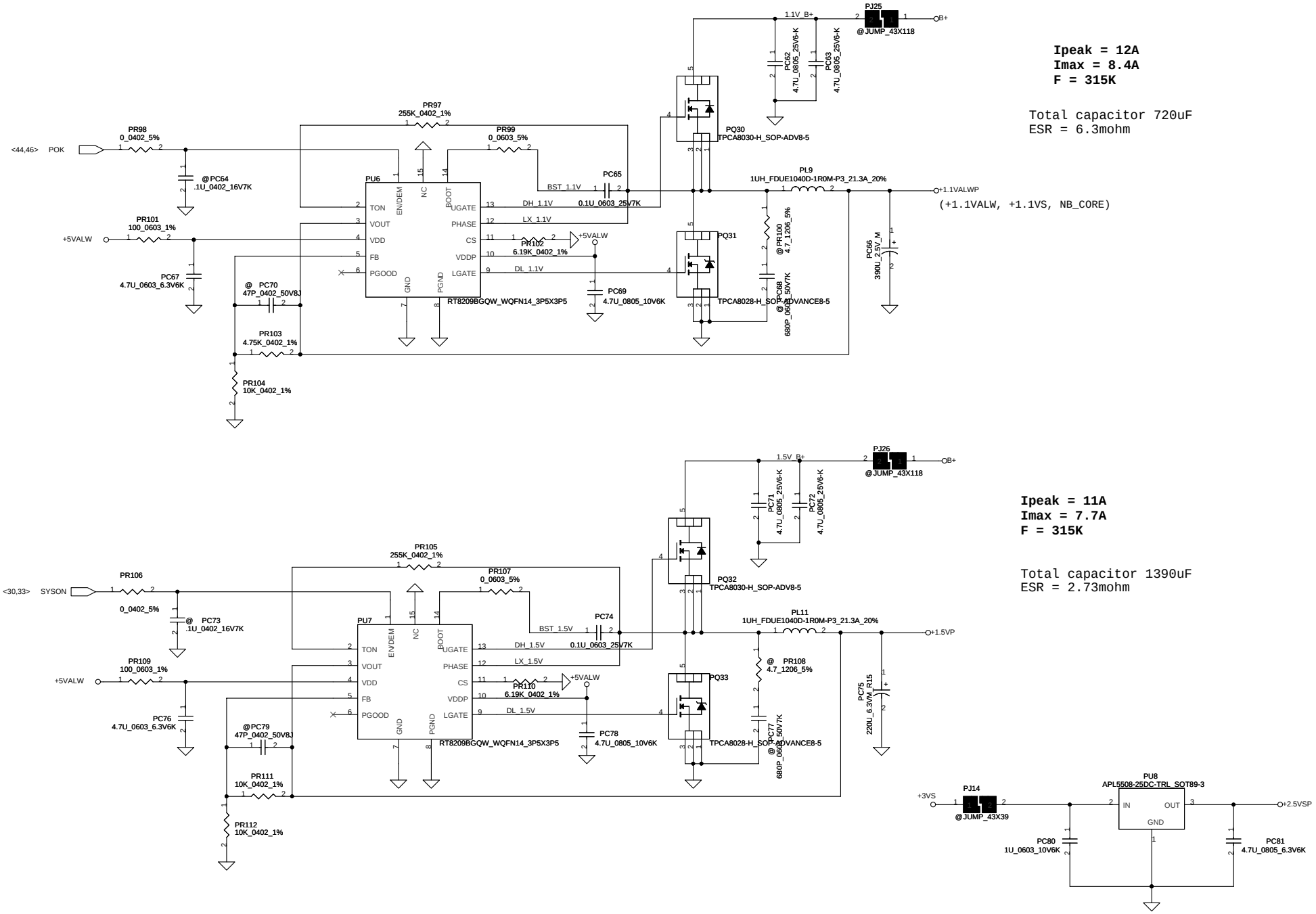

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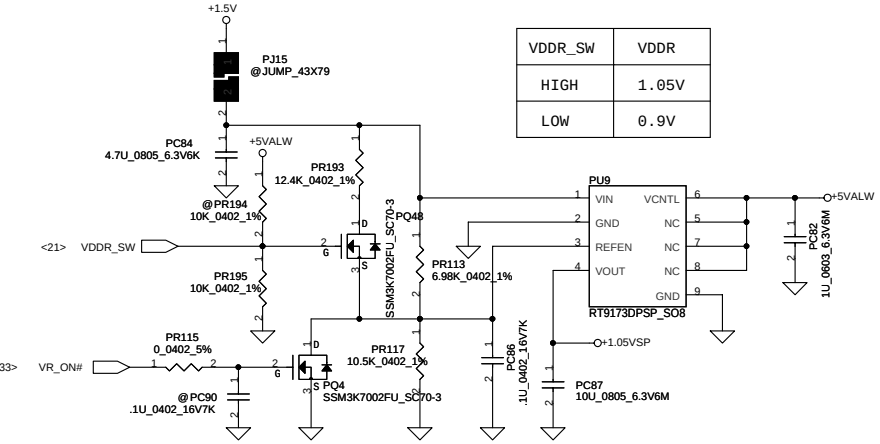
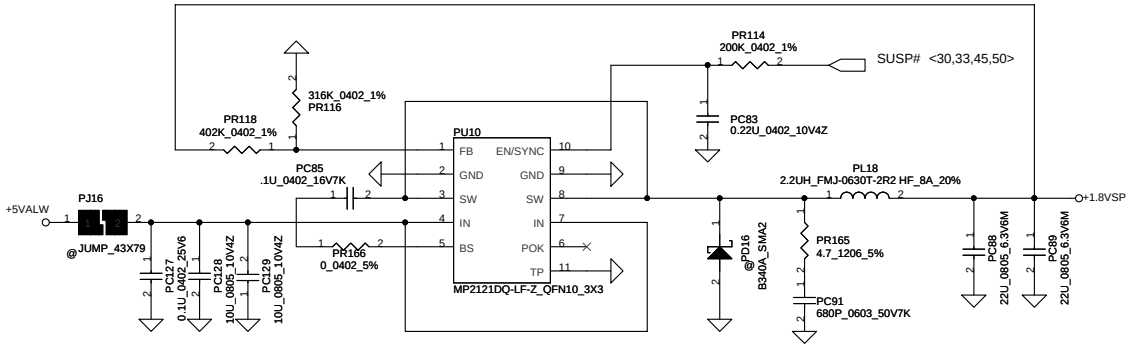
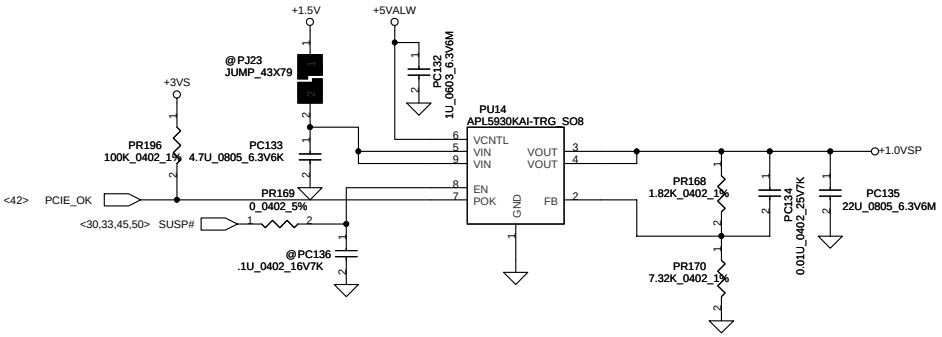
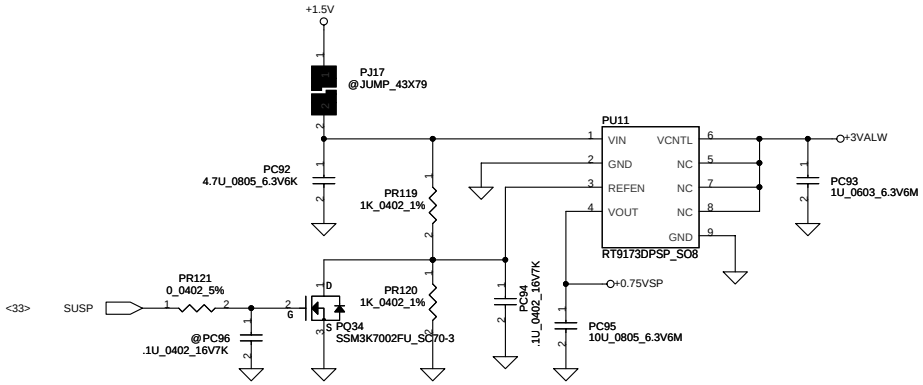


VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V





Madison / Park PCIE : 1.0V	M96 / M92 PCIE : 1.1V
PR170 = 7.32K	PR170 = 4.75K



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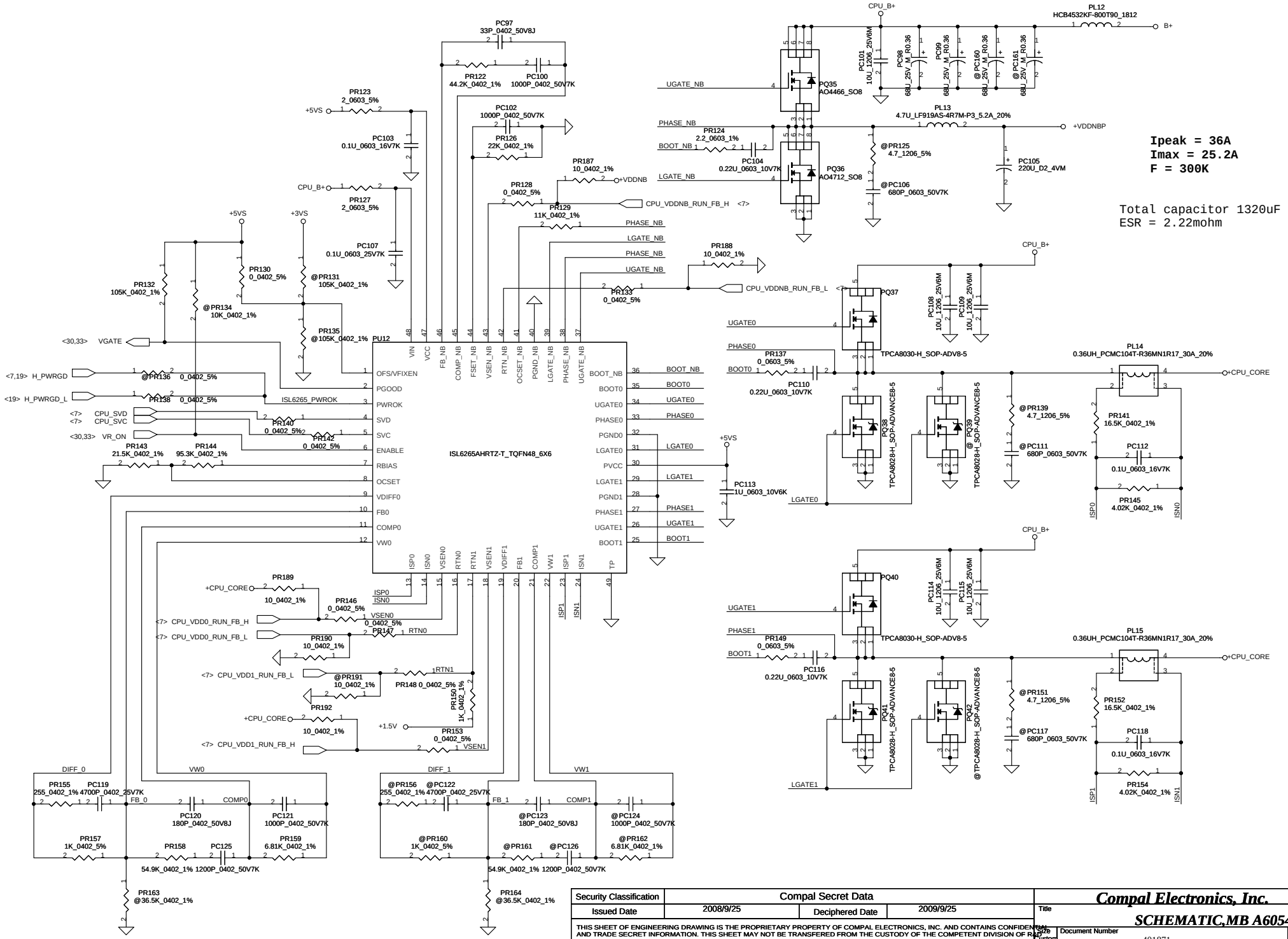

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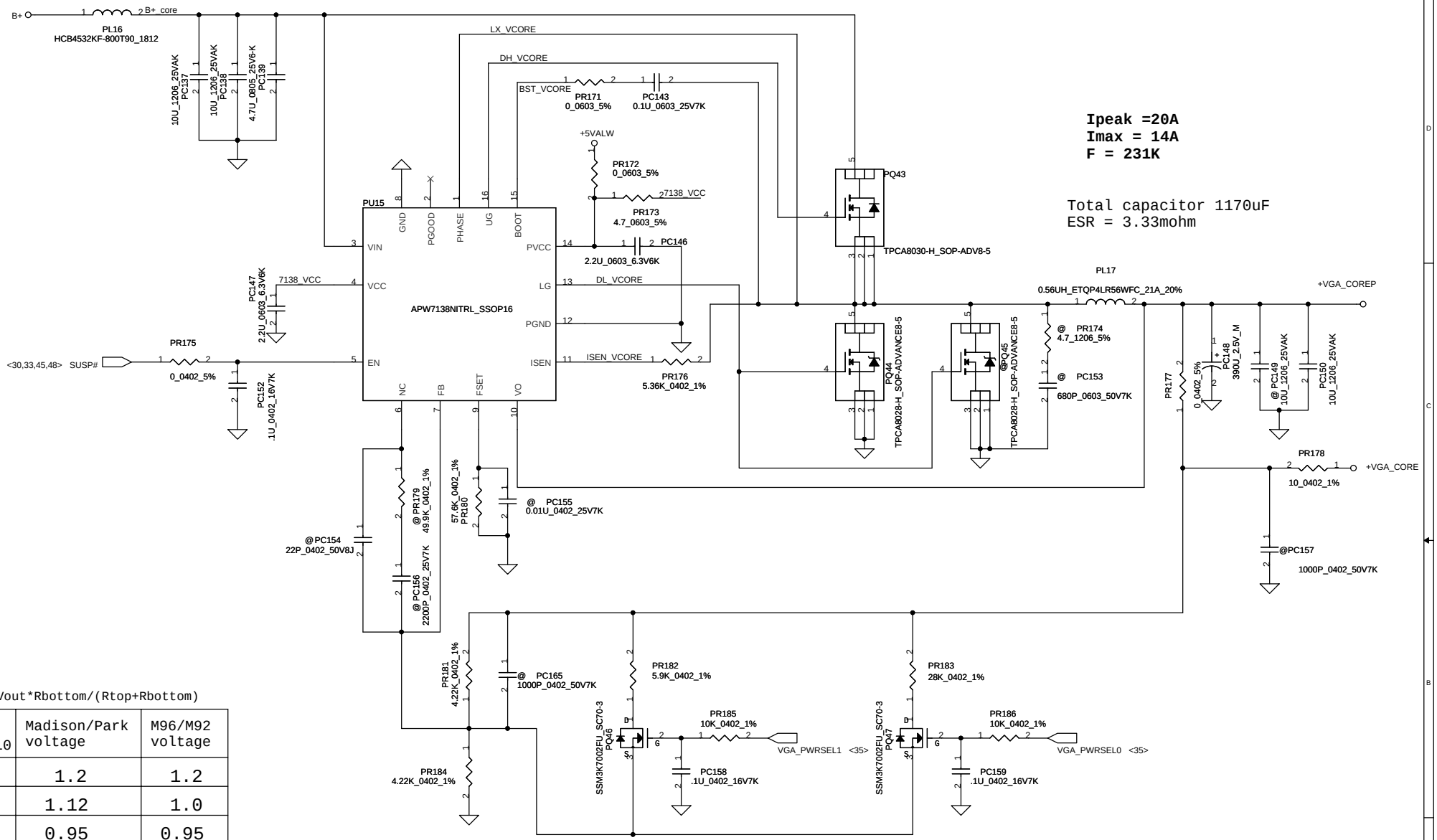

Ipeak =20A
Imax = 14A
F = 231K

Total capacitor 1170uF
ESR = 3.33mohm

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

SEL1	SEL0	Madison/Park voltage	M96/M92 voltage
L	L	1.2	1.2
L	H	1.12	1.0
H	L	0.95	0.95
H	H	0.9	0.9

FSW=1/(75E-12*57.6K)=231.48KHz

Madison Park	M96 M92
PR183 = 28K	PR183 = 12K

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PIR (Product Improve Record)

NALAE LA-6054P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at JWLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cgange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cgange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cgange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cgange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

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Version Change List (P. I. R. List) for Power Circuit

Page#	Item Title	Solution Description
DVT : modification from EVT		
P47	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P47	change 1.1V, 1.5V OCP value	change PR102, PR110 to 6.19K
P48	enlarge output cap	change PC88, PC89 to 22uF(SE000000I10)
P49	don't use NIPPON cap	change PC98, PC99 to SF000000S80
P49	pull high RTN1 1.5V	change PR150 to mount
P50	APW7138 pin6 is NC	change PR179, PC154, PC156 to unmount
P46	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P45	change system power from 90W to 120W	change PR72 to 8.25K, PR75 to 26.7K; PQ11 to mount
P49	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P45	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P48	mount snubber circuit	mount PR165, PC91
P44	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P48	change IC to low cost	change PU9 and PU11 to RT9173
P48	change VDDR(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48
PVT : modification from DVT		
P49	cost down	change PC98, PC99, PC160, PC161 to SF000000W00
P46	common circuit	change PC45 to 1uF
P46	common circuit	mount PC59
P46	change PQ29 solution	change PQ29 to DTC115EUA
P45	add 65W/75W selection circuit	Add PR35 and PQ5, unmount
P47	prevent OVP for HW's cost down	change PC66 to 390uF
P48	PCIE_OK pull high +3VS	add PR196=100K
P50	For 7138 output sensing stability	add PC165=1000p unmount
P45	EMI request for ISN issue	Add PC166, PC167, 10uF 1206
P46	EMI request for ISN issue	Add PC168, 10uF 1206
PreMP : modification from PVT		
P44	Thermal request change OTP	change PR30, PR31 to 23.7K; PR33, PR34 to 11.3K
P45	modify 65W/75W resistor	change PR72 to 53.6K; PR75 to 20K; mount PR35 and PQ5
P48	modify 1.05V voltage setting	change PR113 to 6.98K
P50	modify VGA_CORE Choke	change PL17 to SH12056BM00
P43	modify RTC circuit	

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