Compal confidential

Hamburg 10ADG

NALAE LA-6052P Schematics Document

Mobile AMD S1G4/ RS880M / SB820M

2009-11-27 Rev. 0.2

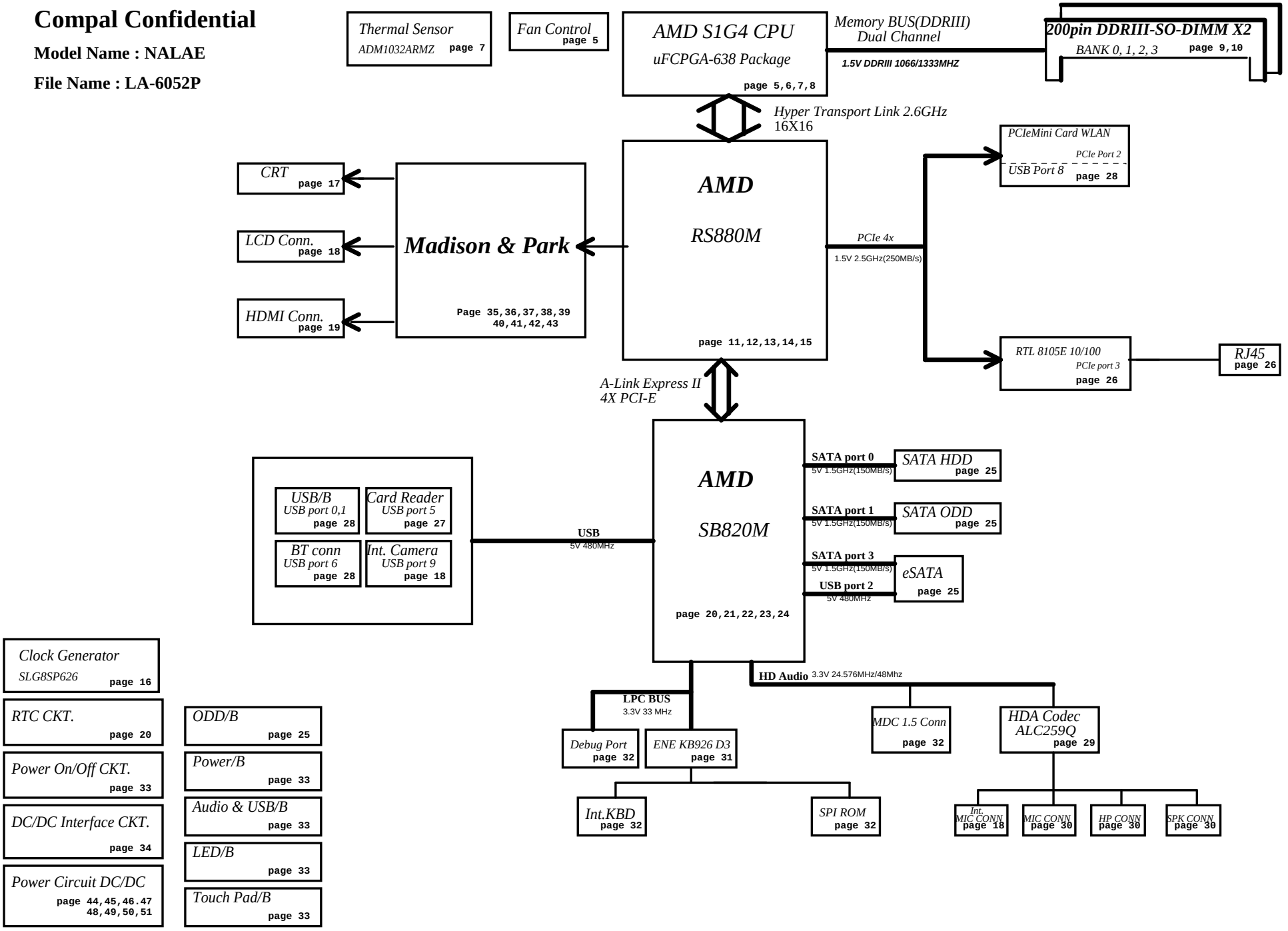
Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.		
Title	*SCHEMATIC,MB A6052*	
Size: Custom	Document Number: *401851*	Rev: A
Date: Wednesday, January 20, 2010	Sheet 1 of 53	

Compal Confidential

Model Name : NALAE

File Name : LA-6052P



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Title: **SCHEMATIC,MB A6052**

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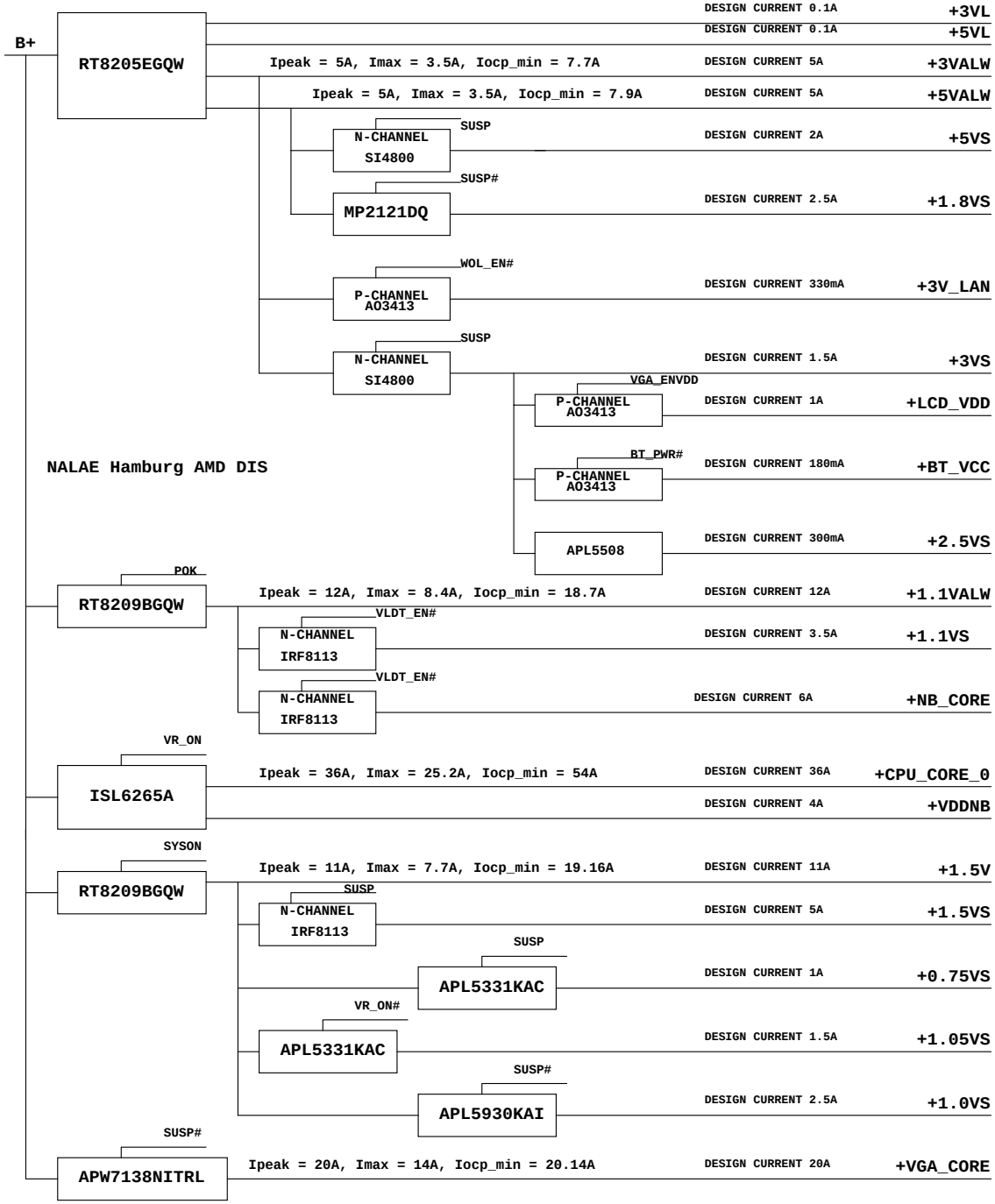

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Voltage Rails

O : ON
X : OFF

power plane / State	B+ +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +VGA_CORE +VDDNB +CPU_CORE +NB_CORE
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: Digital Ground

: Analog Ground

@ : just reserve , no build

Platform	CPU	NB	VGA	SB	Comment
Danube	S1G4	RS880M	NA	SB820M	

GPU	CPU	NB	VGA	SB	Comment
Manhattan	S1G4	RS880M	MADISON	SB820M	MANHA@+MADISON@ or PARK@+ +4PCS or 8PCS
	S1G4	RS880M	PARK	SB820M	
M9X	S1G4	RS880M	M96	SB820M	M9X@+M92@ +4PCS or 8PCS
	S1G4	RS880M	M92	SB820M	

BTO (Build-To-Order) Option Table

Function	BLUE TOOTH	HDMI				
Description	(B)	(Y)				
Explain						
BTO	BT@	H@				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

SMBUS Control Table

	SOURCE	BATT	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM
EC_SMB_CK1 EC_SMB_DA1	KB926	V						
EC_SMB_CK2 EC_SMB_DA2	KB926		V					
I2C_CLK I2C_DATA	RS880M						V	
DDC_CLK0 DDC_DATA0	RS880M							V
SCL0 SDA0	SB820			V	V			
SCL1 SDA1	SB820					V		

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D3		

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+1.1VS

250 mil VLDT CAP. Near CPU Socket

C1 10U_0805_10V4Z
C2 10U_0805_10V4Z
C3 0.22U_0603_16V4Z
C4 0.22U_0603_16V4Z
C5 180P_0402_50V8J
C6 180P_0402_50V8J

<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]
H_CADOP[0..15] H_CADOP[0..15] <11>
H_CADON[0..15] H_CADON[0..15] <11>

+1.1VS

VLDT=500mA

JCPUA

HT LINK

D1	VLDT_A0	VLDT_B0	AE2	+VLDT_B	C7 10U_0805_10V4Z
D2	VLDT_A1	VLDT_B1	AE3		
D3	VLDT_A2	VLDT_B2	AE4		
D4	VLDT_A3	VLDT_B3	AE5		

< VLDT_A & VLDT_B : HyperTransport I/O ring power >

< From NB >

H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	H_CADON5
H_CADIP6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	E5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

< To NB >

<11> H_CLKIP0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	H_CLKOP0 <11>
<11> H_CLKIN0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	H_CLKON0 <11>
<11> H_CLKIP1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	H_CLKOP1 <11>
<11> H_CLKIN1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	H_CLKON1 <11>
<11> H_CTLIP0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	H_CTLOP0 <11>
<11> H_CTLIN0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	H_CTLON0 <11>
<11> H_CTLIP1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	H_CTLOP1 <11>
<11> H_CTLIN1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	H_CTLON1 <11>

FOX_PZ6382A-284S-41F_Champlian

+1.5V J2 +1.5V_CPU
@JUMP_43X118

< FAN Control Circuit : Vout = 1.6 x Vset >

+5VS
1A
+FAN1
C1120 10U_0805_10V4Z
C1119 10U_0805_10V4Z
U31
EN GND
VIN GND
VOUT GND
VSET GND
APL5607KI-TRG_SO8
<31> EN_DFAN1
@ C1121 1000P_0402_25V8J
+FAN1
JFAN
GND GND
@ACES_85204-0300N
+3VS
R795 10K_0402_5%
FAN_SPEED1 <31>
@ C1122 0.01U_0402_25V7K

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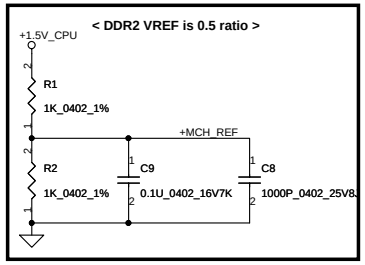
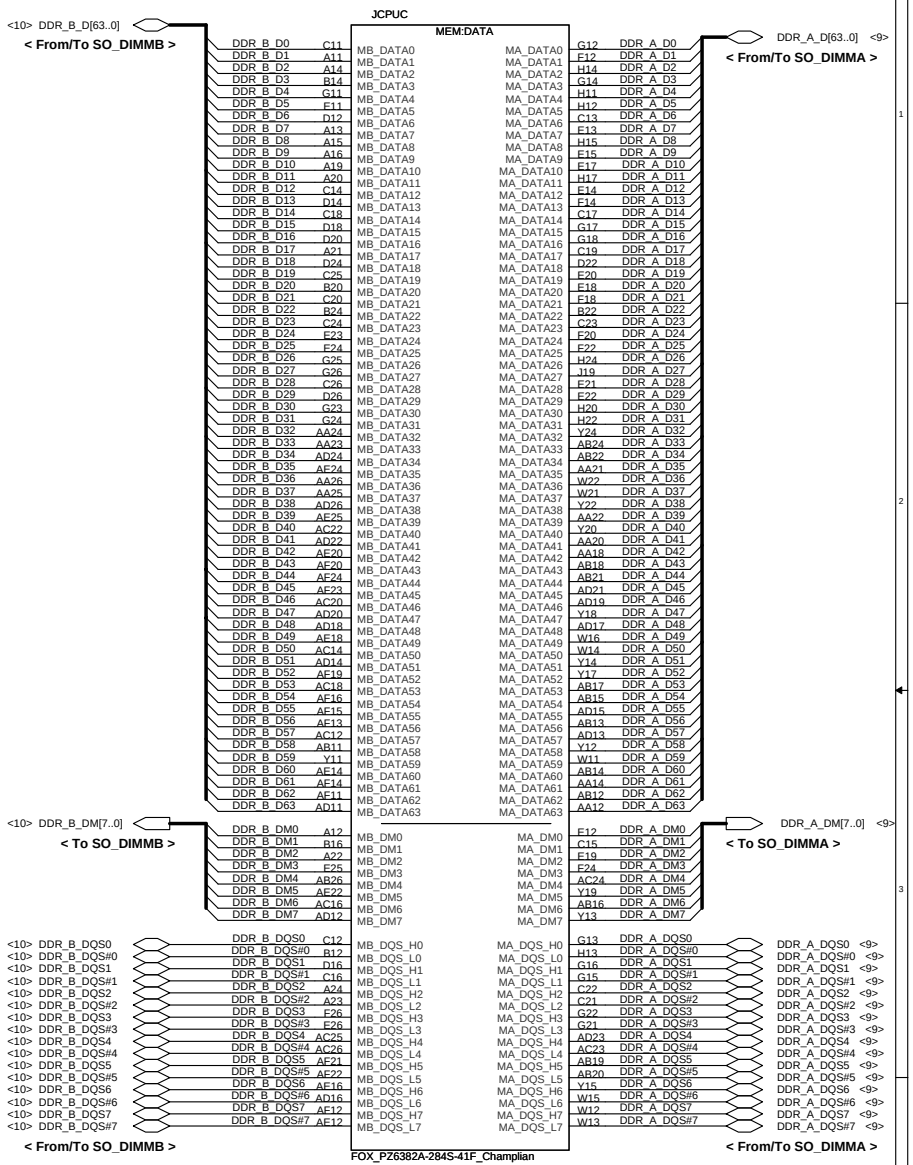
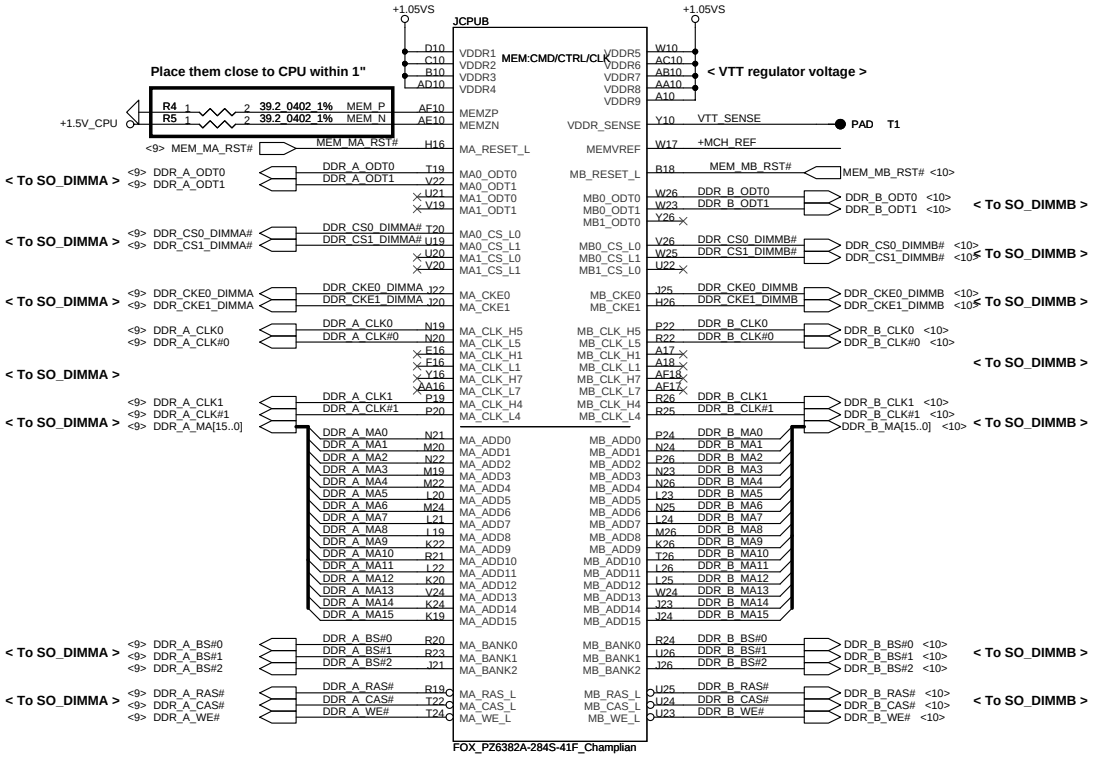
< DDR2 VREF is 0.5 ratio >



< Processor DDR3 Memory Interface >





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< Filtered PLL Supply Voltage >

+2.5VS — L1 FBM_L11_201209_300L_0805 — VDDA=300mA — +2.5VDDA

@ C11 150U_B2_6.3VM_R45M

C12 4.7U_0805_10V4Z

C13 3300P_0402_50V7-K

C14 0.22U_0603_16V4Z

< 200-MHz PLL Reference Clock >

<16> CLK_CPU_BCLK — C16 3900P_0402_50V7K — CPU_CLKIN_SC_P

R10 169_0402_1%

<16> CLK_CPU_BCLK# — C15 3900P_0402_50V7K — CPU_CLKIN_SC_N

Address:100_1100 Place close to CPU wihtin 1.5"

JCPUD

+2.5VDDA — F8 VDDA1, F9 VDDA2

CPU_CLKIN_SC_P — A9 CLKIN_H

CPU_CLKIN_SC_N — A8 CLKIN_L

LDT_RST# — B7 RESET_L

H_PWRGD — A7 PWROK

LDT_STOP# — F10 LDTSTOP_L

C6 LDTREQ_L

T2 PAD

+1.5V_CPU — R12 1K_0402_5% — CPU_SIC — AF4 SIC

+1.5V_CPU — R14 1K_0402_5% — CPU_SID — AF5 SID

AE6 ALERT_L

+1.1VS — R15 44.2_0402_1% — CPU_HTREF0 — R6 HT_REF0

R16 44.2_0402_1% — CPU_HTREF1 — P6 HT_REF1

<50> CPU_VDD0_RUN_FB_H — CPU_VDD0_RUN_FB_H — F6 VDD0_FB_H

<50> CPU_VDD0_RUN_FB_L — CPU_VDD0_RUN_FB_L — E6 VDD0_FB_L

<50> CPU_VDD1_RUN_FB_H — CPU_VDD1_RUN_FB_H — Y6 VDD1_FB_H

<50> CPU_VDD1_RUN_FB_L — CPU_VDD1_RUN_FB_L — AB6 VDD1_FB_L

CPU_DBRDY — G10 DBRDY

CPU_TMS — AA9 TMS

CPU_TCK — AC9 TCK

CPU_TRST# — AD9 TRST_L

CPU_TDI — AF9 TDI

CPU_TEST23 — AD7 TEST23

CPU_TEST18 — H10 TEST18

CPU_TEST19 — G9 TEST19

CPU_TEST25H — E9 TEST25_H

CPU_TEST25L — E8 TEST25_L

CPU_TEST21 — AB8 TEST21

CPU_TEST20 — AE7 TEST20

CPU_TEST24 — AE7 TEST24

CPU_TEST22 — AE8 TEST22

CPU_TEST12 — AC8 TEST12

CPU_TEST27 — AE8 TEST27

R24 0_0402_5% — C2 TEST9, AA6 TEST6

A3 RSVD1, A5 RSVD2, B3 RSVD3, B5 RSVD4, C1 RSVD5

VSS — M11, RSVD11 — W18

SVC — A6 CPU_SVC — CPU_SVC <50>

SVD — A4 CPU_SVD — CPU_SVD <50>

< Serial VID Interface clock & data >

THERMTRIP_L — AF6 CPU_THERMTRIP# R

PROCHOT_L — AC7 CPU_PROCHOT#

MEMHOT_L — AA8 PAD T3

THERMDC — W7 THERMDC_CPU

THERMDA — W8 THERMDA_CPU

route as differential as short as possible testpoint under package

VDDIO_FB_H — W9

VDDIO_FB_L — Y9

VDDNB_FB_H — H6 CPU_VDDNB_RUN_FB_H — CPU_VDDNB_RUN_FB_H <50>

VDDNB_FB_L — G6 CPU_VDDNB_RUN_FB_L — CPU_VDDNB_RUN_FB_L <50>

DBREQ_L — F10 CPU_DBREQ#

TDO — AF9 CPU_TDO

TEST28_H — J7

TEST28_L — H8

TEST17 — D7 CPU_TEST17 — PAD T4

TEST16 — F7 CPU_TEST16 — PAD T5

TEST15 — F7 CPU_TEST15 — PAD T6

TEST14 — C7 CPU_TEST14 — PAD T7

TEST7 — C3

TEST10 — K8

TEST8 — C4

TEST29_H — C9 CPU_TEST29_H_FBCLKOUT_P

TEST29_L — C8 CPU_TEST29_L_FBCLKOUT_N — R25 80.6_0402_1%

H18 RSVD10, H19 RSVD9, AA7 RSVD8, D5 RSVD7, C5 RSVD6

FOX_PZ6382A-284S-41F_Champlian

+1.5V_CPU — R19 1K_0402_5% — CPU_SVC

+1.5V_CPU — R20 1K_0402_5% — CPU_SVD

R11 300_0402_5% — CPU_PROCHOT# — @R13 0_0402_5% — H_PROCHOT# <20>

+1.5V_CPU — R6 10K_0402_5%

R7 1K_0402_5% — Q1 MMBT3904_NL_SOT23-3

CPU_THERMTRIP#_R — H_THERMTRIP# <21>

+1.5V_CPU

R22 510_0402_5% CPU_TEST25H

R28 1K_0402_5% CPU_TEST27

R27 510_0402_5% CPU_TEST25L

R29 1K_0402_5% CPU_TEST12

R30 1K_0402_5% CPU_TEST18

R31 1K_0402_5% CPU_TEST19

R32 1K_0402_5% CPU_TEST20

R33 1K_0402_5% CPU_TEST21

R34 1K_0402_5% CPU_TEST22

R265 1K_0402_5% CPU_TEST23

R35 1K_0402_5% CPU_TEST24

+1.5VS

<20> LDT_RST# — R17 300_0402_5% — LDT_RST# — @ C17 0.01U_0402_25V7K

<20,50> H_PWRGD — R21 300_0402_5% — H_PWRGD — @ C19 0.1U_0402_16V7K

<12,20> LDT_STOP# — R18 300_0402_5% — LDT_STOP# — @ C18 0.01U_0402_25V7K

< HDT Connector >

JP2

+1.5V_CPU — R40 300_0402_5% — CPU_DBREQ#

CPU_DBRDY

R39 220_0402_5% — CPU_TCK

R38 220_0402_5% — CPU_TMS

R37 220_0402_5% — CPU_TDI

+1.5V_CPU — R36 220_0402_5% — CPU_TRST#

CPU_TDO

+1.5V_CPU — LDT_RST#

@ SAMTEC_ASP-68200-07

< Thermal Sensor >

+3VS — C20 0.1U_0402_16V7K

C21 3300P_0402_50V7-K < noise filter cap >

U1 ADM1032ARM-1 ZREEL_MSOP8

VDD — SCLK — EC_SMB_CK2 — EC_SMB_CK2 <31,43>

D+ — SDATA — EC_SMB_DA2 — EC_SMB_DA2 <31,43>

THERMDA_CPU — D- — ALERT#

THERMDC_CPU — THERM# — GND

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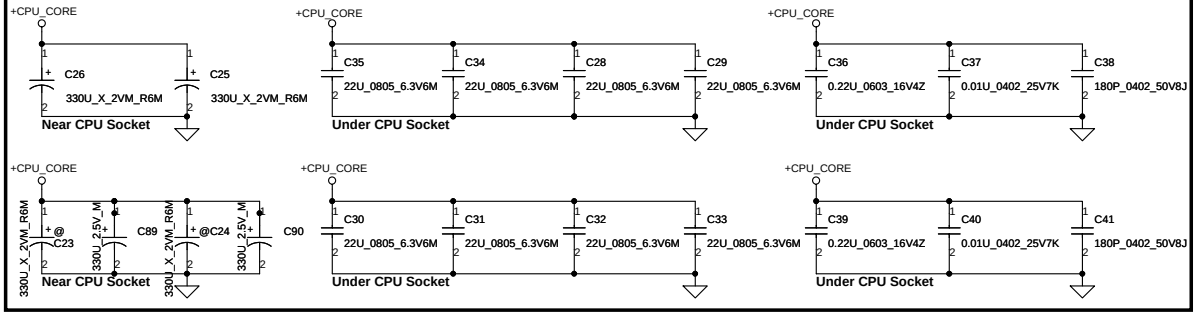
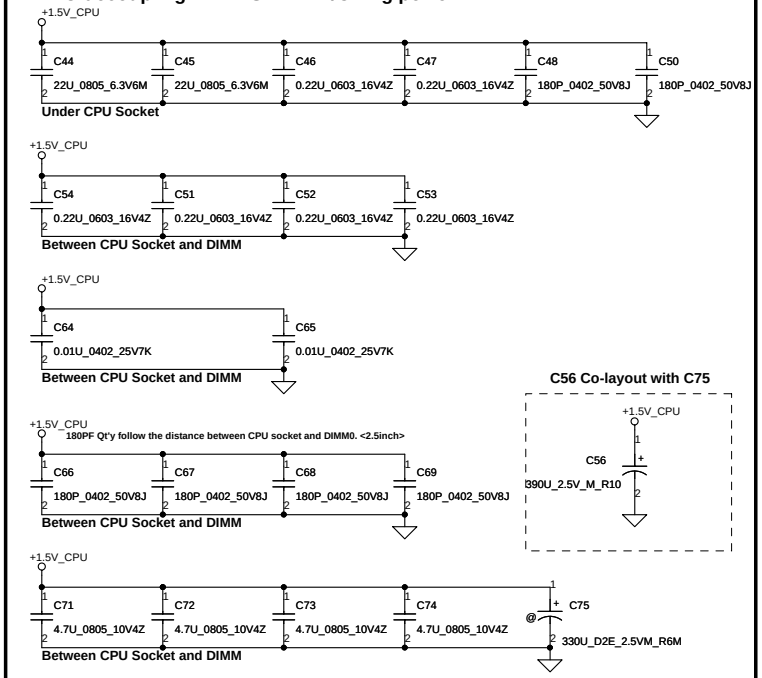
VDD decoupling : +CPU_CORE

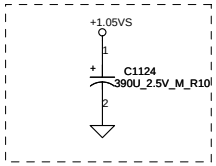


VDDIO decoupling : DDR SDRAM I/O ring power

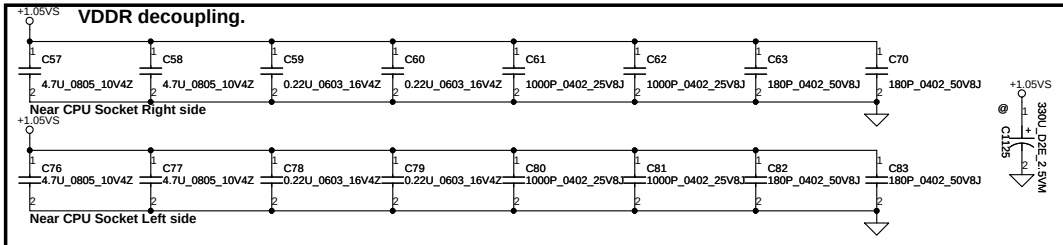


C56 Co-layout with C75

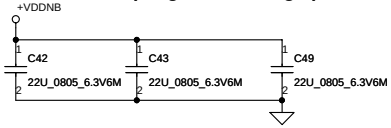
C1124 Co-layout with C1125

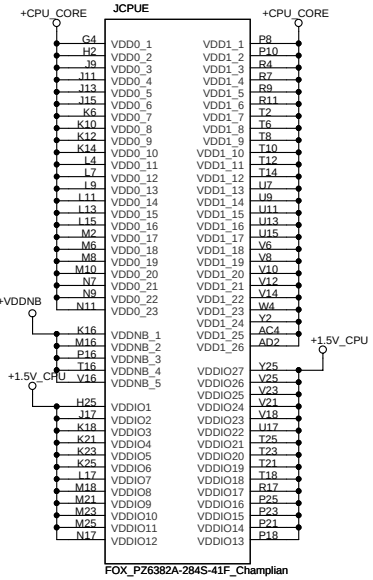


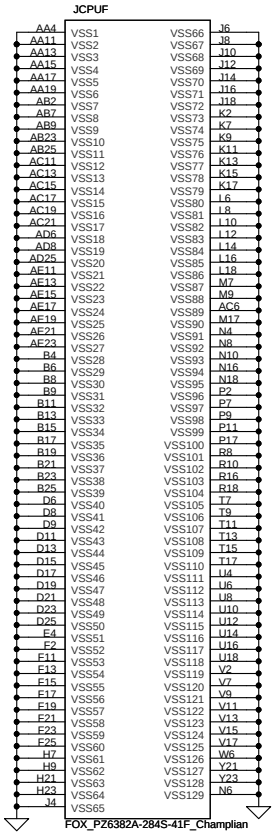
VDDR decoupling.



+VDDNB decoupling : Northbridge power







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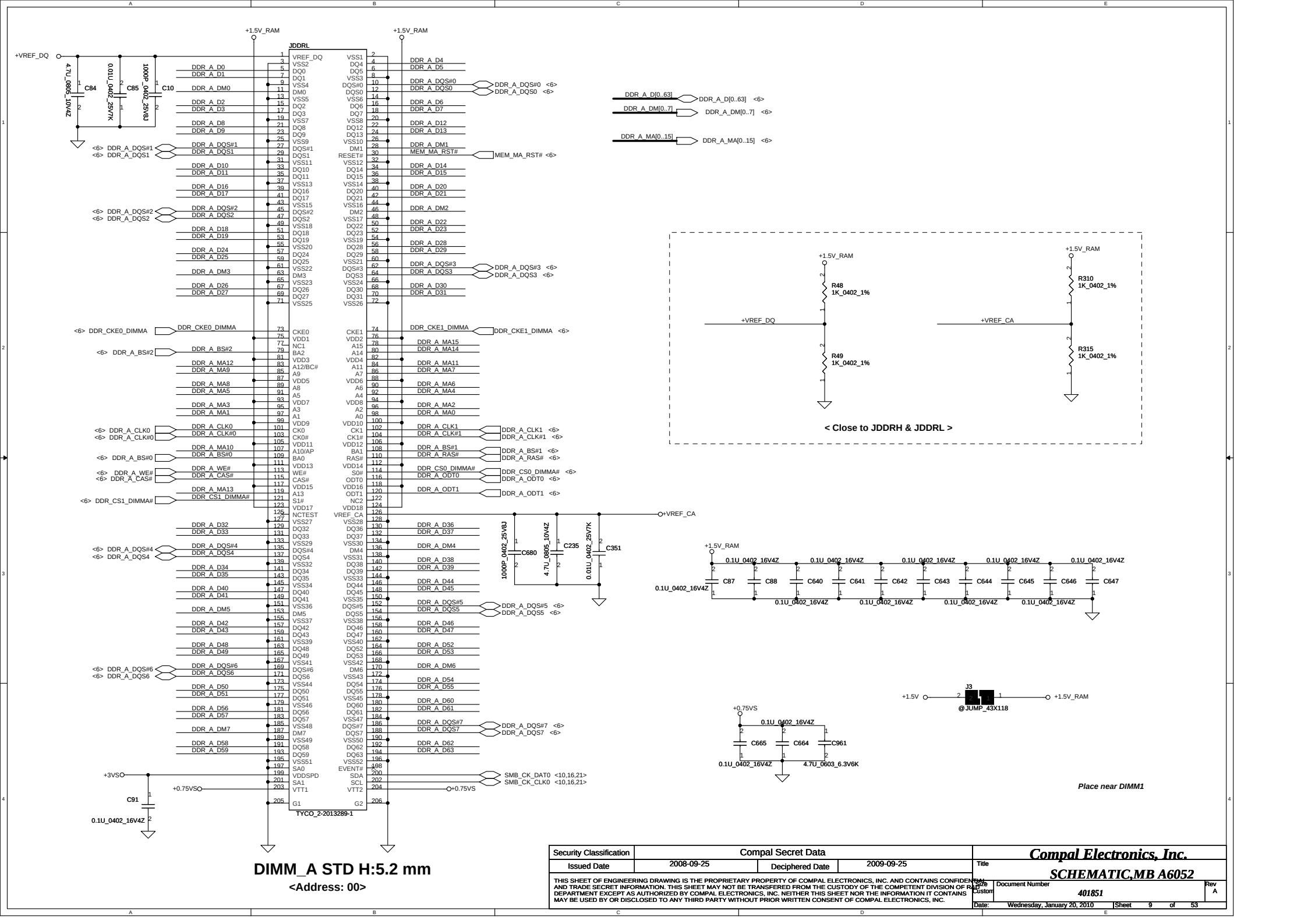

DIMM_A STD H:5.2 mm

<Address: 00>

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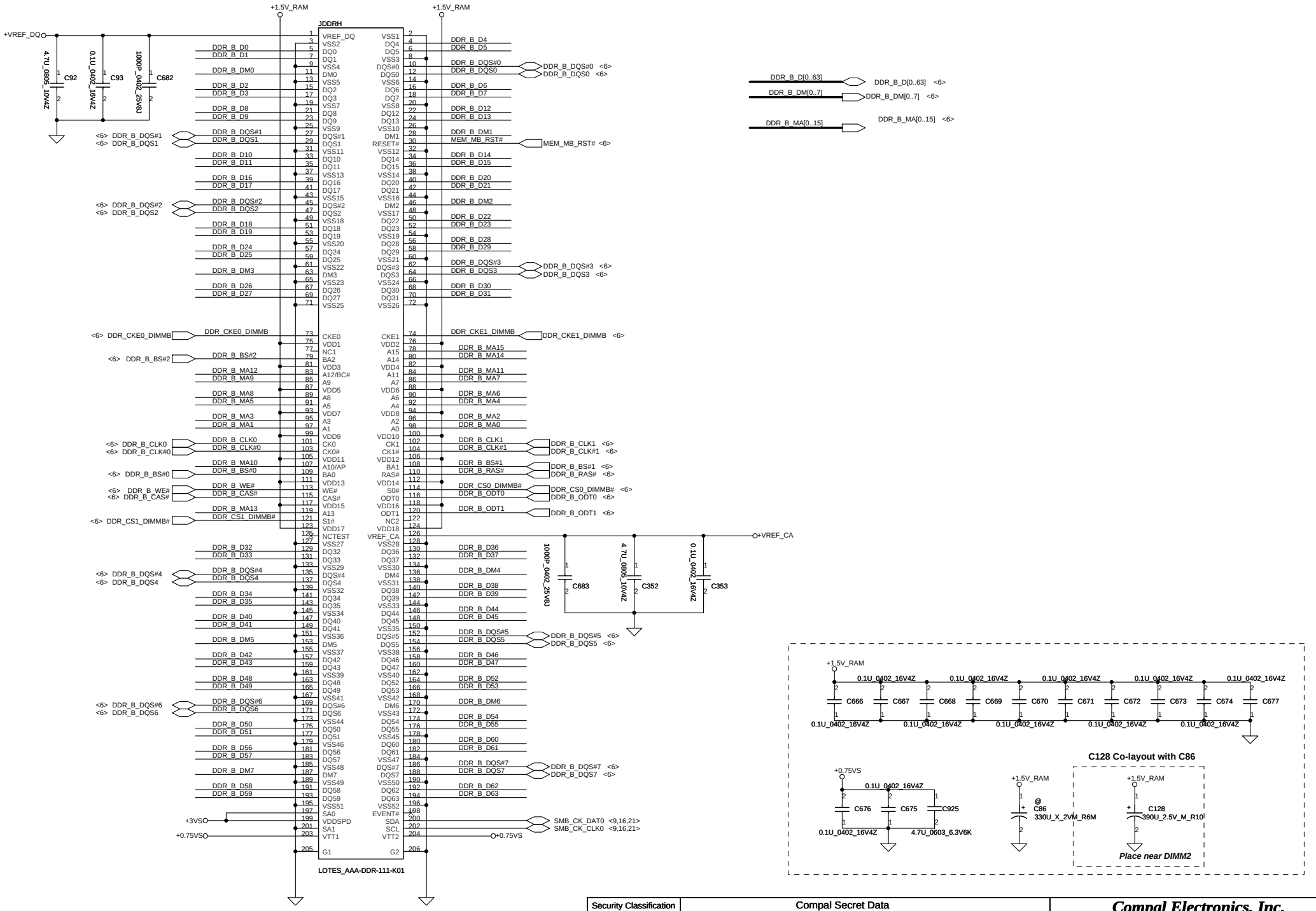

DIMM_B STD H:9.2 mm

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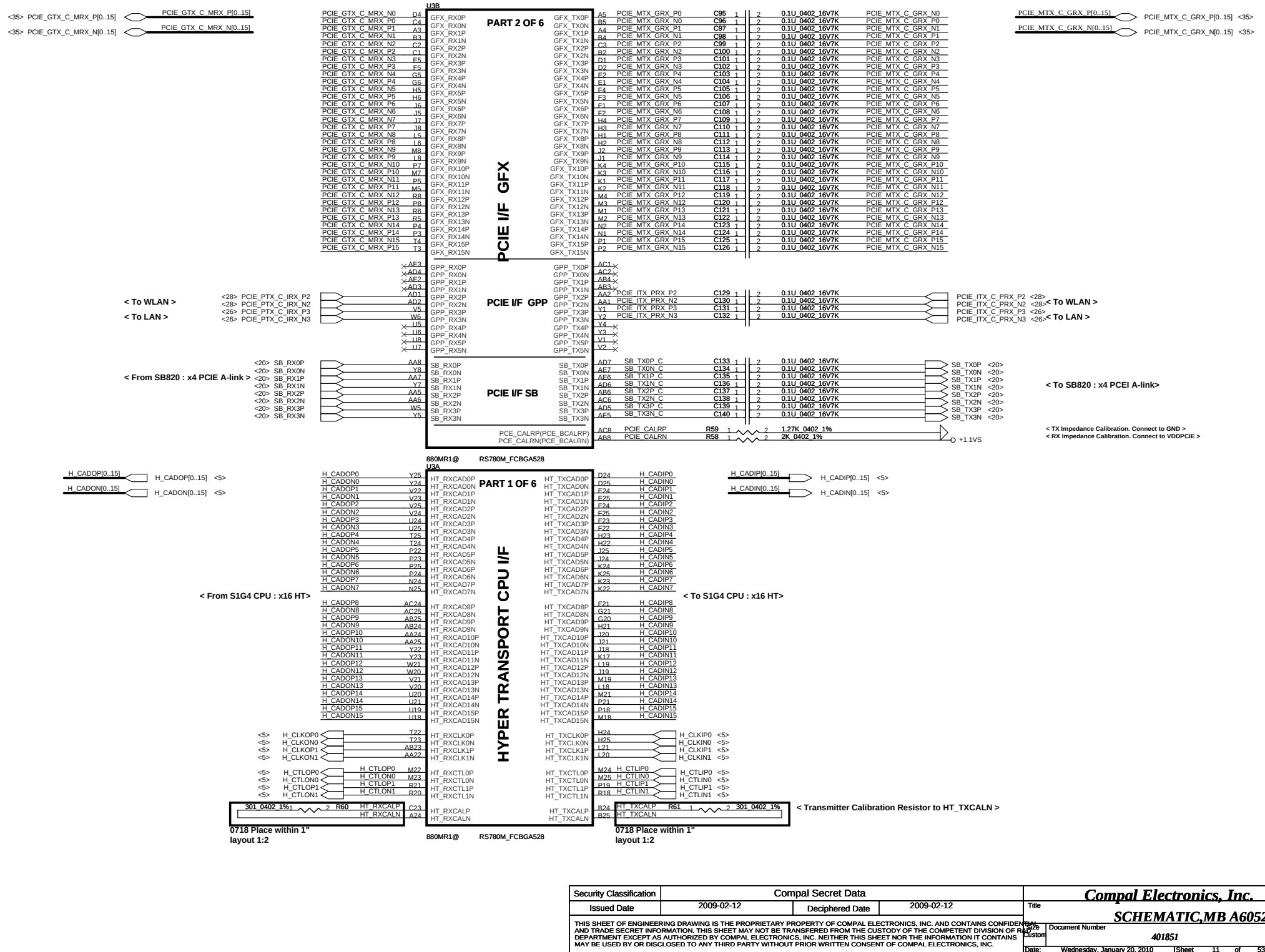

Security Classification	Compal Secret Data		
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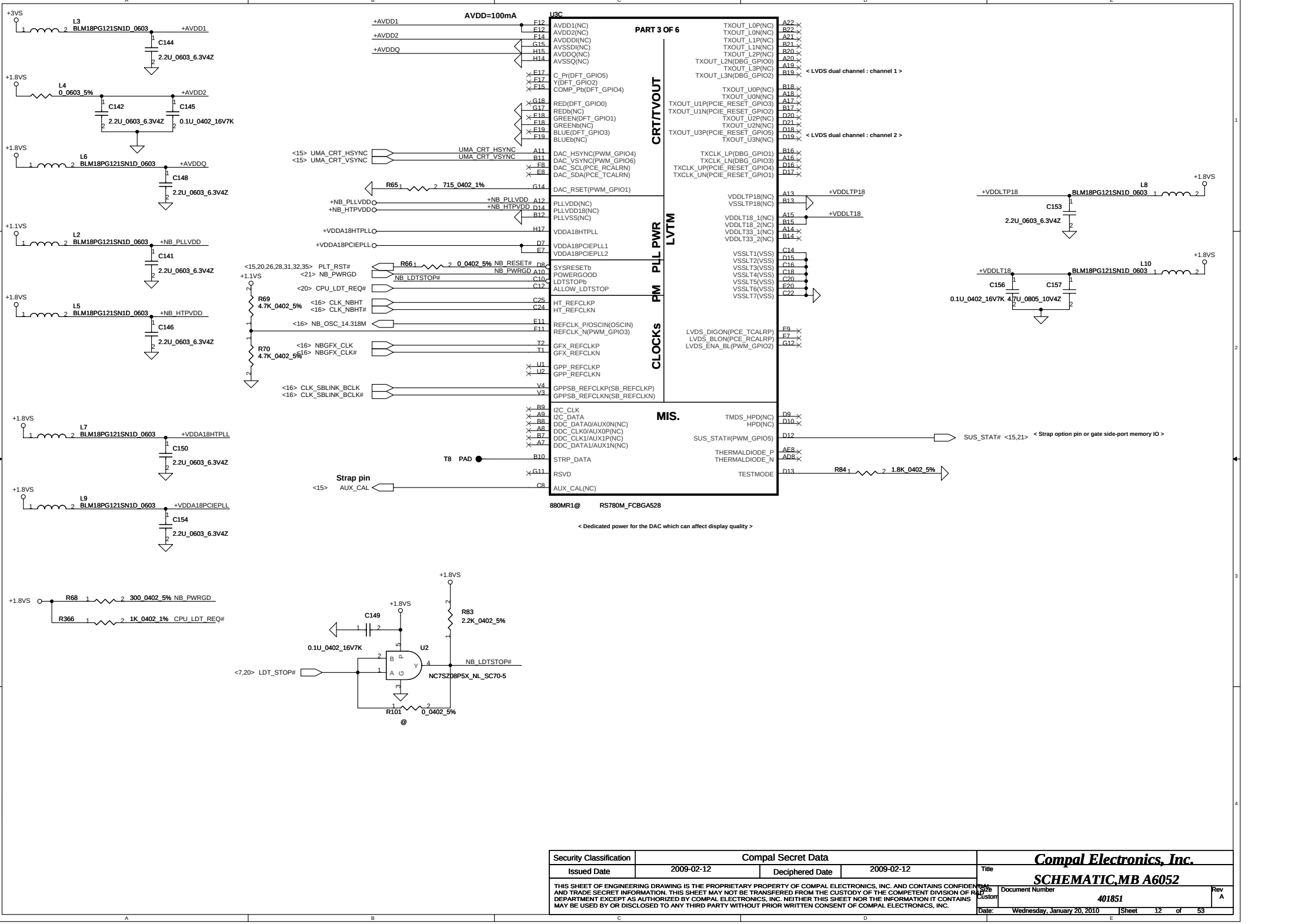

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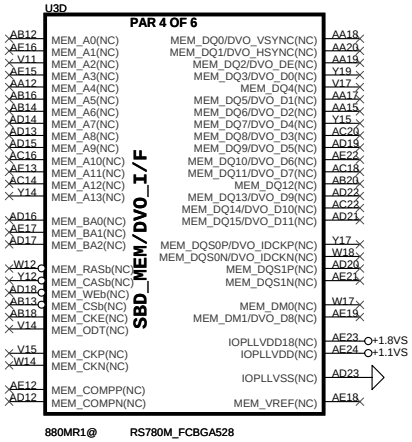

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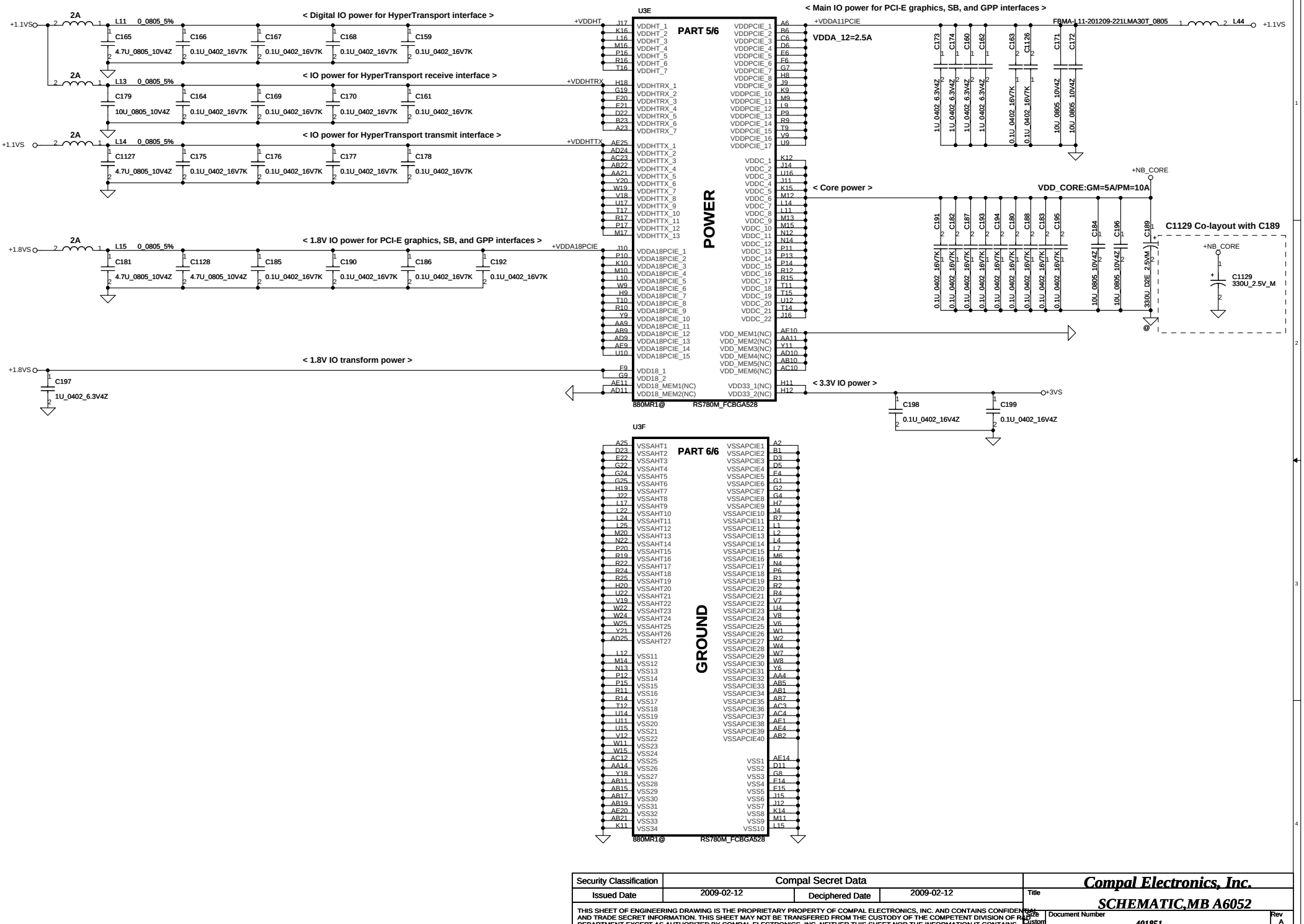

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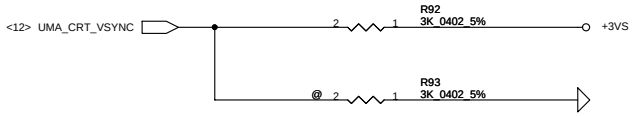
< RS880 VSYNC mux at CRT_VSYNC pull High to 3K >



< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Disable (RX881, RS880)
0 : Enable (RX881, RS880)

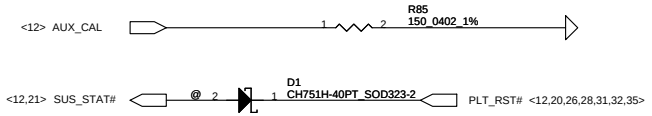
PIN: RS880--> VSYNC#

< RS880 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS880 SUS_STAT# >



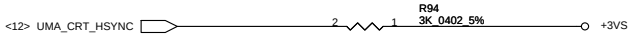
< SUS_SATA# : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS880:SUS_STAT#

< RS880 use HSYNC to enable SIDE PORT (internal pull high) >



< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb >

RX881: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS880: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS880)
0 : Enable (RS880)

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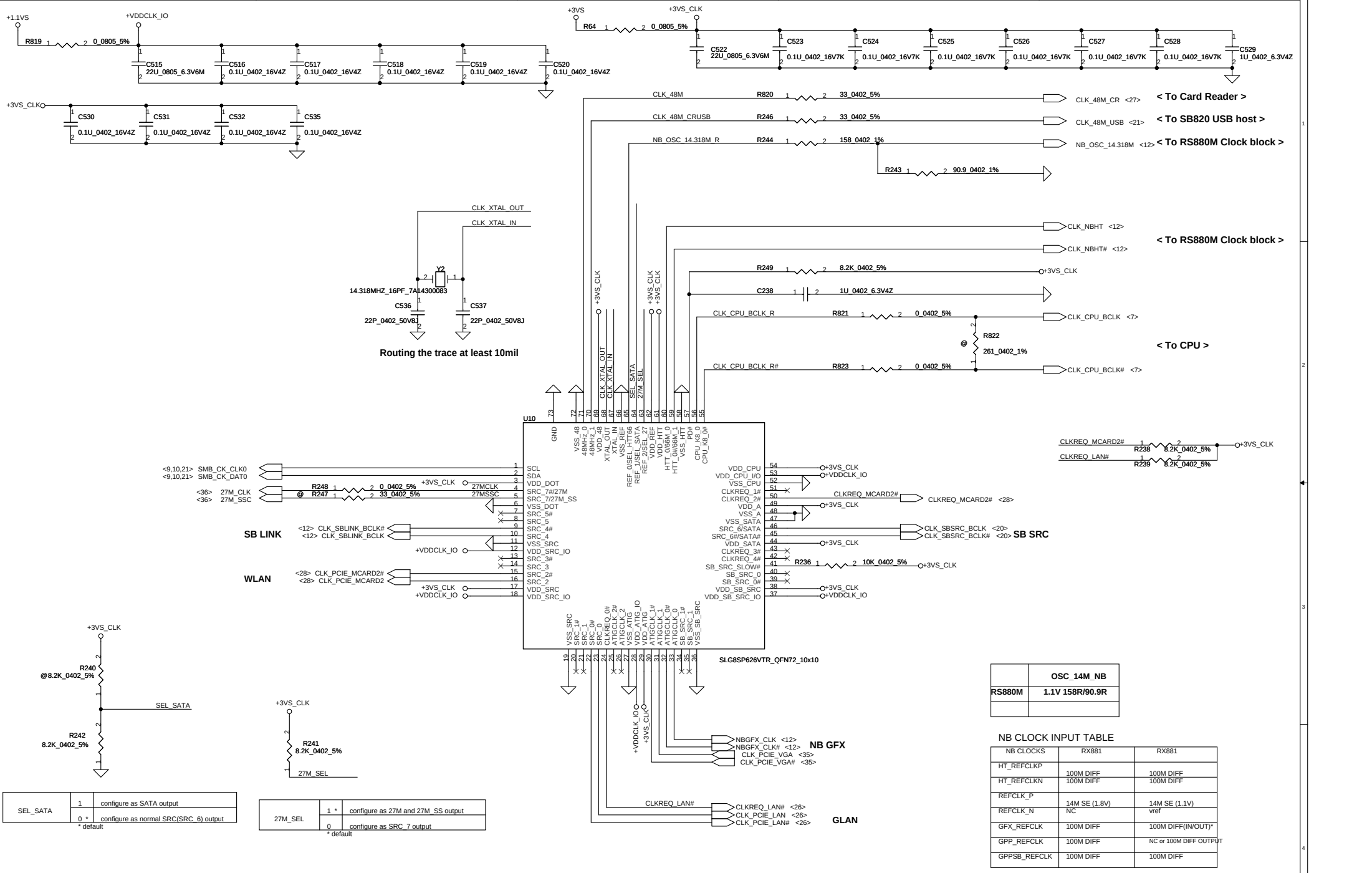

	OSC_14M_NB
RS880M	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RX881	RX881
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

SEL_SATA		
	1	configure as SATA output
	0 *	configure as normal SRC(SRC_6) output

* default

27M_SEL		
	1 *	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

* default

Use voltage divider resistor R243 & R244 to pull low

NB_OSC_14.318M		
	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output

* default

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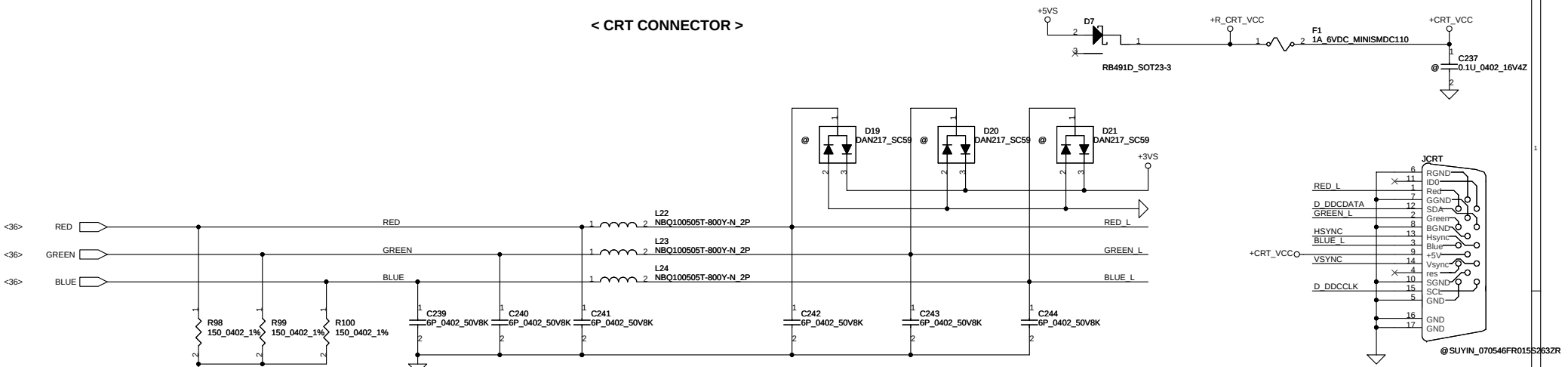
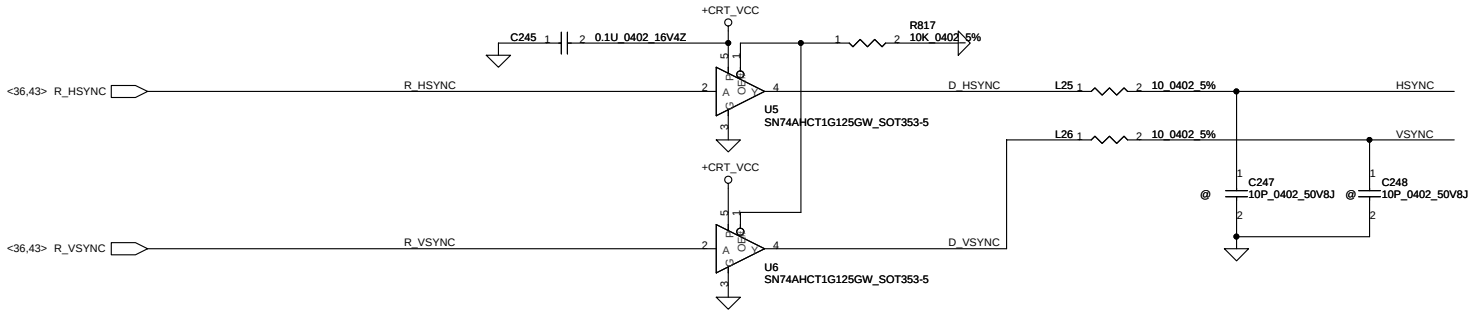
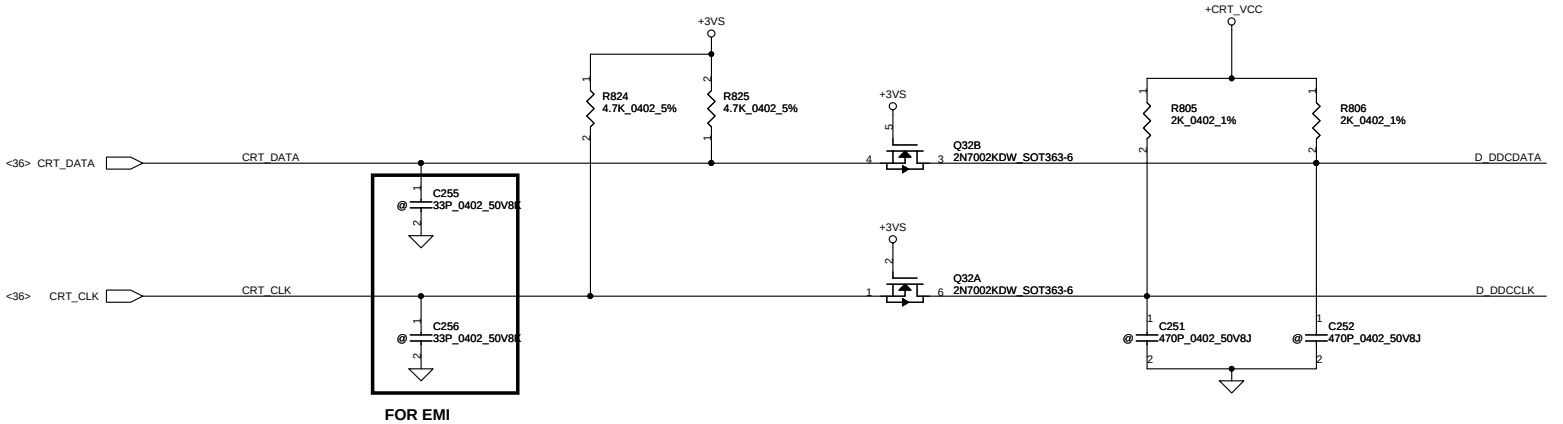
< CRT CONNECTOR >



< SYNC SIGNAL >



< Display Data Channel >



FOR EMI

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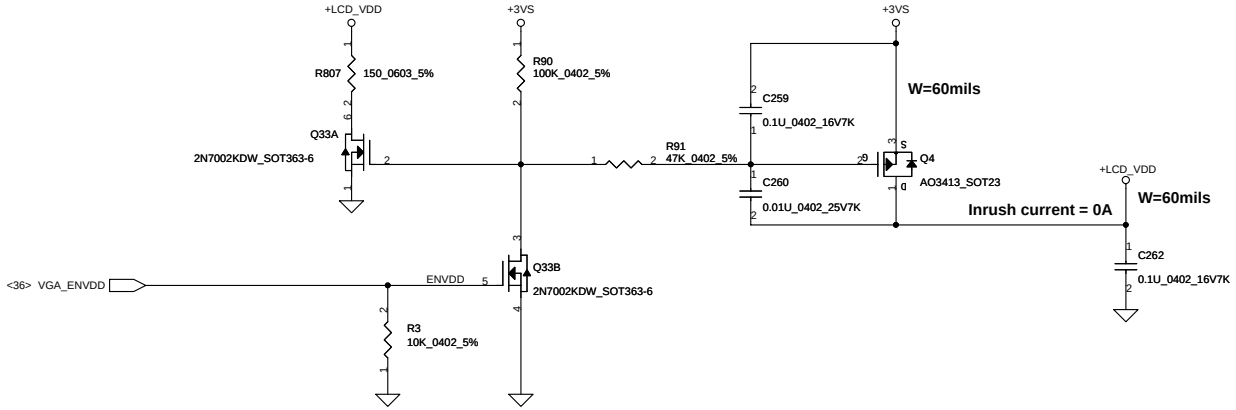
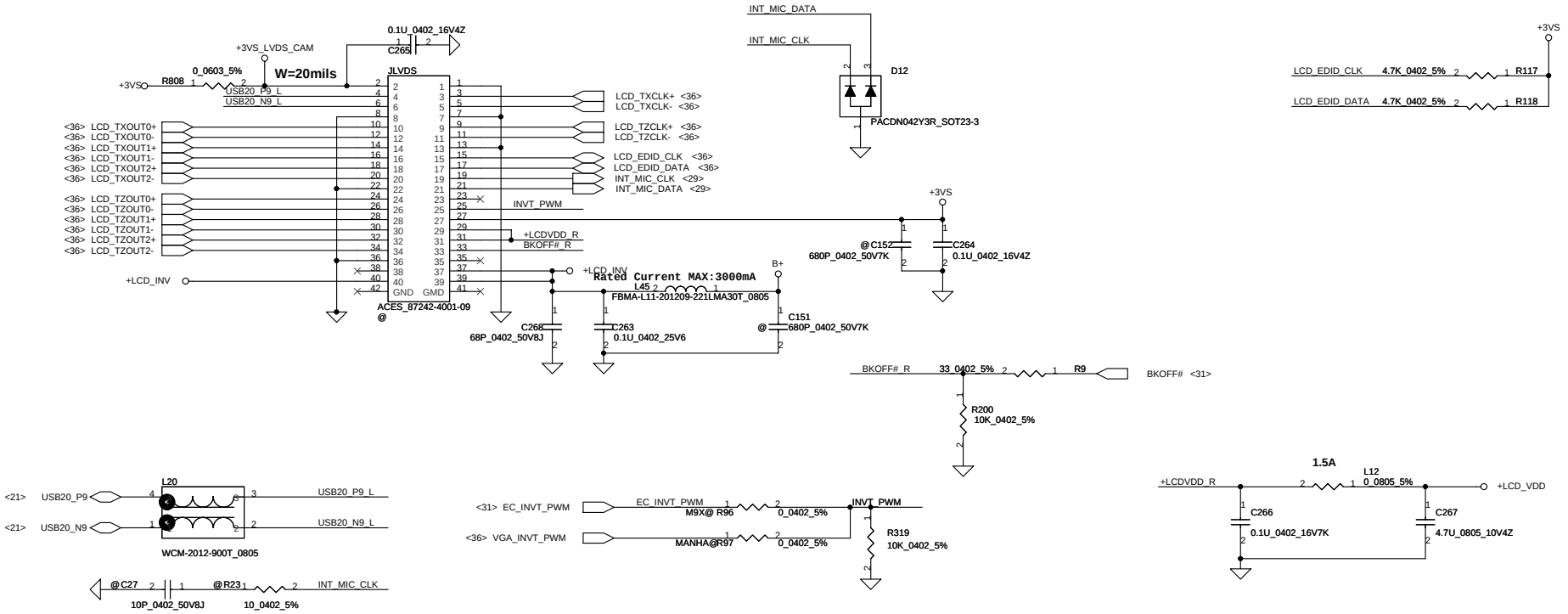
LCD/PANEL BD. Conn.



< LVDS Connector >



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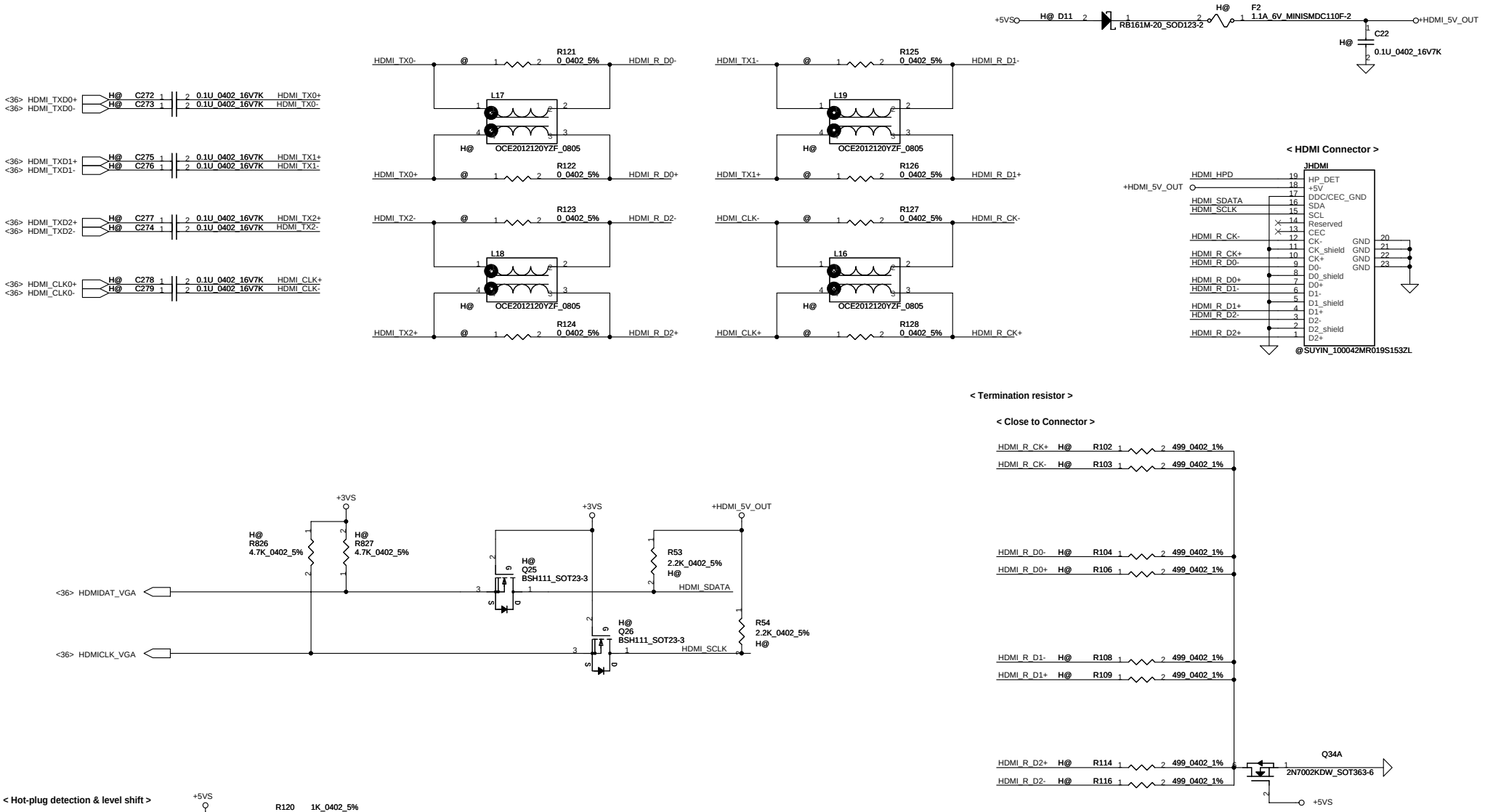

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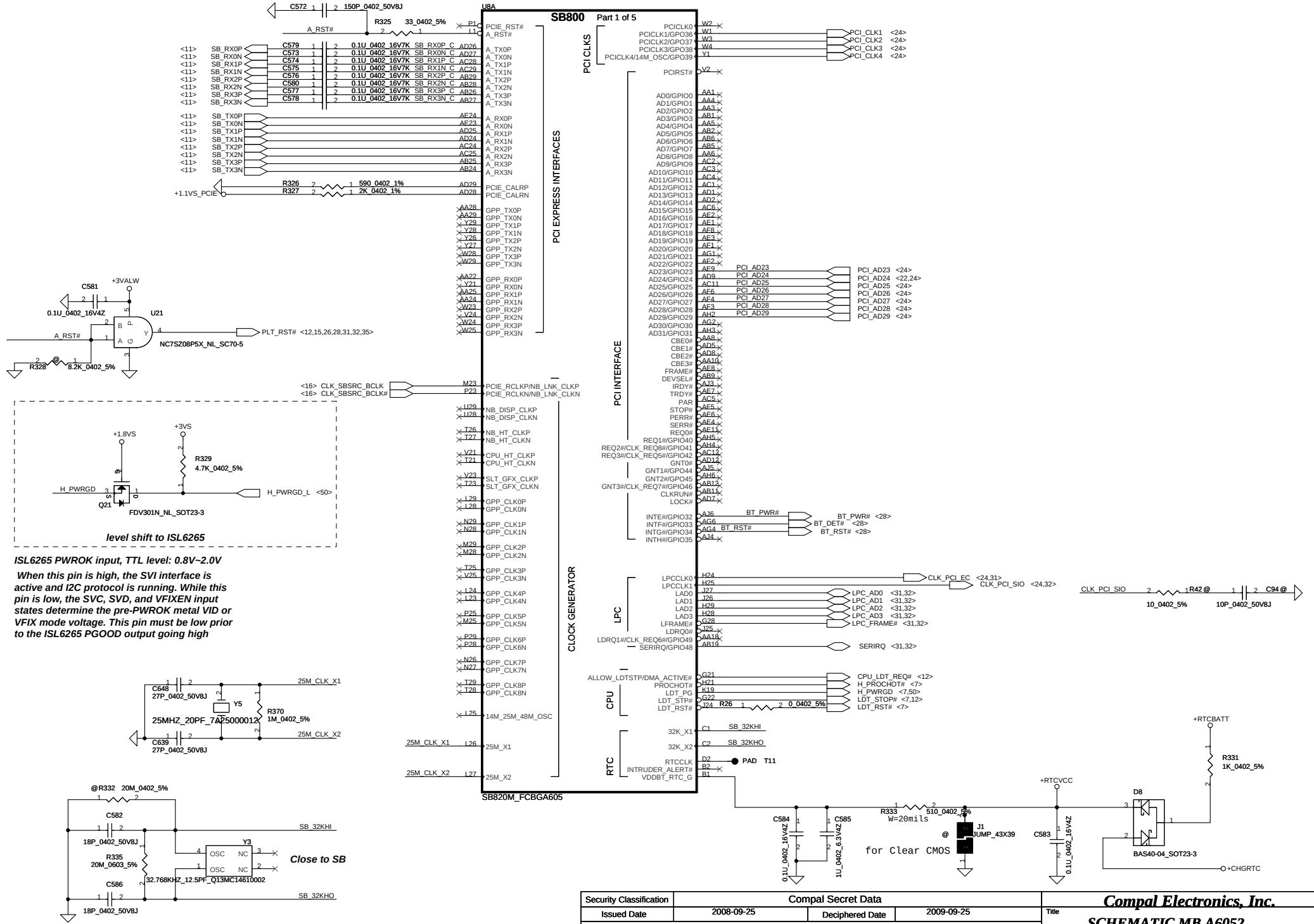

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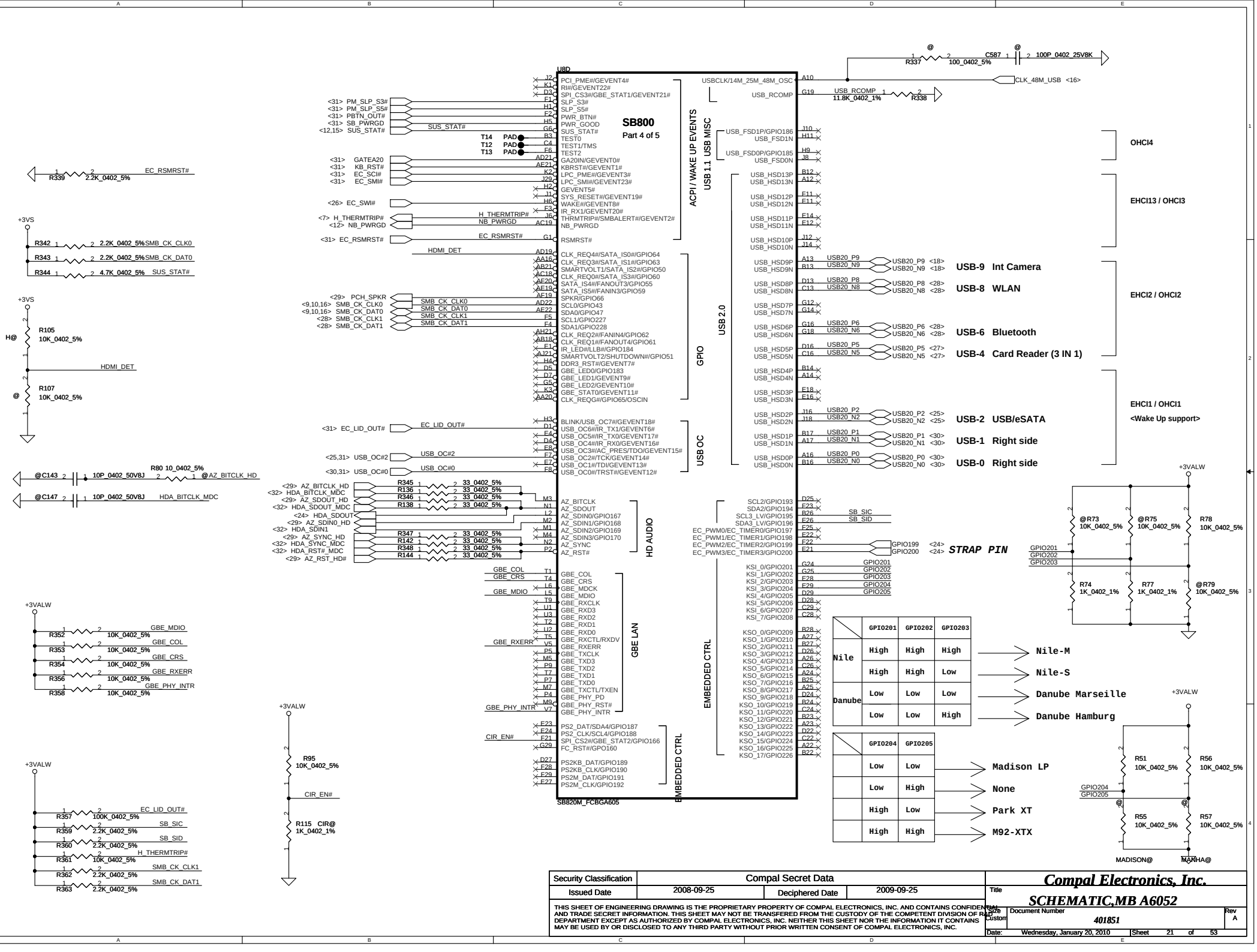

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Compal Electronics, Inc.

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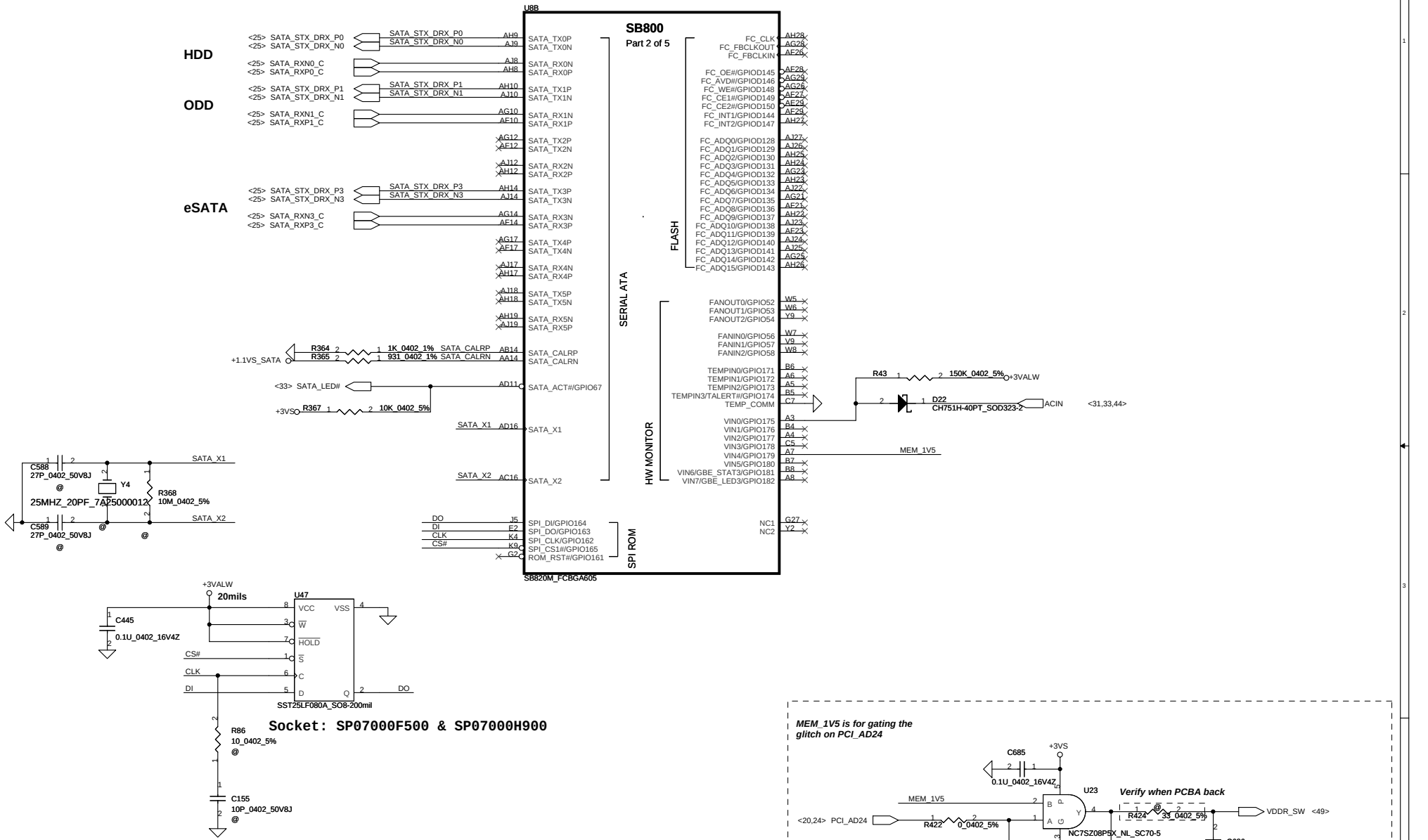

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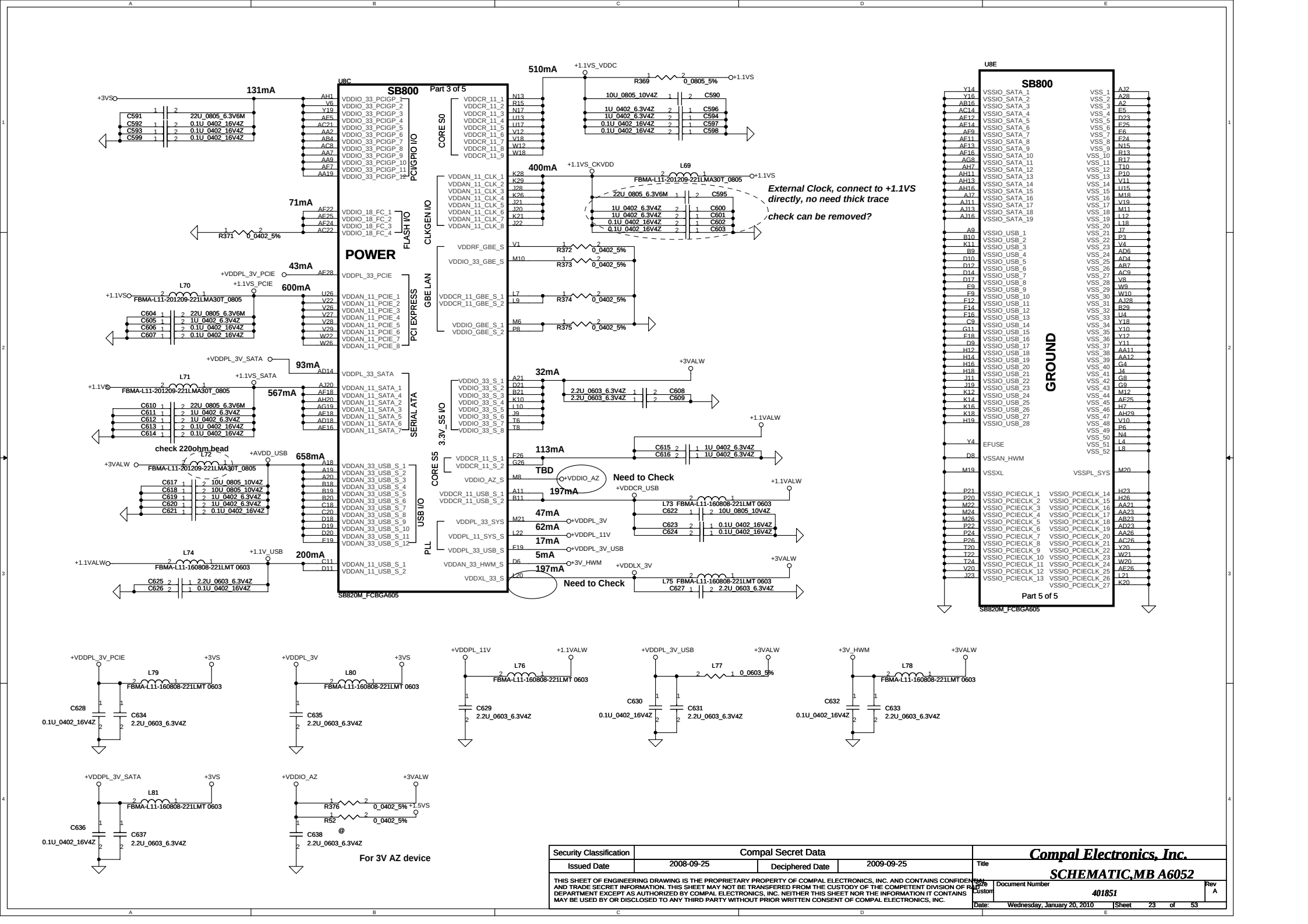

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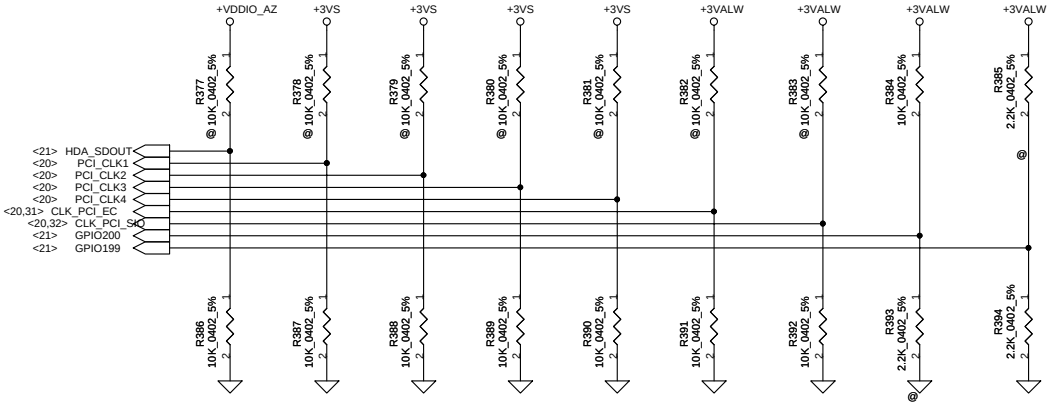
REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved **H,L = SPI ROM (Default)**
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable DEFAULT	EC DISABLE DEFAULT	CLOCKGEN DISABLE DEFAULT		L,H = LPC ROM L,L = FWH ROM



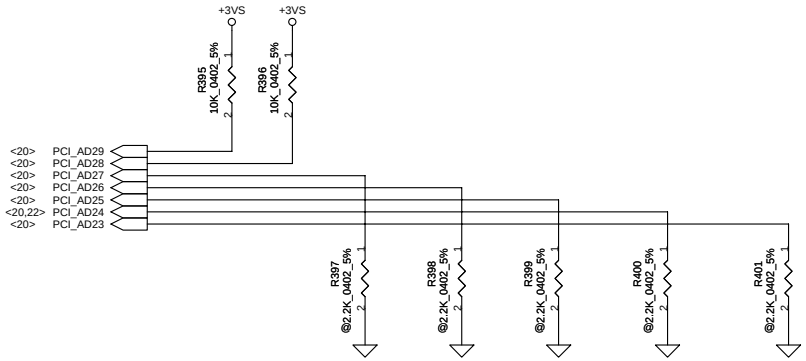
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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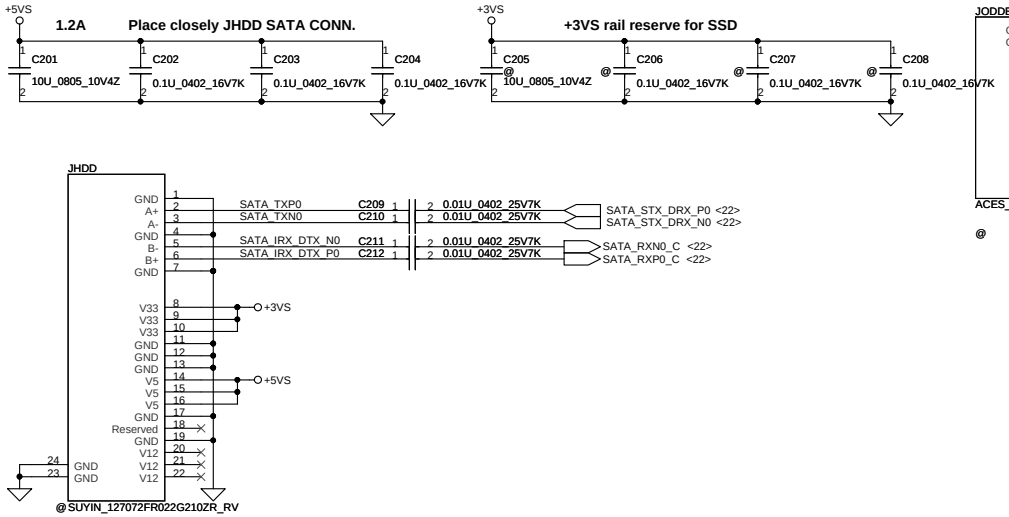
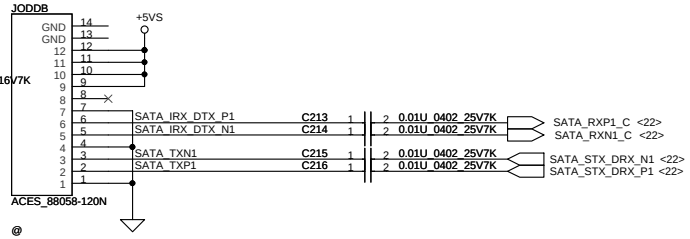
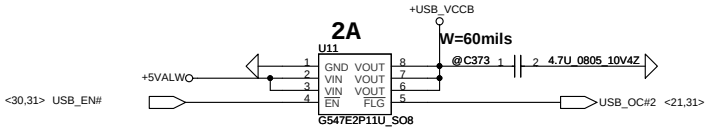
< SATA HDD Conn >

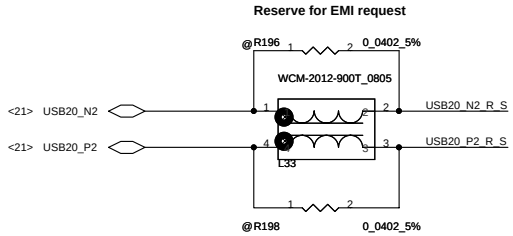


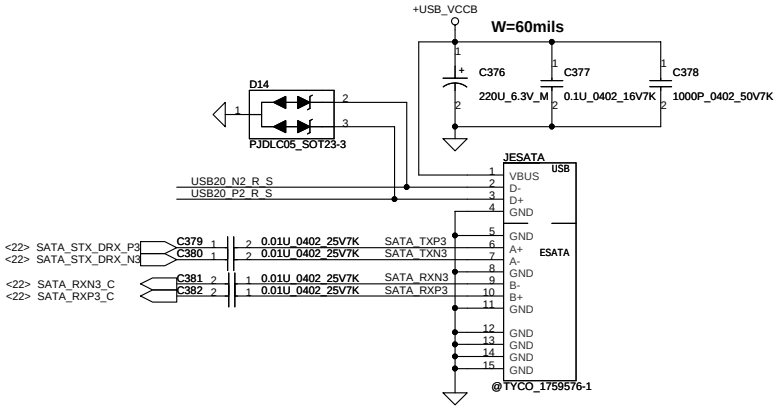
< SATA ODD Conn >



eSATA/USB Conn







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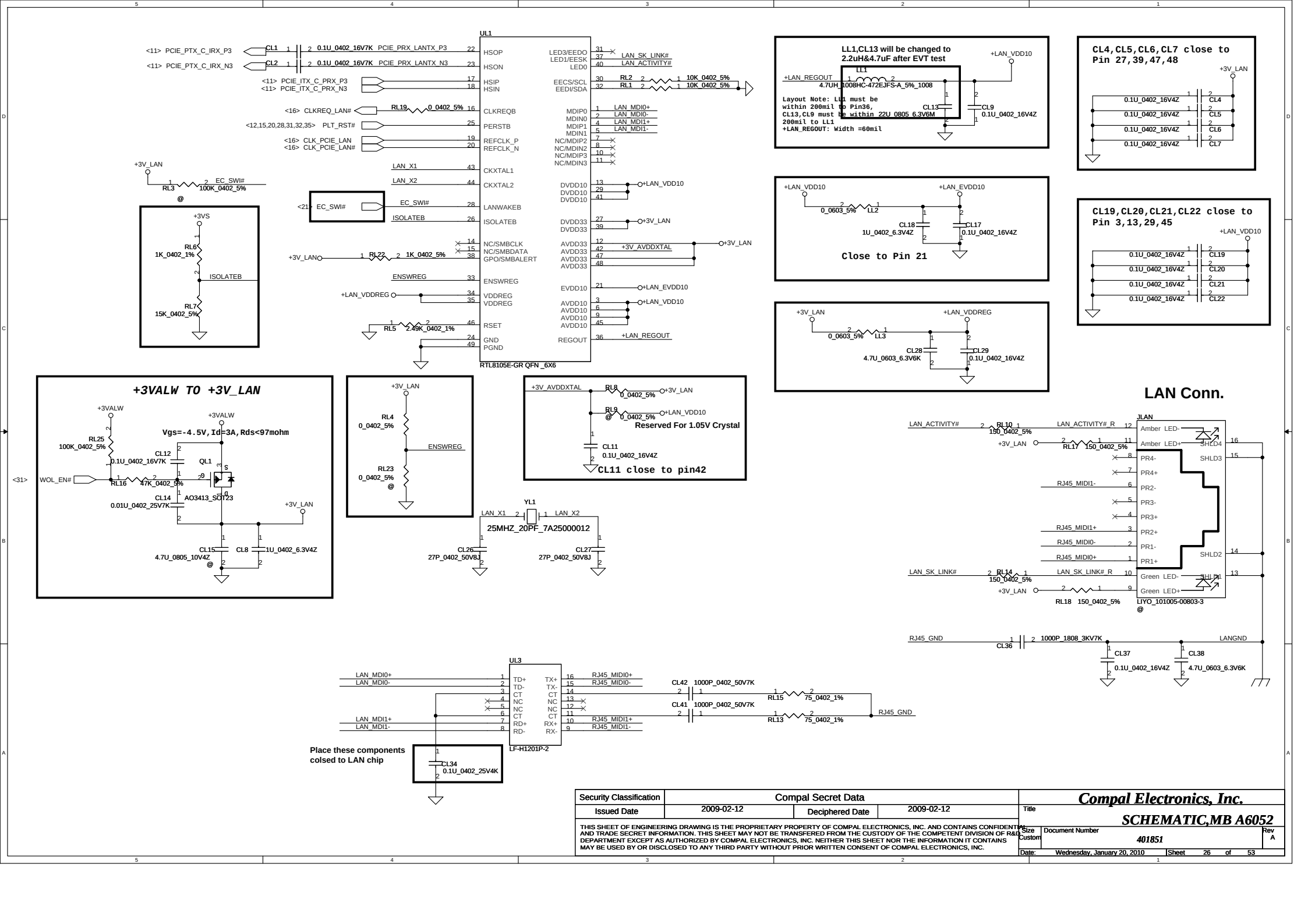

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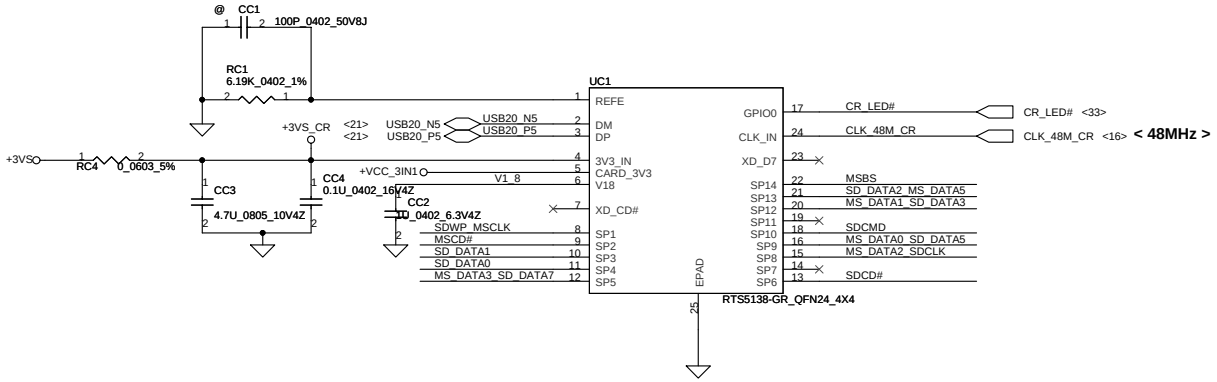
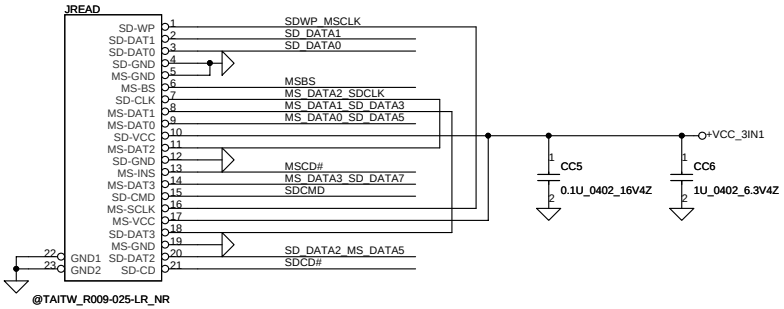
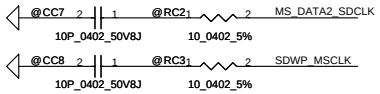


< 3 in 1 Card Reader >





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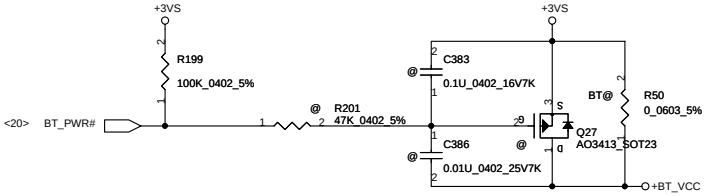
< BlueTooth Interface, USB port6 >

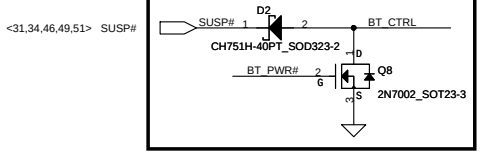


Inrush current = 0A

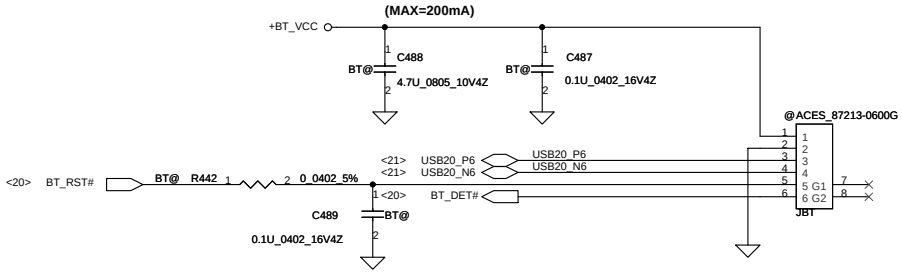
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

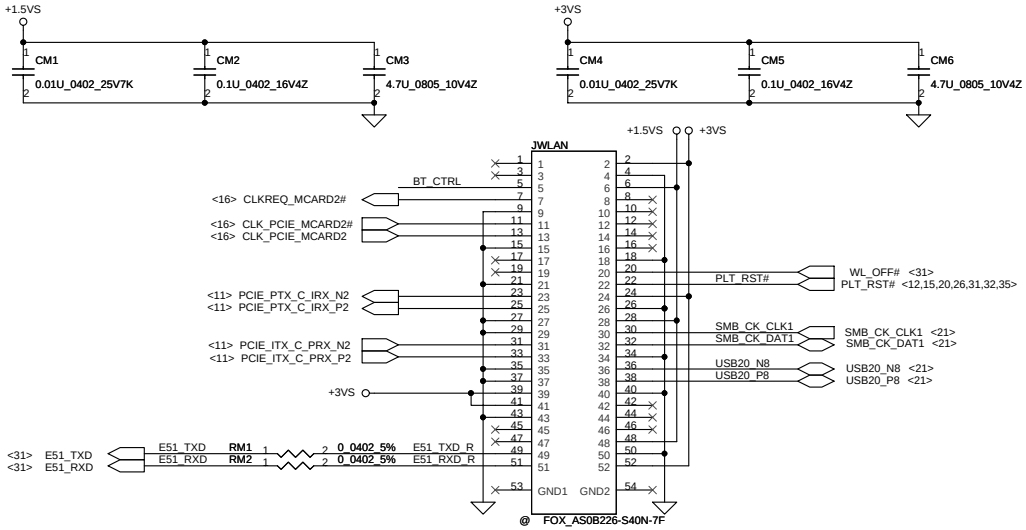
**If +3V_WLAN is +3VS, please remove D21.



< Bluetooth Connector >



< PCIe Mini Card for WLAN >



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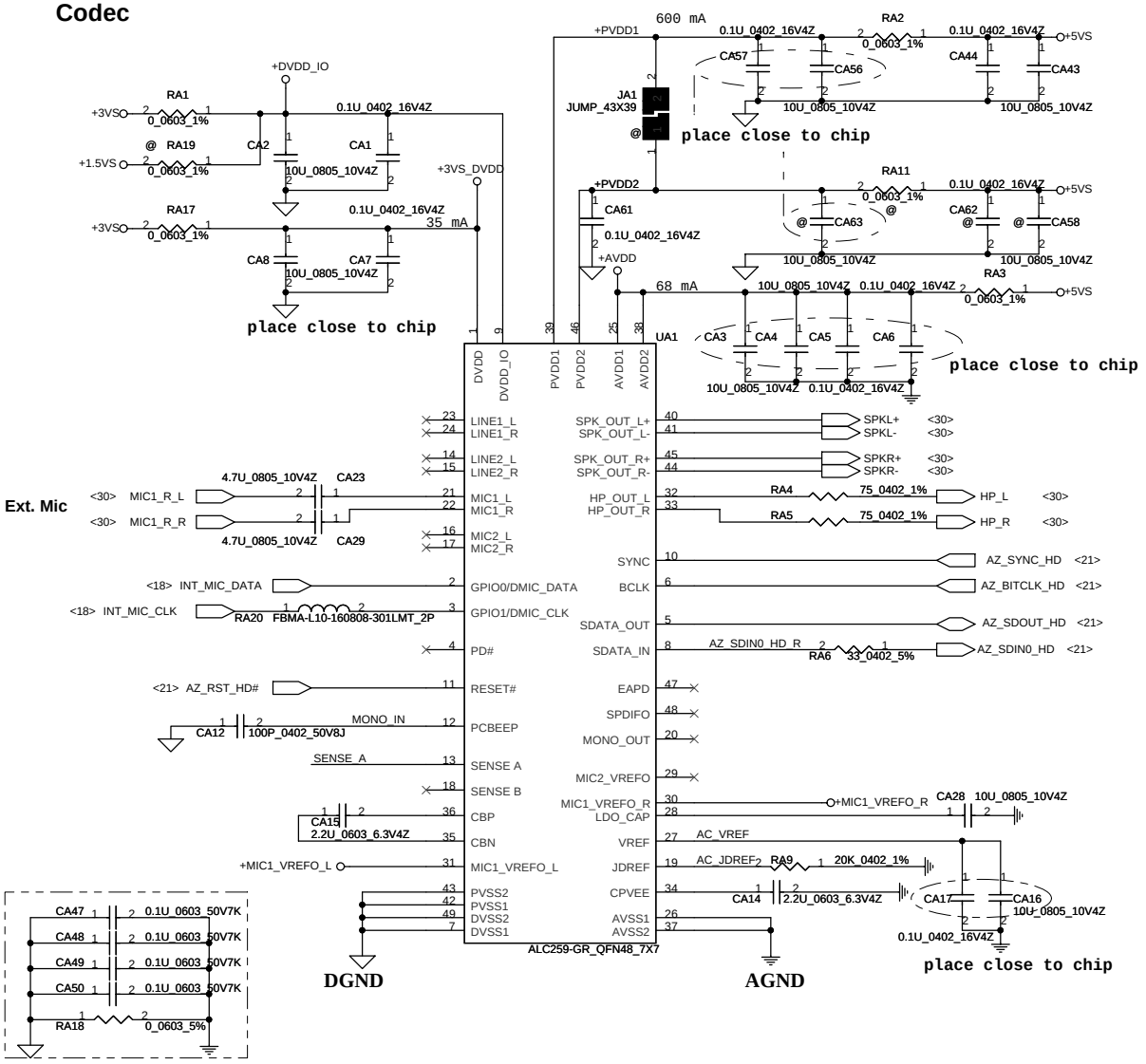
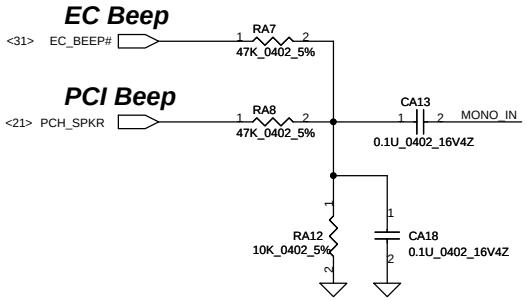
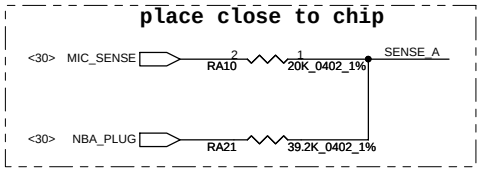
Codec



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



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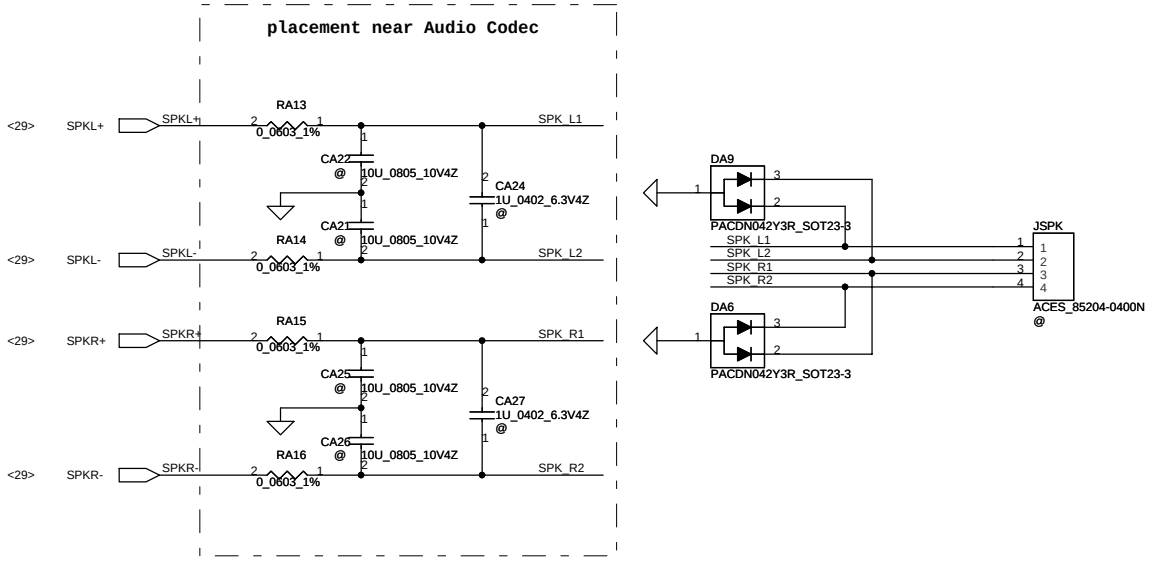
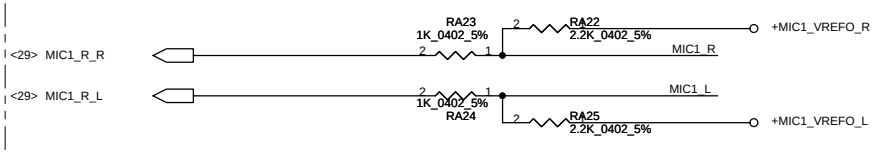
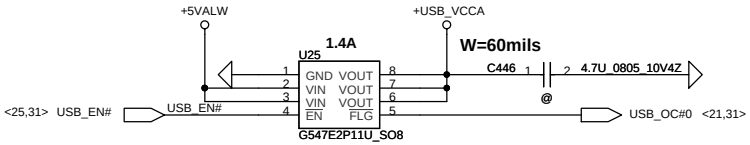
Speaker Connector

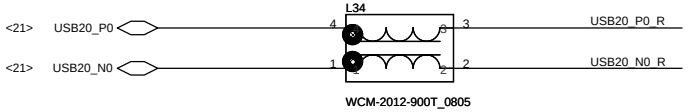


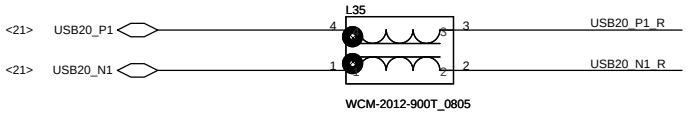
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK

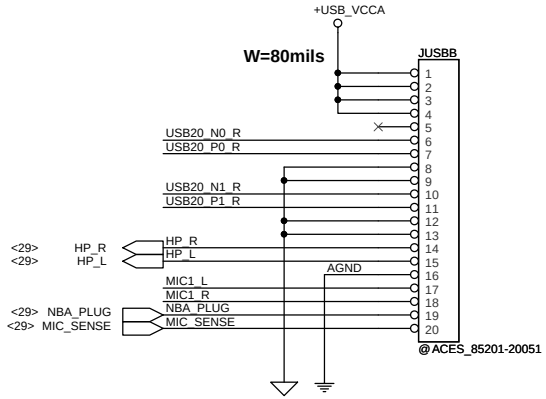








Audio & USB Sub-Board Conn.



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Compal Electronics, Inc.			
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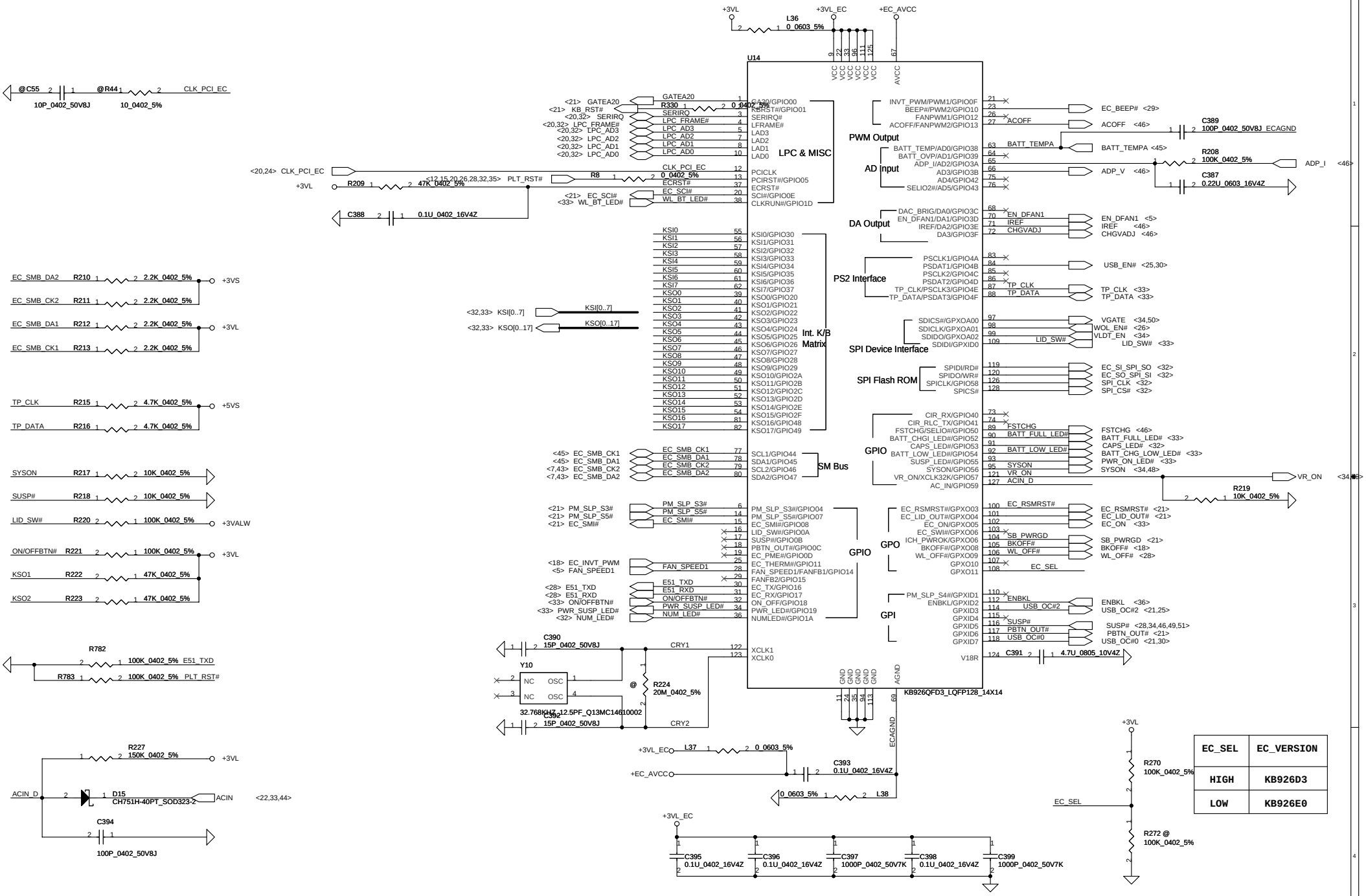

EC_SEL	EC_VERSION
HIGH	KB926D3
LOW	KB926E0

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

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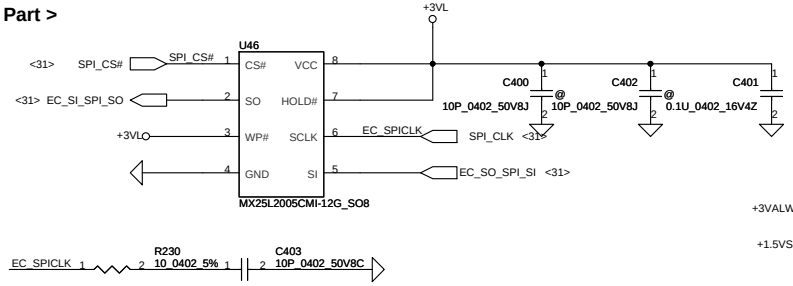
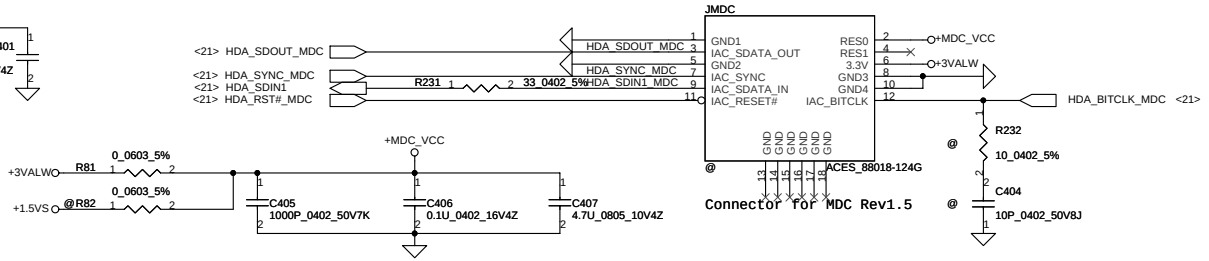
< ROM Part >

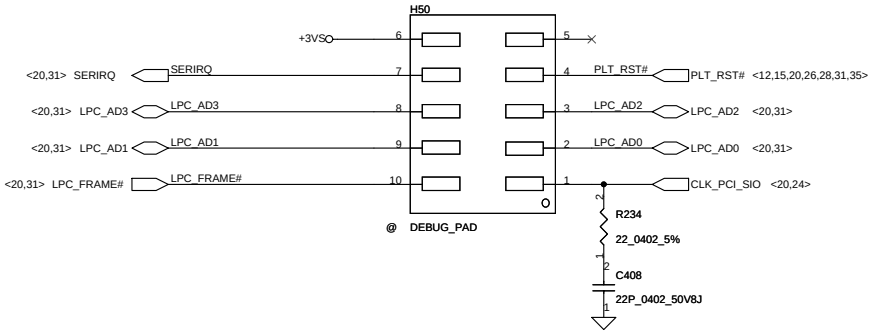


< MDC 1.5 Conn >



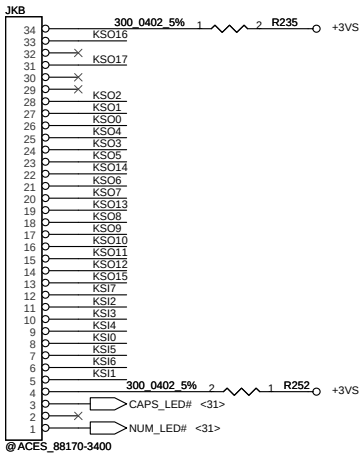
< LPC Debug Port >

Please place the PAD under DDR DIMM.

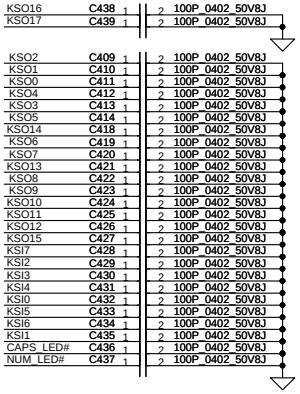


< KEYBOARD Conn >

KSI[0..7] KSI[0..7] <31,33>
KSO[0..17] KSO[0..17] <31,33>



< For EMI >



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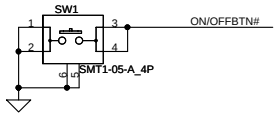
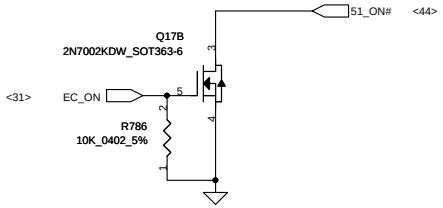
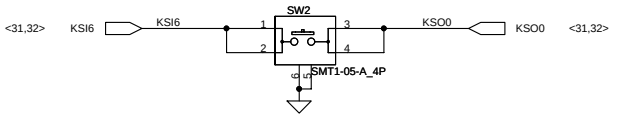
< Power Button for Debug >



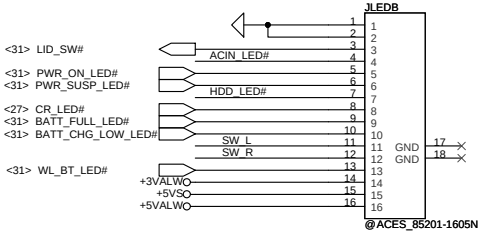
< Power Button Circuit >

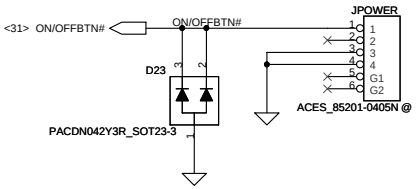


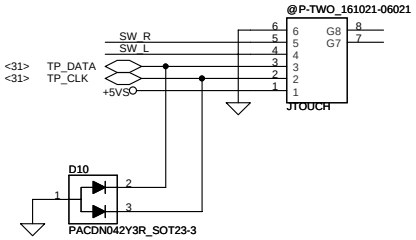
< TP on & off BTN on M/B>

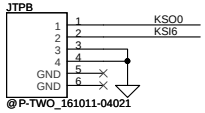


Sub-B Connector



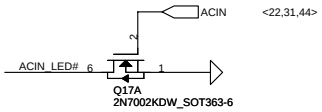




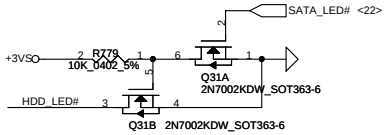


LED Circuit

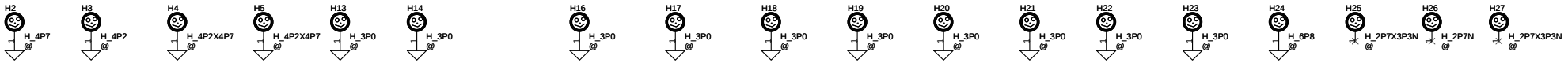
DC-IN LED

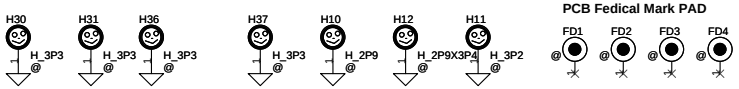


HDD LED



SCREW





PCB Fedical Mark PAD

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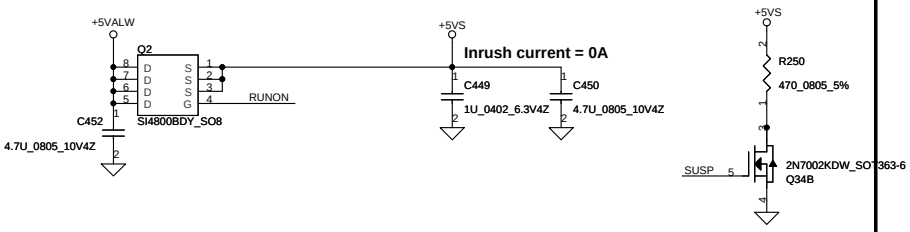
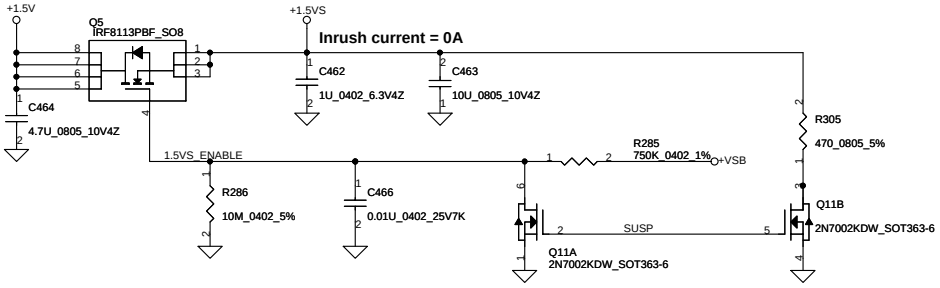
< +5VALW TO +5VS >



< +1.5V TO +1.5VS >



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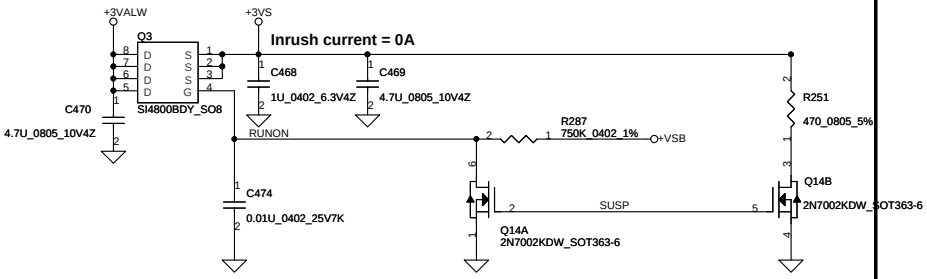

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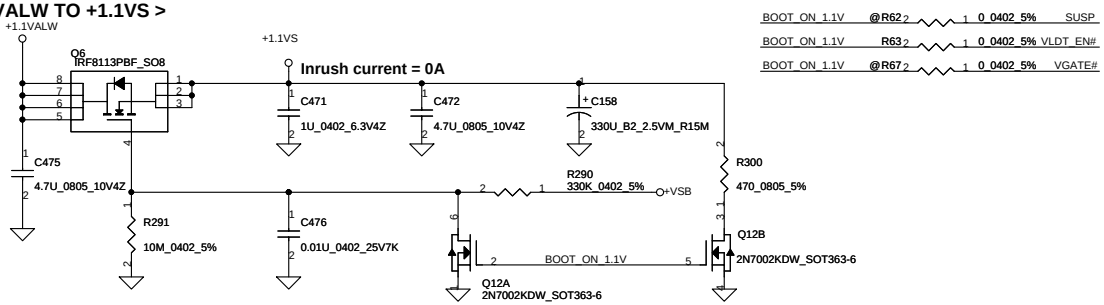

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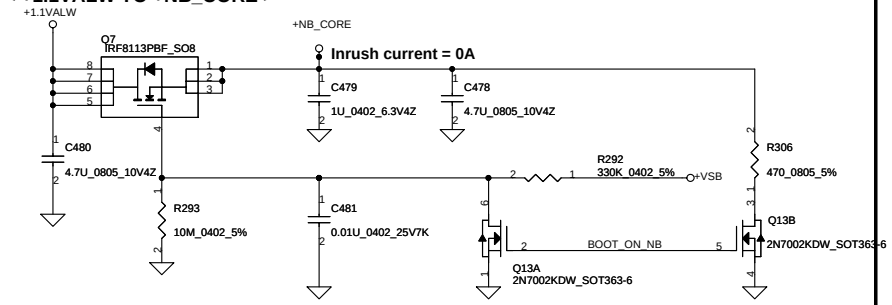
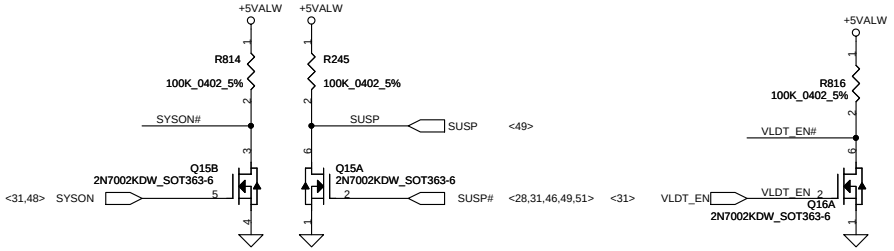
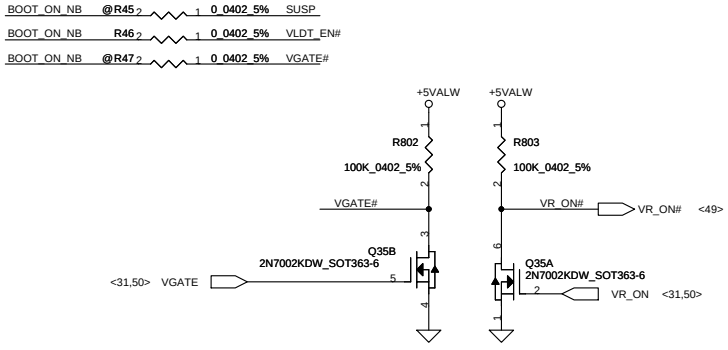
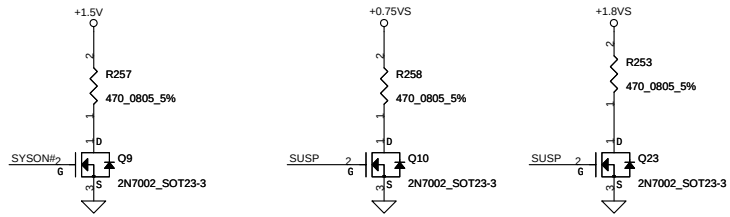


< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >





< Discharge circuit >



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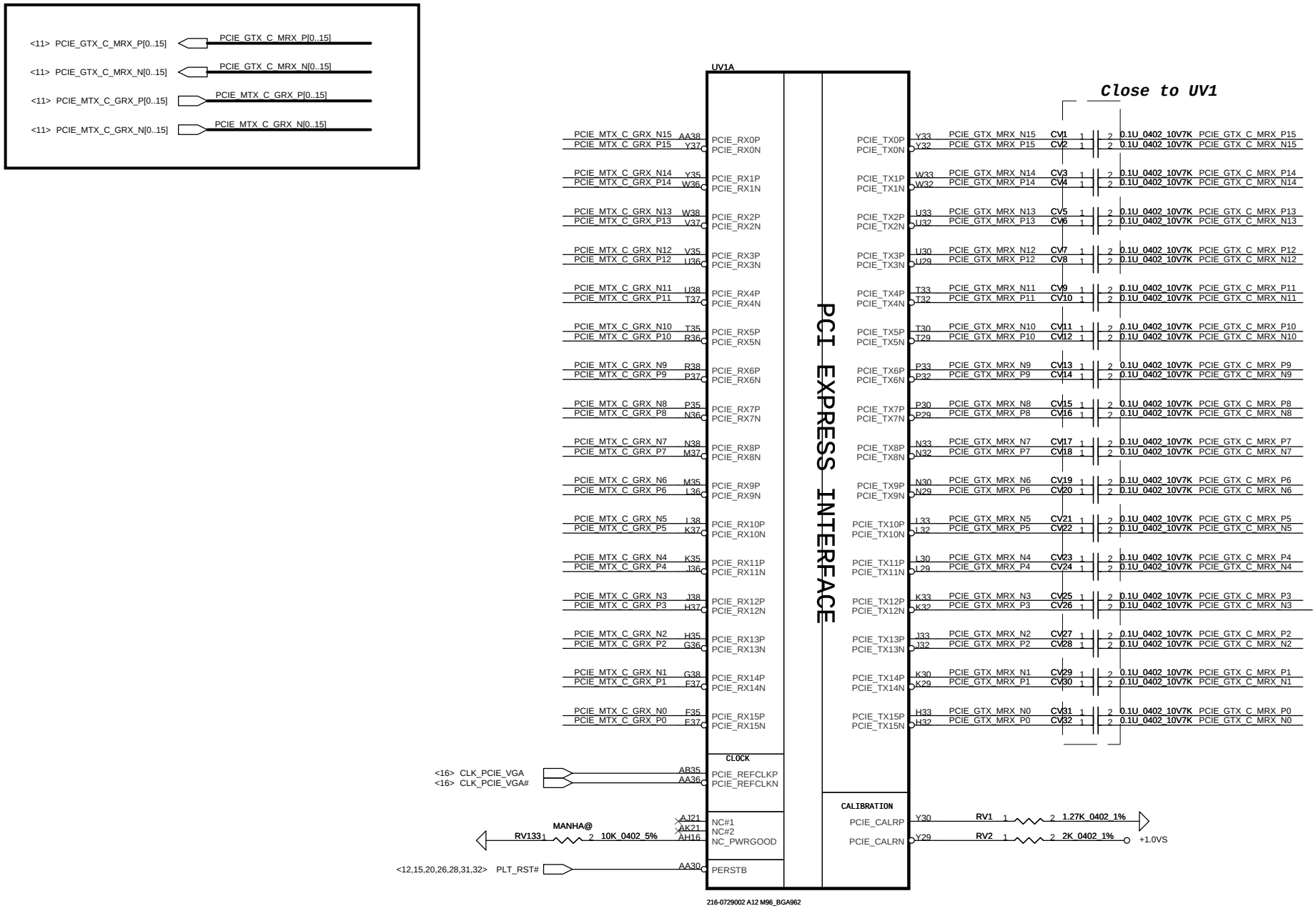

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.

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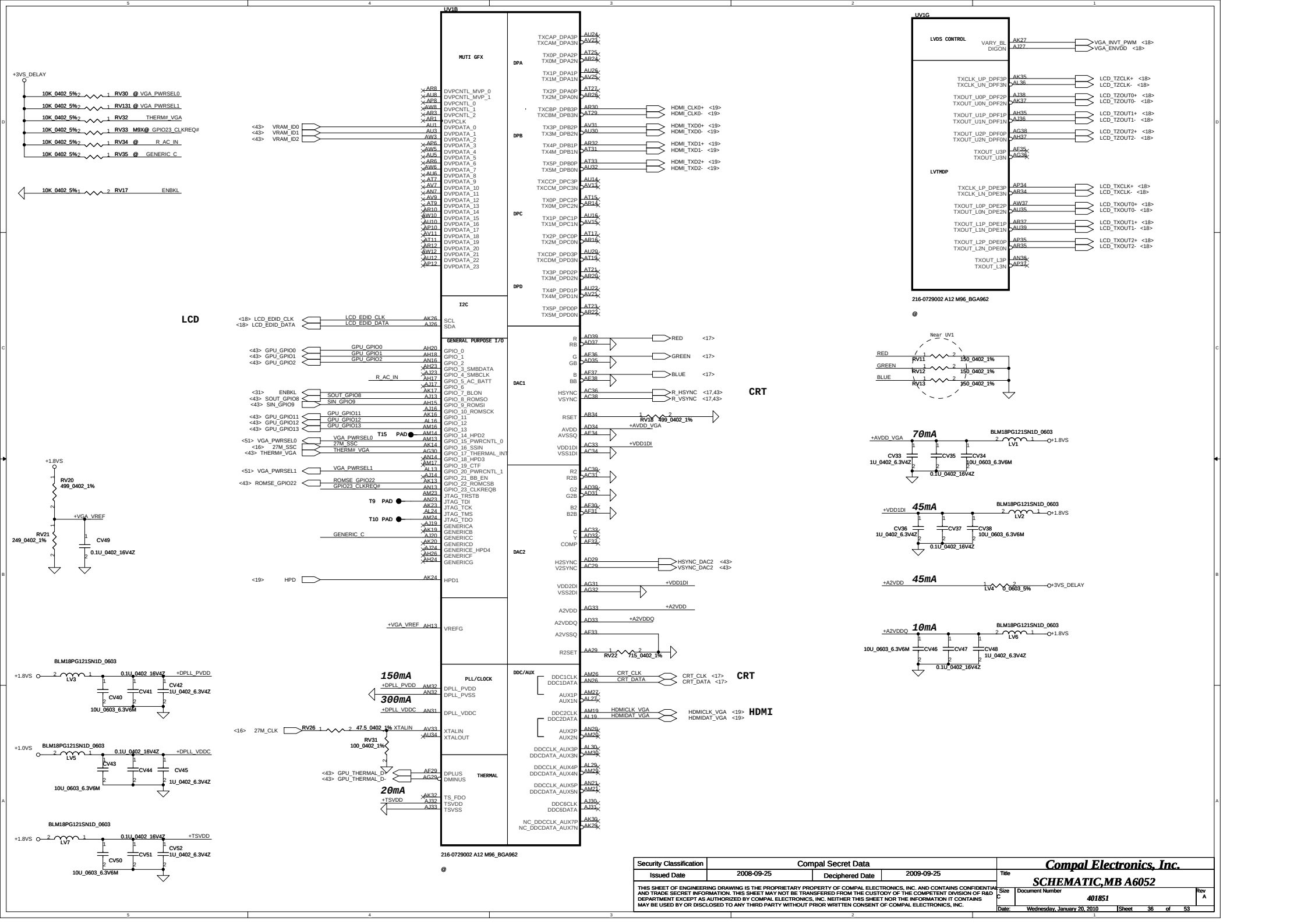

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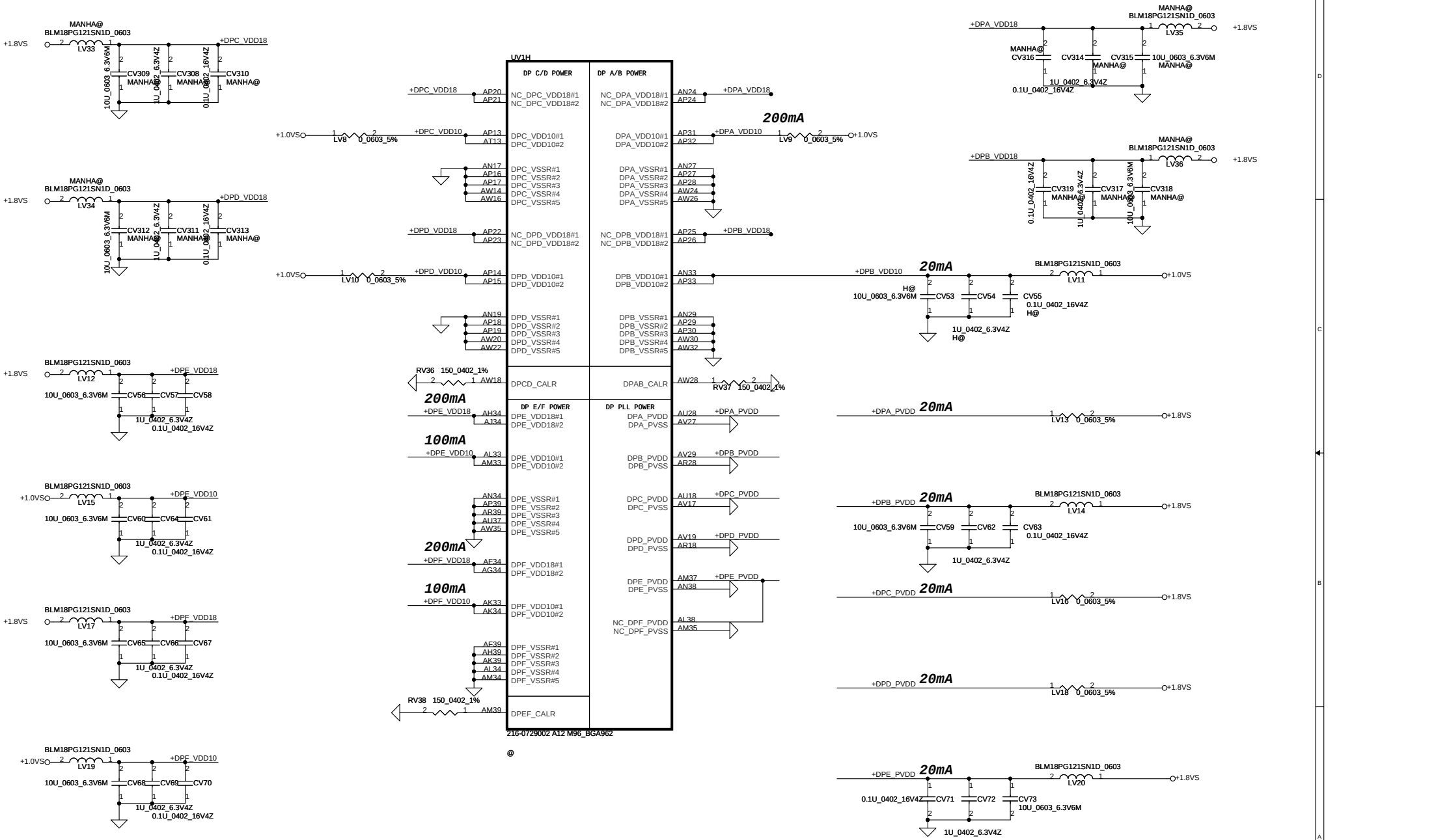

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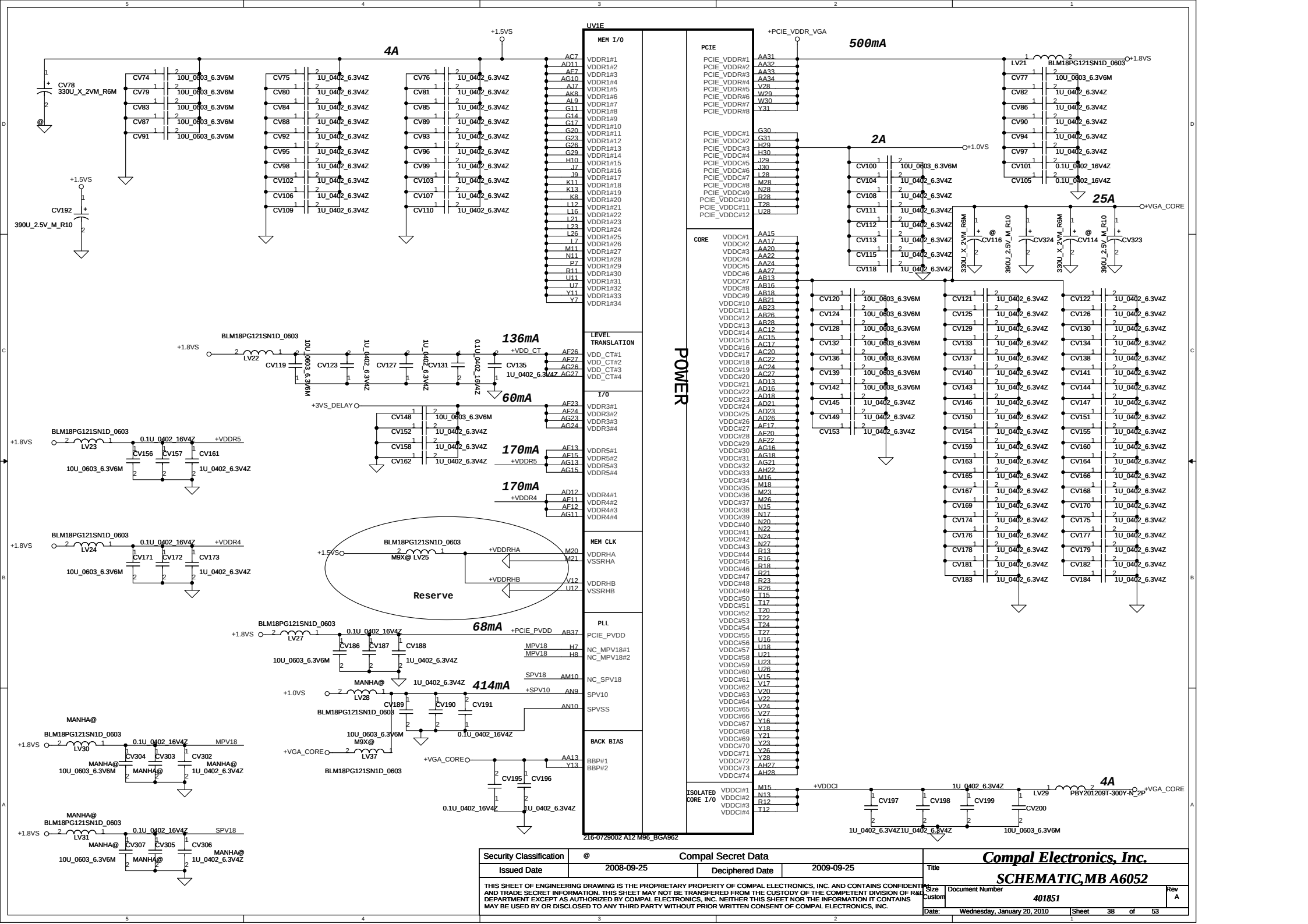

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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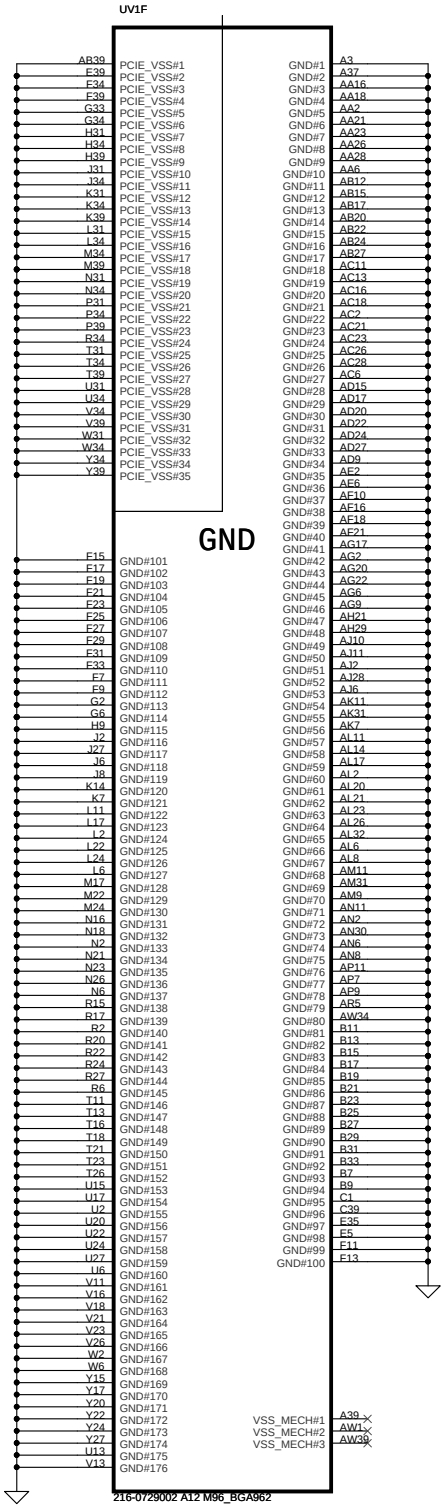

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MDA[0..63] MDA[0..63] <41>

MDB[0..63] MDB[0..63] <42>

Park uses memory group B only

UV1C

MEMORY INTERFACE A

UV1D

MEMORY INTERFACE B

MAA[13..0] MAA[13..0] <41>

A_BA[2..0] A_BA[2..0] <41>

DQMA#[7..0] <41>

QSA[7..0] <41>

QSA#[7..0] <41>

MAB[13..0] MAB[13..0] <42>

B_BA[2..0] B_BA[2..0] <42>

DQMB#[7..0] <42>

QSB[7..0] <42>

QSB#[7..0] <42>

Close to pin L18

RV41 40.2_0402_1%

RV43 100_0402_1%

CV202 0.1U_0402_16V4Z

+MVREFDA

Close to pin Y12

RV42 40.2_0402_1%

CV203 0.1U_0402_16V4Z

RV44 100_0402_1%

+MVREFDB

Close to pin AA12

RV46 40.2_0402_1%

CV205 0.1U_0402_16V4Z

RV52 100_0402_1%

+MVREFSB

Close to pin L20

RV45 40.2_0402_1%

RV47 100_0402_1%

CV204 0.1U_0402_16V4Z

+MVREFSA

+1.5VS

+3VS_DELAY

RV56 10K_0402_5%

RV23 10K_0402_5%

TESTEN

RV57 51_0402_5%

RV58 51_0402_5%

CV320 0.1U_0402_16V4Z

CV321 0.1U_0402_16V4Z

TESTA

TESTB

RV125 4.7K_0402_5%

RV129 4.7K_0402_5%

RV132 0_0402_5%

RV59 10K_0402_5%

CV206 0.01U_0402_25V7K

51_0402_5%

M9X@ CV206

MANHA@RV132

M9X@ RV54

4.7K_0402_5%

DRAM_RST

DRAM_RST# <41,42>

216-0729002 A12 M96_BGA962

68P_0402_50V8J

@

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Issued Date	2008-09-25	Deciphered Date	2009-09-25

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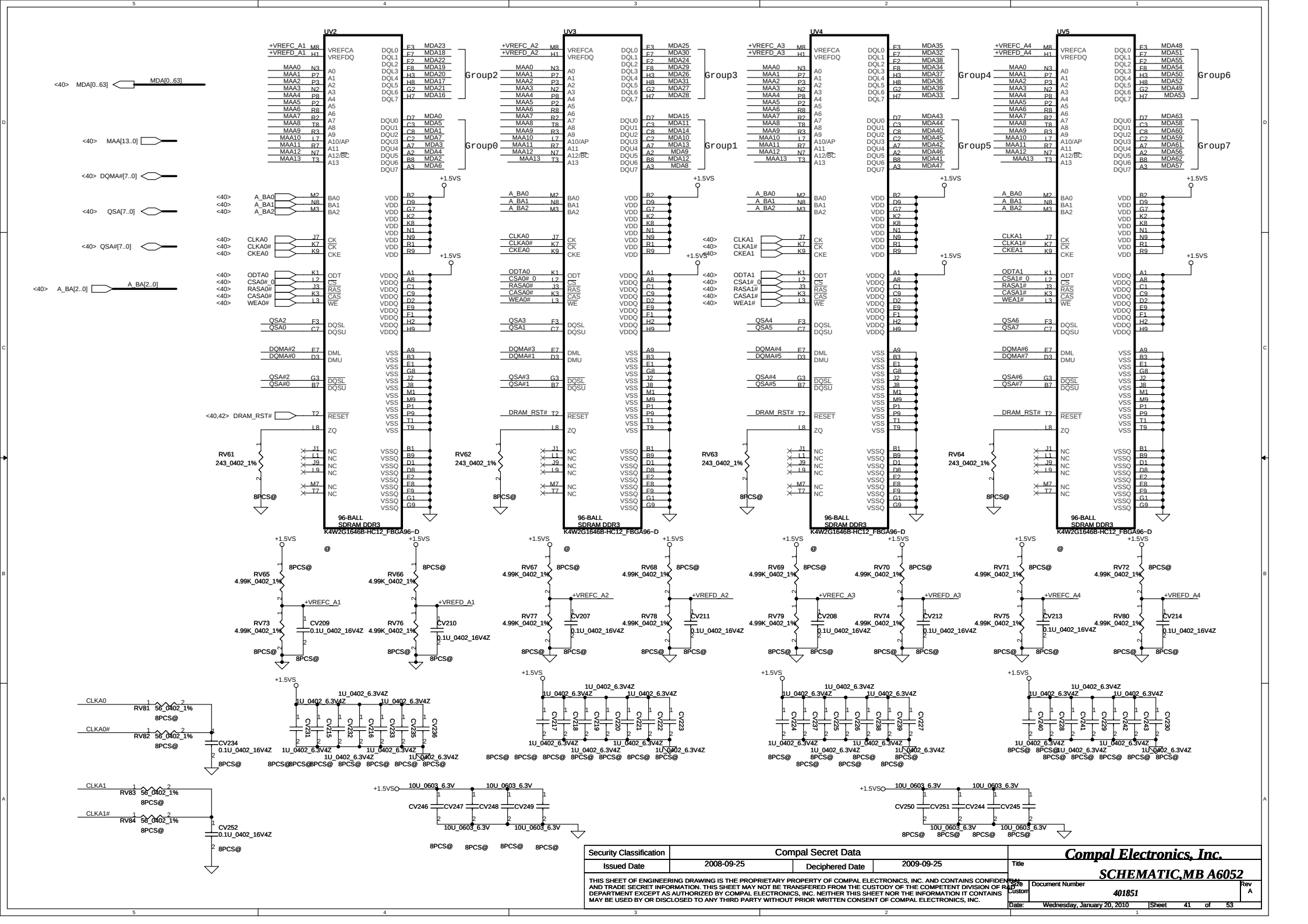

Security Classification	Compal Secret Data		
Issued Date	2008-09-25	Deciphered Date	2009-09-25

Compal Electronics, Inc.			
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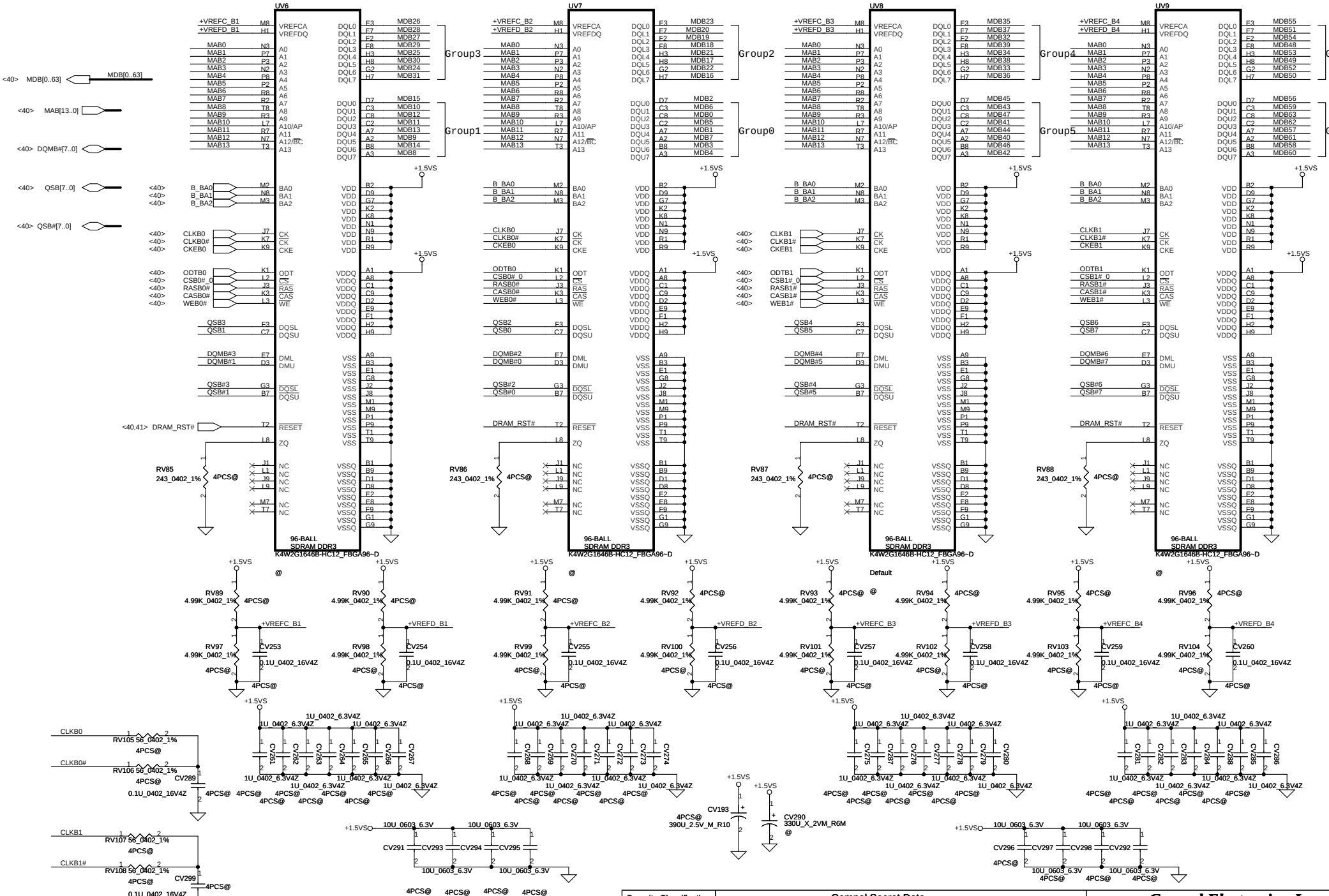

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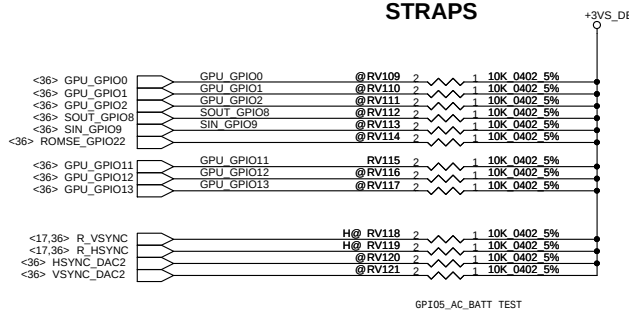
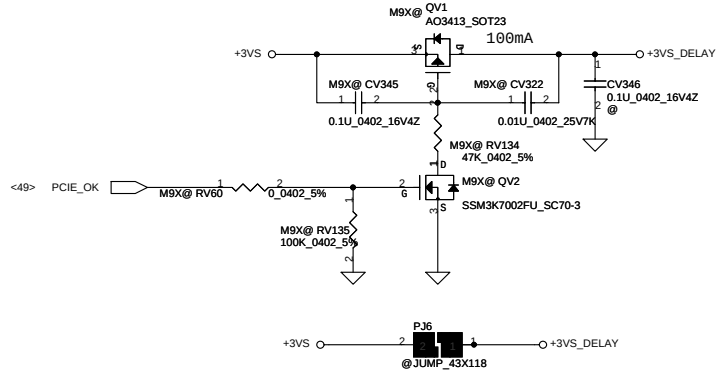
STRAPS

GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	





CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

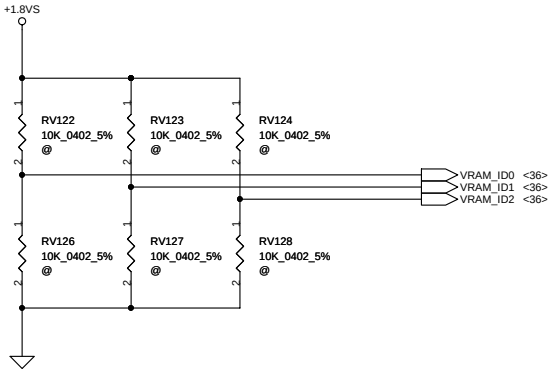
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2 GENERICC

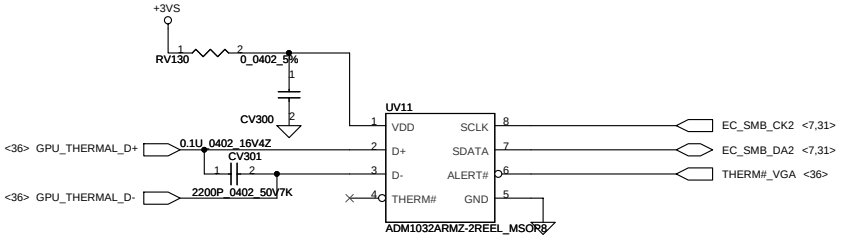
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (2,1,0)	Park M2	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
			512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	0 0 1
			1G 128Mx16 (x4)	HYN		0 1 0 (Reserve)
			1G 128Mx16 (x4)	SAM K4W2G1646B-HC12	SA00003MQ00	0 1 1 (Reserve)
		Madison M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	1 0 0
			1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	1 0 1
			2G 128Mx16 (x8)	HYN		1 1 0 (Reserve)
			2G 128Mx16 (x8)	SAM K4W2G1646B-HC12	SA00003MQ00	1 1 1 (Reserve)

External VGA Thermal Sensor



UV1
M92 XTX
M92@

UV1
Madison
MADISON@

UV1
Park
PARK@

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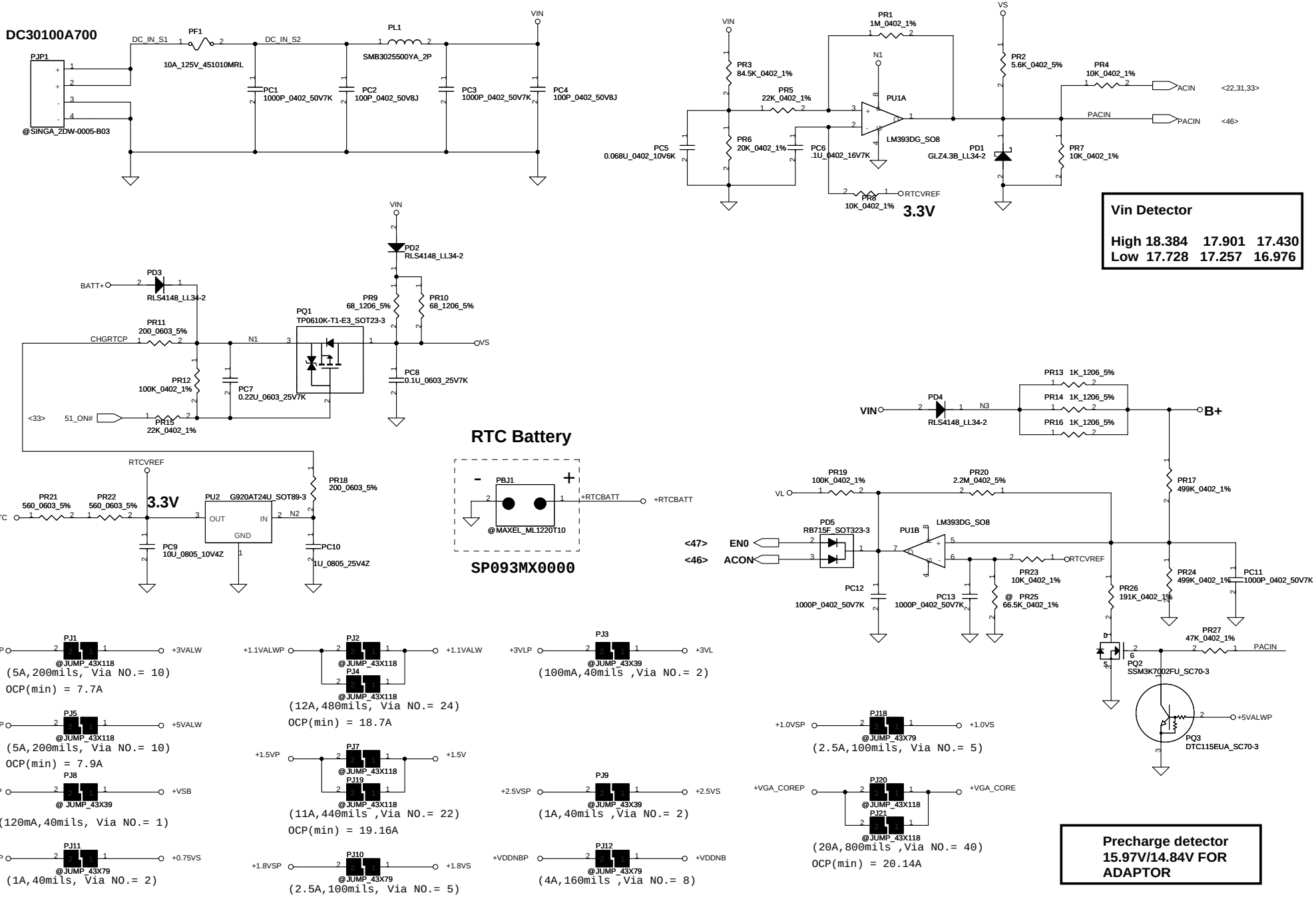

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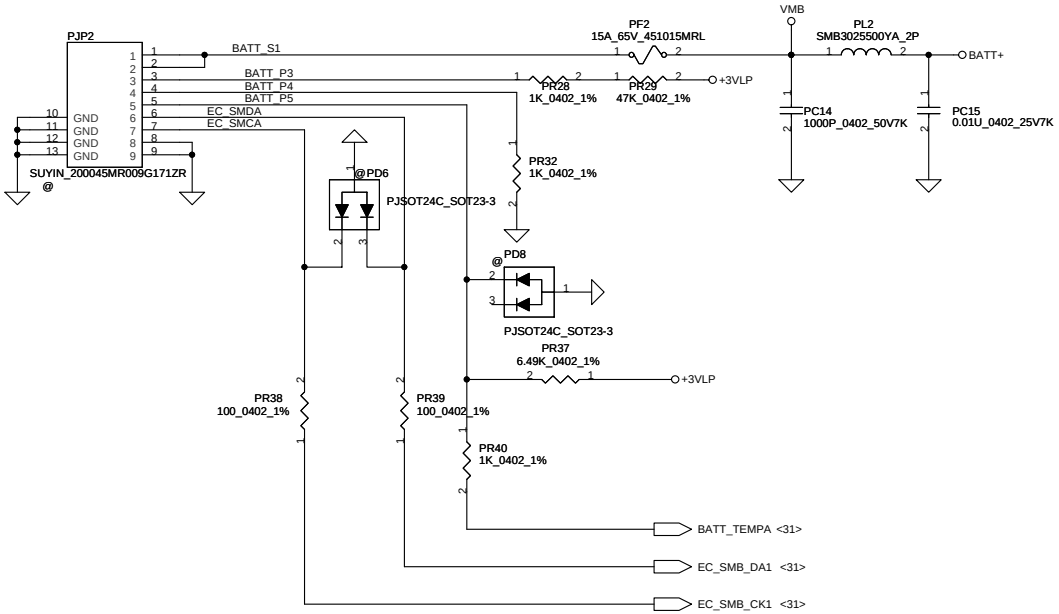
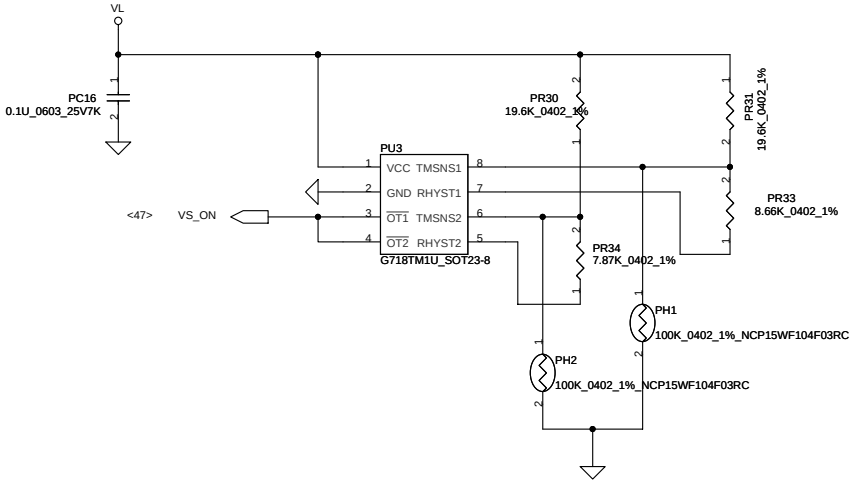
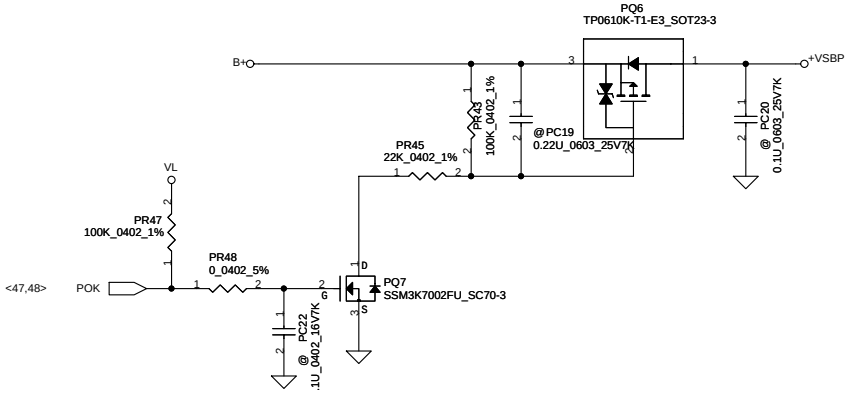


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 95C = 6.64K, Rtml at 57C = 25.1K
Rset = 3 * 6.64K = 19.92K ==> 19.6K
Rhyst = (20K * 25.1K) / (3 * 25.1K - 20K) = 9.078K ==> 9.09K





PH2 near main Battery CONN :
BAT. thermal protection at 95 degree C
Recovery at 48 degree C

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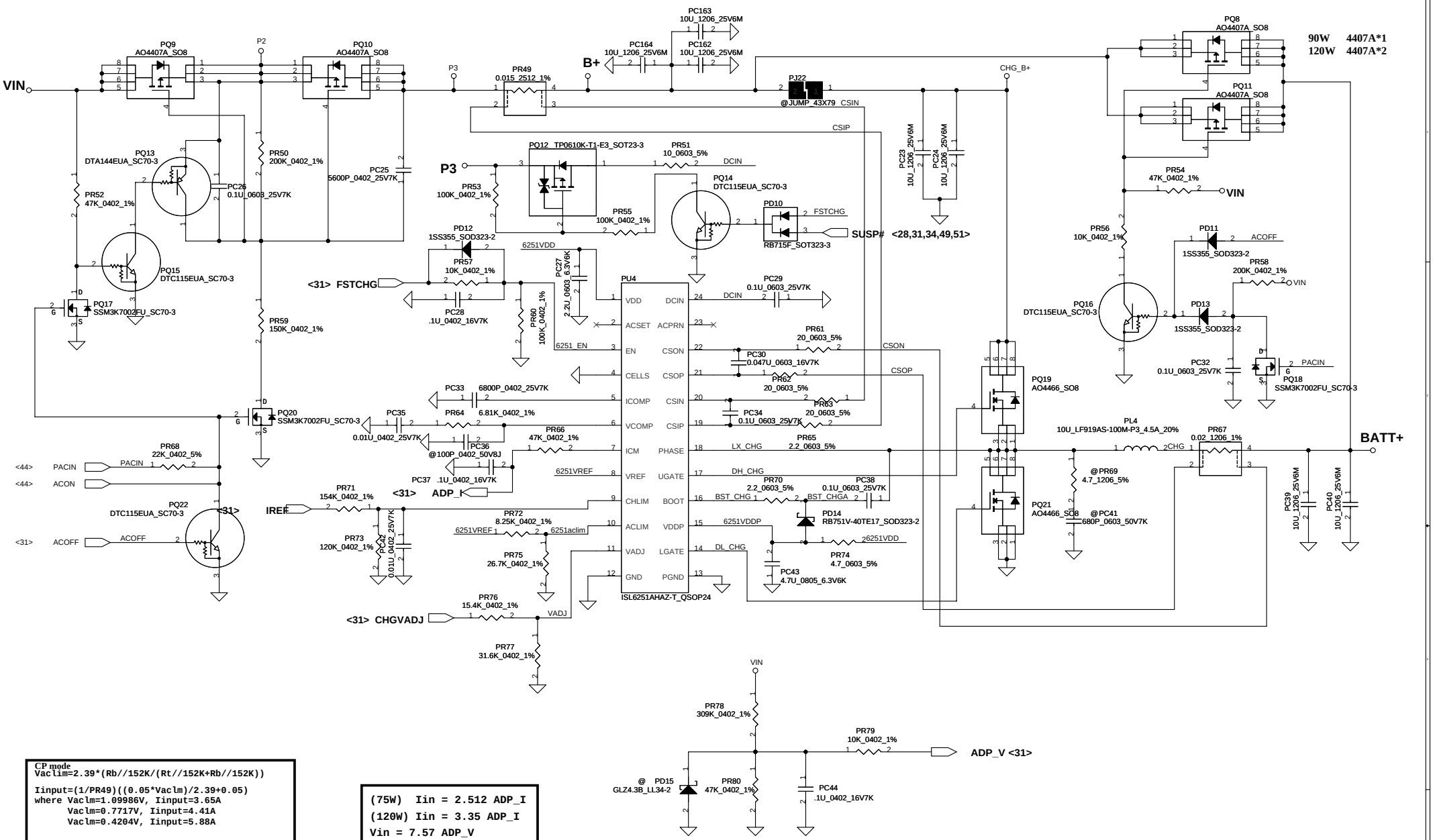

CP mode
Vaclm=2.39*(Rb//152K/(Rt//152K+Rb//152K))

Iinput=(1/PR49)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.09986V, Iinput=3.65A
Vaclm=0.7717V, Iinput=4.41A
Vaclm=0.4204V, Iinput=5.88A

(75W) Iin = 2.512 ADP_I
(120W) Iin = 3.35 ADP_I
Vin = 7.57 ADP_V

CC=0.25A~3A
IREF=0.9133*Icharge
IREF=0.228V~2.74V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445

Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.315V

Iada=0~3.421A(65W) CP=3.15A PR49=0.02, PR72=75k, PR75=20k
Iada=0~3.947A(75W) CP=3.63A PR49=0.02, PR72=24k, PR75=20k
Iada=0~4.737A(90W) CP=4.36A PR49=0.015, PR72=53.6k, PR75=20k
Iada=0~6.316A(120W) CP=5.81A PR49=0.015, PR72=8.25k, PR75=26.7k
CP= 92%*Iada

CELLS	VDD	GND	Float
CELL number	4	3	2

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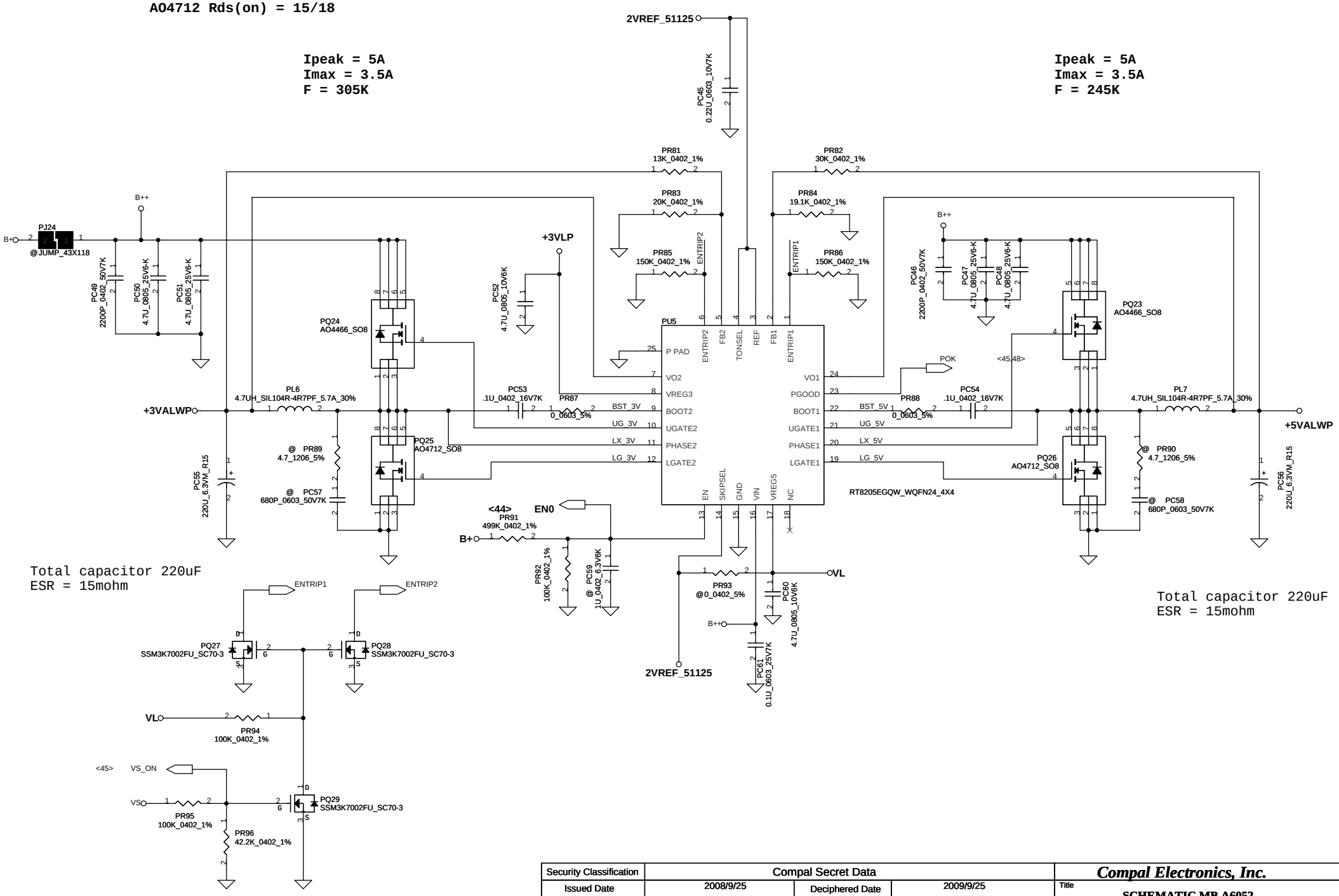
A04712 Rds(on) = 15/18

Ipeak = 5A
Imax = 3.5A
F = 305K

Ipeak = 5A
Imax = 3.5A
F = 245K



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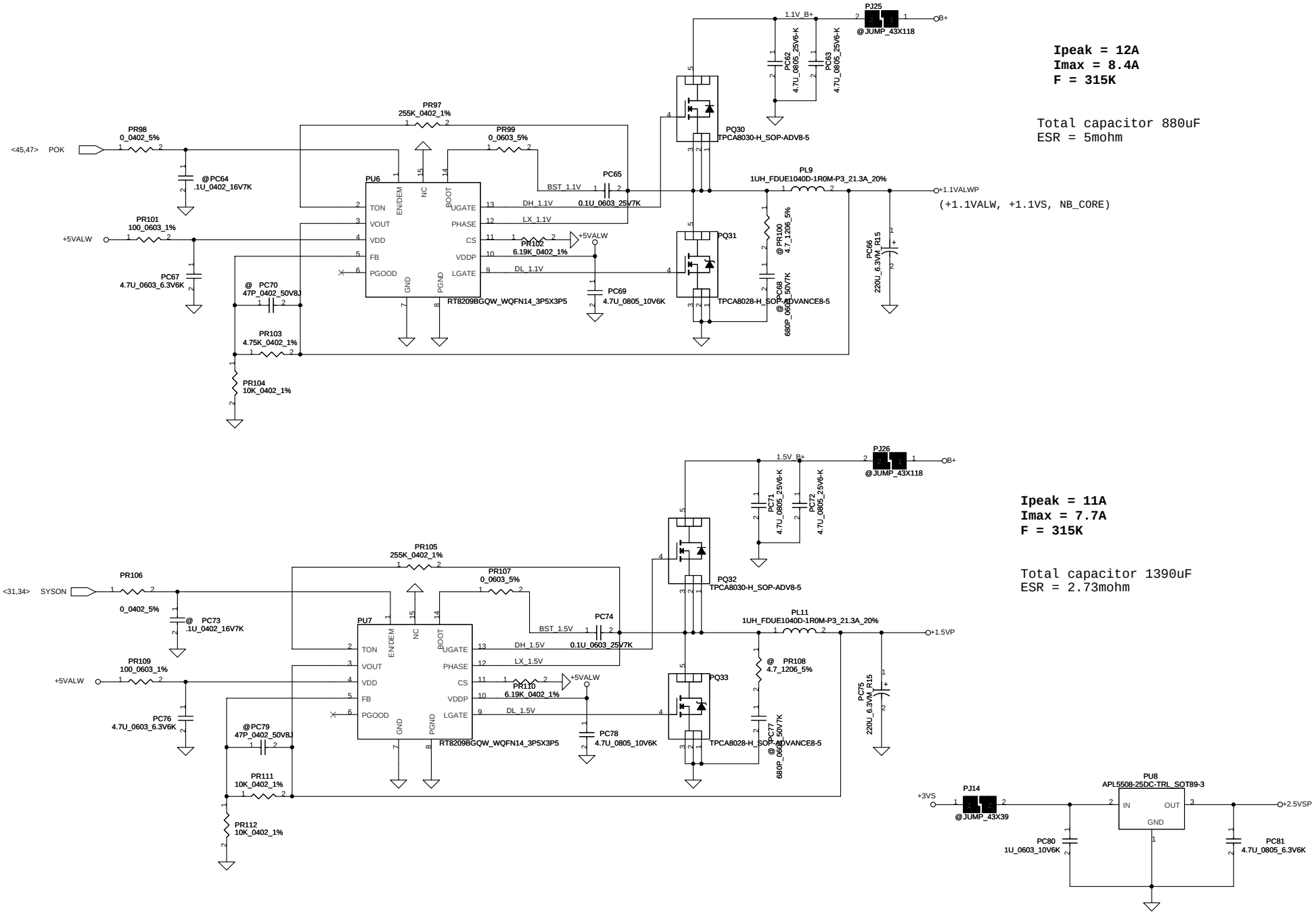

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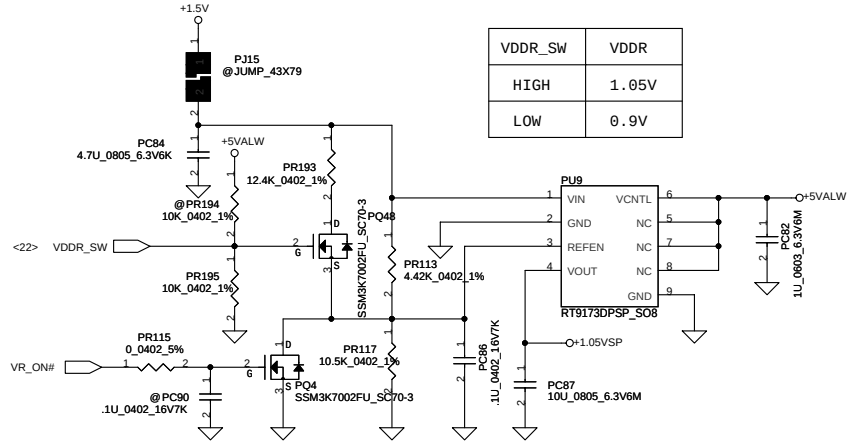
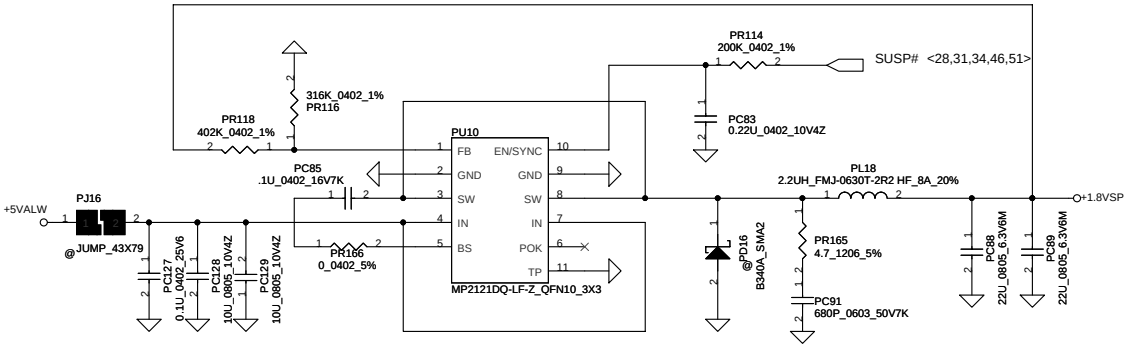
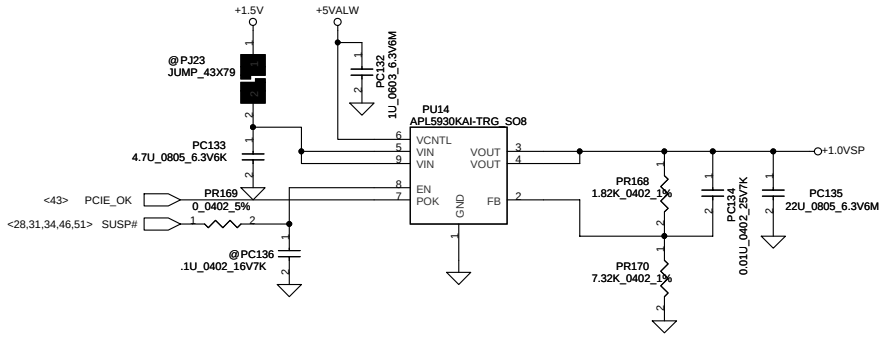
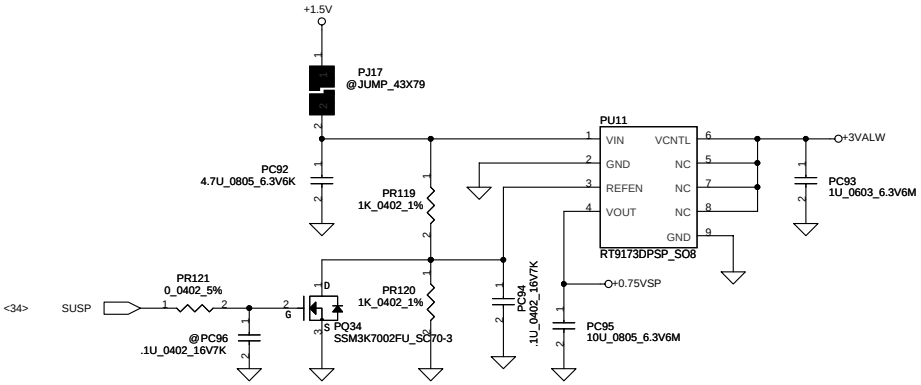


VDDR_SW	VDDR
HIGH	1.05V
LOW	0.9V







Madison / Park PCIE : 1.0V	M96 / M92 PCIE : 1.1V
PR170 = 7.32K	PR170 = 4.75K

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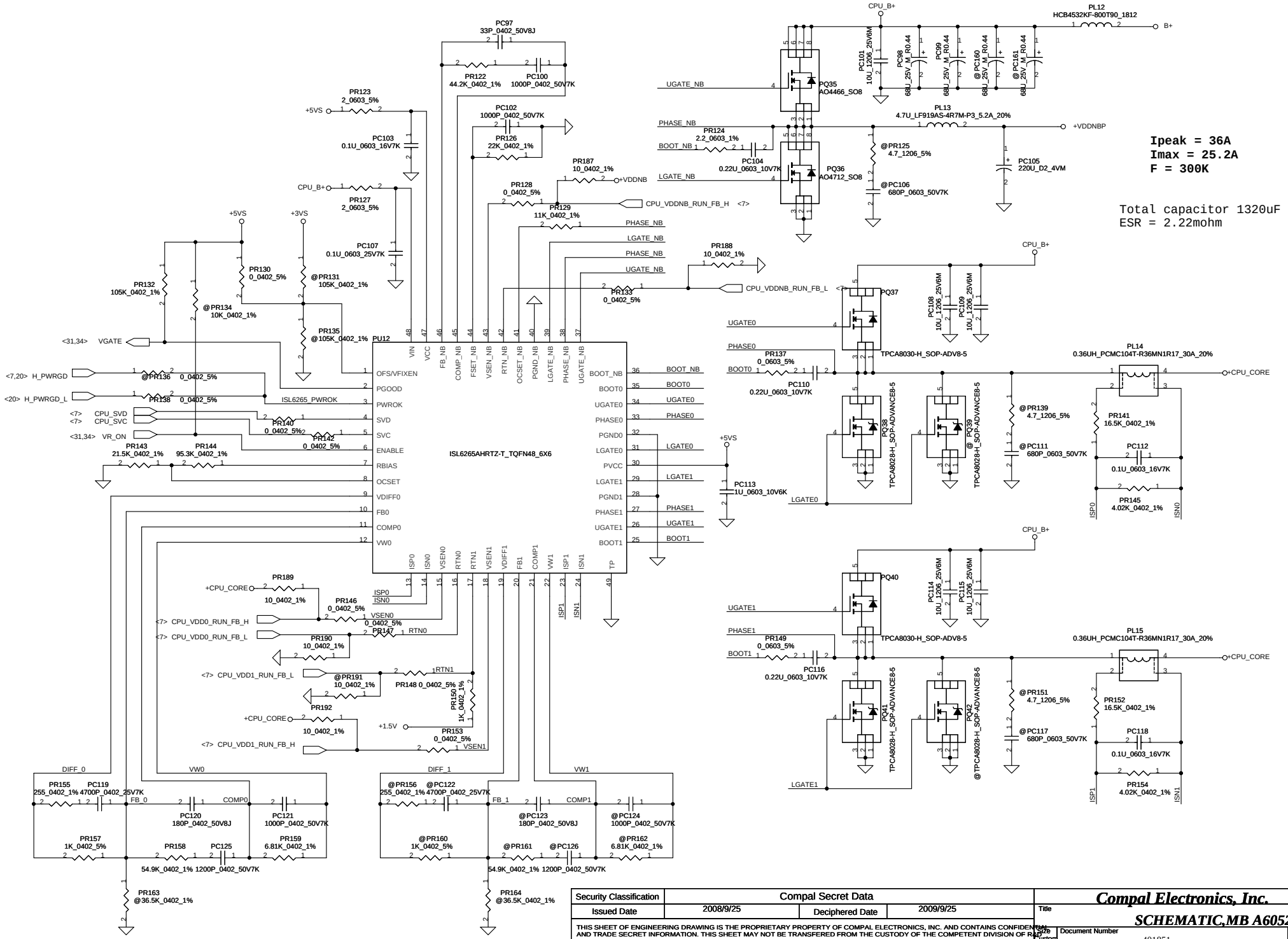

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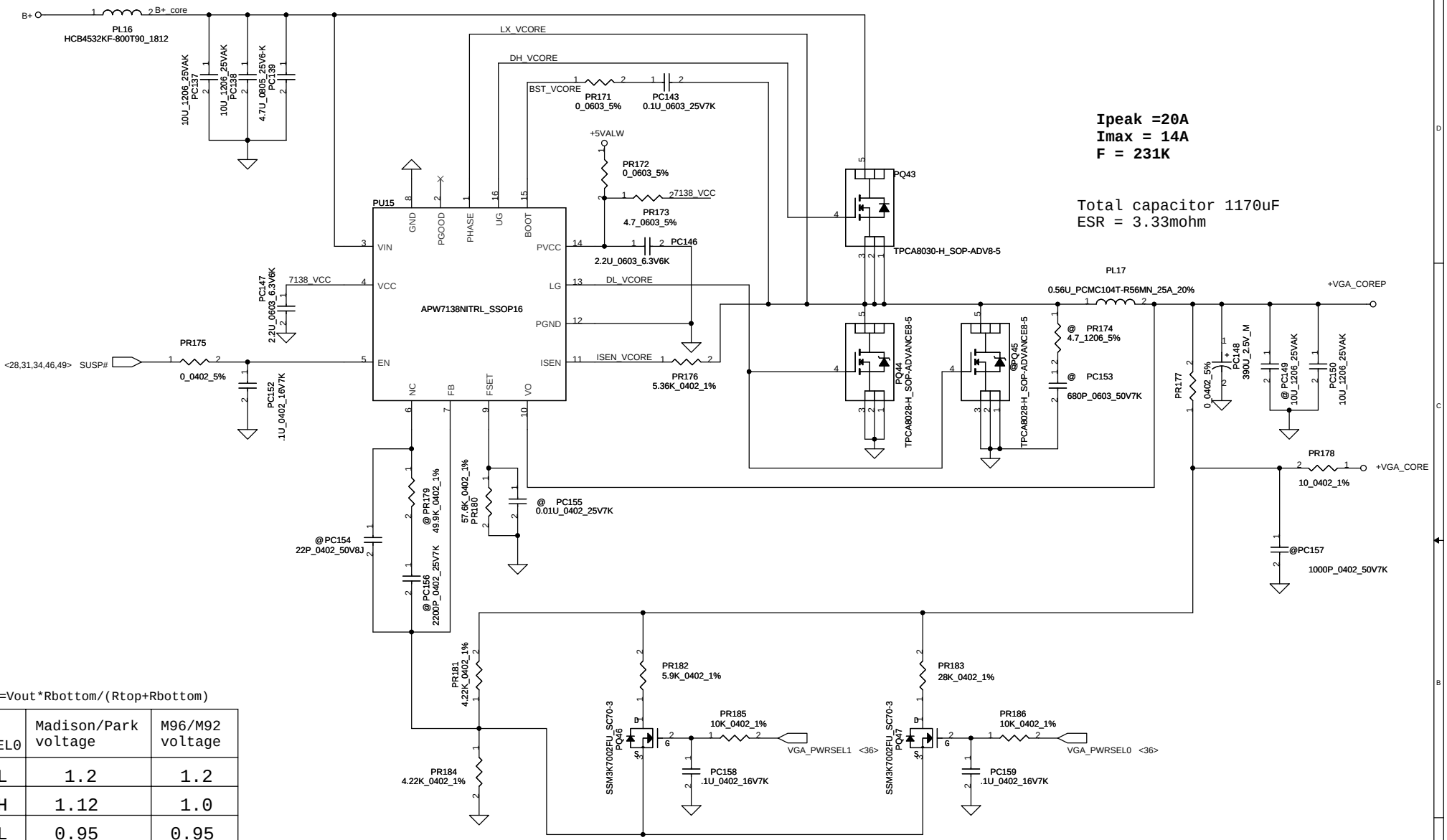

Ipeak =20A
Imax = 14A
F = 231K

Total capacitor 1170uF
ESR = 3.33mohm

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

SEL1	SEL0	Madison/Park voltage	M96/M92 voltage
L	L	1.2	1.2
L	H	1.12	1.0
H	L	0.95	0.95
H	H	0.9	0.9

FSW=1/(75E-12*57.6K)=231.48KHz

Madison Park	M96 M92
PR183 = 28K	PR183 = 12K

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PIR (Product Improve Record)

NALAE LA-6052P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST
1	2009/12/14	33	Change JLEDB pin define as customer request
2	2009/12/14	25,28,30	Delete JODDB, JBT and JUSBB support pin
3	2009/12/14	33	Change JPOWER Pin2 from GND to NC
4	2009/12/15	28	Add R95 at JWLAN Pin5 for BT/WLAN combo Mini Card
5	2009/12/15	25,30	Change U11, U25 P/N from SA00002XX00 to SA000033H00
6	2009/12/15	28	Reverse JBT pin definition
7	2009/12/16	27	Change CC2 from 0.1u to 100P (SE071101J80), and add BOM structure @
8	2009/12/17	33	Cgange JPOWER footprint to ACES_87151-1207_12P (ZIF_上接點)
9	2009/12/17	33	Cgange JTPB footprint to P-TWO_161011-04021_4P-T (NO ZIF), and reverse pin definition
10	2009/12/17	33	Cgange JLEDB footprint to ACES_85201-1205N_12P (ZIF_上接點)
11	2009/12/17	25	Cgange JUSBB footprint to ACES_85201-20051_20P (ZIF_上接點)
12	2009/12/17	33	Change H36, H37 footprint from H_3P3 to H_3P8

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Version Change List (P. I. R. List) for Power Circuit

Page#	Item Title	Solution Description
DVT : modification from EVT		
P48	change voltage divider to less than 10K	change PR104, PR111, PR112 to 10K; PR103 to 4.75K
P48	change 1.1V, 1.5V OCP value	change PR102, PR110 to 6.19K
P49	enlarge output cap	change PC88, PC89 to 22uF(SE000000I10)
P50	don't use NIPPON cap	change PC98, PC99 to SF000000S80
P50	pull high RTN1 1.5V	change PR150 to mount
P51	APW7138 pin6 is NC	change PR179, PC154, PC156 to unmount
P47	choke need to meet thermal module height	change PL6, PL7 to SH000006380
P46	change system power from 90W to 120W	change PR72 to 8.25K, PR75 to 26.7K; PQ11 to mount
P50	production line request	change PC98, PC99 to 68uF; add PC160, PC161 68uF
P46	EMI request for ISN issue	add PC162, PC163, PC164 10uF 1206
P49	mount snubber circuit	mount PR165, PC91
P45	OTP setting common	change PR30 and PR31 to 19.6K; PR34 to 7.87K; PR33 to 8.66K
P49	change IC to low cost	change PU9 and PU11 to RT9173
P49	change VDDR(1.05V) circuit to switchable	add PR193, PR194, PR195 & PQ48

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