

ZZZ1



LA-6001P

DAZ0CG00100

Compal Confidential

NBLB3/5 Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex HM55

2010-04-28

REV:1.0

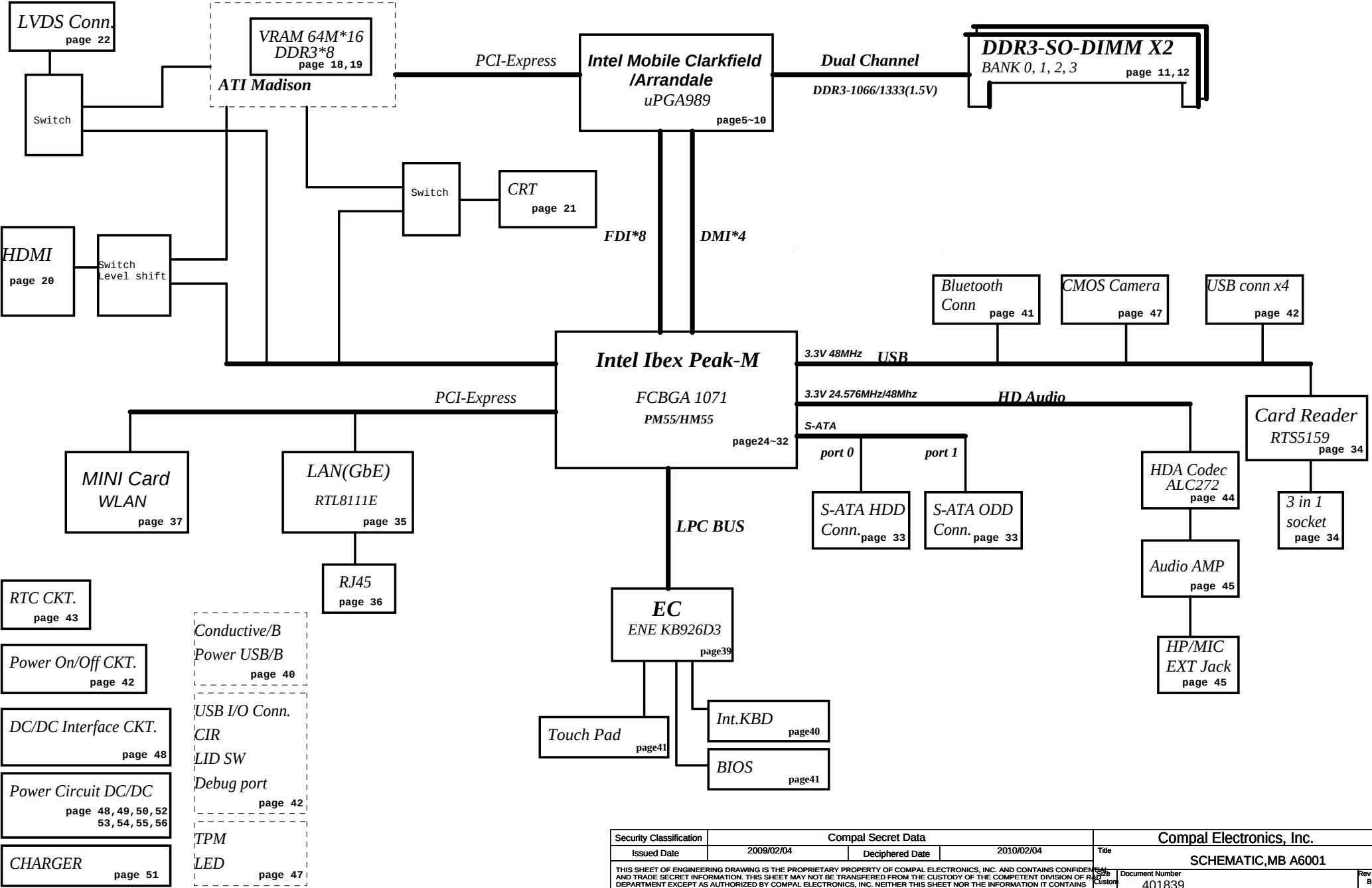
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/02/04	Deciphered Date	2010/02/04	Title		
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				Custom	401839	B
				Date: Thursday, June 10, 2010	Sheet 1 of 59	E

Compal Confidential

Model Name : NBLB3/5

File Name : LA-6001P(Madison)

Clock Gen.
SLG8SP587
9LRS3199AKLFT
page23



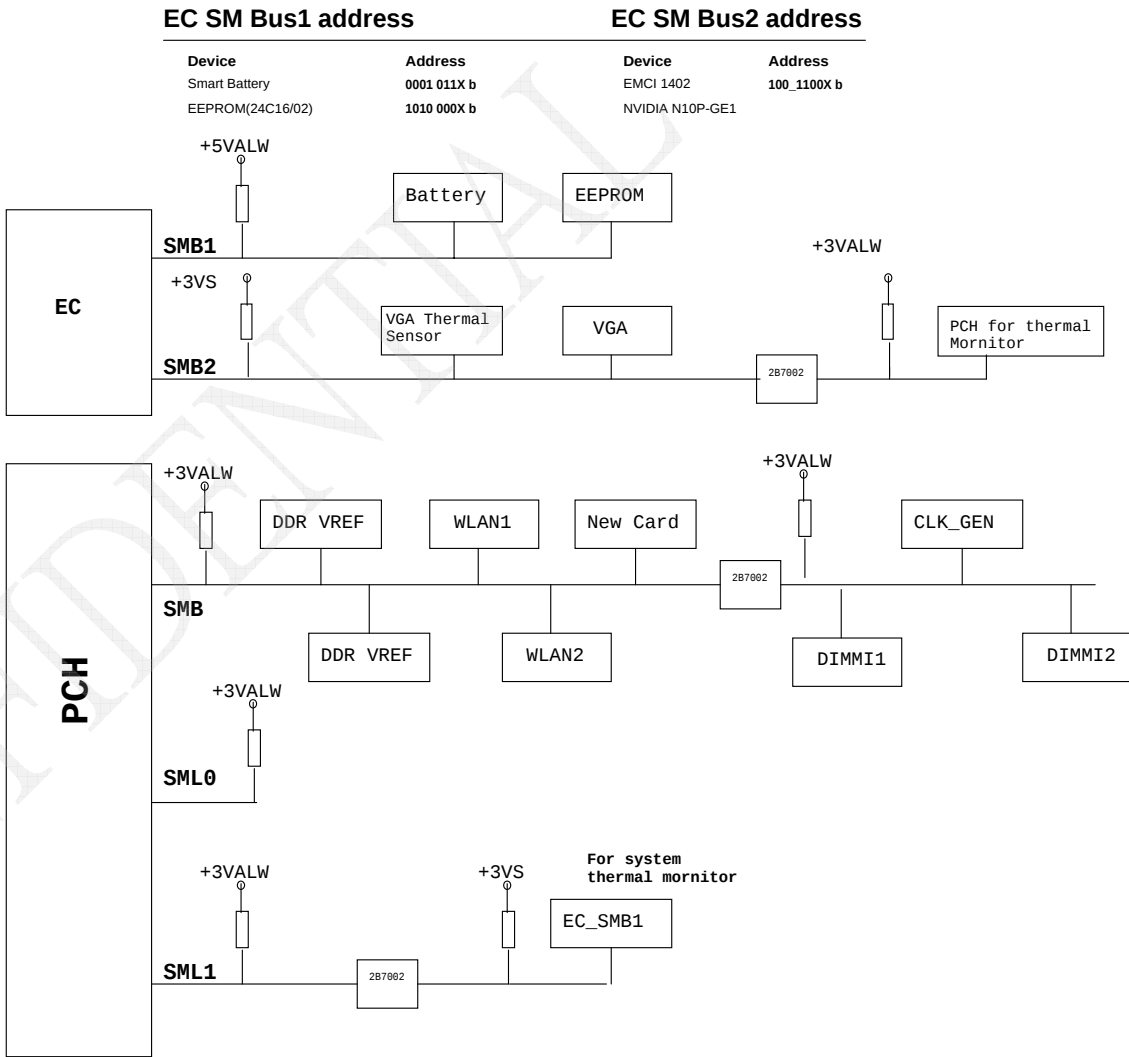
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DDR3 Voltage Rails

power plane				
State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS +1.1VS_VTT +1.5VS_VRAM
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

GPIO PIN Define

	ID3	ID2	ID1	ID0
NBLB2(1100)	R358	R361	R766	R765
Reserve (1101)	X	X	X	X
Reserve (1110)	X	X	X	X
Reserve (1111)	X	X	X	X
NBLB1 (0000)	R353	R350	R766	R765
Reserve(0001)	X	X	X	X
Reserve(0010)	X	X	X	X
Reserve(0011)	X	X	X	X
Reserve(0100)	X	X	X	X
Reserve(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X



VGA (Madison)

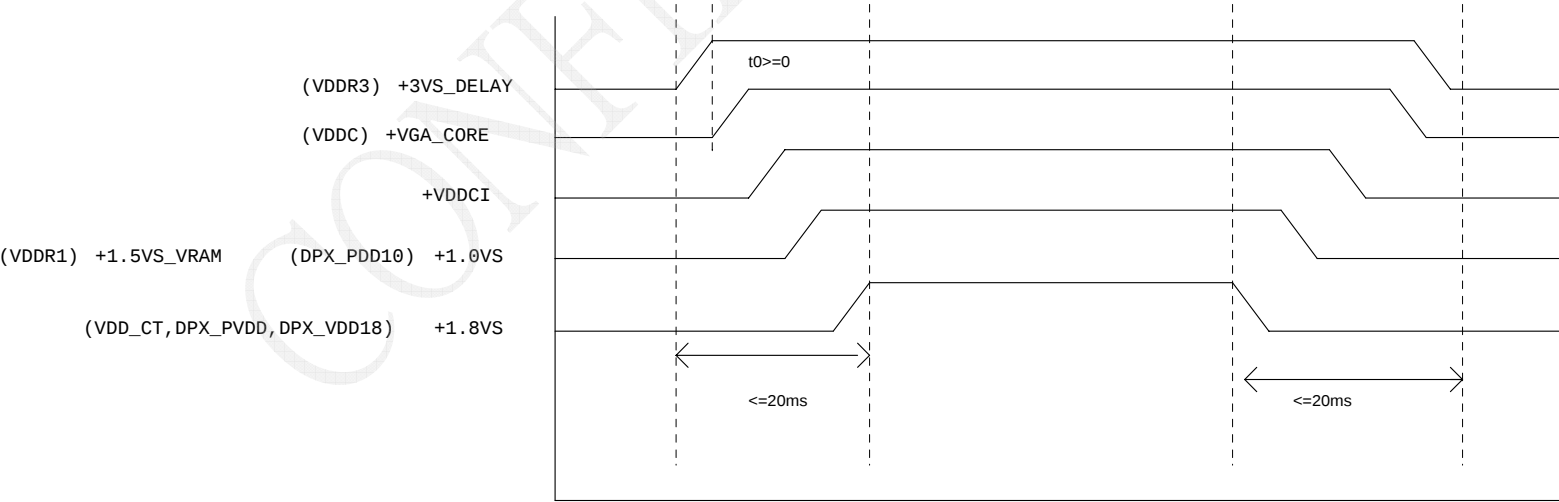
State \ power plane	+1.8VS +1.5VS_VRAM	+3VS_DELAY +VGA_CORE +1.1VS
S0	0	0
S1	0	0
S3	X	X
S5 S4/AC	X	X
S5 S4/ Battery only	X	X
S5 S4/AC & Battery don't exist	X	X

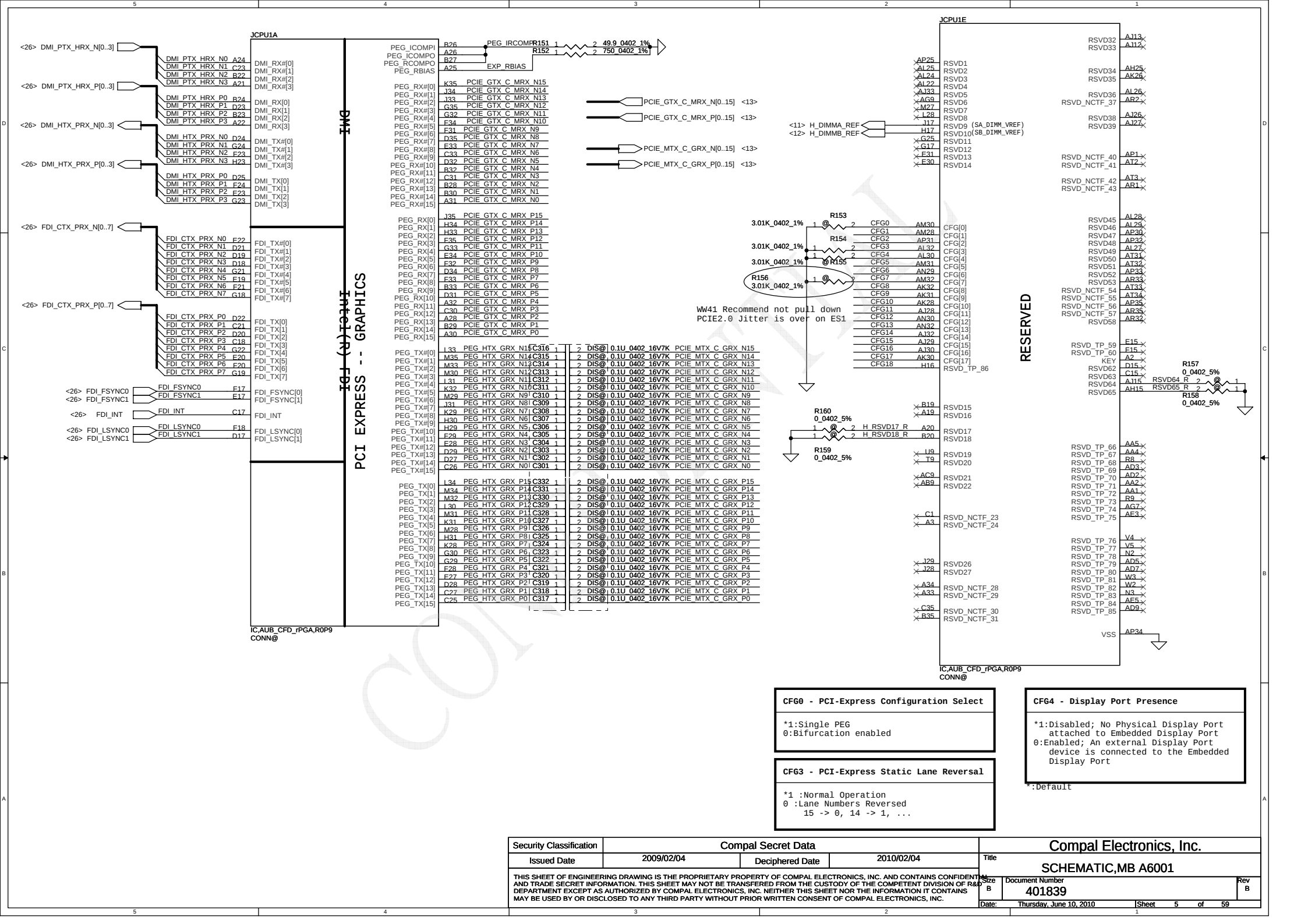
POWER UP/DOWN Sequence

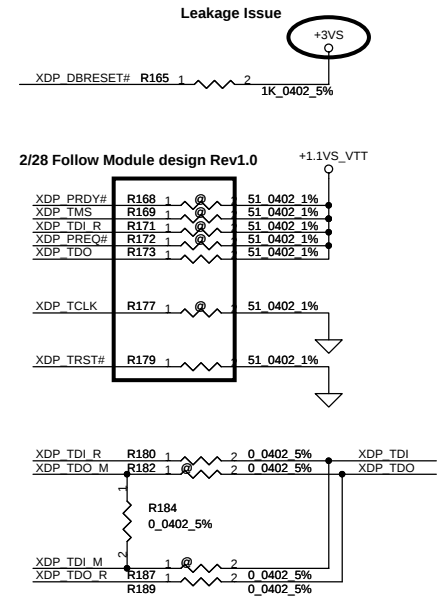
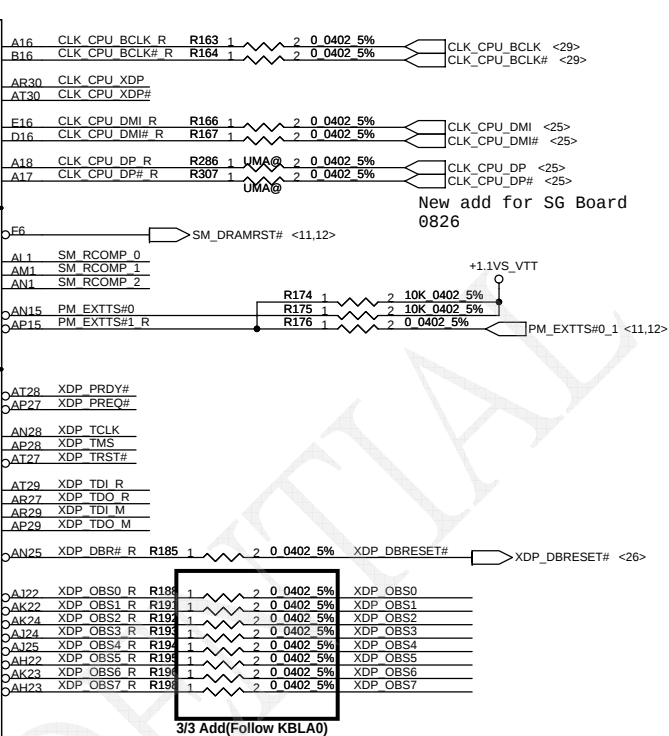
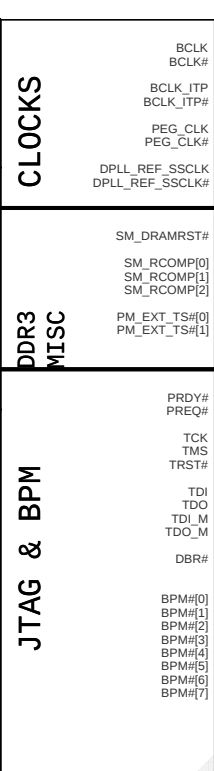
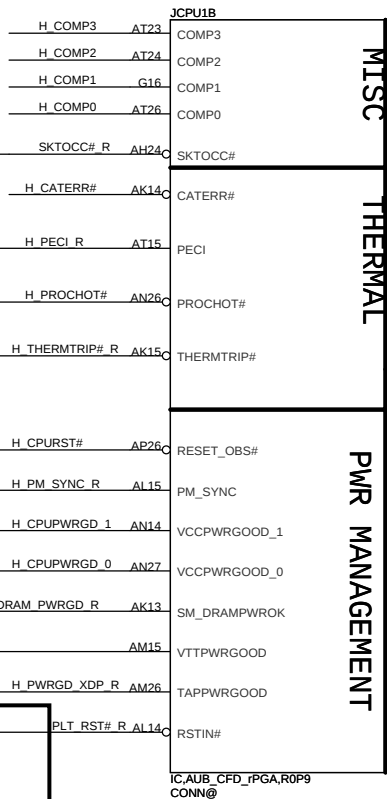
47132_madison_ds_nda_1.04

Madison sequence

- Power-Up/Down Sequence
Madison has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.
- 1, All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
 - 2, VDDR3 should ramp-up before or simultaneously with VDDC.
 - 3, For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
 - 4, The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
 - 5, VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)
 - 6, For power-down, reversing the ramp-up sequence is recommended.



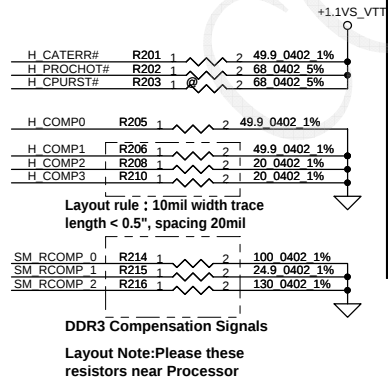
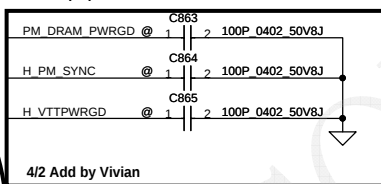
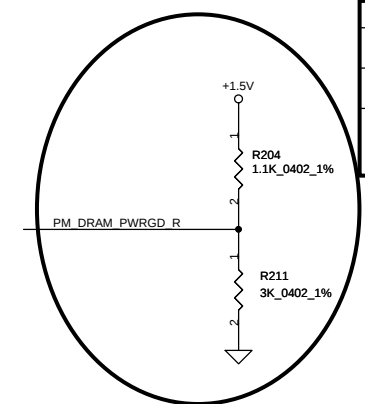




JTAG MAPPING

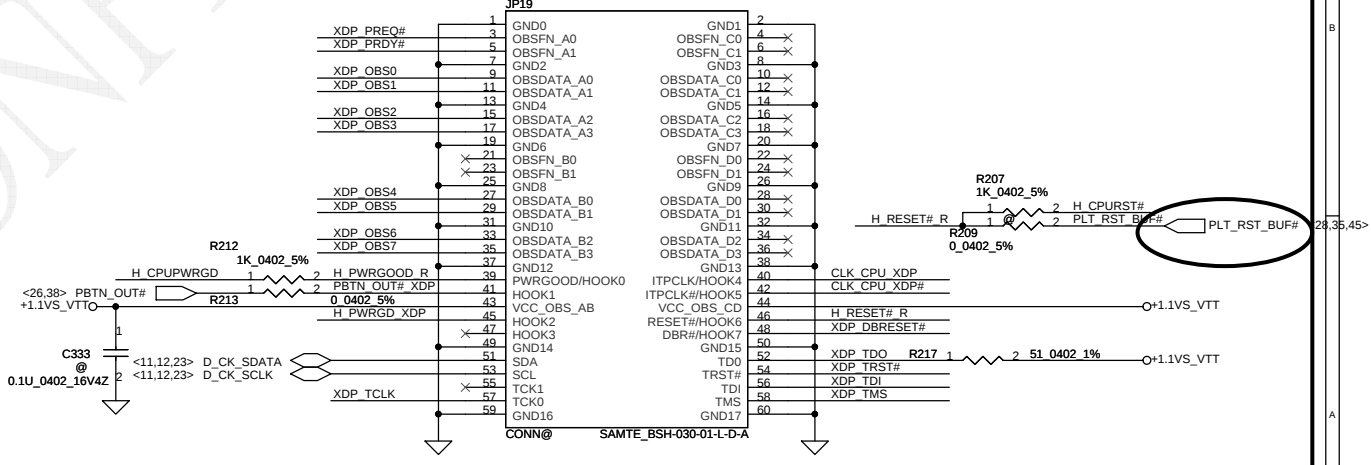
Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657

4/17 Modify R199 to 1.5K ohm, R200 to 750 ohm(see DG414044 p.8)



Intel Suggestion
WW14_2009_Calpeila_MoW
Notice: V_SM should be available in S3

XDP Connector



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				401839	Rev B
				Date: Thursday, June 10, 2010	Sheet 6 of 59

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<11> DDR_A_DQS[0..7]
<11> DDR_A_MA[0..15]

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DDR A D6 E10
DDR A D7 A8
DDR A D8 D8
DDR A D9 F10
DDR A D10 E6
DDR A D11 E7
DDR A D12 E9
DDR A D13 B7
DDR A D14 E7
DDR A D15 C6
DDR A D16 H10
DDR A D17 C8
DDR A D18 K7
DDR A D19 J8
DDR A D20 G7
DDR A D21 G10
DDR A D22 J7
DDR A D23 J10
DDR A D24 L7
DDR A D25 M6
DDR A D26 M8
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DDR A D38 A17
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DDR A D63 AP14

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DDR SYSTEM MEMORY A

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SA_CKE[0] P7
SA_CK[1] Y6
SA_CK#1 Y6
SA_CKE[1] P6
SA_CS#0 AE2
SA_CS#1 AE8
SA_ODT[0] AD8
SA_ODT[1] AF9
SA_DM[0] B9
SA_DM[1] D7
SA_DM[2] H7
SA_DM[3] M7
SA_DM[4] AG6
SA_DM[5] AM7
SA_DM[6] AN10
SA_DM[7] AN13
SA_DQS#0 C9
SA_DQS#1 E8
SA_DQS#2 J8
SA_DQS#3 J9
SA_DQS#4 AH7
SA_DQS#5 AK9
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SA_MA[9] U6
SA_MA[10] AD4
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DDR A D62
DDR A D63
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CONN@

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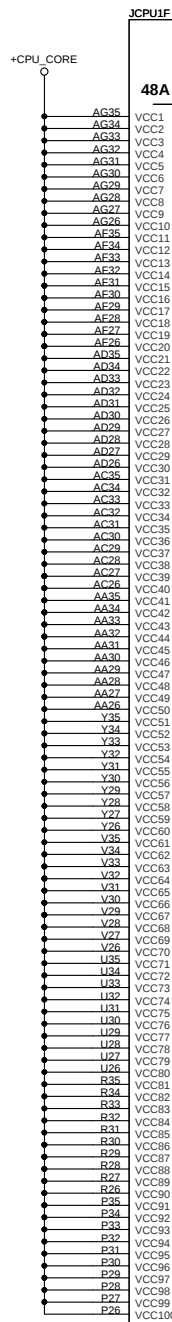
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DDR B WE#

DDR SYSTEM MEMORY - B

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IC:AUB_CFD_rPGA,R0P9
CONN@



WW15 MOW
Peak 21A
Continuous 18A

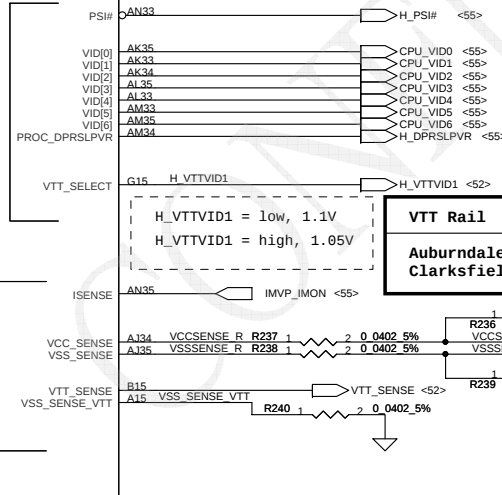
1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

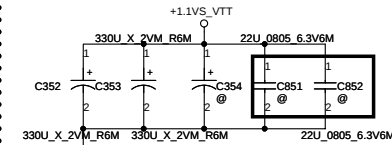
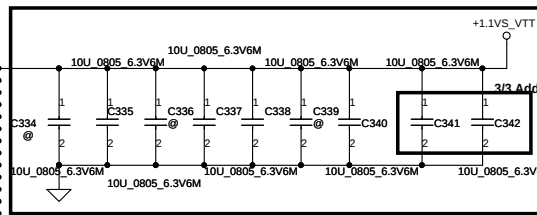


VTT Rail

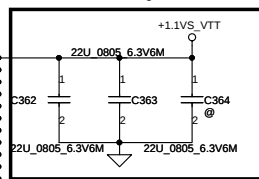
Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

change to SGA00001Q80
DVT

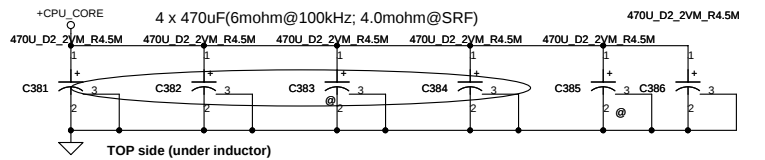
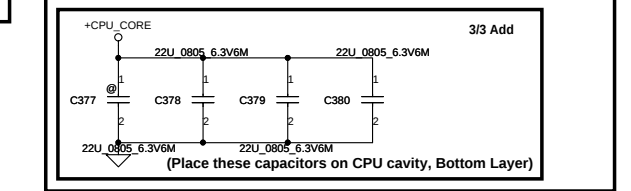
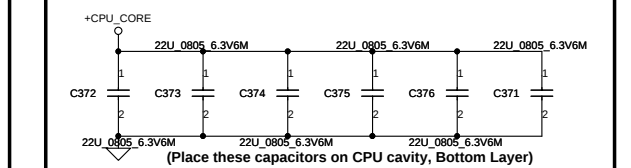
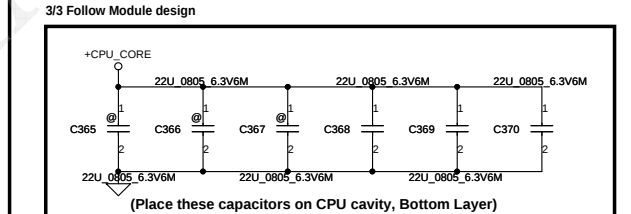
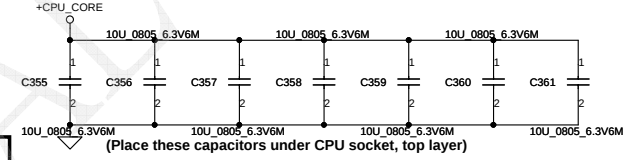
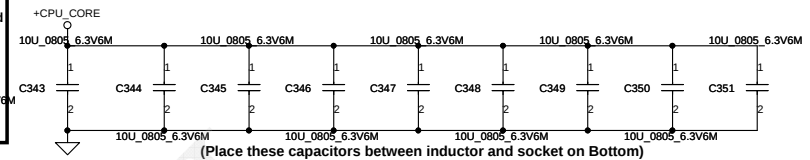
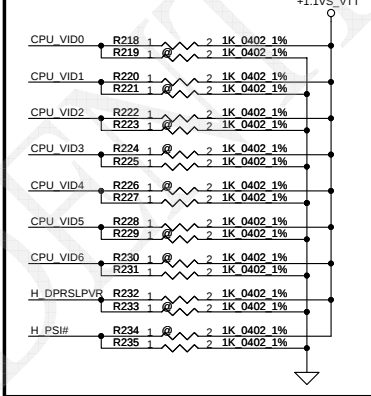
3/3 Follow Module design



3/3 Follow Module design



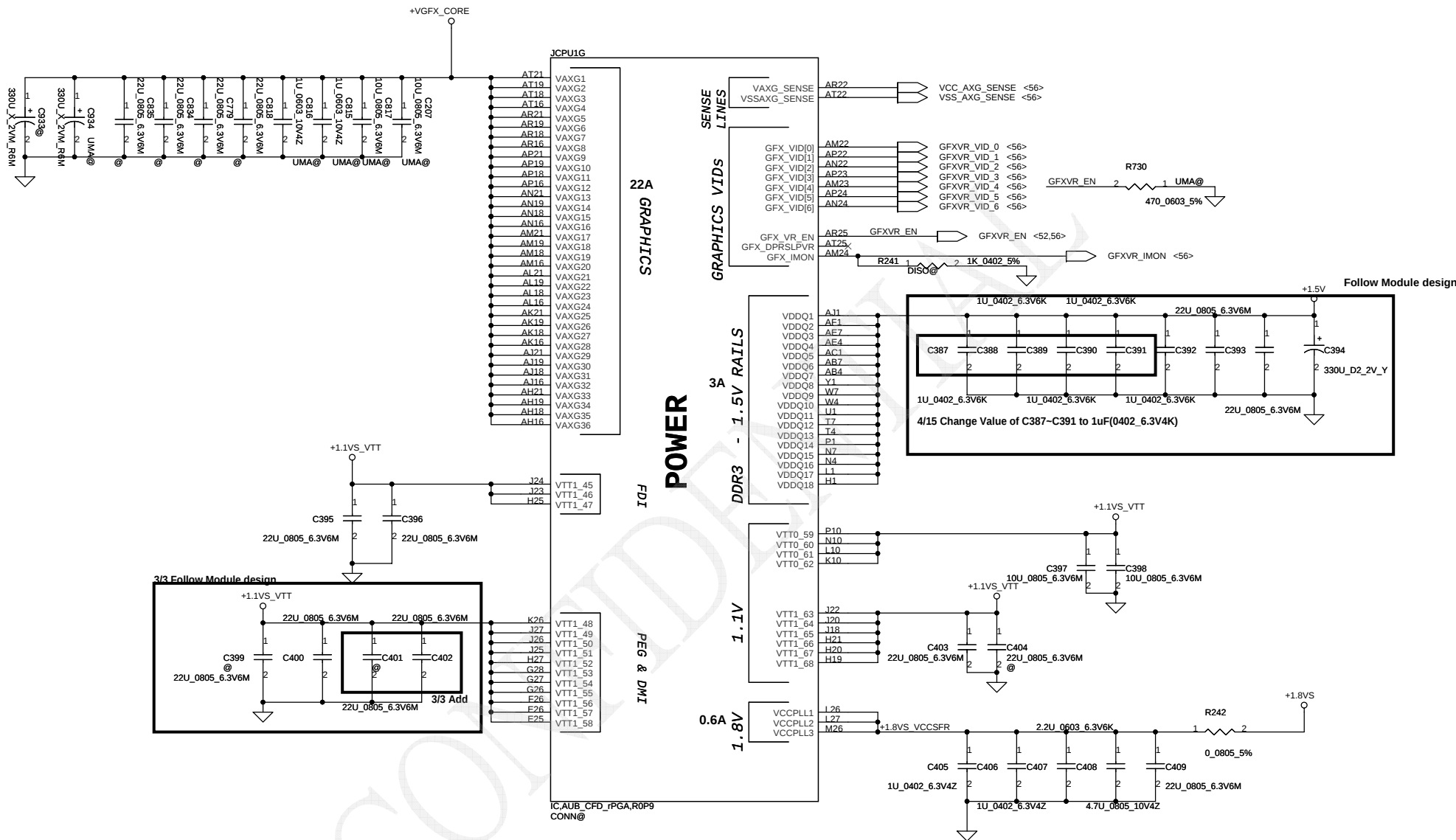
CSC (Current Sense Configuration)
8/25



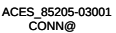
+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP, Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

IC,AUB_CFD_PGA,R0P9
CONN@

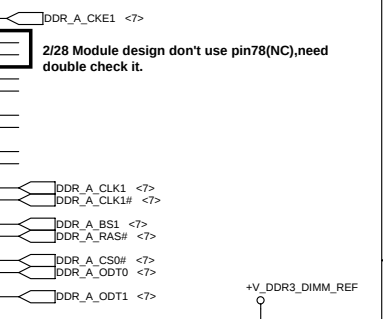
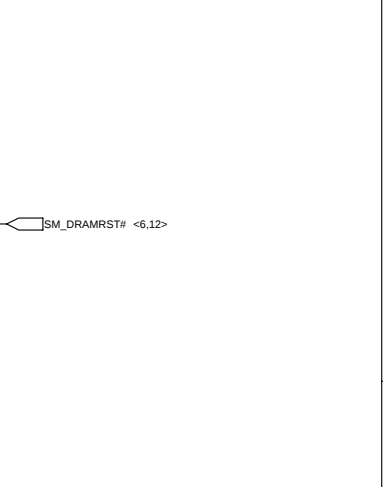
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Issued Date	2009/02/04	Deciphered Date	2010/02/04	SCHEMATIC, MB A6001
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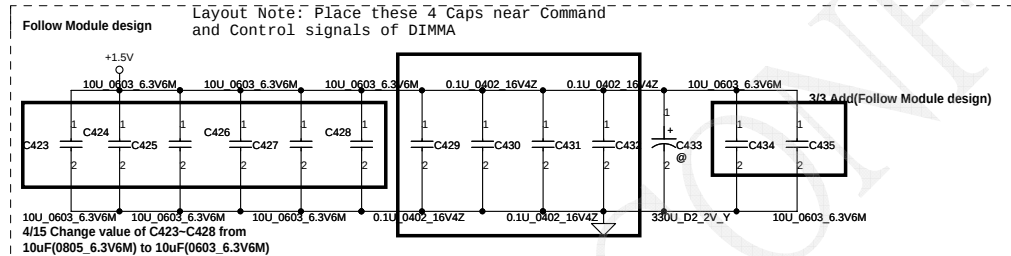
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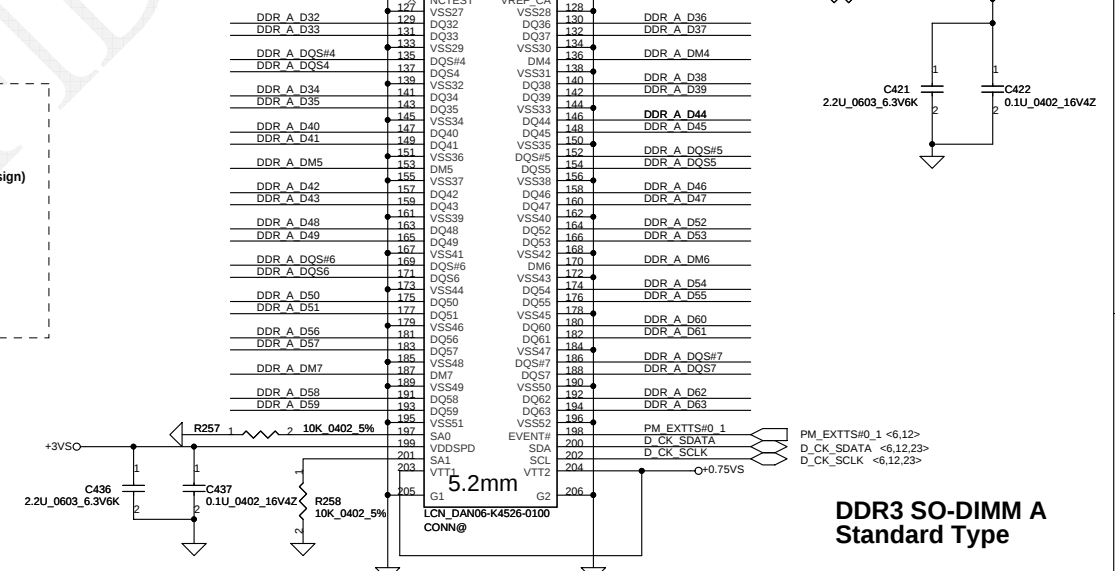
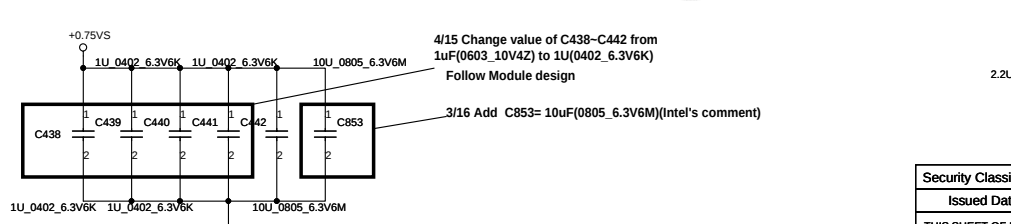
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Layout Note:
Place near JP2



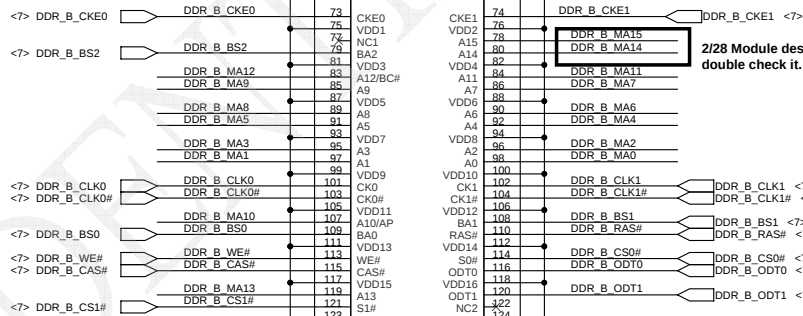
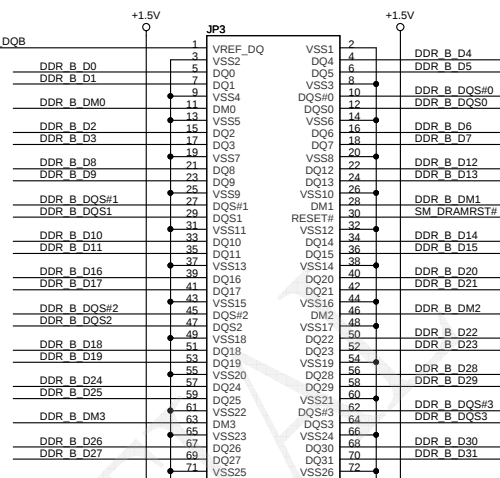
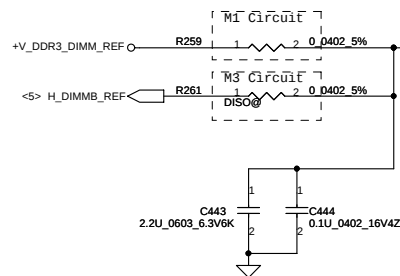
Layout Note:
Place near JP2.203 & JP2.204



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<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DM[0..7]
<7> DDR_B_DQ[0..7]
<7> DDR_B_MA[0..15]

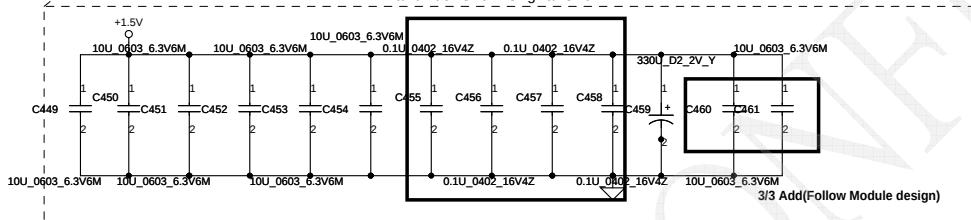
2098/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details



2/28 Module design don't use pin78(NC), need double check it.

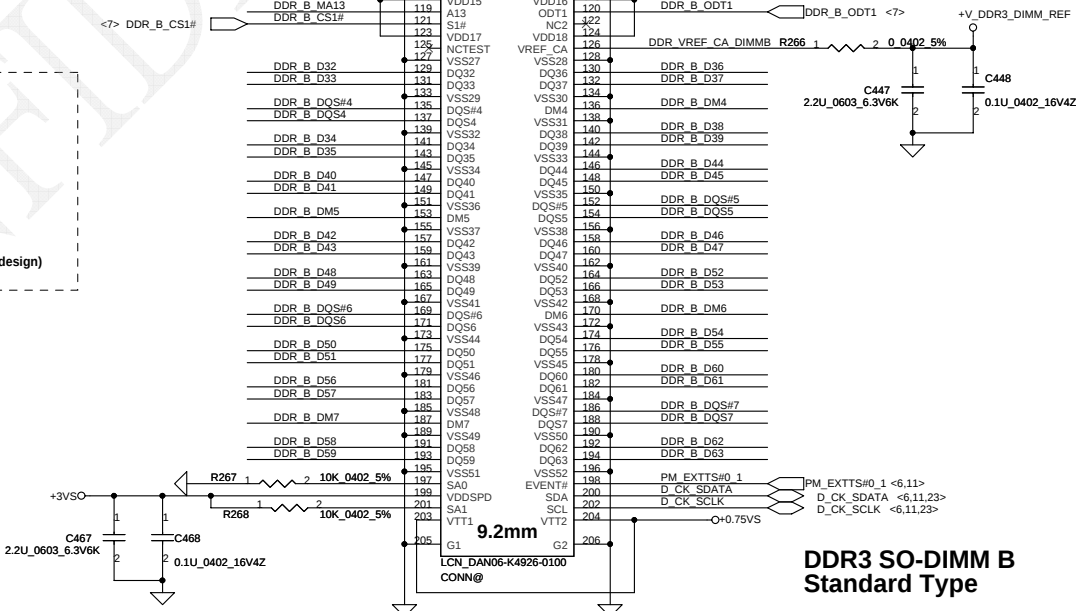
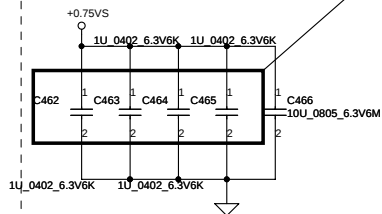
Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JP3.203 & JP3.204

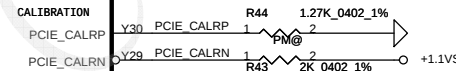
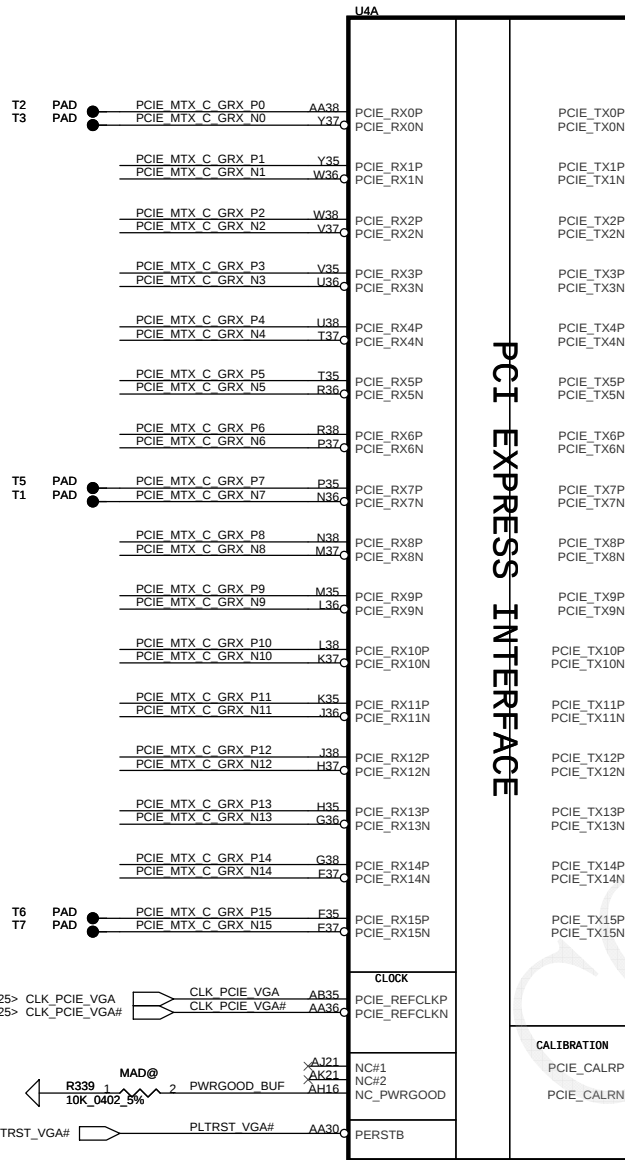
4/15 Change value of C462-C465 from 1uF(0603_10V4Z) to 1U(0402_6.3V6K)
Follow Module design



DDR3 SO-DIMM B
Standard Type

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<5> PCIE_MTX_C_GRX_N[0..15] PCIE MTX C GRX N[0..15]
<5> PCIE_MTX_C_GRX_P[0..15] PCIE MTX C GRX P[0..15]
<5> PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]
<5> PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]

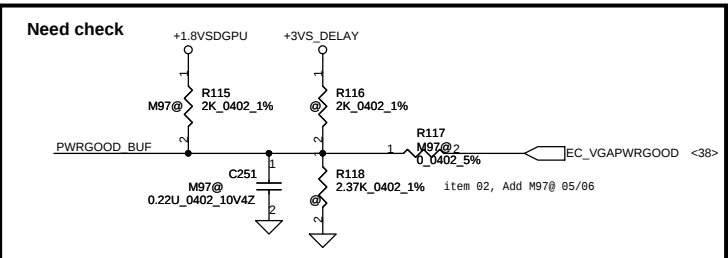
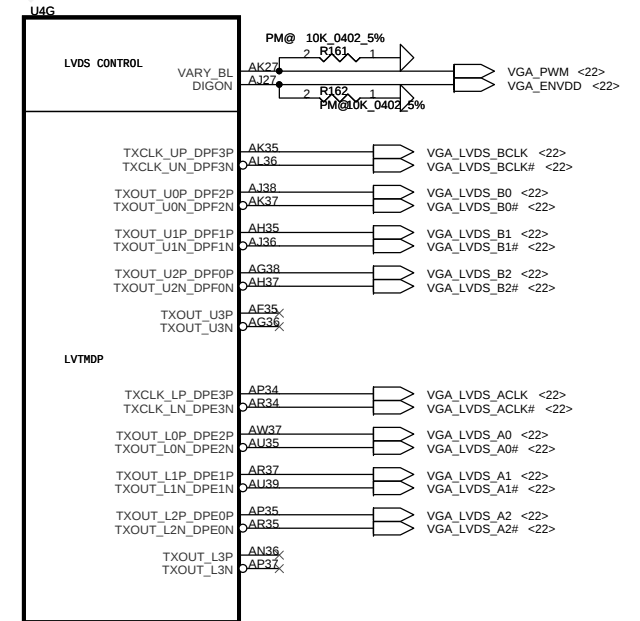


U4
SA00002UQ50
216-0729042 A13 M96-M2 FCBGA962 0FA
M96@

U4
SA00003M320
216-0772000 A11 MADISON PRO 030
MADVGA@

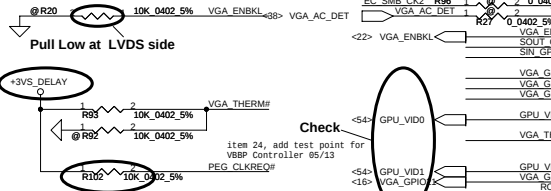
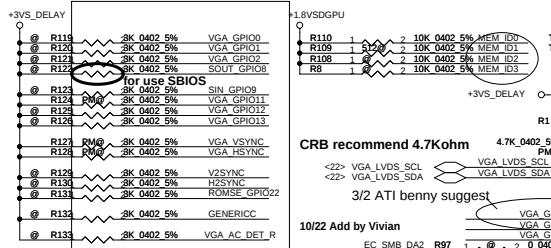
U4
SA00003MC20
216-0774007 A11 PARK XT M2 962P 030
PARKVGA@

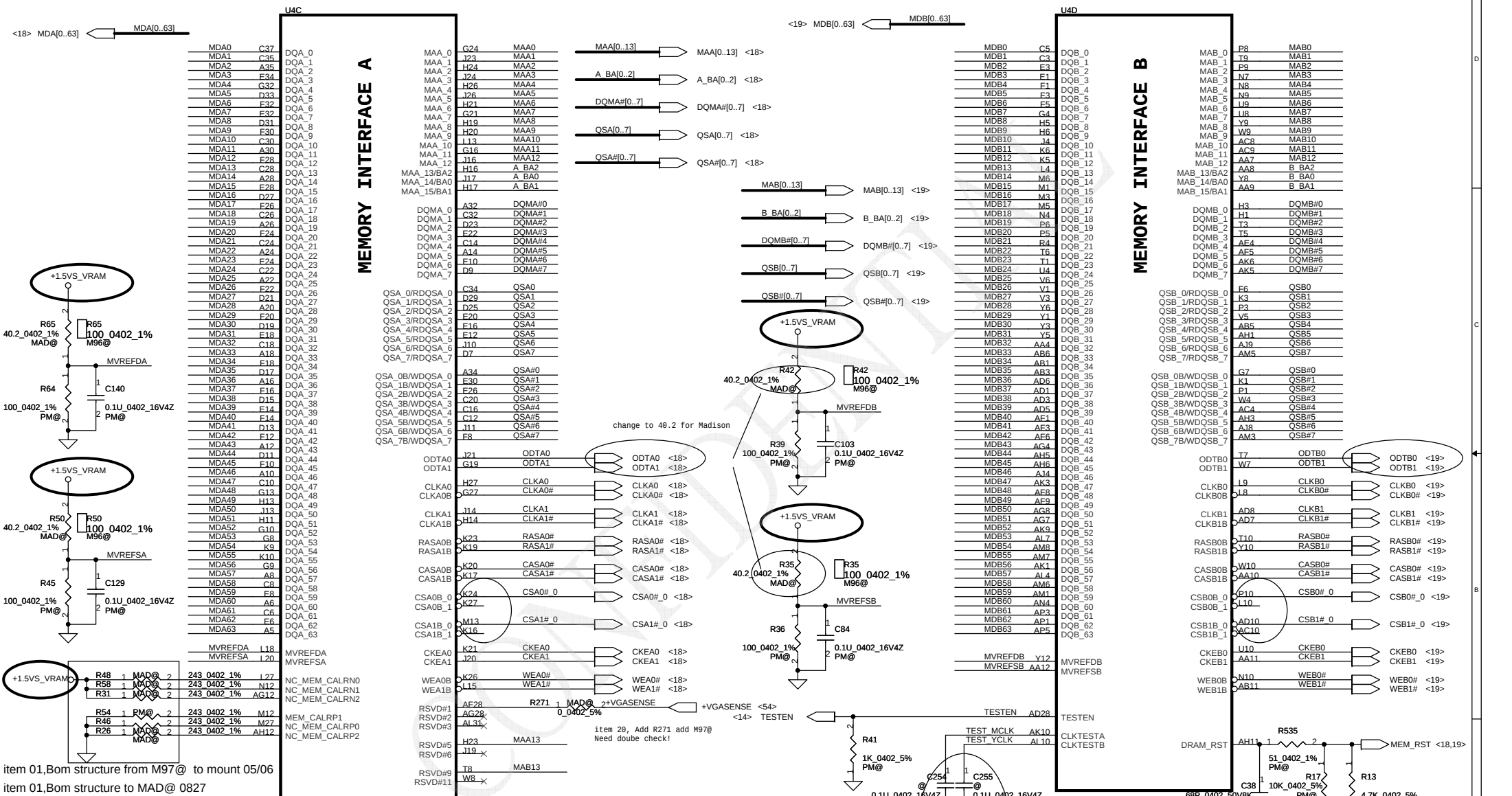
the same with M86



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Strap Name	Pin Straps description	Default Value
TX_PWRS_EN#	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN#	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2 0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
GPIO23 GPIO21	Reserved	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11 a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1
GENERICC H2SYNC	Reserved	0
VIP_DEVICE STRAP_EN	V2SYNC Reserved	0



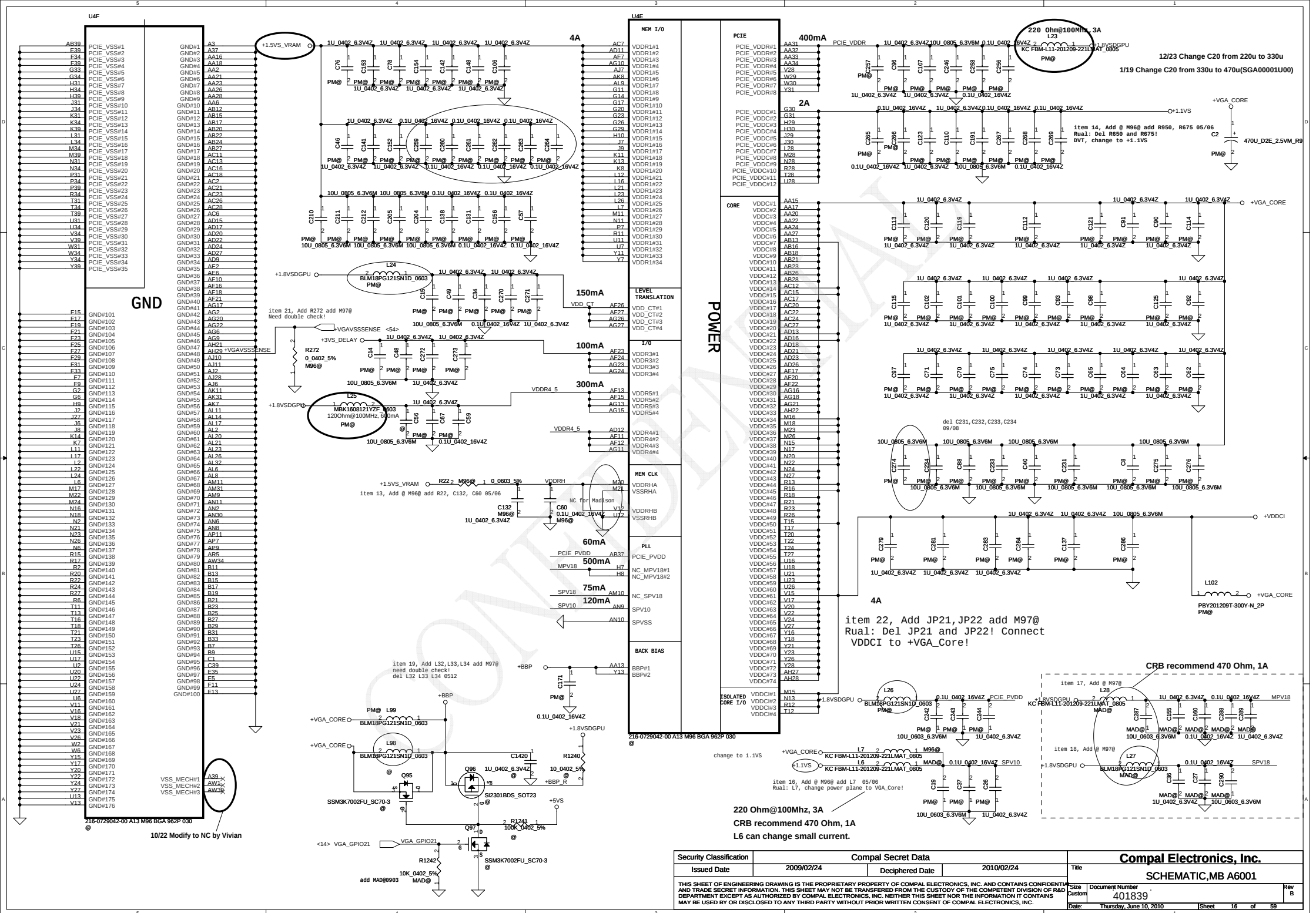


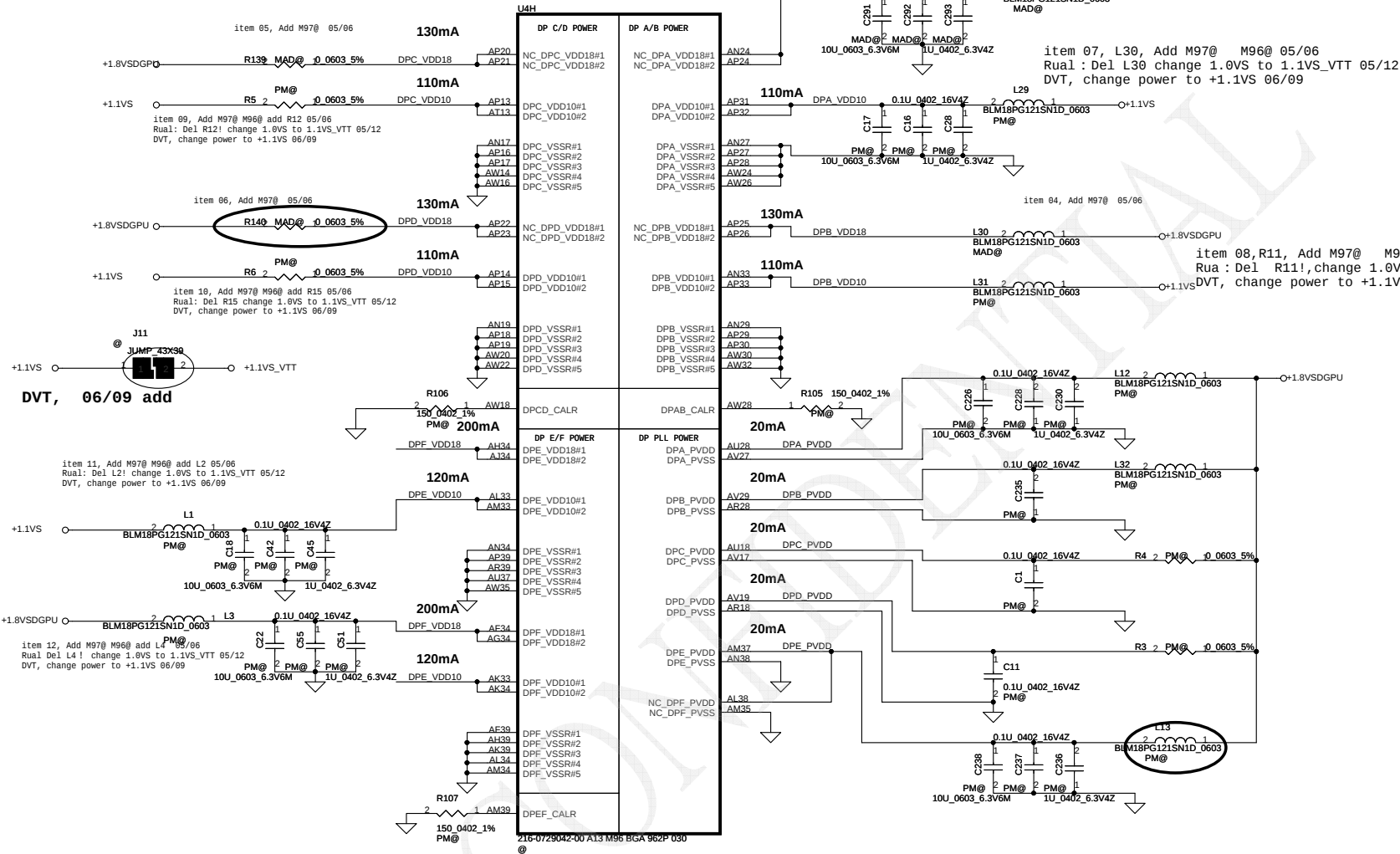
item 01,Bom structure from M97@ to mount 05/06
item 01,Bom structure to MAD@ 0827

Note:
route 50ohms single-ended/100ohms diff
and keep short
REF137-03 suggest

4/24 ATI suggest

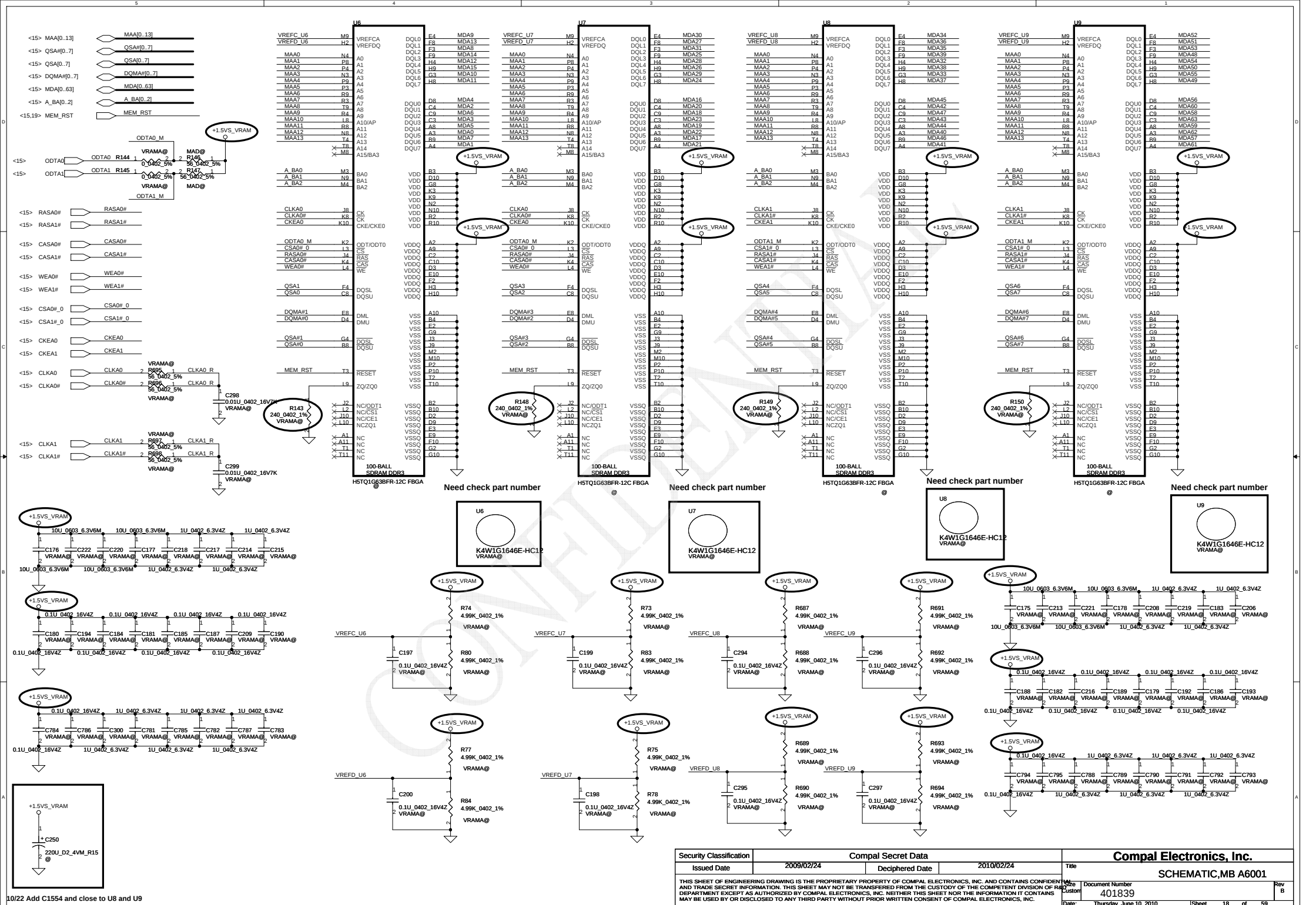
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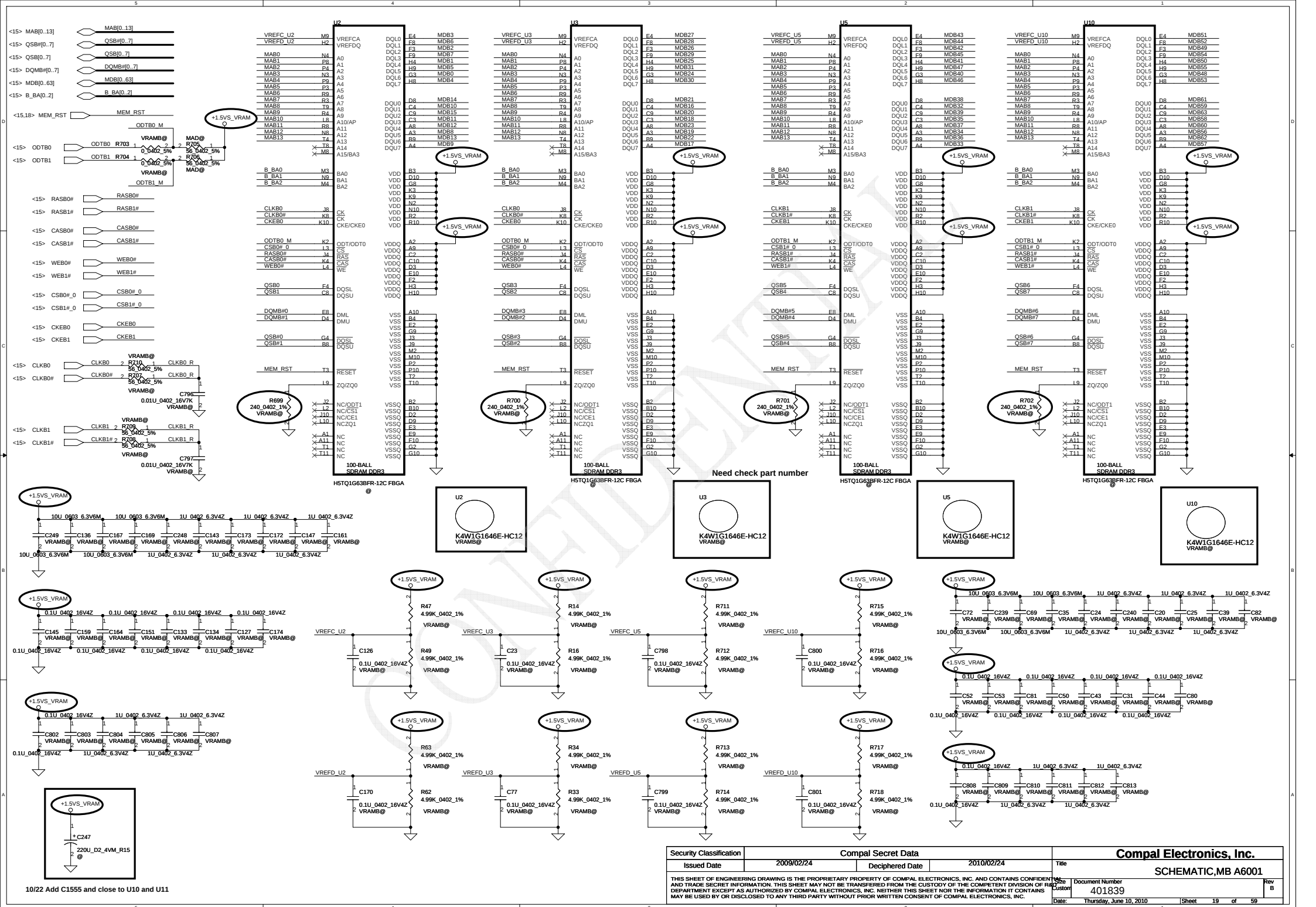




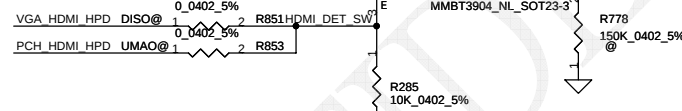
There is no use on DPB/DPC/DPD,DPB_VDD10, DPC_VDD10, DPD_VDD10, DPB_PVDD, DPC_PVDD and DPD_PVDD can be powered without filter

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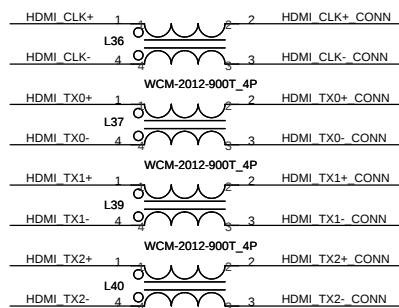




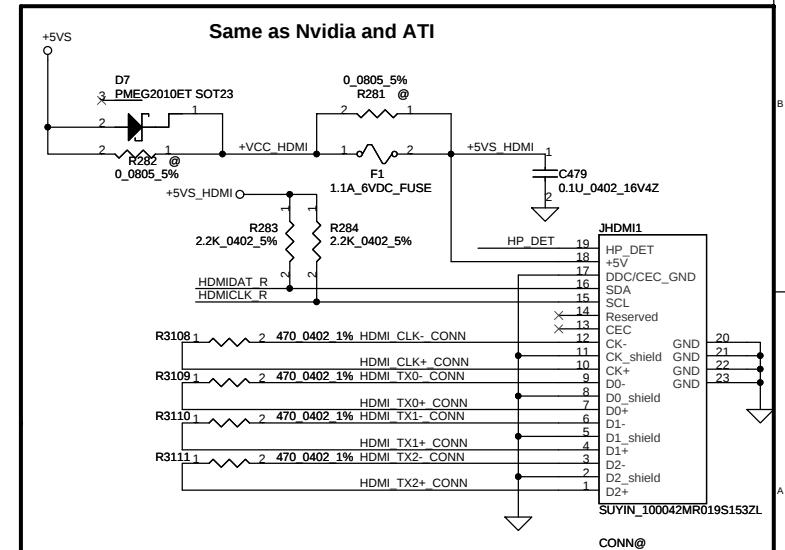
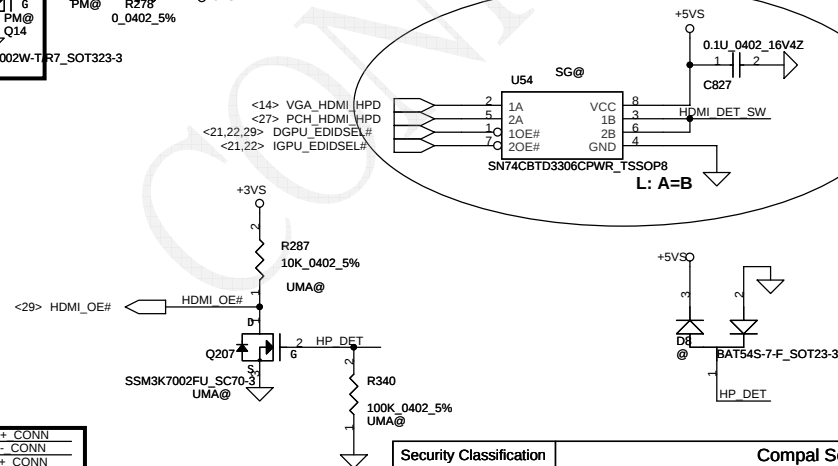
The schematic diagram illustrates the HDMI output circuitry. It features four transistors: Q2050A and Q2050B (NMOS) at the top, and Q38A and Q38B (NMOS) at the bottom. The input signals are DGPU_EDIDSEL# and IGPU_EDIDSEL#. The output signals are HDMI_SDA and HDMI_SCL. The circuit includes several resistors: R418 and R424 (pull-up resistors for the input signals), R855 and R866 (pull-up resistors for the output signals), and R842 and R843 (pull-up resistors for the input signals). The power supply connections are +3V0, +3V5_DELAY, and 12P_0402_50V8. The schematic also shows the connection of the HDMI_SDA and HDMI_SCL signals to the HDMI output pins.



VGA HDMI C CLK+	R269	1	2	PM@ 499_0402_1%
VGA HDMI C CLK-	R270	1	2	PM@ 499_0402_1%
VGA HDMI C TX0+	R273	1	2	PM@ 499_0402_1%
VGA HDMI C TX0-	R274	1	2	PM@ 499_0402_1%
VGA HDMI C TX1+	R275	1	2	PM@ 499_0402_1%
VGA HDMI C TX1-	R276	1	2	PM@ 499_0402_1%
VGA HDMI C TX2+	R279	1	2	PM@ 499_0402_1%
VGA HDMI C TX2-	R280	1	2	PM@ 499_0402_1%



WCM-2012-900T 4P						
HDMI CLK+	Ⓢ	R288	1	2	0.0402 5%	HDMI CLK+ CONN
HDMI CLK-	Ⓢ	R289	1	2	0.0402 5%	HDMI CLK- CONN
HDMI TX0+	Ⓢ	R290	1	2	0.0402 5%	HDMI TX0+ CONN
HDMI TX0-	Ⓢ	R291	1	2	0.0402 5%	HDMI TX0- CONN
HDMI TX1+	Ⓢ	R292	1	2	0.0402 5%	HDMI TX1+ CONN
HDMI TX1-	Ⓢ	R293	1	2	0.0402 5%	HDMI TX1- CONN
HDMI TX2+	Ⓢ	R294	1	2	0.0402 5%	HDMI TX2+ CONN
HDMI TX2-	Ⓢ	R295	1	2	0.0402 5%	HDMI TX2- CONN



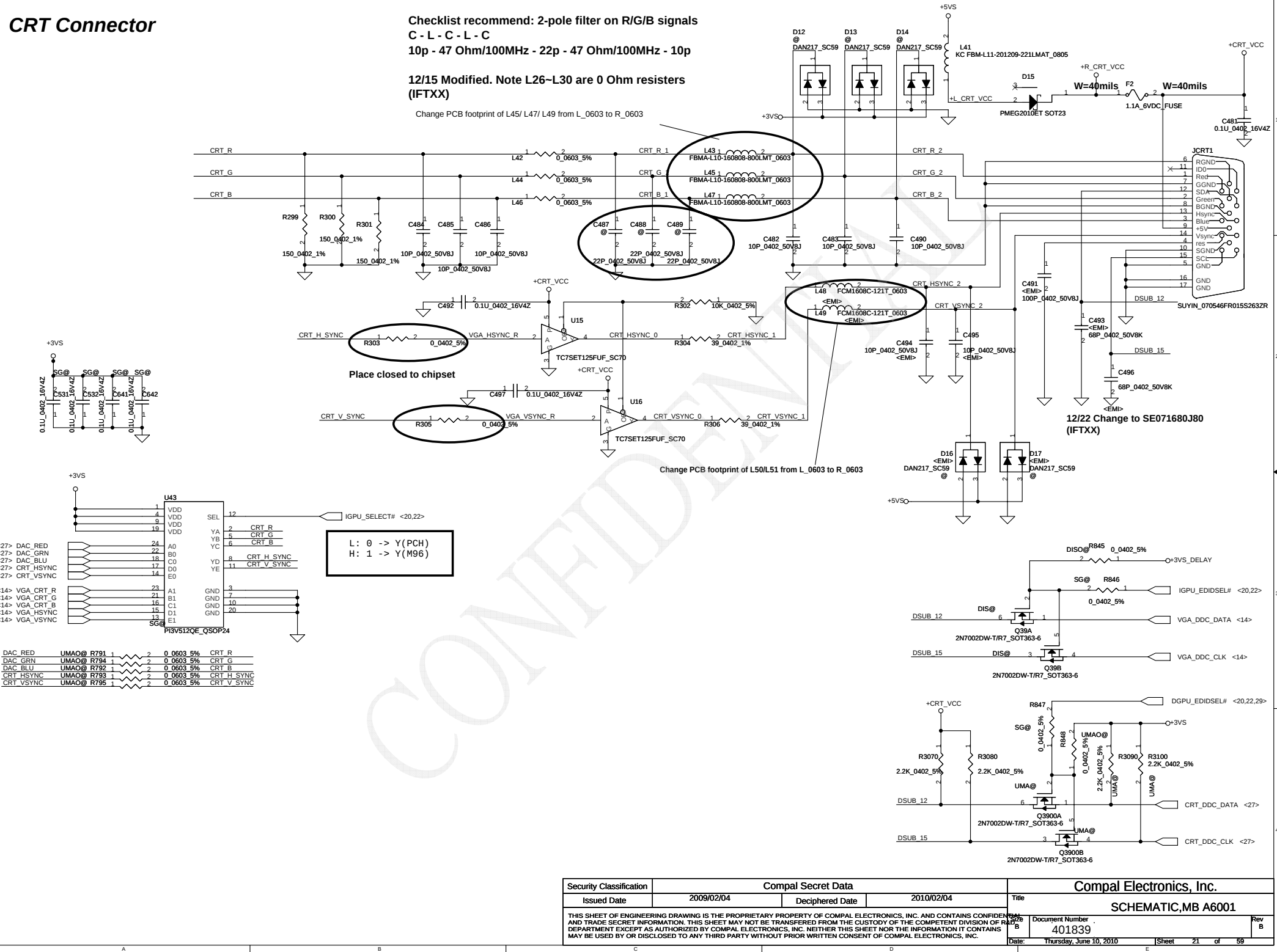
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CRT Connector

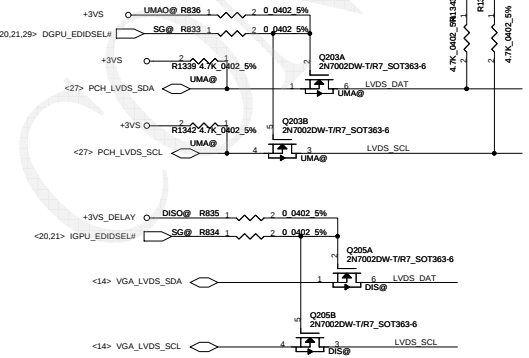
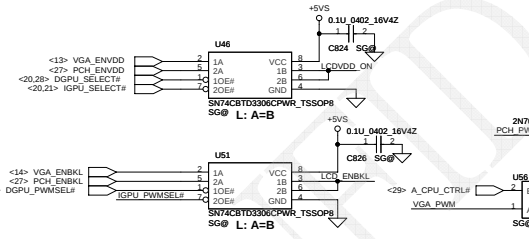
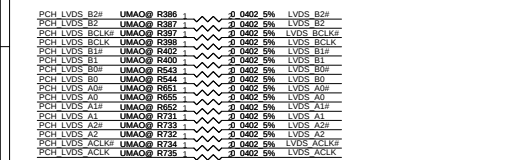
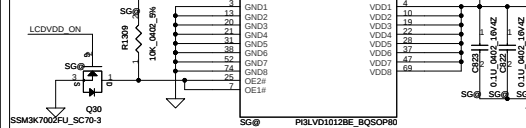
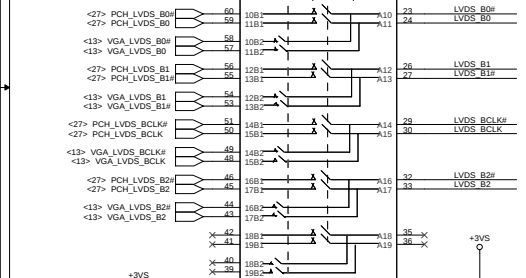
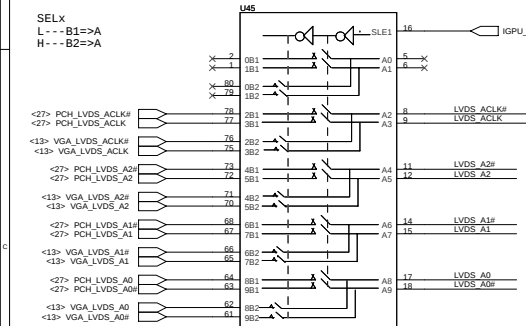
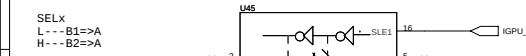
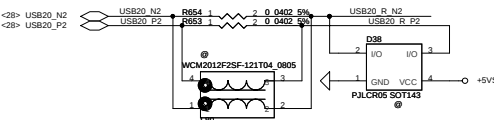
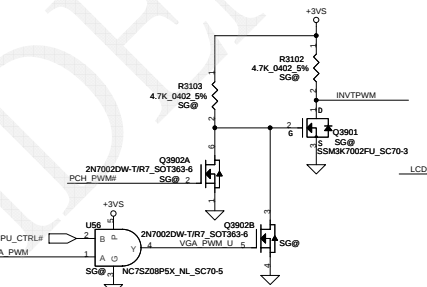
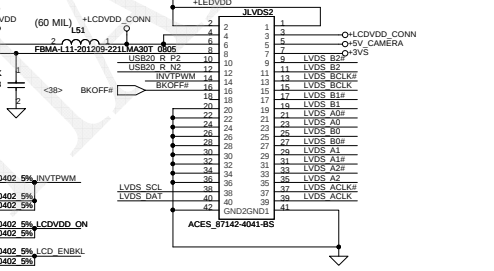
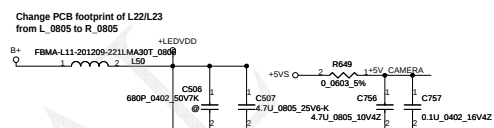
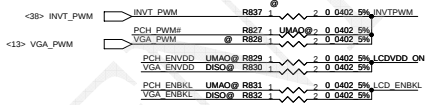
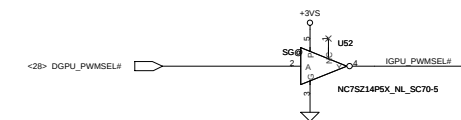
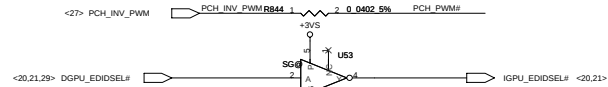
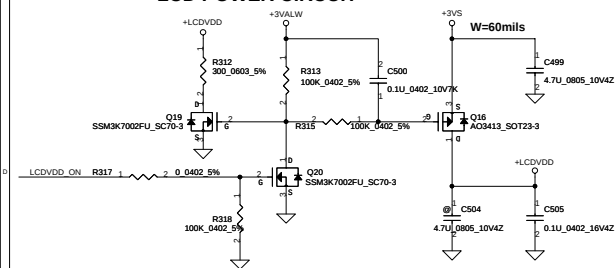
Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resistors (IFTXX)

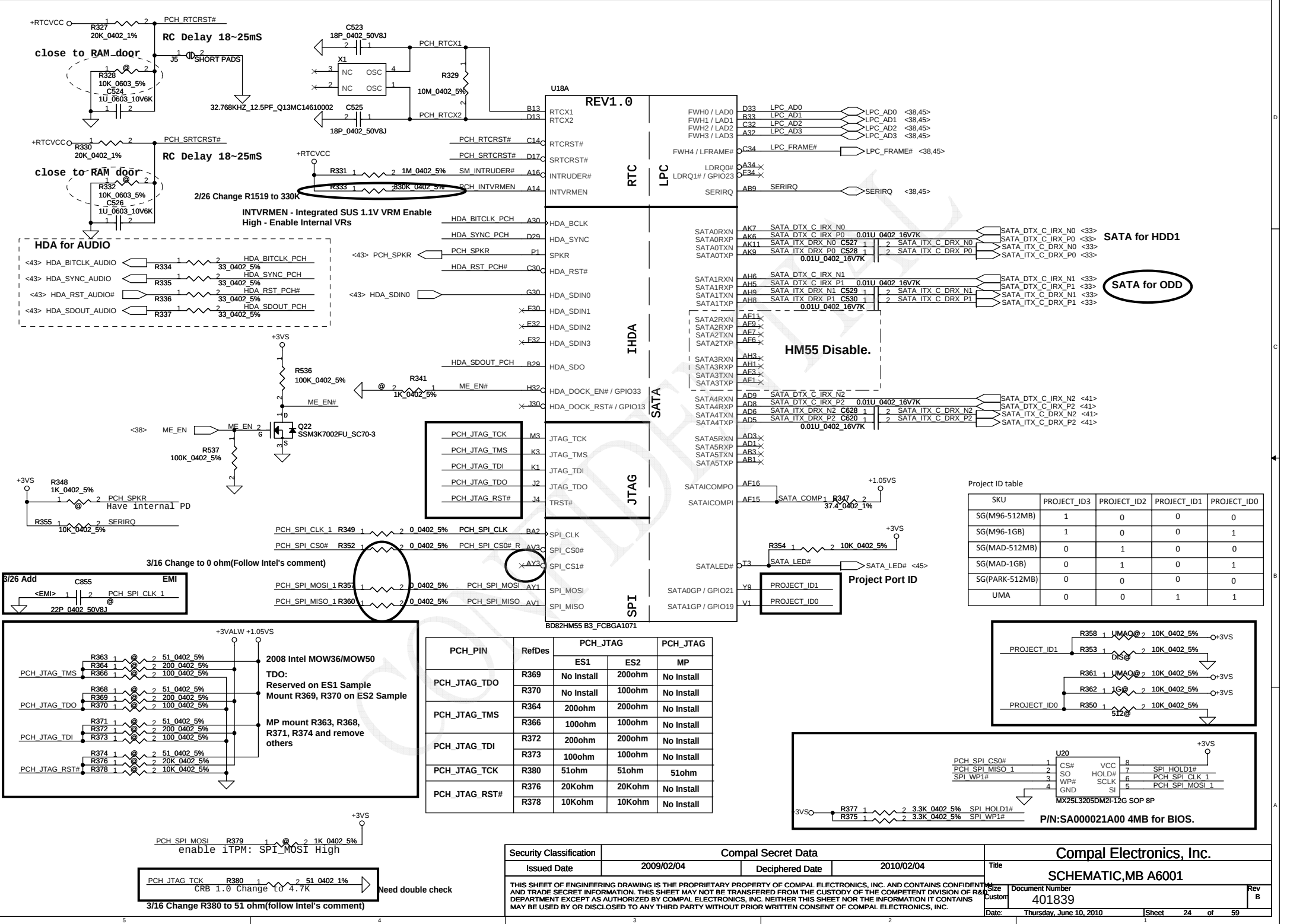
Change PCB footprint of L45/ L47/ L49 from L_0603 to R_0603



LCD POWER CIRCUIT

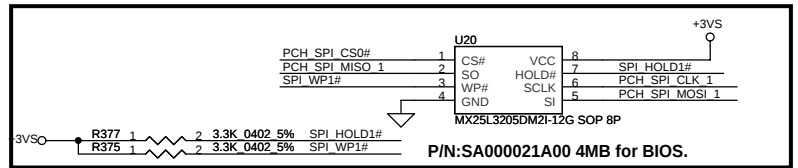
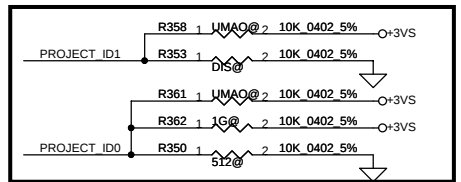


	Arrandale	Clarksfield
A_CPU_CTRL#	0	1



PCH_PIN	RefDes	PCH_JTAG		
		ES1	ES2	MP
PCH_JTAG_TDO	R369	No Install	200ohm	No Install
	R370	No Install	100ohm	No Install
PCH_JTAG_TMS	R364	200ohm	200ohm	No Install
	R366	100ohm	100ohm	No Install
PCH_JTAG_TDI	R372	200ohm	200ohm	No Install
	R373	100ohm	100ohm	No Install
PCH_JTAG_TCK	R380	51ohm	51ohm	51ohm
	R376	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R378	10Kohm	10Kohm	No Install

Project ID table				
SKU	PROJECT_ID3	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
SG(M96-512MB)	1	0	0	0
SG(M96-1GB)	1	0	0	1
SG(MAD-512MB)	0	1	0	0
SG(MAD-1GB)	0	1	0	1
SG(PARK-512MB)	0	0	0	0
UMA	0	0	1	1



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										Custom	401839			
										Date:	Thursday, June 10, 2010			
										Sheet	24		of 59	
		3				2				1				

For Wireless LAN

For PCIE LAN

For Wireless LAN

For PCIE LAN

REV1.0

PCI-E*

From CLK BUFFER

CLKOUT FLEX

Project ID		
ID1	ID0	Project
0	0	Future
0	1	JV

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1. Connect Directly EXPRESS CARD, MINI12
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

Buffer Mode check is need or not

3/20 Remove by Vivian

4/2 Add by Vivian

3/16 Change R408/R409 to 2.2K ohm(follow Intel's comment)

3/16 Add R761/R762 to 2.2K ohm(follow Intel's comment)

<5> DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
<5> DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
<5> DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
<5> DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

U18C

REV1.0

DMI_HTX_PRX_N0 BC24
DMI_HTX_PRX_N1 BJ22
DMI_HTX_PRX_N2 AW20
DMI_HTX_PRX_N3 BJ20

DMI_HTX_PRX_P0 BD24
DMI_HTX_PRX_P1 BC22
DMI_HTX_PRX_P2 BA20
DMI_HTX_PRX_P3 BG20

DMI_PTX_HRX_N0 BE22
DMI_PTX_HRX_N1 BE21
DMI_PTX_HRX_N2 BD20
DMI_PTX_HRX_N3 BE18

DMI_PTX_HRX_P0 BD22
DMI_PTX_HRX_P1 BH21
DMI_PTX_HRX_P2 BC20
DMI_PTX_HRX_P3 BD18

DMIORXN
DMI1RXN
DMI2RXN
DMI3RXN
DMIORXP
DMI1RXP
DMI2RXP
DMI3RXP
DMIOTXN
DMI1TXN
DMI2TXN
DMI3TXN
DMIOTXP
DMI1TXP
DMI2TXP
DMI3TXP

FDI_RXN0
FDI_RXN1
FDI_RXN2
FDI_RXN3
FDI_RXN4
FDI_RXN5
FDI_RXN6
FDI_RXN7

FDI_RXP0
FDI_RXP1
FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7

FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

BA18 FDI_CTX_PRX_N0
BH17 FDI_CTX_PRX_N1
BD16 FDI_CTX_PRX_N2
BI16 FDI_CTX_PRX_N3
BA16 FDI_CTX_PRX_N4
BE14 FDI_CTX_PRX_N5
BA14 FDI_CTX_PRX_N6
BC12 FDI_CTX_PRX_N7

BB18 FDI_CTX_PRX_P0
BE17 FDI_CTX_PRX_P1
BC16 FDI_CTX_PRX_P2
BG16 FDI_CTX_PRX_P3
AW16 FDI_CTX_PRX_P4
BD14 FDI_CTX_PRX_P5
BH14 FDI_CTX_PRX_P6
BD12 FDI_CTX_PRX_P7

08/20 ADD
FDI for SG

FDI_CTX_PRX_N[0..7] <5>
FDI_CTX_PRX_P[0..7] <5>

System Power Management

<6> XDP_DBRESET# XDP_DBRESET# T6

SYS_PWROK R426 2 1 0 0402 5% SYS_PWROK R M6
VGATE R427 2 1 0 0402 5%

SYS_PWROK B17
MEPWROK K5

LAN_RST# A10
LAN_RST# A10

<6> PM_DRAM_PWRGD# D9
DRAMPWROK D9

PCH_RSMRST# C16
RSMRST# C16

<38> SUS_PWR_ACK M1
SUS_PWR_ACK M1

10/2 Intel suggestion change to 10K

<38> PBTN_OUT# P5
PBTN_OUT# P5

<38> EC_ACIN CH751H-40PT_SOD323-2
PCH_ACIN P7

PCH_GPIO72 A6
PCH_GPIO72 A6

<38> EC_SWI# F14
EC_SWI# F14

BD82HM55 B3_FCBGA1071

R725 2 1 0 0402 5%

VR_ON VR_ON_EC <38>
PWR_GD <42>

NC7S208P5X_NL_SC70-5

VR_ON VR_ON_EC <38>
PWR_GD <42>

NC7S208P5X_NL_SC70-5

VR_ON VR_ON_EC <38>
PWR_GD <42>

NC7S208P5X_NL_SC70-5

VR_ON VR_ON_EC <38>
PWR_GD <42>

NC7S208P5X_NL_SC70-5

VR_ON VR_ON_EC <38>
PWR_GD <42>

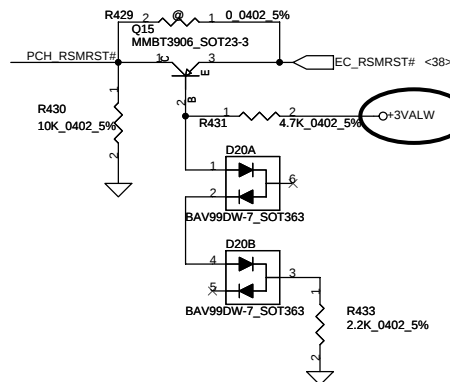
NC7S208P5X_NL_SC70-5

SYS_PWROK R434 1 2 10K_0402 5%
ICH_PWROK R435 1 2 10K_0402 5%
LAN_RST# R436 1 2 10K_0402 5%

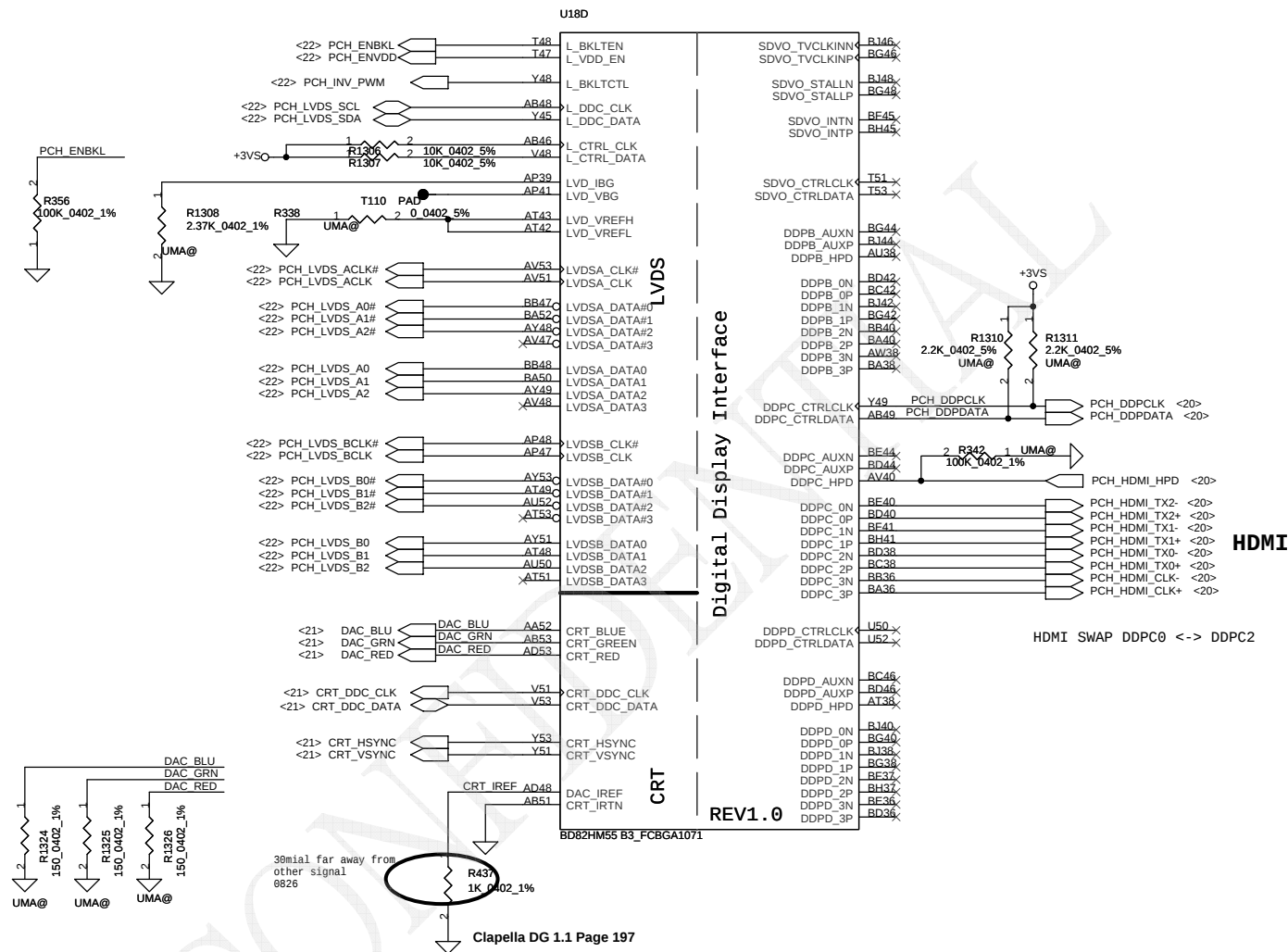
No used Integrated LAN,
connecting LAN_RST# to GND

4/2 Add by Vivian

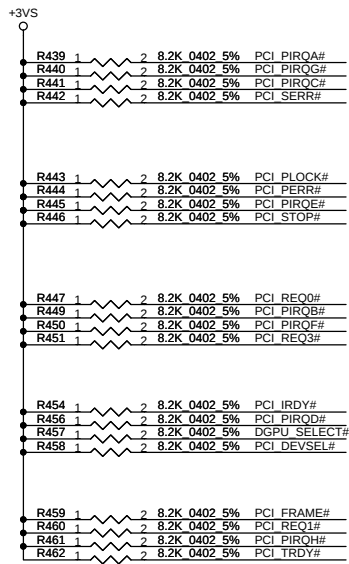
VGATE C866 1 2 100P_0402 50V8J
H PM SYNC C867 1 2 100P_0402 50V8J
PBTN_OUT# C868 1 2 100P_0402 50V8J
VR_ON C862 1 2 100P_0402 50V8J



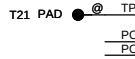
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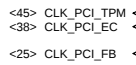
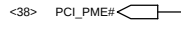
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DIS GPU select, low active
L: to VGA chip
H: to PCH

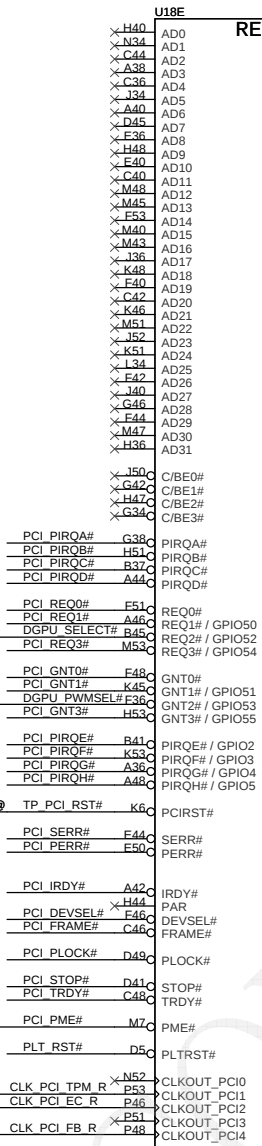


modify on 08/20



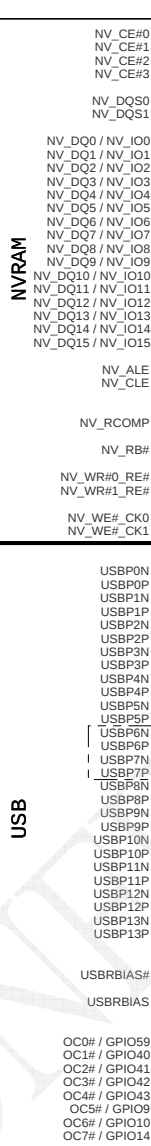
2008/1/6 2009MOW01 change to 22 ohm

REV1.0



PCI

USB



CheckList1.0 1.23.2
Braidwood Disable

3/16 Follow Intel's comment

HM55 Disable.

Camera

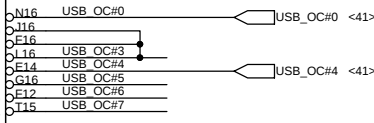
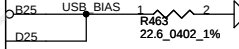
USB(I/O B)

USB(I/O B)

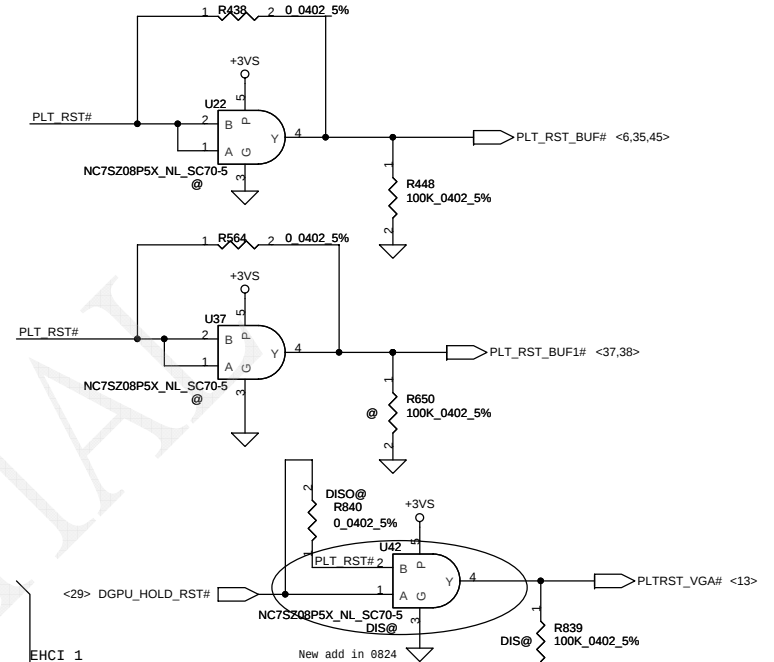
USB 2(I/O/B)

BT

CardReader



OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

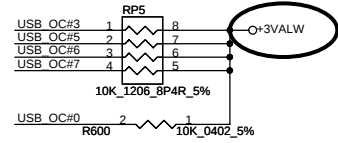


EHCI 1

EHCI 2

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

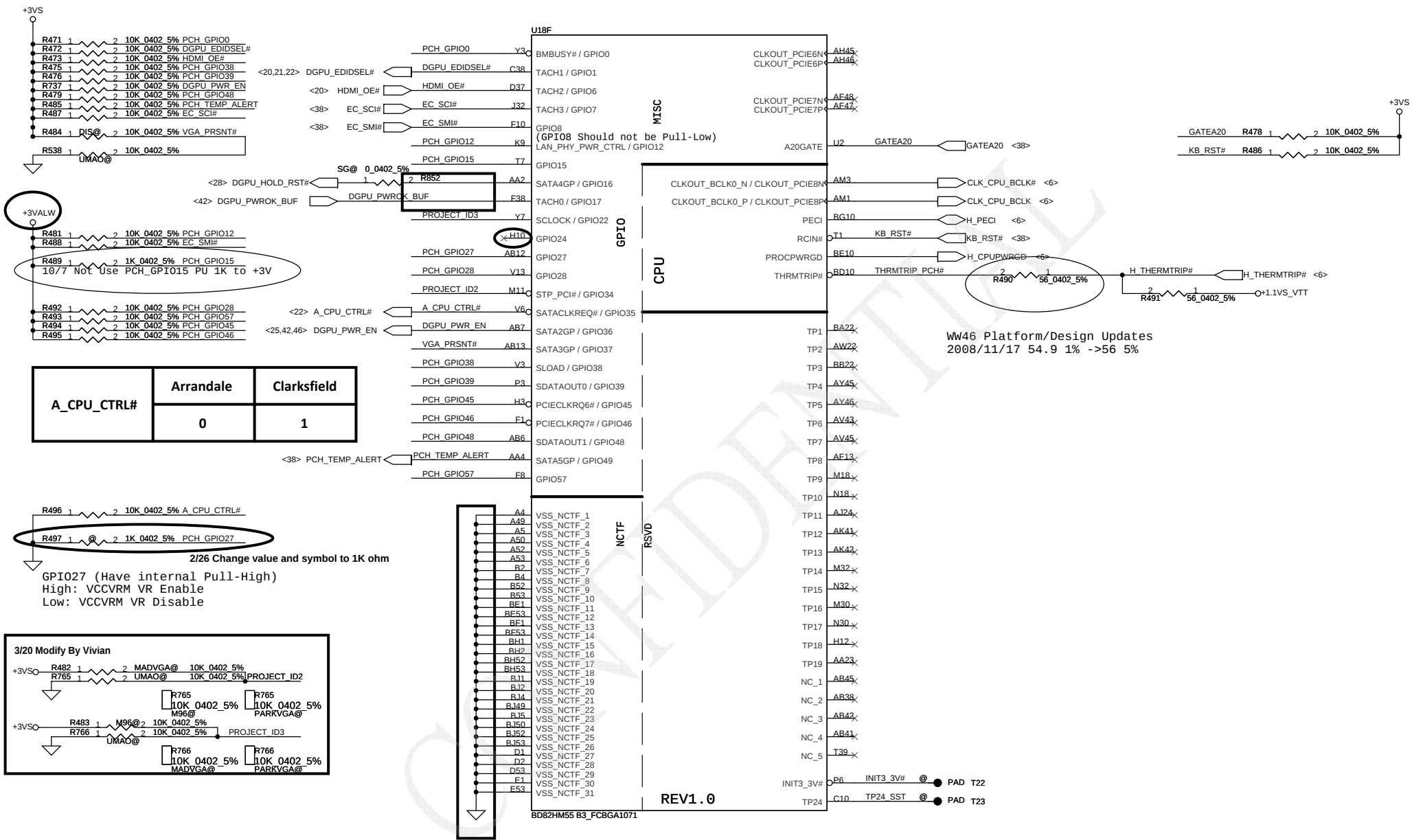
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

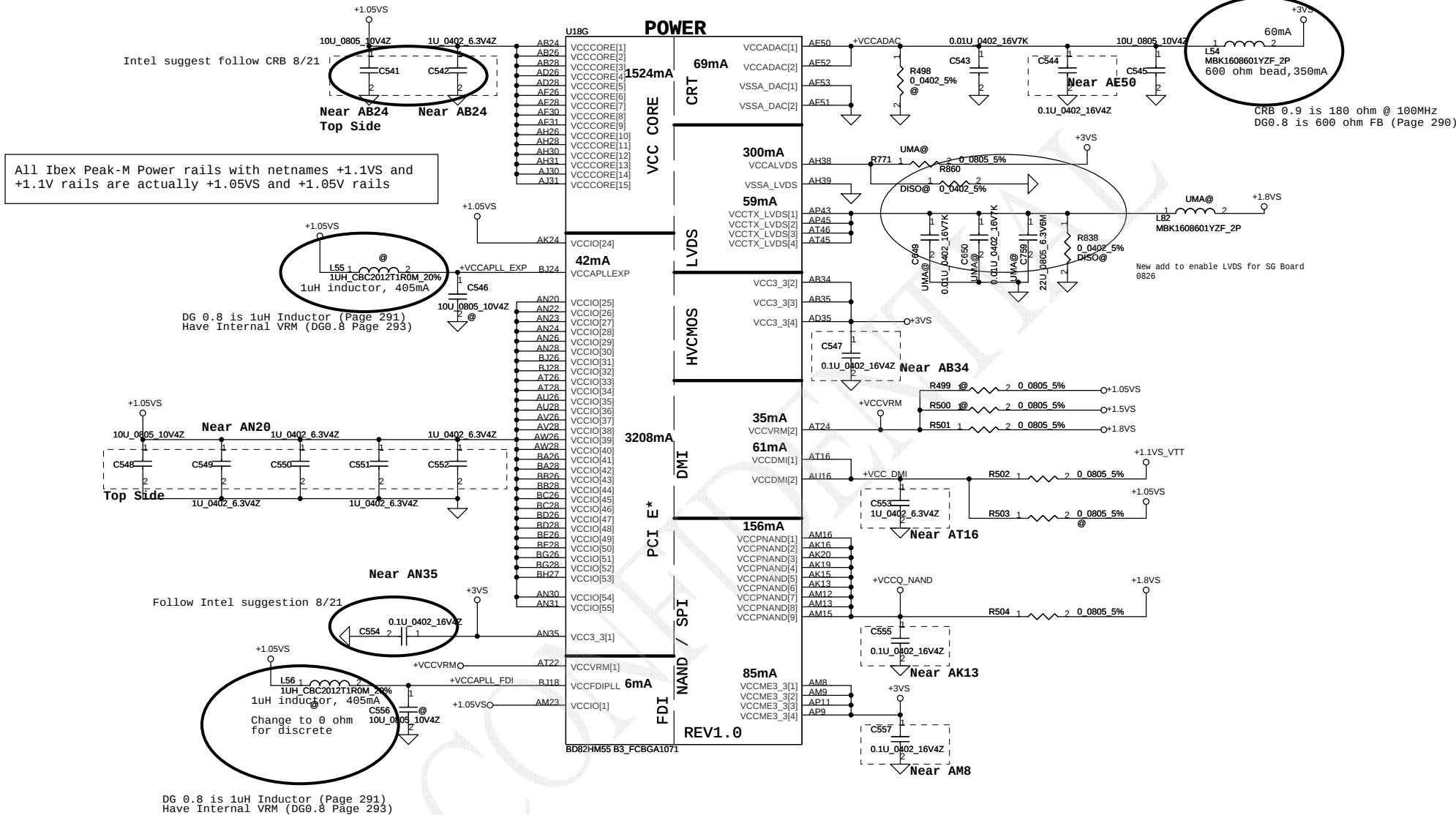


Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

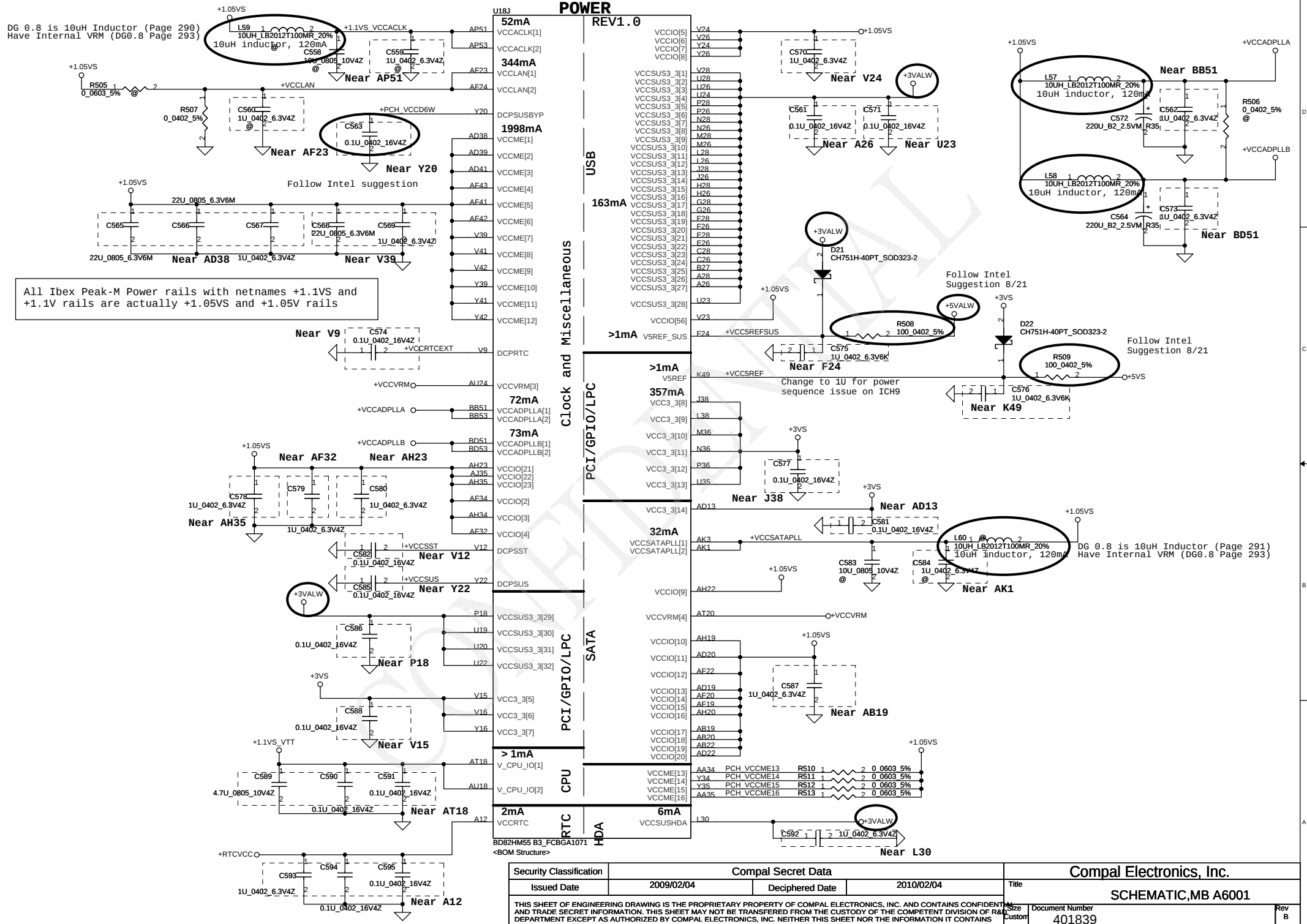
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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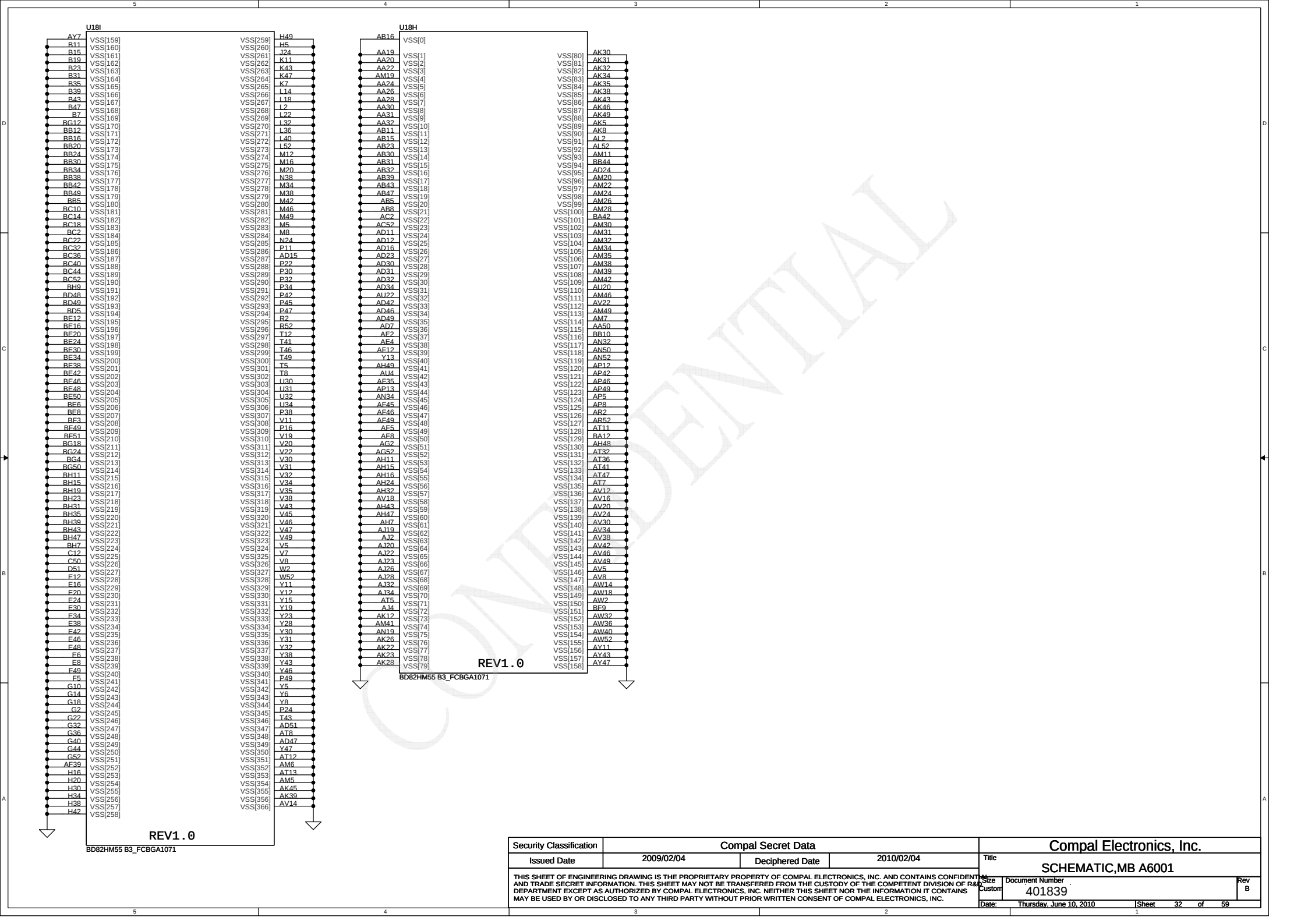




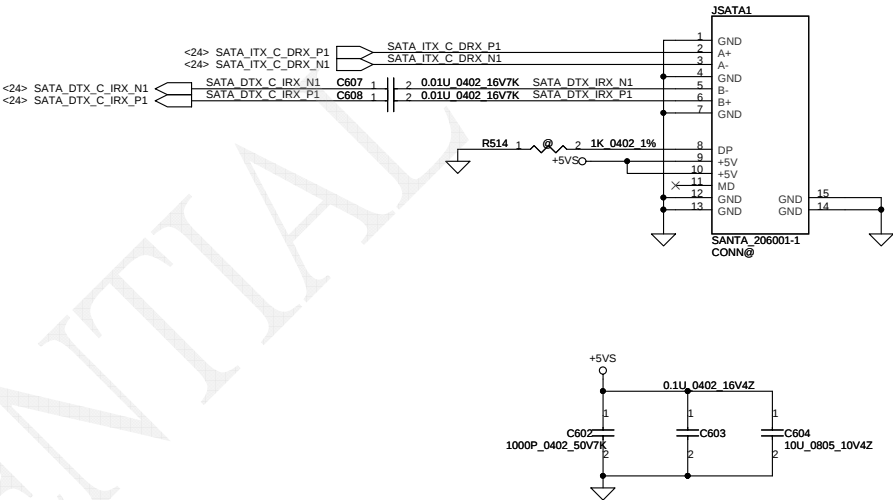
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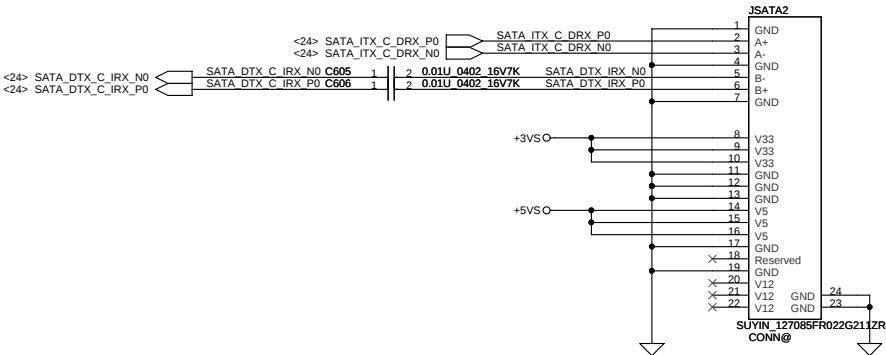
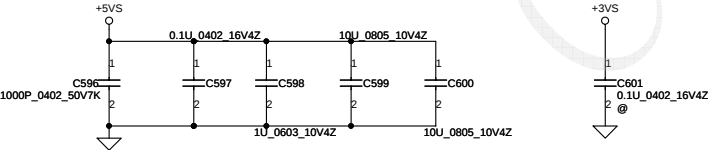
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				Customer	Document Number	B
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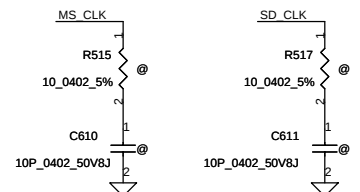
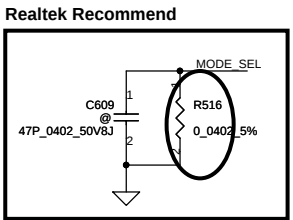
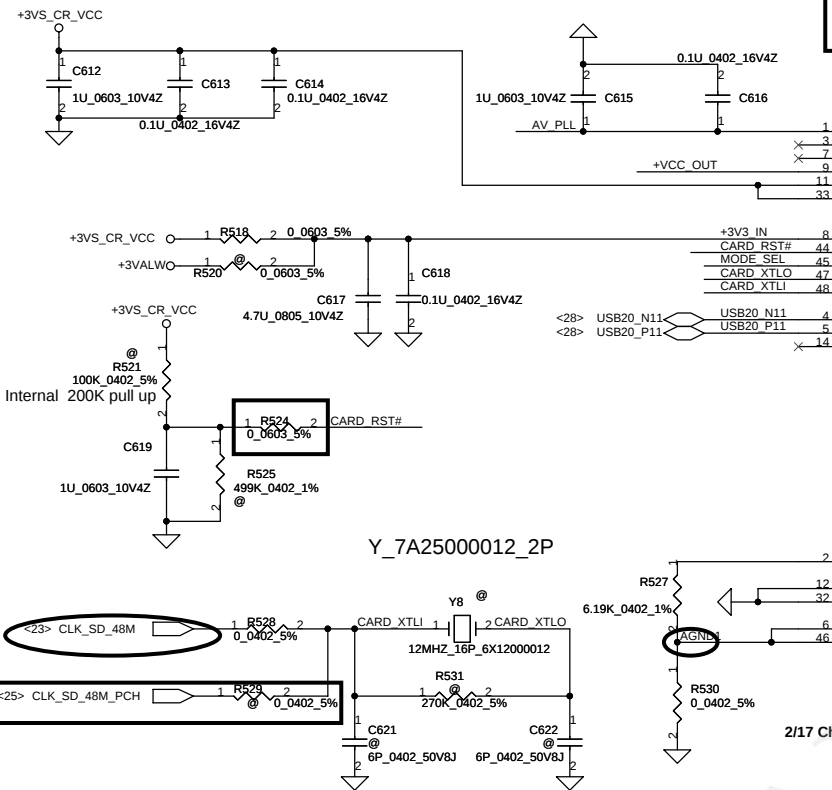
SATA ODD Conn.



SATA HDD Conn.



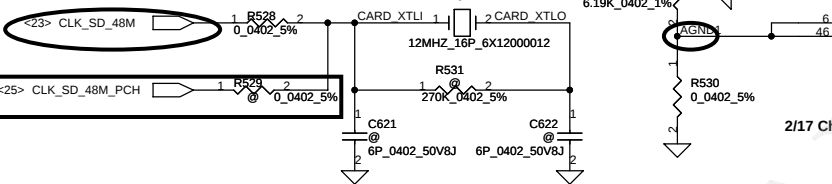
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AV_PLL 20mil (+1.8V internal regulator)

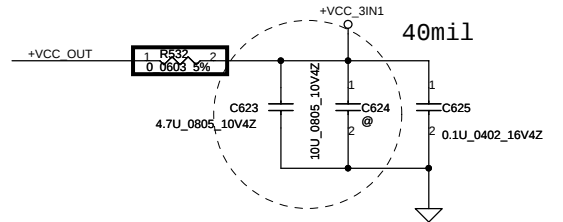
SD, MMC, MS multi-function pin define

MD10 PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			

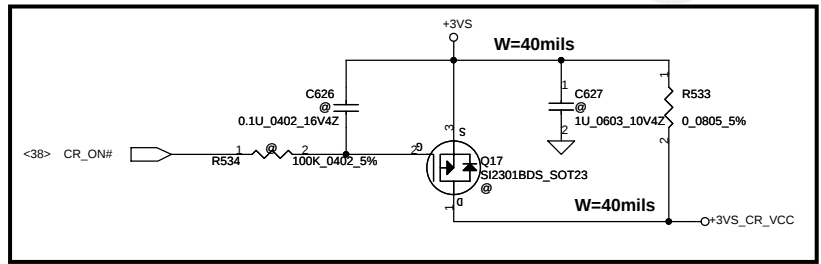
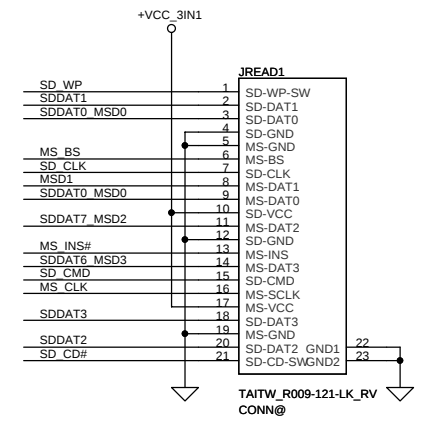


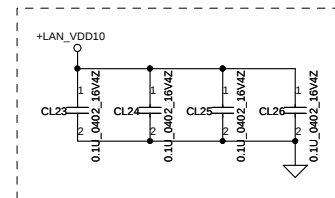
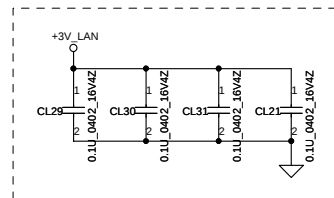
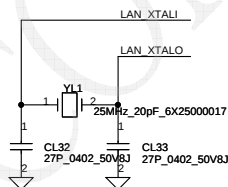
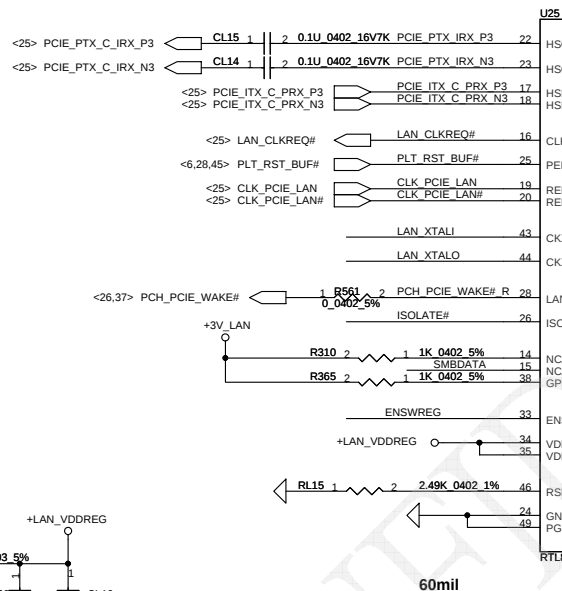
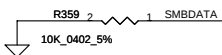
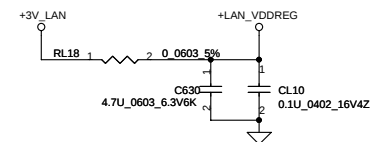
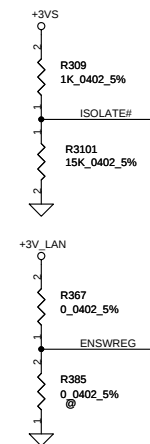
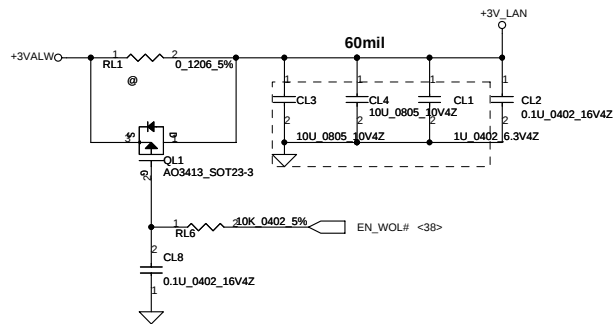
SIC RT55159-GR LQFP 48P CARD READER

2/17 Change Part number of U25 from SA00001NK10 to SA00002YP00



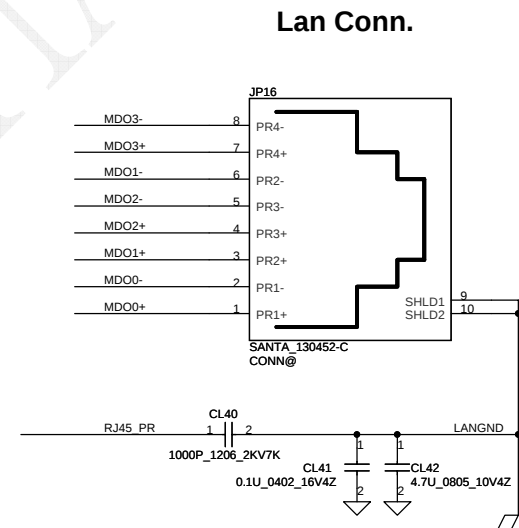
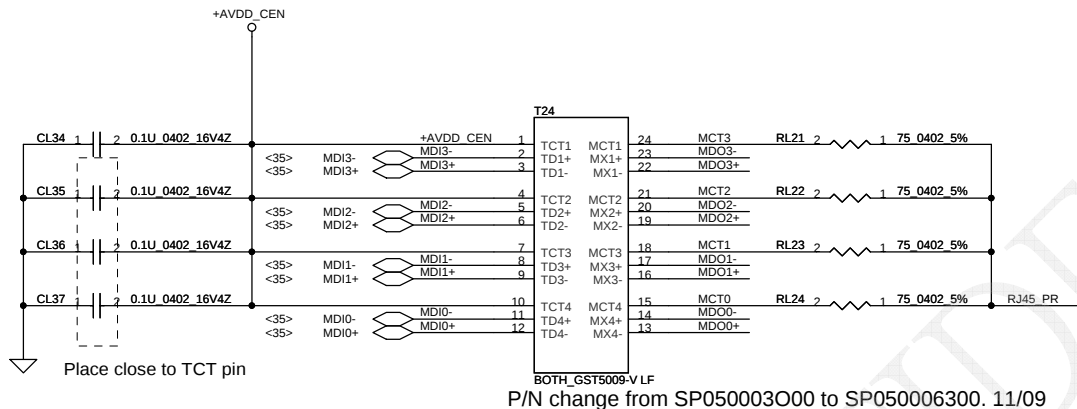
Add C822 4.7u and reserve C808 18u for cost down Michael 2008/5/30





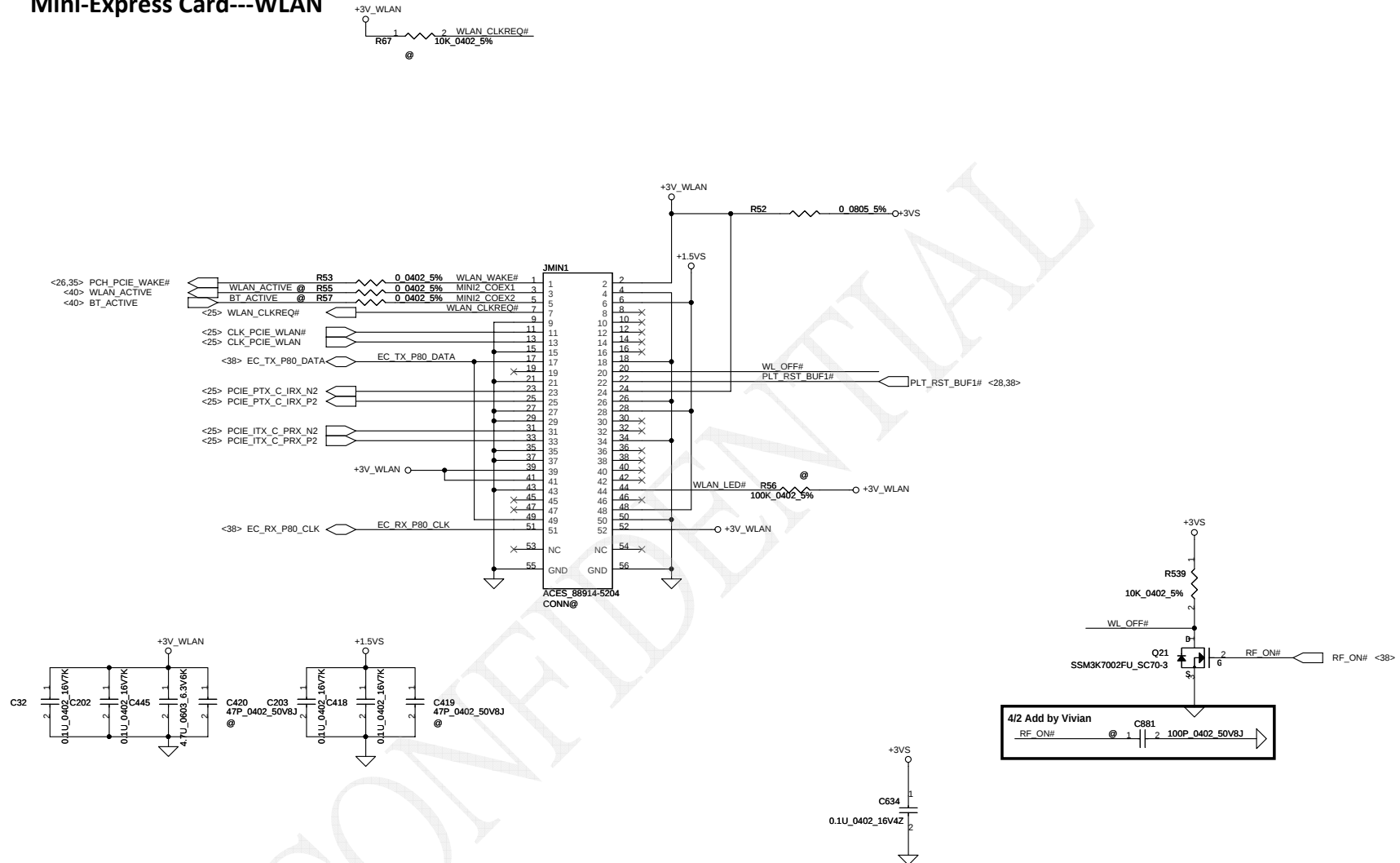
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SCHEMATIC,MB A6001



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				Custom	B
				Document Number	401839
				Date:	Sheet 36 of 59

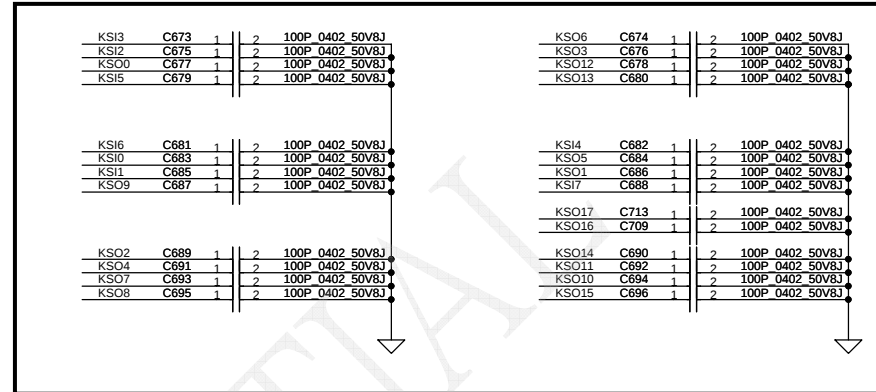
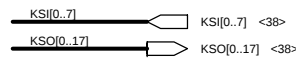
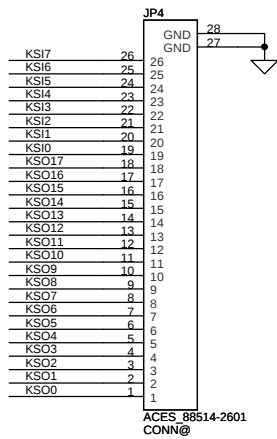
Mini-Express Card---WLAN



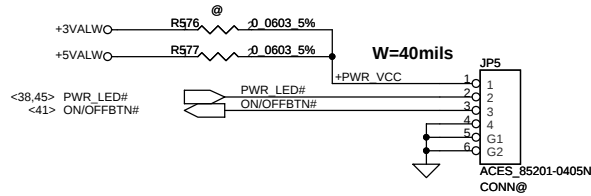
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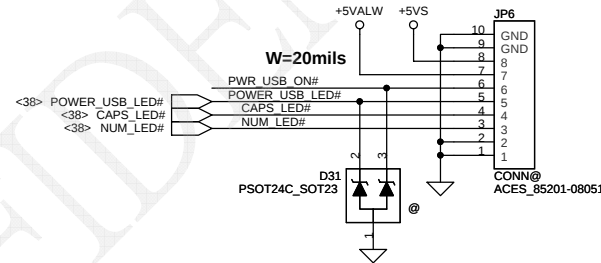
INT_KBD Conn.



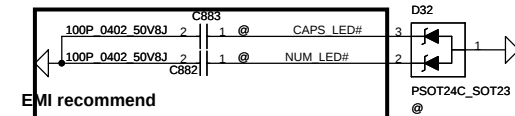
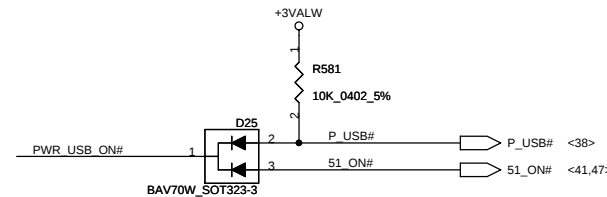
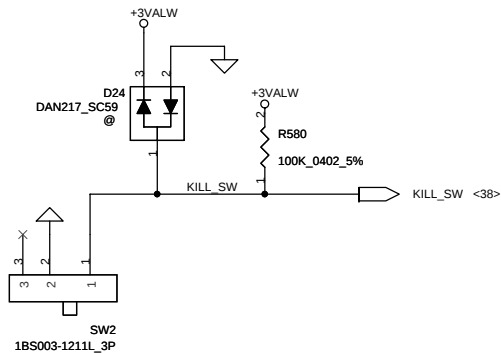
Power BTN Board Conn



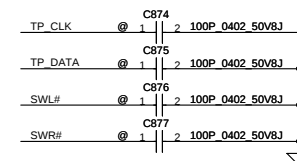
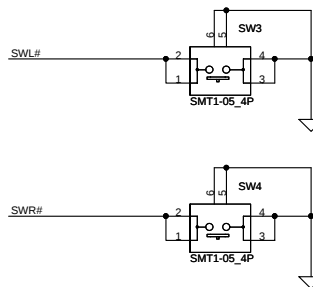
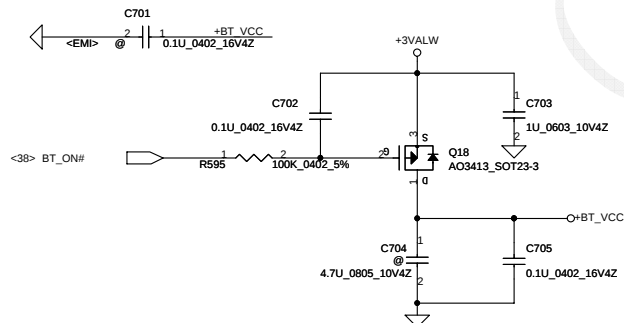
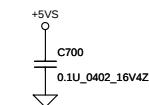
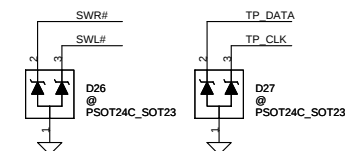
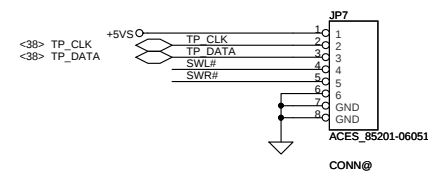
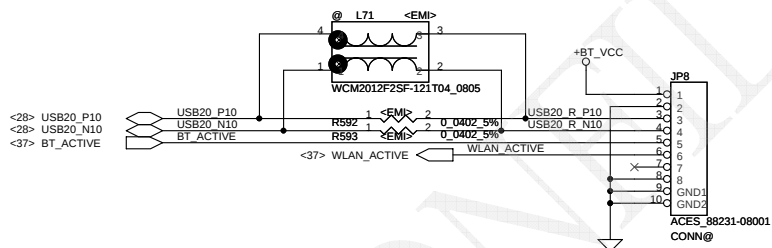
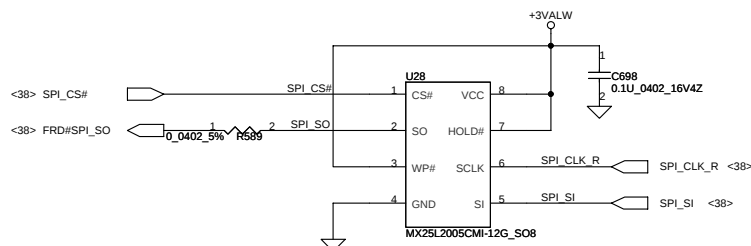
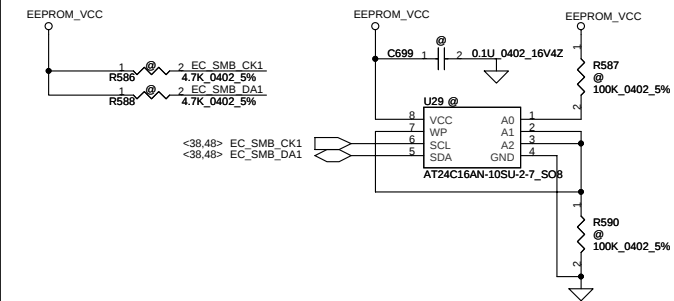
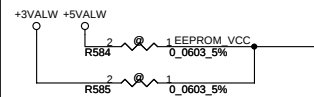
Function board conn



Kill SWITCH



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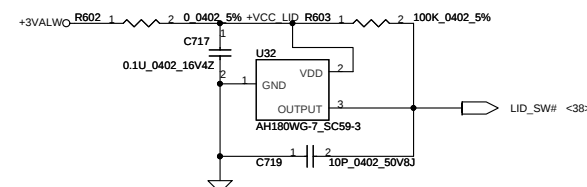
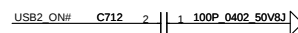
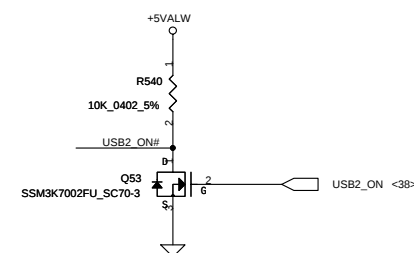
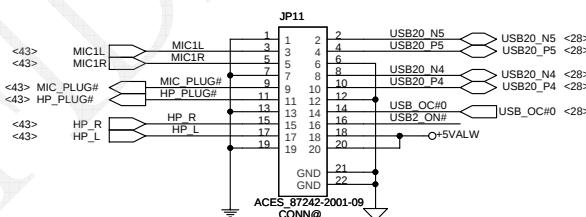
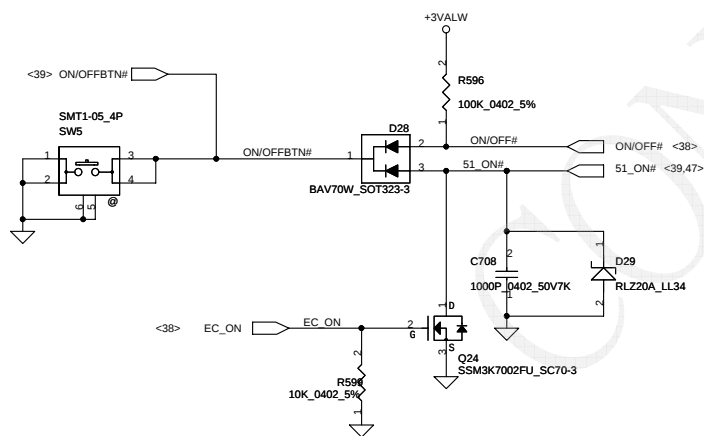
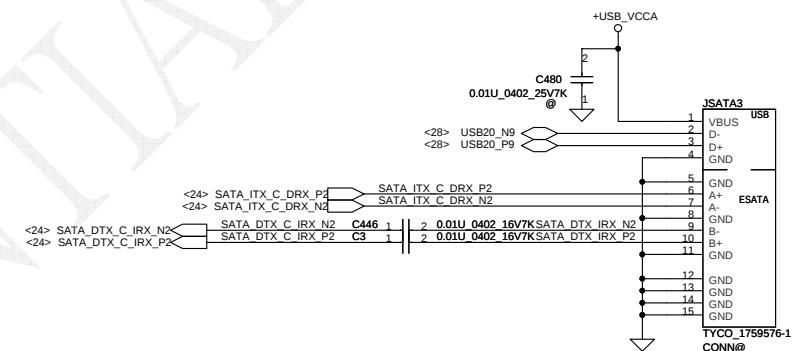
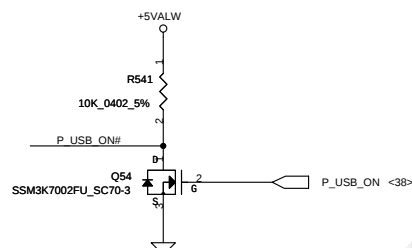
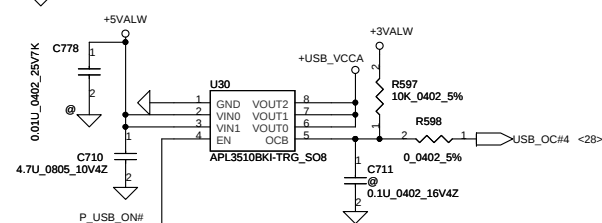
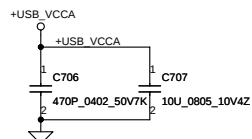
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APL3510
APL3511

□□□-□□□

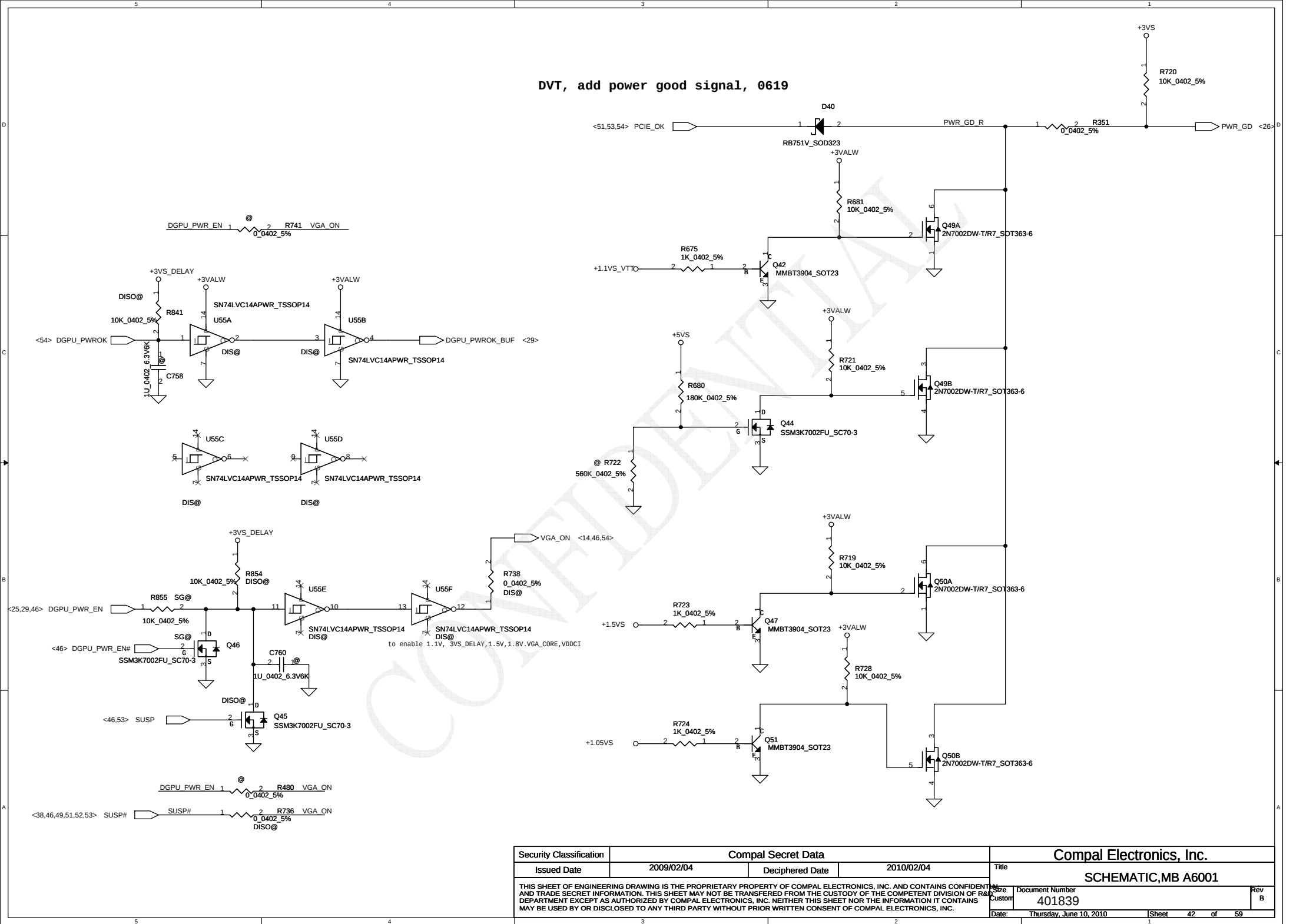
Assembly Material
Handling Code
Temperature Range
Package Code
Output Current/EN Function

Package Code
K : SOP-8 X : MSOP-8 B : SOT-23-5
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Output Current/EN Function
A : 2A/Active High B : 2A/Active Low
C : 1A/Active High D : 1A/Active Low
Assembly Material
G : Halogen and Lead Free Device

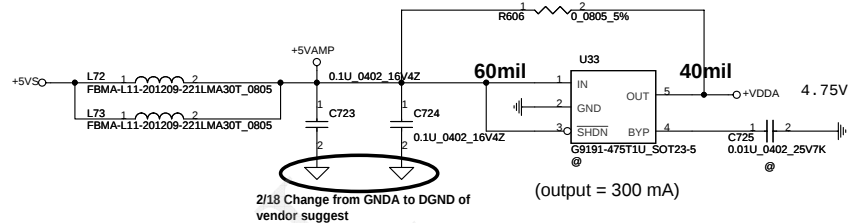
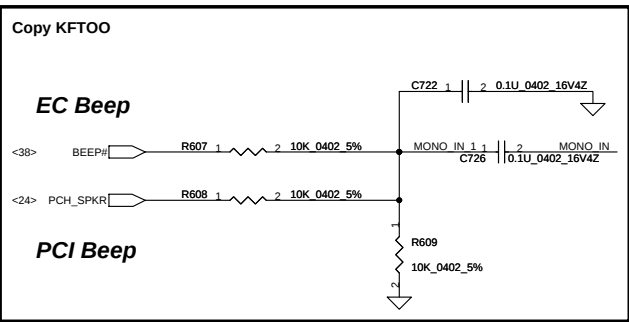


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				Date: Thursday, June 10, 2010
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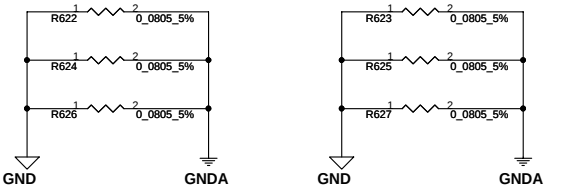
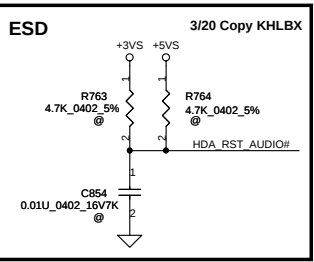
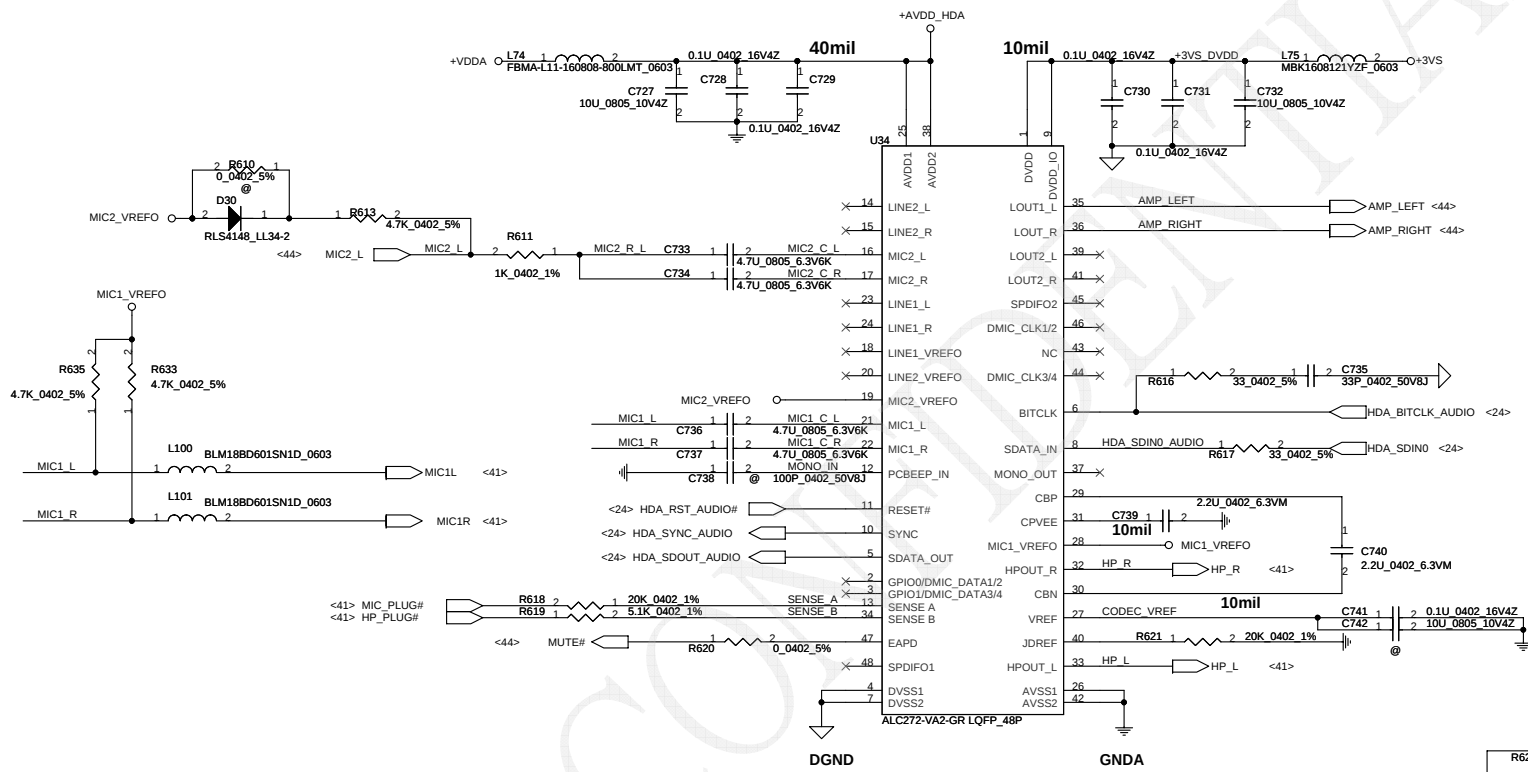
DVT, add power good signal, 0619



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HD Audio Codec

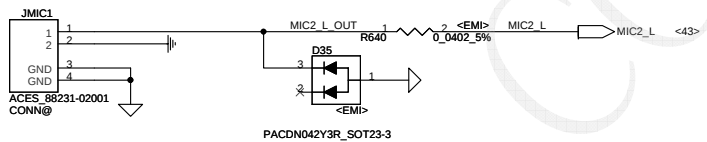
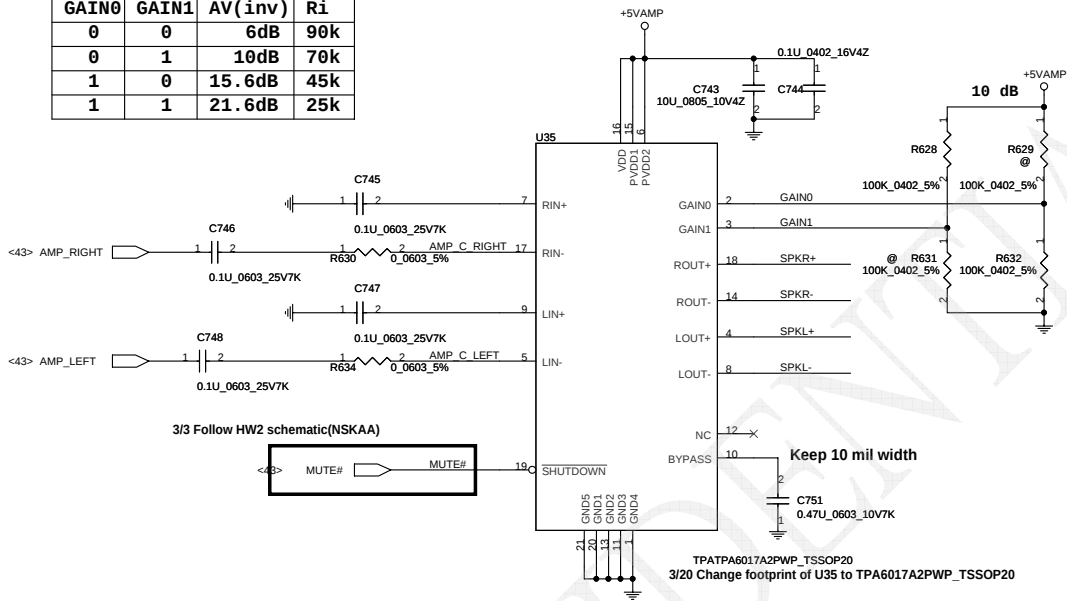


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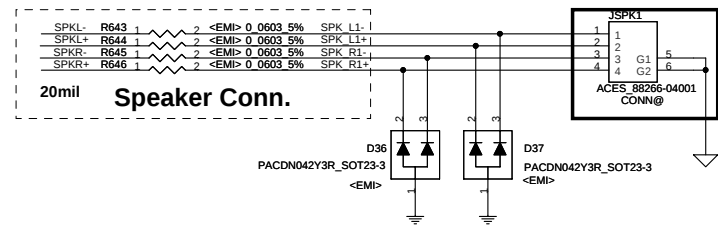
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GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



Int. Speaker Conn.

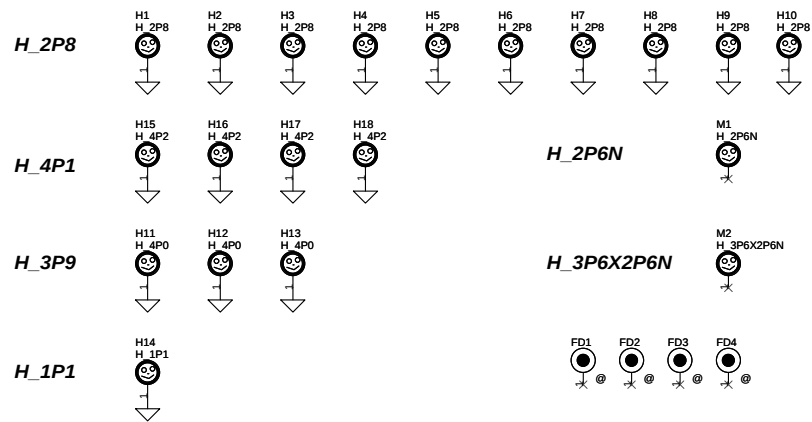


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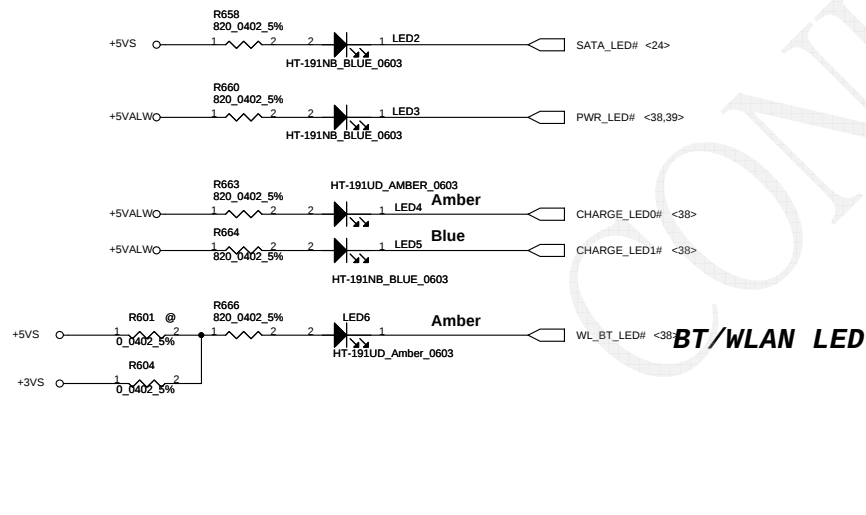
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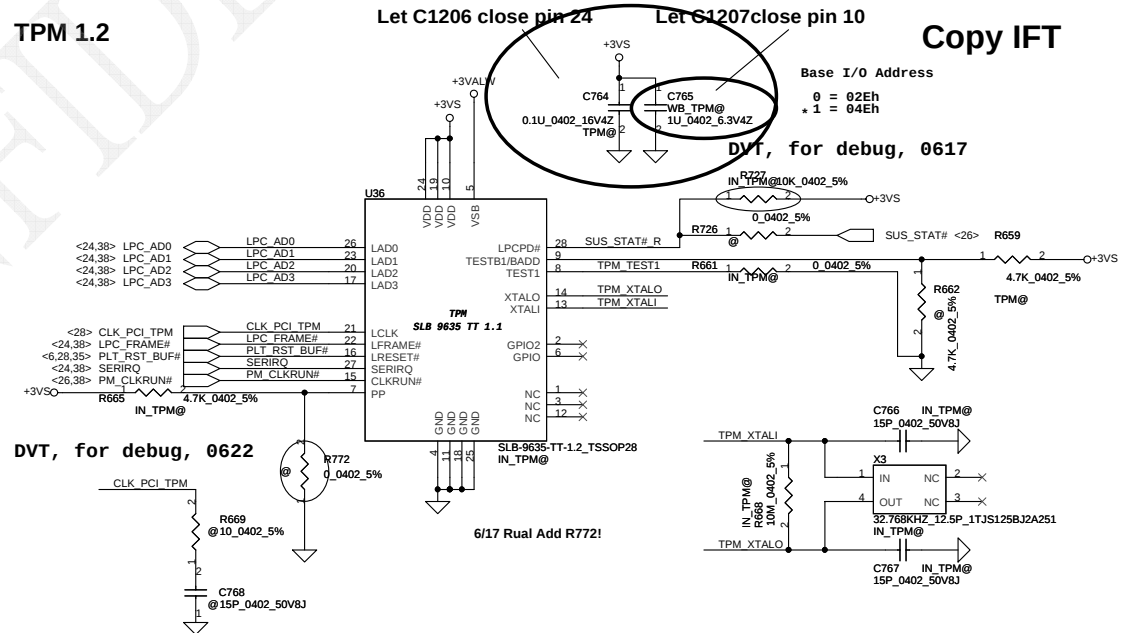


LED



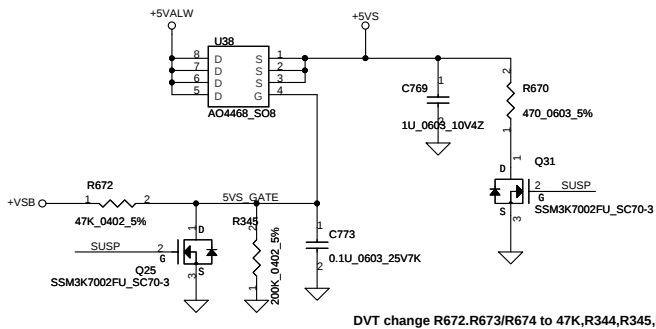
BT/WLAN LED

TPM 1.2



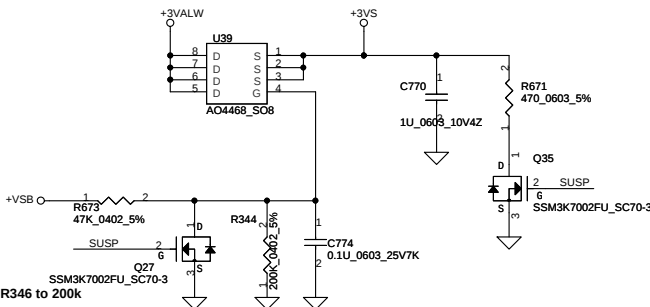
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+5VALW TO +5VS

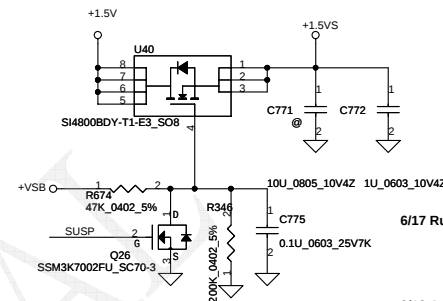


6/17 Rual Add R345!

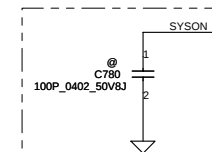
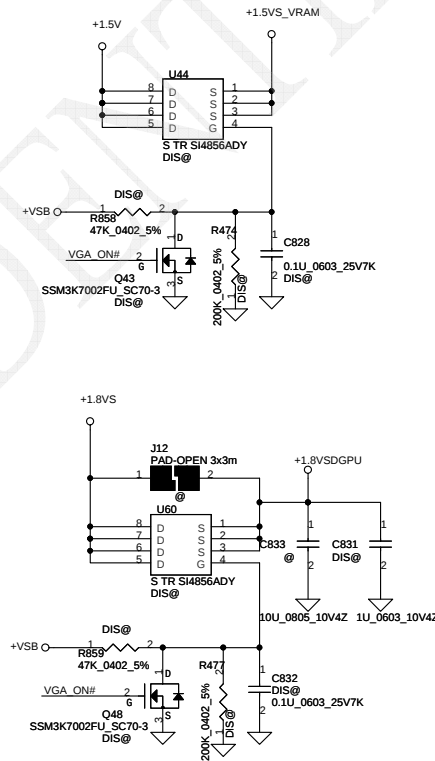
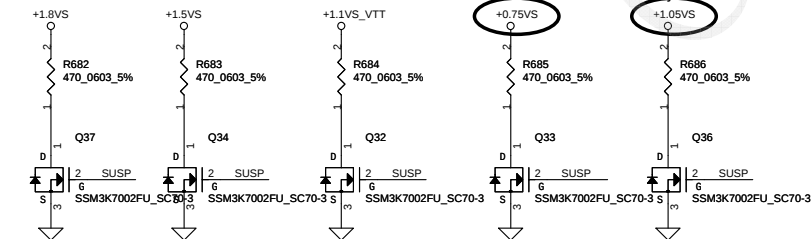
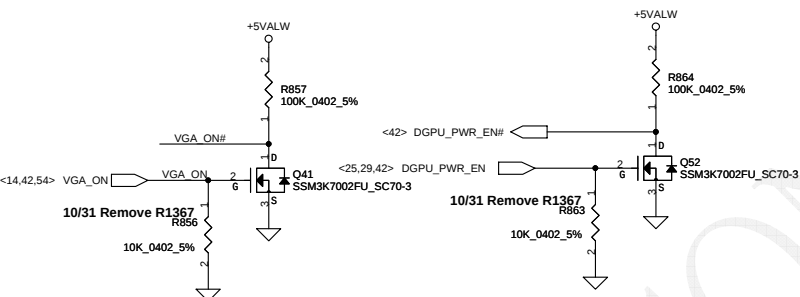
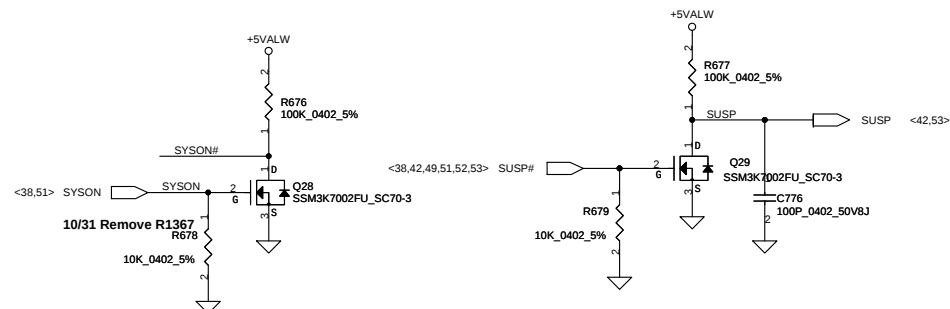
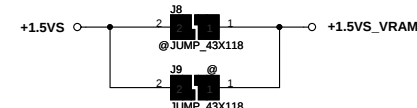
+3VALW TO +3VS



+1.5V TO +1.5VS

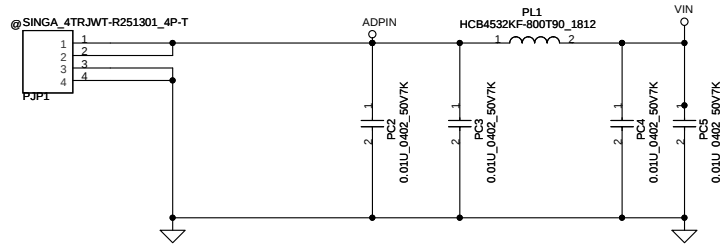


3/12 Add by Vivian



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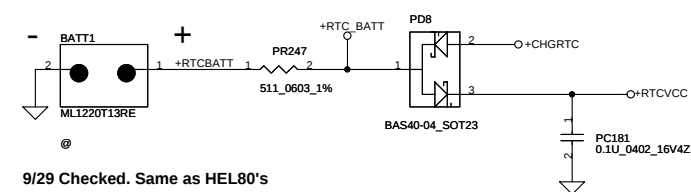
DC301008L00



RTC Battery

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

9/29 modified to follow ISKAA



9/29 Checked. Same as HEL80's

Reserve another location

BOM structure comment

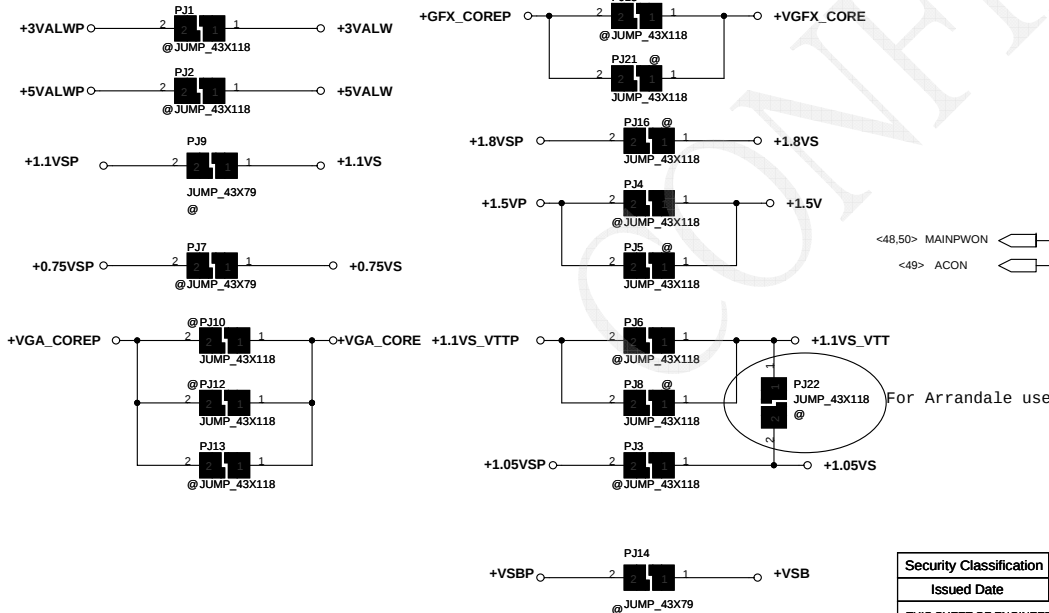
@ ==>unpop

UMA@==>UMA sku only

DIS@==>DIS sku only

06/24 Rual remove BATT2!

SP093MX0000

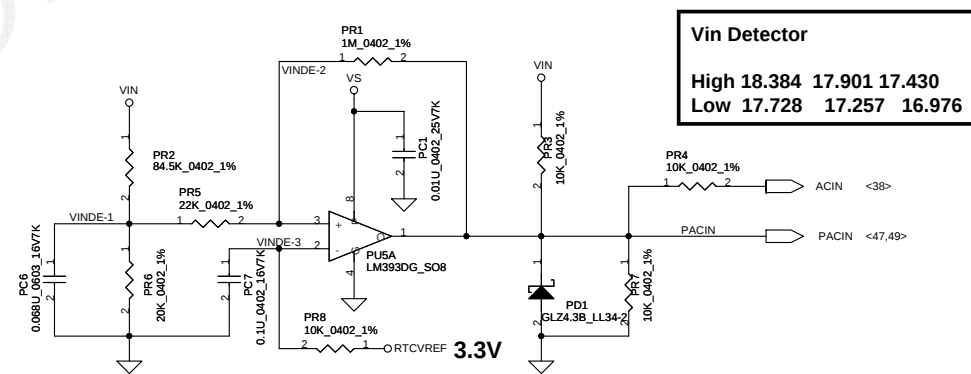
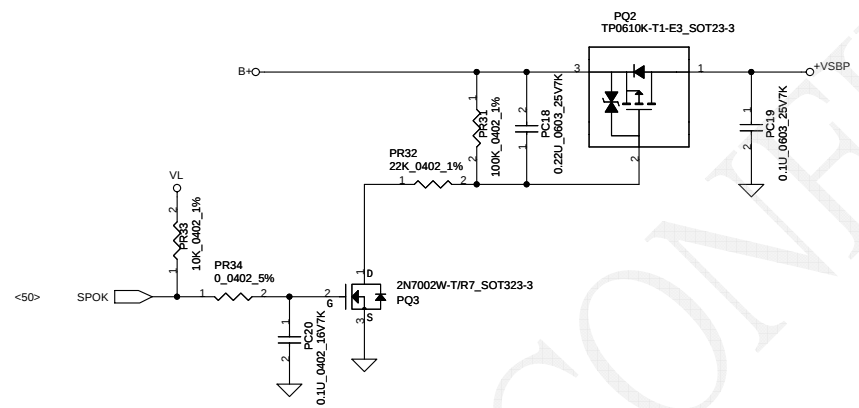
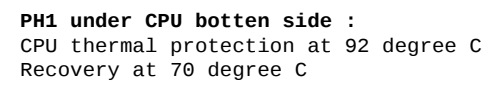


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<49> ACON

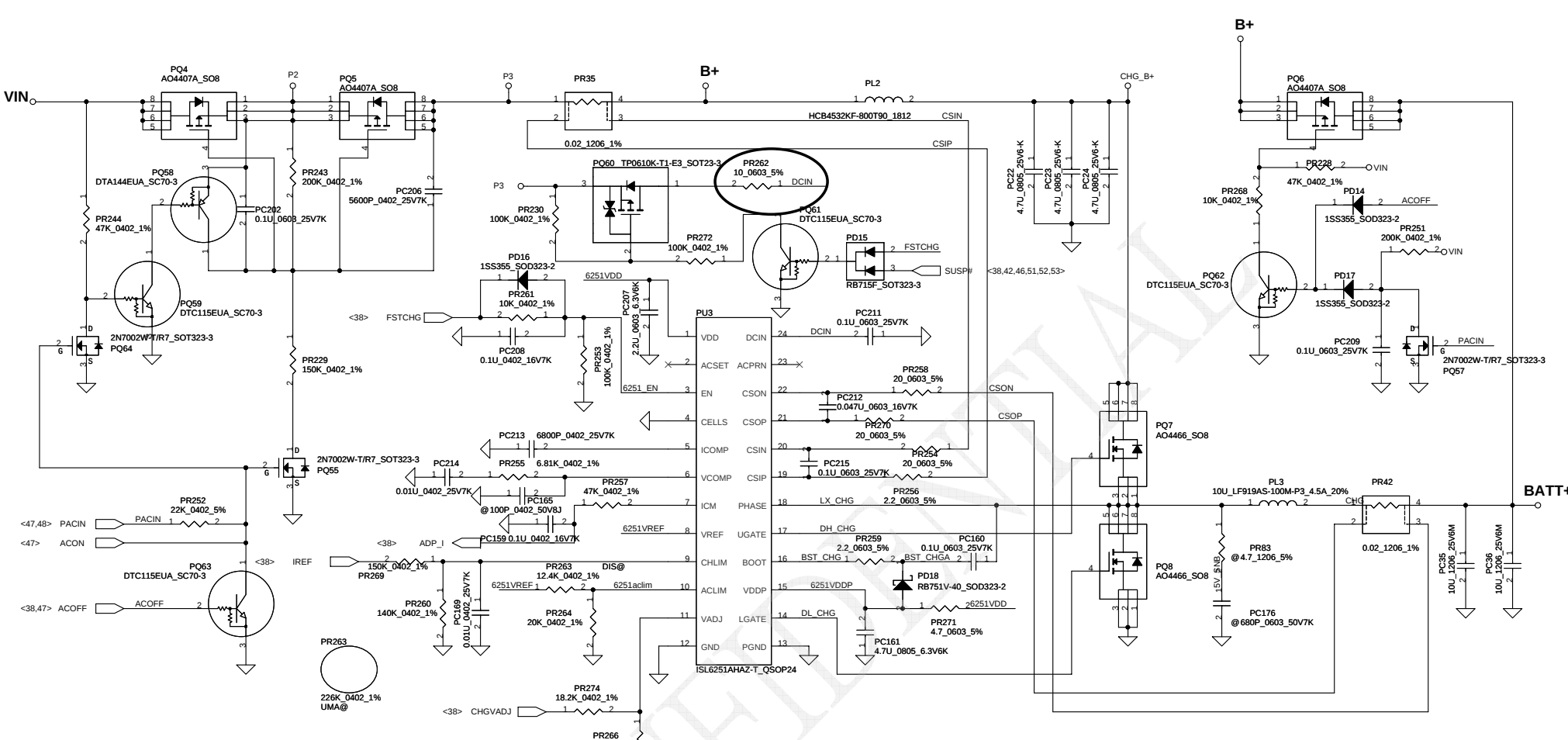
For Arrandale use

Precharge detector
15.97V/14.84V FOR
ADAPTOR

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"CHGVADJ" connect to EC DA pin

PR263
12.4K SD00000A380(DIS)
226K SD034226380(UMA)

Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.02A

CP mode
 $V_{ac11m} = 2.39 * (20K / (152K / (20K / (152K + 12.4K / 152K))) = 1.44966V$
 $I_{input} = (1 / 0.02) * ((0.05 * V_{ac1m}) / 2.39 + 0.05)$
where $V_{ac1m} = 1.44966V$, $I_{input} = 4.02A$

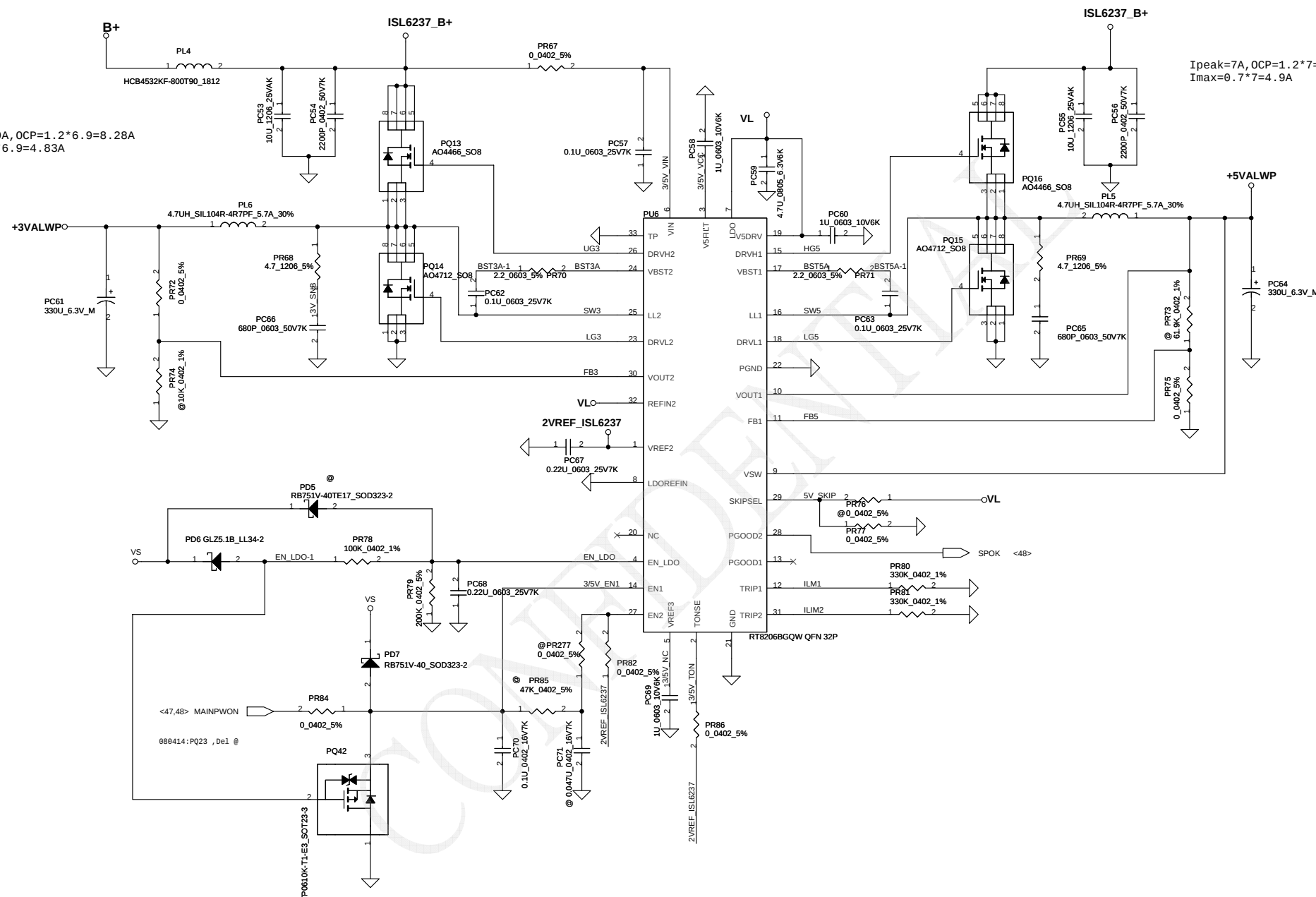
CC=0.5A~3.64A(0.7C)
IREF=2.42V (4.8AH)
2.62V (5.2AH)
IREF=0.4V~2.62V

CHGVADJ=	
Vcell	CHGVADJ
4V	0V
4.2V	1.854V
4.35V	3.12V

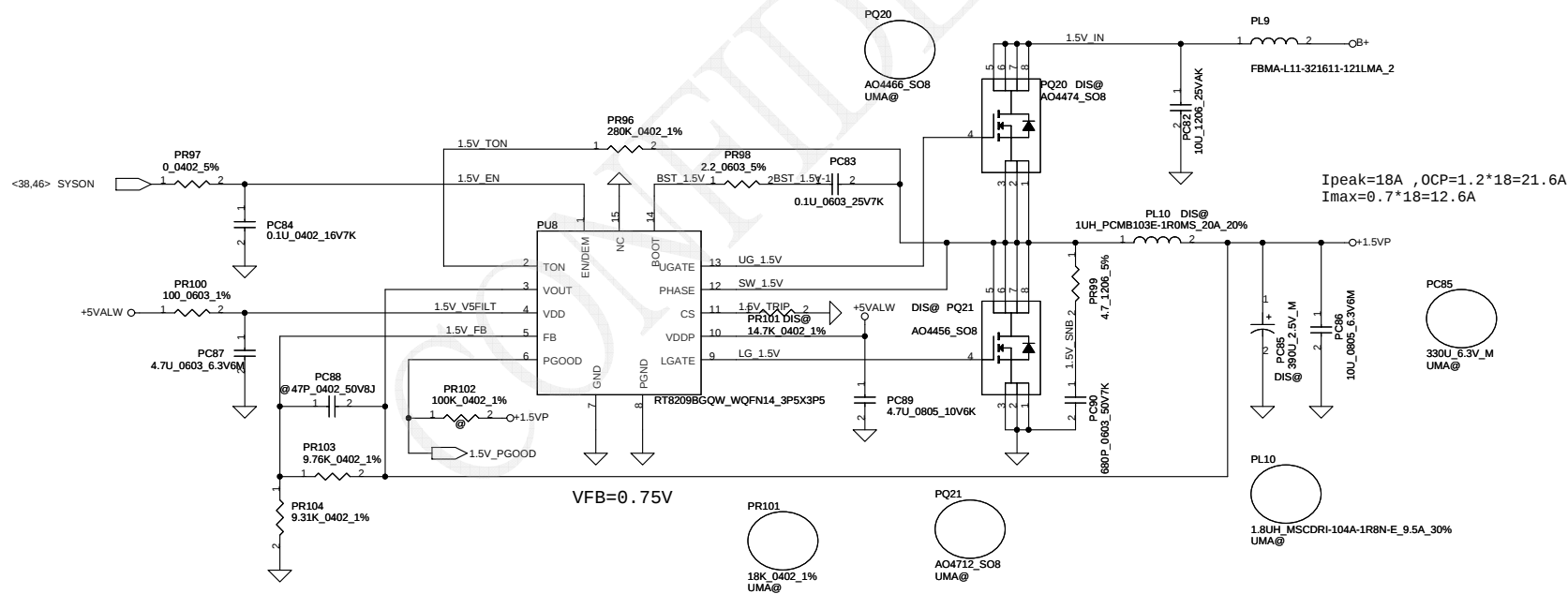
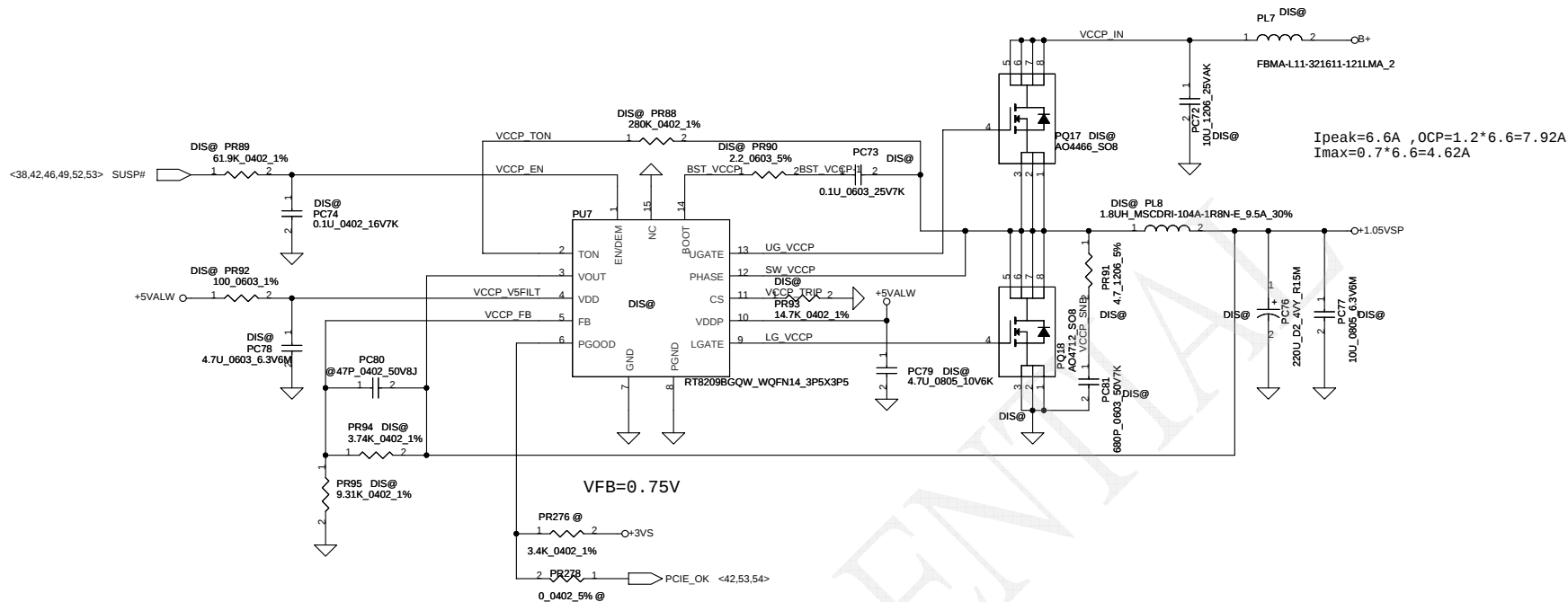
CELLS	VDD	GND	Float
CELL number	4	3	2

Ipeak=6.9A, OCP=1.2*6.9=8.28A
Imax=0.7*6.9=4.83A

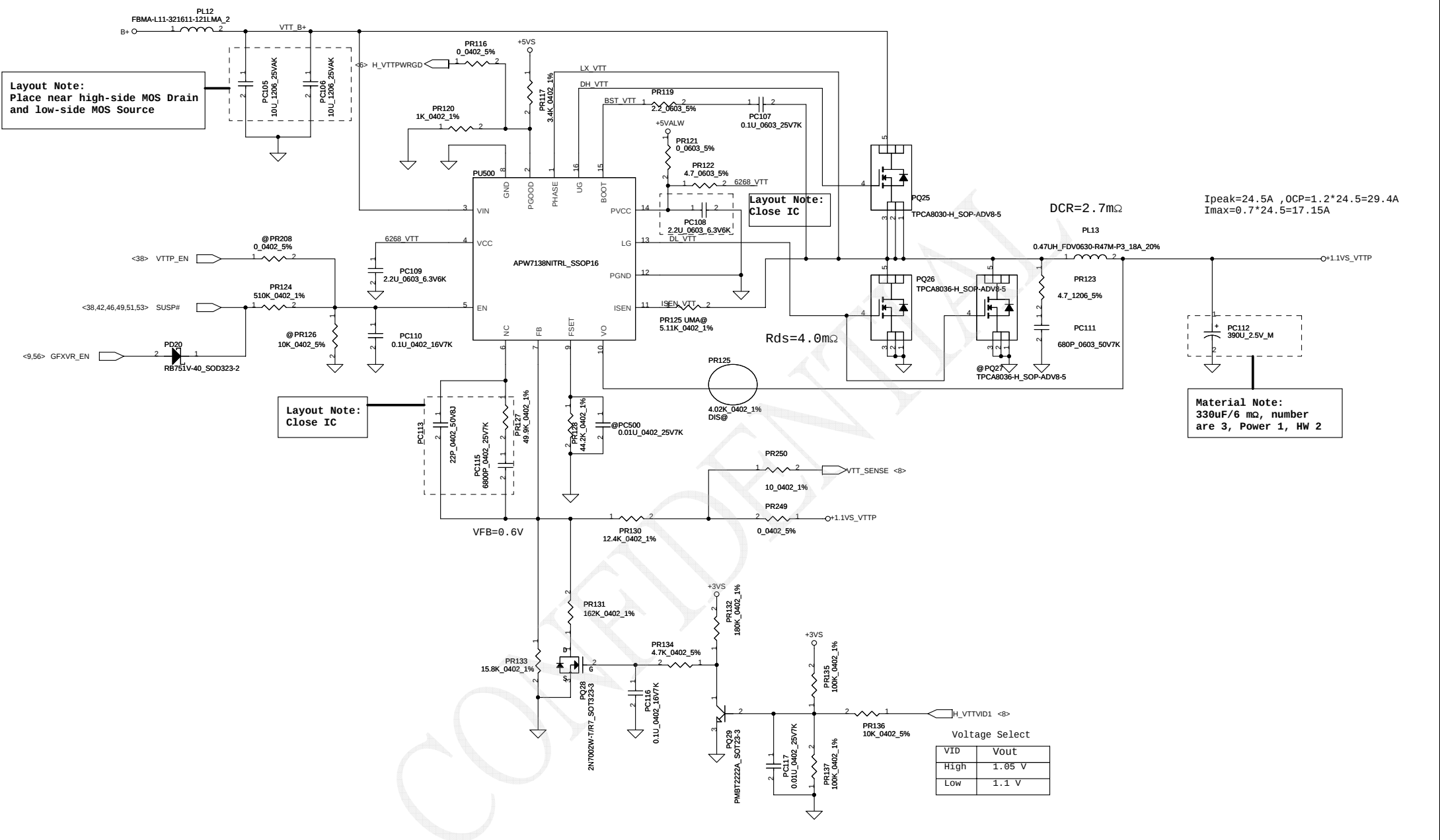
Ipeak=7A, OCP=1.2*7=8.4A
Imax=0.7*7=4.9A



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VID	Vout
High	1.05 V
Low	1.1 V

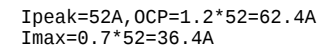
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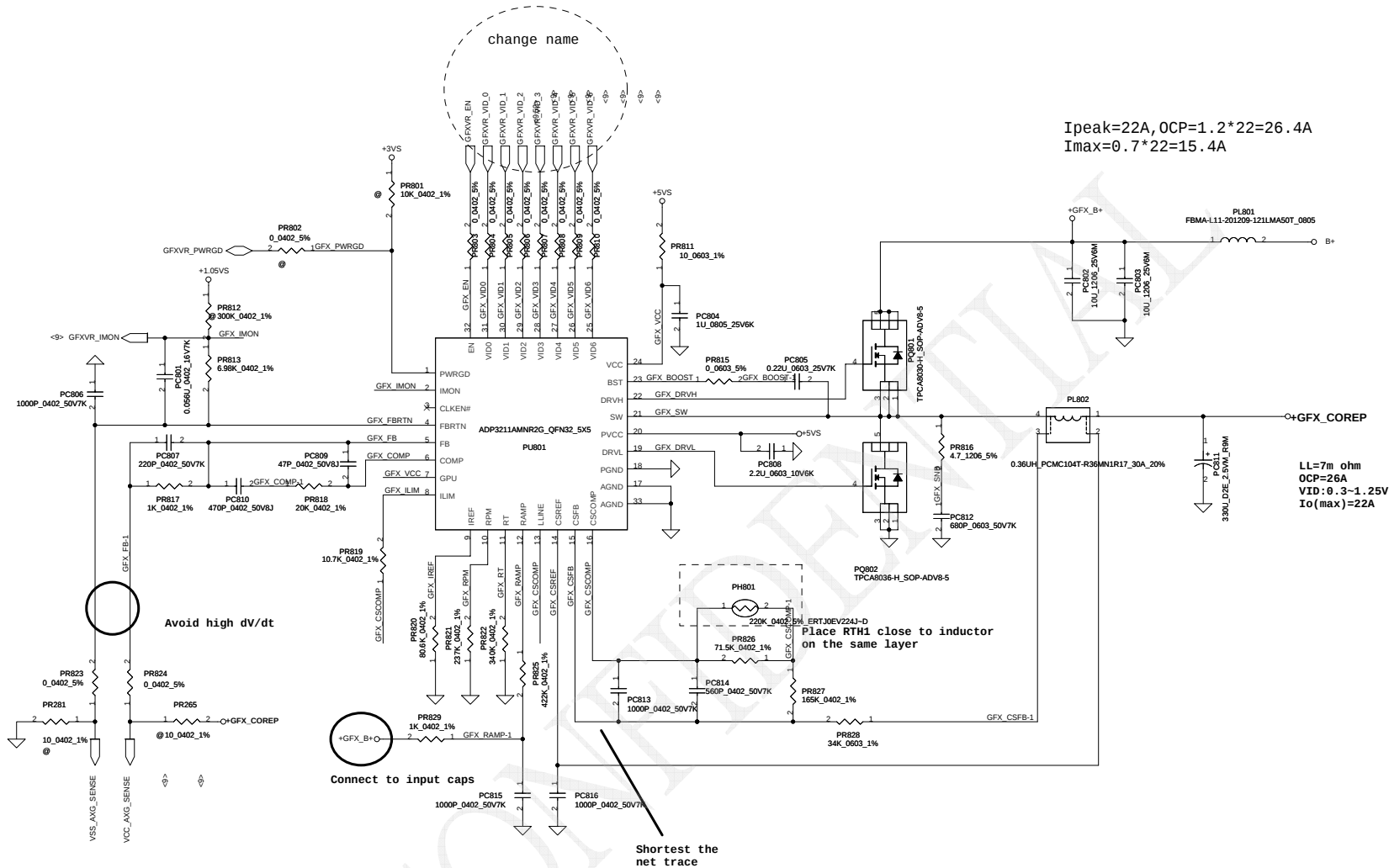
5	4	3	2	1
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1

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dy
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD





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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	can't use PWM to control brightness.	use PCH to control brightness in all SKU.	0.2	22	remove U47, R861,C825; U48; add R844, R827	01/30	DVT
2	Cost down	Cost down	0.2	23	Change Y6 from SJ100002600 to SJ114P3M730	01/30	DVT
3	Cost down	Cost down	0.2	20,21	change D7 and D15 to SCS00003H00	01/30	DVT
4	Cost down	Cost down	0.2	22	delete D18 , change R311 from 4.7K to 10K and pull down to GND.	01/30	DVT
5	Cost down	Cost down	0.2	22,40	change Q16&Q18 from SB923010020 to SB934130000 (A03413)	01/30	DVT
6	Cost down	Cost down	0.2		delete C433, C404;C852; C851;C401;C399; C364	01/30	DVT
7	Cost down	Cost down	0.2	9,30	Change R242;R501;R502;R504 from SD00000S000 to SD002000080 (0805 0ohm)		
8	Cost down	Cost down	0.2		delete C339;C336;C334		
9	Cost down	Cost down	0.2	38	delete crystal for EC		DVT
10	Cost down	Cost down	0.2	35	change YL1 from SJ100003300 to SJ125P0M200		DVT
11	Cost down	Cost down	0.2	35	change QL1 from SB000005X80 to SB934130000 (A03413)		DVT
12	Cost down	Cost down	0.2	41	change U30 from SA005280110 to SA000039E00		DVT
13	Cost down	Cost down	0.2	39,41	change D25&D28 from SC2N202U010 to SC600000B00		DVT
14	EMI Reserved.	EMI Reserved.	0.2	20	Add R865 and R866 on HDMI DDC signals for EMI		DVT
15	EMI&ESD Reserved.	EMI&ESD Reserved.	0.2	39	add D31, D32 and c838.		DVT
16		株y! n%?0 = ""	0.2	22		2/8	DVT
17		? ? n% ? h %-01/30					DVT
18		P? 統y! n%?0 =					
19		"" 0 !					
20							
21							
22							
23							

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1	ADD PQ64 in BOM	BOM STRUCTURE ERROR	0.1	51	Delete error bom structure	11/12	EVT
2	Battery OTP set	Battery OTP set	0.1	50	Change pr27 from 10k to 33.2k (sd034332280)	11/12	EVT
3	For material EOL issue	For material EOL issue	0.1	51	change pq4,pq5,pq6 from ao4407 to ao4407a (sb00000d100)	11/12	EVT
4	PH801 part number change	PH801 part number change	0.1	58	change ph801 from sl200000581 to sl200000500	11/18	EVT
5	output voltage unstable	output voltage unstable	0.1	55	change pc129,pc147 from 4.7u to 22u(se000000i10)	11/18	EVT
6	for material shortage issue	for material shortage issue	0.1	51	change pc22,pc23,pc24 from se142475k80 to se000006r80	11/19	EVT
7	For +3valw&5valw enable singal rising time delay	For +3valw&5valw enable singal rising time delay	0.1	52	change pr23 from 100k to 806k(sd014806380)	11/25	EVT
8	cost down	cost down	0.1	52	del pr830(sd034300080)	11/25	EVT
9	Not need	cost down	0.1	50	del pr22(sd034100180)	12/08	DVT
10	cost down	cost down	0.1	53	change pl11 from 2.2u to 1.8u(sh000008u80)	12/18	DVT
11	cost down	cost down	0.1	49	del pr225,pr226,pr265,pc175	12/24	DVT
12	cost down	cost down	0.1	56	change pq801 from si4686 to tpca8030 (sb00000h100)	12/26	DVT
13	cost down	cost down	0.1	49	change pr35 from 1206 size to 2512 size (sd000001f00)	12/26	DVT
14	pl3 temperature is too hot when charge	pl3 temperature is too hot when charge	0.1	49	change pl3 from sh00000e300 to sh162100m10	12/26	DVT
15	cost down	cost down	0.1	51	change pq20 from ao4474 to ao4466 (sb00000cg00) UMA	12/26	DVT
16	cost down	cost down	0.1	51	change pq21 from ao4456 to ao4712 (sb00000aj00)UMA	12/26	DVT
17	cost down	cost down	0.1	51	change pl10 from 1.0u to 1.8u (sh000008u80)UMA	12/26	DVT
18	cost down	cost down	0.1	51	change pc85 from 390u to 330u (sf000001g00)UMA	12/26	DVT
19	cost down	cost down	0.1	48, 49	change pq3 ,pq10,pq55,pq57,pq64 to sb000006800	01/21	DVT
20	for material shortage issue	for material shortage issue	0.1	56	change pq31 ,pq26,pq44,pq38,pq802 to sb00000hr00	01/21	DVT
21	for material shortage issue	for material shortage issue	0.1	47	change pd2 ,pd3,pd10 to sc100001y80	01/21	DVT
22	for material shortage issue	for material shortage issue	0.1	49	change pd7 ,pd18,pd20 to scs00000z00	01/21	DVT
23	for material shortage issue	for material shortage issue	0.1	48	change pd1 to sc400001200	01/21	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	for material shortage issue	for material shortage issue	0.1	50	change pd6 to sc400001300	01/21	DVT
2	for material shortage issue	for material shortage issue	0.1	49	change pd11,PD15 to scsh715f080	01/21	DVT
3	for material shortage issue	for material shortage issue	0.1	51	change pl17,pl19,pl15,pl802 to sh000005680	01/21	DVT
4	cost down	cost down	0.1	56	change pl16 to sm010020720	01/21	DVT
5	Change 1.1vsp power level from 1.0v to 1.1v	vga chip change from madison to M96	0.1	54	change pr160 from 1.07k to 1.47k(sd000009480)	1/29	DVT
6	ME interface	ME interface	0.1	49	change pr35 from 2512 size to 1206 size	1/29	DVT
7	OCP SETTING	OCP SETTING	0.1	52	change pr125 from 3.74k to 5.11k in UMA sku, change pr125 from 3.74k to 4.02k in DIS sku	2/2	DVT
8	OCP SETTING	OCP SETTING	0.1	51	change pr101 from 12.7k to 18k in UMA sku, change pr125 from 12.7k to 14.7k in DIS sku	2/2	DVT
9	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	0.1	55	change pq38,pq44from TPCA8036 to TPCA8028 in DIS sku	2/4	DVT
10	For madison voltage level change	For madison voltage level change	0.1	54	change pr151 from 10.2k to 9.53k(sd034953180)	2/5	DVT
11	For madison voltage level change	For madison voltage level change	0.1	54	change pr155 from 20.5k to 31.6k(sd034316280)	2/5	DVT
12	For madison voltage level change	For madison voltage level change	0.1	54	change pr149 from 38.3k to 68.1k(sd034681280)	2/5	DVT
13	For madison voltage level change	For madison voltage level change	0.1	54	change pr145 from 4.7k to 4.99k(sd034499180)	2/5	DVT
14	HW sequency request	HW sequency request	0.1	53	change pr199 from 200k to 150k for M96 VGA chip(sd034150380)	2/23	DVT
15	HW sequency request	HW sequency request	0.1	53	change pc177 from 0.22u to 0.1u for M96 VGA chip(se076104k80)	2/23	DVT
16	H_vttpwrgd glitch issue	H_vttpwrgd glitch issue	0.1	52	change PU500 pin14 pull high voltage from +5vs to +5valw	3/22	PVT
17	fix ki for all 030 project	fix ki for all 030 project	0.1	49	change pr269 from 80.6k to 150k(sd034150380) change pr260 from 100k to 140k(sd034140380)	3/29	PVT
18	fix kv for all 030 project	fix kv for all 030 project	0.1	49	change pr274 from 15.4k to 18.2k(sd034182280)	3/29	PVT
19	for IMON setting	for IMON setting	0.1	55	change pr55 from 4.53k to 5.36k, pc174 from 0.1u to 0.068u in UMA SKU	04/1	PVT
20	for RPM frequency setting	for RPM frequency setting	0.1	55	change pr174 from 47.5k to 69.8k,	04/1	PVT
21			0.1	47		01/21	DVT
22			0.1			01/21	DVT
23			0.1			01/21	DVT

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