Compal Confidential

NAYF0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-08-27

REV:0.1

PCB

ZZZ

DAZ@
DA80000GT00

NAYF0 LA-5881P REV0 M/B

LA-5881P MB Rev0: DA80000GT00

VRAM PARK

ZZZ

VRAM PARK@
X76193BOL01

512M HIX

VRAM MAD

ZZZ

VRAM MAD@
X76193BOL03

1G HIX

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Model Name : NAYF0
File Name : LA5881

Fan Control page 38

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader
page 12

MXM III Conn. page 13

PEG(DIS) 100MHz PCI-E 2.0x16 5GT/s PER LANE
eDP(DIS NV)
eDP Conn. page 23
133MHz eDP(UMA)

Intel
Auburndale / Clarksfield
(UMA/DIS) (DIS)
Processor
rPGA988A
page 4,5,6,7,8,9

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066/1333
6.4G/8.5G/10.6G
100M/133M/166M(CFD)
204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3 page 10,11

LVDS(DIS)
HDMI(DIS)
CRT(DIS)
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CRT SW. page 25
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LVDS SW page 24
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FDI x8 (UMA)
100MHz 2.7GT/s
DMI x4
100MHz 1GB/s x4

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USB port 7
USB port 8 HS USB
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Bluetooth Conn
USB port 10
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USB port 3
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Card Reader
RTS5159-GR
USB port 6
page 30

USBx14
3.3V 48MHz

HDMI(UMA)
HDMI Level Shift page 26
LVDS(UMA)
CRT(UMA)
TMDS(UMA)

Intel
Ibex Peak-M
PCH
page 14,15,16,17
18,19,20,21,22

HD Audio 3.3V 24MHz
Dual CH NAND Interface
SPI

PCI-Express x 8 (ABD PCIE1 2.5GT/S CKD PCIE1/2 2.5/5GT/S) 100MHz
SATA x 6 (GEN1 1.5GT/S ,GEN2 3GT/S) 100MHz

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MINI Card x2
WLAN, TV
USB port 4,5
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MDC 1.5 Conn page 35
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TI TPS6017
page 37
Int. Speaker page 37
Phone Jack x 3
+SubWoofer
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33MHz
ENE KB926 page 33

Touch Pad page 34
Int.KBD page 34
EC I/O Buffer page 34
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SJV70
Function/B
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LS-5026P
SJV70
LED/B
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LS-5027P PWR/B
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RTC CKT. page 35
Power On/Off CKT. page 35
DC/DC Interface CKT. page 39
Power Circuit DC/DC page 40~48

PCH XDP page 22
CPU XDP
133MHz
page 5

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
ALC 271	271@
ALC 272	272@
ASM1442	ASM@
CH7318	CH@
S3	S3@
NONS3	NONS3@
XDP	XDP@
Switchable	SG@
VGA	VGA@
UMA	UMA@
UMAO	UMAO@
DISO	DISO@
MADISON	MAD@
PARK	PARK@
VRAM MADISON	VRAM MAD@
VRAM PARK	VRAM PARK@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHCI1	UHCI0	0	Ext1 USB	Ext1 USB
		1	Ext2 USB	Ext2 USB
	UHCI1	2	Ext3 USB (JV only)	
		3	Camera	Camera
	UHCI2	4	1st Min-Card	1st Min-Card
		5	2st Min-Card	2st Min-Card
	UHCI3	6	Card Reader	Card Reader
		7	Ext3 USB (JM only)	
EHCI2	UHCI4	8	Ext4 HS USB	Ext3 HS USB
		9		
	UHCI5	10	Blue Tooth	Blue Tooth
		11		
	UHCI6	12		
		13		

BOM Config

UMA only SKU:UMAO@/UMA@

Switchable PARK SKU: SG@/VGA@/PARK@/VRAM PARK@

Switchable MADISON SKU: SG@/VGA@/MAD@/VRAM MAD@

The same: 272@/ASM@/NONS3@/DAZ@

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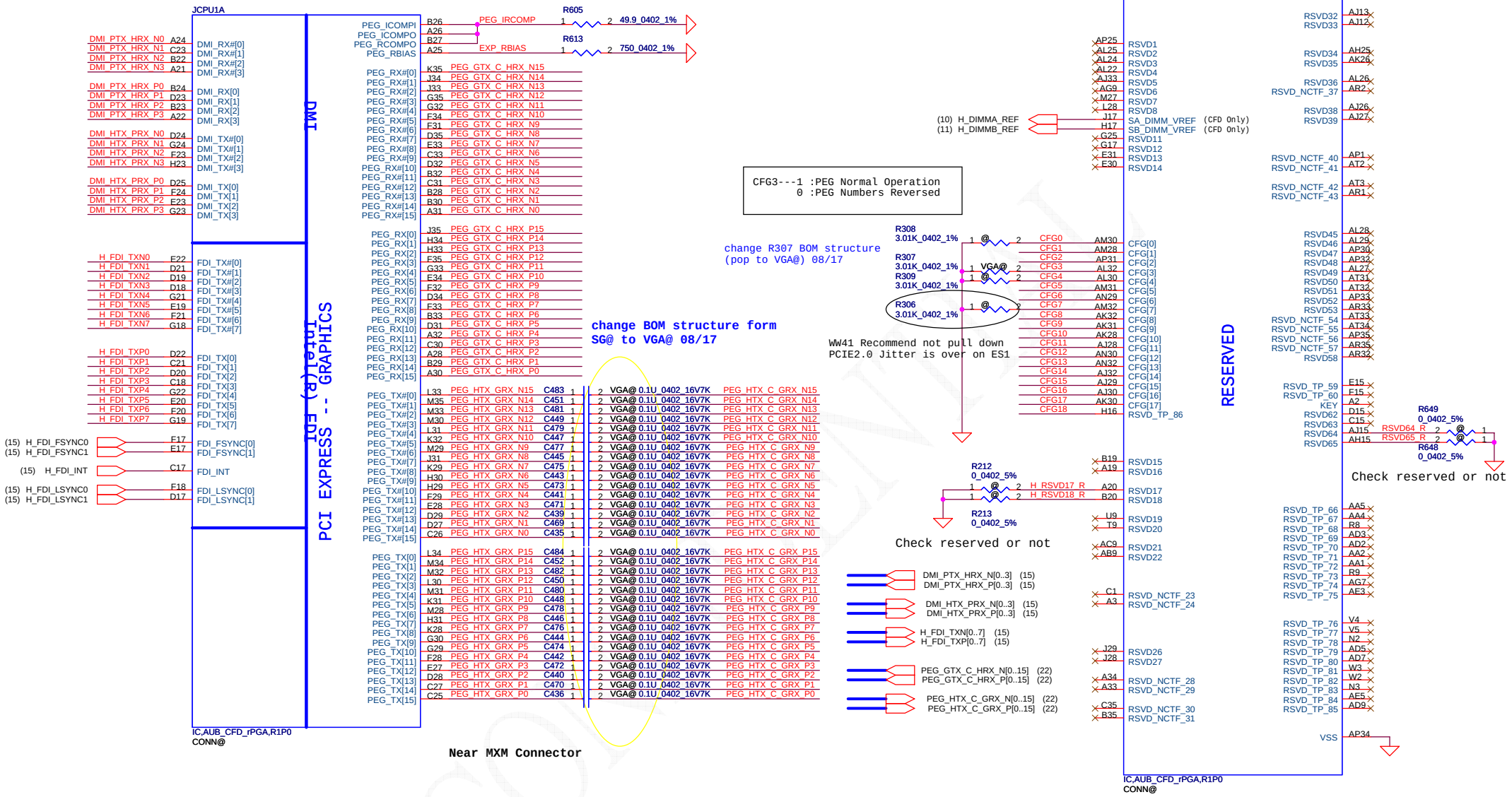

eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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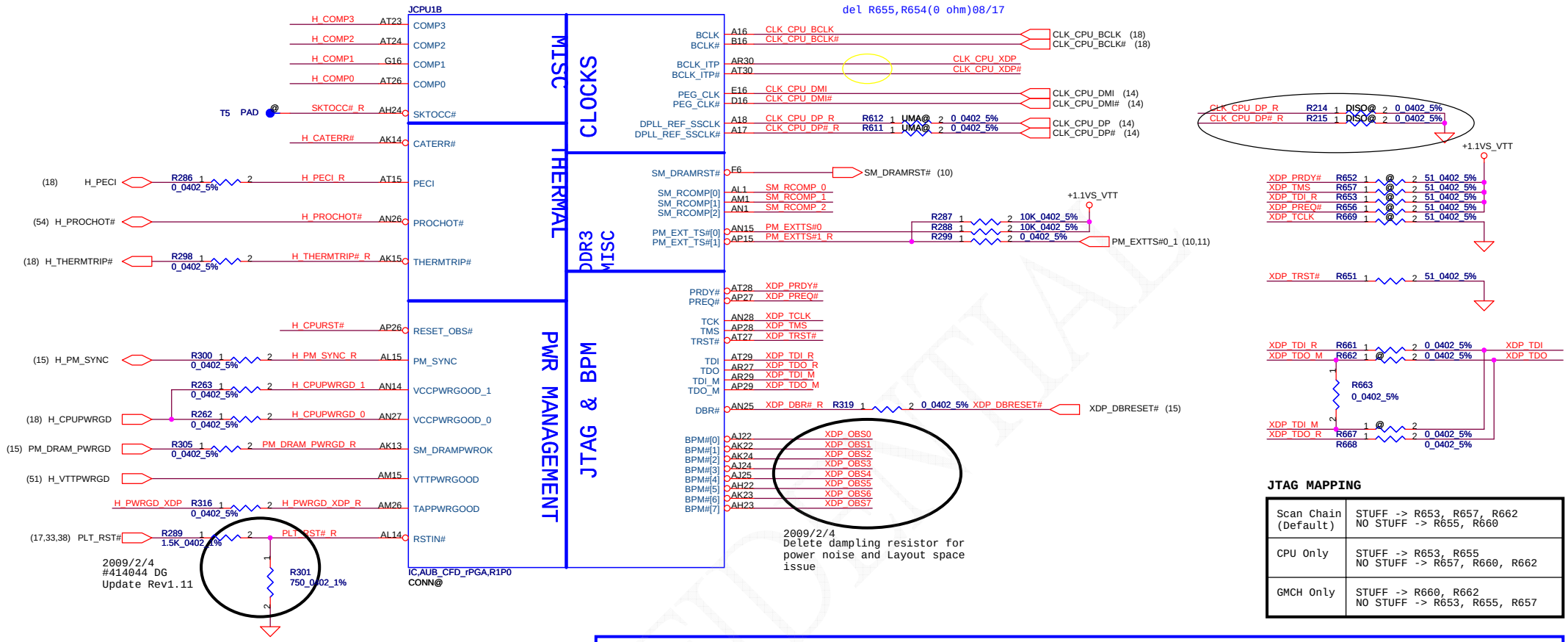

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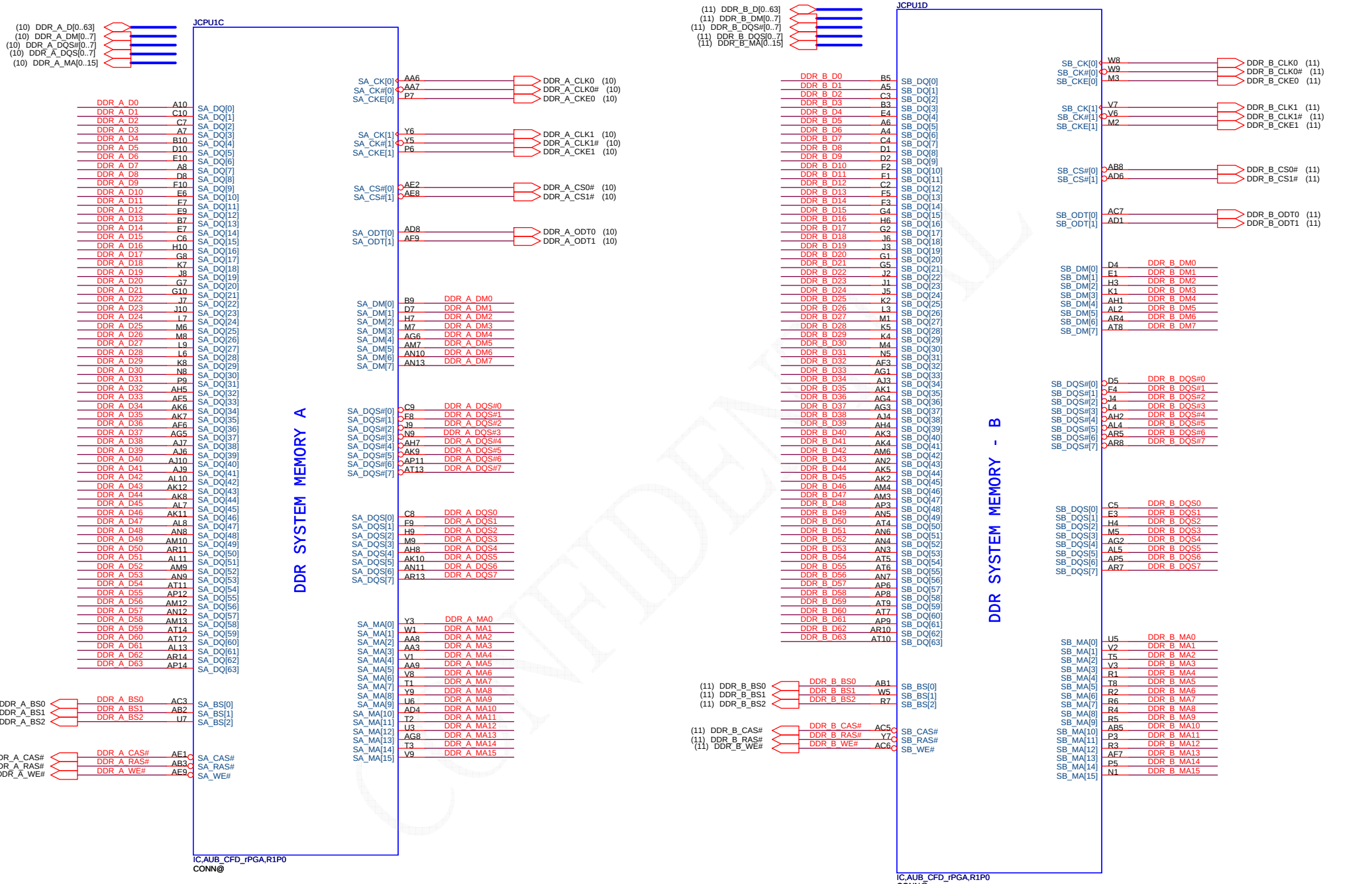

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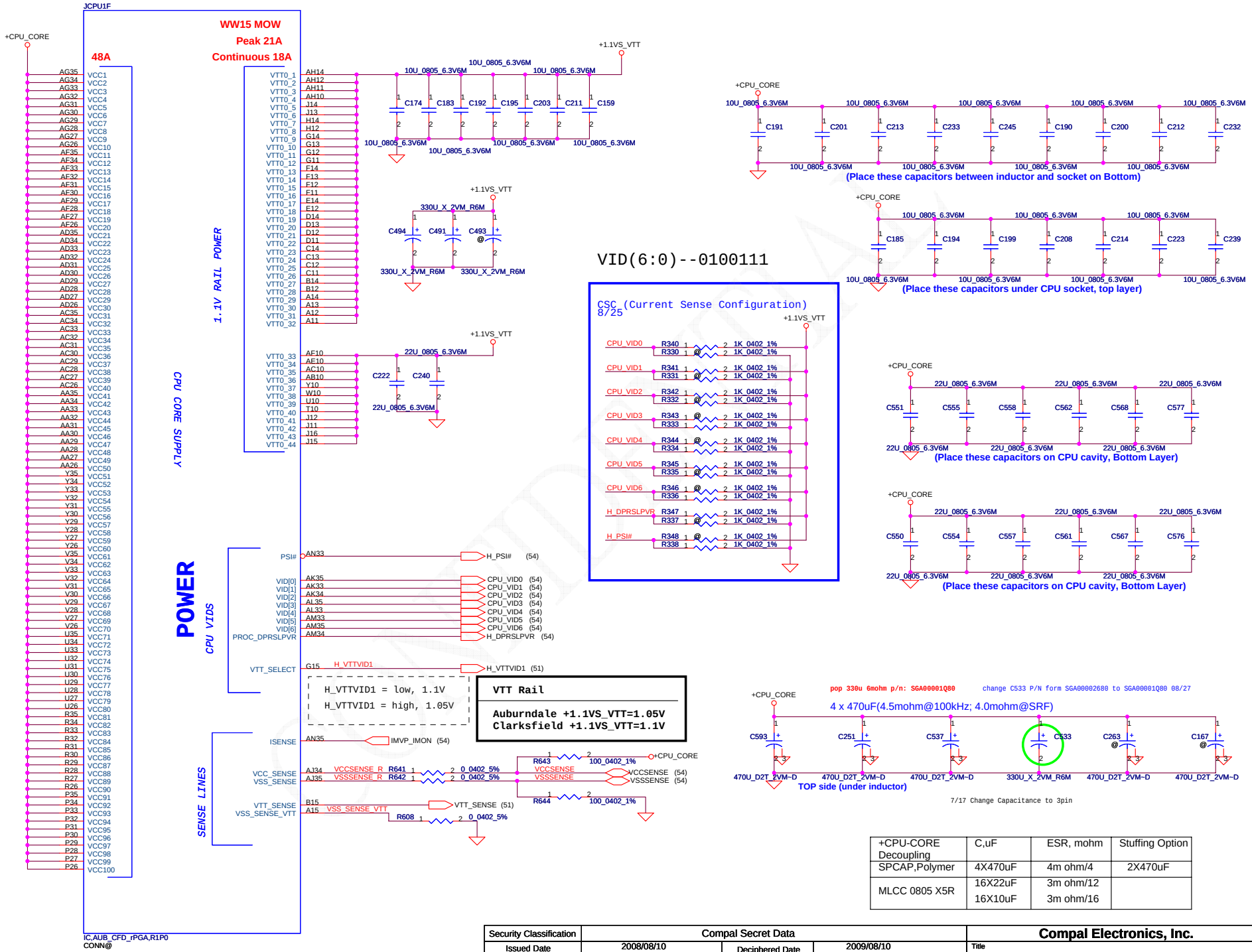

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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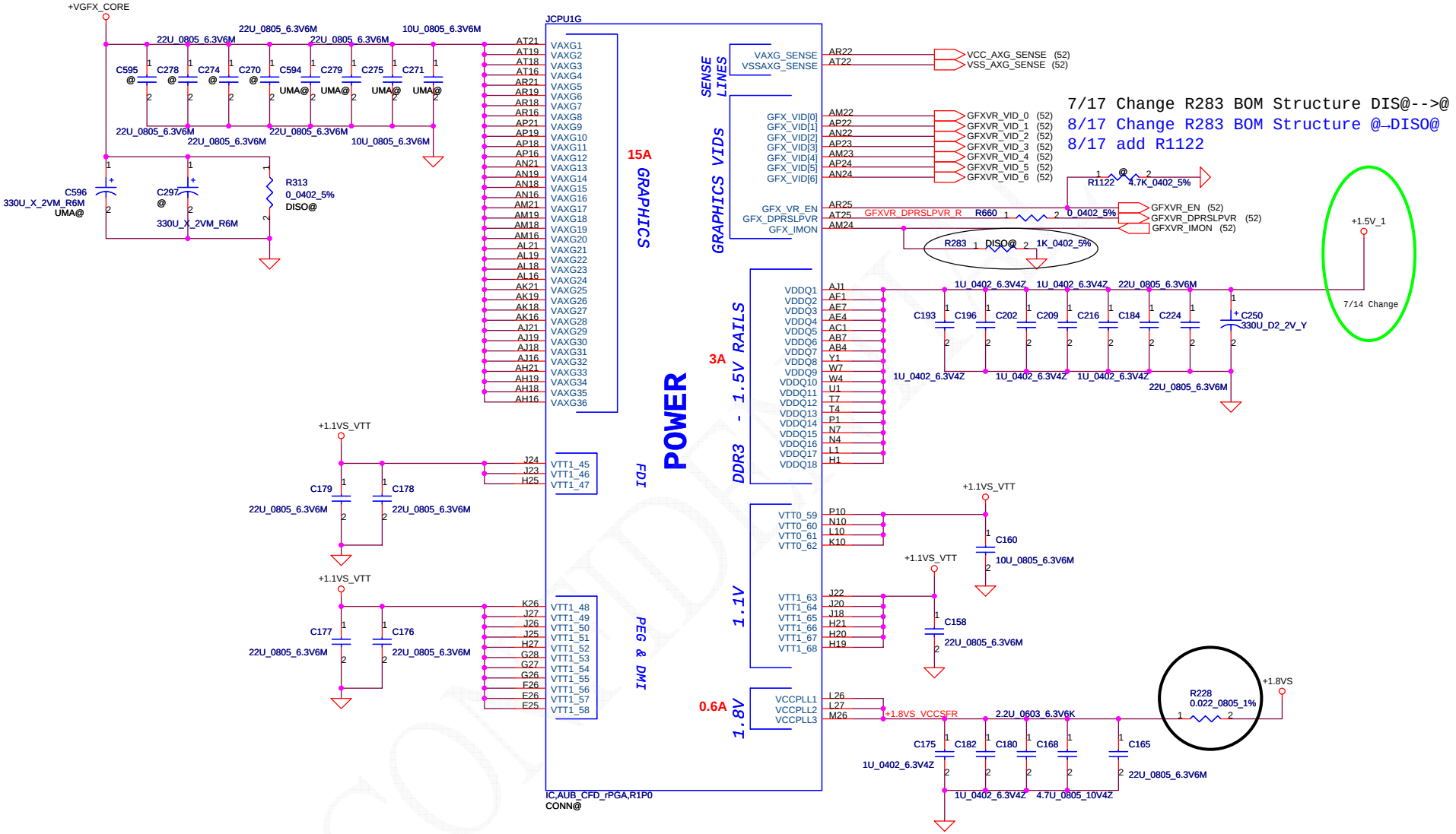

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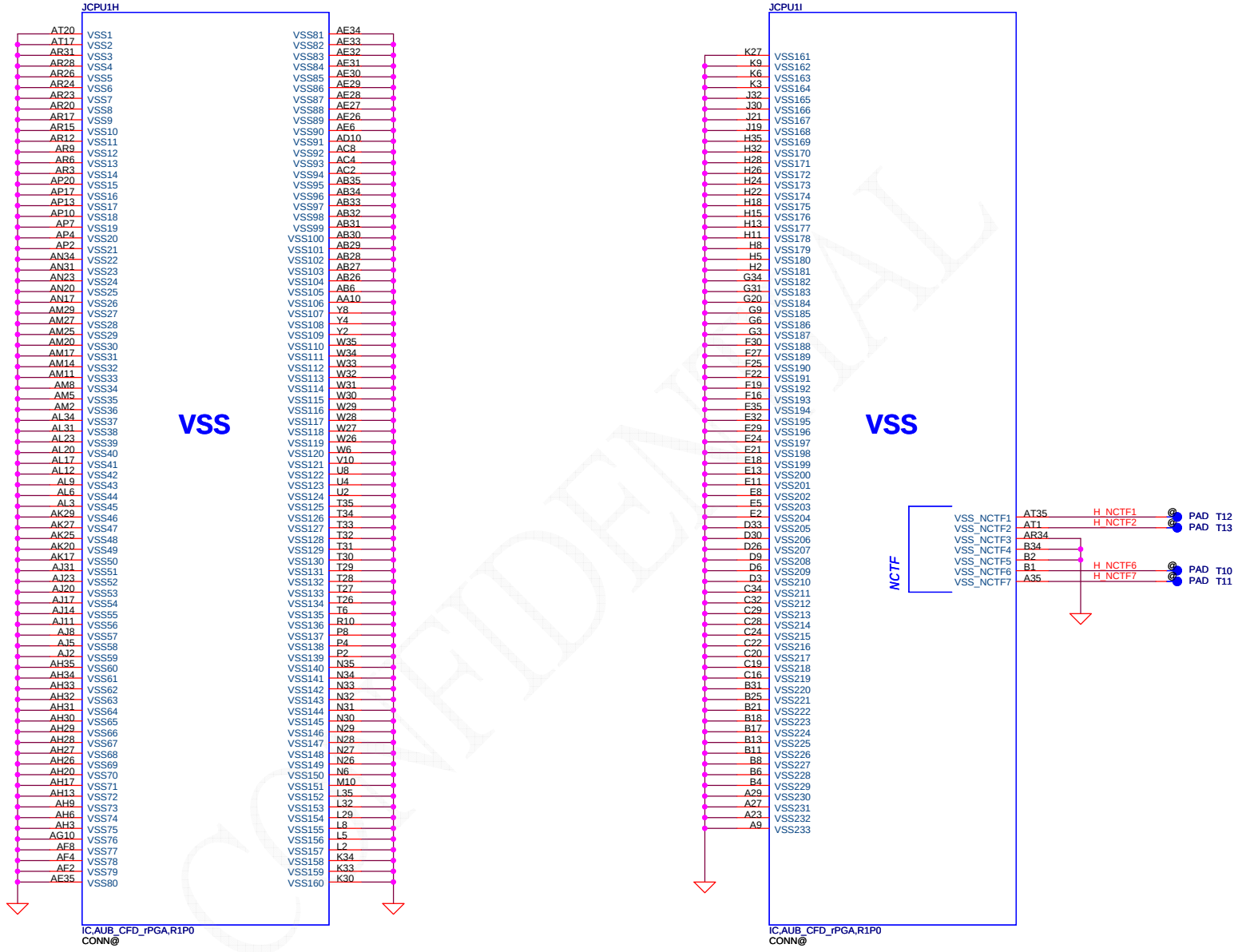

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M1 Circuit

+1.5V

R170 1K_0402_1%

+V_DDR3_DIMM_REF

+V_DDR3_DIMM_REF

R169 1K_0402_1%

(6) DDR_A_DQS#[0..7]
(6) DDR_A_D[0..63]
(6) DDR_A_DM[0..7]
(6) DDR_A_DQS[0..7]
(6) DDR_A_MA[0..15]

(4) H_DIMMA_REF

7/14 Change

M3 Circuit

R178 @ 0_0402_5%

R154 100K_0402_5% @

Q79 2N7002_SOT23 @

RST_GATE

M1 Circuit

+V_DDR3_DIMM_REF

R179 0_0402_5%

2009/05/19
M2 Circuit unpop
Pop M3 Circuit

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

090615 add DDR_VREF_CA_DIMM

+1.5V

R210 1K_0402_1%

+DDR_VREF_CA_DIMM

+DDR_VREF_CA_DIMM

R224 1K_0402_1%

7/14 Change

(5) SM_DRAMRST#

R155 100K_0402_5% S3@

R942 NONS3@ 0_0402_5%

Q80 2N7002_SOT23 S3@

DIMM_DRAMRST#

R941 S3@1K_0402_1%

Change to BSH111

(11,18) RST_GATE

RST_GATE

BOM structure change 08/17
R942 POP→NONS3@
R155,R941,Q80 @→S3@

C124 0.1U_0402_16V4Z

C112 2.2U_0805_16V4Z

JDIMM1

	VREF_DQA	1	2	VSS	
DDR_A_D4	VSS	3	4	DQ4	DDR_A_D5
DDR_A_D0	DQ0	5	6	DQ5	DDR_A_D1
	VSS	7	8	DQ1	
DDR_A_DQS#0	DQS0#	9	10	VSS	DDR_A_DQS0
DDR_A_DM0	DM0	11	12	DQS0	
	VSS	13	14	VSS	
DDR_A_D6	DQ2	15	16	DQ6	DDR_A_D2
DDR_A_D3	DQ3	17	18	DQ7	DDR_A_D7
	VSS	19	20	VSS	
DDR_A_D12	DQ8	21	22	DQ12	DDR_A_D8
DDR_A_D9	DQ9	23	24	DQ13	DDR_A_D13
	VSS	25	26	VSS	
DDR_A_DM1	DQS1#	27	28	DM1	DDR_A_DQS#1
DDR_A_DQS1	DQS1	29	30	RESET#	DIMM_DRAMRST#
	VSS	31	32	VSS	
DDR_A_D14	DQ10	33	34	DQ14	DDR_A_D10
DDR_A_D11	DQ11	35	36	DQ15	DDR_A_D15
	VSS	37	38	VSS	
DDR_A_D20	DQ16	39	40	DQ20	DDR_A_D16
DDR_A_D17	DQ17	41	42	DQ21	DDR_A_D21
	VSS	43	44	VSS	
DDR_A_DM2	DQS2#	45	46	DM2	DDR_A_DQS#2
DDR_A_DQS2	DQS2	47	48	VSS	
DDR_A_D22	VSS	49	50	DQ22	DDR_A_D18
DDR_A_D19	DQ18	51	52	DQ23	DDR_A_D23
	DQ19	53	54	VSS	
DDR_A_D28	VSS	55	56	DQ28	DDR_A_D24
DDR_A_D25	DQ24	57	58	DQ29	DDR_A_D29
	DQ25	59	60	VSS	
DDR_A_DQS#3	VSS	61	62	DQS3#	DDR_A_DM3
DDR_A_DQS3	DM3	63	64	DQS3	
	VSS	65	66	VSS	
DDR_A_D30	DQ26	67	68	DQ30	DDR_A_D26
DDR_A_D31	DQ27	69	70	DQ31	DDR_A_D27
	VSS	71	72	VSS	
DDR_A_CKE1	CKE0	73	74	CKE1	
	VDD	75	76	VDD	
DDR_A_MA15	NC	77	78	A15	
DDR_A_MA14	BA2	79	80	A14	
	VDD	81	82	VDD	
DDR_A_MA11	A12/BC#	83	84	A11	
DDR_A_MA7	A9	85	86	A7	
	VDD	87	88	VDD	
DDR_A_MA6	A8	89	90	A6	
DDR_A_MA4	A5	91	92	A4	
	VDD	93	94	VDD	
DDR_A_MA2	A3	95	96	A2	
DDR_A_MA0	A1	97	98	A0	
	VDD	99	100	VDD	
DDR_A_CLK1	CK0	101	102	CK1	
DDR_A_CLK1#	CK0#	103	104	CK1#	
	VDD	105	106	VDD	
DDR_A_BS1	A10/AP	107	108	BA1	
DDR_A_RAS#	BA0	109	110	RAS#	
	VDD	111	112	VDD	
DDR_A_CS0#	WE#	113	114	S0#	
DDR_A_ODT0	CAS#	115	116	ODT0	
	VDD	117	118	VDD	
DDR_A_ODT1	A13	119	120	ODT1	
	S1#	121	122	NC	
	VDD	123	124	VDD	
DDR_VREF_CA_DIMMA	TEST	125	126	VREF_CA	
	VSS	127	128	VSS	
DDR_A_D36	DQ32	129	130	DQ36	
DDR_A_D37	DQ33	131	132	DQ37	
	VSS	133	134	VSS	
DDR_A_DM4	DQS4#	135	136	DM4	
DDR_A_DQS4	DQS4	137	138	VSS	
DDR_A_D38	VSS	139	140	DQ38	
DDR_A_D39	DQ34	141	142	DQ39	
	DQ35	143	144	VSS	
DDR_A_D44	VSS	145	146	DQ44	
DDR_A_D45	DQ40	147	148	DQ45	
	DQ41	149	150	VSS	
DDR_A_DQS#5	VSS	151	152	DQS5#	
DDR_A_DQS5	DM5	153	154	DQS5	
	VSS	155	156	VSS	
DDR_A_D46	DQ42	157	158	DQ46	
DDR_A_D47	DQ43	159	160	DQ47	
	VSS	161	162	VSS	
DDR_A_D52	DQ48	163	164	DQ52	
DDR_A_D53	DQ49	165	166	DQ53	
	VSS	167	168	VSS	
DDR_A_DM6	DQS6#	169	170	DM6	
DDR_A_DQS6	DQS6	171	172	VSS	
DDR_A_D54	VSS	173	174	DQ54	
DDR_A_D55	DQ50	175	176	DQ55	
	DQ51	177	178	VSS	
DDR_A_D60	VSS	179	180	DQ60	
DDR_A_D61	DQ56	181	182	DQ61	
	DQ57	183	184	VSS	
DDR_A_DQS#7	VSS	185	186	DQS7#	
DDR_A_DQS7	DM7	187	188	DQS7	
	VSS	189	190	VSS	
DDR_A_D62	DQ58	191	192	DQ62	
DDR_A_D63	DQ59	193	194	DQ63	
	VSS	195	196	VSS	
PM_EXTTS#0_1	SA0	197	198	EVENT#	
D_CK_SDATA	VDDSPD	199	200	SDA	
D_CK_SCLK	SA1	201	202	SCL	
+0.75VS	VTT	203	204	VTT	
	GND1	205	206	BOSS1	
	GND2	207	208	BOSS2	

FOX_AS0A626-U2SN-7F_204P

CONN@

(6) DDR_A_CKE0
(6) DDR_A_BS2
(6) DDR_A_CLK0
(6) DDR_A_CLK0#
(6) DDR_A_BS0
(6) DDR_A_WE#
(6) DDR_A_CAS#
(6) DDR_A_CS1#

DDR_A_CKE1 (6)
DDR_A_CLK1 (6)
DDR_A_CLK1# (6)
DDR_A_BS1 (6)
DDR_A_RAS# (6)
DDR_A_CS0# (6)
DDR_A_ODT0 (6)
DDR_A_ODT1 (6)

DIMM_DRAMRST# (11)

PM_EXTTS#0_1 (5,11)
D_CK_SDATA (11,12)
D_CK_SCLK (11,12)

+0.75VS

7/14 Change

+DDR_VREF_CA_DIMM

R245 0_0402_5%

C230 2.2U_0603_6.3V4Z

C220 0.1U_0402_16V4Z

R293 10K_0402_5%

+3VS

C287 2.2U_0603_6.3V4Z

C276 0.1U_0402_16V4Z

R314 10K_0402_5%

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

10U_0805_6.3V6M C186
10U_0805_6.3V6M C204
10U_0805_6.3V6M C171
10U_0805_6.3V6M C187
10U_0805_6.3V6M C170
10U_0805_6.3V6M C205
0.1U_0402_16V4Z C538
0.1U_0402_16V4Z C547
0.1U_0402_16V4Z C559
0.1U_0402_16V4Z C569
330U_D2_2V_Y C197

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

1U_0603_10V4Z C294
1U_0603_10V4Z C280
1U_0603_10V4Z C292
1U_0603_10V4Z C281
10U_0805_6.3V6M C293

DDR3 SO-DIMM A
Standard Type

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: SCHEMATIC MB A5881

Size	Document Number	Rev
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(6) DDR_B_DQS#[0..7]
(6) DDR_B_D[0..63]
(6) DDR_B_DM[0..7]
(6) DDR_B_DQS[0..7]
(6) DDR_B_MA[0..15]

2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

2009/05/19
M2 Circuit unpop
Pop M3 Circuit

7/14 Change
M3 Circuit
(4) H_DIMMB_REF
R165 1 @ 2 0_0402_5%
VREF_DQB
Q81
2N7002_SOT23
@
(10,18) RST_GATE
RST_GATE
M1 Circuit
+V_DDR3_DIMM_REF
R166 1 2 0_0402_5%

C110 1 2 2.2U_0805_16V4Z
C122 1 2 0.1U_0402_16V4Z

+1.5V

JDIMM2

1	VREF_DQ	2	VSS		
3	VSS	4	DQ4	DDR_B_D0	DDR_B_D4
5	DQ0	6	DQ5	DDR_B_D1	DDR_B_D5
7	DQ1	8	VSS		
9	VSS	10	DQS0#	DDR_B_DM0	DDR_B_DQS#0
11	DM0	12	DQS0		DDR_B_DQS0
13	VSS	14	VSS		
15	DQ2	16	DQ6	DDR_B_D2	DDR_B_D6
17	DQ3	18	DQ7	DDR_B_D3	DDR_B_D7
19	VSS	20	VSS		
21	DQ8	22	DQ12	DDR_B_D8	DDR_B_D12
23	DQ9	24	DQ13	DDR_B_D9	DDR_B_D13
25	VSS	26	VSS		
27	DQS1#	28	DM1	DDR_B_DQS#1	DDR_B_DM1
29	DQS1	30	RESET#	DDR_B_DQS1	DIMM_DRAMRST#
31	VSS	32	VSS		
33	DQ10	34	DQ14	DDR_B_D10	DDR_B_D14
35	DQ11	36	DQ15	DDR_B_D11	DDR_B_D15
37	VSS	38	VSS		
39	DQ16	40	DQ20	DDR_B_D16	DDR_B_D20
41	DQ17	42	DQ21	DDR_B_D17	DDR_B_D21
43	VSS	44	VSS		
45	DQS2#	46	DM2	DDR_B_DQS#2	DDR_B_DM2
47	DQS2	48	VSS	DDR_B_DQS2	
49	VSS	50	DQ22		DDR_B_D22
51	DQ18	52	DQ23	DDR_B_D18	DDR_B_D23
53	DQ19	54	VSS	DDR_B_D19	
55	VSS	56	DQ28		DDR_B_D28
57	DQ24	58	DQ29	DDR_B_D24	DDR_B_D29
59	DQ25	60	VSS	DDR_B_D25	
61	VSS	62	DQS3#		DDR_B_DQS#3
63	DM3	64	DQS3	DDR_B_DM3	DDR_B_DQS3
65	VSS	66	VSS		
67	DQ26	68	DQ30	DDR_B_D26	DDR_B_D30
69	DQ27	70	DQ31	DDR_B_D27	DDR_B_D31
71	VSS	72	VSS		
73	CKE0	74	CKE1	DDR_B_CKE0	DDR_B_CKE1
75	VDD	76	VDD		
77	NC	78	A15		DDR_B_MA15
79	BA2	80	A14	DDR_B_BS2	DDR_B_MA14
81	VDD	82	VDD		
83	A12/BC#	84	A11	DDR_B_MA12	DDR_B_MA11
85	A9	86	A7	DDR_B_MA9	DDR_B_MA7
87	VDD	88	VDD		
89	A8	90	A6	DDR_B_MA8	DDR_B_MA6
91	A5	92	A4	DDR_B_MA5	DDR_B_MA4
93	VDD	94	VDD		
95	A3	96	A2	DDR_B_MA3	DDR_B_MA2
97	A1	98	A0	DDR_B_MA1	DDR_B_MA0
99	VDD	100	VDD		
101	CK0	102	CK1	DDR_B_CLK0	DDR_B_CLK1
103	CK0#	104	CK1#	DDR_B_CLK0#	DDR_B_CLK1#
105	VDD	106	VDD		
107	A10/AP	108	BA1	DDR_B_MA10	DDR_B_BS1
109	BA0	110	RAS#	DDR_B_BS0	DDR_B_RAS#
111	VDD	112	VDD		
113	WE#	114	S0#	DDR_B_WE#	DDR_B_CS0#
115	CAS#	116	ODT0	DDR_B_CAS#	DDR_B_ODT0
117	VDD	118	VDD		
119	A13	120	ODT1	DDR_B_MA13	DDR_B_ODT1
121	S1#	122	NC	DDR_B_CS1#	
123	VDD	124	VDD		
125	TEST	126	VREF_CA		DDR_VREF_CA_DIMM
127	VSS	128	VSS		
129	DQ32	130	DQ36	DDR_B_D32	DDR_B_D36
131	DQ33	132	DQ37	DDR_B_D33	DDR_B_D37
133	VSS	134	VSS		
135	DQS4#	136	DM4	DDR_B_DQS#4	DDR_B_DM4
137	DQS4	138	VSS	DDR_B_DQS4	
139	VSS	140	DQ38		DDR_B_D38
141	DQ34	142	DQ39	DDR_B_D34	DDR_B_D39
143	DQ35	144	VSS	DDR_B_D35	
145	VSS	146	DQ44		DDR_B_D44
147	DQ40	148	DQ45	DDR_B_D40	DDR_B_D45
149	DQ41	150	VSS	DDR_B_D41	
151	VSS	152	DQS5#		DDR_B_DQS#5
153	DM5	154	DQS5	DDR_B_DM5	DDR_B_DQS5
155	VSS	156	VSS		
157	DQ42	158	DQ46	DDR_B_D42	DDR_B_D46
159	DQ43	160	DQ47	DDR_B_D43	DDR_B_D47
161	VSS	162	VSS		
163	DQ48	164	DQ52	DDR_B_D48	DDR_B_D52
165	DQ49	166	DQ53	DDR_B_D49	DDR_B_D53
167	VSS	168	VSS		
169	DQS6#	170	DM6	DDR_B_DQS#6	DDR_B_DM6
171	DQS6	172	VSS	DDR_B_DQS6	
173	VSS	174	DQ54		DDR_B_D54
175	DQ50	176	DQ55	DDR_B_D50	DDR_B_D55
177	DQ51	178	VSS	DDR_B_D51	
179	VSS	180	DQ60		DDR_B_D60
181	DQ56	182	DQ61	DDR_B_D56	DDR_B_D61
183	DQ57	184	VSS	DDR_B_D57	
185	VSS	186	DQS7#		DDR_B_DQS#7
187	DM7	188	DQS7	DDR_B_DM7	DDR_B_DQS7
189	VSS	190	VSS		
191	DQ58	192	DQ62	DDR_B_D58	DDR_B_D62
193	DQ59	194	DQ63	DDR_B_D59	DDR_B_D63
195	VSS	196	VSS		
197	SA0	198	EVENT#		PM_EXTTS#0_1
199	VDDSPD	200	SDA		D_CK_SDATA
201	SA1	202	SCL		D_CK_SCLK
203	VTT	204	VTT		+0.75VS
205	GND1	206	BOSS1		
207	GND2	208	BOSS2		

TYCO_2-2013310-1_204P
CONN@

(6) DDR_B_CKE0
(6) DDR_B_BS2
(6) DDR_B_CLK0
(6) DDR_B_CLK0#
(6) DDR_B_BS0
(6) DDR_B_WE#
(6) DDR_B_CAS#
(6) DDR_B_CS1#

DDR_B_CKE1 (6)
DDR_B_CLK1 (6)
DDR_B_CLK1# (6)
DDR_B_BS1 (6)
DDR_B_RAS# (6)
DDR_B_CS0# (6)
DDR_B_ODT0 (6)
DDR_B_ODT1 (6)

+3VS
R294 1 2 10K_0402_5%
R315 1 2 10K_0402_5%
C288 1 2 2.2U_0603_6.3V4Z
C277 1 2 0.1U_0402_16V4Z

+DDR_VREF_CA_DIMM
DDR_VREF_CA_DIMM R246 1 2 0_0402_5%
7/14 Change
C231 1 2 2.2U_0603_6.3V4Z
C221 1 2 0.1U_0402_16V4Z

PM_EXTTS#0_1 (5,10)
D_CK_SDATA (10,12)
D_CK_SCLK (10,12)

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
10U_0805_6.3V6M
0.1U_0402_16V4Z
C172 C188 C206 C173 C189 C207 C546 C552 C540 C544 C198 330U_D2_2V_Y

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

+0.75VS
1U_0603_10V4Z
C295 C282 C283 C296 C298
10U_0805_6.3V6M

DDR3 SO-DIMM B
Standard Type

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Clock Generator

7/14 Change

+1.05VS
L44 FBMA-L11-201209-221LMA30T_0805
C563 10U_0805_10V4Z
C564 10U_0805_10V4Z
C565
C578 0.1U_0402_16V4Z
+CLK_VDDSRC

+1.5VS
L62 FBMA-L11-201209-221LMA30T_0805 @
+3VS
L45 FBMA-L11-201209-221LMA30T_0805
+CLK_VDD
C571 10U_0805_10V4Z
C570 10U_0805_10V4Z
C575 C582 C585 C581 C579 0.1U_0402_16V4Z

+3VS
L52 FBMA-L11-201209-221LMA30T_0805
+CLK_SE
C669 C670 C671 0.1U_0402_16V4Z
10U_0805_10V4Z

Integrated 33ohm Resistor
0_0404_4P2R_5%
RP30 CLK_BUF_DREF_96M / CLK_BUF_DREF_96M# → CLK_BUF_DREF_96M_R / CLK_BUF_DREF_96M#_R
RP29 CLK_BUF_PCIE_SATA / CLK_BUF_PCIE_SATA# → CLK_BUF_PCIE_SATA_R / CLK_BUF_PCIE_SATA#_R
RP28 CLK_BUF_CPU_DMI / CLK_BUF_CPU_DMI# → CLK_BUF_CPU_DMI_R / CLK_BUF_CPU_DMI#_R

PCH (14) CLK_BUF_DREF_96M / (14) CLK_BUF_DREF_96M#
PCH (14) CLK_BUF_PCIE_SATA / (14) CLK_BUF_PCIE_SATA#
PCH (14) CLK_BUF_CPU_DMI / (14) CLK_BUF_CPU_DMI#
VGA
Card reader (35) CLK_SD_48M
CLK_SD_48M → R628 33_0402_5% → CLK_SD_48M_R
C1227 22P_0402_50V8J

U36
VDD_USB_48 (1)
VSS_48M (2)
DOT_96 (3)
DOT_96# (4)
VDD_27 (5)
27MHZ (6)
27MHZ_SS (7)
USB_48 (8)
VSS_27M (9)
SATA (10)
SATA# (11)
VSS_SRC (12)
SRC_1 (13)
SRC_1# (14)
VDD_SRC_IO (15)
CPU_STOP# (16)
TGND (33)
SLG8SP587VTR_QFN32_5X5
<BOM Structure>
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY00
SILEGO SA00002XY00

SCL (32)
SDA (31)
REF_0/CPU_SEL (30) ← D_CK_SCLK / D_CK_SDATA / REF_0/CPU_SEL
VDD_REF (29)
XTAL_IN (28) ← CLK_XTAL_IN
XTAL_OUT (27) ← CLK_XTAL_OUT
VSS_REF (26)
CKPWRGD/PD# (25) ← CK505_PWRGD
VDD_CPU (24)
CPU_0 (23) ← CLK_BUF_CPU_BCLK_R
CPU_0# (22) ← CLK_BUF_CPU_BCLK#_R
VSS_CPU (21)
CPU_1 (20)
CPU_1# (19)
VDD_CPU_IO (18)
VDD_SRC (17)

R633 33_0402_5% → C1226 22P_0402_50V8J
D_CK_SCLK (10,11)
D_CK_SDATA (10,11)
CLK_BUF_ICH_14M (14) PCH

RP31 CLK_BUF_CPU_BCLK / CLK_BUF_CPU_BCLK# → CLK_BUF_CPU_BCLK_R / CLK_BUF_CPU_BCLK#_R
0_0404_4P2R_5%
CLK_BUF_CPU_BCLK (14)
CLK_BUF_CPU_BCLK# (14) PCH

Integrated 33ohm Resistor

reserve C1227,C1226 for EMI request 08/23

+3VS
Silego Have Internal Pull-Up
R627 10K_0402_5% H_STP_CPU#

IDT Have Internal Pull-Down
R634 10K_0402_5% REF_0/CPU_SEL

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

+3VS
R631 10K_0402_5%
R632 0_0402_5% @
CK505_PWRGD → VGATE (15,54)
Q45 2N7002_SOT23
CLK_ENABLE# (54)

+3VS
R638 4.7K_0402_5%
Q83A 2N7002DW-T/R7_SOT363-6
(14,36) PCH_SMBDATA
D_CK_SDATA
R951 0_0402_5% XDP@
SMB_DATA_S3 (5)

+3VS
R635 4.7K_0402_5%
Q83B 2N7002DW-T/R7_SOT363-6
(14,36) PCH_SMBCLK
D_CK_SCLK
R952 0_0402_5% XDP@
SMB_CLK_S3 (5)

CLK_XTAL_IN
C584 27P_0402_50V8J
Y4 14.31818MHz_20P_FSX8L14.318181M20FDB
C583 27P_0402_50V8J
CLK_XTAL_OUT

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RC Delay 18~25mS

close to RAM door

RC Delay 18~25mS

close to RAM door

HDA for AUDIO

HDA for MDC

32.768KHZ_12.5PF_Q13MC14610002

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

del R916 08/10

GPIO33 can not pull down
(manufacturing environments)

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull
under door.

reserve C1228,C1229 for EMI request 08/23

reserve C1230 for EMI request 08/23

Have internal PD

7/14 Change

2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R516, R517 on ES2 Sample

MP mount R689, R690,
R691, R692 and remove
others

enable iTPM: SPI_MOSI High

CRB 1.0 Change to 4.7K

add ME_EN reversed circuit 08/10

SATA for HDD1

SATA for ODD

2/10 SATA2, SATA3 not support on HM55

SATA for HDD2

1/6 Change from Port2 to Port4

11/18 SPI ROM Change to SA00002TO00

SPI ROM Footprint 150mil

11/18 SPI ROM Change to SA00002TO00

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U32B

REV1.0

IBEXPEAK-M_FCBGA107

For PCIE LAN

For Wireless LAN

For Mini2

2/10 PCIE7, PCIE8 not support on HM55

7/21 DEL

For PCIE LAN

For Wireless LAN

For Mini2

7/21 DEL

PCIECLKREQ(0,3,4,5,6,7)# Should have a 10K pull up to +3VALW,PCIECLKREQ(1,2),Should have a 10K pull up to +3VS

7/14 Change

7/17: Change to +3VALW

7/14 Change

20090512
add double mosfet prevent
ATI M92 electric leakage

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

7/14 Change

change Q77 to R1116,R1117 08/12

Add R1114,R1115 ,del R758 08/12

del PEG_CLKREQ# 08/17

change Q59 bom @ to SG@ 08/17

change R1115 from 2.2K to 0 ohm 08/17

change to 0 ohm 08/12

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

Project Port ID

7/17 Del CLK_CARD_48M

Project ID		
ID1	ID0	Project
* 0	0	JV
0	1	Future

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(4) DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
(4) DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
(4) DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
(4) DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

(4) H_FDI_TXN[0..7] H_FDI_TXN[0..7]
(4) H_FDI_TXP[0..7] H_FDI_TXP[0..7]

7/17 R110 Change BOM Structure for follow check list p.23

+3VS
R538 1 2 8.2K_0402_5% PM_CLKRUN#
R110 1 2 10K_0402_5% XDP_DBRESET#

+3VALW
7/14 Change
R529 1 2 10K_0402_5% SUS_PWR_ACK
R503 1 2 8.2K_0402_5% PCH_GPIO72
R72 1 2 10K_0402_5% EC_SWI#
R55 1 2 1K_0402_5% PCH_PCIE_WAKE#
R69 1 @ 2 10K_0402_5% PM_SLP_LAN#

7/17 R72 KAV60 DEL

+1.05VS
R590 1 2 49.9_0402_1%

U32C
REV1.0
IBEXPEAK-M_FCBGA107

DMI
DMI_HTX_PRX_N0 BC24 DMI0RXN
DMI_HTX_PRX_N1 BJ22 DMI1RXN
DMI_HTX_PRX_N2 AW20 DMI2RXN
DMI_HTX_PRX_N3 BJ20 DMI3RXN
DMI_HTX_PRX_P0 BD24 DMI0RXP
DMI_HTX_PRX_P1 BG22 DMI1RXP
DMI_HTX_PRX_P2 BA20 DMI2RXP
DMI_HTX_PRX_P3 BG20 DMI3RXP
DMI_PTX_HRX_N0 BE22 DMI0TXN
DMI_PTX_HRX_N1 BF21 DMI1TXN
DMI_PTX_HRX_N2 BD20 DMI2TXN
DMI_PTX_HRX_N3 BE18 DMI3TXN
DMI_PTX_HRX_P0 BD22 DMI0TXP
DMI_PTX_HRX_P1 BH21 DMI1TXP
DMI_PTX_HRX_P2 BC20 DMI2TXP
DMI_PTX_HRX_P3 BD18 DMI3TXP
DMI_COMP BF25
BH25 DMI_ZCOMP
DMI_IRCOMP

FDI
FDI_RXN0 BA18 H_FDI_TXN0
FDI_RXN1 BH17 H_FDI_TXN1
FDI_RXN2 BD16 H_FDI_TXN2
FDI_RXN3 BJ16 H_FDI_TXN3
FDI_RXN4 BA16 H_FDI_TXN4
FDI_RXN5 BE14 H_FDI_TXN5
FDI_RXN6 BA14 H_FDI_TXN6
FDI_RXN7 BC12 H_FDI_TXN7
FDI_RXP0 BB18 H_FDI_TXP0
FDI_RXP1 BF17 H_FDI_TXP1
FDI_RXP2 BC16 H_FDI_TXP2
FDI_RXP3 BG16 H_FDI_TXP3
FDI_RXP4 AW16 H_FDI_TXP4
FDI_RXP5 BD14 H_FDI_TXP5
FDI_RXP6 BB14 H_FDI_TXP6
FDI_RXP7 BD12 H_FDI_TXP7
FDI_INT BJ14 H_FDI_INT (4)
FDI_FSYNC0 BF13 H_FDI_FSYNC0 (4)
FDI_FSYNC1 BH13 H_FDI_FSYNC1 (4)
FDI_LSYNC0 BJ12 H_FDI_LSYNC0 (4)
FDI_LSYNC1 BG14 H_FDI_LSYNC1 (4)

System Power Management
(5) XDP_DBRESET# XDP_DBRESET# T6 SYS_RESET#
SYS_PWROK R58 0_0402_5% SYS_PWROK_R M6 SYS_PWROK
VGATE R70 @ 0_0402_5%
SYS_PWROK B17 PWROK
R877 2 1 0_0402_5%
K5 MEPWROK
LAN_RST# A10 LAN_RST#
(5) PM_DRAM_PWRGD D9 DRAMPWROK
PCH_RSMRST# C16 RSMRST#
(38) SUS_PWR_ACK SUS_PWR_ACK M1 SUS_PWR_DN_ACK / GPIO30
PBTN_OUT# P5 PWRBTN#
(23,38) ACIN_R R1160 2 1 0_0402_5% PCH_ACIN P7 ACPRESENT / GPIO31
PCH_GPIO72 A6 BATLOW# / GPIO72
(38) EC_SWI# EC_SWI# F14 RI#

WAKE# J12 PCH_PCIE_WAKE# PCH_PCIE_WAKE# (33,36)
CLKRUN# / GPIO32 Y1 PM_CLKRUN# PM_CLKRUN# (38)
SUS_STAT# / GPIO61 P8 PCH_GPIO61 @ PAD T4
SUSCLK / GPIO62 F3 PCH_GPIO62 @ PAD T7
SLP_S5# / GPIO63 F4 PM_SLP_S5# (38)
SLP_S4# H7 PM_SLP_S4# (38)
SLP_S3# P12 PM_SLP_S3# (38)
SLP_M# K8 PM_SLP_M# @ PAD T2
TP23 N2 PM_SLP_DSW# @ PAD T8
PMSYNCH BJ10 H_PM_SYNC (5)
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

10/2 Intel suggestion change to 10K
7/14 Change
+3VALW
@ R66 10K_0402_5%
Change D4 to R1160 08/21
change EC_ACIN net name to ACIN_R 08/21
del R917 08/21

R37 2 @ 1 0_0402_5%
+3VS
U2
NC7SZ08P5X_NL_SC70-5
SYS_PWROK EC_PWROK EC_PWROK (38)
VGATE VGATE (12,54)

SYS_PWROK R31 10K_0402_5%
EC_PWROK R41 10K_0402_5%
LAN_RST# R506 10K_0402_5%
No used Integrated LAN, connecting LAN_RST# to GND

R30 @ 0_0402_5%
Q4 MMBT3906_SOT23-3
PCH_RSMRST# EC_RSMRST# (38)
R32 10K_0402_5%
R27 4.7K_0402_5% +3VALW
7/14 Change
D3A BAV99DW-7_SOT363
D3B BAV99DW-7_SOT363
R39 2.2K_0402_5%

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7/14 Change

+3VS
11/21 intel JIM suggest Pull high at LVDS Conn

R132 10K_0402_5% LCTLA_CLK
R123 10K_0402_5% LCTLB_DATA
R534 2.2K_0402_5% PCH_CRT_CLK
R532 2.2K_0402_5% PCH_CRT_DATA

R542 PCH_CRT_B 150_0402_1%
R544 PCH_CRT_G 150_0402_1%
R545 PCH_CRT_R 150_0402_1%

U32D

IGPU_BKLT_EN T48 L_BKLTEN
(29) PCH_ENVDD T47 L_VDD_EN
(29) DPST_PWM Y48 L_BKLTCTL
(29) PCH_LCD_CLK PCH_LCD_CLK AB48 L_DDC_CLK
(29) PCH_LCD_DATA PCH_LCD_DATA Y45 L_DDC_DATA
LCTLA_CLK AB46 L_CTRL_CLK
LCTLB_DATA V48 L_CTRL_DATA
R140 1 UMA@ 2 2.37K_0402_1% LVDS_IBG AP39 LVD_IBG
R150 1 UMA@ 2 0_0402_5% LVD_VREF AT43 LVD_VREFH
AP41 LVD_VBG
AT42 LVD_VREFL

(29) PCH_TXCLK- PCH_TXCLK- AV53 LVDSA_CLK#
(29) PCH_TXCLK+ PCH_TXCLK+ AV51 LVDSA_CLK
(29) PCH_TXOUT0- PCH_TXOUT0- BB47 LVDSA_DATA#0
(29) PCH_TXOUT1- PCH_TXOUT1- BA52 LVDSA_DATA#1
(29) PCH_TXOUT2- PCH_TXOUT2- AY48 LVDSA_DATA#2
AV47 LVDSA_DATA#3
(29) PCH_TXOUT0+ PCH_TXOUT0+ BB48 LVDSA_DATA0
(29) PCH_TXOUT1+ PCH_TXOUT1+ BA50 LVDSA_DATA1
(29) PCH_TXOUT2+ PCH_TXOUT2+ AY49 LVDSA_DATA2
AV48 LVDSA_DATA3

(29) PCH_TZCLK- PCH_TZCLK- AP48 LVDSB_CLK#
(29) PCH_TZCLK+ PCH_TZCLK+ AP47 LVDSB_CLK
(29) PCH_TZOUT0- PCH_TZOUT0- AY53 LVDSB_DATA#0
(29) PCH_TZOUT1- PCH_TZOUT1- AT49 LVDSB_DATA#1
(29) PCH_TZOUT2- PCH_TZOUT2- AU52 LVDSB_DATA#2
AT53 LVDSB_DATA#3
(29) PCH_TZOUT0+ PCH_TZOUT0+ AY51 LVDSB_DATA0
(29) PCH_TZOUT1+ PCH_TZOUT1+ AT48 LVDSB_DATA1
(29) PCH_TZOUT2+ PCH_TZOUT2+ AU50 LVDSB_DATA2
AT51 LVDSB_DATA3

LVDS

(30) PCH_CRT_B PCH_CRT_B AA52 CRT_BLUE
(30) PCH_CRT_G PCH_CRT_G AB53 CRT_GREEN
(30) PCH_CRT_R PCH_CRT_R AD53 CRT_RED
(30) PCH_CRT_CLK PCH_CRT_CLK V51 CRT_DDC_CLK
(30) PCH_CRT_DATA PCH_CRT_DATA V53 CRT_DDC_DATA
(30) PCH_CRT_HSYNC Y53 CRT_HSYNC
(30) PCH_CRT_VSYNC Y51 CRT_VSYNC
CRT_IREF AD48 DAC_IREF
AB51 CRT_IRTN

CRT

Digital Display Interface

SDVO_TVCLKINN BJ46
SDVO_TVCLKINP BG46
SDVO_STALLN BJ48
SDVO_STALLP BG48
SDVO_INTN BF45
SDVO_INTP BH45
SDVO_CTRLCLK T51
SDVO_CTRLDATA T53
DDPB_AUXN BG44
DDPB_AUXP BJ44
DDPB_HPD AU38
DDPB_0N BD42
DDPB_0P BC42
DDPB_1N BJ42
DDPB_1P BG42
DDPB_2N BB40
DDPB_2P BA40
DDPB_3N AW38
DDPB_3P BA38
DDPC_CTRLCLK Y49
DDPC_CTRLDATA AB49
DDPC_AUXN BE44
DDPC_AUXP BD44
DDPC_HPD AV40
DDPC_0N BE40
DDPC_0P BD40
DDPC_1N BF41
DDPC_1P BH41
DDPC_2N BD38
DDPC_2P BC38
DDPC_3N BB36
DDPC_3P BA36
DDPD_CTRLCLK U50
DDPD_CTRLDATA U52
DDPD_AUXN BC46
DDPD_AUXP BD46
DDPD_HPD AT38
DDPD_0N BJ40
DDPD_0P BG40
DDPD_1N BJ38
DDPD_1P BG38
DDPD_2N BF37
DDPD_2P BH37
DDPD_3N BE36
DDPD_3P BD36

REV1.0

IBEXPEAK-M_FCBGA107
<BOM Structure>

R126 1K_0402_0.5%
2/3 Change to 1K_0402_0.5% from Intel Suggestion. (EDS 1.0 is incorrect)

change Bom structure UMA@→UMA@ 08/18

SDVO_SCLK (31)
SDVO_SDATA (31)
R151 1 UMA@ 2 100K_0402_5%
PCH_DPB_HPD (31,38)

PCH_DPB_N0 C462 UMA@ 0.1U_0402_16V7K PCH_TMDS_D2# (31)
PCH_DPB_P0 C461 UMA@ 0.1U_0402_16V7K PCH_TMDS_D2 (31) HDMI D2
PCH_DPB_N1 C466 UMA@ 0.1U_0402_16V7K PCH_TMDS_D1# (31)
PCH_DPB_P1 C465 UMA@ 0.1U_0402_16V7K PCH_TMDS_D1 (31) HDMI D1
PCH_DPB_N2 C460 UMA@ 0.1U_0402_16V7K PCH_TMDS_D0# (31)
PCH_DPB_P2 C459 UMA@ 0.1U_0402_16V7K PCH_TMDS_D0 (31) HDMI D0
PCH_DPB_N3 C464 UMA@ 0.1U_0402_16V7K PCH_TMDS_CK# (31)
PCH_DPB_P3 C463 UMA@ 0.1U_0402_16V7K PCH_TMDS_CK (31) HDMI CLK

change PWMSEL_1# net name to DGPU_PWMSEL# 08/17

U40
(23) VGA_BKL_EN
IGPU_BKLT_EN
(17,29) DGPU_PWMSEL#
(29) IGPU_PWM_SELECT#
1A VCC
2A 1B
1OE# 2B
2OE# GND
SN74CBTD3306CPWR_TSSOP8
SG@

+5VS C646 SG@ 0.1U_0402_16V4Z
ENBKL
ENBKL (38)
R747 100K_0402_5%

IGPU_BKLT_EN R705 1 UMA@ 2 0_0402_5% ENBKL
Reserved for UMA Only
VGA_BKL_EN R1123 1 DISO@ 2 0_0402_5% ENBKL

7/17 Del R760 (Dis only)
Add R1123 (Dis only) 08/18

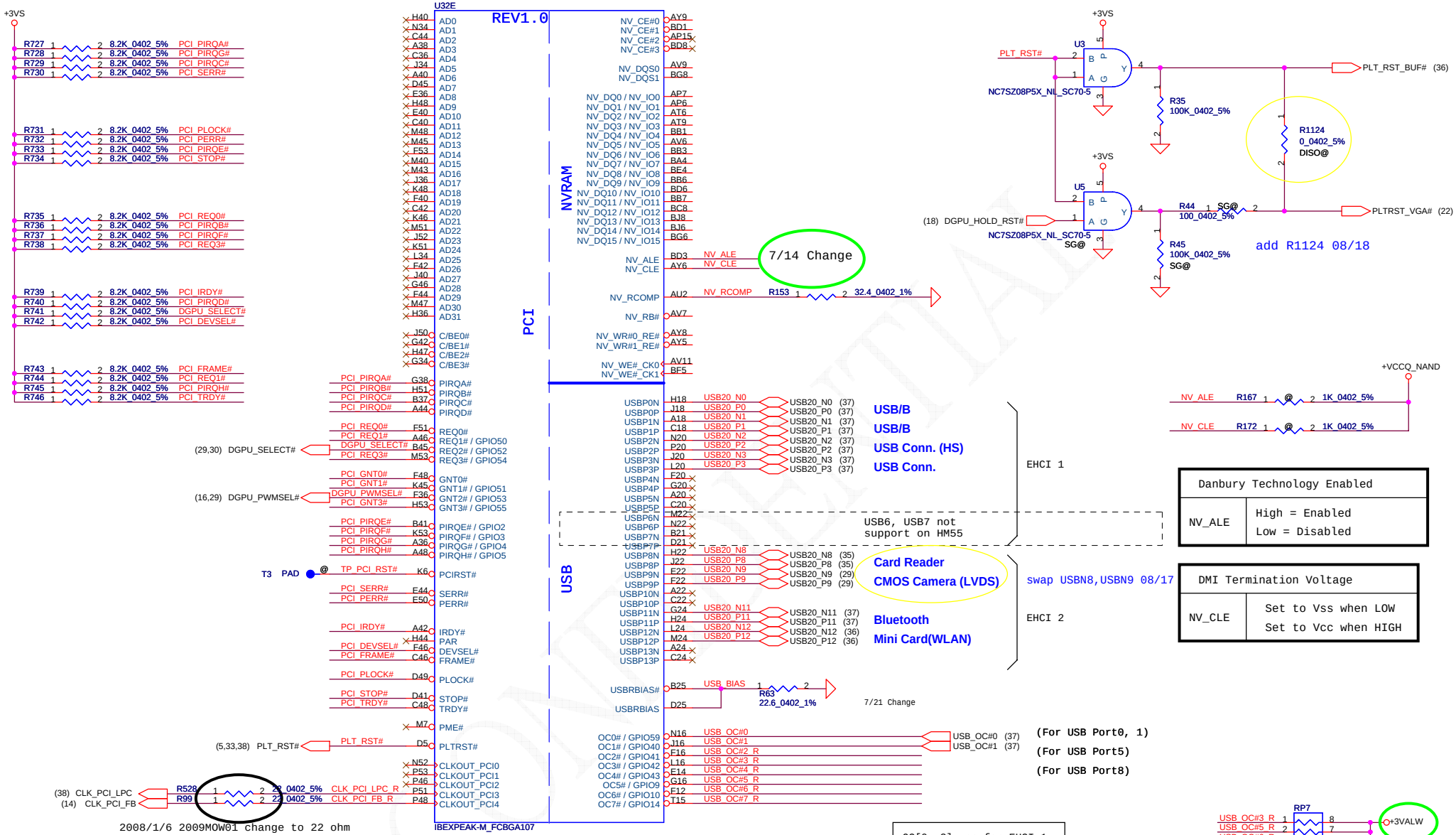
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: SCHEMATIC MB A5881

Size: Custom | Document Number: 401805 | Rev: A

Date: Tuesday, September 01, 2009 | Sheet 16 of 60



Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI *

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

Security Classification	Compal Secret Data		
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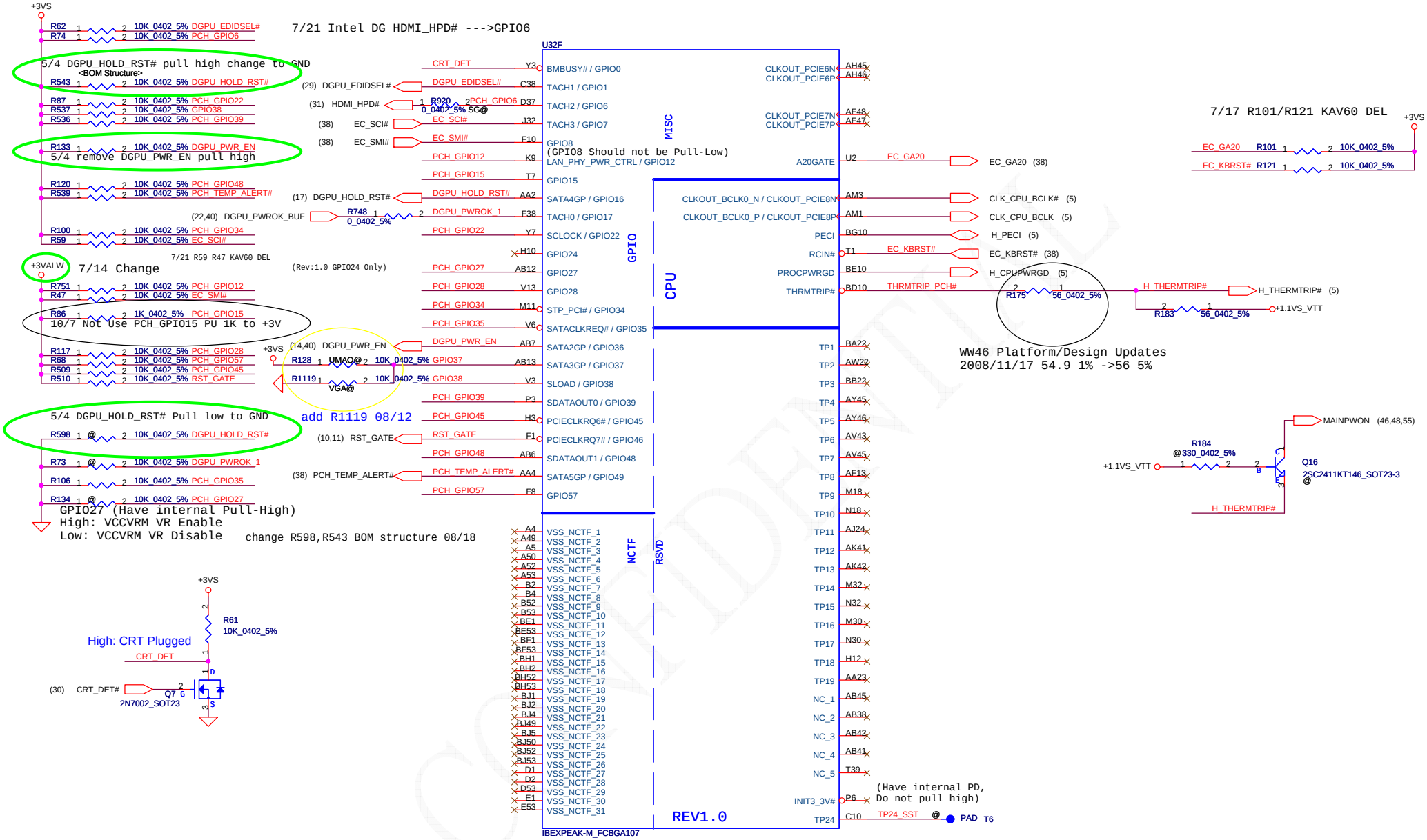
Size: Custom | Document Number: 401805 | Rev: A

Date: Tuesday, September 01, 2009 | Sheet 17 of 60



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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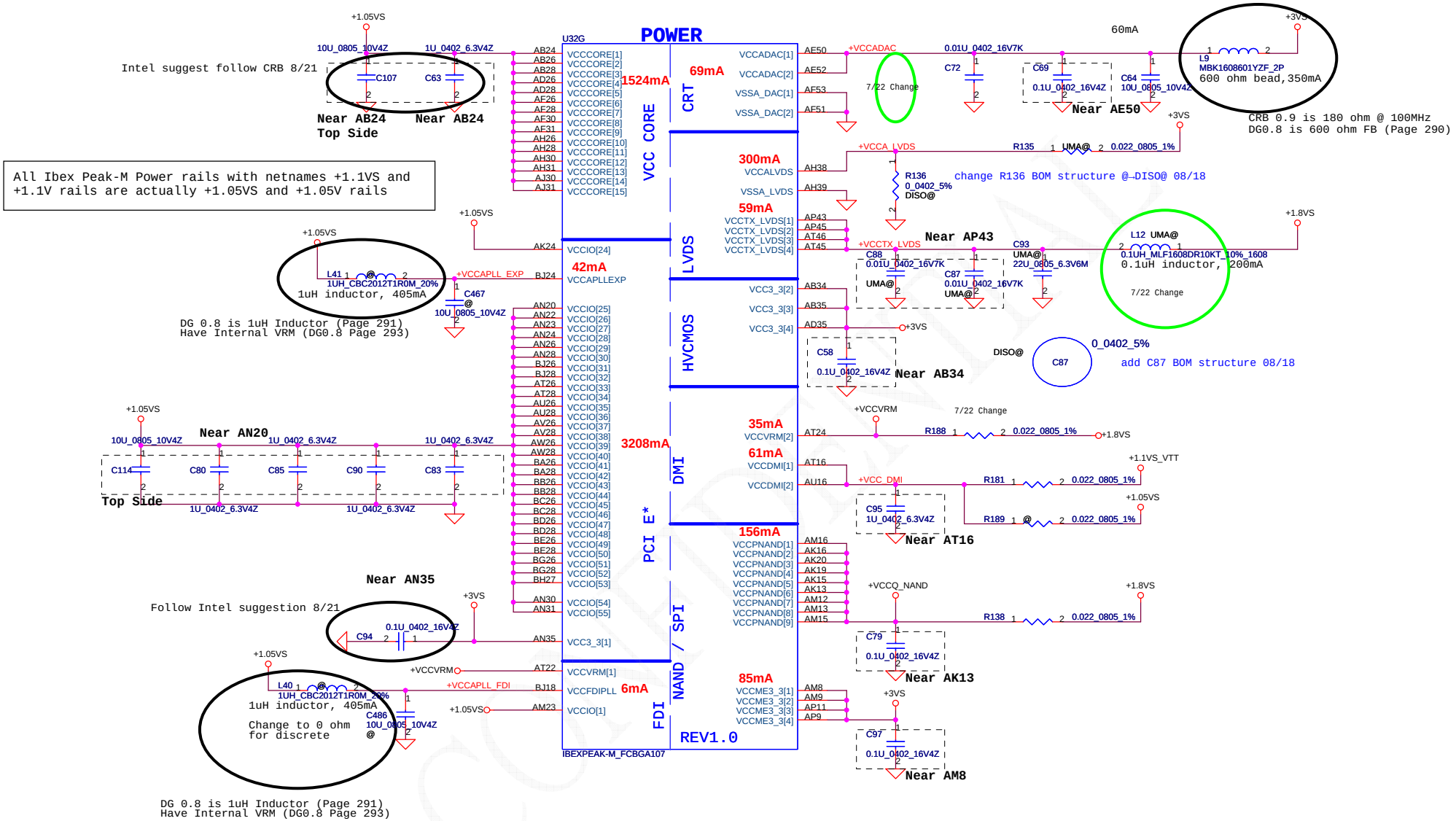
Size	Document Number	Rev
Custom	401805	A

Date: Tuesday, September 01, 2009 | Sheet 18 of 60



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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Size: Custom | Document Number: 401805 | Rev: A

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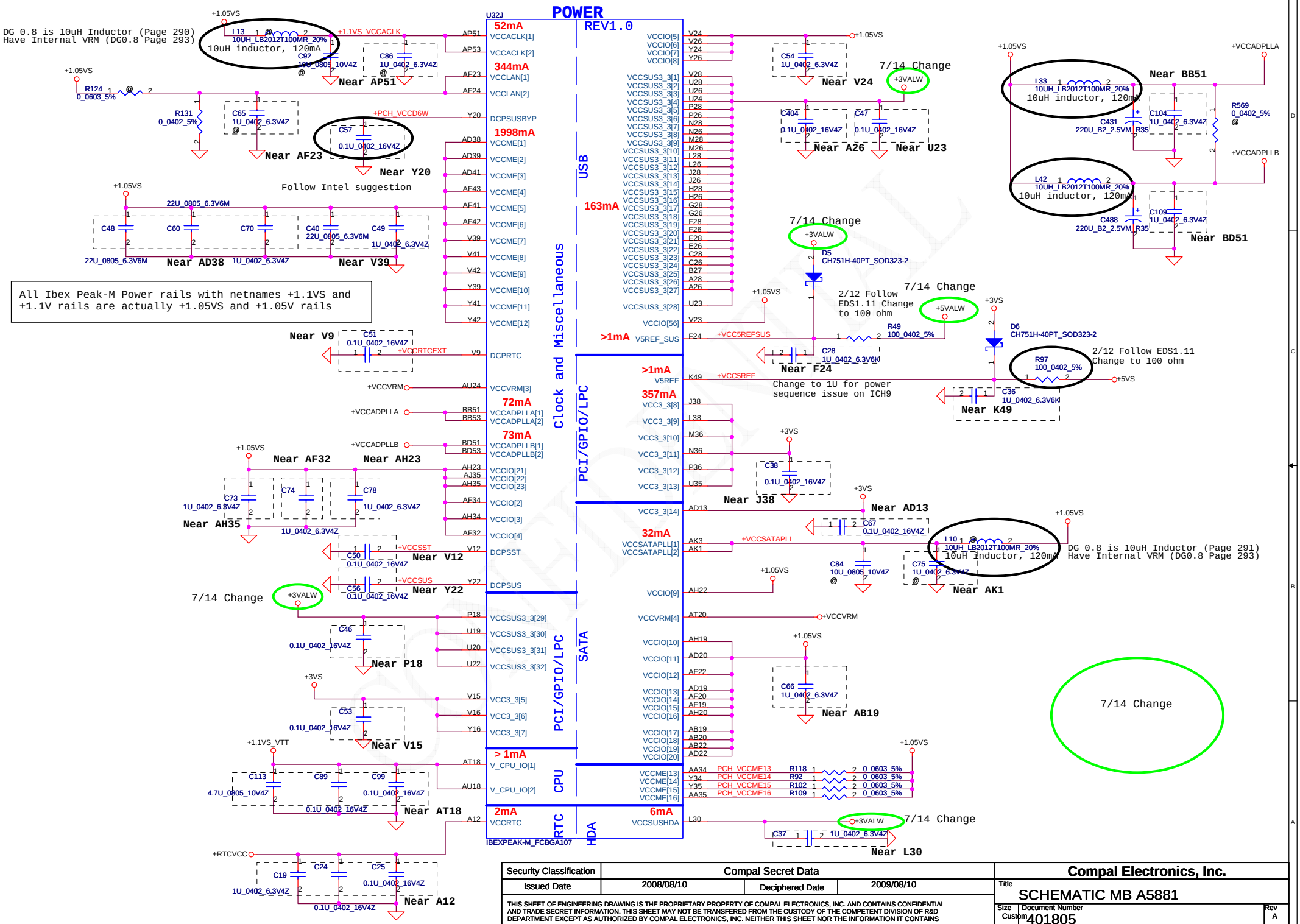

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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Size	Document Number	Rev
Custom	401805	A

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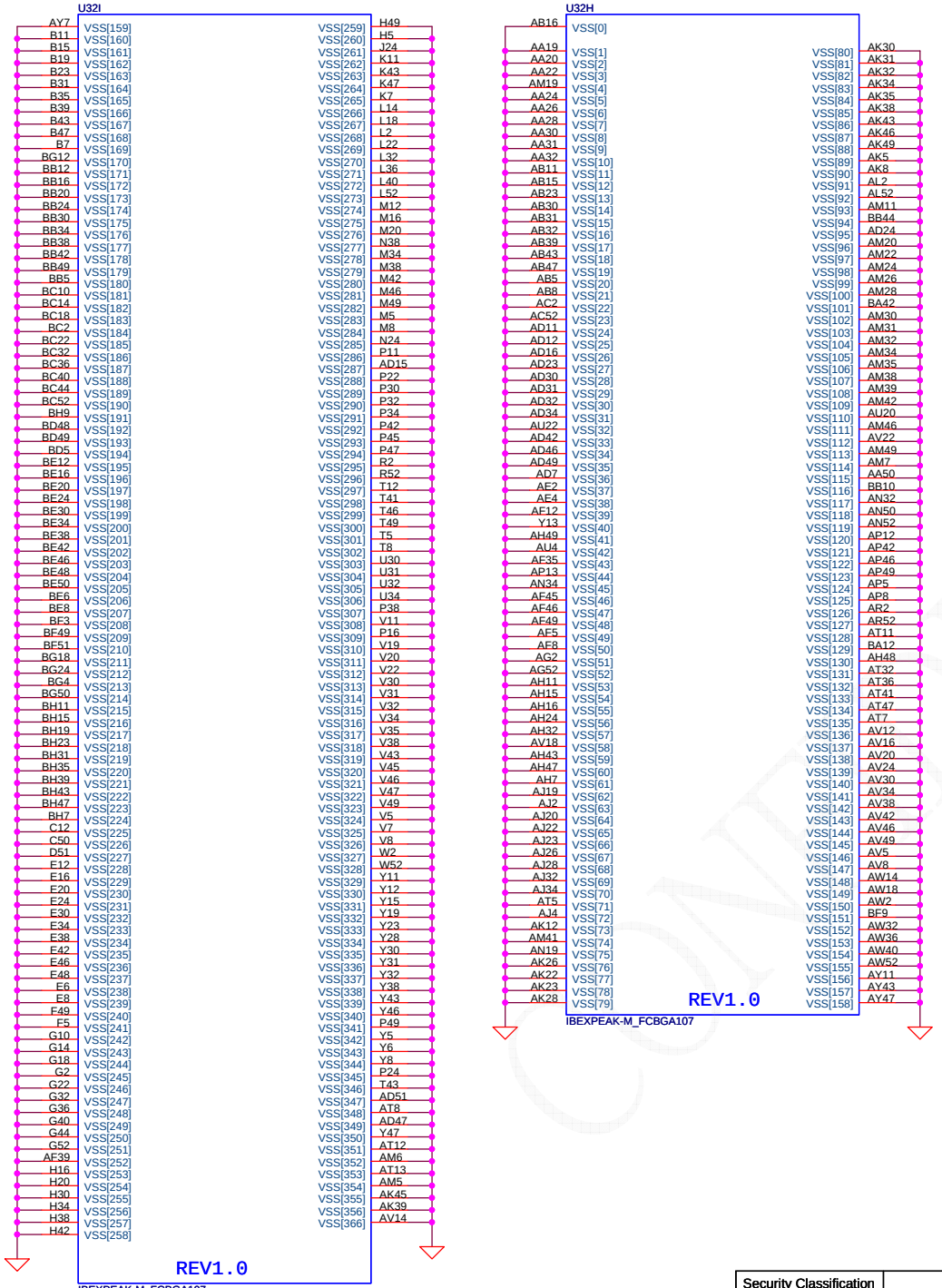

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

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PARK@ U75

216-0774007 All PARK PRO M2 0FA

U75A

PCI EXPRESS INTERFACE

(4) PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_GTX_HRX_P0	C932	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P0 (4)
(4) PEG_HTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_GTX_HRX_N0	C933	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N0 (4)
(4) PEG_HTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_GTX_HRX_P1	C934	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P1 (4)
(4) PEG_HTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_GTX_HRX_N1	C935	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N1 (4)
(4) PEG_HTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_GTX_HRX_P2	C936	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P2 (4)
(4) PEG_HTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_GTX_HRX_N2	C937	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N2 (4)
(4) PEG_HTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_GTX_HRX_P3	C938	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P3 (4)
(4) PEG_HTX_C_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_GTX_HRX_N3	C939	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N3 (4)
(4) PEG_HTX_C_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_GTX_HRX_P4	C940	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P4 (4)
(4) PEG_HTX_C_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_GTX_HRX_N4	C941	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N4 (4)
(4) PEG_HTX_C_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_GTX_HRX_P5	C942	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P5 (4)
(4) PEG_HTX_C_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_GTX_HRX_N5	C943	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N5 (4)
(4) PEG_HTX_C_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_GTX_HRX_P6	C944	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P6 (4)
(4) PEG_HTX_C_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_GTX_HRX_N6	C945	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N6 (4)
(4) PEG_HTX_C_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_GTX_HRX_P7	C946	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P7 (4)
(4) PEG_HTX_C_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_GTX_HRX_N7	C947	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N7 (4)
(4) PEG_HTX_C_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_GTX_HRX_P8	C948	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P8 (4)
(4) PEG_HTX_C_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_GTX_HRX_N8	C949	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N8 (4)
(4) PEG_HTX_C_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_GTX_HRX_P9	C950	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P9 (4)
(4) PEG_HTX_C_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_GTX_HRX_N9	C951	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N9 (4)
(4) PEG_HTX_C_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_GTX_HRX_P10	C952	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P10 (4)
(4) PEG_HTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_GTX_HRX_N10	C953	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N10 (4)
(4) PEG_HTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_GTX_HRX_P11	C954	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P11 (4)
(4) PEG_HTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_GTX_HRX_N11	C955	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N11 (4)
(4) PEG_HTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_GTX_HRX_P12	C956	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P12 (4)
(4) PEG_HTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_GTX_HRX_N12	C957	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N12 (4)
(4) PEG_HTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_GTX_HRX_P13	C958	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P13 (4)
(4) PEG_HTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_GTX_HRX_N13	C959	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N13 (4)
(4) PEG_HTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_GTX_HRX_P14	C960	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P14 (4)
(4) PEG_HTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_GTX_HRX_N14	C961	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N14 (4)
(4) PEG_HTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_GTX_HRX_P15	C962	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_P15 (4)
(4) PEG_HTX_C_GRX_N15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_GTX_HRX_N15	C963	VGA@ 0.1U_0402_16V7K	PEG_GTX_C_HRX_N15 (4)

CLOCK

(14) CLK_PEG_VGA	AB35	PCIE_REFCLKP
(14) CLK_PEG_VGA#	AA36	PCIE_REFCLKN

	AJ21	NC#1
	AK21	NC#2
(18,40) DGPU_PWROK_BUF	AH16	NC_PWRGOOD

(17) PLTRST_VGA#	AA30	PERSTB

CALIBRATION

PCIE_CALRP	Y30	R961 VGA@ 1.27K_0402_1%	
PCIE_CALRN	Y29	R963 VGA@ 2K_0402_1%	+1.1VSDGPU

R962 0_0402_5% @

8/10 change net name

R964 10K_0402_1% VGA@

Mannhatton Only
NC in M96

216-0772000 MADISON PRO FCBFA OFA
MAD@

M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)
M92 P/N : SA00002YX10 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FA)

MADISON P/N:SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
PARK P/N:SA00003MC00 (S IC 216-0774007 All PARK PRO M2 0FA)

add for DPST support.

U75G

R959 10K_0402_5% VGA@
R960 10K_0402_5% VGA@

LVDS CONTROL

VARY_BL	AK27	VGA_PNL_PWM (29)	
DIGON	AJ27	ENVDD (29)	
TXCLK_UP_DPF3P	AK35	VGA_TZCLK+	VGA_TZCLK+ (29)
TXCLK_UN_DPF3N	AL36	VGA_TZCLK-	VGA_TZCLK- (29)
TXOUT_U0P_DPF2P	AJ38	VGA_TZOUT0+	VGA_TZOUT0+ (29)
TXOUT_U0N_DPF2N	AK37	VGA_TZOUT0-	VGA_TZOUT0- (29)
TXOUT_U1P_DPF1P	AH35	VGA_TZOUT1+	VGA_TZOUT1+ (29)
TXOUT_U1N_DPF1N	AJ36	VGA_TZOUT1-	VGA_TZOUT1- (29)
TXOUT_U2P_DPF0P	AG38	VGA_TZOUT2+	VGA_TZOUT2+ (29)
TXOUT_U2N_DPF0N	AH37	VGA_TZOUT2-	VGA_TZOUT2- (29)
TXOUT_U3P	AF35	T15	
TXOUT_U3N	AG36	T14	

LVTMDP

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ (29)
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- (29)
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ (29)
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- (29)
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ (29)
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- (29)
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ (29)
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- (29)
TXOUT_L3P	AN36	T16	
TXOUT_L3N	AP37	T17	

216-0772000 MADISON PRO FCBFA OFA
MAD@

Security Classification	Compal Secret Data		
Issued Date	2009/7/14	Deciphered Date	2010/07/14

Compal Electronics, Inc.

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Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 256 MB 001 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	O	O	O	O
HYNIX	1	O	O	O

External VGA Thermal Sensor

U76 ADM1032ARMZ-2REEL_MSOP8 (VDD, D+, D-, THERM#, SCLK, SDATA, ALERT#, GND)

+3VS_DELAY

8/10 change circuit — Q100 SI2301BDS_SOT23 — 100mA

Madison & Park Power Up

+3VS_DELAY, VGA_CORE (VDDC), +1.8VS

FLASH ROM

del U77,R1011,R1012,C988 08/12

HDMI

CRT

M96 only

change EC_ACIN net name to ACIN_R 08/21

del R982,R981,R980,R979 08/12

Do not PU R177 for GPIO22 if not implement external flash ROM

change R1107 from 2.2K to 10K 08/27

change to 0402 08/12

add R1125 08/18

del C984 08/18

change R1010 from 0603 to 0402 08/18

Security Classification	Compal Secret Data		
Issued Date	2009/7/14	Deciphered Date	2010/07/14

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Size: C | Document Number: 401805 | Rev: A

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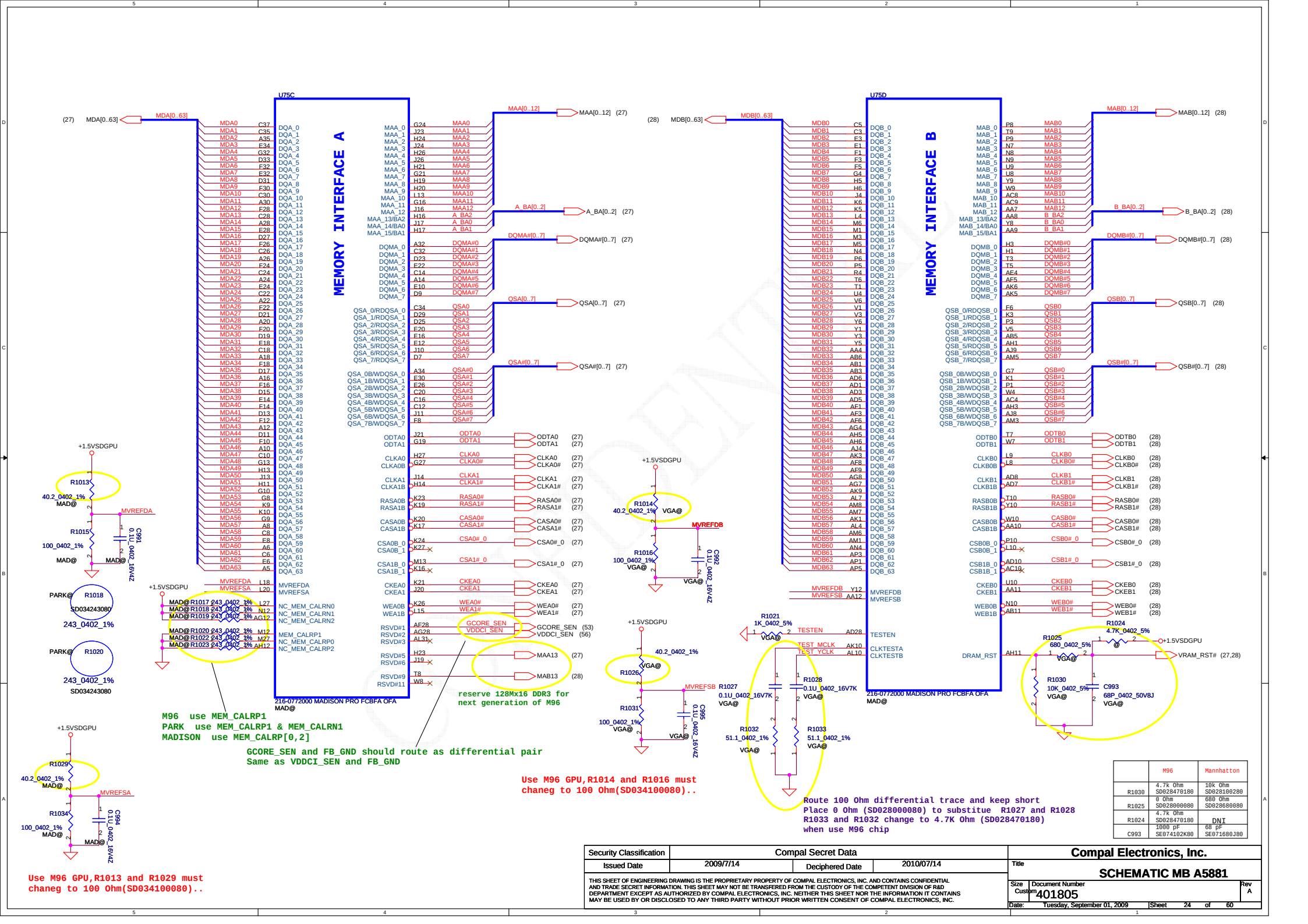
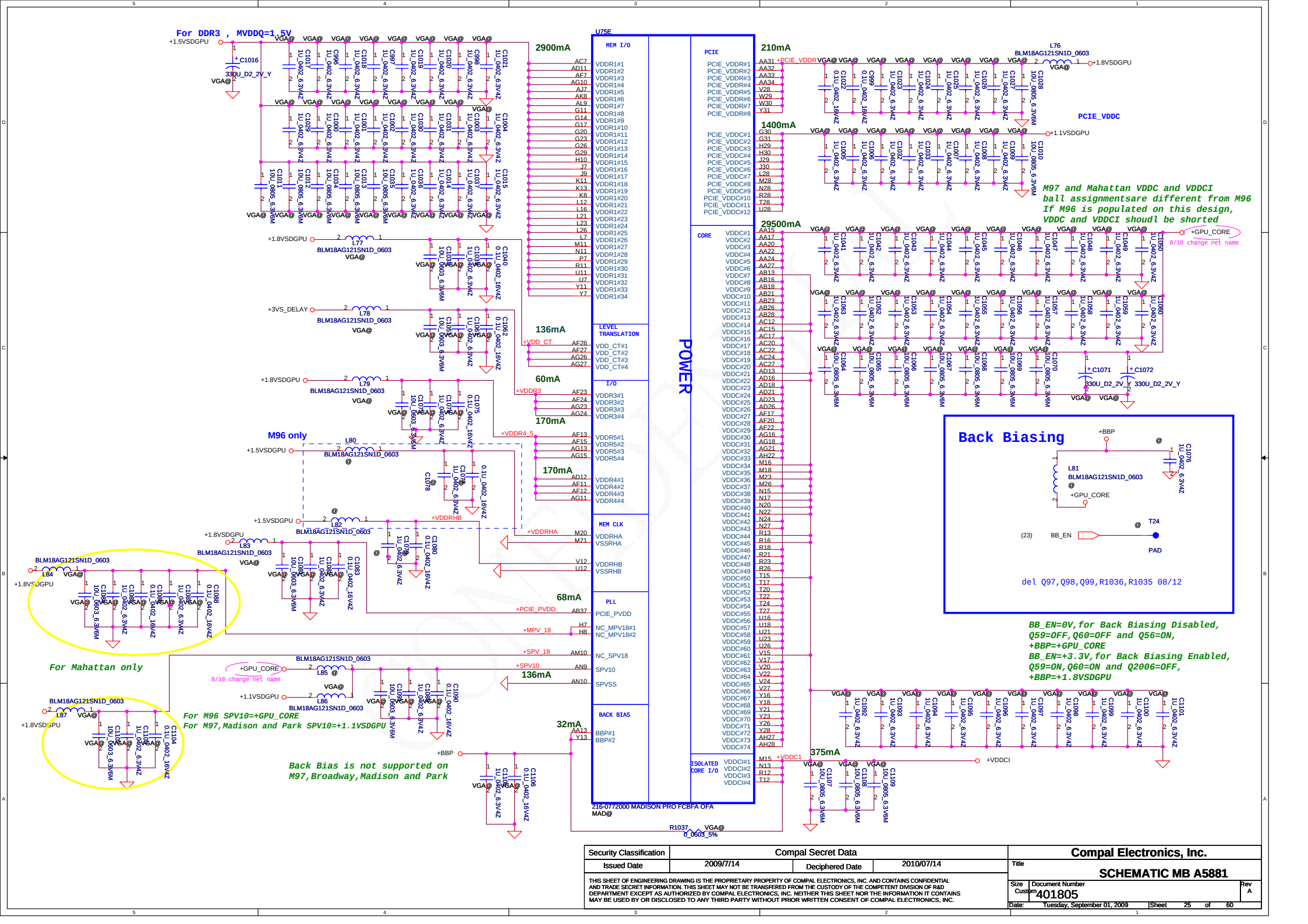


	M96	Mannhatton
R1030	4.7k Ohm SD028470180	10k Ohm SD028100280
R1025	0 Ohm SD028000080	680 Ohm SD028680080
R1024	4.7k Ohm SD028470180	DNI
C993	1000 pF SE074102K80	68 pF SE071680J80



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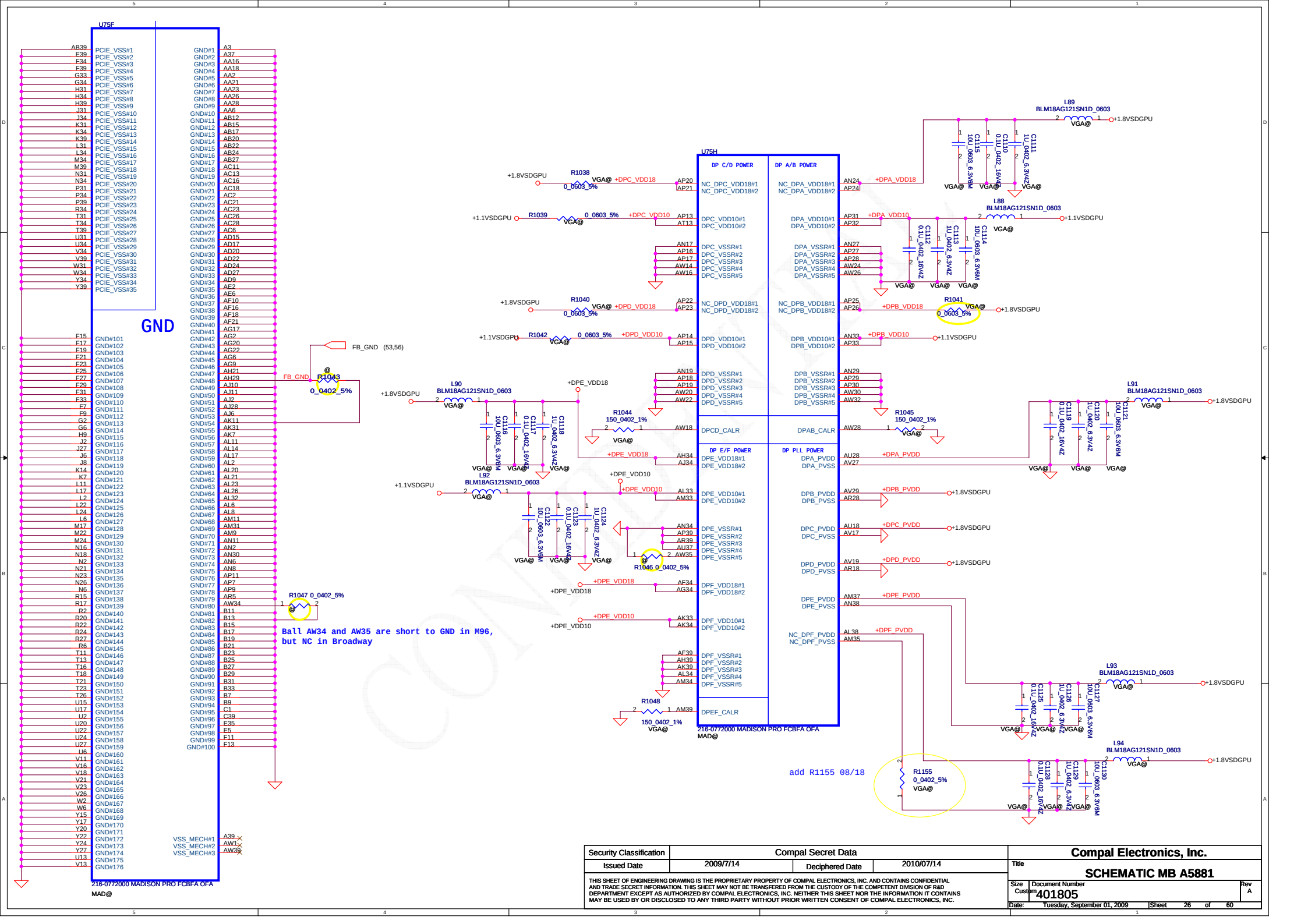
U75F
GND
216-0772000 MADISON PRO FCBFA OFA
MAD@
U75H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
216-0772000 MADISON PRO FCBFA OFA
MAD@
FB_GND (53,56)
R1043 @ 0_0402_5%
R1047 0_0402_5%
Ball AW34 and AW35 are short to GND in M96, but NC in Broadway
R1046 @ 0_0402_5%
R1048 150_0402_1%
R1044 150_0402_1%
R1045 150_0402_1%
R1041 0_0603_5%
add R1155 08/18
R1155 0_0402_5% VGA@
L89 BLM18AG121SN1D_0603
L88 BLM18AG121SN1D_0603
L90 BLM18AG121SN1D_0603
L91 BLM18AG121SN1D_0603
L92 BLM18AG121SN1D_0603
L93 BLM18AG121SN1D_0603
L94 BLM18AG121SN1D_0603
+1.8VSDGPU
+1.1VSDGPU
+1.1VSDGPU
+DPA_VDD18
+DPA_VDD10
+DPB_VDD18
+DPB_VDD10
+DPC_VDD18
+DPC_VDD10
+DPD_VDD18
+DPD_VDD10
+DPE_VDD18
+DPE_VDD10
+DPA_PVDD
+DPB_PVDD
+DPC_PVDD
+DPD_PVDD
+DPE_PVDD
+DPF_PVDD
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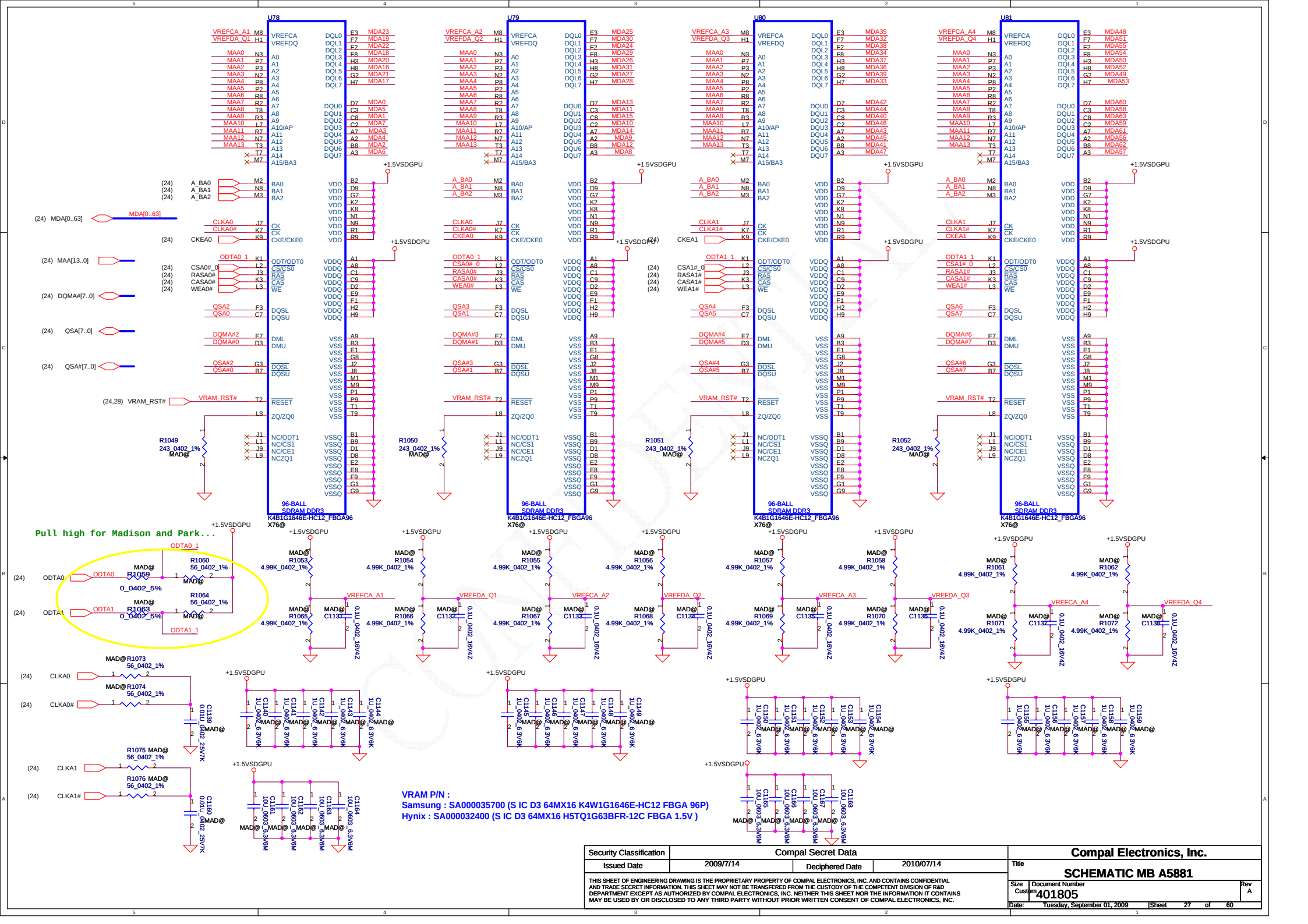

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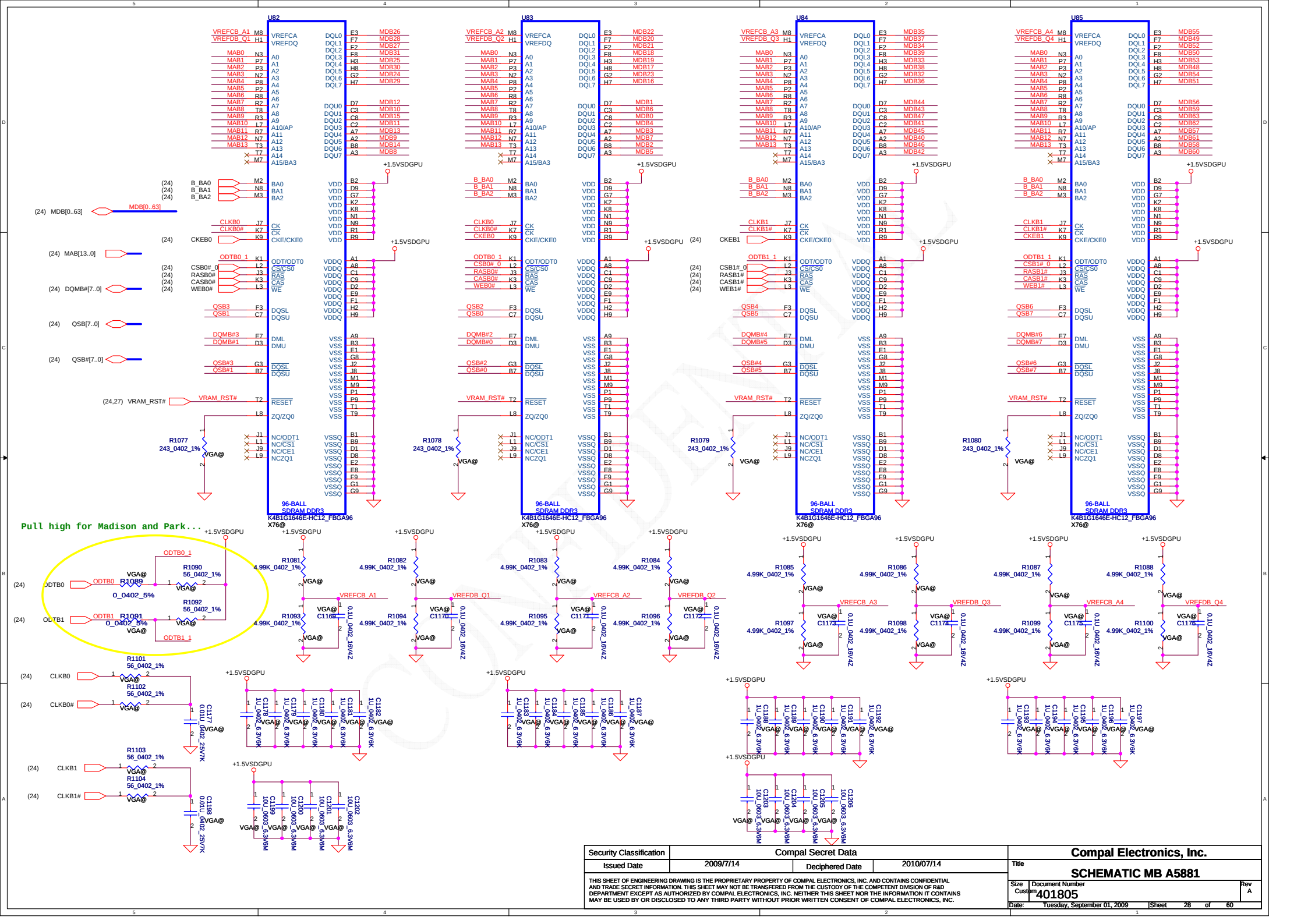

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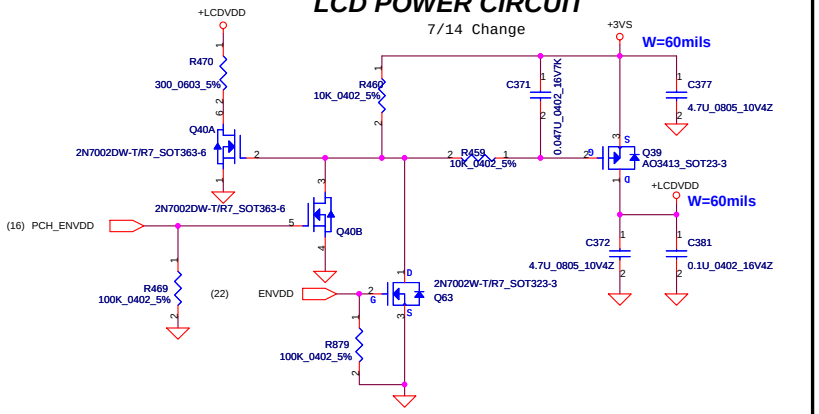
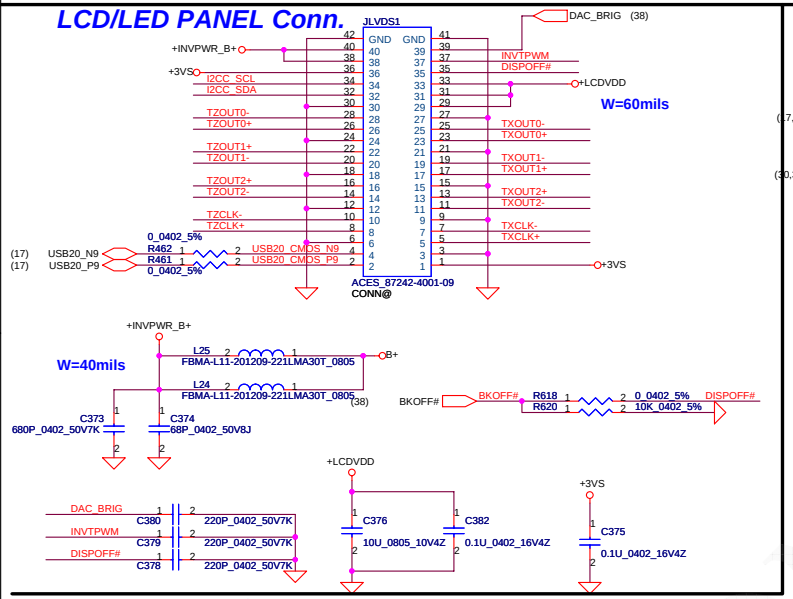
LCD POWER CIRCUIT

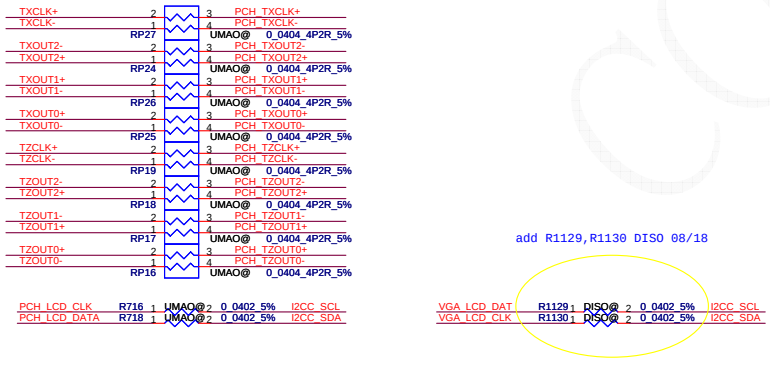
7/14 Change



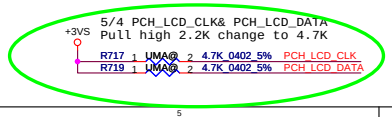
LCD/LED PANEL Conn.



UMA ONLY

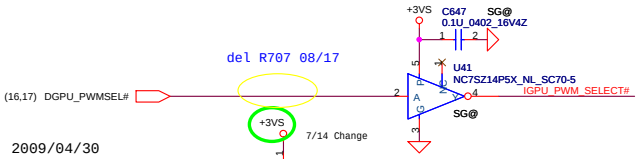


add R1129,R1130 DISO 08/18

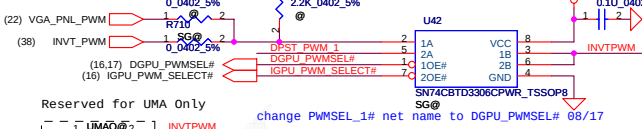


7/21 DEL R464 R878

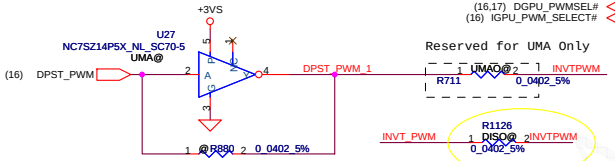
del R707 08/17



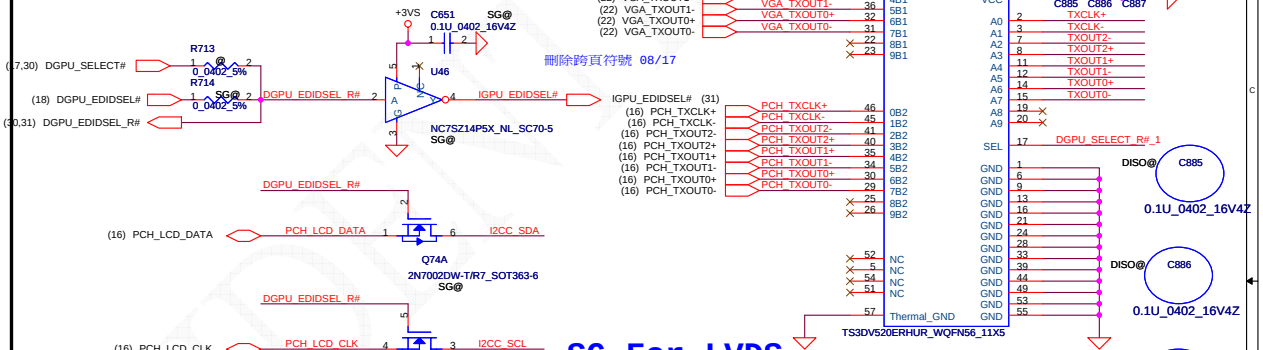
2009/04/30
R709 move to R710



change PWMSEL_1# net name to DGPU_PWMSEL# 08/17

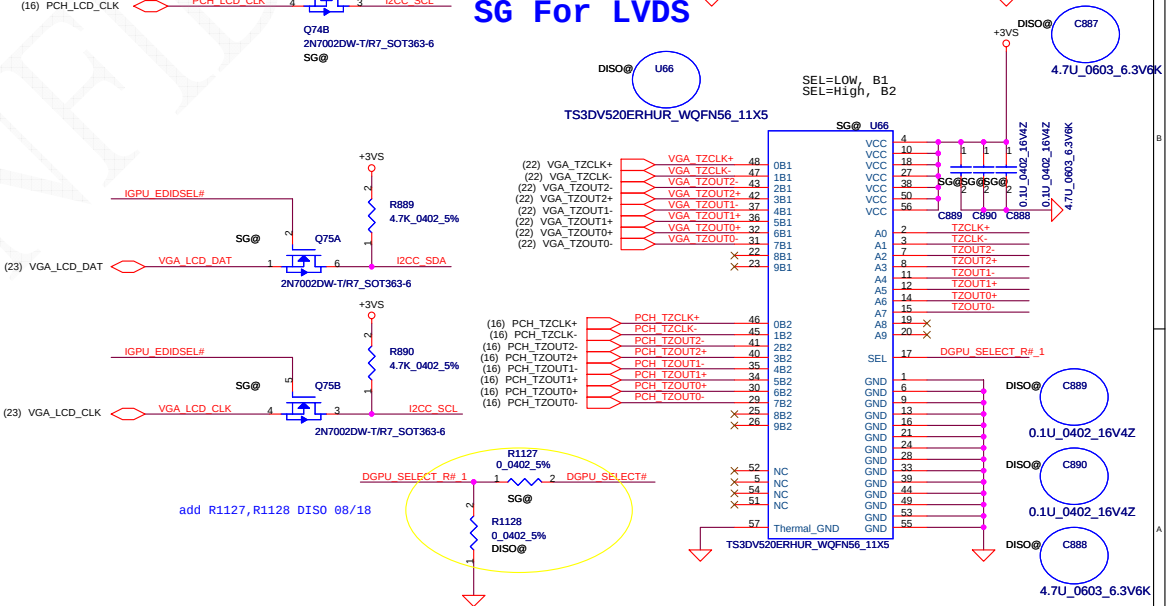


add R1126 DISO 08/18



删除跨頁符號 08/17

SG For LVDS



add R1127,R1128 DISO 08/18

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CRT Connector

Change L31,L28,L26,C415,C411,C405,C412,C409,C401
BOM structure UMA@→POP 08/18

Change to 0 ohm for Discrete

Change to 15pf for Discrete

Change to 12pf for Discrete

W=40mils

W=40mils

D26 DAN217_SC59 D25 DAN217_SC59 D24 DAN217_SC59

+5VS +R_CRT_VCC +CRT_VCC

D2 RB491D_SC59-3 F1 1.1A_6VDC_FUSE C399 0.1U_0402_16V4Z

+3VS

CRT_R CRT_G CRT_B

L31 0_0805_5% L28 0_0805_5% L26 0_0805_5%

CRT_R_1 CRT_G_1 CRT_B_1

L32 FCM2012CF-800T06_2P L29 FCM2012CF-800T06_2P L27 FCM2012CF-800T06_2P

CRT_R_2 CRT_G_2 CRT_B_2

R523 150_0402_1% R515 150_0402_1% R508 150_0402_1%

C414 @ 10P_0402_50V8J C406 @ 10P_0402_50V8J C403 @ 10P_0402_50V8J

C415 22P_0402_50V8J C411 22P_0402_50V8J C405 22P_0402_50V8J

C412 10P_0402_50V8J C409 10P_0402_50V8J C401 10P_0402_50V8J

JCRT1 SUYIN_070546FR015S233ZR CONN@

CRT_DET# (18)

C16 100P_0402_50V8J C26 68P_0402_50V8J C11 68P_0402_50V8J

DSUB_12 DSUB_15

R29 100K_0402_5%

+CRT_VCC

C33 0.1U_0402_16V4Z R56 10K_0402_5%

U6 74AHCT1G125GW_SOT353-5

CRT_HSYNC CRT_HSYNC_1

L3 22_0402_5% L2 22_0402_5%

CRT_HSYNC_2 CRT_VSYNC_2

C21 10P_0402_50V8J C14 10P_0402_50V8J

C20 0.1U_0402_16V4Z

U4 74AHCT1G125GW_SOT353-5

CRT_VSYNC CRT_VSYNC_1

DISO@ C643 0.1U_0402_16V4Z
DISO@ C640 0.1U_0402_16V4Z
DISO@ C641 0.1U_0402_16V4Z
DISO@ C642 0.1U_0402_16V4Z

DISO@ U67 PI3V712-AZLEX_TQFN32_6X3~D

PCH DDC PU 2.2K
on Page 17

+3VS

C643 C640 C641 C642 0.1U_0402_16V4Z SG@

U67 SG@

+3VS

VDD VDD VDD VDD VDD

A0 A1 A2 A3 A4

CRT_R CRT_G CRT_B CRT_HSYNC CRT_VSYNC

add R1133,R1134,R1135,R1136 08/18

(23) VGA_CRT_R (23) VGA_CRT_G (23) VGA_CRT_B (23) VGA_CRT_HSYNC (23) VGA_CRT_VSYNC

0B1 1B1 2B1 3B1 4B1

A5 A6

DSUB_12_R DSUB_15_R

(23) VGA_DDC_DATA (23) VGA_DDC_CLK

5B1 6B1

SEL1 SEL2

DGPU_SELECT_R# DGPU_EDIDSEL_R_R#

R1133 SG@ 0_0402_5% DGPU_SELECT# (17,29)

R1135 DISO@ 0_0402_5%

R1134 SG@ 0_0402_5% DGPU_EDIDSEL_R# (29,31)

R1136 0_0402_5% DISO@

pull-up 2.2k on PCH side

pull-up 2k on GPU SIDE

(16) PCH_CRT_R (16) PCH_CRT_G (16) PCH_CRT_B (16) PCH_CRT_HSYNC (16) PCH_CRT_VSYNC

0B2 1B2 2B2 3B2 4B2

GND GND GND GND GPAD

(16) PCH_CRT_DATA (16) PCH_CRT_CLK

5B2 6B2

PI3V712-AZLEX_TQFN32_6X3~D

SEL1->Port 0~4 SEL2->Port5~6
(L--B1 Output H--B2 Output)

7/17 Del R895 R897 DIS only@
add R1131,R1132 DIS only 08/18
del R1131,R1132 08/19

Check bom

+3VS +CRT_VCC

R893 2.2K_0402_5% R894 2.2K_0402_5%

Q76A 2N7002DW-T/R7_SOT363-6

Q76B 2N7002DW-T/R7_SOT363-6

PCH_CRT_DATA R896 UMAO@ 0_0402_5% DSUB_12_R

PCH_CRT_CLK R898 UMAO@ 0_0402_5% DSUB_15_R

Reserved for UMA only

PCH_CRT_R R699 UMAO@ 0_0402_5% CRT_R
PCH_CRT_G R700 UMAO@ 0_0402_5% CRT_G
PCH_CRT_B R701 UMAO@ 0_0402_5% CRT_B
PCH_CRT_HSYNC R702 UMAO@ 0_0402_5% CRT_HSYNC
PCH_CRT_VSYNC R703 UMAO@ 0_0402_5% CRT_VSYNC

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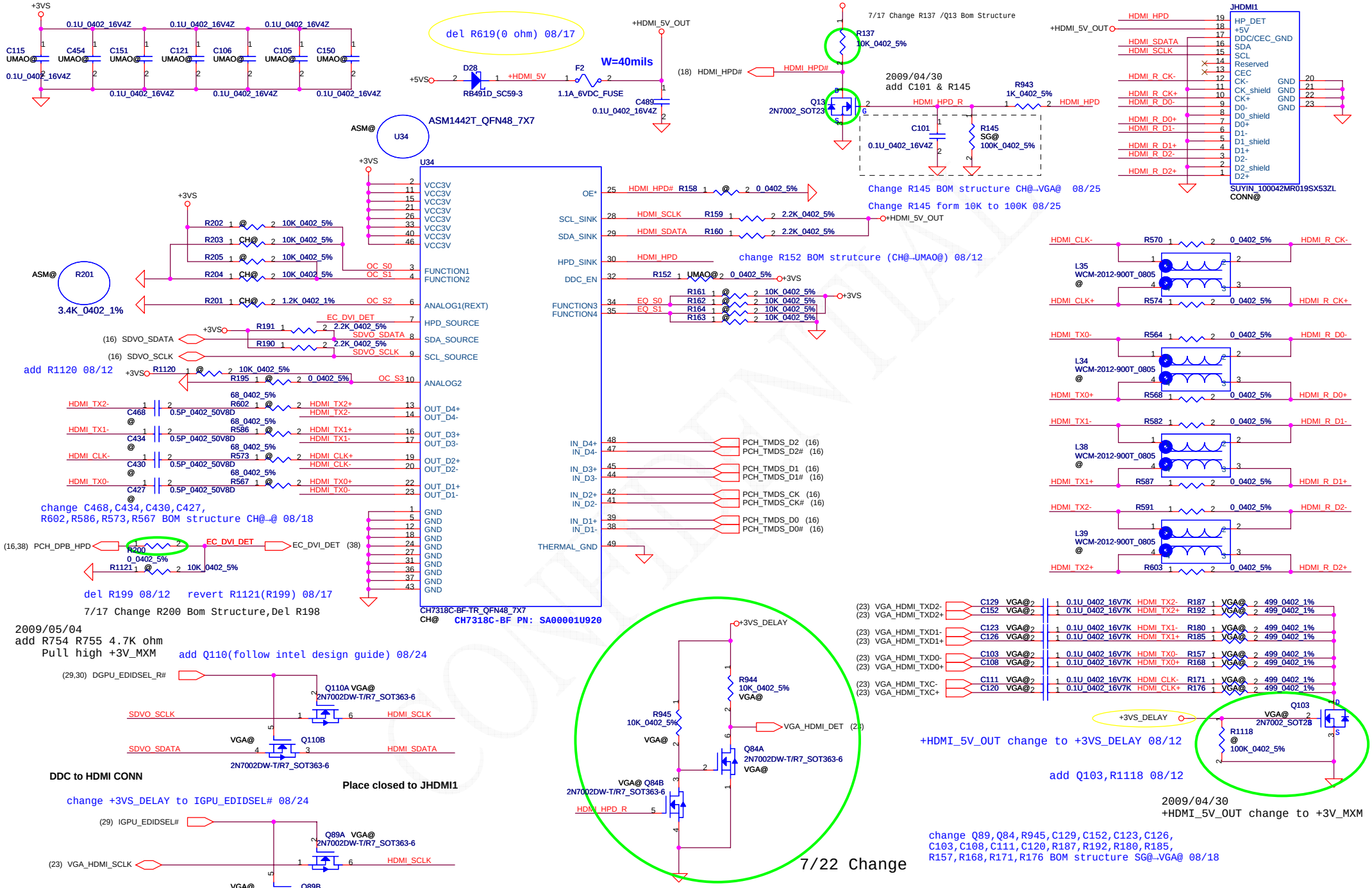

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PI2EQX323BLZHE change to SN75LVCP412R

+1.5vs change to +3vs 08/11

Adjust HDD1 PCH TX Swing

Add R953,R954,R955,R956 08/10

Placea caps. near ODD CONN.

SATA HDD1 Conn.

CL 8.6 mm

JHDD1

SUYIN_127043FR022G226ZL_NR

CONN@

10/7 Change HDD Part Number

SATA ODD Conn.

CL 6.0 mm

JODD1

OCTEK_0709015-SD001_RV

CONN@

SATA HDD2 Conn.

CL 4.0 mm

JHDD2

OCTEK_SAT-22SB1G_RV

CONN@

10/7 Change HDD Part Number

x_EQ	Compliance Channel @ 1.5 GHz
0	1.5dB ± 1.0dB
1	5.5dB ± 1.0dB

x_EM	Compliance Channel @ 1.5 GHz
0	0dB
1	-3.5dB

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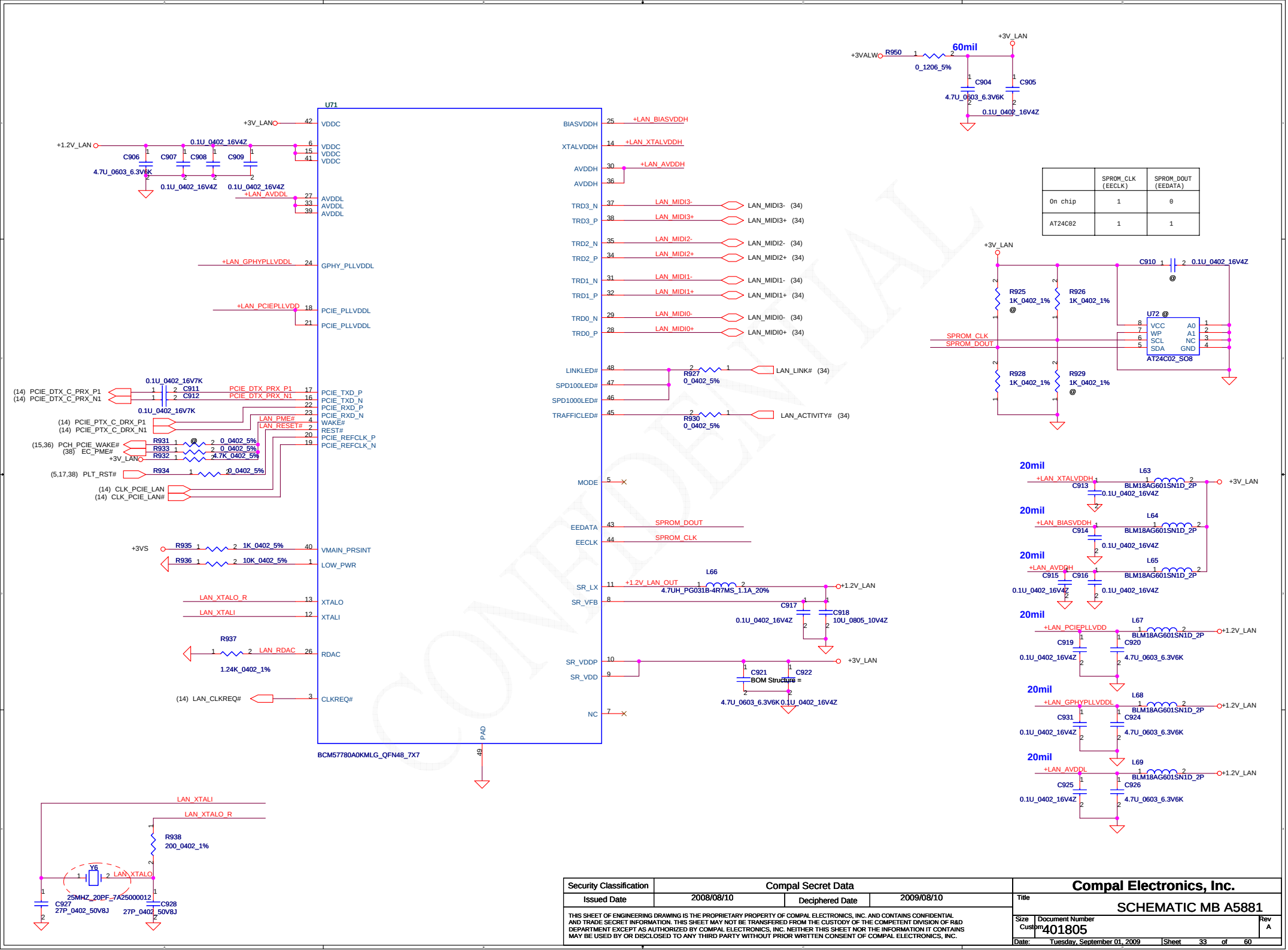

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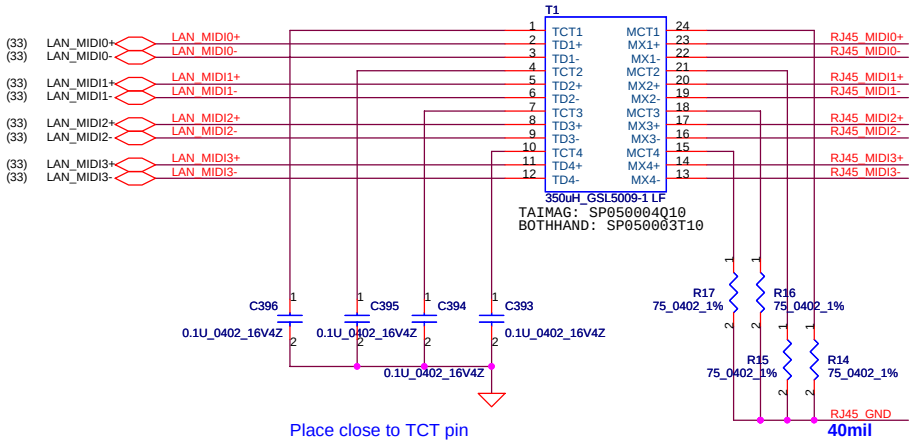

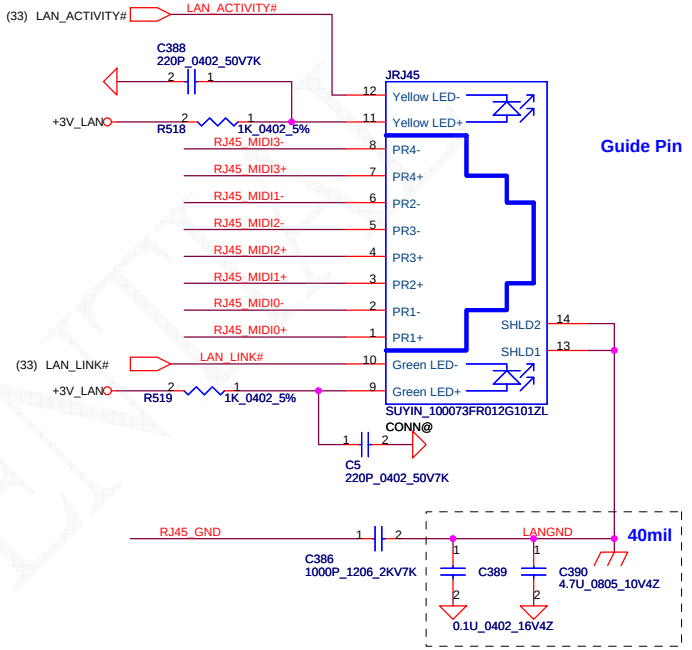

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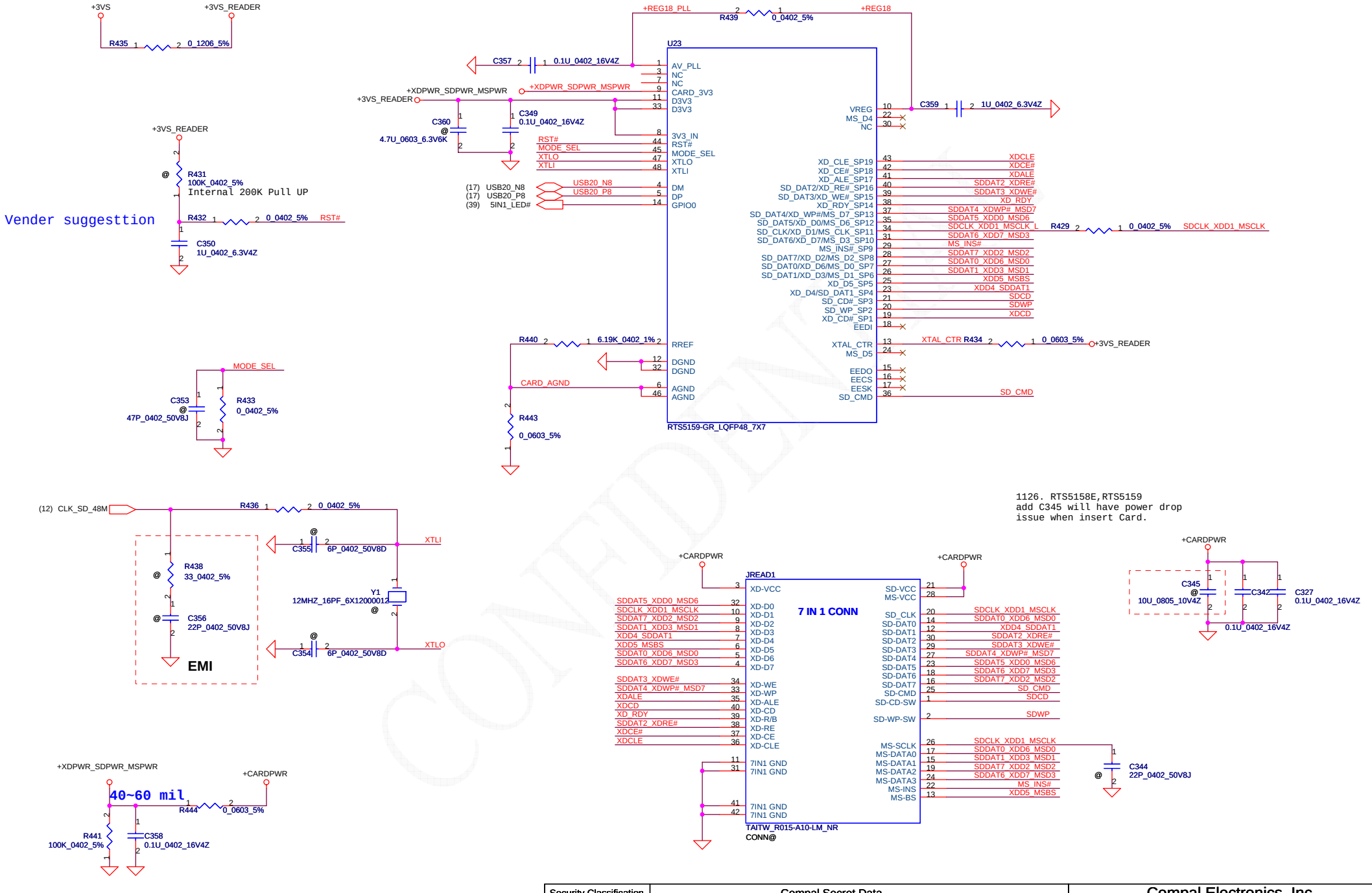

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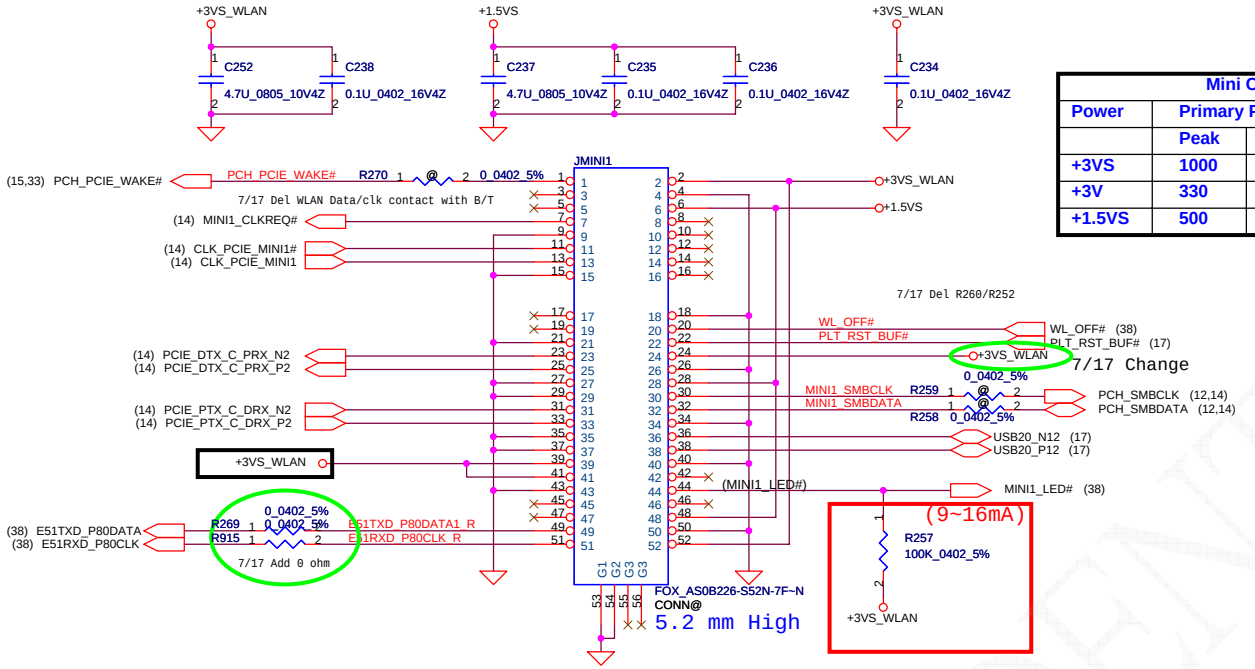
+3VS_WLAN R273 1 2 0_1206_5% +3VS

For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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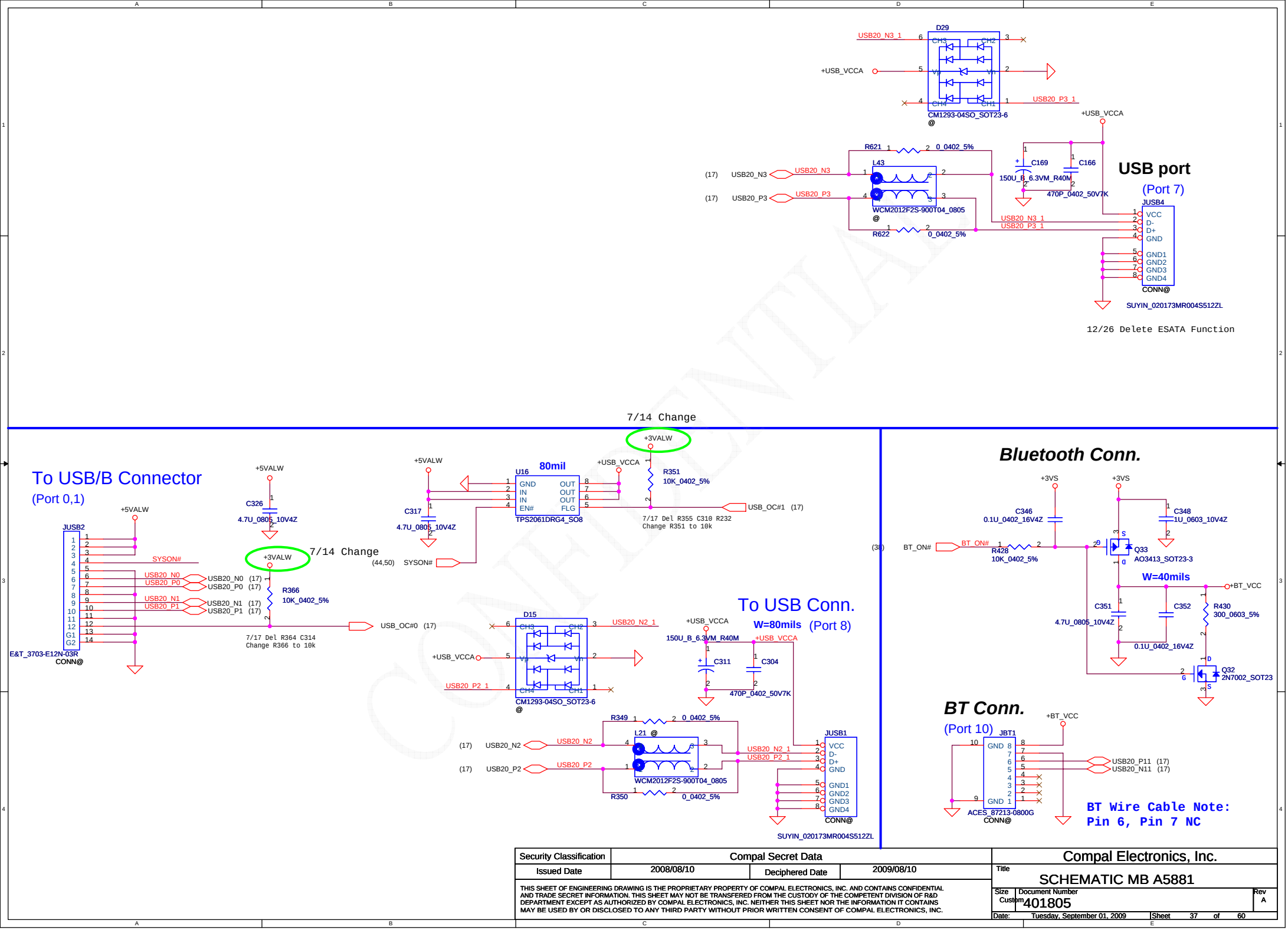

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For EC Tools

7/14 DEL PCH_SPKR (PCH to EC)

+3VALW

R399 0_0805_5%

0.1U_0402_16V4Z C309, C318, C323, C331, C334

+3VALW_EC

L22 FBMA-L11-160808-800LMT_0603

+EC_VCCA

C325 1000P_0402_50V7K

C316 0.1U_0402_16V4Z

ECAGND

KSI[0..7] KSI[0..7] (39)

KSO[0..17] KSO[0..17] (39)

Place on RAM door

JP11 ACES_85205-0400 @

E51RXD_P80CLK E51TXD_P80DATA

E51RXD_P80CLK (36) E51TXD_P80DATA (36)

Place on MiniCard

JP10 ACES_85205-0400 @

E51RXD_P80CLK E51TXD_P80DATA

(44,45) ACIN — R1159 0_0402_5% — ACIN_R (15,23)

EC_ACIN — R1158 0_0402_5% — ACIN_R

add R1158,R1159 08/21

U18

VCC VCC VCC VCC VCC VCC AVCC

將INVT_PWM跟EC_ACIN交換 08/11

C321 @22P_0402_50V8J

R388 @33_0402_5%

(17) CLK_PCI_LPC

+3VALW R354 47K_0402_5%

C308 0.1U_0402_16V4Z

(18) EC_GA20 — EC_GA20 — GA20/GPIO00

(18) EC_KBRST# — EC_KBRST# — KBRST#/GPIO01

(13) SERIRQ — SERIRQ — SERIRQ#

(13) LPC_FRAME# — LPC_FRAME# — LFRAME#

(13) LPC_AD3 — LPC_AD3 — LAD3

(13) LPC_AD2 — LPC_AD2 — LAD2

(13) LPC_AD1 — LPC_AD1 — LAD1

(13) LPC_AD0 — LPC_AD0 — LAD0

LPC & MISC

PCICLK

(5,17,33) PLT_RST# — EC_RST# — PCIRST#/GPIO05

ECRST#

(18) EC_SCI# — EC_SCI# — SCI#/GPIO0E

(15) PM_CLKRUN# — CLKRUN#/GPIO1D

INVT_PWM/PWM1/GPIO0F

BEEP#/PWM2/GPIO10

FANPWM1/GPIO12

ACOFF/FANPWM2/GPIO13

PWM Output

BATT_TEMP/AD0/GPIO38

BATT_OVP/AD1/GPIO39

ADP_I/AD2/GPIO3A

AD3/GPIO3B

AD4/GPIO42

SELIO2#/AD5/GPIO43

AD Input

DAC_BRIG/DA0/GPIO3C

EN_DFAN1/DA1/GPIO3D

IREF/DA2/GPIO3E

DA3/GPIO3F

DA Output

PSCLK1/GPIO4A

PSDAT1/GPIO4B

PSCLK2/GPIO4C

PSDAT2/GPIO4D

TP_CLK/PSCLK3/GPIO4E

TP_DATA/PSDAT3/GPIO4F

PS2 Interface

SDICS#/GPXOA00

SDICLK/GPXOA01

SDIDO/GPXOA02

SDIDI/GPXID0

SPI Device Interface

SPIDI/RD#

SPIDO/WR#

SPICLK/GPIO58

SPICS#

SPI Flash ROM

CIR_RX/GPIO40

CIR_RLC_TX/GPIO41

FSTCHG/SELIO#/GPIO50

BATT_CHGI_LED#/GPIO52

CAPS_LED#/GPIO53

BATT_LOW_LED#/GPIO54

SUSP_LED#/GPIO55

SYSON/GPIO56

VR_ON/XCLK32K/GPIO57

AC_IN/GPIO59

GPIO

EC_RSMRST#/GPXO03

EC_LID_OUT#/GPXO04

EC_ON/GPXO05

EC_SWI#/GPXO06

ICH_PWROK/GPXO06

BKOFF#/GPXO08

WL_OFF#/GPXO09

GPXO10

GPXO11

GPO

PM_SLP_S4#/GPXID1

ENBKL/GPXID2

GPXID3

GPXID4

GPXID5

GPXID6

GPXID7

GPI

V18R

C333 4.7U_0805_10V4Z

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17

KSI0/GPIO30 … KSO17/GPIO49

Int. K/B Matrix

(46) EC_SMB_CK1 — EC_SMB_CK1 — SCL1/GPIO44

(46) EC_SMB_DA1 — EC_SMB_DA1 — SDA1/GPIO45

(14,23) EC_SMB_CK2 — EC_SMB_CK2 — SCL2/GPIO46

(14,23) EC_SMB_DA2 — EC_SMB_DA2 — SDA2/GPIO47

SM Bus

(15) PM_SLP_S3# — PM_SLP_S3# — PM_SLP_S3#/GPIO04

(15) PM_SLP_S5# — PM_SLP_S5# — PM_SLP_S5#/GPIO07

(18) EC_SMI# — EC_SMI# — EC_SMI#/GPIO08

(39) EC_I2C_INT2 — EC_I2C_INT2 — LID_SW#/GPIO0A

(39) EC_ESB_CK — EC_ESB_CK — SUSP#/GPIO0B

(39) EC_ESB_DA — EC_ESB_DA — PBTN_OUT#/GPIO0C

(13) MF_EN — MF_EN — EC_PME#/GPIO0D

(29) INVT_PWM — INVT_PWM — EC_THERM#/GPIO11

(43) FAN_SPEED1 — FAN_SPEED1 — FAN_SPEED1/FANFB1/GPIO14

(37) BT_ON# — BT_ON# — FANFB2/GPIO15

E51TXD_P80DATA — EC_TX/GPIO16

E51RXD_P80CLK — EC_RX/GPIO17

(40) ON/OFF — ON/OFF — ON_OFF/GPIO18

(39) PWR_SUSP_LED — PWR_SUSP_LED — PWR_LED#/GPIO19

(39) NUM_LED# — NUM_LED# — NUMLED#/GPIO1A

EC_CRY1 — XCLK1

EC_CRY2 — XCLK0

GND GND GND GND GND AGND

KB926QFD3_LQFP128_14X14

20mil

<BOM Structure>

L23 0_0603_5%

L23 change to 0 ohm 08/12

EC_ACIN — EC_ACIN

BEEP# — BEEP# (41)

ACOFF — ACOFF (47,55)

C307 0.01U_0402_16V7K

BATT_TEMP — BATT_TEMP (46)

BATT_OVP — BATT_OVP (47)

ADP_I — ADP_I (47)

AD_BID0

GFX_CORE_PWRGD change to ME_EN 08/10

MEDIA_LED#_IN (39)

change ME_EN for U18.75 to U18.19 08/20

DAC_BRIG — DAC_BRIG (29)

EN_DFAN1 — EN_DFAN1 (43)

IREF — IREF (47)

CALIBRATE# — CALIBRATE# (47)

EC_MUTE# — EC_MUTE# (41,42)

MINI1_LED# — MINI1_LED# (36)

MEDIA_LED_OUT (39)

change MEDIA_LED#_OUT to MEDIA_LED_OUT 08/10

BT_LED# — BT_LED# (39)

TP_CLK — TP_CLK (39)

TP_DATA — TP_DATA (39)

3S/4S# — 3S/4S# (47)

65W/90W# — 65W/90W# (47)

LID_SW# — LID_SW# (39)

EC_SI_SPI_SO — EC_SO_SPI_SI (39)

EC_SO_SPI_SI — EC_SI_SPI_SO (39)

EC_SPICLK — EC_SPICLK (39)

EC_SPICS#/FSEL# — EC_SPICS#/FSEL# (39)

EC_RCIRRX

PCH_TEMP_ALERT# — PCH_TEMP_ALERT# (18)

FSTCHG — FSTCHG (47)

BATT_GRN_LED# — BATT_GRN_LED# (39)

CAPS_LED# — CAPS_LED# (39)

BATT_AMB_LED# — BATT_AMB_LED# (39)

PWR_LED — PWR_LED (39)

SYSON — SYSON (44,49)

VR_ON — VR_ON (54)

ACIN — change ACIN net name to ACIN_R 08/21

EC_RSMRST# — EC_RSMRST# (15)

EC_LID_OUT# — EC_LID_OUT# (14)

EC_ON — EC_ON (40)

EC_SWI# — EC_SWI# (15)

EC_PWROK — EC_PWROK (15)

BKOFF# — BKOFF# (29)

WL_OFF# — WL_OFF# (36)

EC_DVI_DET_IN

EC_DVI_DET_OUT

PM_SLP_S4# — PM_SLP_S4# (15)

ENBKL — ENBKL (16)

EAPD — EAPD (41)

SUS_PWR_ACK — SUS_PWR_ACK (15)

SUSP# — SUSP# (40,44,47,50)

PBTN_OUT# — PBTN_OUT# (5,15)

EC_PME# — EC_PME# (33)

Ra R358 100K_0402_5%

Rb R359 8.2K_0402_5%

C313 0.1U_0402_16V4Z

TP_CLK 4.7K_0402_5% R392

TP_DATA 4.7K_0402_5% R393

10/1 EC Recommand

3S/4S# R402 100K_0402_5%

65W/90W# R403 100K_0402_5%

R368 10K_0402_5%

del D17 08/21

Analog Board ID definition, Please see page 3.

EC_CRY1 EC_CRY2

C340 15P_0402_50V8J

C339 15P_0402_50V8J

X1 32.768KHZ_12.5P_MC-306

C306 100P_0402_50V8J

C305 100P_0402_50V8J

C332 100P_0402_50V8J

BATT_TEMP

BATT_OVP

ACIN

change ACIN net name to ACIN_R 08/21

+3VALW

R405 100K_0402_5%

R371 2.2K_0402_5%

R377 2.2K_0402_5%

R353 47K_0402_5%

R352 47K_0402_5%

10/1 ENE Recommand

R406 @ 10K_0402_5%

7/14 Pin 19/99 DEL

del R385 R378(0 ohm) 08/10

change R376.R391 BOM structure 0812

+3VS

R376 @ EC_SMB_CK2 4.7K_0402_5%

R391 @ EC_SMB_DA2 4.7K_0402_5%

del C1(15P) 08/10

R389 EC_ESB_CK 4.7K_0402_5%

chane net name 08/17

R372 EC_ESB_DA 4.7K_0402_5%

R369 @ PCH_TEMP_ALERT# 2.2K_0402_5%

R384 EC_I2C_INT2 2.2K_0402_5%

del R375(GFX_CORE_PWRGD pull up resistance) 08/12

R370 @ 10K_0402_5% MEDIA_LED# IN

del R404,R412 08/12

(31) EC_DVI_DET — R411 @ 0_0402_5% — EC_DVI_DET_IN

(16,31) PCH_DPB_HPD — R413 @ 0_0402_5% — EC_DVI_DET_OUT

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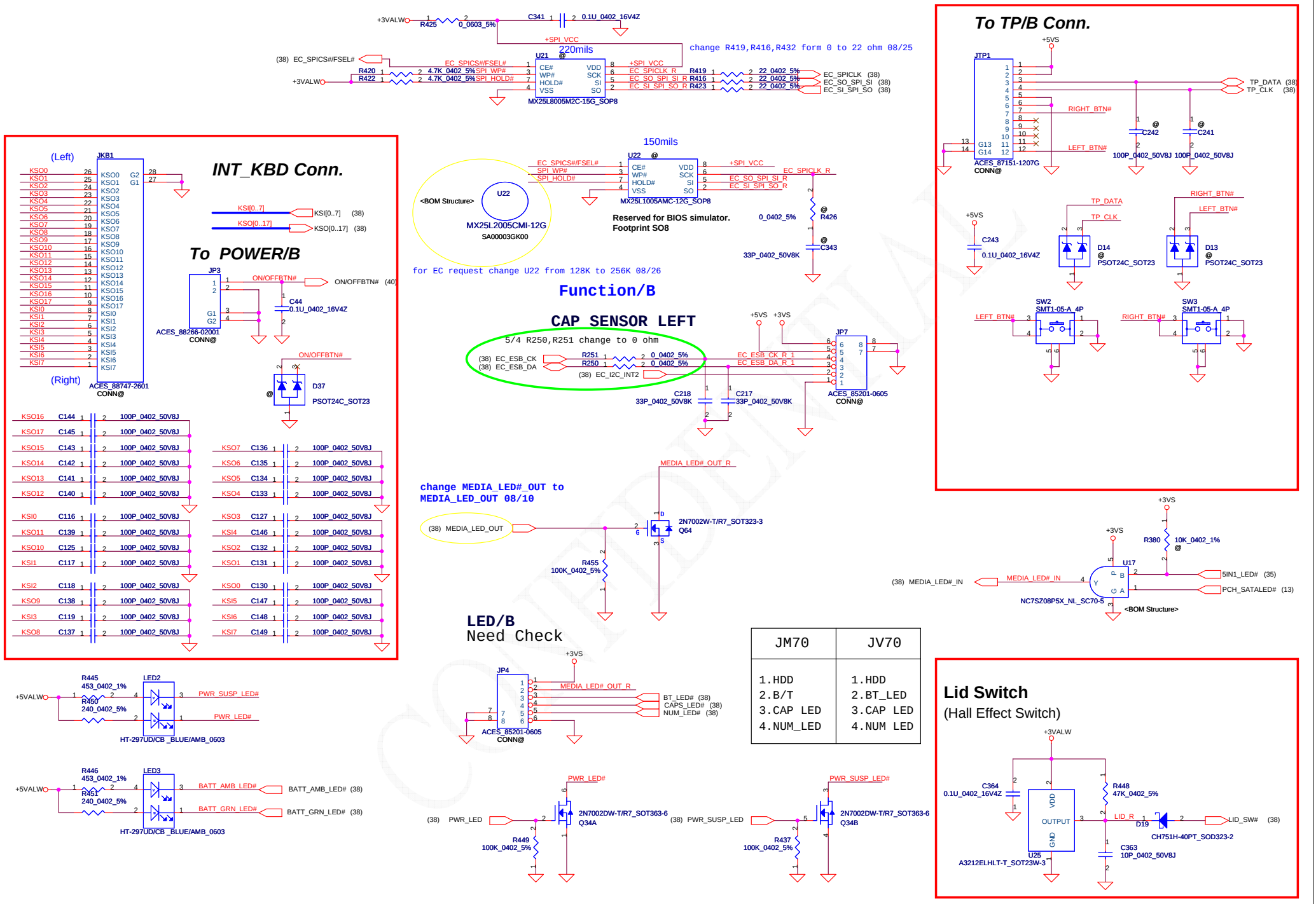

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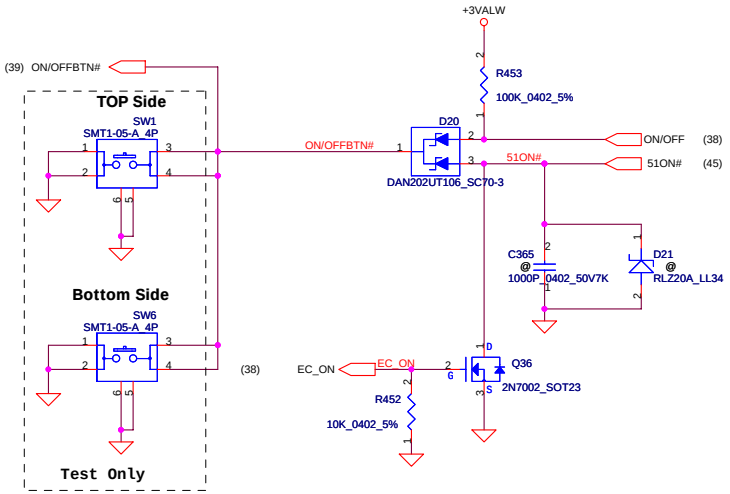
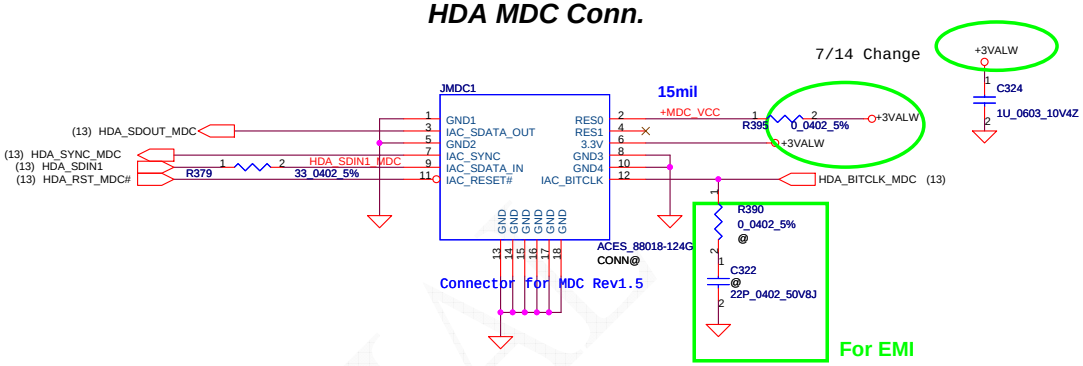
Power Button

ON/OFF switch



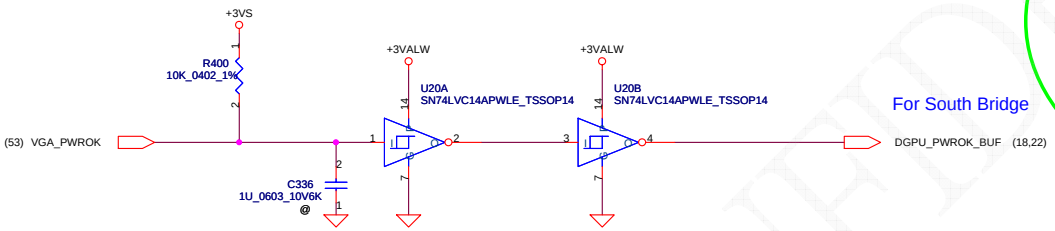
HDA MDC Conn.

7/14 Change

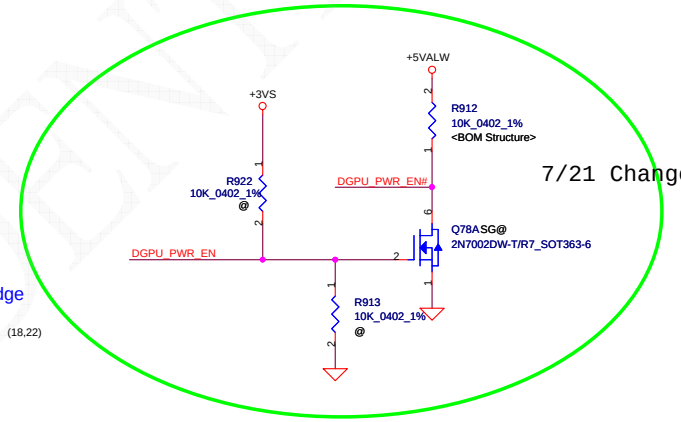


change R390,C322 BOM structure POP→@ 08/25

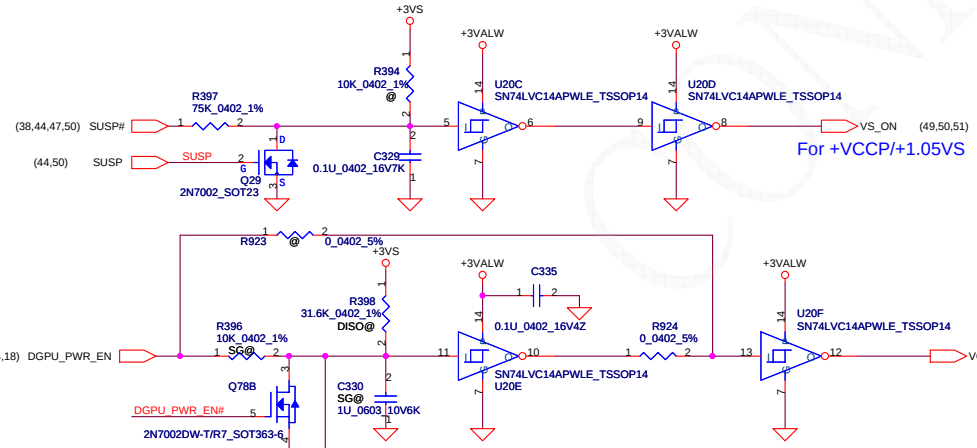
Power ON Circuit



For South Bridge

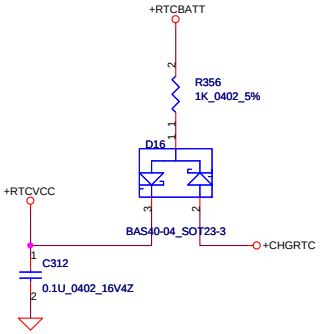


7/21 Change



For +VCCP/+1.05VS

del R442,C362,C361,IR1(CIR) 08/21



add Q104 and change R398 bom structure (@→DISO@) 08/18

7/21 DG Define DGPU_PWR_EN#

2009/6/19
add Q28,C330 fix ATI MXM S3 resume thermal IC can't read VGA temp

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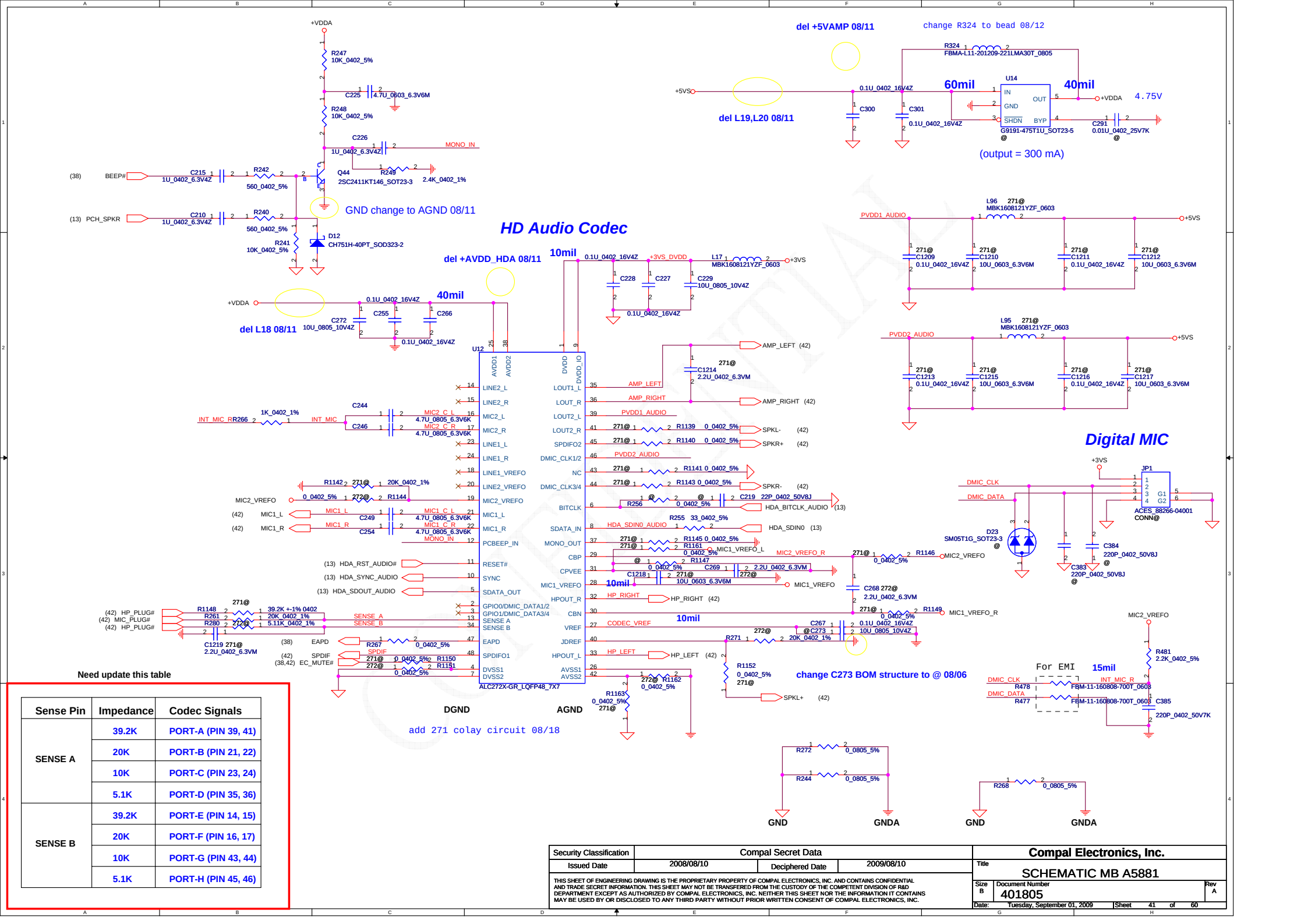

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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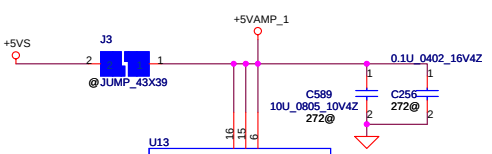
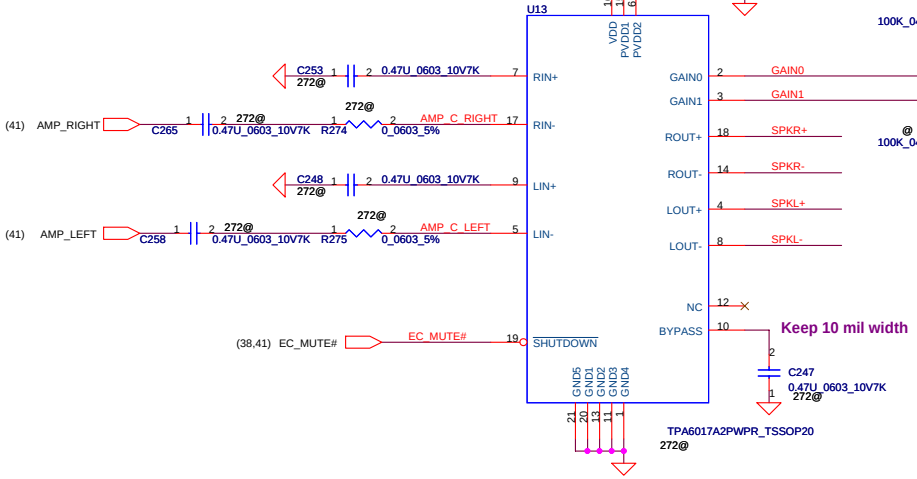
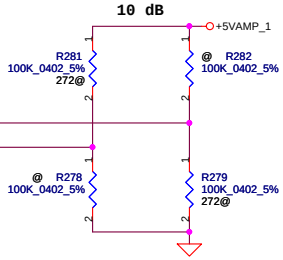
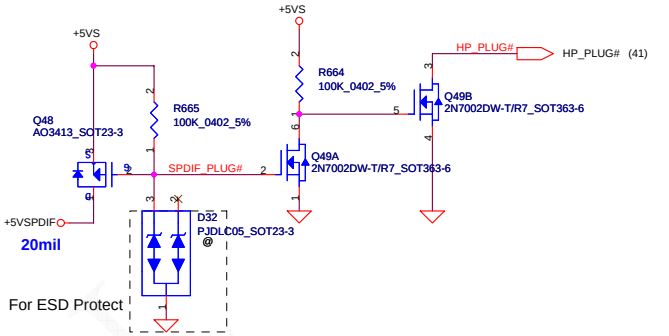
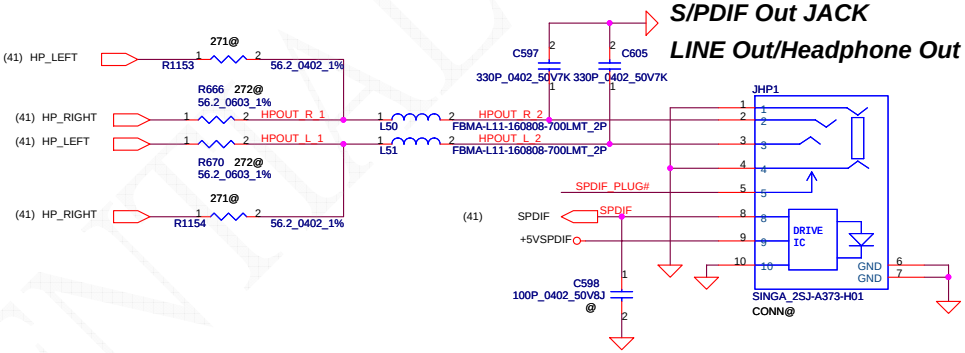
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



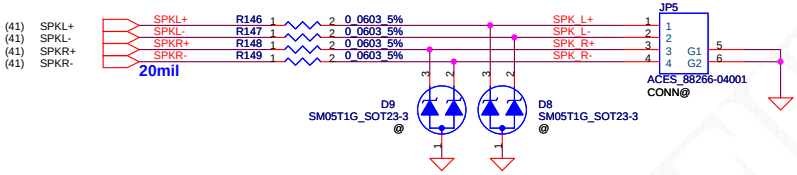


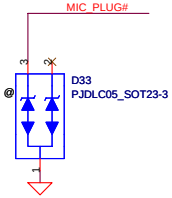


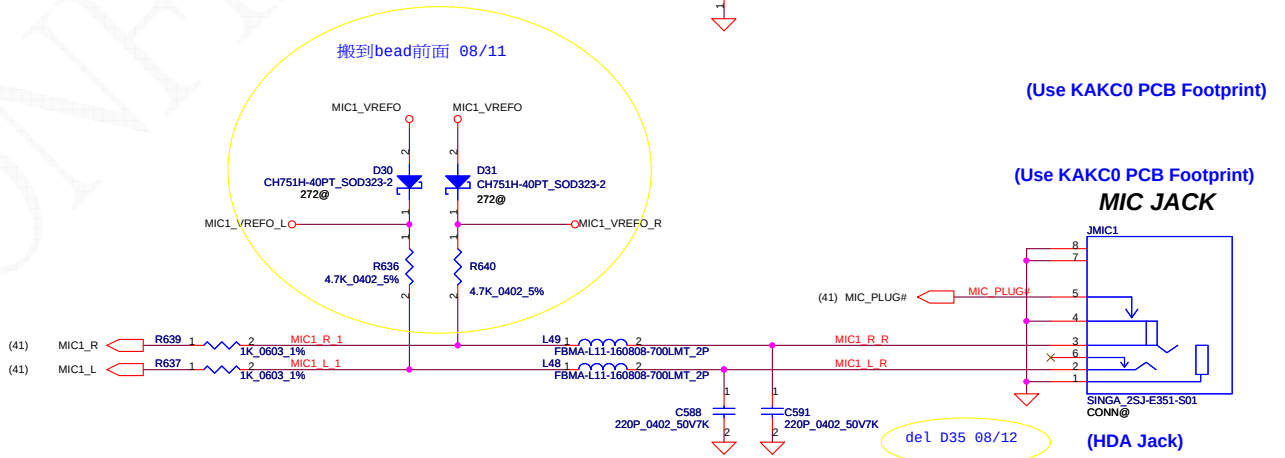




Int. Speaker Conn.







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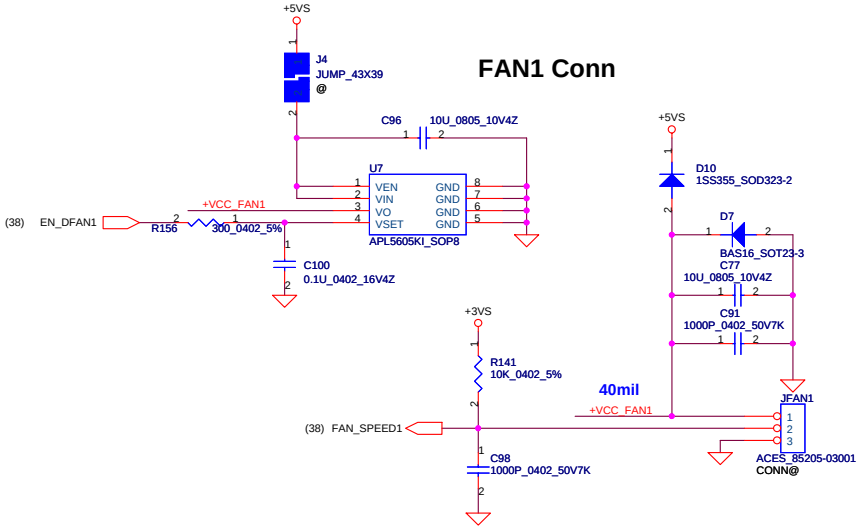
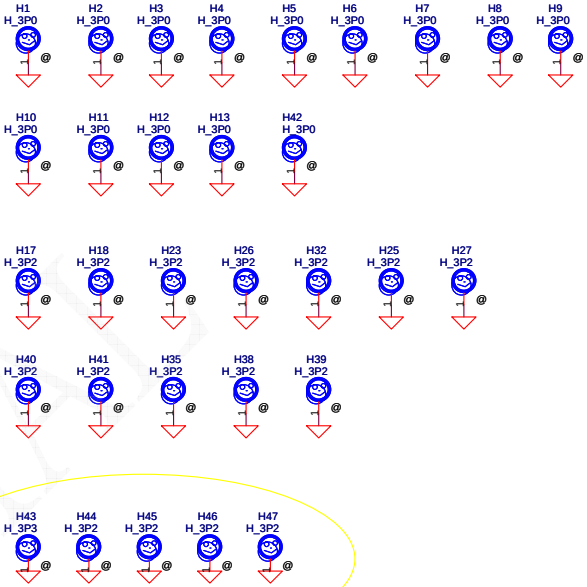
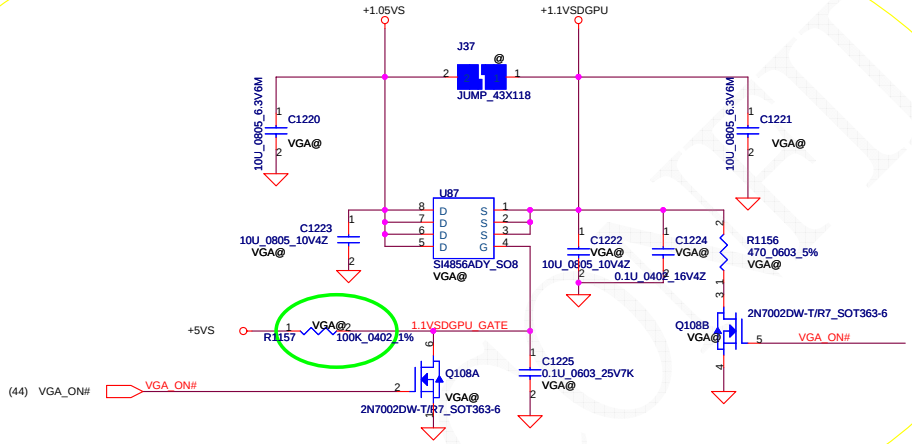


7/20 Del

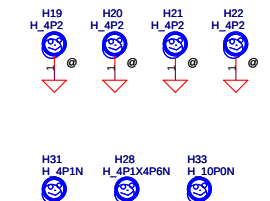


add screw 08/19

+1.05VS to +1.1VSDGPU Transfer



add +1.05VS to +1.1VSDGPU Transfer 08/20



change BOM structure @→VGA@ 08/25

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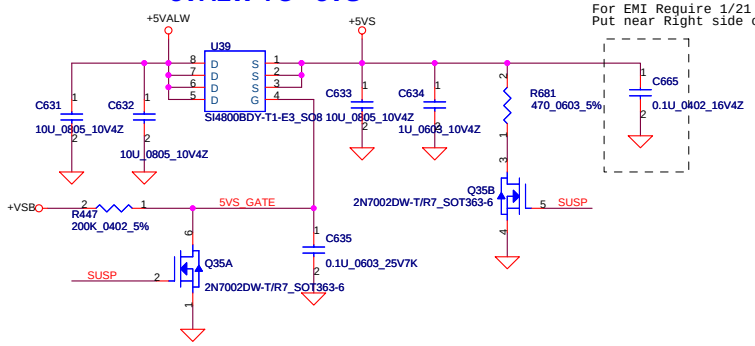
+5VALW TO +5VS

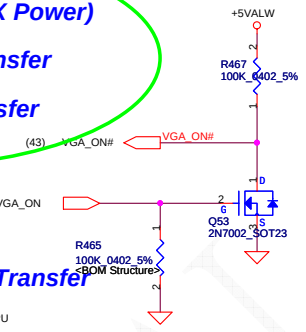


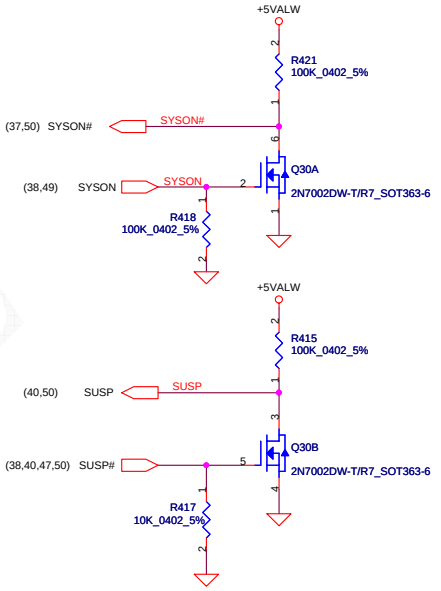
For EMI Require 1/21
Put near Right side of DIMM

+3VALW TO +3VMXM Transfer

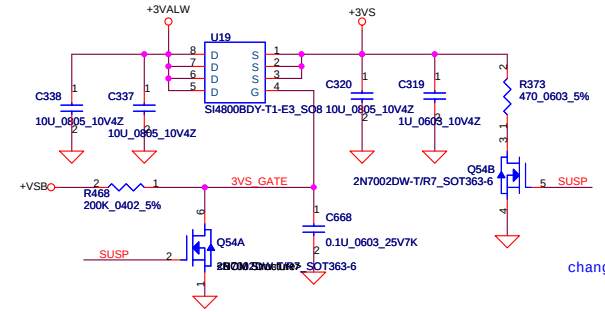
+5VALW to +5VMXM Transfer

7/14 Change

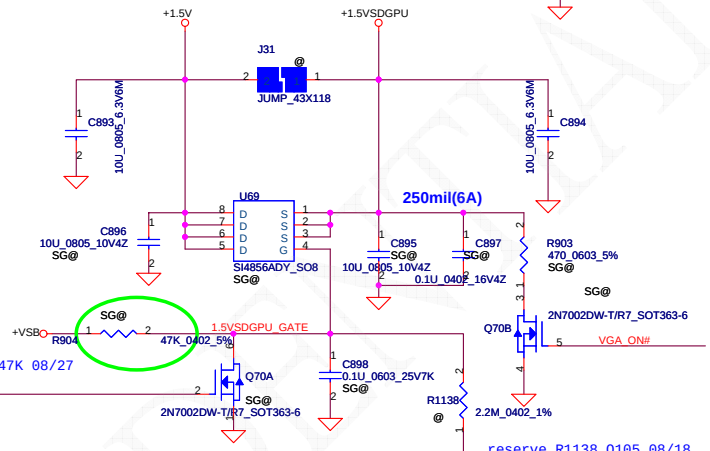




+3VALW TO +3VS



+1.5V to +1.5VSDGPU Transfer



change R904 from 100K to 47K 08/27

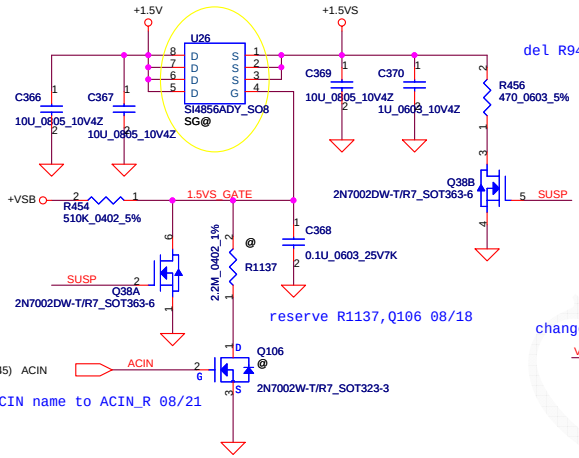
reserve R1138,Q105 08/18

For Calpella CPU S3 DRAM Power

(1.5V_CPU VDDQ)

+1.5V to +1.5VS

U26 change to SI4856(Vgs=20) 08/18

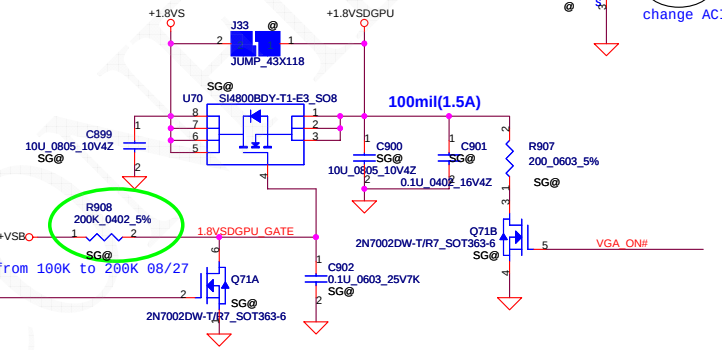


del R947 08/18

reserve R1137,Q106 08/18

change ACIN name to ACIN_R 08/21

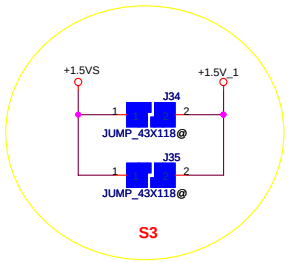
+1.8VS to +1.8VSDGPU Transfer



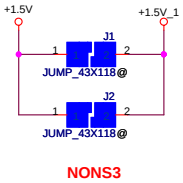
change R904 from 100K to 200K 08/27

change ACIN name to ACIN_R 08/21

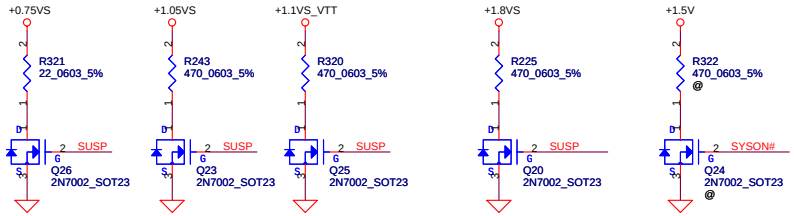
add J34,J35 08/17

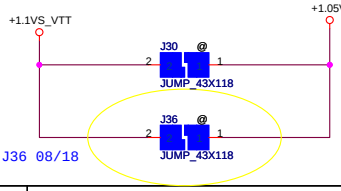


S3



NONS3





add J36 08/18

del U74 C929,C930,R948,R949,Q90,Q91
(+1.5V to +1.5V_1 circuit) 08/17

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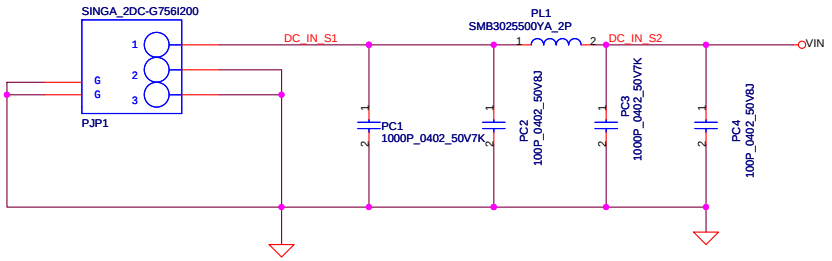
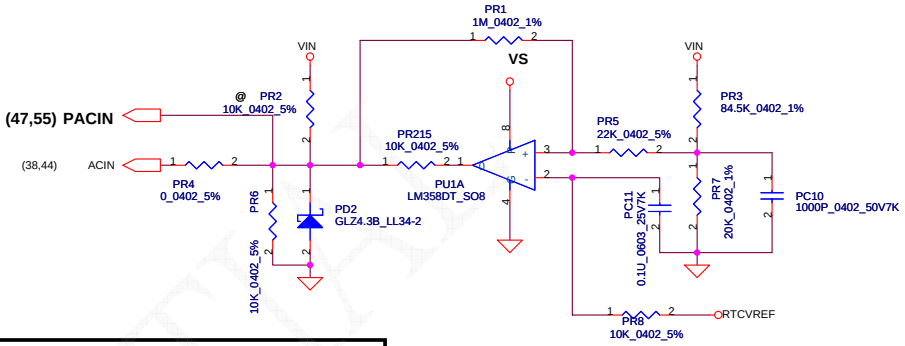
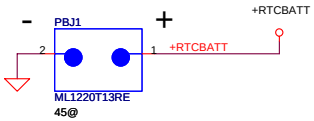
DC231000500

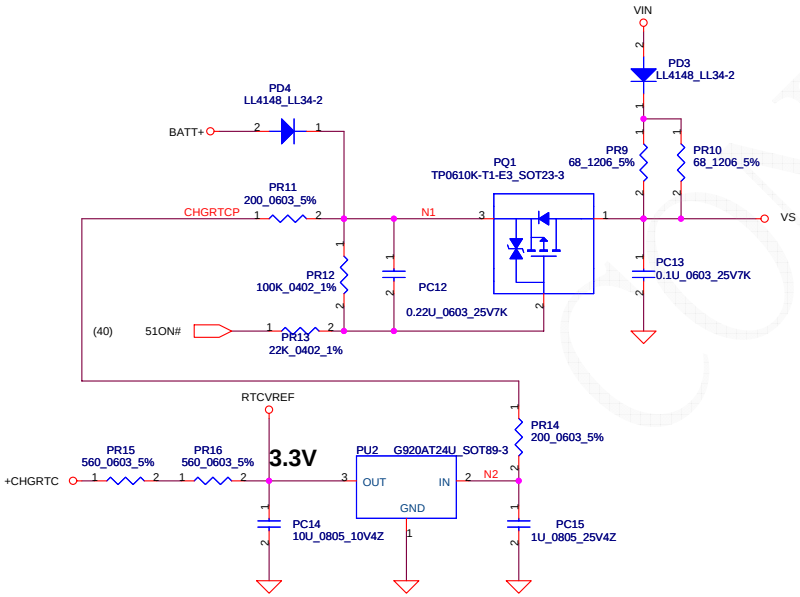


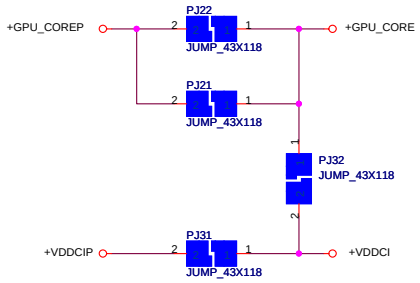


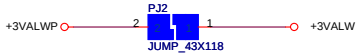
Vin Detector

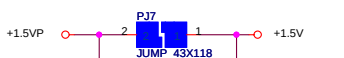
	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V

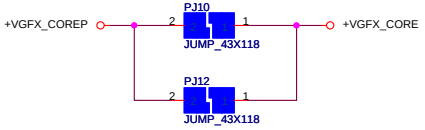


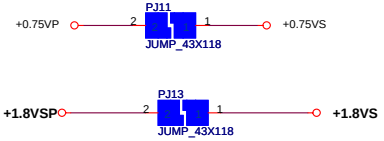












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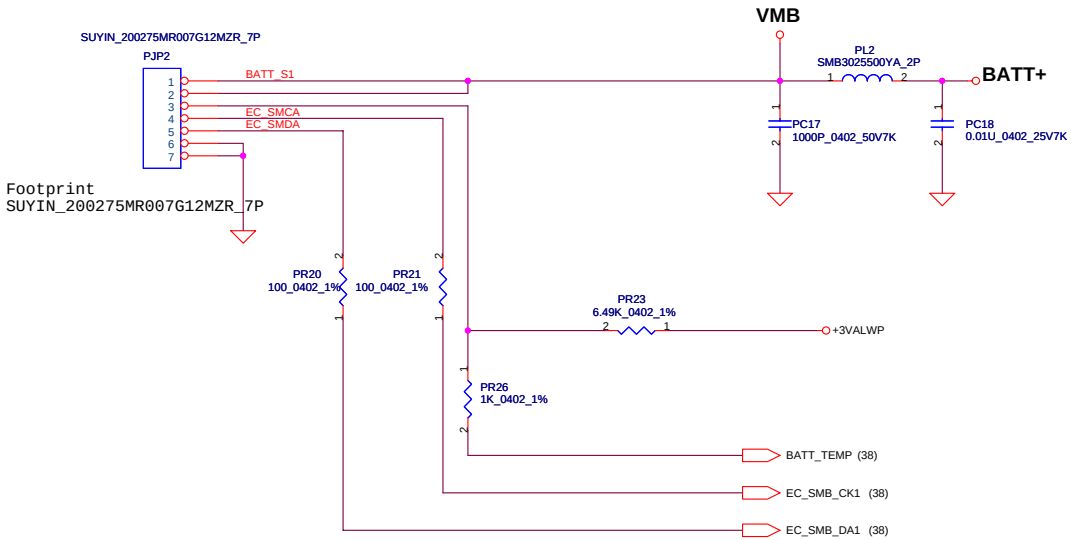
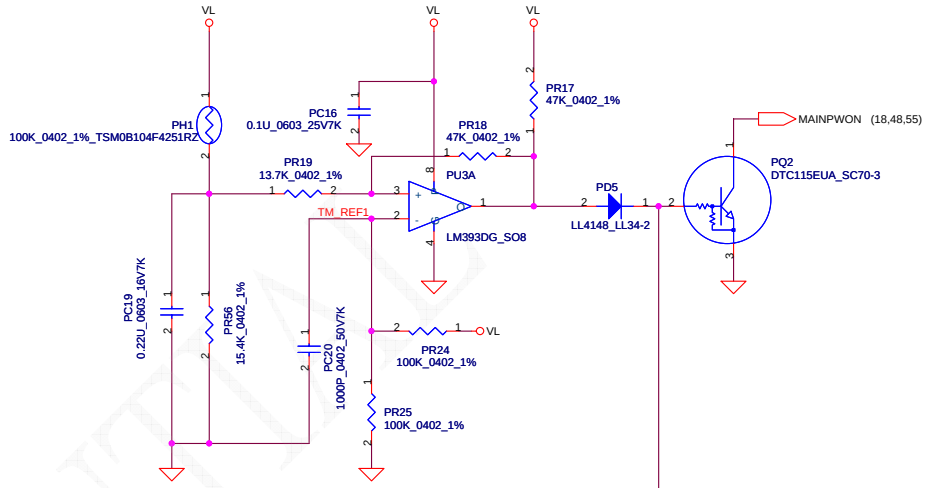
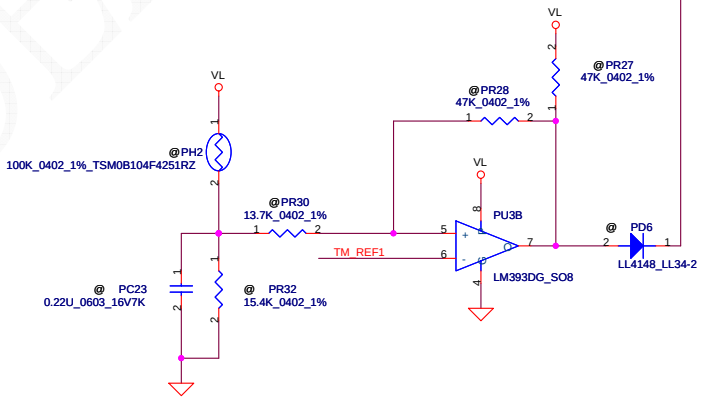
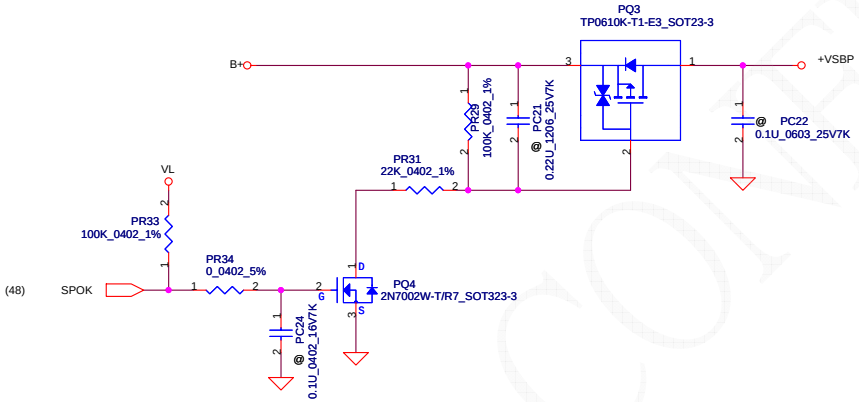
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





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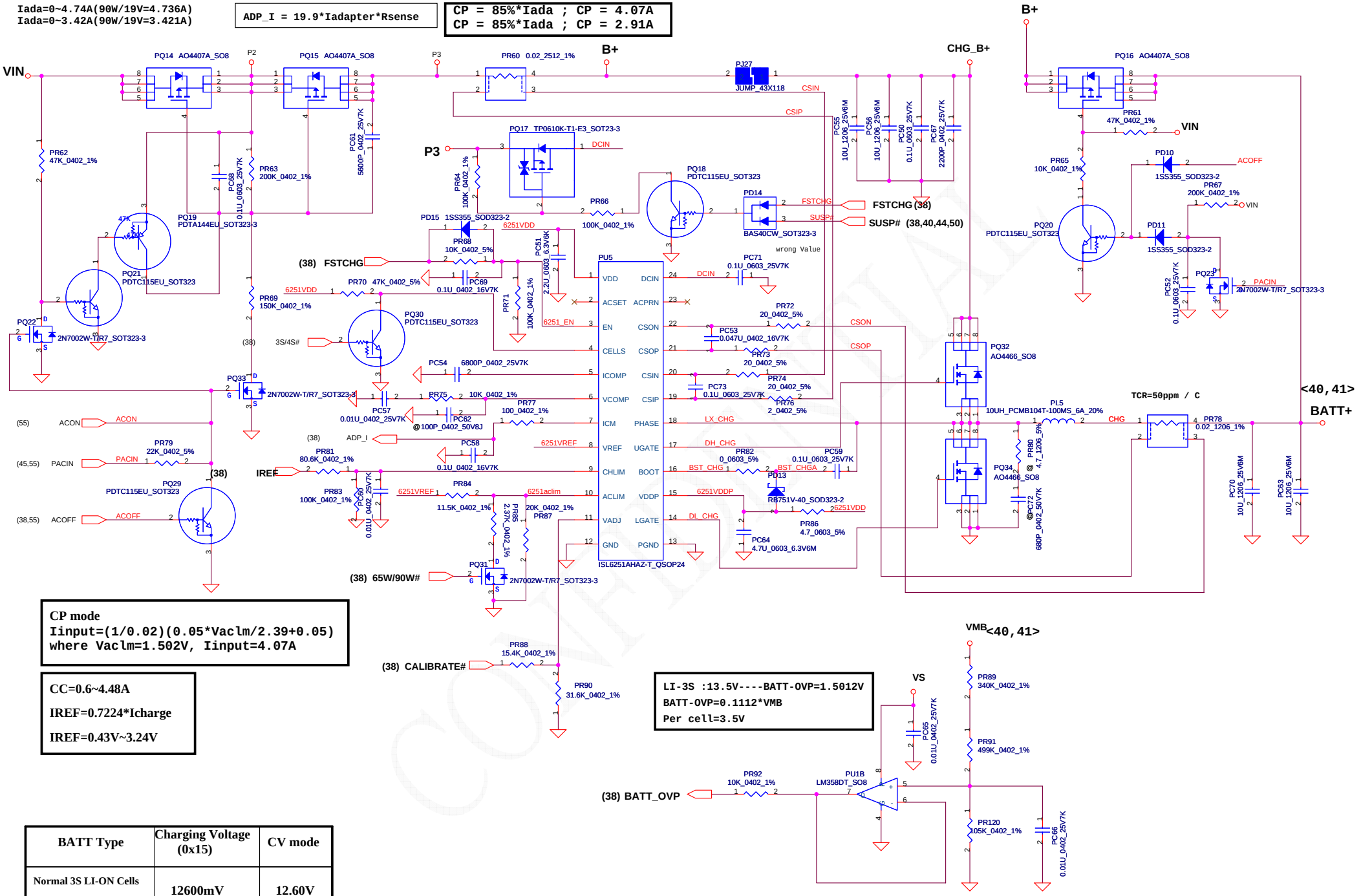
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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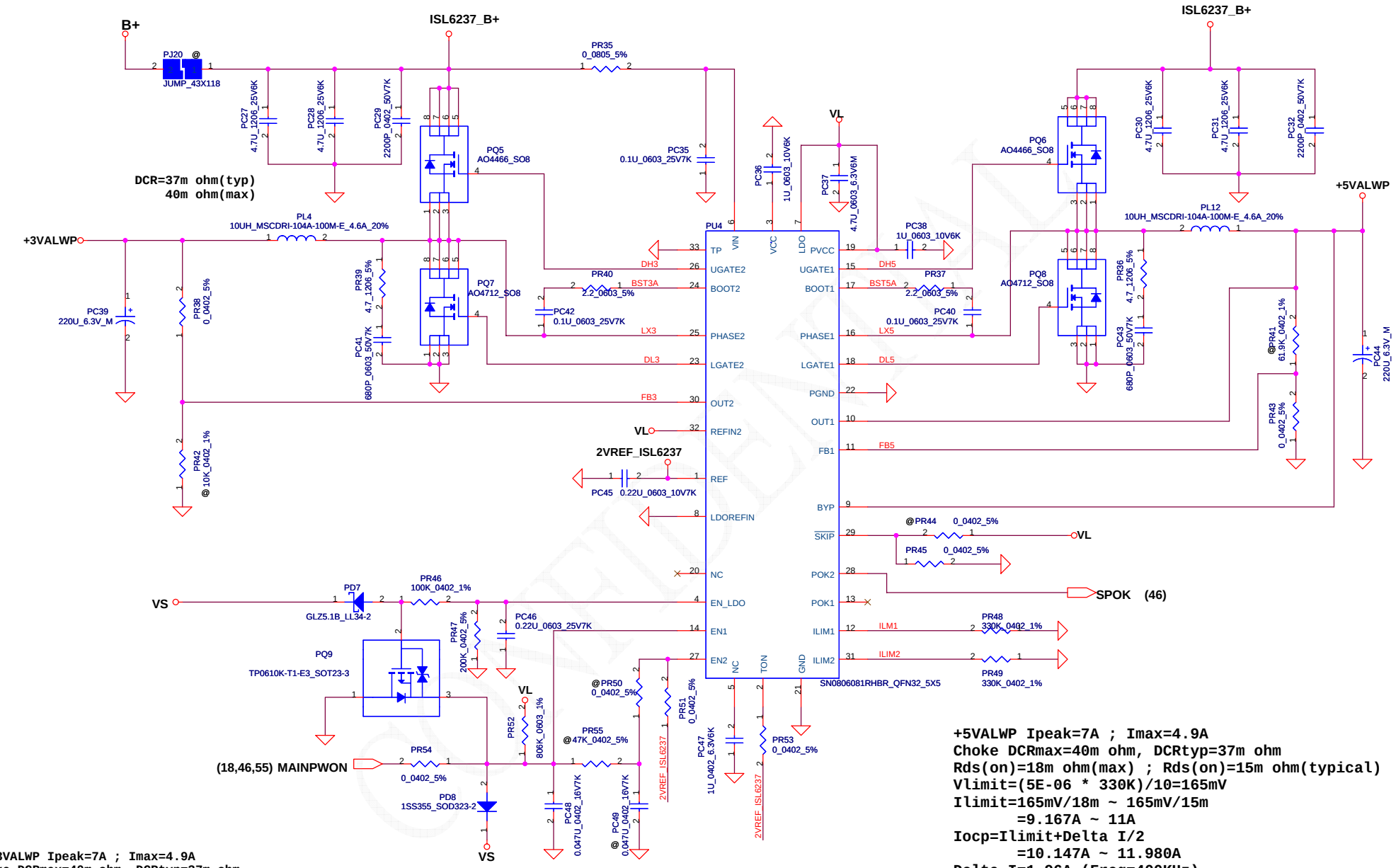

+3.3VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=7A ; Imax=4.9A
Choke DCRmax=40m ohm, DCRtyp=37m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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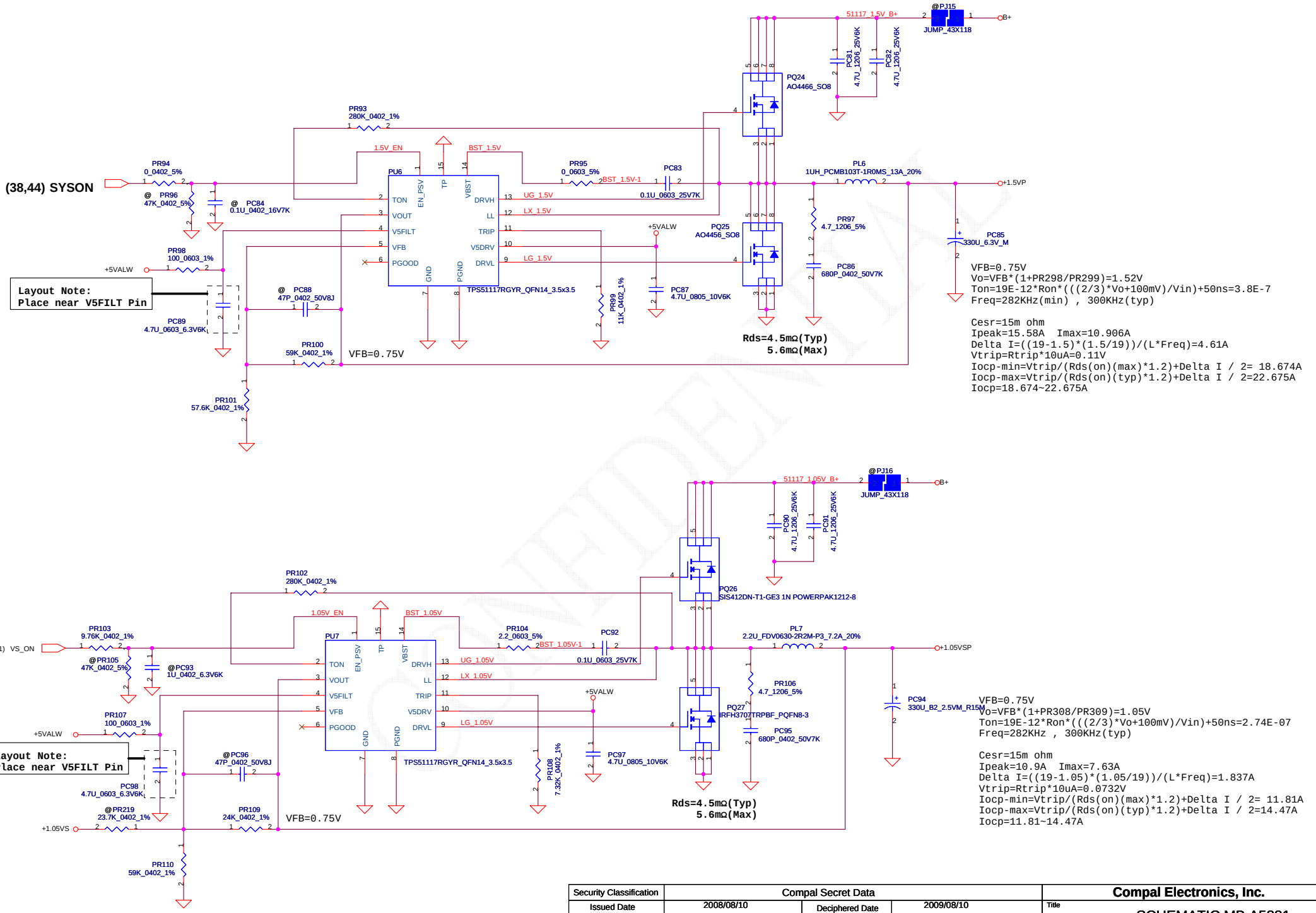

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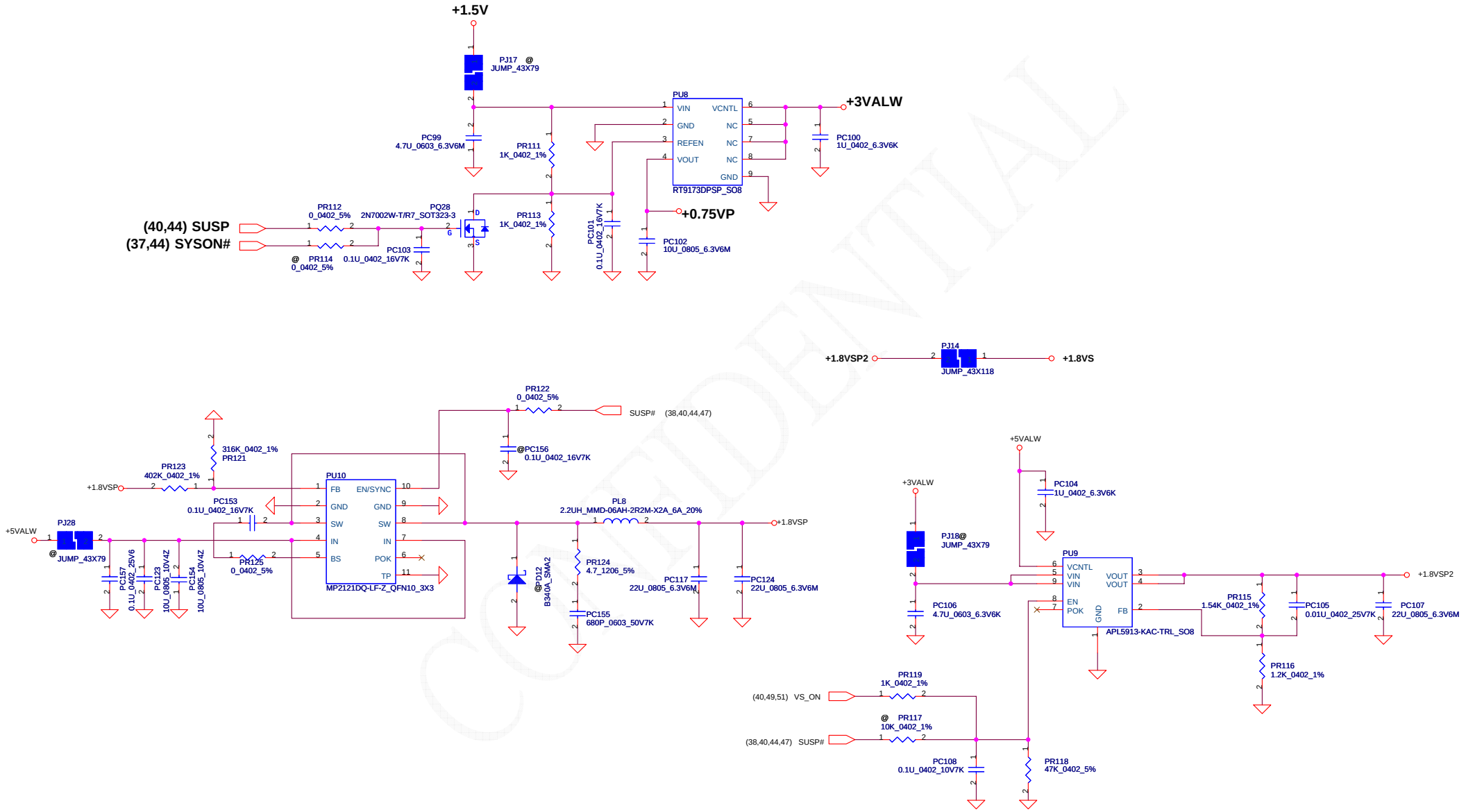

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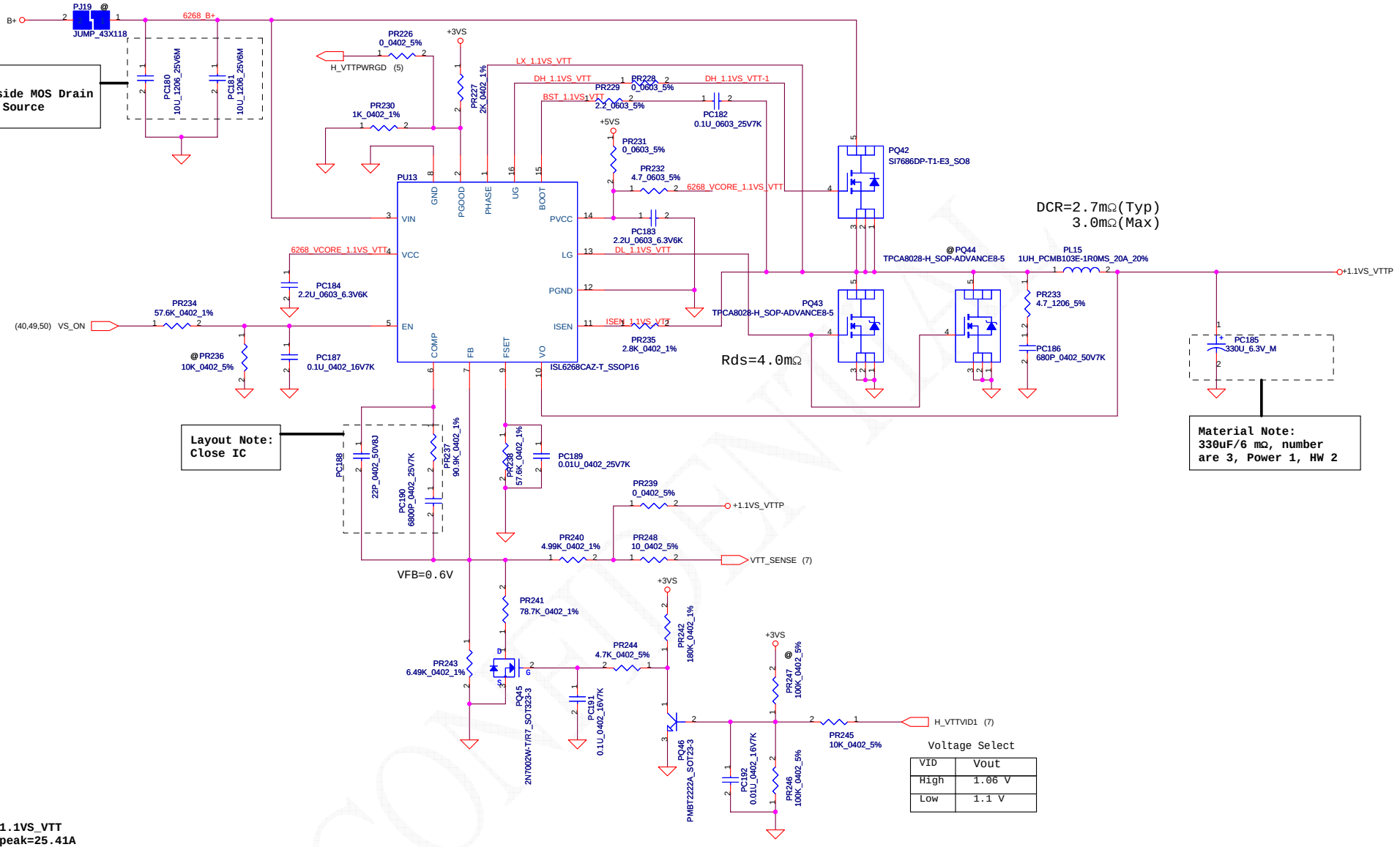

+1.1VS_VTT
Ipeak=25.41A
Imax=17.79A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 27.586A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.787K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=38.372A
Iocp=27.586~38.272A

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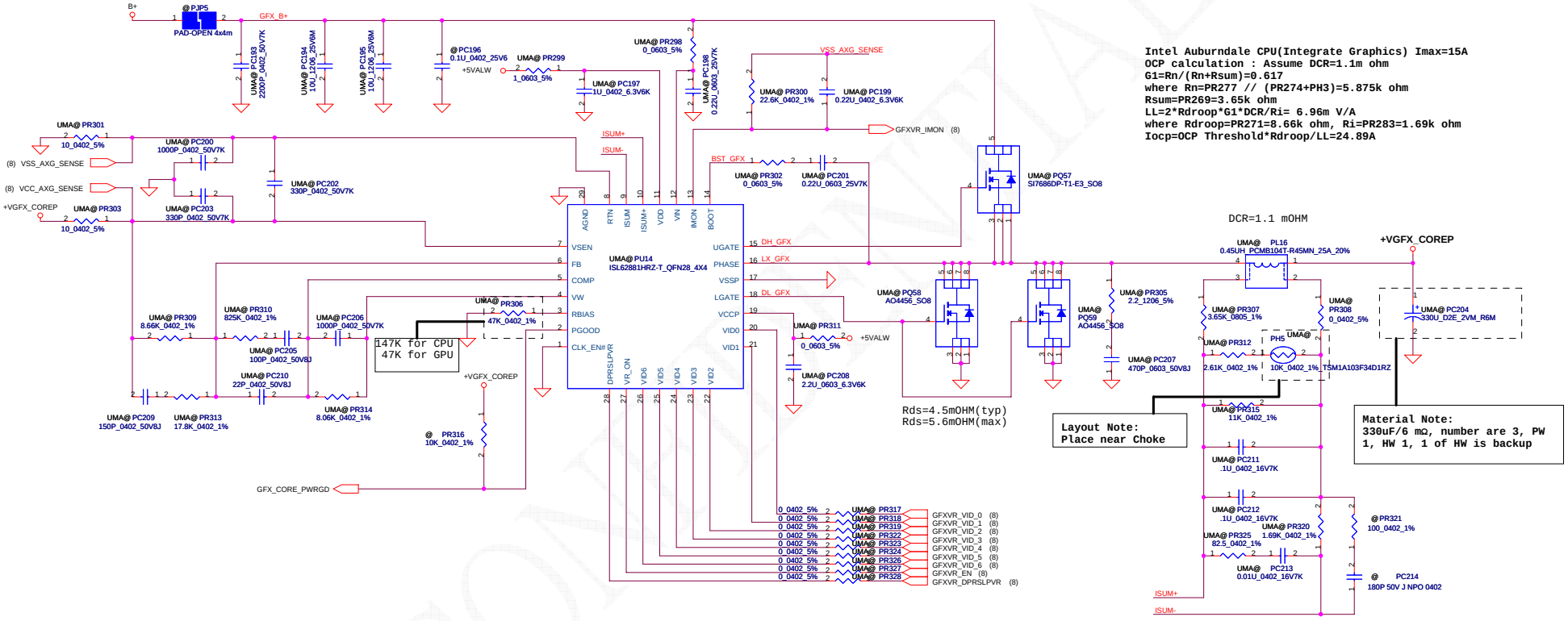

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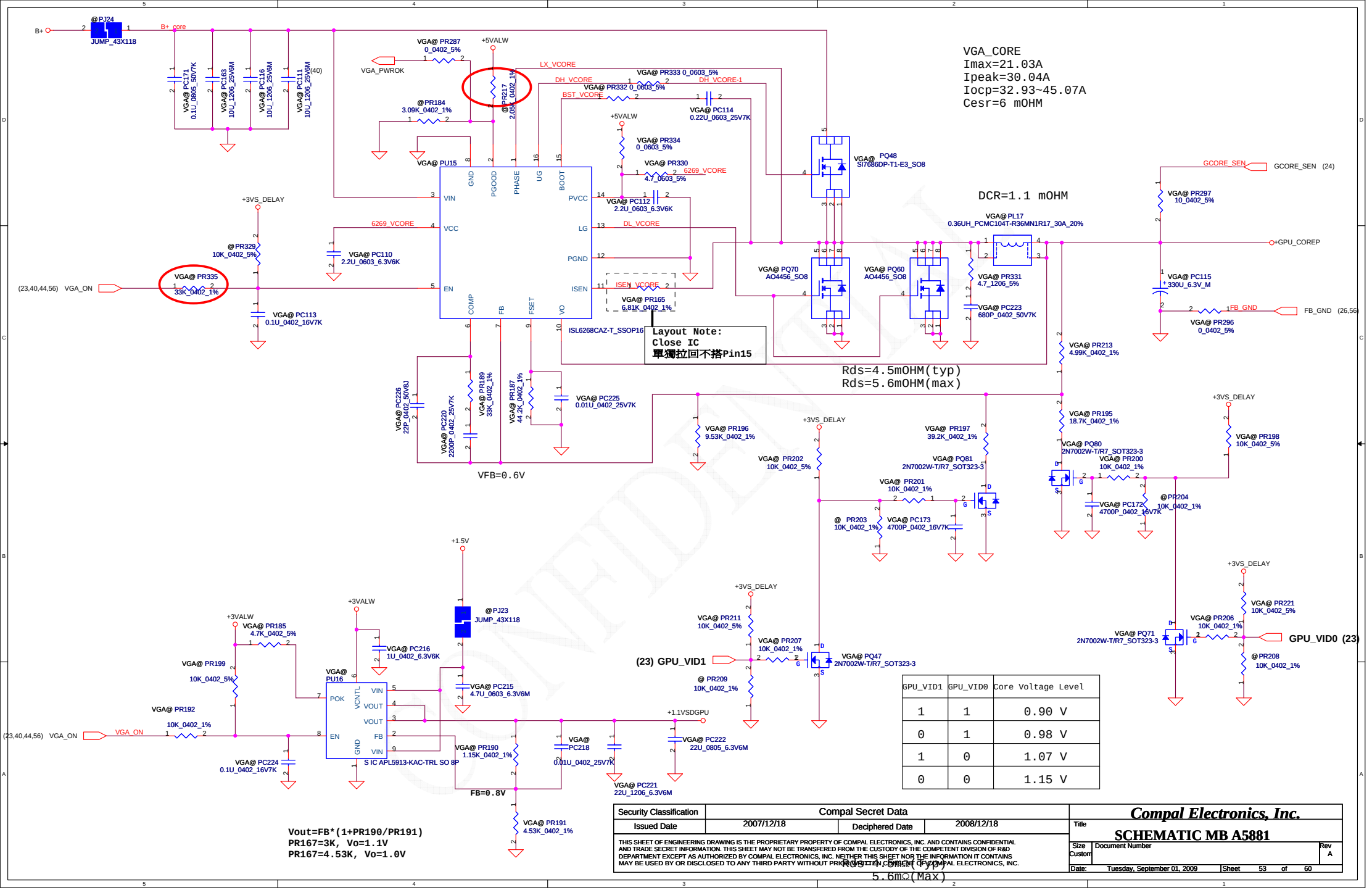
VGA_CORE
Imax=21.03A
Ipeak=30.04A
Iocp=32.93~45.07A
Cesr=6 mOHM
DCR=1.1 mOHM
Rds=4.5mOHM(typ)
Rds=5.6mOHM(max)
VFB=0.6V
FB=0.8V
Vout=FB*(1+PR190/PR191)
PR167=3K, Vo=1.1V
PR167=4.53K, Vo=1.0V
Layout Note:
Close IC
單獨拉回不搭Pin15
ISL6268CAZ-T_SSOP16
S IC APL5913-KAC-TRL SO 8P
JUMP_43X118
SI7686DP-T1-E3_SO8
AO4456_SO8
2N7002W-T/R7_SOT323-3
0.36UH_PCMC104T-R36MN1R17_30A_20%
B+
B+ core
VGA_ON
VGA_PWROK
+5VALW
+3VS_DELAY
+3VALW
+1.5V
+1.1VSDGPU
+GPU_COREP
GCORE_SEN
FB_GND
GPU_VID0 (23)
(23) GPU_VID1
LX_VCORE
DH_VCORE
DH_VCORE-1
BST_VCORE
6269_VCORE
DL_VCORE
ISEN_VCORE
GND
PGOOD
PHASE
UG
BOOT
VIN
VCC
LG
PGND
ISEN
COMP
FB
FSET
VO
PVCC
EN
POK
VCNTL
VOUT
GPU_VID1 | GPU_VID0 | Core Voltage Level
1 | 1 | 0.90 V
0 | 1 | 0.98 V
1 | 0 | 1.07 V
0 | 0 | 1.15 V
Security Classification
Compal Secret Data
Issued Date
2007/12/18
Deciphered Date
2008/12/18
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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum/2)=0.763
where Rn=PR258 // (PR251+PH6)=5.875k ohm
Rsum=PR221, PR253 =3.65k ohm
LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A
where Rdroop=PR239=2.61k ohm , Ri=PR256=1.21k ohm
Iocp= OCP Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A

Layout Note:
PH3 place near Phase1 L-MOS

Layout Note:
Place near Phase1 Choke

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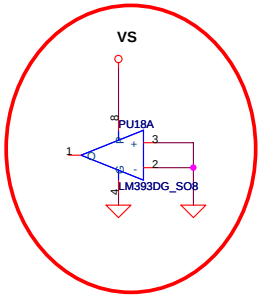

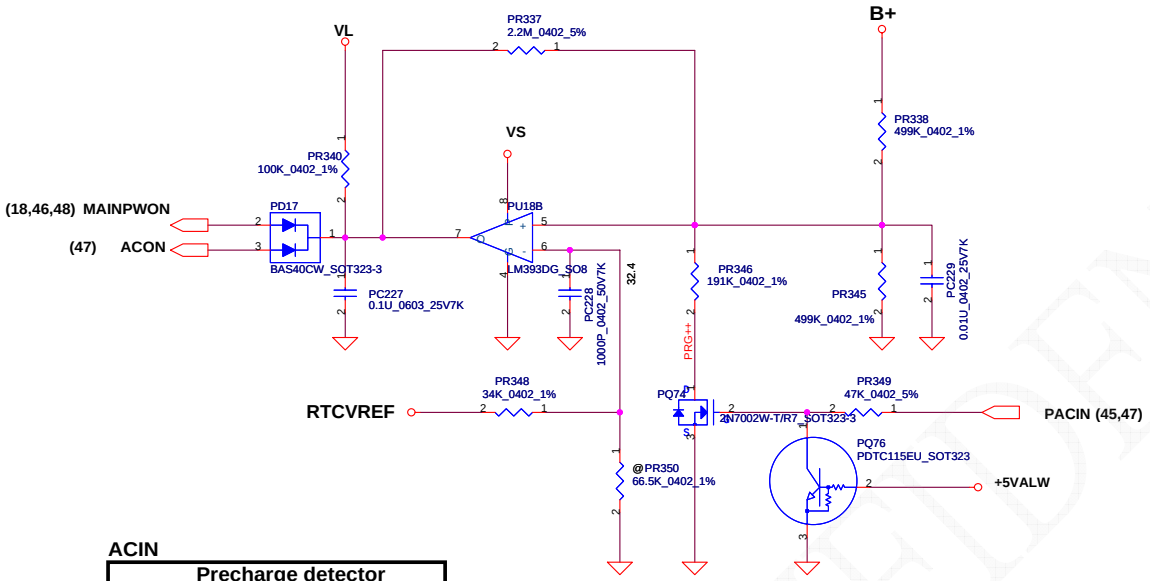

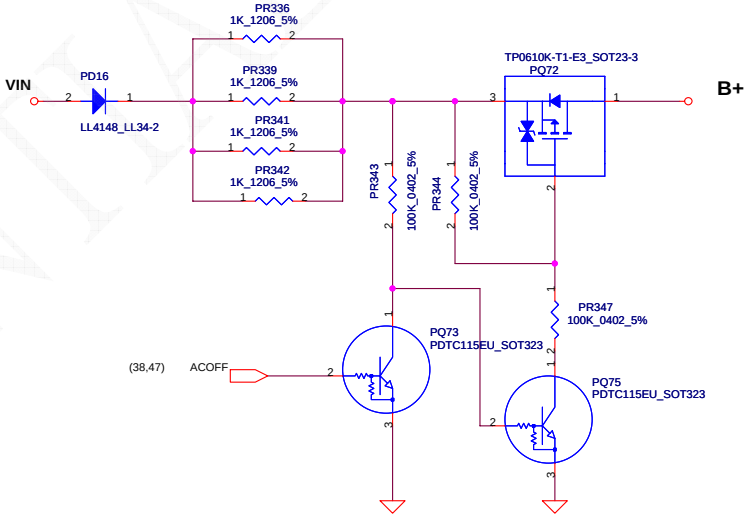

ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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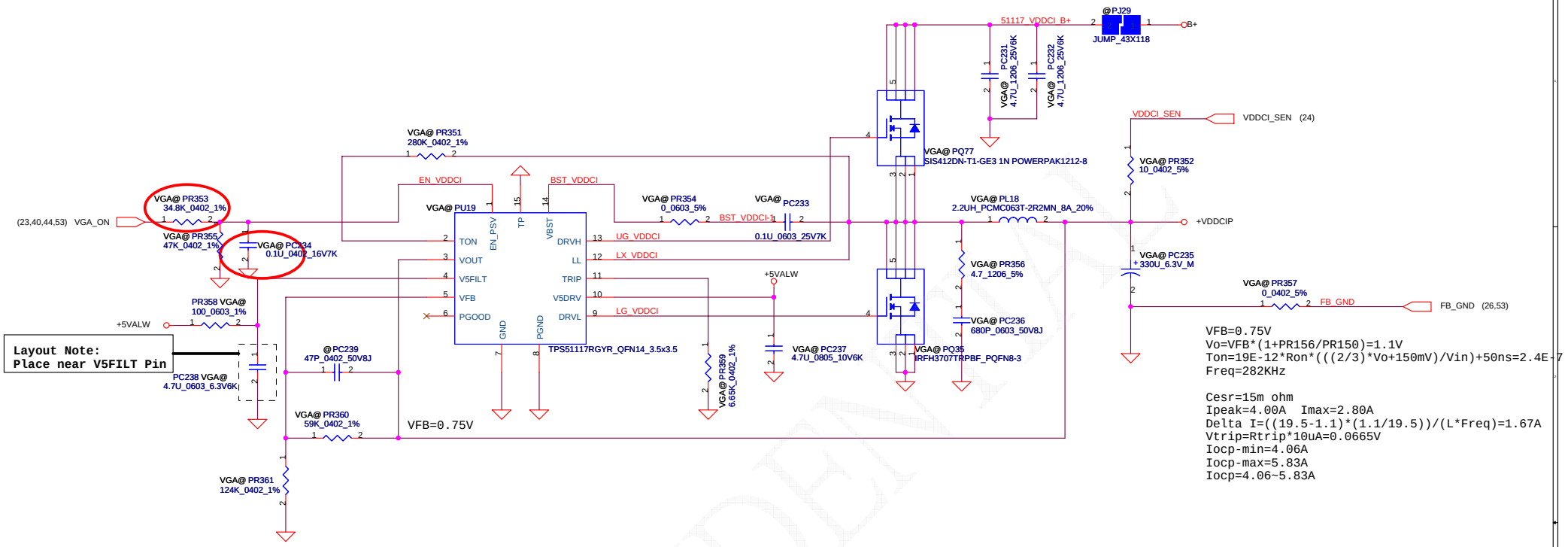

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A --> B Change List

Reference to KBLA0 LA4811 Change List Excel File

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add all sunbber R	EMI solution	0.1	52		09/08/27	DVT
2	add all sunbber C	EMI solution	0.1	52		09/08/27	DVT
3	remove VGA enable R	HW request	0.1	53	delete PR217 2.05K_0402_1%	09/08/27	DVT
4	VDDCI EN sequency regulate	HW request	0.1	53	PR335:32k P/N:SD034330280	09/08/27	DVT
5	VGA EN sequency regulate	HW request	0.1	53	PR353 : 35k P/N:SD00000UD80 PC234 :@==> add	09/08/27	DVT
6							
7							
8							
9							
10							
11							
12							
13							
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16							
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23							

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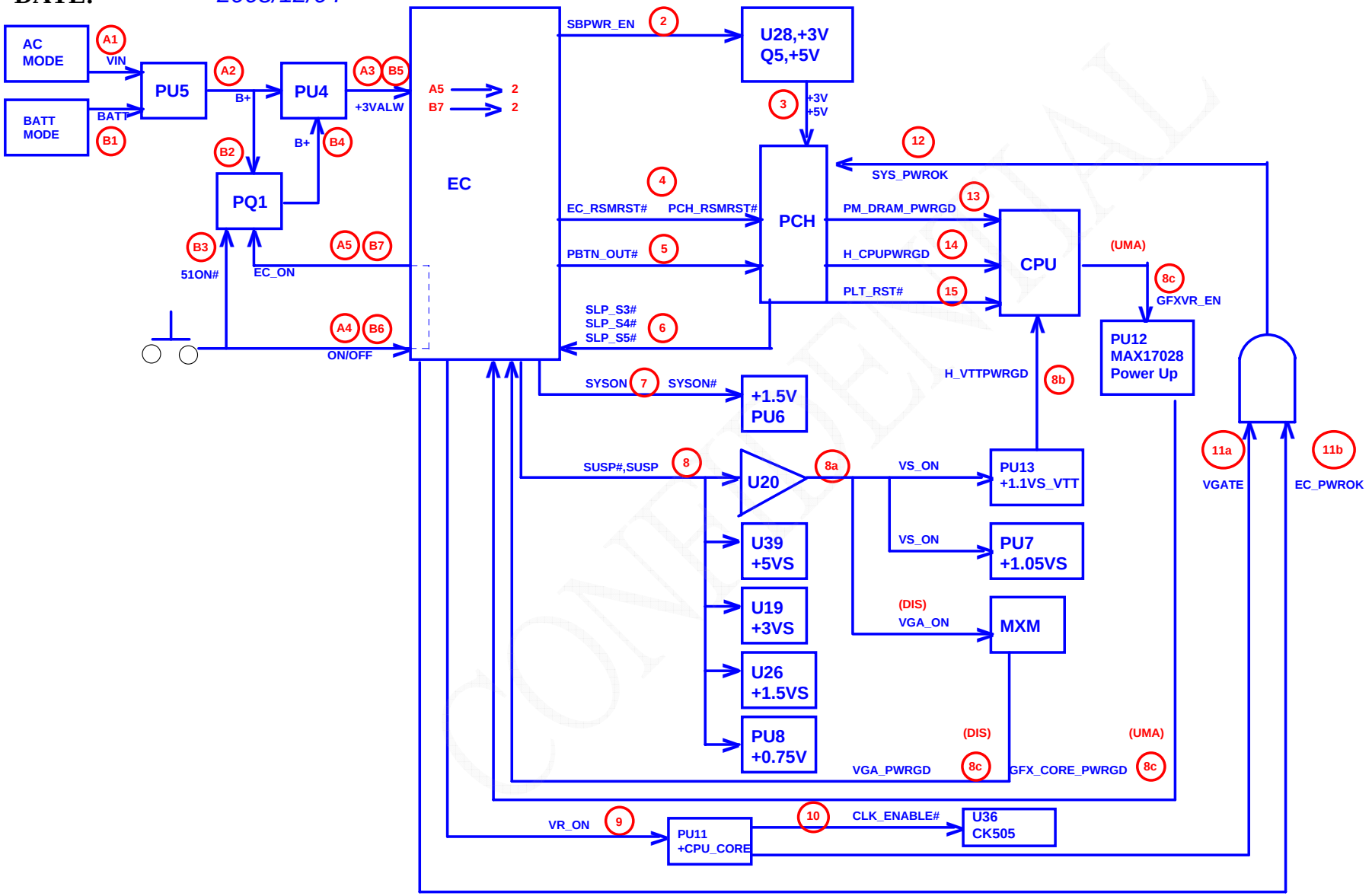
MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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