

Compal Confidential

NTV00

LA-5662 Rev 0.2 Schematics

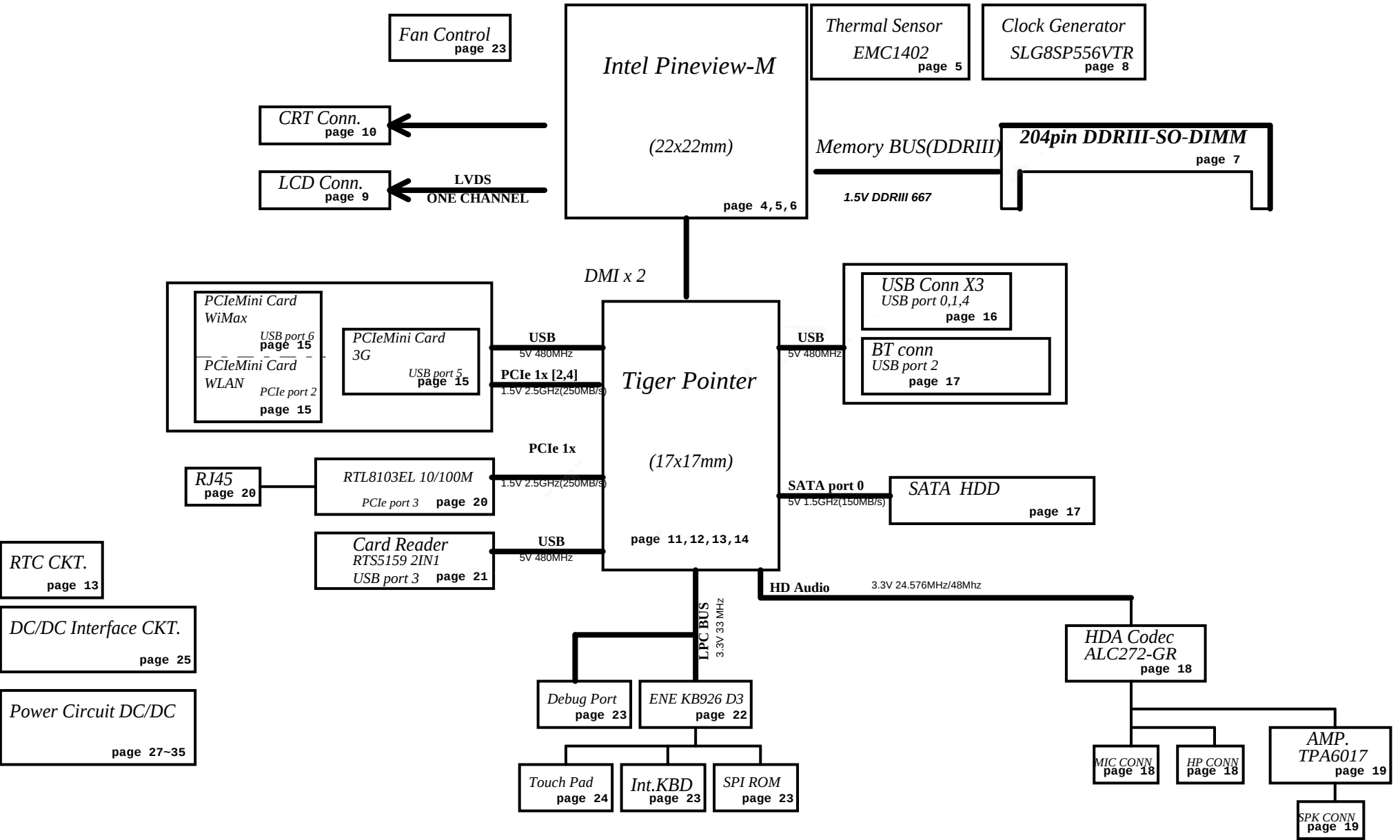
Intel PineView Processor/ Tiger point

2010-05-10 REV : 1.0

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Compal Confidential

Model Name : NTV00
File Name : LA-5661P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				STAR			
description								
explain	Wi-Fi	WiMax	3G		POWER SAVING			
BTO	WLAN@	WIMAX@	3G@		STAR@			

Function			
description			
explain			
BTO			

EC SM Bus1 address

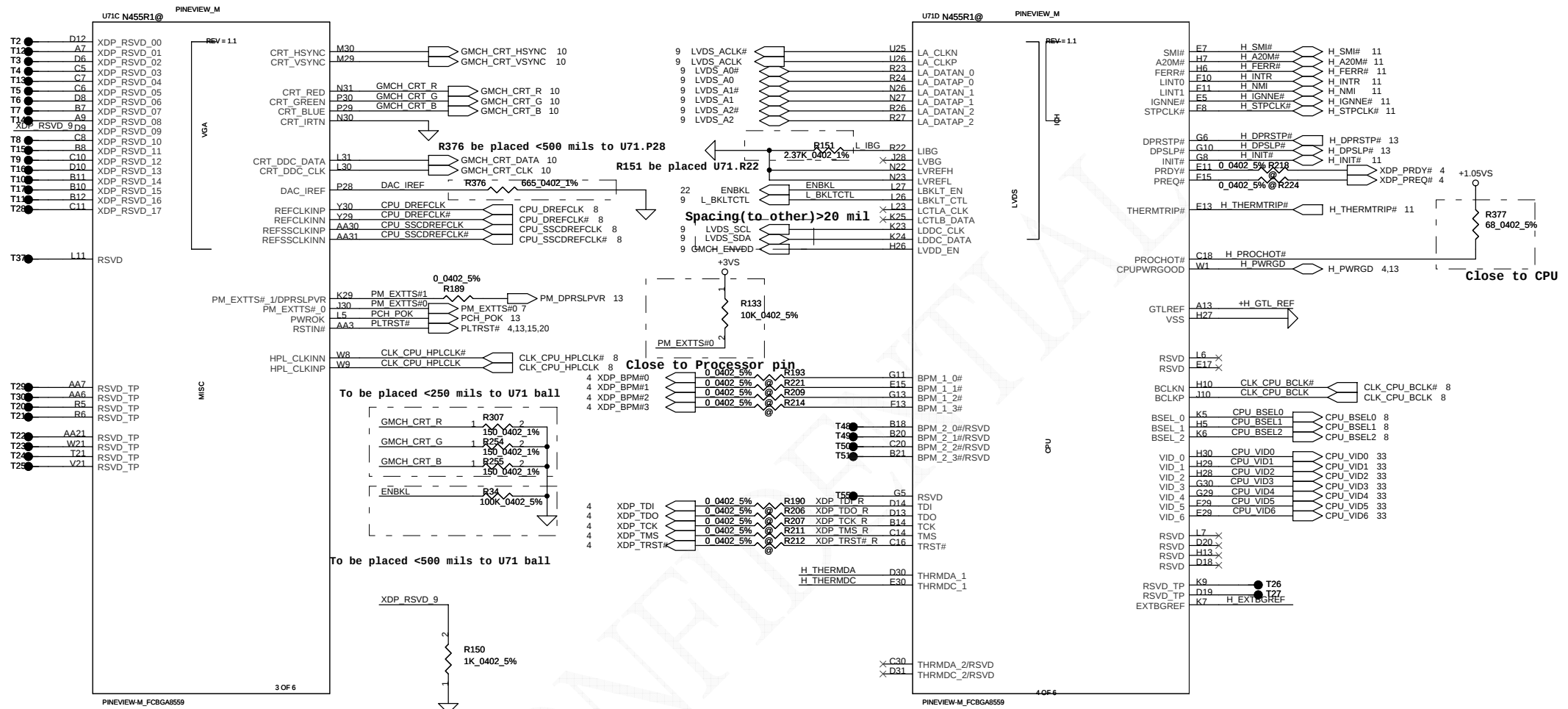
EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

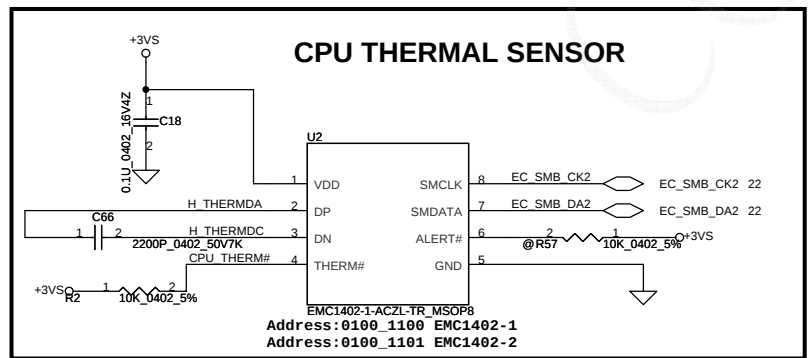
Tiger point SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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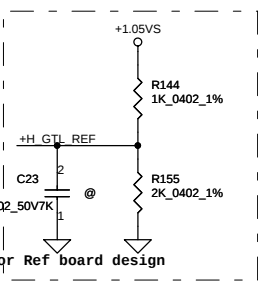
Pull down 1K to GND for Intel request



H DPRSTP#	C416	2	220P 0402 50V7K
H DPSLP#	C398	1	2 220P 0402 50V7K
H PWRGD	C514	1	2 220P 0402 50V7K
H A20M#	C419	1	2 220P 0402 50V7K
H IGNNE#	C441	1	2 220P 0402 50V7K
H INIT#	C399	1	2 220P 0402 50V7K
H INTR	C414	1	2 220P 0402 50V7K
H FERR#	C424	1	2 220P 0402 50V7K
H NMI	C445	1	2 220P 0402 50V7K
H SMI#	C415	1	2 220P 0402 50V7K
H STPCLK#	C447	1	2 220P 0402 50V7K

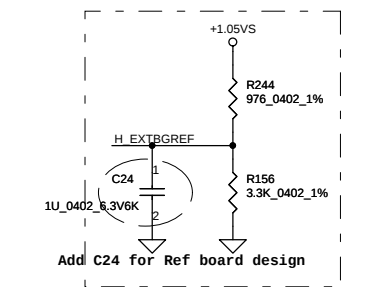
ESD request

placed within 0.5" of processor pin.



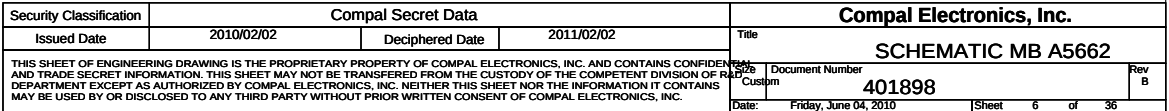
Reserve C23 for Ref board design

placed within 0.5" of processor pin and 5 mils spacing

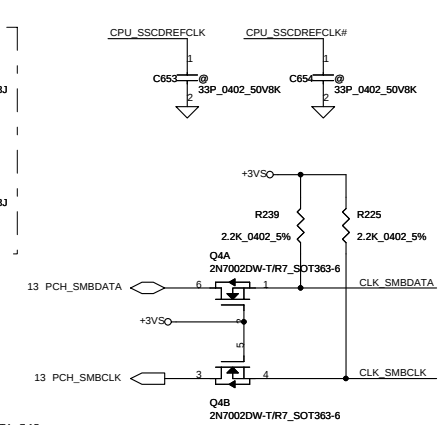
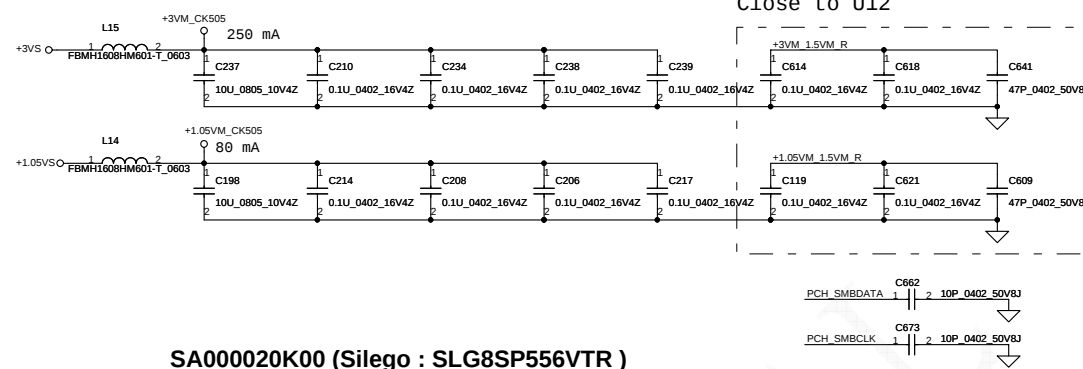


Add C24 for Ref board design

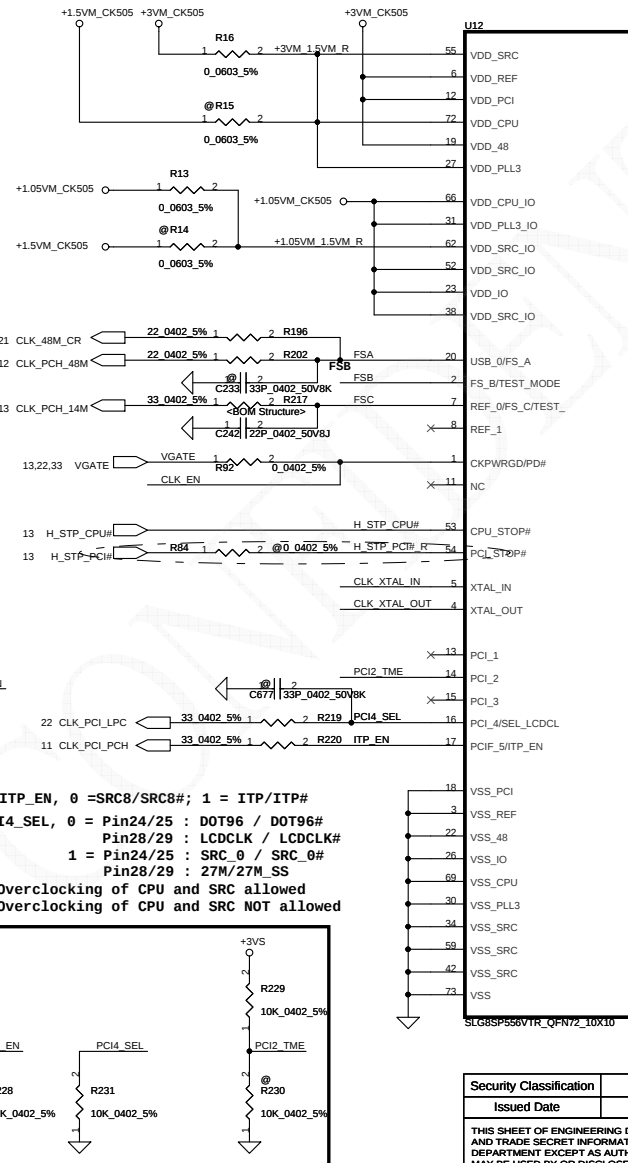
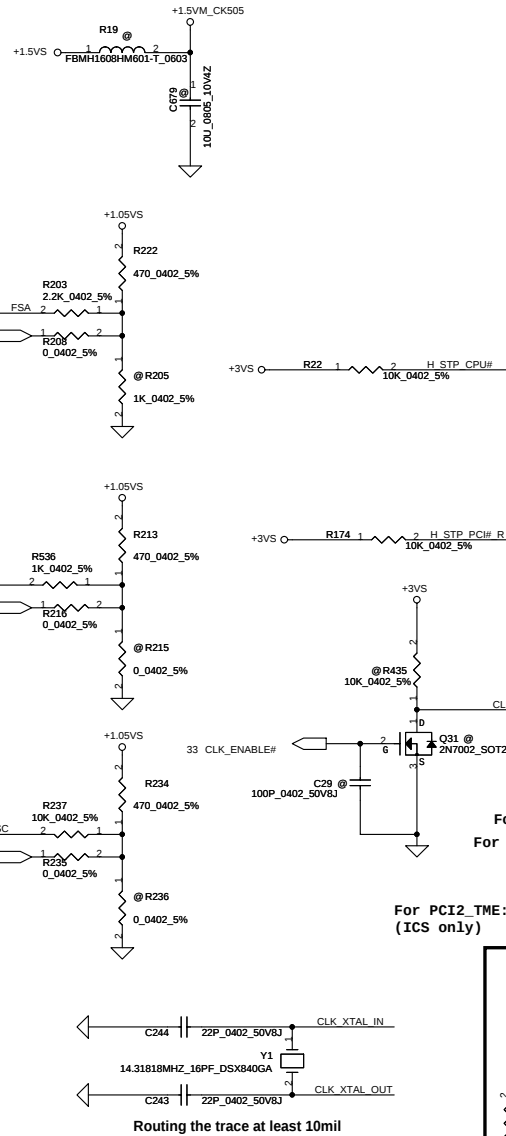
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHZ	SRC MHZ	PCI MHZ	REF MHZ	DOT_96 MHZ	USB MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



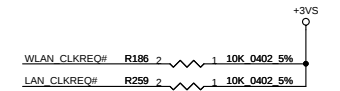
SA000020K00 (Silego : SLG8SP556VTR)



Pin	Signal	Direction	Signal	Direction
9	CLK_SMBDATA	Input	CLK_SMBDATA	7,15
10	CLK_SMBCLK	Input	CLK_SMBCLK	7,15
71	CLK_CPU_BCLK	Input	CLK_CPU_BCLK	5
CPU_0#	CLK_CPU_BCLK#	Output	CLK_CPU_BCLK#	5
CPU_0#	CLK_CPU_HPLCLK	Input	CLK_CPU_HPLCLK	5
CPU_1	CLK_CPU_HPLCLK#	Output	CLK_CPU_HPLCLK#	5
CPU_1#	CLK_CPU_HPLCLK#	Input	CLK_CPU_HPLCLK#	5
24	CPU_DREFCLK	Input	CPU_DREFCLK	5
SRC_0IDOT_96	CPU_DREFCLK#	Output	CPU_DREFCLK#	5
SRC_0#IDOT_96#	CPU_DREFCLK#	Input	CPU_DREFCLK#	5
28	CPU_SSCDREFCLK	Input	CPU_SSCDREFCLK	5
LCDCLK#27M	CPU_SSCDREFCLK#	Output	CPU_SSCDREFCLK#	5
LCDCLK#27M_SS	CPU_SSCDREFCLK#	Input	CPU_SSCDREFCLK#	5
32	CLK_CPU_EXP	Input	CLK_CPU_EXP	4
SRC_2#	CLK_CPU_EXP#	Output	CLK_CPU_EXP#	4
SRC_3	—X			
SRC_3#	—X			
39	CLK_PCIE_SATA	Input	CLK_PCIE_SATA	11
SRC_4#	CLK_PCIE_SATA#	Output	CLK_PCIE_SATA#	11
57	CLK_PCIE_WLAN	Input	CLK_PCIE_WLAN	15
SRC_6#	CLK_PCIE_WLAN#	Output	CLK_PCIE_WLAN#	15
SRC_7	—X			
SRC_7#	—X			
64	CLK_PCIE_I2P	Input	CLK_PCIE_I2P	20
SRC_8#(CPU_I2P)	—X			
44	CLK_PCIE_LAN	Input	CLK_PCIE_LAN	20
SRC_9#	CLK_PCIE_LAN#	Output	CLK_PCIE_LAN#	20
50	CLK_PCIE_PCH	Input	CLK_PCIE_PCH	12
SRC_10#	CLK_PCIE_PCH#	Output	CLK_PCIE_PCH#	12
SRC_11	—X			
SRC_11#	—X			
37	—X			
41	—X			
58	WLAN_CLKREQ#	Input	WLAN_CLKREQ#	15
43	LAN_CLKREQ#	Input	LAN_CLKREQ#	20
49	—X			
21	—X			

SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	CPU_EXP
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	



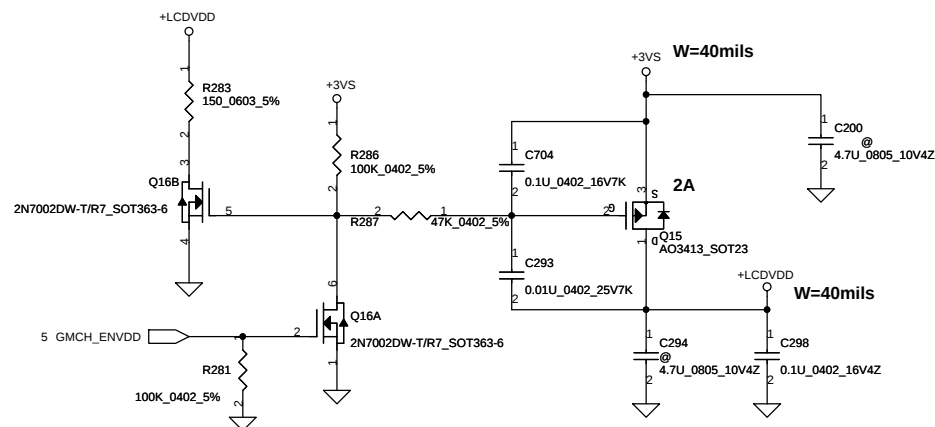
REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	
REQ_A#	

Routing the trace at least 10mil

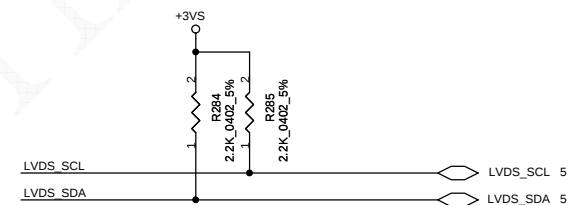
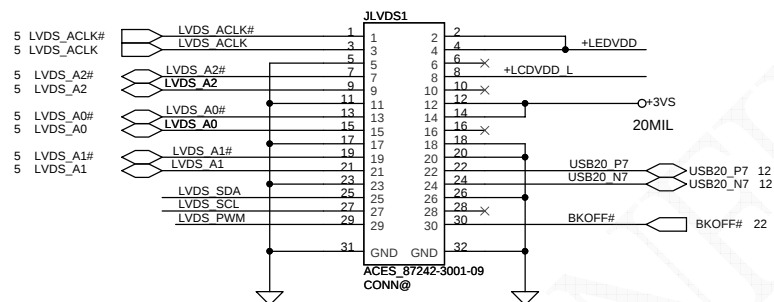
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LCD POWER CIRCUIT

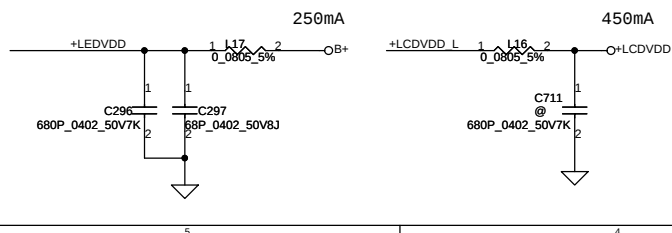
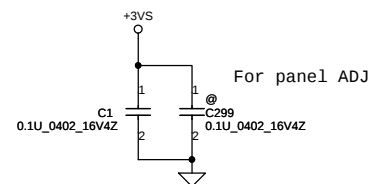
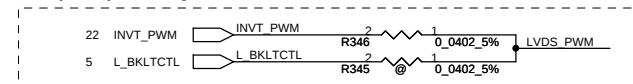


LED/PANEL BD. Conn.

Combine INT.CAMERA with
LVDS

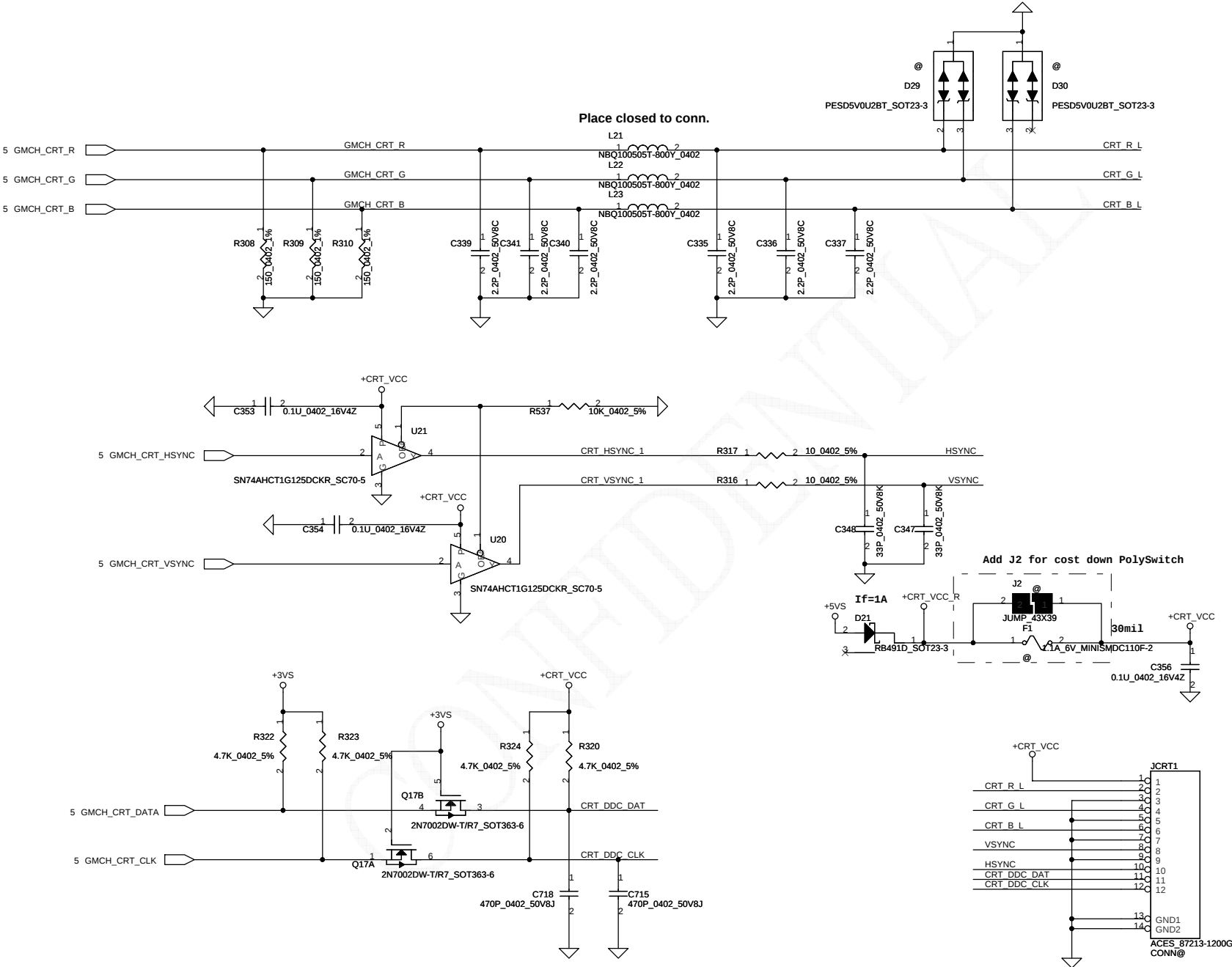


Option panel brightness control

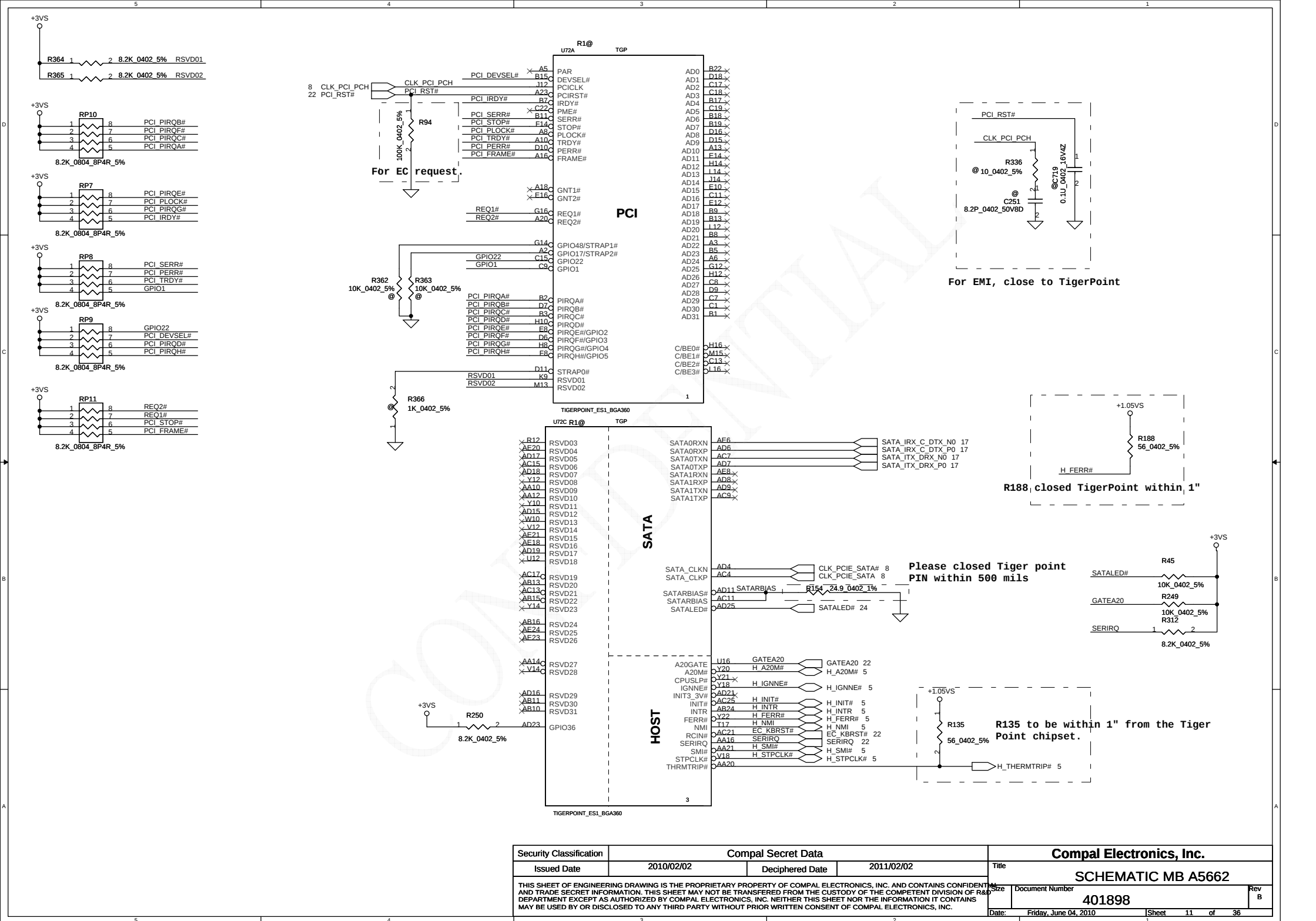


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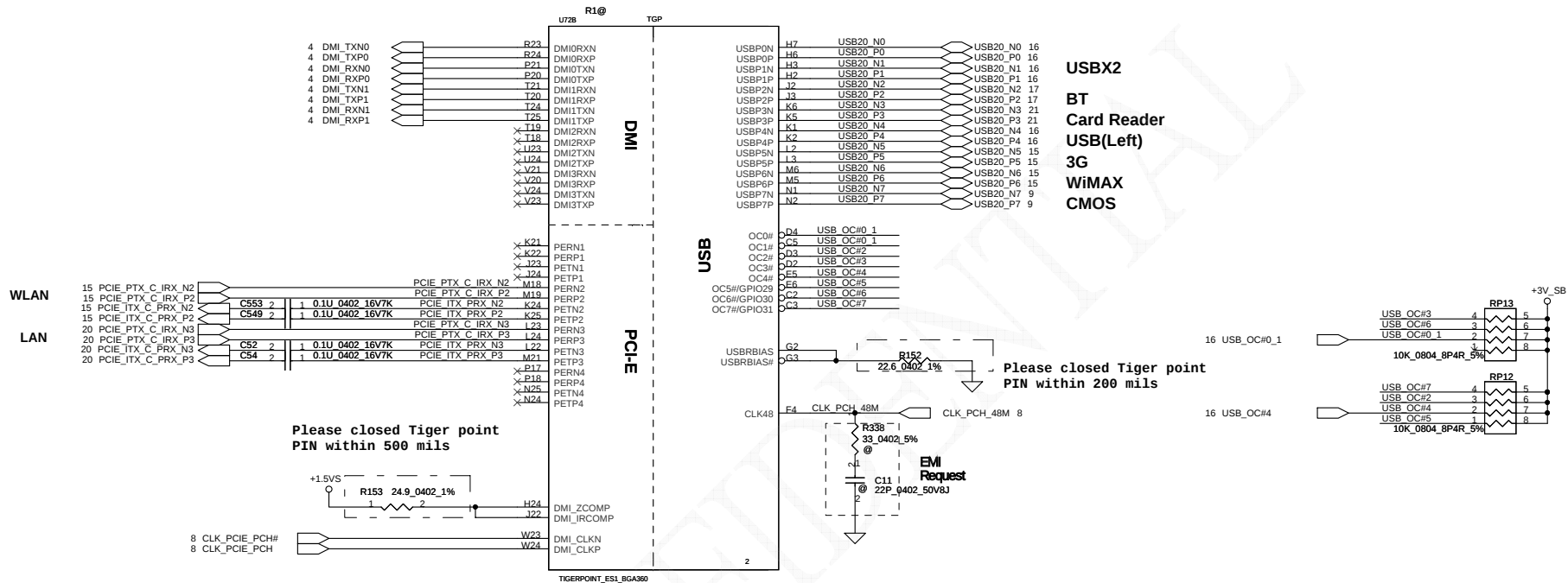
CRT CONNECTOR



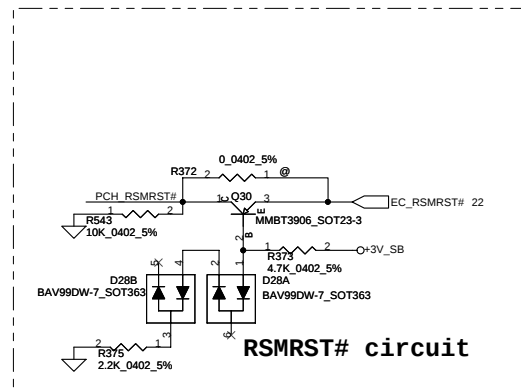
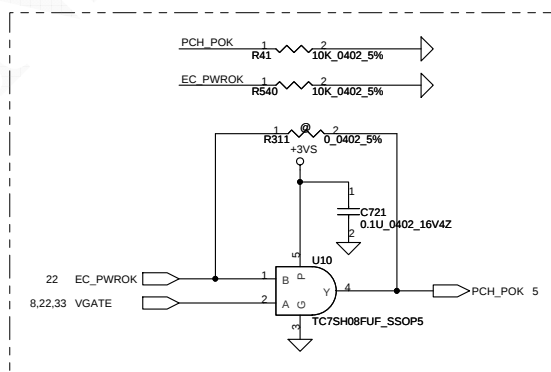
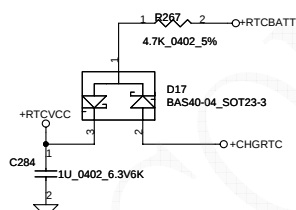
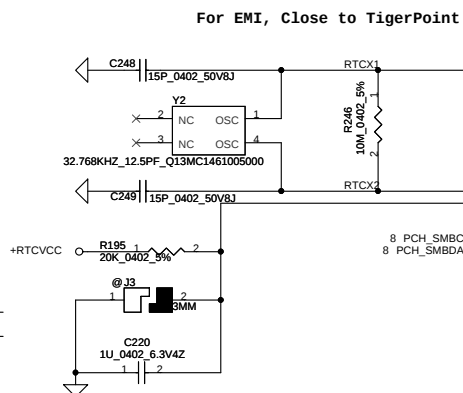
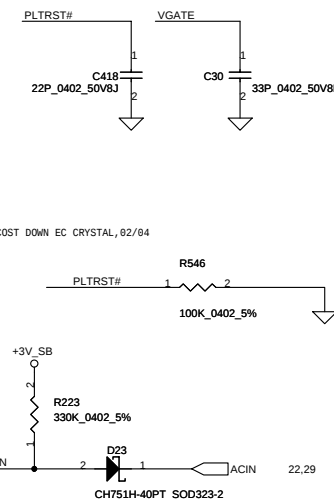
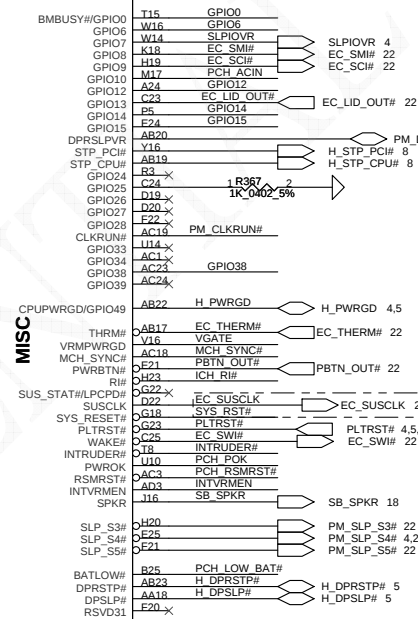
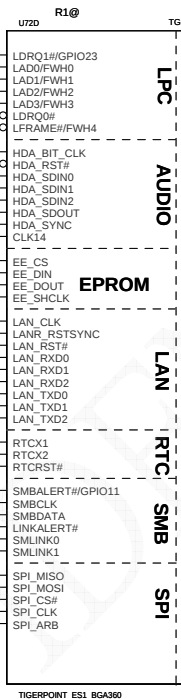
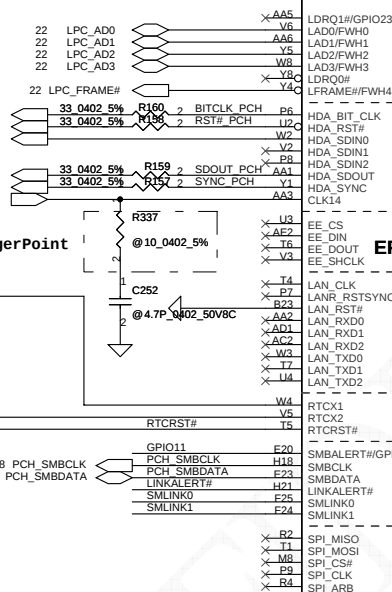
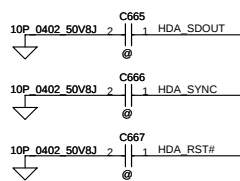
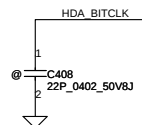
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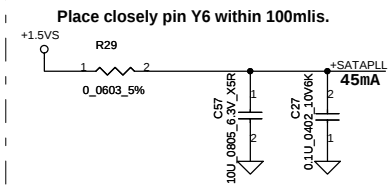
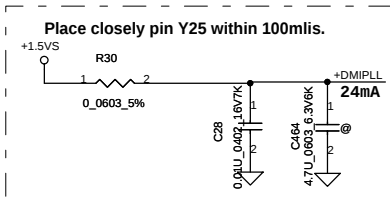
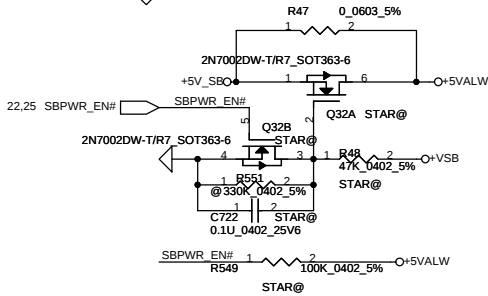
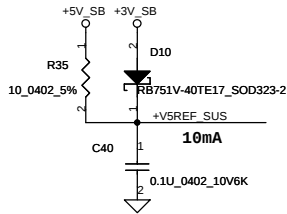
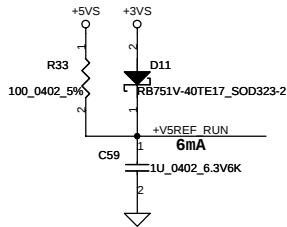
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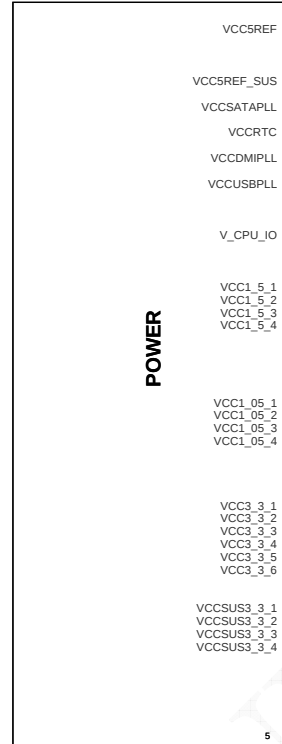
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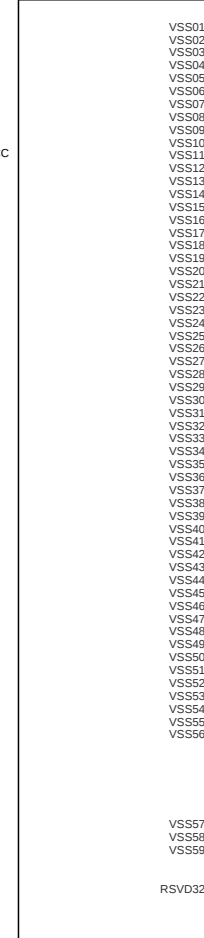


R1@ TGP



TIGERPOINT_ES1_BGA360

R1@ TGP



TIGERPOINT_ES1_BGA360

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WLAN/ WiFi

3VS 120 mil 0.1U 0402 16V4Z 0.01U_0402_25V7K C388 C94 C103 C245 22U_0805_6.3V6M 4.7U_0805_10V4Z

17 WLAN_BT_DATA WLAN_BT_DATA
17 WLAN_BT_CLK WLAN_BT_CLK
8 WLAN_CLKREQ# WLAN_CLKREQ#
8 CLK_PCIE_WLAN# CLK_PCIE_WLAN#
12 PCIE_PTX_C_IRX_N2
12 PCIE_PTX_C_IRX_P2
12 PCIE_ITX_C_PRX_N2
12 PCIE_ITX_C_PRX_P2

3VS 1.5VS 0.1U 0402 16V4Z 0.01U_0402_25V7K 4.7U_0805_10V4Z C125 C116 C124

2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52

JMINI2

WL_OFF# WL_OFF# 22
PLTRST# PLTRST# 4.5,13,20
CLK_SMBCLK 7.8
CLK_SMBCLK 7.8
USB20_N6 12
USB20_P6 12
WLAN_LED# MO
WLAN_LED# MO (9-)

R60 1 2 0.0402 5%
R74 1 2 0.0402 5%
R68 100K_0402_5%
R418 100K_0402_5%

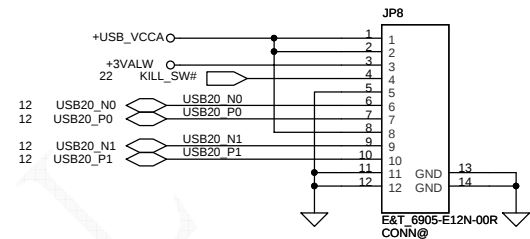
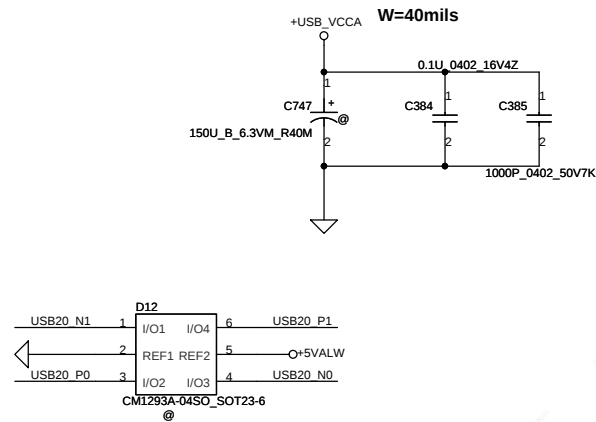
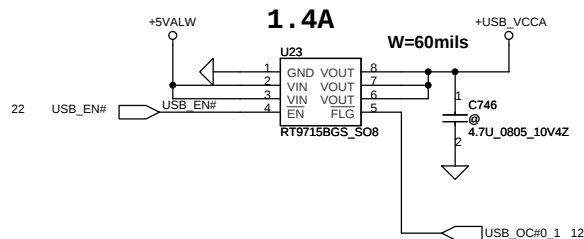
Debug card using

FOX AS06226-S40N-7F CONN@

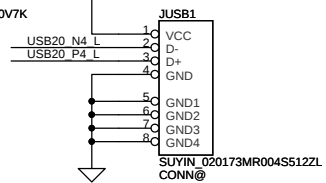
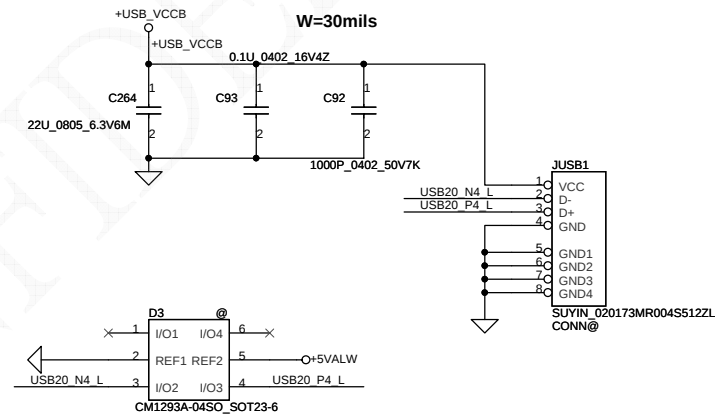
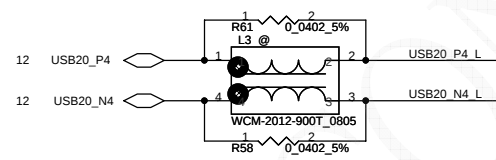
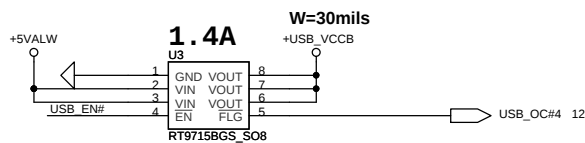
10P_0402_50V8J
10P_0402_50V8J

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USB X2

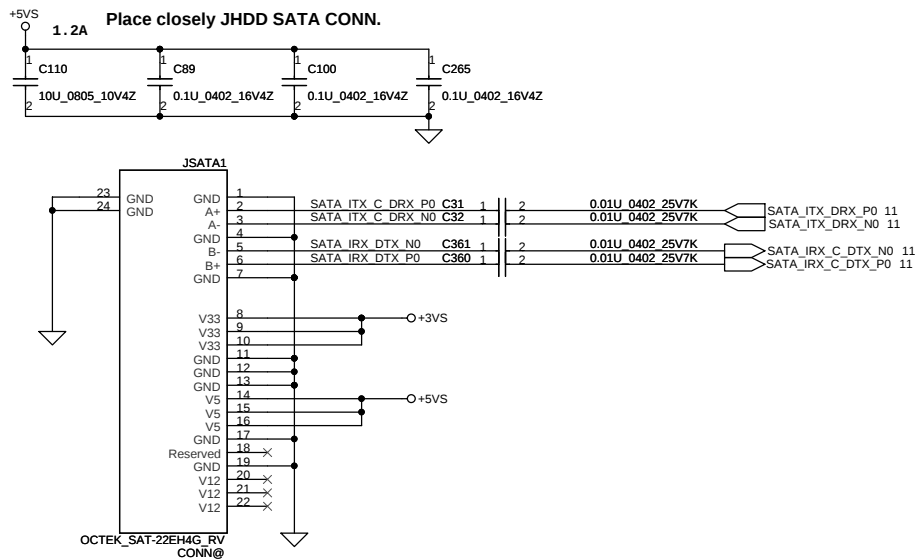


USB Board--Left

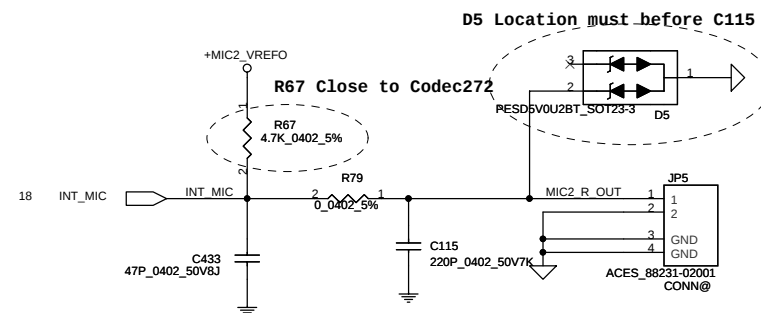
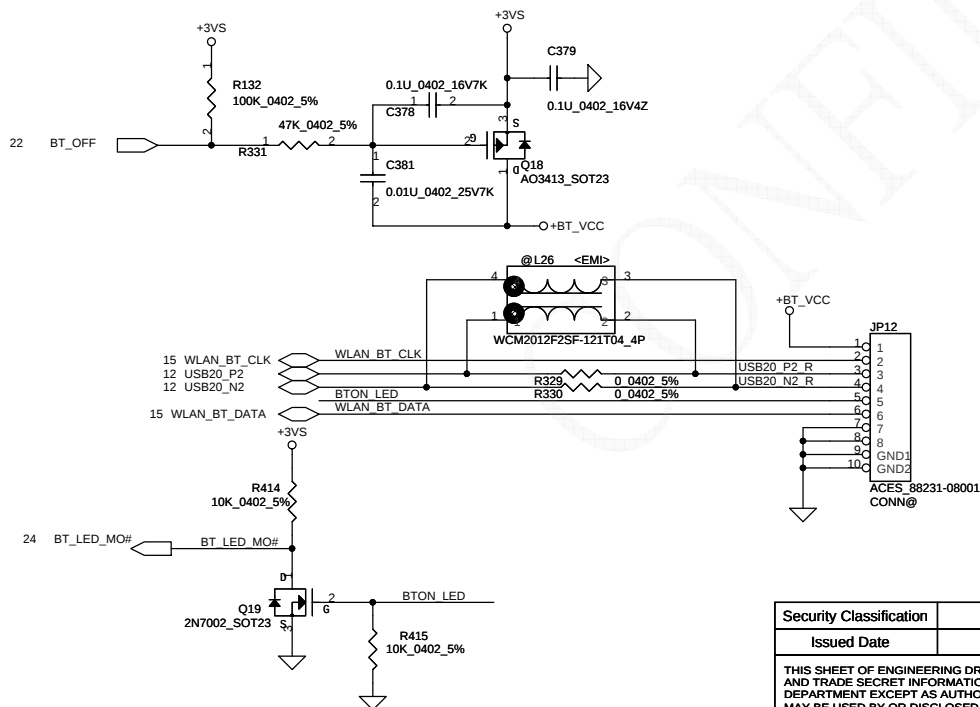


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SATA Conn.



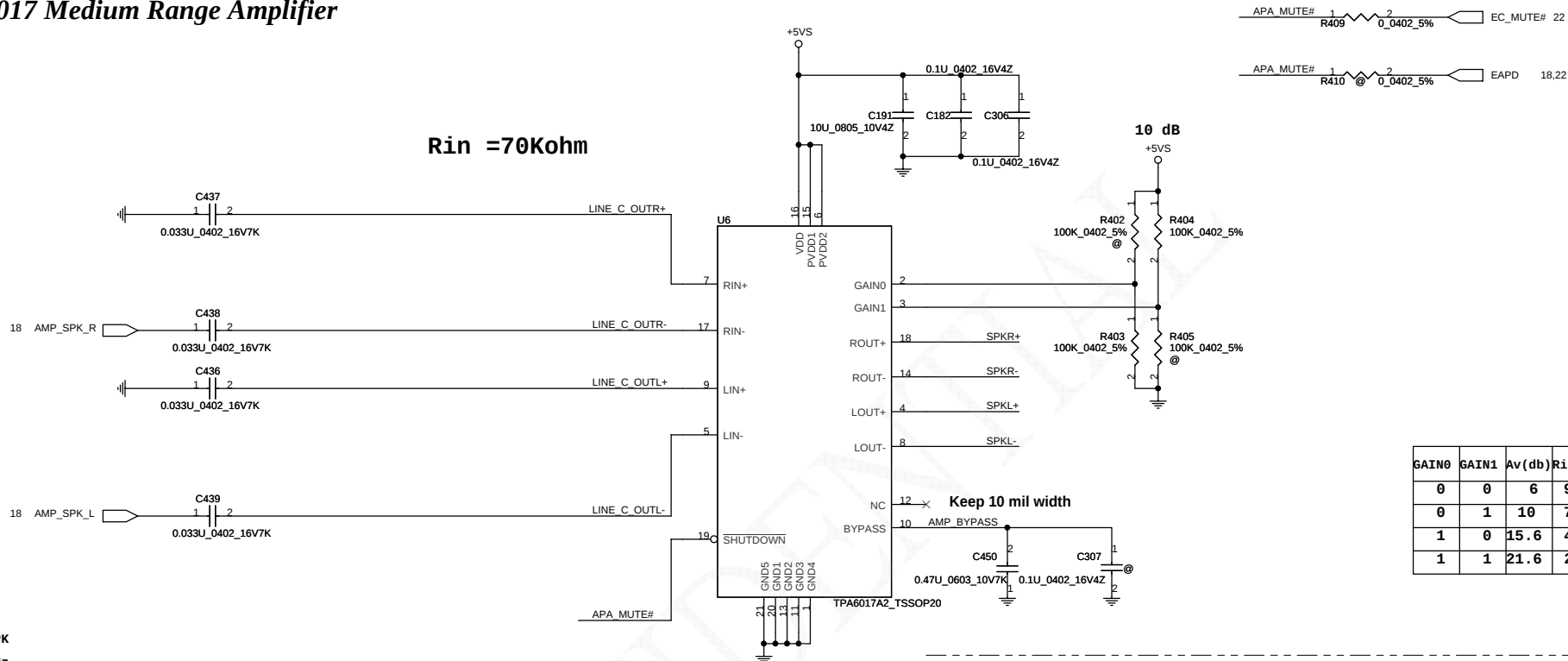
BlueTooth Interface



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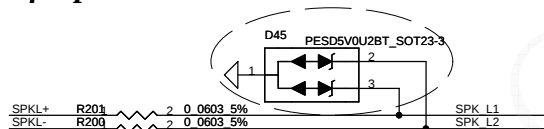
TPA6017 Medium Range Amplifier

Rin =70Kohm



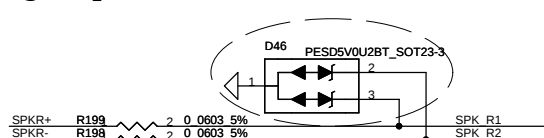
Use mono SPK
setting 68Hz
F=1/2πRC --> -3db
C=0.033U, R=70K, F=68Hz

Left Speaker Connector

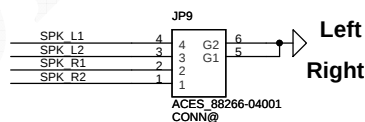


7/3 Change to SCA00000T00 for ESD request

Right Speaker Connector

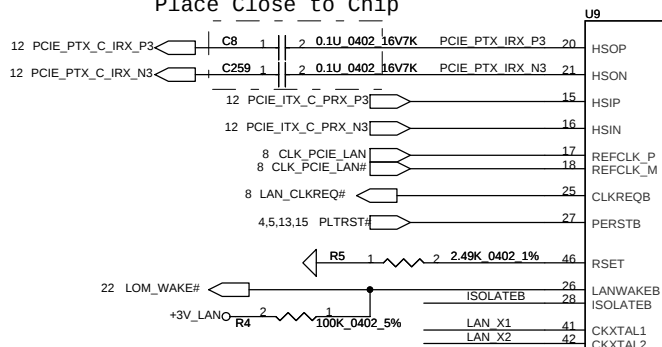


7/3 Change to SCA00000T00 for ESD request

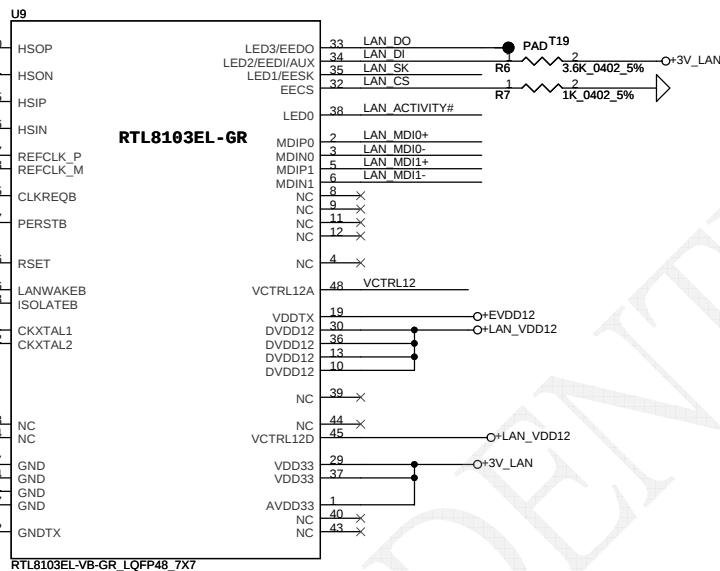


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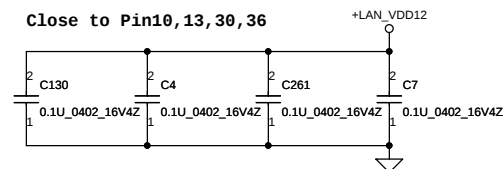
Place Close to Chip



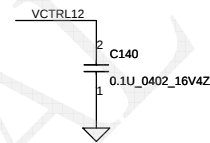
RTL8103EL-GR



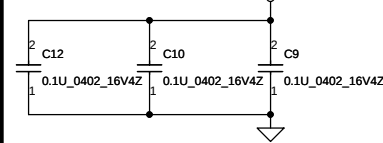
Close to Pin10,13,30,36



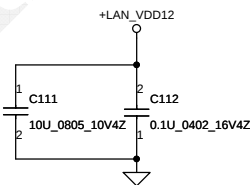
Close to Pin48



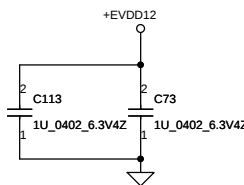
Close to Pin1,37,29



Close to Pin 45

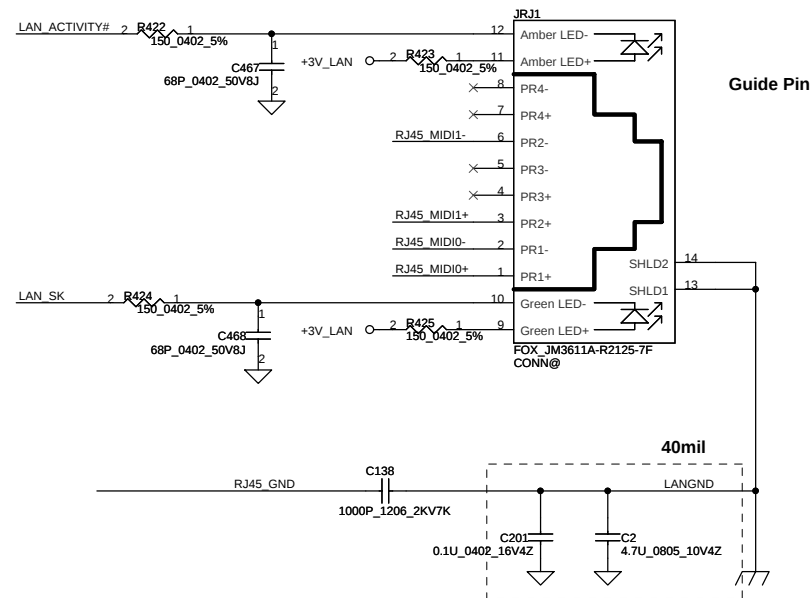
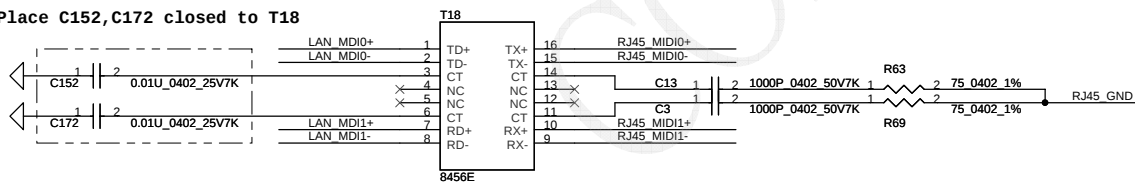


Close to Pin19

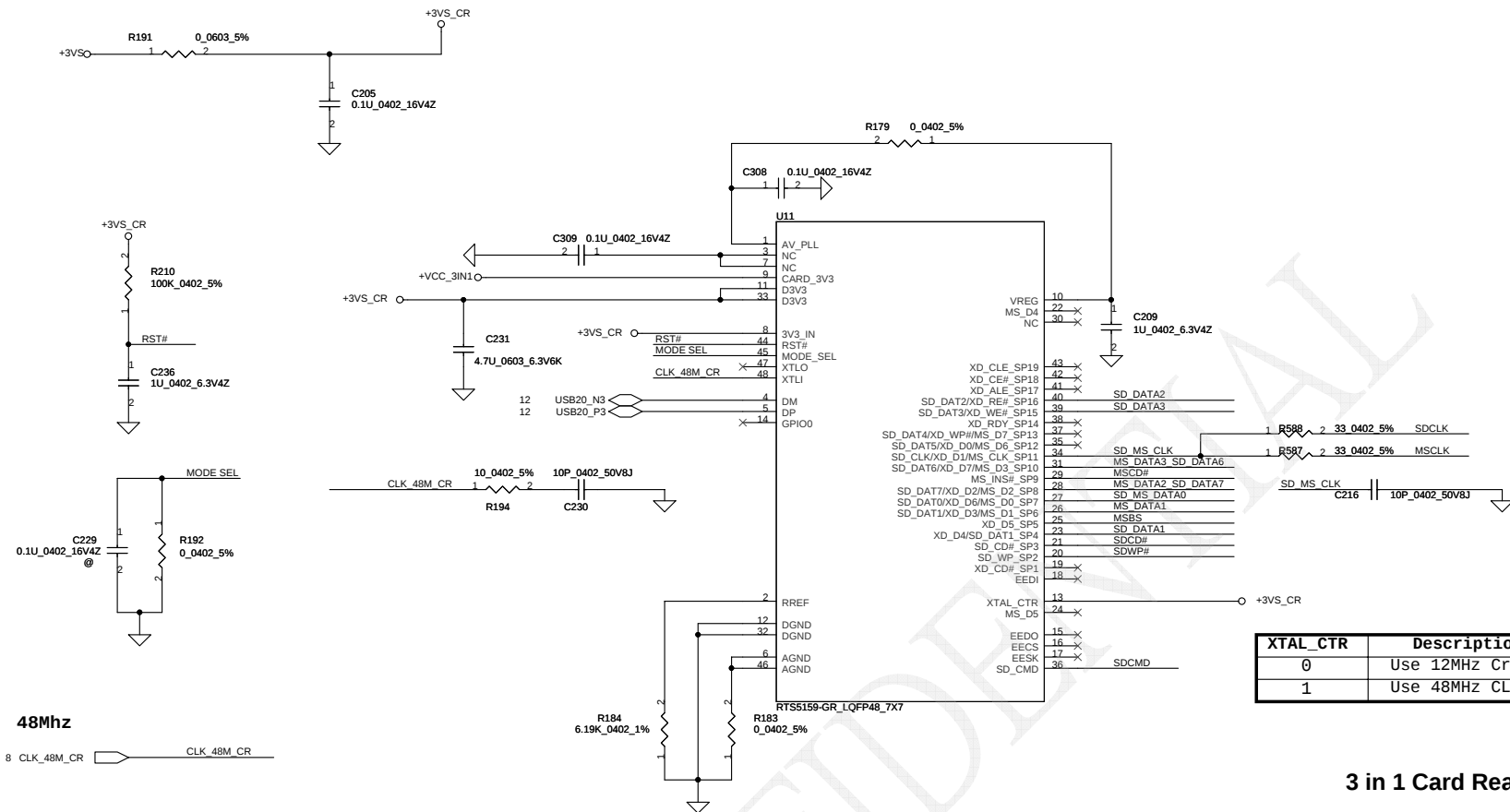


Lan Conn.

Place C152,C172 closed to T18

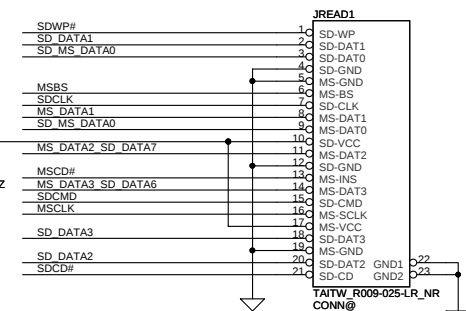


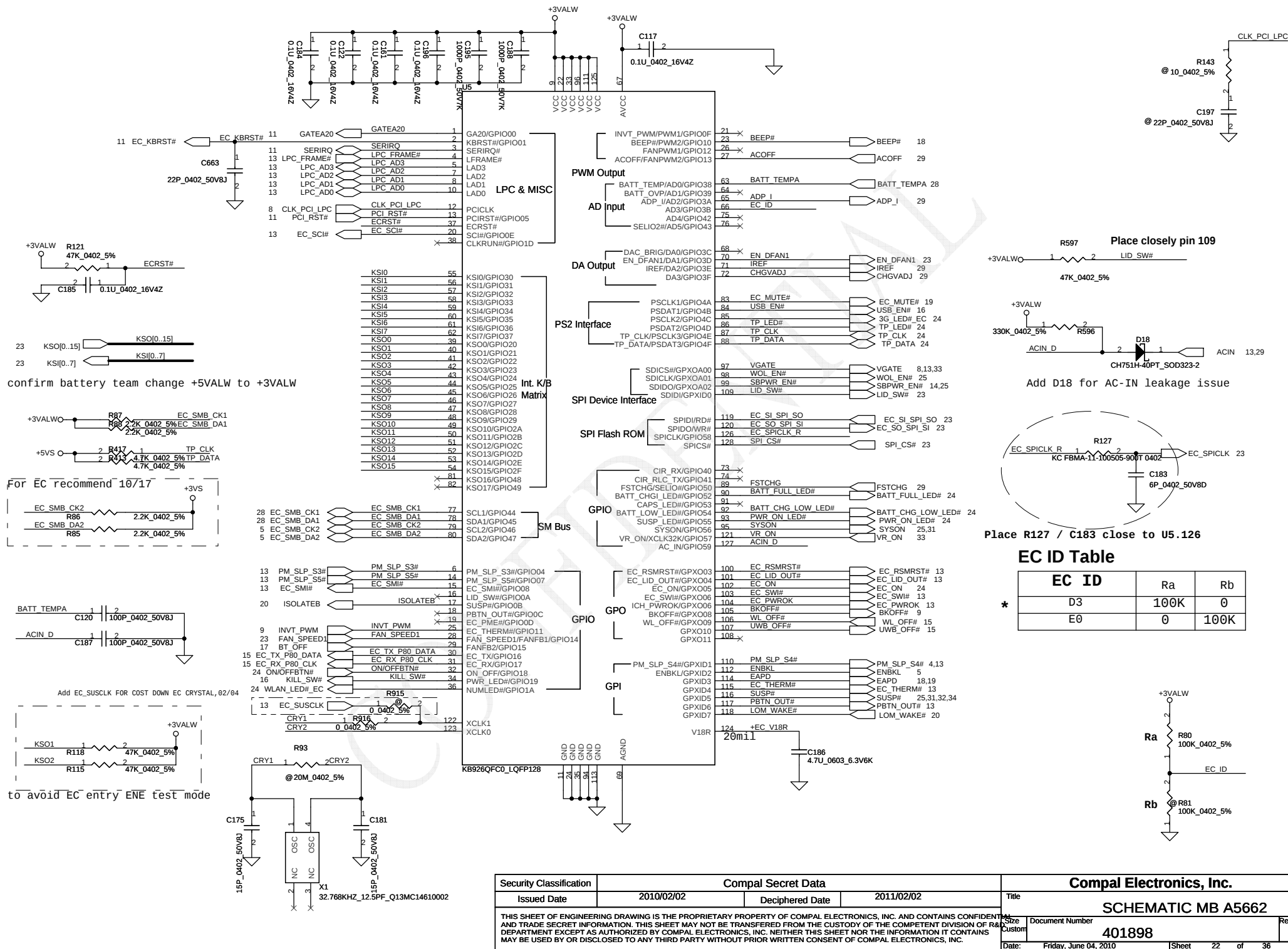
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3 in 1 Card Reader

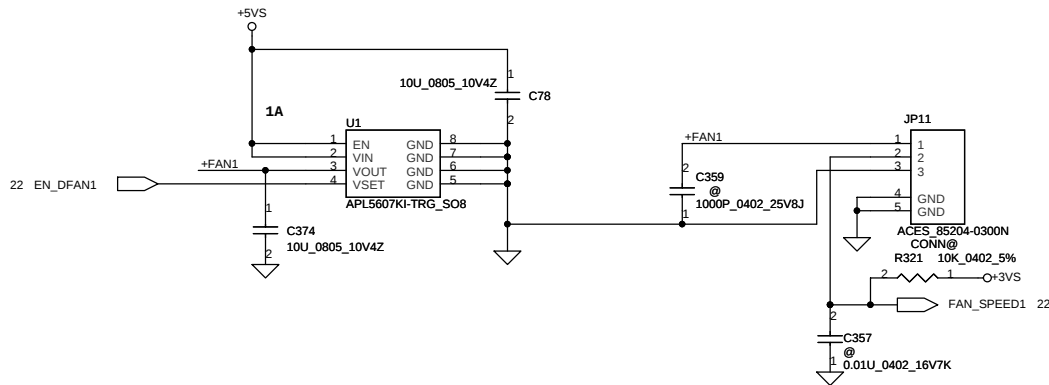
R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	



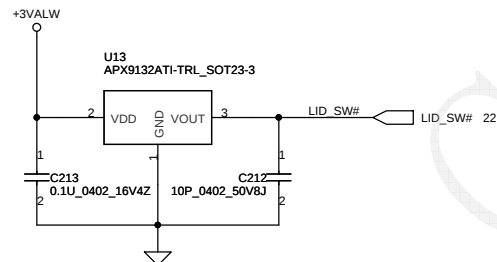
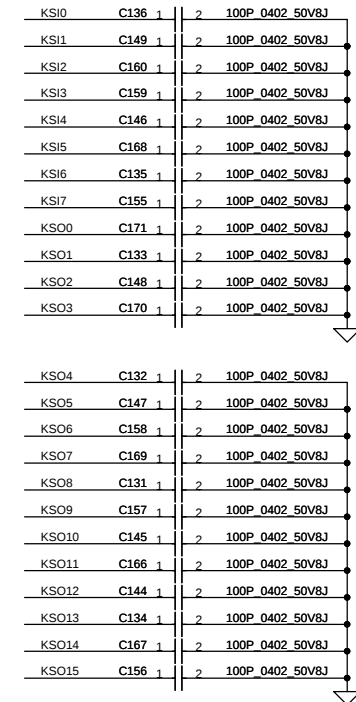
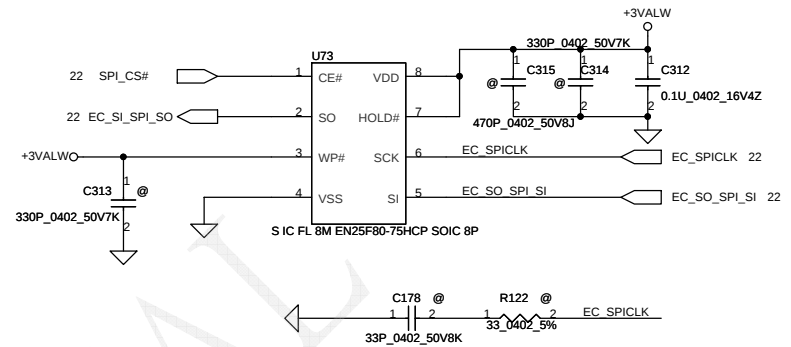
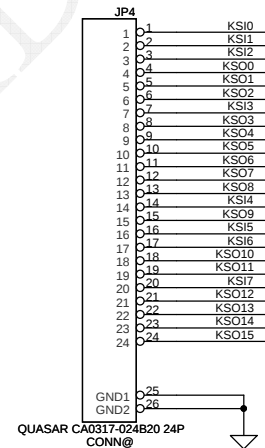
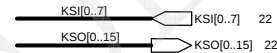


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Lid SW

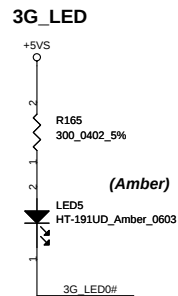
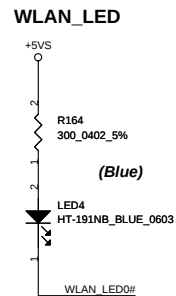
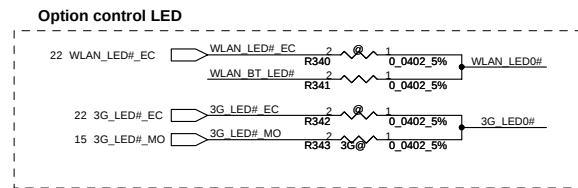
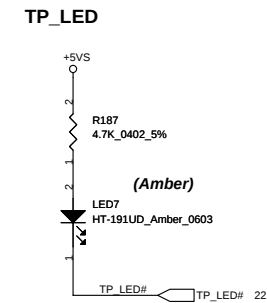
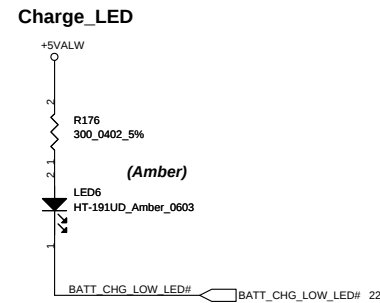
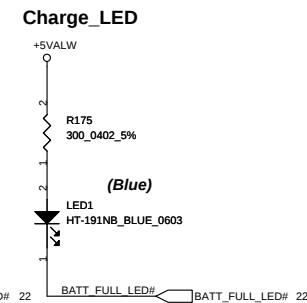
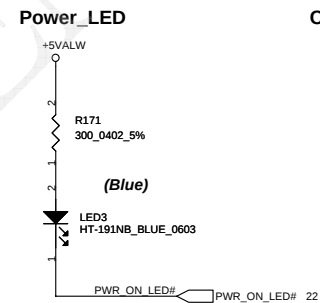
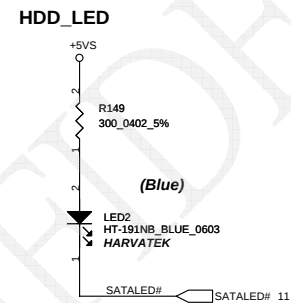
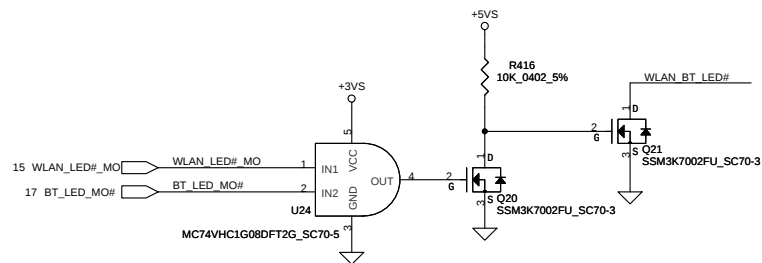
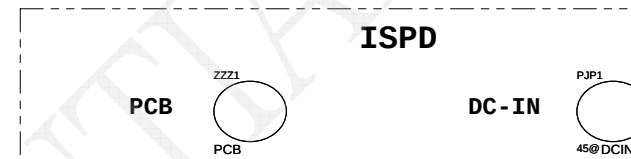
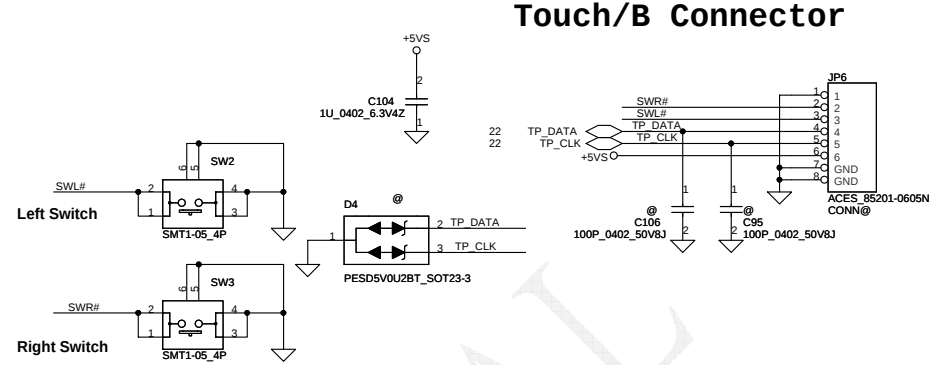
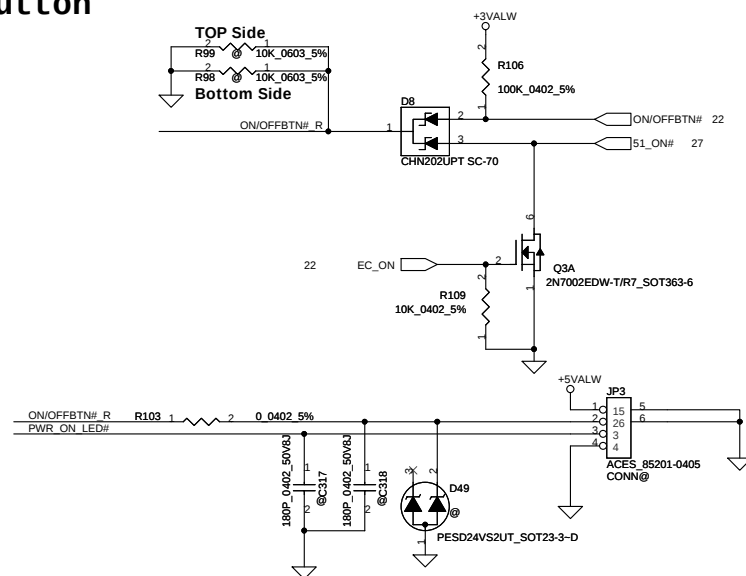


**KEYBOARD
CONN.**



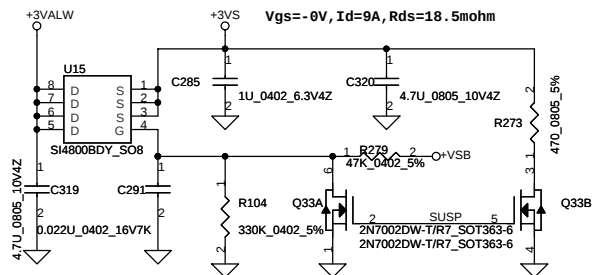
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Power Button

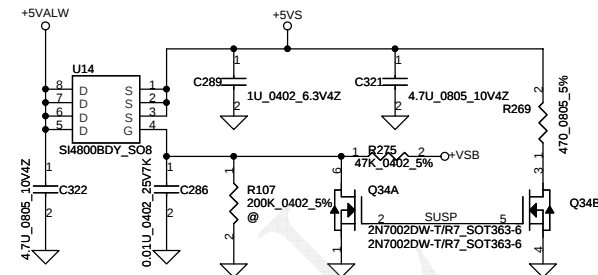


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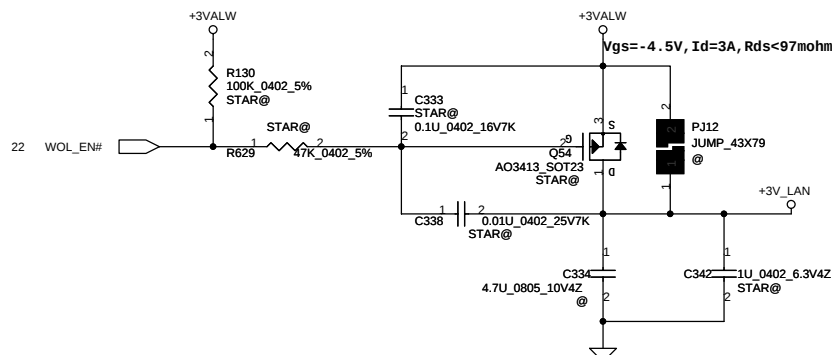
+3VALW TO +3VS



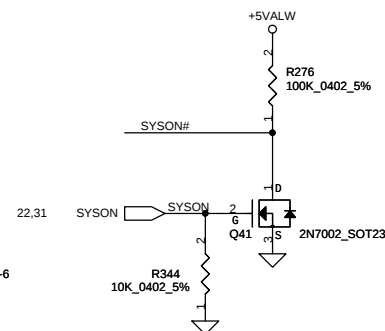
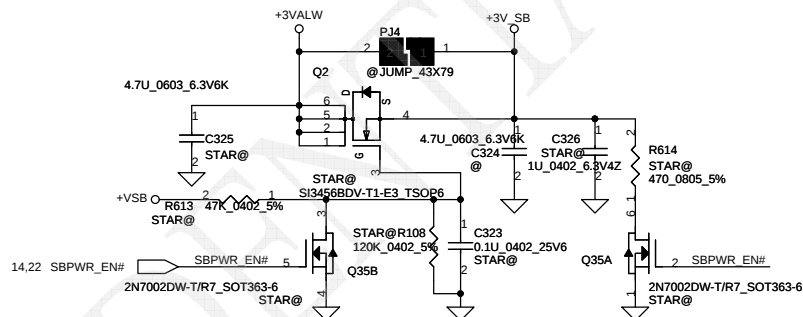
+5VALW TO +5VS



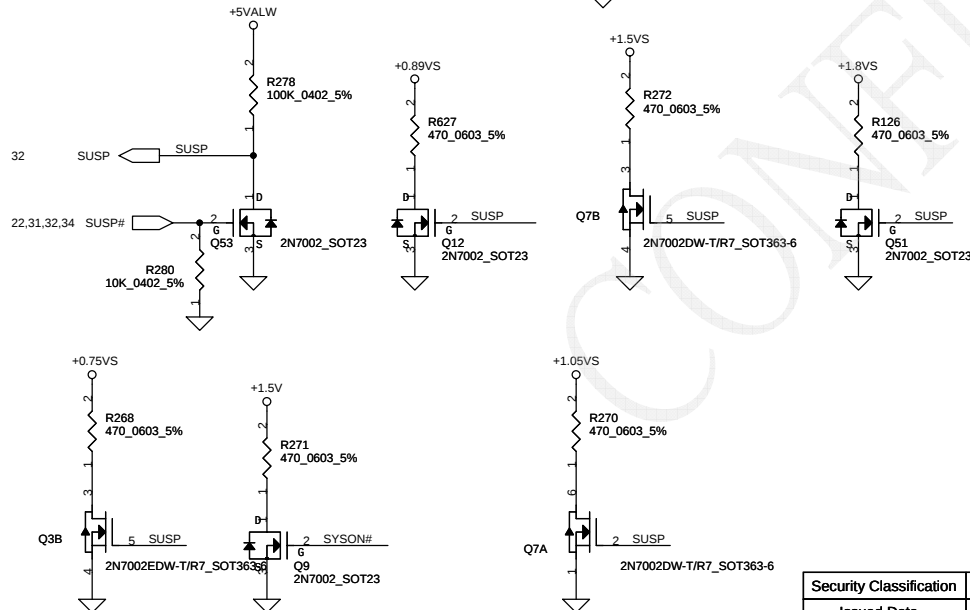
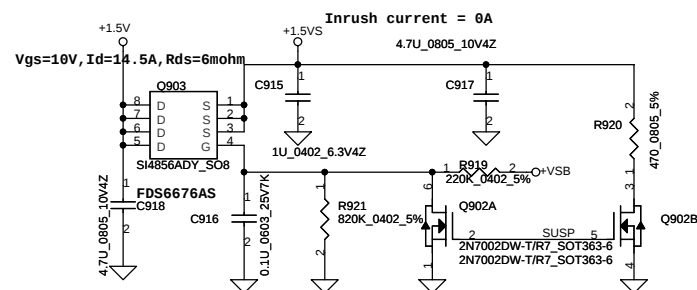
+3VALW TO +3V_LAN



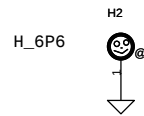
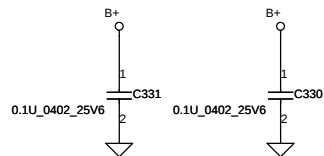
+3VALW TO +3V_SB



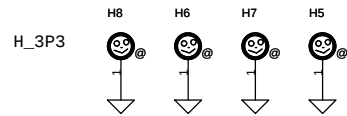
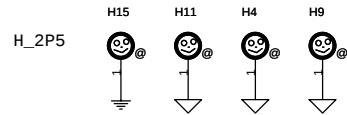
+1.5V to +1.5VS



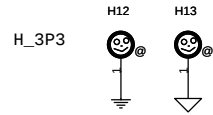
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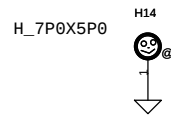
02/12 H2 change to H_6P6



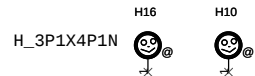
01/06 H_3P8 change to H_3P3



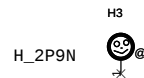
01/06 H_3P1 change to H_3P3



02/12 H_7P0X5P0N change to H_7P0X5P0



01/06 Add a H_3P1X4P1N



01/06 H_2P9N change to H_2P7N

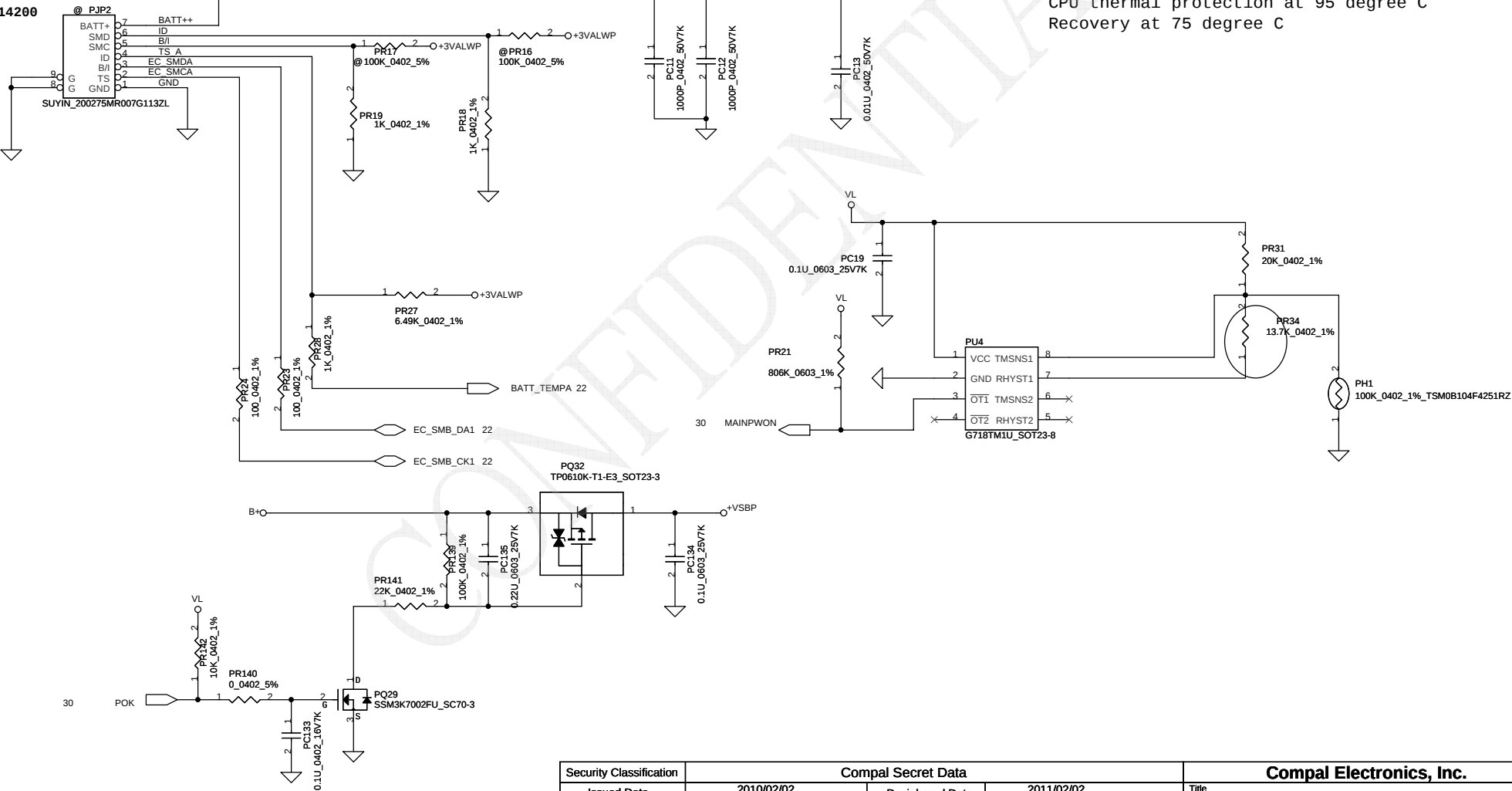
03/11 H_2P7N change to H_2P9N



FIDUCIAL_C40M80

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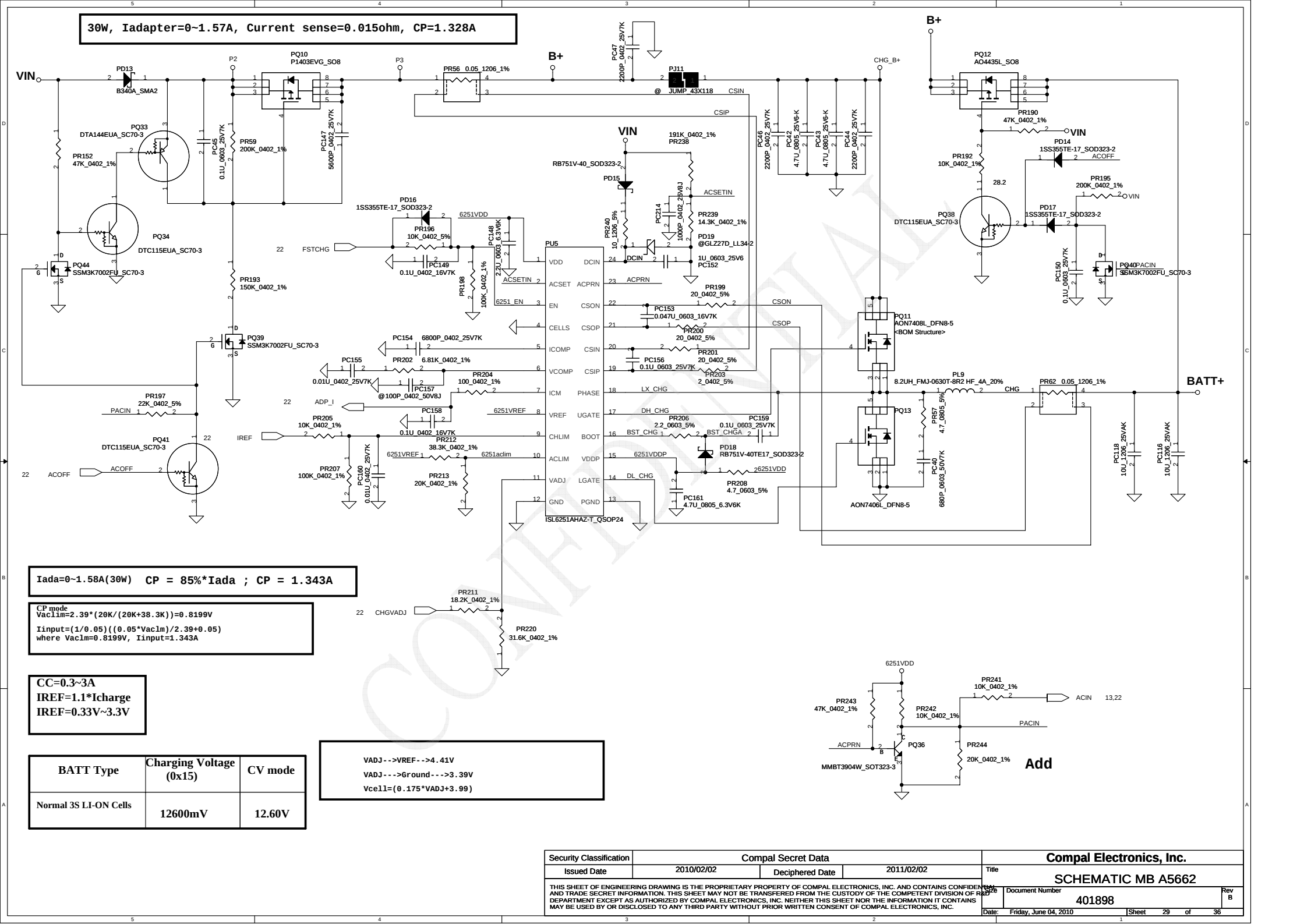
DC040014200



PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 75 degree C

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30W, Iadapter=0~1.57A, Current sense=0.015ohm, CP=1.328A



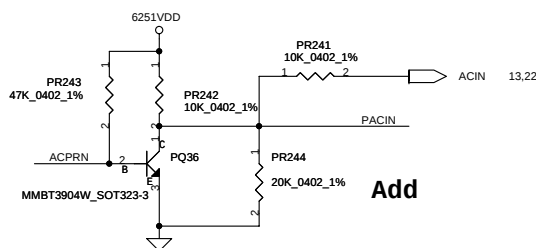
Iada=0~1.58A(30W) CP = 85%*Iada ; CP = 1.343A

CP mode
 $V_{ac1m} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1/0.05) * ((0.05 * V_{ac1m}) / (2.39 + 0.05))$
 where $V_{ac1m} = 0.8199V$, $I_{input} = 1.343A$

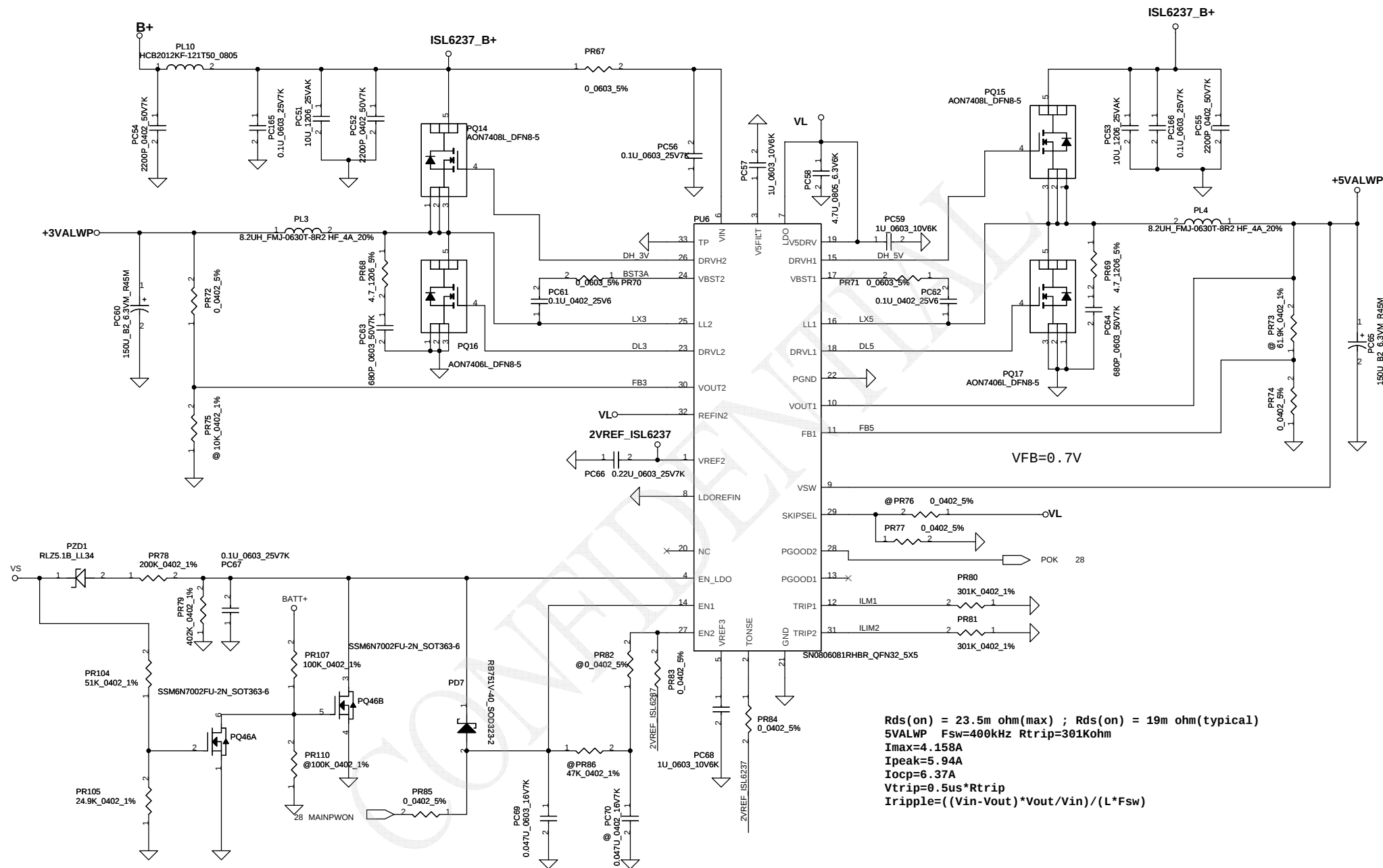
CC=0.3~3A
 $I_{REF} = 1.1 * I_{charge}$
 $I_{REF} = 0.33V \sim 3.3V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

VADJ-->VREF-->4.41V
 VADJ-->Ground-->3.39V
 $V_{cell} = (0.175 * VADJ + 3.99)$



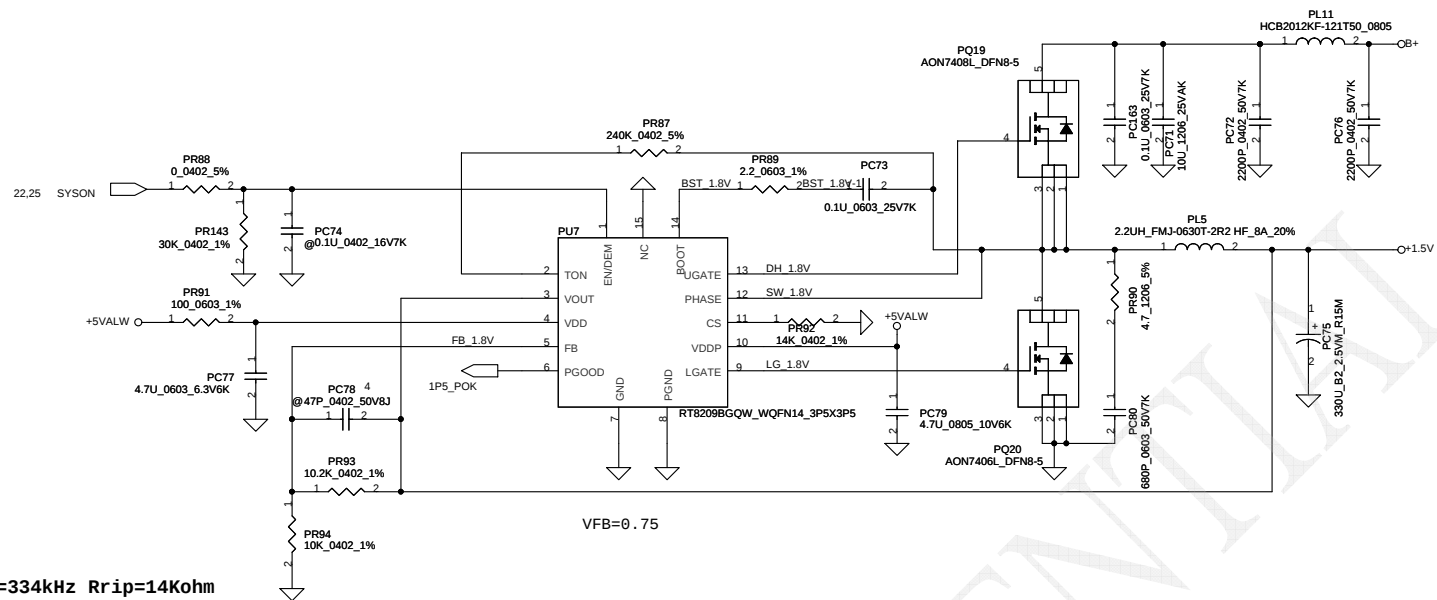
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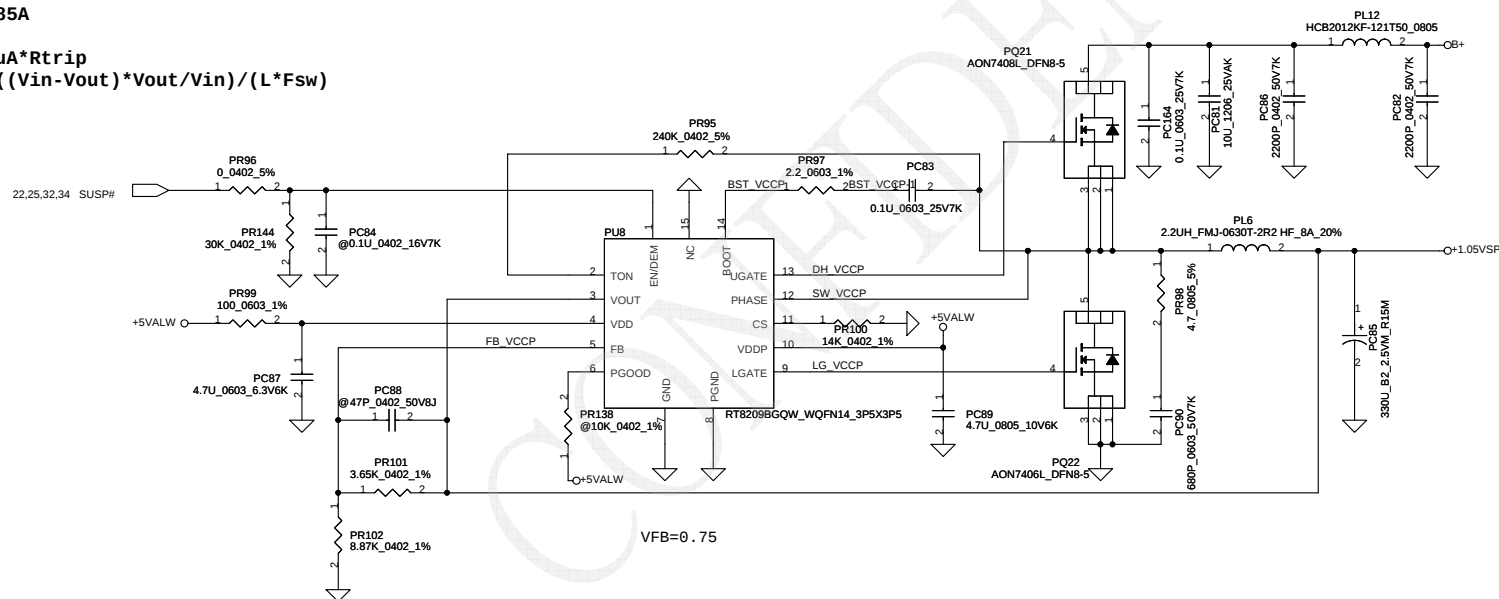
$R_{ds(on)} = 23.5m \text{ ohm(max)} ; R_{ds(on)} = 19m \text{ ohm(typical)}$
 $5VALWP \text{ Fsw}=400kHz \text{ Rtrip}=301Kohm$
 $I_{max}=4.158A$
 $I_{peak}=5.94A$
 $I_{ocp}=6.37A$
 $V_{trip}=0.5us \cdot R_{trip}$
 $I_{ripple}=(V_{in}-V_{out}) \cdot V_{out}/V_{in} / (L \cdot F_{sw})$

$R_{ds(on)} = 23.5m \text{ ohm(max)} ; R_{ds(on)} = 19m \text{ ohm(typical)}$
 $3.3VALWP \text{ Fsw}=300kHz \text{ Rtrip}=301K$
 $I_{max}=4.319A$
 $I_{peak}=6.17A$
 $I_{ocp}=6.43A$
 $V_{trip}=0.5us \cdot R_{trip}$
 $I_{ripple}=(V_{in}-V_{out}) \cdot V_{out}/V_{in} / (L \cdot F_{sw})$

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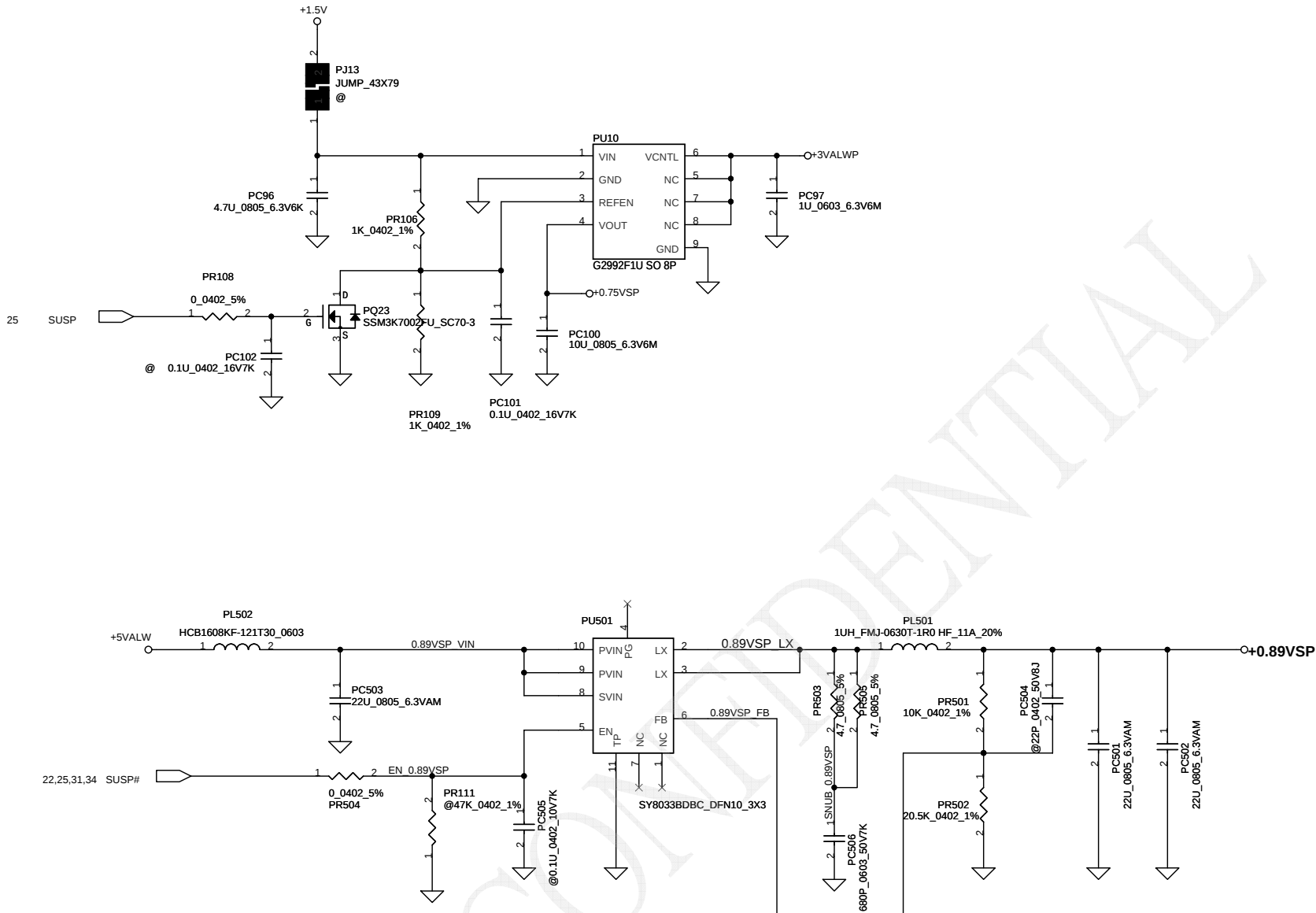


1.5VP Fsw=334kHz Rrip=14Kohm
 Imax=4.795A
 Ipeak=6.85A
 Iocp=6A
 Vtrip=10uA*Rtrip
 Irripple=((Vin-Vout)*Vout/Vin)/(L*Fsw)

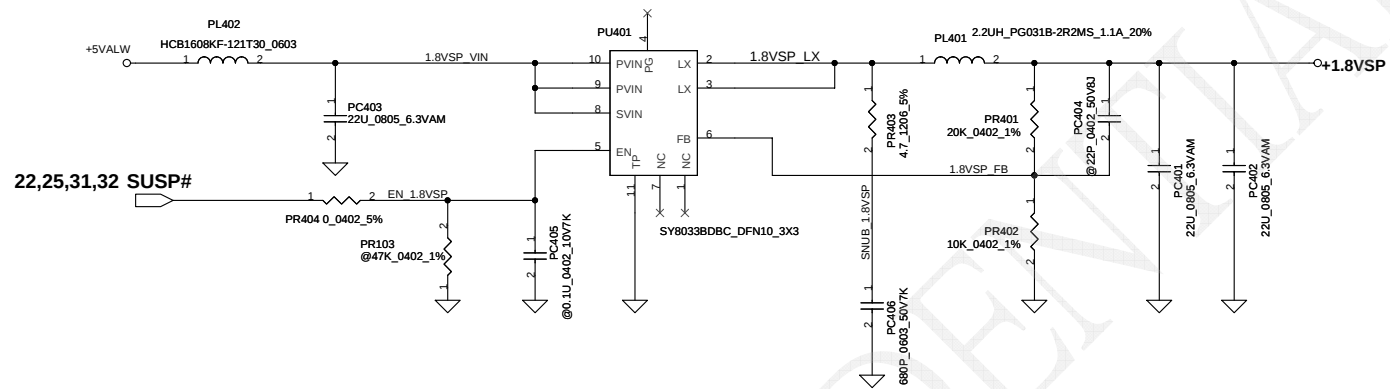


VCCPP(1.05V) Fsw=338kHz Rrip=14Kohm
 Imax=2.4493A
 Ipeak=3.499A
 Iocp=6.01A
 Vtrip=10uA*Rtrip
 Irripple=((Vin-Vout)*Vout/Vin)/(L*Fsw)

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$<V_o=1.8V>$ $V_{FB}=0.6V$
 $V_o=V_{FB} \cdot (1+PR401/PR402)=0.6 \cdot (1+40.2K/20K)=1.806V$
 $I_{peak}=2.64A$, $I_{max}=1.848A$

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Page	Reason for change	Modify list
28	DFX issue	PQ39 from SB000006800 to SB000009610
29	DFX issue	PQ29、PQ40、PQ44 from SB000006800 to SB000009610
32	DFX issue	PQ23 from SB000006800 to SB000009610
28	let PH1 and PH4 use the same material	PH1 from SL200000V00 to SL200000U00
29	Improve switching ability	PQ13 from A0N7408 to A0N7406
32	SY8033 design change	PL501 from 2R2 to 1R0 PR501 from 121k to 12.1k PR502 from 249k to 24.9k
34	SY8033 design change	PR401 from 40.2k to 20k, PR402 from 20k to 10k

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PIR (Product Improve Record)

SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1--> 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/29	P.23	Mount C136,C149,C160,C159,C146,C168,C135,C155,C171,C133,C148,C170 C132,C147,C158,C169,C131,C157,C145,C166,C144,C134,C167,C156	For EMI request.
2	3/29	P.5	Remove R906,Q901,R905,C913,R907,C914 Mount R903	For EMI request.
3	5/7	P.25	change C291 from 0.01u to 0.022u	For design change.

PINEVIEW-M



PINEVIEW-M_FCBGA8559
N475R1@

PINEVIEW-M



PINEVIEW-M_FCBGA8559
N455R3@

PINEVIEW-M



PINEVIEW-M_FCBGA8559
N475R3@

TGP



TIGERPOINT_ES1_BGA360
R3@

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