Compal Confidential

NCL20 ULV M/B Schematics Document

Intel Penryn Processor with Cantiga SFF + DDRIII + ICH9M SFF

2009-10-08

REV:0.4

Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

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Title	Cover Page	
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Compal confidential
File Name : LA-5631P

LS5631P I/O Board
LS5632P C/R Board
LS5633P LED Board
LS5634P SW Board
LS5635P TP/B Board
LS5636P ODD/B Board

Mobile Penym
LV/ULV Dual Core
uFCPGA-956 CPU - SFF
page 4,5,6,7

H_A#(3..35)
H_D#(0..63)
FSB
667/800/1066MHz 1.05V

Thermal Sensor
EMC1402-1-ACZL
page4

CK505
Clock Generator
ICS9LPRS387
page 19

HDMI Conn.
page25

LCD CONN.
page 17

CRT CONN.
page 18

Level shift

LVDS

TMDS

Intel Cantiga GS45
FCBGA 1363 - SFF
page 8,9,10,11,12,13

DDR3 800MHz 1.5V
Dual Channel

DDR3
SO-DIMM X2
page 14,15

DMI X4

IO board

PCI-Express

Intel ICH9-M
WBMMAP-569 - SFF
page 19,20,21,22

USB conn x2
page 28

Bluetooth
conn
page 28

CMOS
Camera 1.3M
page23

3.3V 48MHz
USB

3.3V 24.576MHz/48Mhz
HD Audio

USB conn x1

MINI Card x1
3G

MINI Card x1
WLAN
page 27

LAN ATHEROS
AR8131L
page 24

SIM CONN.

RJ45 LAN
connector
page 25

S-ATA

port 0

HDD
connector
page 23

port 1

CDROM
connector
page 23

LPC BUS

ENE KB926 D2
page 29

HDA Codec
ALC269X-GR
page 32

Card Reader
RTS5159-GR
page23

IO board

SPEAKER
page 33

Audio Jack
page 33

Touch Pad
page 30

Int.KBD
page 30

BIOS
page 30

RTC CKT.
page 24

Power On/Off CKT.
page 32

DC/DC Interface CKT.
page 35

Power Circuit DC/DC
page 36~~42

IO/B Conn.
page 29

TP/B Conn.
page 31

Speaker Conn.
page 31

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Title: **Block Diagram**

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
		ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

ICH9M SMBUS Address

Device	HEX	Address
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (ICS9LPRS387, SLG8SP556V)	D2	1 1 0 1 0 0 1 0

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

USB table

EHCI1	UHCI1	Port0	MB USB Conn1.
		Port1	MB USB Conn2.
	UHCI2	Port2	sub board
		Port3	WLAN
	UHCI3	Port4	Card Reader
		Port5	3G
EHCI2	UHCI4	Port6	BT
		Port7	CMOS Camera
	UHCI5	Port8	
		Port9	
	UHCI6	Port10	
		Port11	

PCIE table

PCIE port1	3G Card
PCIE port2	Wireless Card
PCIE port3	GLAN
PCIE port4	
PCIE port5	
PCIE port6	

SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

zzz1

PCB-MB

DA80000GO00

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Title: Notes List

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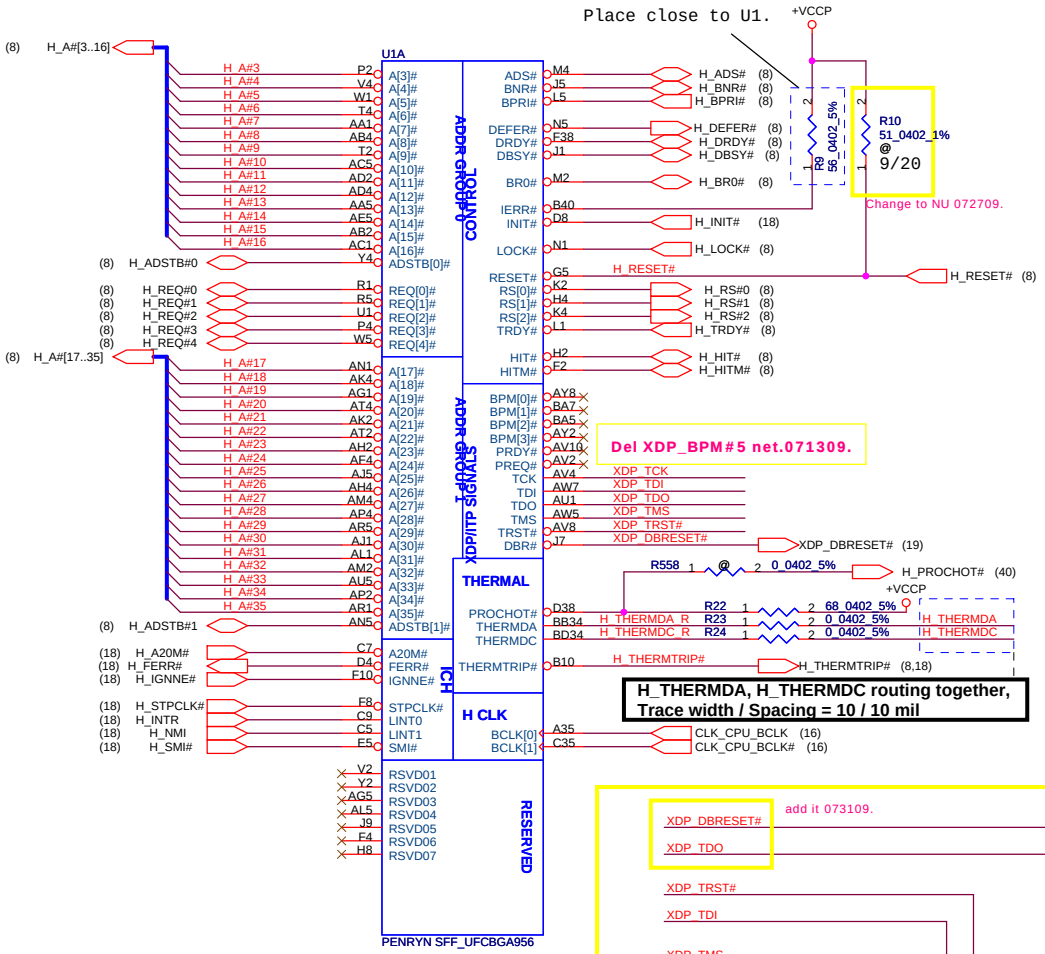

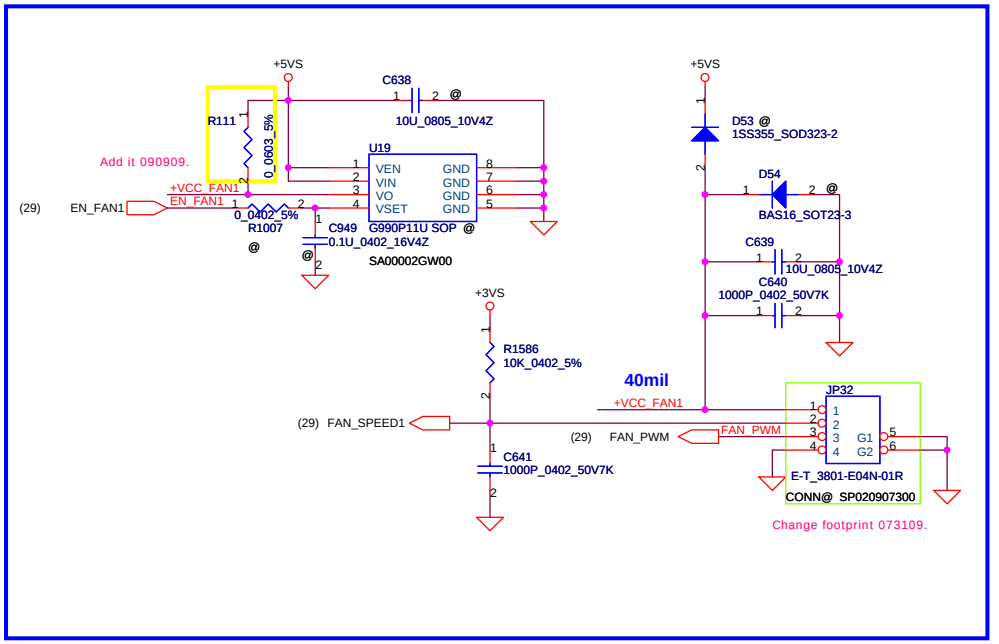

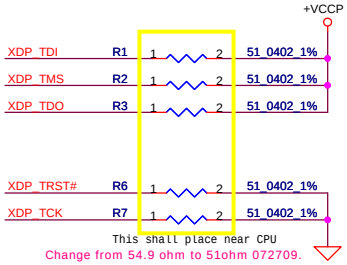

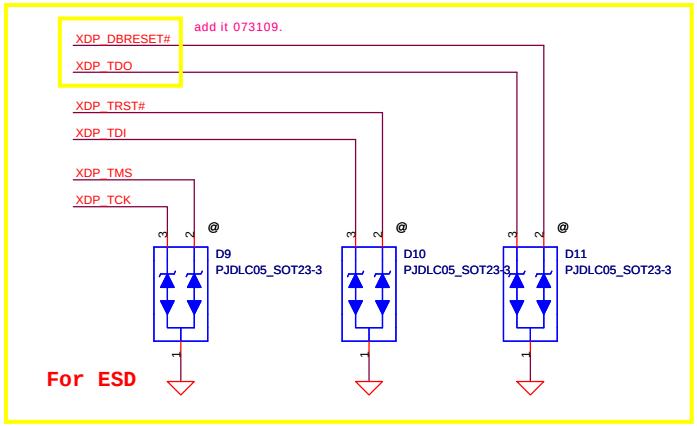

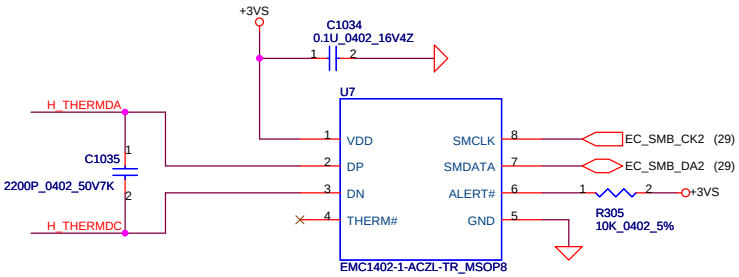

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Title: Penryn (1/3) & FAN

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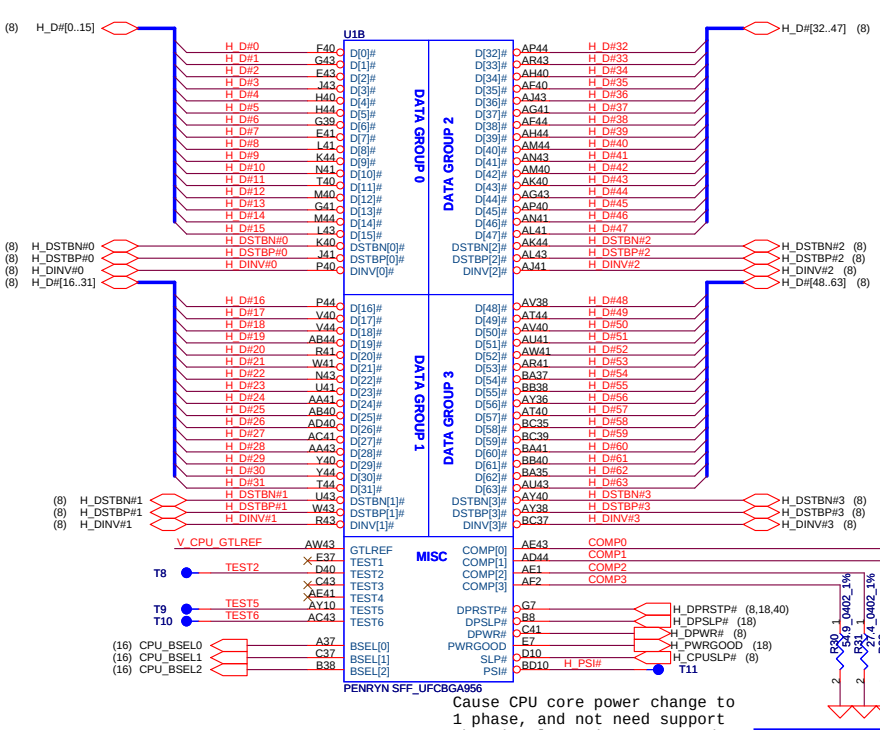
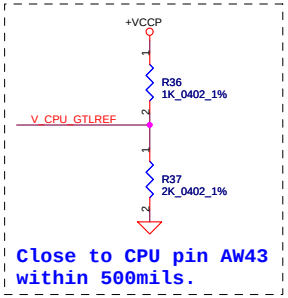


Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

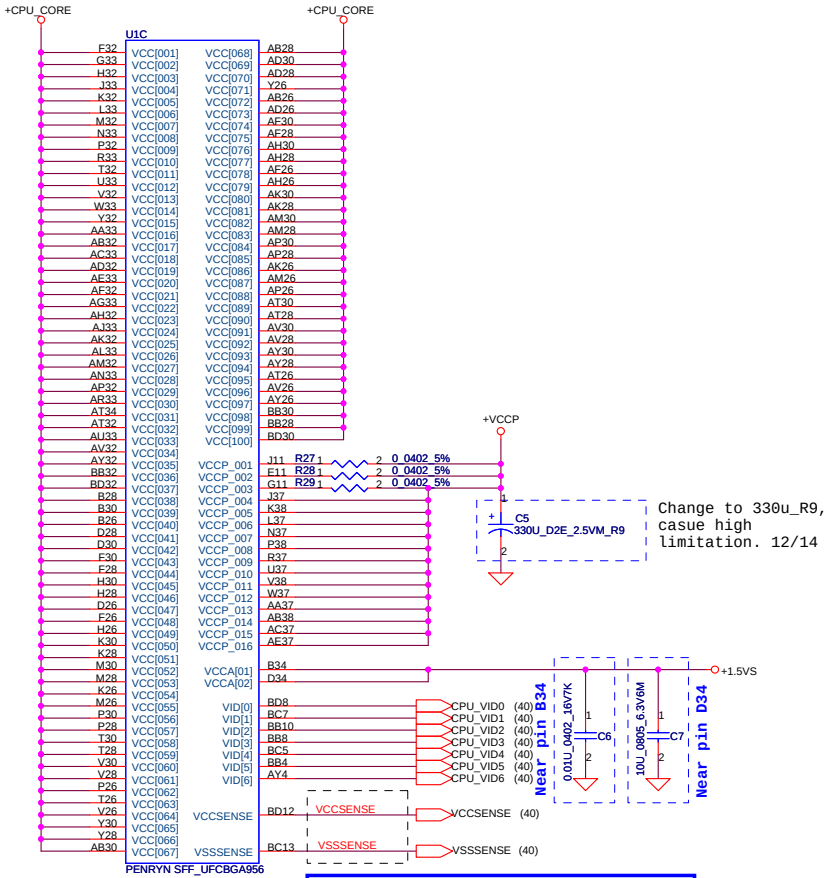
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

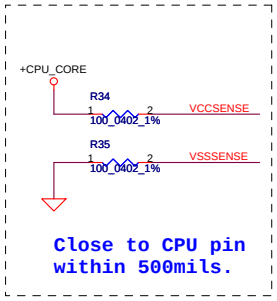
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Close to CPU pin AW43 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

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Title: **Penryn(2/3)-AGTL+/ITP-XDP**

Size: Custom | Document Number: **NCL20 M/B LA-5631P Schematic** | Rev: 0.1

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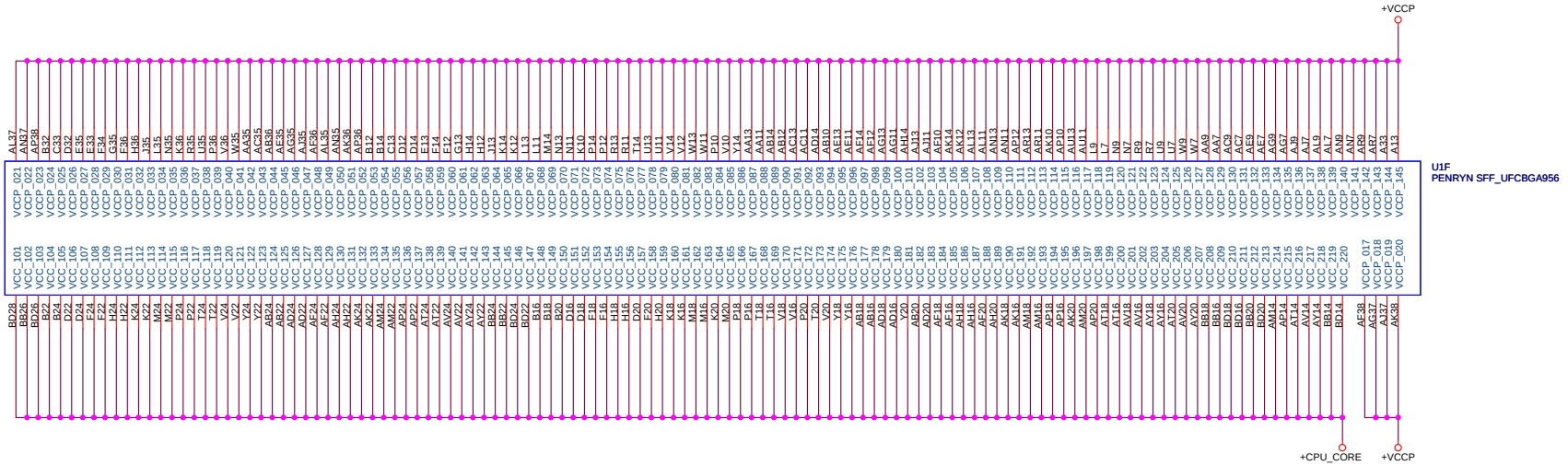

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Compal Electronics, Inc.

Title: **Penryn(3/3)-Power**

Size	Document Number	Rev
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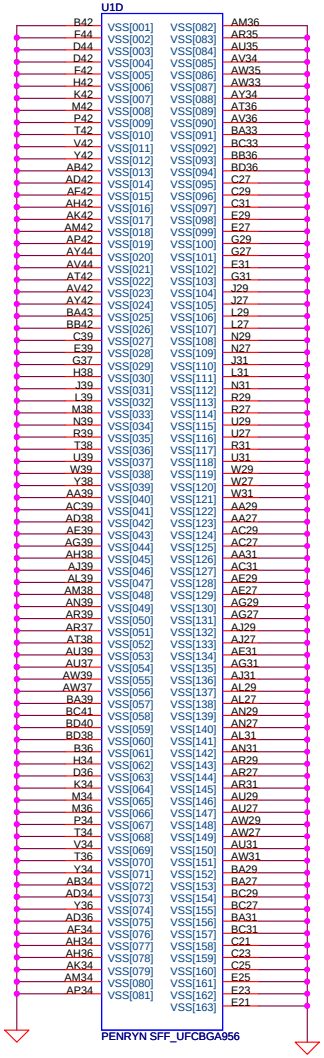

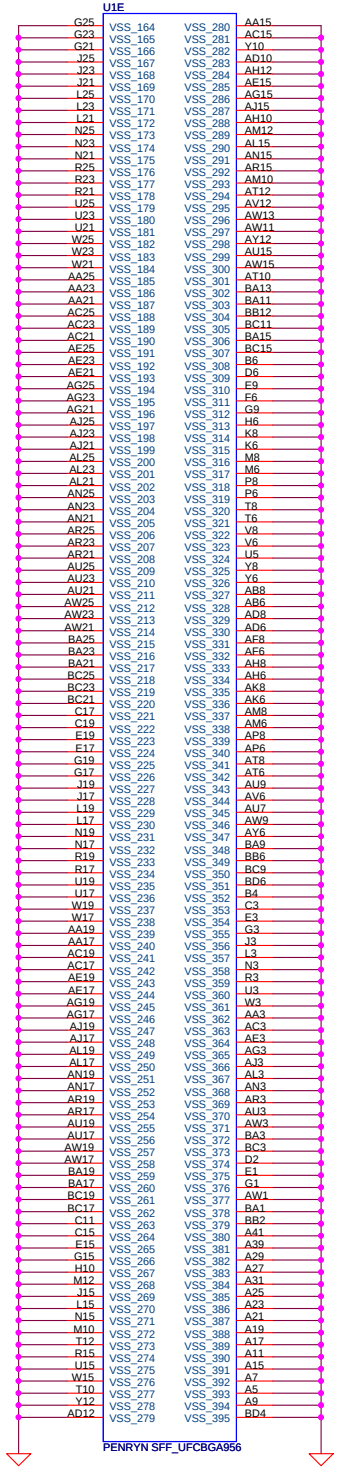

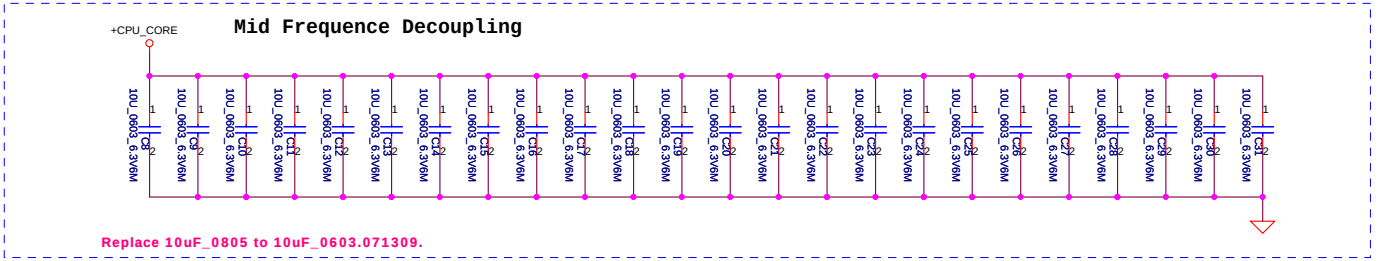

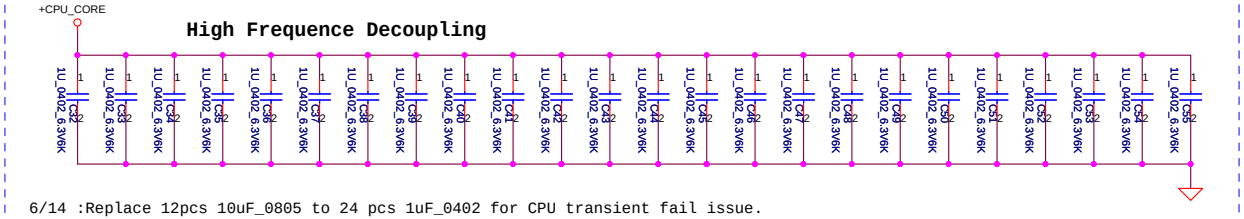

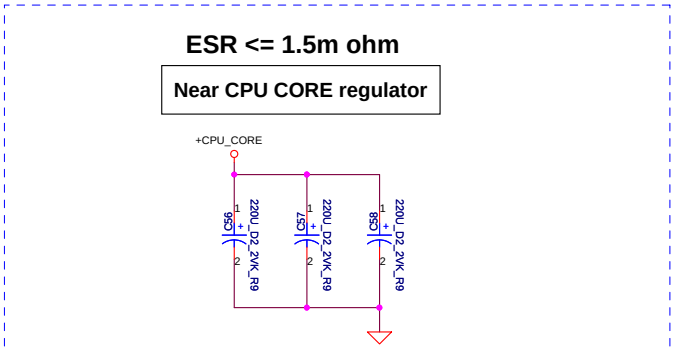

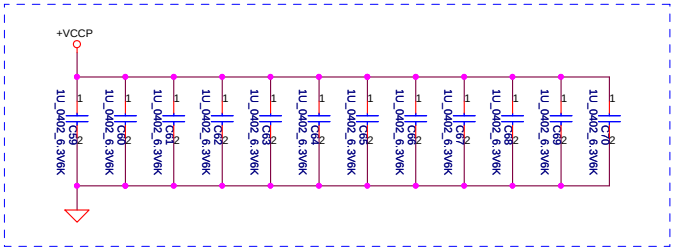

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Title: **Penryn(3/3)-GND/Bypass**

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Add them for Boundary Scan. 10/23

Trace < = 500mils

layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

Near B6 pin

layout note:
Place them close to U4 pin BC51.

Layout Note: V_DDR_MCH_REF trace width and spacing is 20/20.

Add R428 in 9/26

Modify in 9/26

add it.062309

Refer to spec. pull low 100k.062909

Change from 511 to 499.070709.

add it for change to use DDR3.070309

CANTIGA GMCH SFF_FCBGA1363

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Title: Cantiga(1/6)-AGTL/DMI/DDR

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

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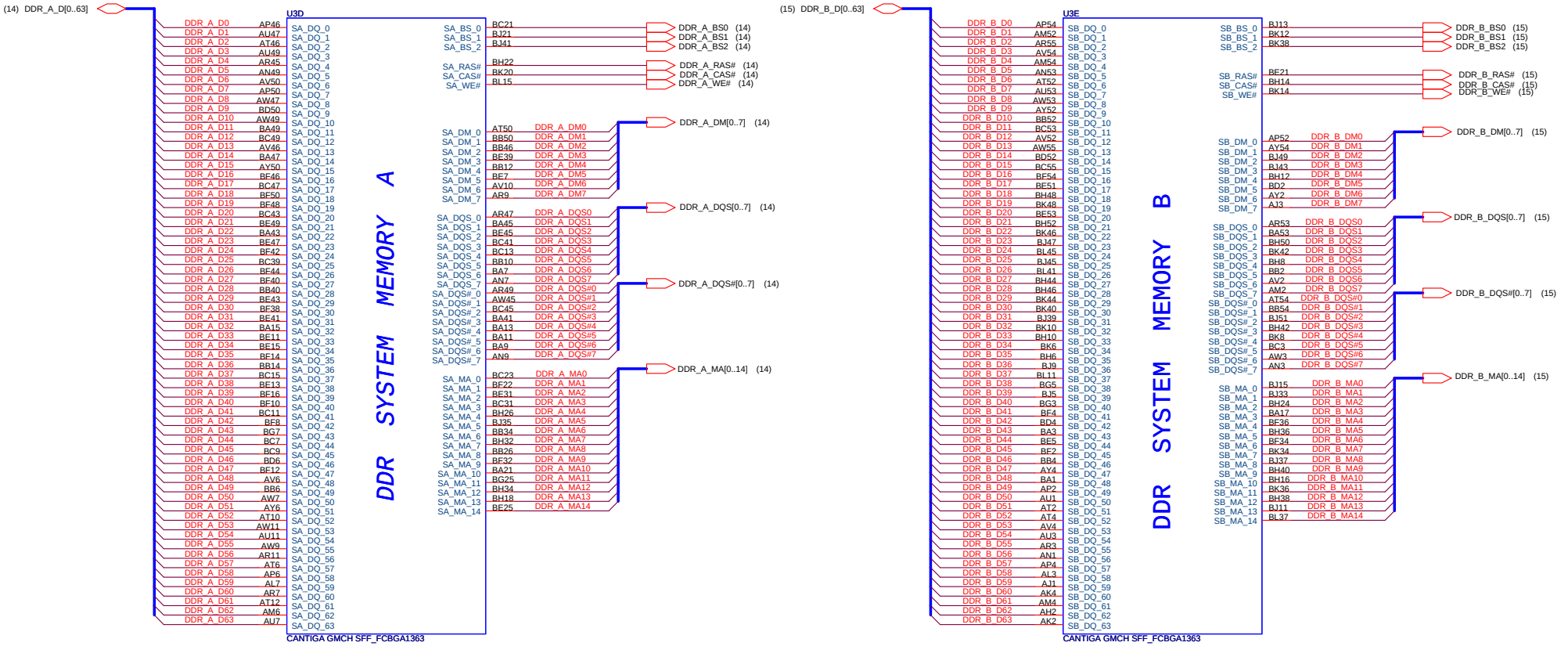

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Title: **Cantiga(2/6)-DDR2 A/B CH**

Size	Document Number	Rev
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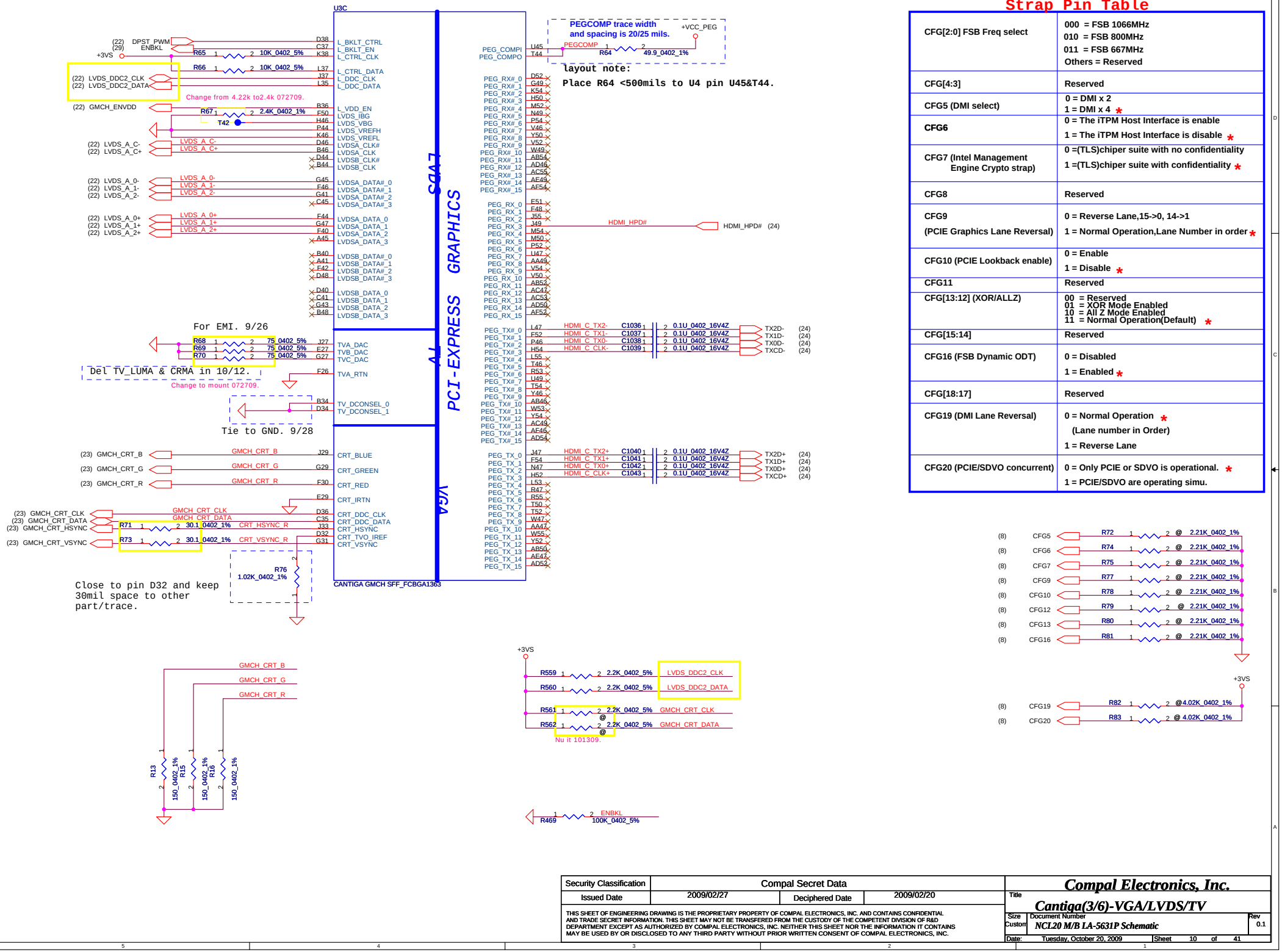

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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Title: Cantiga(3/6)-VGA/LVDS/TV

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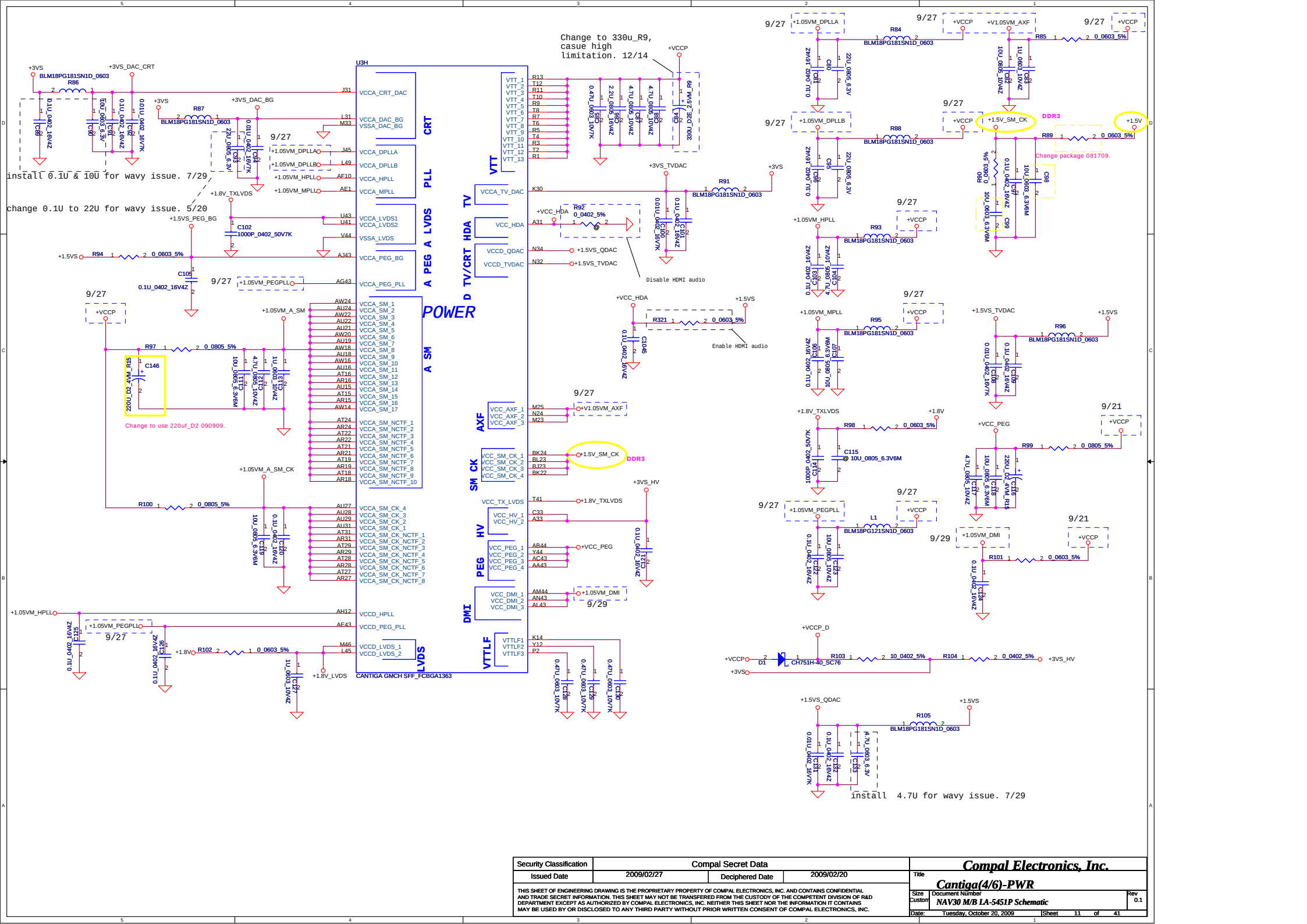

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Title: Cantiga(4/6)-PWR

Size: Custom | Document Number: NAV30 M/B LA-5451P Schematic | Rev: 0.1

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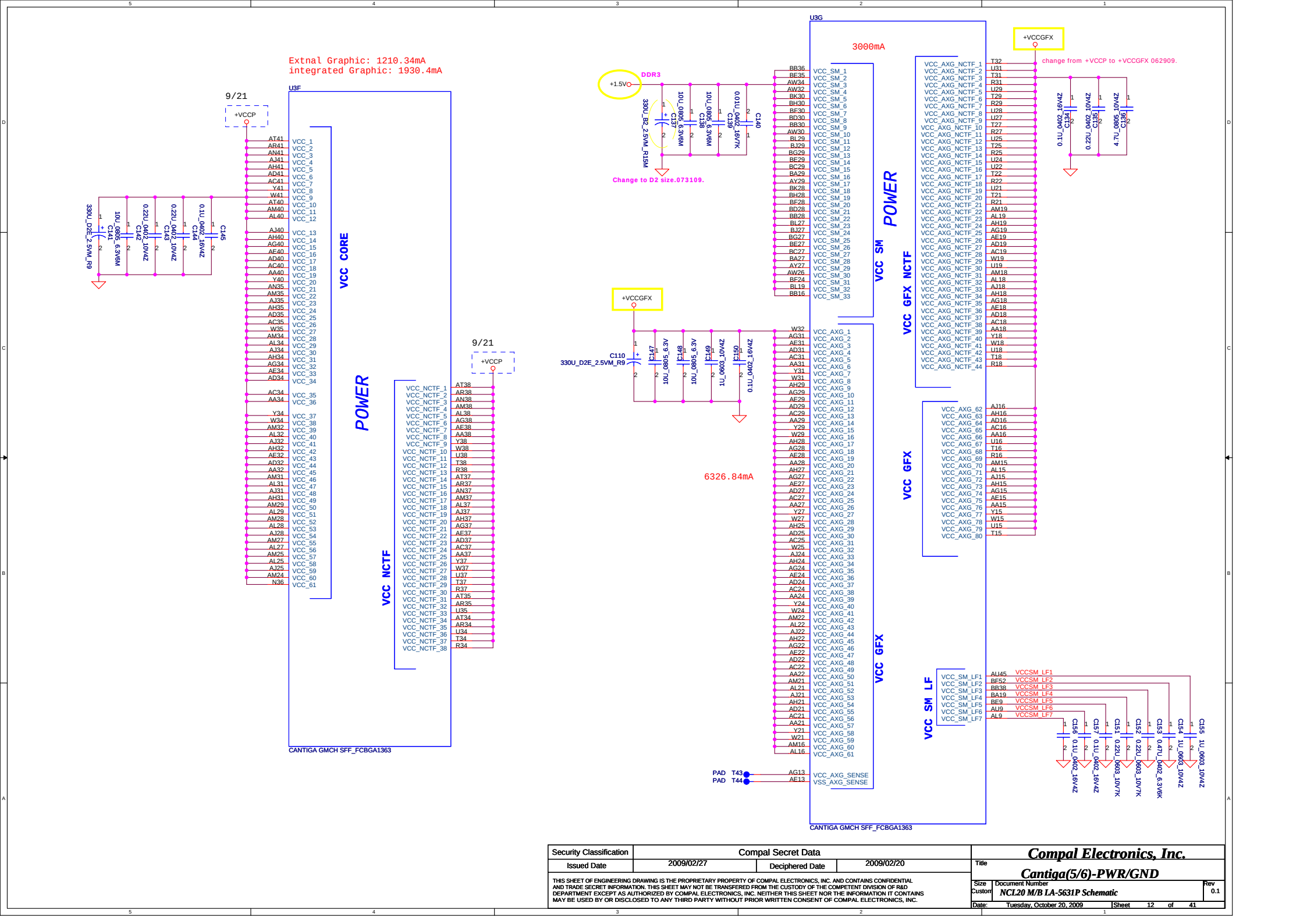

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Title: **Cantiga(5/6)-PWR/GND**

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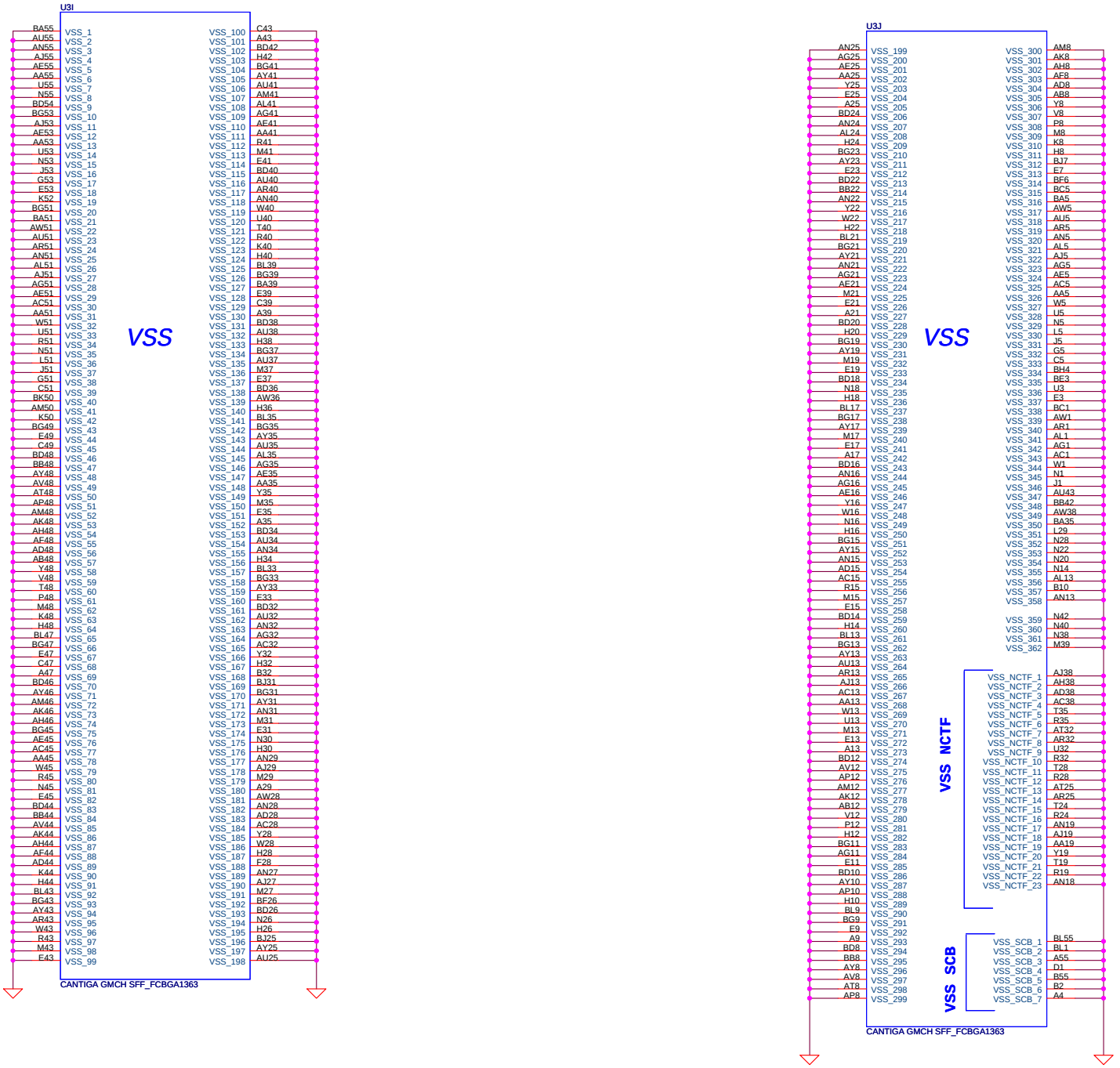

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Title: **Cantiga(6/6)-PWR/GND**

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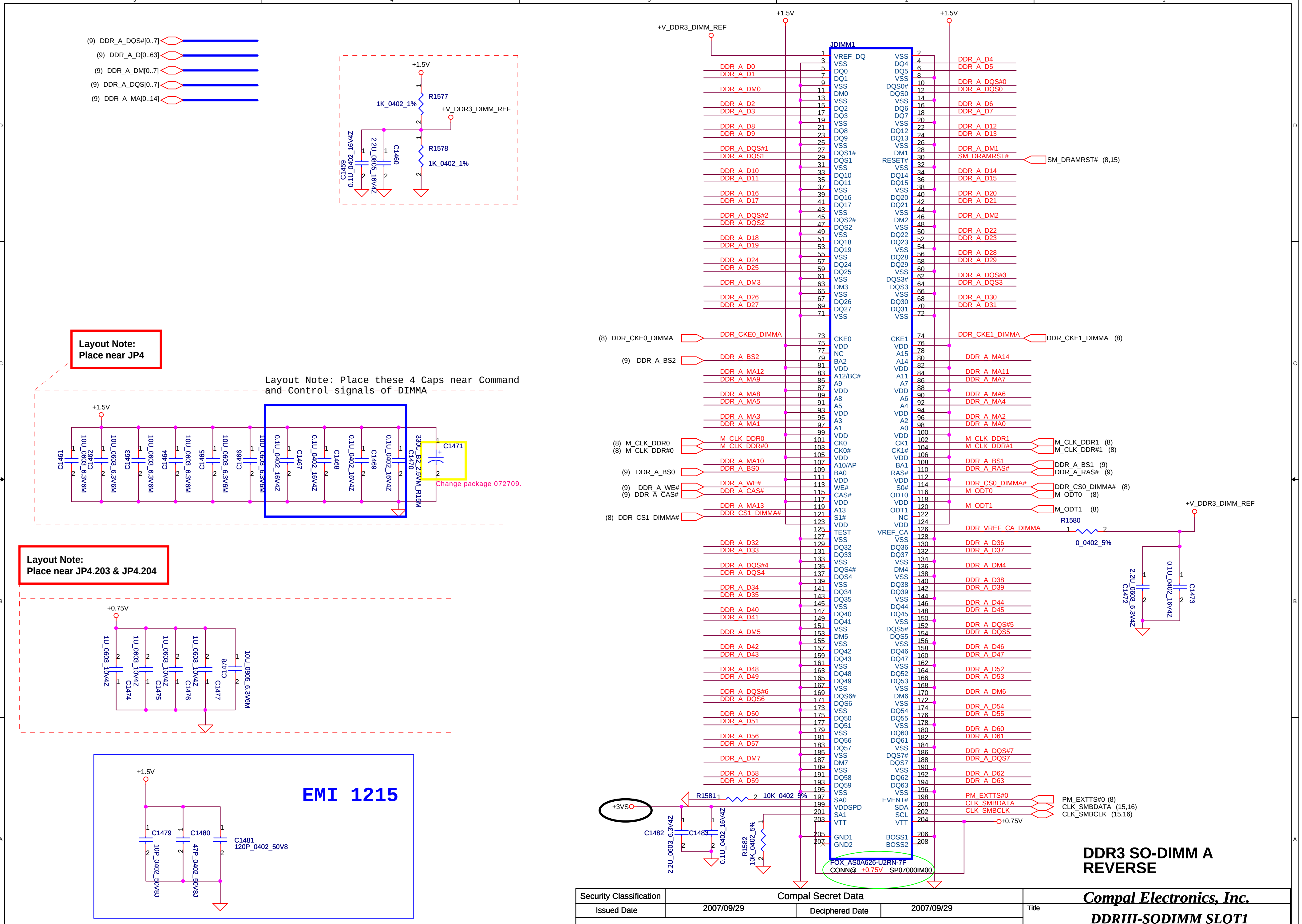

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Title: **DDRIII-SODIMM SLOT1**

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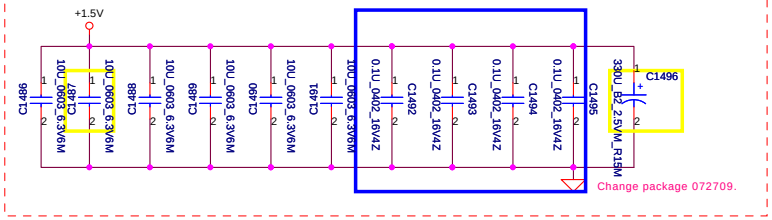
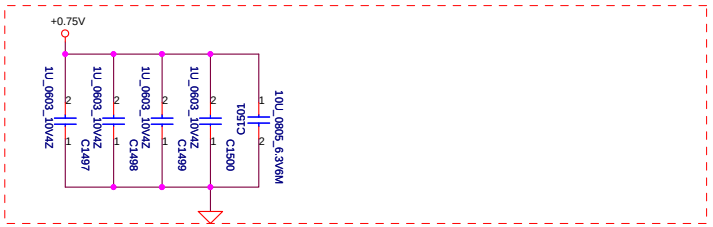
(9) DDR_B_DQS#[0..7]
(9) DDR_B_D[0..63]
(9) DDR_B_DM[0..7]
(9) DDR_B_DQS[0..7]
(9) DDR_B_MA[0..14]

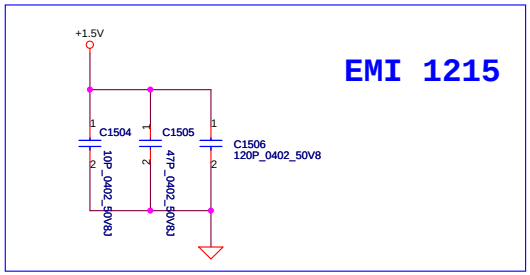
Layout Note:
Place near JDIMM2

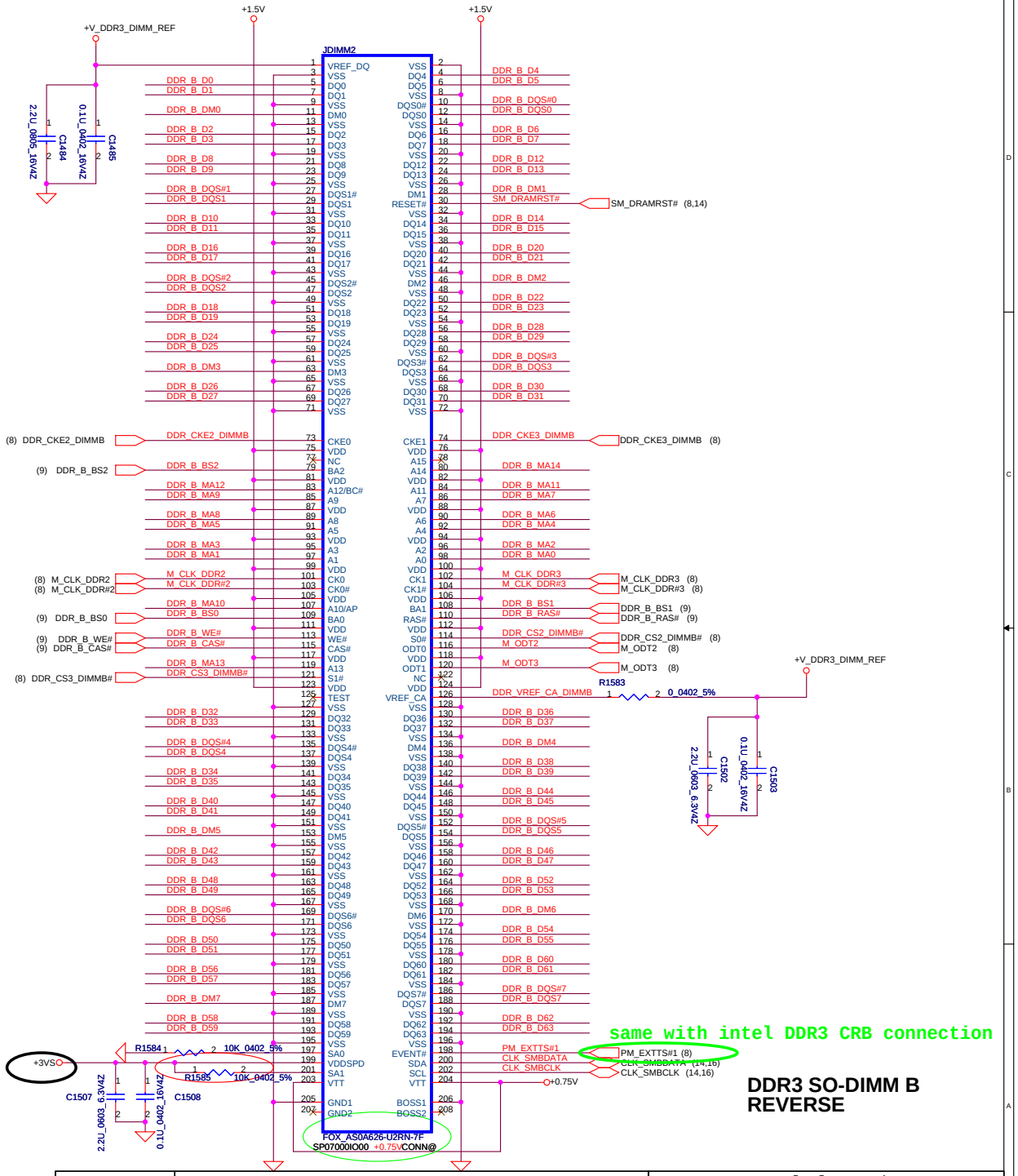
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM2.203 & JDIMM2.204







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Title: DDRIII-SODIMM SLOT2

Size	Document Number	Rev
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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS R343 10K_0402_5% CLK_PCI2

CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

R344 @10K_0402_5% **mount to Enable ITP_CLK**

add it.073109

+3VS @R379 10K_0402_5%

R345 10K_0402_5% CLK_PCI5

CLK_PCI5=0, Pin63,64 is SRC_CLK

CLK_PCI5=1, Pin63,64 is ITP_CLK

+3VS @R380 10K_0402_5%

R346 10K_0402_5% CLK_PCI4

CLK_PCI4=0, Pin28, 29 is SRC_CLK Pin24, 25 is DOT96_CLK

+3VS R342 10K_0402_5% @ CK505_PWRGD

Q3 2N7002_SOT23 @ CLKEN# (40)

R347 @10K_0402_5% CK_PWRGD

+VCCP R352 @56_0402_5%

R353 2.2K_0402_5% R354 1K_0402_5% CLKSEL0 MCH_CLKSEL0 (8)

R356 @1K_0402_5% R357 0_0402_5% CPU_BSEL0 (5)

+VCCP R360 @1K_0402_5%

R361 1K_0402_5% CLKSEL1 MCH_CLKSEL1 (8)

R366 @0_0402_5% R367 0_0402_5% CPU_BSEL1 (5)

<BOM Structure>

+VCCP R372 @1K_0402_5%

R373 10K_0402_5% R374 1K_0402_5% CLKSEL2 MCH_CLKSEL2 (8)

R375 @0_0402_5% R376 0_0402_5% CPU_BSEL2 (5)

+VCCP +CLK_VDDSRC

L2 FBMA-L11-201209-221LMA30T_0805

C1102 10U_0805_10V4Z C1109 0.1U_0402_16V4Z

C1455 47P_0402_50V8J @ C1103 10U_0805_10V4Z C1104 C1105 C1106 C1107 C1108 0.1U_0402_16V4Z

add it.071109

+3VS L3 FBMA-L11-201209-221LMA30T_0805 +CLK_VDD

C1110 10U_0805_10V4Z C1117 0.1U_0402_16V4Z

C1456 47P_0402_50V8J @ C1111 10U_0805_10V4Z C1112 C1113 C1114 0.1U_0402_16V4Z

add it.071109

+1.5VS +CLK_VDD

R1551 0_0603_5% +1.5VSCLK_VDD

R1552 @ 0_0603_5% 0.1U_0402_16V4Z

C1450 C1451 C1452 C1453

10U_0603_6.3V6M 0.1U_0402_16V4Z 0.1U_0402_16V4Z

add it.062309

+CLK_VDDSRC R1563 0_0603_5%

+1.5VSCLK_VDD R1564 @ 0_0603_5% C1454 0.1U_0402_16V4Z

(19) H_STP_CPU# H_STP_CPU#

(19) H_STP_PCI# H_STP_PCI#

(29) CLK_PCI_LPC CLK_PCI_LPC R348 33_0402_5% CLK_PCI3

(17) CLK_PCI_ICH CLK_PCI_ICH R349 33_0402_5% CLK_PCI5

(19) CK_PWRGD (8,19,40) VGATE 0_0402_5% R350 0_0402_5% @ R351 CK505_PWRGD

C1120 22P_0402_50V8J 22P_0402_50V8J Y3 14.31818MHz_20P_FSX8L14.318181M20FDB C1121

Change to use 22pf.091509

CLK_XTALIN CLK_XTALOUT

(19) CLK_ICH_48M (30) CLK_SD_48M CLK_ICH_48M R355 CLK_SD_48M R358 @ 33_0402_5% 22_0402_5% CLKSEL0 CLKSEL1

(19) CLK_ICH_14M CLK_ICH_14M R359 33_0402_5% CLKSEL2

C1289 10P_0402_50V8J @ C1286 10P_0402_50V8J @ C1284 @

add it for EMI.072409.

+3VS R362 4.7K_0402_5% +3VS

(19,28) ICH_SMBDATA 2N7002DW-T/R7_SOT363-6 Q4A CLK_SMBDATA

+3VS R369 4.7K_0402_5% +3VS

(19,28) ICH_SMBCLK Q4B 2N7002DW-T/R7_SOT363-6 CLK_SMBCLK

U27

ICS9LPRS387, PN:SA000020H10
SLG8SP556V, PN:SA000020K00

VDDREF	6		
VDD48	19		
VDDCPU	72		
VDDPCI	12		
VDDPLL3	27		
VDDSRC	55		
VDDSRC_IO	52		
VDDSRC_IO	38		
VDDSRC_IO	62		
VDDPLL3_IO	31		
VDDCPU_IO	66		
VDD96_IO	23		
CPU_STOP#	53		
PCI_STOP#	54		
PCI1	13		
PCI2/TME	14		
PCI3	15		
PCI4/27_SELECT	16		
PCI_F5/ITP_EN	17		
CK_PWRGD/PD#	1		
X1	5		
X2	4		
NC	11		
USB_48MHz/FSLA	20		
FSLB/TEST_MODE	2		
FSLC/TEST_SEL/REF0	7		
REF1	8		
GNDCPU	69		
GNDREF	3		
GNDPCI	18		
GND48	22		
GND	30		
GND	26		
GNDSRC	34		
GNDSRC	59		
GNDSRC GND_THERMAL_PAD	42 73		
SDATA	9	CLK_SMBDATA	CLK_SMBDATA (14,15)
SCLK	10	CLK_SMBCLK	CLK_SMBCLK (14,15)
CPUT0_LPR_F	71	CLK_CPU_BCLK	CLK_CPU_BCLK (4)
CPUC0_LPR_F	70	CLK_CPU_BCLK#	CLK_CPU_BCLK# (4)
CPUT1_LPR_F	68	CLK_MCH_BCLK	CLK_MCH_BCLK (8)
CPUC1_LPR_F	67	CLK_MCH_BCLK#	CLK_MCH_BCLK# (8)
SRCT0_LPR/DOTT_96_LPR	24	CLK_DREF_96M	CLK_DREF_96M (8)
SRCC0_LPR/DOTC_96_LPR	25	CLK_DREF_96M#	CLK_DREF_96M# (8)
27MHz_NonSS/SRCT1_LPR/SE1	28	CLK_DREF_SSC	CLK_DREF_SSC (8)
27MHz_SS/SRCC1_LPR/SE2	29	CLK_DREF_SSC#	CLK_DREF_SSC# (8)
SRCT2_LPR/SATAT_LPR	32	CLK_PCIE_SATA	CLK_PCIE_SATA (18)
SRCC2_LPR/SATAC_LPR	33	CLK_PCIE_SATA#	CLK_PCIE_SATA# (18)
SRCT3_LPR	35	CLK_PCIE_ICH	CLK_PCIE_ICH (19)
SRCC3_LPR	36	CLK_PCIE_ICH#	CLK_PCIE_ICH# (19)
SRCT4_LPR	39	CLK_PCIE_WWAN	CLK_PCIE_WWAN (28)
SRCC4_LPR	40	CLK_PCIE_WWAN#	CLK_PCIE_WWAN# (28)
SRCT6_LPR	57	CLK_MCH_3GPLL	CLK_MCH_3GPLL (8)
SRCC6_LPR	56	CLK_MCH_3GPLL#	CLK_MCH_3GPLL# (8)
SRCT7_LPR	61		
SRCC7_LPR	60		
CPUT2_ITP_LPR/SRCT8_LPR	64		
CPUC2_ITP_LPR/SRCC8_LPR	63		
SRCT9_LPR	44	CLK_PCIE_MINI2	CLK_PCIE_MINI2 (28)
SRCC9_LPR	45	CLK_PCIE_MINI2#	CLK_PCIE_MINI2# (28)
SRCT10_LPR	50		
SRCC10_LPR	51		
SRCT11_LPR	48	CLK_PCIE_LAN	CLK_PCIE_LAN (28)
SRCC11_LPR	47	CLK_PCIE_LAN#	CLK_PCIE_LAN# (28)
CR#3	37		
CR#4	41		
CR#6	58		
CR#7	65		
CR#9	43		
CR10#	49		
CR#11	46		
CR#A	21		

ICS9LPRS387BKLFT_MLF72_10x10

RAM **CPU** **NB** **NB** **NB_SSC** **SATA** **ICH** **WWAN** **3G_PLL**

UMA: disable this pair by BIOS

WLAN **GLAN**

R363 10K_0402_5% +3VS WWAN_CLKREQ# (28)

R364 10K_0402_5% R365 0_0402_5% +3VS MCH_CLKREQ# (8)

R368 10K_0402_5% +3VS MINI2_CLKREQ# (28)

R370 10K_0402_5% +3VS LAN_CLKREQ# (28)

R371 10K_0402_5% +3VS SATA_CLKREQ# (19)

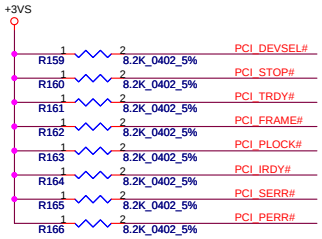
Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

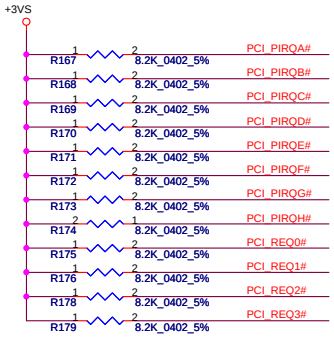
Compal Electronics, Inc.

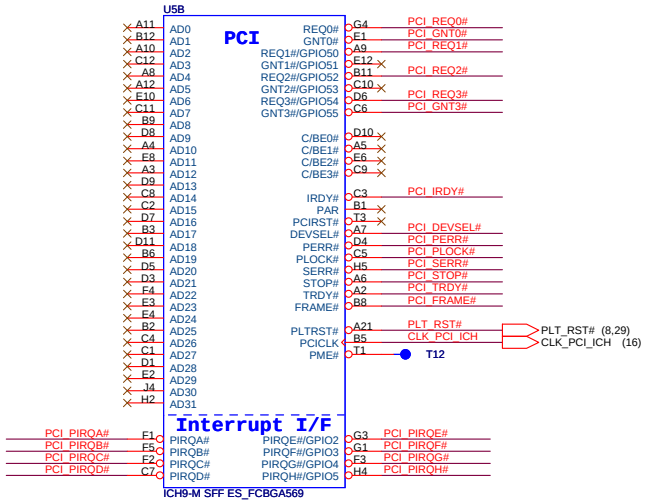
Title: Clock Generator (CK505)

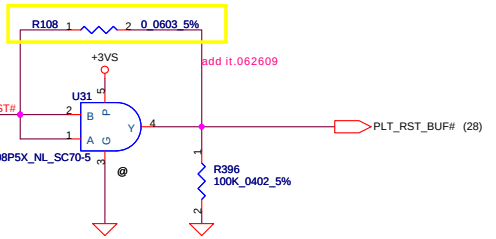
Size: Custom | Document Number: NAV30 M/B LA-5451P Schematic | Rev: 0.1

Date: Tuesday, October 20, 2009 | Sheet 16 of 41

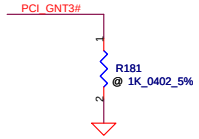




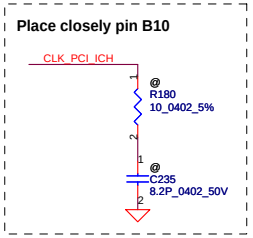


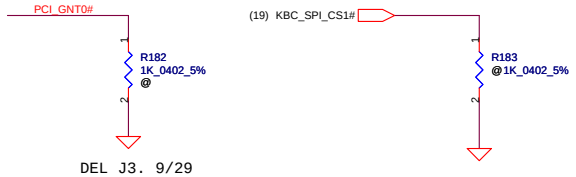


A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

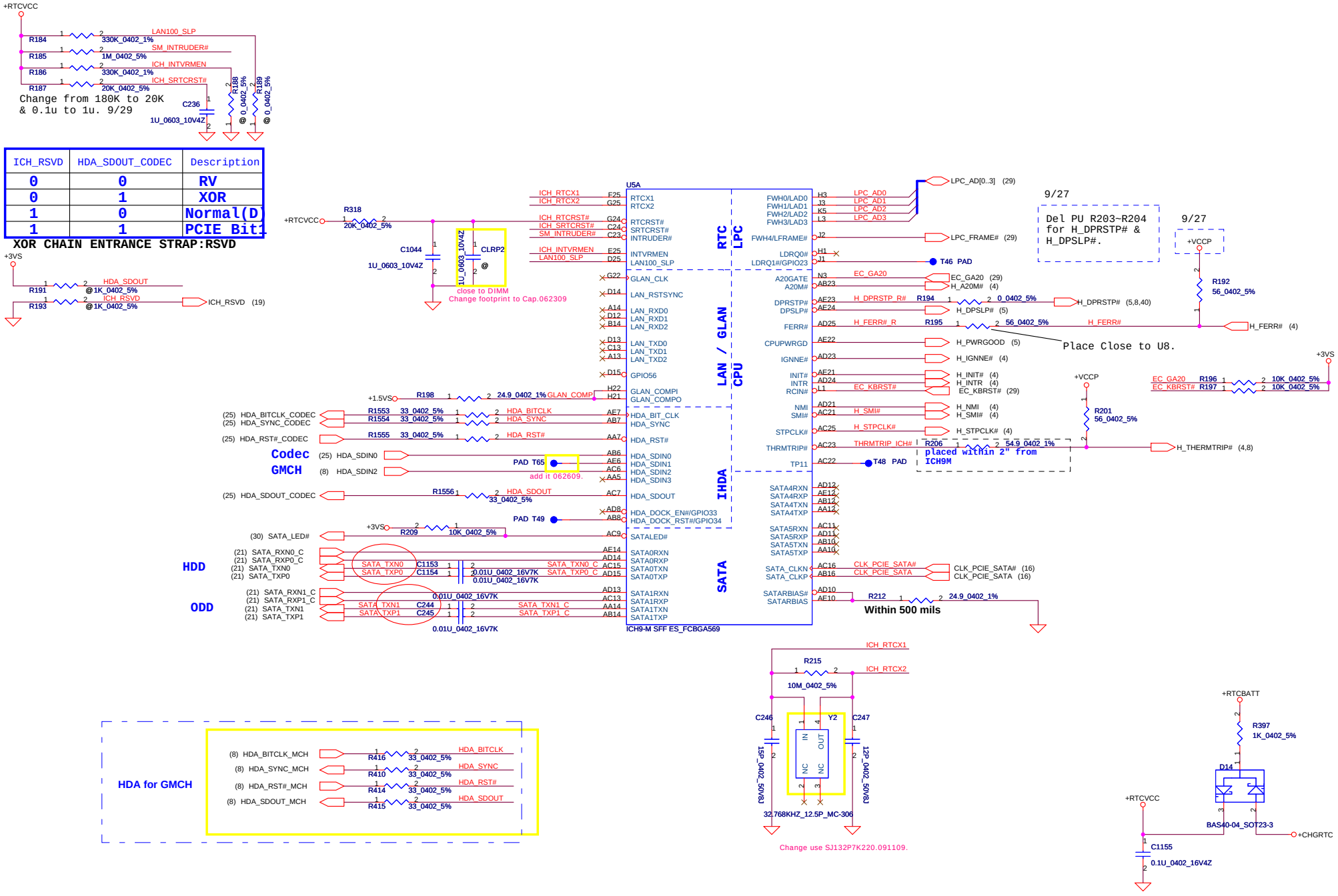




DEL J3. 9/29

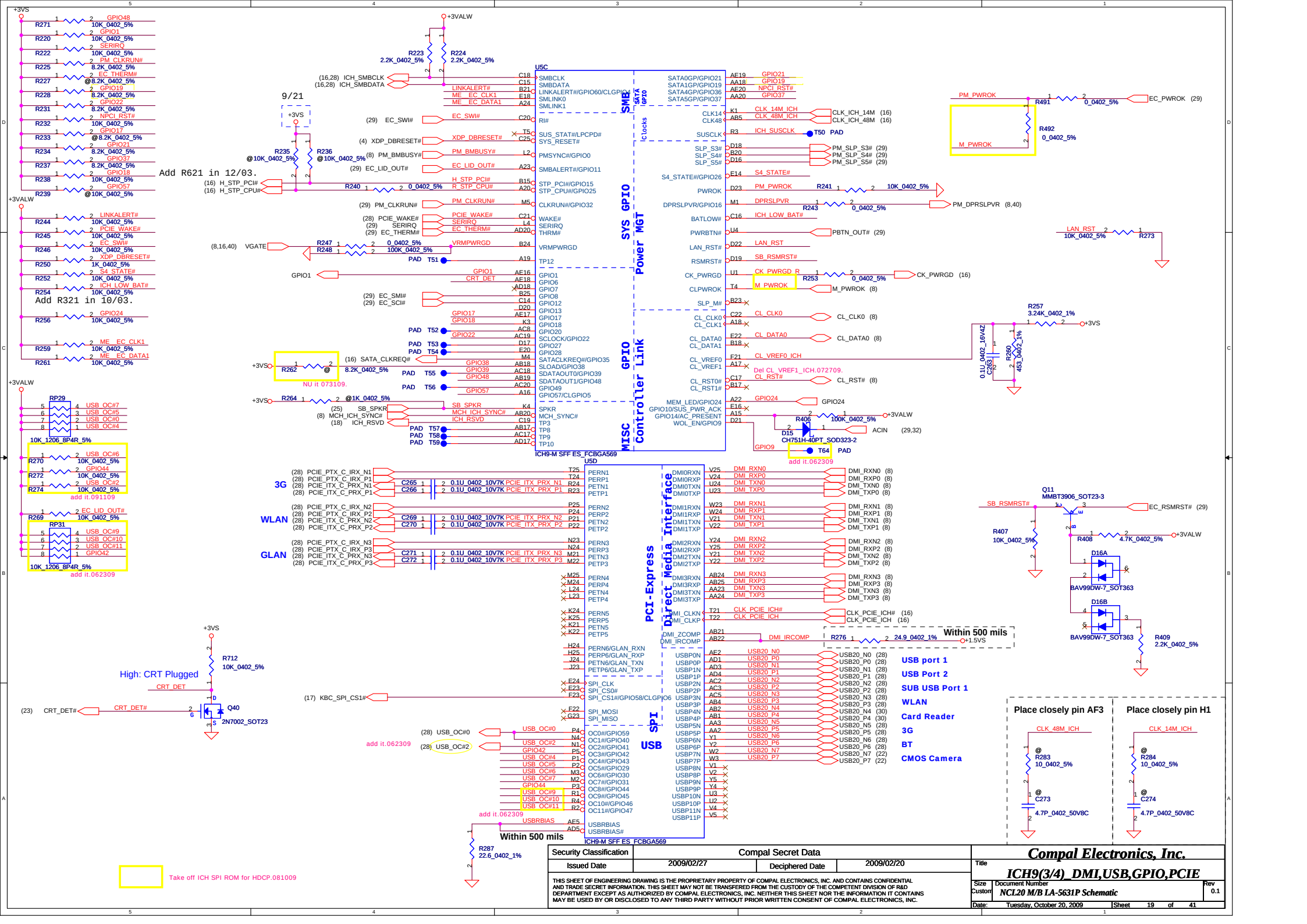
Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2009/02/20

Compal Electronics, Inc.			
Title	ICH9(1/4)-PCI/INT		
Size	Document Number		Rev
	NCL20 M/B LA-5631P Schematic		0.1
Date:	Tuesday, October 20, 2009	Sheet	17 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2009/02/20

Compal Electronics, Inc.	
Title	ICH9(2/4)_LAN,HD,IDE,LPC
Size: Custom	Document Number: NCL20 M/B LA-5631P Schematic
Rev	0.1
Date: Tuesday, October 20, 2009	Sheet 18 of 41



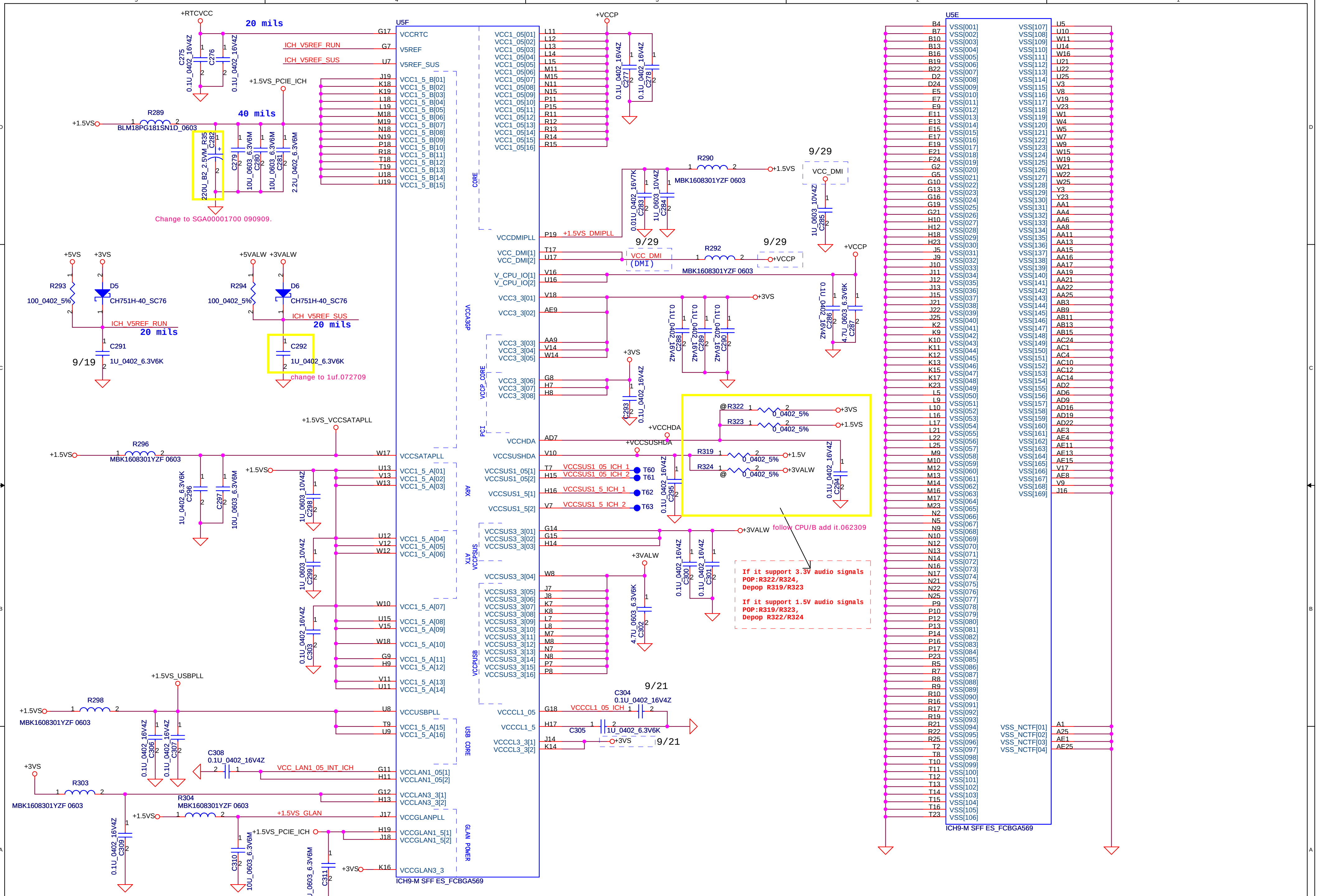
Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2009/02/20

Compal Electronics, Inc.

Title: ICH9(3/4)_DMI,USB,GPIO,PCIE

Size	Document Number	Rev
Custom	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 Sheet 19 of 41



Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2009/02/20

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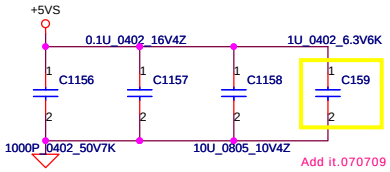
Compal Electronics, Inc.

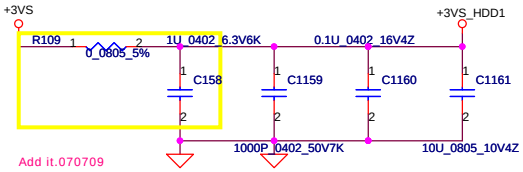
Title: **ICH9(4/4)_POWER&GND**

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

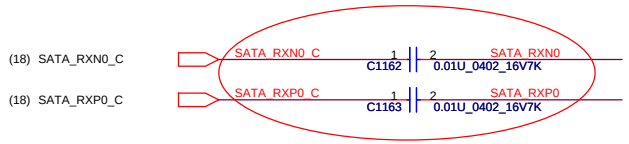
Date: Tuesday, October 20, 2009 | Sheet 20 of 41



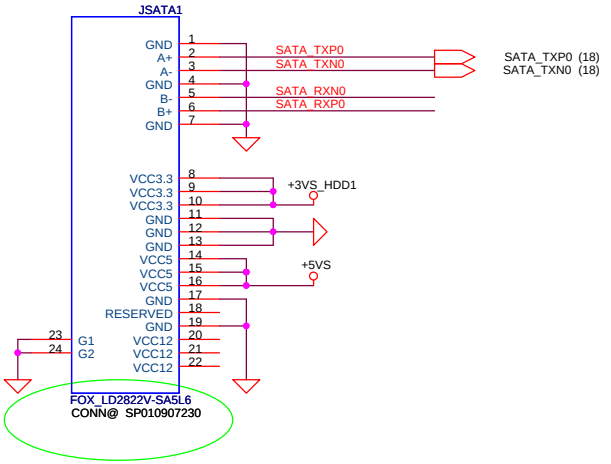
Add it.070709



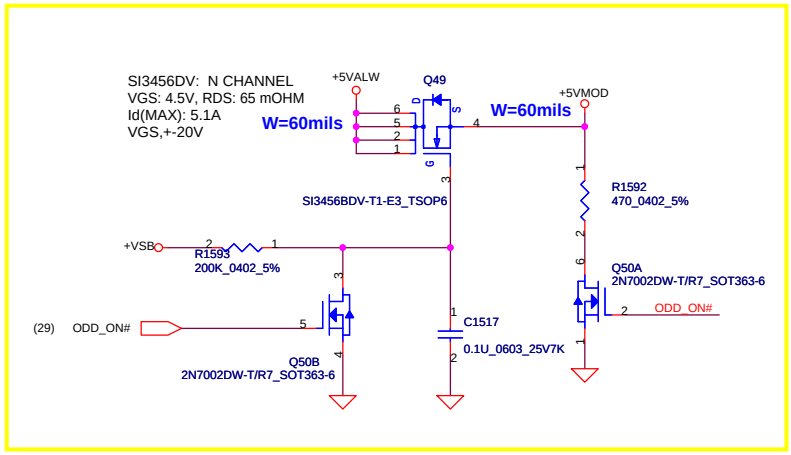
Add it.070709



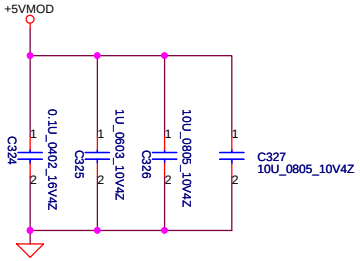
SATA HDD Conn.

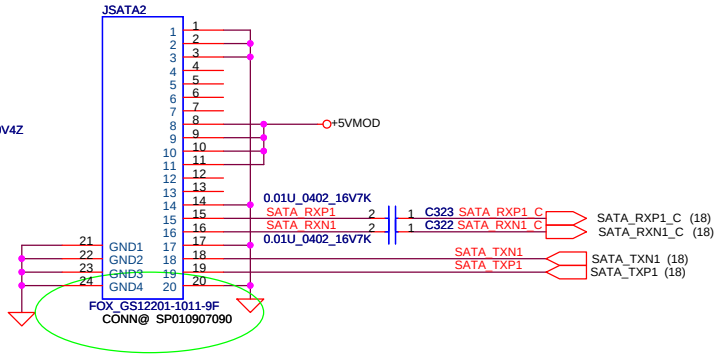


CD-ROM Connector



Modify +5VMOD control schematic 100809.





Add it for ODD button.072109.

Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

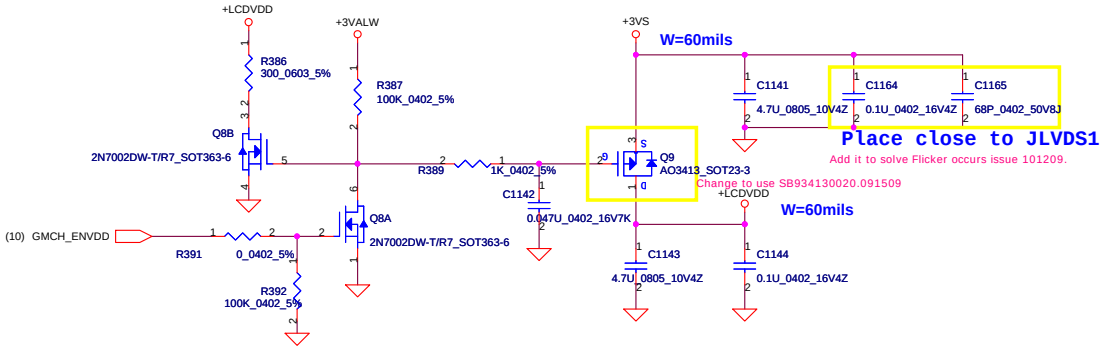
Compal Electronics, Inc.

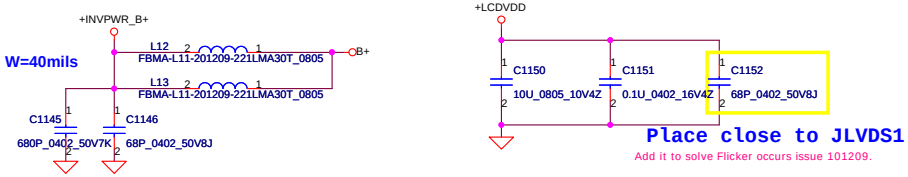
Title: HDD & ODD Connector

Size: Custom | Document Number: *NCL20 M/B LA-5631P Schematic* | Rev: 0.1

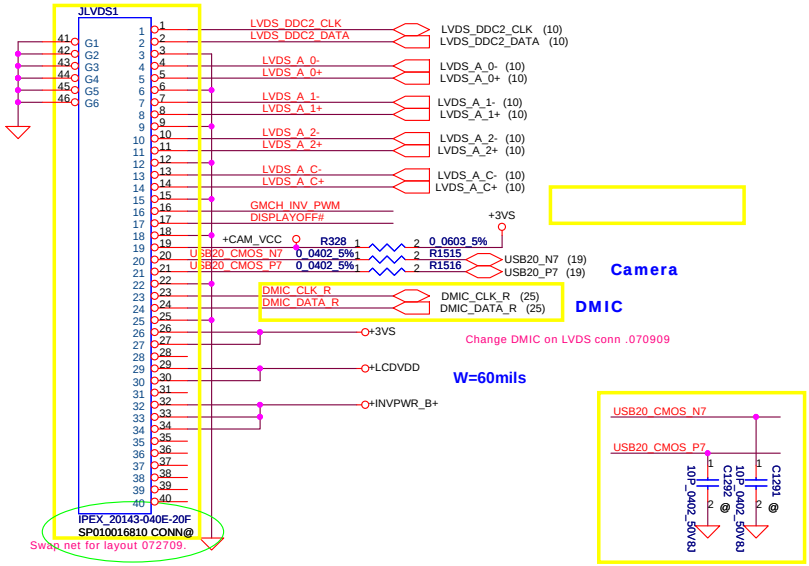
Date: Tuesday, October 20, 2009 | Sheet 21 of 41

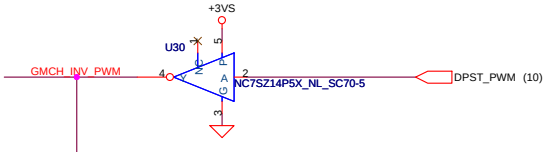
LCD POWER CIRCUIT

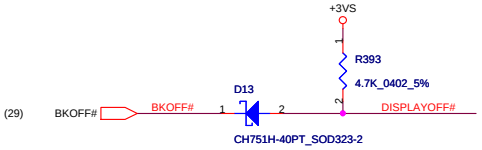


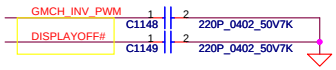


LVDS and USB CAM connector









Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

Compal Electronics, Inc.

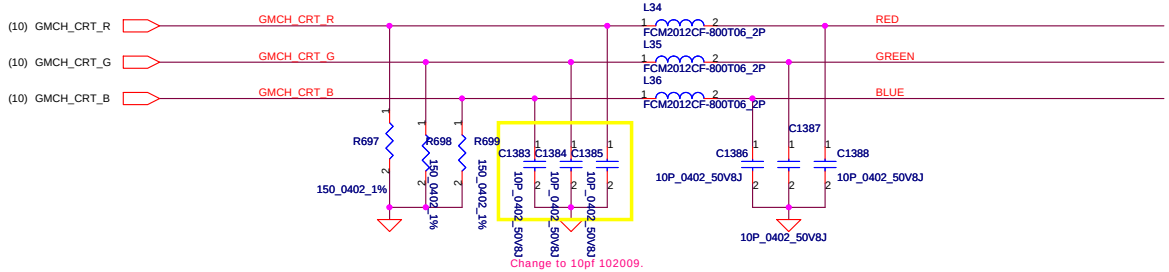
Title: LVDS Connector

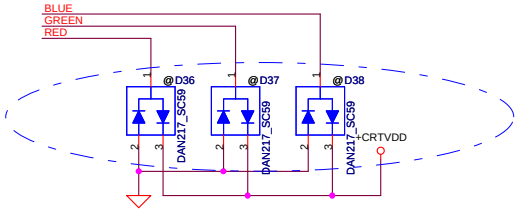
Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

Date: Tuesday, October 20, 2009 | Sheet 22 of 41

NOTE: L : A-->B1
H: A-->B2

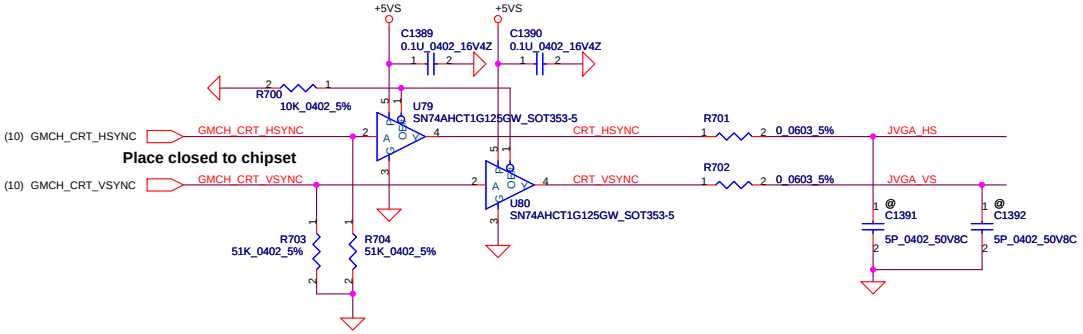
Place closed to chipset

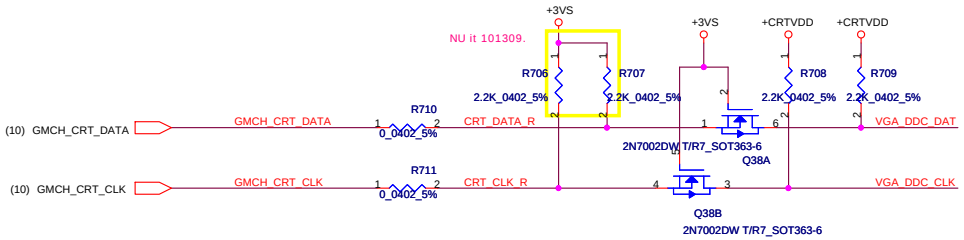


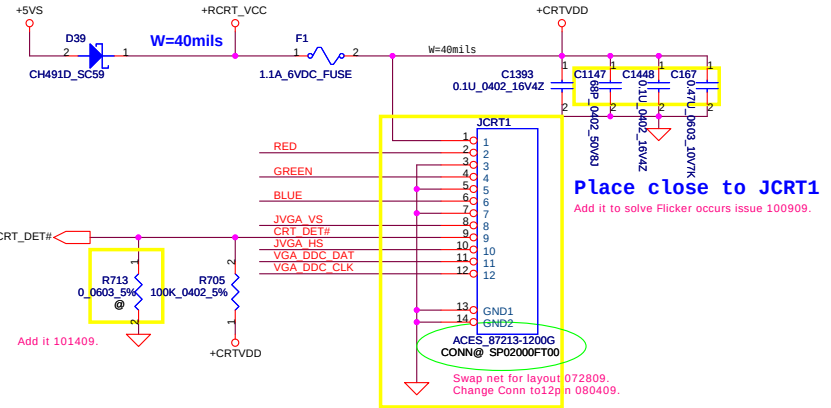


Place close to JCRT1

CRT PORT







Place close to JCRT1
Add it to solve Flicker occurs issue 100909.

Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: CRT Connector

Size | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

Date: Tuesday, October 20, 2009 | Sheet 23 of 41

EQ_1	EQ_0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

PC_2	PC_1	PC_0	Swing	Pre-amp	Slew-rate	
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	

close to IC VCC (+3VS) pins (one Pin one Capacitor)

Change package 081709.

NU it for vender's suggestion 091509.

Add it.071109

Add it to solve Flicker occurs issue 100909.

Trace AS Short PASS

Change use from ST to ASM1442T 091009.

U84. 49 (THERMAL_GND) to GND Plane

Take off Q48 090909.

Place closed to JHDMI1

Add it.071109

inverting level shift for NB

add it.062309

For Power Saving Application
When Plug-in HDMI
HDMI_HPD=High OE#=Low Enable Level Shift
When Plug-out HDMI
HDMI_HPD=Low OE#=High Disable Level Shift

HDMI Connector

NU 090909.

For Vender suggest to add it.062609

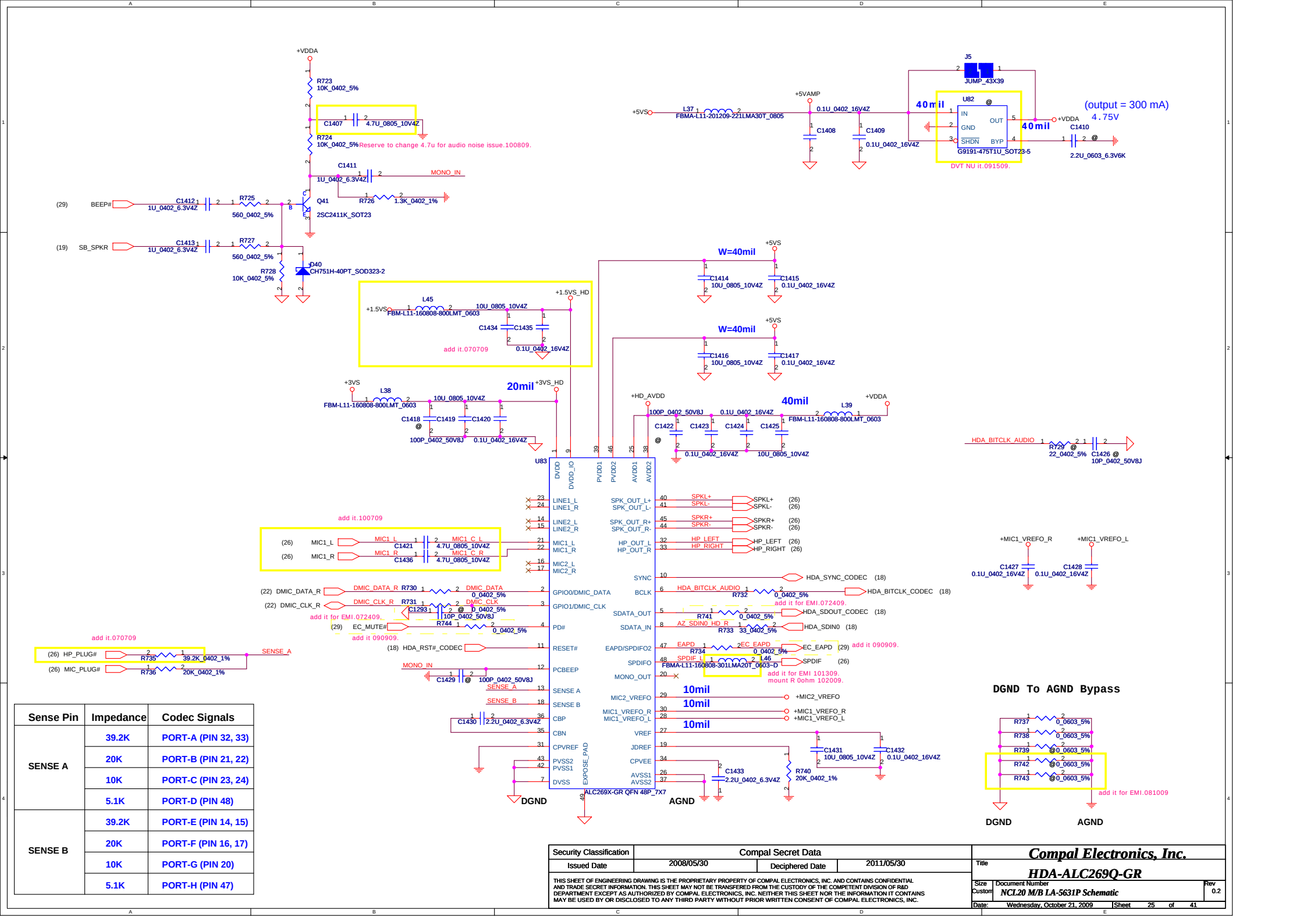
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

Compal Electronics, Inc.

Title: HDMI

Size	Document Number	Rev
	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 Sheet 24 of 41



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)

Security Classification	Compal Secret Data		
Issued Date	2008/05/30	Deciphered Date	2011/05/30

Compal Electronics, Inc.

Title: HDA-ALC269Q-GR

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.2

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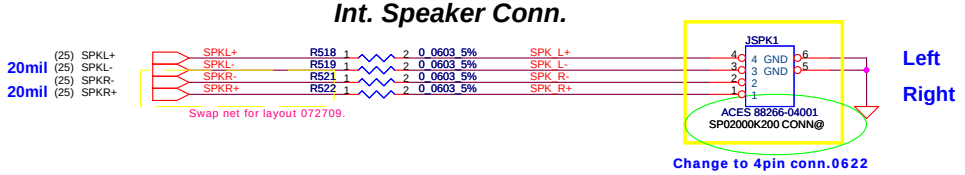
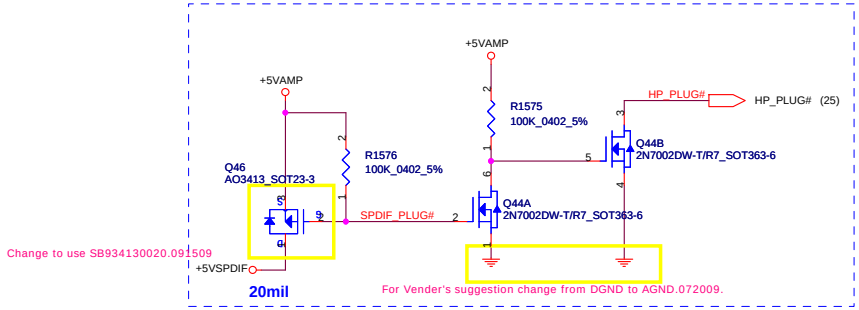
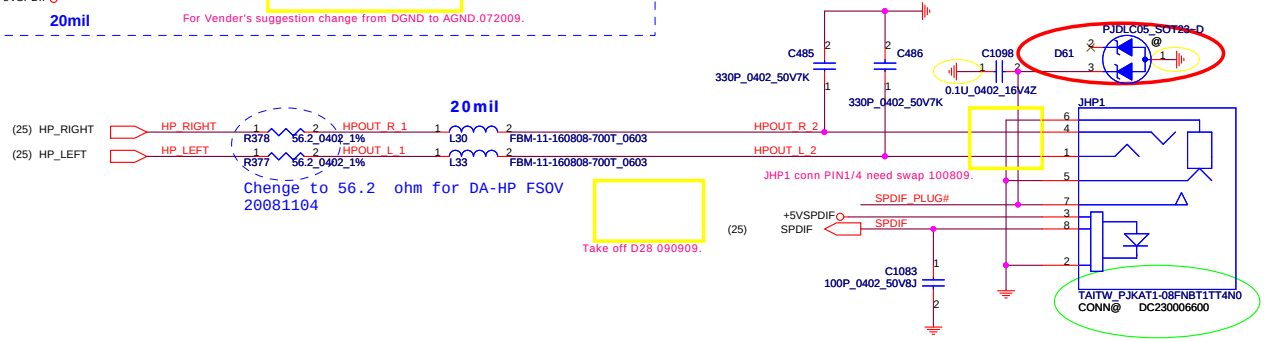
Int. Speaker Conn.

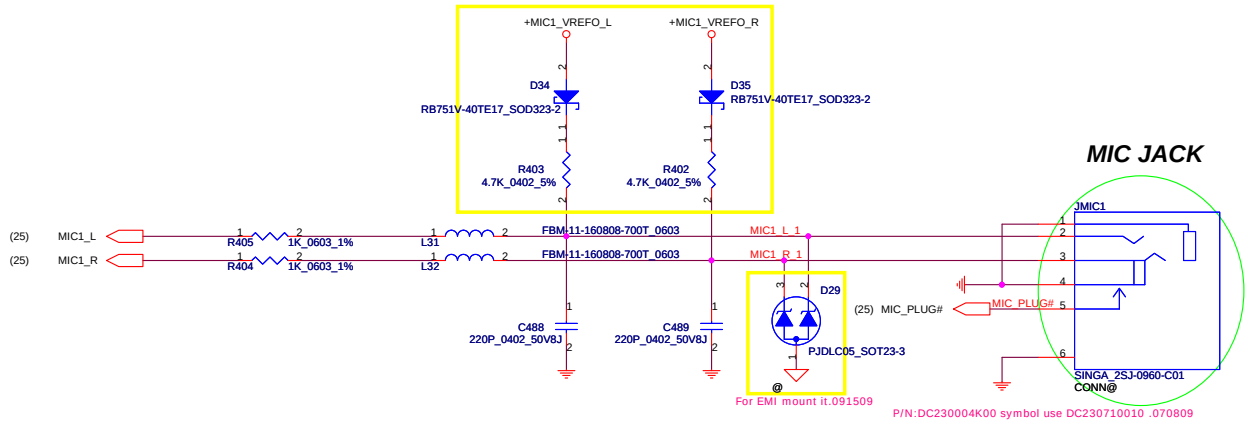




LINE Out/Headphone Out



MIC JACK



Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size	Document Number	Rev
B	*NCL20 M/B LA-5631P Schematic*	0.1

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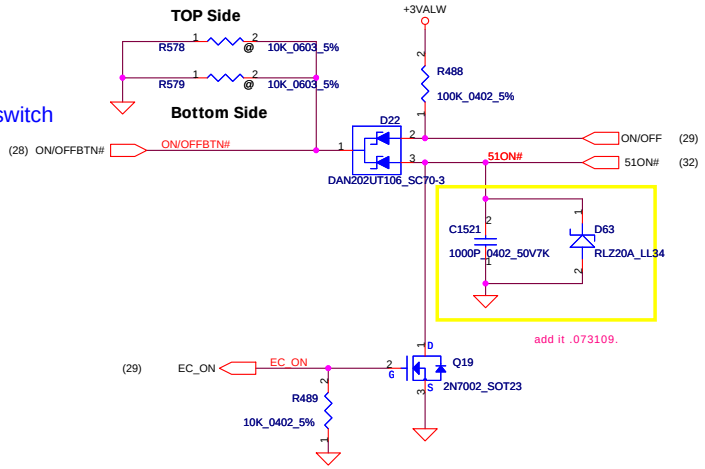
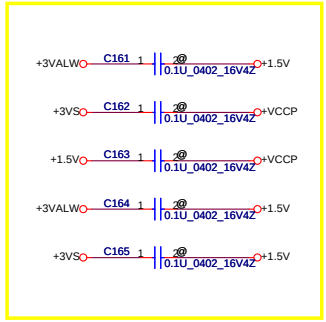
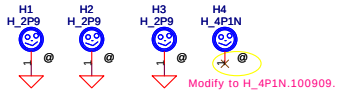
Power Button Logic

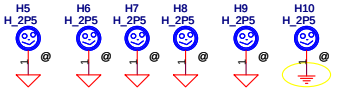
ON/OFF switch

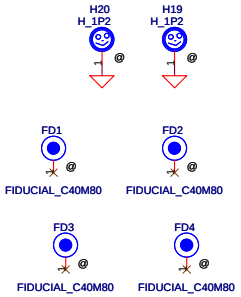




For EMI to add it.091109.

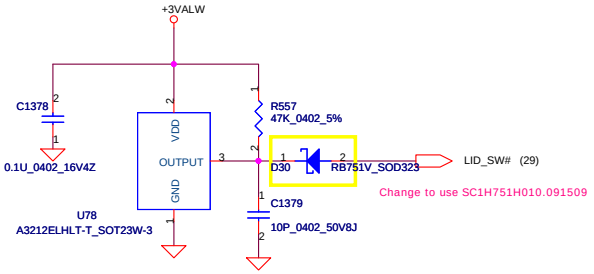






Lid Switch

(Hall Effect Switch)



Security Classification	Compal Secret Data		
Issued Date	2009/01/22	Deciphered Date	2009/11/20

Compal Electronics, Inc.

Title: PWR ON/OFF & Screw Hole

Size: Custom | Document Number: *NCL20 M/B LA-5631P Schematic* | Rev: 0.1

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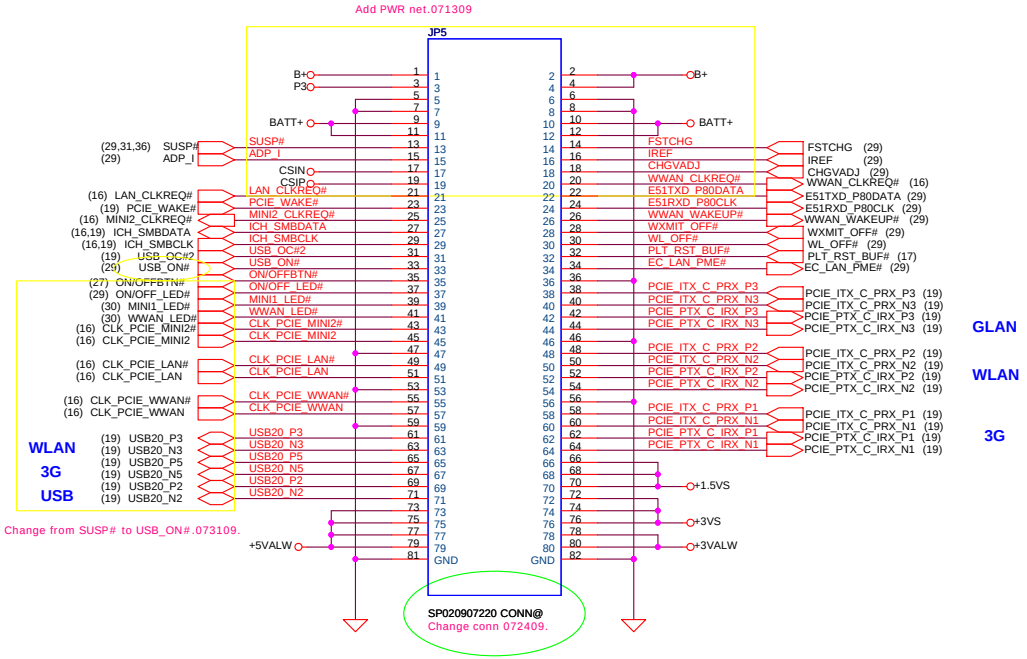

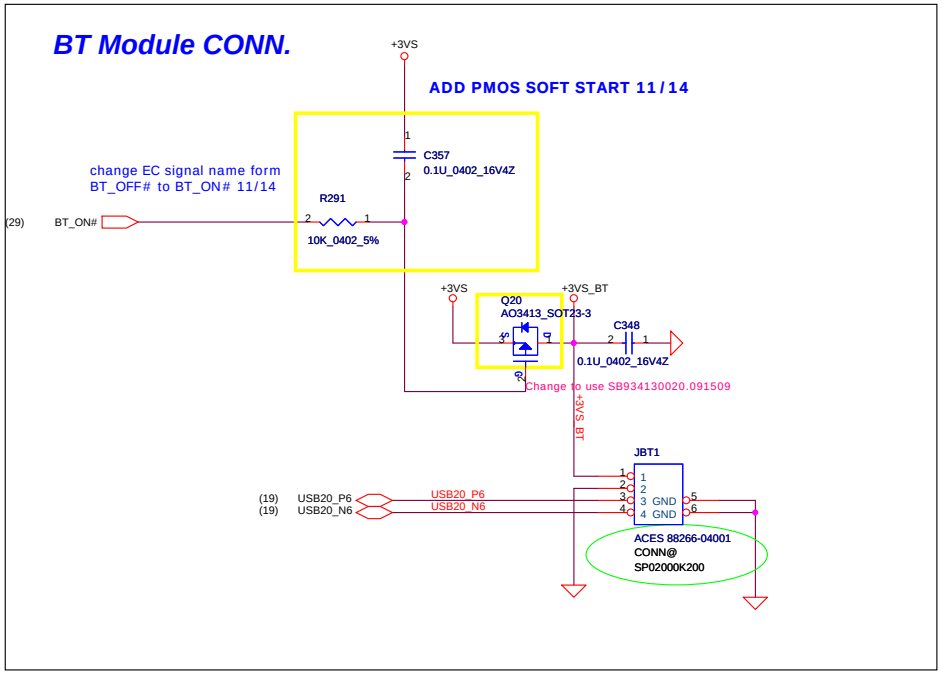

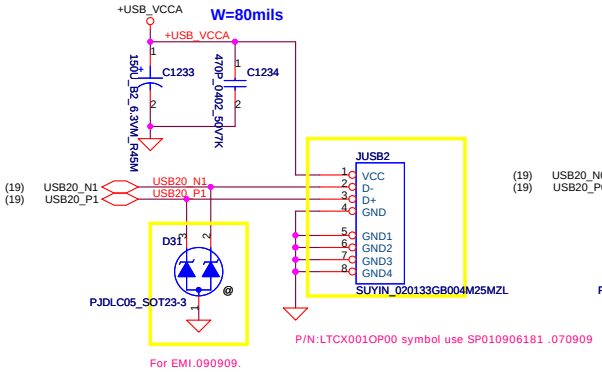

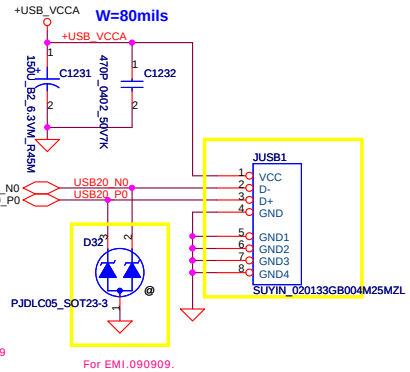

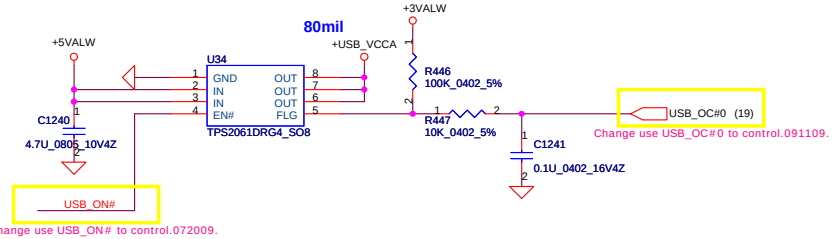

Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

Compal Electronics, Inc.

Title: NEW CARD & USB Connector

Size	Document Number	Rev
B	NCL20 M/B LA-5631P Schematic	0.1

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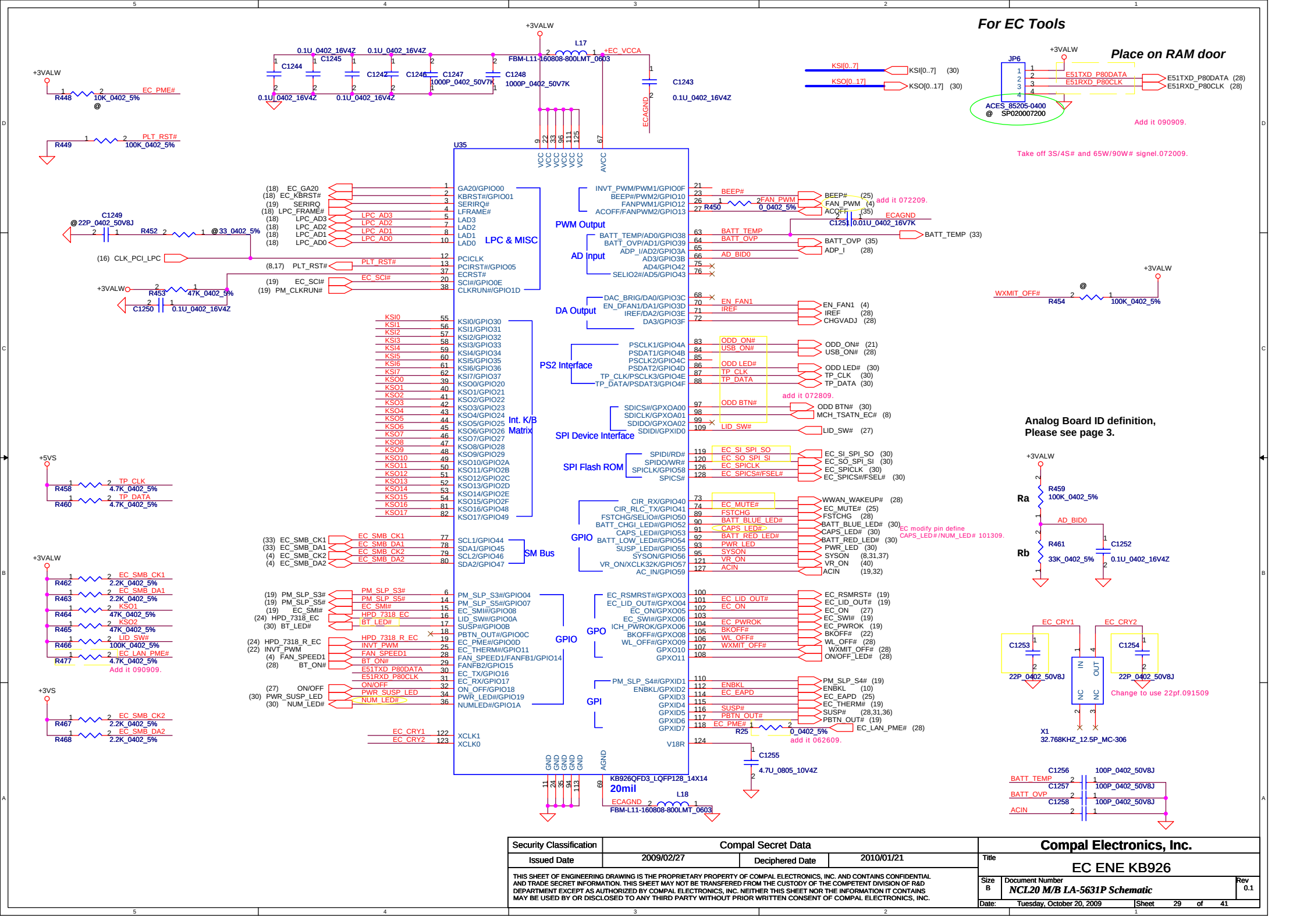
For EC Tools
Place on RAM door
Add it 090909.
Take off 3S/4S# and 65W/90W# signel.072009.
U35
KB926QFD3_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
add it 072209.
add it 072809.
Analog Board ID definition,
Please see page 3.
EC modify pin define
CAPS_LED#/NUM_LED# 101309.
Change to use 22pf.091509
Add it 090909.
Security Classification
Compal Secret Data
Issued Date
2009/02/27
Deciphered Date
2010/01/21
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Compal Electronics, Inc.
Title
EC ENE KB926
Size B
Document Number
NCL20 M/B LA-5631P Schematic
Rev 0.1
Date: Tuesday, October 20, 2009
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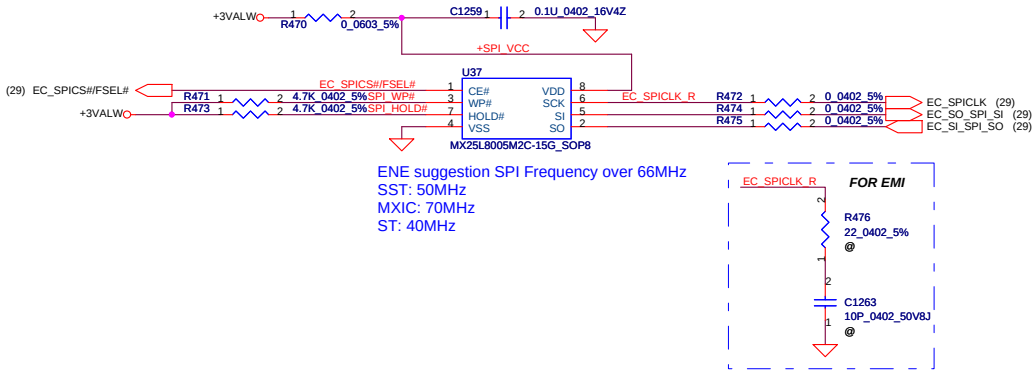
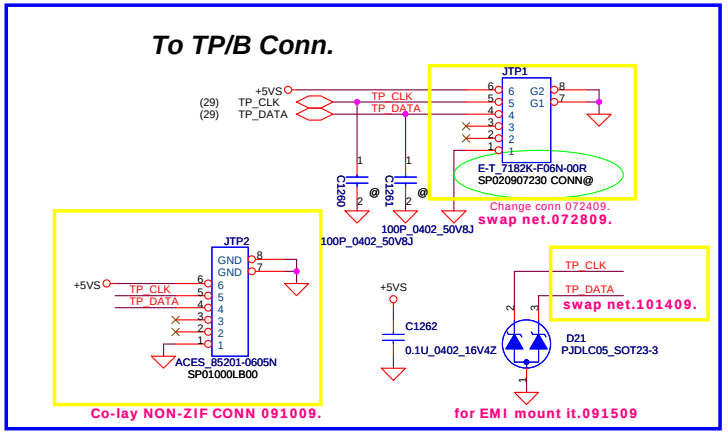
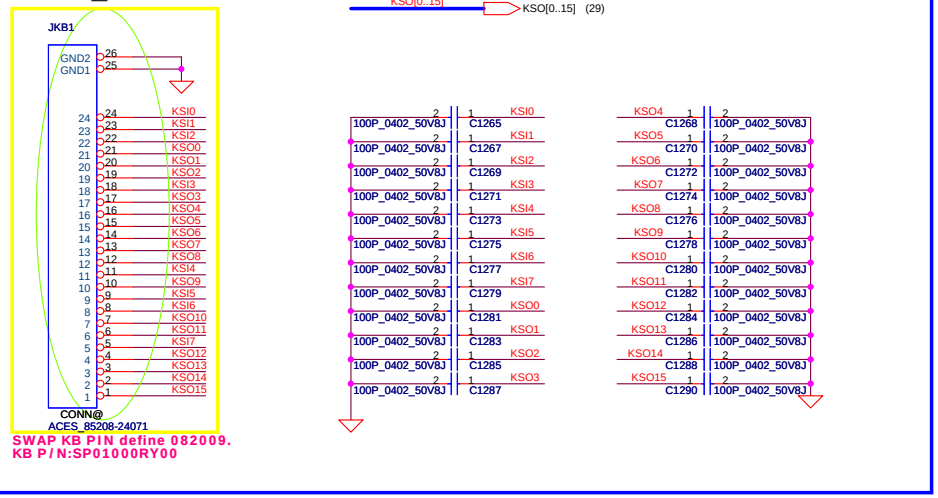


Take off U36.072009

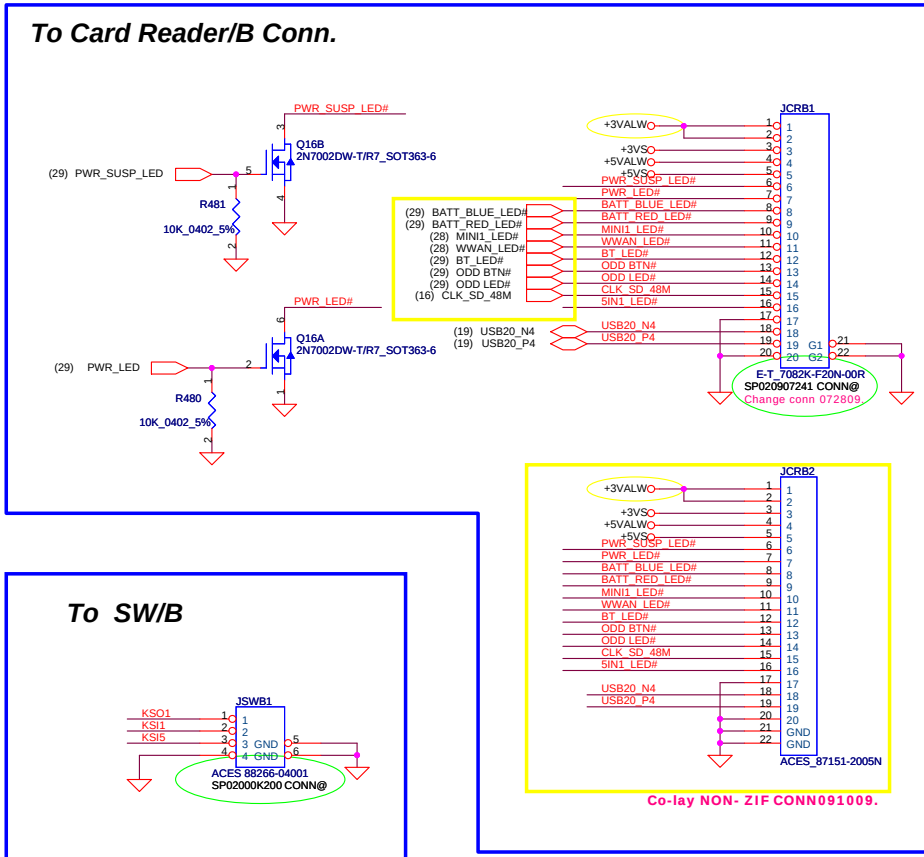
To TP/B Conn.



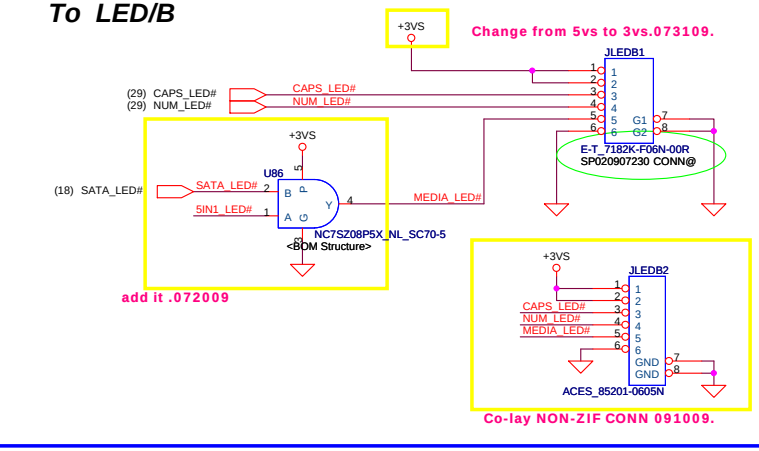
INT_KBD Conn.



To Card Reader/B Conn.



To LED/B



To SW/B

Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

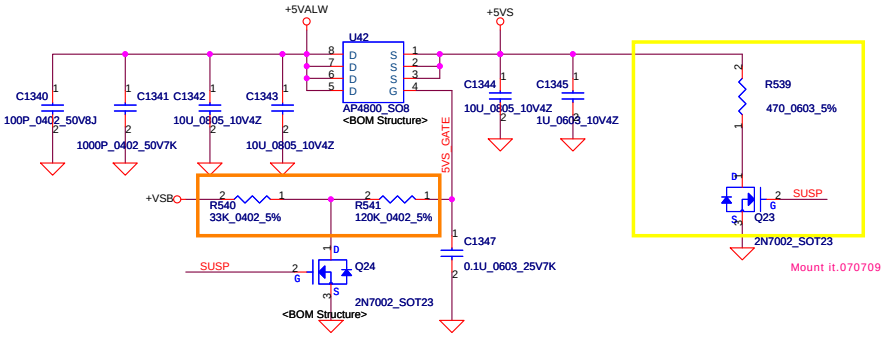
Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

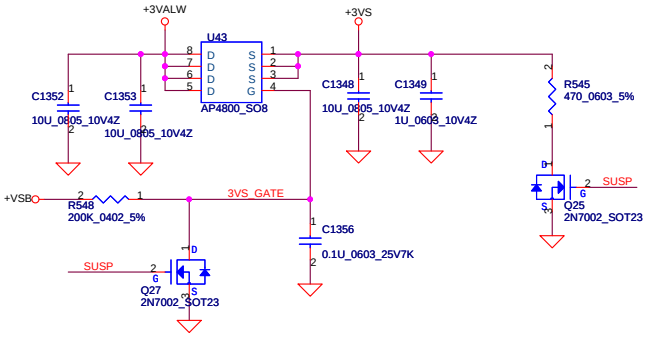
Size	Document Number	Rev
B	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 | Sheet 30 of 41

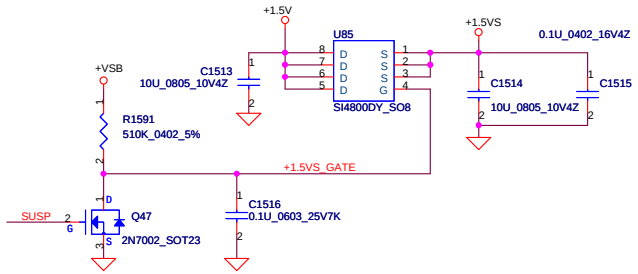
+5VALW TO +5VS



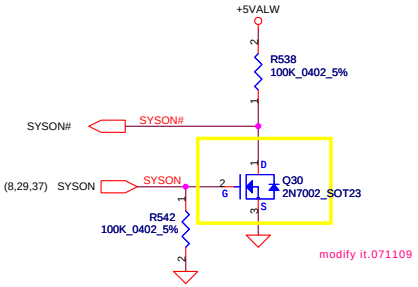
+3VALW TO +3VS

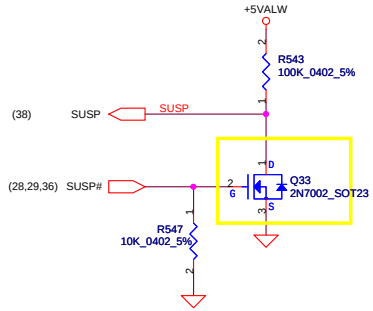


+1.5V to +1.5VS Transfer

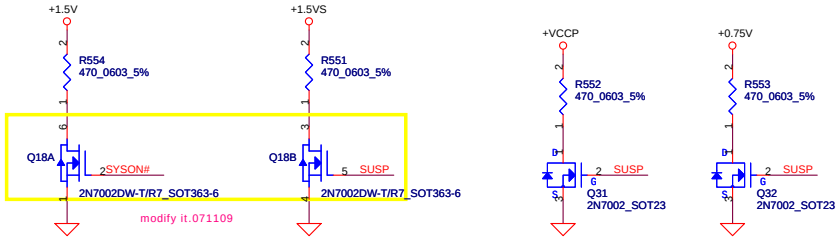


add it.070709





Discharge circuit



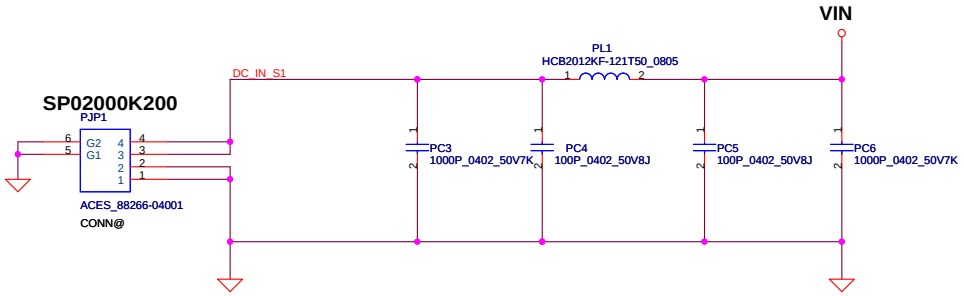
Security Classification	Compal Secret Data		
Issued Date	2009/02/27	Deciphered Date	2010/01/21

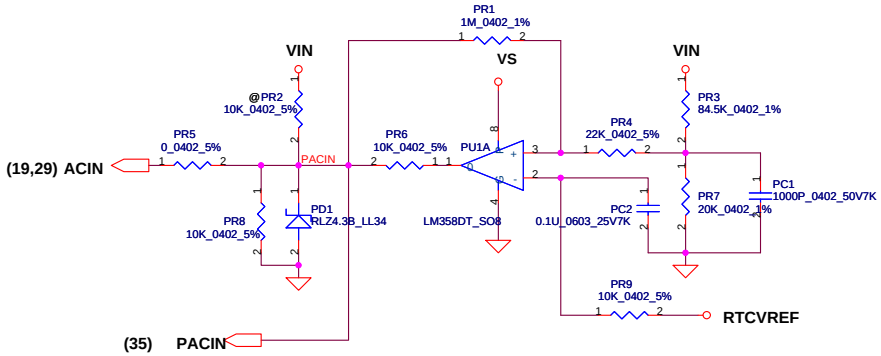
Compal Electronics, Inc.

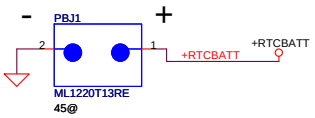
Title: DC Interface

Size	Document Number	Rev
B	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 | Sheet 31 of 41

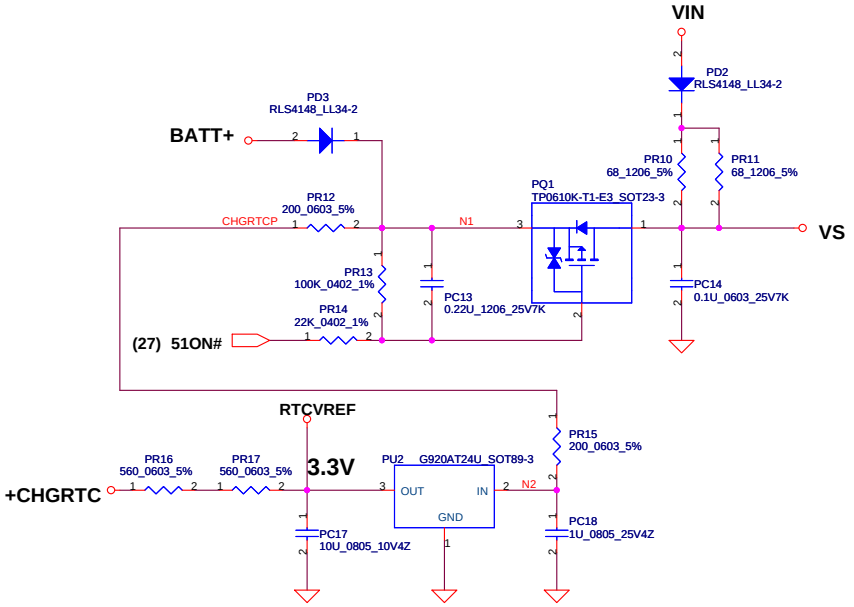


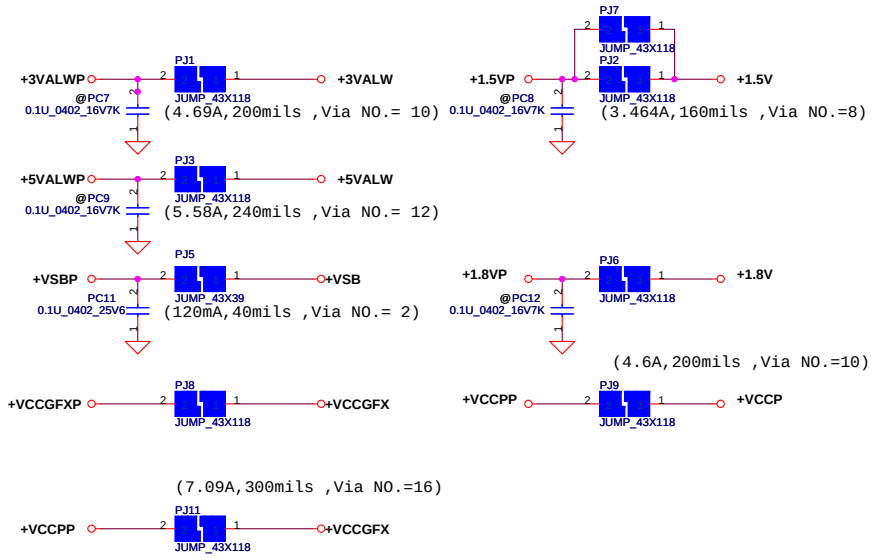




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





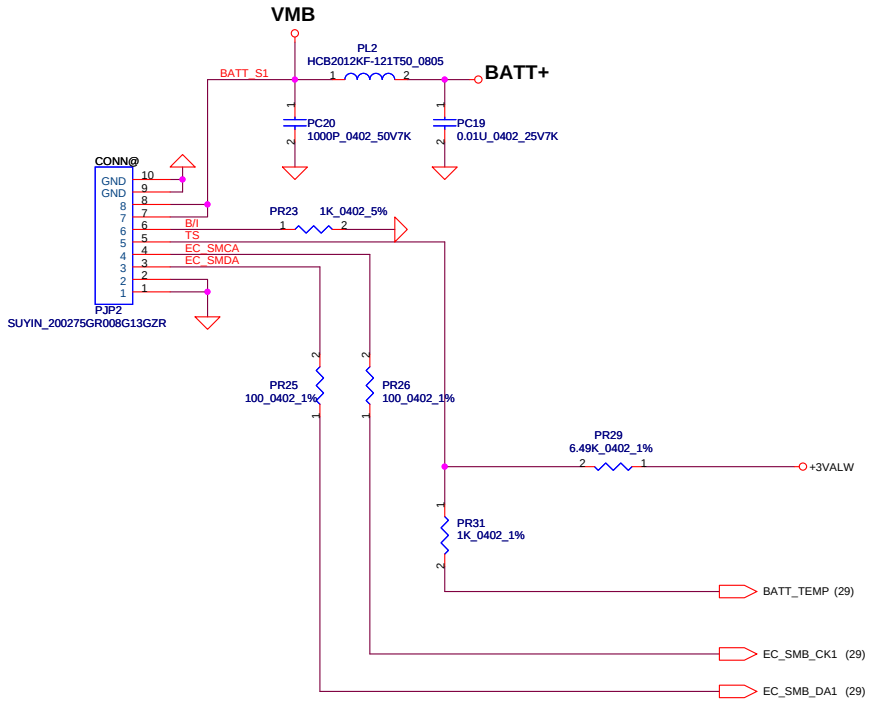
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

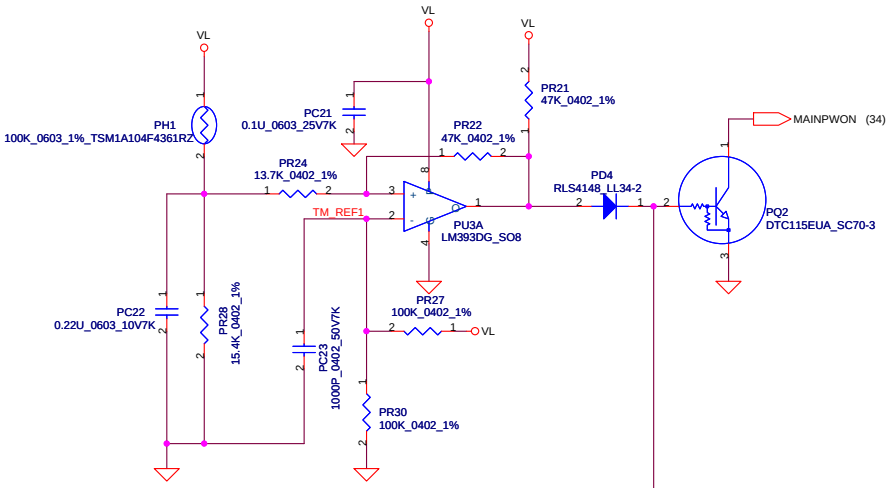
Title: DCIN & DETECTOR

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

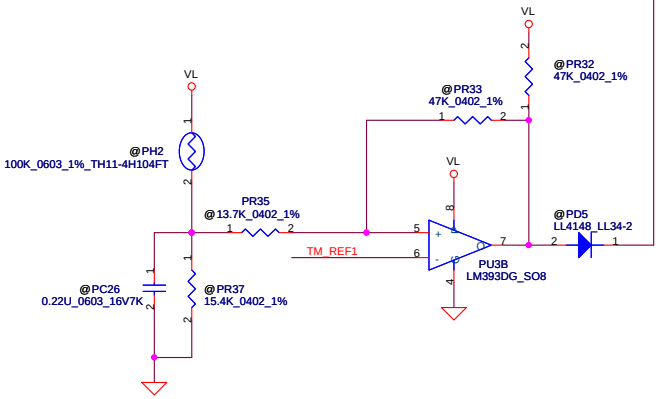
Date: Tuesday, October 20, 2009 | Sheet 32 of 41

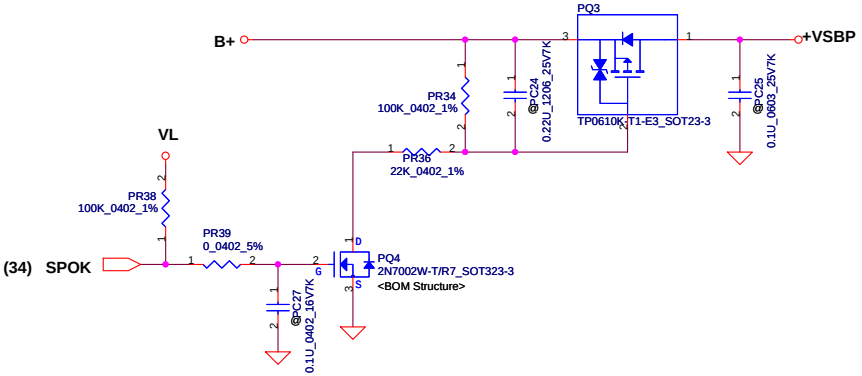


PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C





Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
Custom	NCL20 M/B LA-5631P Schematic	0.1

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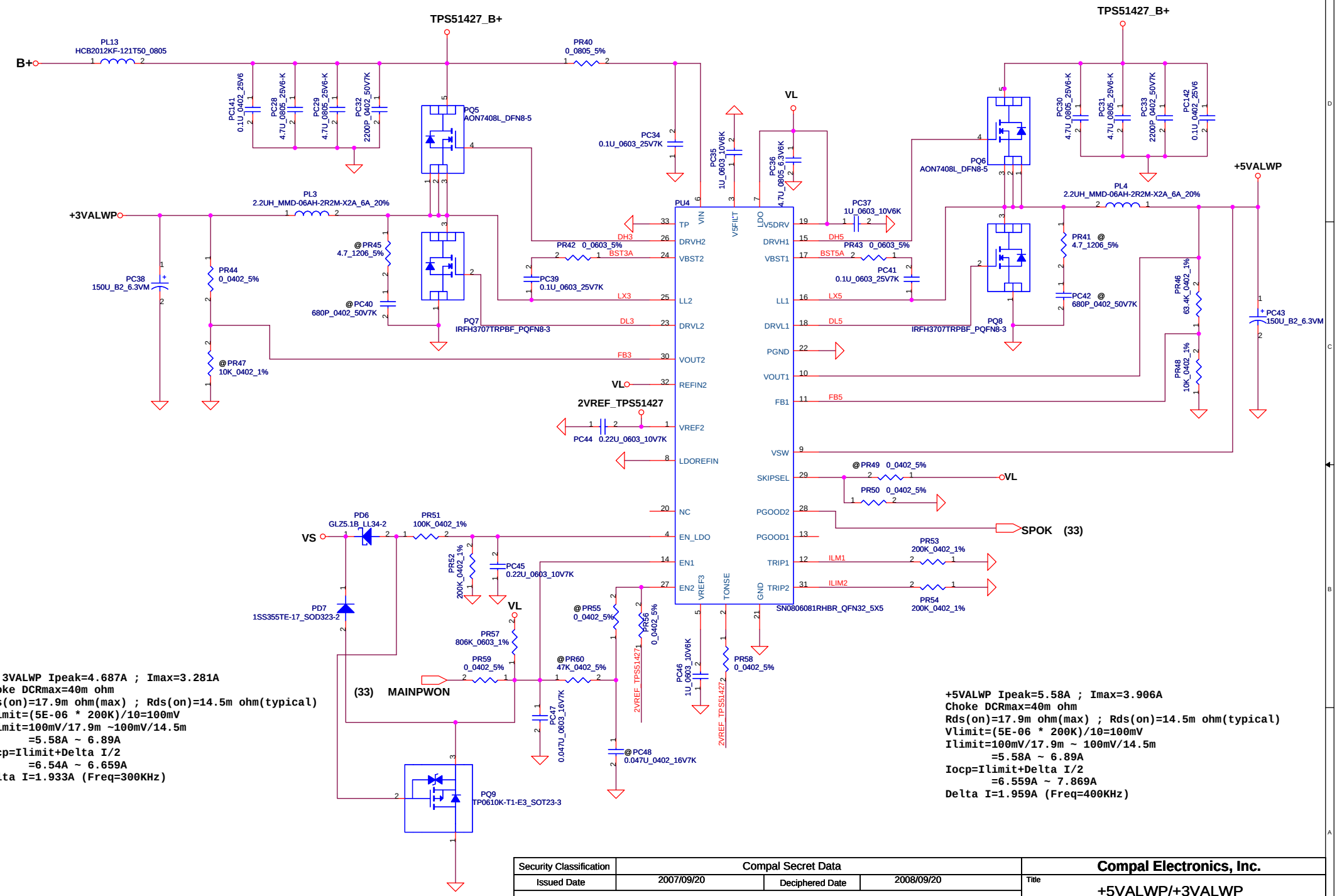


+3.3VALWP Ipeak=4.687A ; Imax=3.281A
Choke DCRmax=40m ohm
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/17.9m ~100mV/14.5m
=5.58A ~ 6.89A
Iocp=Ilimit+Delta I/2
=6.54A ~ 6.659A
Delta I=1.933A (Freq=300KHz)

+5VALWP Ipeak=5.58A ; Imax=3.906A
Choke DCRmax=40m ohm
Rds(on)=17.9m ohm(max) ; Rds(on)=14.5m ohm(typical)
Vlimit=(5E-06 * 200K)/10=100mV
Ilimit=100mV/17.9m ~ 100mV/14.5m
=5.58A ~ 6.89A
Iocp=Ilimit+Delta I/2
=6.559A ~ 7.869A
Delta I=1.959A (Freq=400KHz)

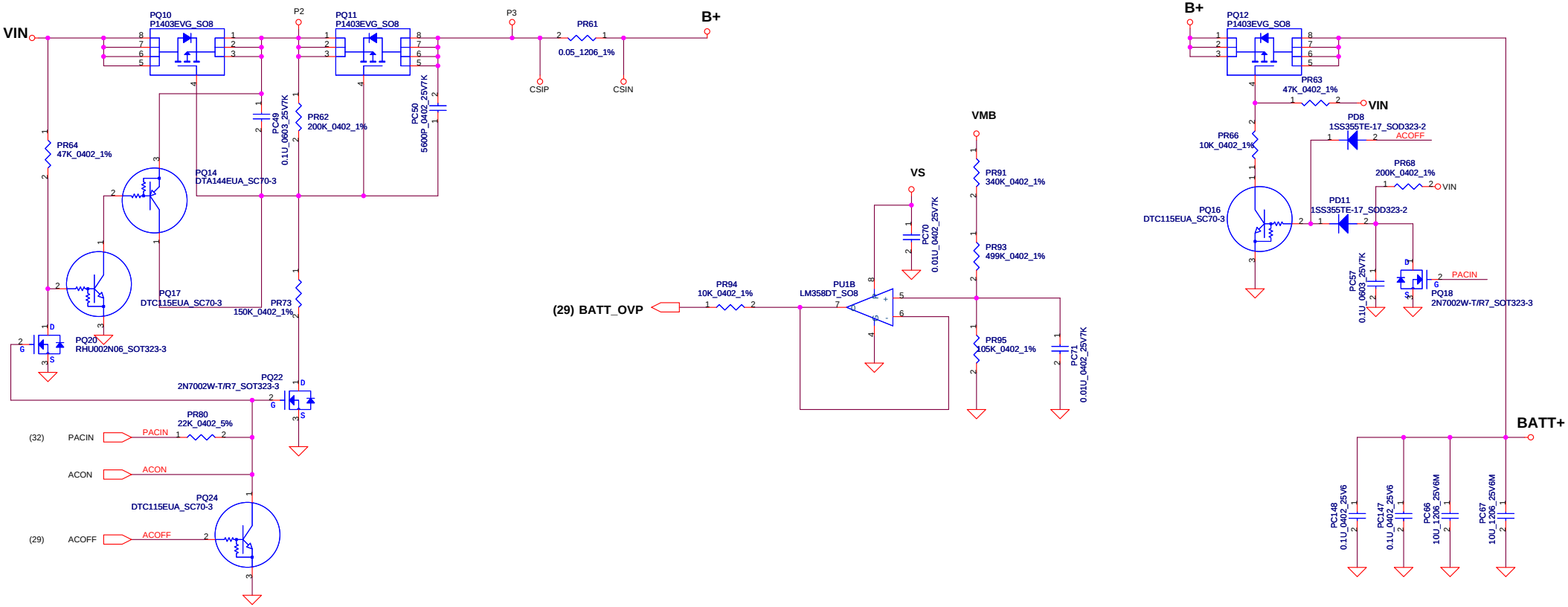
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 1.1

Date: Tuesday, October 20, 2009 | Sheet 34 of 41

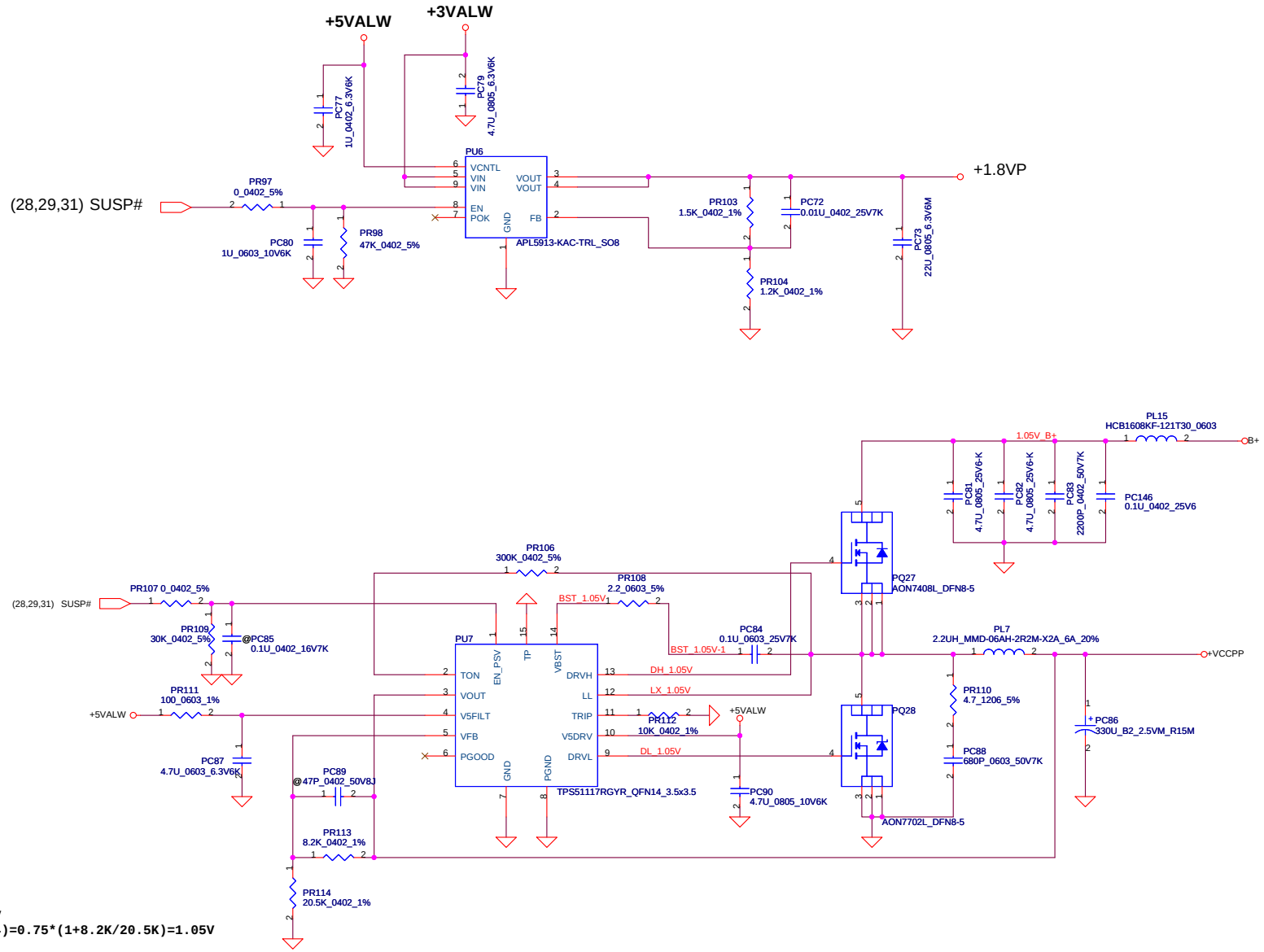


Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
Custom	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 | Sheet 35 of 41



<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR113/PR114)=0.75*(1+8.2K/20.5K)=1.05V
Fsw=261KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(min)=14.5m
Ipeak=5A, Imax=5A, Iocp=6A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=1.72A
=>1/2DeltaI=0.86A
Vtrip=Rtrip*10uA=12K*10uA=0.12V
Iocpmin=Vtrip/Rdsonmax*1.2+0.86
=0.12/(0.0179*1.2)+0.86=6.446A
Iocpmax=(0.12/(0.0145*1.2))+0.86A=7.756A
Iocp=6.446A~7.756A

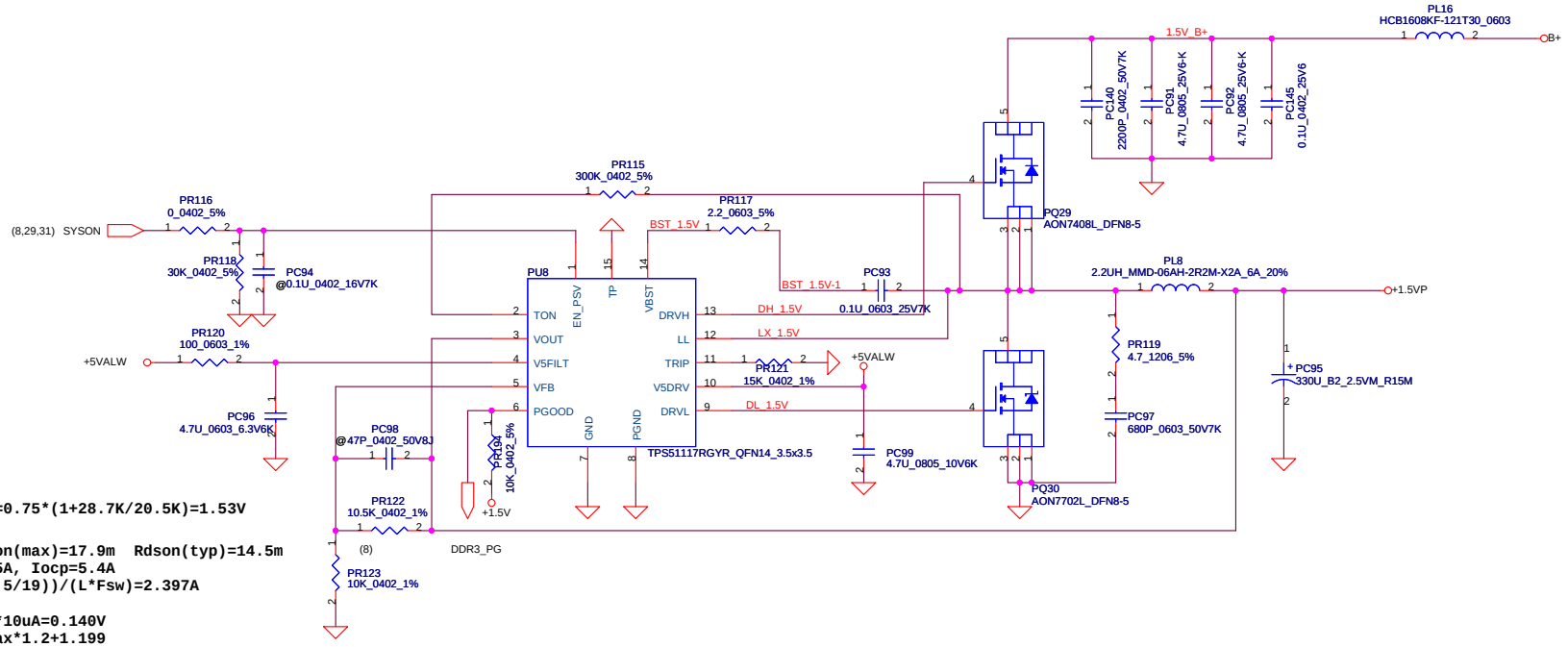
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +1.8VP / +VCCPP

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

Date: Tuesday, October 20, 2009 | Sheet 36 of 41



<Vo=1.5V> VFB=0.75V
Vo=VFB*(1+PR91/PR92)=0.75*(1+28.7K/20.5K)=1.53V
Fsw=262KHz

Cout ESR=15m ohm Rdson(max)=17.9m Rdson(typ)=14.5m
Ipeak=4.5A, Imax=3.15A, Iocp=5.4A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.397A
=>1/2Delta I=1.199A
Vtrip=Rtrip*10uA=14K*10uA=0.140V
Iocpmin=Vtrip/Rdsonmax*1.2+1.199
=0.140/(0.0179*1.2)+1.199=7.717A
Iocpmax=(0.140/(0.0145*1.2))+1.199A=9.245A
Iocp=7.717A~9.245A

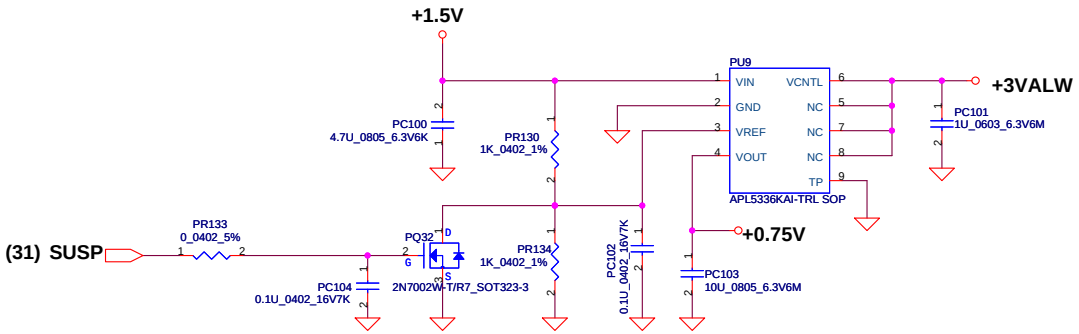
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +1.5VP

Size	Document Number	Rev
Custom	NCL20 M/B LA-5631P Schematic	0.1

Date: Tuesday, October 20, 2009 | Sheet 37 of 41



Ipeak=1A, Imax=0.7A

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: +0.75VSP

Size: Custom | Document Number: NCL20 M/B LA-5631P Schematic | Rev: 0.1

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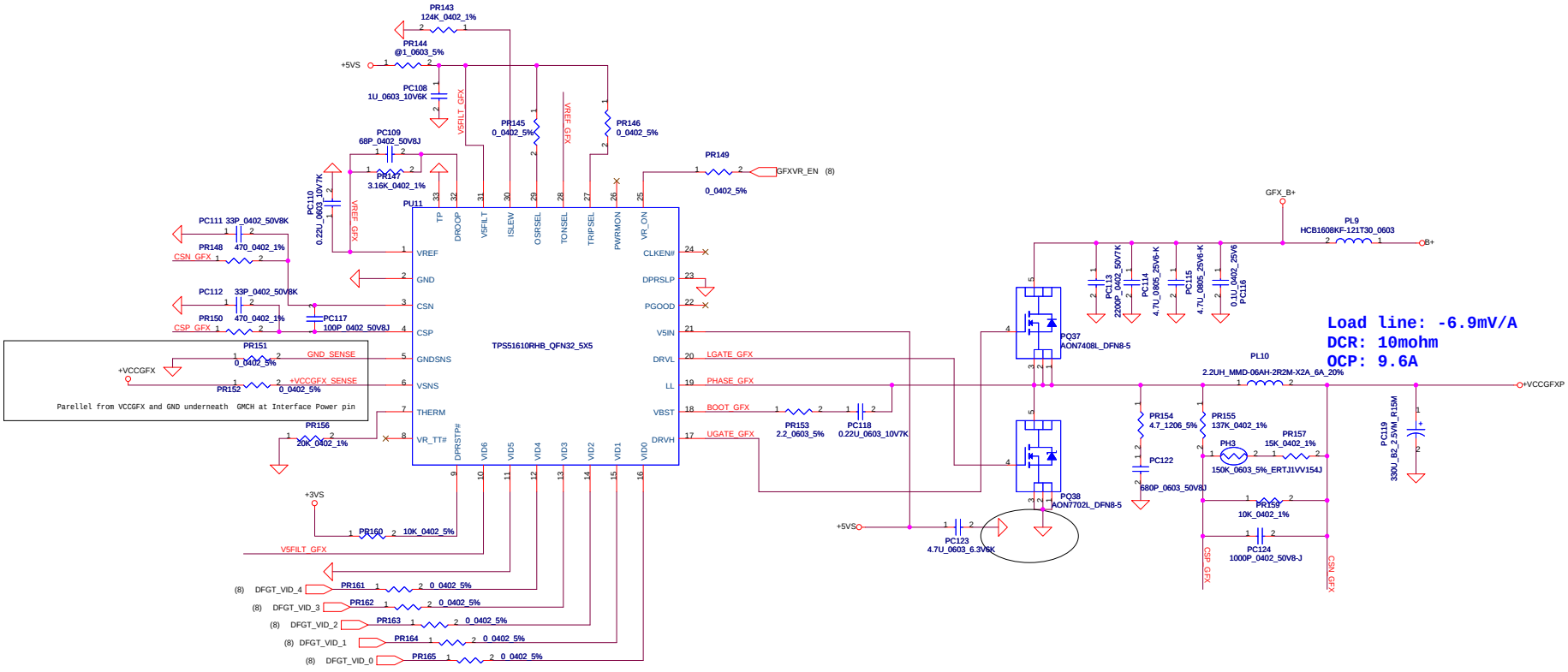

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Title	GFX		
Size C	Document Number NCL20 M/B LA-5631P Schematic		Rev 0.1
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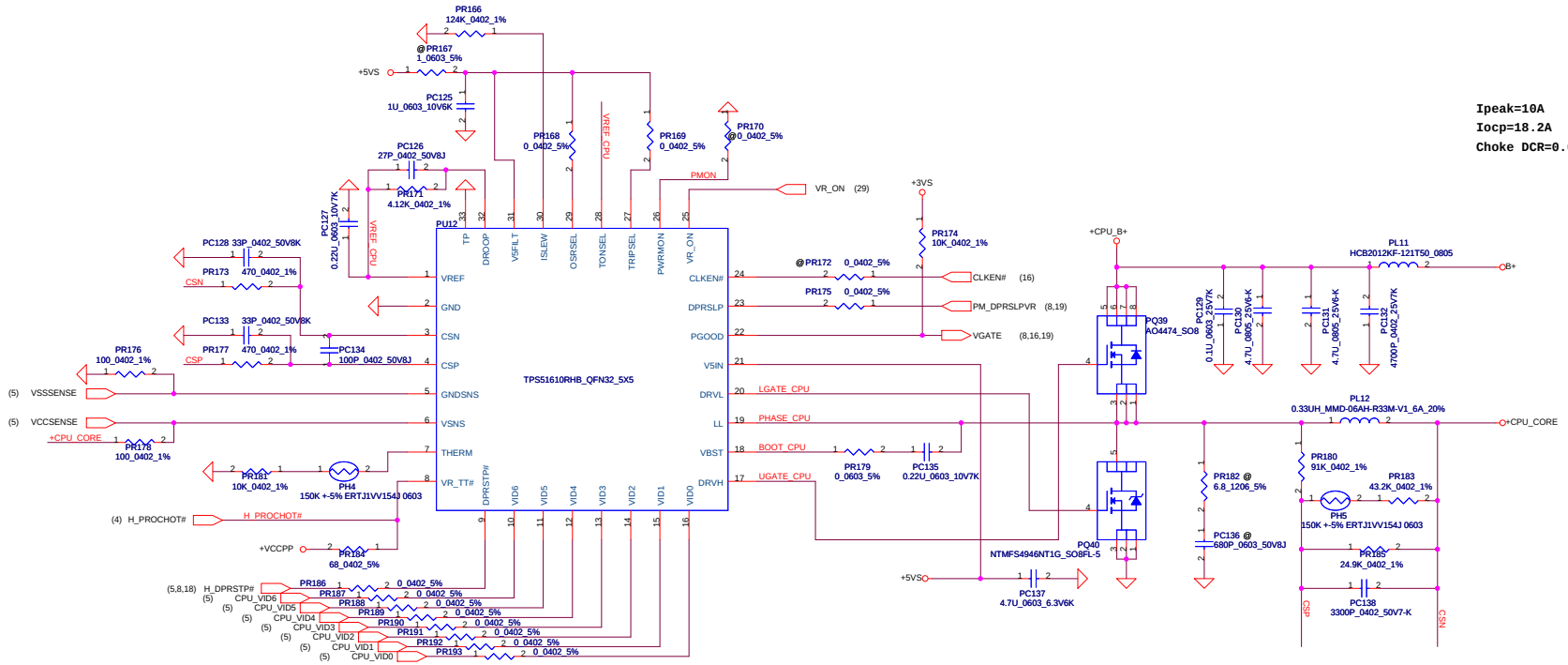

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Title	+CPU_CORE		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR121 to 18K	modify 1.5VP OCP to 12A	0.2	44	Change PR121 to 18K	08/23	EVT2
2	Change GFXVCCP OCP	Change GFXVCCP OCP to 9.1A	0.2	46	Change PR147 PR155 PH3 PR157 PR159 PC124	08/23	EVT2
3	Improve VCCP Efficiency	Decrease L/S DCR value to 11m ohm	0.3	43	Change PQ28 from IRE3707 to AON7702L	09/16	DVT
4	Change VCCP OCP	Change VCCP OCP to 6.8A~8.4A	0.3	43	Change PR112 from 12K to 10K	09/16	DVT
5	Delete 0.75V enable signal	Delete 0.75V enable signal(reserve)	0.3	45	Delete PR131	09/16	DVT
6	Change GFXVCCP OCP	Change GFXVCCP OCP to 9.1A	0.3	46	Change PR147 PR155 PH3 PR157 PR159 PC124	09/16	DVT
7	Change PR121 to 15K	modify 1.5VP OCP to 10A	0.3	44	Change PR121 to 15K	09/16	DVT
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Compal Electronics, Inc.

Title: PIR (PWR)

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