

Compal confidential

Liverpool/Sunderland 10ATG

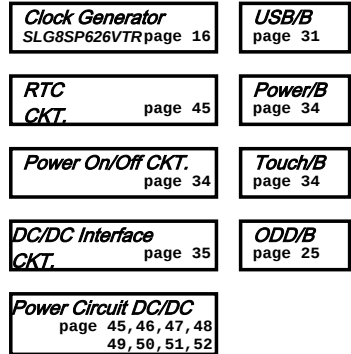
NSWAE/NTWAE LA-5331P Schematics Document

Mobile AMD S1G3/
RX881
SB710

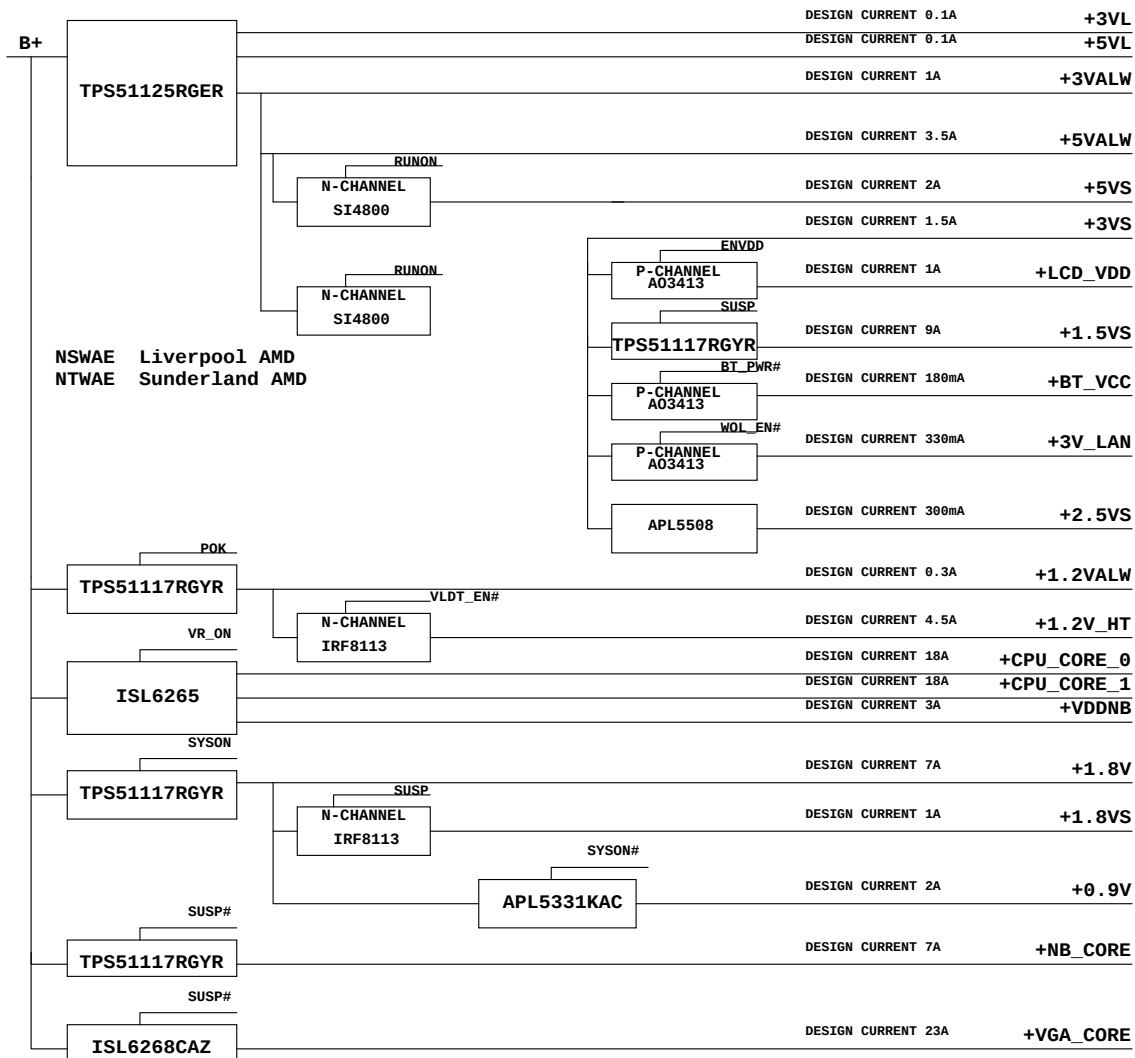
2009-10-02 Rev. 1.0

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Tigris Platform



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Voltage Rails

O : ON
X : OFF

power plane	State				
					+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
		+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	
S0		0	0	0	0
S1		0	0	0	0
S3		0	0	0	X
S5 S4/AC		0	0	X	X
S5 S4/ Battery only		0	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

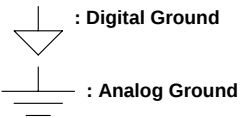
EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
HDMI-CEC	34H	0011 010X b
EC KB926D4		

EC SM Bus2 address

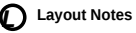
Device	HEX	Address
ADI1032-1 CPU	98H	1001 100X b
ADI1032-2 VGA	9AH	1001 101X b
EC KB926D3		

Symbol Note :



@ : just reserve , no build

DEBUG@ : reserve for debug.



UMA@: means for RS780M.

BTO (Build-To-Order) Option Table

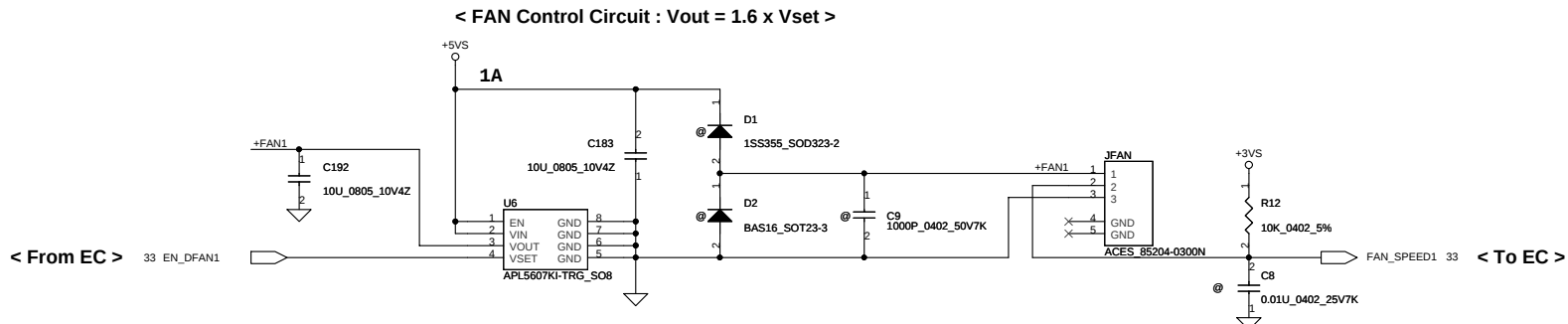
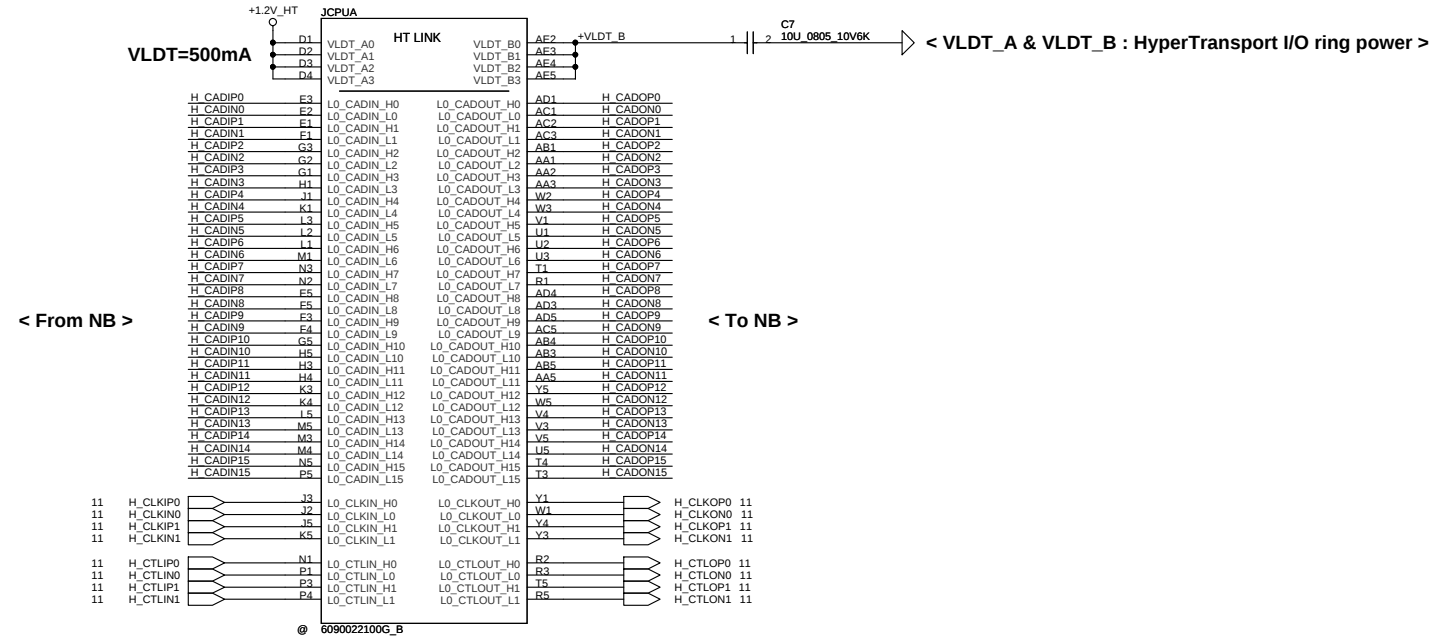
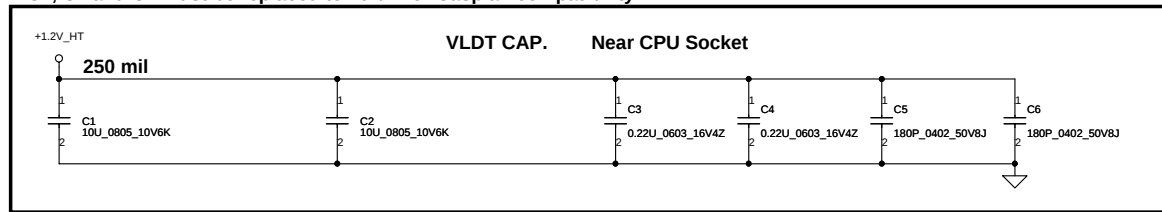
Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WiFi		G- sensor		3 in 1 card reader
Description	(E / A)	(B)	(R)	(S)			(H)				
Explain					16"	17"	Half - size		First	Second	RTS5159
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	WIMAX@	G@ + G_1st@	G@ + G_2nd@	CARD@

Function	FingerPrinter	CAMERA & MIC		HDMI			LVDS wireset	DC-IN		CHIPSET	
Description	(F)	(X)		(Y)							
Explain		CAMERA	MIC	AMD(UMA)	ATI VGA/B	COMMON	Cost down				
BTO	FP@	CAM@	MIC@	IHDMI@	HDMI@	H@	LVDSSET@	16inch_45@	17inch_45@	PUMA@	TIGRIS@

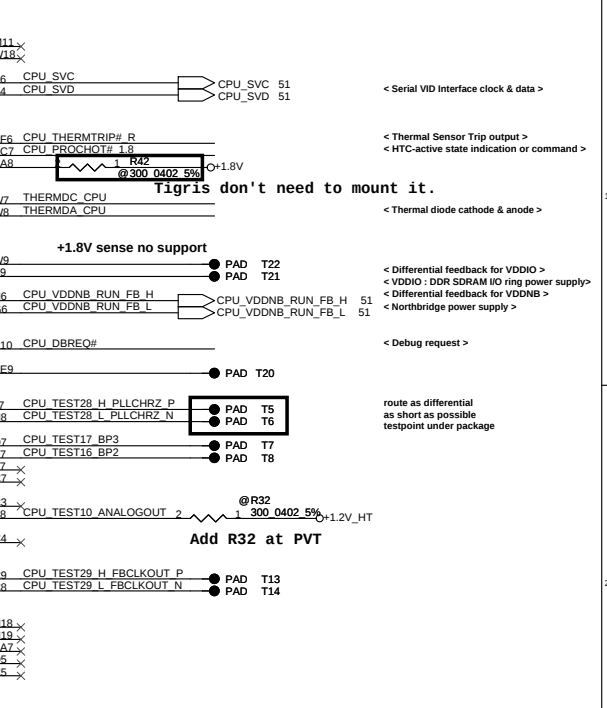
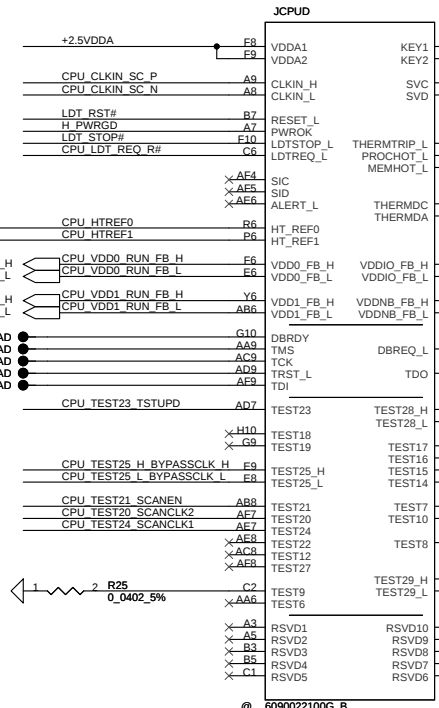
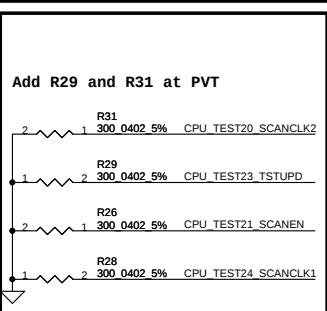
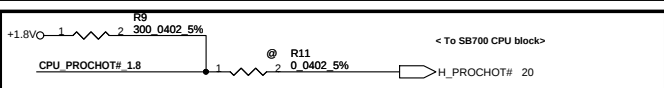
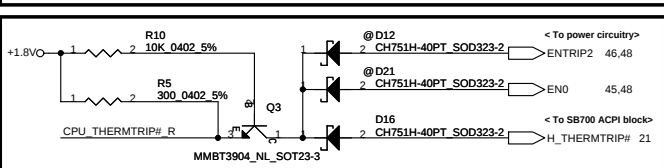
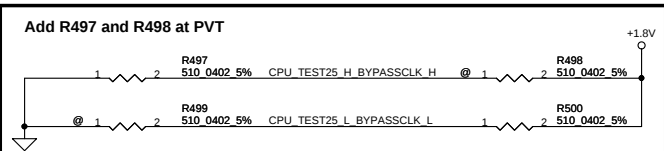
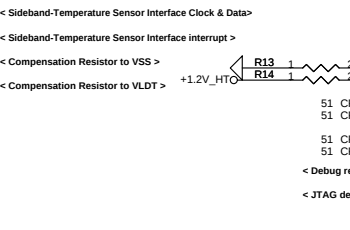
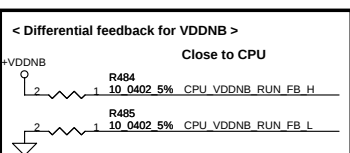
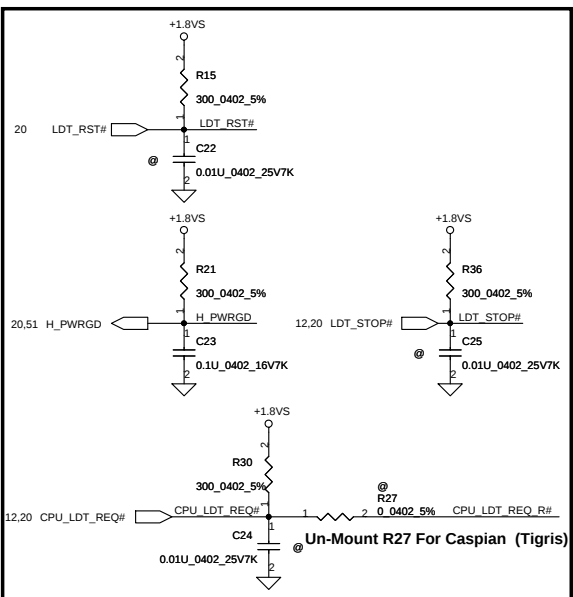
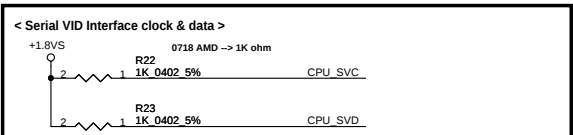
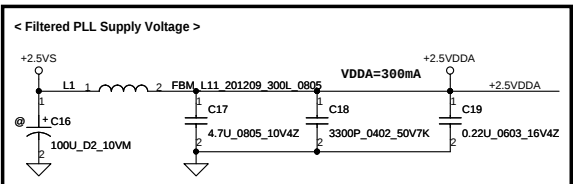
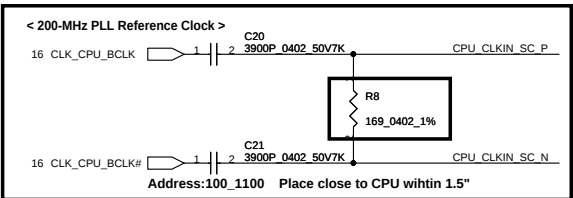
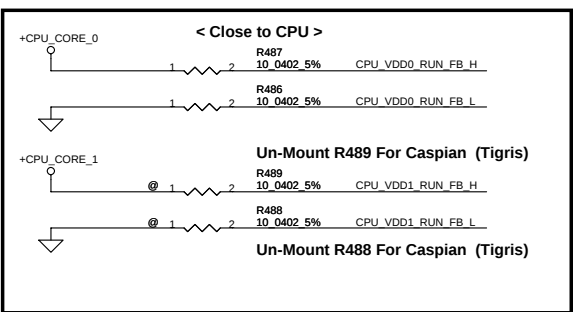
SMBUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	KB926		V	V								
EC_SMB_CK2 EC_SMB_DA2	KB926				V							V
I2C_CLK I2C_DATA	RX881								V			
DDC_CLK0 DDC_DATA0	RX881									V		
DDC_CLK1 DDC_DATA1	RX881											
SCL0 SDA0	SB710					V	V				V	
SCL1 SDA1	SB710							V				
SCL2 SDA2	SB710											
SCL3 SDA3	SB710											

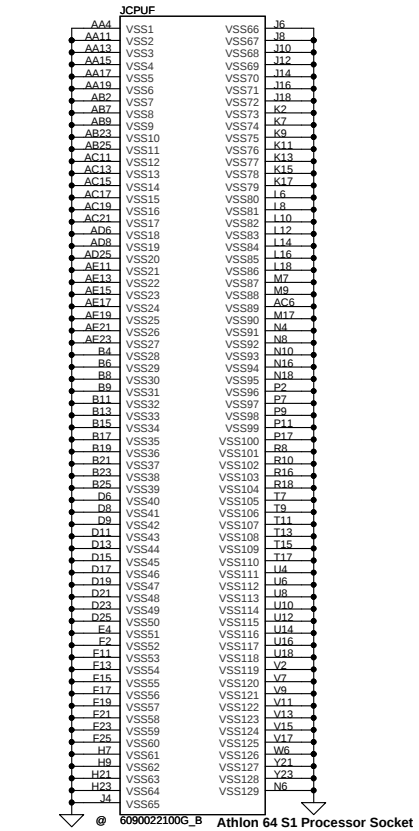
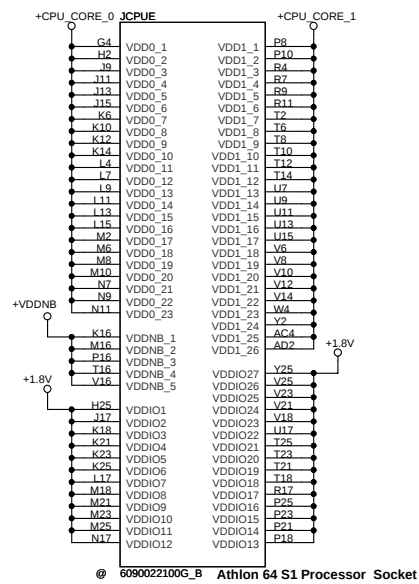
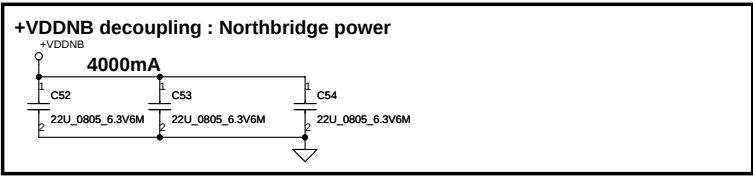
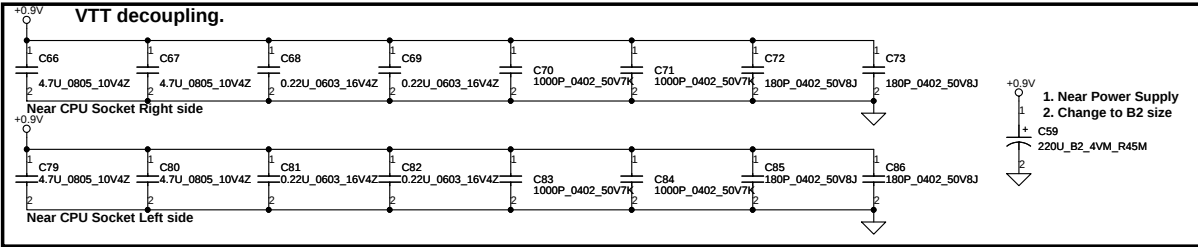
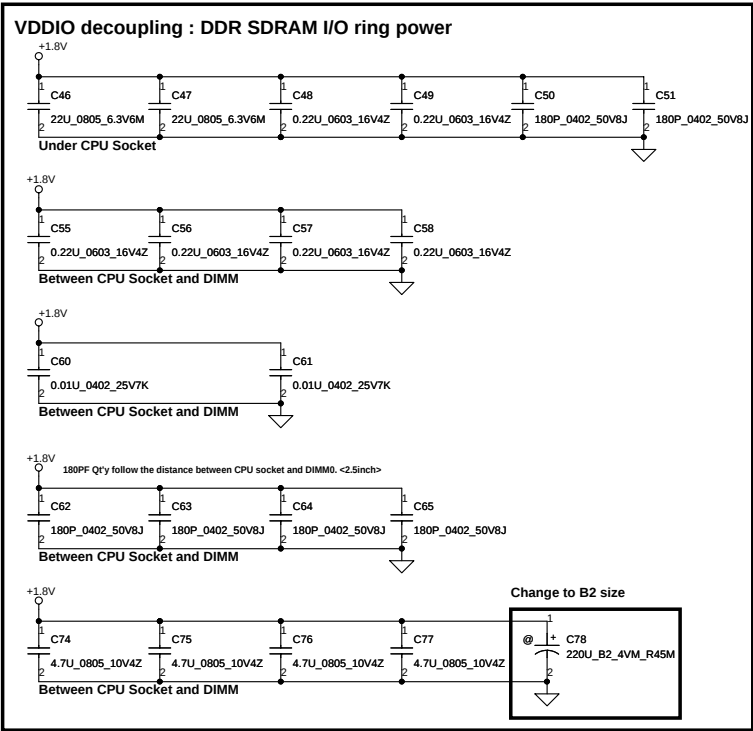
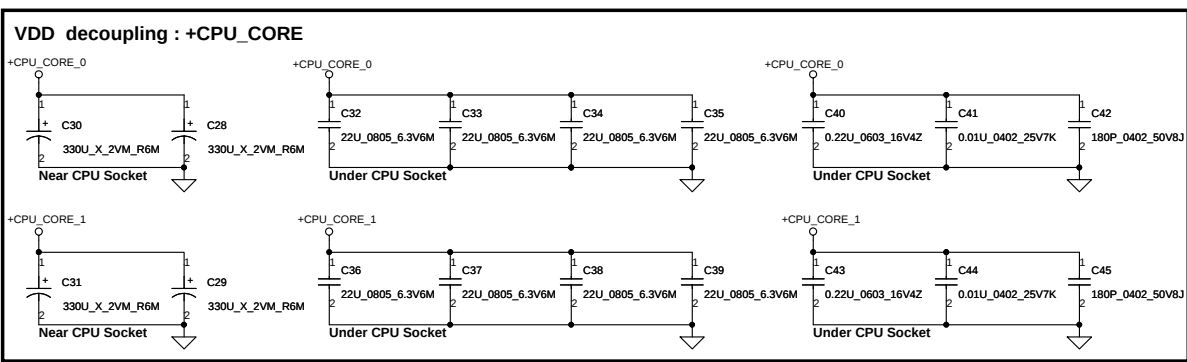
< C1, C2 and C7 must be replaced to 10-uF for Caspian compatibility >



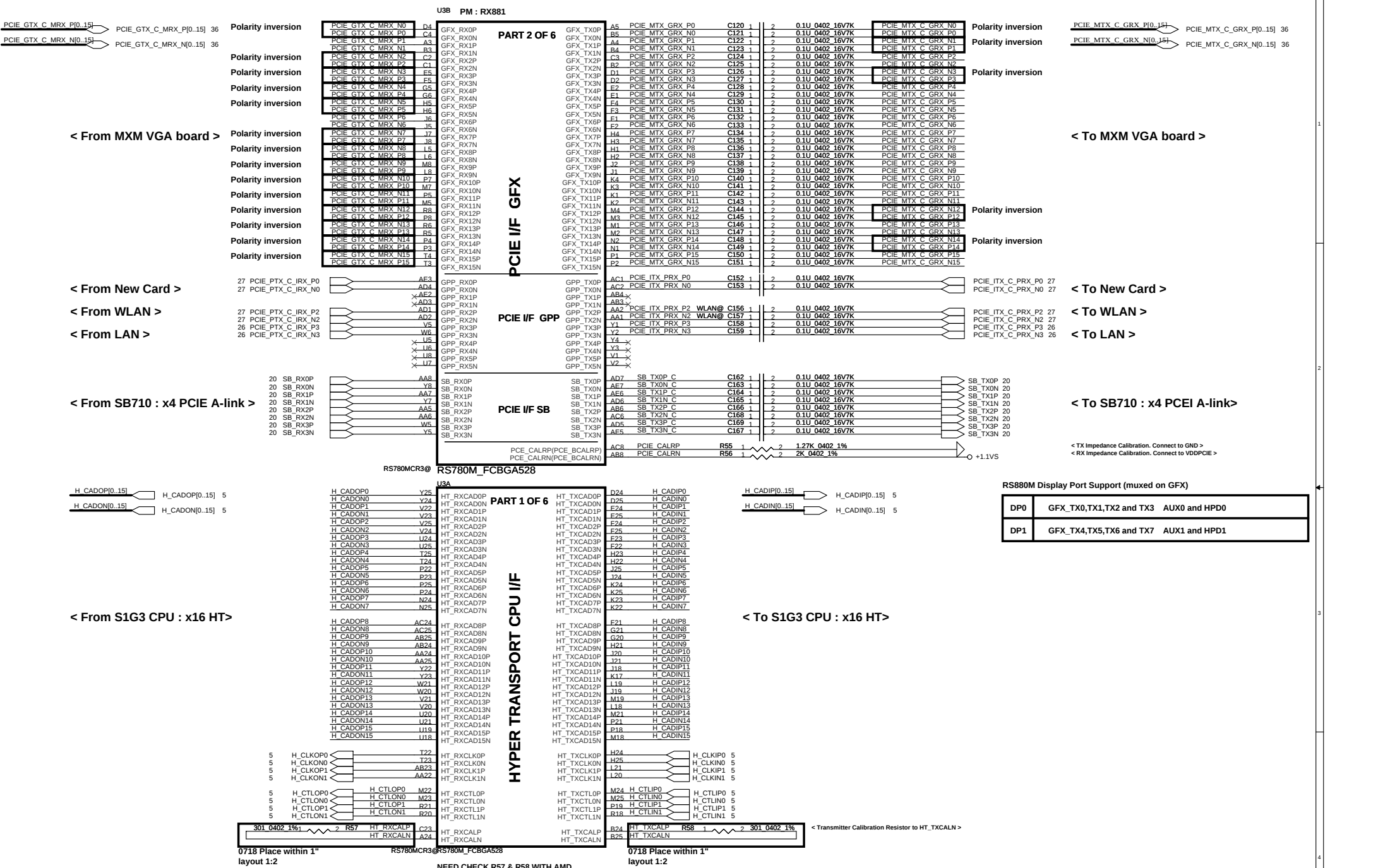
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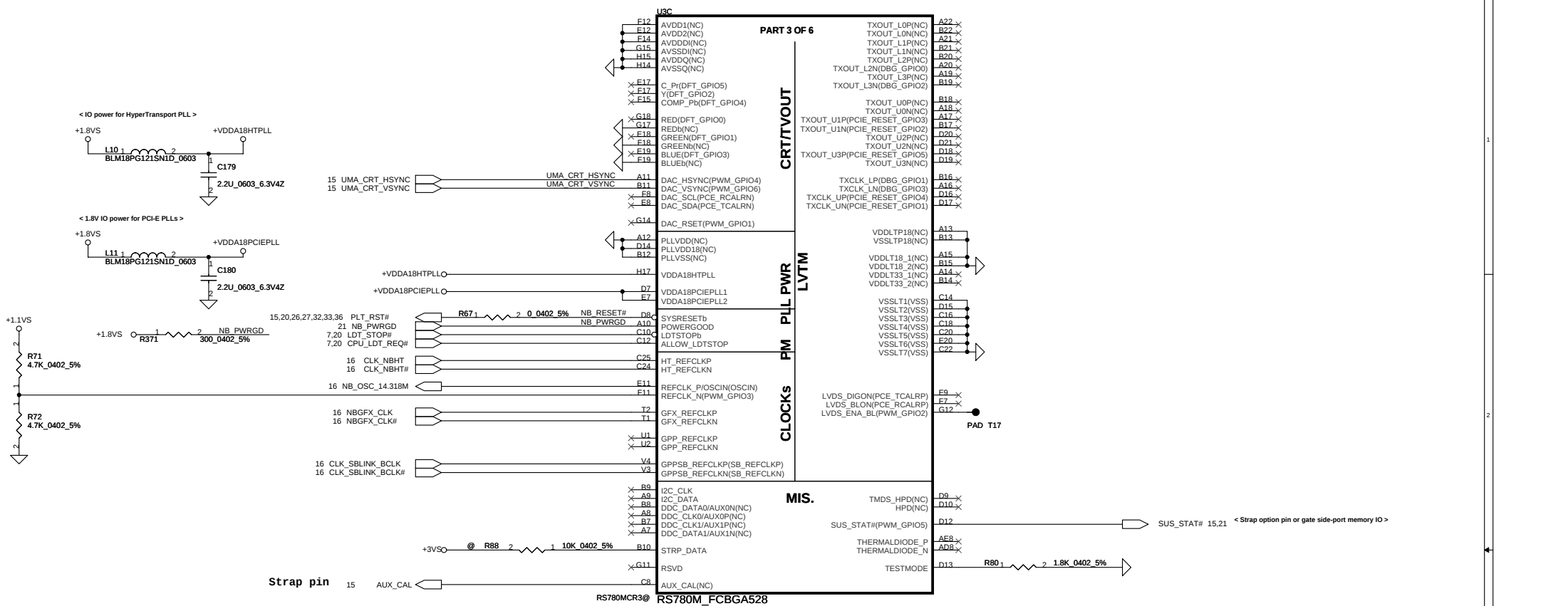


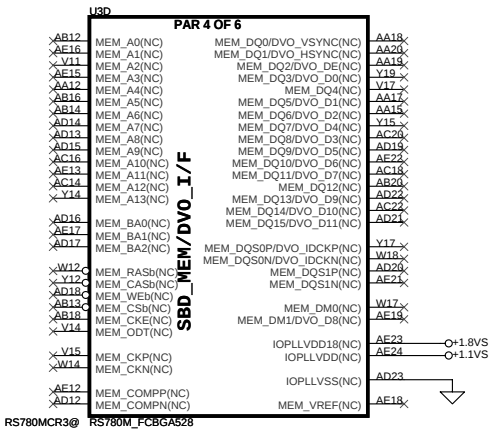
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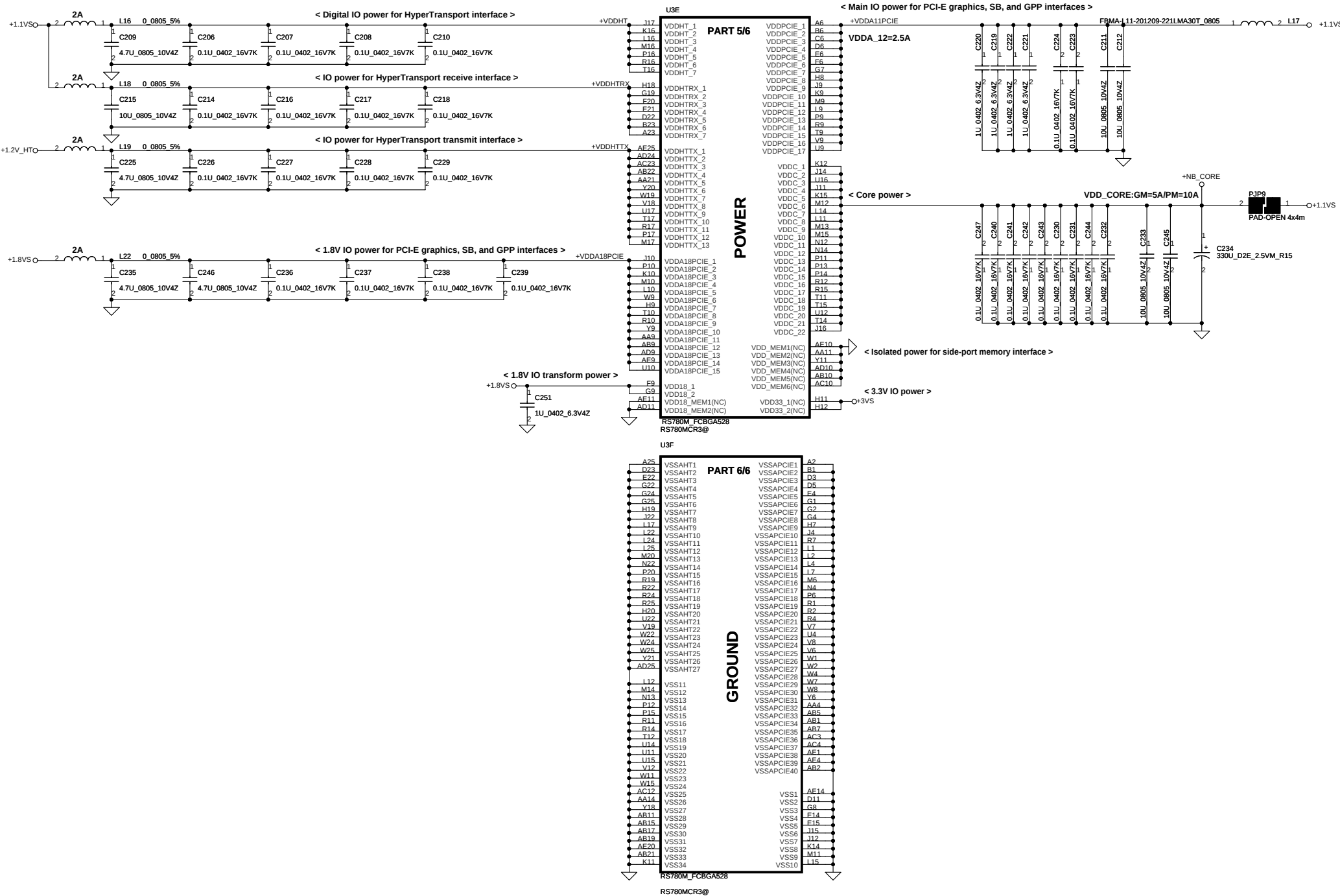
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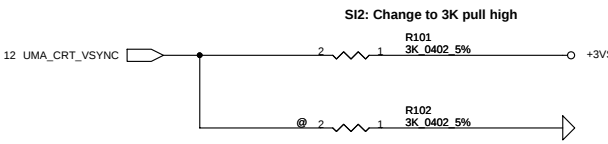
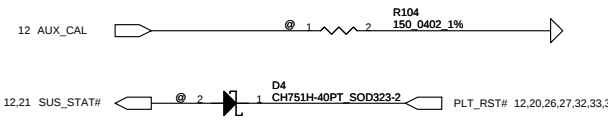
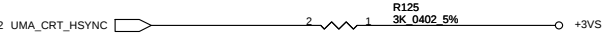




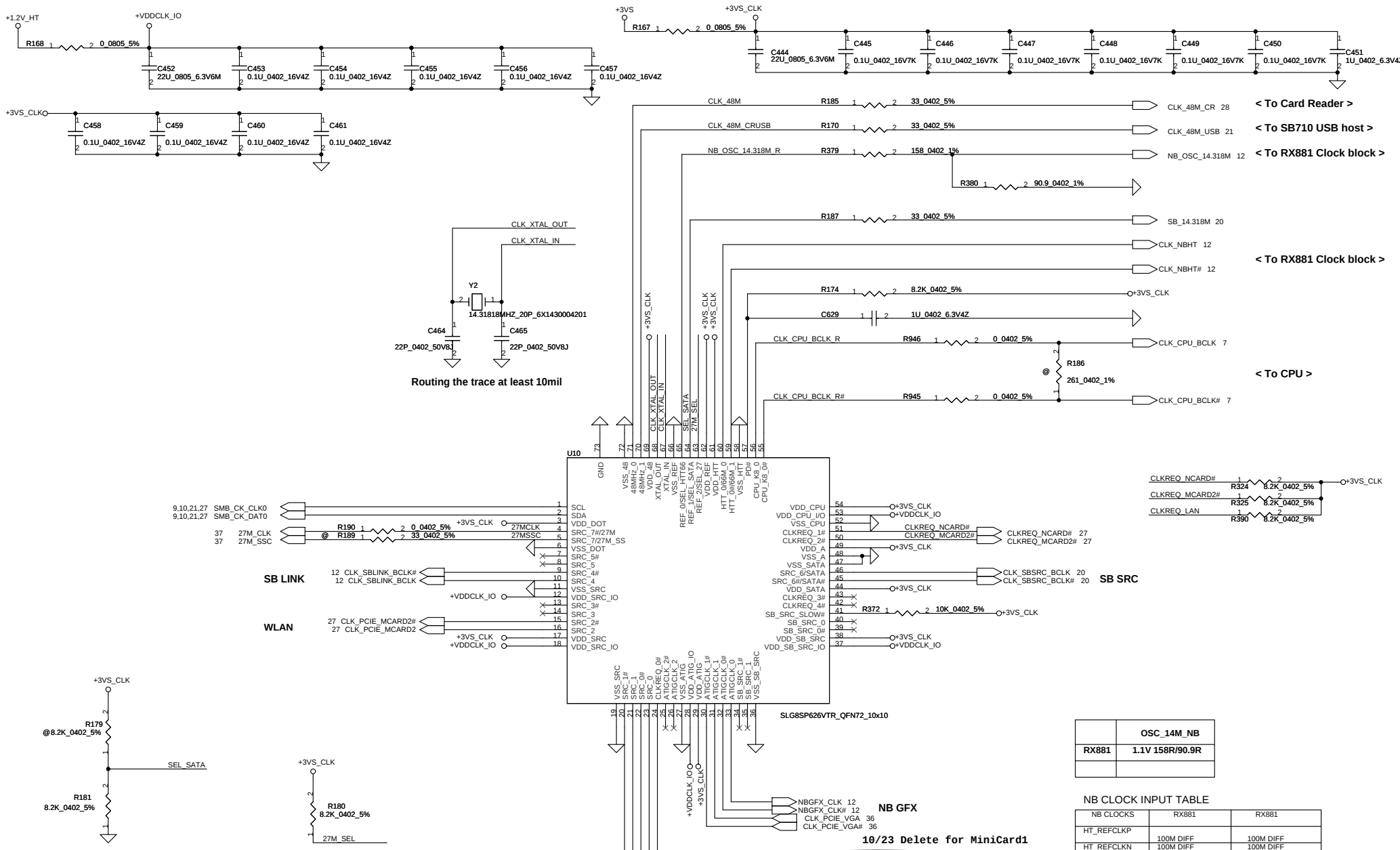
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< RX881 VSYNC mux at CRT_VSYNC pull High to 3K > SI2: Change to 3K pull high 	< VSYNC:STRAP_DEBUG_BUS_GPIO_ENABLEb > Enables the Test Debug Bus using GPIO. 1 : Enable (RX881, RS880) 0 : Disable (RX881, RS880) PIN: RS880--> VSYNC#
< RX881 use register to control PCI-E configure >	< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] > These pin straps are used to configure PCI-E GPP mode. 000 : 00001 001 : 00010 010 : 01011 011 : 00100 100 : 01010 101 : 01100 111 : 01011
< RX881 SUS_STAT# > 	< SUS_STAT# : LOAD_EEPROM_STRAPS > Selects Loading of STRAPS from EPROM 1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected RX881:SUS_STAT#
< RX881 use HSYNC to enable SIDE PORT (internal pull high) > 	< HSYNC: STRAP_DEBUG_BUS_PCIE_ENABLEb > RX881: Enables the Test Debug Bus using PCIE bus 1 : Disable (Can still be enabled using nbcfg register access) 0 : Enable RS880: Enables Side port memory (RS780 use HSYNC#) 1. Disable (RS780) 0 : Enable (RS780)

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SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC 6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC 7 output * default

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output * default

	OSC 14M_NB
RX881	1.1V 158R/90.9R

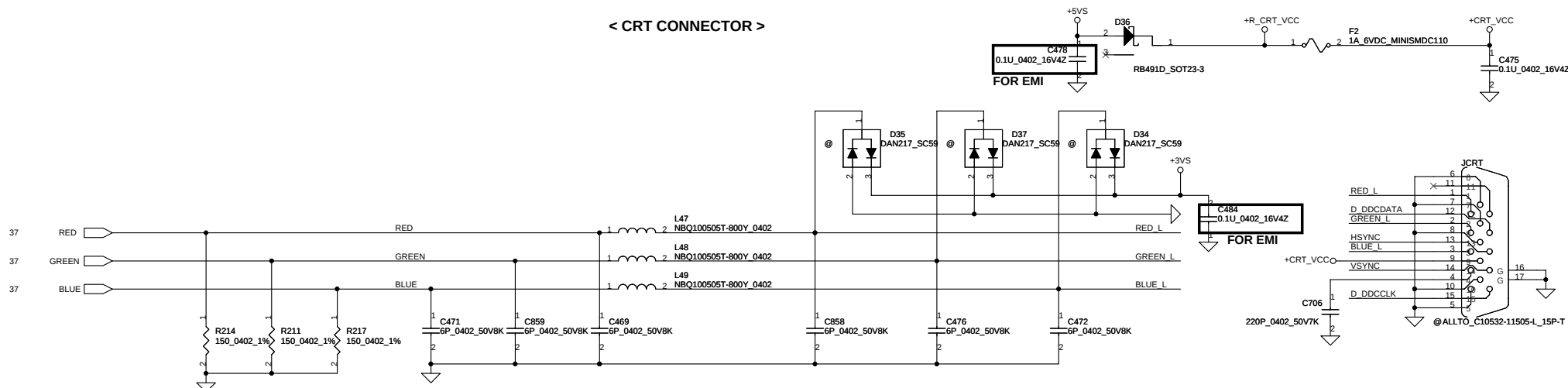
NB CLOCK INPUT TABLE

NB CLOCKS	RX881	RX881
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

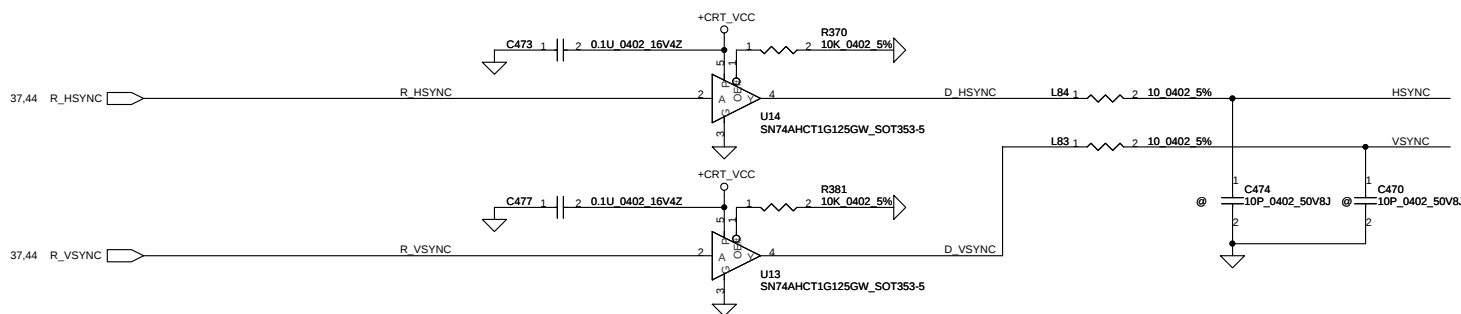
Use voltage divider resistor R379 & R380 to pull low

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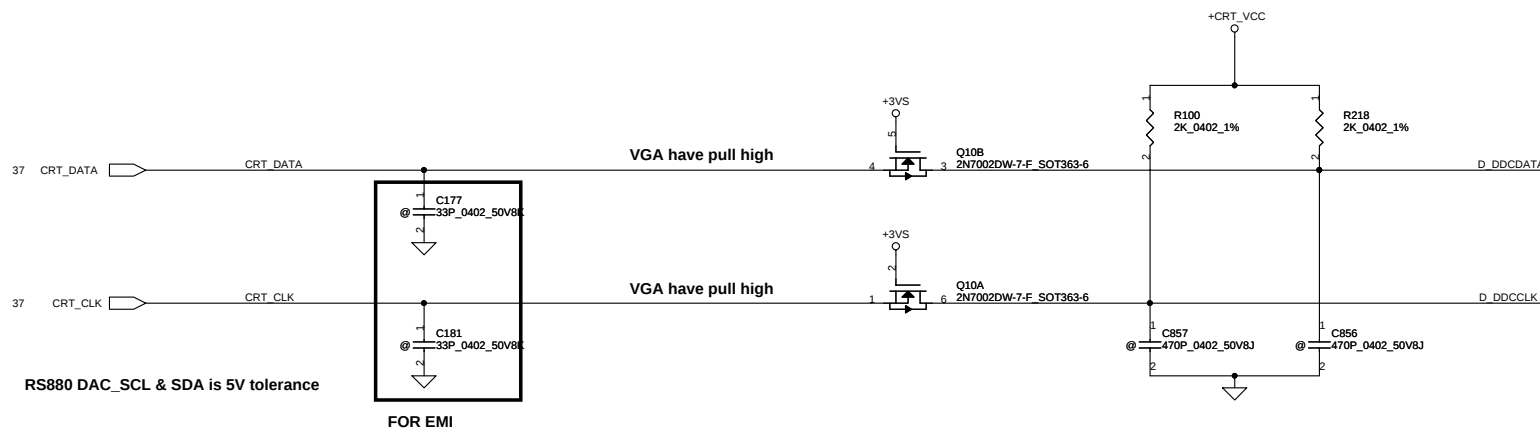
< CRT CONNECTOR >



RS780 use 140 ohm, check RS880 use what value



< SYNC SIGNAL >



< Display Data Channel >

RS880 DAC_SCL & SDA is 5V tolerance

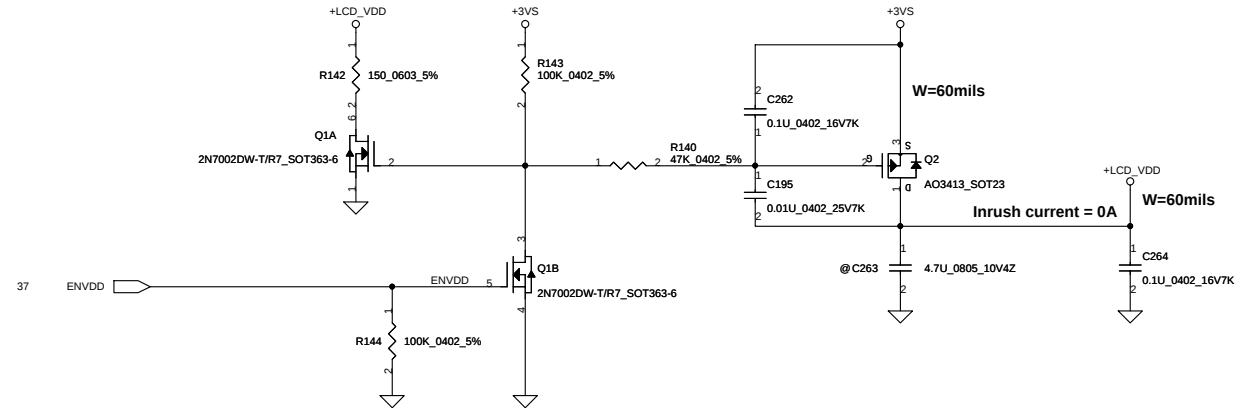
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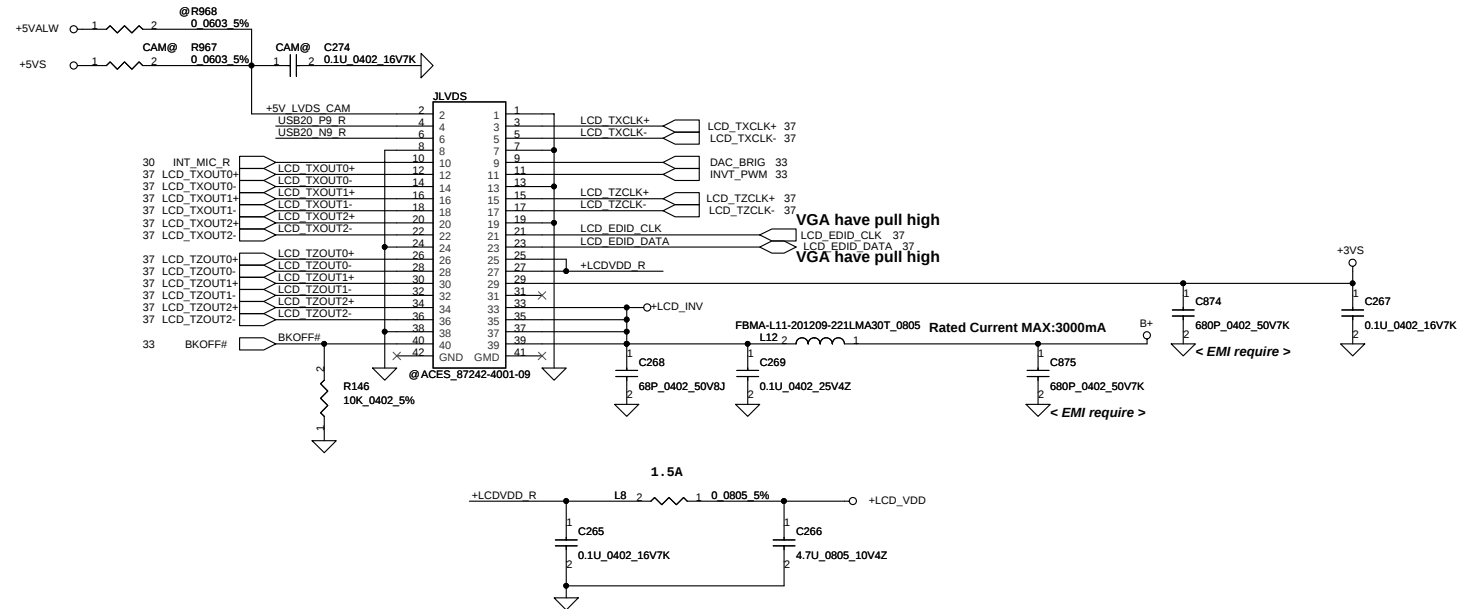
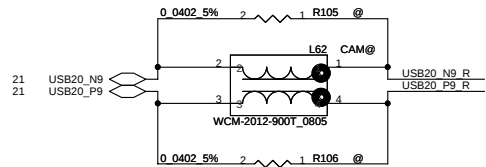
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LCD/PANEL BD. Conn.



< Int. Camera, USB port 9 >

< EMI require >

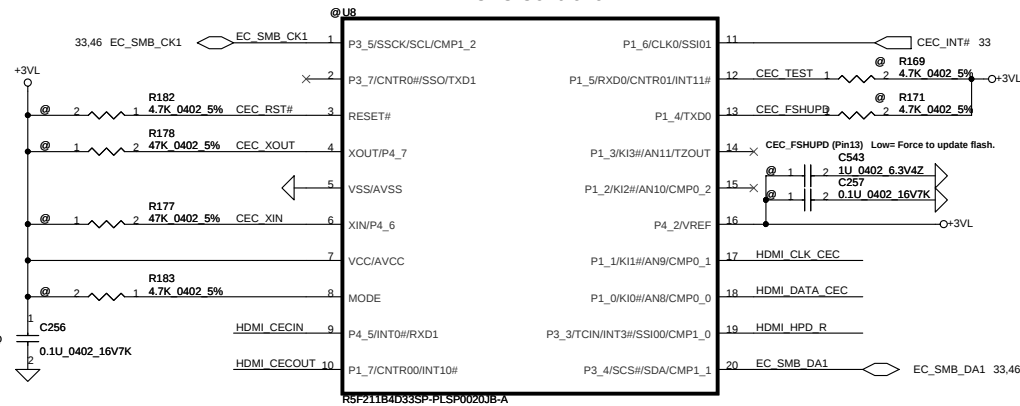


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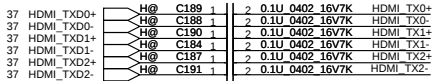
Compal Electronics, Inc.

Schematic, M/B LA-5331P

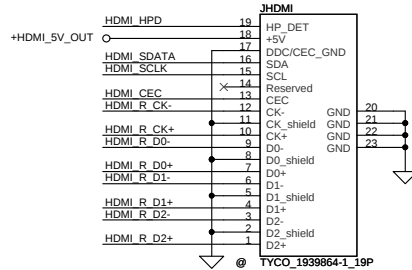
< HDMI CEC Controller >



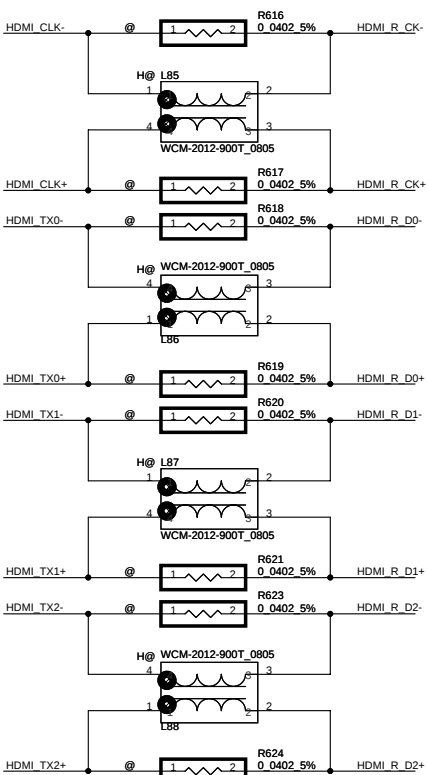
SI:Add R616~R624 for EMI request



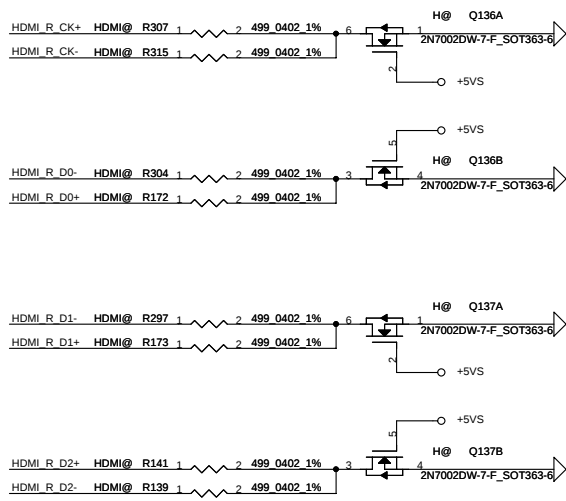
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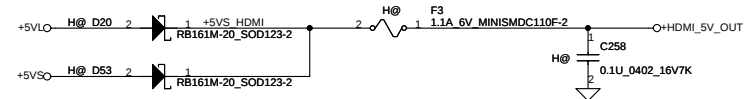
< EMI solution >



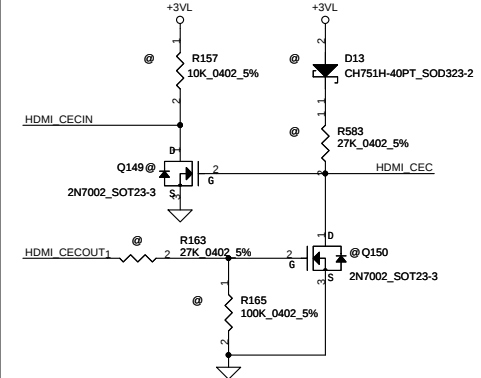
< Termination resistor >



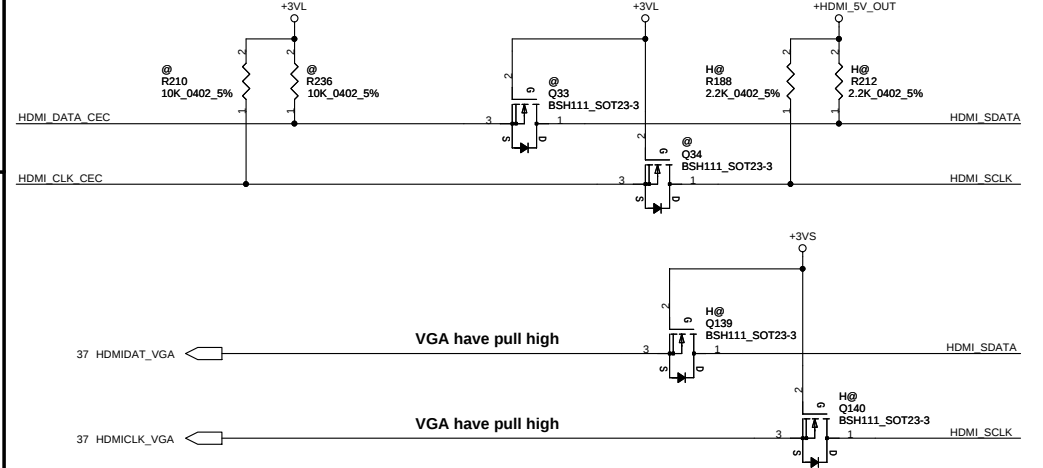
< Power, reset and crystal >



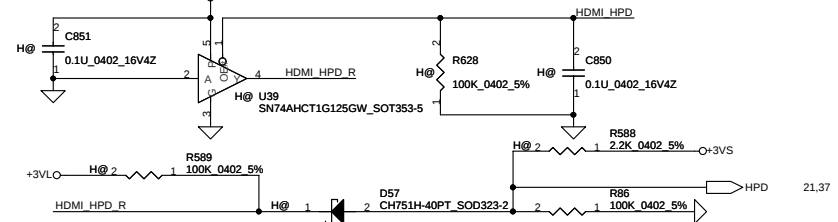
< HDMI_CEC level shift=Place MOSFET close to HDMI connector >



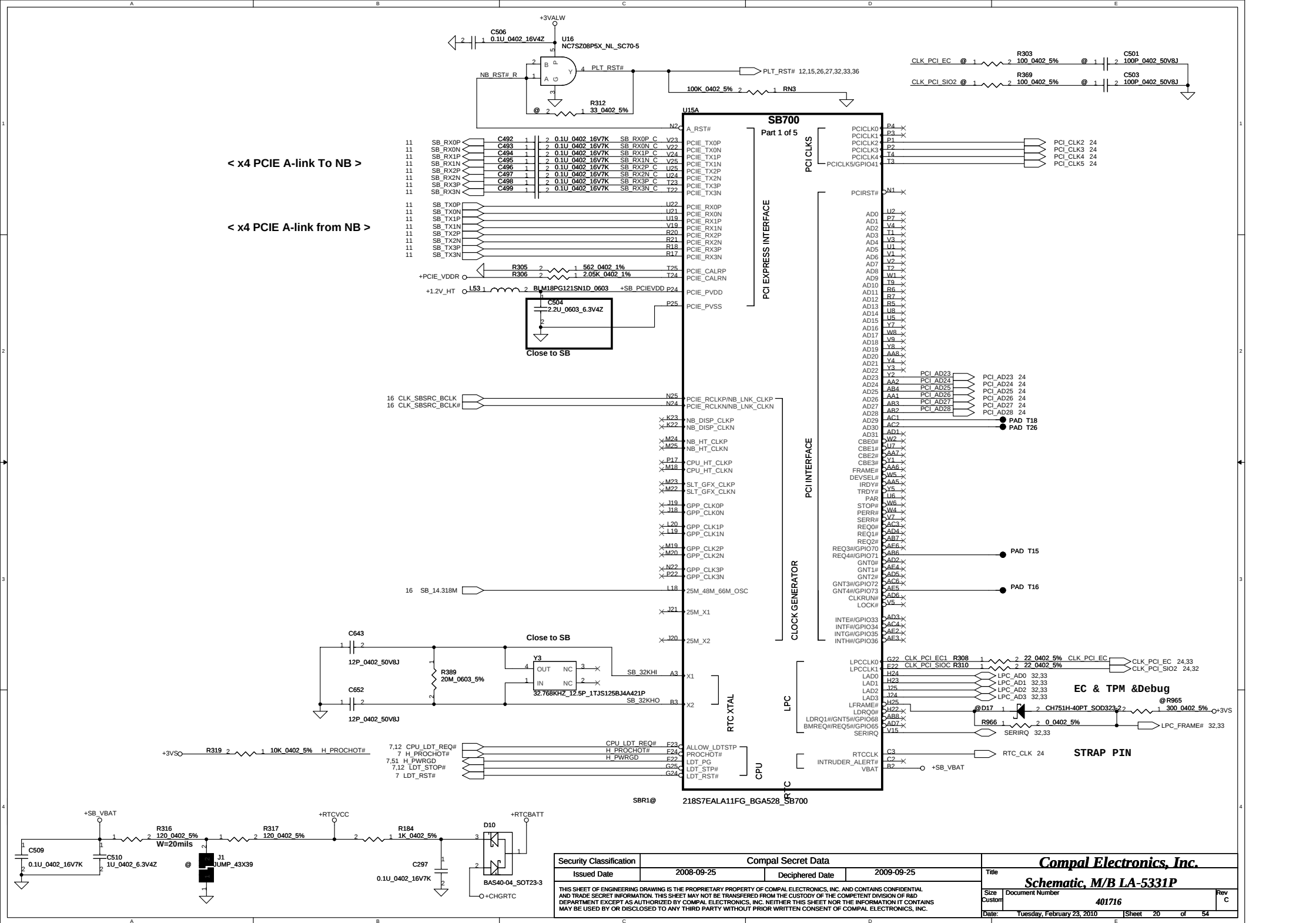
< HDMI DDC channel to device >

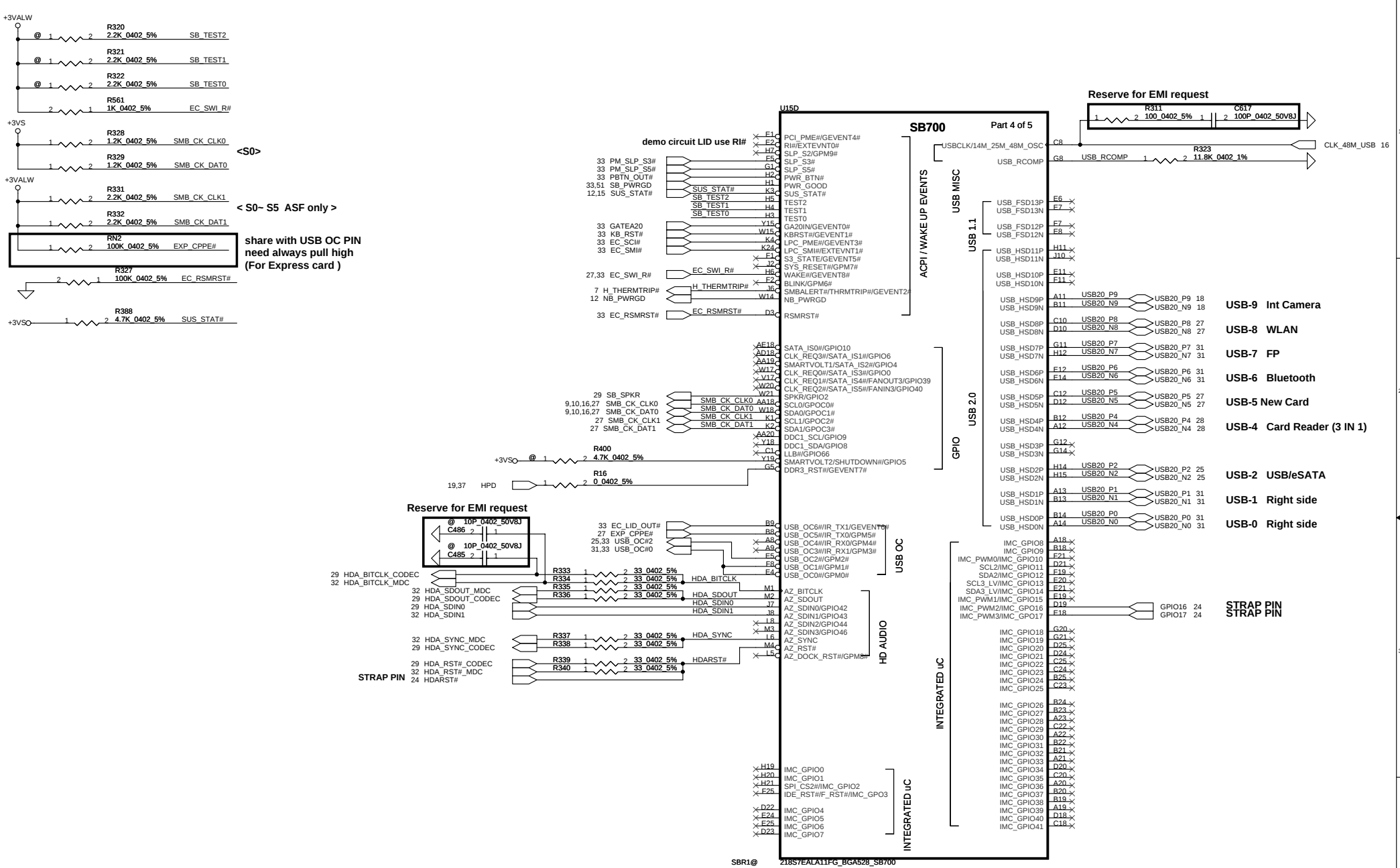


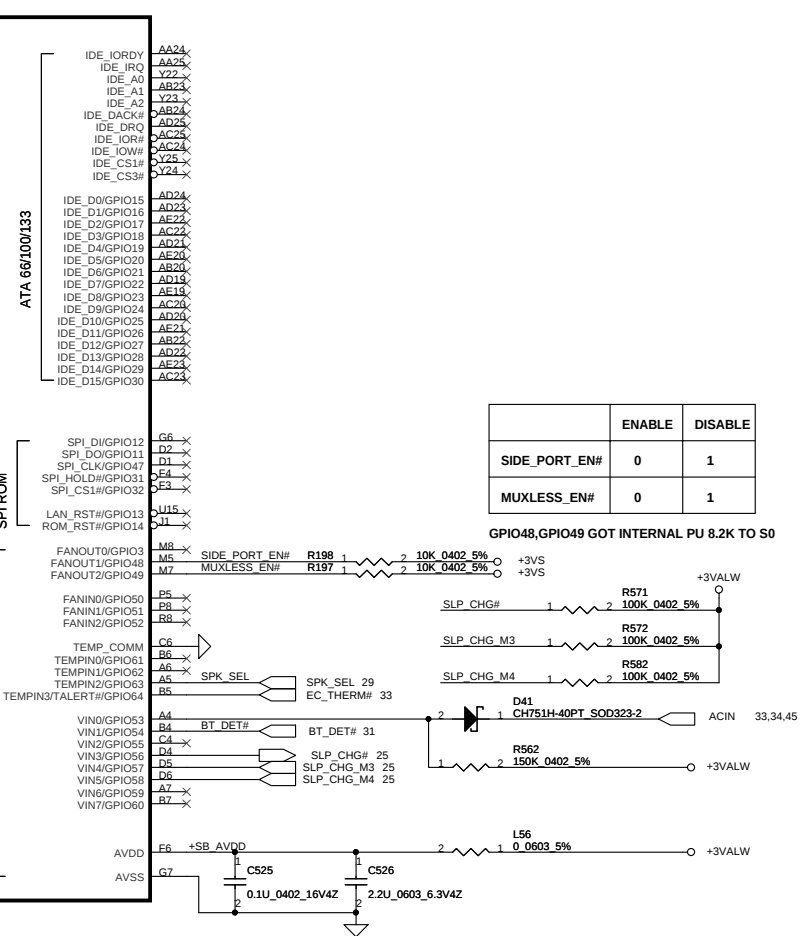
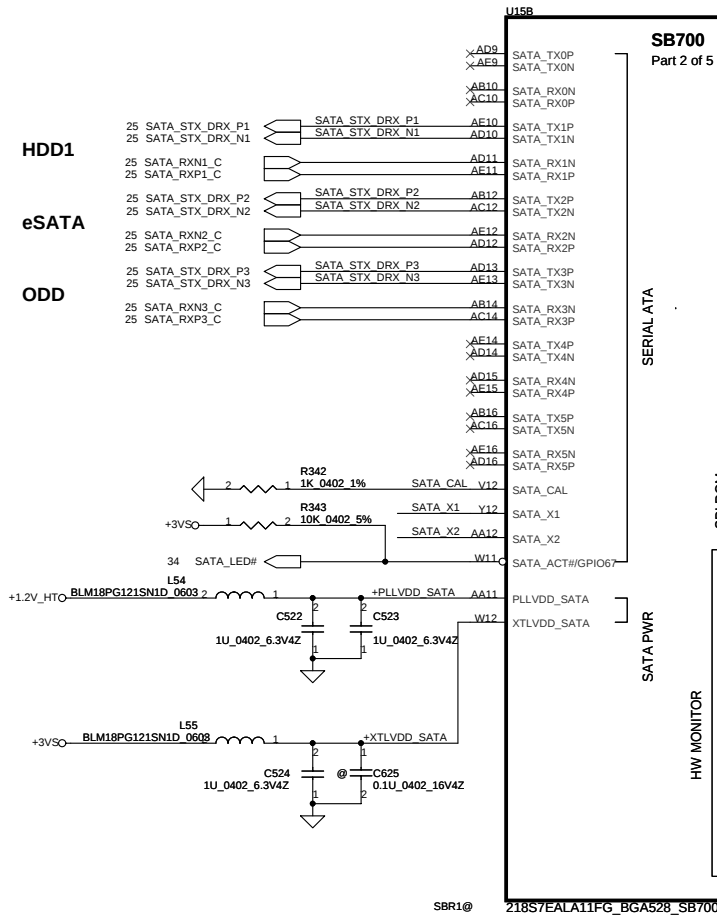
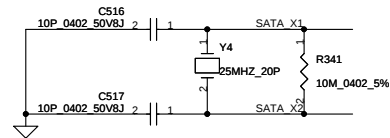
< Hot-plug detection & level shift >



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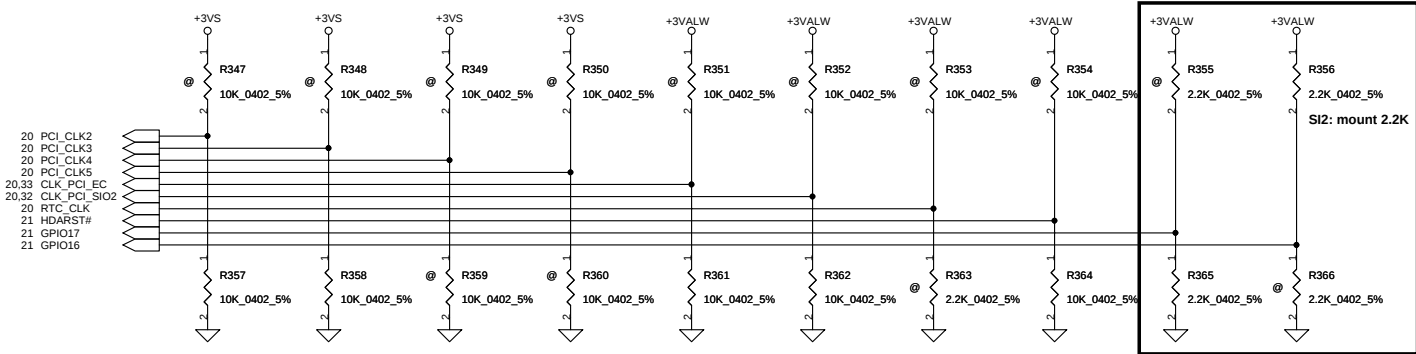




REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM

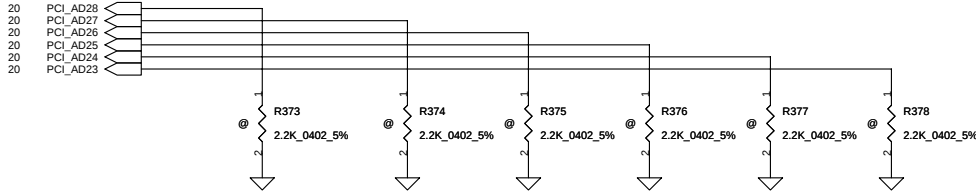


Need to confirm if SB SPI ROM will mount

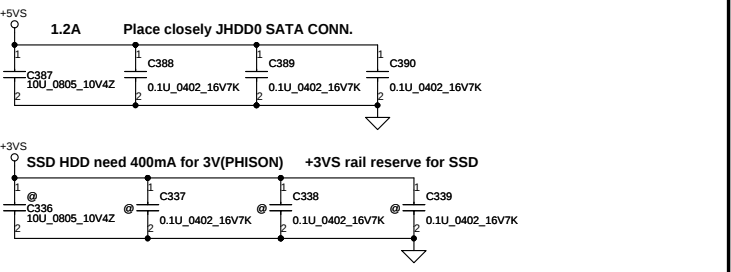
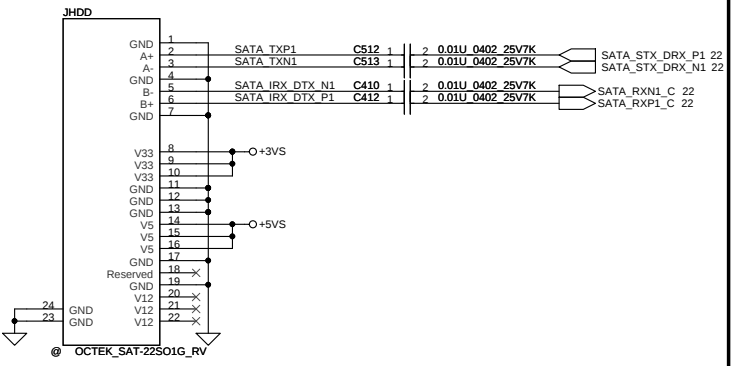
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

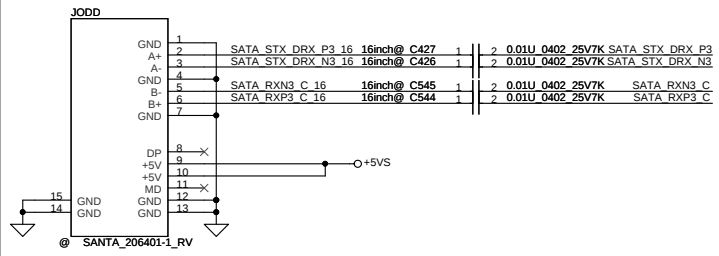
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



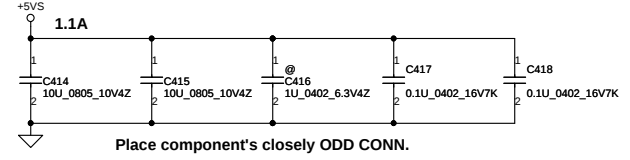
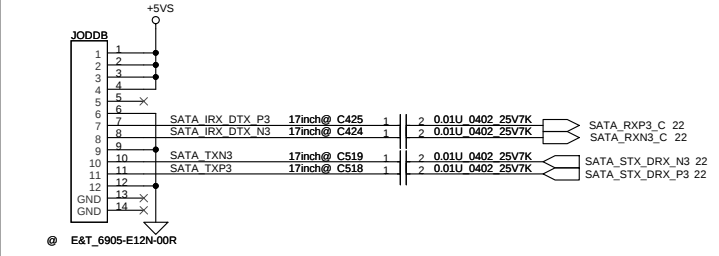
< SATA HDD1 Conn >



< 16" SATA ODD Conn >

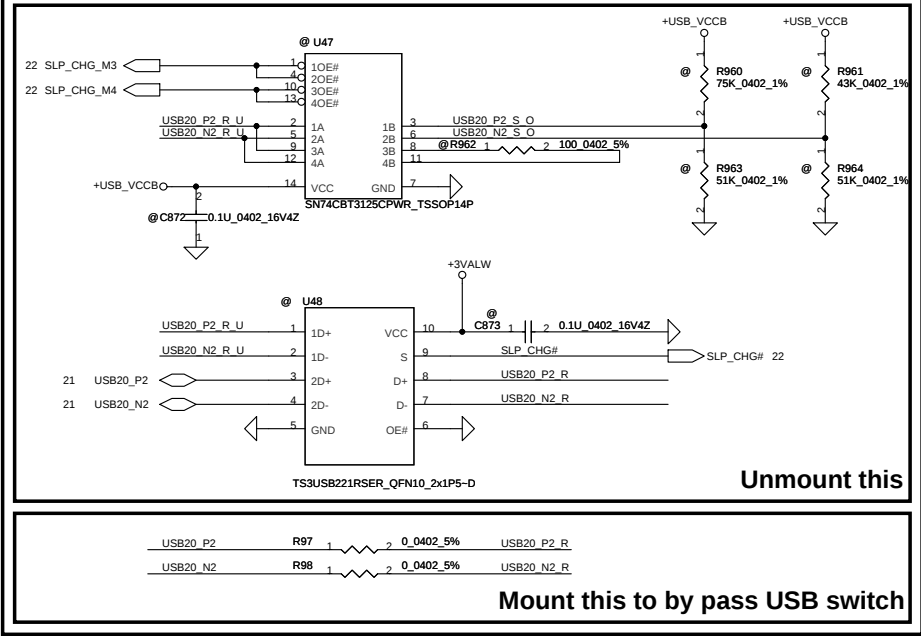


< 17" SATA ODD Conn >

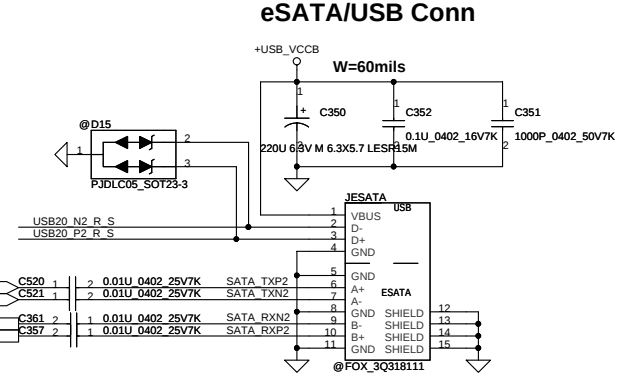
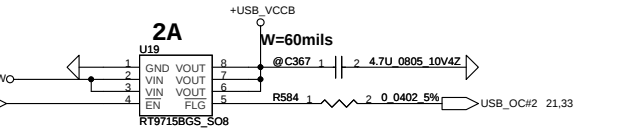
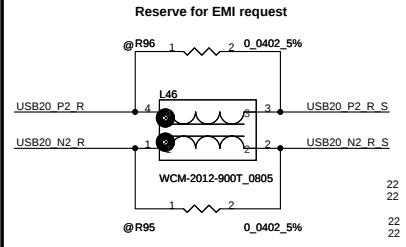


< eSATA/USB >

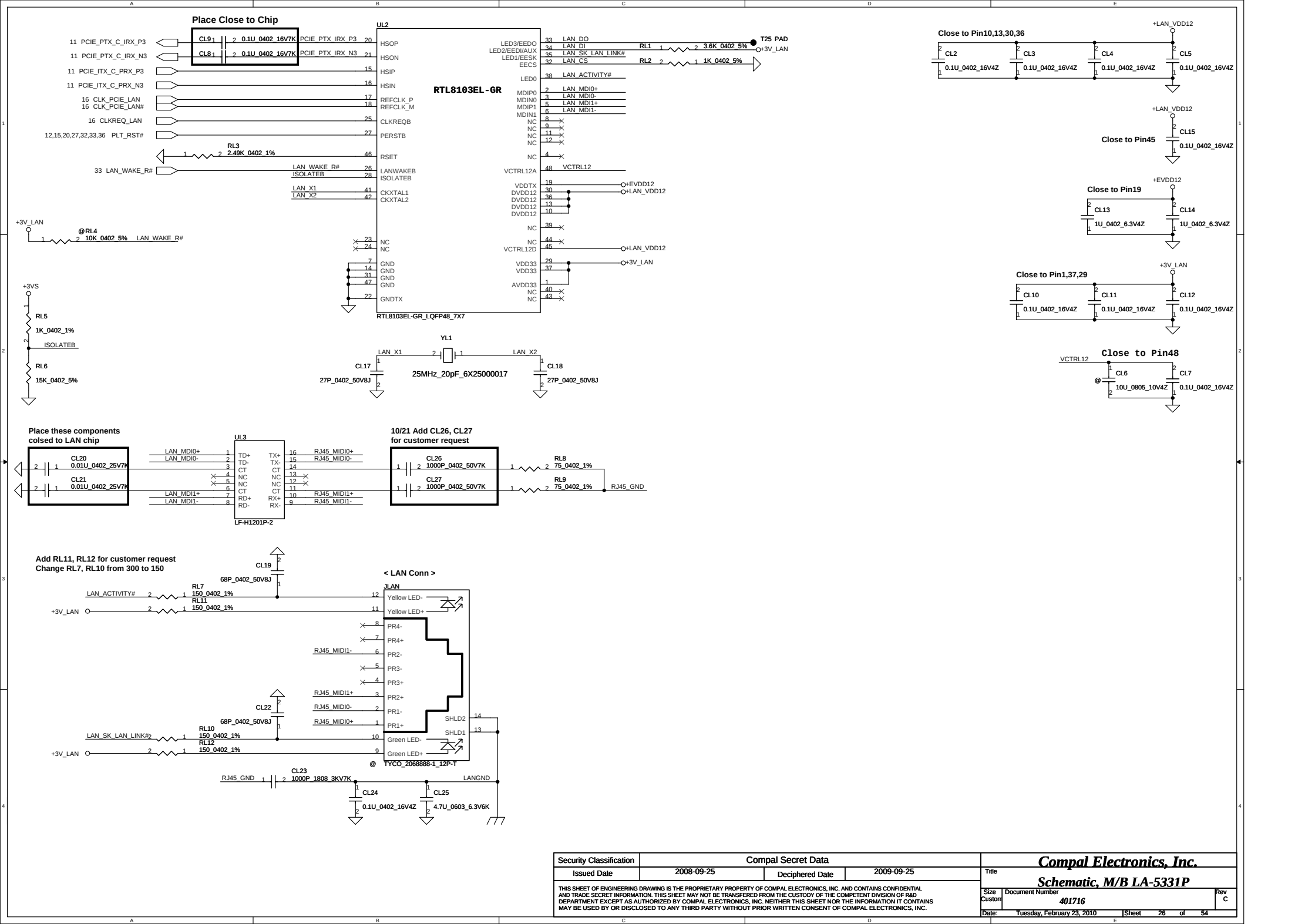
10/22 Add for USB Sleep & Charge M3/M4



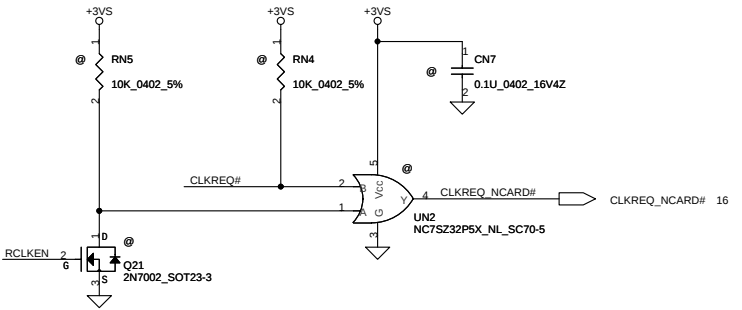
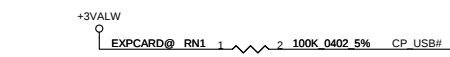
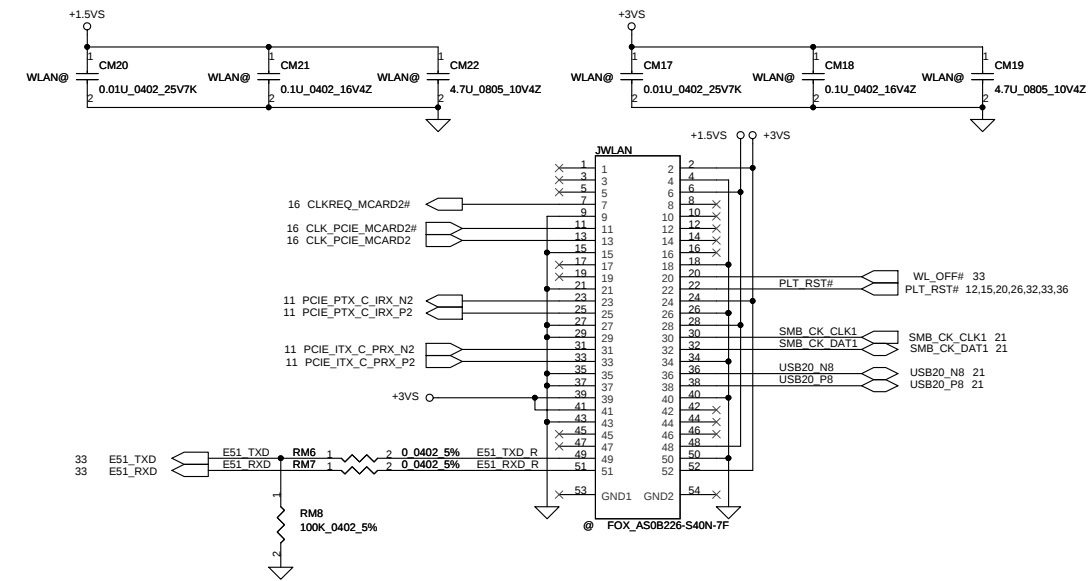
	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG#	FUNCTION
Mode 3	HIGH	LOW	LOW	D=1D
Mode 4	LOW	HIGH	HIGH	D=2D



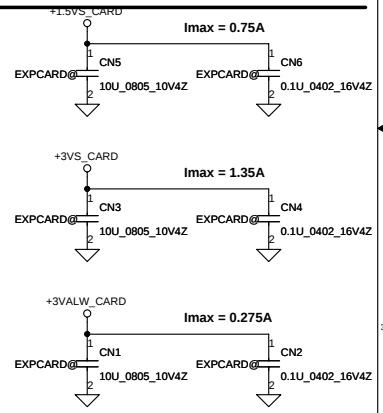
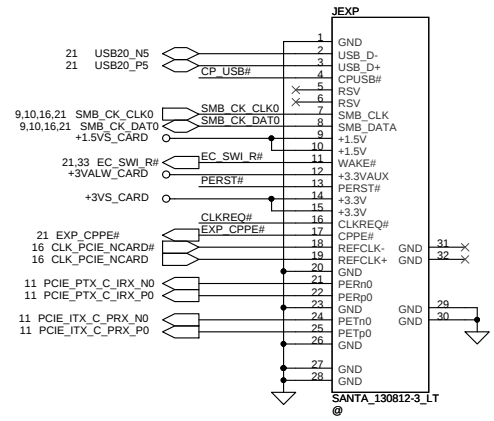
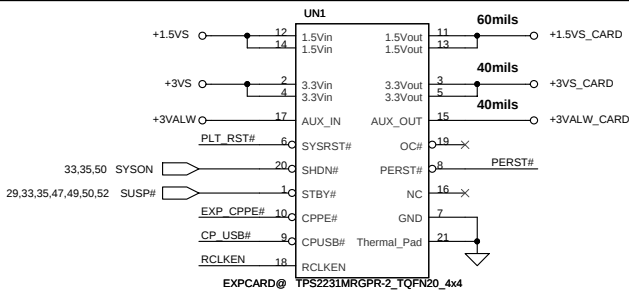
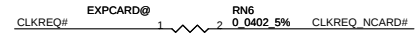
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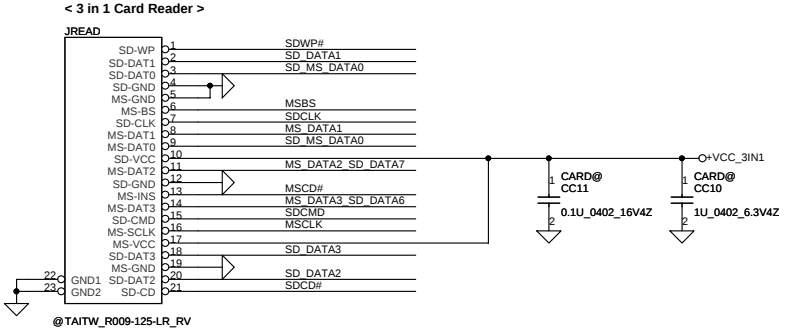
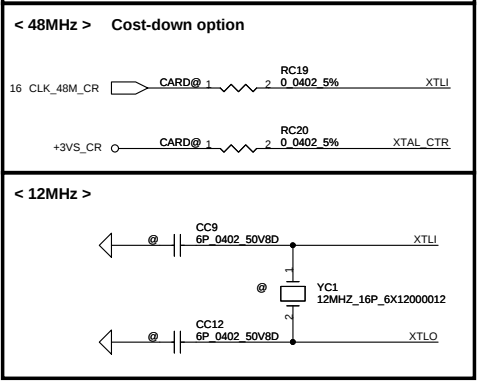
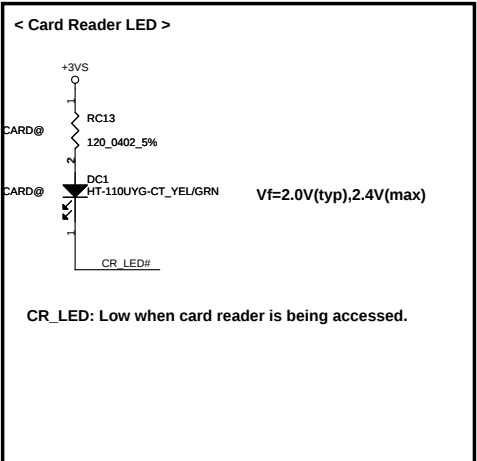
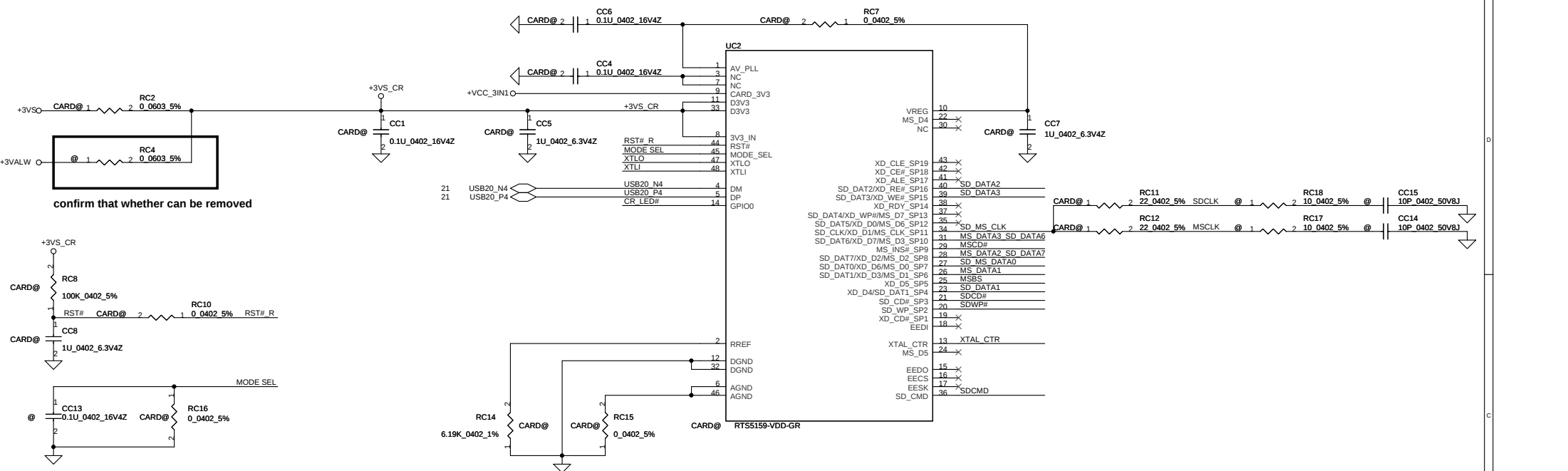
< PCIe Mini Card for WLAN >



< Reserve for test >

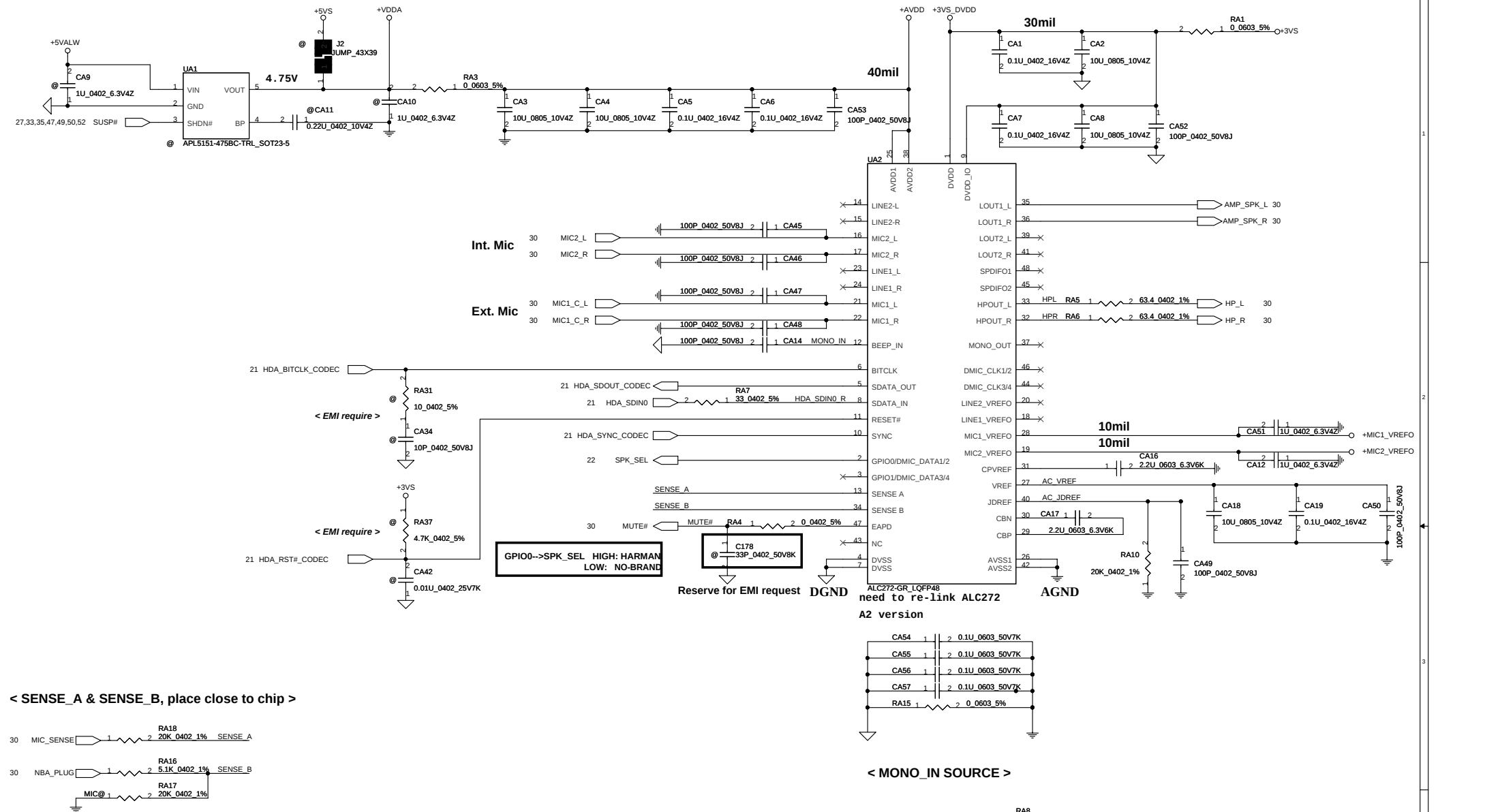


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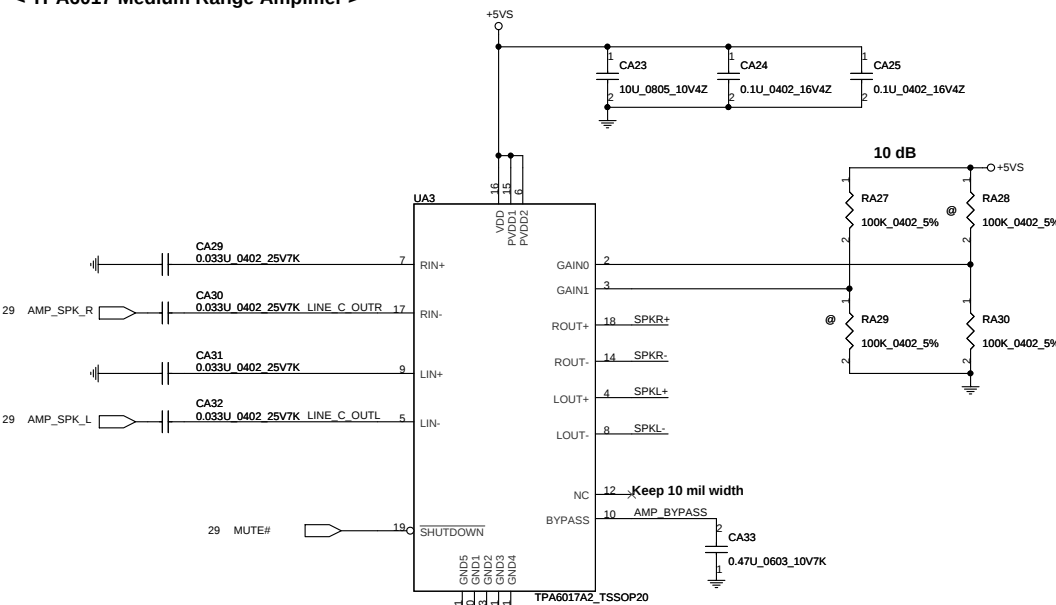
R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

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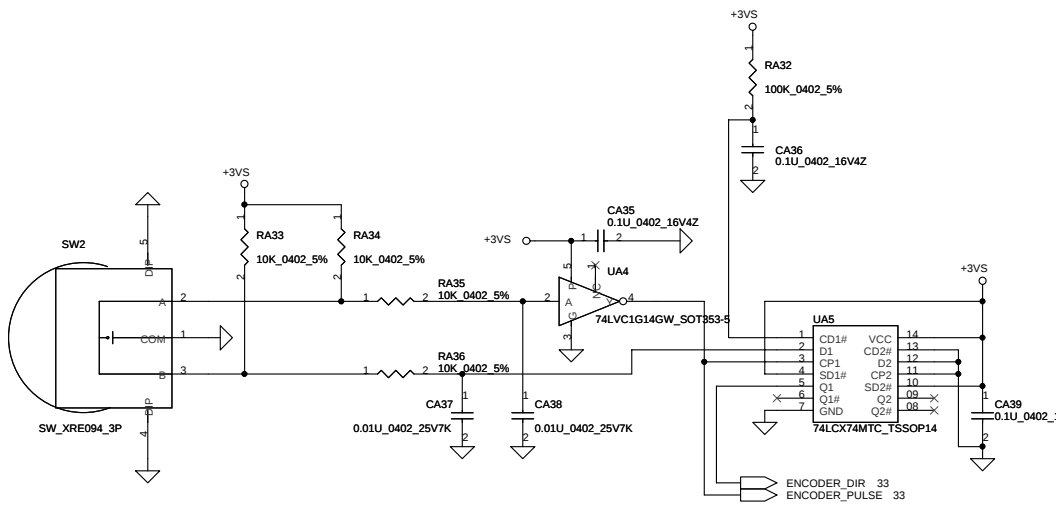


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

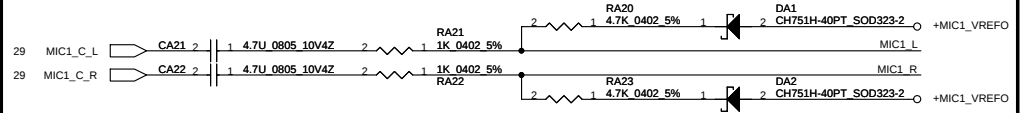
< TPA6017 Medium Range Amplifier >



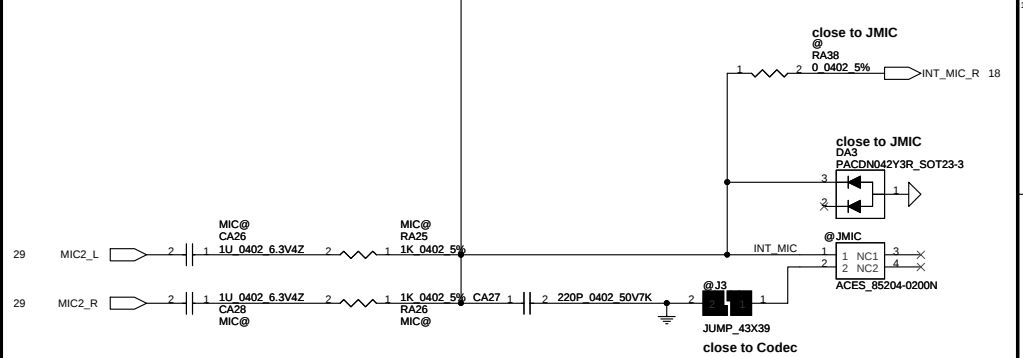
< Volume Control >



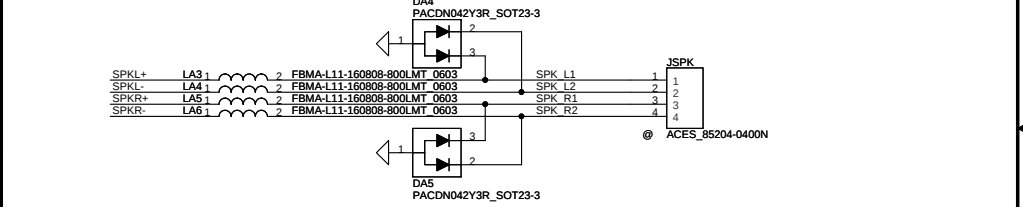
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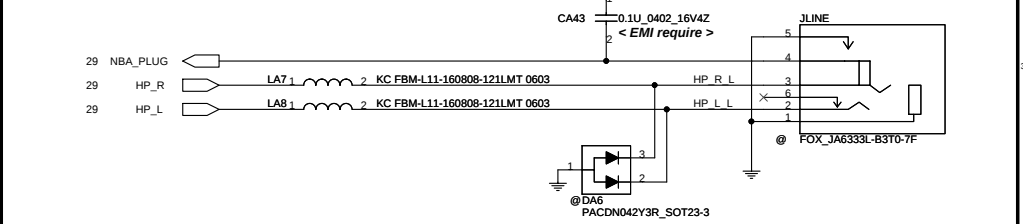
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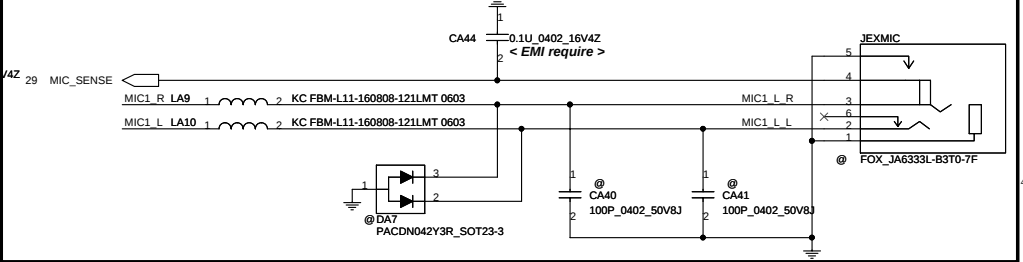
< Speaker Connector >



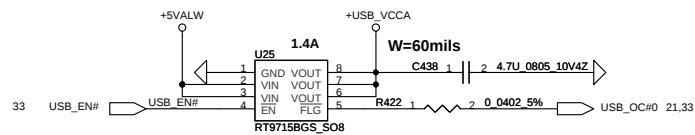
< HeadPhone JACK >



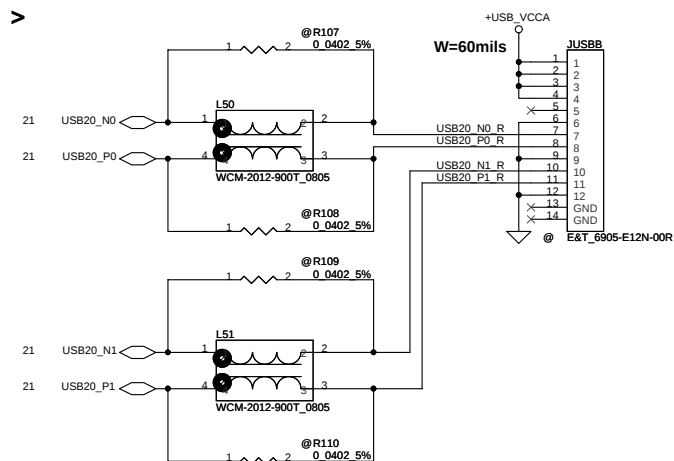
< Ext.MIC/LINE IN JACK >



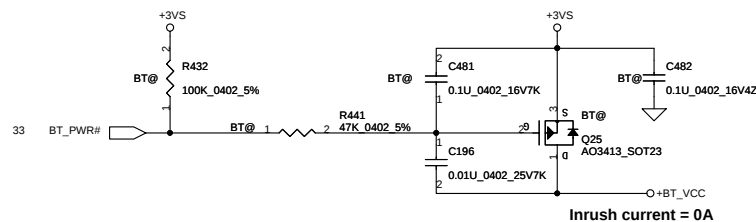
< USB Right-side Board, USB port 0,1 >



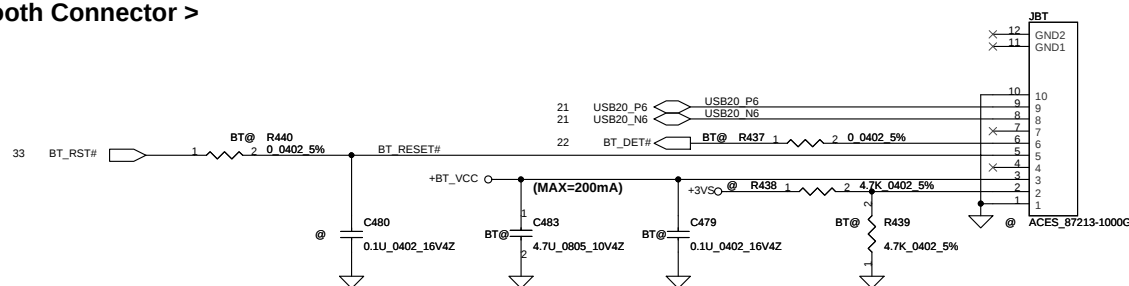
< Reserve for EMI request >



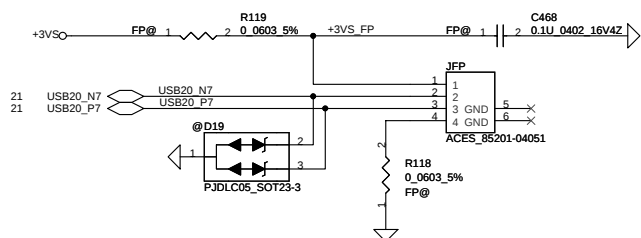
< BlueTooth Interface, USB port6 >



< Bluetooth Connector >



< Finger Printer, USB port 7 >



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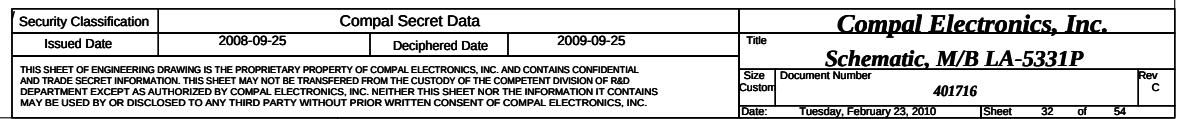
Compal Electronics, Inc.
Schematic, M/B LA-5331P

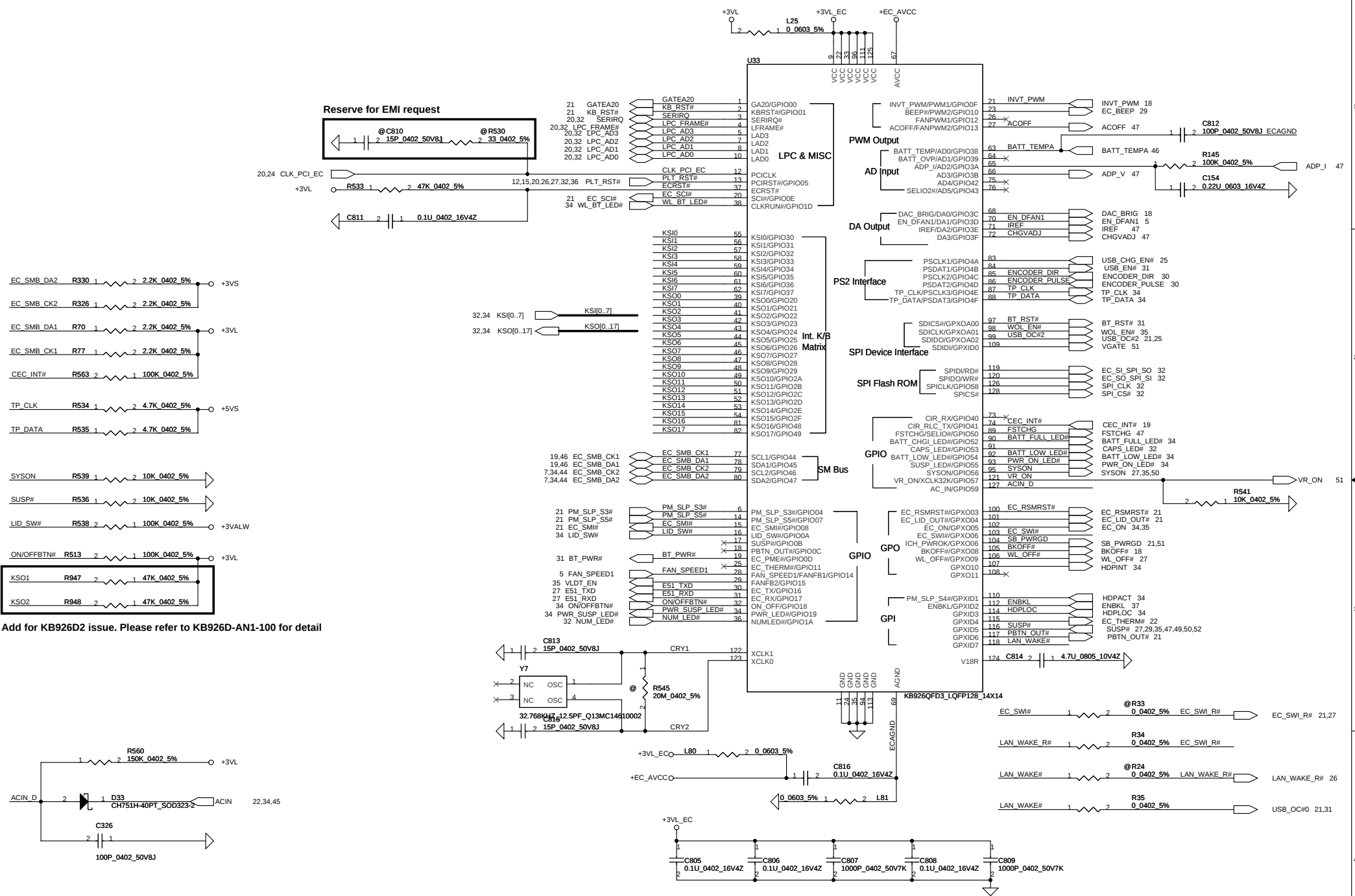
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< MDC 1.5 Conn >

< For EMI >

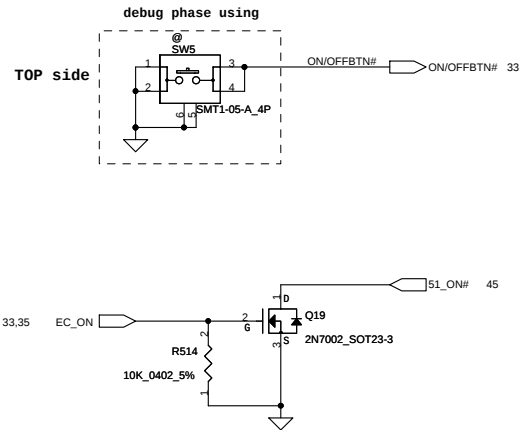




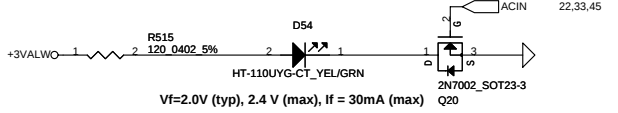
Add for KB926D2 issue. Please refer to KB926D-AN1-100 for detail

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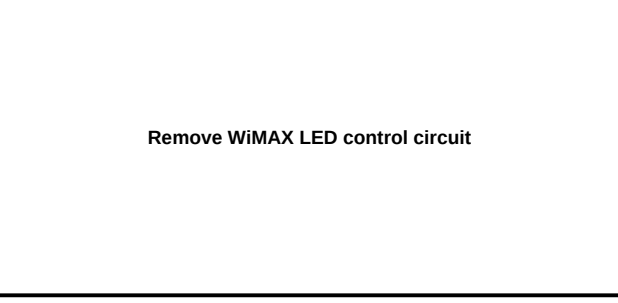
< Power Button for Debug >



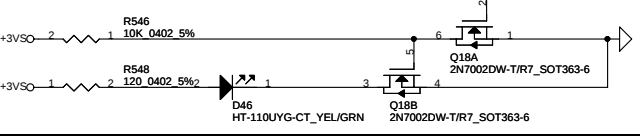
< DC-IN LED >



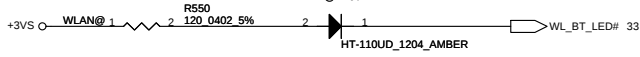
< WiMAX LED >



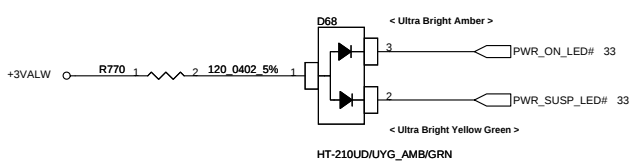
< HDD LED >



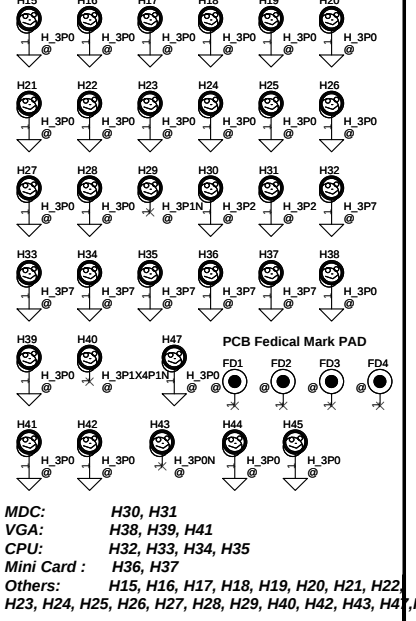
< WL&BT LED >



< POWER-ON & SUSPEND LED >

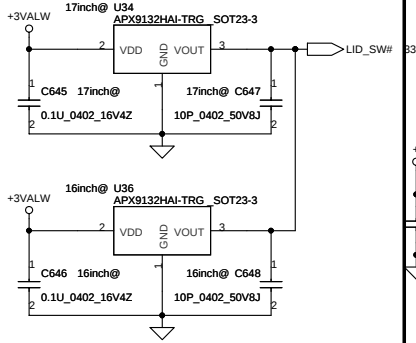


< Screw Hole >

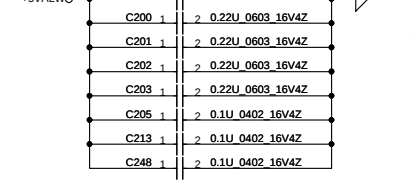


MDC: H30, H31
VGA: H38, H39, H41
CPU: H32, H33, H34, H35
Mini Card: H36, H37
Others: H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H25, H26, H27, H28, H29, H40, H42, H43, H44, H45

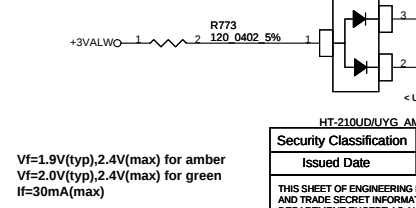
< LID Switch >



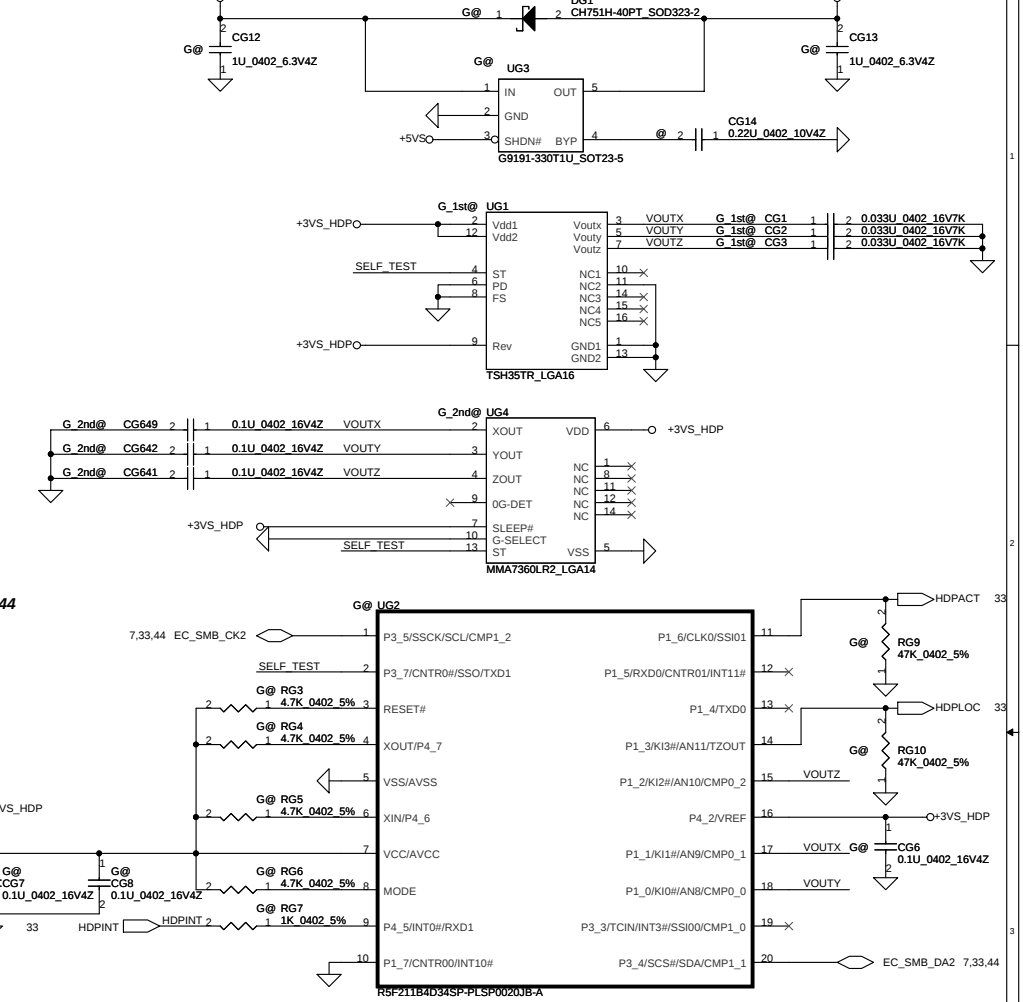
< EMI reserve >



< BATT CHARGE/FULL LED >

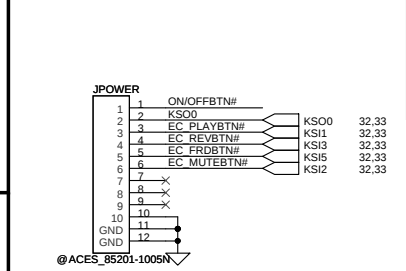


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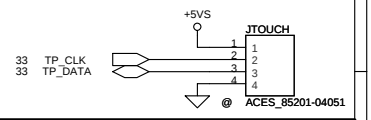


- 1.C199 : U19
- 2.C200 : PU5
- 3.Top side of PU12 for noise bounce.
- 4.C202 : U25
- 5.C203 : PU9
- 6.C205 : PU6
- 7.C213 : PJ5
- 8.C248 : Q35

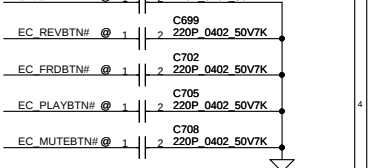
< SW/B Connector >



< Touch/B Connector >

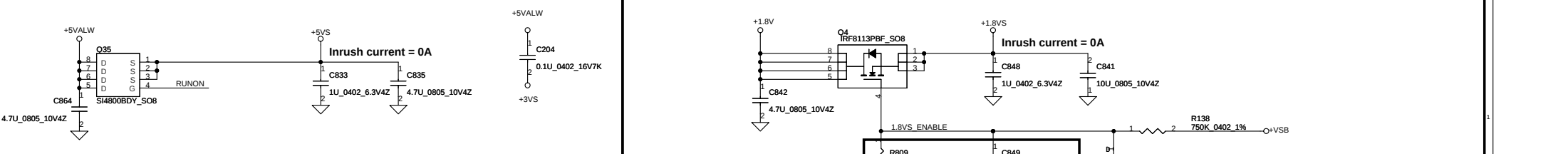


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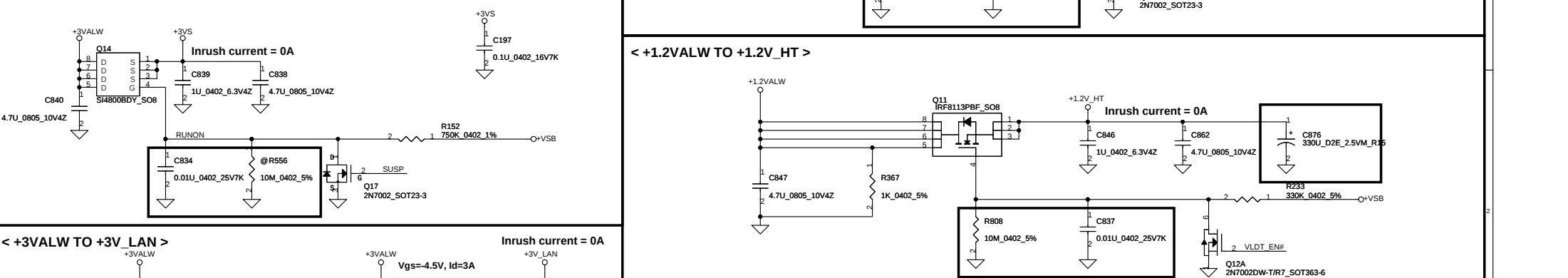


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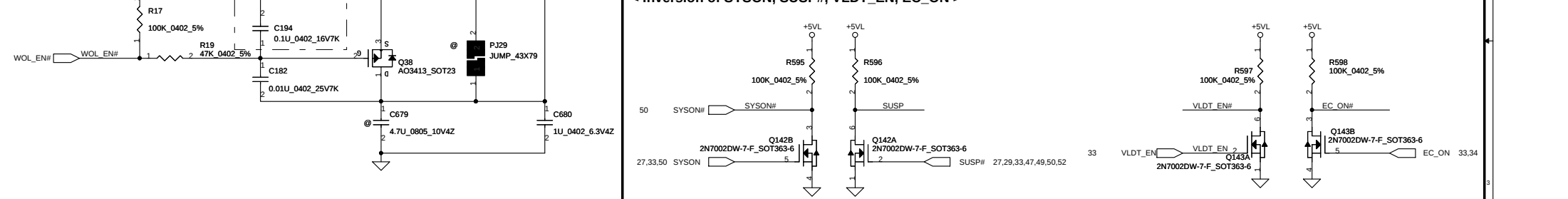
< +5VALW TO +5VS > < close to PQ20, must EMI confirm > < +1.8V TO +1.8VS >



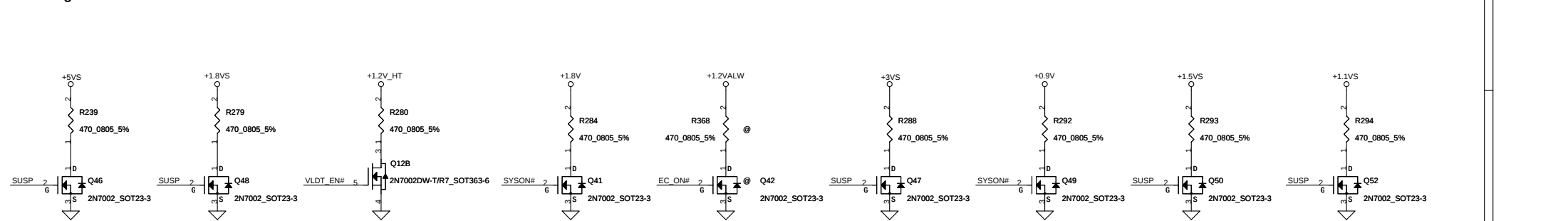
< +3VALW TO +3VS > < close to PQ20, must EMI confirm > < +1.2VALW TO +1.2V_HT >



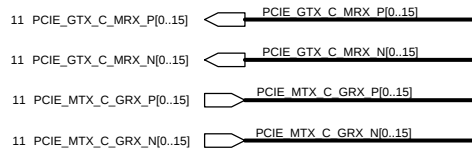
< +3VALW TO +3V_LAN > < Inrush current = 0A > < Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



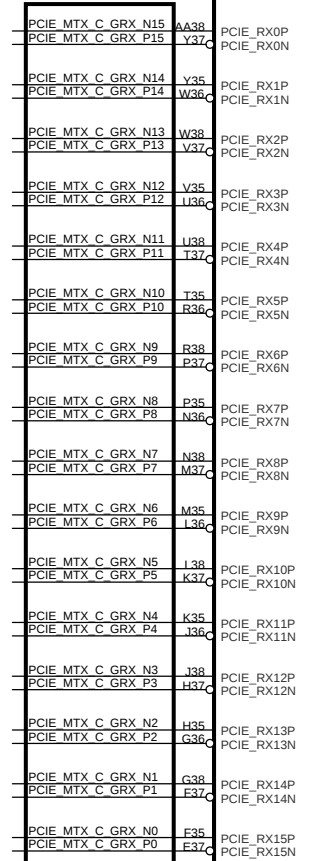
< Discharge circuit >



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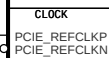
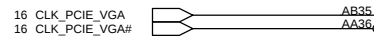
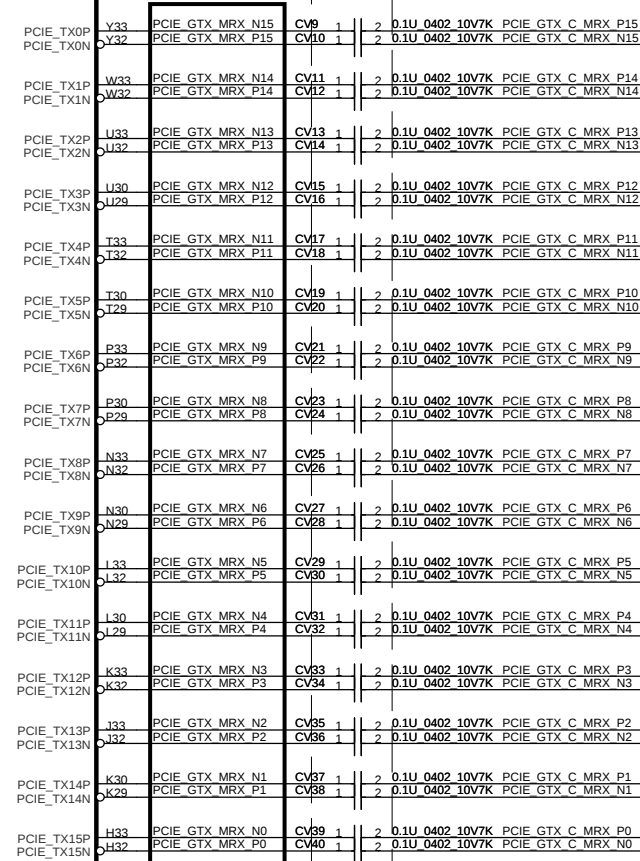
Swap PCIE & polarity inversion



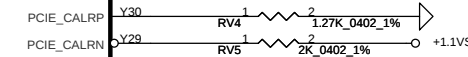
UV1A

PCI EXPRESS INTERFACE

Swap PCIE & polarity inversion



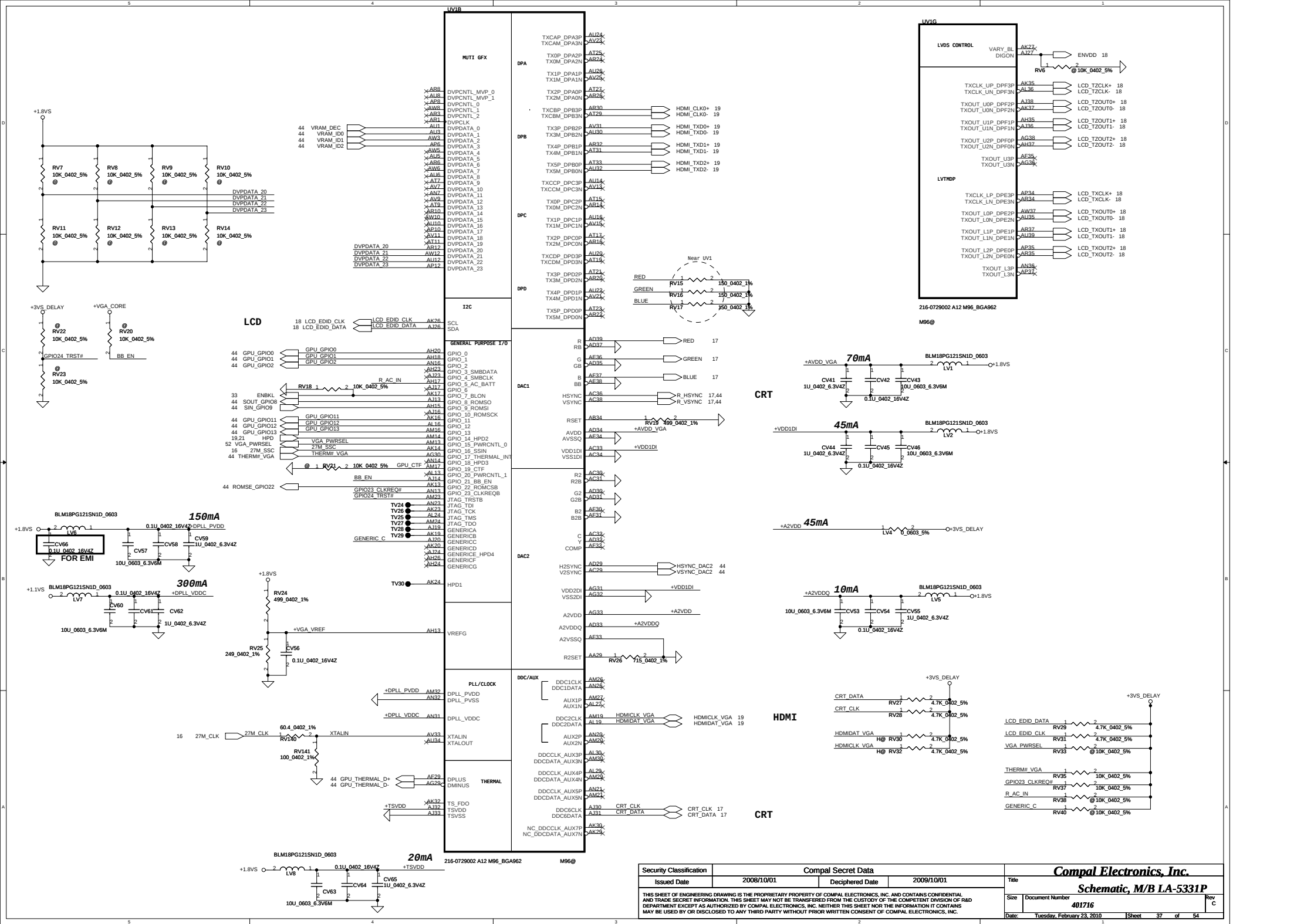
CALIBRATION

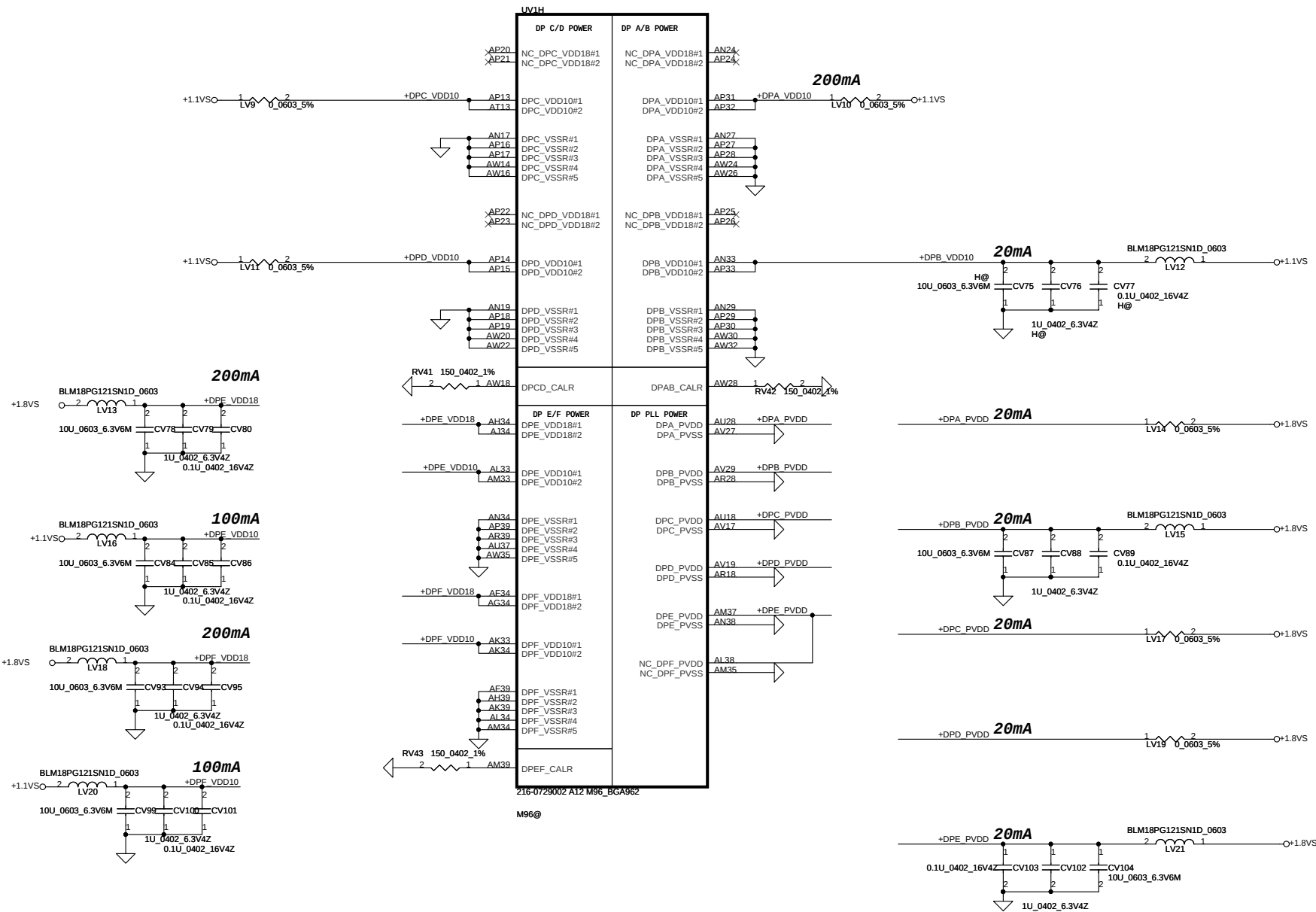


M96@

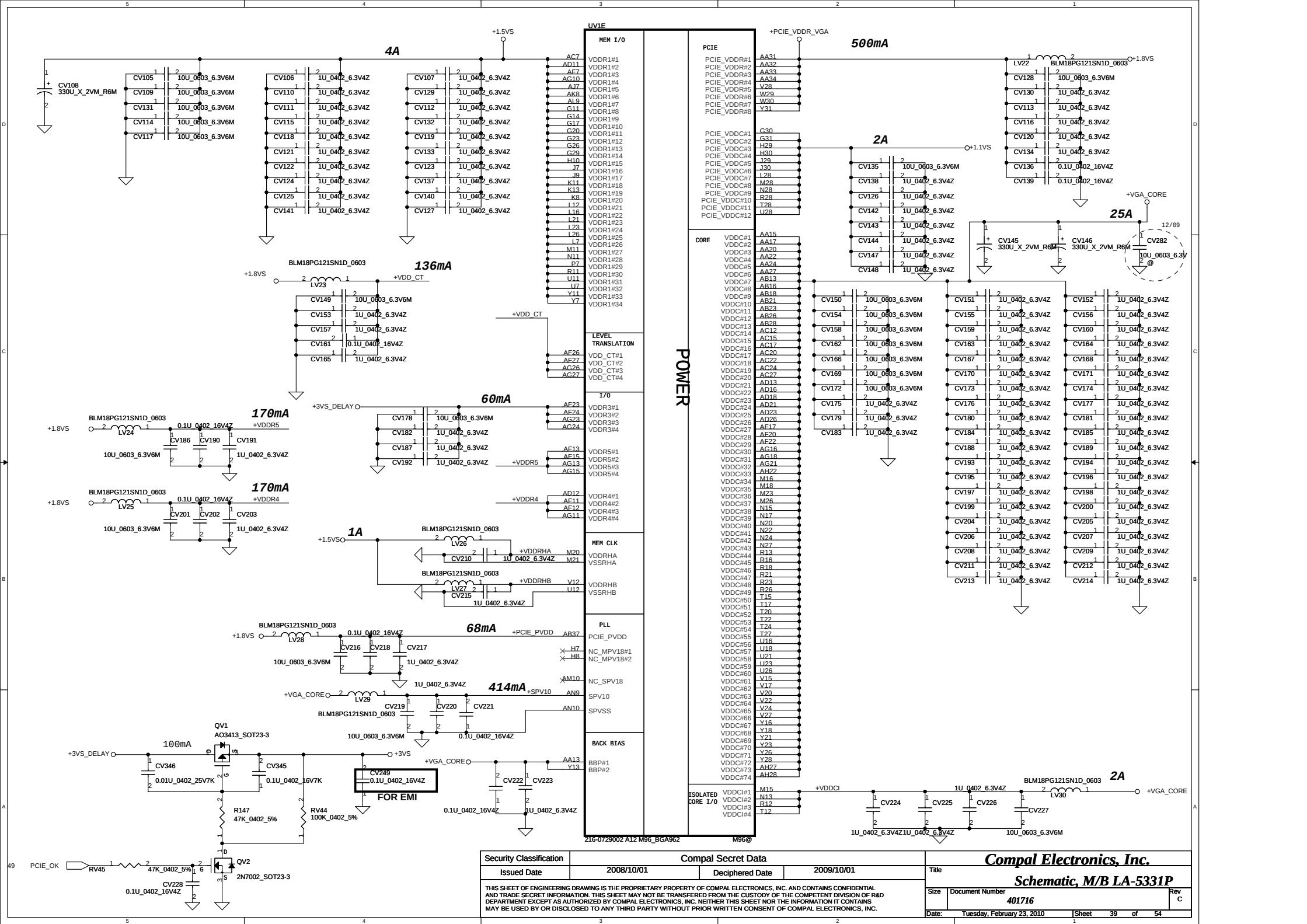
216-0729002 A12 M96_BGA062

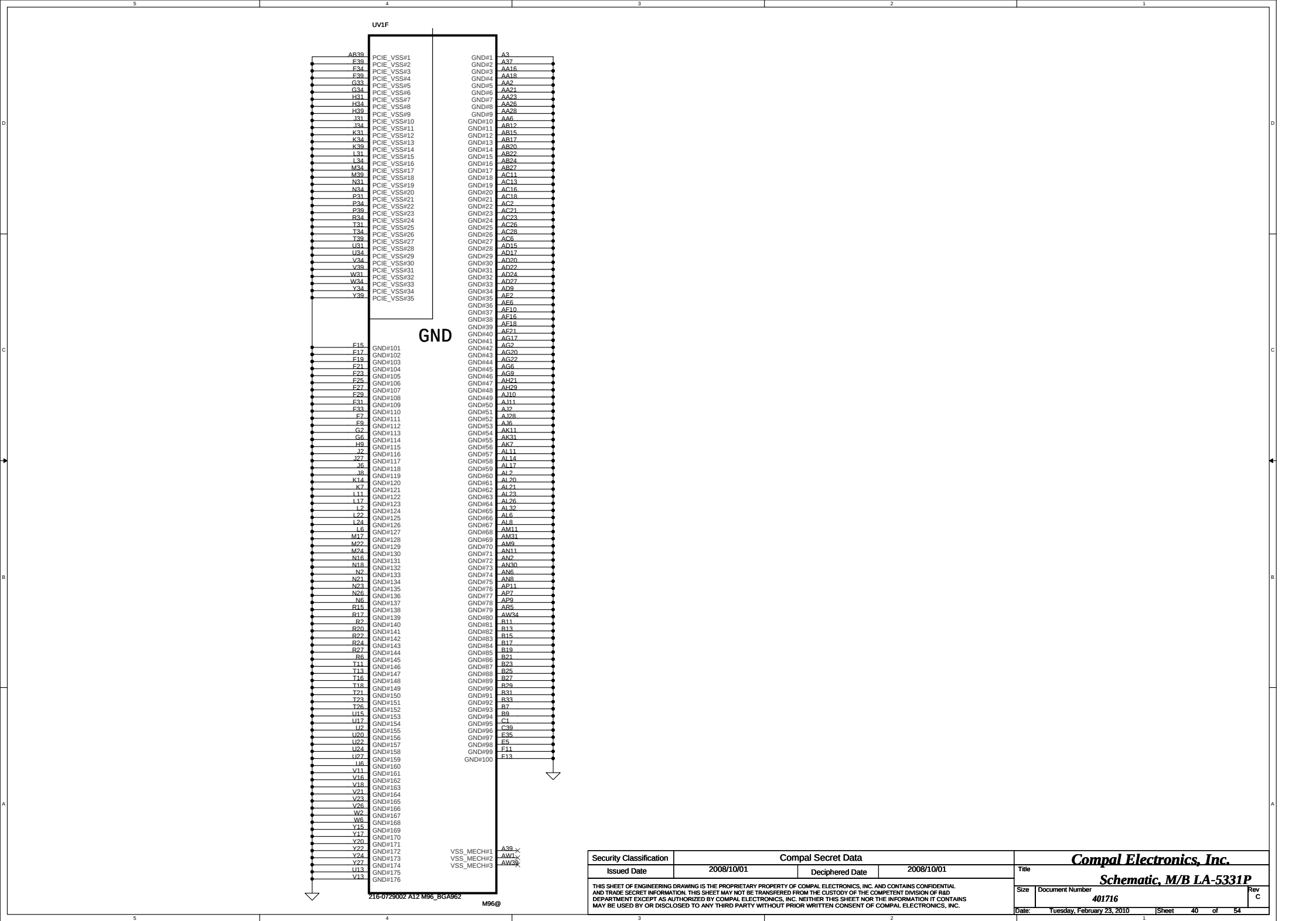
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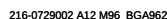
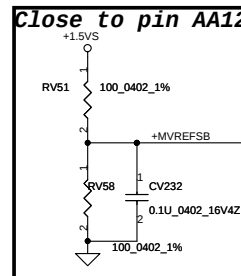
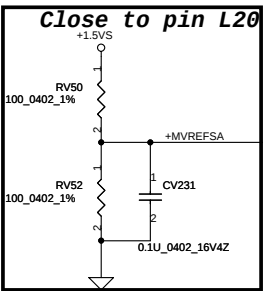


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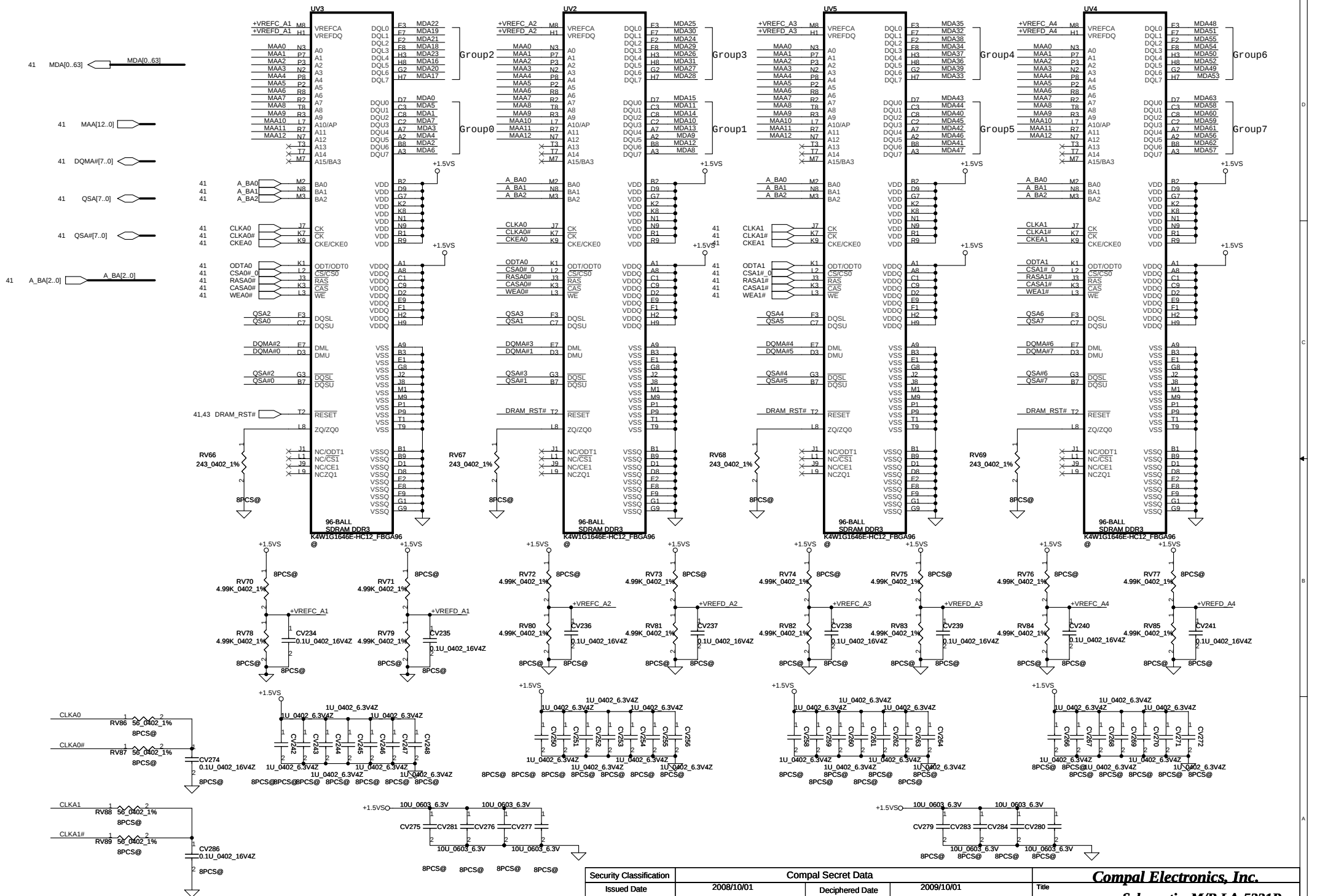
MEMORY INTERFACE A

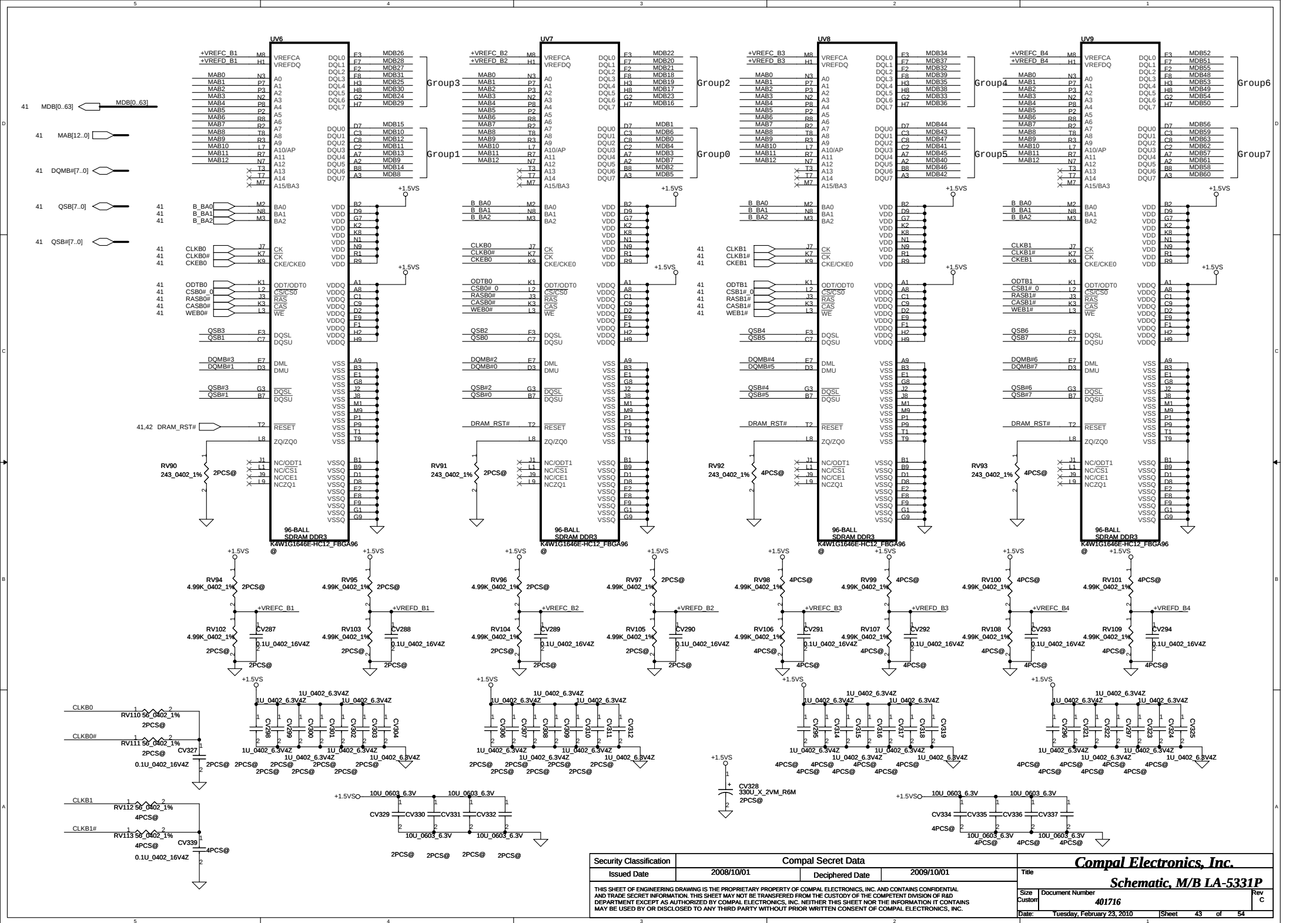
MEMORY INTERFACE B



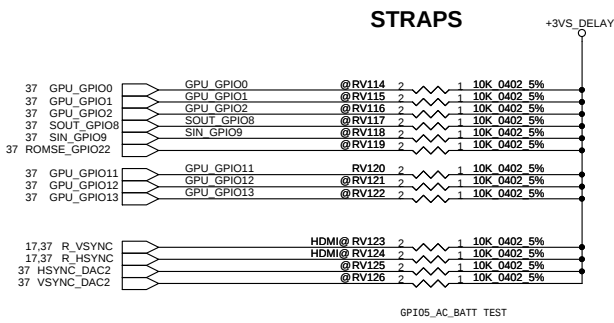
M96@

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GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

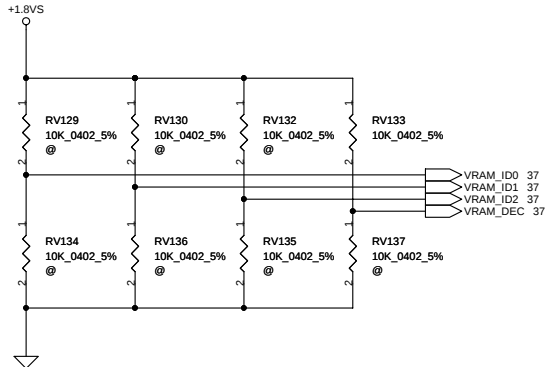
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2 GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

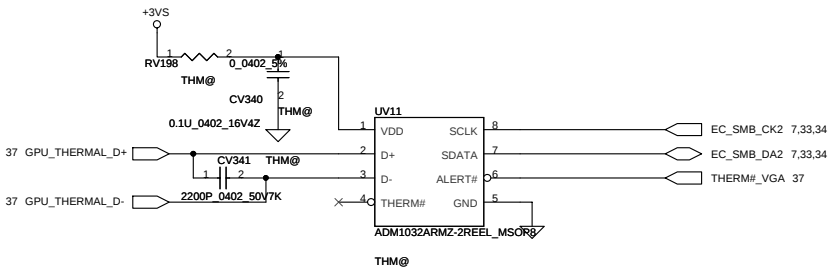
GPIO_28_TDO GPIO21_BB_EN



DDR3	
VRAM_DEC	1

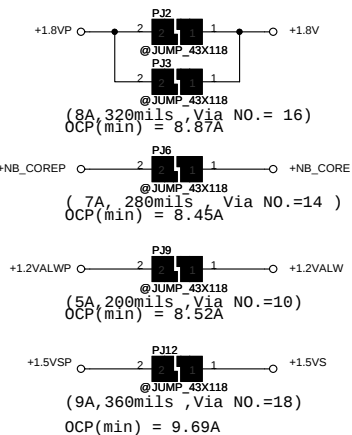
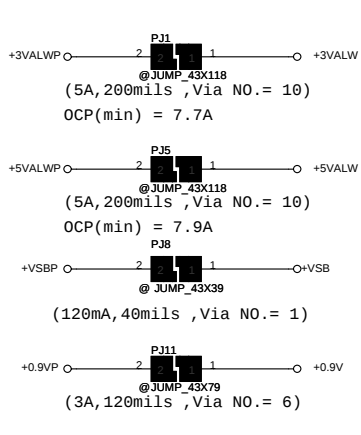
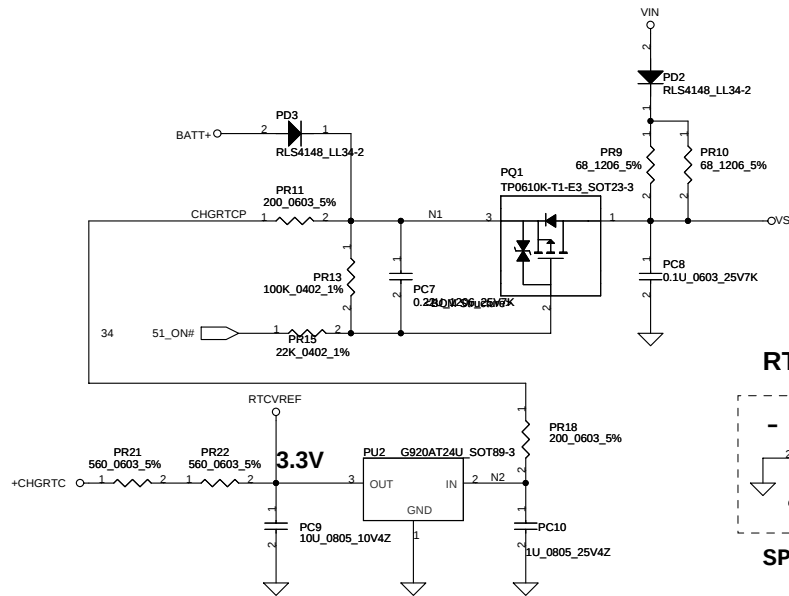
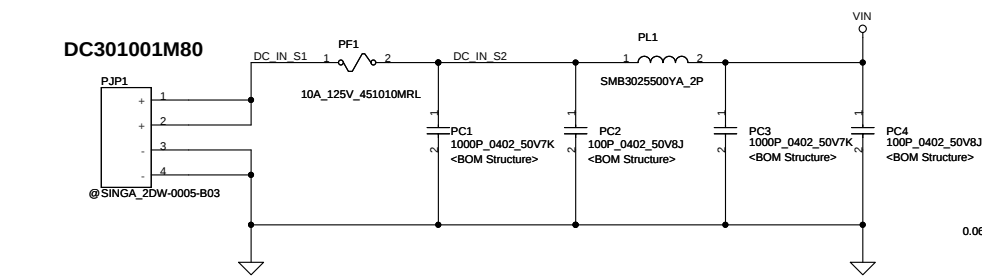
STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
		M96-M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 1
		M92-M2 XT	256M 64Mx16 (x2)	HYN H5TQ1G63BFR-12C	SA000032400	0 1 0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 0
		M96-M3	1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	0 1 1
		M92-M2 XT	256M 64Mx16 (x2)	SAM K4W1G1646E-HC12	SA000035700	1 0 1

External VGA Thermal Sensor

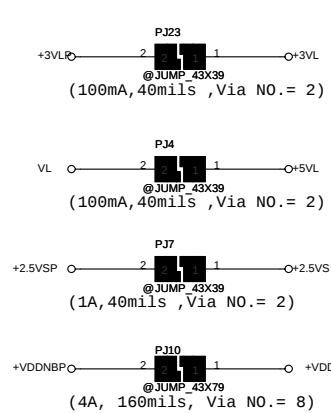
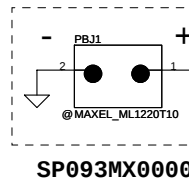


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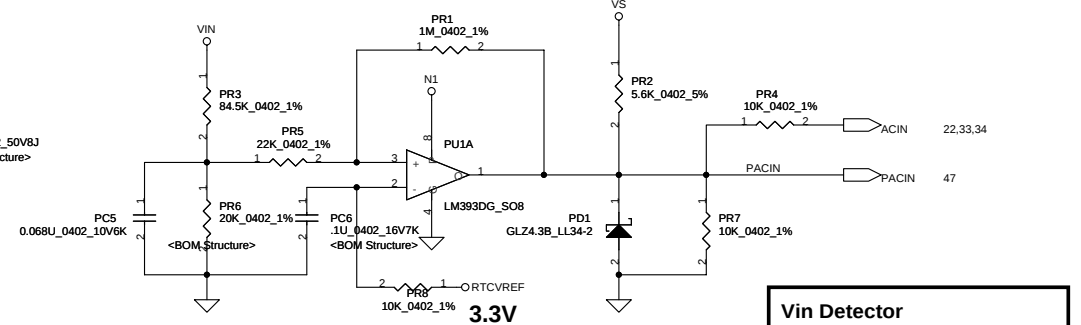
DC301001M80



RTC Battery

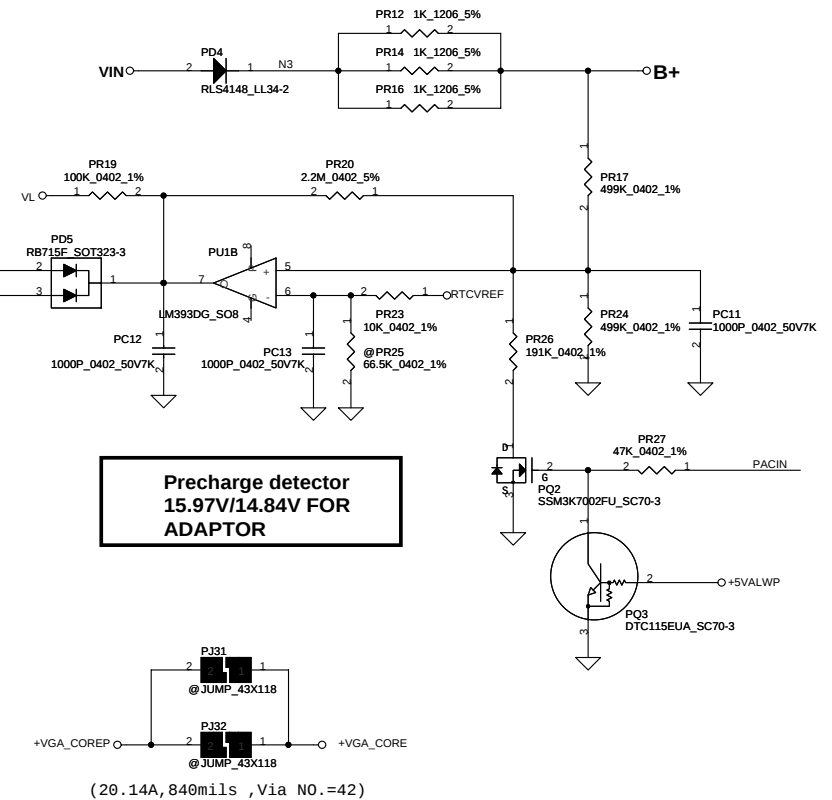


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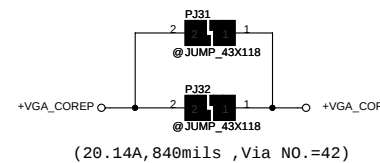


Vin Detector

High	18.384	17.901	17.430
Low	17.728	17.257	16.976



Precharge detector 15.97V/14.84V FOR ADAPTOR

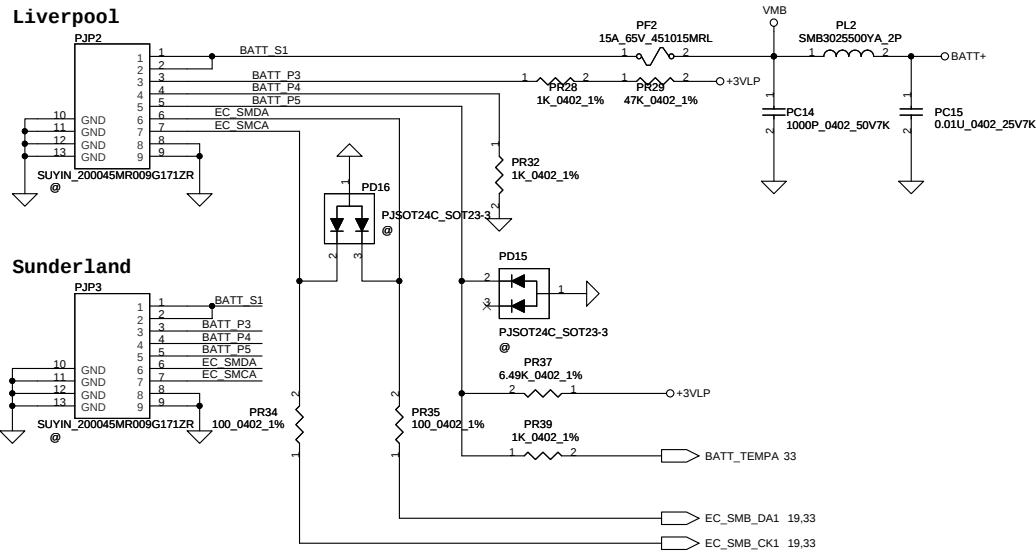


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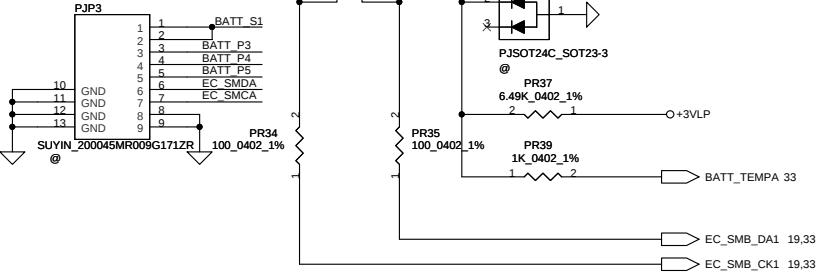
Schematic, M/B LA-5331P

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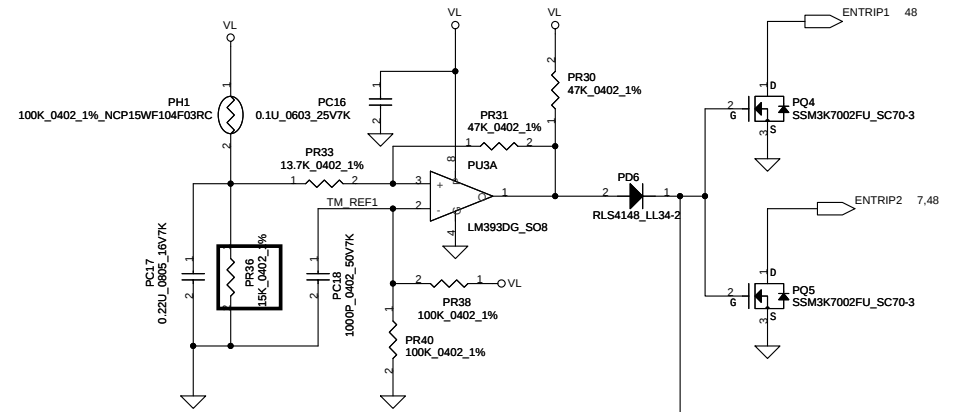
Liverpool



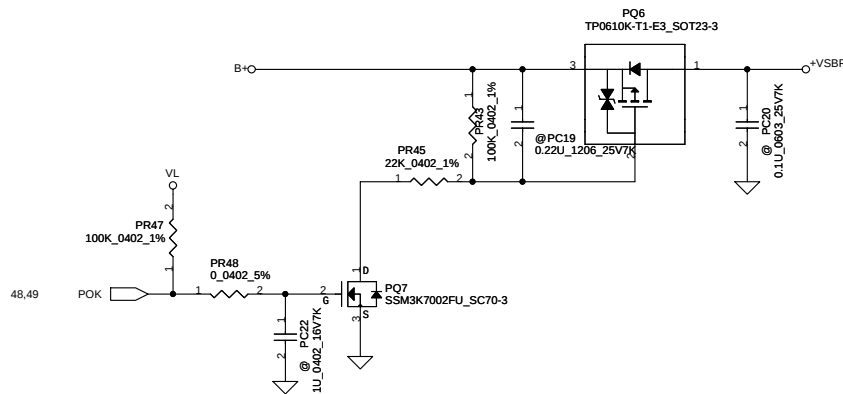
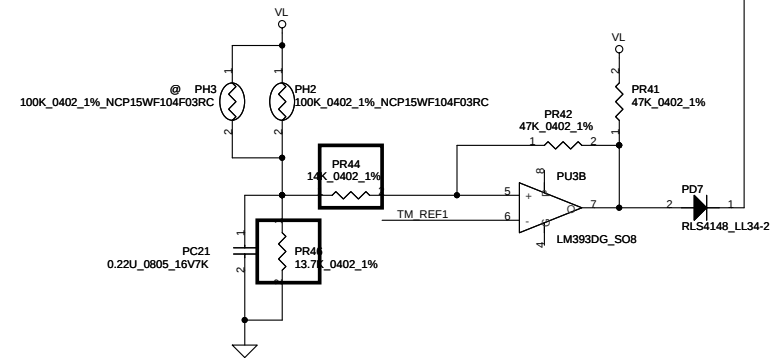
Sunderland



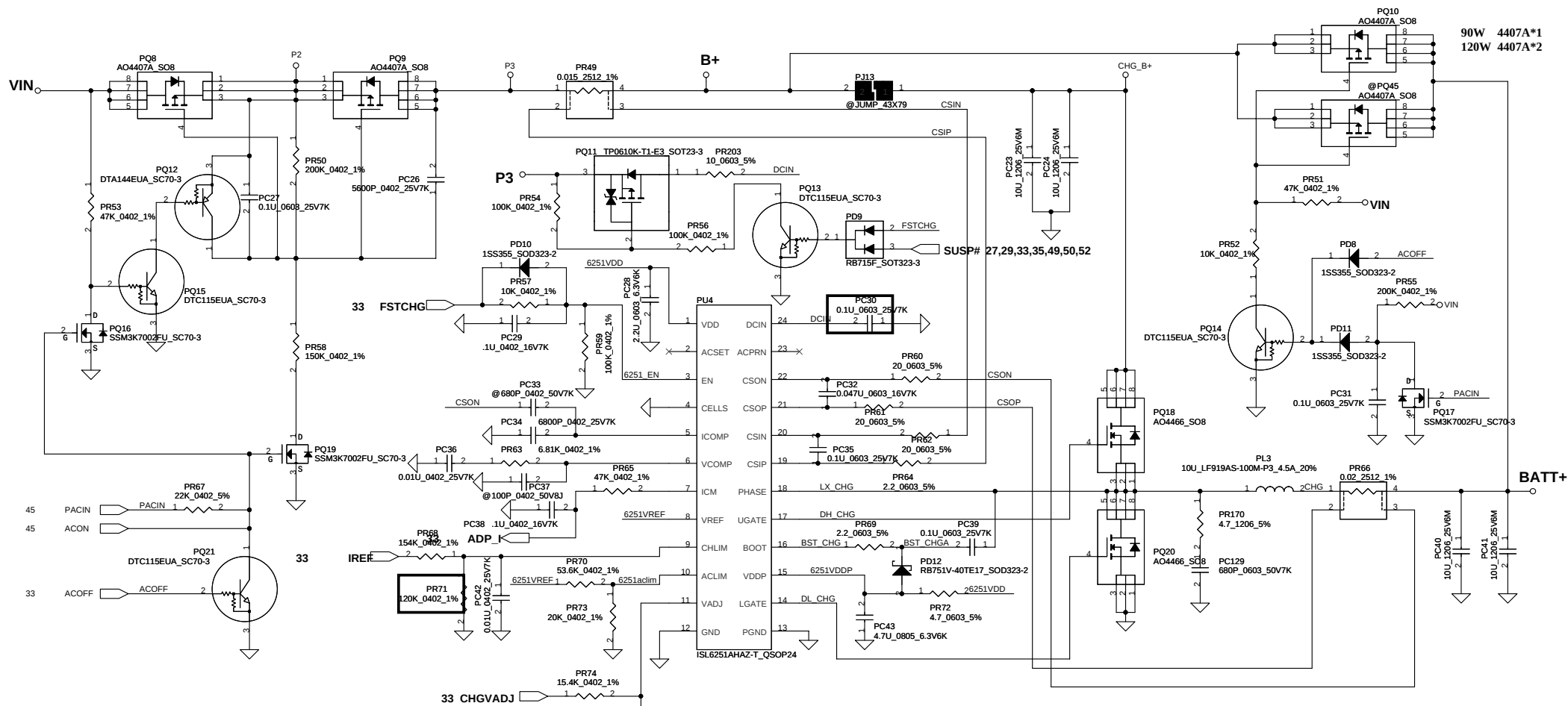
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 57 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 98 degree C
Recovery at 60 degree C



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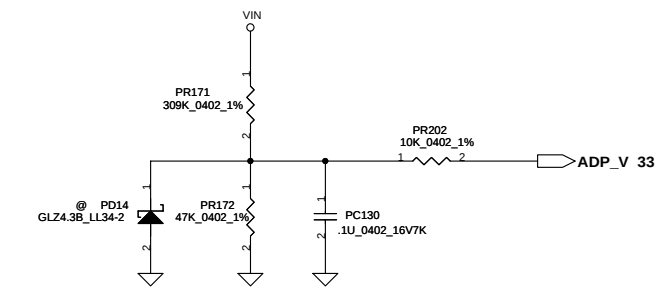
Iada=0-3.421A(65W) CP=3.15A PR49=0.02, PR70=75k, PR73=20k
Iada=0-3.947A(75W) CP=3.63A PR49=0.02, PR70=24k, PR73=20k
Iada=0-4.737A(90W) CP=4.36A PR49=0.015, PR70=53.6k, PR73=20k
Iada=0-6.316A(120W) CP=5.81A PR49=0.015, PR70=8.25k, PR73=26.7k
CP= 92%*Iada

CP mode
 $V_{ac1m} = 2.39 * (R_b / (152K) / (R_t / (152K) + R_b / (152K)))$
 $I_{input} = (1 / PR49) * ((0.05 * V_{ac1m}) / (2.39 + 0.05))$
 where $V_{ac1m} = 1.09986V$, $I_{input} = 3.65A$
 $V_{ac1m} = 0.7717V$, $I_{input} = 4.41A$
 $V_{ac1m} = 0.4204V$, $I_{input} = 5.88A$

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

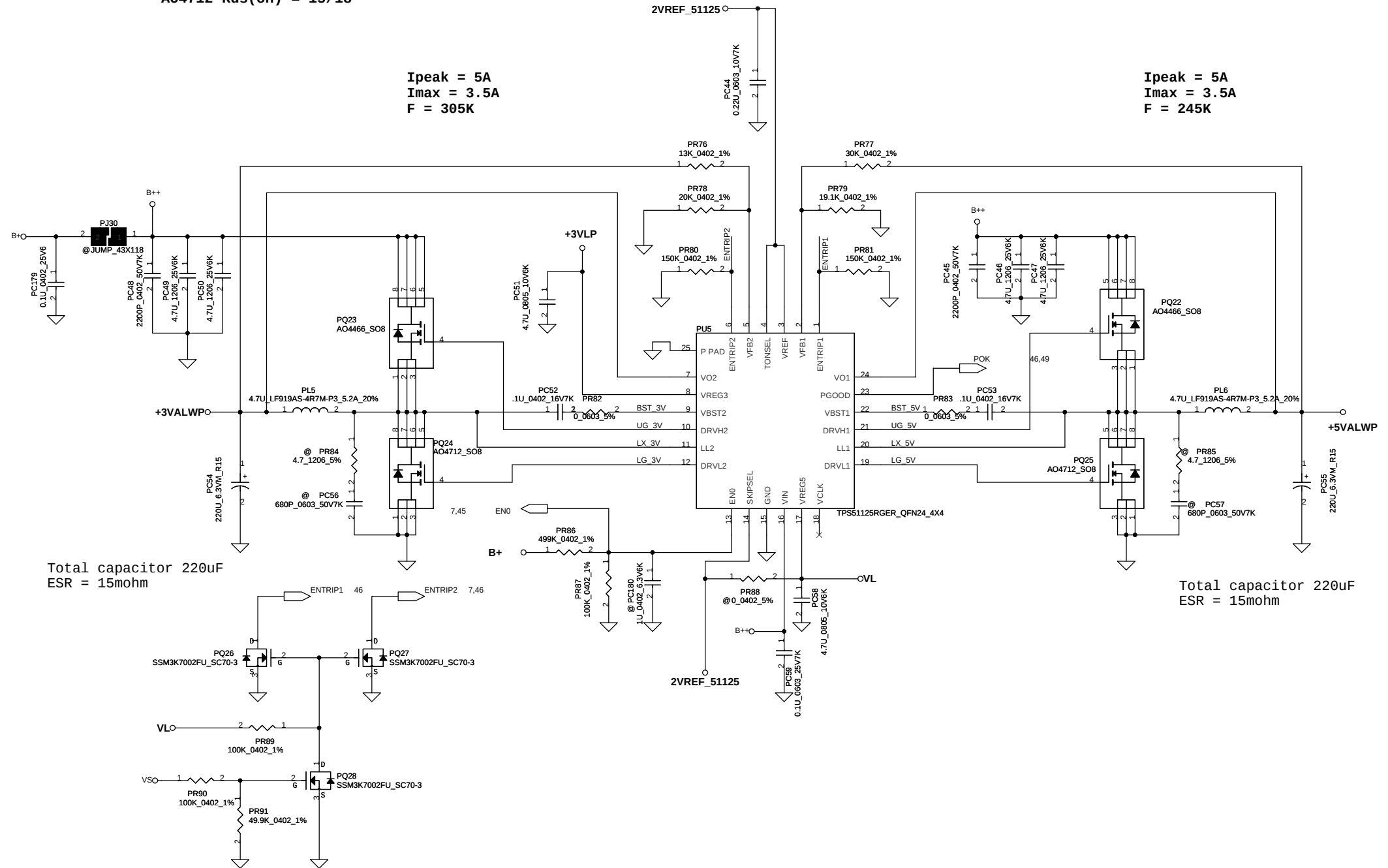
CELLS	VDD	GND	Float
CELL number	4	3	2



A04712 Rds(on) = 15/18

Ipeak = 5A
Imax = 3.5A
F = 305K

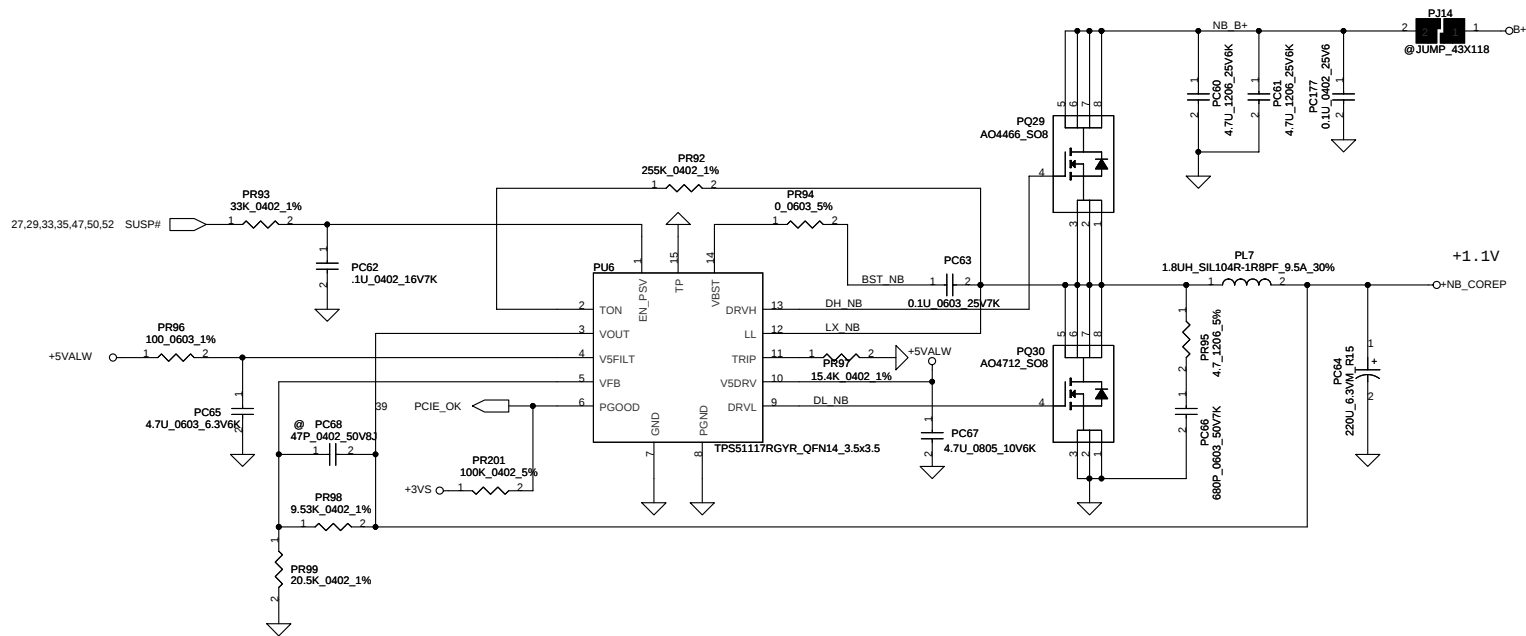
Ipeak = 5A
Imax = 3.5A
F = 245K



Total capacitor 220uF
ESR = 15mohm

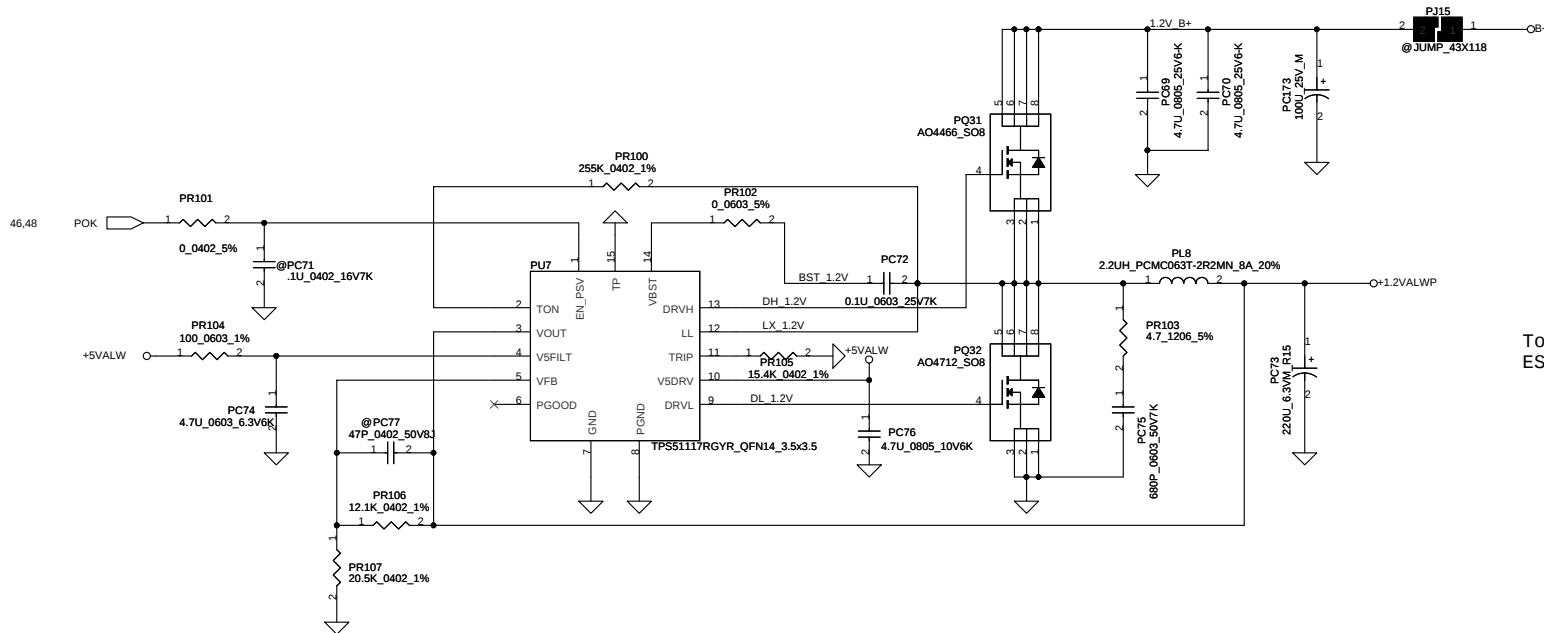
Total capacitor 220uF
ESR = 15mohm

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Ipeak = 7A
Imax = 4.9A
F = 315K

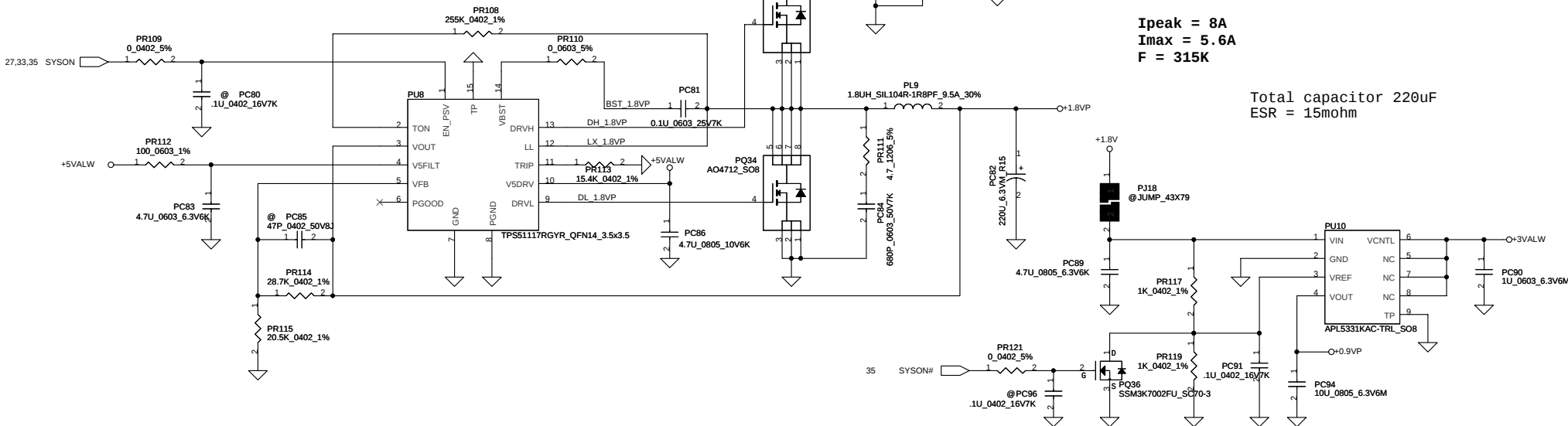
Total capacitor 550uF
ESR = 30mohm



Ipeak = 5A
Imax = 3.5A
F = 315K

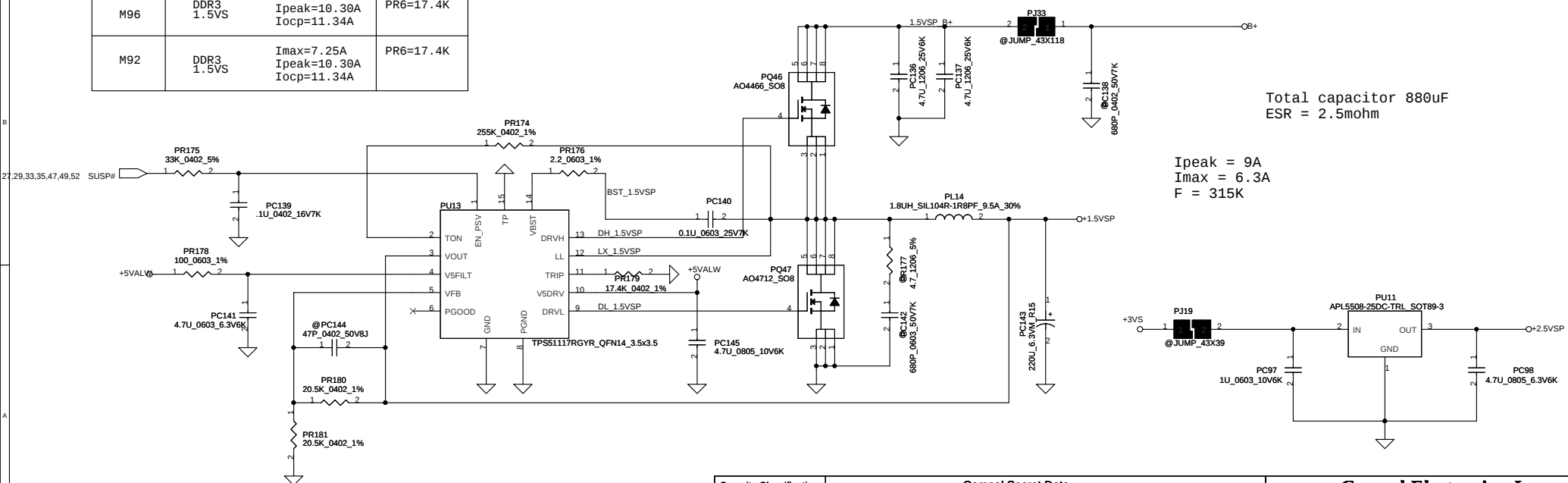
Total capacitor 220uF
ESR = 15mohm

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				Size	Document Number
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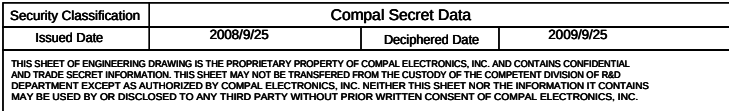


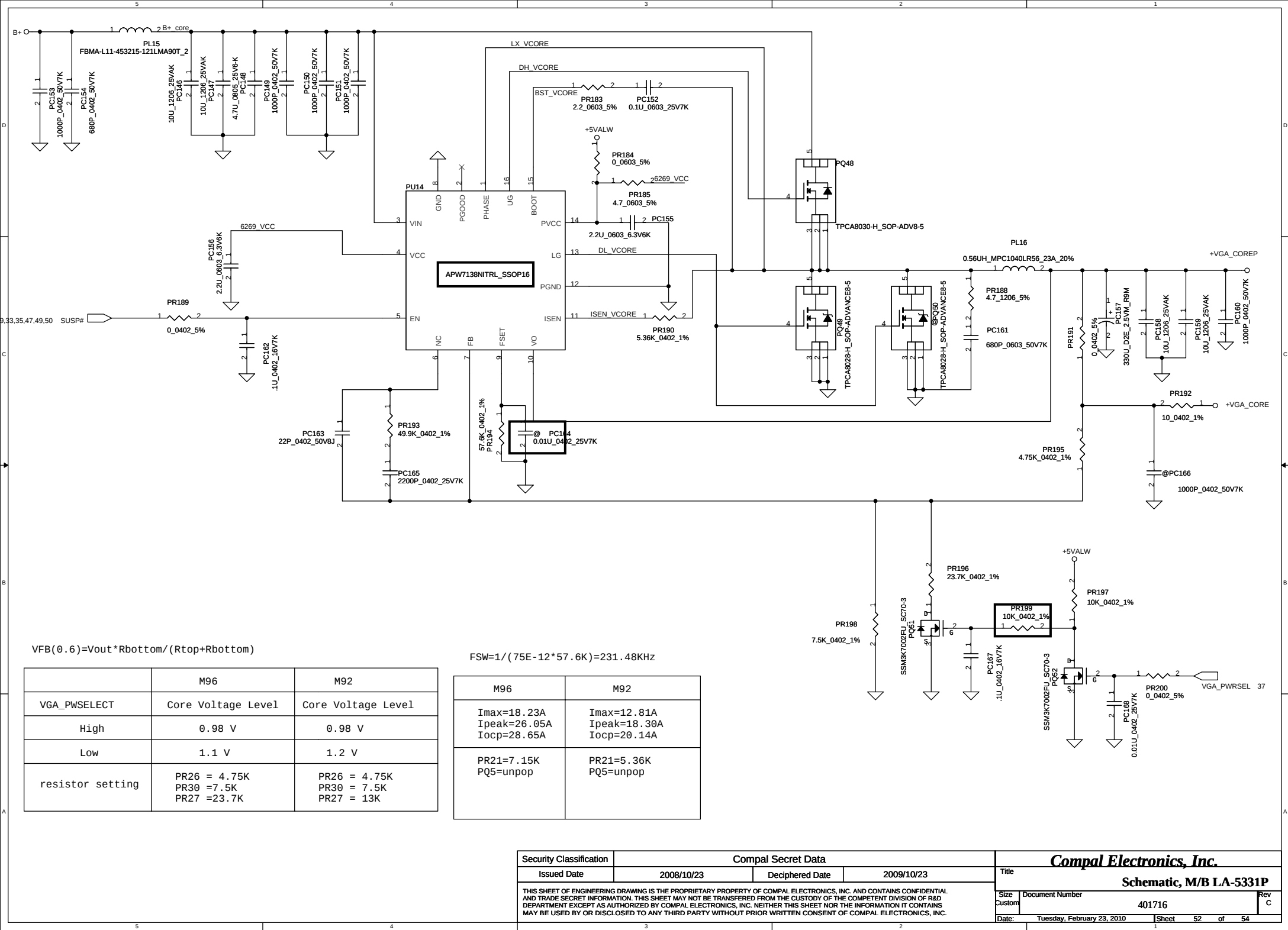
M96	DDR3 1.5VS	Imax=7.25A Ipeak=10.30A Iocp=11.34A	PR6=17.4K
M92	DDR3 1.5VS	Imax=7.25A Ipeak=10.30A Iocp=11.34A	PR6=17.4K

FSW=312KHz



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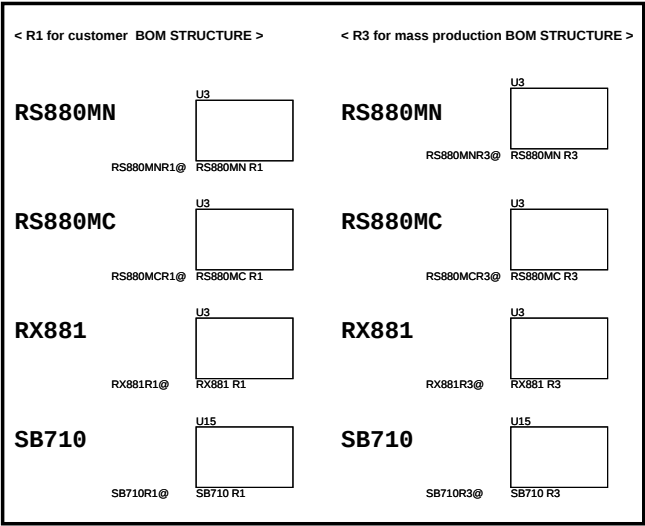


Version Change List (P. I. R. List) for Power Circuit

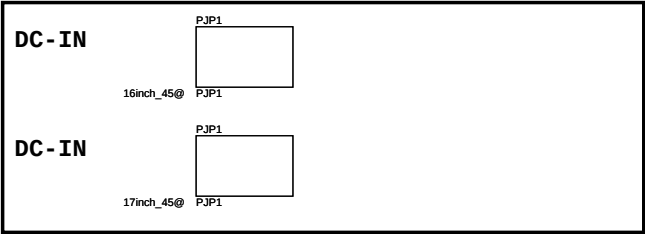
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
		Pre EVT modification					
1		01. 2009/02/09 --> change UG3 to G9191-330T1U, P/N is SA000022100				55. 2009/04/02 --> ADD RM8	
		02. 2009/02/10 --> change UL3's P/N to SP050005V00				56. 2009/04/02 --> Change R440 from 100k ohm to 0 ohm and unmount C480	
		03. 2009/02/10 --> change R489 & R488 BOM structure				57. 2009/04/02 --> Change +HDMI_5V_OUT circuit, add D20, D53	
		04. 2009/02/10 --> change R142 from 300 ohm to 150 ohm				58. 2009/04/14 --> Add C205, C213, C248, C478, C484, CV66, CV249 for EMI request	
		05. 2009/02/10 --> change R143 from 1M ohm to 100K ohm				59. 2009/04/14 --> Mount CA54, CA55, CA56, CA57 for EMI request	
		06. 2009/02/10 --> change JREAD footprint to TAITW_R009-125-LR_21P_RV-T				60. 2009/04/14 --> Add C876 for Power noise issue	
		07. 2009/02/11 --> change +HDMI_5V_OUT circuit, add D18, R160, Q26, R557, C876 and change power				61. 2009/04/14 --> Add D21 for Power issue	
		08. 2009/02/11 --> change UG1 P/N and velue to SA000039900 and TSH35TR				62. 2009/04/15 --> Del TV2, TV3, TV4, TV5, TV6, TV7, TV8, TV9, TV10, TV11, TV12, TV13, TV14, TV15, TV16, TV17, TV18, TV19, TV20, TV21, TV22, TV23	
		09. 2009/02/11 --> change location from CV2 to C706				63. 2009/04/17 --> Un-mount D12	
		10. 2009/02/13 --> remove WIMAX LED control circuit					
		11. 2009/02/17 --> remove Audio codec digital GND to analog GND net				Pre DVT modification	
		12. 2009/02/17 --> Add JFAN1 for M96 FAN				64. 2009/04/27 --> Un-mount DA6, DA7	
		13. 2009/02/17 --> change JTOUCH footprint				65. 2009/04/27 --> Change C234, C876 P/N to SGA19331D00	
		14. 2009/02/17 --> add NPTH Hole H42, H43				66. 2009/04/27 --> Change RV45 P/N to SD028470280	
		15. 2009/02/17 --> add CA12				67. 2009/04/27 --> Change RV140 P/N to SD034604A80	
		16. 2009/02/17 --> change Int MIC ground to AGND between CA27 and J3				68. 2009/04/27 --> Un-mount R42	
		17. 2009/02/17 --> change UN1 P/N to SA00001SL20				69. 2009/04/27 --> Mount R367	
		18. 2009/02/17 --> Add JPWR1 for co-lay with JPOWER				70. 2009/05/07 --> Change U25, U19 from SA005280110 to SA00002XX00	
		19. 2009/02/19 --> add CA45, CA46, CA47, CA48, CA49, CA50, CA51, CA52, CA53				71. 2009/05/07 --> Change RA38 from LVDSSET@ to @	
		20. 2009/02/19 --> replace RA12, RA13, RA14 with CA54, CA55, CA56 and add CA57				72. 2009/05/07 --> Change U34, U36 from SA00001NT00 to SA00001WP00	
		21. 2009/02/19 --> Delete CV81, CV82, CV83, CV90, CV91, CV92, CV96, CV97, CV98				73. 2009/05/07 --> Change QV1 from SB923010020 to SB934130000	
		22. 2009/02/19 --> Change LV14, LV17, LV19 to 0 ohm				74. 2009/05/07 --> Change QV2 from SB000009610 to SB770020010	
		23. 2009/02/19 --> Swap M9X PCIE net & polarity inversion				Pre PVT modification	
		24. 2009/02/19 --> Add CV345, CV346, R147 for soft start				75. 2009/05/24 --> Add H44,H45 H_3P0 for express dummy card	
		25. 2009/02/19 --> Delete CV249, CV257, CV265, CV273, CV278, CV285, CV305, CV313, CV320, CV326, CV333, CV338				76. 2009/05/24 --> Change C350 from SF22001M300 to SF22001M200.	
						77. 2009/05/24 --> Add C178,C485,C486 for EMI request.	
		26. 2009/02/20 --> Add R189, R190 & Net : 27MCLK, 27M_CLK, 27MSSC, 27M_SSC				78. 2009/05/24 --> Del JPWR1	
		27. 2009/02/20 --> Delete UV12, RV142, CV343, CV344, CV342, RV138, XV1, RV139				79. 2009/05/24 --> Del JPWR1,JCAM,R430,R428,C744,R20,R18	
		28. 2009/02/24 --> change R70, R77 from 4.7K to 2.2K				80. 2009/05/24 --> Change net name from USB20_N9_R_CAM & USB20_P9_R_CAM to USB20_N9_R & USB20_P9_R	
		29. 2009/02/24 --> change R178 from 4.7K to 47K				81. 2009/05/24 --> Change UV2 ~ UV9 P/N & symbol to SA000035700	
		30. 2009/02/26 --> change UG2 P/N to SA00003A600				Pre Pre-MP modification	
		31. 2009/02/27 --> change T9, T10, T11,T12, T19, T20 footprint to TPC24				82. 2009/07/07 --> Change C643 & C652 to SE071120J80 .	
		32. 2009/02/27 --> Delete JFAN1				83. 2009/07/07 --> Change C350 to SF000001H00.	
		33. 2009/02/28 --> Change D36 from SC1B491D000 to SCS00002000				84. 2009/08/06 --> Change Y7 PN from SJ100003D00 to SJ132P7KW10.	
		34. 2009/02/28 --> Change 5V camera power at JLVDS connector and add R968, R967, C274				85. 2009/08/27 --> Change RV123 & RV124 BOM structure to HDMI@.	
		35. 2009/02/28 --> Change SPI ROM from SST to MXIC				86. 2009/09/21 --> Change C9, C13, C70, C71, C83, C84, C95, C104, CL26, CL27 to SE074102K80	

HW4 Product Improvement Record (P.I.R.)

< Tigris >



< DC Jack >



< PCB >



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