

KSKAA

Bradford 10M/10MG

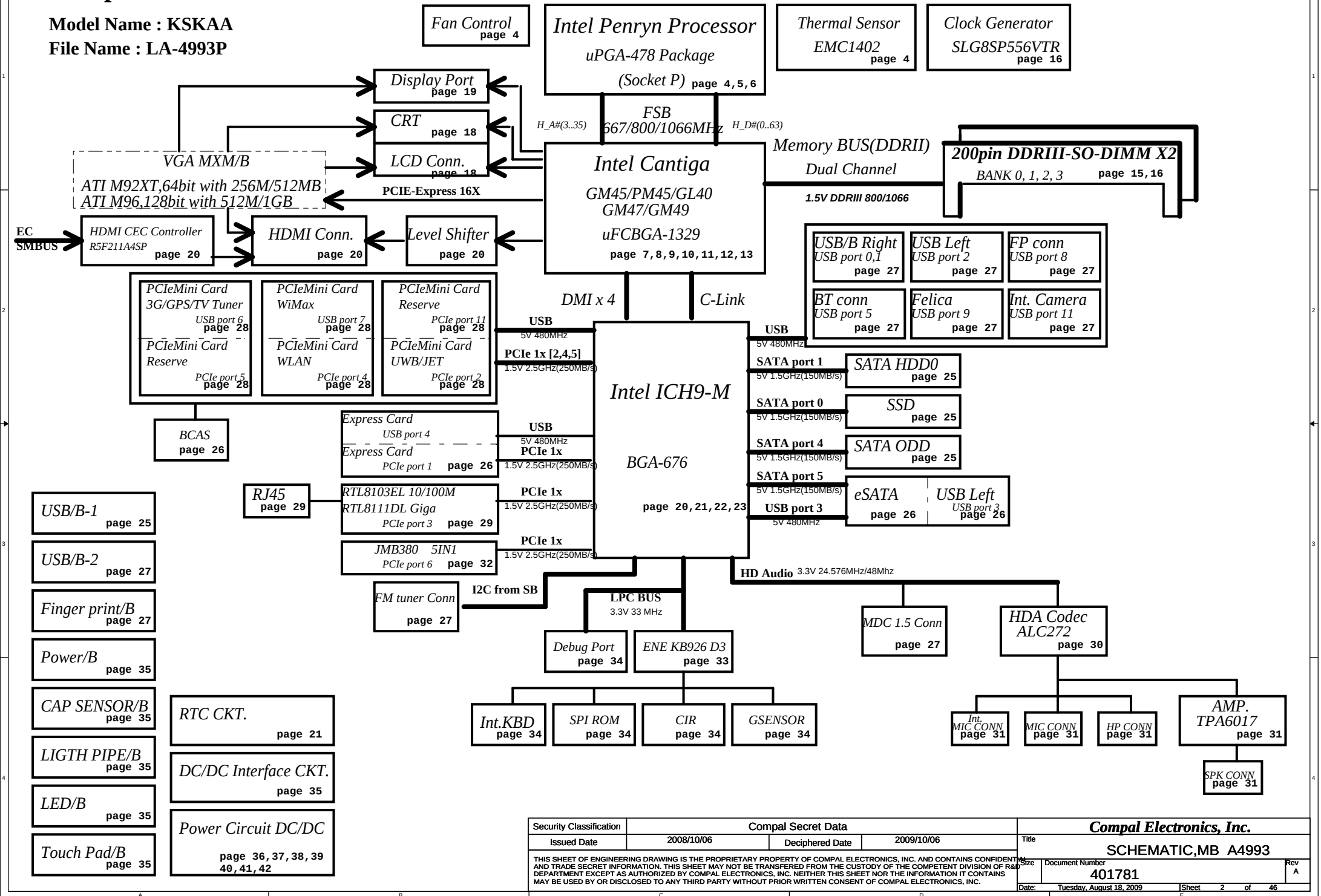
LA-4993P REV 1.0 Schematic

Intel Penryn/ Cantiga/ ICH9M
2009-07-23 Rev. 1.0

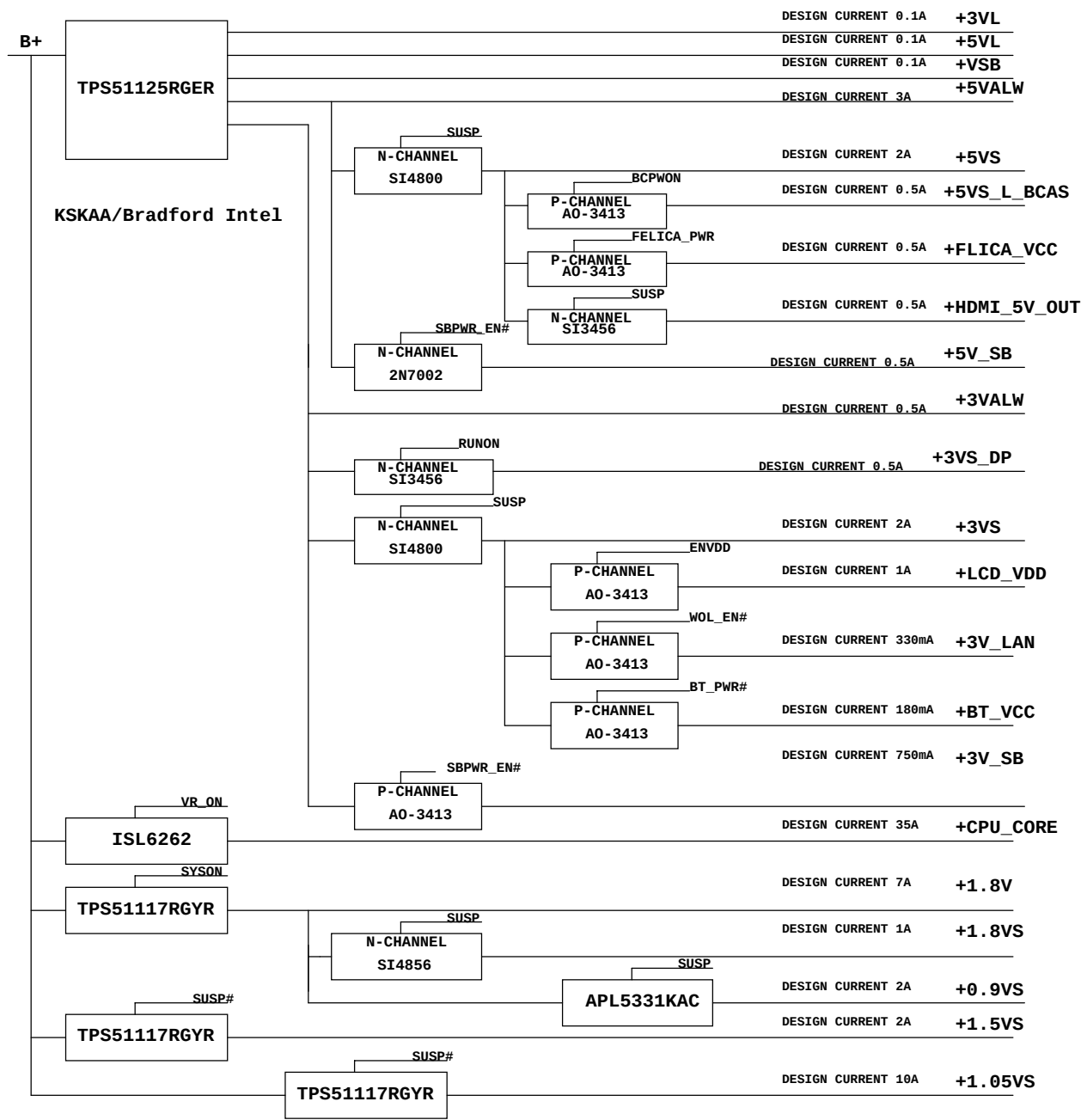
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Compal Confidential

Model Name : KSKAA
File Name : LA-4993P



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													401781			A
													Date:			Tuesday, August 18, 2009



Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

External PCI Devices

EC SM Bus1 address

Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D3		+3VS	EC KB926 D3	
+5VL	Smart Battery	0001 011X b			
+5VL	HDMI-CEC	0011 010x b	+3VS	CPU THM Sen	
				SMSC SMC1402	0100 110x b
+3VL	FUN/B (CAP Sensor)				

EC SM Bus2 address

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	

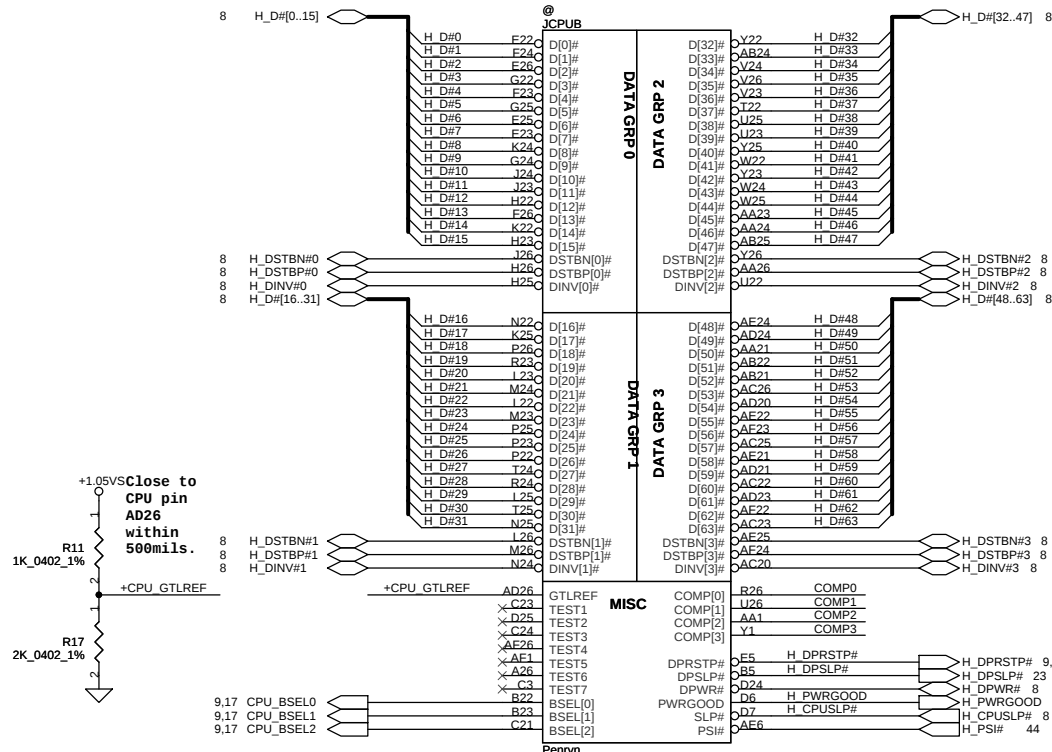
STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

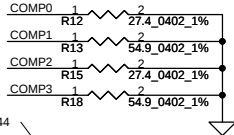
Function	HDMI			CRT	Display	LAN		
description	(Y)			(Q)	(Z)	(E)	(C)	
explain	Intel(UMA)	ATI MXM/B	COMMON			10/100M	Giga	
BTO	IHDMI@	NIHDMI@	HDMI@	H@	CRT@	DP@	8103EL@	8111DL@

Function	3G SIM slot	Mini card	Felica	Finger printer	CIR	CAMERA & MIC		BLUE T00TH
description	(3)	(D2)	(J)	(F)	(I)	(X)		(B)
explain		Two Cards				CAMERA	MIC	
BTO	3G@	3G@	FLICA@	FP@	CIR@	CAM@	MIC@	BT@

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							401781		A
						Date:	Tuesday, August 18, 2009		Sheet 4 of 46



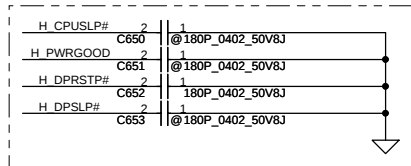
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



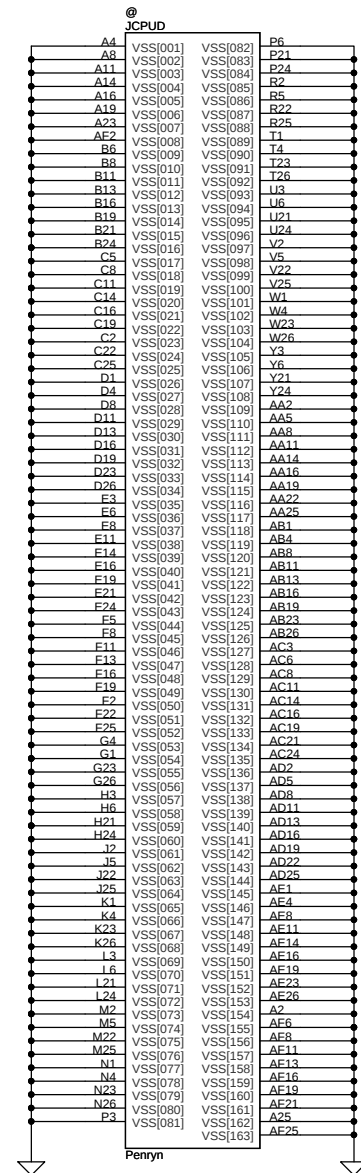
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

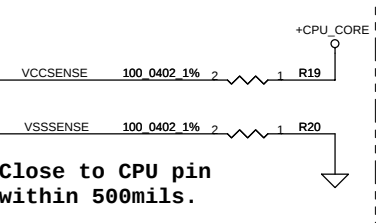
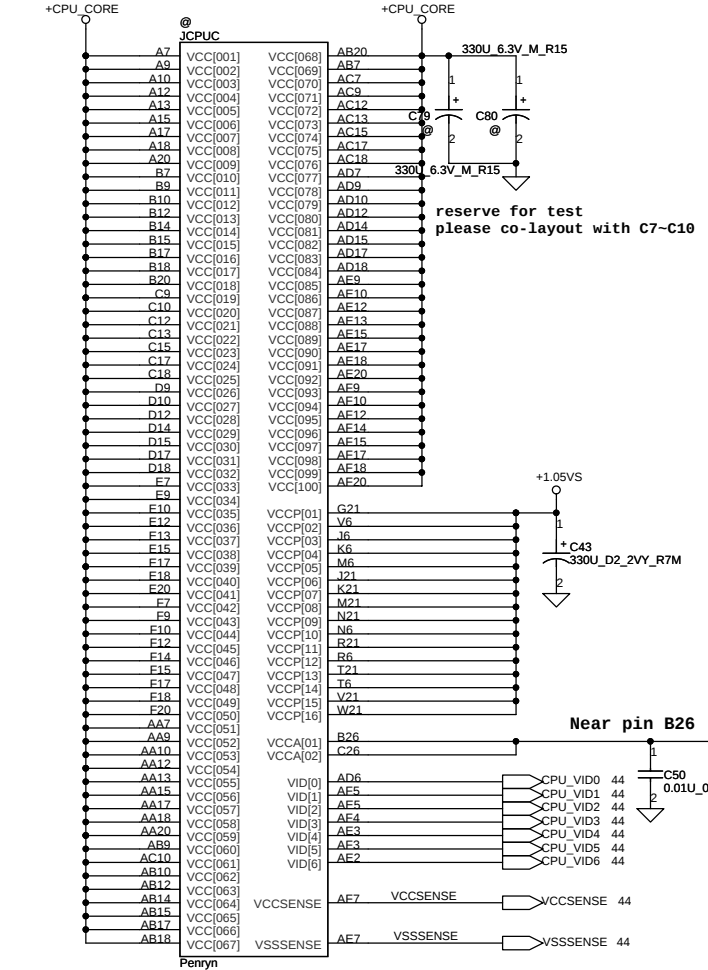
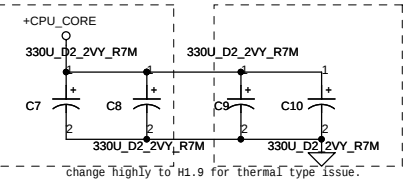


Reserve for debug close to CPU

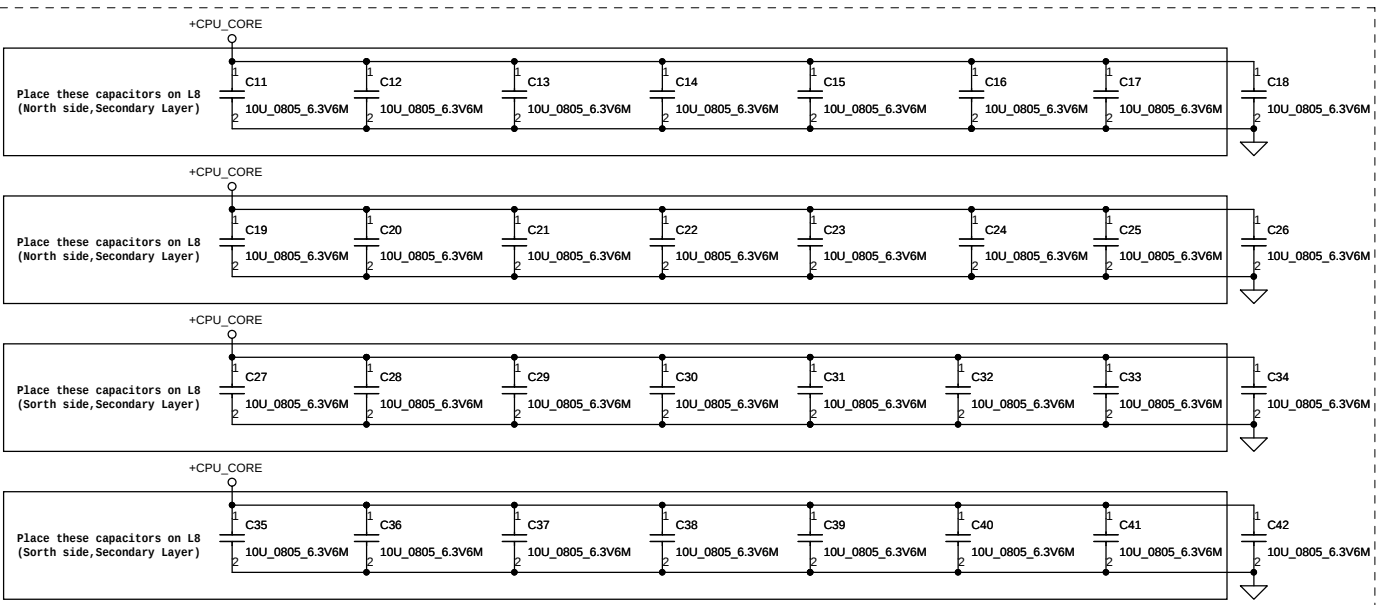


Near CPU CORE regulator

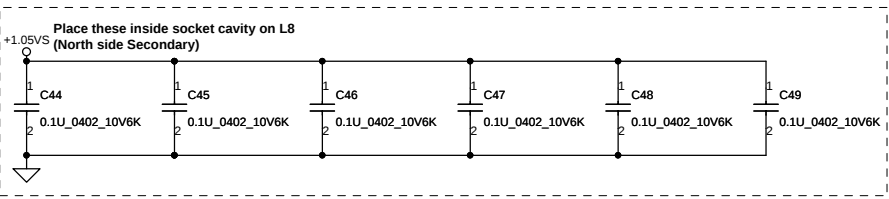
ESR <= 1.5m ohm
Capacitor > 1980uF



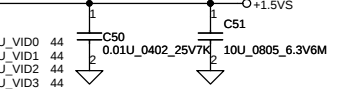
Length match within 25 mils.
The trace width/space/other is 14/7/25.



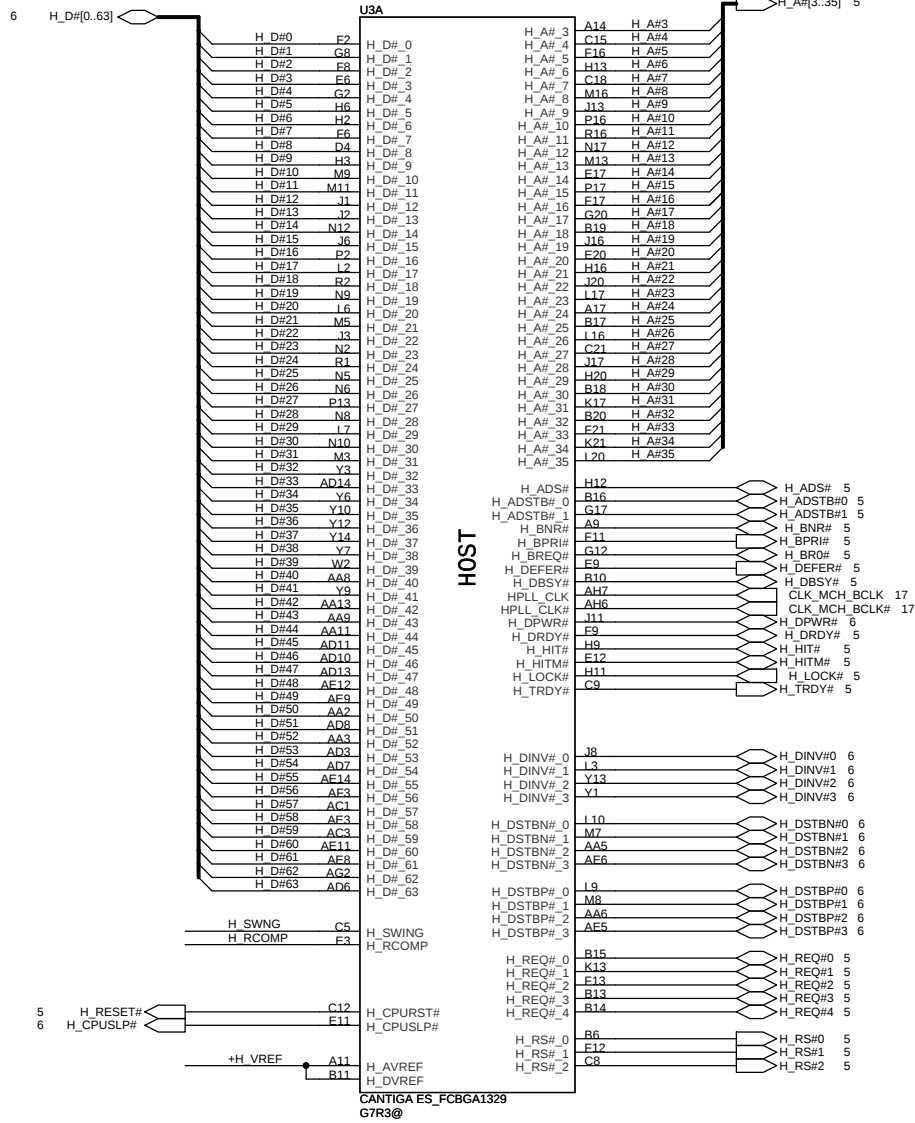
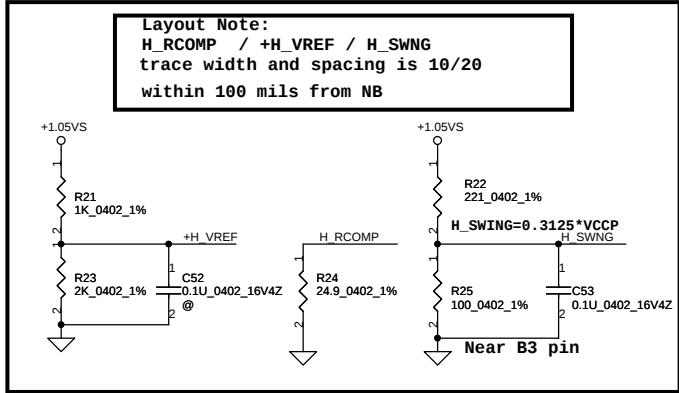
Mid Frequency Decoupling



Near pin B26

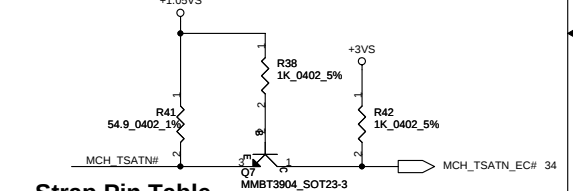
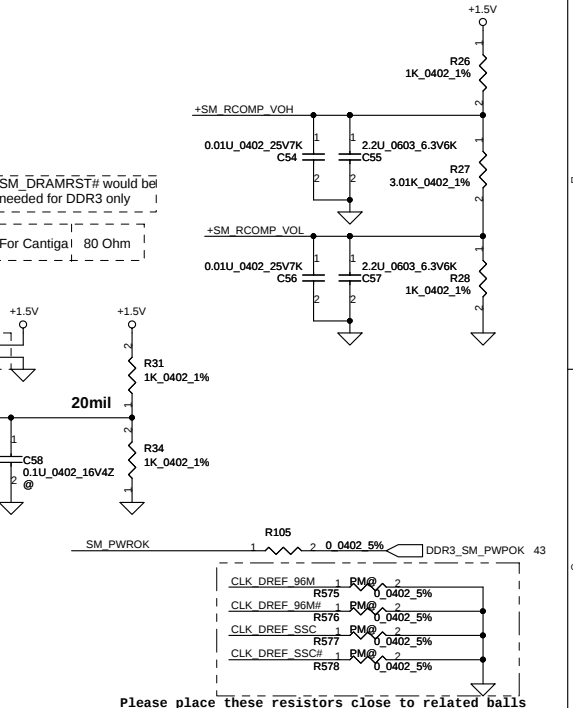
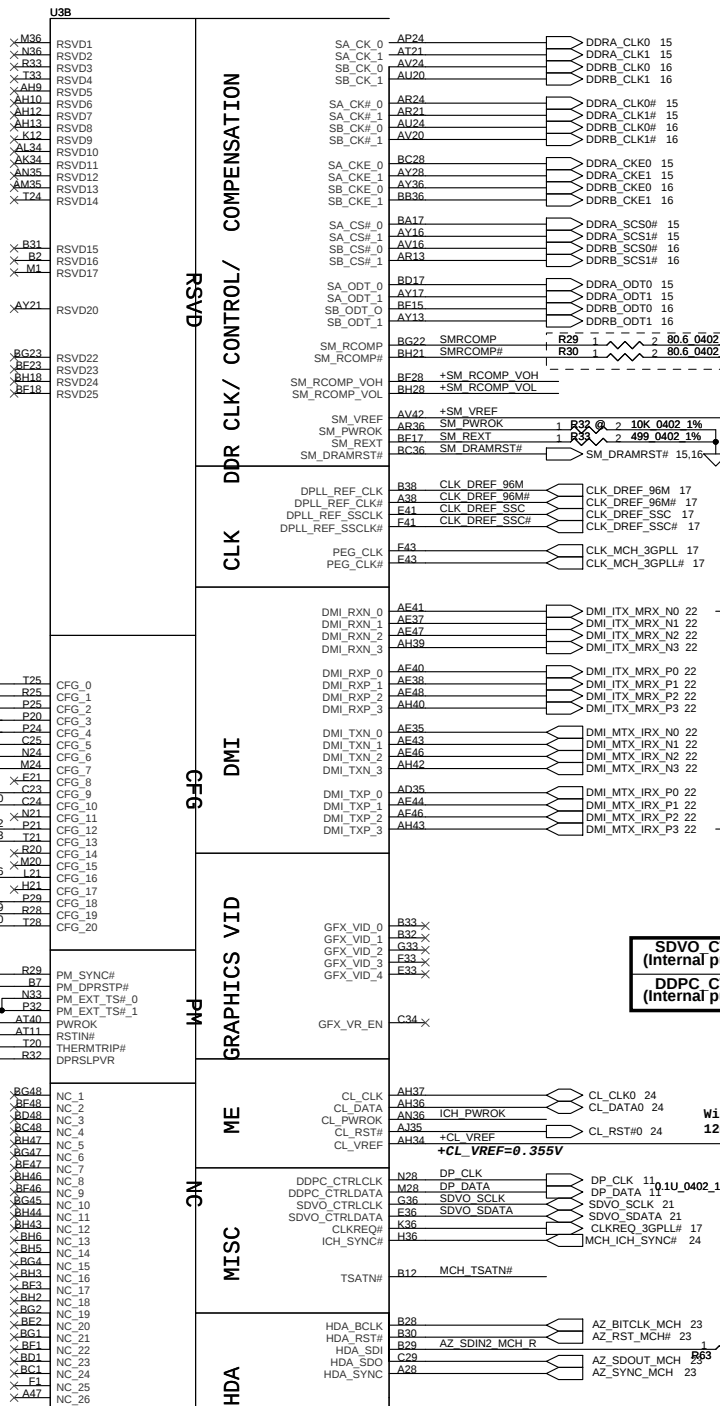
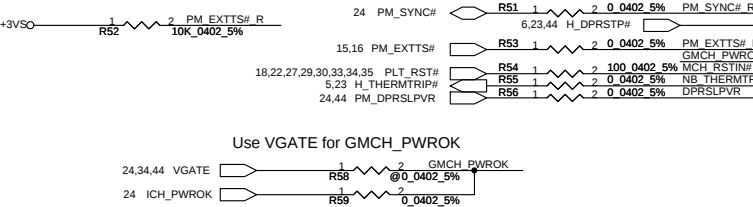
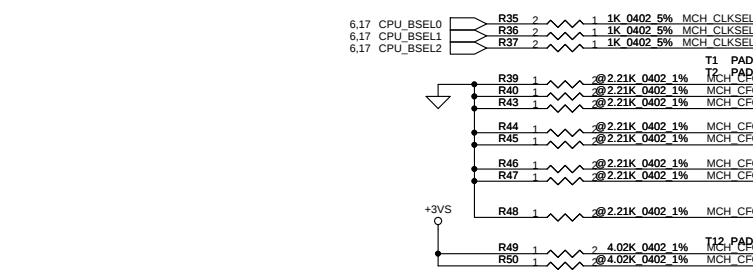


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Date		Tuesday, August 18, 2009		Sheet	7 of 46

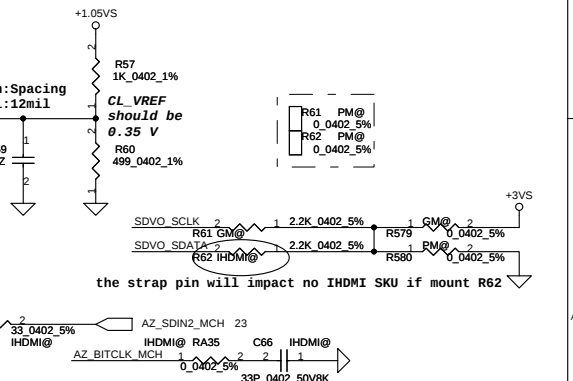


Strap Pin Table

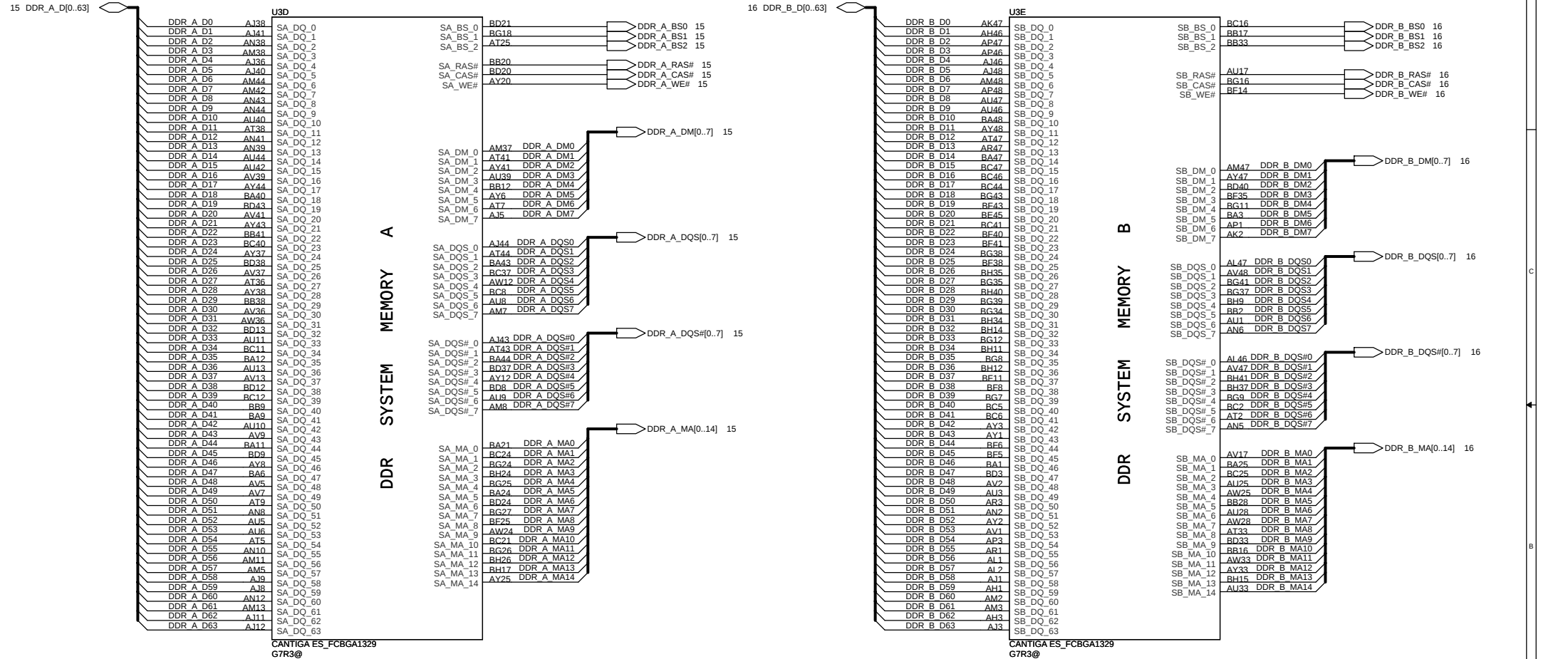
CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5 Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6 Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7 Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9 Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10 Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12] Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16 Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19 Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 Internal pull-down (PCIe/SDVO select)	0 = Only PCIe or [SDVO/DP/HDMI] is operational. *(Default) 1 = PCIe/[SDVO/DP/HDMI] are operating simu.



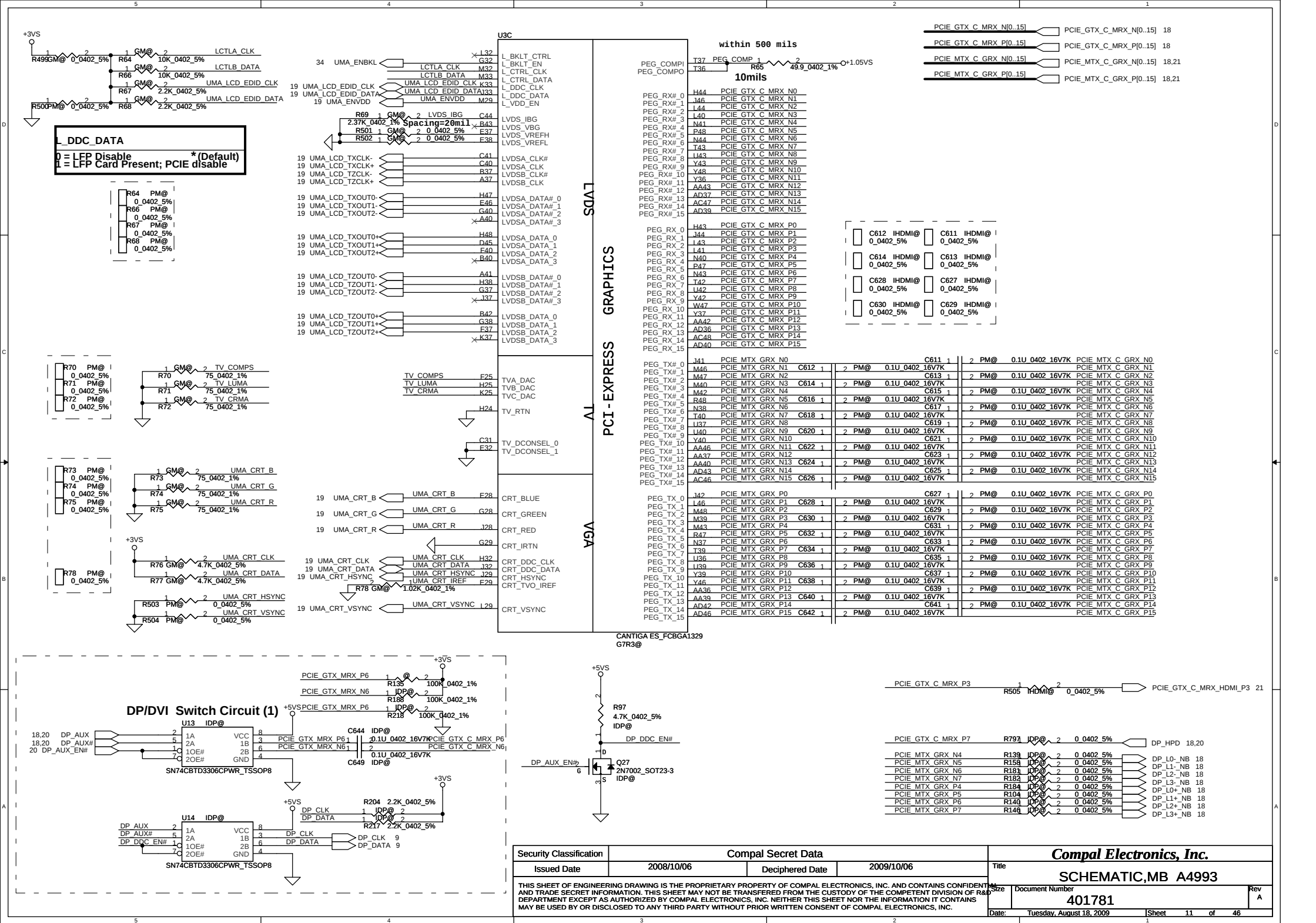
SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enable*(Default)

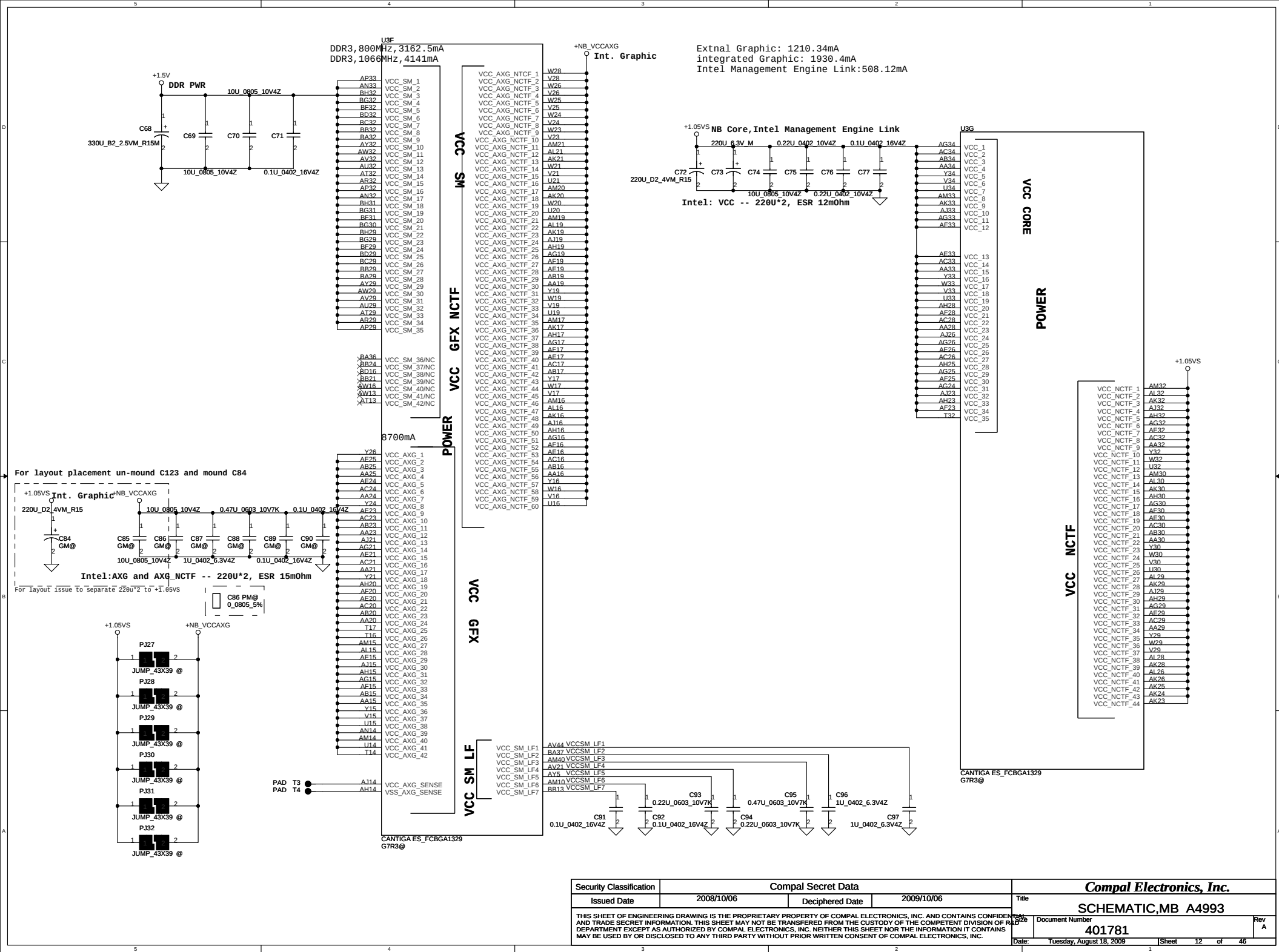


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		Date	Tuesday, August 18, 2009
		Sheet	9 of 46

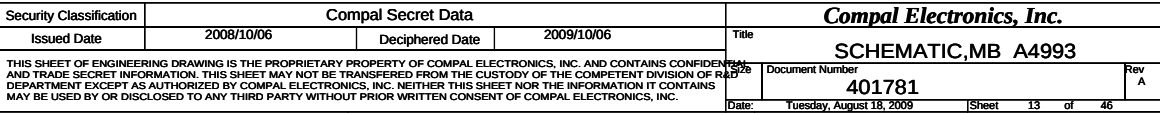


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							401781		A	
						Date: Tuesday, August 18, 2009			Sheet 10 of 46	



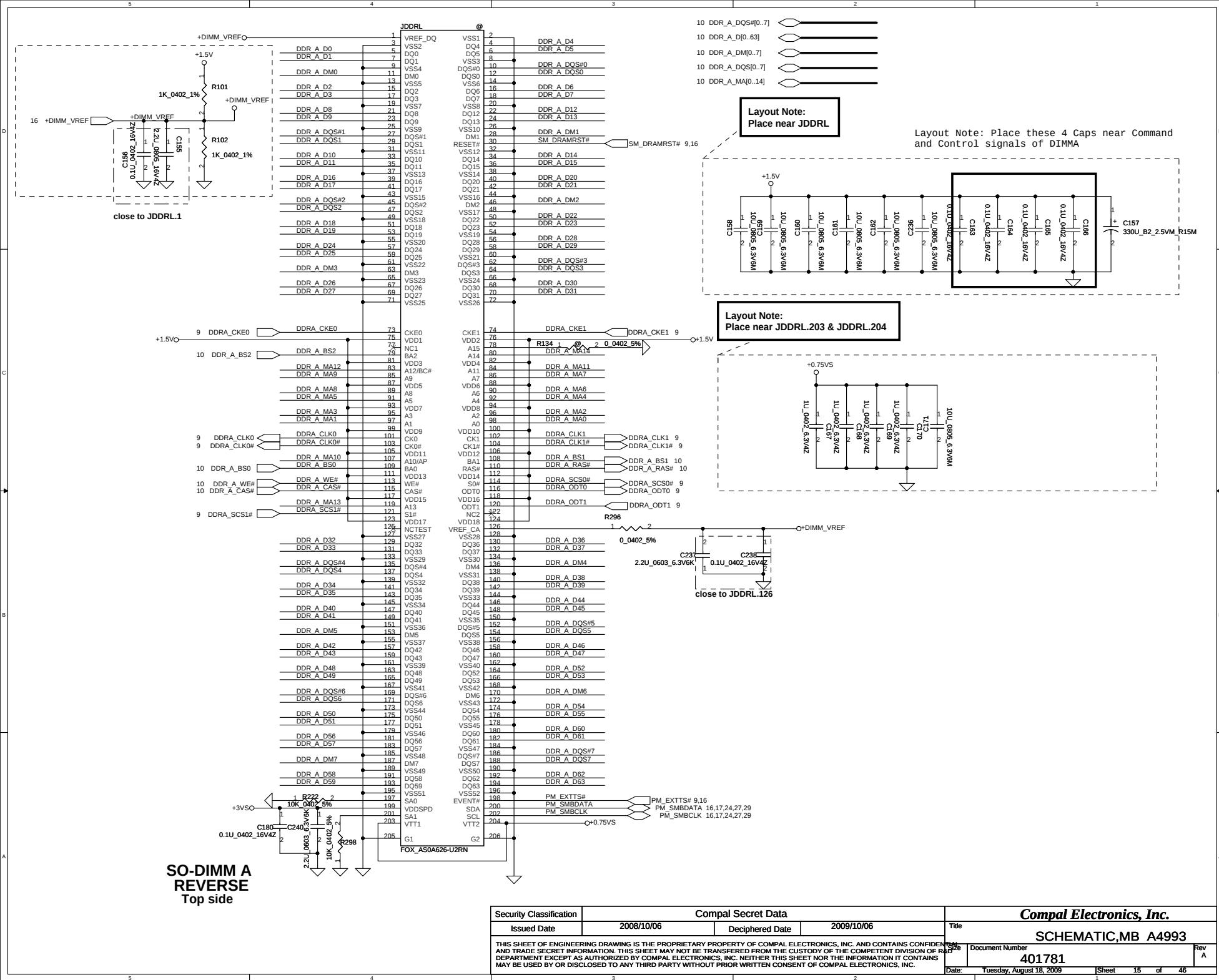


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				401781	
Date: Tuesday, August 18, 2009				Sheet 12 of 46	

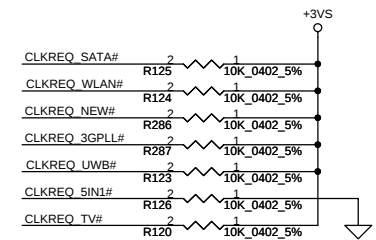
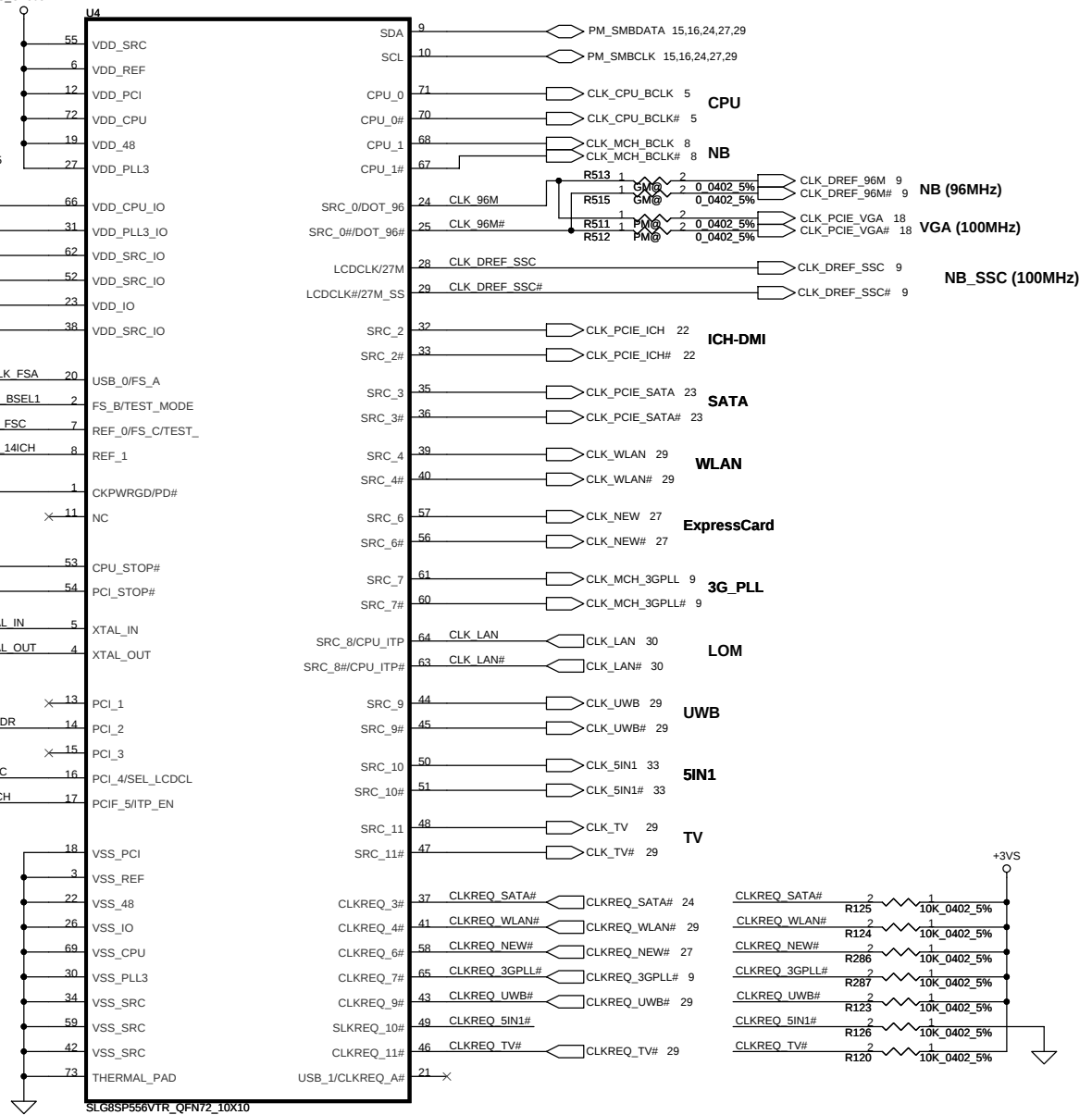
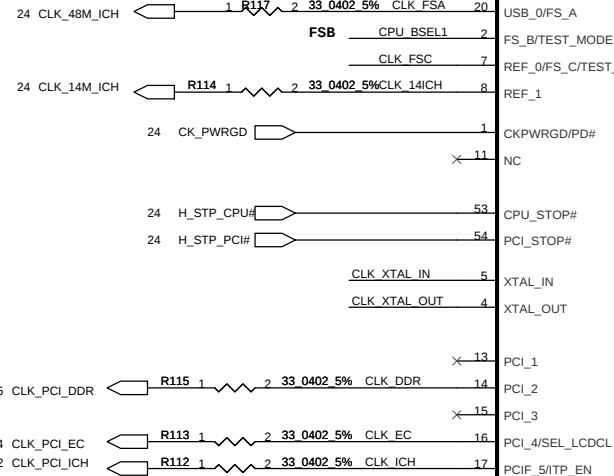
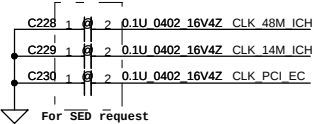
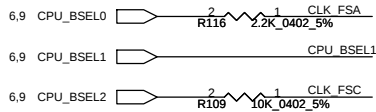
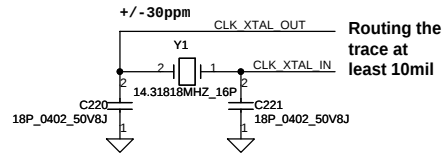
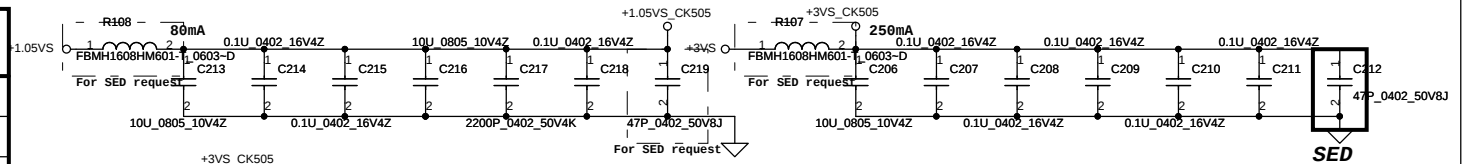




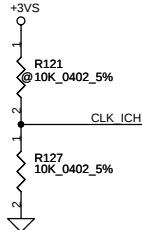
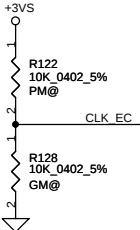
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					401781	A
				Date:	Tuesday, August 18, 2009	Sheet 14 of 46



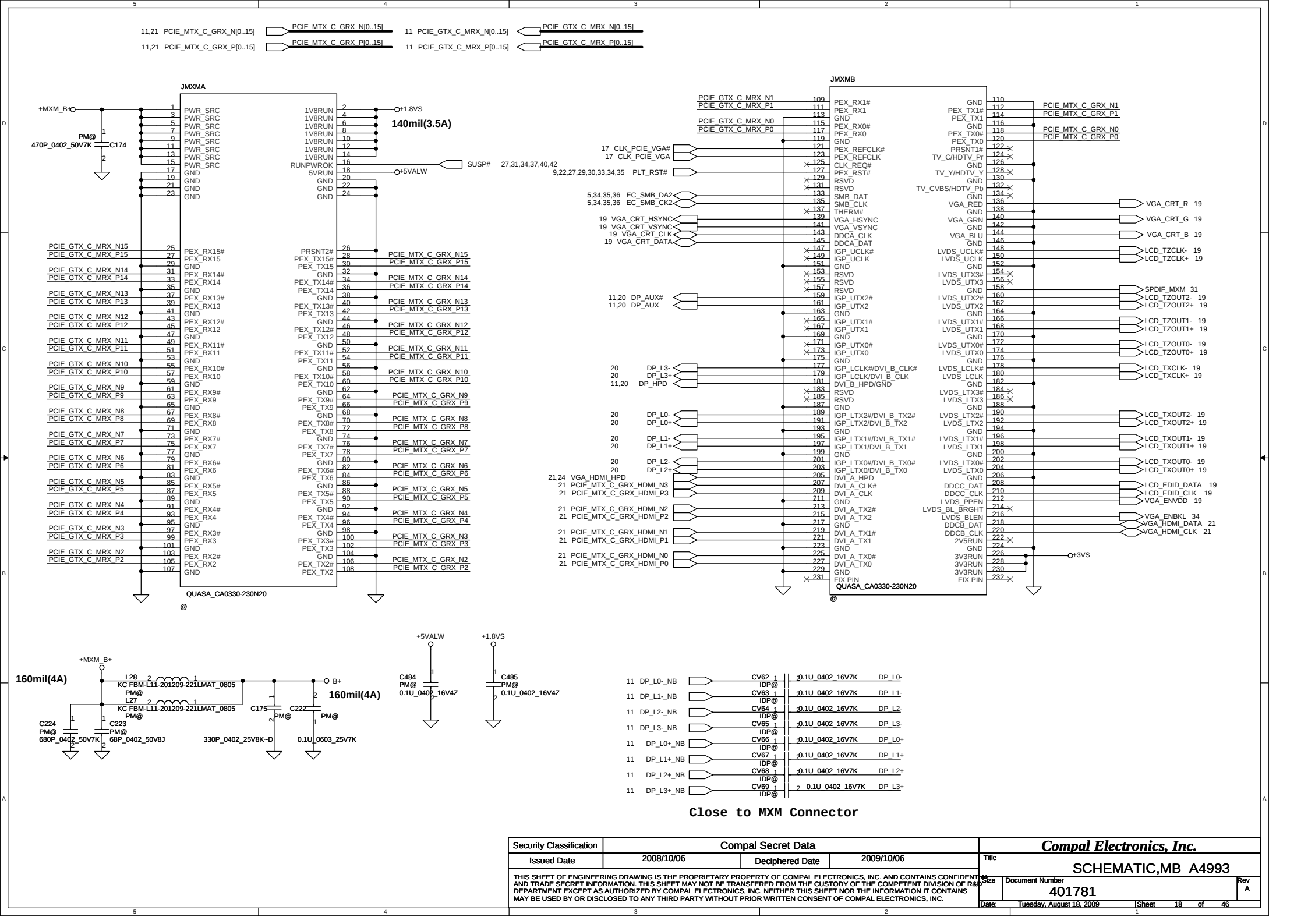
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



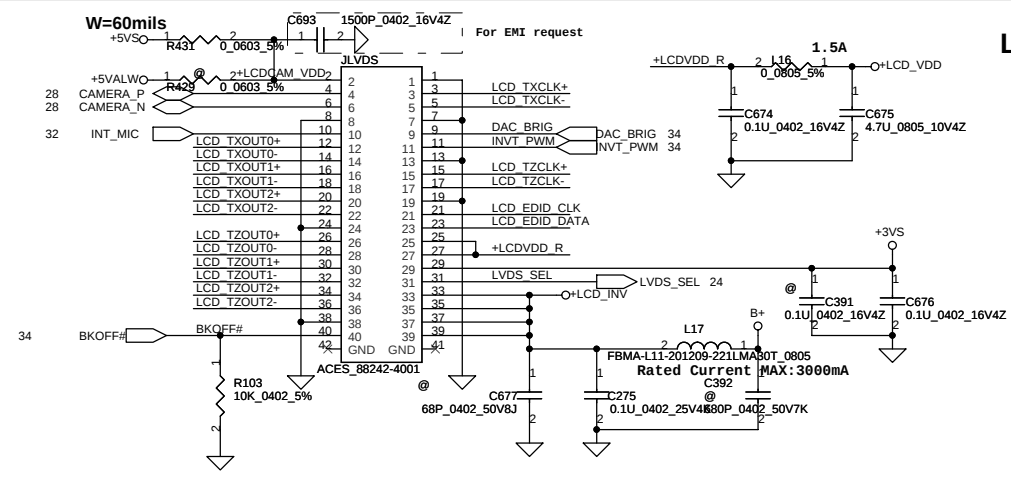
CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

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					401781	
				Date:	Tuesday, August 18, 2009	Sheet 17 of 46



LCD/PANEL BD. Conn.

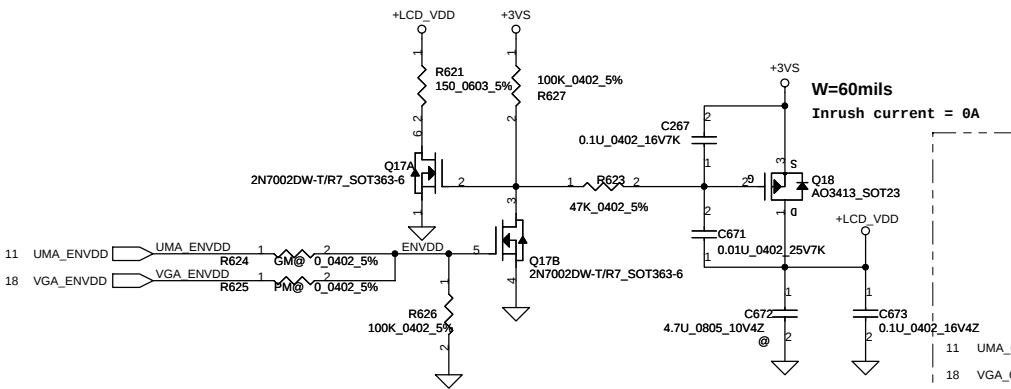
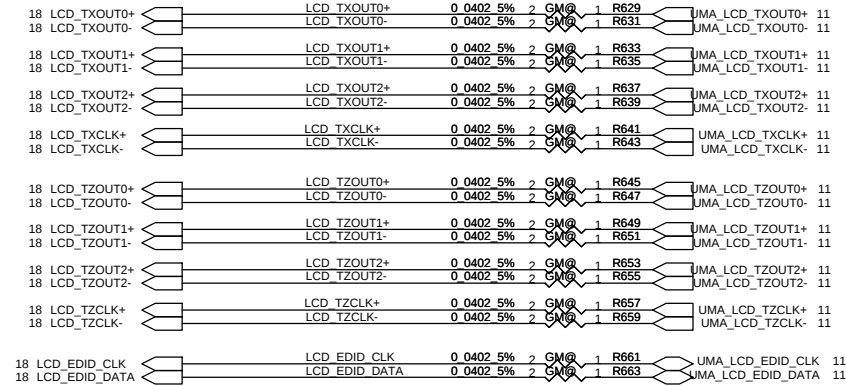


VGA side

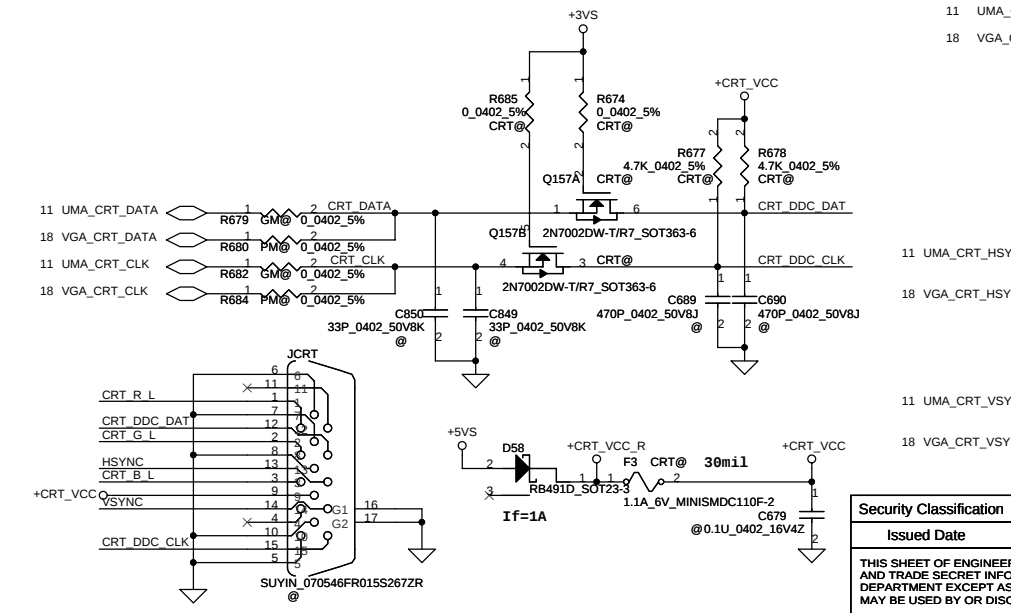
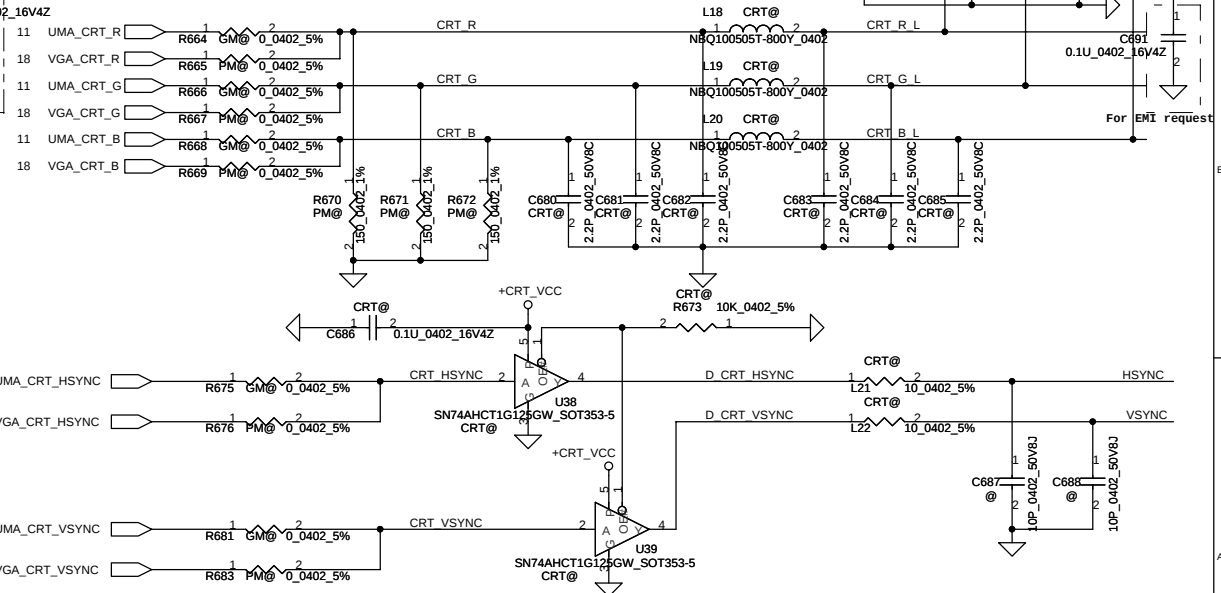
please link to VGA Conn. then link to LVDS Conn.

LVDS conn.

NB side

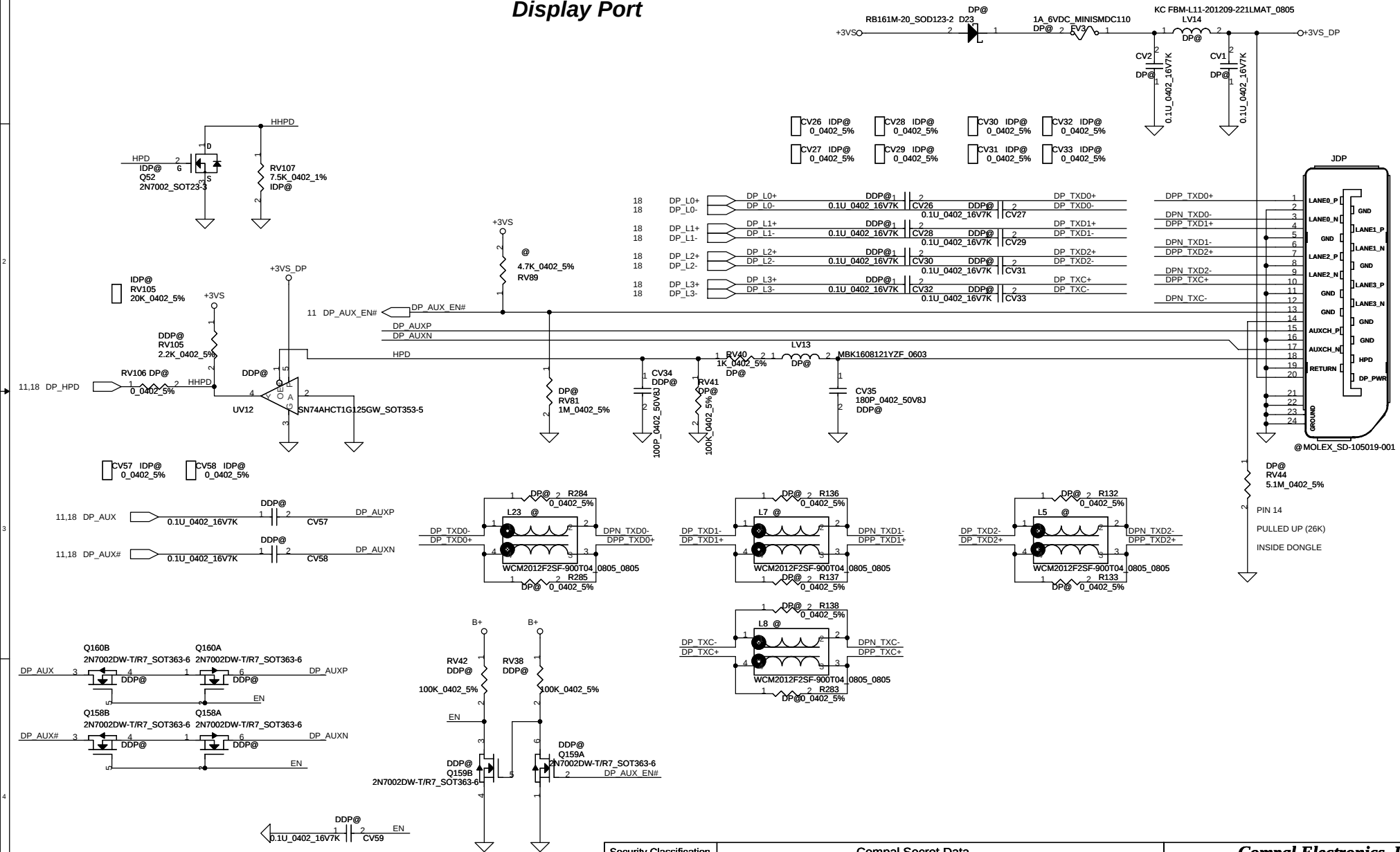


CRT CONNECTOR

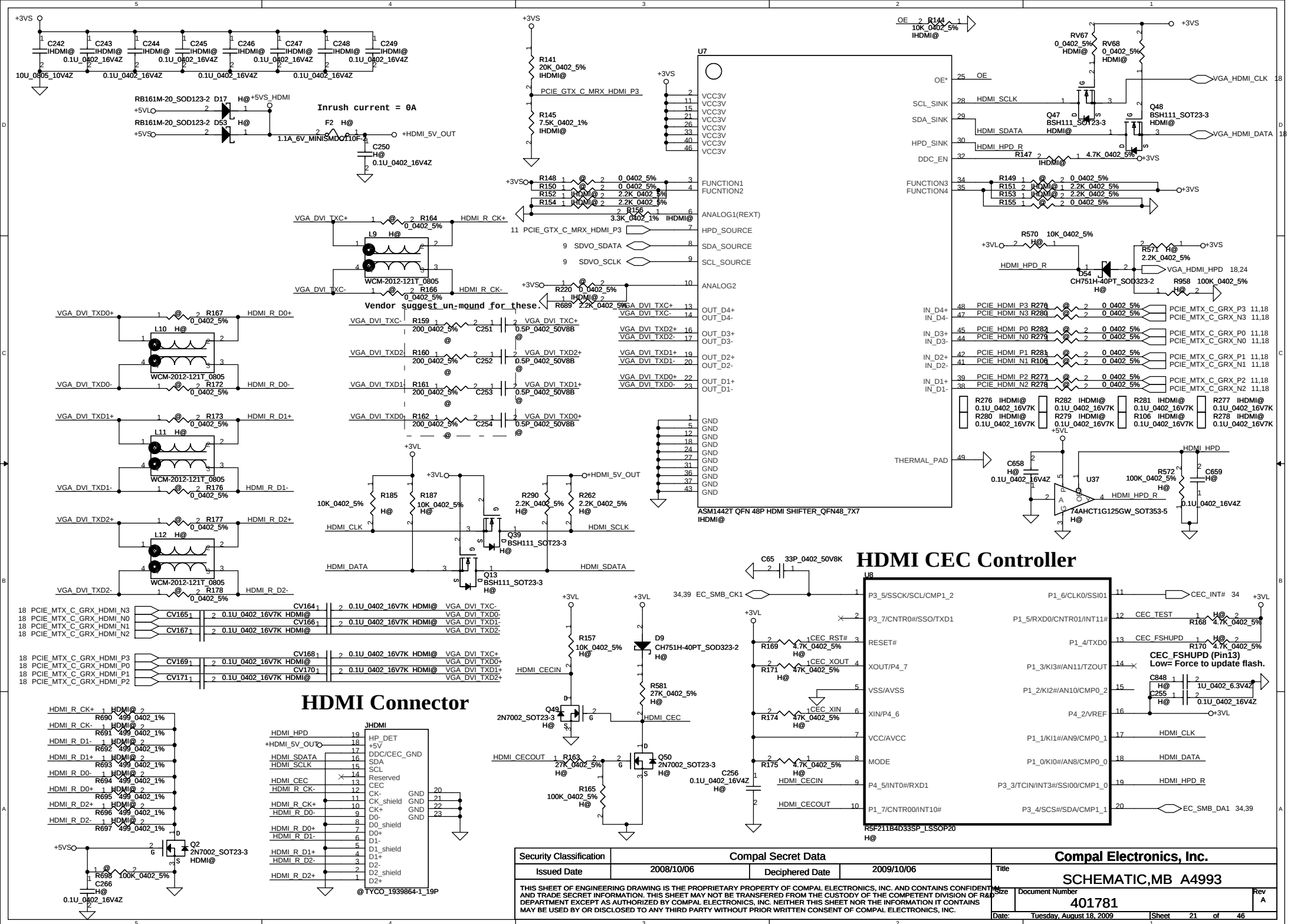


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				Date	Tuesday, August 18, 2009
				Sheet	19 of 46

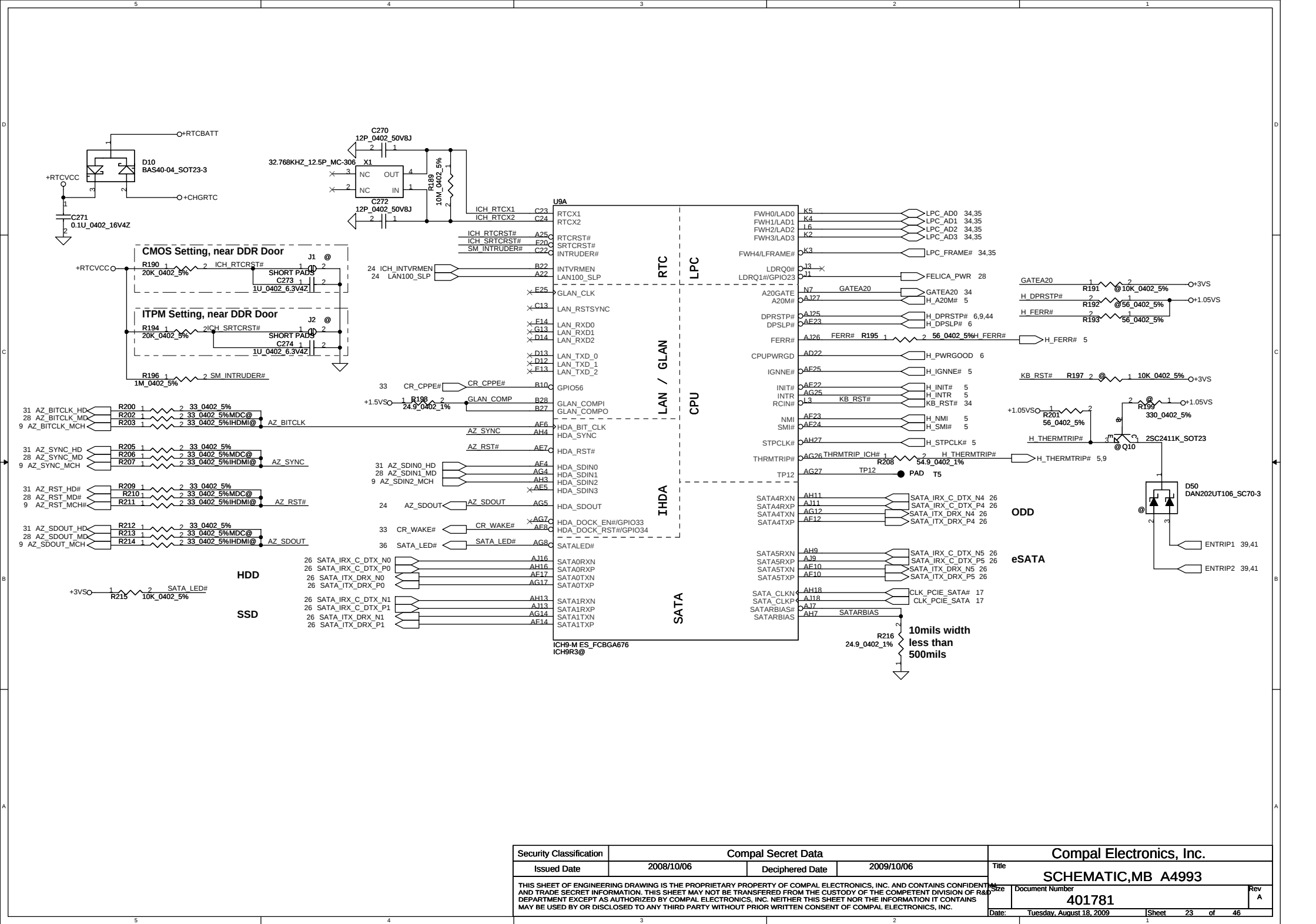
Display Port

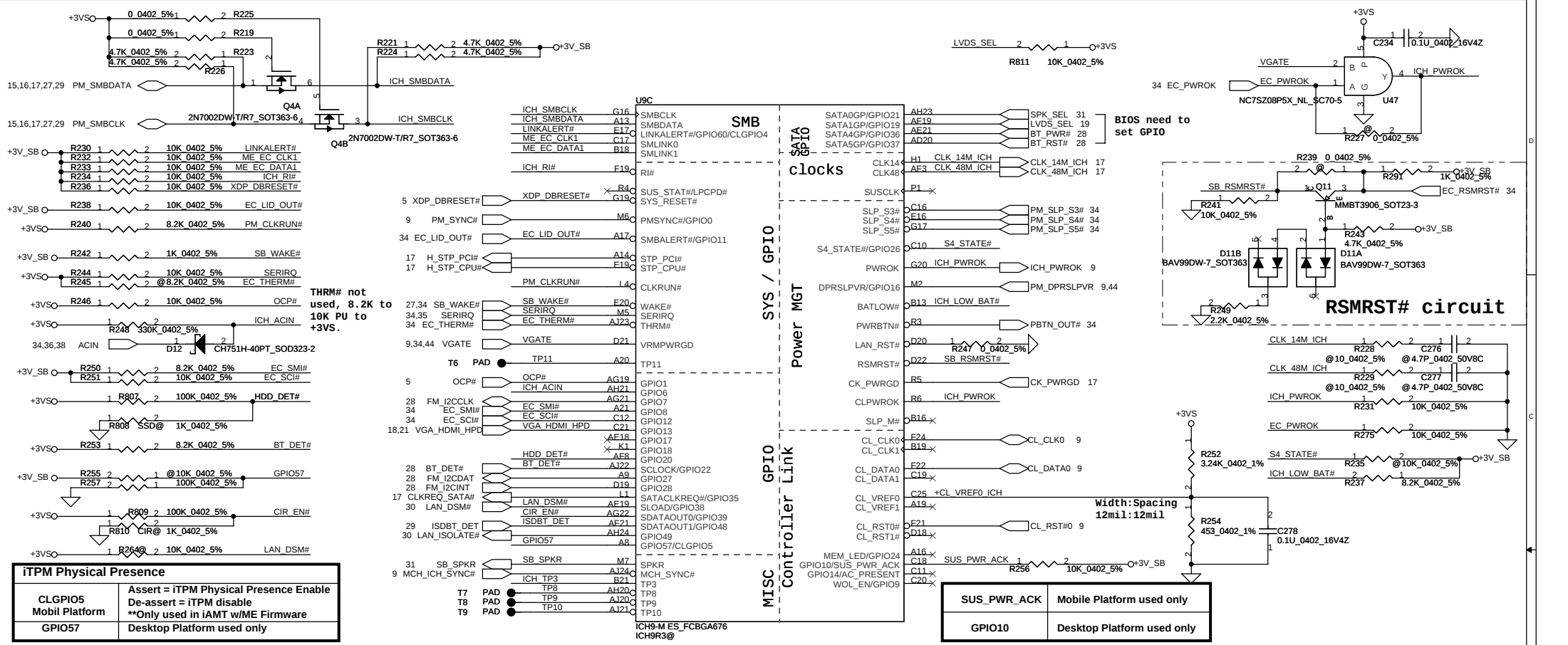


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				Date	Tuesday, August 18, 2009
				Sheet	20 of 46



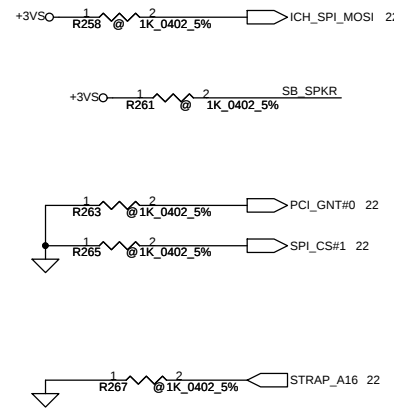
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							401781	A
Date:				Tuesday, August 18, 2009		Sheet	22	of 46





iTPM Physical Presence	
CLGPIO5	Assert = iTPM Physical Presence Enable
Mobil Platform	De-assert = iTPM disable
	**Only used in iAMT w/ME Firmware
GPIO57	Desktop Platform used only

ICH9M Strap Pin

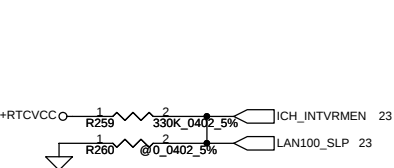


Internal TPM Strap(Internal pull-down)	
SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)	
SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)



Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

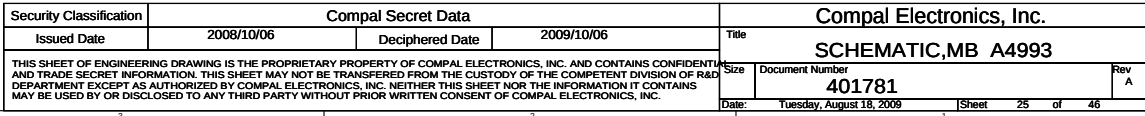
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

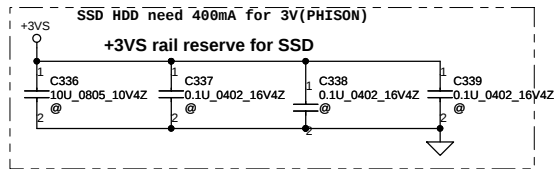
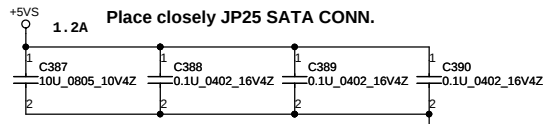
Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

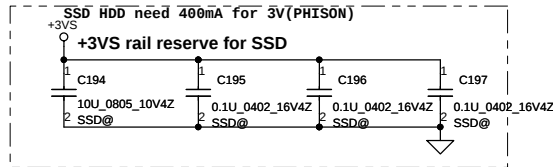
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				401781	Rev A
				Date	Tuesday, August 18, 2009
				Sheet	24 of 46



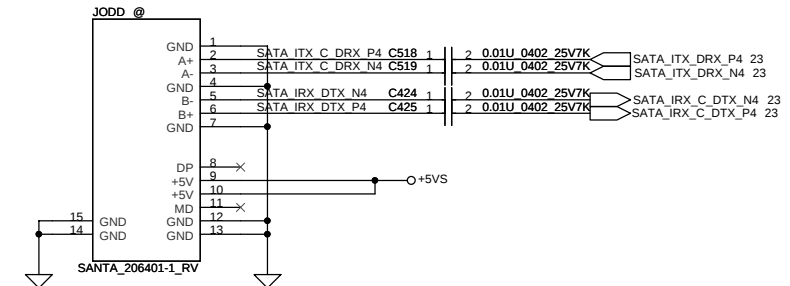
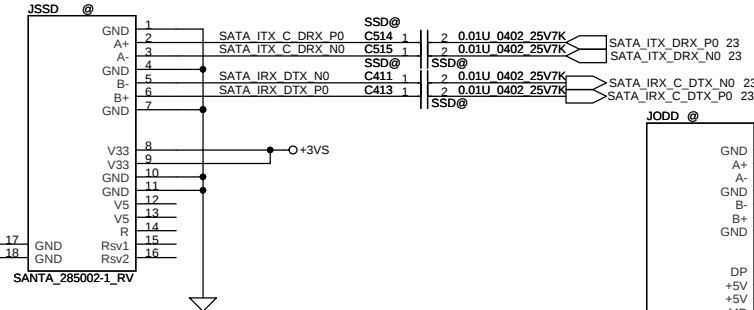
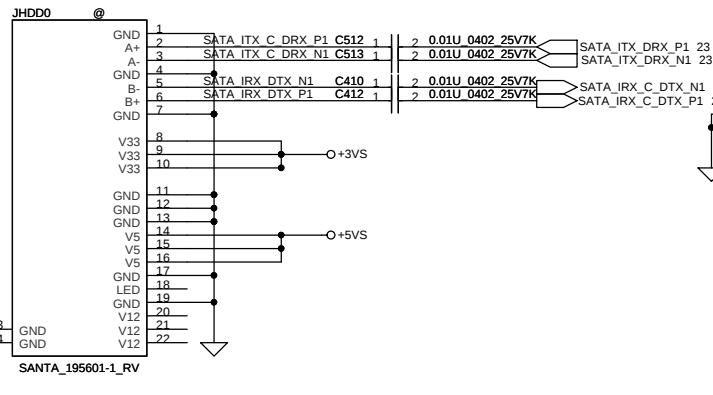
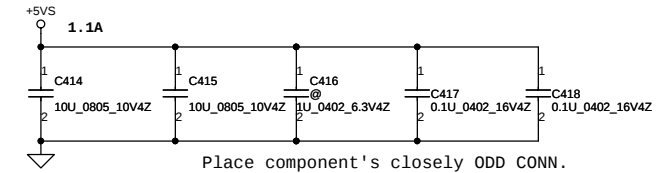
SATA HDD Conn.



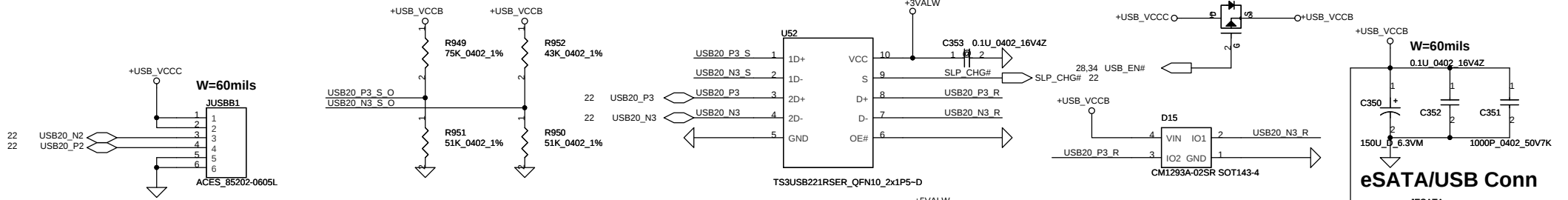
SSD Conn.



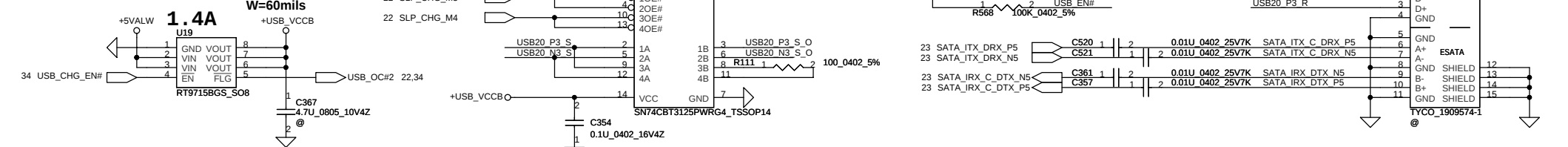
SATA ODD Conn



USB Conn.

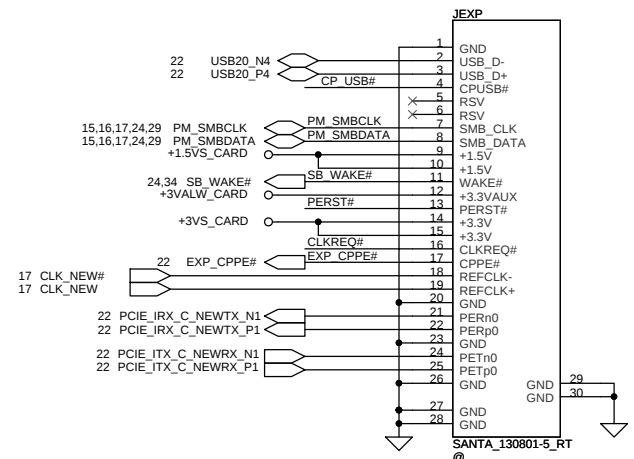
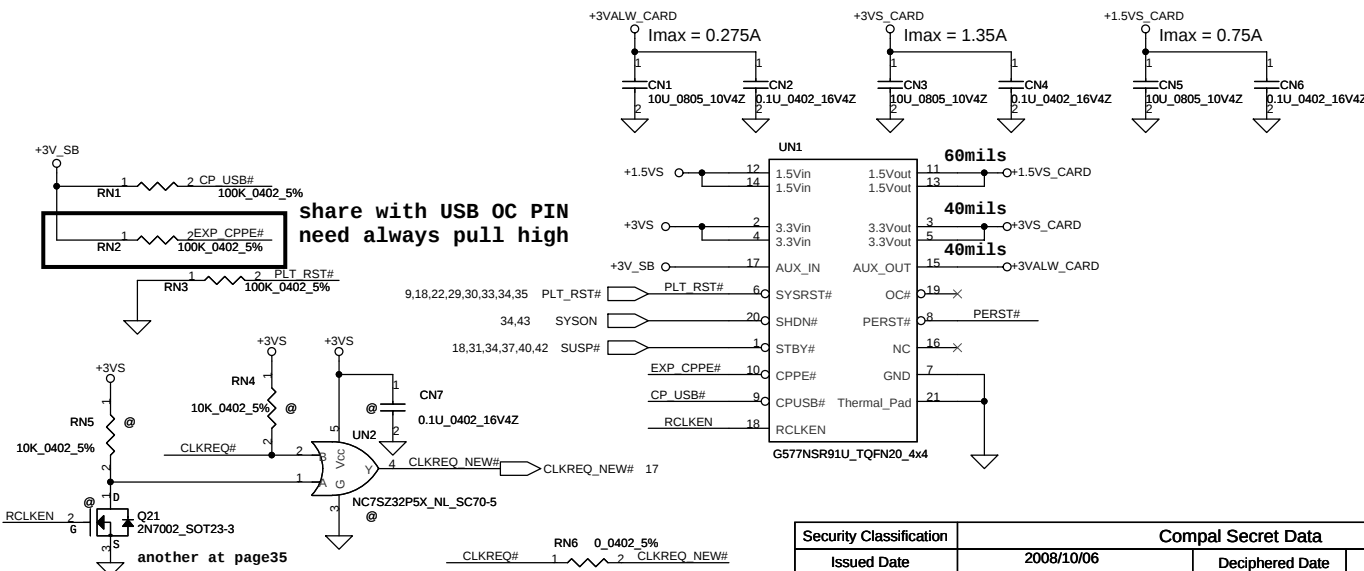
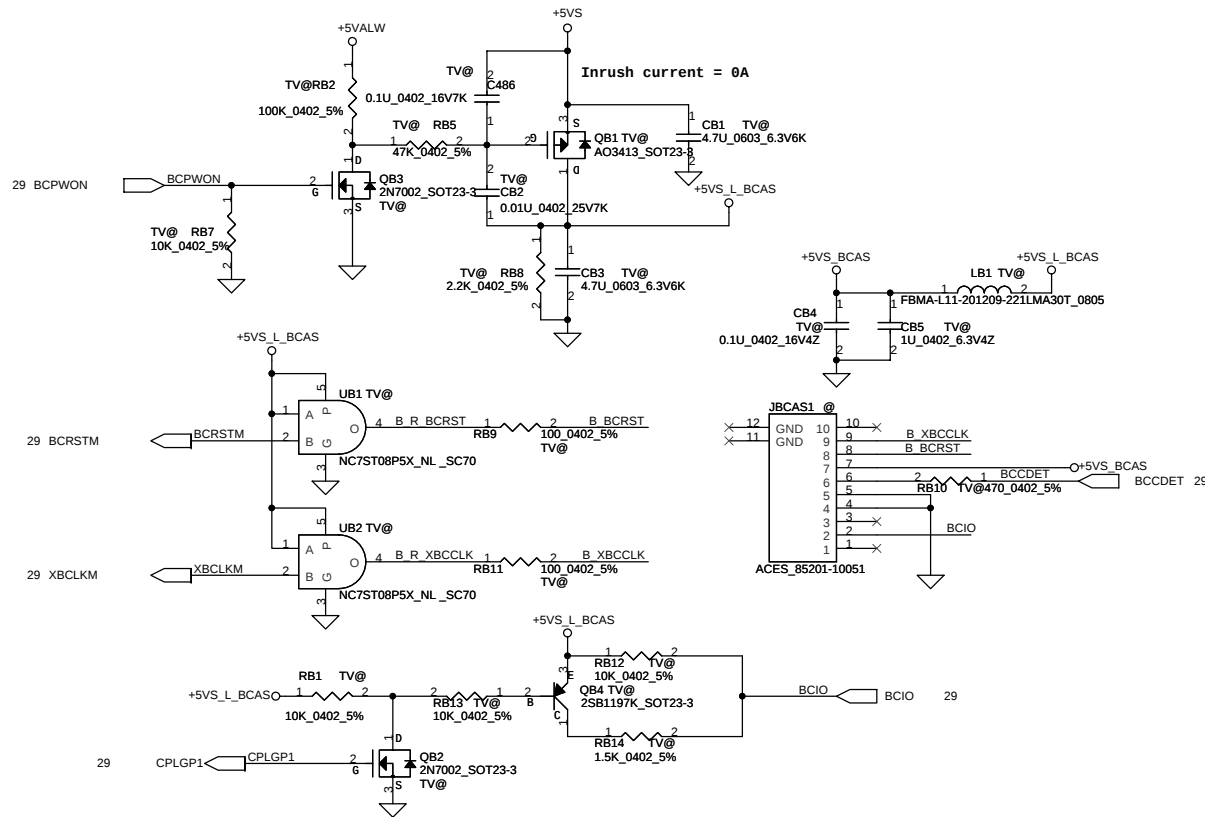


eSATA/USB



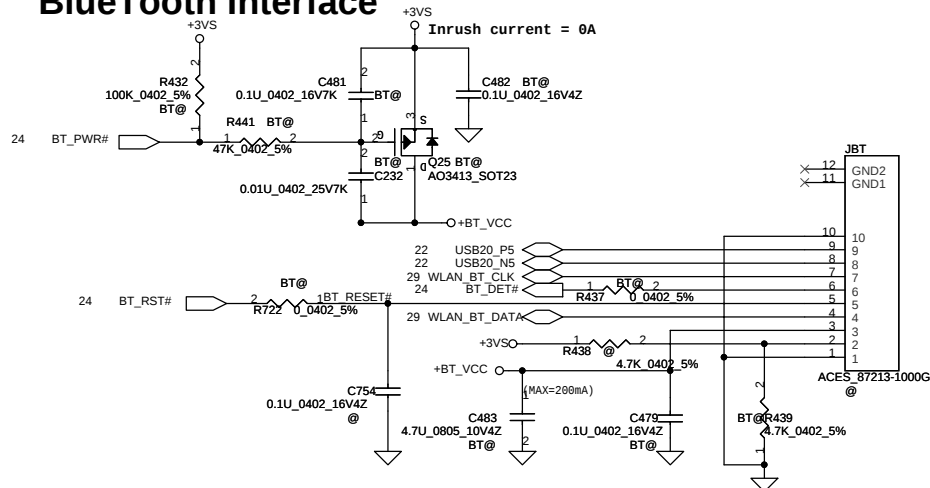
	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG	FUNCTION	Security Classification	Compal Secret Data	Compal Electronics, Inc.	
Mode 3	HIGH	LOW	LOW	D=1D	Issued Date	2008/10/06	Deciphered Date	2009/10/06
Mode 4	LOW	HIGH	HIGH	D=2D	Title			
					SCHEMATIC,MB A4993			
					Size			
					Document Number			
					401781			
					Date			
					Tuesday, August 18, 2009			
					Sheet			
					26 of 46			
					Rev			
					A			

B-CAS Circuit

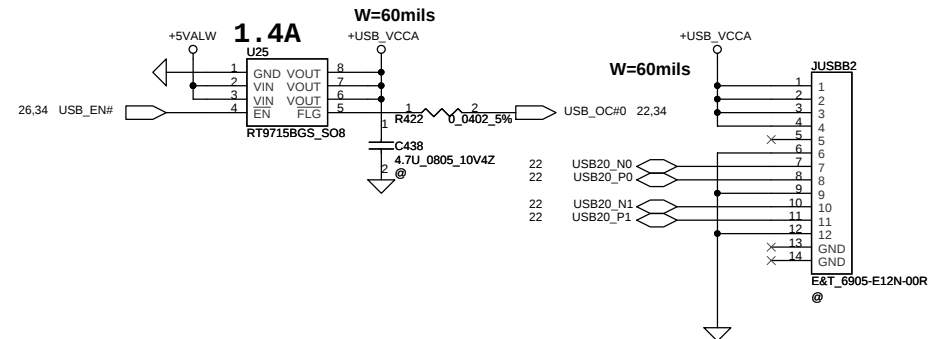


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				401781	
Date: Tuesday, August 18, 2009				Sheet 27	of 46

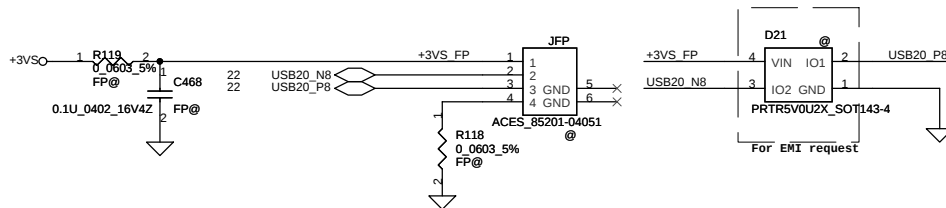
BlueTooth Interface



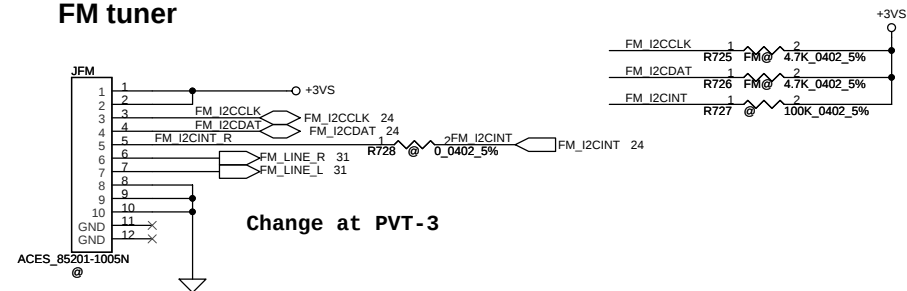
Right USB Board



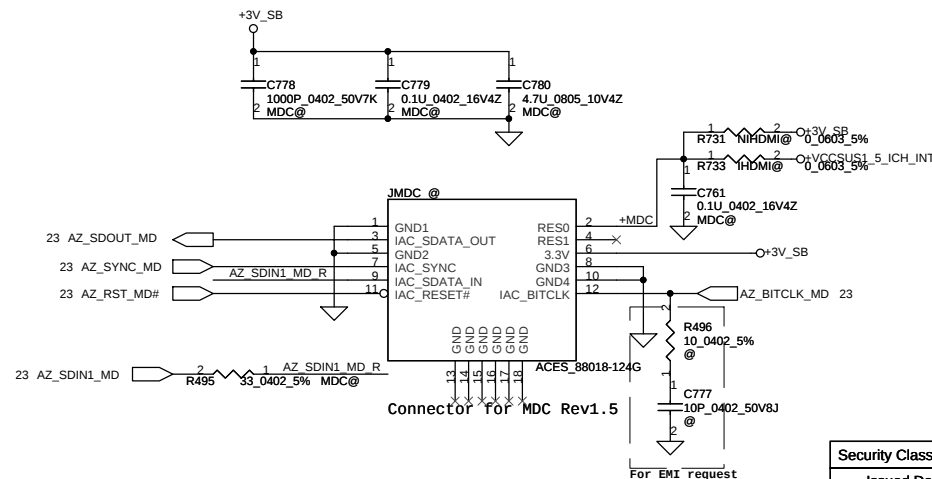
Finger printer



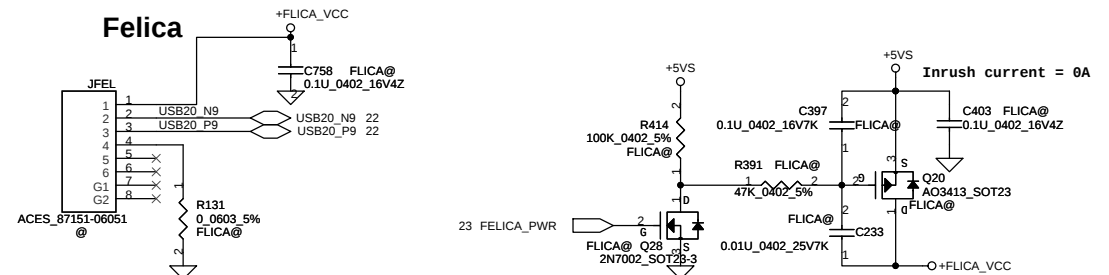
FM tuner



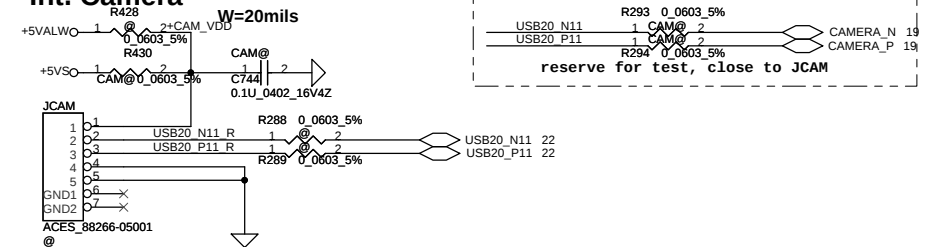
MDC 1.5 Conn.



Felica

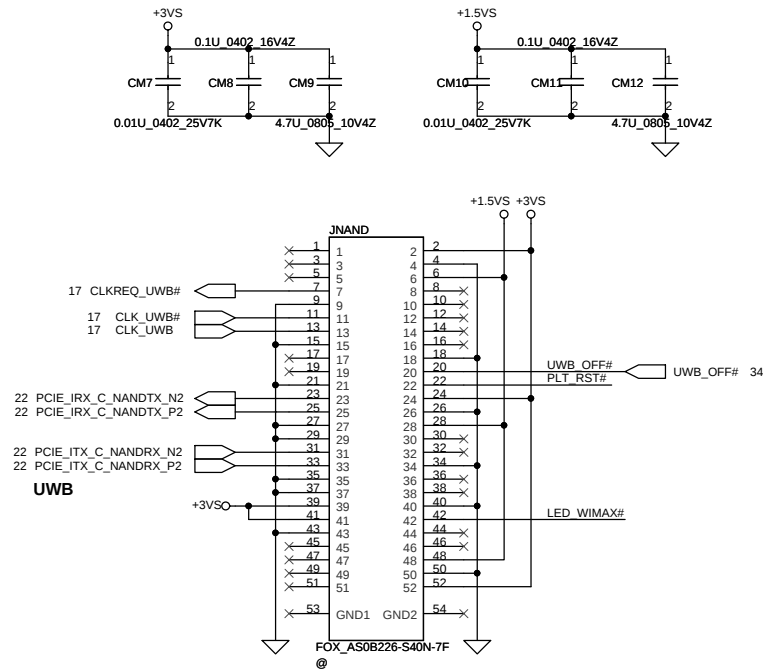


Int. Camera

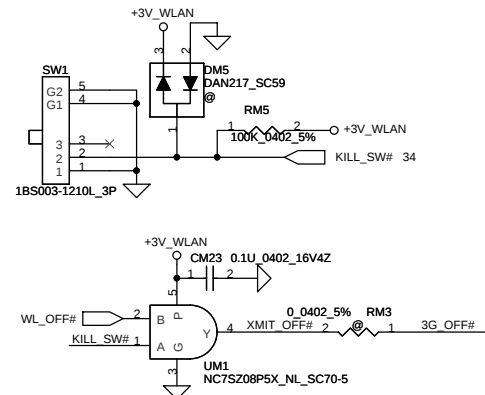


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				401781				Rev A			
Date:				Tuesday, August 18, 2009				Sheet 28 of 46			

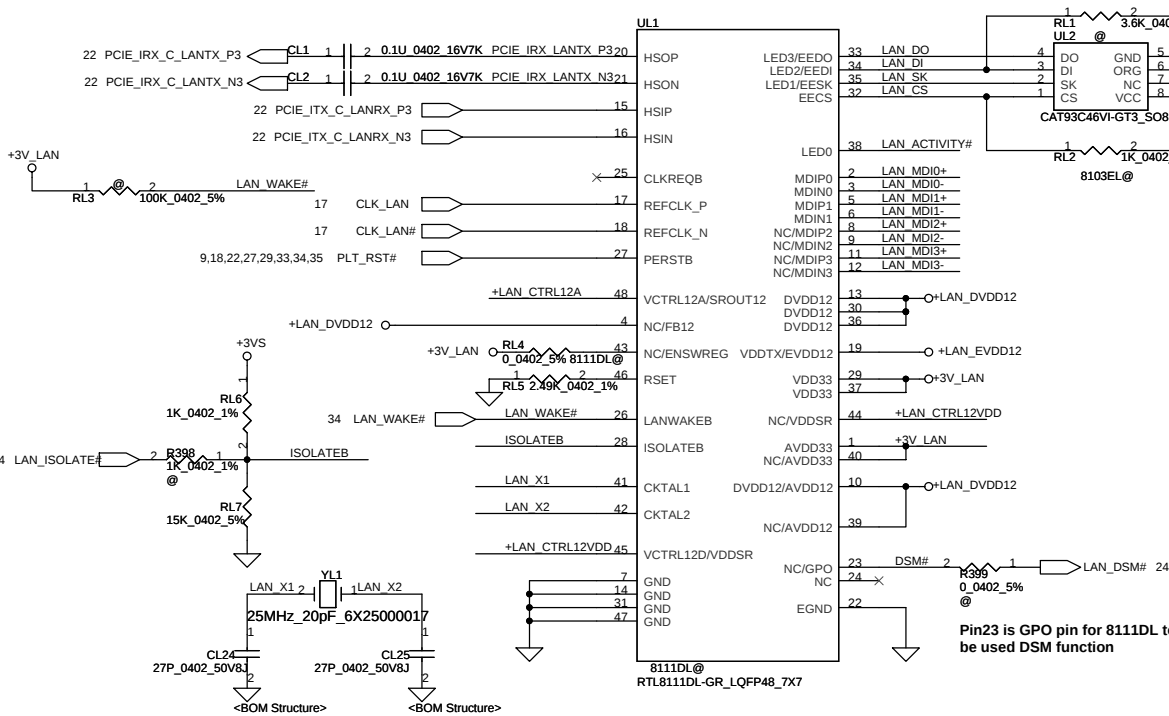
UWB/JET (Slot3)



Kill SWITCH

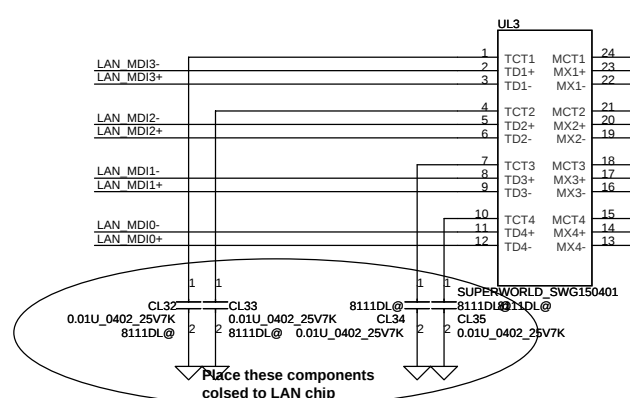


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				401781		
				Date:	Tuesday, August 18, 2009	Sheet 29 of 46

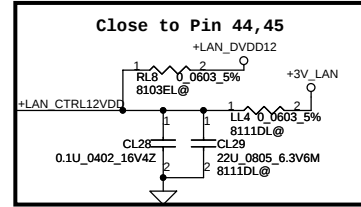
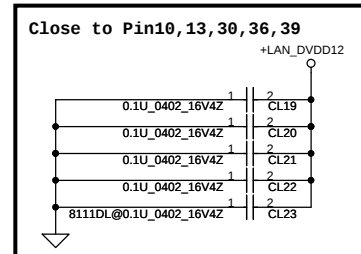
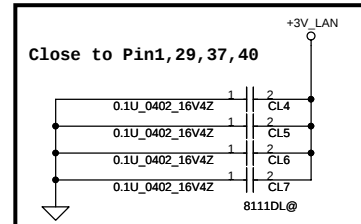
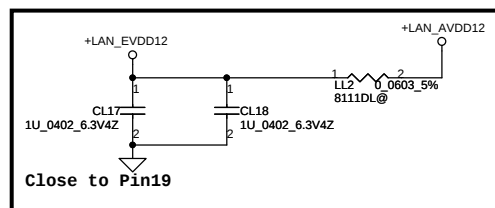
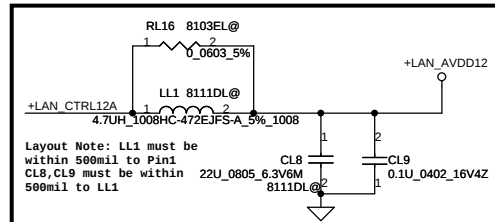
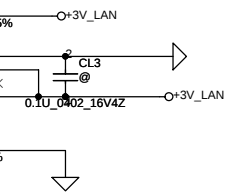


pin assignments table for difference

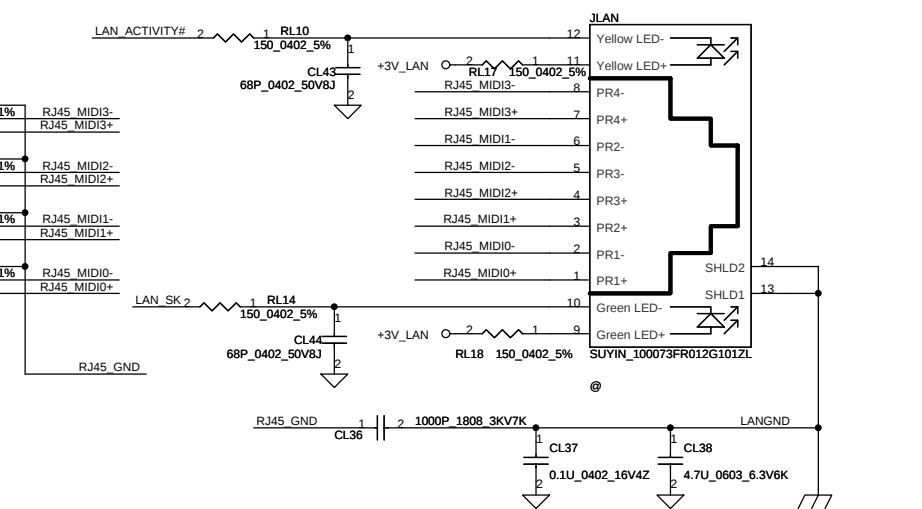
Pin	8111DL	8103EL
4	FB12	NC
8	MDIP2	NC
9	MDIN2	NC
10	AVDD12	DVDD12
11	MDIP3	NC
12	MDIN3	NC
19	EVDD12	VDDTX
23	GPO	NC
33	EED0	LED3
34	EED1	LED2
35	EESK	LED1
39	AVDD12	NC
40	AVDD33	NC
43	ENSR	NC
44	VDDSR	NC
45	VDDSR	VCTRL12D
48	SROUT12	VCTRL12A



Place these components
closer to LAN chip

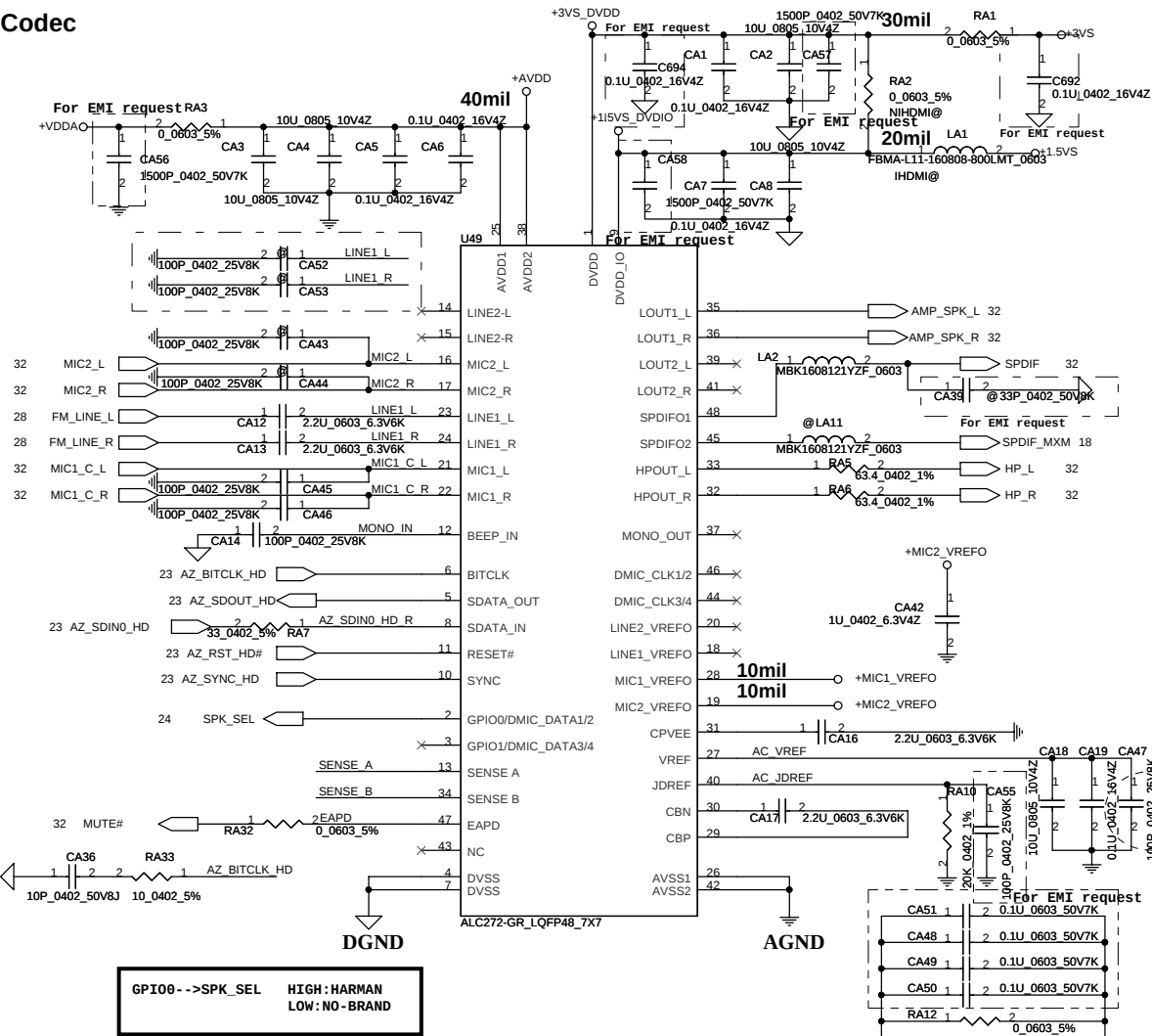


LAN Conn.

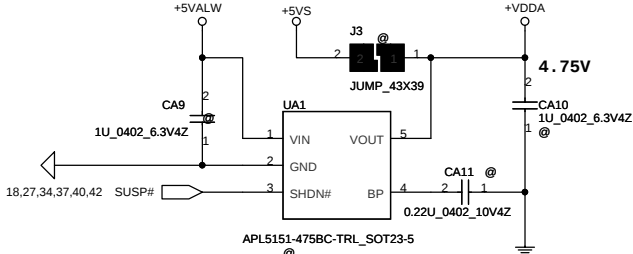


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				401781	
Date: Tuesday, August 18, 2009				Sheet 30	of 46

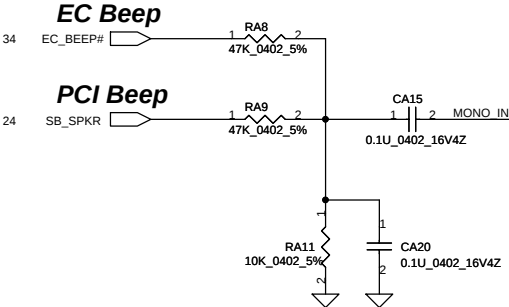
Codec



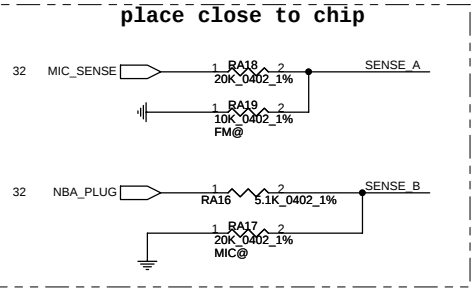
Audio regulator



Beep sound

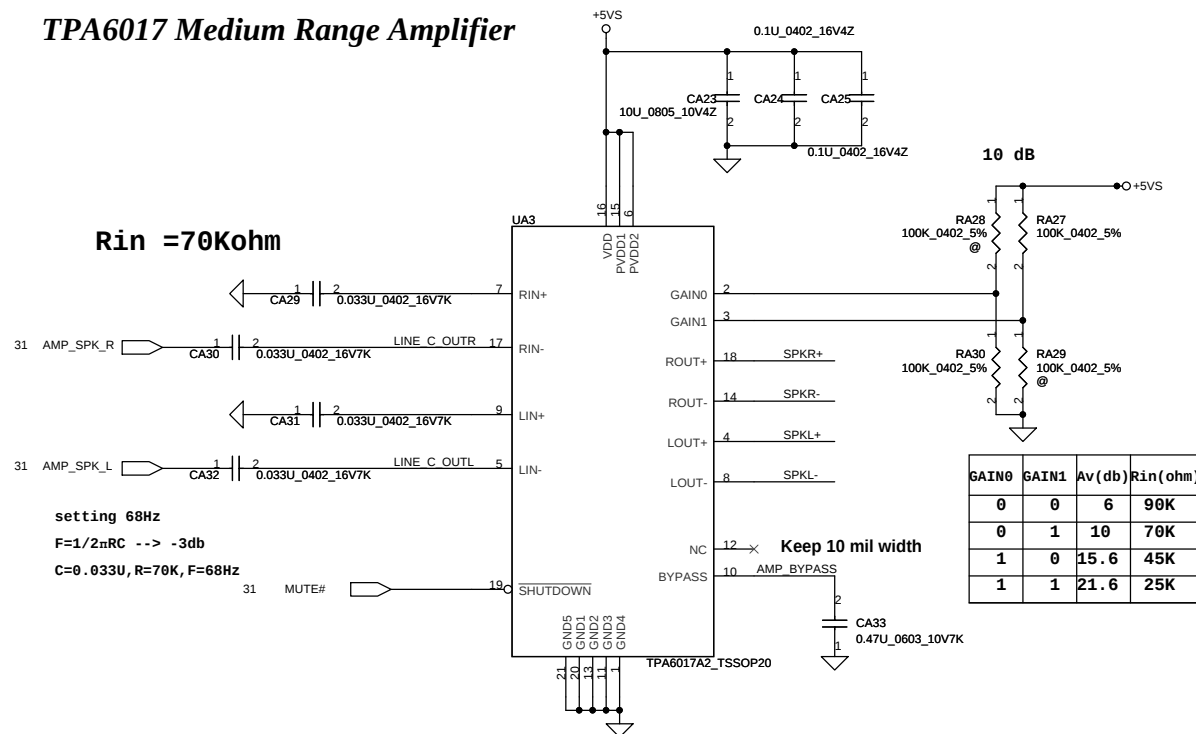


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

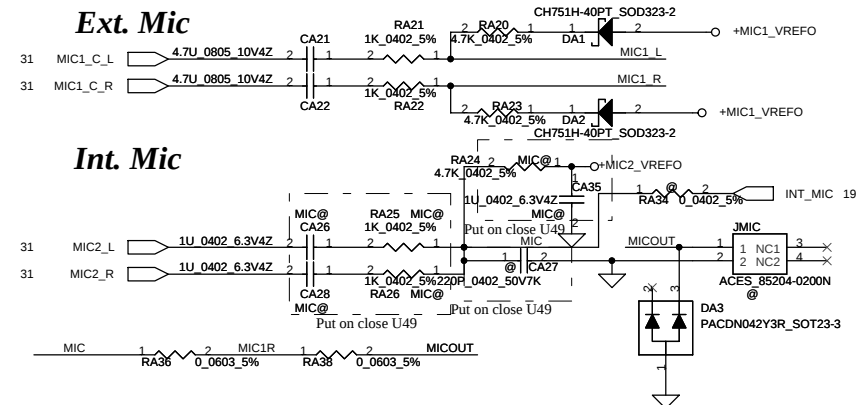


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				Document Number	Rev A
				Date	Tuesday, August 18, 2009
				Sheet	31 of 46

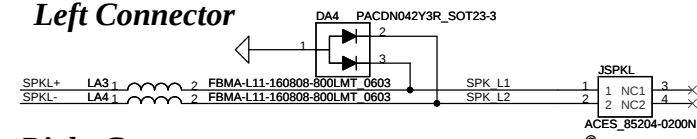
TPA6017 Medium Range Amplifier



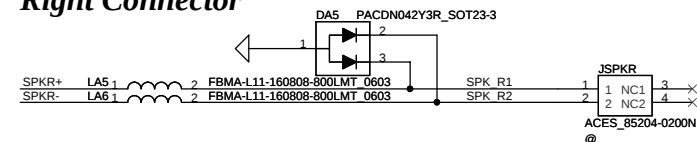
GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K



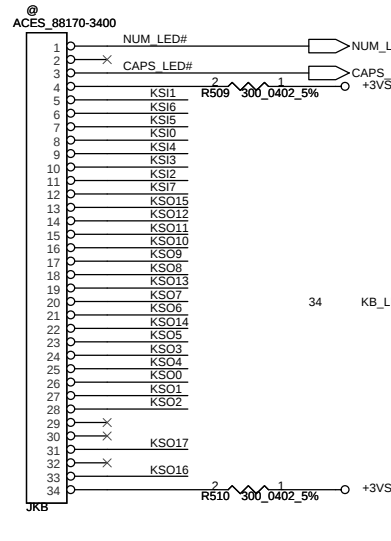
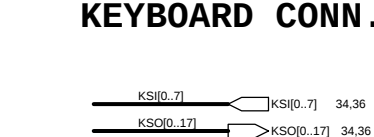
Left Connector



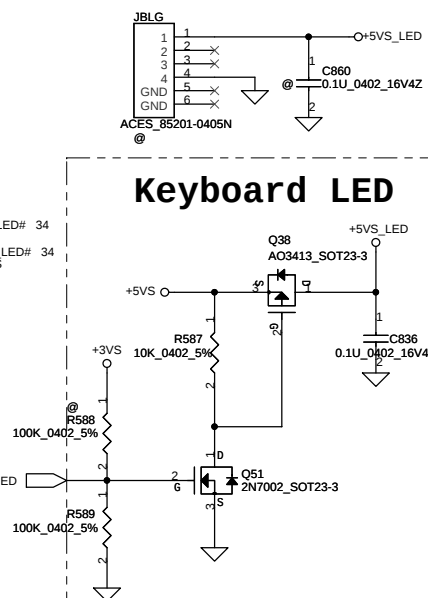
Right Connector



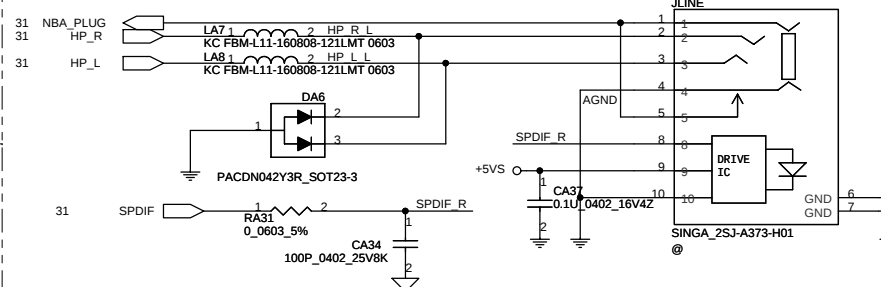
KEYBOARD CONN.



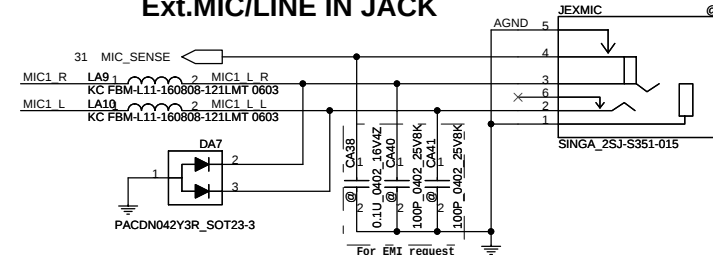
Keyboard LED



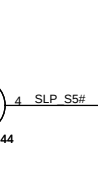
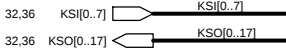
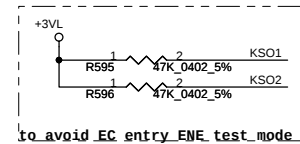
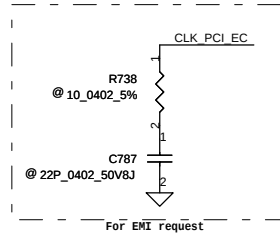
HeadPhone/LINE Out JACK



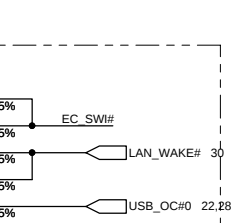
Ext.MIC/LINE IN JACK



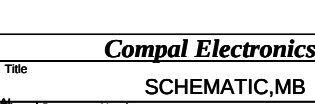
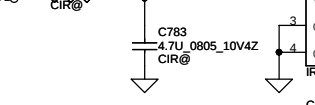
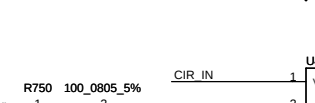
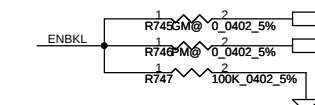
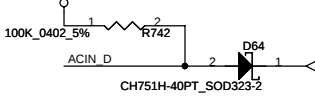
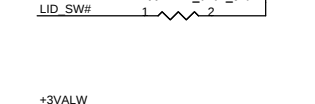
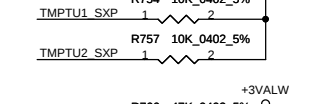
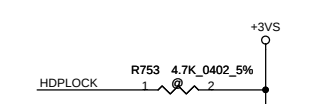
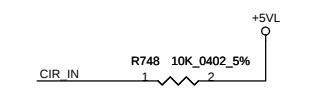
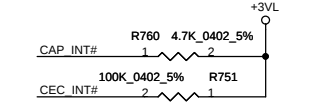
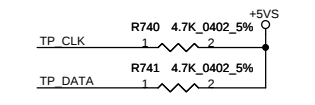
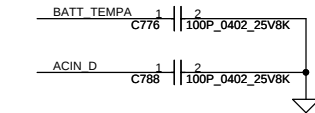
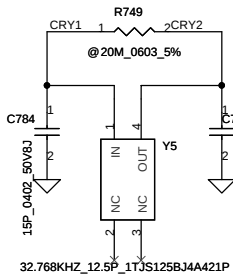
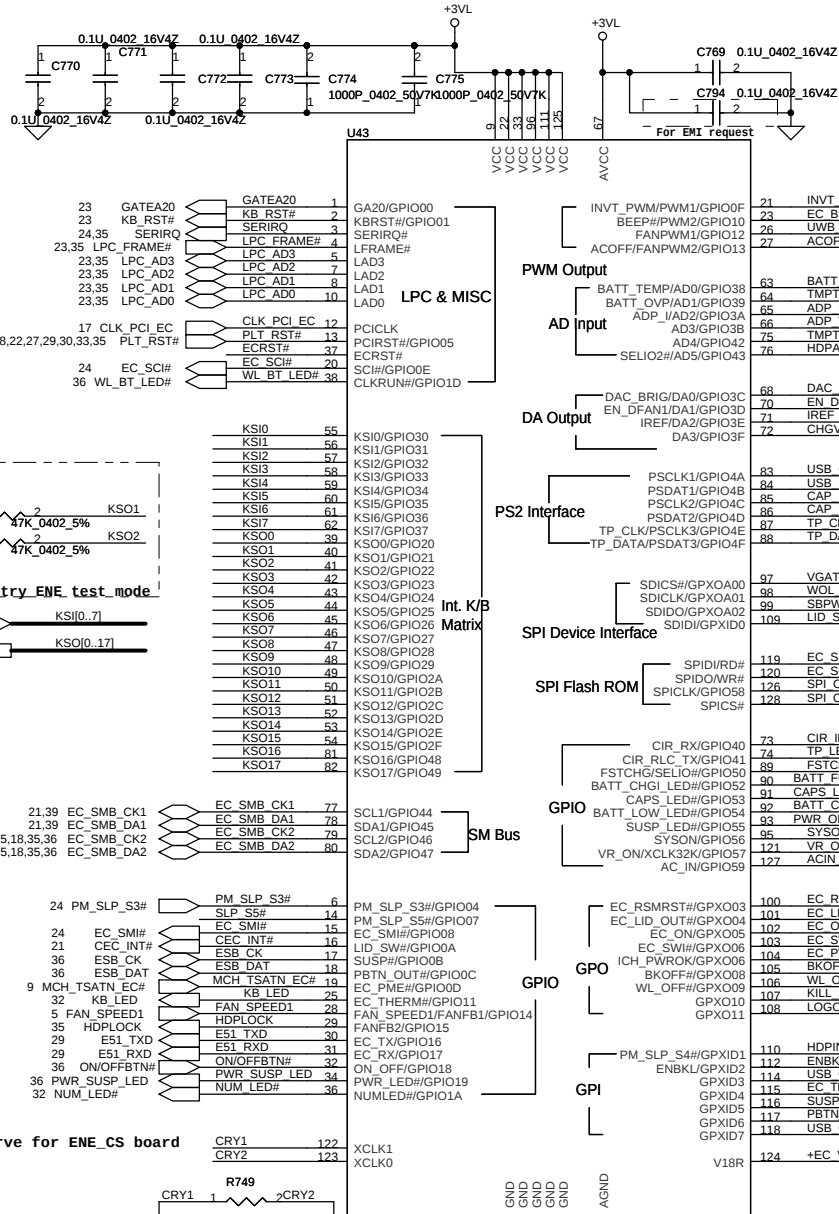
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					401781	
Date: Tuesday, August 18, 2009				Sheet	32	of 46



reserve for ENE_CS board

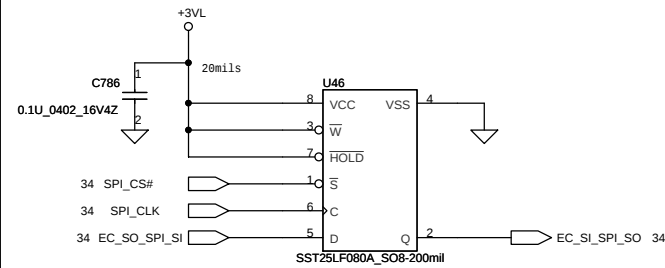


The circuit is reserve for new design for pre-MP

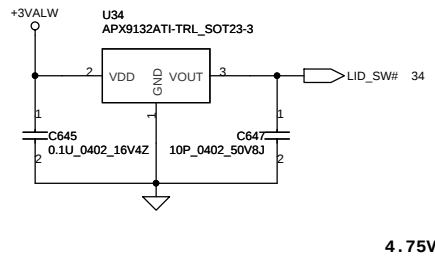


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				Date	Tuesday, August 18, 2009
				Sheet	34 of 46

SPI Flash (16Mb*1)



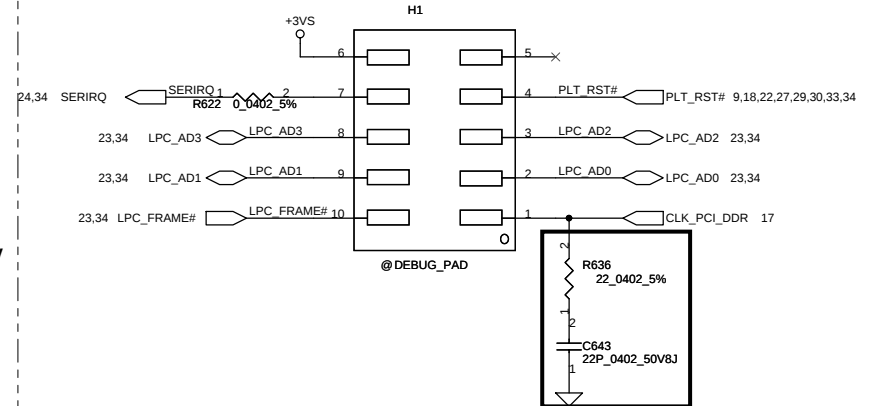
Lid SW



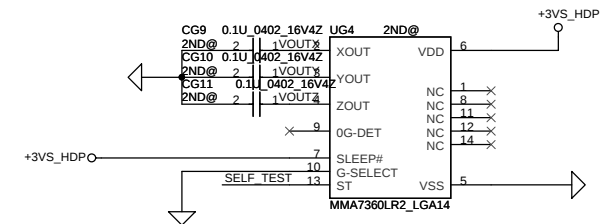
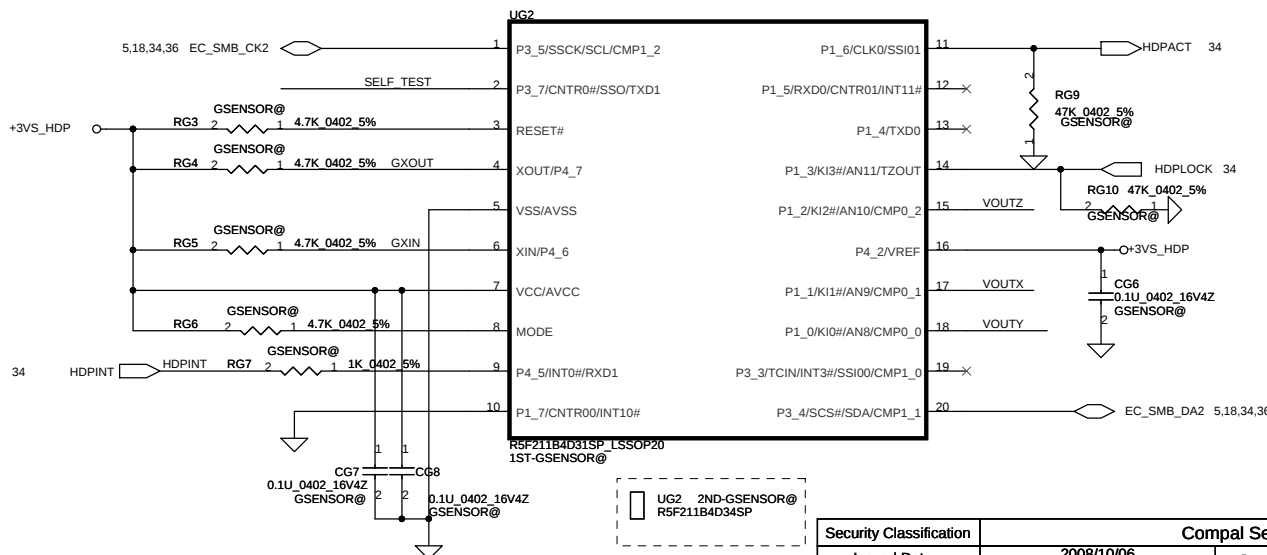
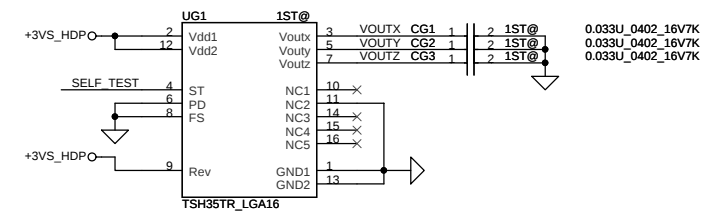
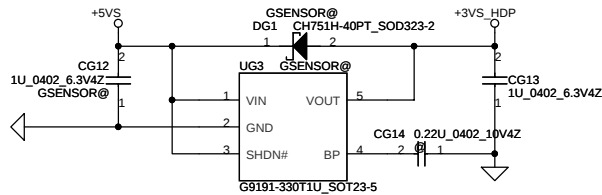
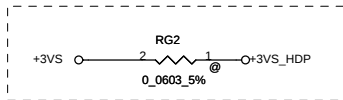
4.75V

LPC Debug Port

Please place the PAD under DDR DIMM.

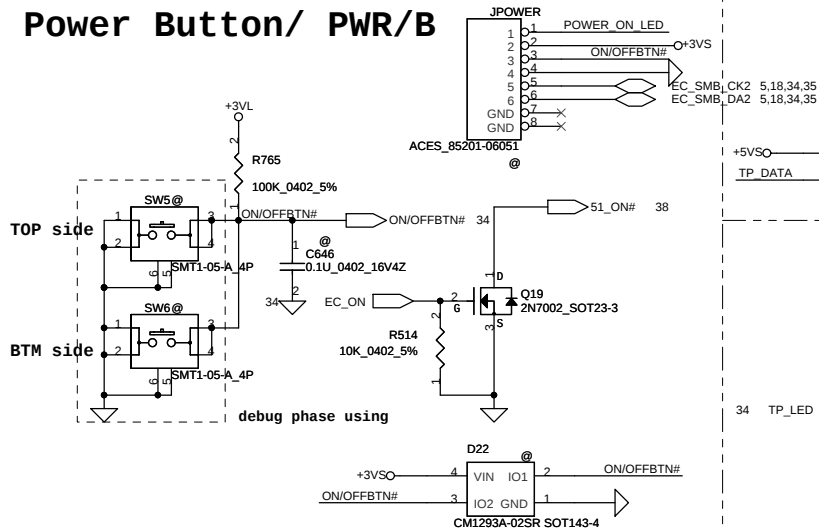


G-Sensor

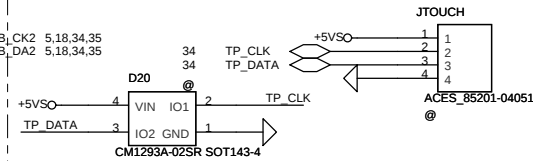


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					401781	A
				Date:	Tuesday, August 18, 2009	Sheet 35 of 46

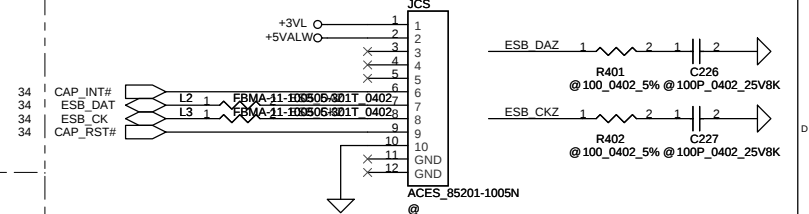
Power Button/ PWR/B



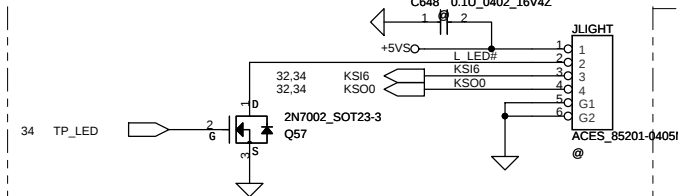
Touch/B Connector



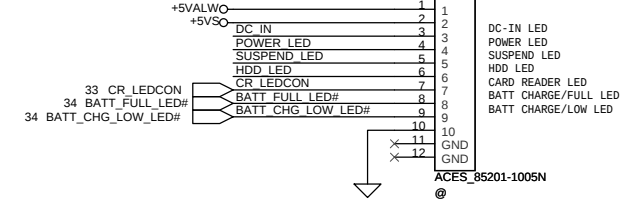
Caps Sensor Connector



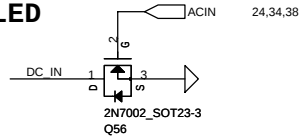
Light Pipe Connector



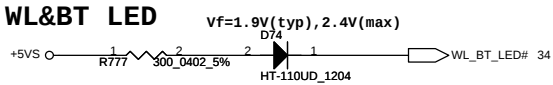
LED/B Connector



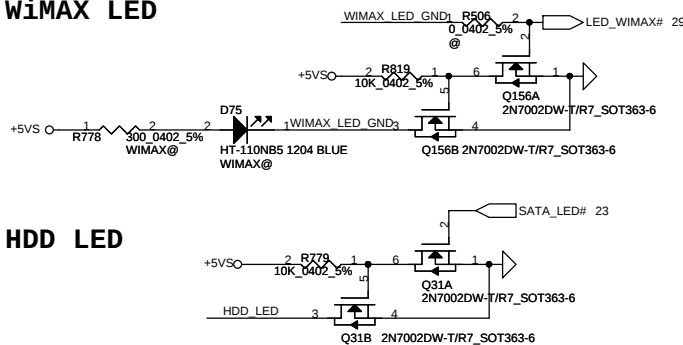
DC-IN LED



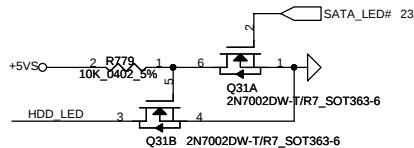
WL&BT LED



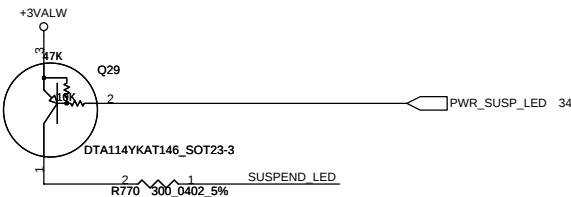
WiMAX LED



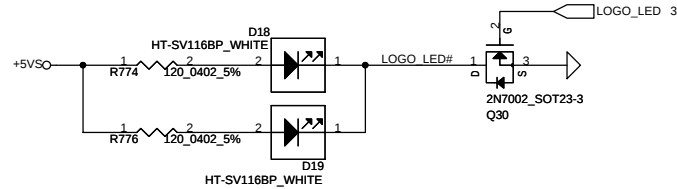
HDD LED



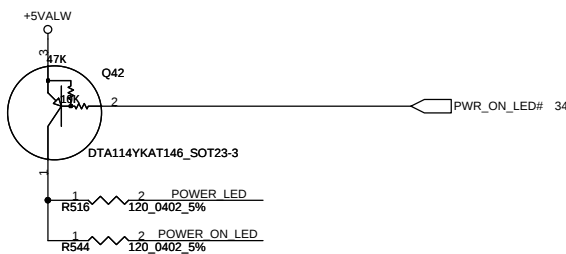
SUSPEND LED



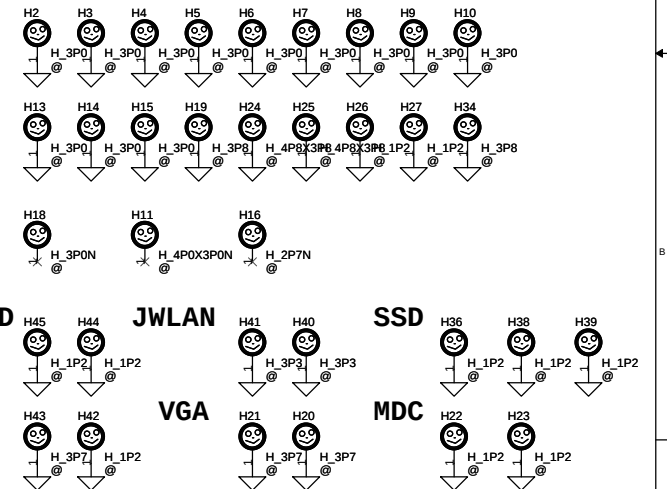
Satellite LED



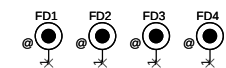
POWER LED



Screw Hole



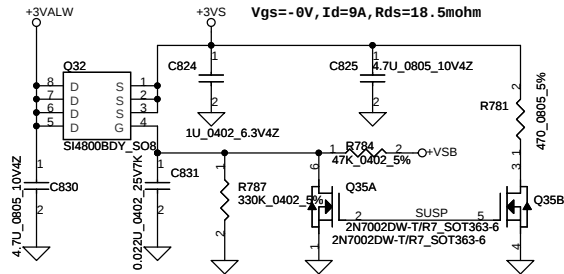
PCB Federal Mark PAD



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				Date	Tuesday, August 18, 2009
				Sheet	36 of 46

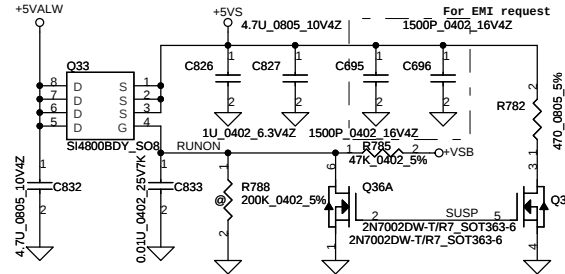
+3VALW TO +3VS

Inrush current = 0A
Vgs=-0V, Id=9A, Rds=18.5mohm



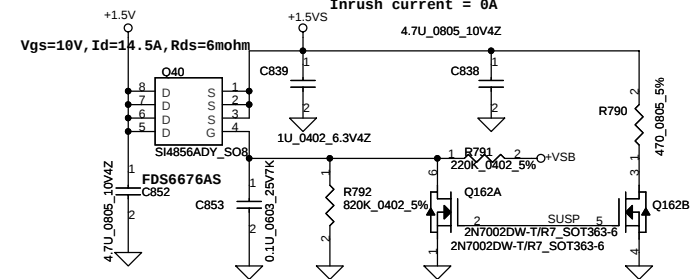
+5VALW TO +5VS

Inrush current = 0A



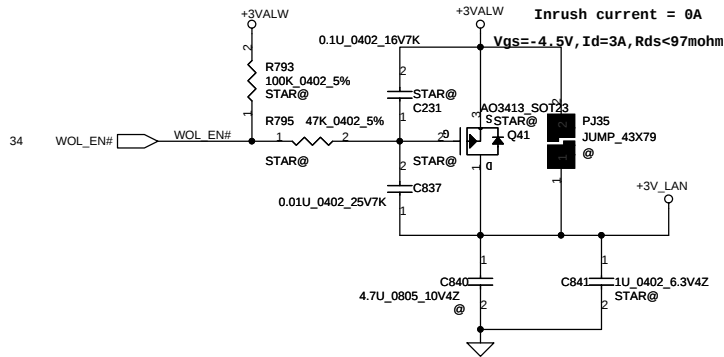
+1.5V to +1.5VS

Inrush current = 0A



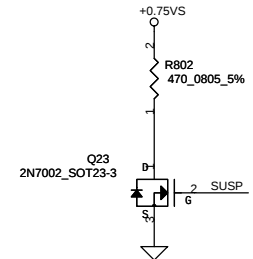
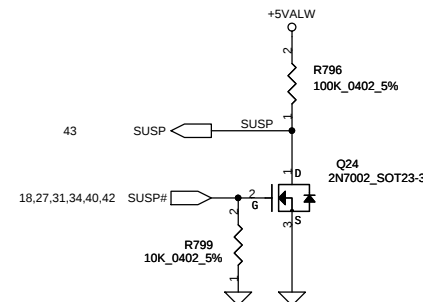
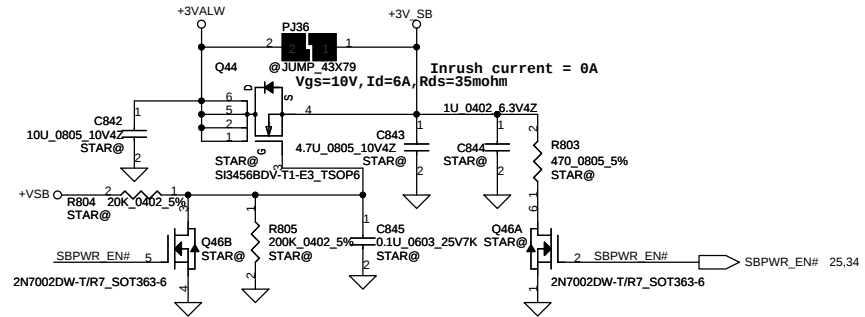
+3VALW TO +3V_LAN

Inrush current = 0A



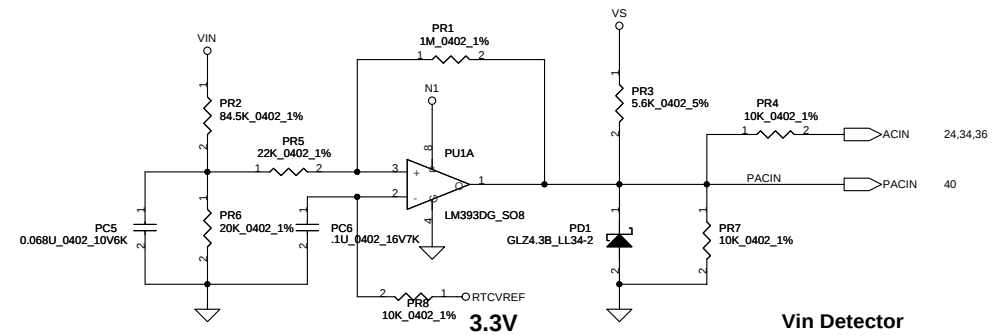
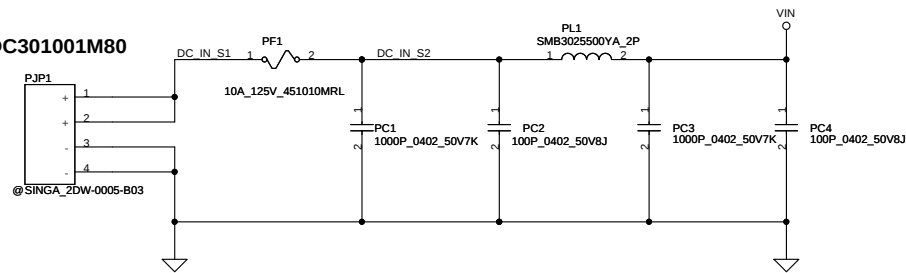
+3VALW TO +3V_SB

Inrush current = 0A



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				Date	Tuesday, August 18, 2009
				Sheet	37 of 46

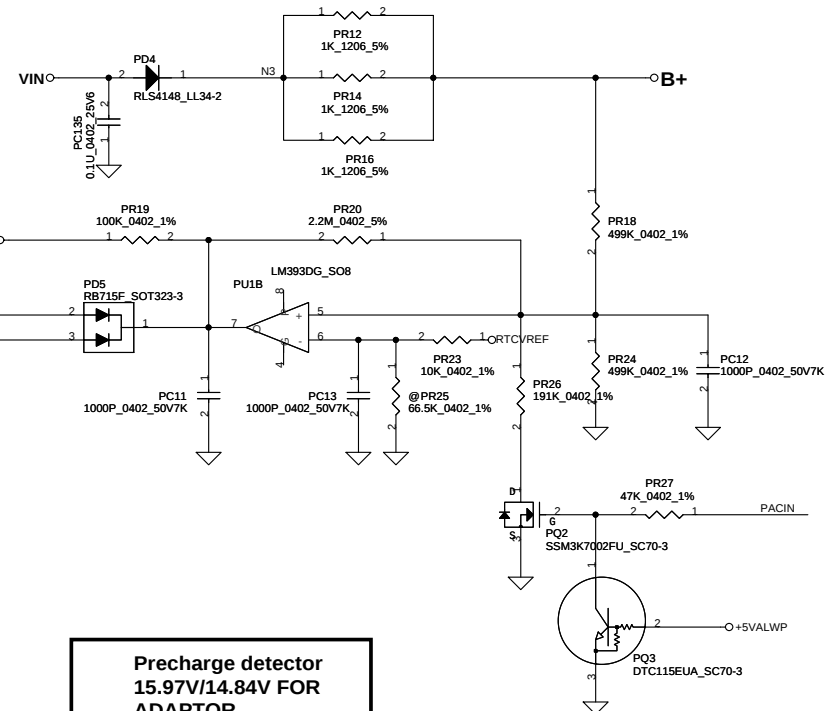
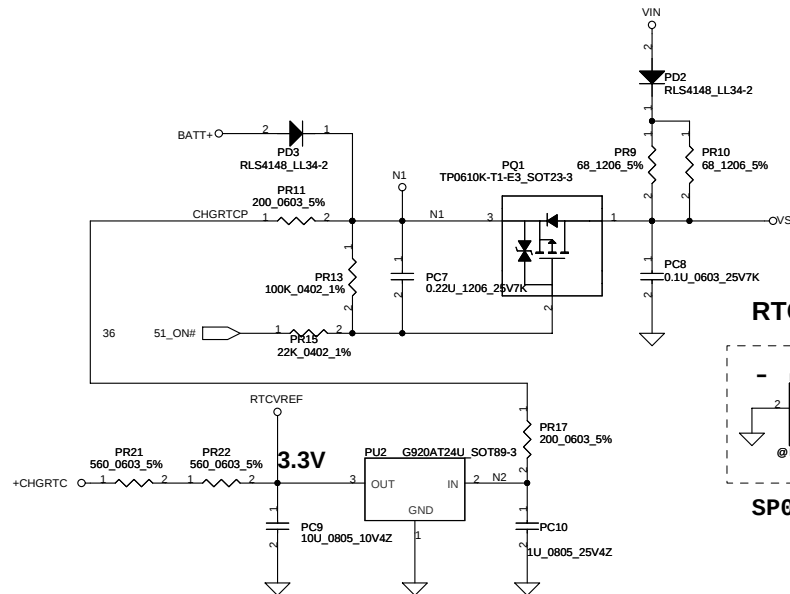
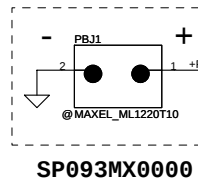
DC301001M80



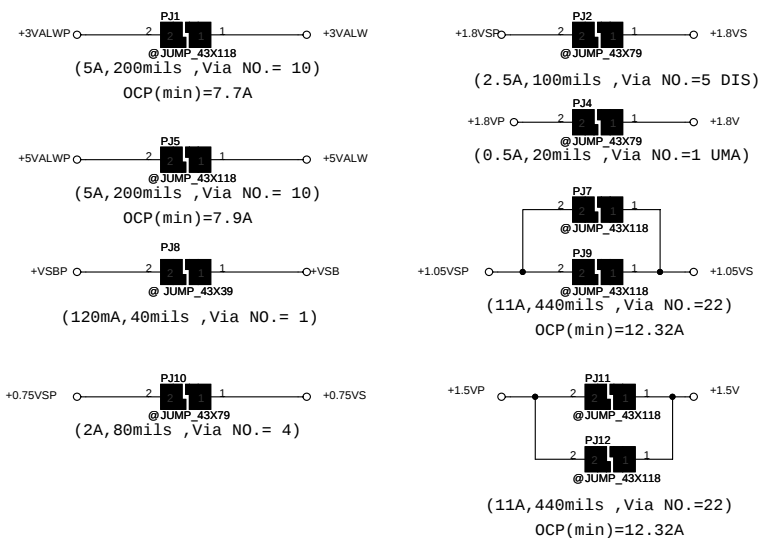
Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

RTC Battery

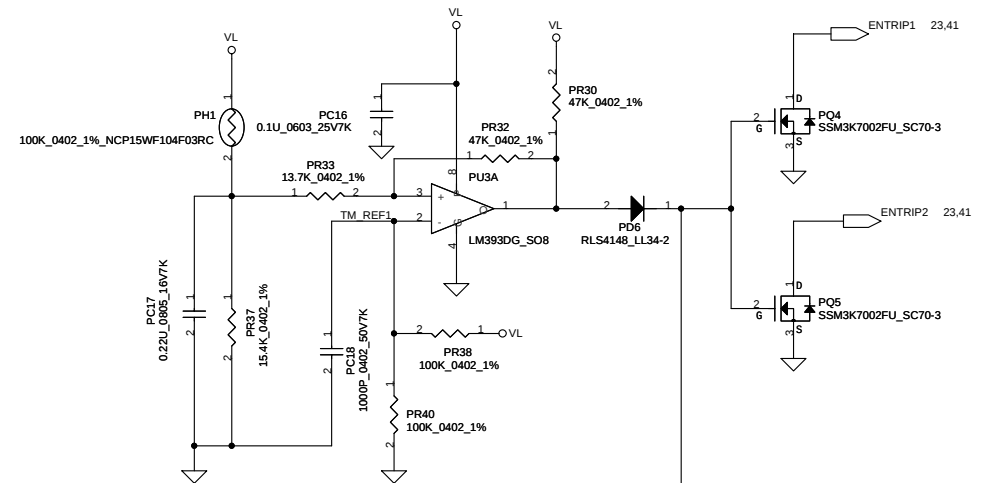


Precharge detector
15.97V/14.84V FOR
ADAPTOR

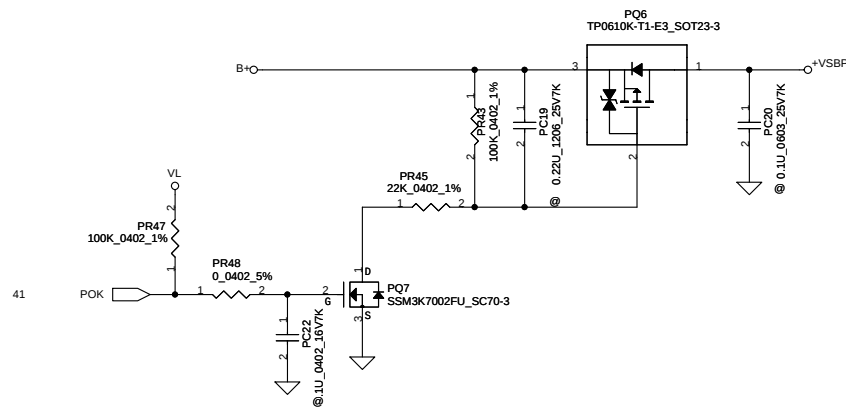
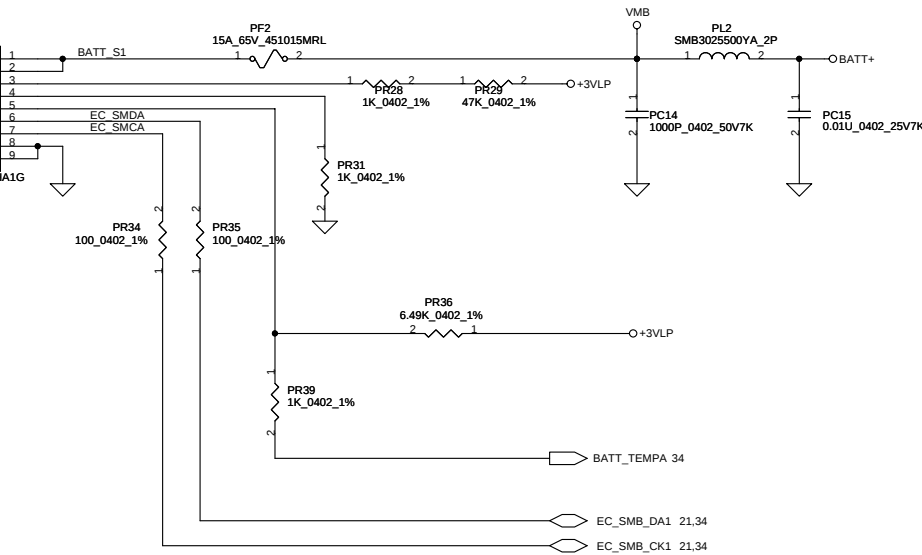
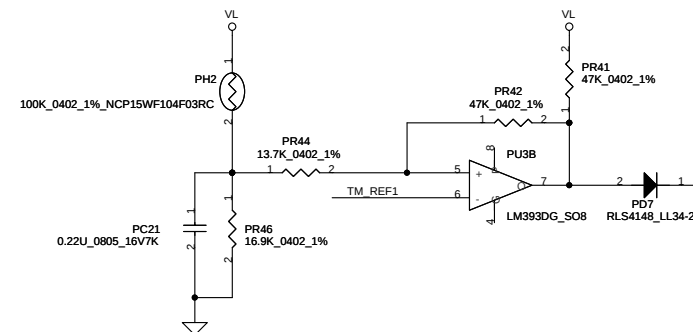


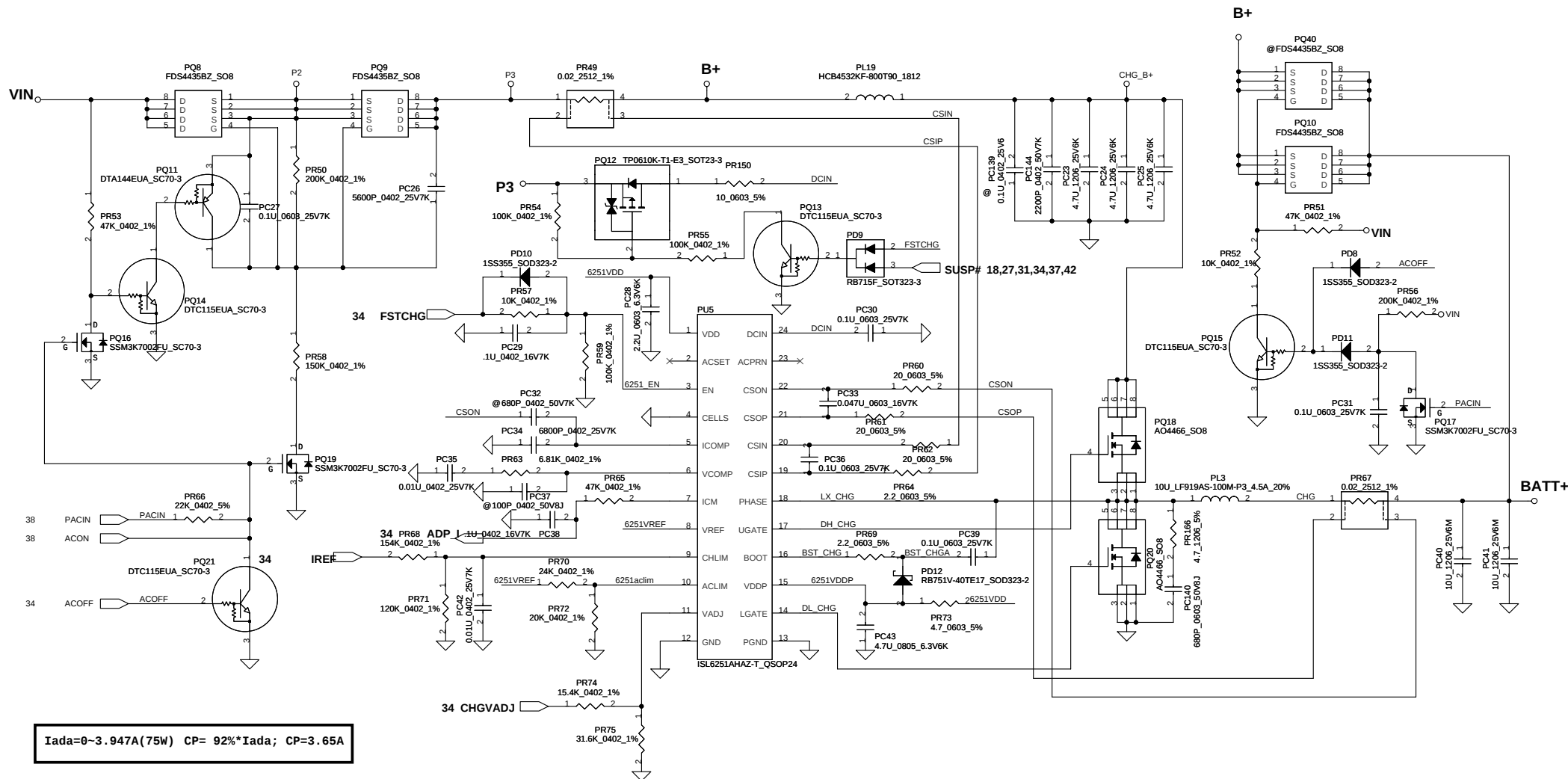
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Date: Tuesday, August 18, 2009				Document Number 401781
Sheet 38 of 46				Rev A

PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C





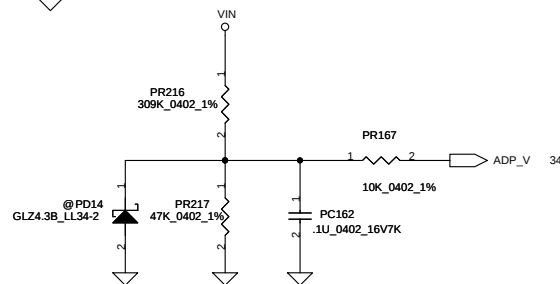
$$I_{ada}=0-3.947A(75W) \quad CP= 92\% \cdot I_{ada}; \quad CP=3.65A$$

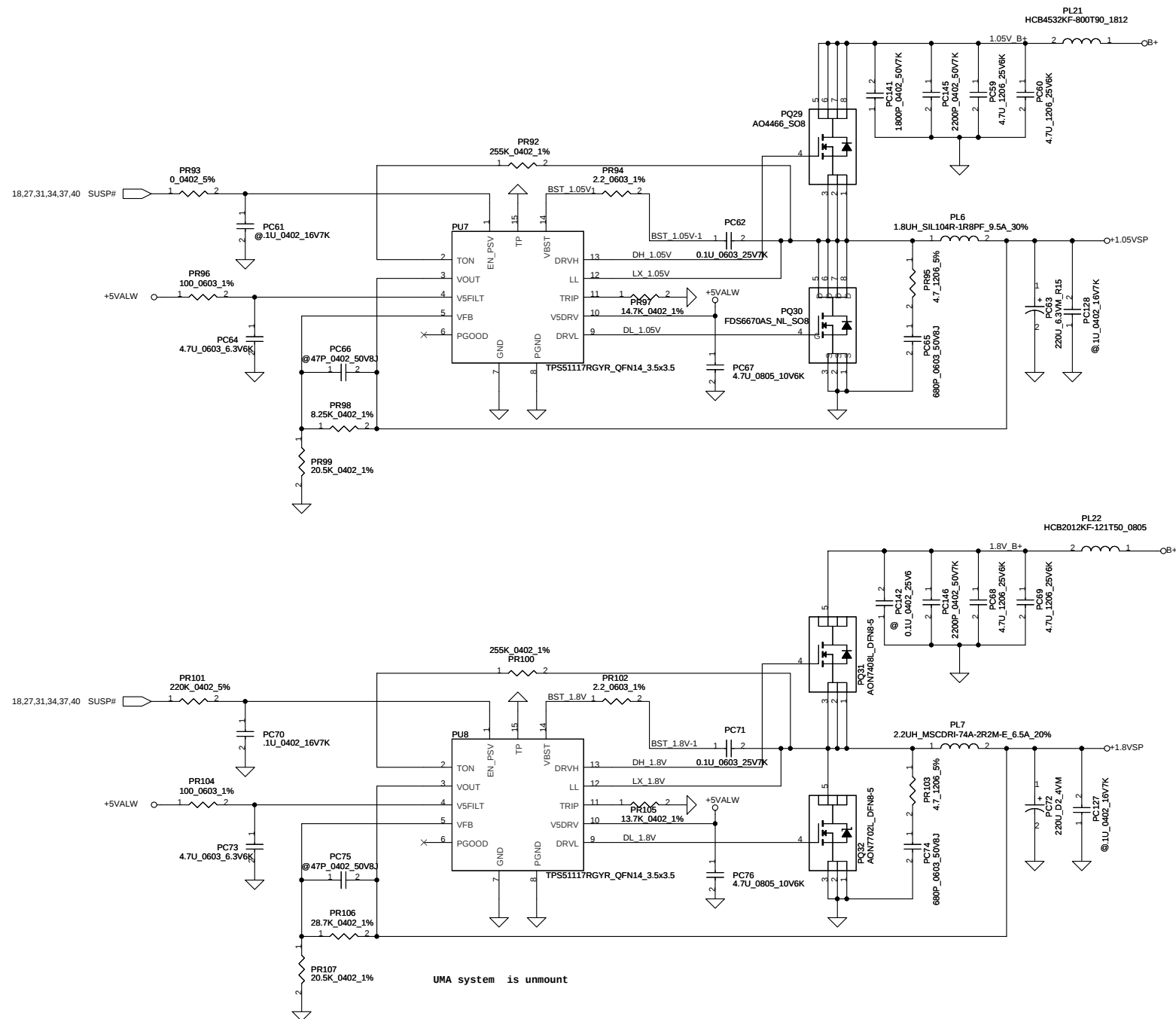
CP mode
 $V_{ac1m}=2.39 \cdot (20K//152K/(20K//152K+24K//152K))=1.09986V$
 $I_{input}=(1/0.02) \cdot ((0.05 \cdot V_{ac1m})/2.39+0.05)$
 where $V_{ac1m}=1.09986V$, $I_{input}=3.65A$

$CC=0.25A \sim 3A$
 $I_{REF}=1.016 \cdot I_{charge}$
 $I_{REF}=0.254V \sim 3.048V$
 V_{CHLIM} need over 95mV

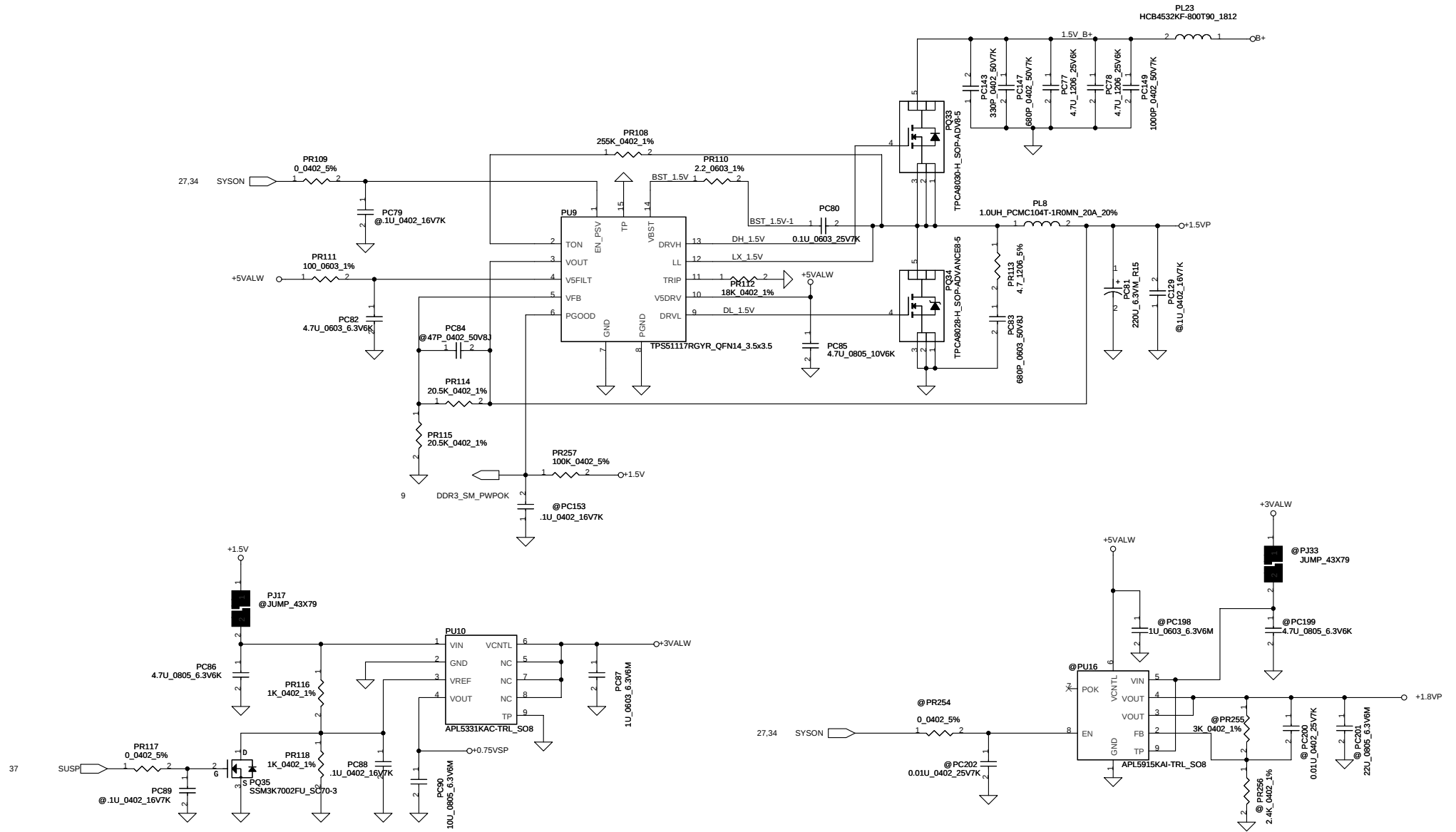
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

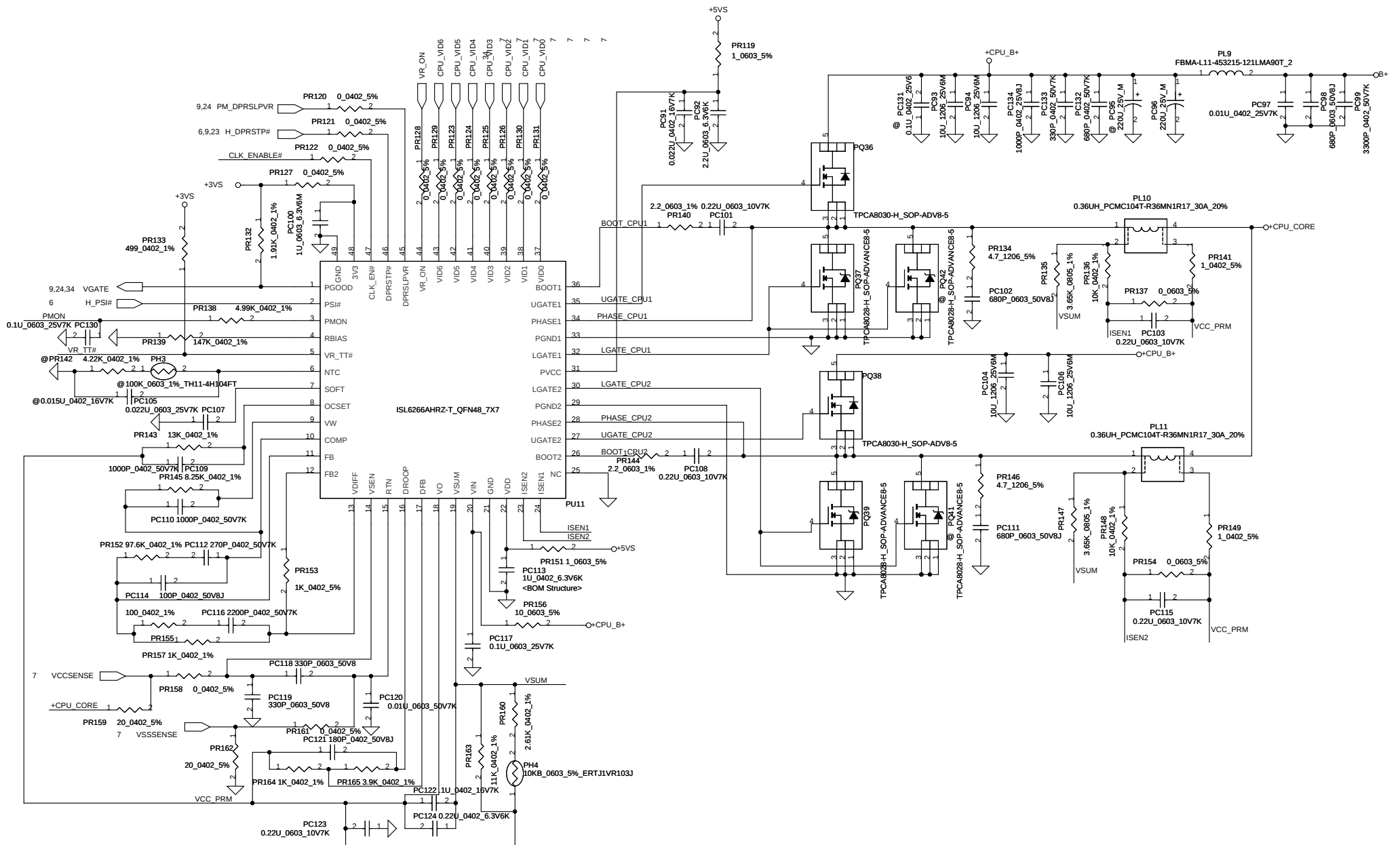




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				401781	A
Date: Tuesday, August 18, 2009		Sheet 42 of 46			



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				Document Number	401781
Date: Tuesday, August 18, 2009					Sheet 43 of 46



Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
38-44	DVT Release	2009/06/03			
42	Change PQ31,PQ32,PC72,PL7	2009/06/10	POWER		Change to small size
43	Change PC81	2009/06/10	POWER		Change to POSCAP

ISPD

Revision Change: LA-4991 1.0 to LA-4993 0.1

NB_PM_R3	 U3 CANTIGA PM PMR3@	PCB	 77Z PCB ZKU LA-4993P REV0
NB_PM_R1	 U3 CANTIGA PM PMR1@	DC-IN	 PJP1 45@
NB_G5_R3	 U3 CANTIGA GM45 G5R3@	Trans former	 UL3 10/100M transformer 8103EL@
NB_GL_R1	 U3 CANTIGA GL40 GMLR1@	LAN	 UL1 8103EL 8103EL@
NB_GL_R3	 U3 CANTIGA GL40 GMLR3@	SB_GL_R1	 U9 ICH9-M ES ICH9R1@
NB_GM7_R1	 U5 CANTIGA GM47 GMLR1@		
NB_GM_R3	 U6 CANTIGA GM47 @		
NB_GM9_R1	 U10 CANTIGA GM49 GMLR1@		
NB_GM9_R3	 U11 CANTIGA GM49 @		

Revision Change: LA-4993 0.1 to LA-4993 1.0

NB_GM_R3

U16

CANTIGA GM47

@

NB_GM9_R1

U10

CANTIGA GM49

GMLR1@

NB_GM9_R3

U11

CANTIGA GM49

@

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					401781	A
				Date:	Tuesday, August 18, 2009	Sheet 46 of 46