

Compal Confidential

Schematics Document

AUBURNDALE with Intel
IBEX PEAK-M core logic

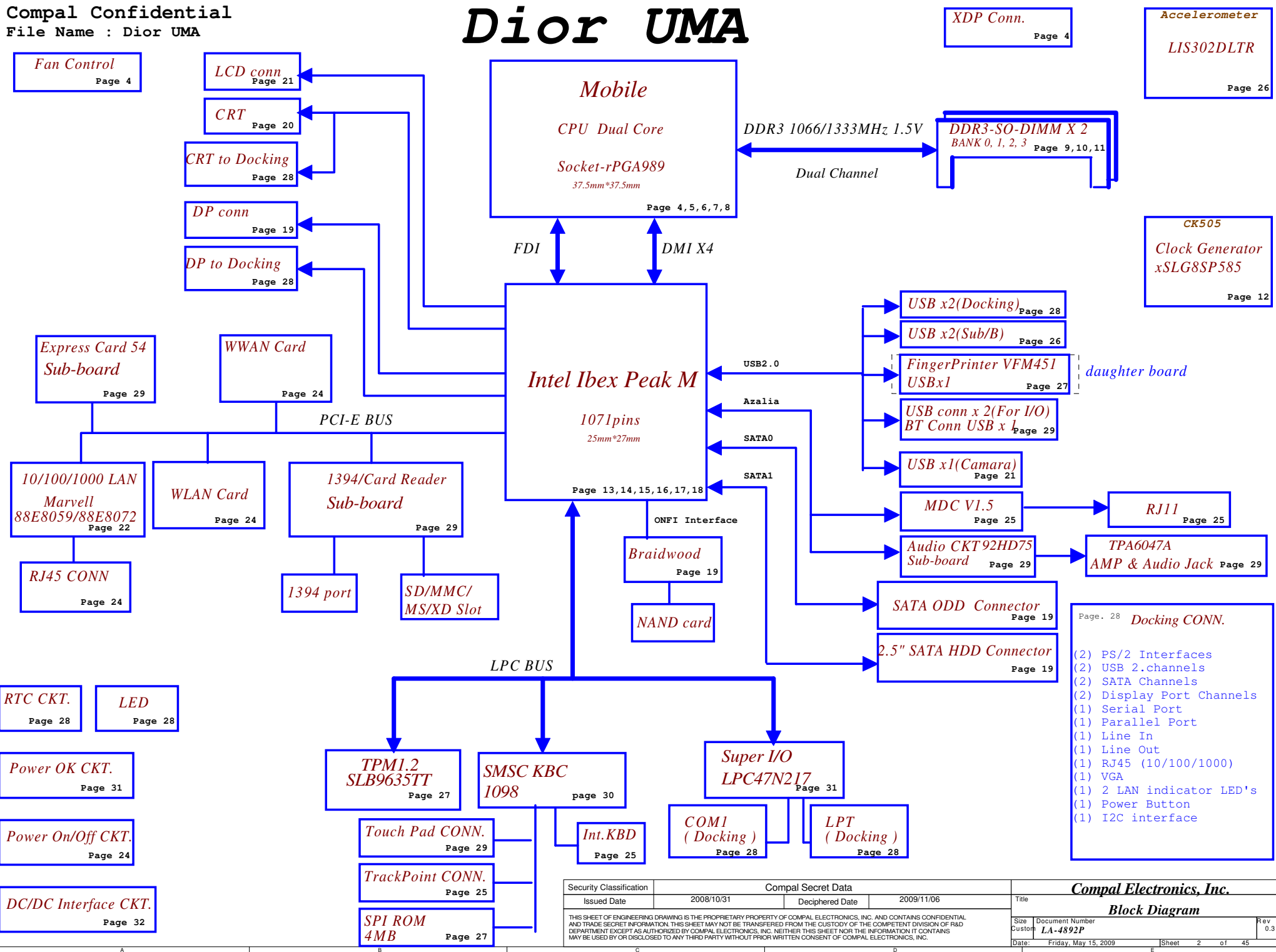
Dior UMA

2009-05-16

REV: 0.3

Security Classification	Compal Secret Data			Title		
Issued Date	2008/10/31	Deciphered Date	2009/11/06	Cover Sheet		
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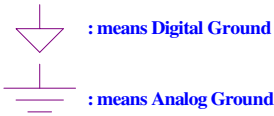


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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	+B +3VL	+5VALW +3VALW	+1.5V +0.75V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +1.05VS +1.8VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

Symbol Note :



Install below 43 level BOM structure for ver. 0.2

8072@ : Install for 8072 NIC controller

Install below 45 level BOM structure for ver. 0.2

45@ : means just put it in the BOM of 45 level.

Reserve below BOM structure for ver. 0.2

@ : means just reserve , no build

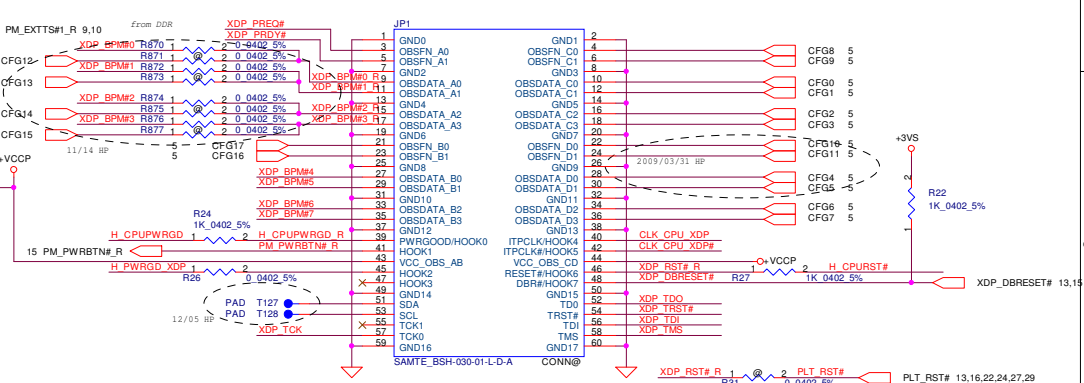
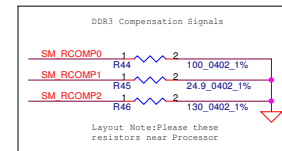
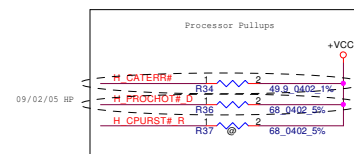
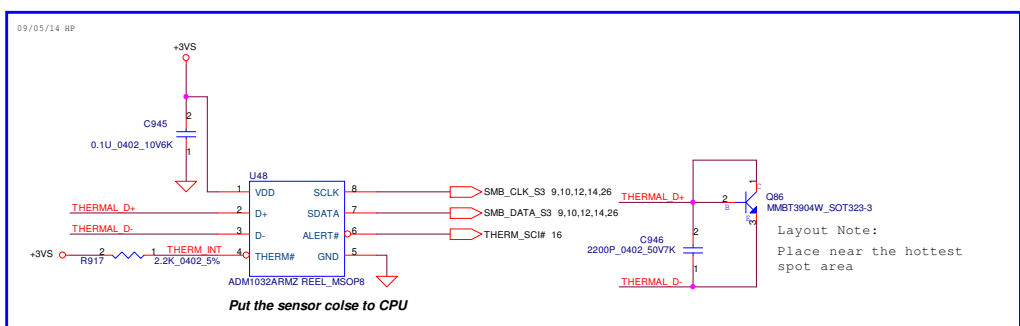
CONN@ : means ME part.

8059@ : Install for 8059 NIC controller

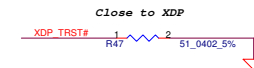
SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	CLK CHIP	MINI CARD	DOCK	NIC	THERMAL SENSOR	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	SMSC1098	V	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	Calpella	X	V	V	V	V	V	V	X	V
SML0CLK SML0DATA	Calpella	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	X	X	V	X

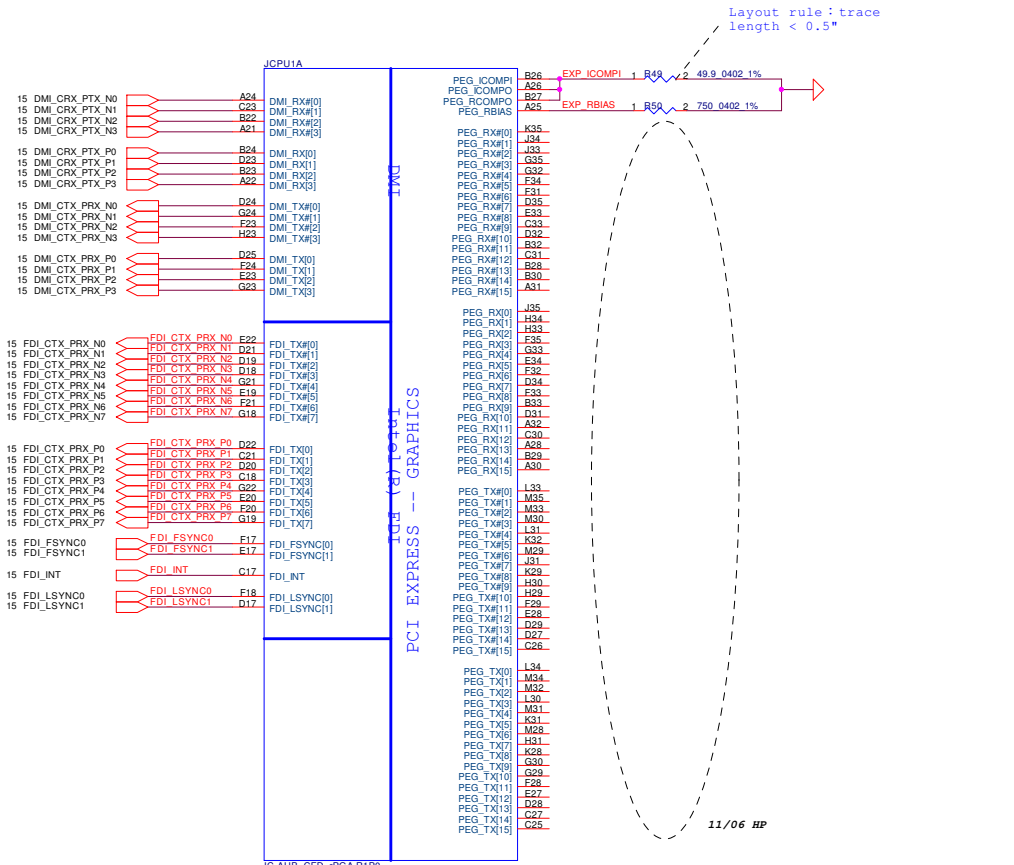
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[illegible][illegible]

11/12 remove the mapping option



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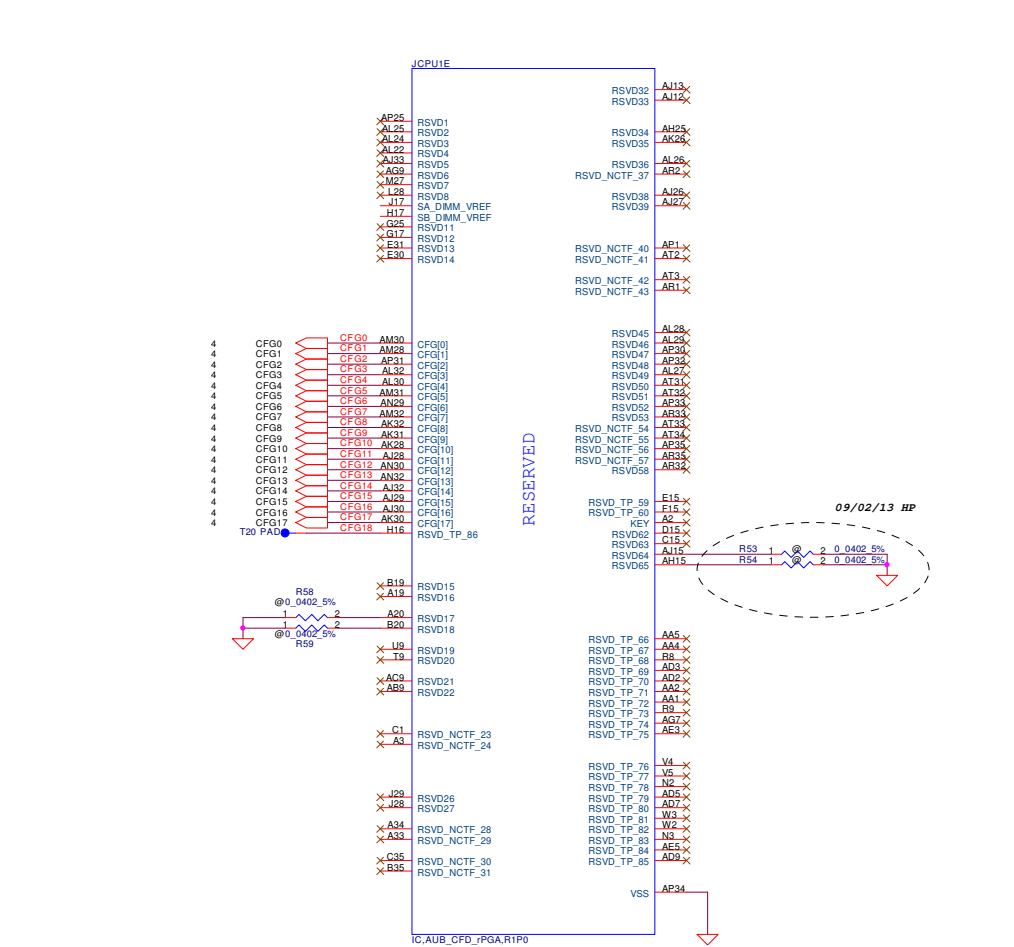
CFG Straps for PROCESSOR

CFG0
R60 @ 5.01K_0402_1%
PCI-Express Configuration Select
CFG0 1: Single FBG
0: Bifurcation enabled
Not applicable for Clocksfield Processor

CFG3
R62 @ 5.01K_0402_1%
CFG01-PCI Express Static Lane Reversal
CFG3 1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 3,

CFG4
R63 @ 5.01K_0402_1%
CFG04-Display Port Presence
CFG4 1: Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7
R61 @ 5.01K_0402_1%
Only temporary for early CPD samples (rPGA/BGA)
No needed by MoW41.



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+CPU CORE

JCPU1F

48A

18A

+VCCP

VTTO_1

VTTO_2

VTTO_3

VTTO_4

VTTO_5

VTTO_6

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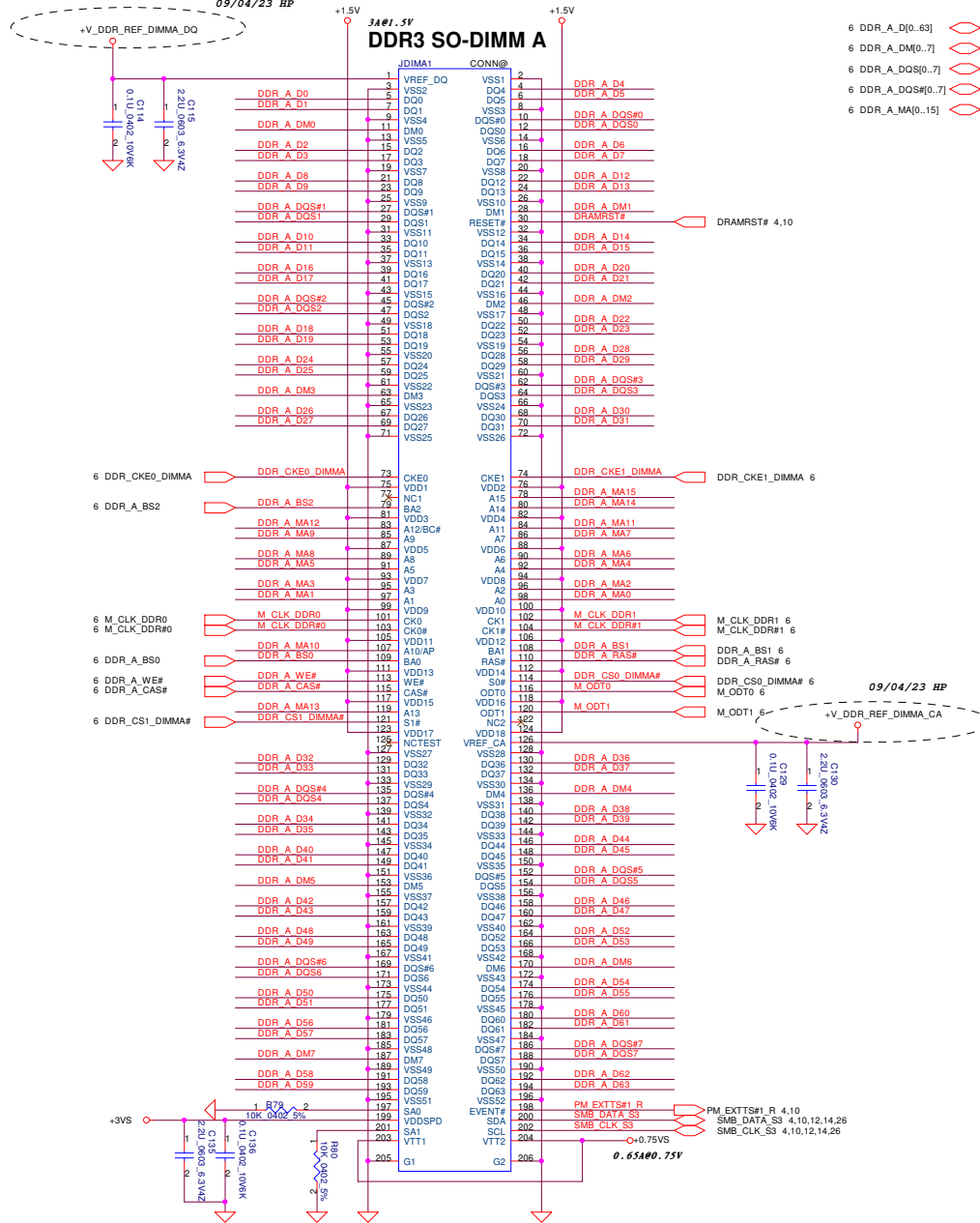
VTTO_319

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DDR3 SO-DIMM A

TOP SLOT



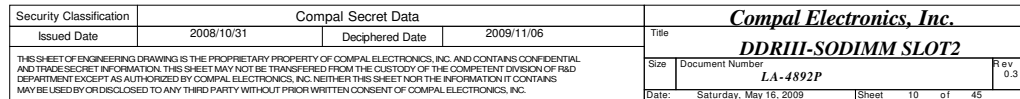
- 6 DDR_A_D[0..63]
- 6 DDR_A_DM[0..7]
- 6 DDR_A_DQS[0..7]
- 6 DDR_A_DQS[0..7]
- 6 DDR_A_MA[0..15]

Layout Note:
Place near DIMM

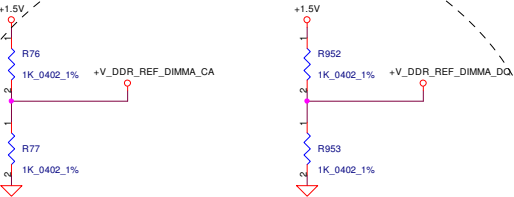
Layout Note:
Place near DIMM

Layout Note:
Shared between the two
SO-DIMMs.
Place two capacitors close
to the VR and one
between the two SODIMMs

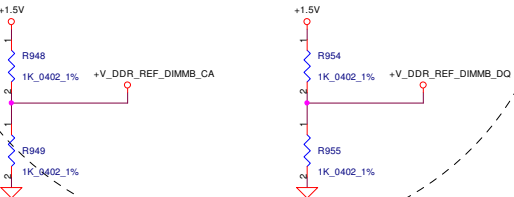
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09/04/03 Auburndale/Arrandale only supports M1 change Vref to +V_DDR_CPU_REF



09/04/23 HP



11/20 Auburndale does not require to support M2 for VrefDQ, HP

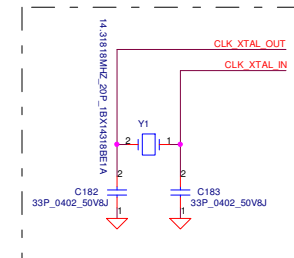
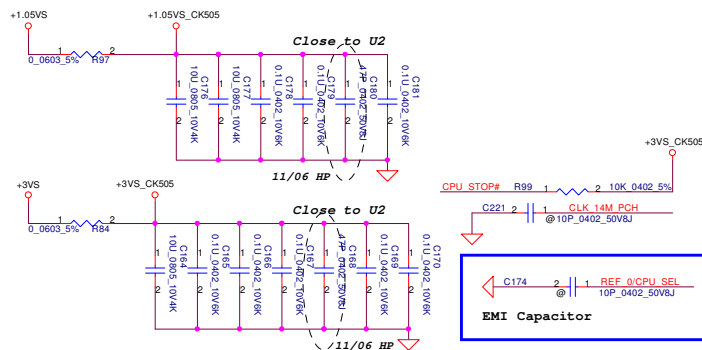
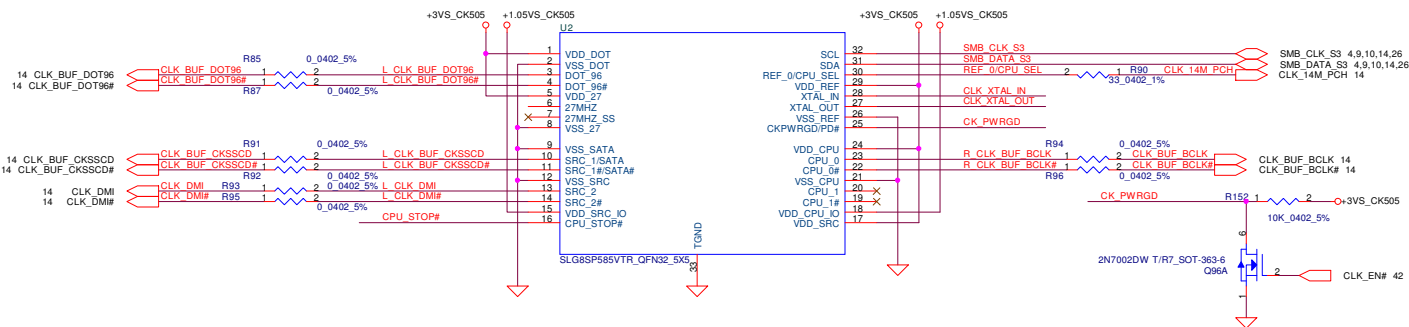
11/20 HP

09/03/31 Auburndale/Arrandale only supports M1, HP

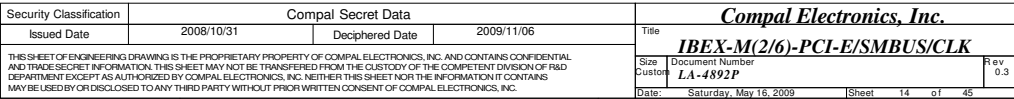
11/20 HP

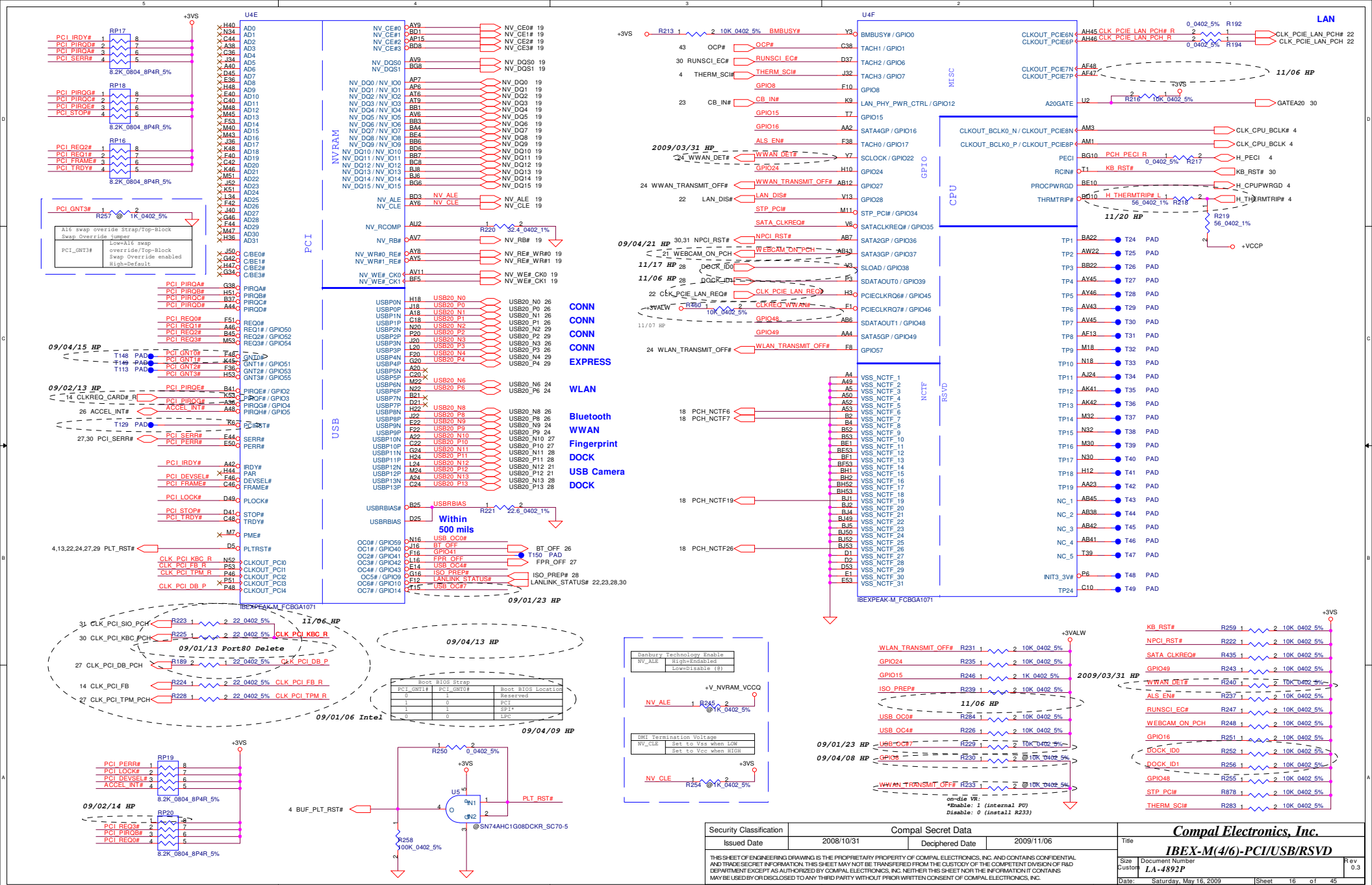
09/03/31 Auburndale/Arrandale only supports M1, HP

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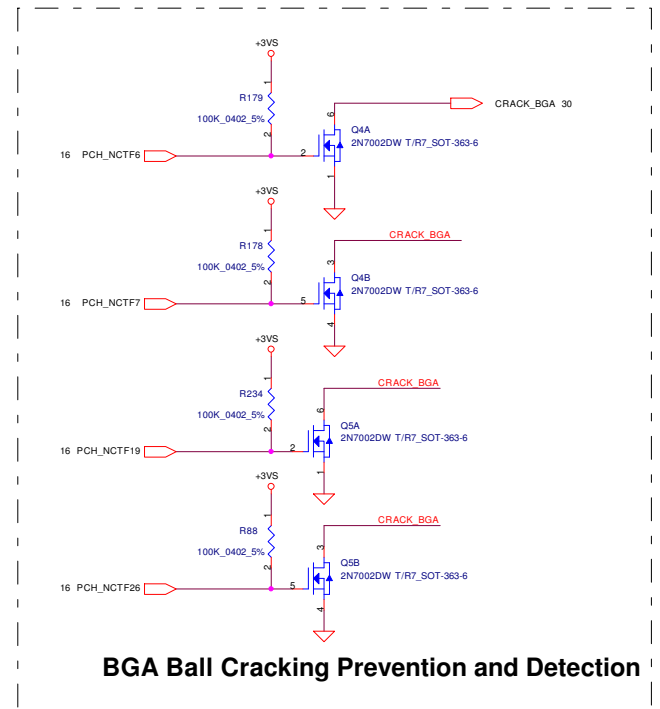
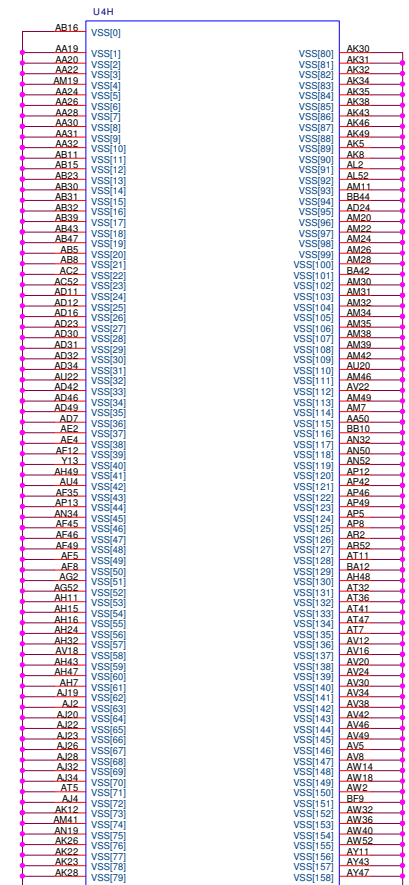
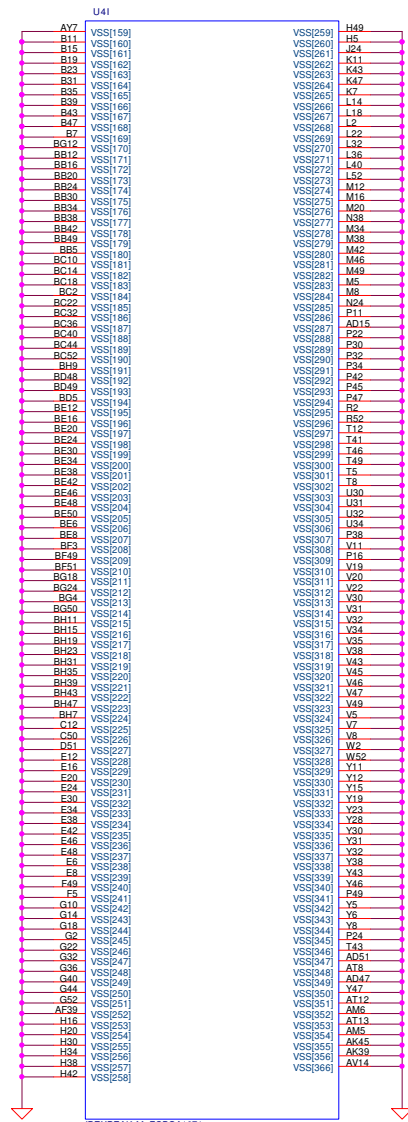


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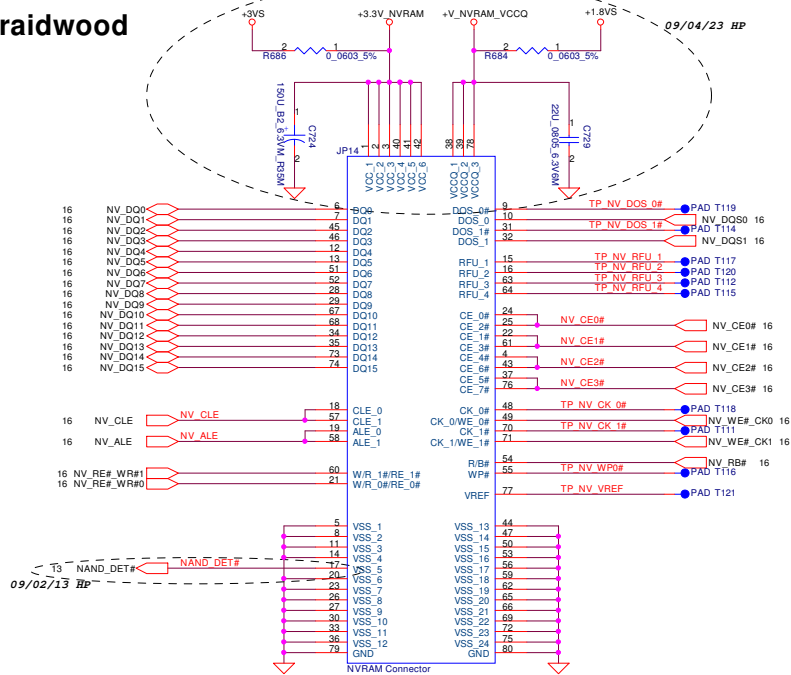


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Title	Compal Electronics, Inc. IBEX-M(4/6)-PCI/USB/RSVD		
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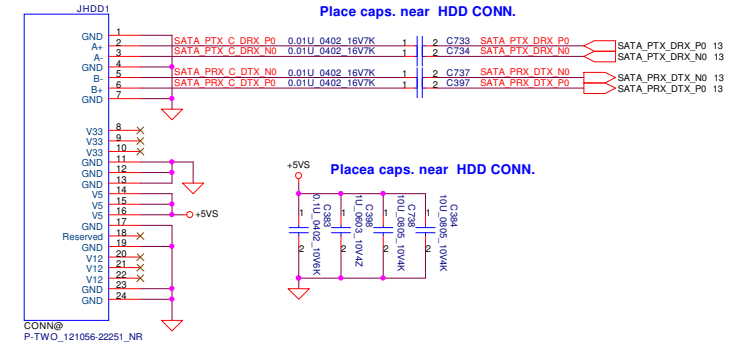


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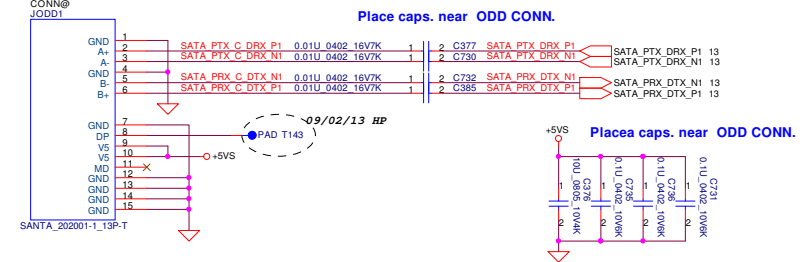
Braidwood



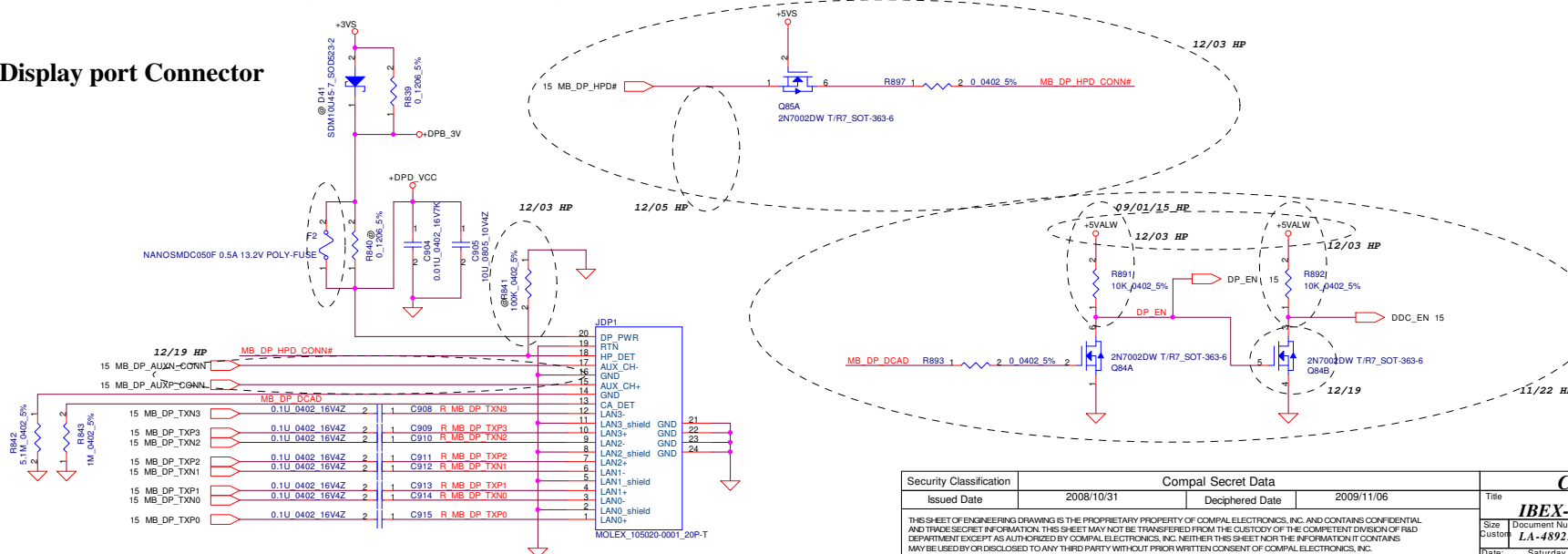
SATA HDD CONN.



SATA ODD CONN.

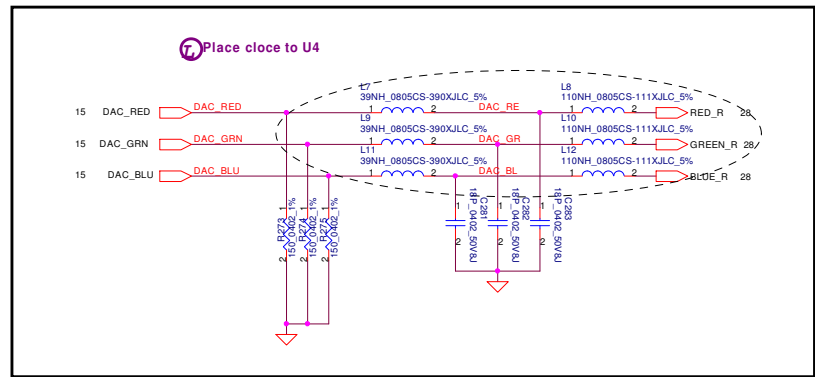
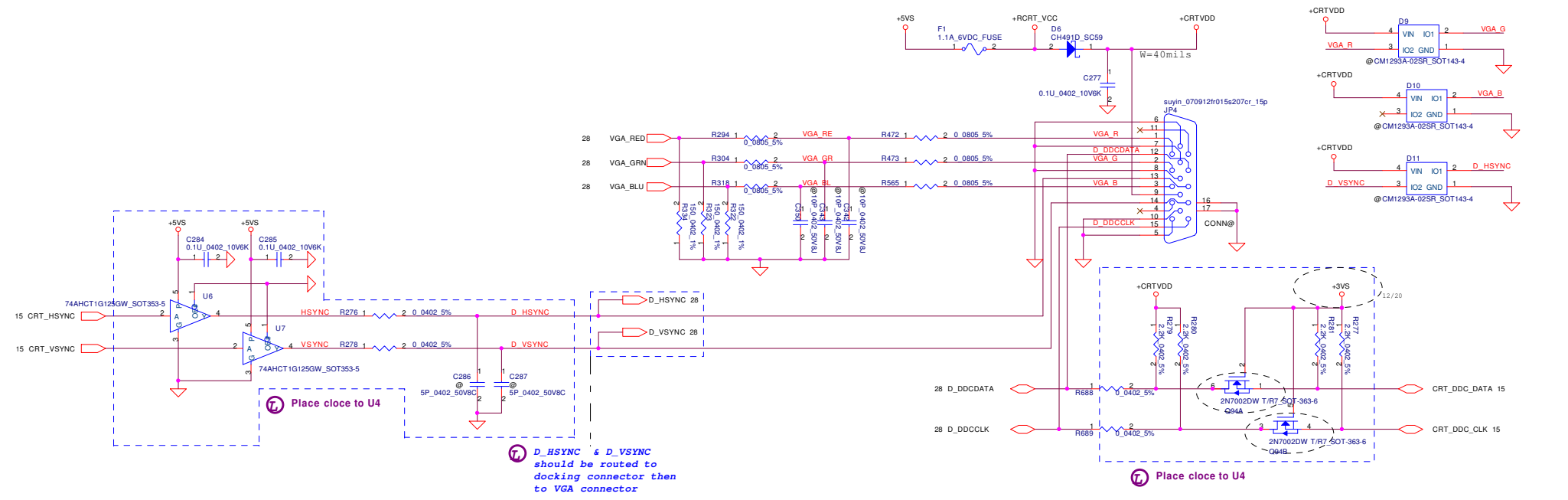


Display port Connector



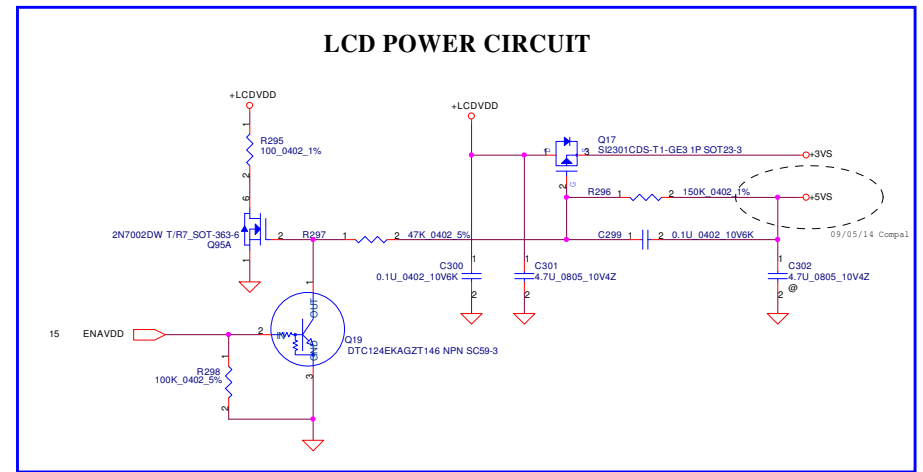
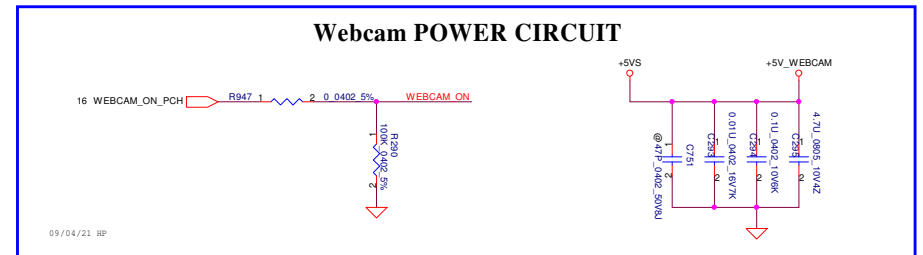
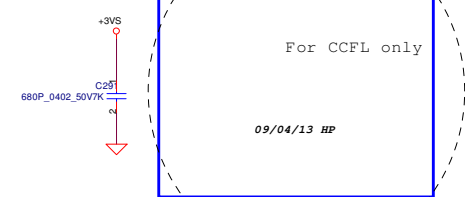
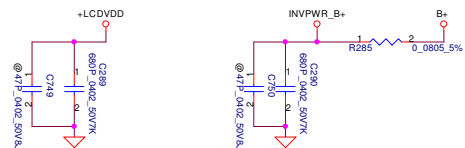
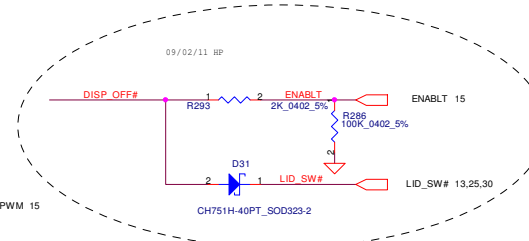
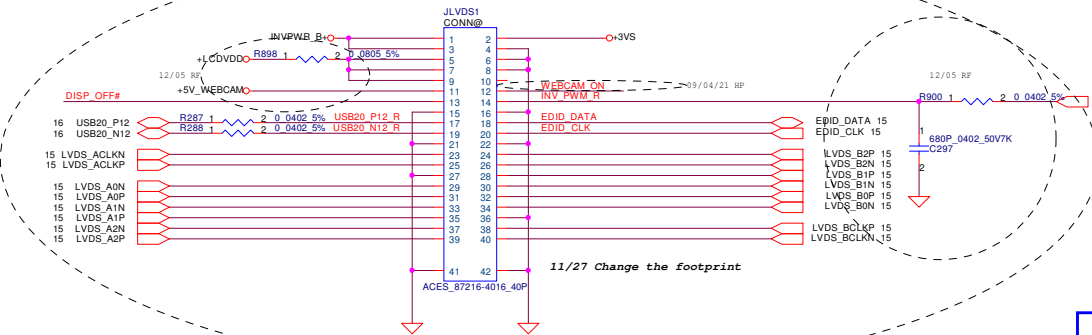
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CRT Connector



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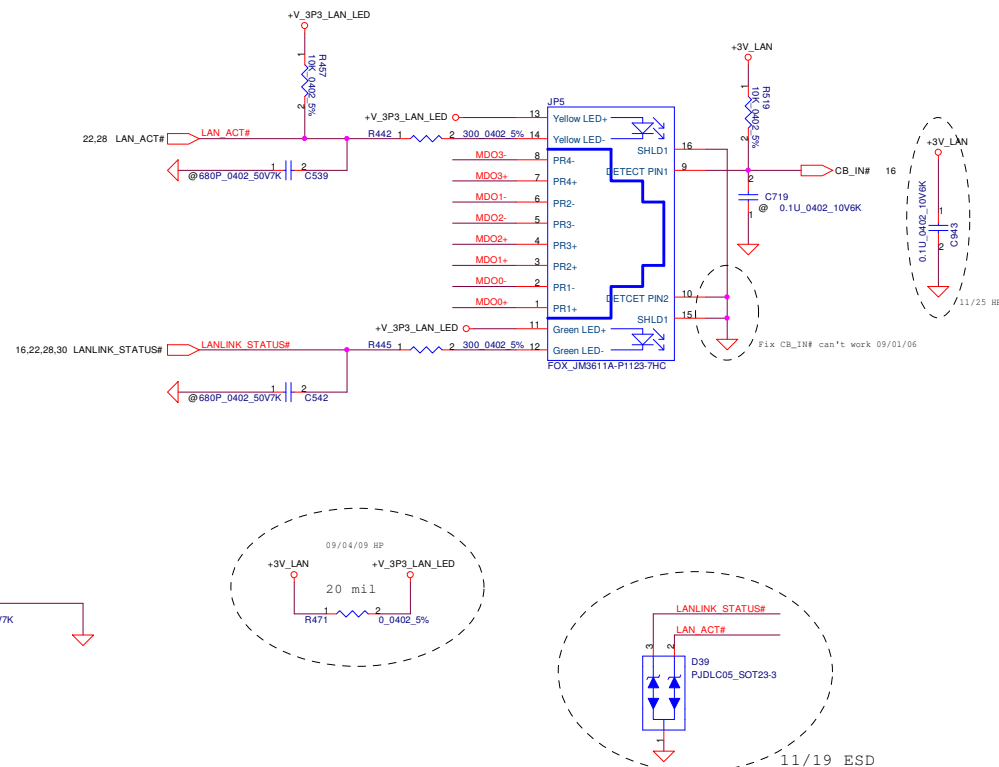
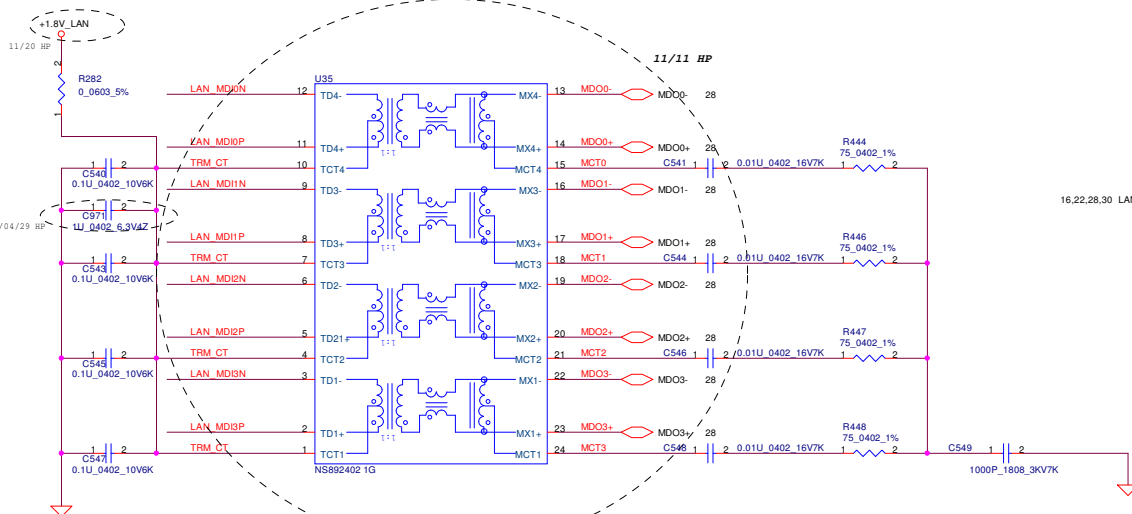
LCD/PANEL BD. CONN.



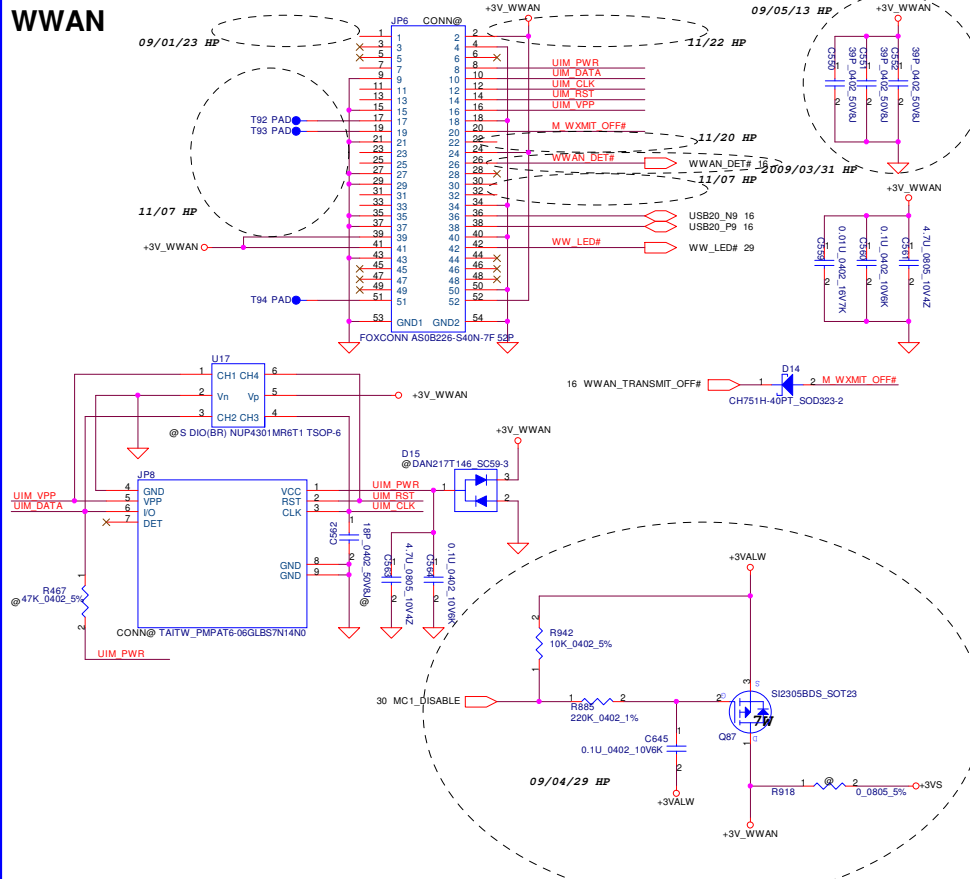
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Compal Electronics, Inc.
LCD CONN & O-Switch & GPIO Ext.

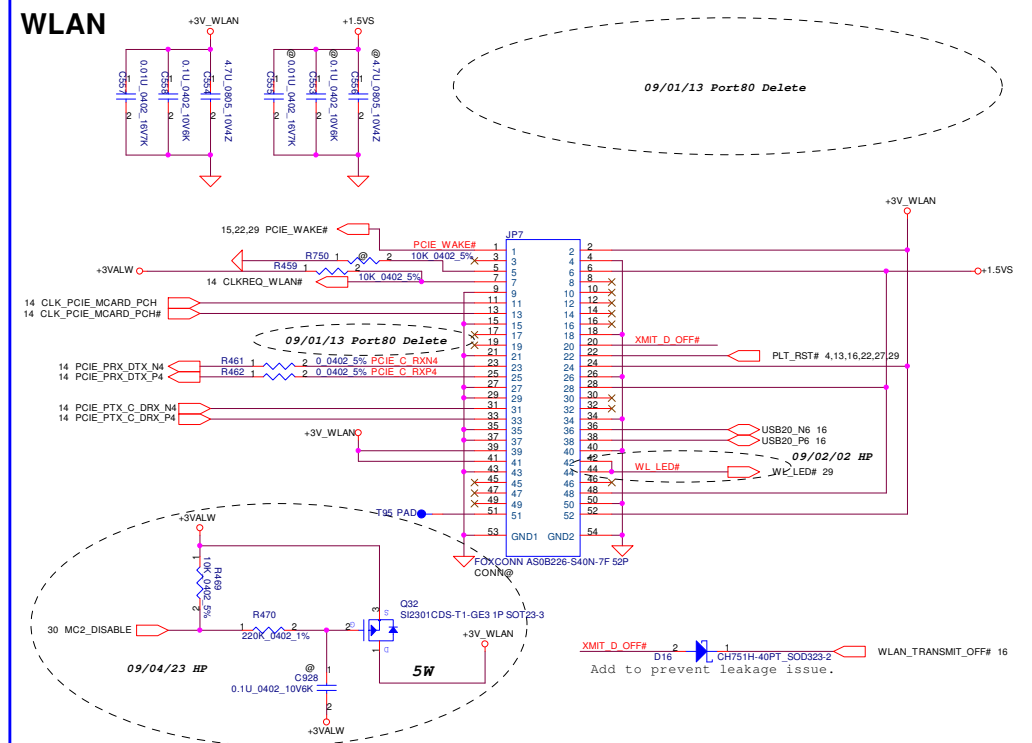
22 LAN_MD10P LAN_MD10P
22 LAN_MD10N LAN_MD10N
22 LAN_MD11P LAN_MD11P
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22 LAN_MD12N LAN_MD12N
22 LAN_MD13P LAN_MD13P
22 LAN_MD13N LAN_MD13N



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WWAN

WLAN



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[illegible]

MDC 1.5 Conn.

13 HDA_SDOUT_MDC

13 HDA_SYNC_MDC

13 HDA_SDINT1_MDC

13 HDA_RST#_MDC

HDA_SDOUT_MDC

HDA_SYNC_MDC

HDA_SDINT1_MDC

R482 1 2 0.0402 5%

R908 1 2 0.0402 5%

09/01/15 HP

JP13 CONN@ ACES 88021-12011 12P

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

HDA_BIT_CLK_MDC 13

R483 2 0.0402 5%

C586 1 2 @10P_0402_50V6J

+3VS

12/01 For HDA

+3VS

12/01 For HDA

C585 1 2 1000P_0402_50V7K

C585 1 2 0.1U_0402_10V6K

47U 0805_10V4Z @

The schematic diagram illustrates the ON/OFF control circuit for the CH7511H-40PT LED driver. The circuit is powered by a +3VL input. A 47.0402 5% resistor (R486) is connected between the +3VL input and the ON/OFFBTN_KBC# 30 pin of the CH7511H-40PT. A 100K 0402 5% resistor (R484) is connected between the +3VL input and the ON/OFFBTN# 15 pin of the SOD323-2 package. A 10.0603 10V4Z capacitor (C591) is connected between the ON/OFFBTN_KBC# 30 pin and ground. A 47.0402 5% resistor (R487) is connected between the ON/OFFBTN# 15 pin and the ON/OFFBTN_KBC# 30 pin. The output of the CH7511H-40PT is connected to the ON/OFFBTN# 15 pin of the SOD323-2 package. The circuit is powered by +3VALW.

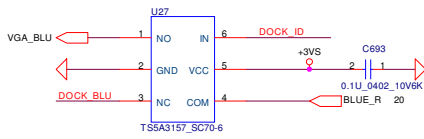
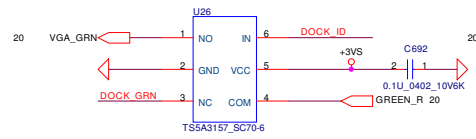
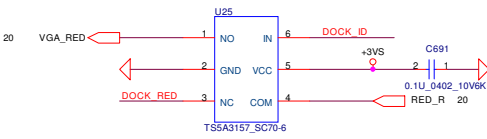
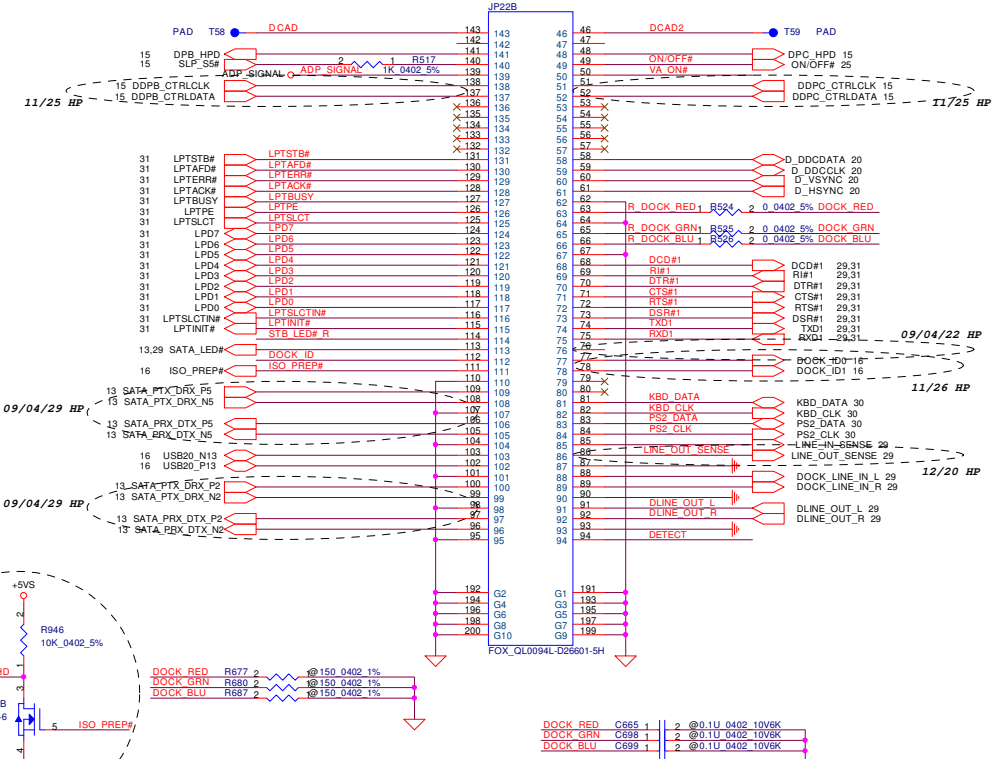
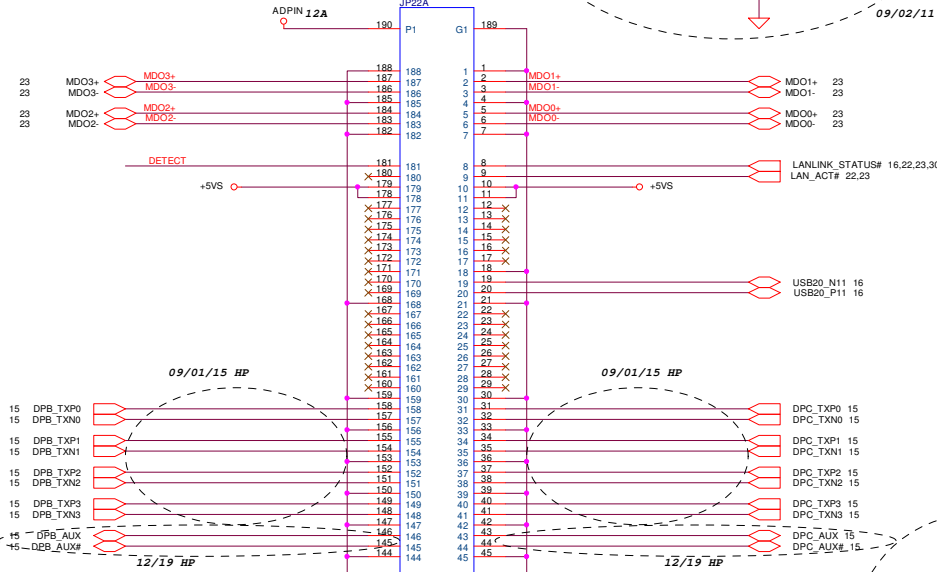
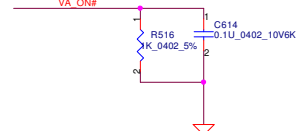
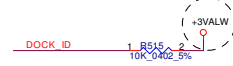
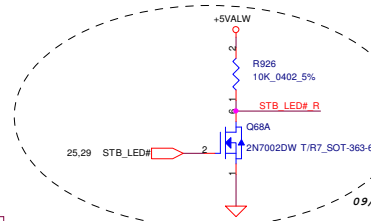
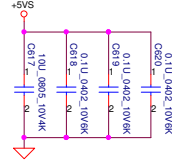
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TrackPoint CONN.

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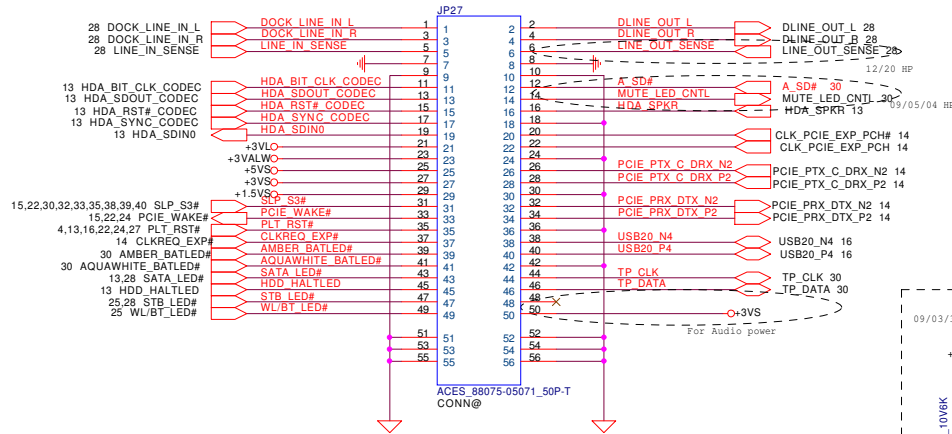
DOCKING CONNECTOR



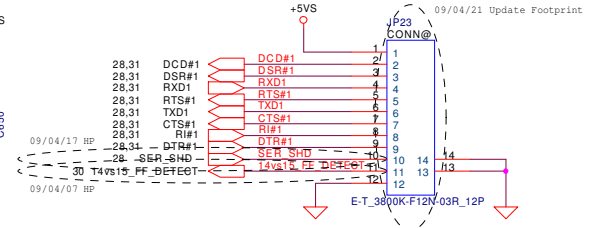
IN	NC<--->COM	NO<--->COM
L	ON	OFF
H	OFF	ON

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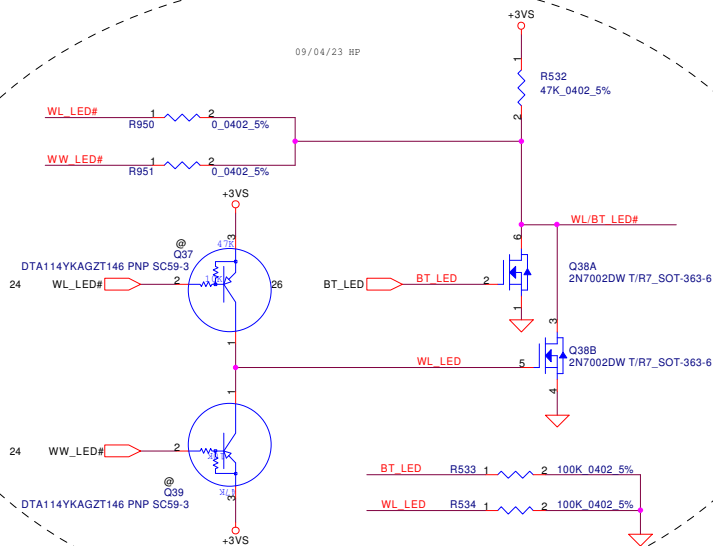
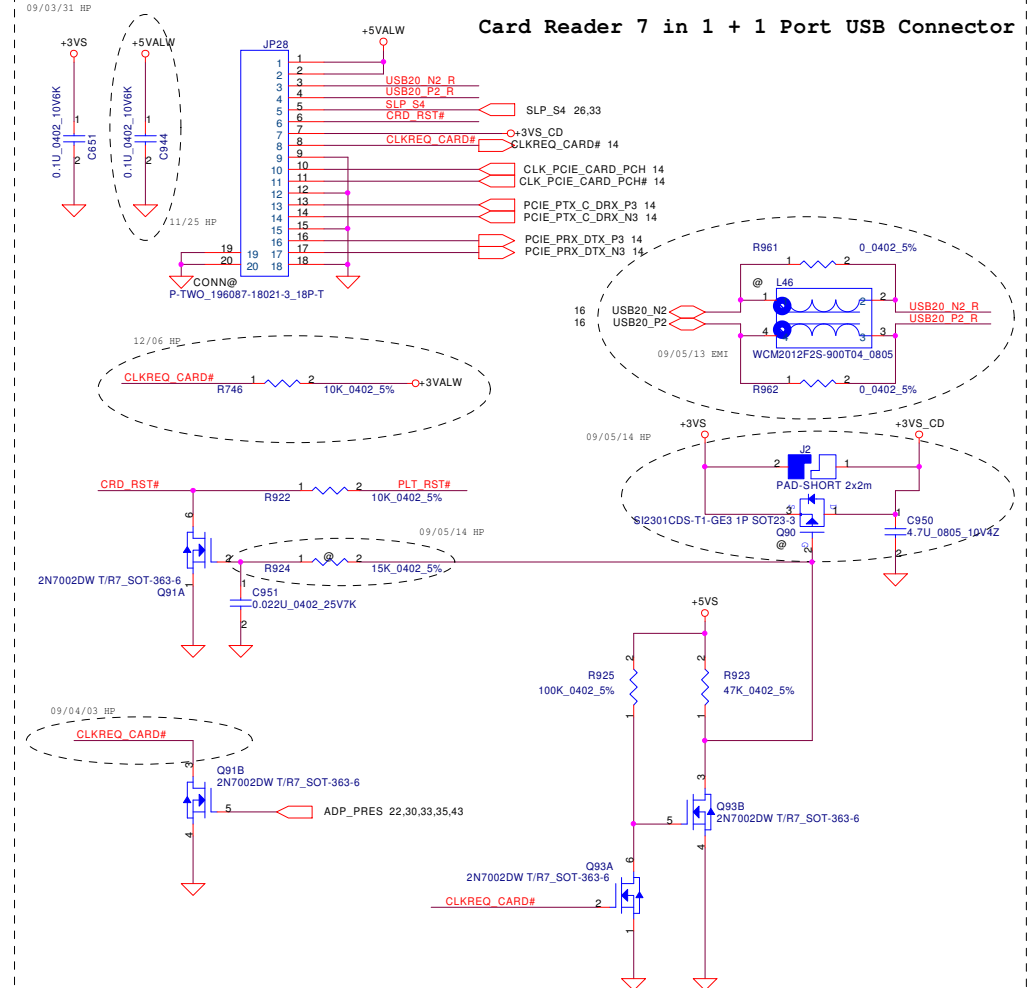
Audio/Express Card/TP/LEDs Connector



Serial Port CONN



Card Reader 7 in 1 + 1 Port USB Connector



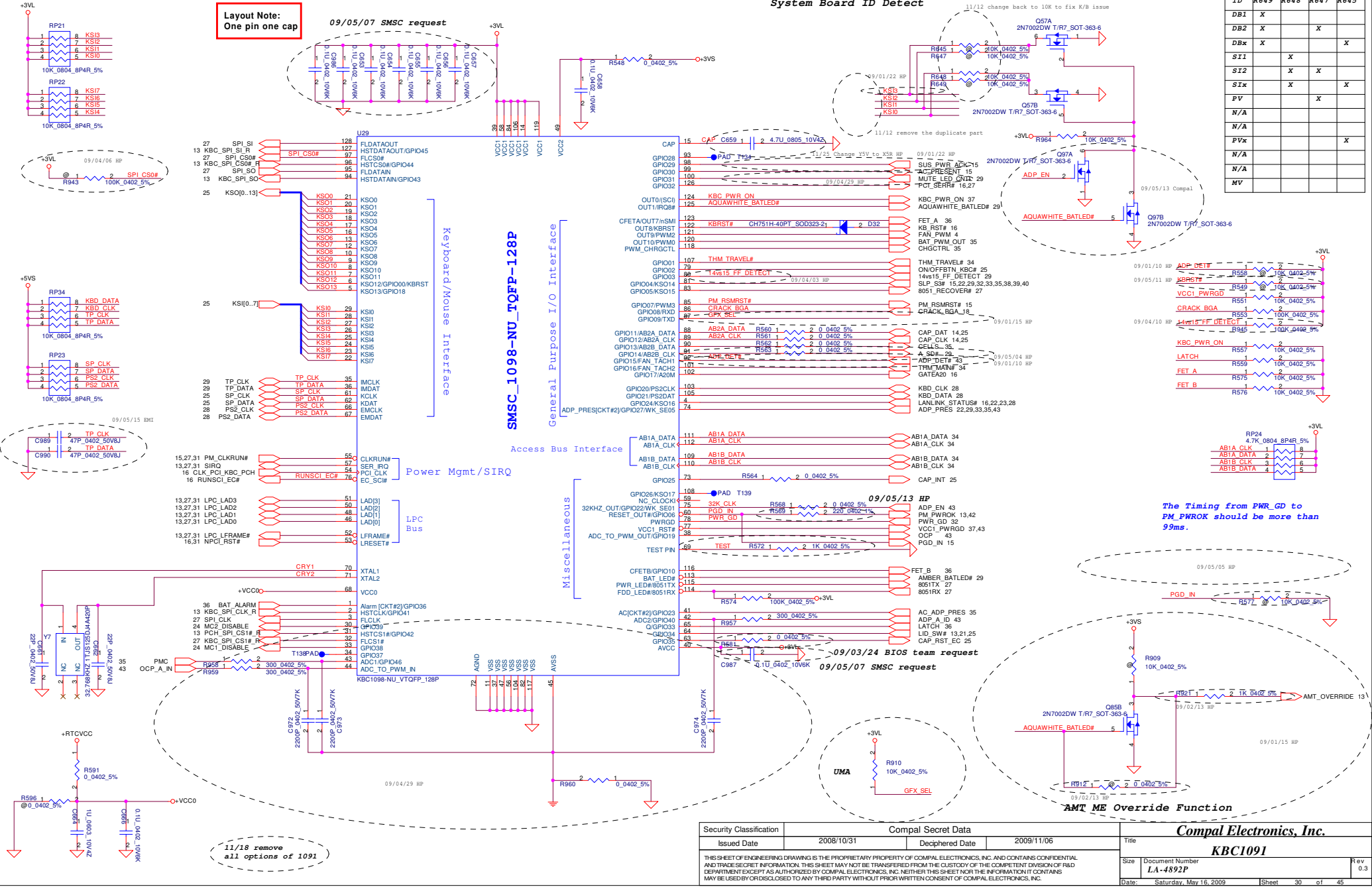
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Layout Note:
One pin one cap

09/05/07 SMSC request

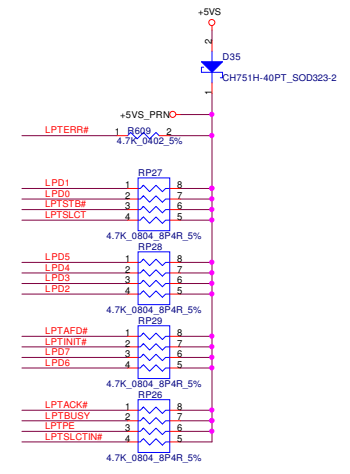
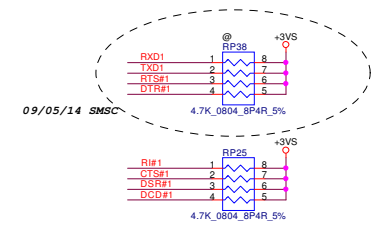
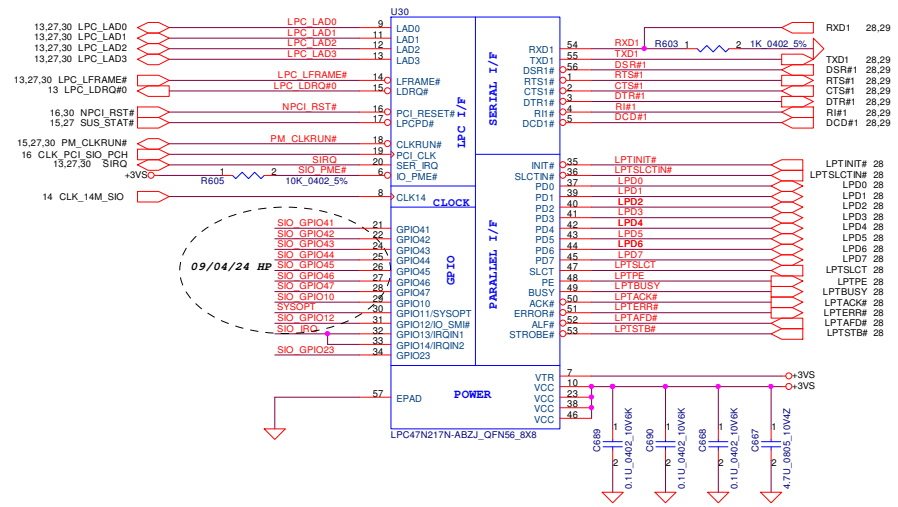
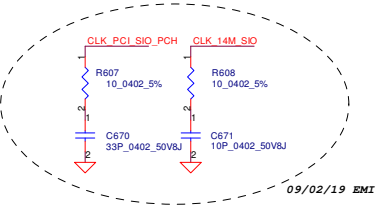
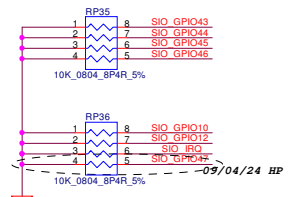
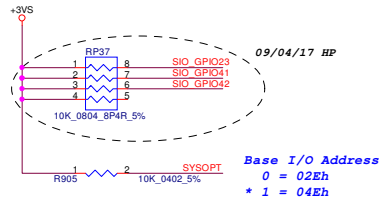
System Board ID Detect

ID	R649	R648	R647	R645
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2			X	X
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				

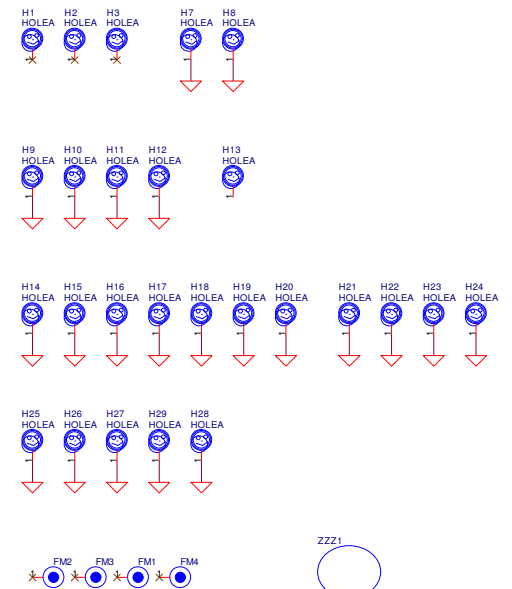
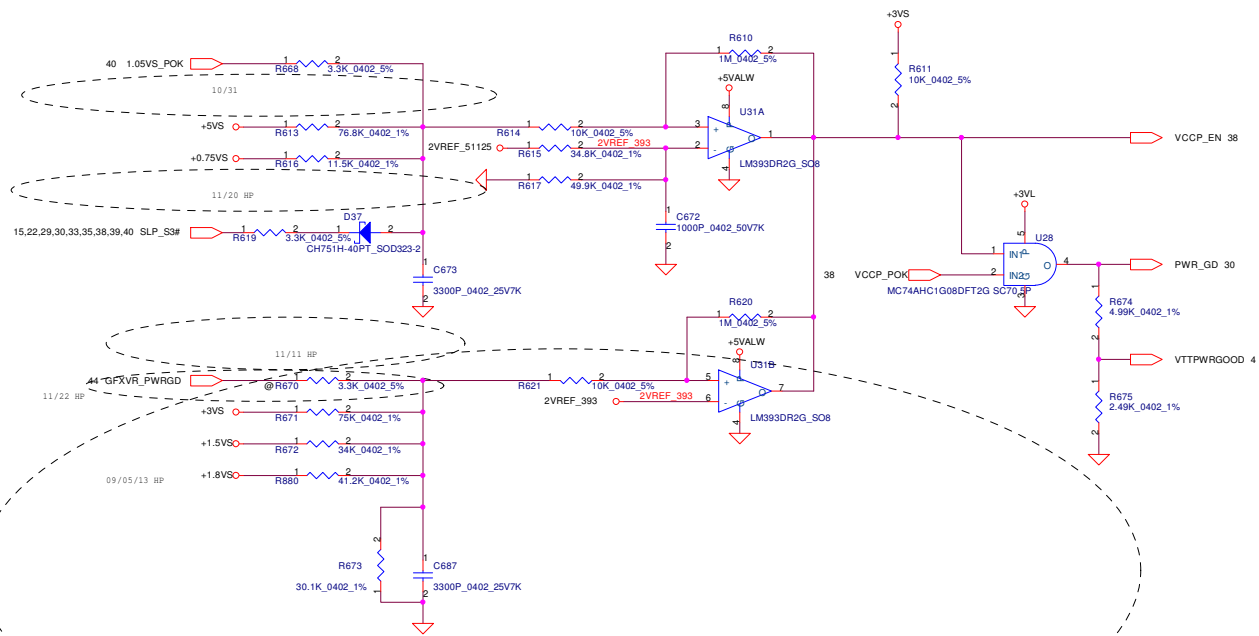


The Timing from PWR_GD to PM PWROK should be more than 99ms.

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ZZZ1
PCB-LA-4982P

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[illegible]

+5VALW to +5VS Transfer

The diagram illustrates the transfer of power from the +5VALW rail to the +5VS rail. A MOSFET (U34) acts as a switch, controlled by +5VALW. The drain of the MOSFET is connected to the +5VS rail via a 10uF capacitor (C681). The source of the MOSFET is connected to ground through a 10k resistor (R1000). A label 'RUNON' is placed near the source connection.

+1.5VALV to +1.5V Transfer

The schematic diagram illustrates the transfer of a signal from the +1.5VALV input to the +1.5V output. The circuit includes the following components and connections:

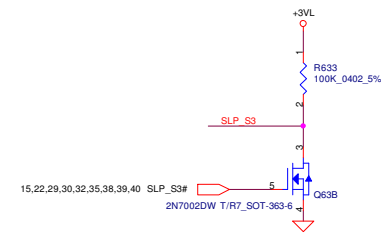
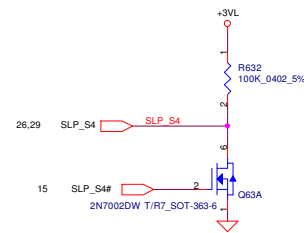
- Inputs:** +1.5VALV and +1.5V.
- Resistors:**
 - R791: 330K_0402_5%
 - R793: 820K_0402_5%
 - R794: 470_0402_5%
- Capacitors:**
 - C785: 0.1u_0402_100MK
 - C786: 10u_0805_100MK
 - C787: 0.1u_0402_100MK
 - C788: 0.1u_0402_16V7K
- MOSFETs:**
 - Q69A: 2N7002DW T/R7_SOT-363-6
 - Q69B: 2N7002DW T/R7_SOT-363-6
- Signal Path:**
 - The +1.5VALV input is connected to the gate of Q69A through R791 and C786.
 - The gate of Q69A is connected to the gate of Q69B through R793 and C787.
 - The gate of Q69B is connected to the +1.5V output through R794 and C788.
 - The source of Q69A is connected to the source of Q69B through R793 and C787.
 - The source of Q69B is connected to the +1.5V output through R794 and C788.
- Control Signal:**
 - A dashed oval labeled **ADP PRES** is connected to the gates of Q69A and Q69B.
 - The ADP PRES signal is also connected to the gates of Q69A and Q69B through R793 and C787.

+1.5VALW to +1.5VS Transfer

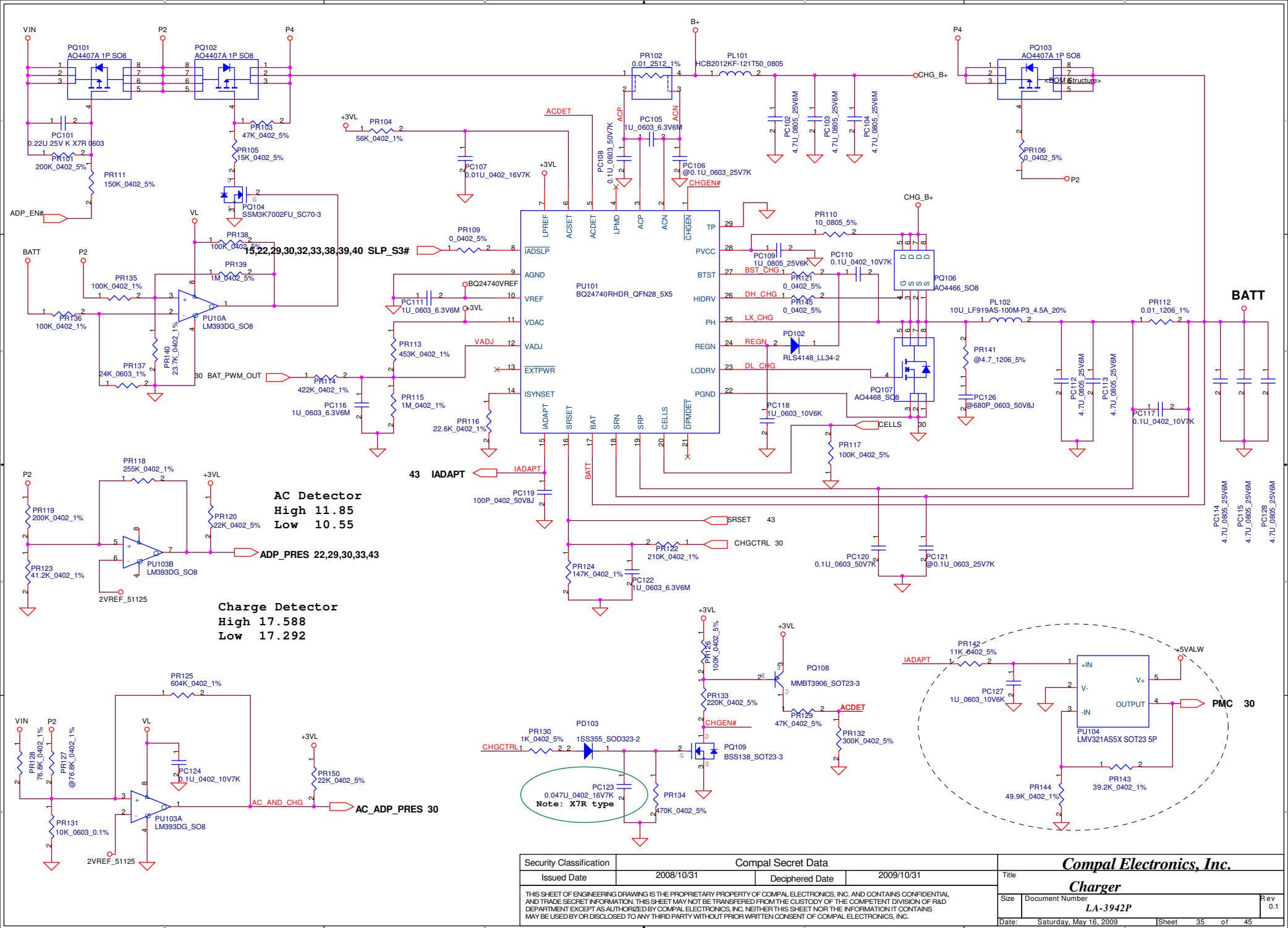
The diagram shows a MOSFET circuit for transferring power from +1.5VALW to +1.5VS. The MOSFET (U38) has its gate connected to +1.5VALW via capacitor C777. Its drain is connected to +1.5VS via capacitor C779 and to the RUNON signal. The source is connected to ground via resistor R792 and capacitor C784.

[illegible]

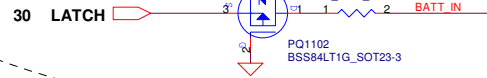
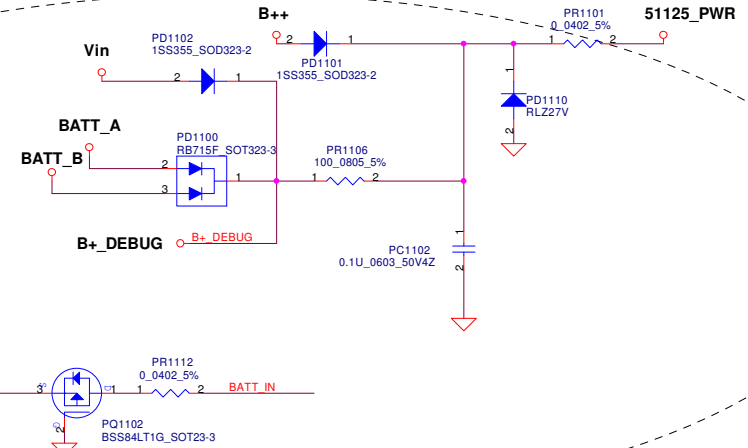
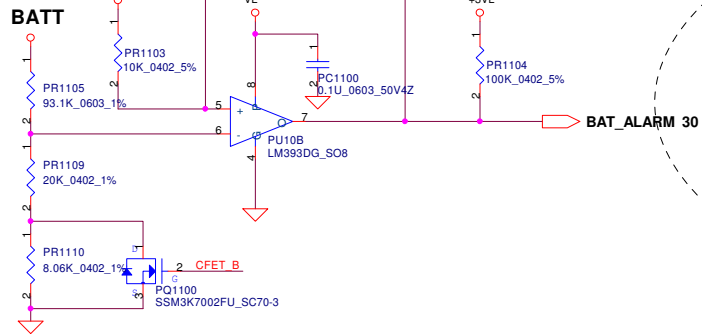
Discharge circuit-1



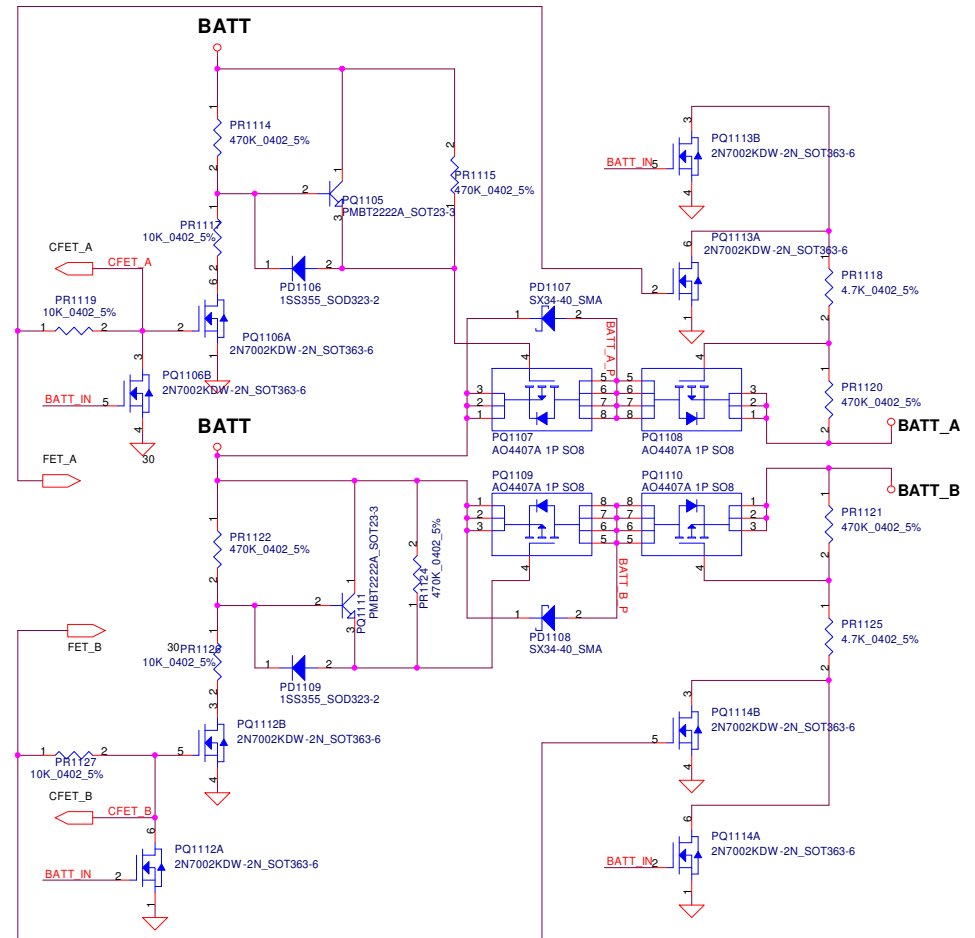
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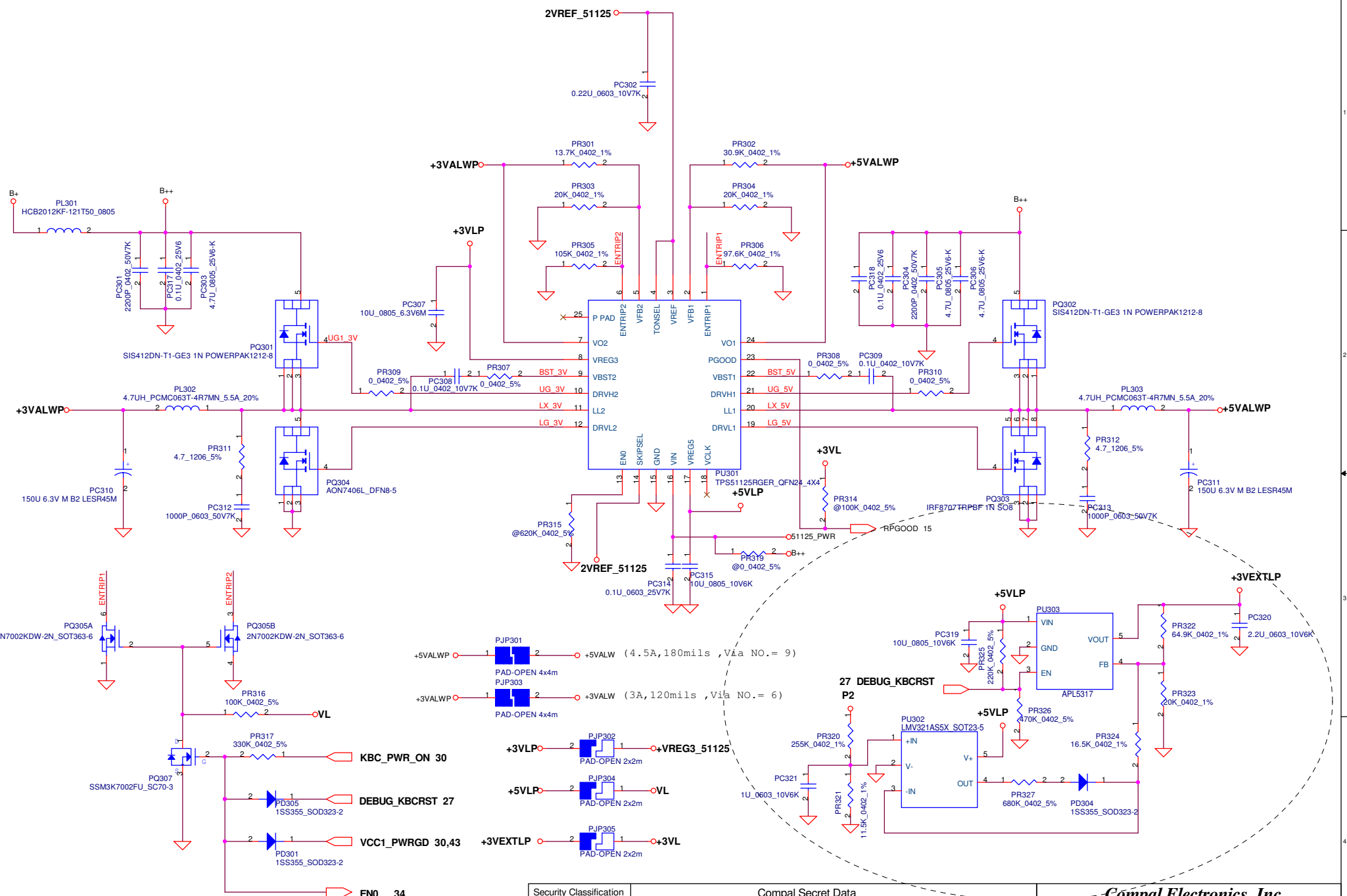
BATT



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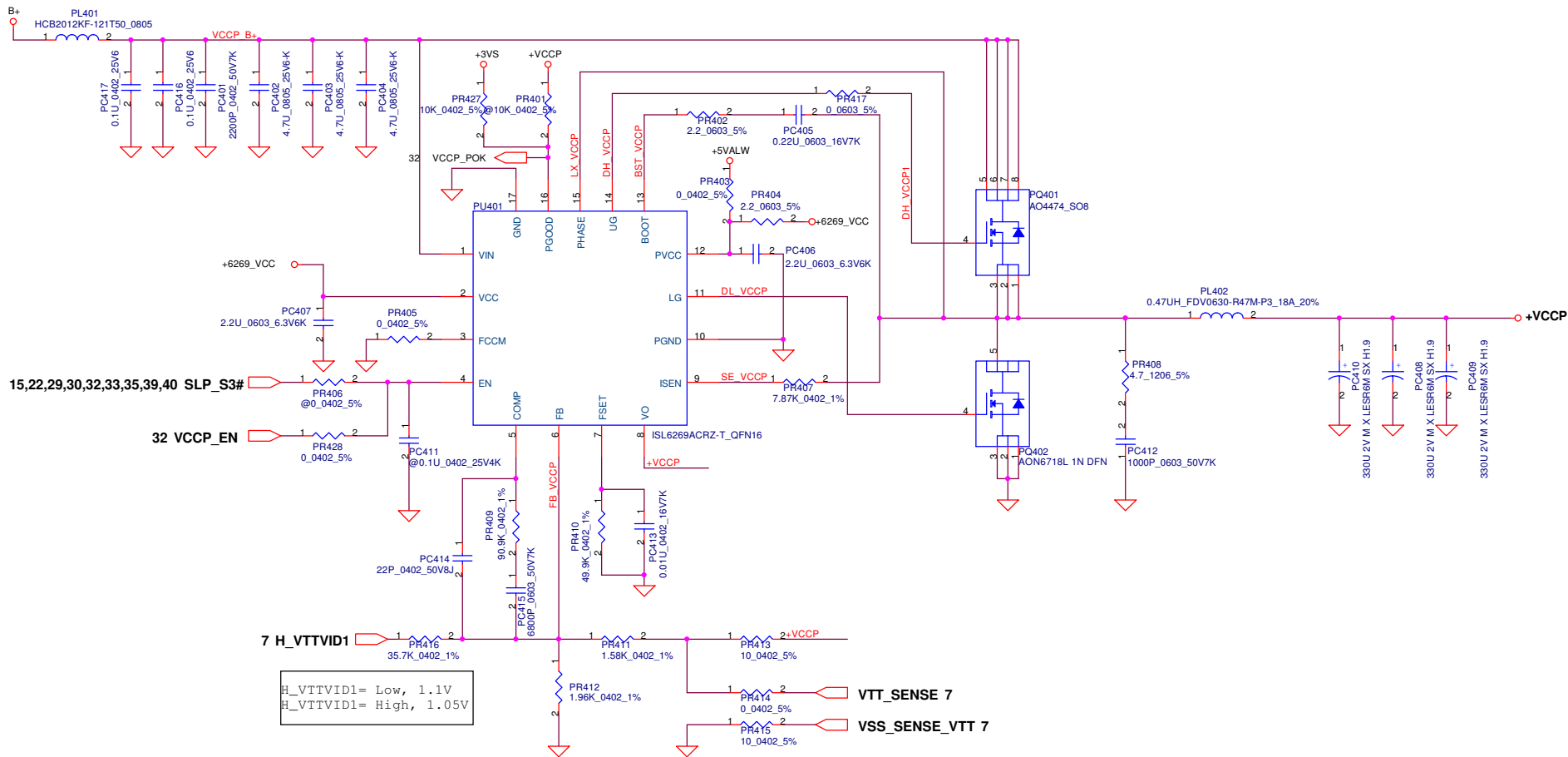


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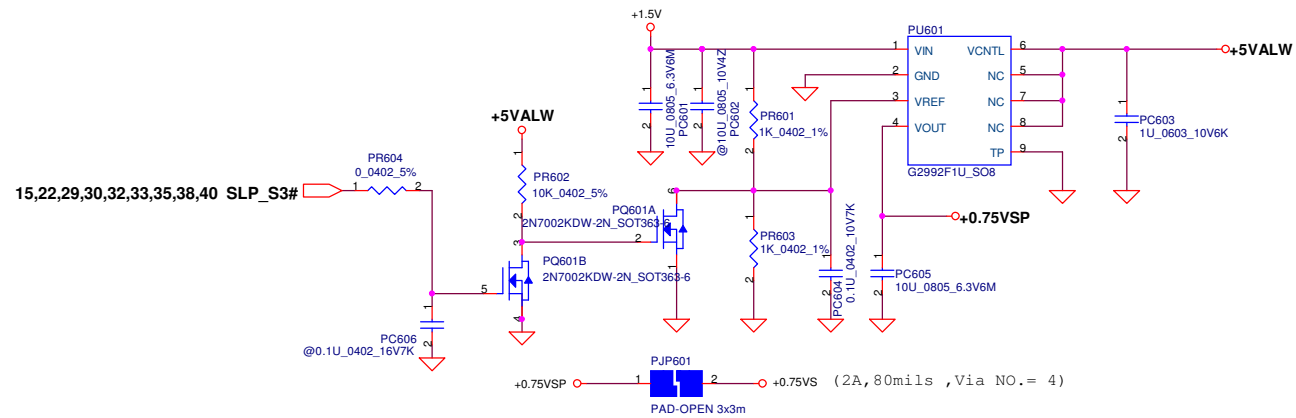
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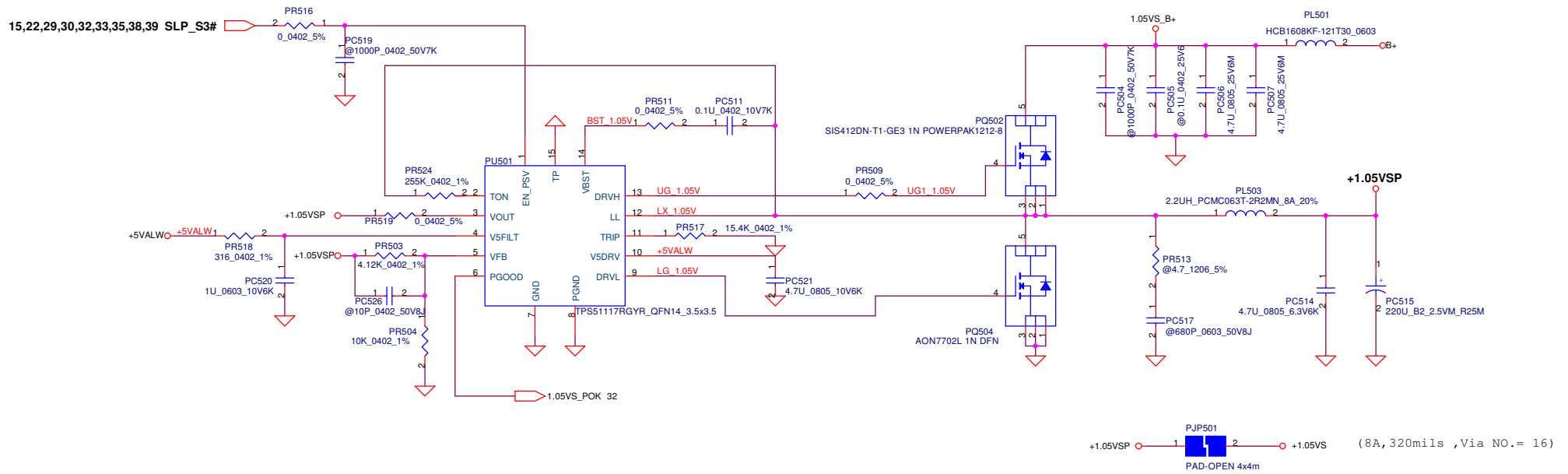


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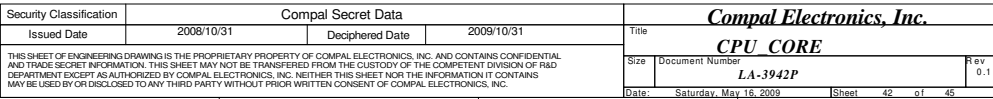
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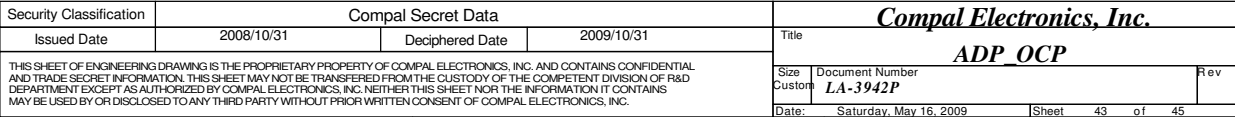


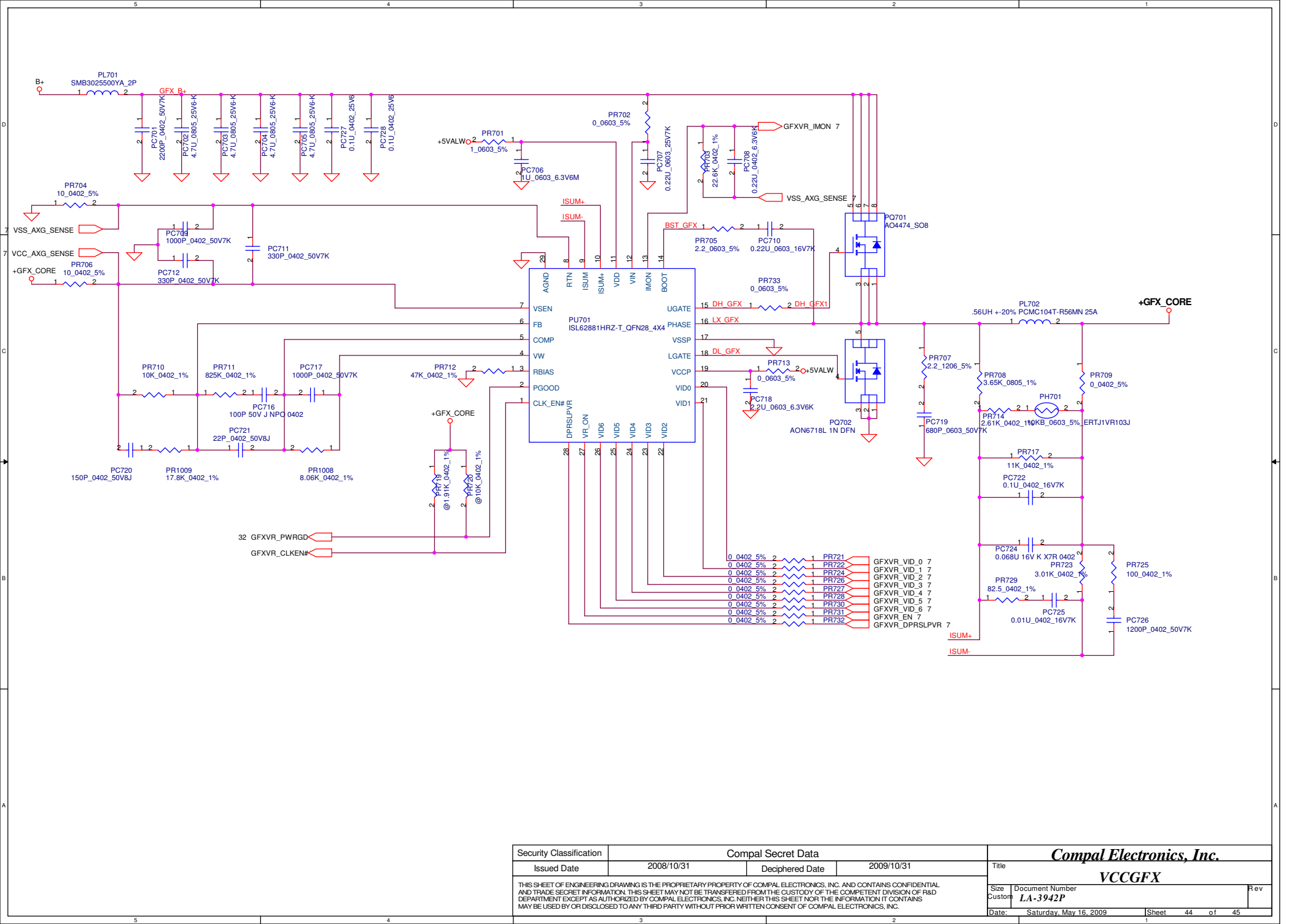
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Item	Reason for change	PG#	Modify List	Date	Phase
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