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KHLB2 Schematics Document

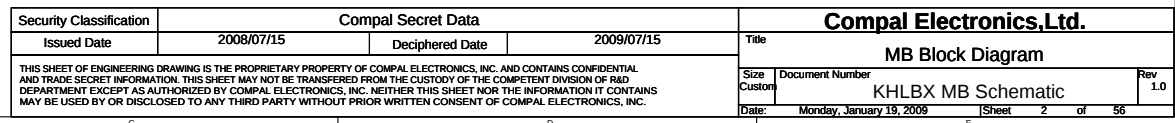
Intel Mobile Penryn uFCPGA with Cantiga_PM + DDRIII + ICH9M

2009-01-19

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics,Ltd.		
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title Cover Sheet		
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				Date: Monday, January 19, 2009	Sheet 1 of 56	

File Name : LA-4772P(ATI)



DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC 1402	100_1100X b
EEPROM(24C16/02)	1010 000X b	ATI M96	

EC SM Bus2 address

GPIO PIN Define

	ID3	ID2	ID1	ID0
JHT00(1100)	X	X	R361	R357
JHT01 (1101)	X	X	R361	R355
JHL90 (1110)	X	X	R360	R357
JHL91 (1111)	X	X	R360	R355
KHLB0 (0000)	R1052	R1150	R922	R928
KHLB1(0001)	R1052	R1150	R922	R923
KHLB2(0010)	R1052	R1150	R927	R928
12 inch(0011)	X	X	X	X
12 inch(0100)	X	X	X	X
12 inch(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X

VGA and DDR2 Voltage Rails (NB9M-GS)

State \ power plane			+1.8VS	+3VS +VGA_CORE +1.1VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	X	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

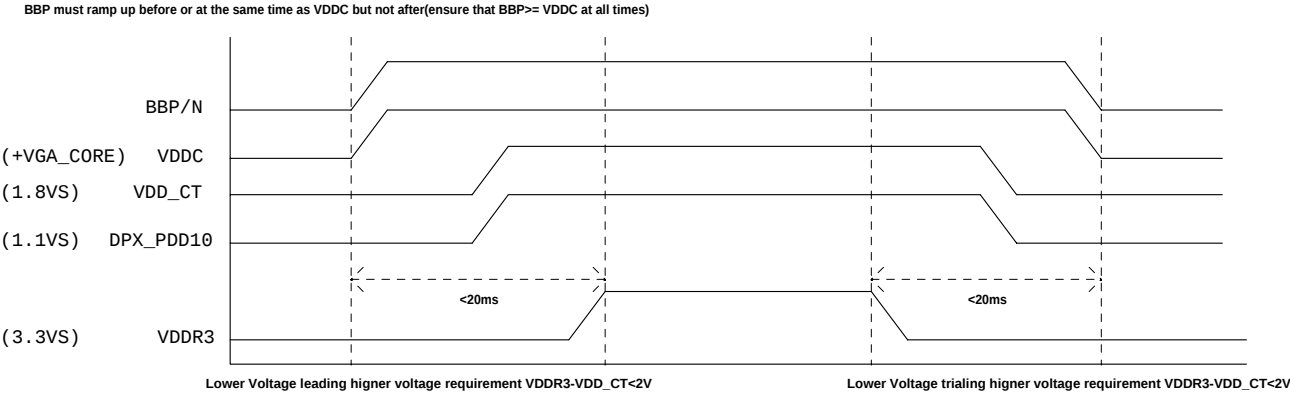
GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	Available
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2 or MEM VID
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	FAN control and/or Thermal Alert (PWM)
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP link E
GPIO16	IN	-	Dongle DVI Mode control for Primary Displayport
GPIO17	IN	-	Dongle HDMI Mode control for Primary Displayport
GPIO18	IN	-	Dongle DVI Mode control for Secondary Displayport
GPIO19	IN	-	Dongle HDMI Mode control for Secondary Displayport
GPIO20	IN	-	Hot plug detect for IFP link D
GPIO21	IN	-	Hot plug detect for IFP link E
GPIO22	IN	-	SLI swap ready signal
GPIO23	N/A	N/A	Available

VRAM POWER SEQUENCE
GDDR3 FOR 4 UNIT = 5.4A

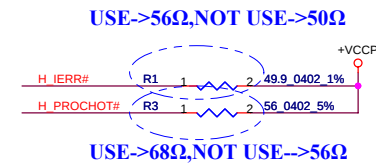
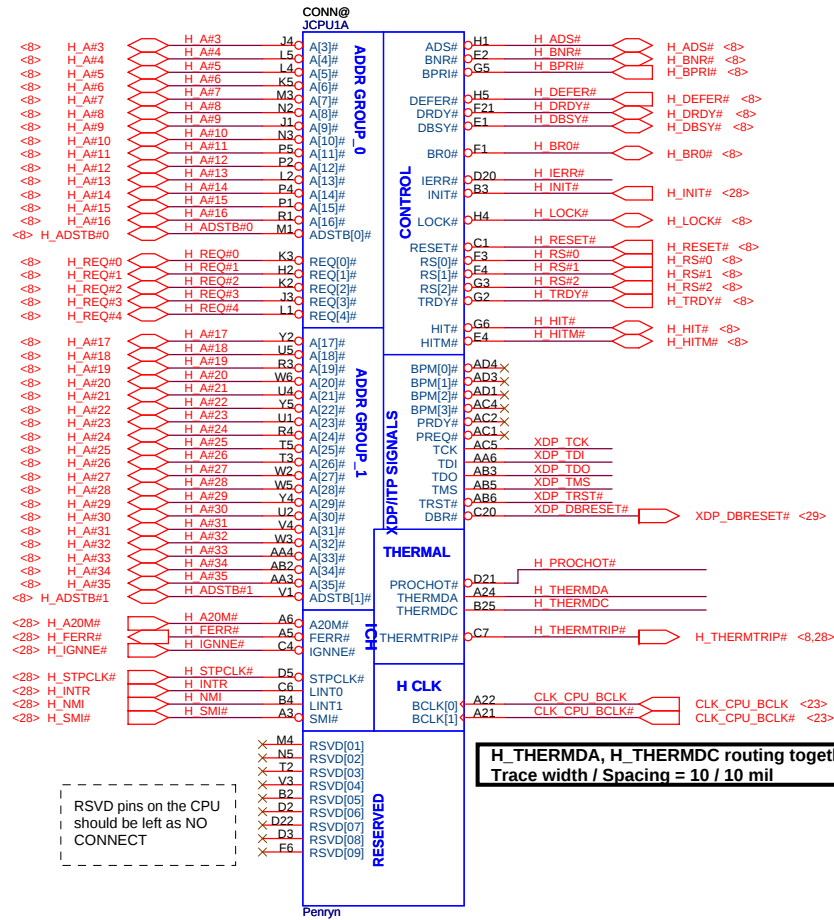
EDP at Tj = 97C*

Power Supply Rail		NB9P-GS		NB9P-GE2	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	20.65A	16.96A	18.47A	16.06A
FB_DLLAVDD	1.1	10mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	80mA			
IFPD_IOVDD	1.1	80mA			
IFPE_IOVDD	1.1	160mA			
IFPF_IOVDD	1.1	160mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	90mA			
PLLVDD	1.1	45mA			
SP_PLLVDD	1.1	45mA			
VID_PLLVDD	1.1	45mA			
TOTAL	1.1	2.3A			
FBVDD/Q	1.8	3.37A	2.02A	3.21A	2.25A
IFPA_IOVDD	1.8	95mA			
IFPB_IOVDD	1.8	95mA			
IFPAB_PLLVDD	1.8	70mA			
IFPCD_PLLVDD	1.8	25mA			
IFPEF_PLLVDD	1.8	85mA			
TOTAL	1.8	5.76A	3.69A	5.47A	3.96A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	120mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	150mA			
TOTAL	3.3	0.51A			

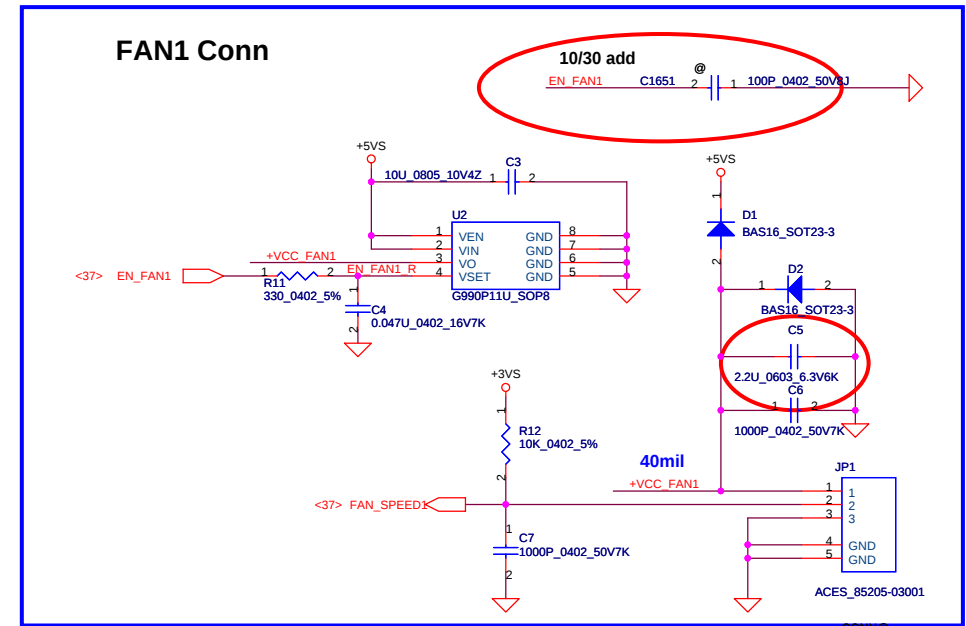
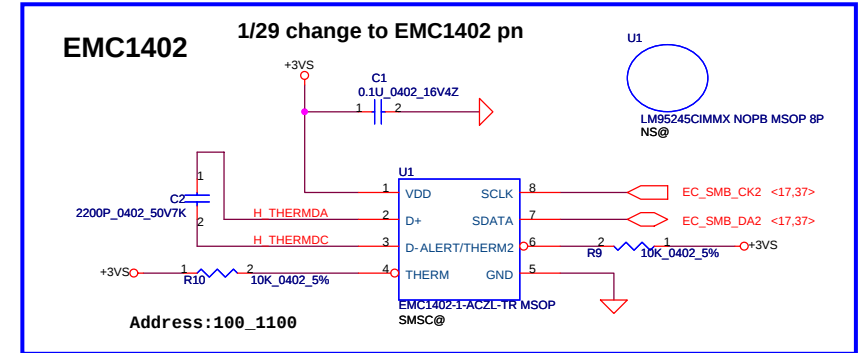
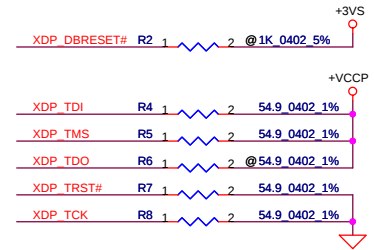
POWER UP/DOWN Sequence



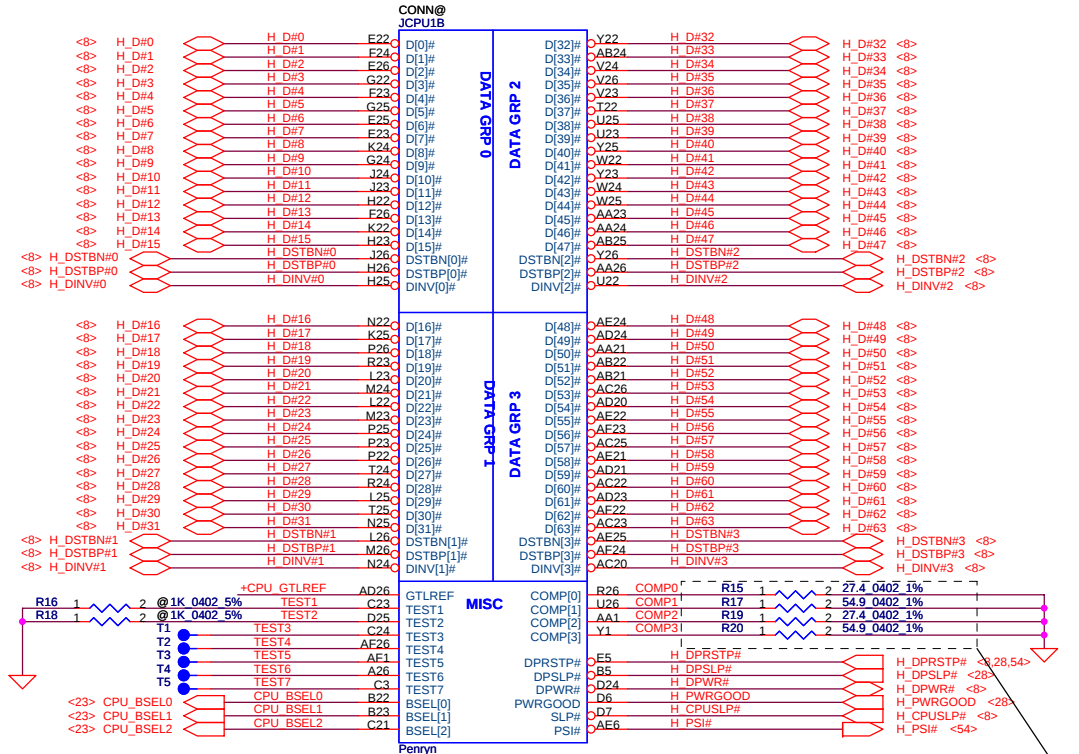
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				Date:	Monday, January 19, 2009	Sheet 4 of 56



XDP Reserve



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				Size		Document Number		Rev 1.0
				Custom		KHLBX MB Schematic		
Date: Monday, January 19, 2009				Sheet 5 of 56				



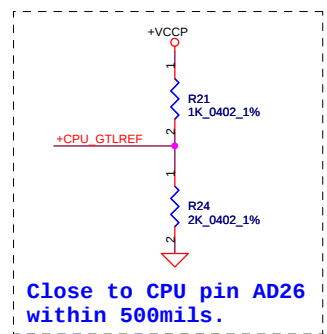
Trace Close CPU < 0.5"

Width=4 mil ,
Spacing: 15mil
(55Ohm)

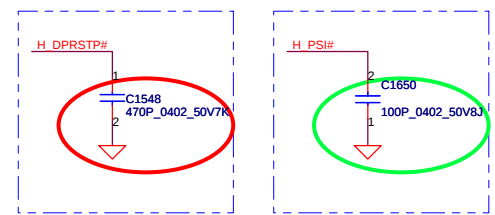
TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)

Layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs
0.5" max for GTLREF.

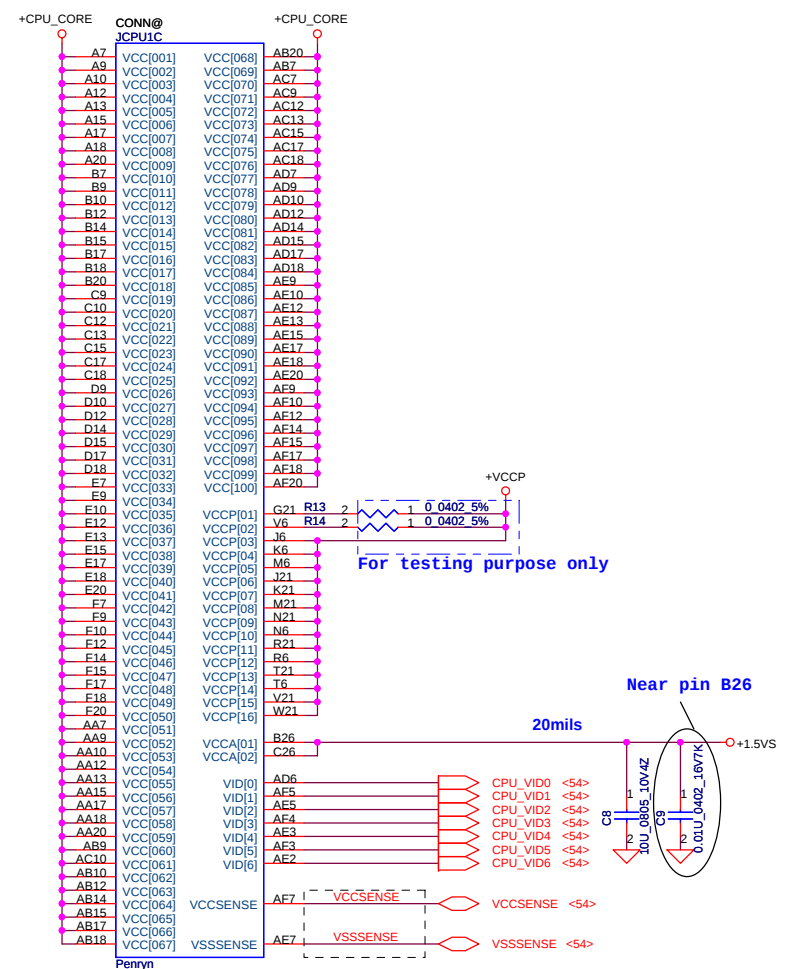
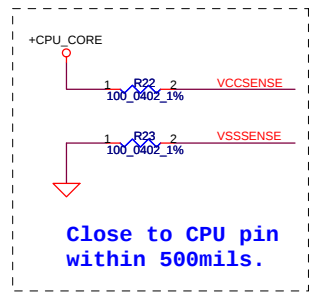


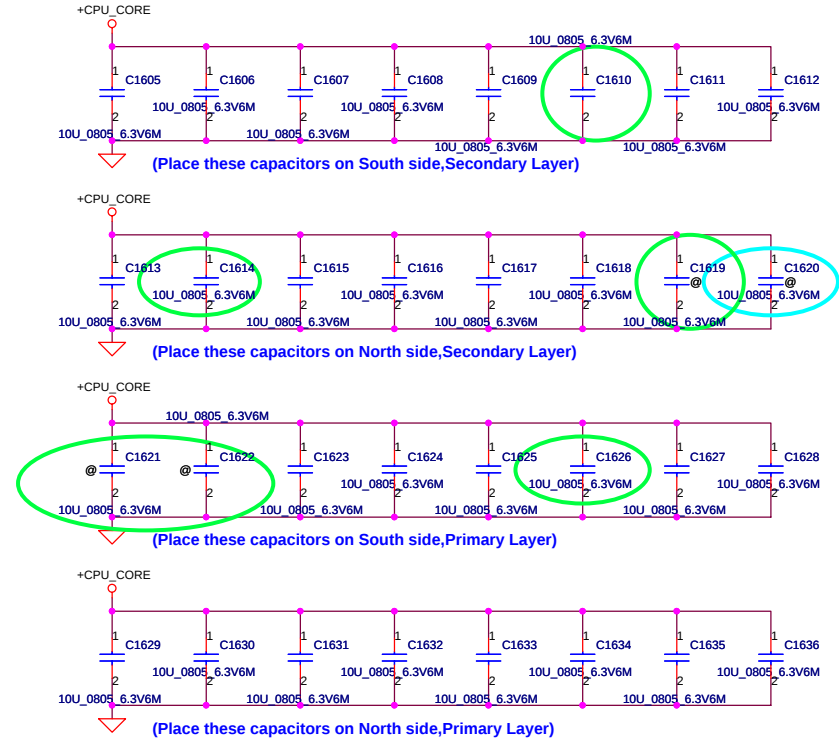
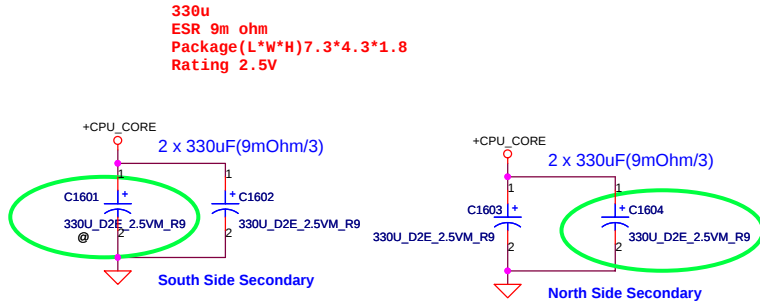
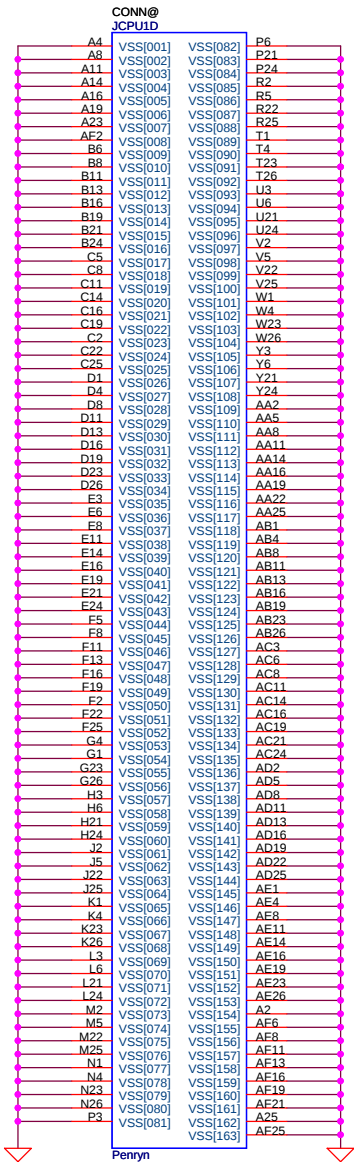
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



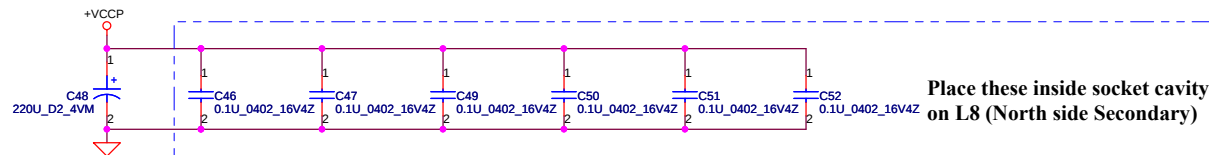
Length match within 25 mils.
The trace width/space/other is 18/7/25.

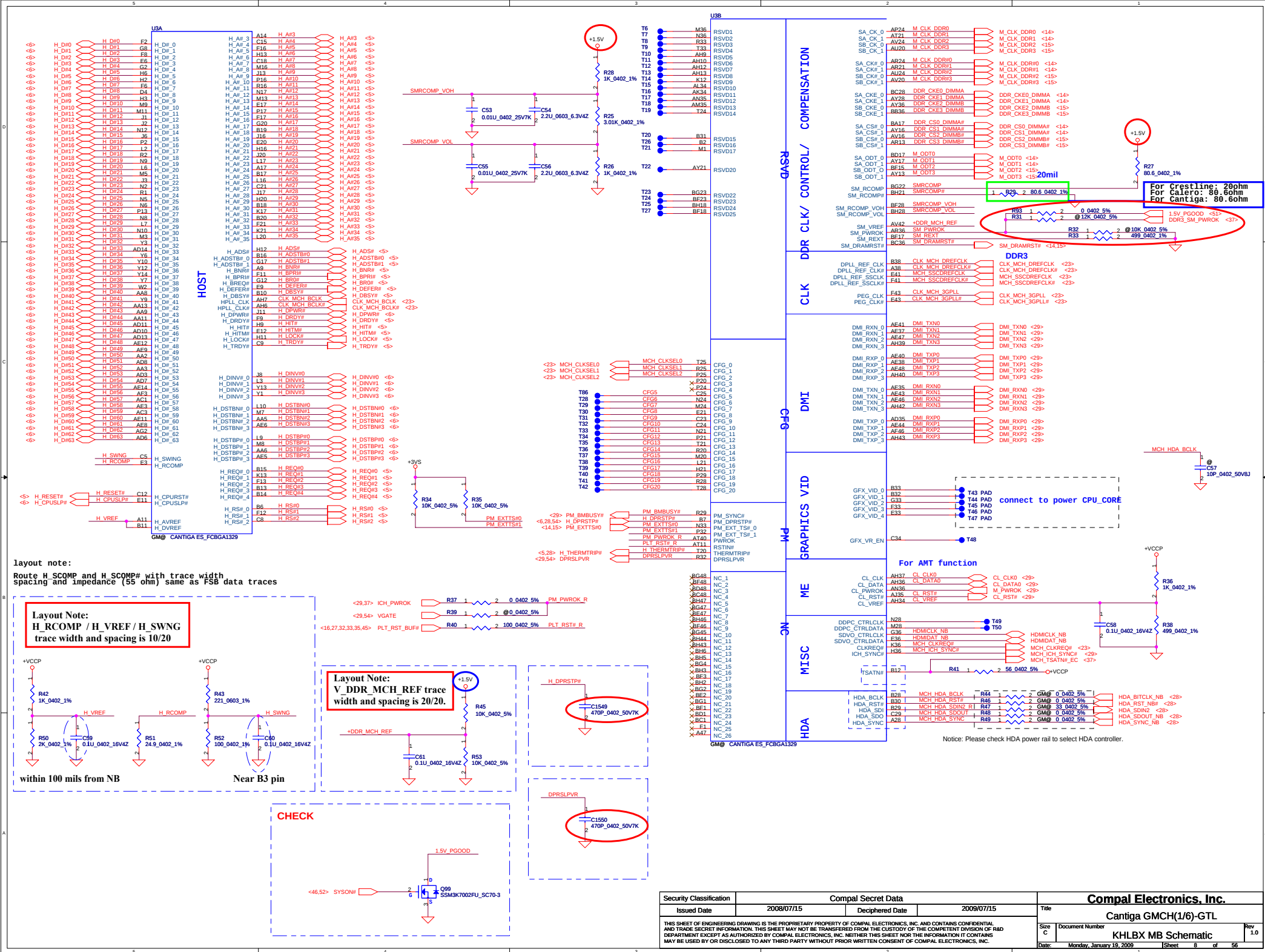
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

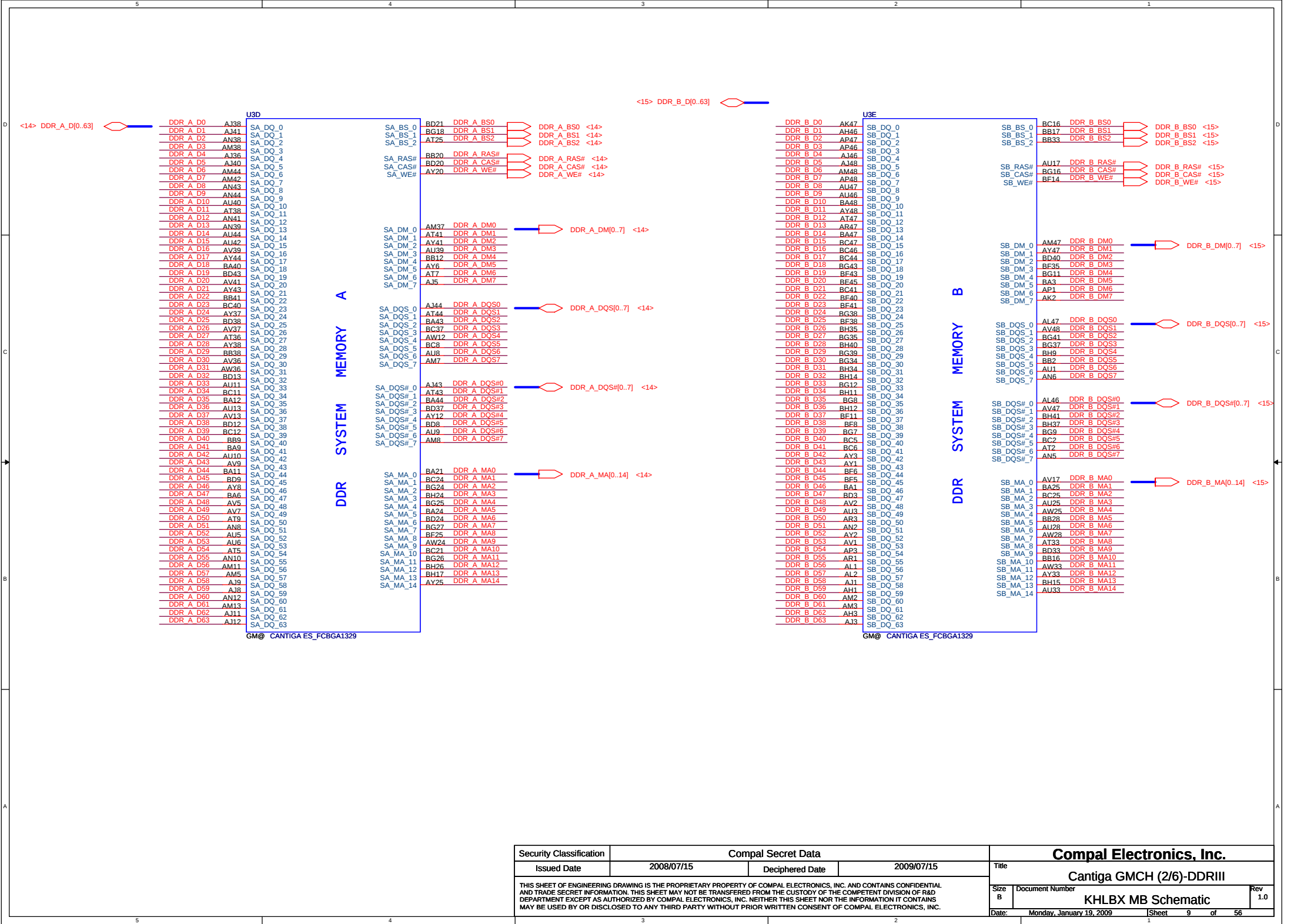


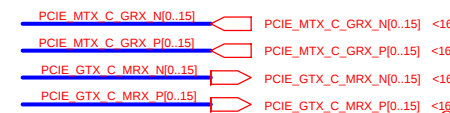
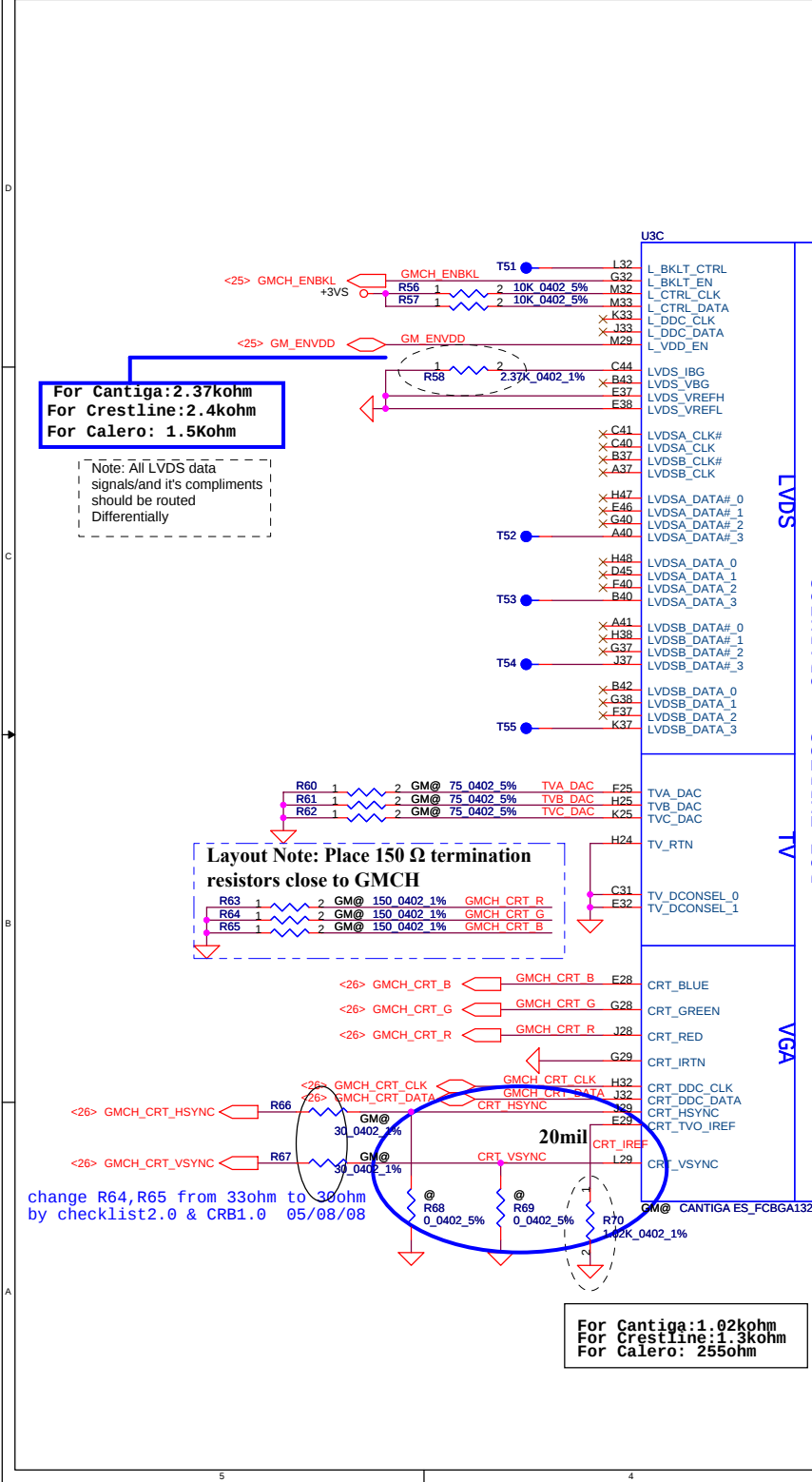


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32









Place the resistor within 500mils (1.27mm) of the (G)MCH
PEGCOMP trace width and spacing is 20/25 mils.



Please check Power source if want support IAMT

PEG_RX#_0	H44	PCIE GTX C MRX N0
PEG_RX#_1	J46	PCIE GTX C MRX N1
PEG_RX#_2	L44	PCIE GTX C MRX N2
PEG_RX#_3	L40	PCIE GTX C MRX N3
PEG_RX#_4	P48	PCIE GTX C MRX N4
PEG_RX#_5	N44	PCIE GTX C MRX N5
PEG_RX#_6	T43	PCIE GTX C MRX N6
PEG_RX#_7	U43	PCIE GTX C MRX N7
PEG_RX#_8	Y48	PCIE GTX C MRX N8
PEG_RX#_9	Y48	PCIE GTX C MRX N9
PEG_RX#_10	Y36	PCIE GTX C MRX N10
PEG_RX#_11	AA43	PCIE GTX C MRX N11
PEG_RX#_12	AD37	PCIE GTX C MRX N12
PEG_RX#_13	AC47	PCIE GTX C MRX N13
PEG_RX#_14	AD39	PCIE GTX C MRX N14
PEG_RX#_15		

PEG_RX#_0	H43	PCIE GTX C MRX P0
PEG_RX#_1	J44	PCIE GTX C MRX P1
PEG_RX#_2	L43	PCIE GTX C MRX P2
PEG_RX#_3	L41	PCIE GTX C MRX P3
PEG_RX#_4	N40	PCIE GTX C MRX P4
PEG_RX#_5	P47	PCIE GTX C MRX P5
PEG_RX#_6	N43	PCIE GTX C MRX P6
PEG_RX#_7	T42	PCIE GTX C MRX P7
PEG_RX#_8	U42	PCIE GTX C MRX P8
PEG_RX#_9	Y42	PCIE GTX C MRX P9
PEG_RX#_10	W47	PCIE GTX C MRX P10
PEG_RX#_11	Y37	PCIE GTX C MRX P11
PEG_RX#_12	AA42	PCIE GTX C MRX P12
PEG_RX#_13	AD38	PCIE GTX C MRX P13
PEG_RX#_14	AC48	PCIE GTX C MRX P14
PEG_RX#_15	AD40	PCIE GTX C MRX P15

CLOSE TO MCH

PEG_TX#_0	J41	PCIE MTX GRX N0	C62	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N0
PEG_TX#_1	M46	PCIE MTX GRX N1	C63	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N1
PEG_TX#_2	M47	PCIE MTX GRX N2	C64	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N2
PEG_TX#_3	M40	PCIE MTX GRX N3	C65	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N3
PEG_TX#_4	M42	PCIE MTX GRX N4	C66	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N4
PEG_TX#_5	R48	PCIE MTX GRX N5	C67	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N5
PEG_TX#_6	N38	PCIE MTX GRX N6	C68	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N6
PEG_TX#_7	T40	PCIE MTX GRX N7	C69	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N7
PEG_TX#_8	U37	PCIE MTX GRX N8	C70	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N8
PEG_TX#_9	U40	PCIE MTX GRX N9	C71	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N9
PEG_TX#_10	Y40	PCIE MTX GRX N10	C72	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N10
PEG_TX#_11	AA46	PCIE MTX GRX N11	C73	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N11
PEG_TX#_12	AA37	PCIE MTX GRX N12	C74	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N12
PEG_TX#_13	AA40	PCIE MTX GRX N13	C75	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N13
PEG_TX#_14	AD43	PCIE MTX GRX N14	C76	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N14
PEG_TX#_15	AC46	PCIE MTX GRX N15	C77	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX N15

PEG_TX#_0	J42	PCIE MTX GRX P0	C78	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P0
PEG_TX#_1	L46	PCIE MTX GRX P1	C79	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P1
PEG_TX#_2	M48	PCIE MTX GRX P2	C80	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P2
PEG_TX#_3	M39	PCIE MTX GRX P3	C81	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P3
PEG_TX#_4	M43	PCIE MTX GRX P4	C82	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P4
PEG_TX#_5	R47	PCIE MTX GRX P5	C83	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P5
PEG_TX#_6	N37	PCIE MTX GRX P6	C84	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P6
PEG_TX#_7	T39	PCIE MTX GRX P7	C85	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P7
PEG_TX#_8	U36	PCIE MTX GRX P8	C86	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P8
PEG_TX#_9	U39	PCIE MTX GRX P9	C87	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P9
PEG_TX#_10	Y39	PCIE MTX GRX P10	C88	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P10
PEG_TX#_11	Y46	PCIE MTX GRX P11	C89	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P11
PEG_TX#_12	AA36	PCIE MTX GRX P12	C90	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P12
PEG_TX#_13	AA39	PCIE MTX GRX P13	C91	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P13
PEG_TX#_14	AD42	PCIE MTX GRX P14	C92	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P14
PEG_TX#_15	AD46	PCIE MTX GRX P15	C93	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX C GRX P15

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational.* 1 = PCIe/SDVO are operating simu.

For Cantiga:2.37kohm
For Crestline:2.4kohm
For Calero: 1.5Kohm

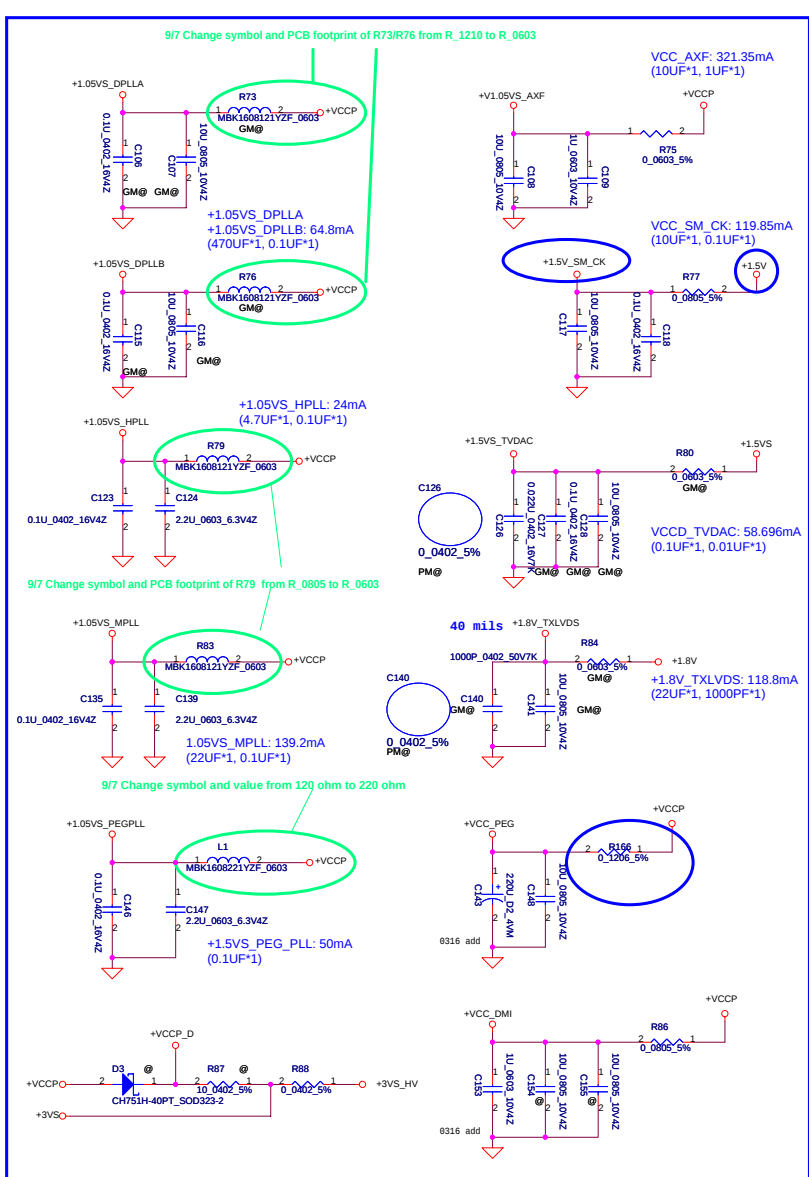
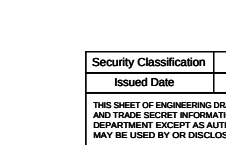
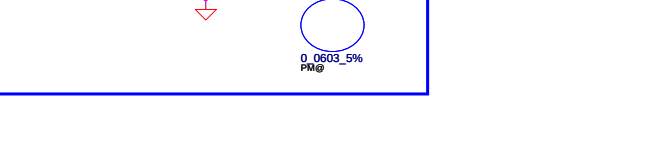
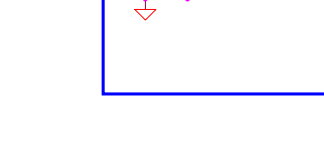
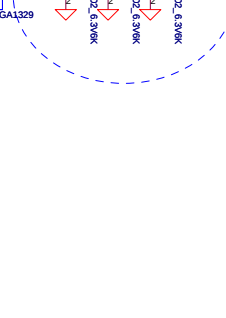
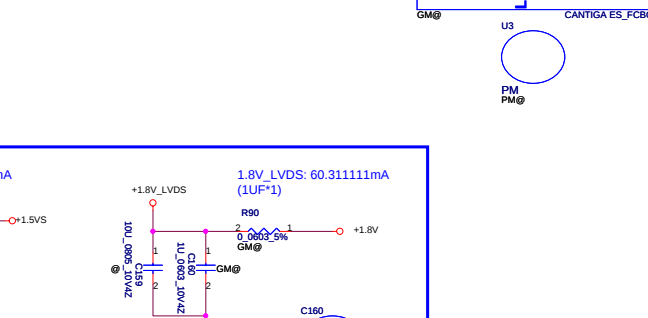
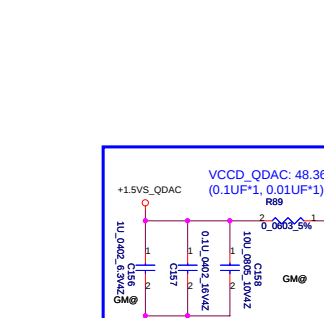
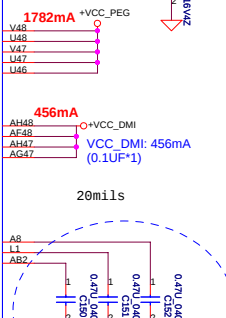
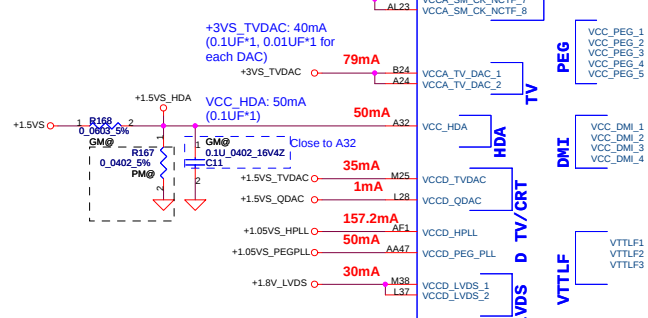
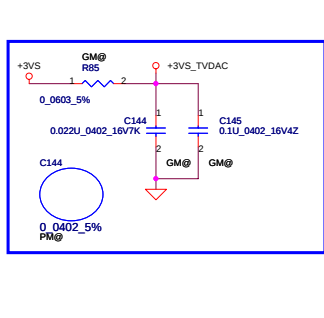
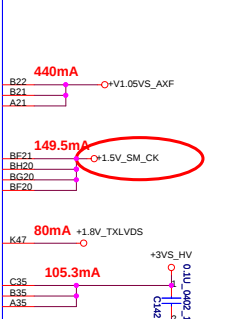
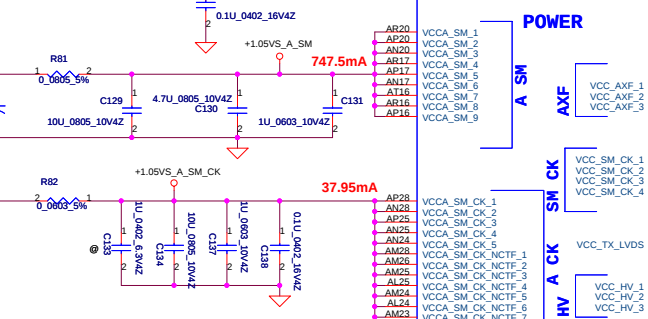
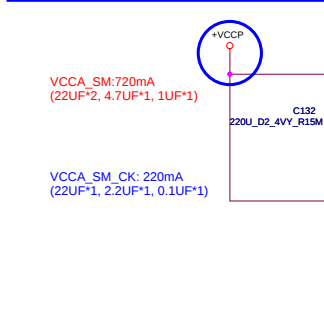
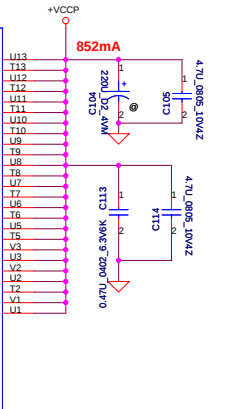
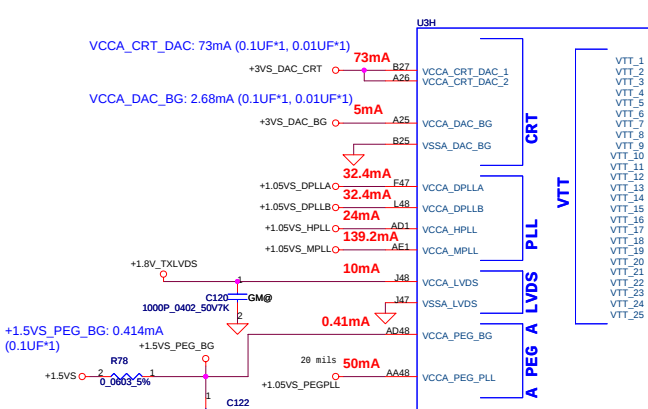
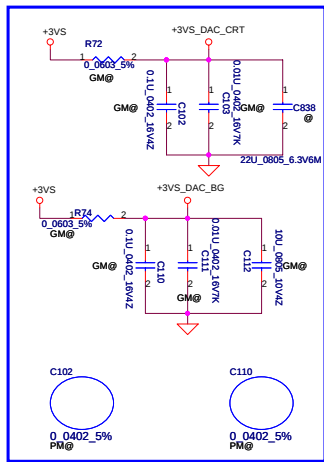
Note: All LVDS data signals/and it's compliments should be routed Differentially

Layout Note: Place 150 Ω termination resistors close to GMCH

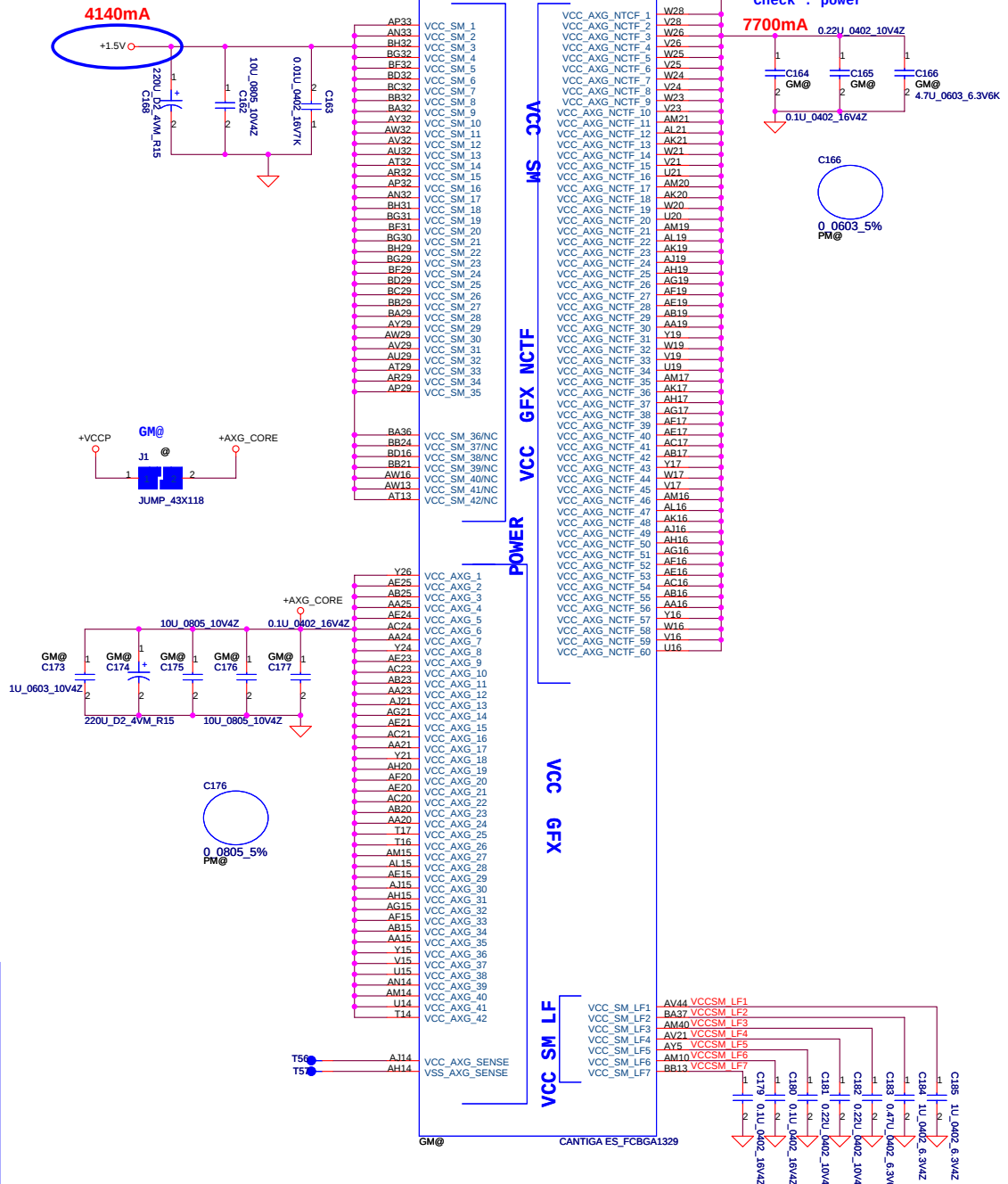
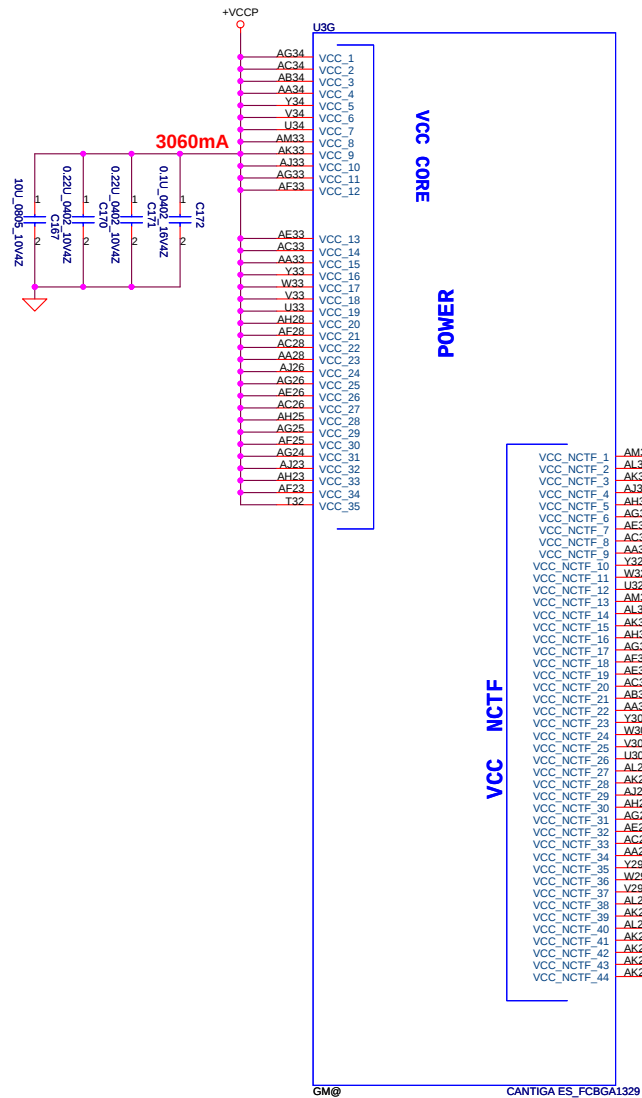
change R64,R65 from 33ohm to 30ohm by checklist2.0 & CRB1.0 05/08/08

For Cantiga:1.02kohm
For Crestline:1.3kohm
For Calero: 255ohm

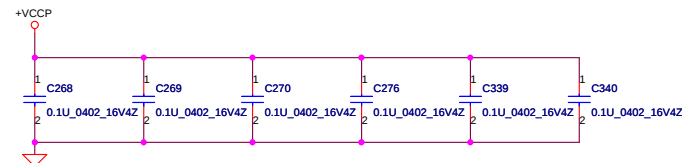
Security Classification	Compal Secret Data			Compal Electronics,Ltd.		
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title		
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Size	Document Number	KHLBX MB Schematic		Rev	1.0	
Date:	Monday, January 19, 2009	Sheet	10	of	56	



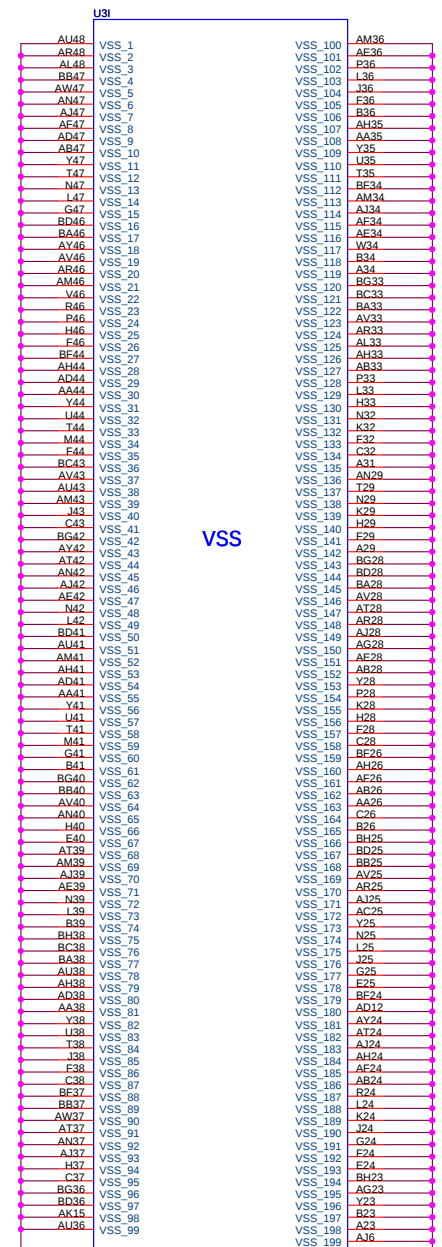
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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	Crestone GMCH (4/6)-VCC
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				Rev	1.0
				Date	Monday, January 19, 2009
				Sheet	11 of 56



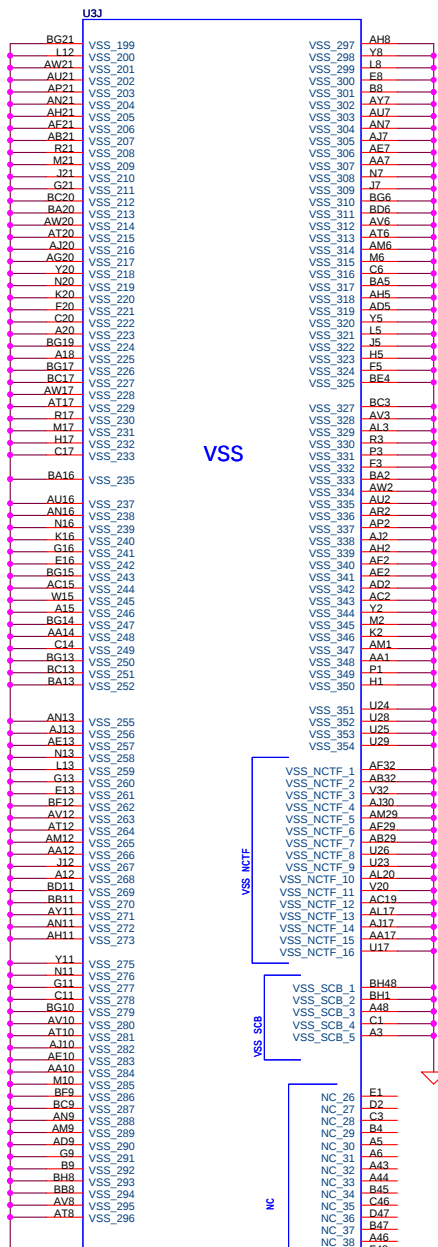
Add these caps around PCI-E bus of NB



Security Classification		Compal Secret Data		Title	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Crestline GMCH (5/6)-VCC	
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				Custom	1.0
				KHLBX MB Schematic	
				Date	Monday, January 19, 2009
				Sheet	12 of 56

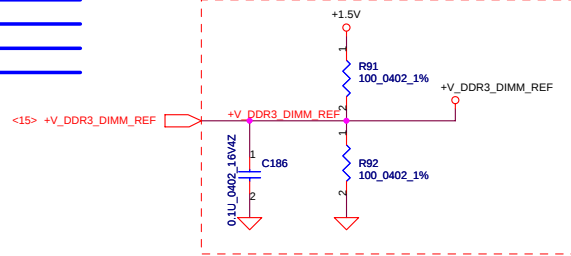


GM® CANTIGA ES_FCBGA1329



GM® CANTIGA ES_FCBGA1329

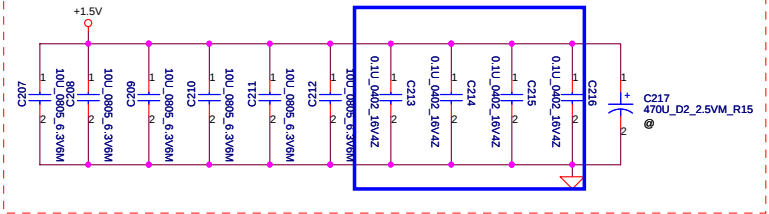
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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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Size	Document Number	KHLBX MB Schematic		Rev 1.0	
Custom		Date: Monday, January 19, 2009		Sheet 13 of 56	

[illegible]

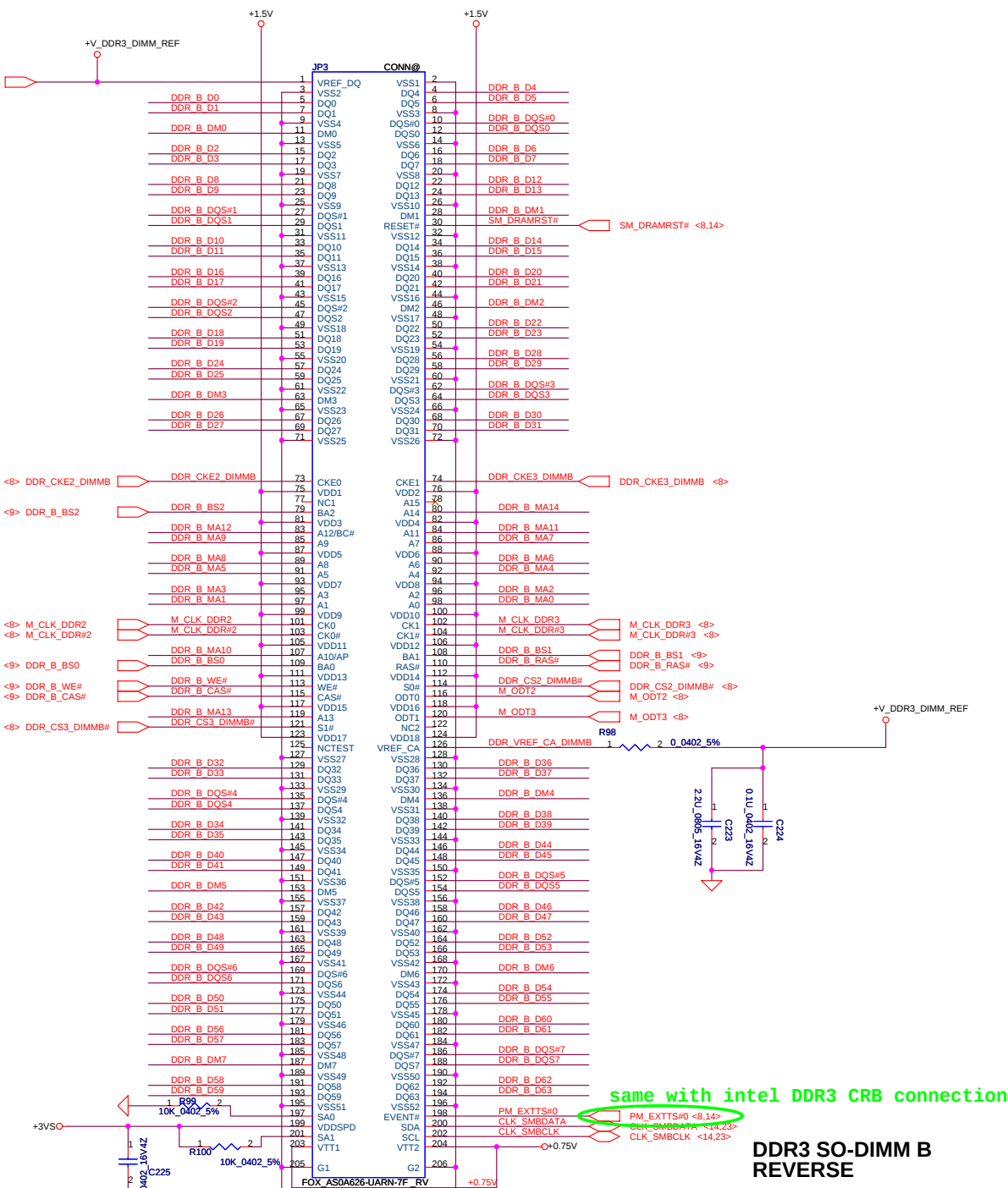
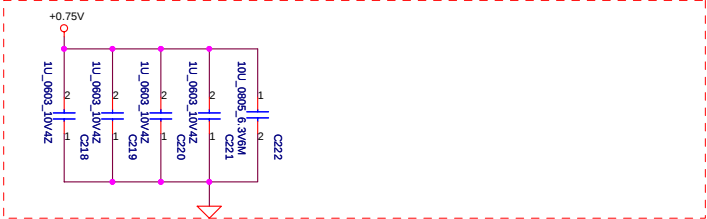
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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	DDRIII-SODIMM SLOT1	
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				Custom	KHLBX MB Schematic	1.0
				Date:	Monday, January 19, 2009	Sheet 14 of 56

<9> DDR_B_DQS#[0..7]
<9> DDR_B_D[0..63]
<9> DDR_B_DM[0..7]
<9> DDR_B_DQS[0..7]
<9> DDR_B_MA[0..14]

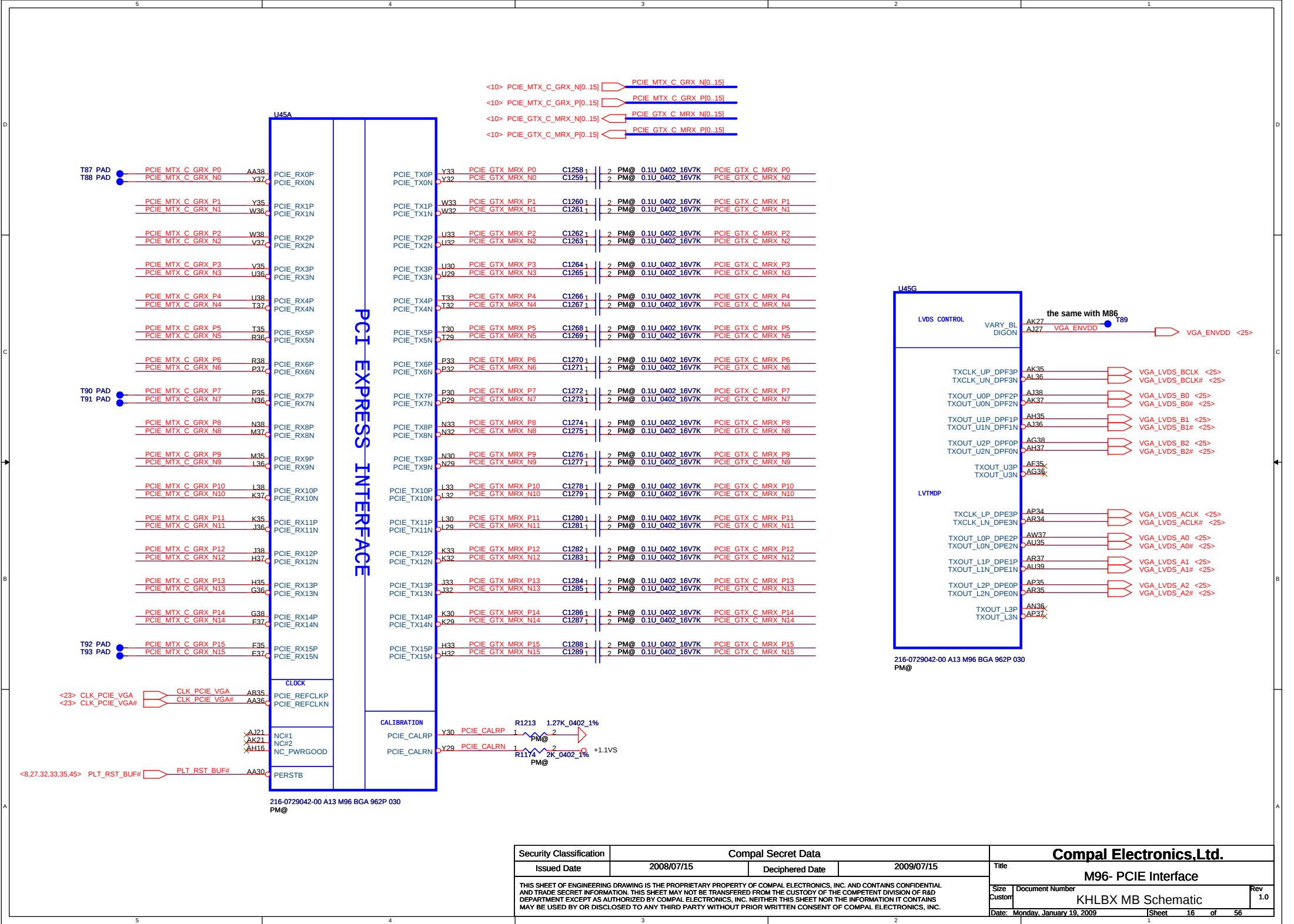
Layout Note:
Place near JP5



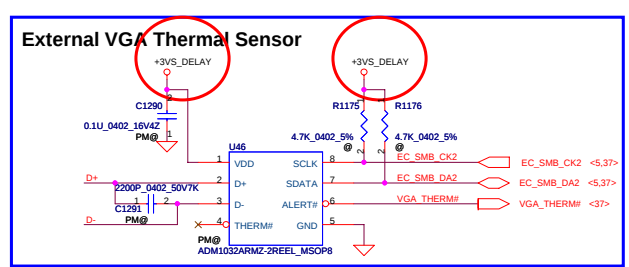
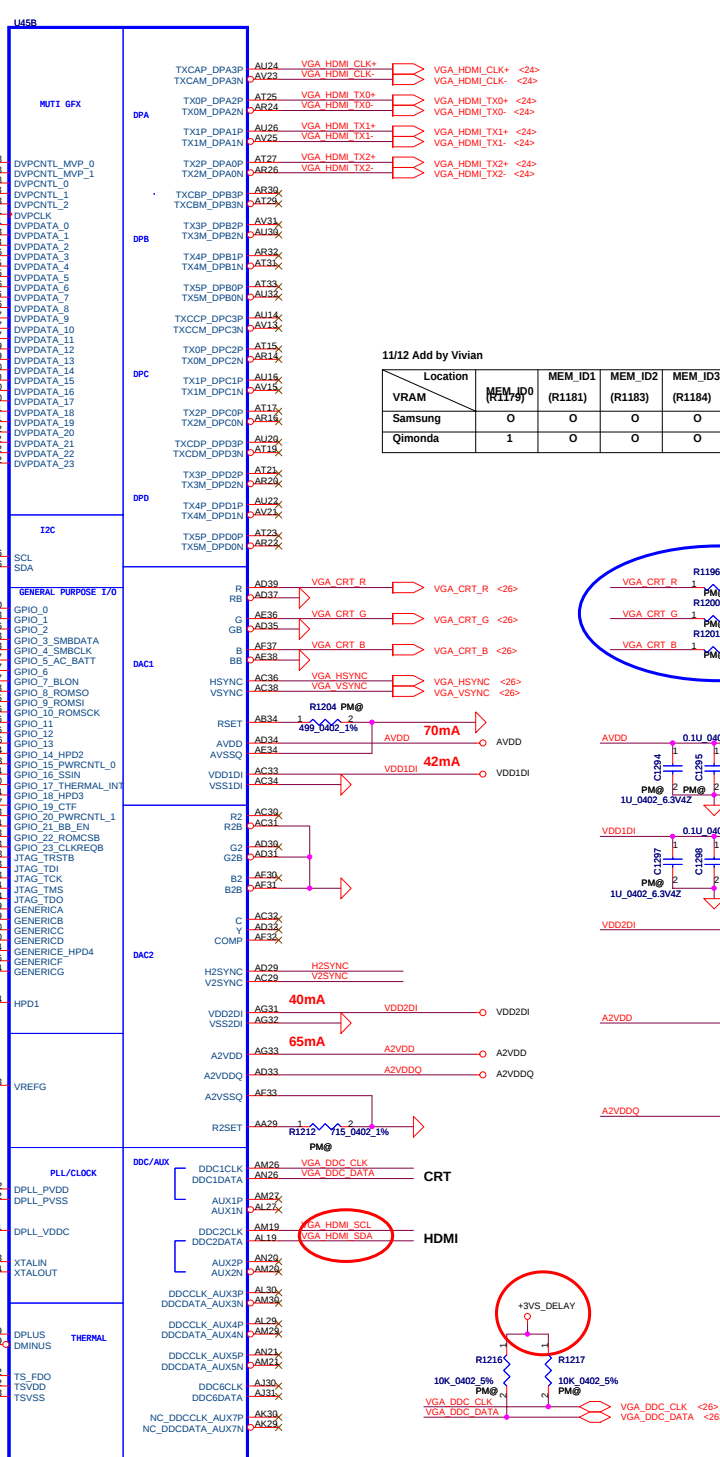
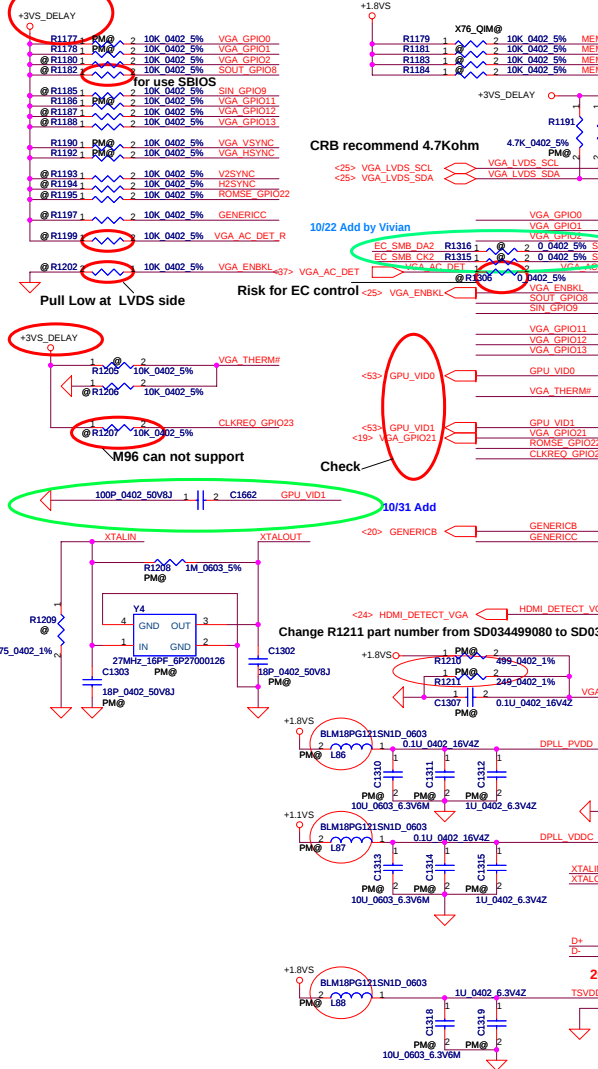
Layout Note:
Place near JP5.203 & JP5.204



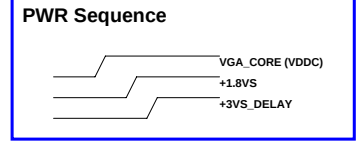
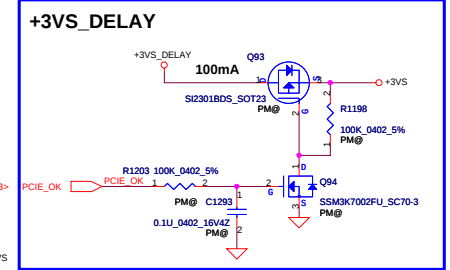
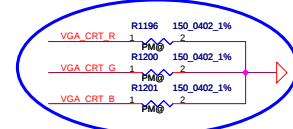
Security Classification		Compal Secret Data		Title	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	DDRIII-SODIMM SLOT2	
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				Custom	KHLBX MB Schematic
				Date:	Monday, January 19, 2009
				Sheet	15 of 56

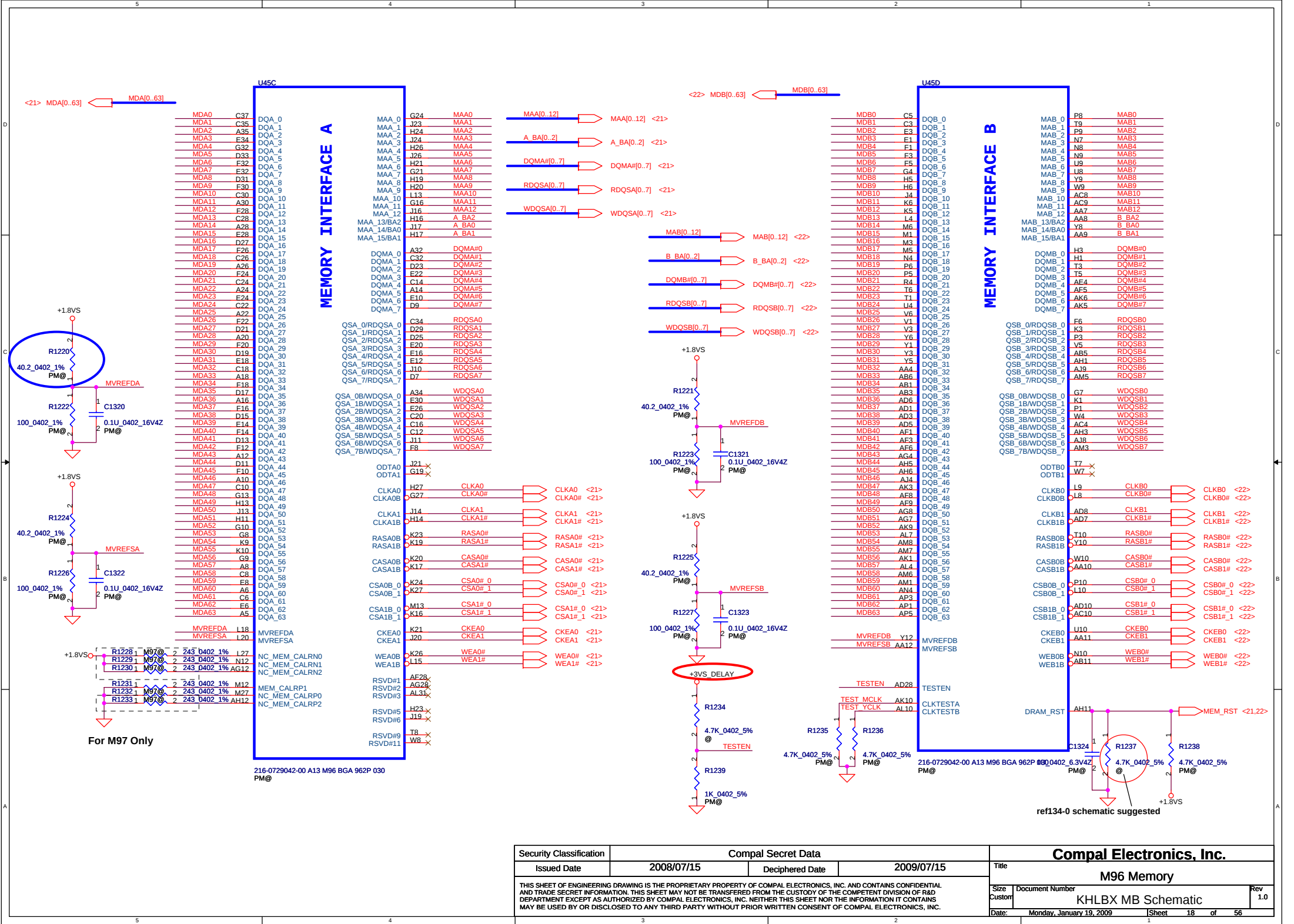


Strap Name	Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0 Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1 PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
BIF_GEN2_EN	GPIO2 0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on	0
STRAP_BIF_CLK_BIF_EN	GPIO22 0: CLKREQ power management capability is disabled 1: CLKREQ power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11 a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22 Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC 00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1
CCBYPASS SMS_EN_HARD	GENERICC H2SYNCR 0: Bypass, 1: Hard	0
VIP_DEVICE STRAP_DIS	V2SYNCR If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

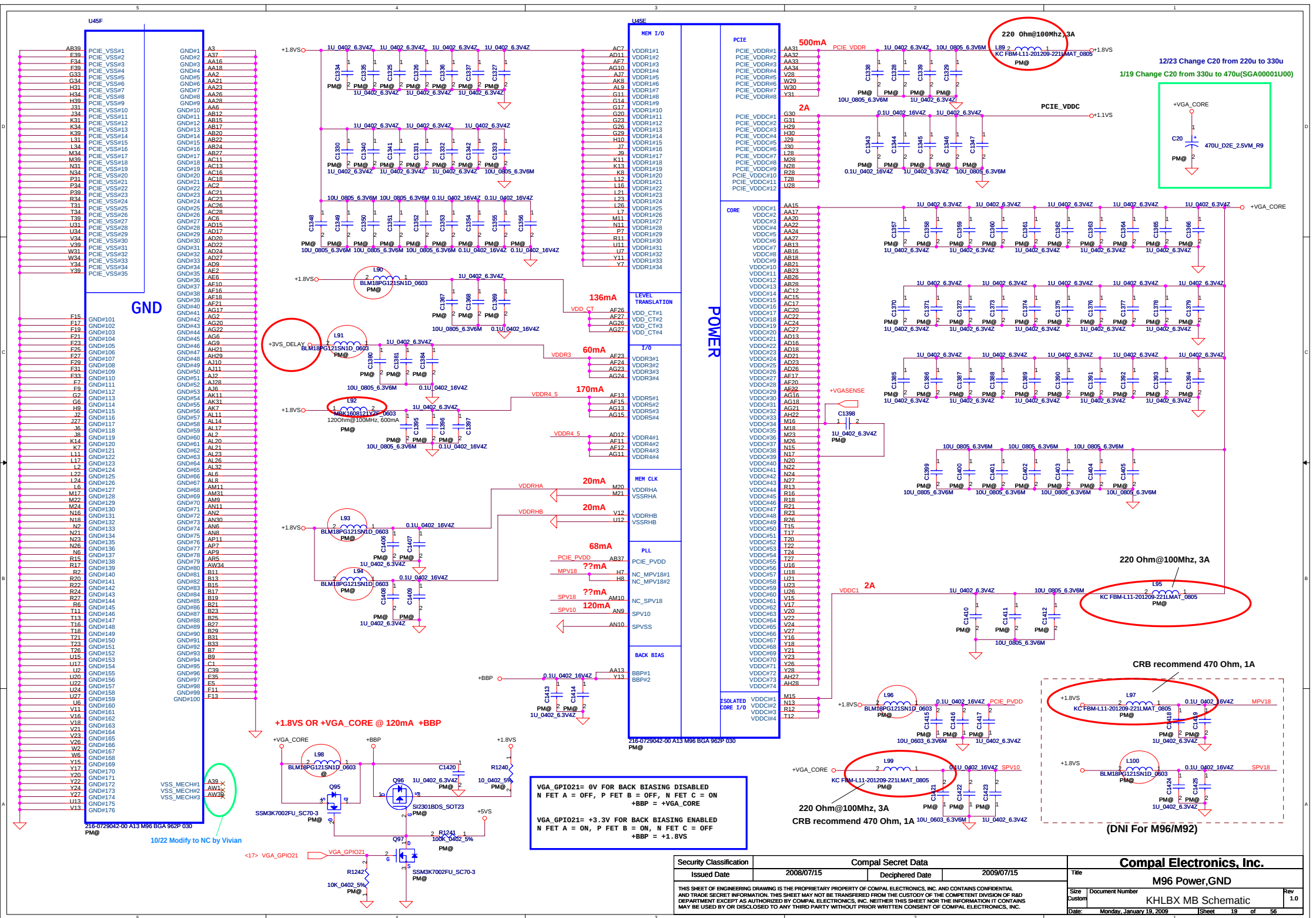


Location	MEM_ID0 (R1179)	MEM_ID1 (R1181)	MEM_ID2 (R1183)	MEM_ID3 (R1184)
VRAM	0	0	0	0
Samsung	0	0	0	0
Qimonda	1	0	0	0



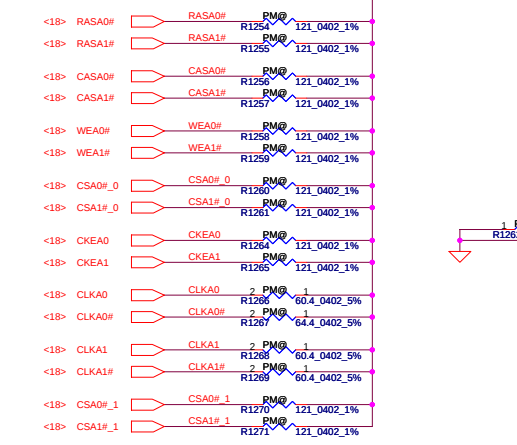


Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		M96 Memory	
2008/07/15		2009/07/15		KHLBX MB Schematic	
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		Sheet		18	56

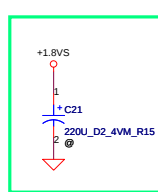
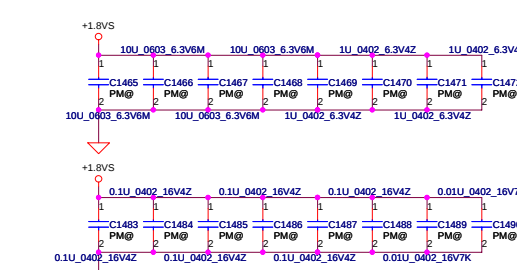


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	M96 Power,GND
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				KHLBX MB Schematic	
				Date:	Monday, January 19, 2009
				Sheet	19 of 56

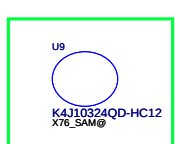
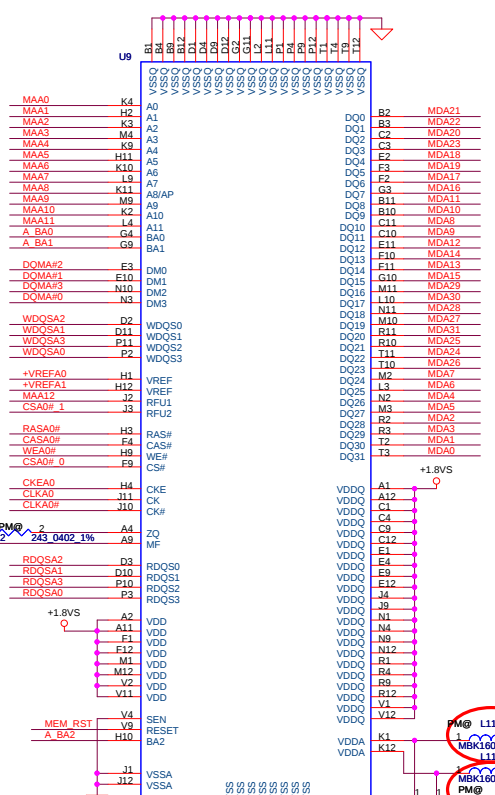
<18> MAA[0..12] MAA[0..12]
<18> WDQSA[0..7] WDQSA[0..7]
<18> RDQSA[0..7] RDQSA[0..7]
<18> DQMA[0..7] DQMA[0..7]
<18> MDA[0..63] MDA[0..63]
<18> A_BA[0..2] A_BA[0..2]
<18,22> MEM_RST MEM_RST



R121_0402_1% CIS download



10/22 Add C1554 and close to U8 and U9



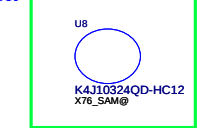
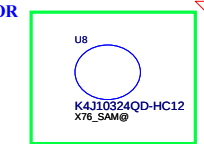
CRB use BLM15BD1231SN1 P/N :SM010009U9L 120Ohm@100MHz, 300mA

BGA 84 ADR/CMND MAPPING

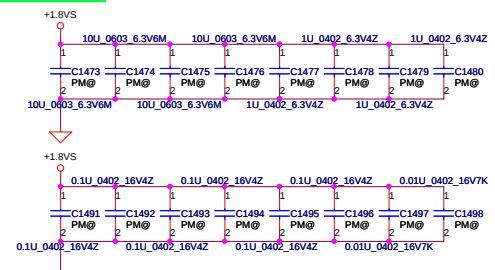
DATA Bus	
Address	0..31 32..63
CMD0	A4
CMD1	RAS*
CMD2	A5
CMD3	BA1
CMD4	A6
CMD5	A9
CMD6	
CMD7	CS1* CKE
CMD8	CS0* CAS*
CMD9	A11
CMD10	CAS*
CMD11	WE*
CMD12	BA0
CMD13	A1
CMD14	A12
CMD15	RST/ODT
CMD16	A7
CMD17	A10
CMD18	CKE WE#
CMD19	A0
CMD20	A9
CMD21	A6
CMD22	A2
CMD23	A8
CMD24	A3
CMD25	A1
CMD26	A13
CMD27	BA2
CMD28	RFU0
CMD29	RFU1
CMD30	RFU2

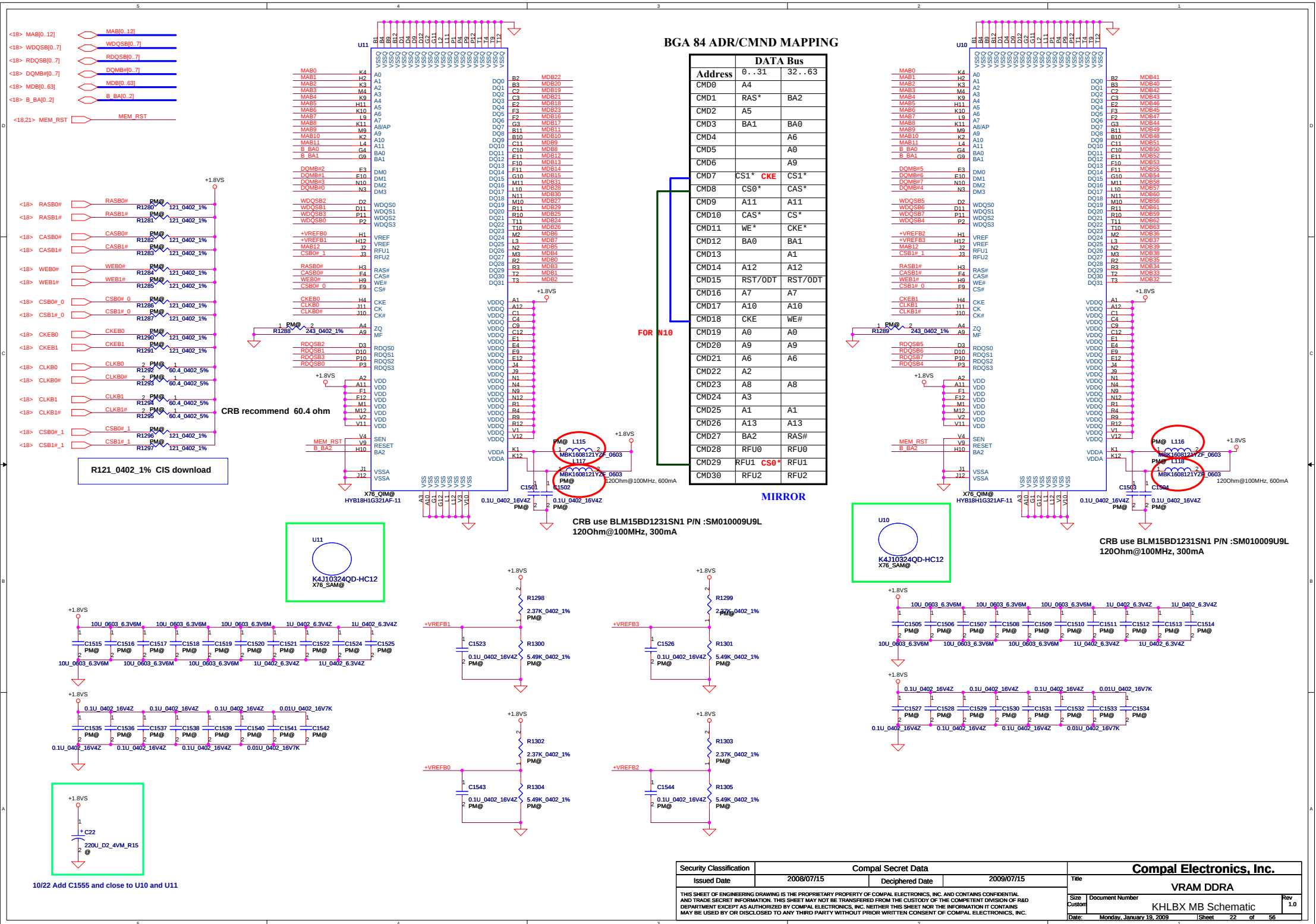
FOR N10

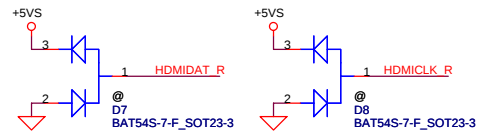
MIRROR



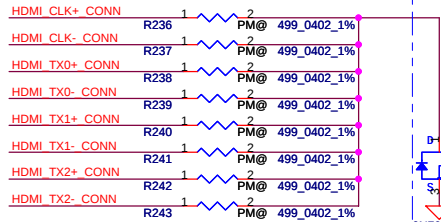
CRB use BLM15BD1231SN1 P/N :SM010009U9L 120Ohm@100MHz, 300mA



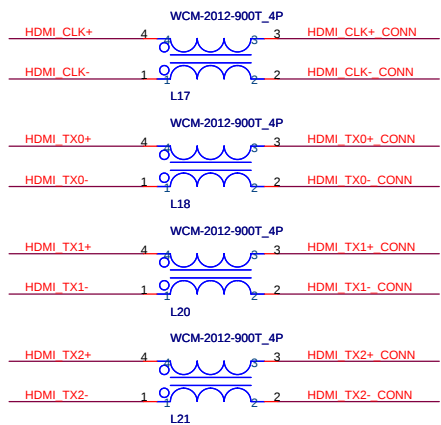




TMDs pull down (500ohm) resistors G9x only

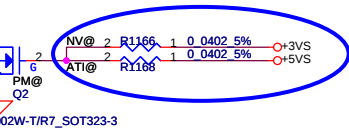


NEAR CONNECT

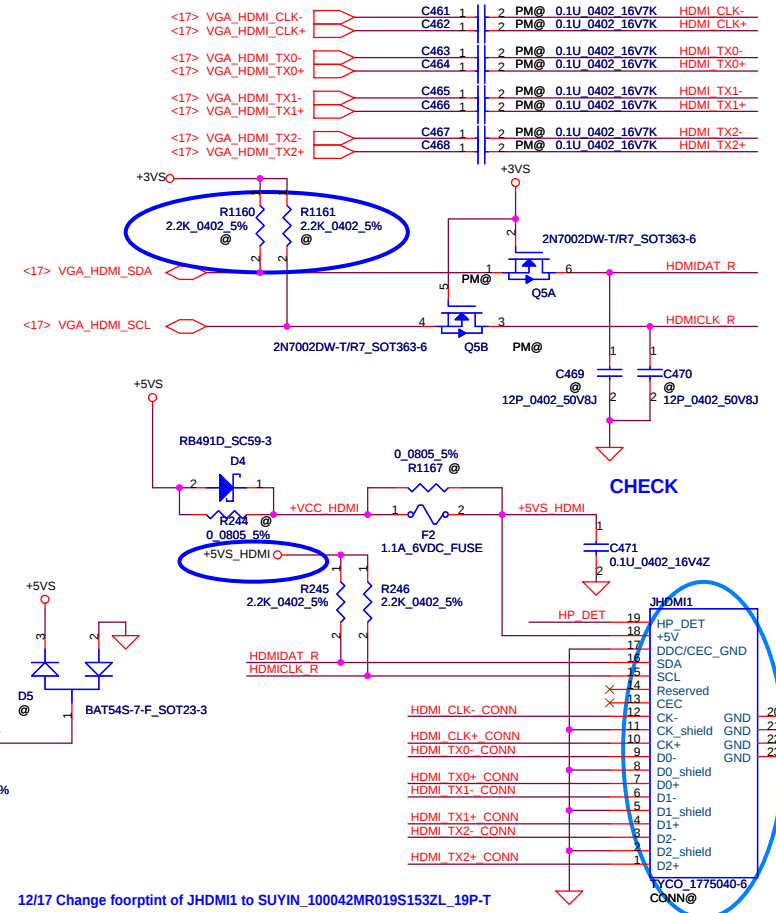
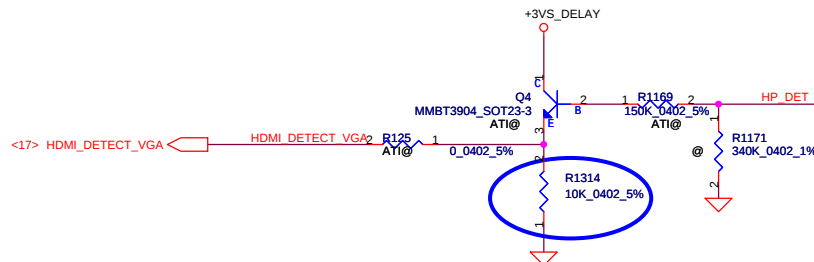


HDMI CLK+	R251	1	2	0.0402_5%	HDMI CLK+ CONN
HDMI CLK-	R252	1	2	0.0402_5%	HDMI CLK- CONN
HDMI TX0+	R253	1	2	0.0402_5%	HDMI TX0+ CONN
HDMI TX0-	R254	1	2	0.0402_5%	HDMI TX0- CONN
HDMI TX1+	R255	1	2	0.0402_5%	HDMI TX1+ CONN
HDMI TX1-	R256	1	2	0.0402_5%	HDMI TX1- CONN
HDMI TX2+	R257	1	2	0.0402_5%	HDMI TX2+ CONN
HDMI TX2-	R258	1	2	0.0402_5%	HDMI TX2- CONN

9/14 Modify for
UMA used



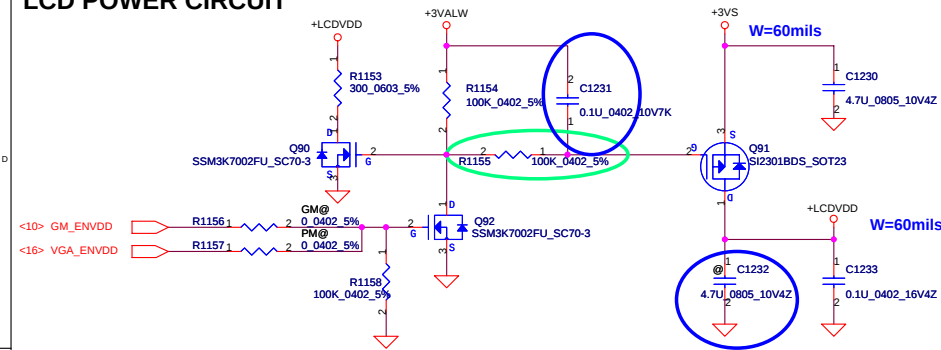
9/14 Reserve for VGA
used;check pin name



12/17 Change footprint of JHDMI1 to SUYIN_100042MR019S153ZL_19P-T

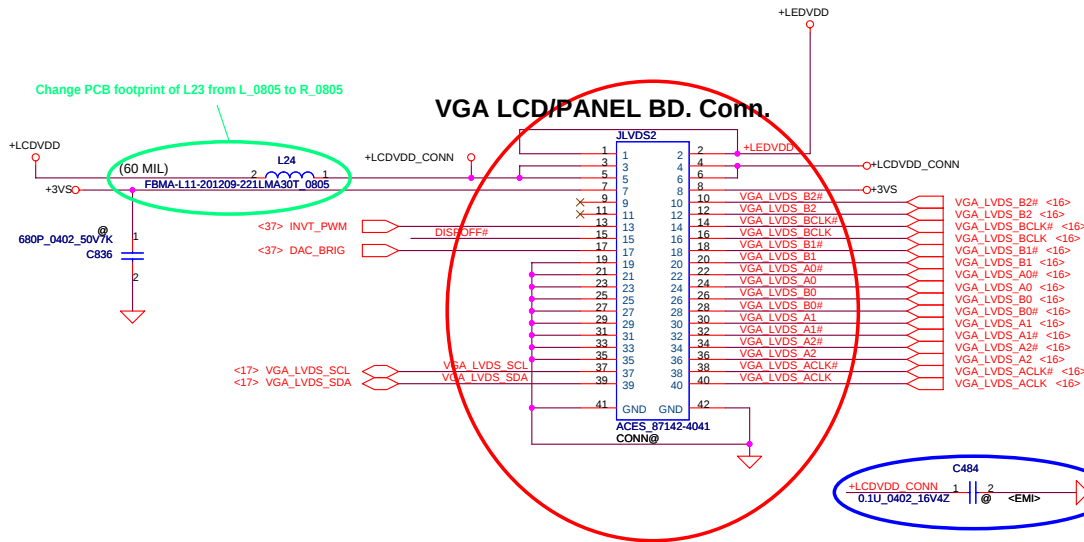
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Level Shifter_PS8101T	
2008/07/15		2009/07/15		KHLBX MB Schematic	
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		Custom		1.0	
Date: Monday, January 19, 2009		Sheet		24 of 56	

LCD POWER CIRCUIT

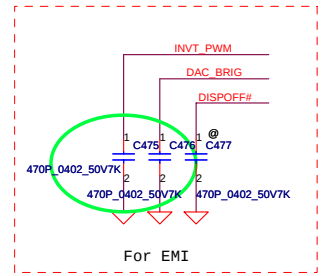
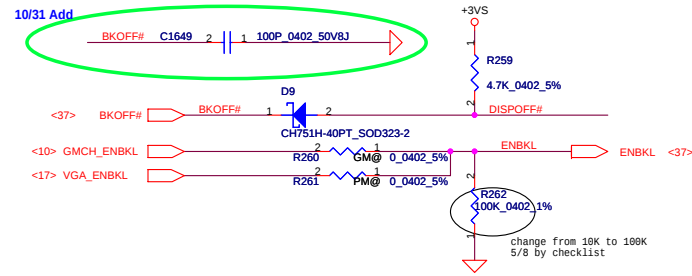


Change PCB footprint of L22 from L_0805 to R_0805

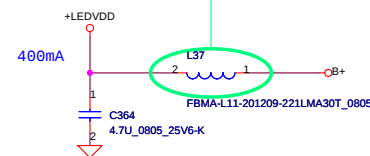
VGA LCD/PANEL BD. Conn.



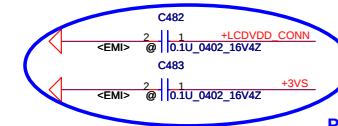
10/31 Add



Change PCB footprint of L37 from L_0805 to R_0805



Plac C484 close to JLVS2



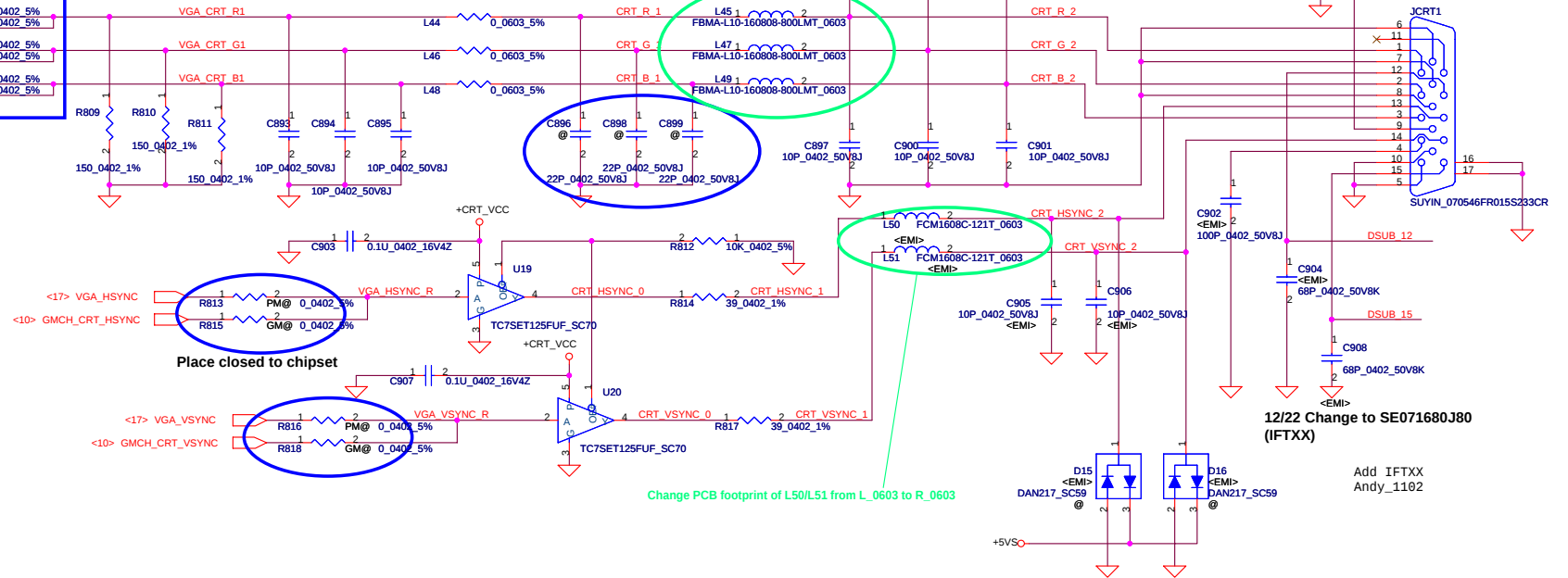
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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				KHLBX MB Schematic	
				Date: Monday, January 19, 2009	Rev 1.0
				Sheet 25	of 56

CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p
12/15 Modified. Note L26-L30 are 0 Ohm resistors (IFTXX)

Place closed to chipset

<17> VGA_CRT_R	R803	1	2	PM@	0.0402_5%
<10> GMCH_CRT_R	R804	1	2	GM@	0.0402_5%
<17> VGA_CRT_G	R805	1	2	PM@	0.0402_5%
<10> GMCH_CRT_G	R806	1	2	GM@	0.0402_5%
<17> VGA_CRT_B	R807	1	2	PM@	0.0402_5%
<10> GMCH_CRT_B	R808	1	2	GM@	0.0402_5%

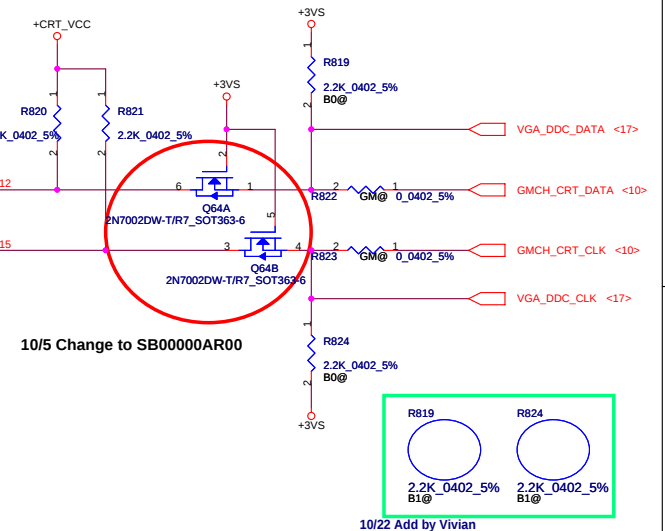


<17> VGA_HSYNC
<10> GMCH_CRT_HSYNC

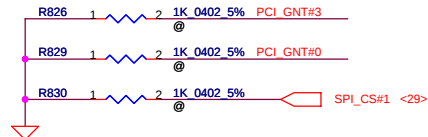
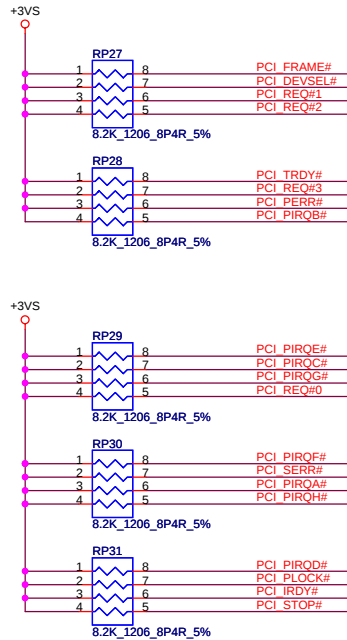
Place closed to chipset

<17> VGA_VSYNC
<10> GMCH_CRT_VSYNC

Change PCB footprint of L50/L51 from L_0603 to R_0603



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						Size B	Document Number			Rev 1.0	
						KHLBX MB Schematic					
Date: Monday, January 19, 2009						Sheet 26 of 56					

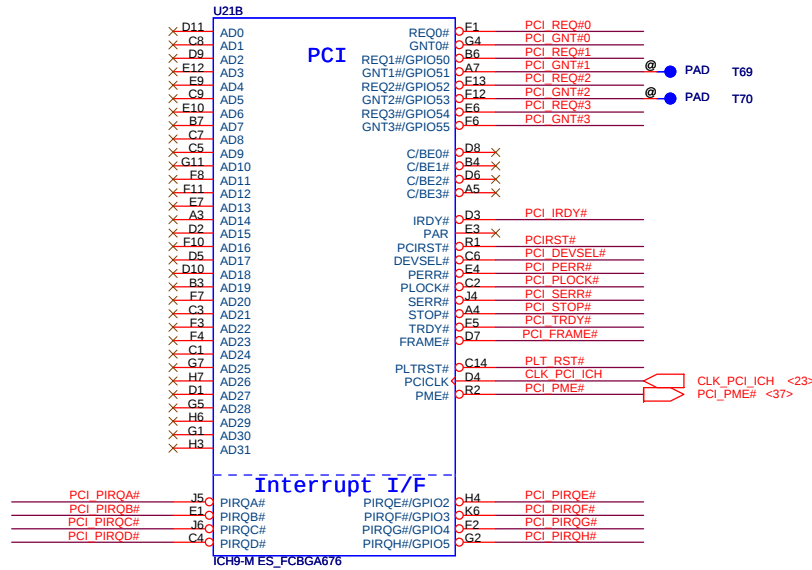


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

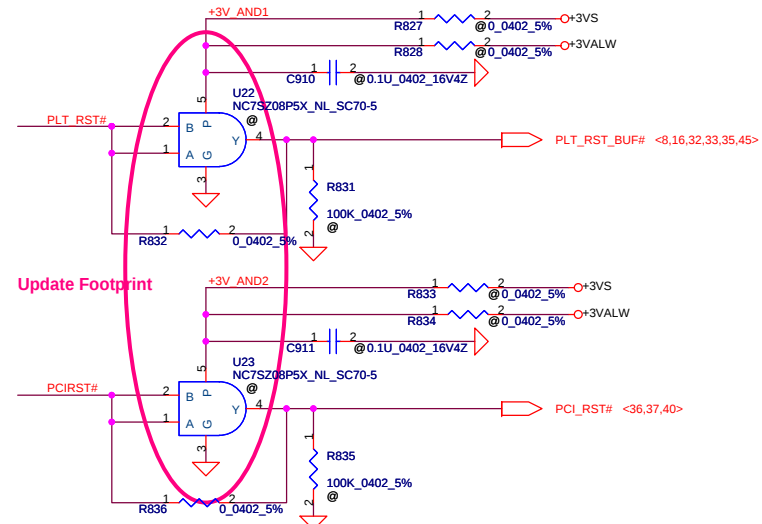
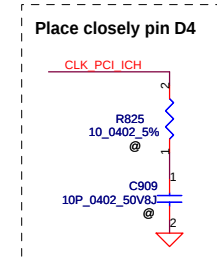
CRB: GNT#0 and SPI_CS#1 have a weak internal pull up

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

9/18 Change U21 from SA00002JH00 to SA00002JH80



DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

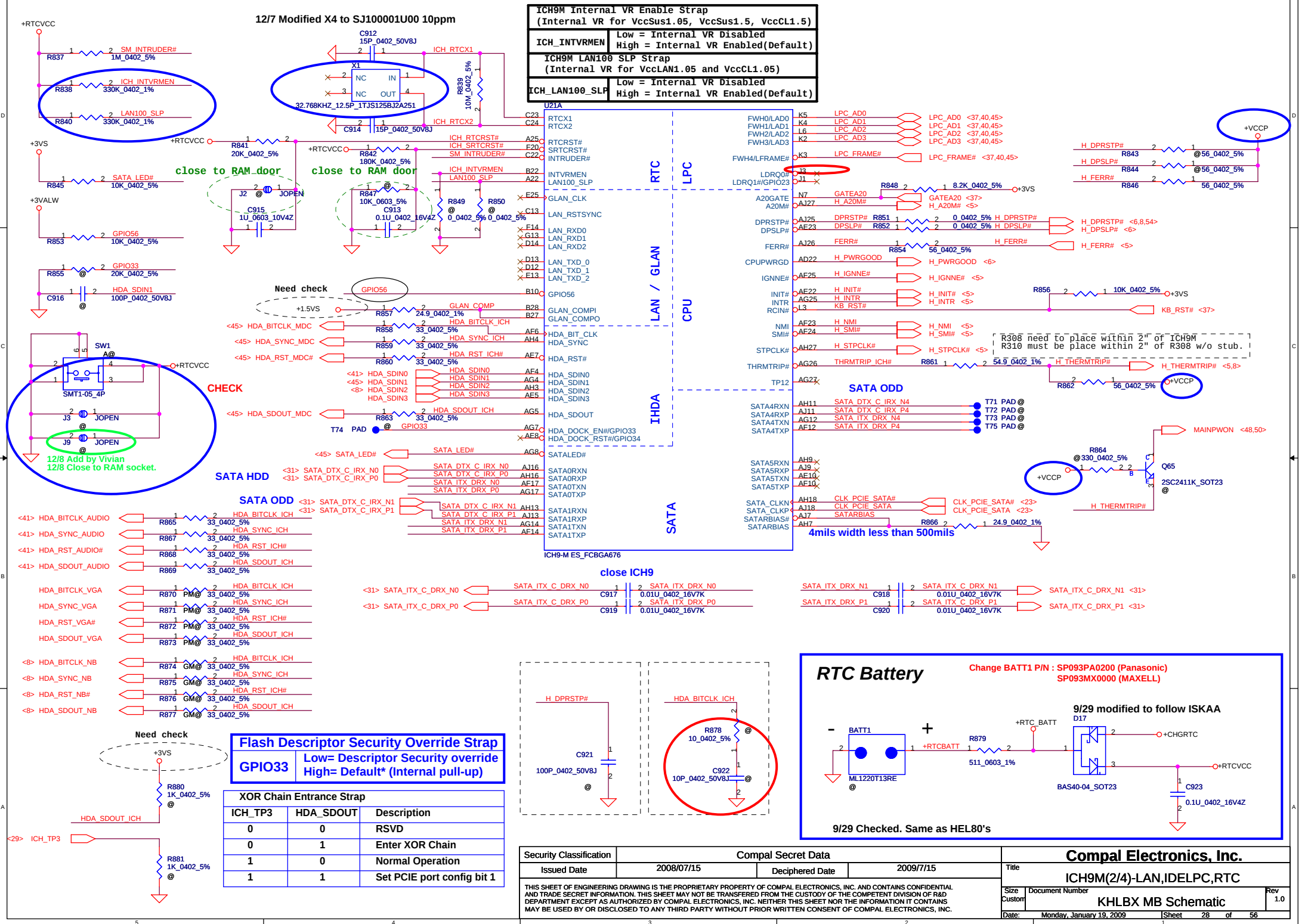


Security Classification				Compal Secret Data			Compal Electronics, Inc.		
Issued Date		2008/07/15		Deciphered Date		2009/07/15		Title	
								ICH9M(1/4)-PCI	
								KHLBX MB Schematic	
								Rev 1.0	
								Date: Monday, January 19, 2009	
								Sheet 27 of 56	

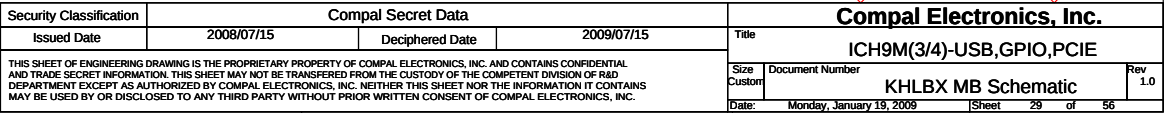
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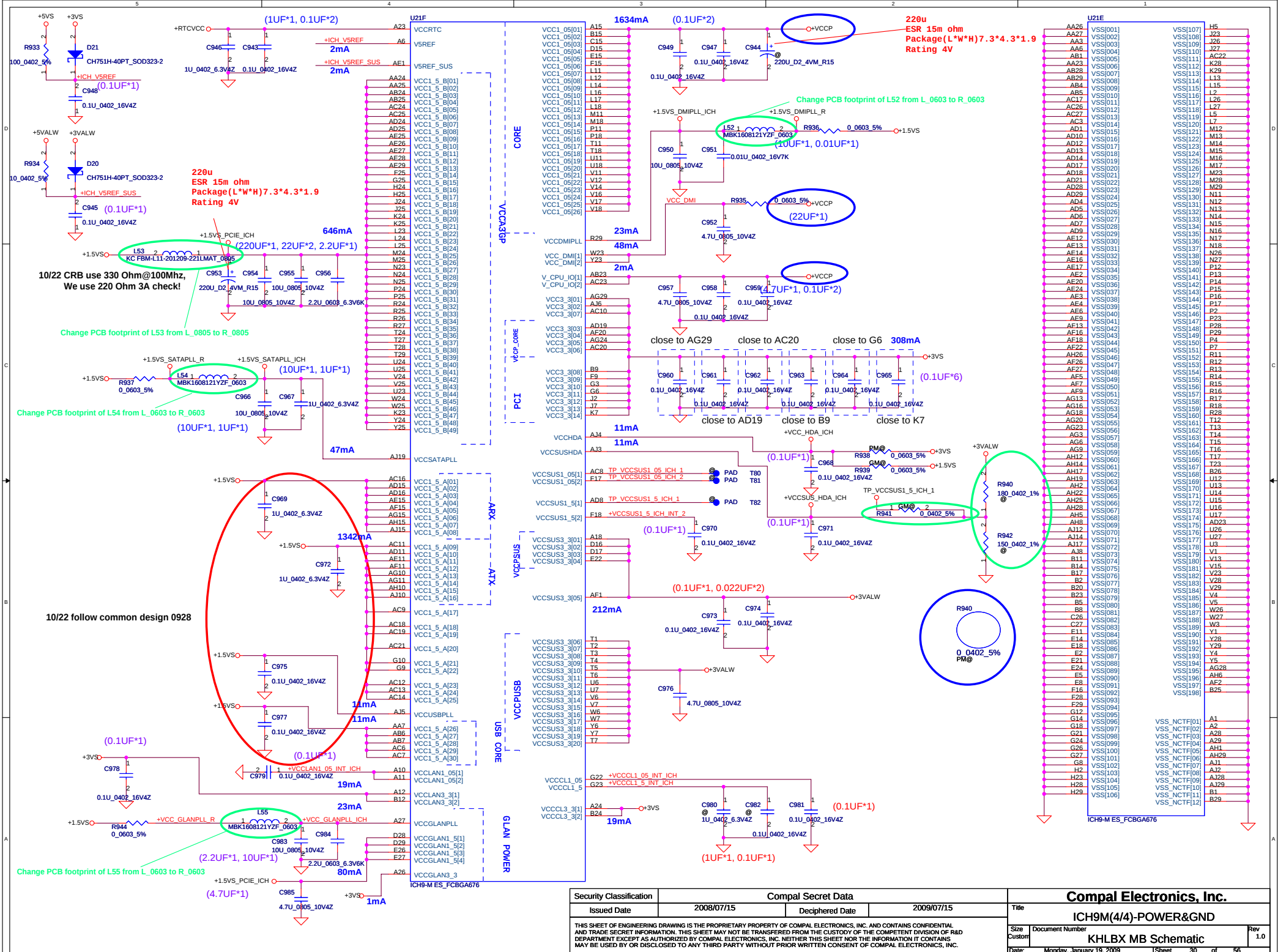
12/7 Modified X4 to SJ100001U00 10ppm

ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH9M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



Security Classification		Compal Secret Data		Title	
Issued Date	2008/07/15	Deciphered Date	2009/7/15	ICH9M(2/4)-LAN, IDELPC, RTC	
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				Custom	KHLBX MB Schematic
				Date	Monday, January 19, 2009
				Sheet	28 of 56
				Rev	1.0

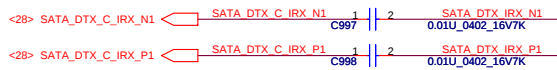
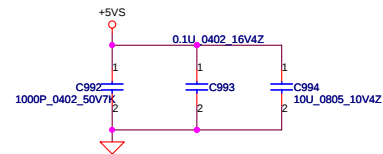




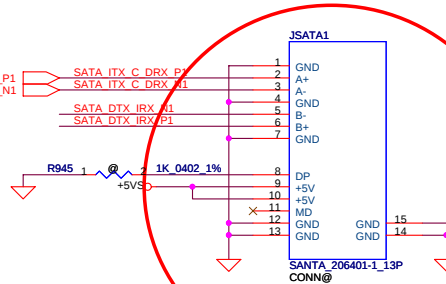
Security Classification		Compal Secret Data	
Issued Date	2008/07/15	Deciphered Date	2009/07/15
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Compal Electronics, Inc.			
ICH9M(4/4)-POWER&GND			
Title	Document Number	Rev	1.0
KHLBX MB Schematic			
Date	Monday, January 19, 2009	Sheet	30 of 56

SATA ODD Conn.



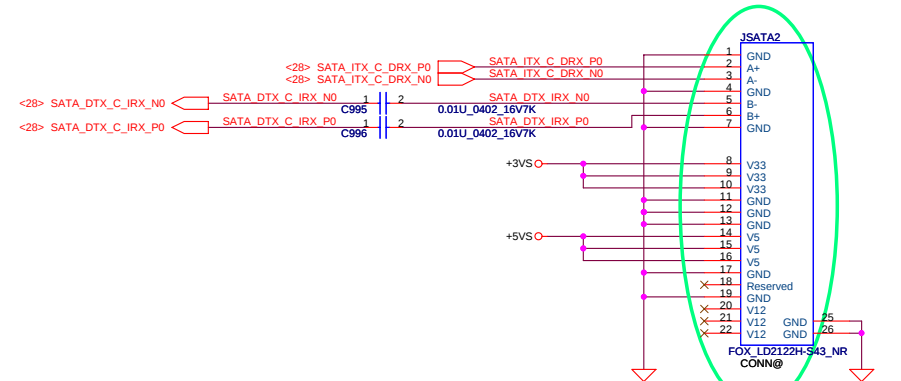
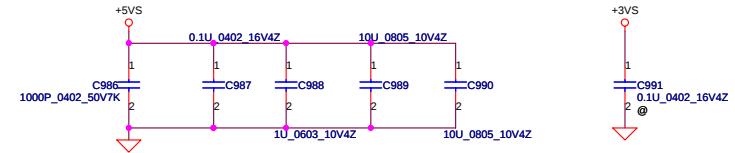
Copy JAL90 Symbol



Change ODD connector from OCTEK_SLS-13SB1G to SANTA_206401-1_13P

Need check layout !!

SATA HDD Conn.

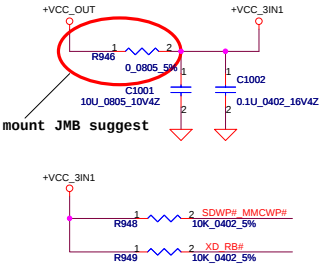


9/4 Change symbol follow KSWXX by Vivian

(NEW)

Change Library
Update Symbol
SP01000G800
FOX_LD2122H-S43_NR
Manually update pin number

Security Classification		Compal Secret Data		Title	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	HDD & ODD Connector	
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				KHLBX MB Schematic	
				Date: Monday, January 19, 2009	Sheet 31 of 56
				Rev 1.0	



reserved power circuit

20mil

0.1uF 0402 16V4Z

+1.8VS_CR

1 2 3 4

1000P_0402_50V7K

0.1uF 0402 16V4Z

+1.8VS_CRR

1000P_0402_50V7K

40mil

+1.8VS_CR

10/23 Add by Vivian

W=40mils

CR_ON#

0.1uF_0402_16V4Z

10K 0.063_5%

Q6 Si2301BDS_SOT23

10K 0.063_5%

1uF_0603_10V4Z

0.063_5%

W=40mils

3V3_CR

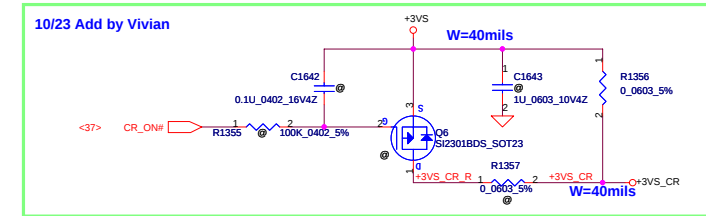
0.063_5%

3V3_CR

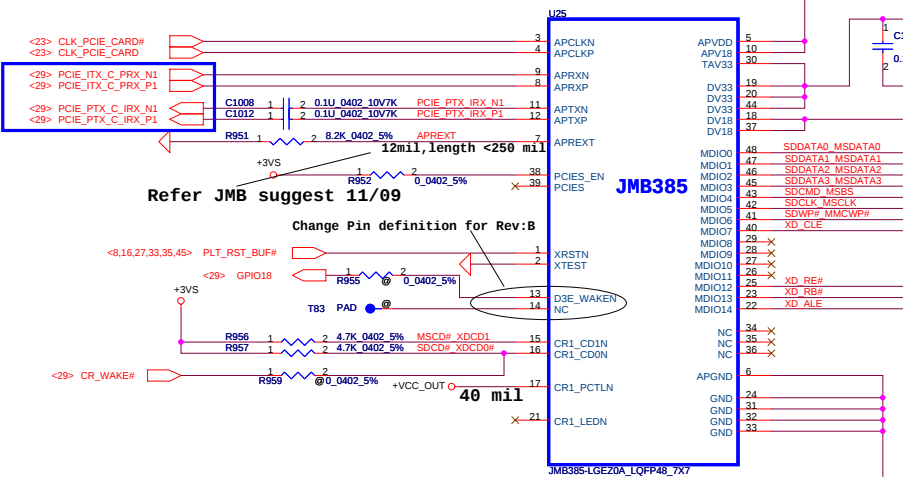
0.063_5%

3V3_CR

0.063_5%



SD, MMC, MS multi-function pin define		
MDIO PIN Name	SD/MMC Card PIN Name	MS Card PIN Name
MDIO00	SD1_DAT0	MS1_DAT0
MDIO01	SD1_DAT1	MS1_DAT1
MDIO02	SD1_DAT2	MS1_DAT2
MDIO03	SD1_DAT3	MS1_DAT3
MDIO04	SD1_CMD	MS1_BS
MDIO05	SD1_CLK	MS1_CLK
MDIO06	SD1_WP	
MDIO07		
MDIO08	MMC_DAT4	MS1_DAT4
MDIO09	MMC_DAT5	MS1_DAT5
MDIO10	MMC_DAT6	MS1_DAT6
MDIO11	MMC_DAT7	MS1_DAT7
MDIO12		
MDIO13		
MDIO14		
CR1_LEDN	SD1_LED#	MS1_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#
CR1_CD0	SD1_CD#	
CR1_CD1		MS1_CD#



D22

C1015

270P_0402_50V7K

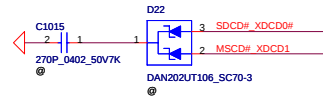
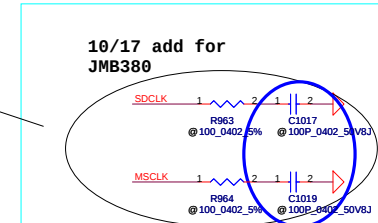
3

2

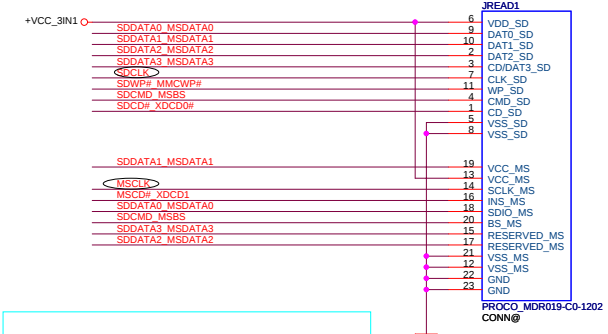
SDCD#_XDCD0#

MSCD#_XDCD1

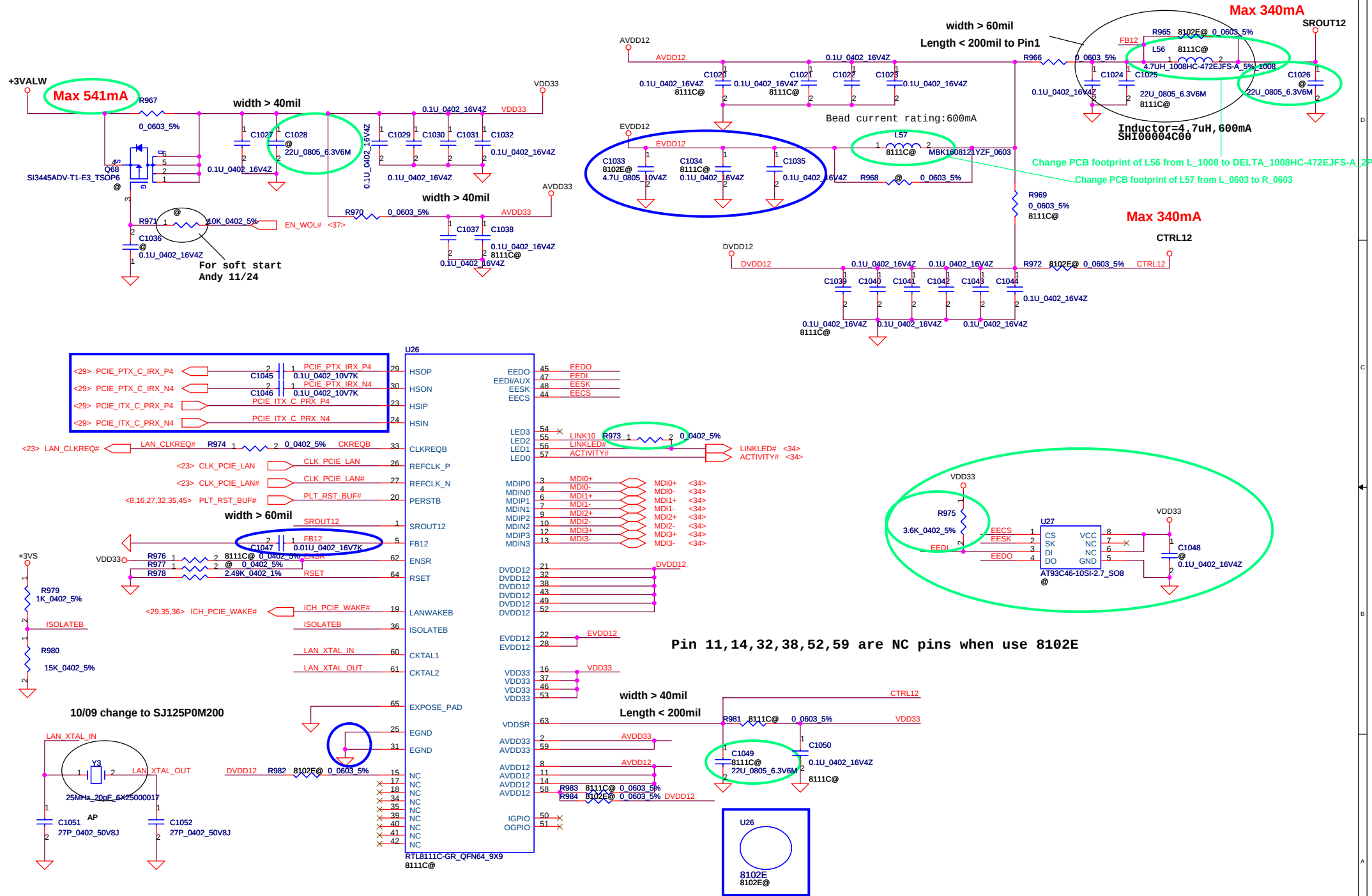
DAN202UT106_SC70-3

[illegible]

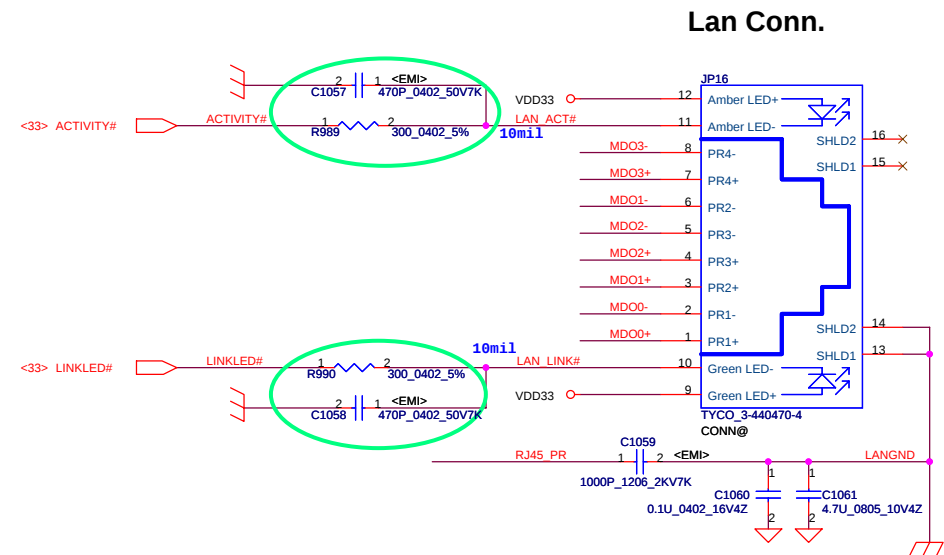
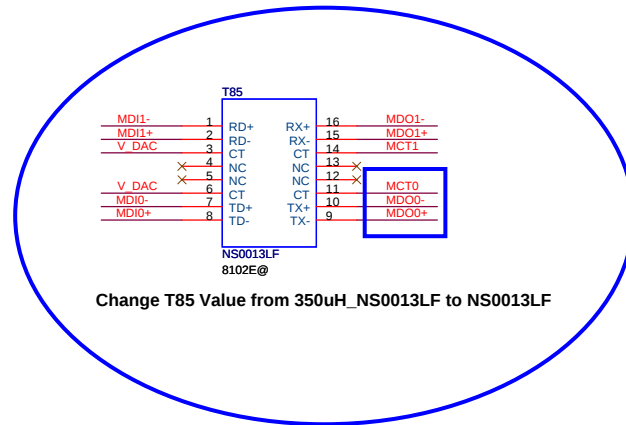
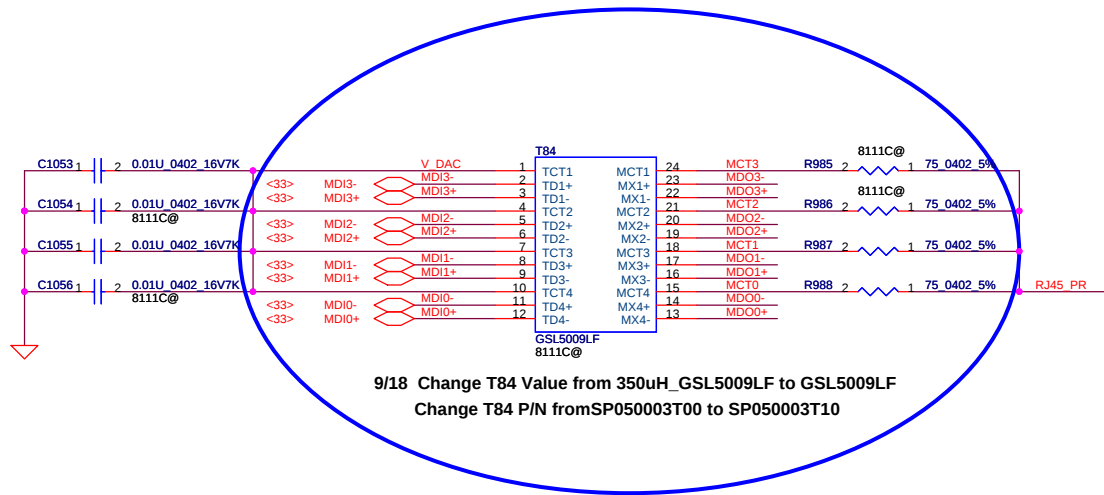
3 in 1 Card Reader



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				Custom	KHLBX MB Schematic	1.0
				Date:	Monday, January 19, 2009	Sheet

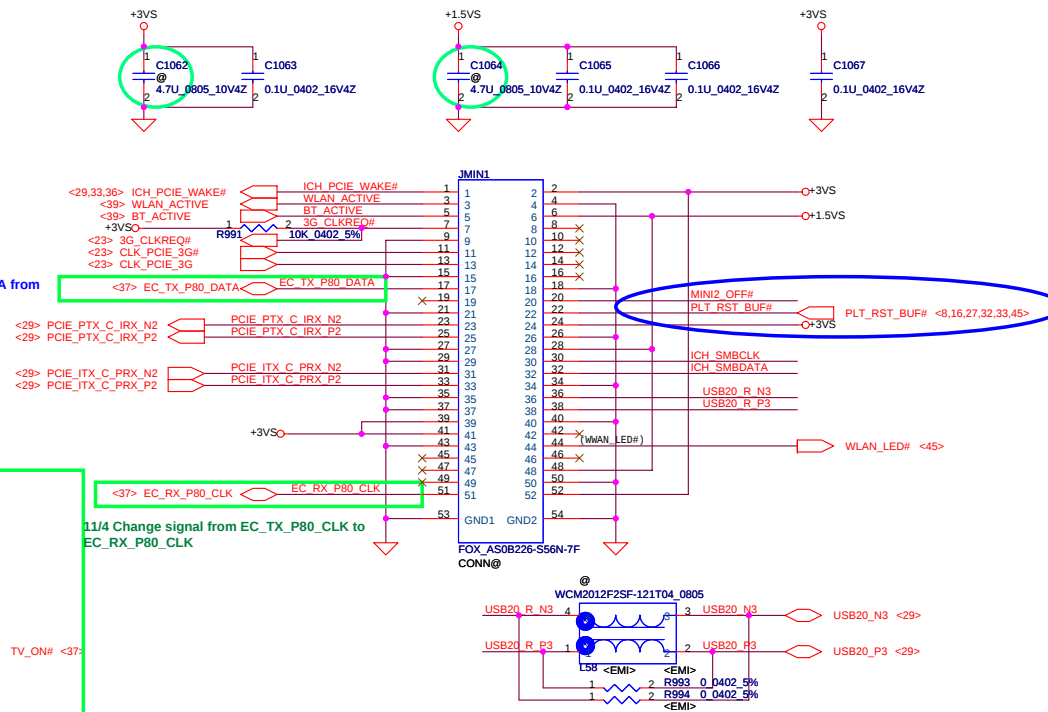
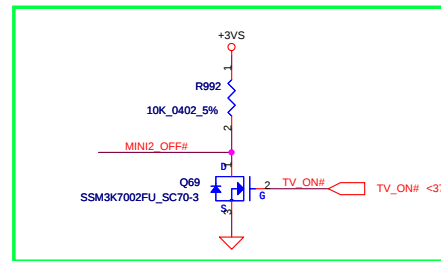
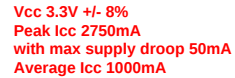


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Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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Size	Document Number	KHLBX MB Schematic		Rev	1.0
Date:	Monday, January 19, 2009	Sheet	33	of	56

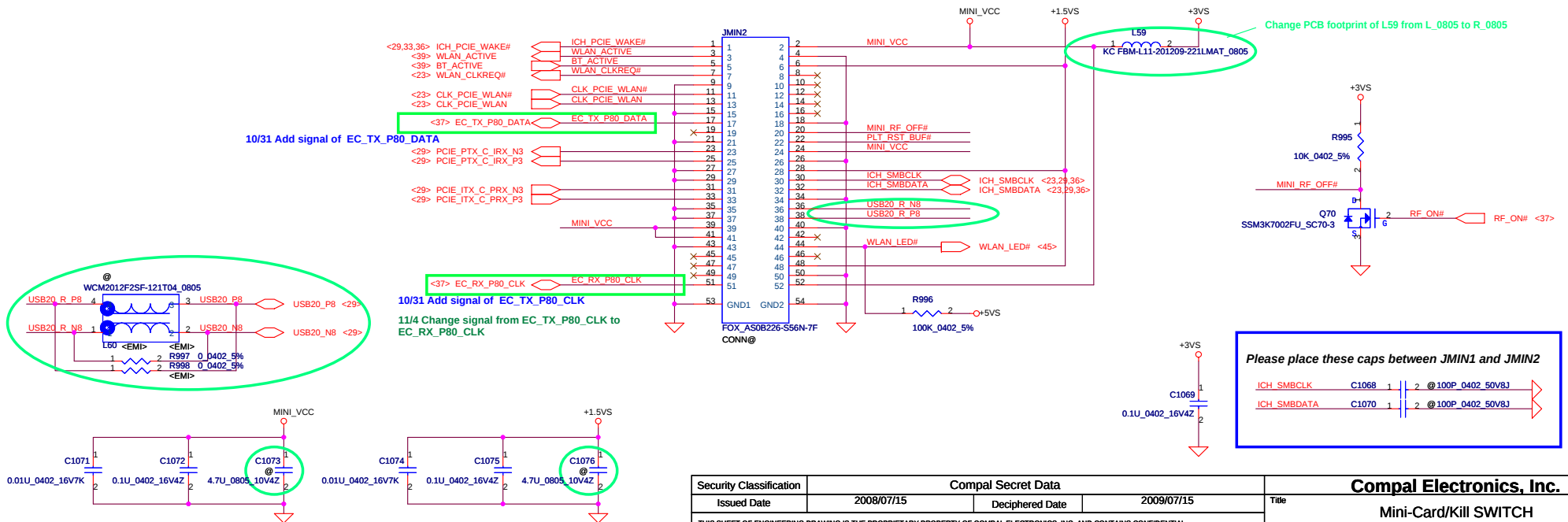


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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Size	Document Number	KHLBX MB Schematic		Rev	1.0
Date:	Monday, January 19, 2009	Sheet	34	of	56

Mini-Express Card for TV Tuner



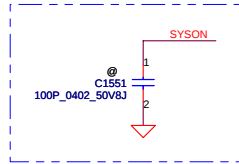
Mini-Express Card for WLAN



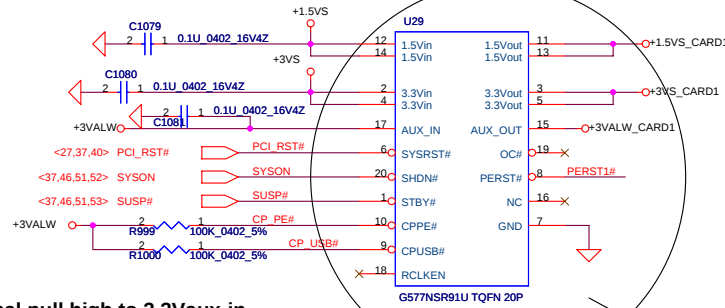
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Issued Date		2008/07/15		Deciphered Date		2009/07/15		
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				Mini-Card/Kill SWITCH				
				Size Custom	Document Number			Rev 1.0
				KHLBX MB Schematic				
				Date:		Monday, January 19, 2009		Sheet 35 of 56

New Card Power Switch

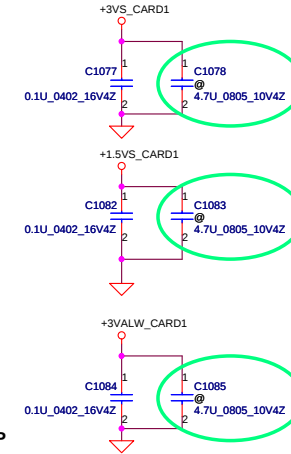
New Card



internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

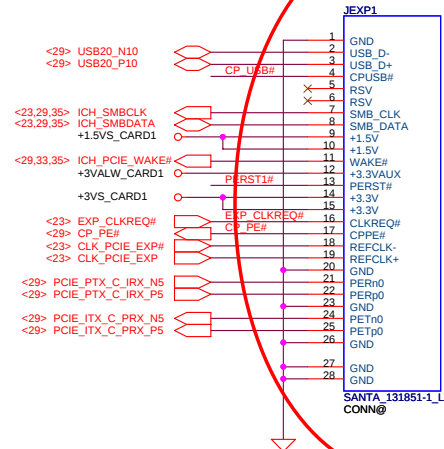


10/20 Change to value to G577NSR91U TQFN 20P



New Card Socket (Left/TOP)

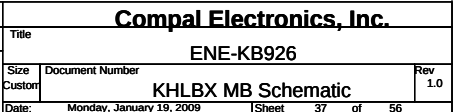
Copied from HAL10



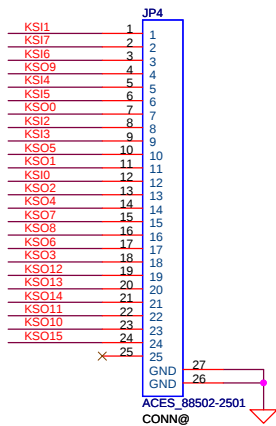
Need checking layout !!

Change connector from SANTA_130810-1 to SANTA_13185-1_LT

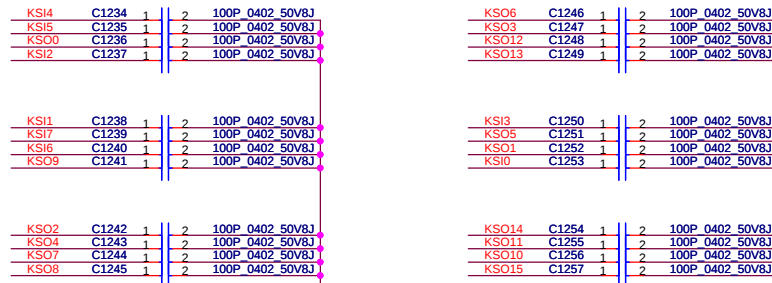
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/07/15	Deciphered Date	2009/07/15	Title	
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				Size B	Document Number
				KHLBX MB Schematic	
Date: Monday, January 19, 2009				Sheet	36 of 56



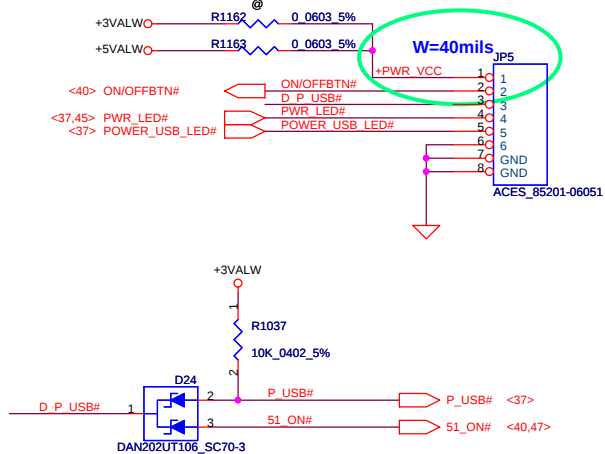
INT_KBD Conn.



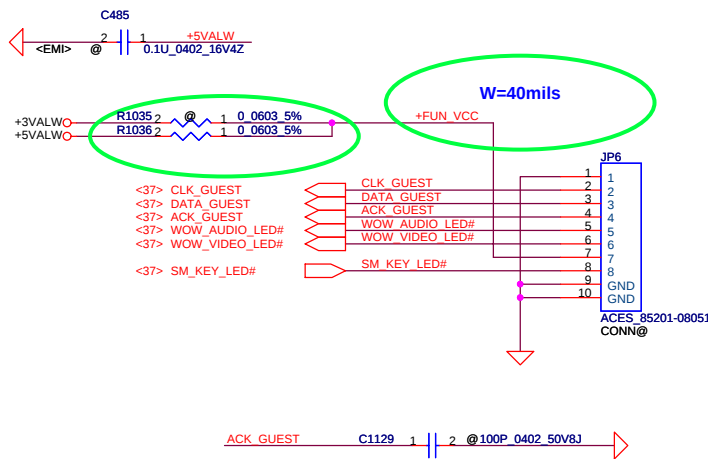
KSIO[0..7] <37>
KSO[0..15] <37>



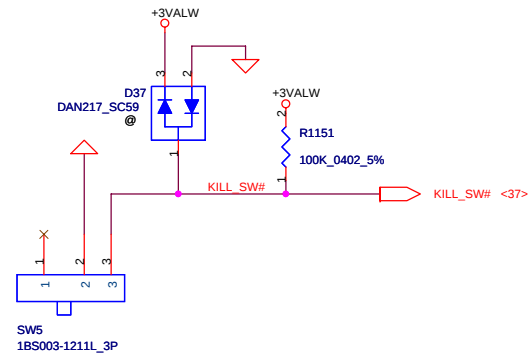
Power USB Board Conn



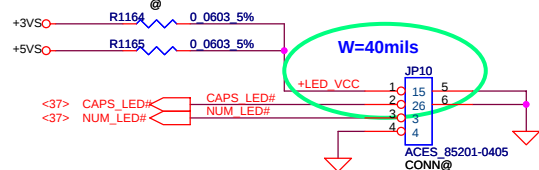
Fun conn



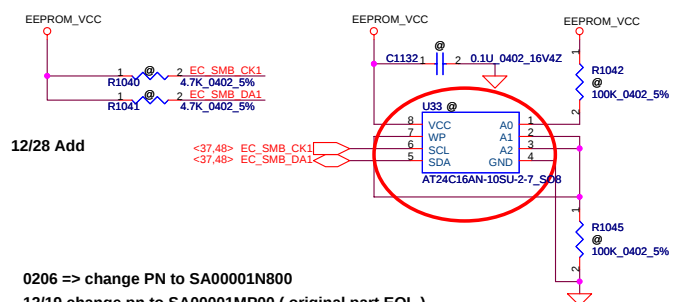
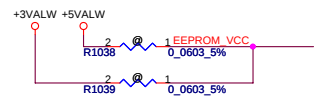
Kill SWITCH



LED Board Conn

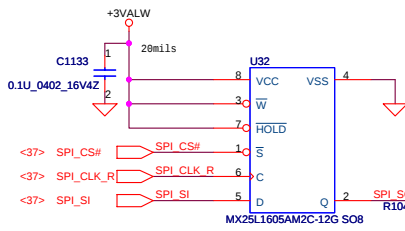


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Size B	Document Number	KHLBX MB Schematic		Rev 1.0	
Date:	Monday, January 19, 2009	Sheet	38	of	56



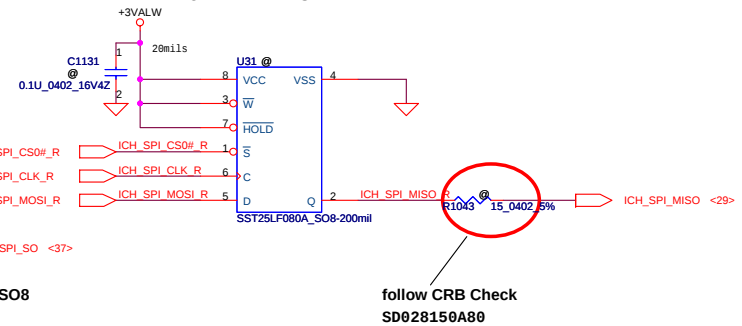
0206 ==> change PN to SA00001N800
 12/19 change pn to SA00001MP00 (original part EOL)
 12/25 change back to SA024160140 (Samples can not on time)

16M SPI ROM For EC+BIOS+VBIOS



10/20 Change value of U32 to MX25L1605AM2C-12G SO8
 12/15 change from 15 to 0 ohm'

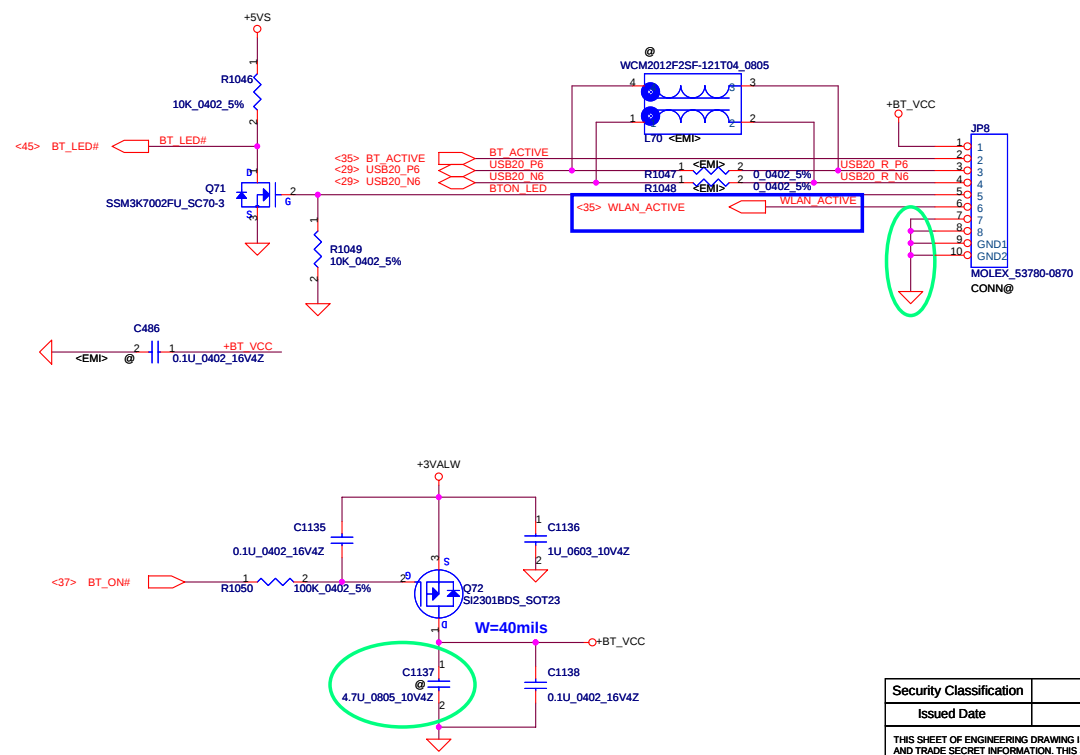
8M SPI ROM For iTPM+HDCP



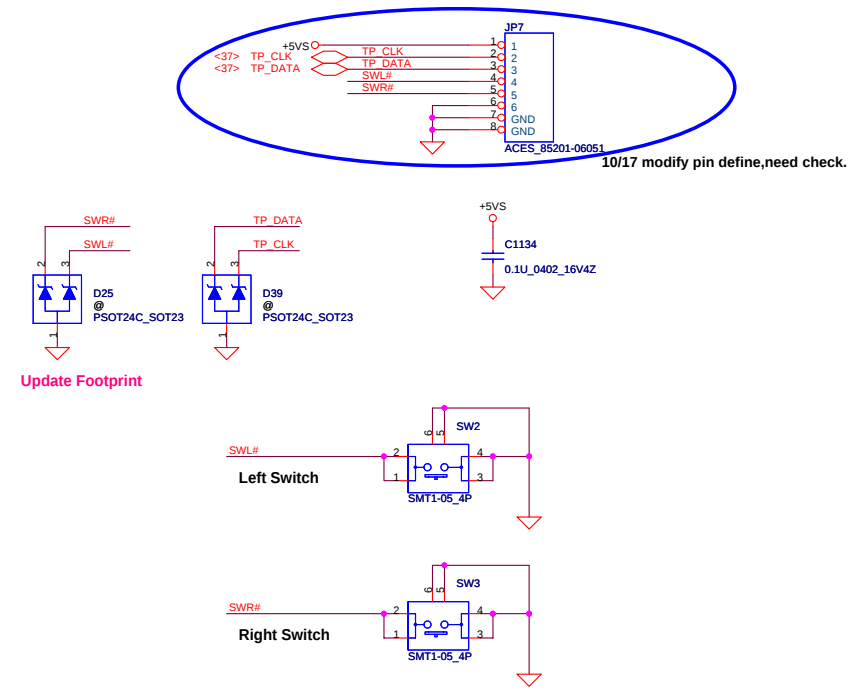
follow CRB Check
SD028150A80

Bluetooth Conn.

Need to check BT pin definition again!
 9/20 modified this block

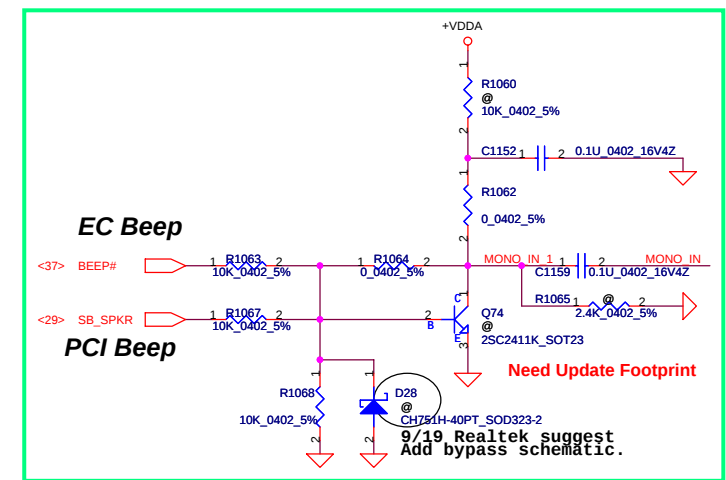
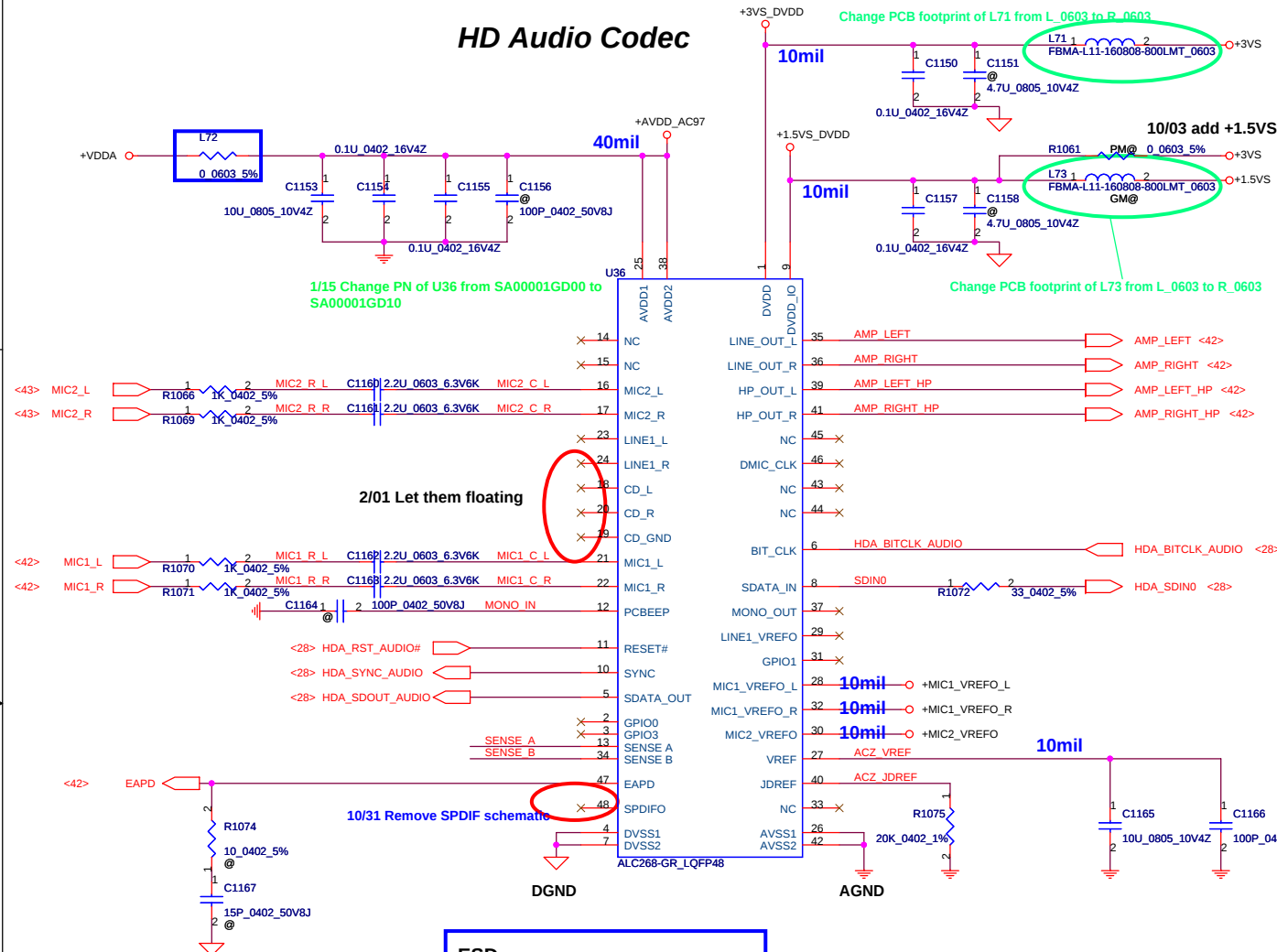


To TP/B Conn.



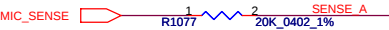
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2008/07/15				Title			
Deciphered Date				2009/07/15				BIOS, TP & BT Connector			
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								KHLBX MB Schematic			
								Date: Monday, January 19, 2009			
								Sheet 39 of 56			

HD Audio Codec

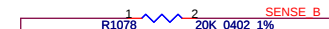


Sense Pin	Impedance	Codec Signals	Funnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE OUT
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE OUT

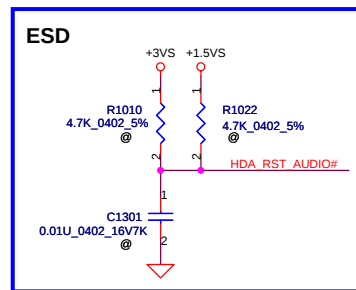
SENSE FOR Ext. Mic.



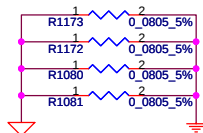
SENSE FOR Solo Int. Mic.



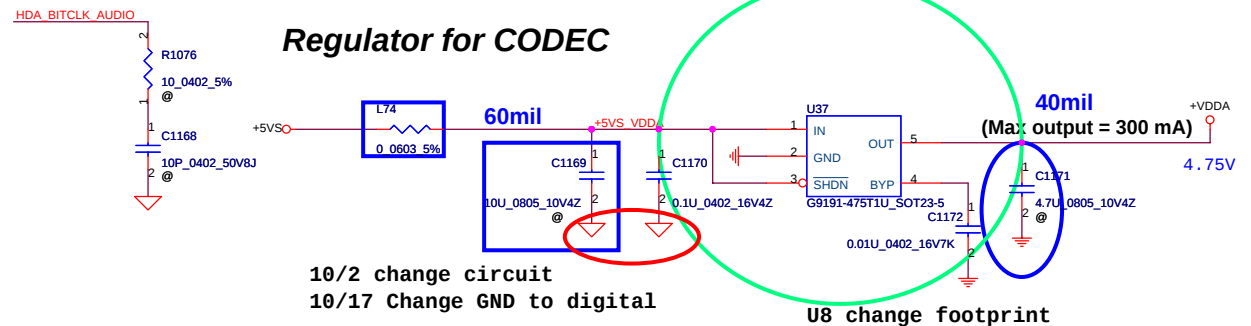
SENSE FOR HP



Moat Bridge



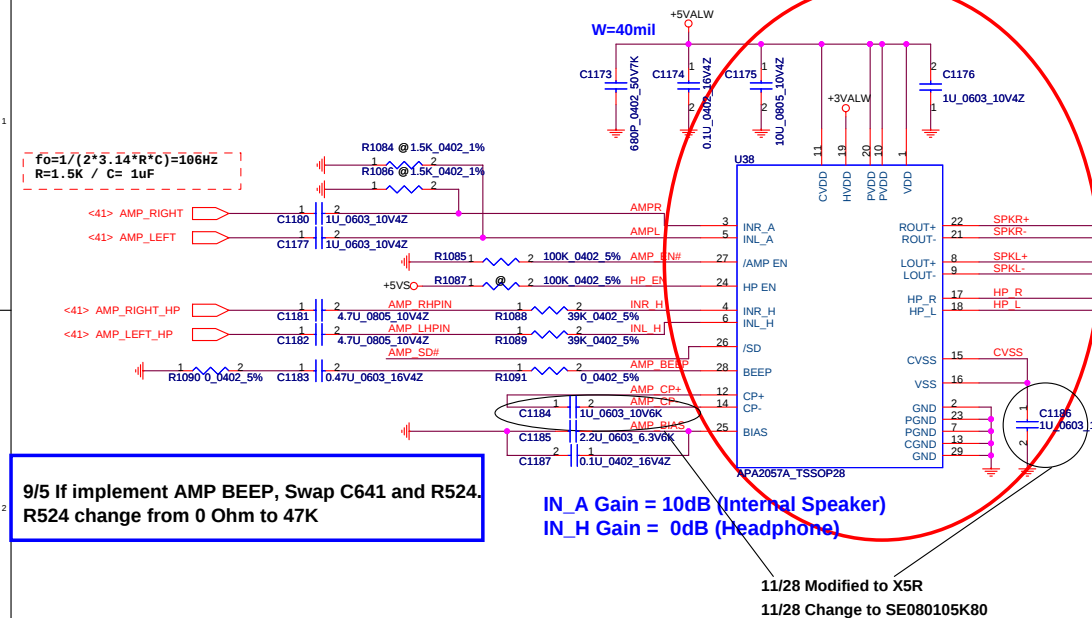
Regulator for CODEC



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				Date:	Monday, January 19, 2009	Sheet 41 of 56

APA2057 SPK/HP Amplifier

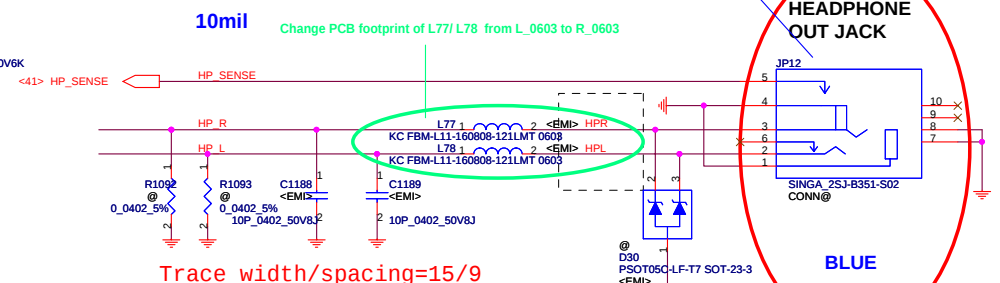
10/2 U6 APA2057A P/N:SA00001QD00



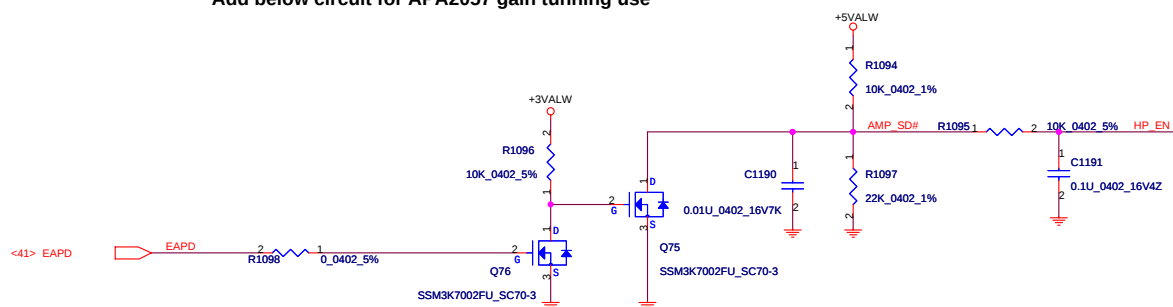
Trace width/spacing/other=8/6/50

9/3 Change PCB footprint of JP12/JP13 from FOX JA6033L-B5S3-7F 6P to SINGA 2SJ-B351-S01 6P

12/8 Change value conn location of JP13 and JP12.



Add below circuit for APA2057 gain tuning use



Gain= 10dB

Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82

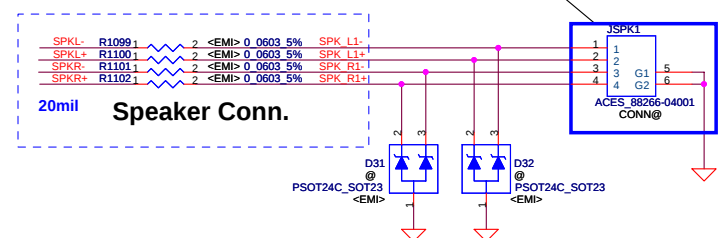
+5VALW assume equal 5.1V
10 dB ---> $5.1 \times 220 / 320 = 3.5$

10/30 add

SPK_L1-	C1654	2	1	100P_0402_50V8J
SPK_L1+	C1653	2	1	100P_0402_50V8J
SPK_R1-	C1655	2	1	100P_0402_50V8J

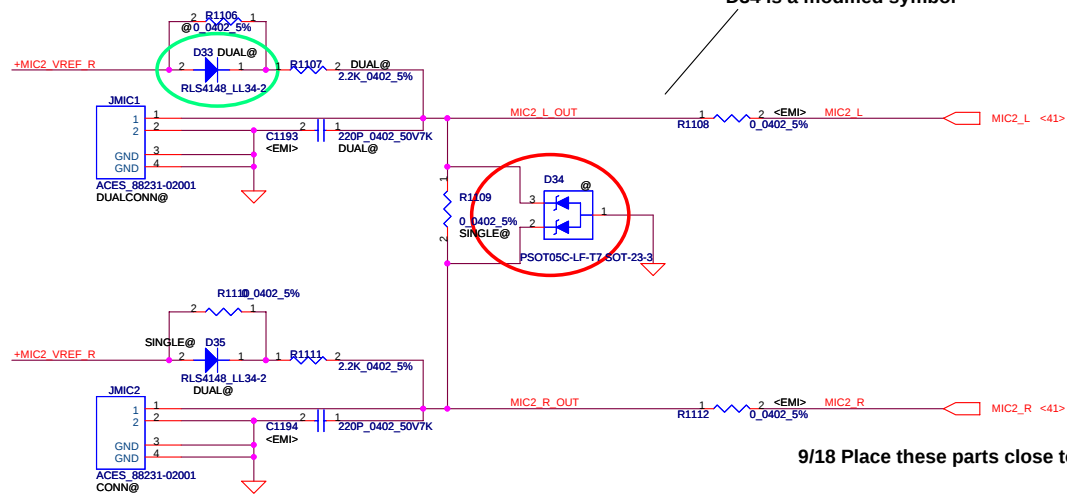
1/8 change JSPK1 following JAW91

9/3 Change footprint from ACES 88266-04001 N to ACES 88266-04001



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				Custom	KHLBX MB Schematic	1.0
				Date:	Monday, January 19, 2009	Sheet 42 of 56

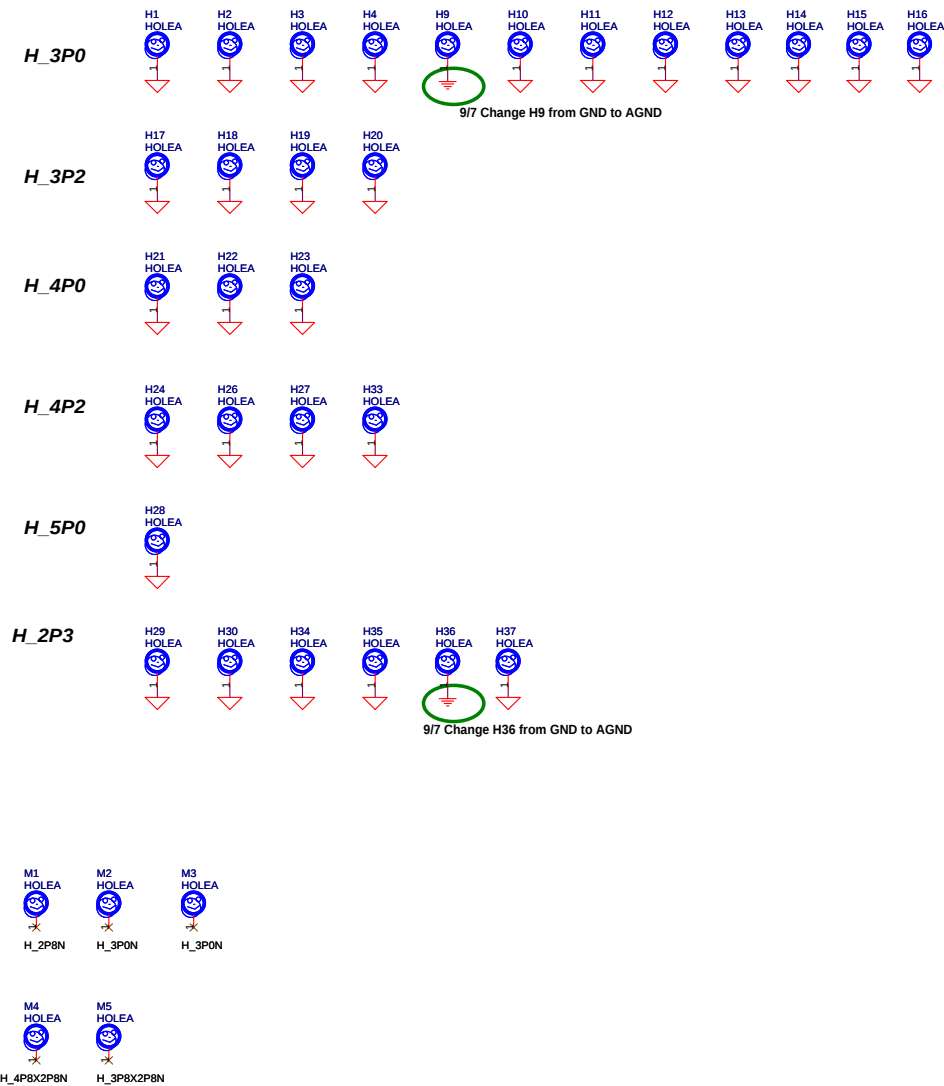
D34 is a modified symbol



9/18 Place these parts close to CODEC (U36)

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				KHLBX MB Schematic		
				Date	Monday, January 19, 2009	Sheet 43 of 56

11/27 Add screw for layout request

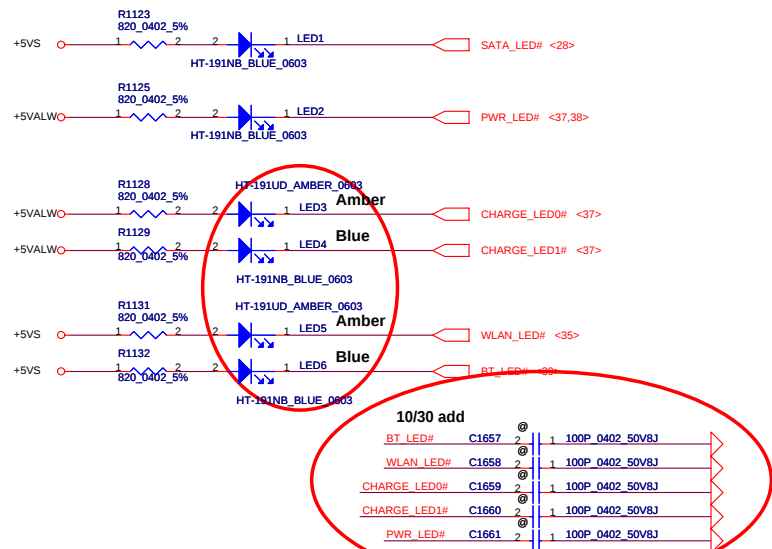


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Size	Custom	Document Number	KHLBX MB Schematic		Rev
Date:		Monday, January 19, 2009	Sheet	44	of 56

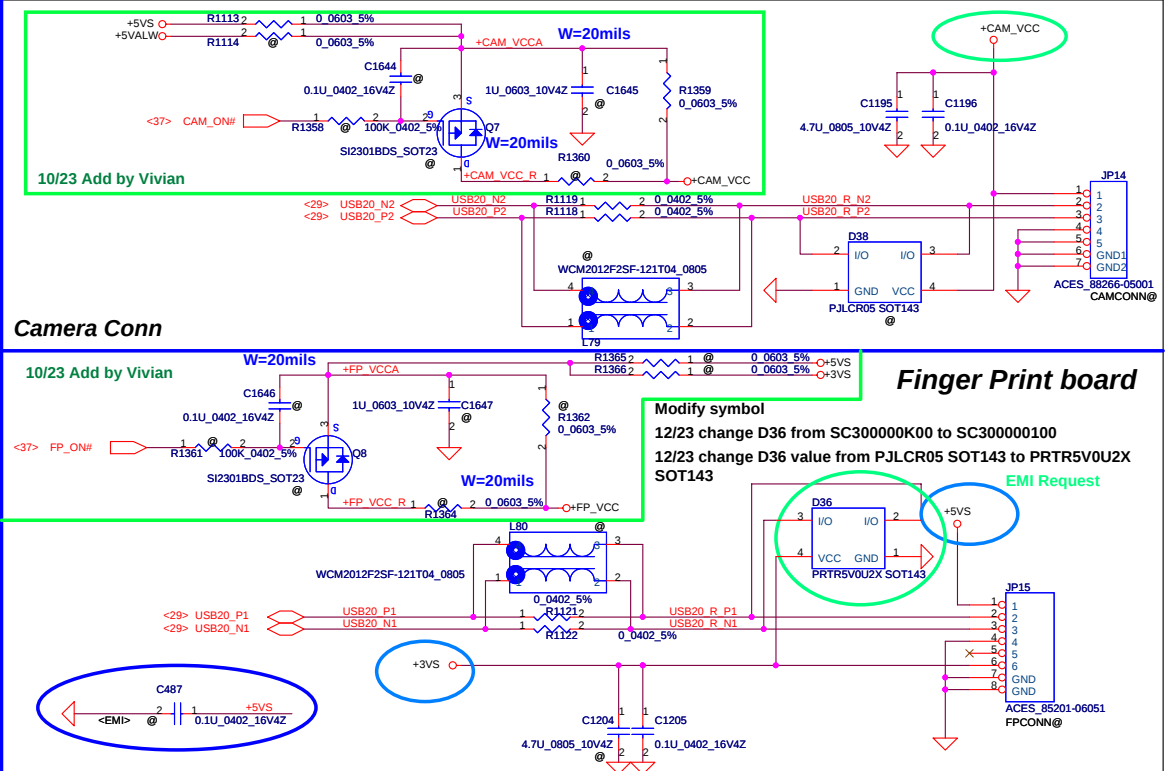
LED

TPM X76 Information

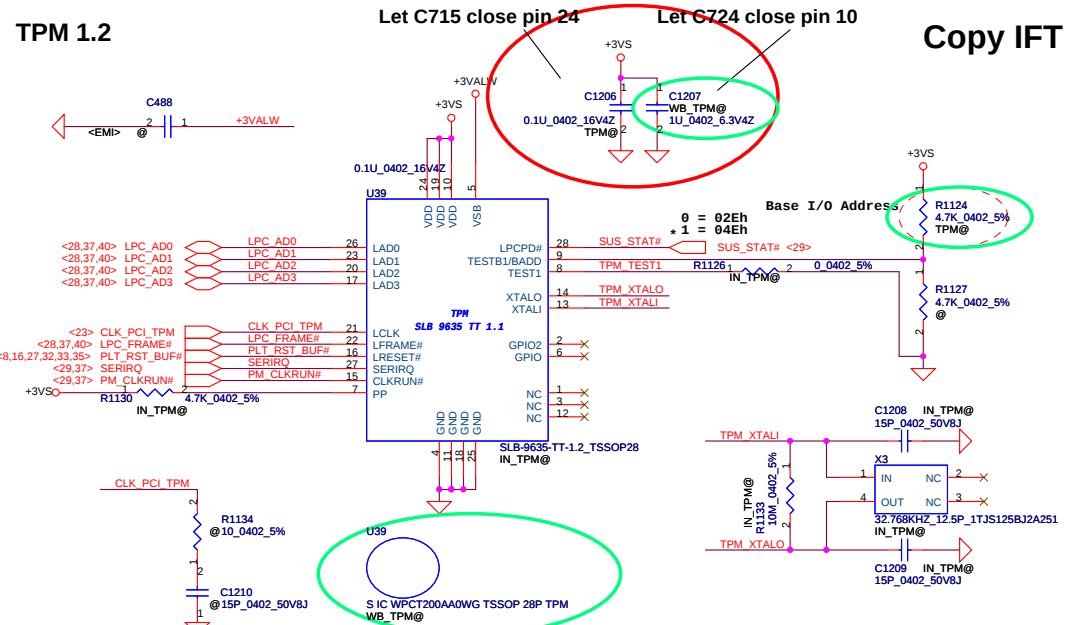
X76 P/N	Vendor	Location	Bom Structure
X7611630L07	Infineon	C717,C718,R698,R702,R703,U32,X3	IN_TPM@
X7611630L08	Winbond	C724,U32	WB_TPM@



~~12/7 Modified LED footprint to LED_HT-207UD-CB_4P~~
12/15 Modified to correct LED symbol!

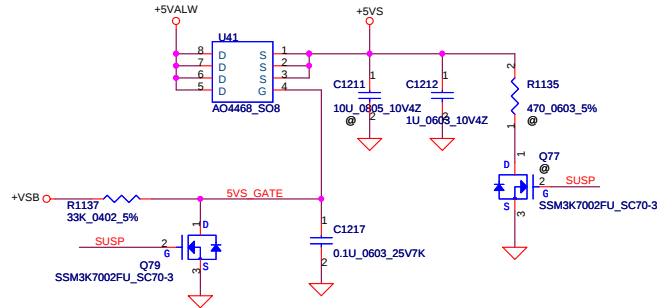


TPM 1.2

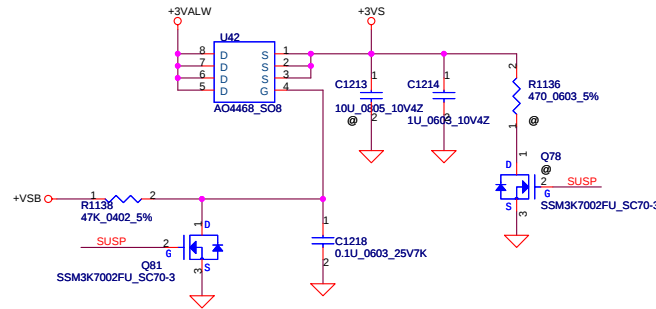


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				MDC/LED/Camera/FP			
				Size B	Document Number		
				KHLBX MB Schematic			
Date:		Monday, January 19, 2009		ISheet	45	of	56

+5VALW TO +5VS

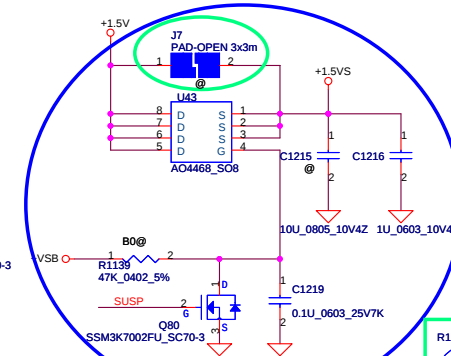


+3VALW TO +3VS

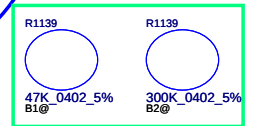


+1.5V TO +1.5VS

CHECK

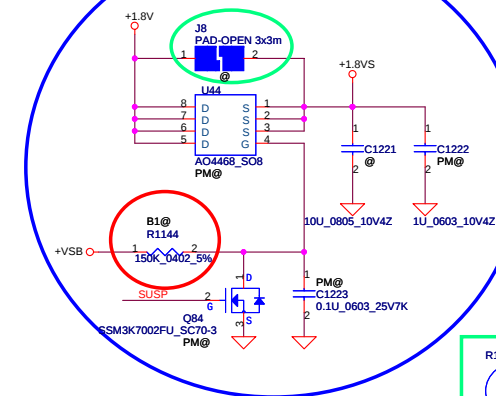


10/22 Add by Vivian

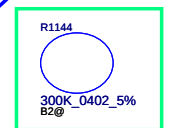


+1.8V TO +1.8VS

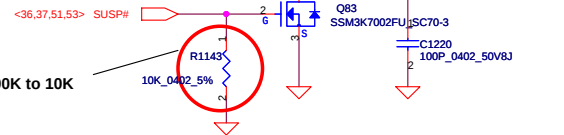
CHECK



10/22 Add by Vivian



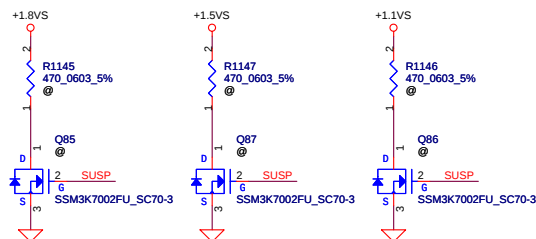
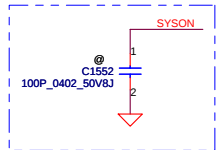
3/14 Change R16 from 100K to 10K



<8,52> SYSON#

<36,37,51,52> SYSON#

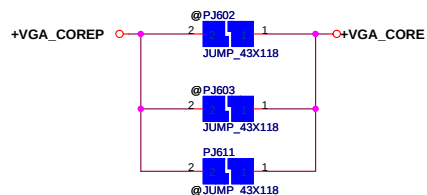
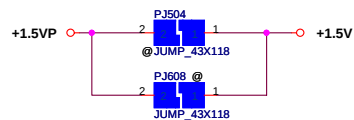
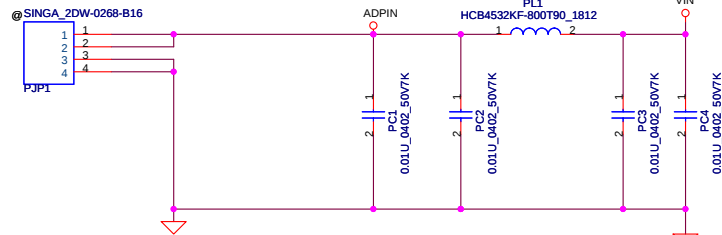
10/31 Remove R1367



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				Deciphered Date				DC Interface			
				2009/07/15				Size B			
								Document Number			
								KHLBX MB Schematic			
								Rev 1.0			
								Date: Monday, January 19, 2009			
								Sheet 46 of 56			

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DC301001Y00



BOM structure comment

@ ==>unpop

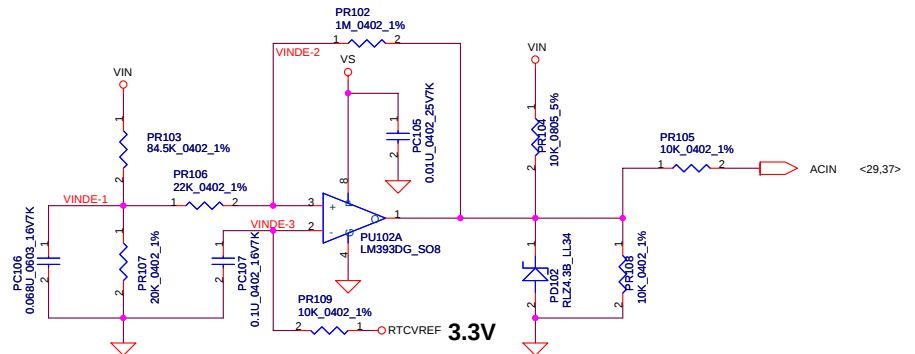
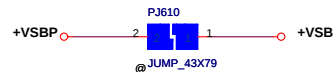
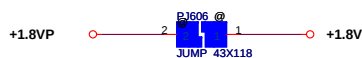
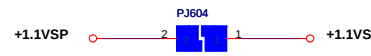
65@==> UMA only

90@==>DIS only

NV@==>Nvidia sku only

M96@==>ATI sku only

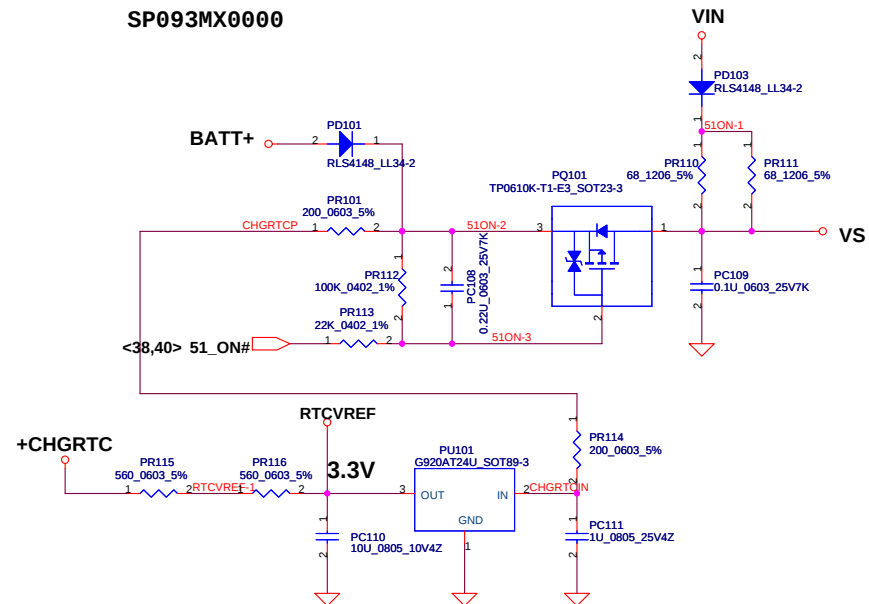
65NV@==>UMA and NV sku only



Vin Detector

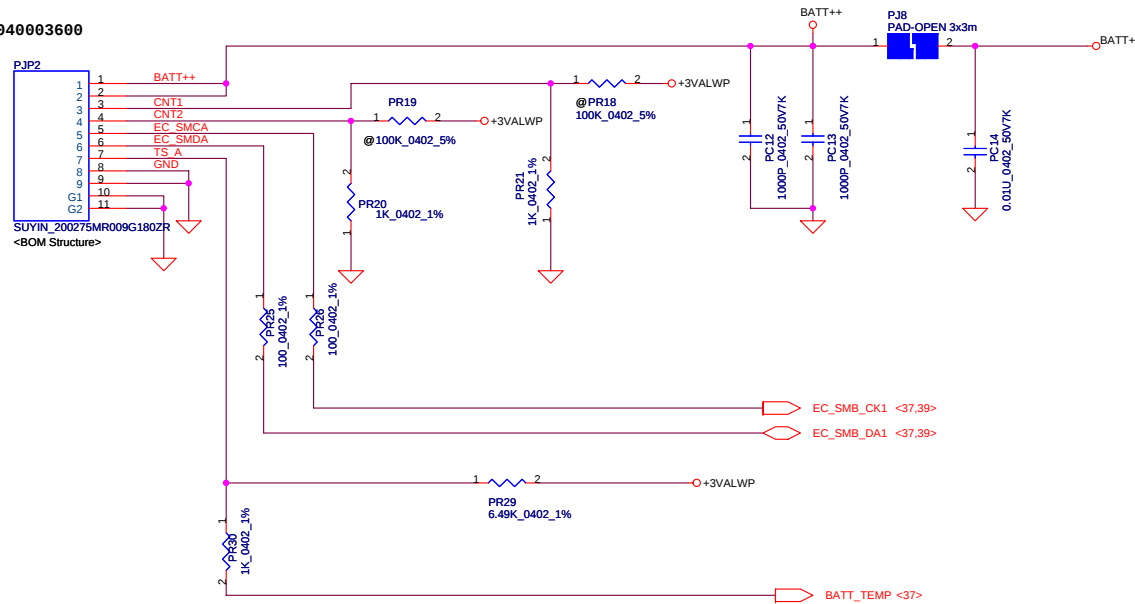
High 18.384 17.901 17.430
Low 17.728 17.257 16.976

SP093MX0000

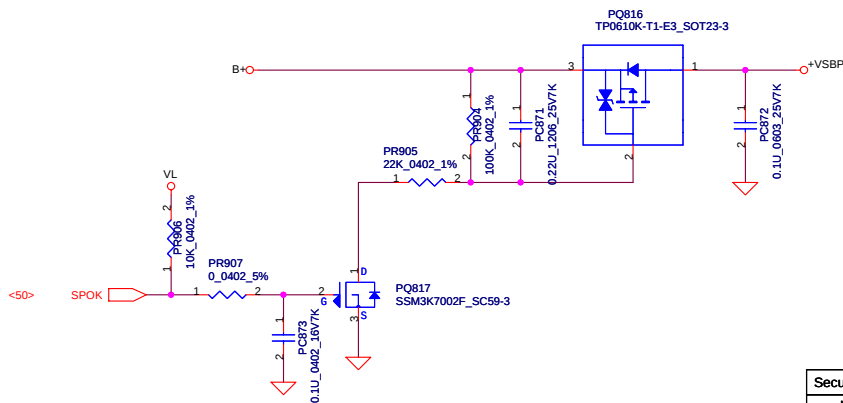
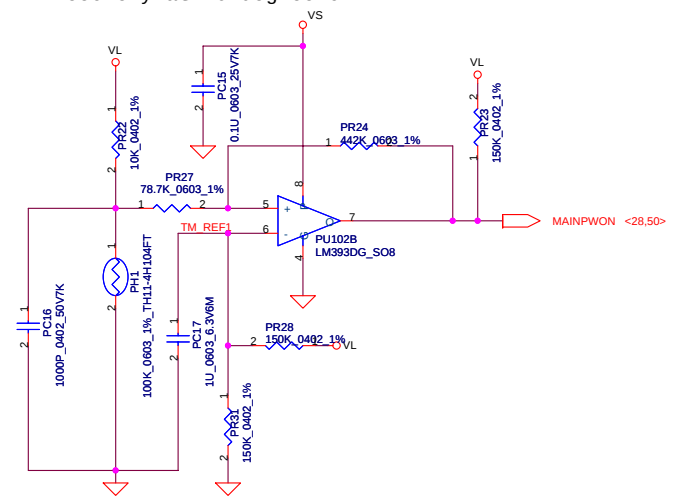


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Size	Document Number	KHLBX MB Schematic			Rev
Custom					1.0
Date:	Monday, January 19, 2009	Sheet	47	of	56

DC040003600

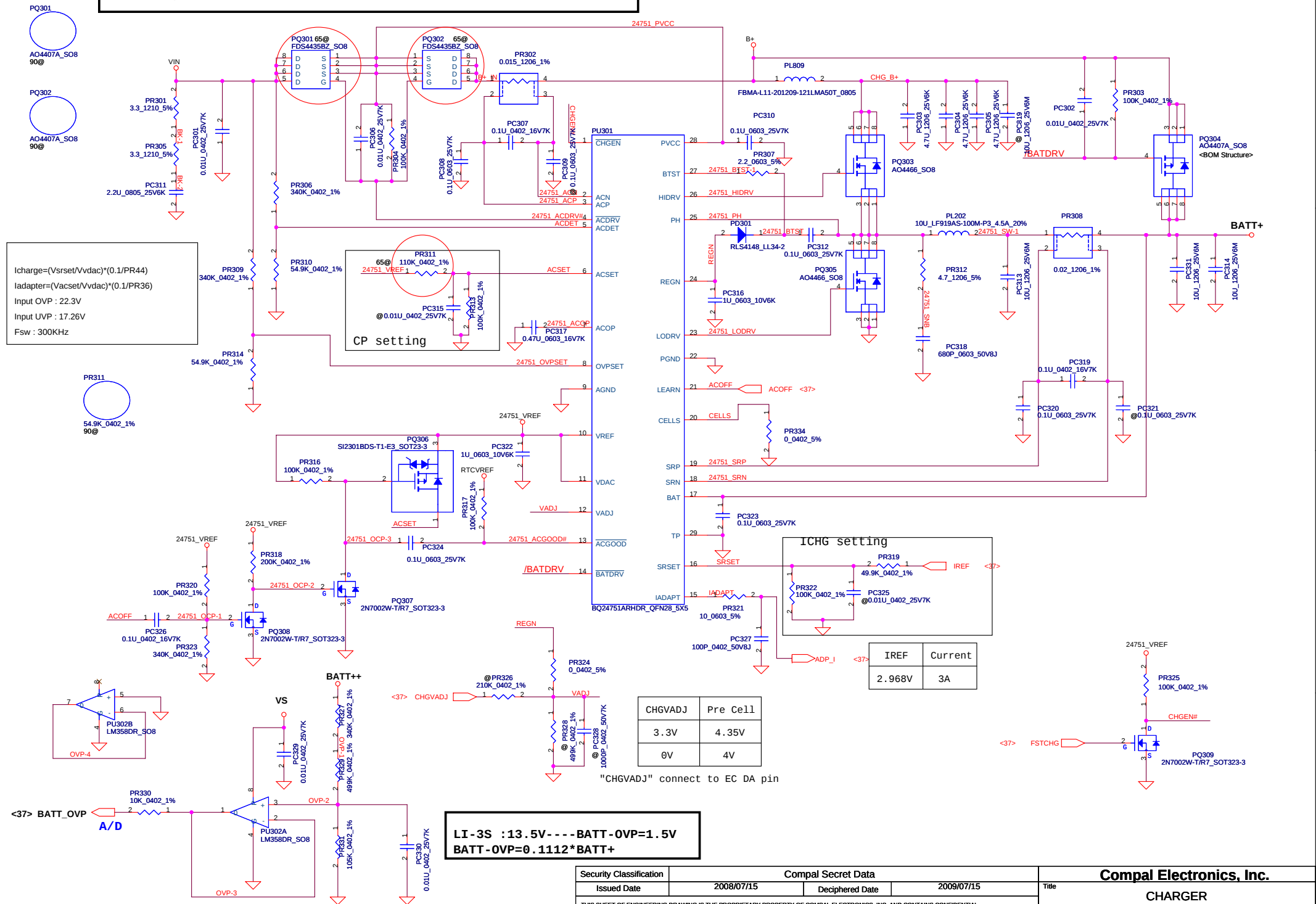


PH1 under CPU botten side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C

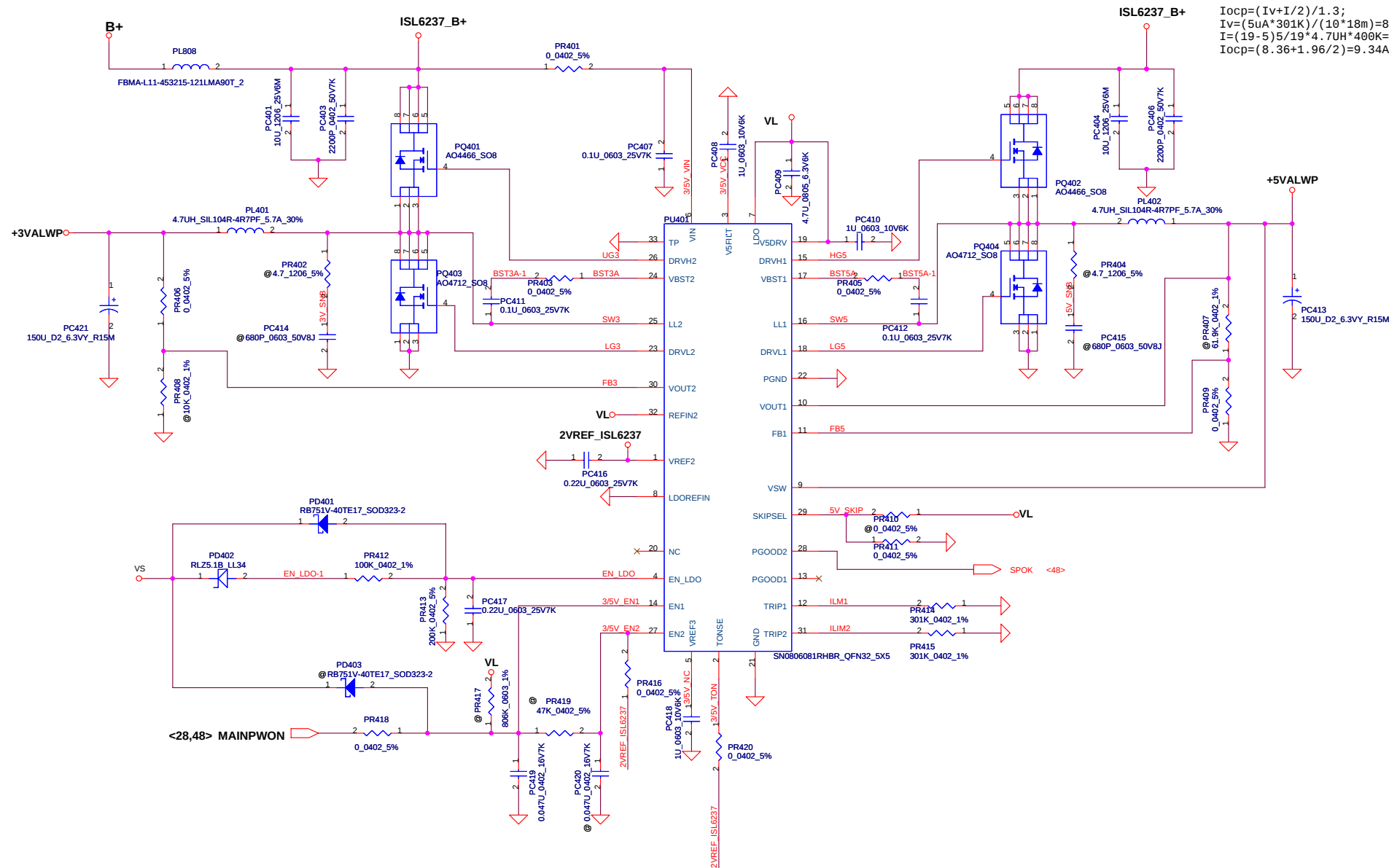


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Size	Document Number	KHLBX MB Schematic		Rev	
Custom				1.0	
Date:	Monday, January 19, 2009	Sheet	48	of	56

65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A

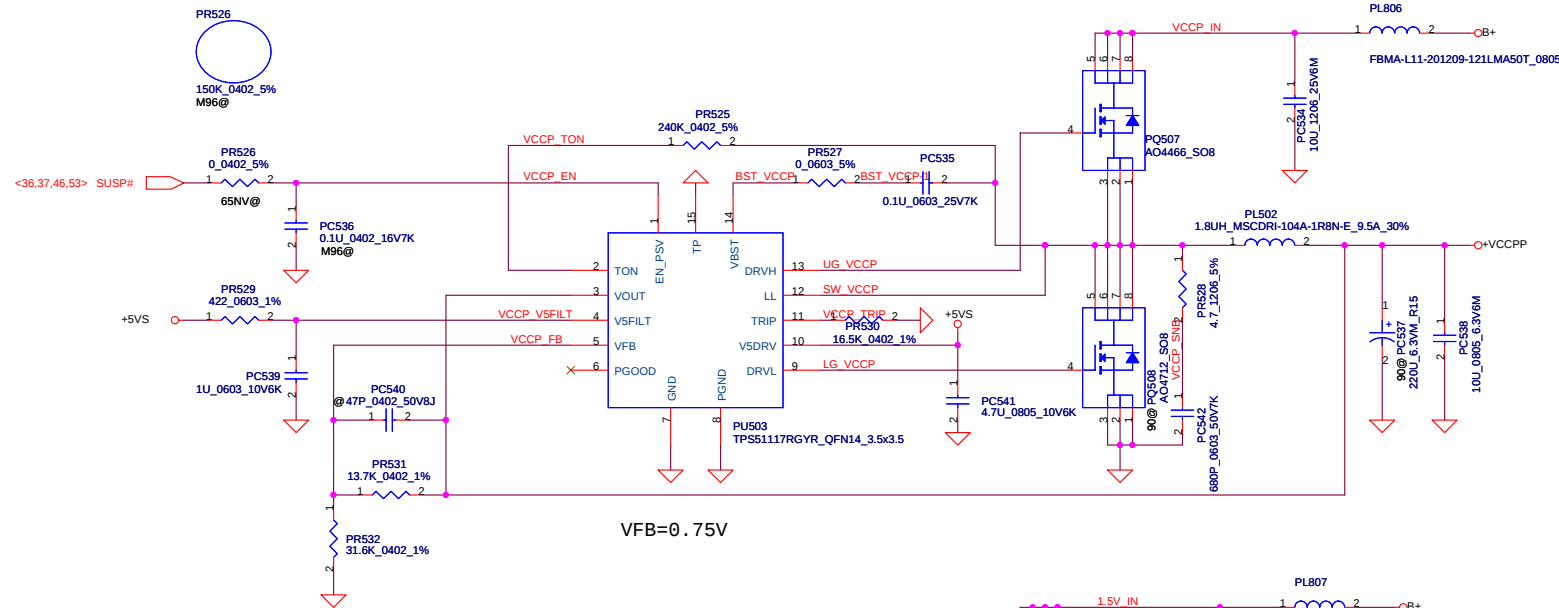


$I_{ocp} = I_v + I/2$; $I_v = (5\mu A * 301K) / (10 * 18m) = 8.36A$
 $I = (19 - 3.3) 3.3 / 19 * 4.7\mu H * 300K = 1.93A$ $I_{ocp} = 8.36 + 1.93 / 2 = 9.32A$



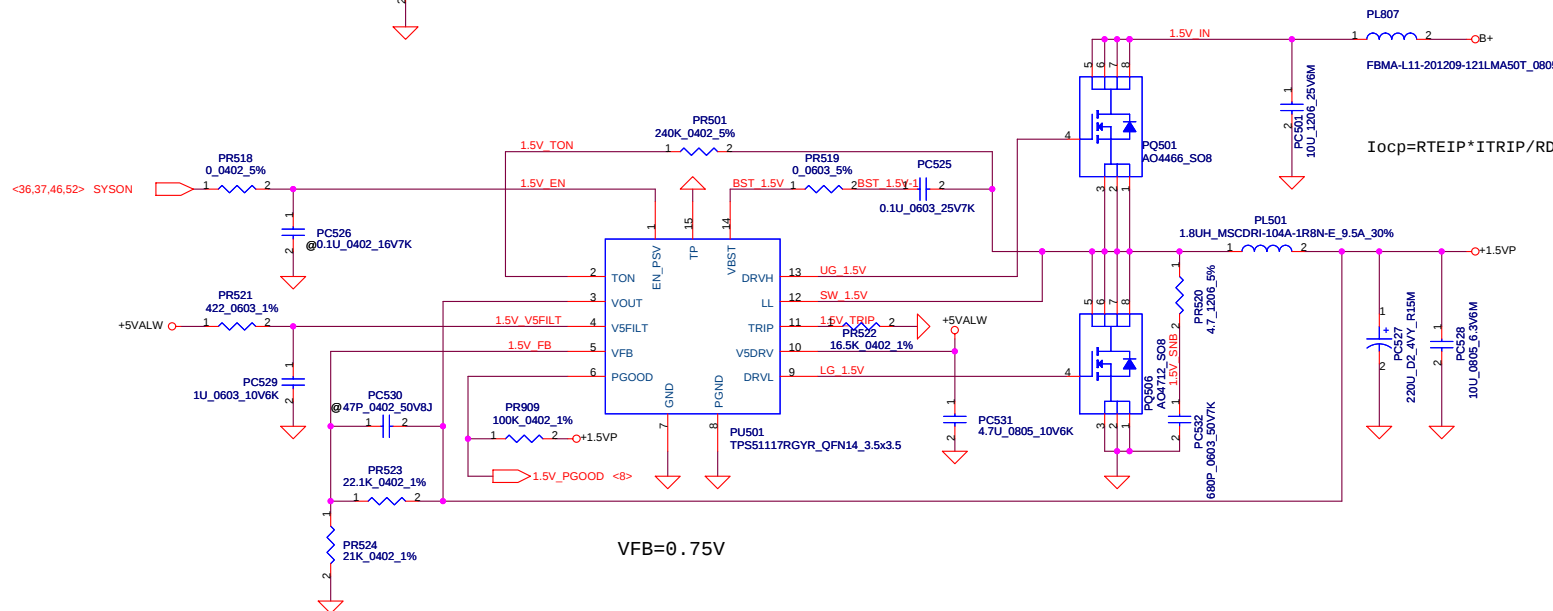
$I_{ocp} = (I_v + I/2) / 1.3$;
 $I_v = (5\mu A * 301K) / (10 * 18m) = 8.36A$;
 $I = (19 - 5) 5 / 19 * 4.7\mu H * 400K = 1.96A$;
 $I_{ocp} = (8.36 + 1.96 / 2) = 9.34A$

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				KHLBX MB Schematic	
				Date	Monday, January 19, 2009
				Sheet	50 of 56
				Rev	1.0



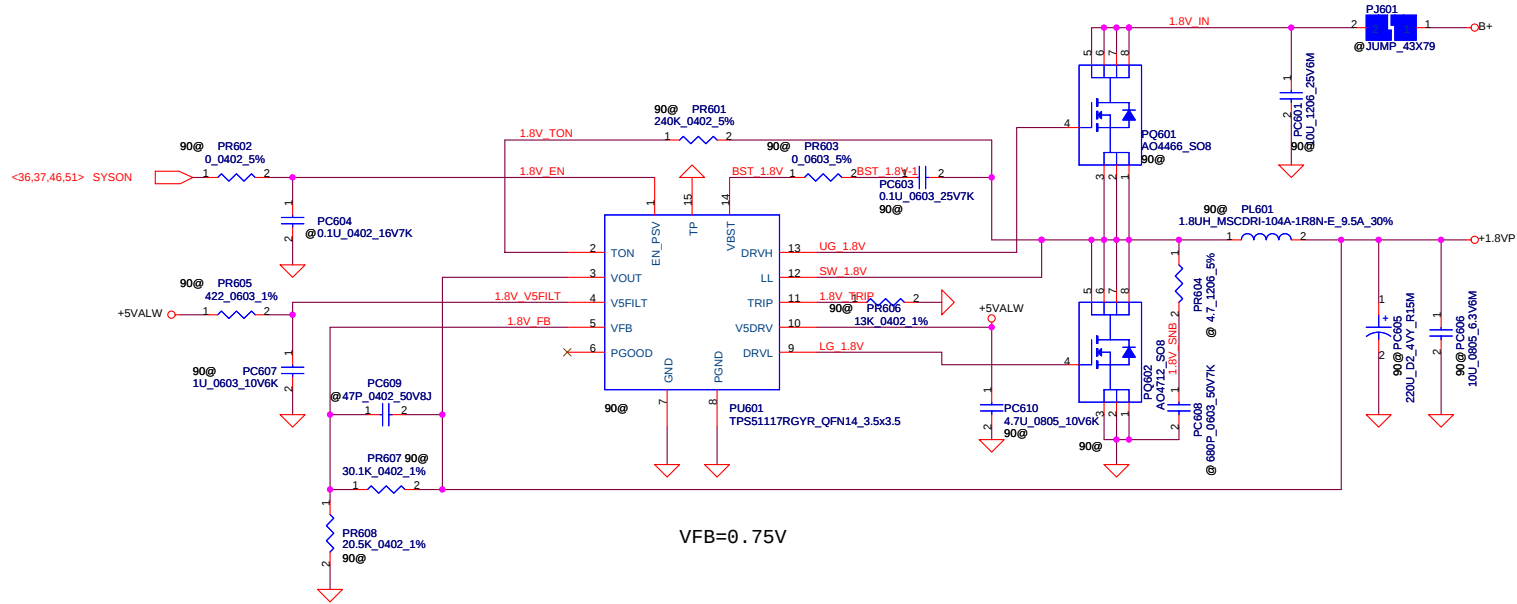
PC537
330U 6.3V_M
65@

PQ508
S TR FDS6670AS_NL 1N SO8
65@

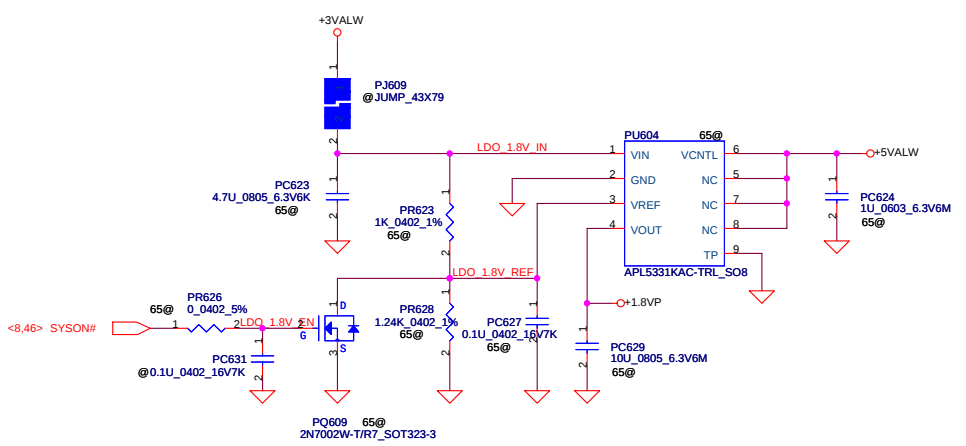
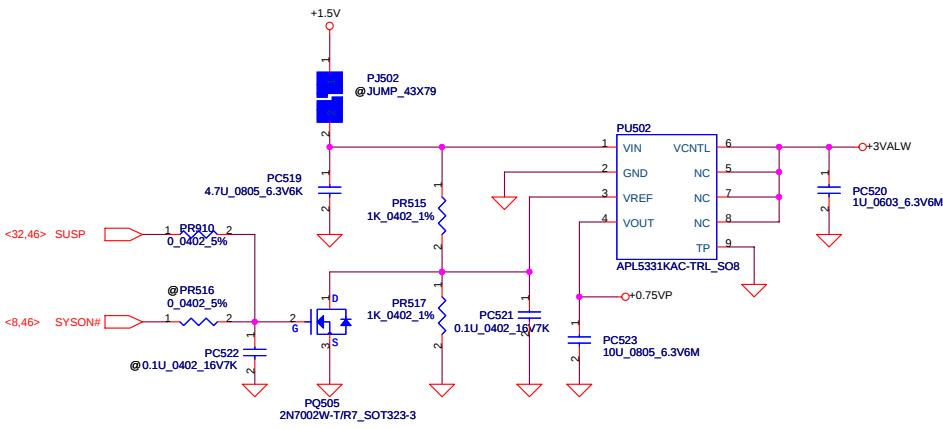


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				KHLBX MB Schematic		
				Date: Monday, January 19, 2009	Sheet 51	of 56

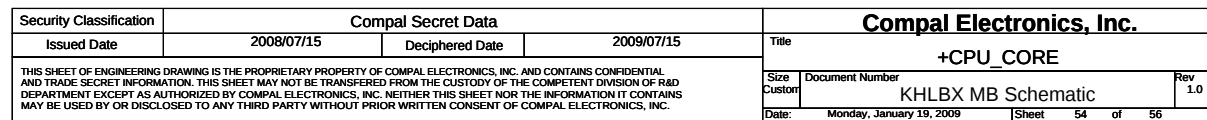
$$I_{ocp} = R_{TEIP} \cdot I_{TRIP} / R_{DS(ON)} + 1/2 \quad I = 13k \cdot 9u / 15m + 1/2 \cdot 2.7 = 9.15A$$



VFB=0.75V



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Size	Custom	Document Number	KHLBX MB Schematic	
Date	Monday, January 19, 2009	Sheet	52	Rev 1.0



Page

DVT

Reason for change

Change Diode 4148 vendor for layout footprint

modify VGA_core OCP to 29A

modify VGA_core sequence for NV and ATI

modify 1.05V sequence for ATI

Change 2N06 to 2N7002 for costdown

Add snubber & bead at cpu_core for EMI request

Add snubber & bead at VGA_core for EMI request

Add snubber & bead at VCCP & 1.5VP for EMI request

Add boost res. & bead & snubber at charger for EMI request

Change 1.8UH vender to mgalaer for ZIZI nosie

Modify 1.05V OCP for UMA(12A~19A) & DIS for (8A~12A)

Modify CPU loadline

Modify VGA CHOKE to 4mm high

Modify 1.1V to APL5912 for over loading

Change VCCP output cap to 330U for reduce ripper

Change PU500 & PC500 to X76 group for 2nd

Add 10UF in charger output for unstable

Modify 1.5V OCP to 8A~12A

PVT

Modify ATI VGA_core from 1.1 to 1.15V

Modify 220U/25V vender to SANYO from PPM suggest

Add 10UF in VGA B+ for over current(VGA B+ about 5.6A)

Modify CPU loadline

Change VGA frquency to 300K, reduce I

Change VGA FB cap for better response

Change VGA OCP set to around 41A

Change VGA output choke for rating.

Add extra VGA Low Side MOS

Change VGA high mos for cost down.

Change CPU high mos for cost down.

Modify list

PD101,PD103,PD301

Change PR874 to 5.9K

Remove PC845 & change PR873 to 0 ohm

Change PR526 to 150K ohm and PC536 to 0.1U

PQ810 & PQ811 for DIS, PQ812 & PQ813 for M96

Add PR819 & PR829 to 4.7 OHM , PC815 & PC823 to 680pF,
Change PL801 to 120 ohm bead & change PR841 & PR846 to 2.2 OHM

Add PR875 to 4.7 OHM , PC844 to 680pF,
Change PJ605 to 120 ohm bead and change PR868 to 2.2 OHM

Add PR528 & PR520 to 4.7 OHM , PC542 & PC532 to 680pF

change PJ506 and PJ501 to 120 ohm bead

Change PJ301 to 120 Ohm bead and Changer PR307 to 2.2 OHM,
Add PR312 to 4.7 Ohm & PC318 to 680P

PL502,PL501,PL601(DIS)

Change PR530 to 16.5K & PQ508 to FDS6670

Change PR839 to 4.64K

PL804

PU603

PC537

Del PU500 & PC500 in 90W SKU

PC331

Change PR522 to 16.5K

Change PR881 to 7.15K

Add PC853 to 10U

Change PR839 to 4.75K

Change PR880to 44.2K

Change PC848 to 2200pF

Change PR874 to 8.66K

Change PL804 to 0.36U

Add PQ809

Change PQ807 to S TR TPCA8030-H 1N SOP-ADV

Change PQ801 and PQ804 to S TR TPCA8030-H 1N SOP-ADV

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				Custom	KHLBX MB Schematic	1.0
				Date:	Monday, January 19, 2009	Sheet 55 of 56

Page

PVT

Reason for change

Change VGA response
Change VGA OCP set

Modify list

Change PR876 to 0 and PR878 to10
Change PR876 to 0 and PR874 to 5.1K

PVT

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Date: Monday, January 19, 2009				Sheet	56 of 56	

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