

COMPAL CONFIDENTIAL

MODEL NAME : IAQ20

PCB NO : LA-3751P (DA800008Y0L)

BOM P/N : 46149031L0121

Converse

**uFCPGA Mobile Merom
Intel Crestline + ICH8M**

21-05-2007

REV : 0.1(X00)

@ : Nopop Component

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.5V_RUN +1.25V_RUN +0.9V_DDR_VTT +1.05V_VCCP +VCC_CORE
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#1 / GNT#1	PIRQC, D
Docking	AD24	REQ#0 / GNT#0	PIRQA

ICH8-M	USB PORT#	DESTINATION
	0	Rear Right Bottom
	1	Rear Right Top
	2	EXPRESS CARD
	3	Bluetooth
	4	Rear Left Bottom
	5	Rear Left Top
	6	OZ77CR6/Smart Card Reader
	7	Docking
	8	Side Bottom
	9	Side Top
OZ77CR6	UPD+/D-, pin 16/17	ICH8-M
	DPD+/D-, pin 18/19	Biometric Reader
	EGATED+/D-, pin 20/21	SMART CARD

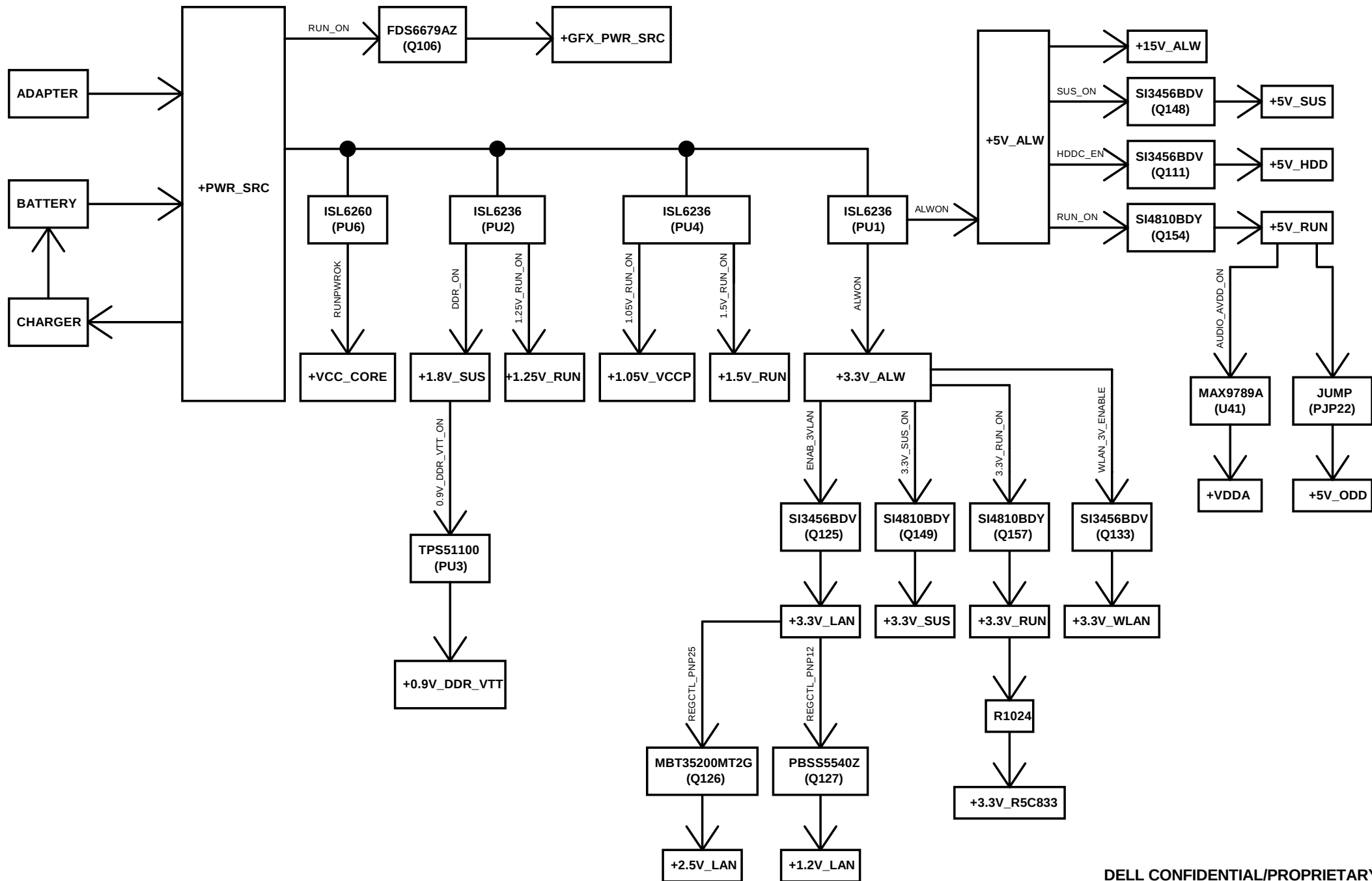
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD 1- Robson
Lane 2	MINI CARD 2- WLAN
Lane 3	None
Lane 4	EXPRESS CARD
Lane 5	None
Lane 6	GIGA LAN

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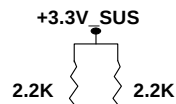
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ICH8-M

AJ26 ICH_SMBCLK
AD19 ICH_SMBDATA



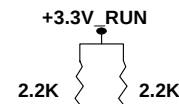
B6 D7
BCM5756
SMBUS Address [C8]

11 9
EXPRESS CARD
SMBUS Address [TBD]

32 30
MINI WLAN
SMBUS Address [TBD]

2N7002
2N7002

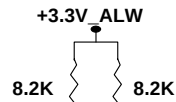
MEM_SCLK
MEM_SDATA



197
195
DIMMA
SMBUS Address [A0]
197
195
DIMMB
SMBUS Address [A4]
30
32
MINI ROBSON
SMBUS Address [TBD]

SIO
MEC5025

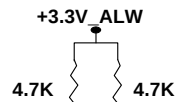
8 LCD_SMBCLK
7 LCD_SMBDAT



+3.3V_ALW

8
10
Graphic BTB CONN inverter
SMBUS Address [58]

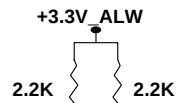
100 THRM_SMBCLK
99 THRM_SMBDAT



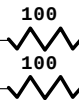
+3.3V_ALW

12
11
9
10
GUARDIAN EMC4001
SMBUS Address [2F]
CHARGER ISL88731
SMBUS Address [12]

112 PBAT_SMBCLK
111 PBAT_SMBDAT

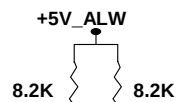


+3.3V_ALW



3
4
BATTERY Connector
SMBUS Address [16]

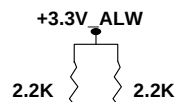
6 DOCK_SMBCLK
5 DOCK_SMBDAT



+5V_ALW

39
40
DOCKING
SMBUS Address [C4, 72, 70, 48]

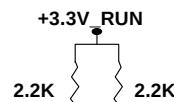
13 CKG_SMBCLK
12 CKG_SMBDAT



+3.3V_ALW

2N7002
2N7002

CLK_SCLK
CLK_SDATA



+3.3V_RUN

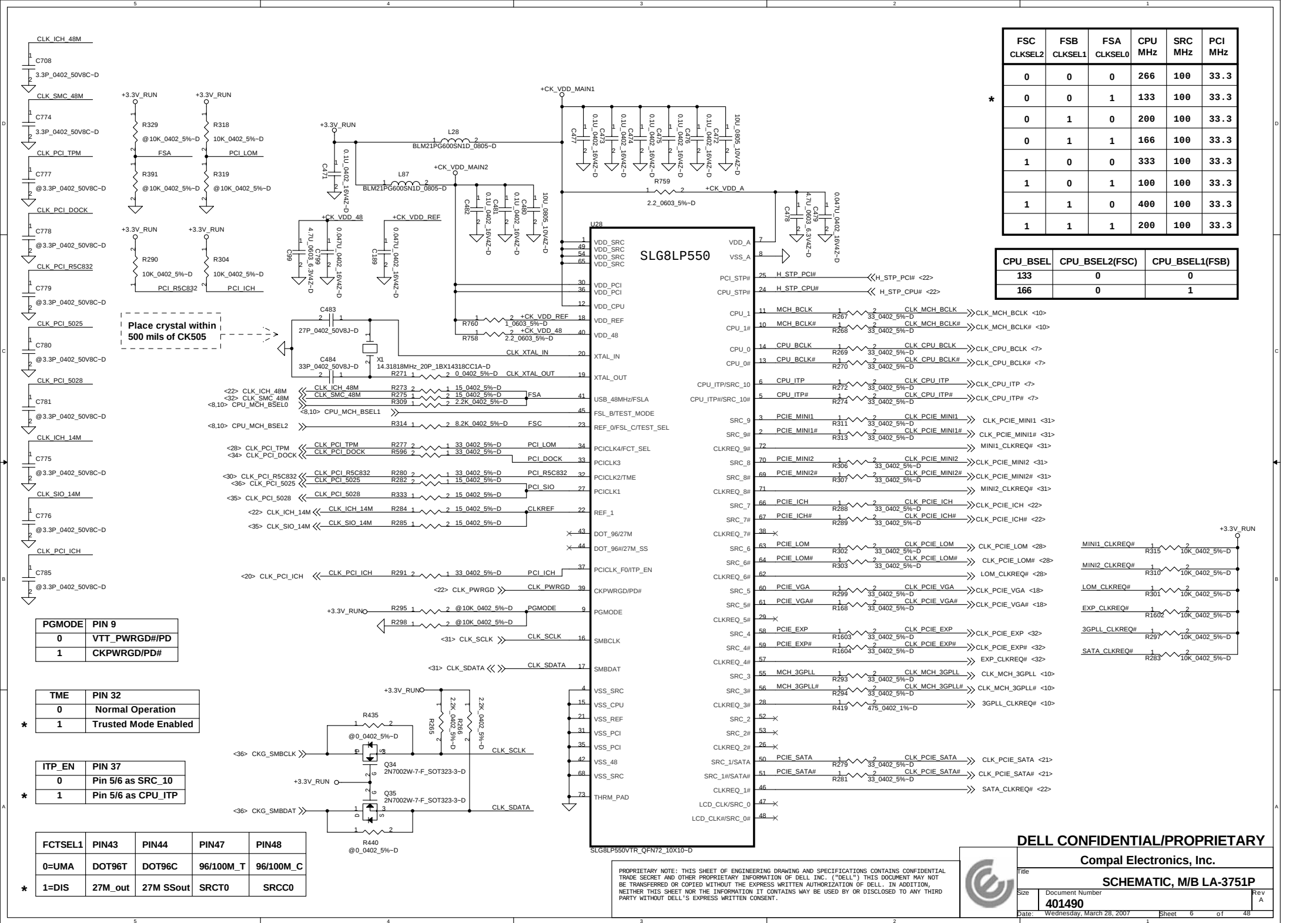
16
17
CLOCK GENERATOR
SMBUS Address [D2]

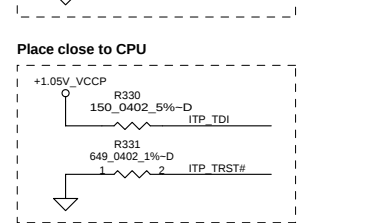
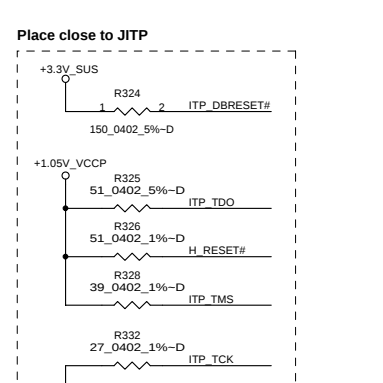
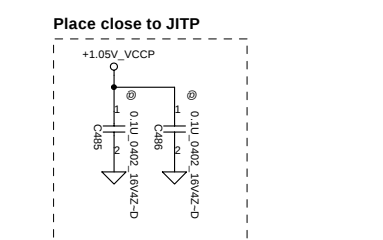
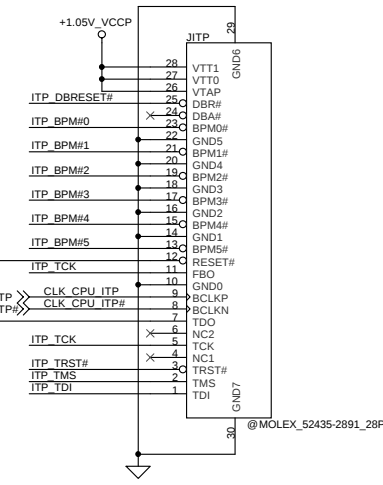
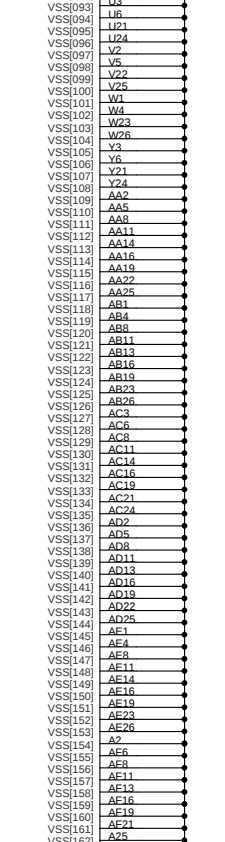
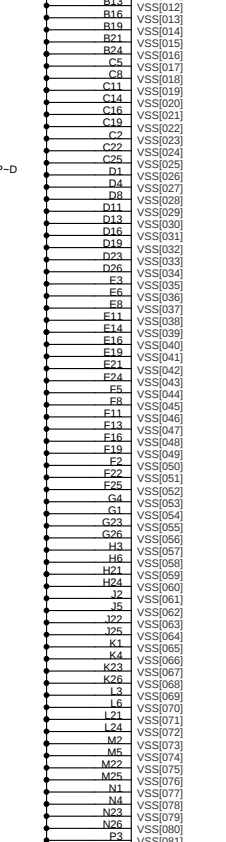
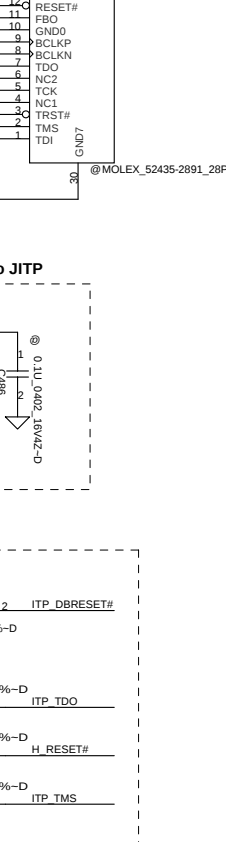
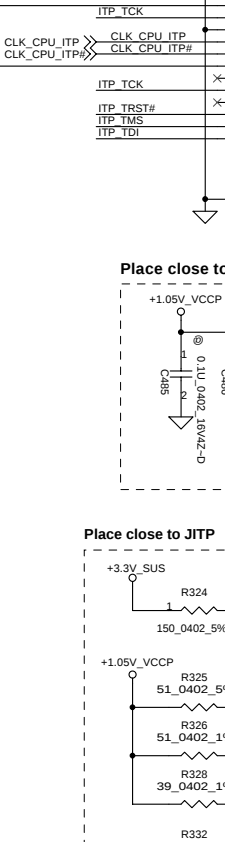
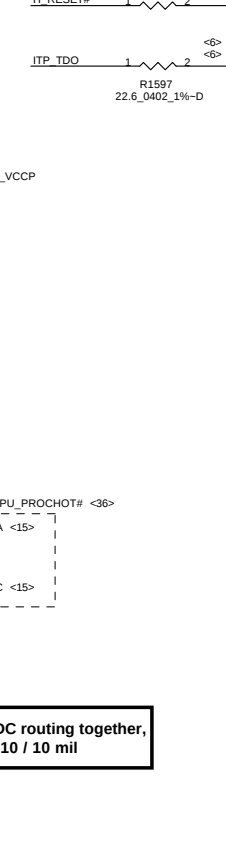
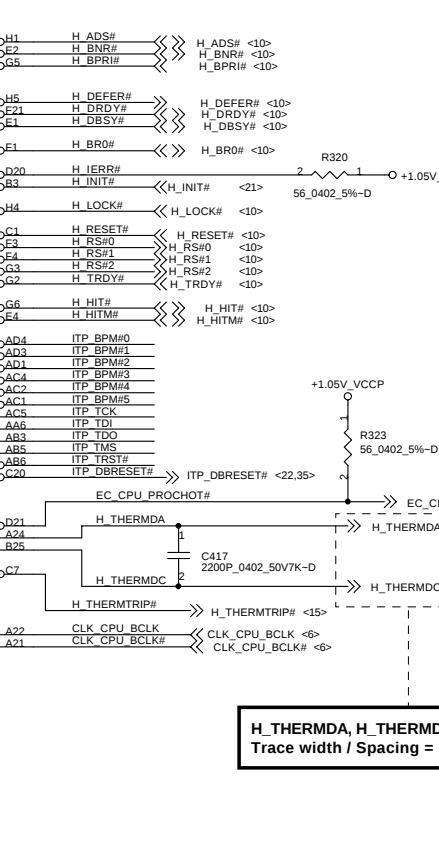
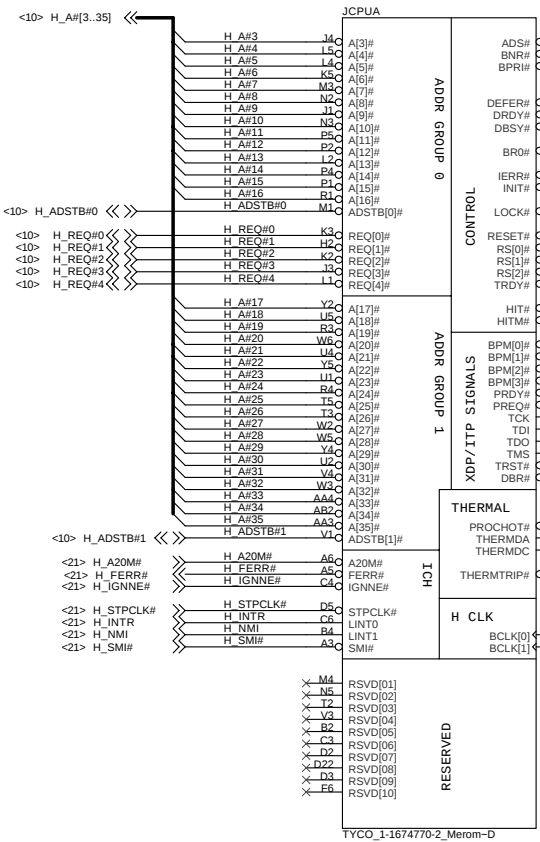
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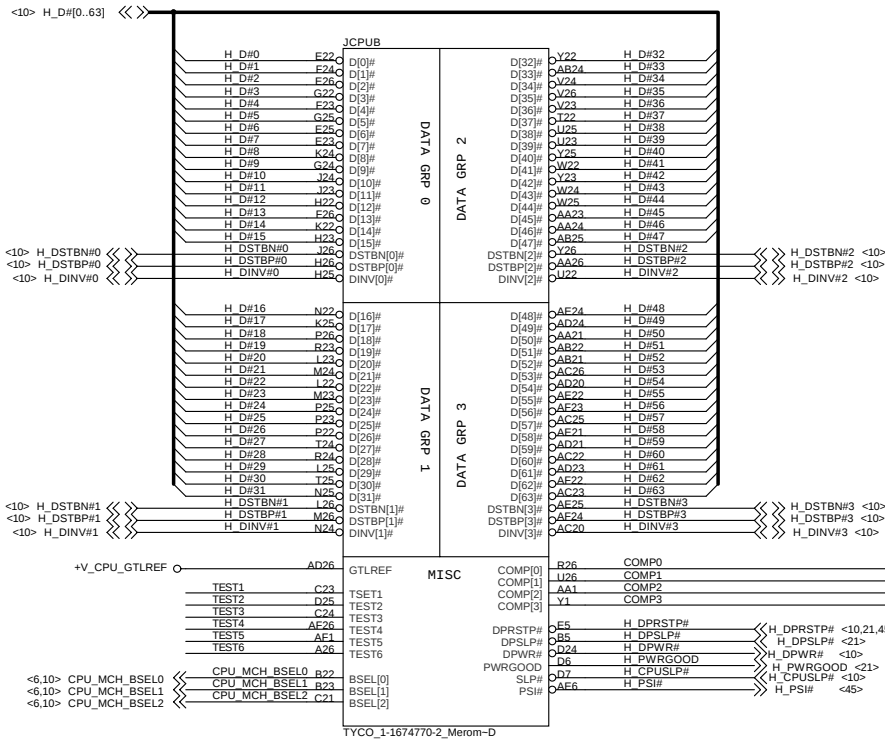
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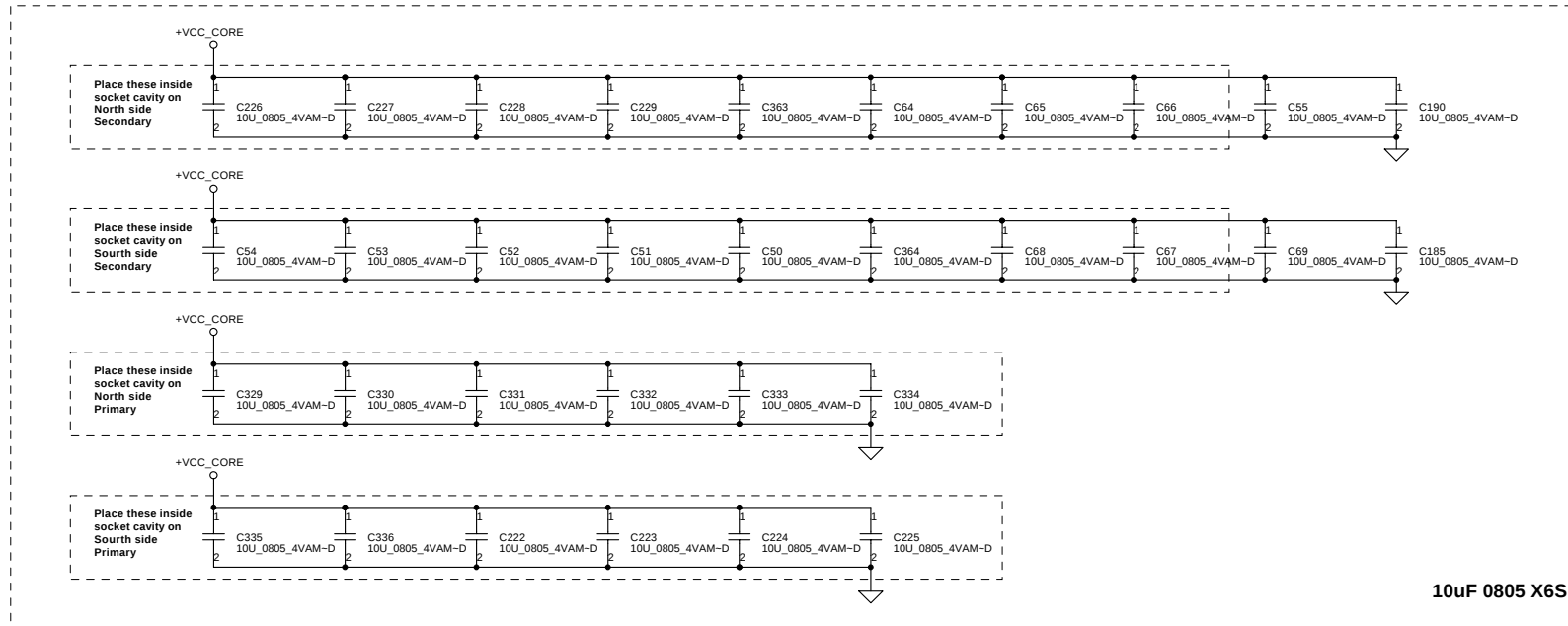
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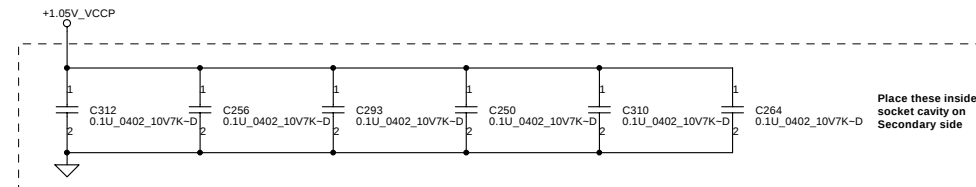
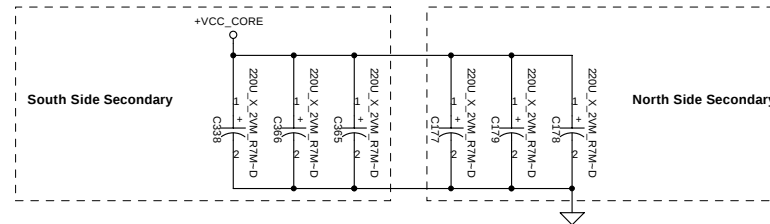
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High Frequency Decoupling



Near VCORE regulator.

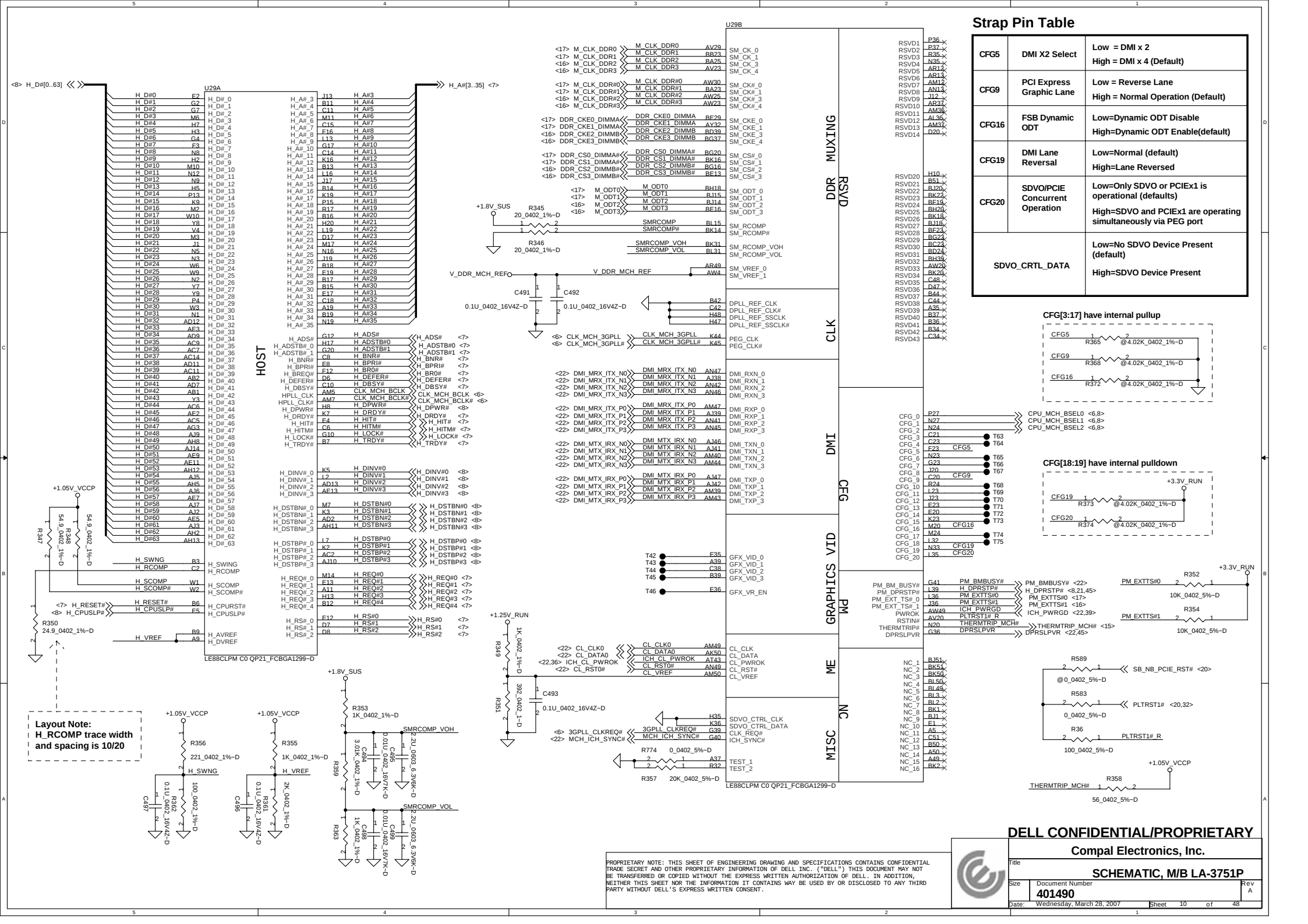


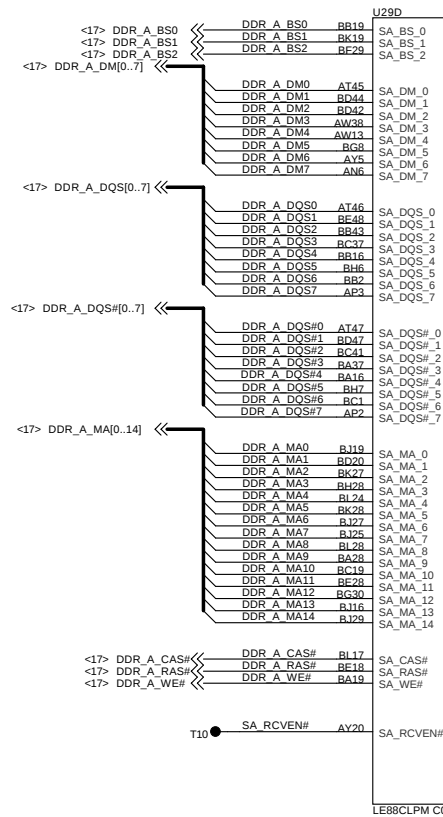
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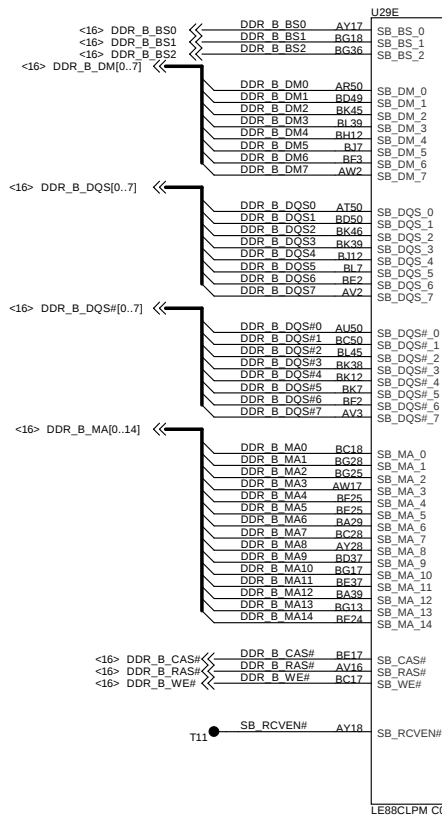
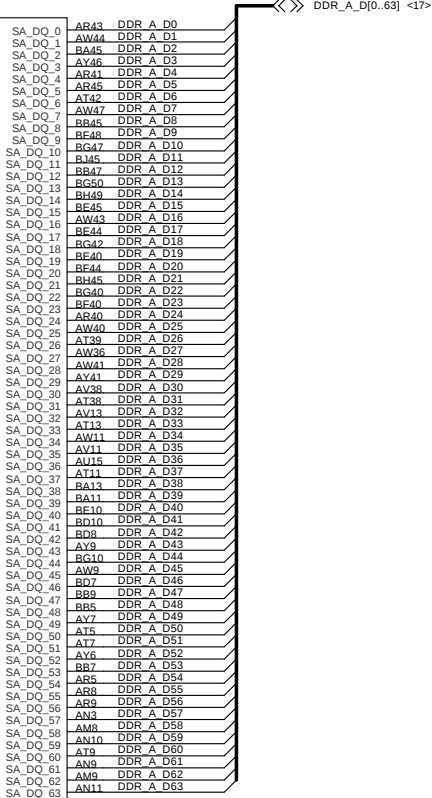
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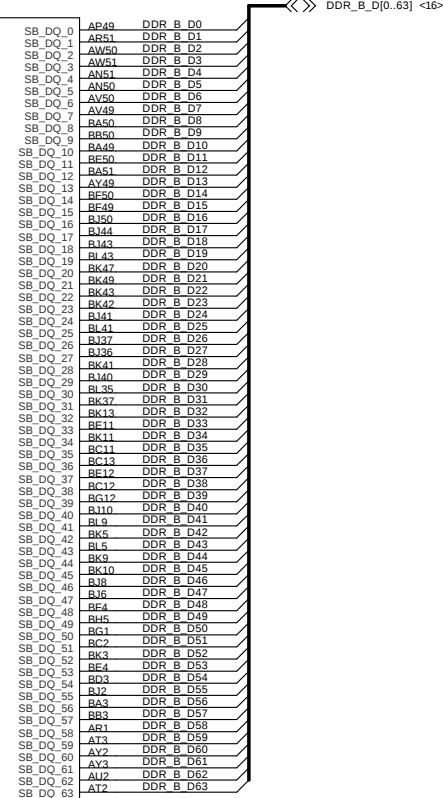




DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

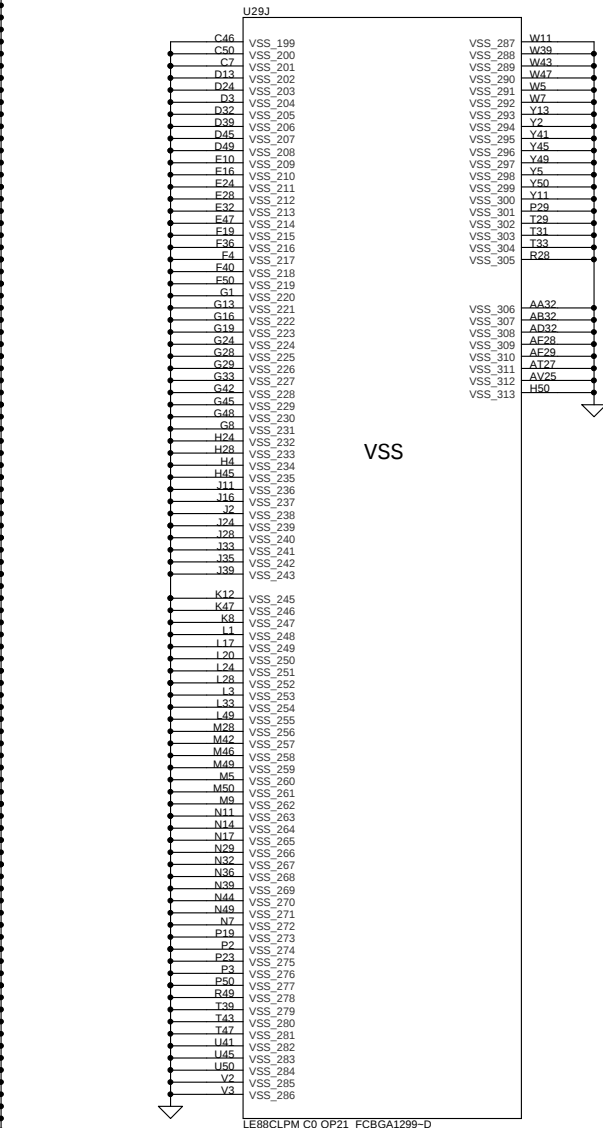


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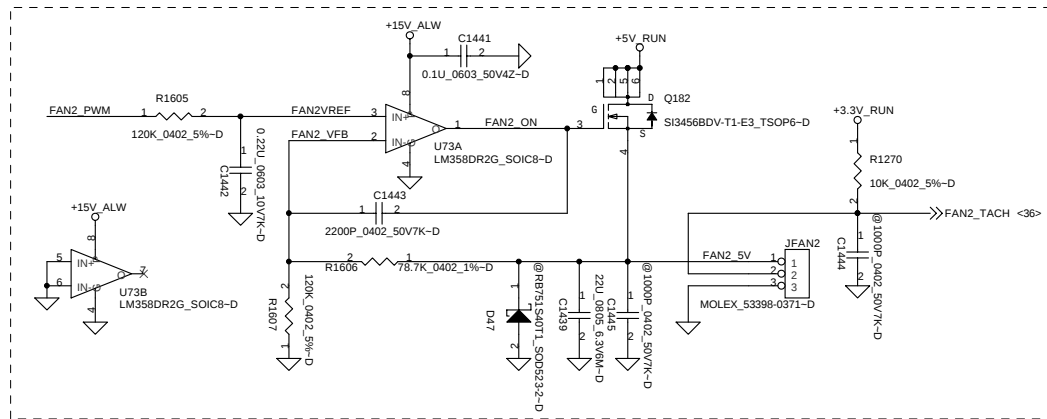
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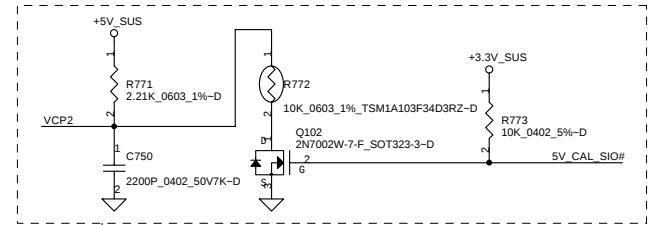
VGA fan control and Tachometer



$$VSET = \frac{R438}{R436+R438} \times 3.3V = 0.865V$$

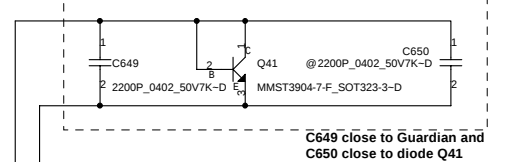
$$VSET = \left(\frac{Tp-70}{21} \right) \Rightarrow Tp = 88.2\text{ C}$$

Place close to JDIMA

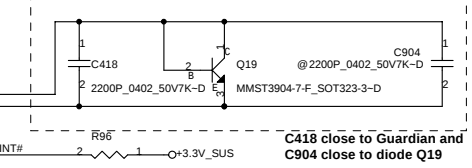


Place Q41 close to JDIMMB

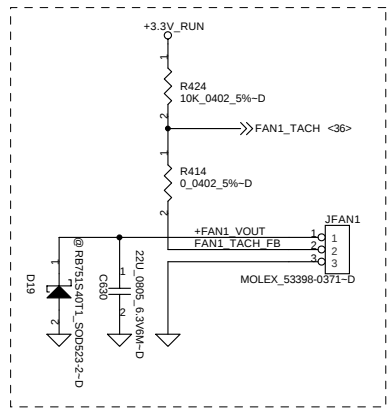
REM_DIODE3_N, REM_DIODE3_P routing together.
Trace width / Spacing = 10 / 10 mil



Diode circuit at DP4/DN4 is used for skin temp sensor
(placed optimally between CPU, MCH and GPU)

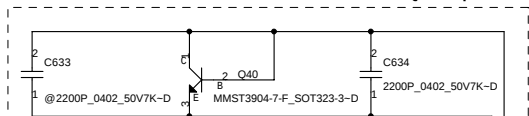


Main fan control and Tachometer



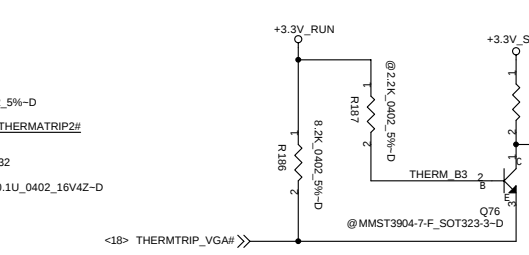
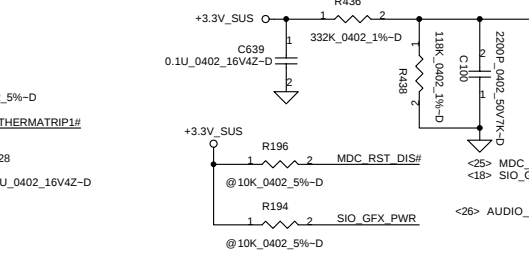
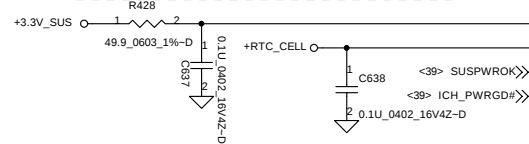
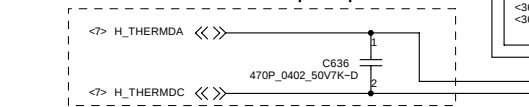
Place under CPU

Place C633 close to the Q40 as possible

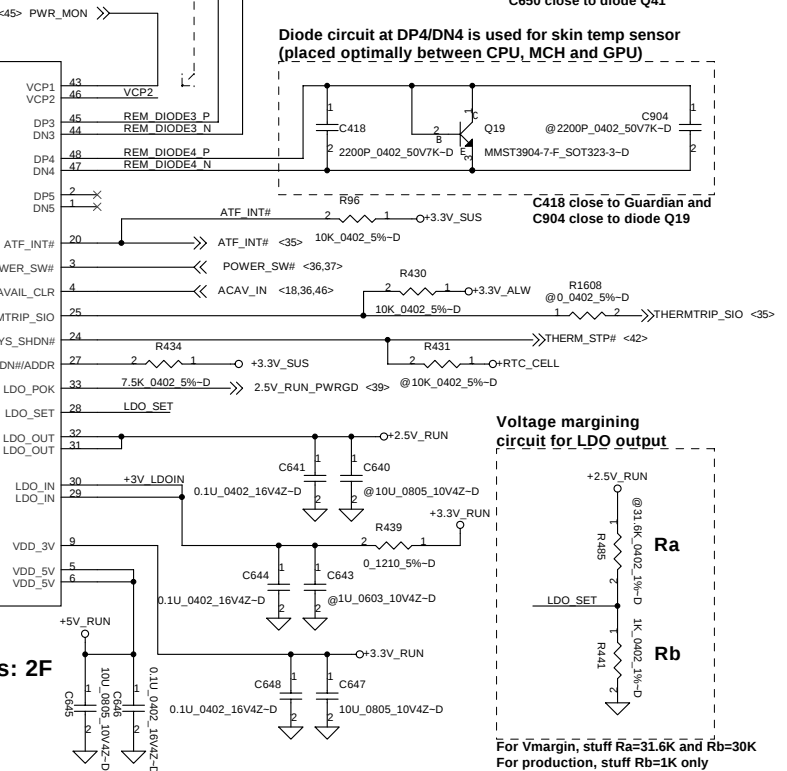


Place C634 close to the Guardian pins as possible

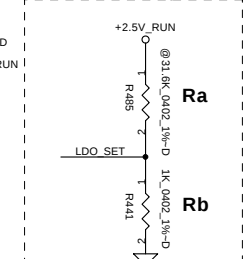
Place C636 close to Guardian pin as possible



SMBus address: 2F



Voltage margining circuit for LDO output



For Vmargin, stuff Ra=31.6K and Rb=30K
For production, stuff Rb=1K only

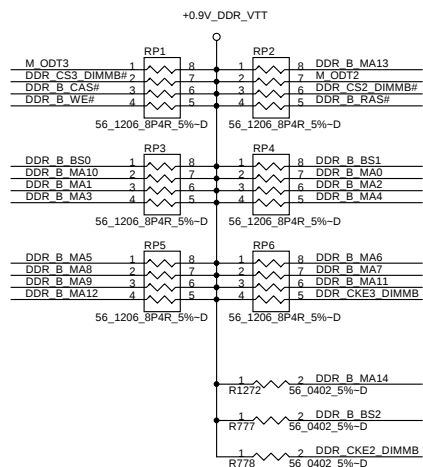
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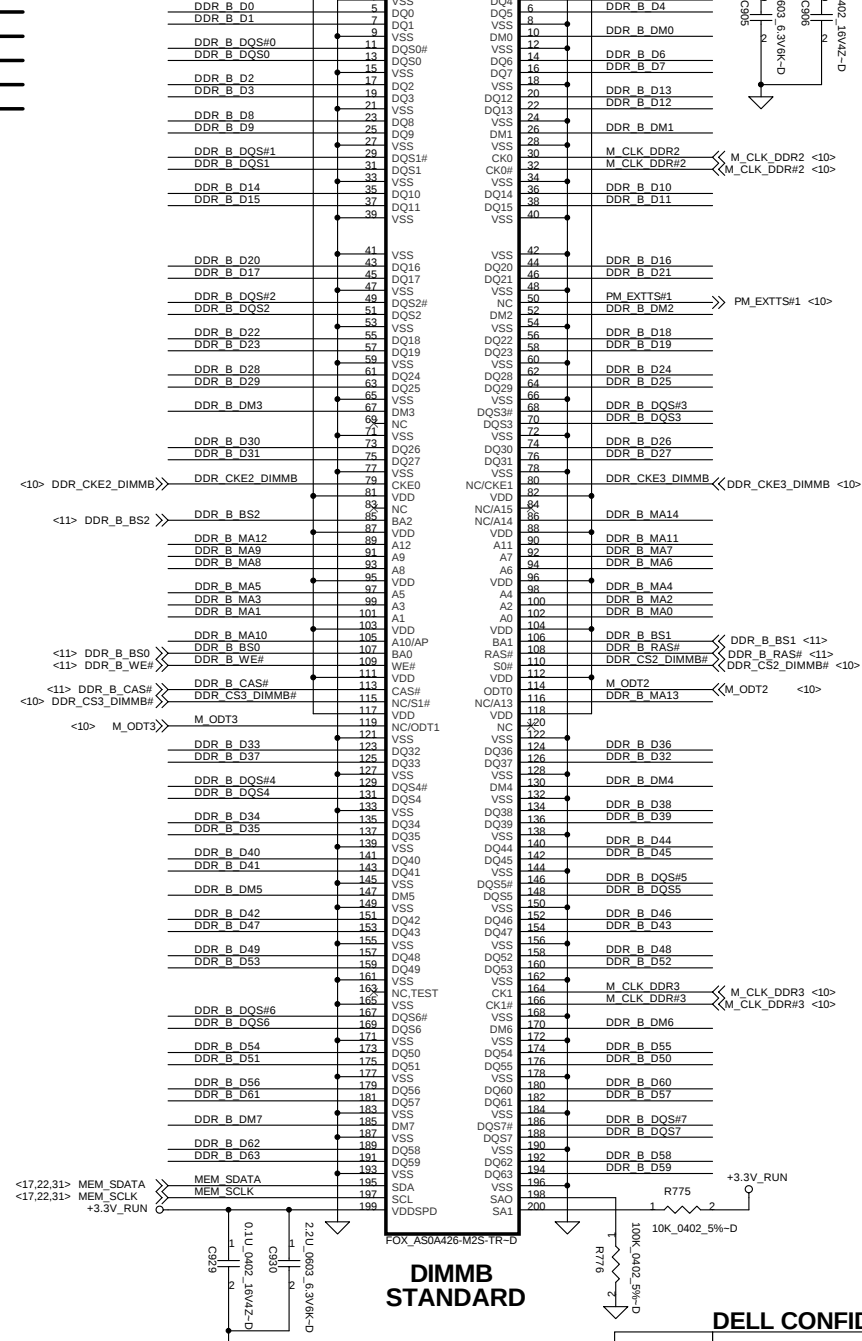
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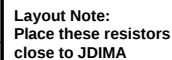
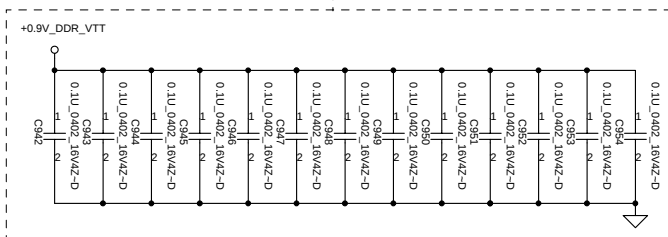
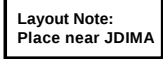
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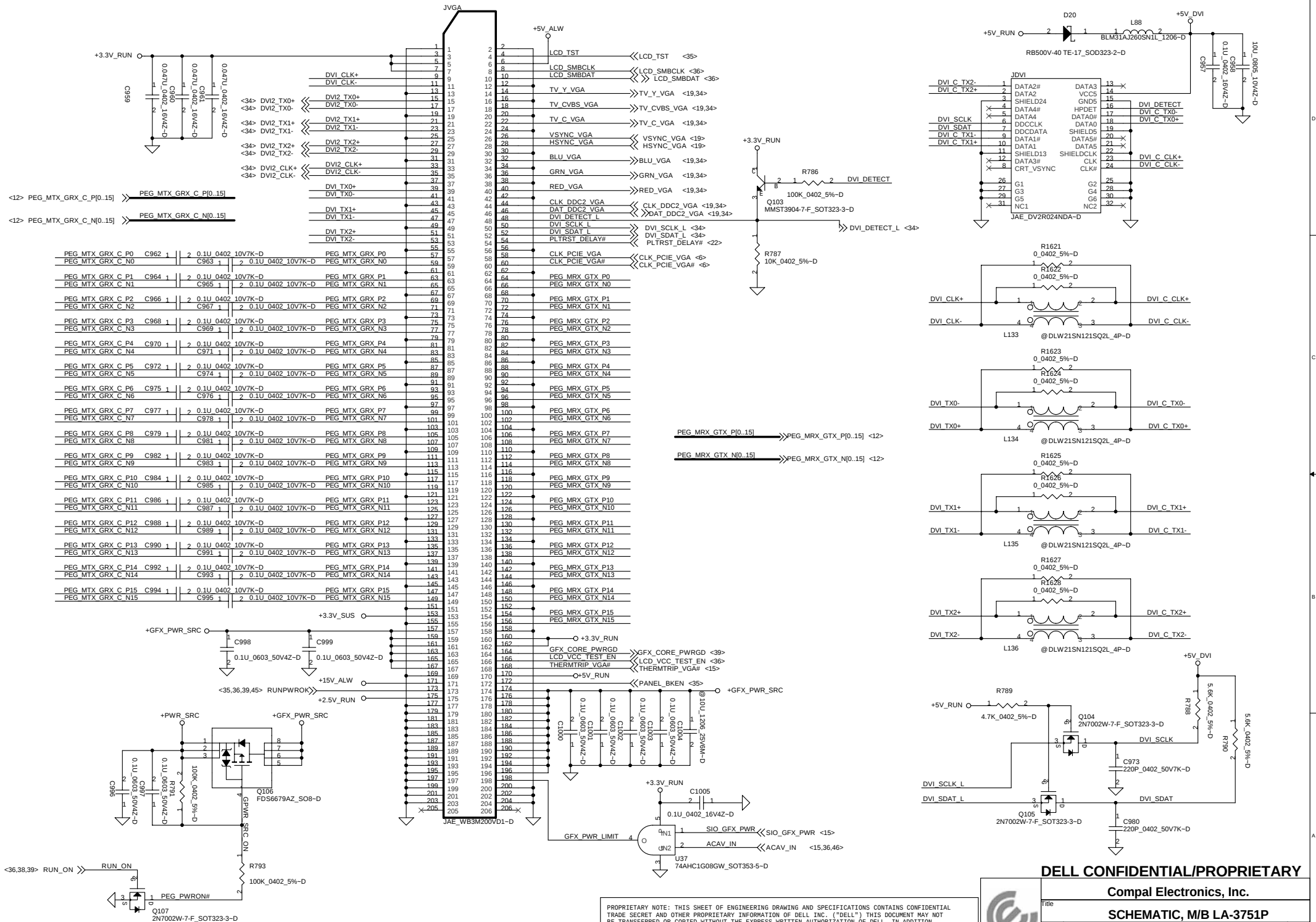
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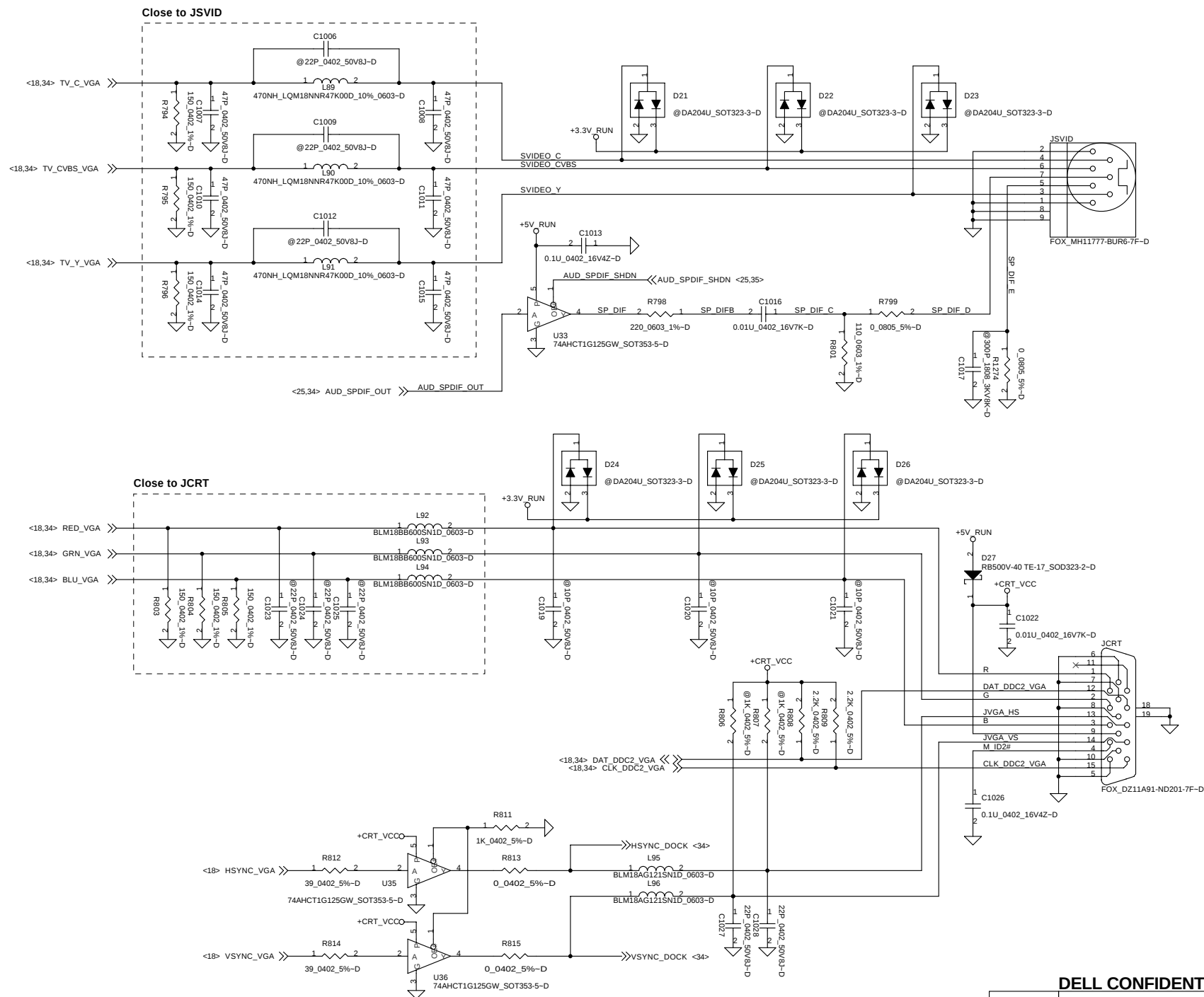


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Place R813 near U35 and R815 near U36

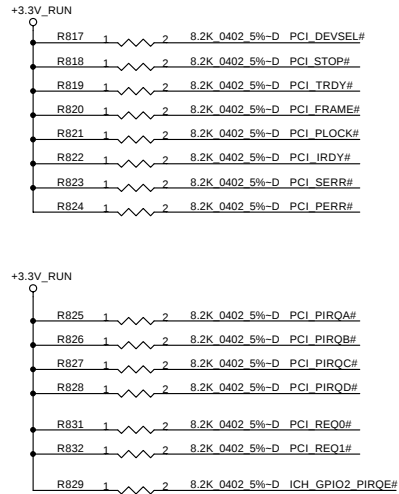
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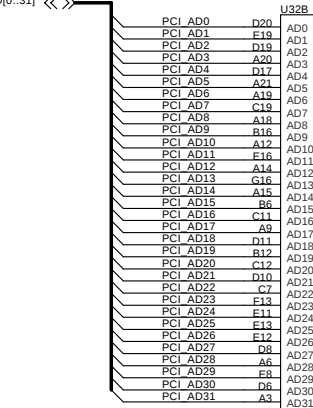
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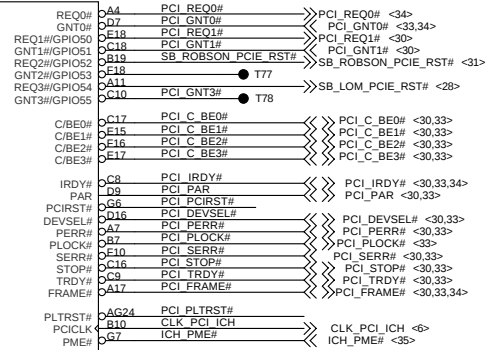
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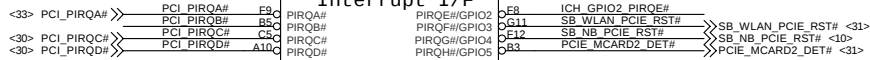
<30,33> PCI_AD[0..31] <<>



PCI

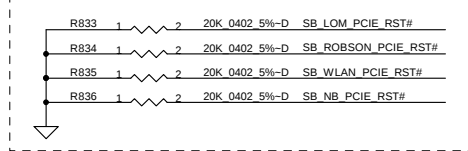


Interrupt I/F



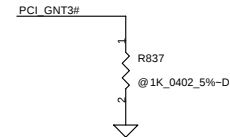
NH82801HEM B1 QN24_BGA676-D

BIOS should not enable the internal GPIO pull up resistor

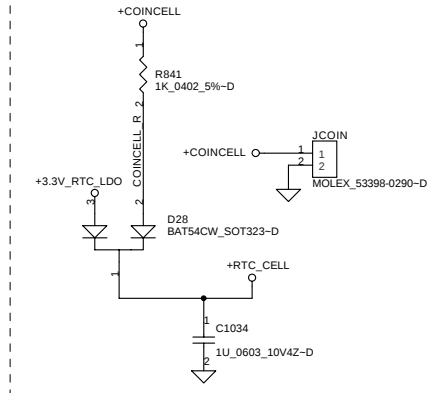


A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled. High = Default.
-----------	---



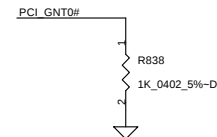
COIN CELL RTC BATTERY



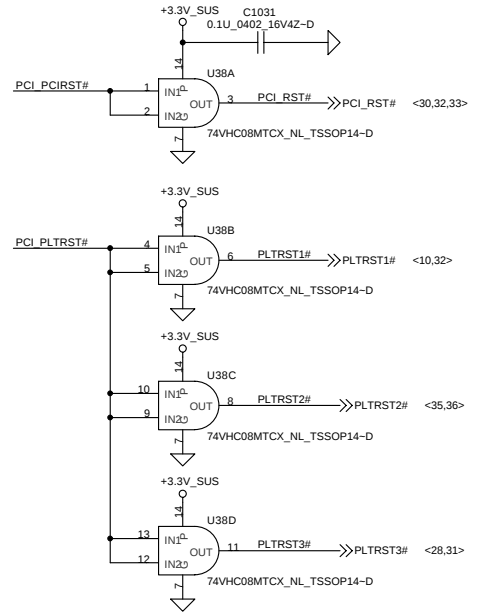
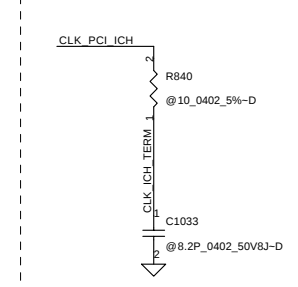
*

BOOT BIOS STRAP

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC



Place close to pin U32.B10



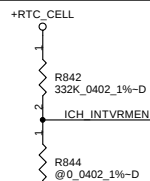
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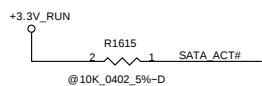
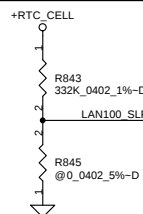
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ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
--------------	---



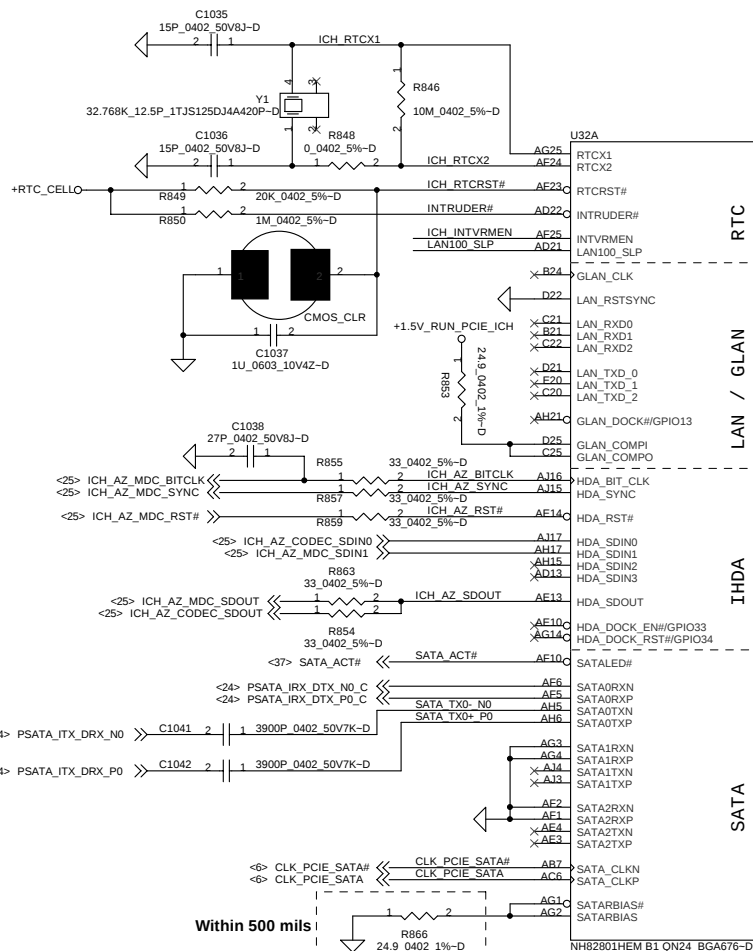
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
----------------	---



<25> ICH_AZ_CODECLK BITCLK <<< 1 R862 ICH_AZ_BITCLK 2 33_0402_5%-D
 1 C1040
 27P_0402_50V8J-D
 P

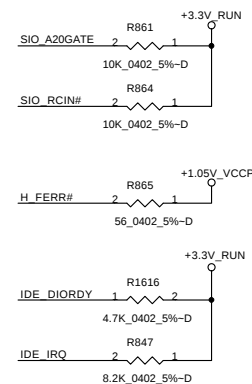
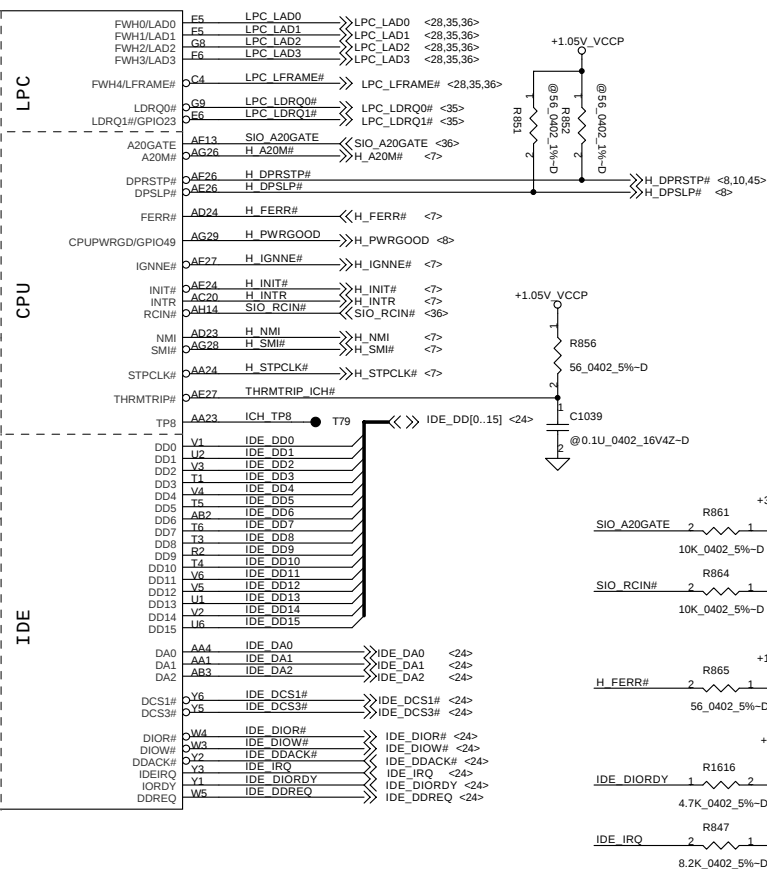
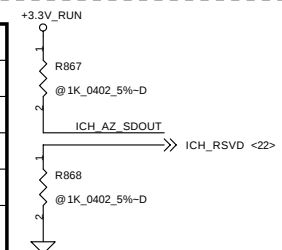
<25> ICH_AZ_CODECLK_SYNC <<< 1 R858 ICH_AZ_SYNC 2 33_0402_5%-D

<25> ICH_AZ_CODECLK_RST# <<< 1 R860 ICH_AZ_RST# 2 33_0402_5%-D



Within 500 mls

XOR Chain Entrance STRAP		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1

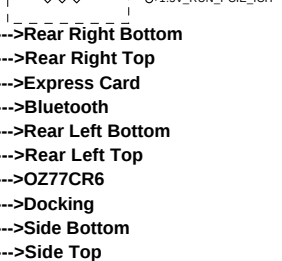
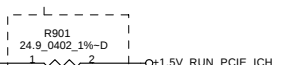
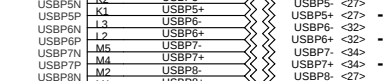
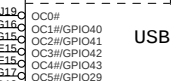
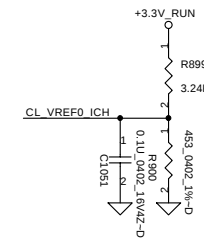
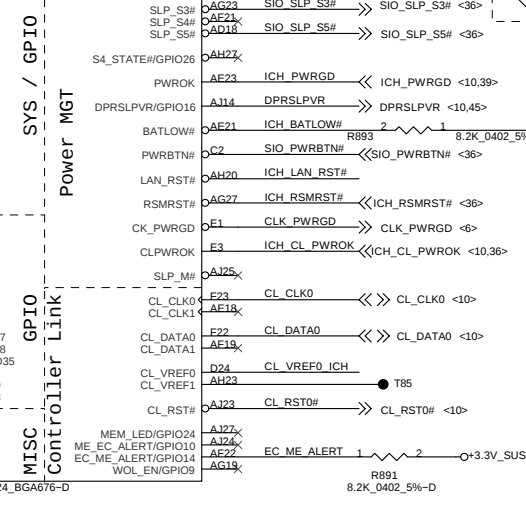
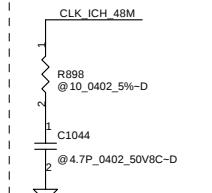
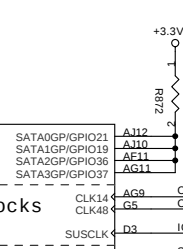


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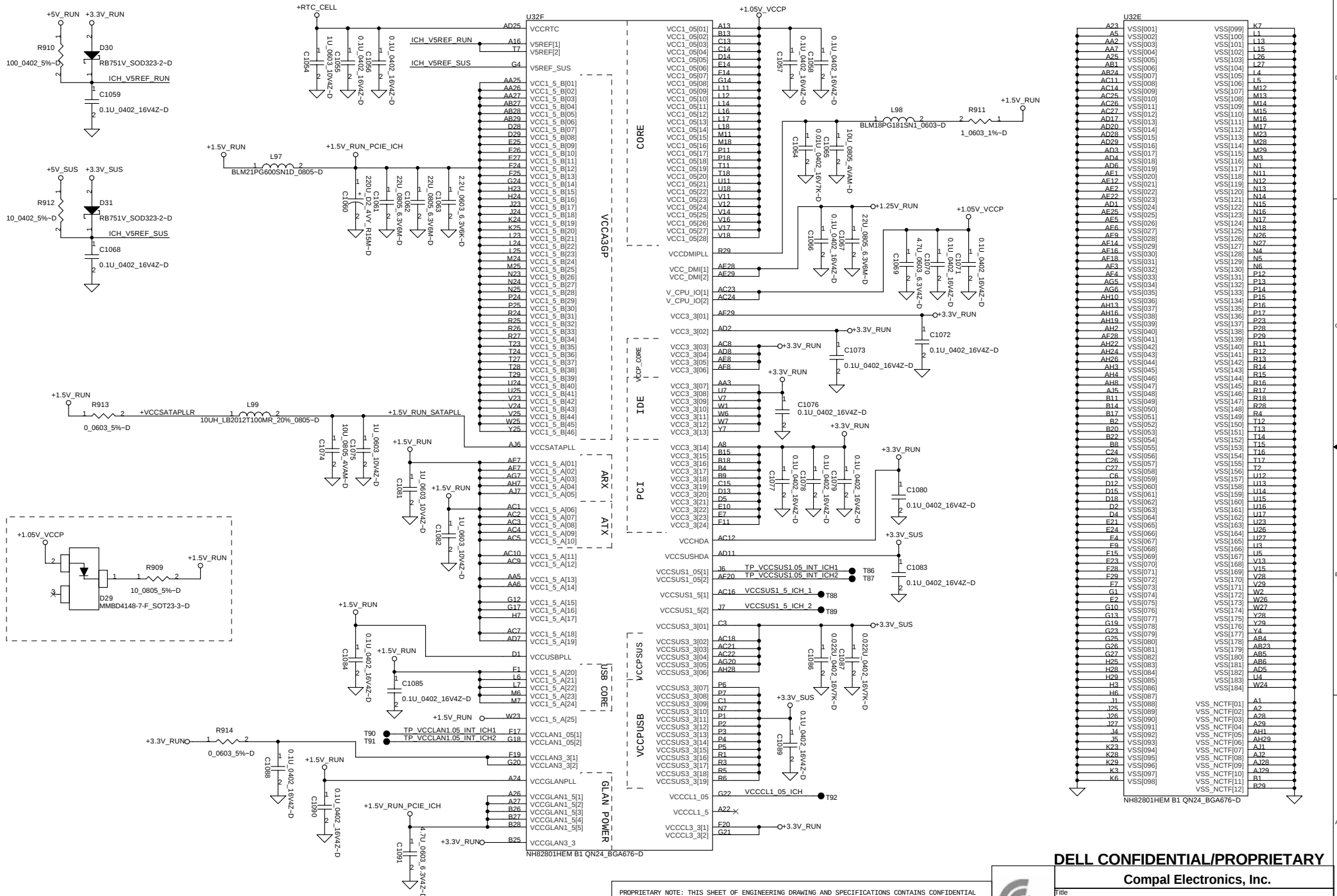
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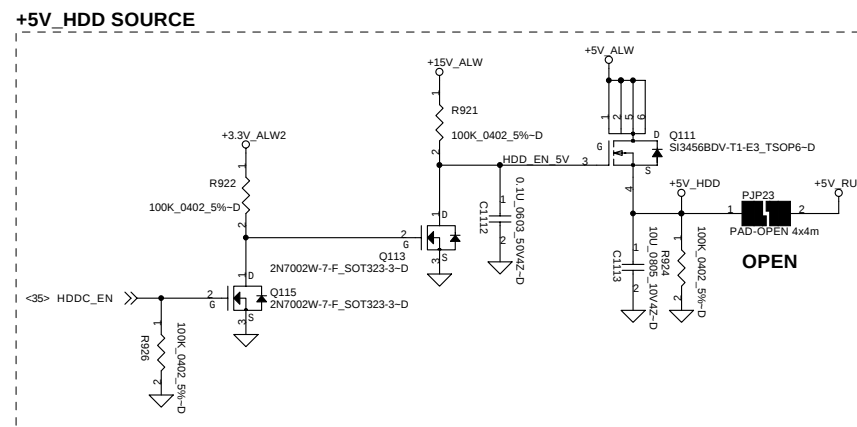
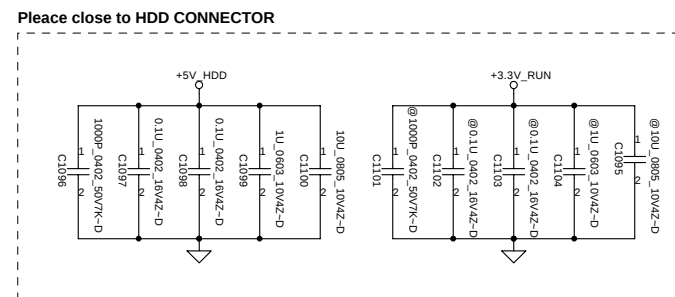
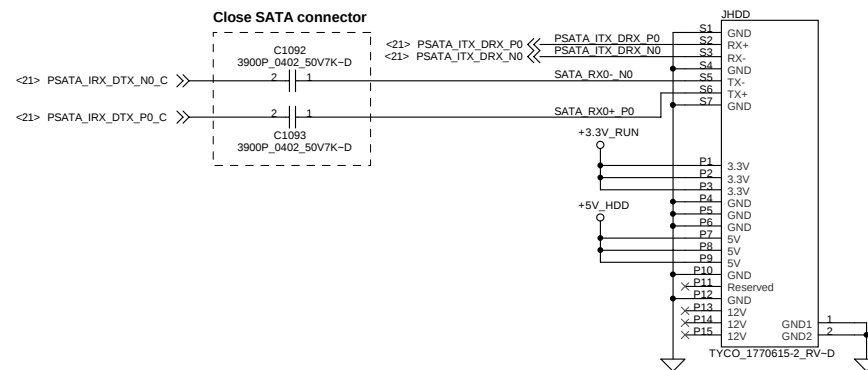
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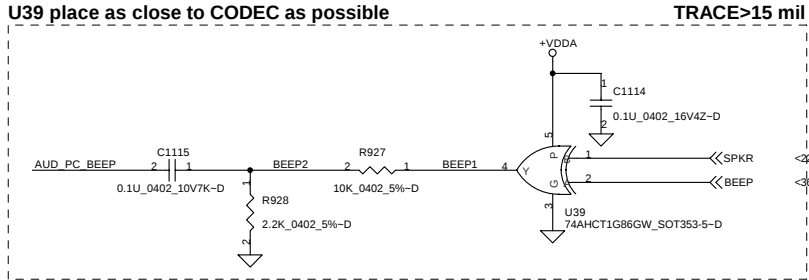
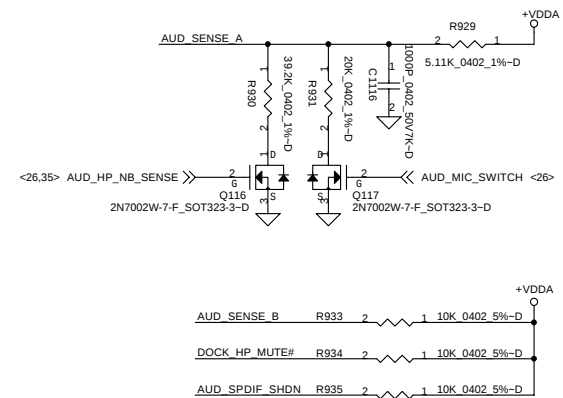
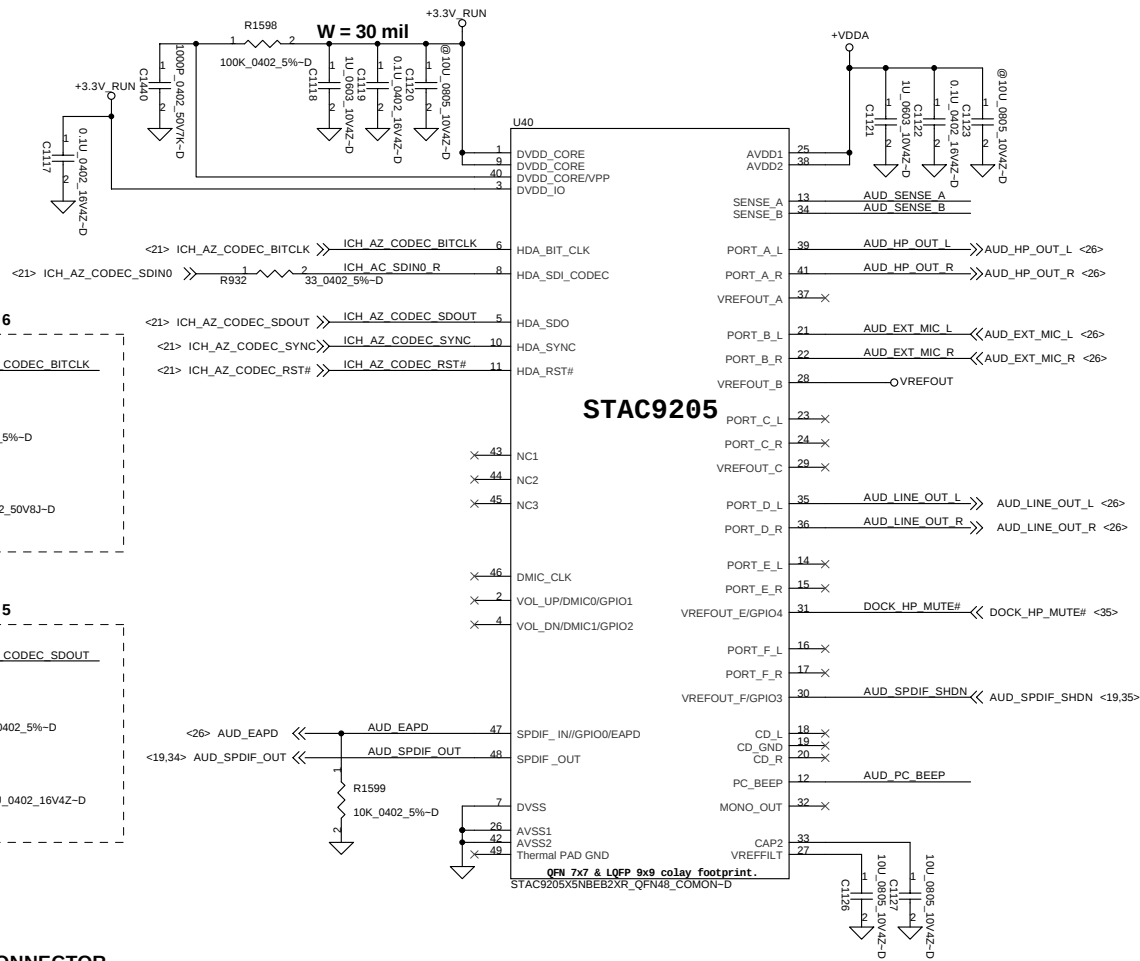
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The schematic shows a pull-up resistor R947 connected to the +5V_AMPVCC supply. A resistor R948 is connected between the AUDIO_AVDD_ON signal and the AUD_AMP_MUTE# pin. The AUD_AMP_MUTE# pin is also labeled @100K_0402_5%-D.

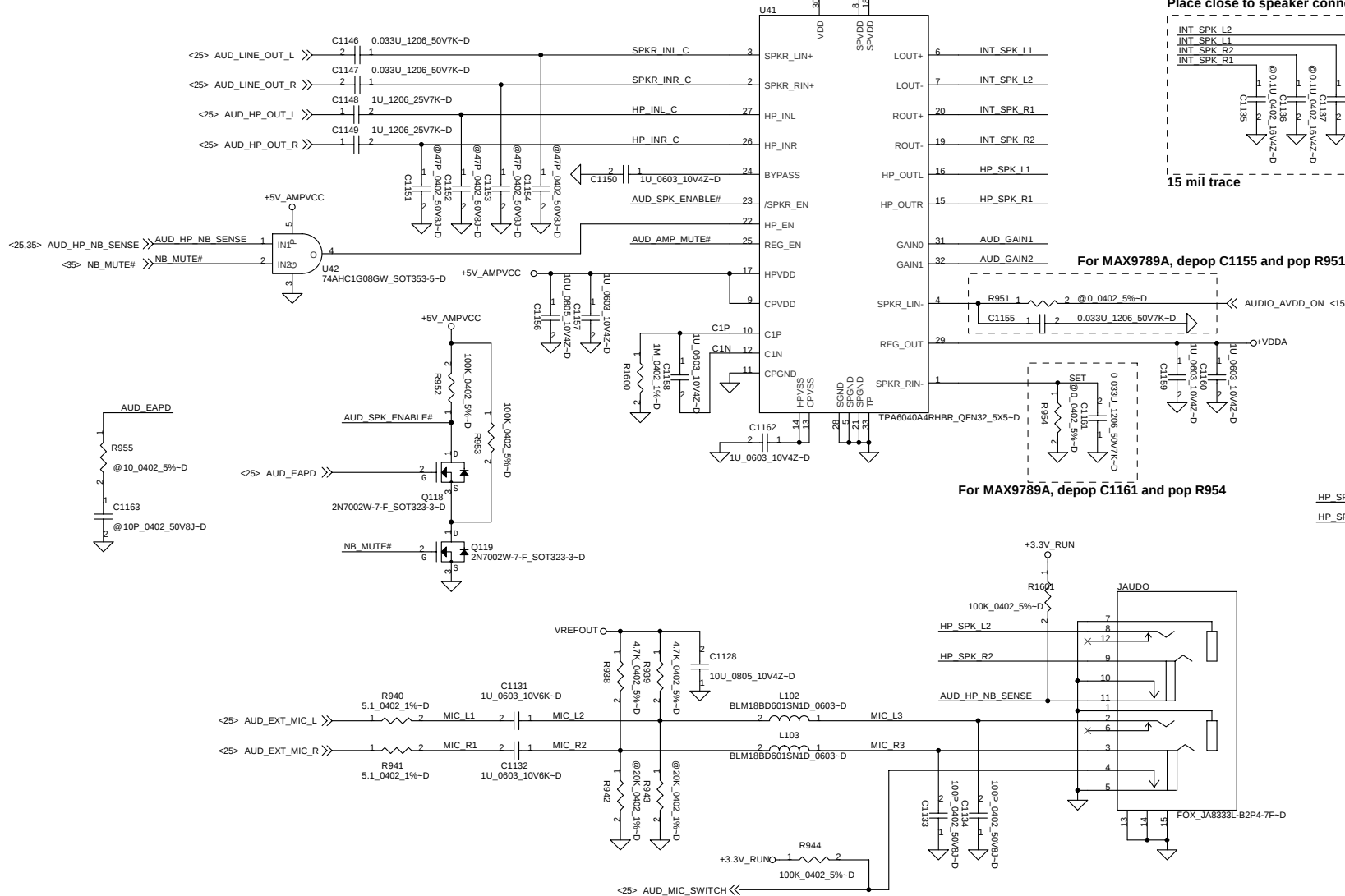
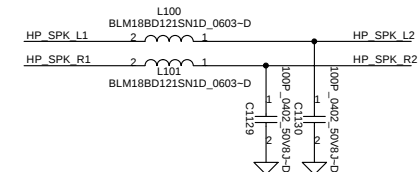
The schematic shows a power distribution network. A +5V_RUN0 input is connected to one terminal of inductor L104. The other terminal of L104 connects to a common rail that branches out to various components. This rail passes through capacitor C1139 and inductor L104's second terminal. It then splits to feed two parallel paths: one path goes through capacitor C1141 and inductor L104's third terminal to a junction before capacitor C1142; the other path goes through capacitor C1140 and inductor L104's fourth terminal to a junction before capacitor C1144. Both paths then lead to a final junction before capacitor C1145. From this final junction, the signal goes through capacitor C1142 and inductor L104's fifth terminal to a junction before capacitor C1146. Finally, it passes through capacitor C1147 and inductor L104's sixth terminal to the +5V_AMPVCC output.

INT SPK R1 1
INT SPK R2 2
INT SPK L1 3
INT SPK L2 4

JSPK
MOLEX_53398-0490-D

For MAX9789A, depop C1161 and pop R954

	GAIN1	GAIN2	AV(inv)	INPUT IMPEDANCE
	0	0	6dB	82K ohm
	0	1	10dB	66K ohm
	1	0	15.6dB	45K ohm
*	1	1	21.6dB	26K ohm



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5.0V

3.3V

REGCTL_PNP12

0.047uF 0.047uF 0.047uF 0.047uF

C126 C126 C126 C126

2.12k 2.12k 2.12k 2.12k

R974 R974 R974 R974

56k 56k 56k 56k

R973 R973 R973 R973

U1 U2

5V 3.3V

10u 0.0805, 10V4Z-D

C1231

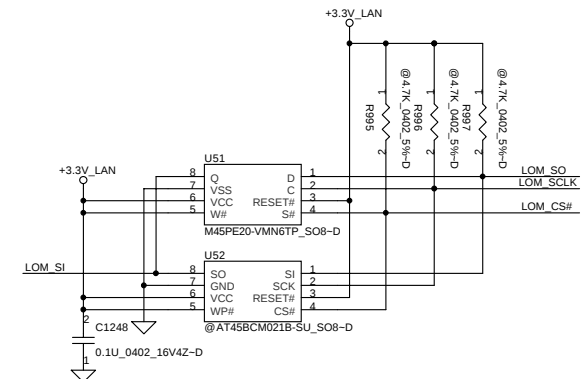
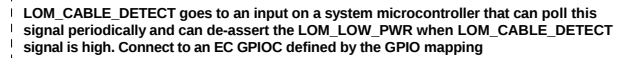
0.1u 0.0402, 16V4Z-D

C1230

1.2V_LAN

Q127

PBSS5540Z_SOT223-3-D



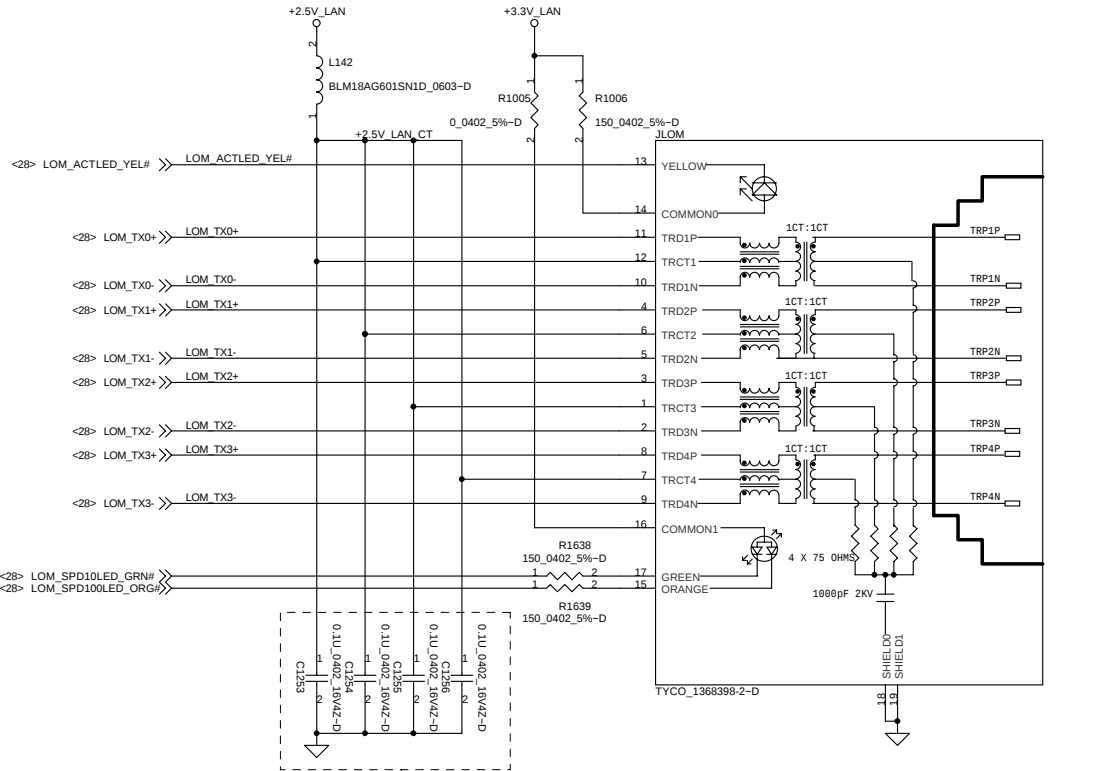
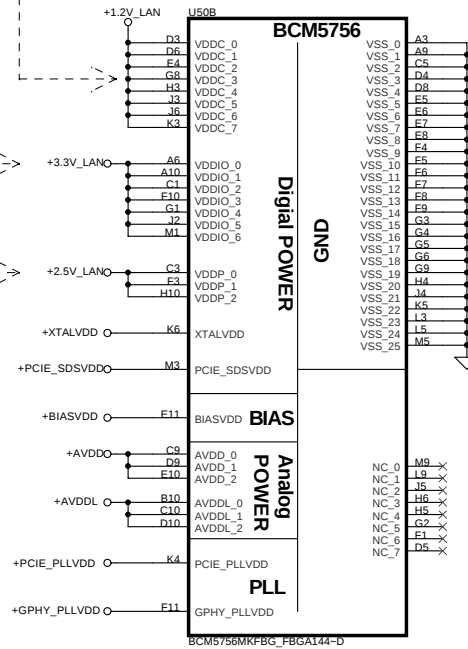
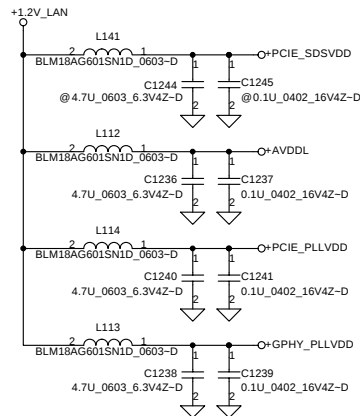
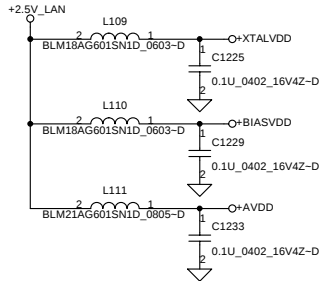
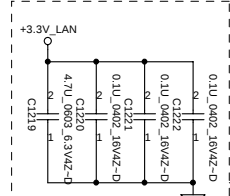
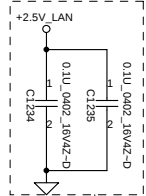
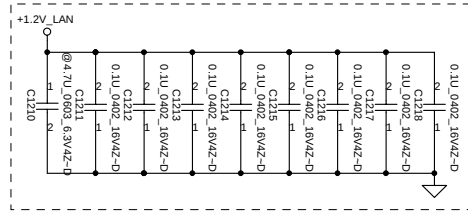
	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1

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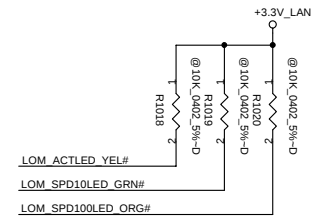


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Place as close as U50 as possible



Place these caps as close to the center tap pins of the mag/connector



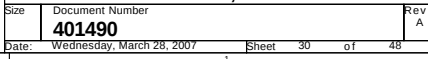
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The schematic diagram illustrates the JMINI1 connector and its associated components. The connector pins are numbered 1 through 54. The diagram shows the following connections and components:

- Power Supply:**
 - +3.3V_RUN:** Connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, and 53.
 - +1.5V_RUN:** Connected to pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, and 54.
- Signal Connections:**
 - PCIE_WAKE#:** Connected to pin 1.
 - MINI1_CLKREQ#:** Connected to pin 3.
 - CLK_PCIE_MINI1#:** Connected to pin 5.
 - CLK_PCIE_MINI1:** Connected to pin 7.
 - PCIE_IRX_ROBSONTX_N1:** Connected to pin 17.
 - PCIE_IRX_ROBSONTX_P1:** Connected to pin 19.
 - PCIE_ITX_ROBSONRX_N1_C:** Connected to pin 31.
 - PCIE_ITX_ROBSONRX_P1_C:** Connected to pin 33.
 - PCIE_MCARD2_DET#:** Connected to pin 41.
 - ROBSON_RADIO_DIS#:** Connected to pin 20.
 - ROBSON_PLTRST3# R:** Connected to pin 22.
 - ROBSON_SCLK:** Connected to pin 24.
 - ROBSON_SDATA:** Connected to pin 26.
 - SB_ROBSON_PCIE_RST#:** Connected to pin 28.
 - MEM_SCLK:** Connected to pin 30.
 - MEM_SDATA:** Connected to pin 32.
 - USB_MCARD2_DET#:** Connected to pin 43.
- Component Values:**
 - R1067:** 100K_0402_5%-D
 - R1068:** 100K_0402_5%-D
 - R1069:** 0_0402_5%-D
 - R1095:** 0_0402_5%-D
 - R1643:** 0_0402_5%-D
 - R1644:** 0_0402_5%-D
 - R1610:** 0_0402_5%-D
 - T96:** 0_0402_5%-D
- Other Components:**
 - C1236:** 33p_0402_50V/3-D
 - C1237:** 33p_0402_50V/3-D
 - C1238:** 33p_0402_50V/3-D
 - C1239:** 33p_0402_50V/3-D
 - C1240:** 33p_0402_50V/3-D
 - C1241:** 33p_0402_50V/3-D
 - C1242:** 33p_0402_50V/3-D
 - C1243:** 33p_0402_50V/3-D
 - C1244:** 33p_0402_50V/3-D
 - C1245:** 33p_0402_50V/3-D
 - C1246:** 33p_0402_50V/3-D
 - C1247:** 33p_0402_50V/3-D
 - C1248:** 33p_0402_50V/3-D
 - C1249:** 33p_0402_50V/3-D
 - C1250:** 33p_0402_50V/3-D
 - C1251:** 33p_0402_50V/3-D
 - C1252:** 33p_0402_50V/3-D
 - C1253:** 33p_0402_50V/3-D
 - C1254:** 33p_0402_50V/3-D
 - C1255:** 33p_0402_50V/3-D
 - C1256:** 33p_0402_50V/3-D
 - C1257:** 33p_0402_50V/3-D
 - C1258:** 33p_0402_50V/3-D
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 - C1282:** 33p_0402_50V/3-D
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 - C1298:** 33p_0402_50V/3-D
 - C1299:** 33p_0402_50V/3-D
 - C1300:** 33p_0402_50V/3-D

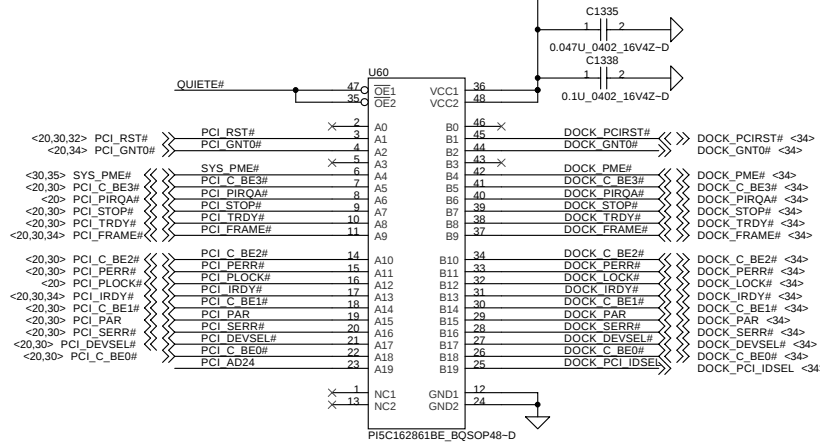
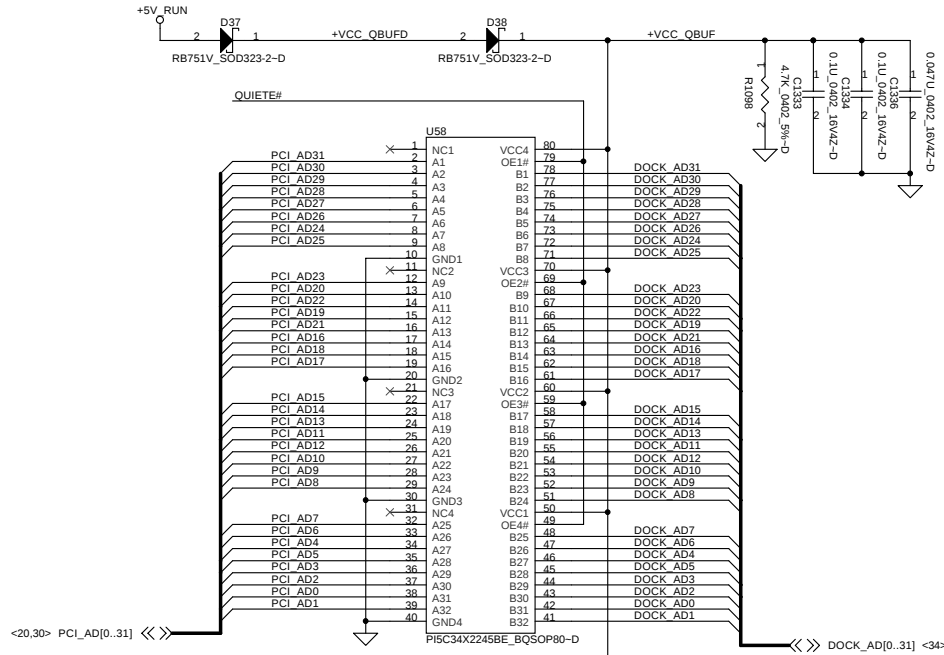
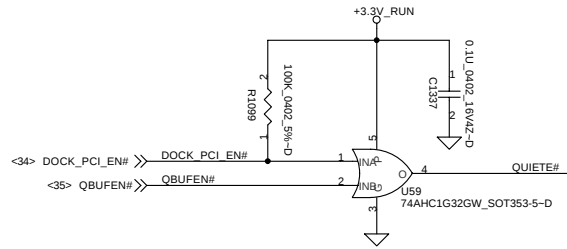
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+1.5V_CARD: Max. 650mA, Average 500mA
+3.3V_CARD: Max. 1300mA, Average 1000mA

[illegible]

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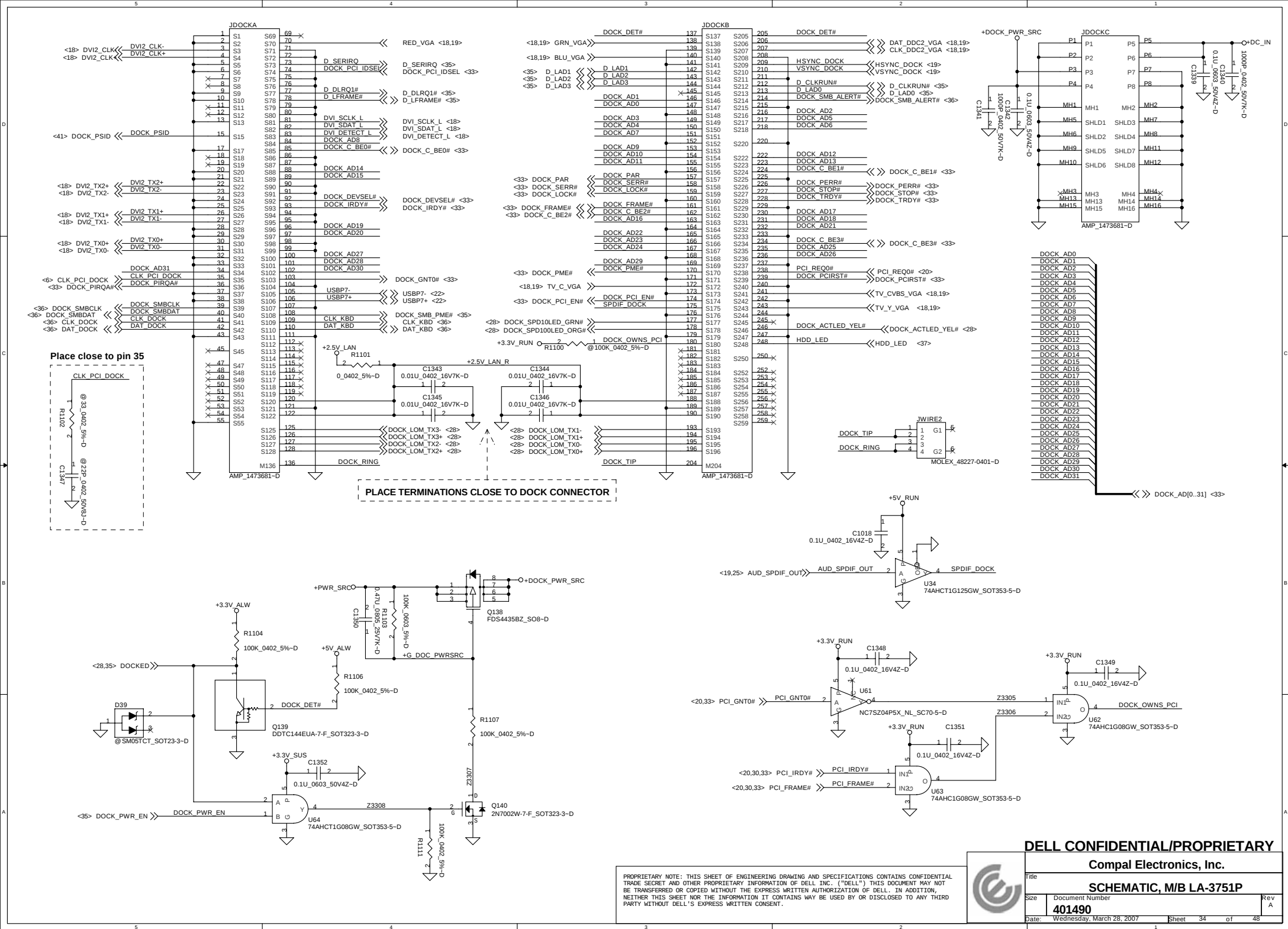
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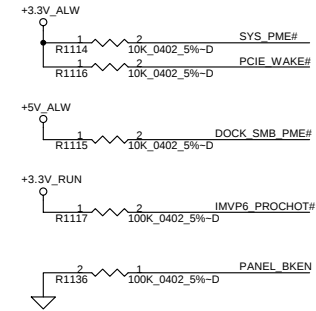
Compal Electronics, Inc.

Schematic, M/B LA-3751P

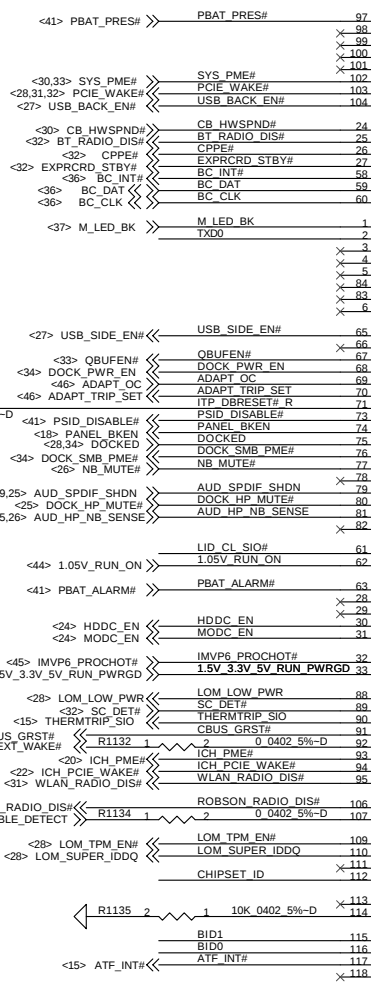
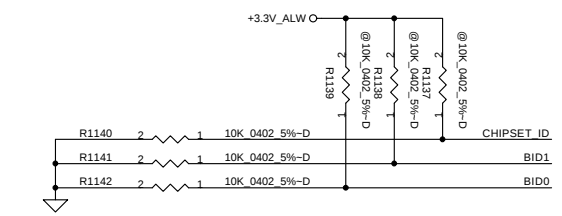
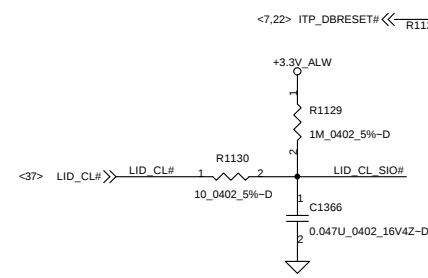
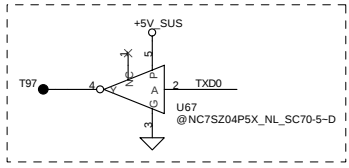
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Note: For system debug pin4 connect to serial port pin3



REV	BID1	BID0
X00	0	0
X01	0	1

ECE5028-NU (ECE5018)

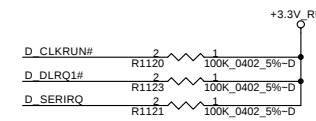
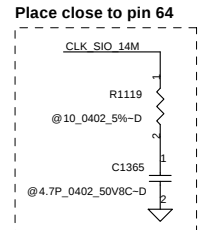
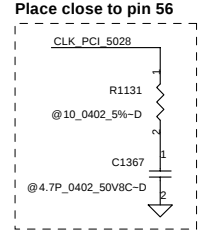
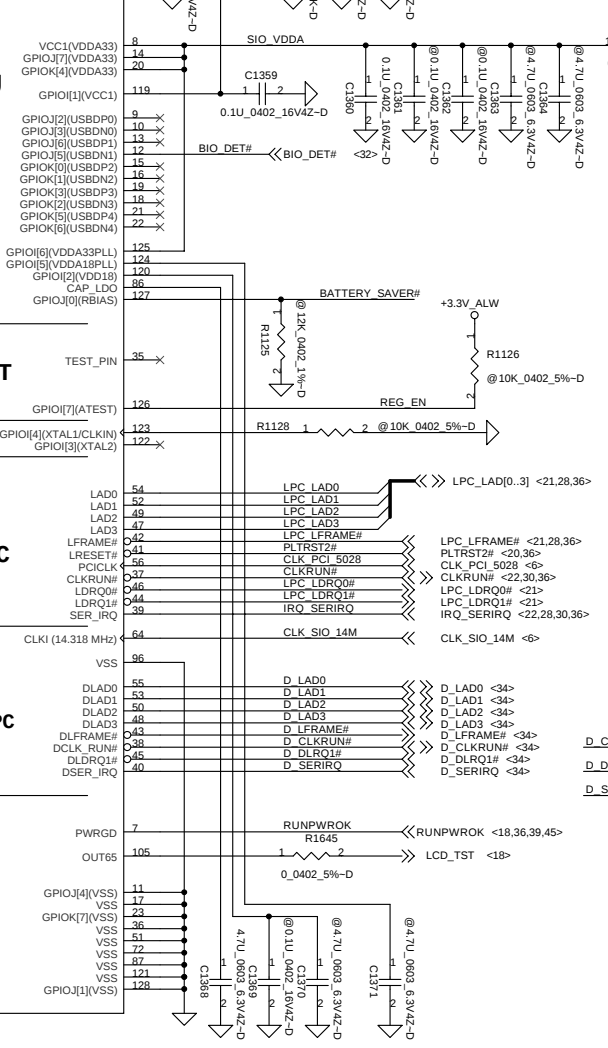
USB

TEST

CLK

LPC

DLPC



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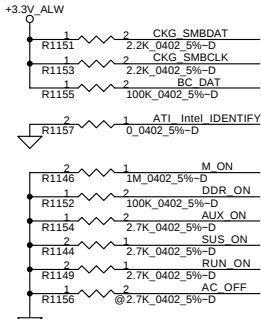
Compal Electronics, Inc.

SCHEMATIC, M/B LA-3751P

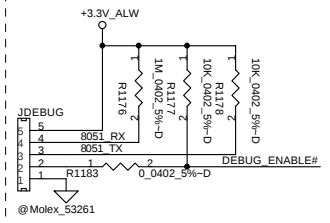
401490

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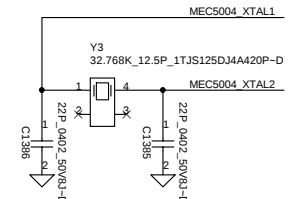
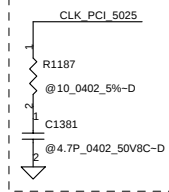
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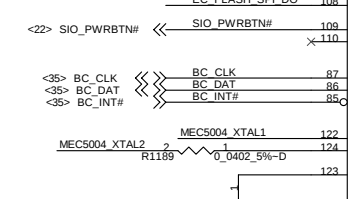
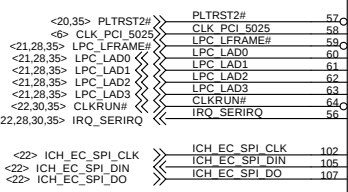
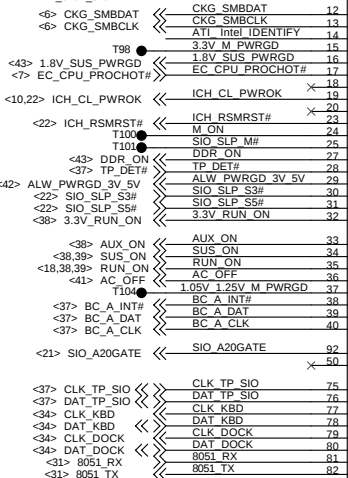
R1752 no stuff when doing flash recovery



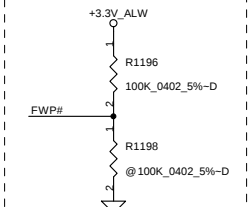
Place close to pin 58



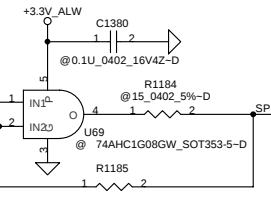
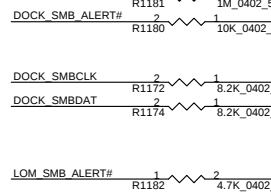
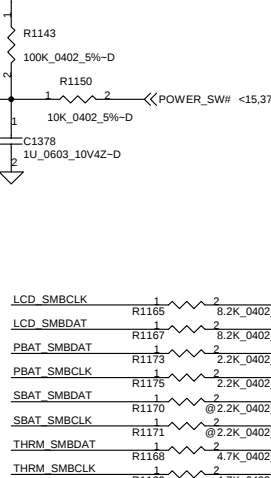
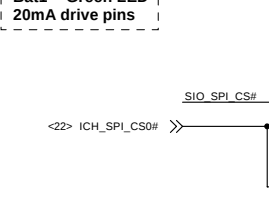
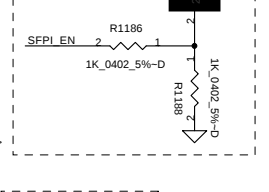
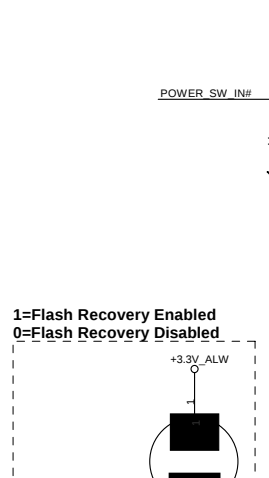
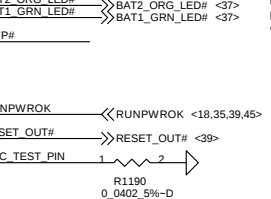
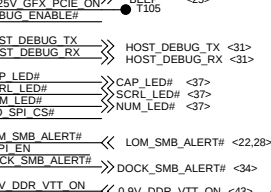
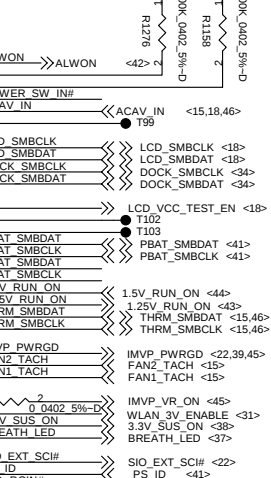
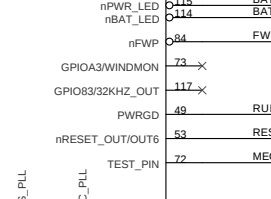
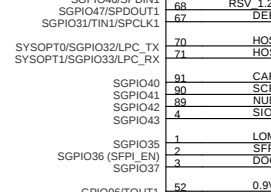
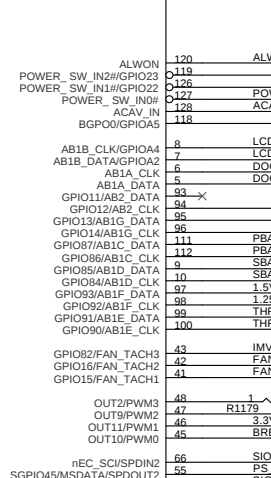
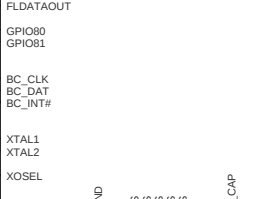
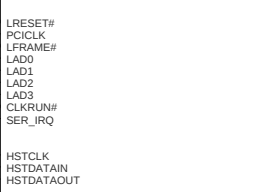
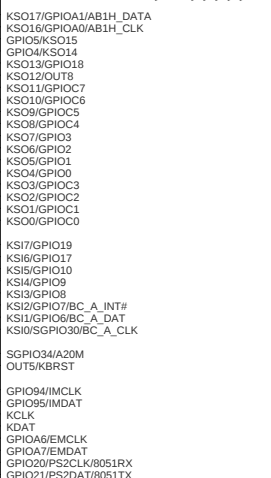
Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
CH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA
LOM_LOW_PWR	NC	Refer to UMA
LOM_CABLE_DETECT	NC	Refer to UMA



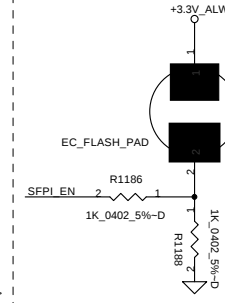
low=write protected



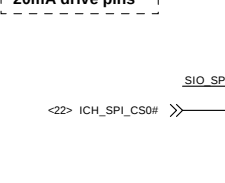
Flash write protect bottom 4K of internal bootblock flash



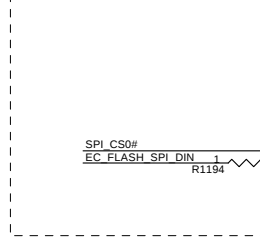
1=Flash Recovery Enabled
0=Flash Recovery Disabled



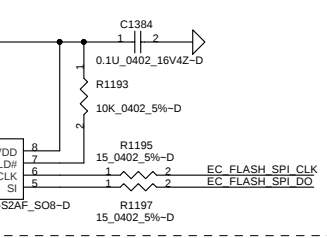
Bat2 = Amber LED
Bat1 = Green LED
20mA drive pins



Place R1194 close to Flash ROM.



Place R1195 and R1197 close to EMC5025.

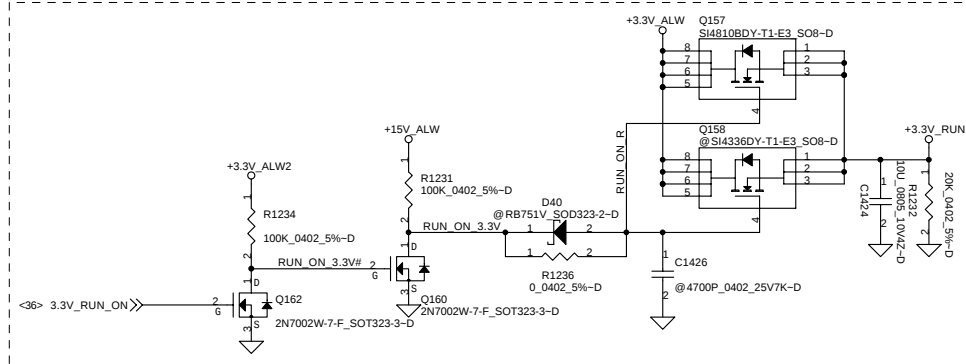


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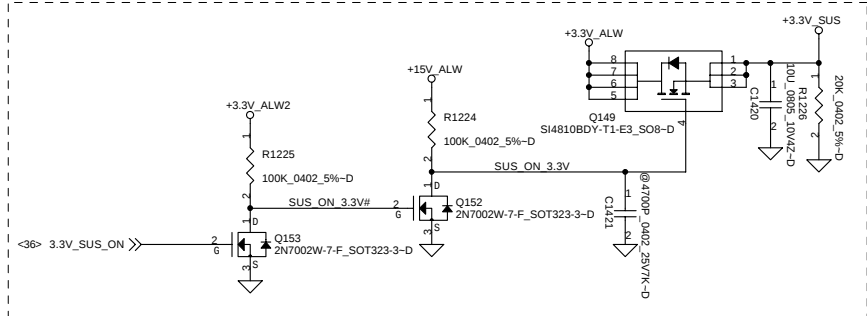


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SCHEMATIC, M/B LA-3751P			
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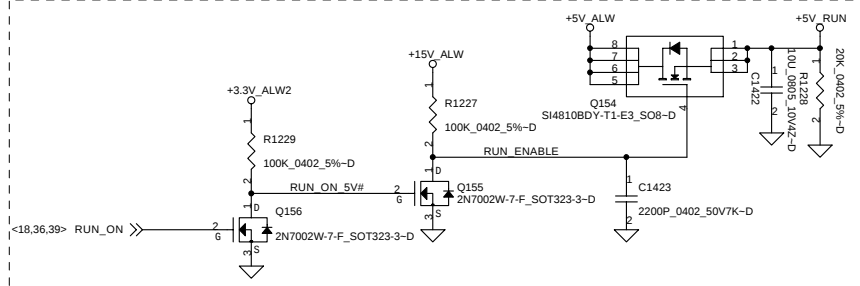
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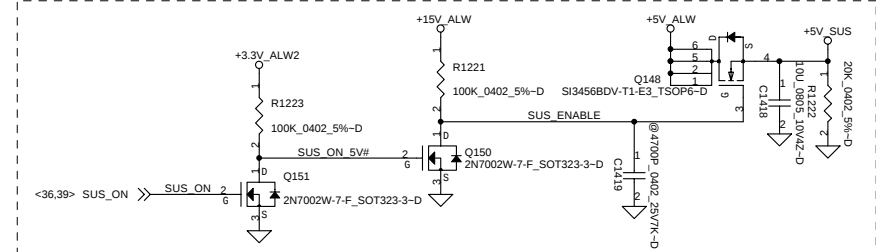
+3.3V_SUS Source



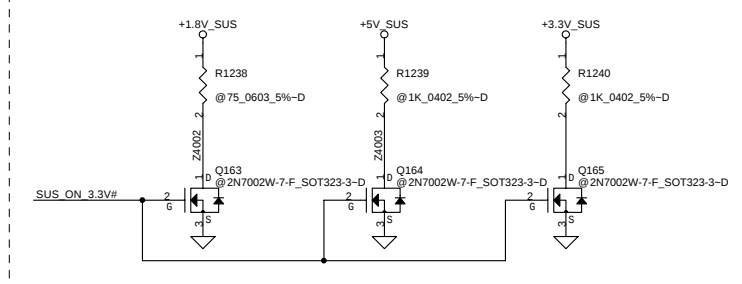
+5V_RUN Source



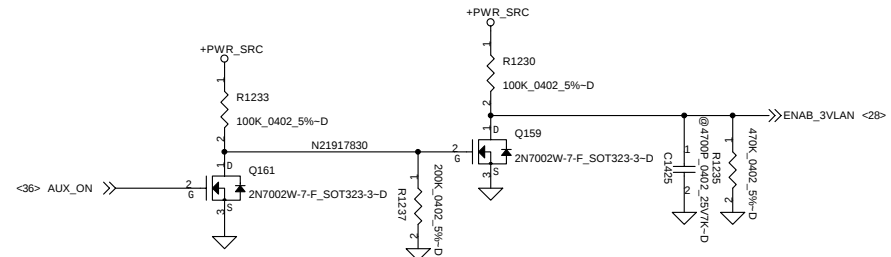
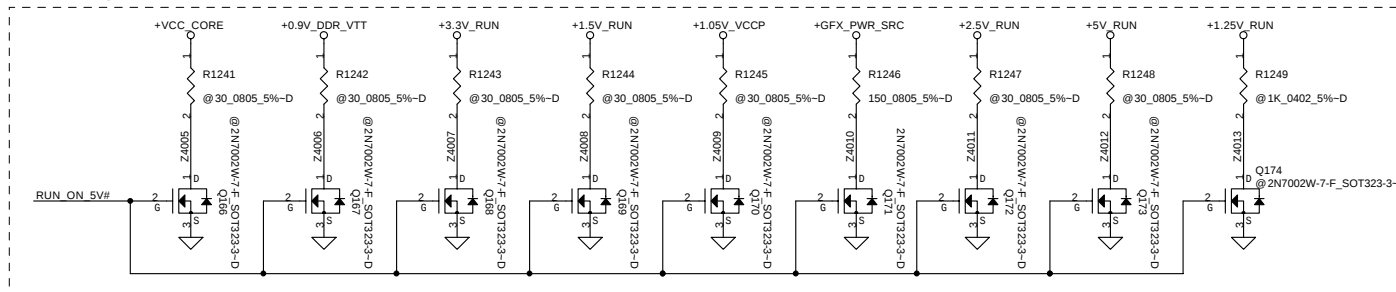
+5V_SUS Source



Discharg Circuit



Discharg Circuit



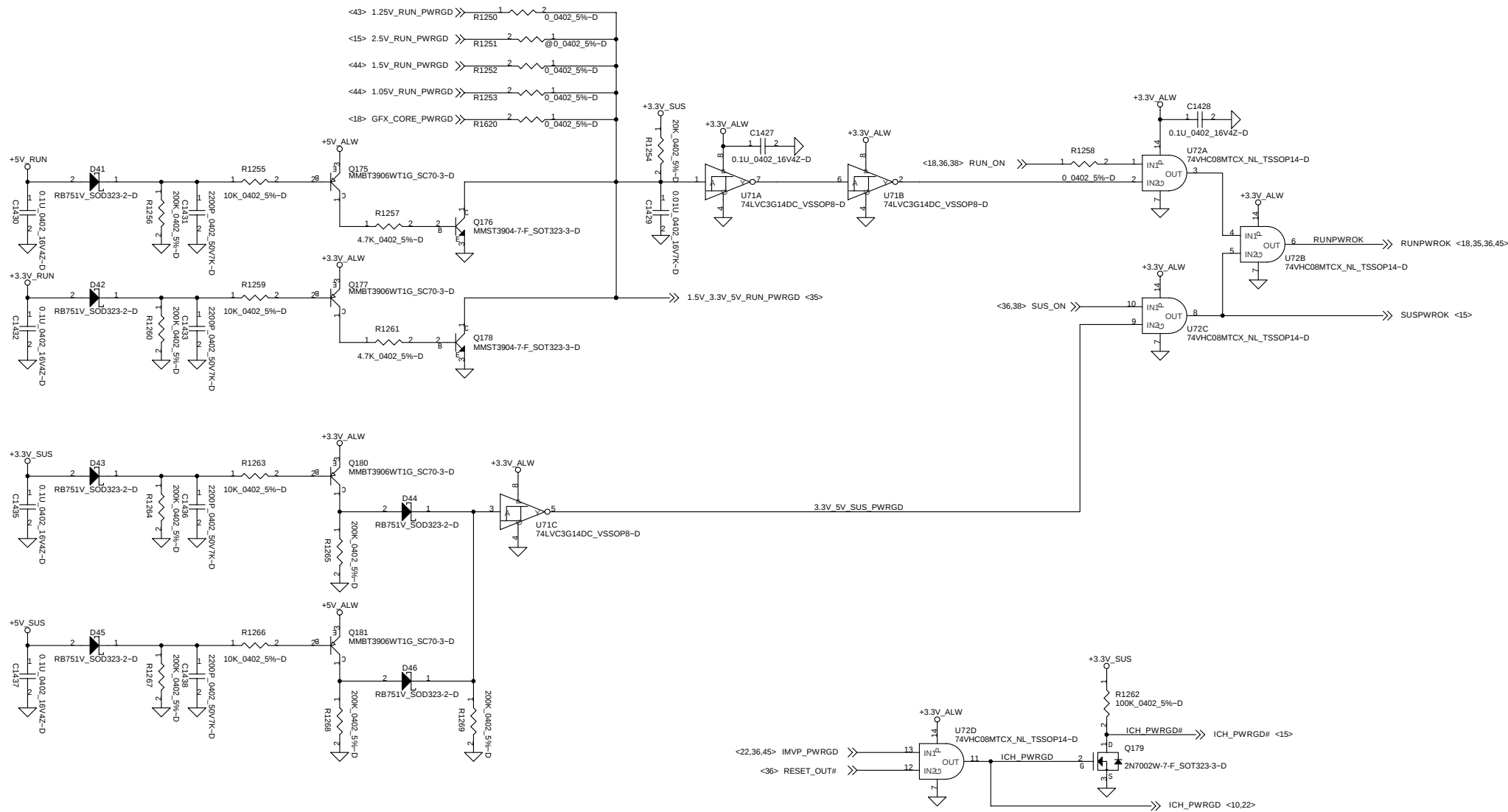
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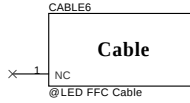
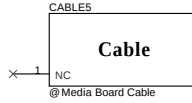
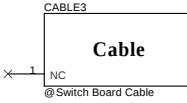
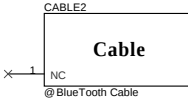
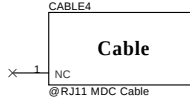
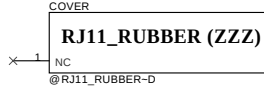
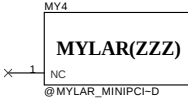
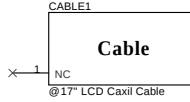
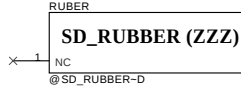
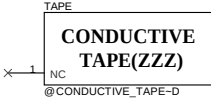
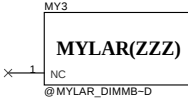
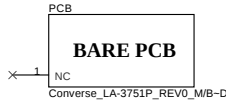
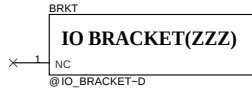
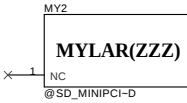
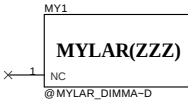
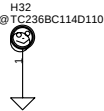
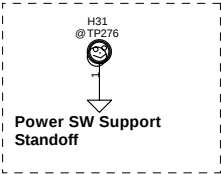
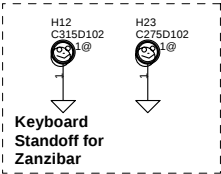
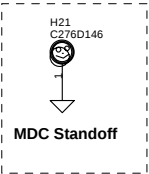
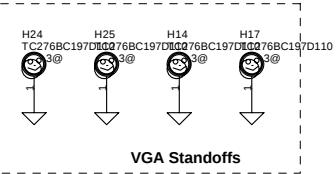
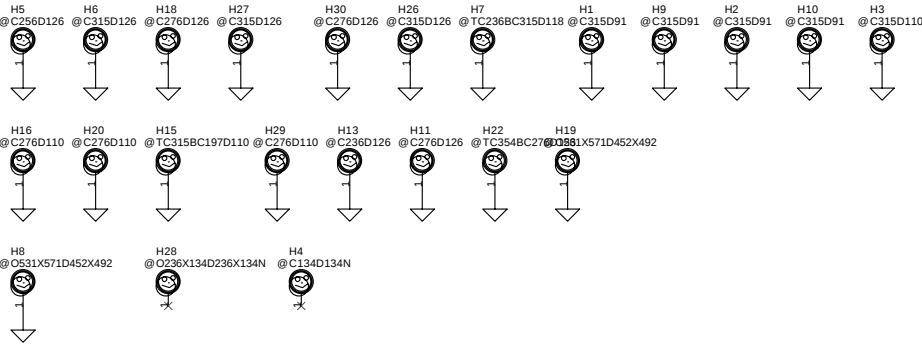
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HEX STANDOFF



Fiducial Mark



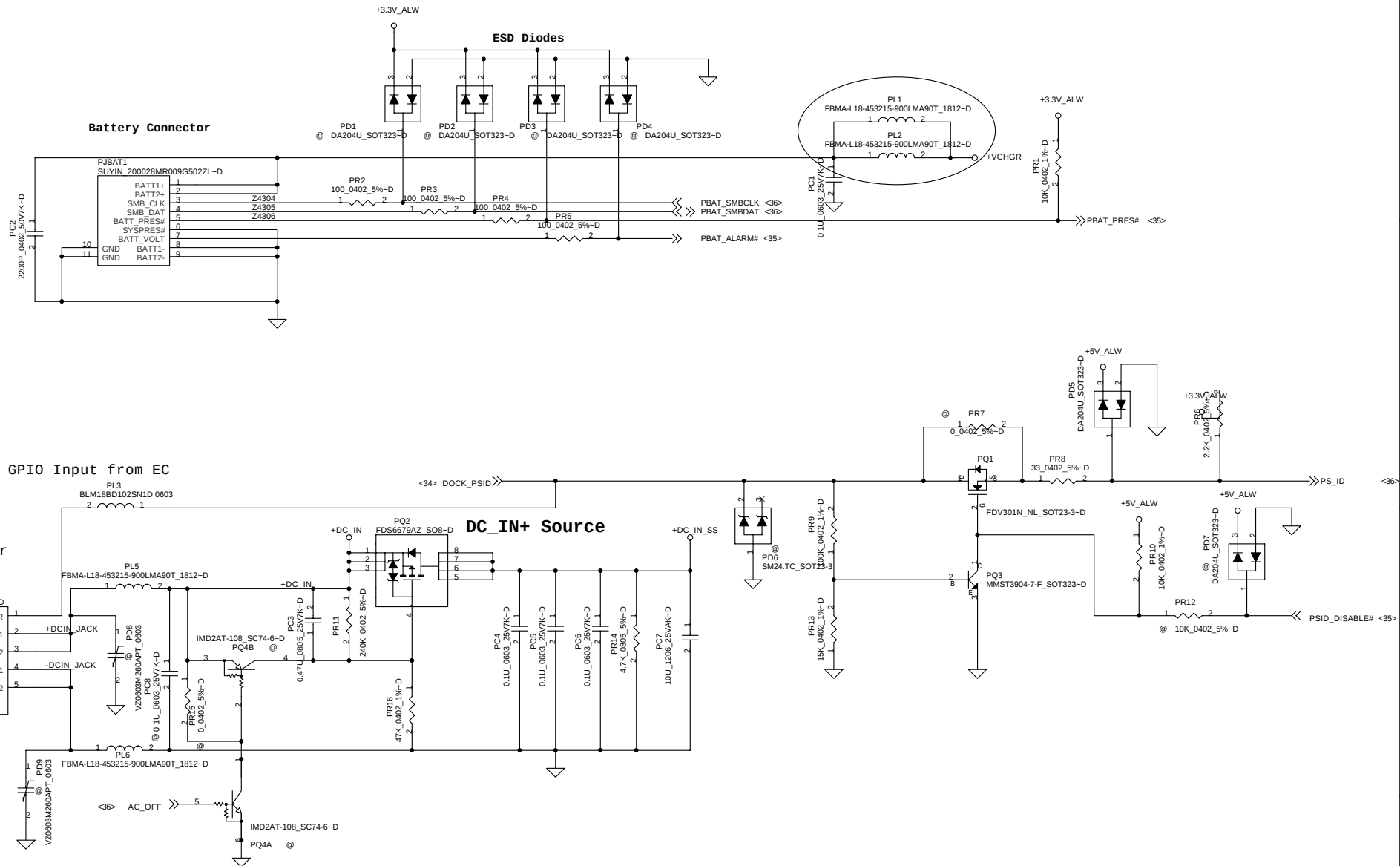
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Size: Document Number **401490** Rev A

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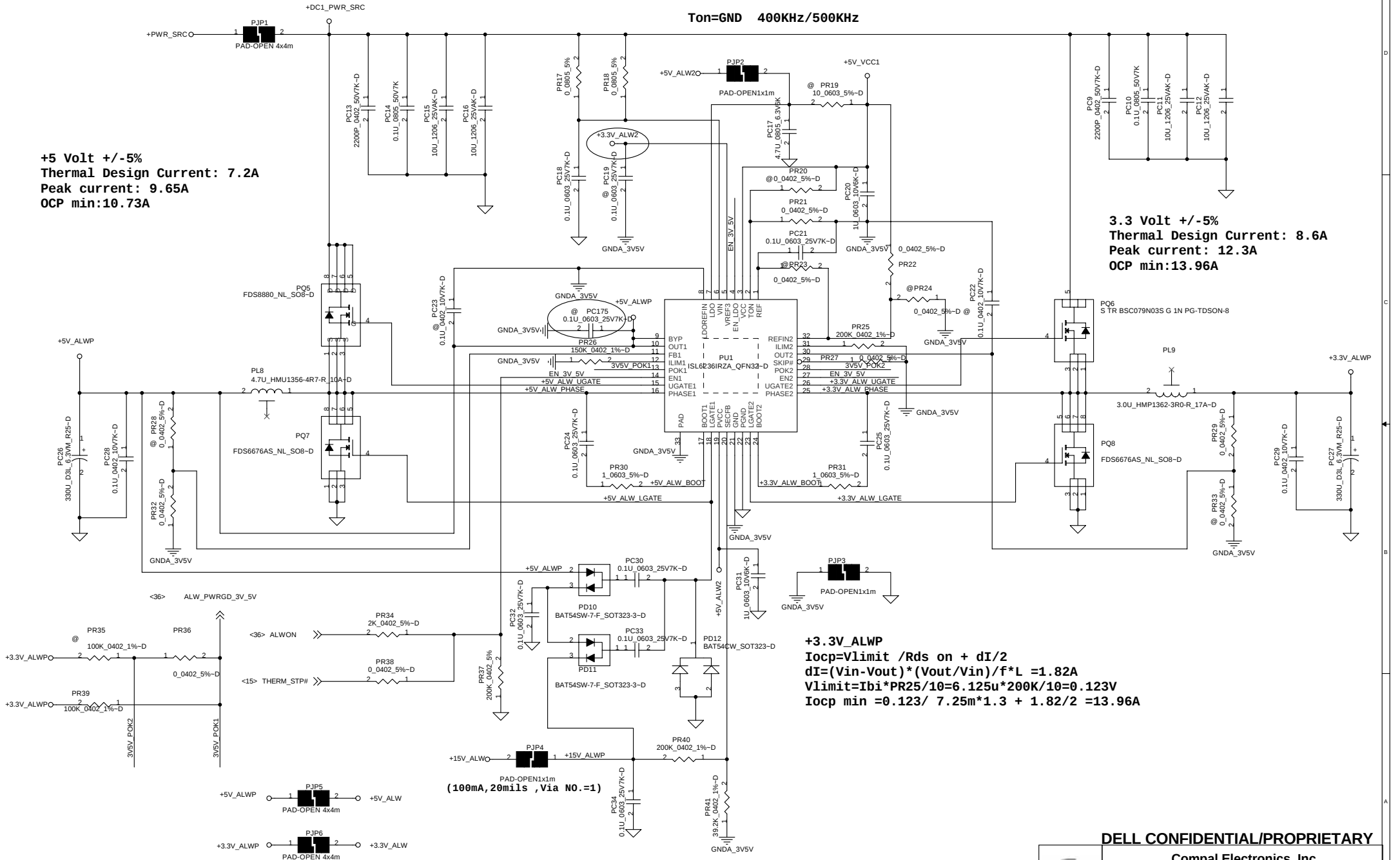
+5V_ALWP
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 1.96A$
 $V_{limit} = I_{bi} * PR26 / 10 = 6.125u * 150K / 10 = 0.92V$
 $I_{ocp\ min} = 0.92 / 7.25m * 1.3 + 1.96 / 2 = 10.73A$

+3.3V_ALWP/ +5V_ALWP/ +5V_ALW2 / +15V_ALWP/+15V_SUBW00FERP

Ton=GND 400KHz/500KHz

+5 Volt +/-5%
Thermal Design Current: 7.2A
Peak current: 9.65A
OCp min:10.73A

3.3 Volt +/-5%
Thermal Design Current: 8.6A
Peak current: 12.3A
OCp min:13.96A



+3.3V_ALWP
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 1.82A$
 $V_{limit} = I_{bi} * PR25 / 10 = 6.125u * 200K / 10 = 0.123V$
 $I_{ocp\ min} = 0.123 / 7.25m * 1.3 + 1.82 / 2 = 13.96A$

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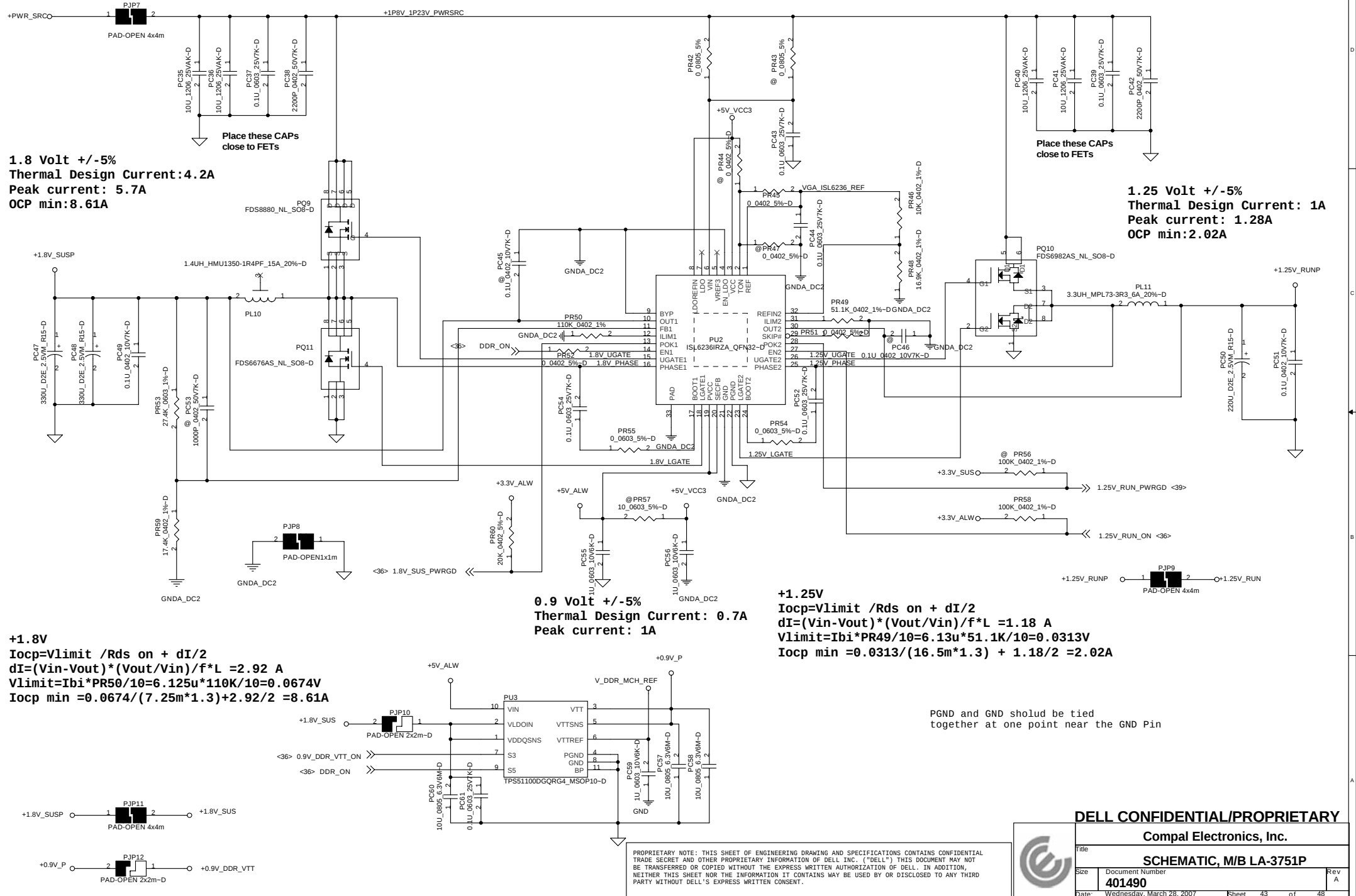
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1.8V/1.25V/0.9V VTT

Ton=REF 400KHz/300KHz



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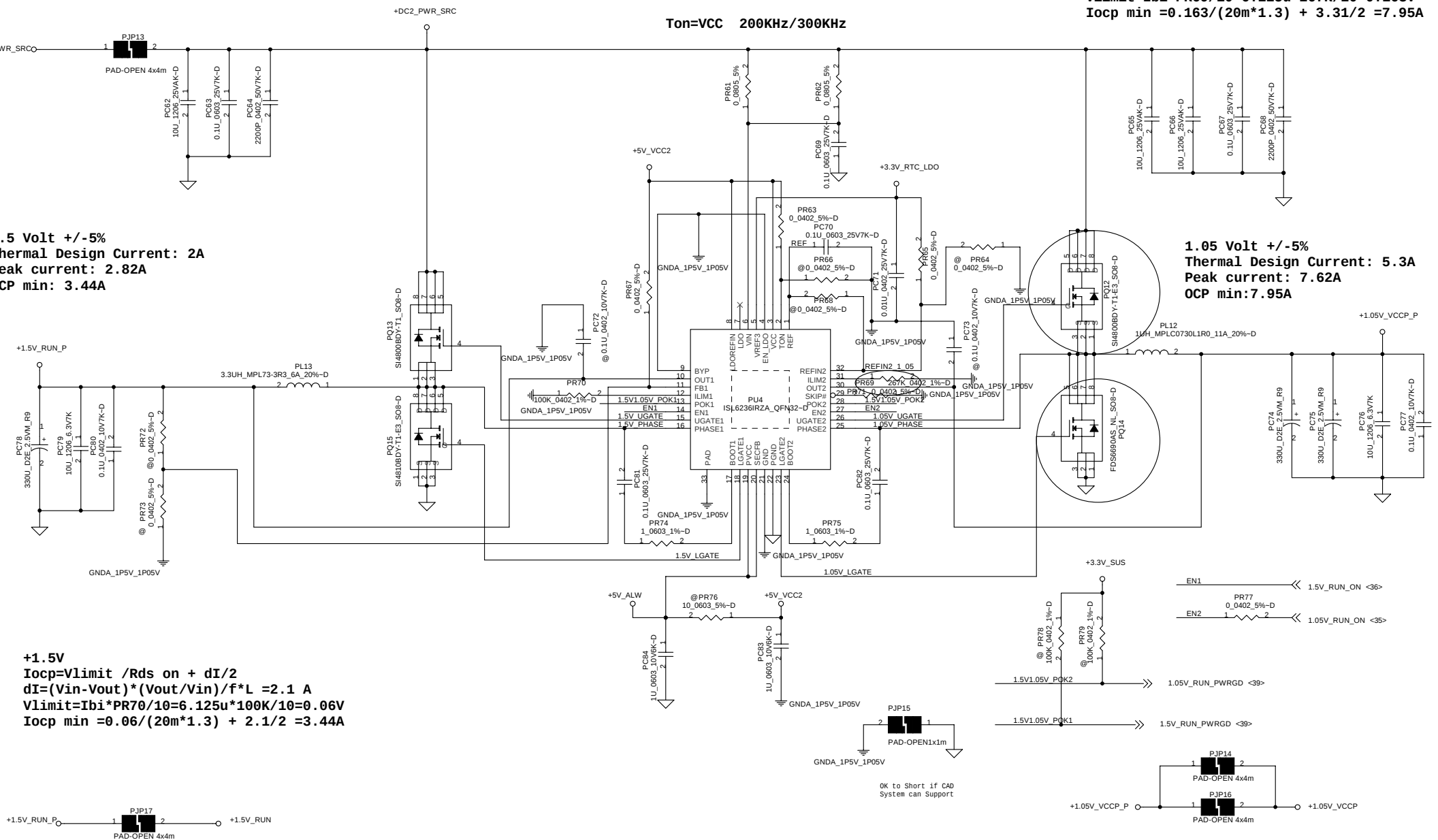
1.5 Volt +/-5%
Thermal Design Current: 2A
Peak current: 2.82A
OCP min: 3.44A

+1.5V_RUN / +1.05V_VCCP / +3.3V_ALW / +3.3V_RTC_LDO

Ton=VCC 200KHz/300KHz

+1.05V
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 3.31A$
 $V_{limit} = I_{bi} * PR69 / 10 = 6.125u * 267K / 10 = 0.163V$
 $I_{ocp\ min} = 0.163 / (20m * 1.3) + 3.31 / 2 = 7.95A$

1.05 Volt +/-5%
Thermal Design Current: 5.3A
Peak current: 7.62A
OCP min: 7.95A



+1.5V
 $I_{ocp} = V_{limit} / R_{ds\ on} + dI/2$
 $dI = (V_{in} - V_{out}) * (V_{out} / V_{in}) / f * L = 2.1 A$
 $V_{limit} = I_{bi} * PR70 / 10 = 6.125u * 100K / 10 = 0.06V$
 $I_{ocp\ min} = 0.06 / (20m * 1.3) + 2.1 / 2 = 3.44A$

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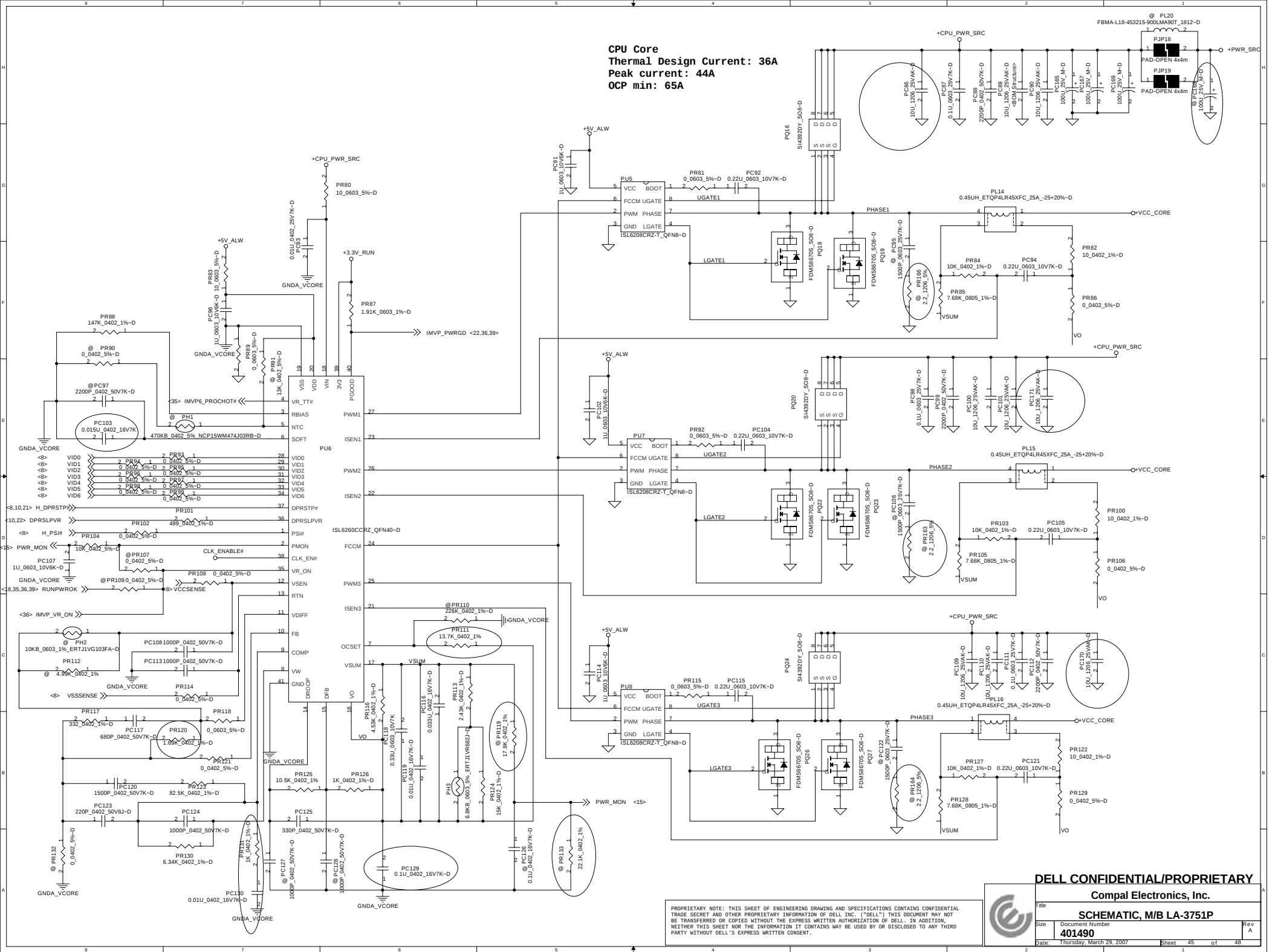
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CPU Core
Thermal Design Current: 36A
Peak current: 44A
OCP min: 65A



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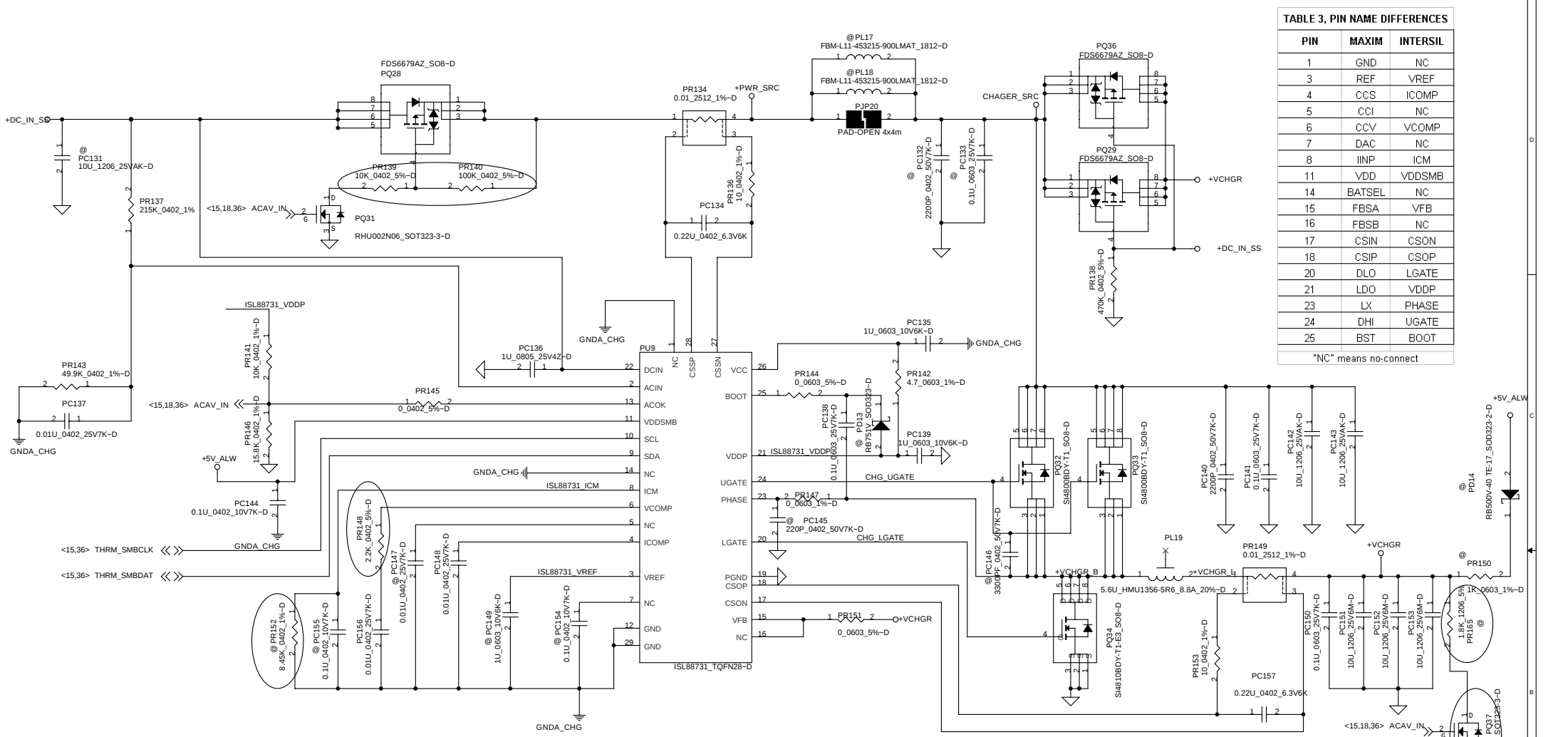
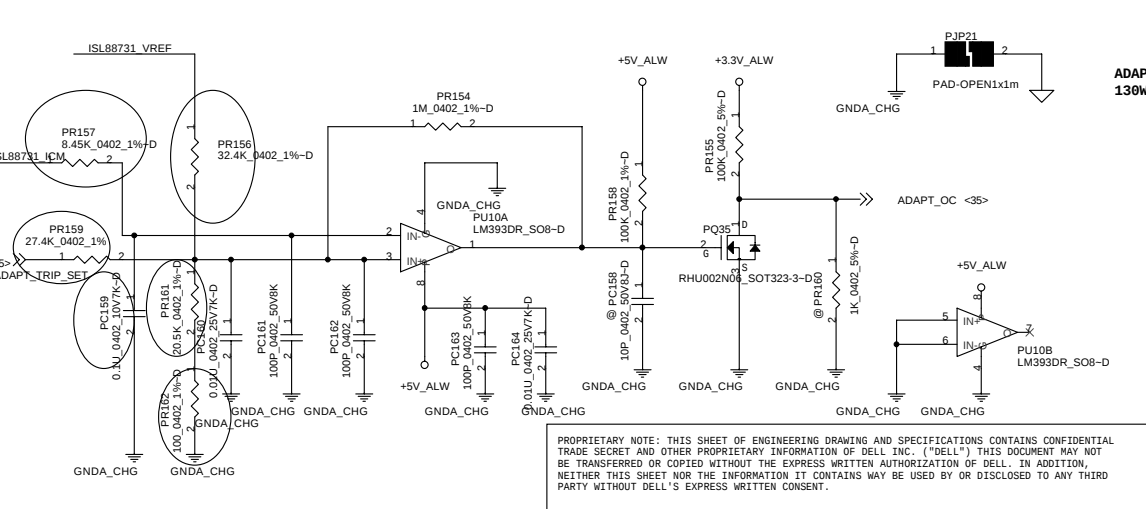


TABLE 3, PIN NAME DIFFERENCES			
PIN	MAXIM	INTERSIL	
1	GND	NC	
3	REF	VREF	
4	CCS	ICOMP	
5	CCI	NC	
6	CCV	VCOMP	
7	DAC	NC	
8	IINP	ICM	
11	VDD	VDDSMB	
14	BATSEL	NC	
15	FBSA	VFB	
16	FBSB	NC	
17	CSIN	CSON	
18	CSIP	CSOP	
20	DLO	LGATE	
21	LDO	VDDP	
23	LX	PHASE	
24	DHI	UGATE	
25	BST	BOOT	
"NC" means no-connect			

Ref DES	MAXIM
PR152	8.45K 0402 1%
PC159	0.01uF
PC155	0.1uF 0402 10V
PC149	1.0uF 0603 10V
PR137	365K 0402 1%
PR153	0 0402 5%
PR136	0 0402 5%
PC157	No STUFF
PC134	No STUFF
PC147	0.01uF
PC154	0.1uF 0402 10V
PC145	220pF 0402 50V
PD13	RB751V-40
PC146	3.3nF
PR147	1 0603 1%
PR151	100 0402 5%
PC156	0.01uF
PC148	0.01uF
PD14	1SS355
PR150	1K 0603 1%-D
PR157	0 0402 5%
PR148	10K 0402 5%
PR165	1.8K 1206 5%
PQ37	RHU002N06

INTERSIL
No STUFF
0.1uF
No STUFF
215K 0402 1%
10 0402 5%
10 0402 5%
0.22uF
0.22uF
No STUFF
No STUFF
No STUFF
0 0603 5%
0 0402 5%
0.01uF
0.01uF
No STUFF
No STUFF
8.45K 0402 5%
2.2K 0402 5%
No STUFF
No STUFF



Maximum charging current is 6.24A

ADAPTER (W)	TRIP current	PR156	PR161	PR162	PR159
130W	6.43A	32.4k	20.5k	100	27.4k

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