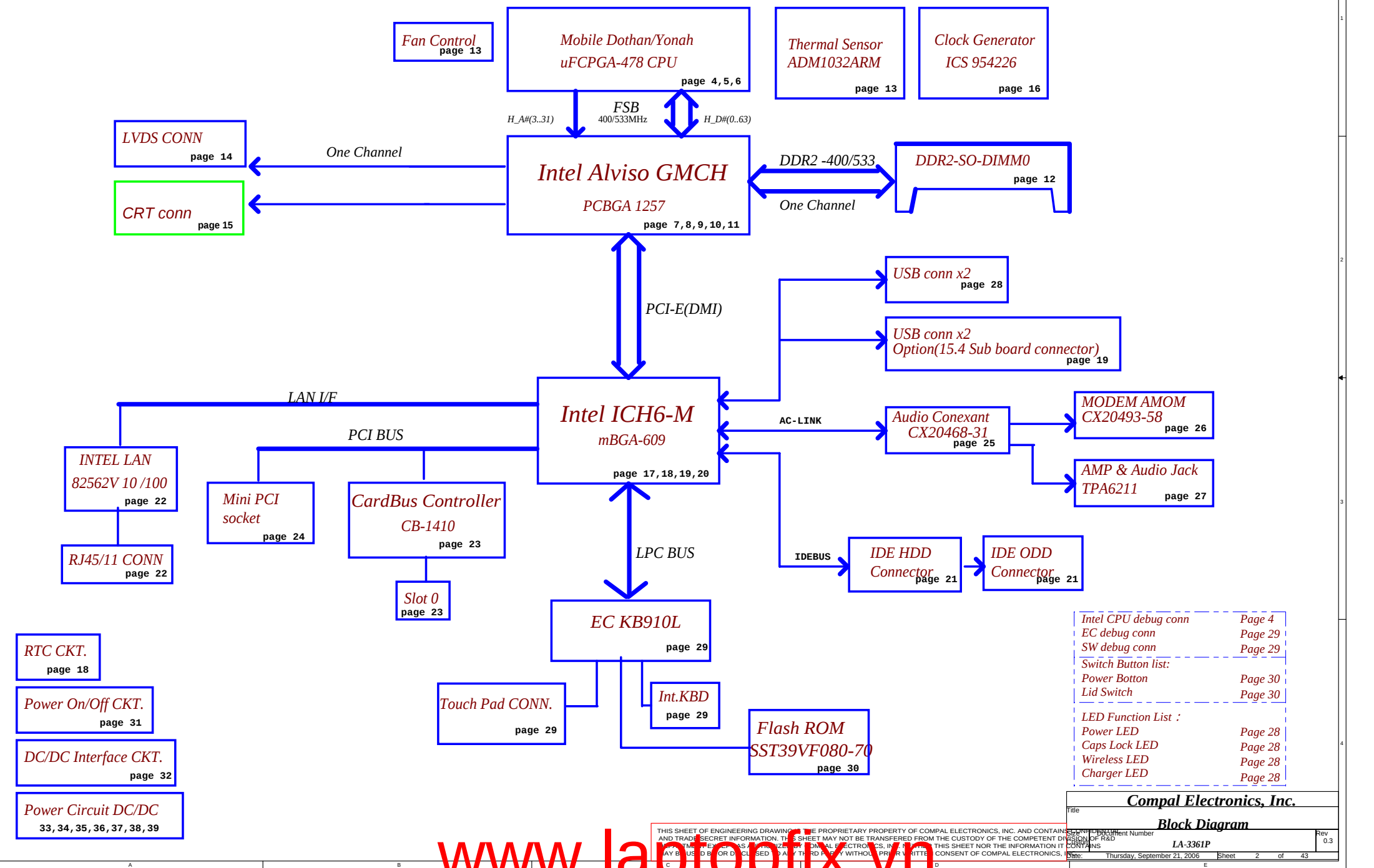


Compal confidential

Schematics Document Mobile Dothan uFCPGA with Intel Alviso_GM+ICH6-M core logic

2006-09-15

REV:1.0



I2C / SMBUS ADDRESSING

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	AD22	2	C
Wireless LAN(MINI PCI)	AD20	0	E, F

Power Managment table

Signal State	+3VALW +5VALW	+1.8V	+CPU CORE +VCCP(1.05V) +5VS +3VS +2.5VS +1.5VS +1.8VS +0.9VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADM1032	SODIMM	CLK CHIP	MINI PCI	LCD
SMB_EC_CK1 SMB_EC_DA1	KB910L	×	✓	×	×	×	×	×	×
SMB_EC_CK2 SMB_EC_DA2	KB910L	×	×	×	✓	×	×	×	×
ICH_SMBCLK ICH_SMBDATA	ICH6-M	×	×	×	×	✓	✓	×	×
LCD_DDCCLK LCD_DDCDATA	Alviso GM-GP	×	×	×	×	×	×	×	✓
I2CC_SCL I2CC_SDA	NV44M	×	×	×	×	×	×	×	✓

Alviso 915GM SA00000K040

Alviso 910GML SA00000K100

BOM

@ : not install

45@ : 45 level

14@ : 14"(IAT00) install

WLAN@ : with WLAN (mini PCI) install

AMOM@ : with AMOM install

BATT@ : 45 level

SPI@ : SPI ROM install

conn@ : ME part

IAT00 14"

46144232L01 915GM

46144232L02 910GML W/O WLAN

46144232L03 910GML

IAT10 15.4"

46144232L11 910GML

46144232L12 915GM

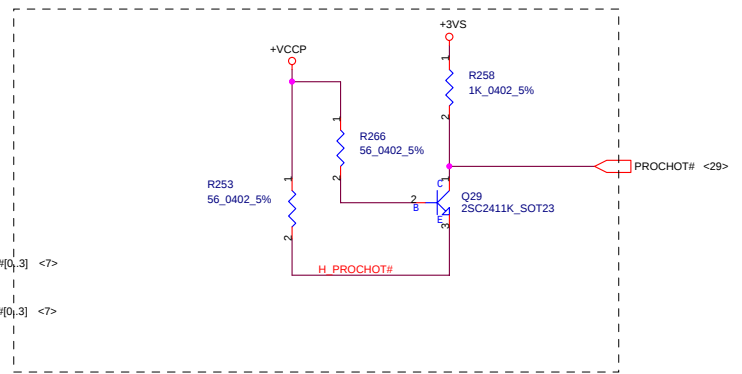
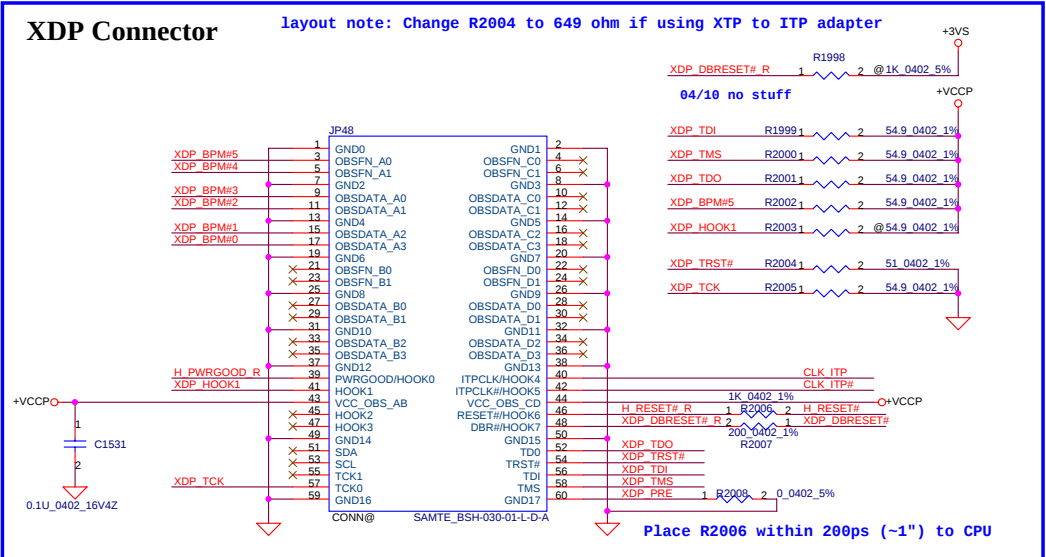
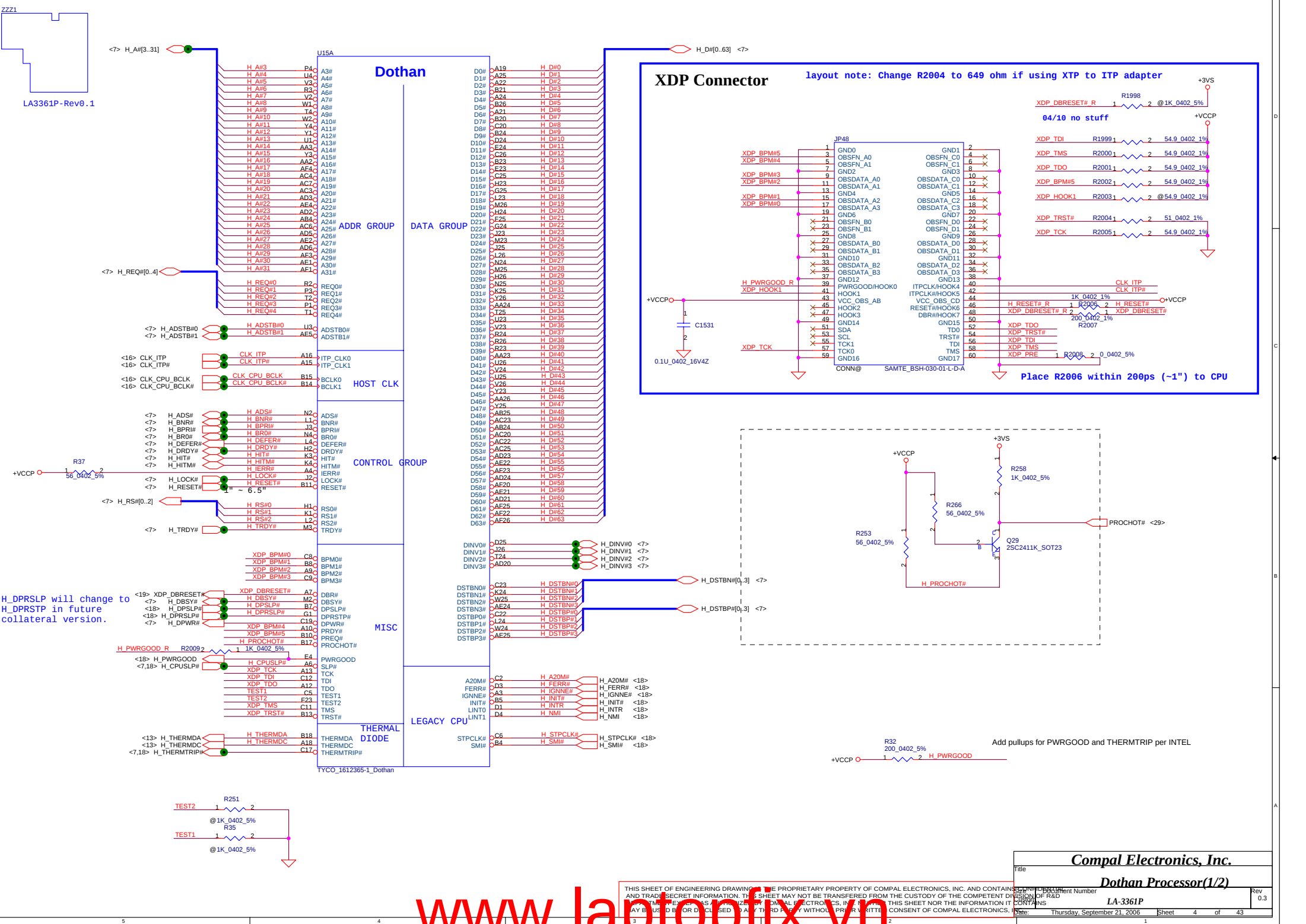
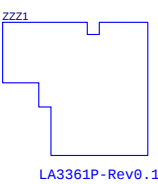
46144232L13 910GML W/O WLAN

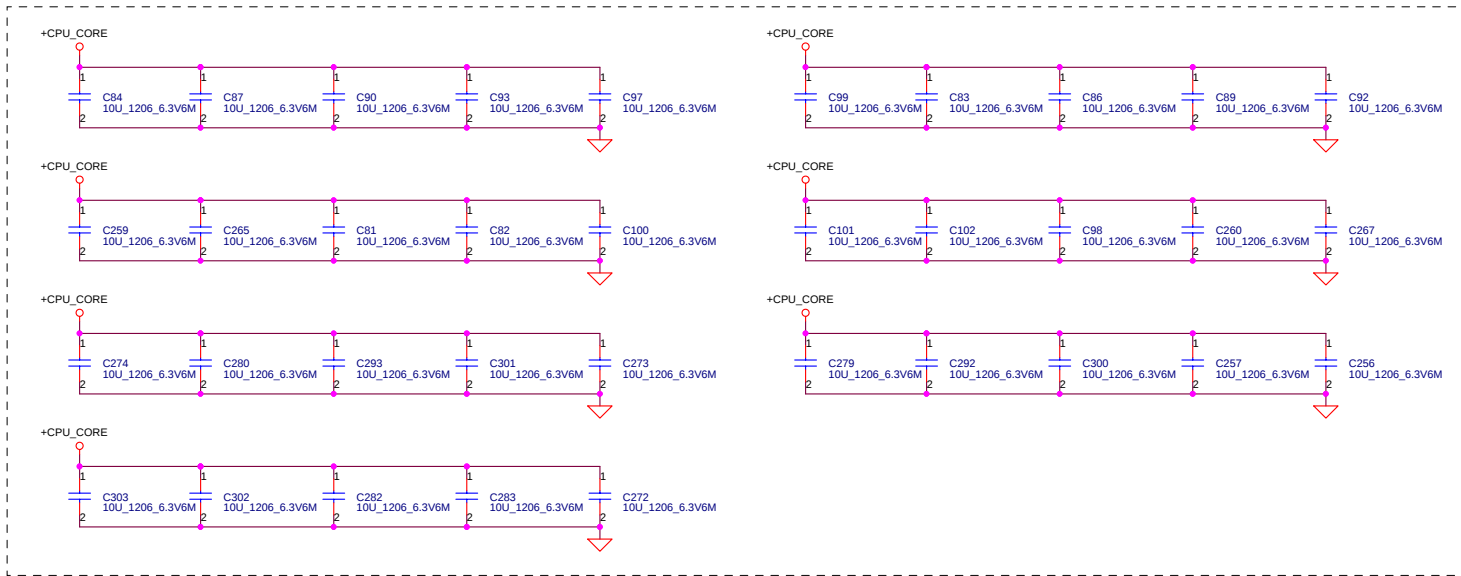
Compal Electronics, Inc.

Design Note

LA-3361P

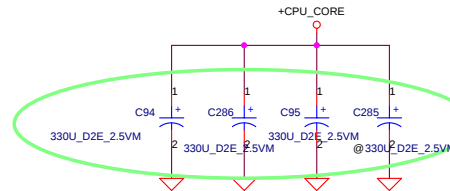
Thursday, September 21, 2006 Sheet 3 of 43





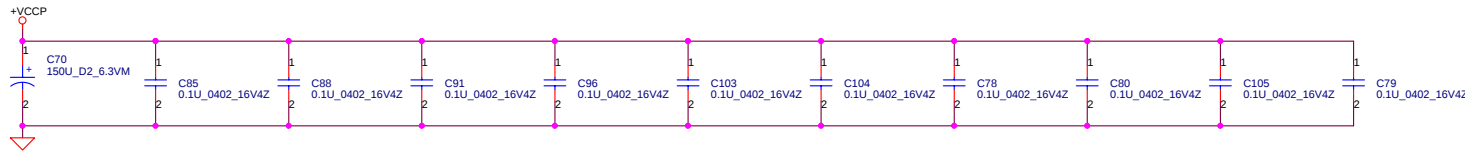
Near VCORE regulator.

6/21



ESR <= 3m ohm

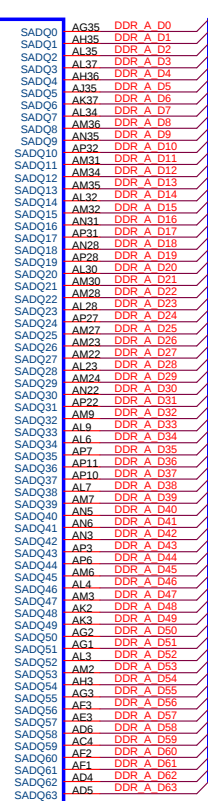
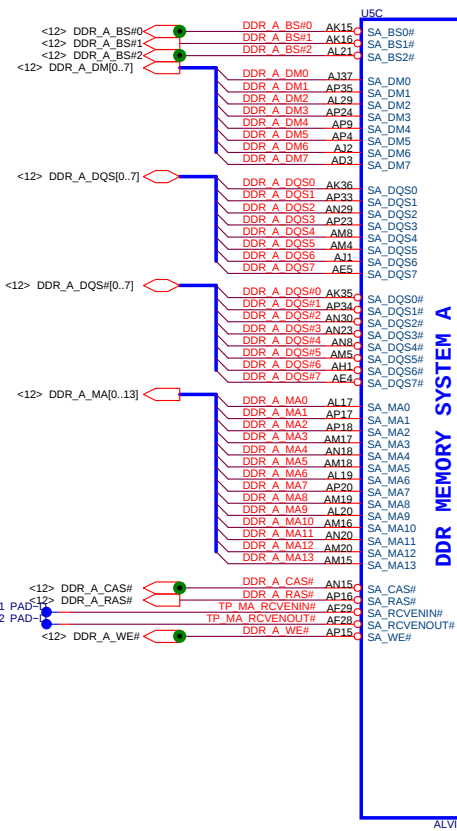
Capacitor > 880 uF



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Compal Electronics, Inc.			
Title	Dothan Bypass	Rev	0.3
Document Number	LA-3361P	Date	Thursday, September 21, 2006
Sheet	6	of	43

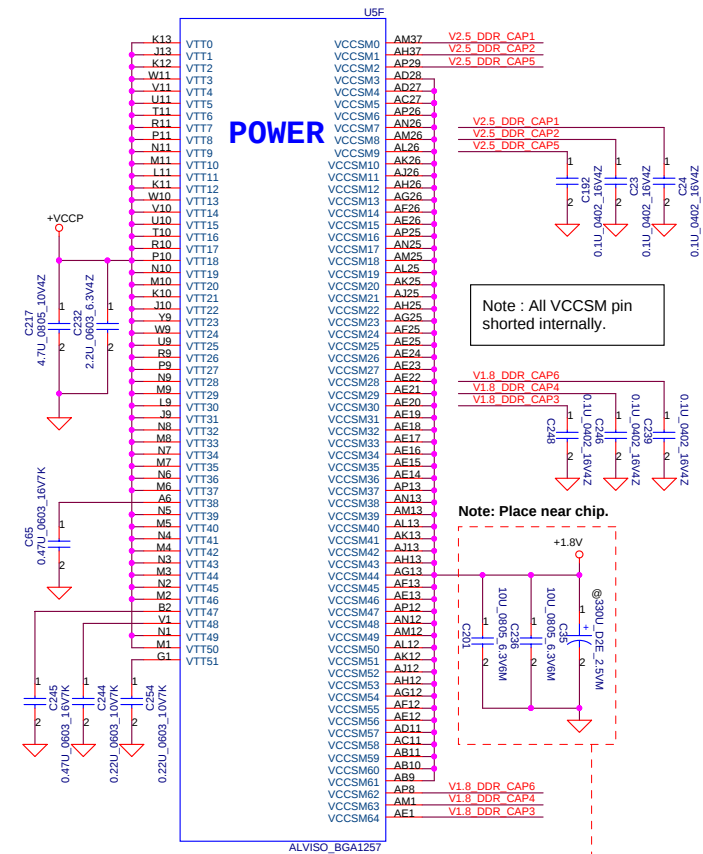
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This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.



POWER

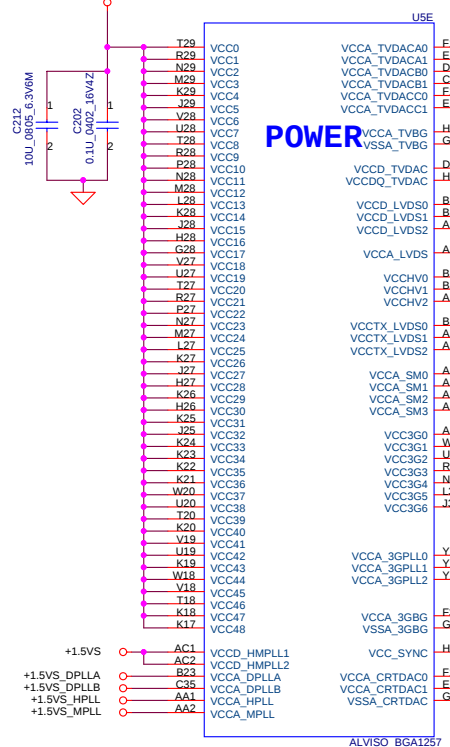


Note: All VCCSM pin shorted internally.

Note: Place near chip.

W=20 mils

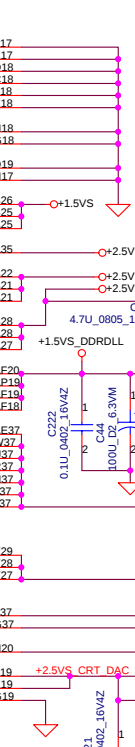
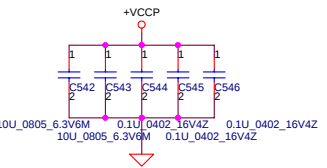
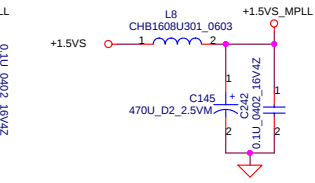
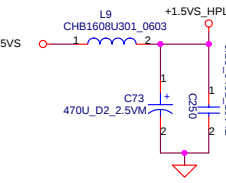
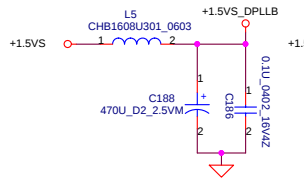
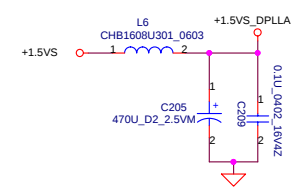
POWER

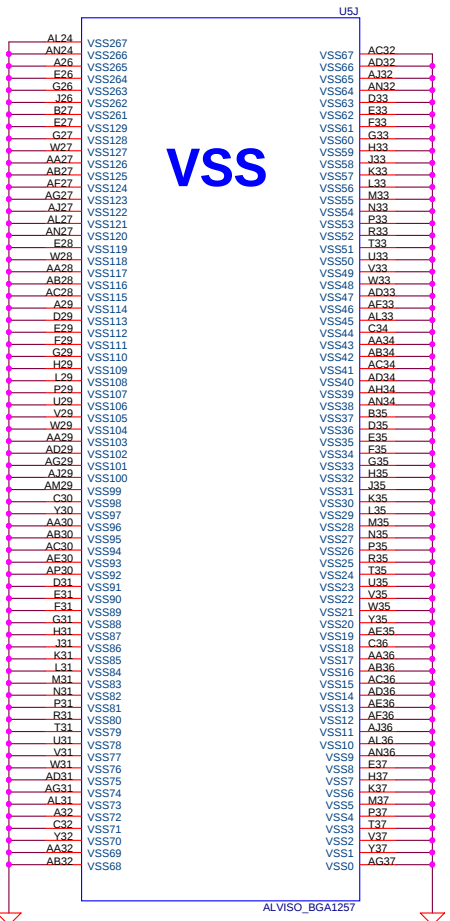
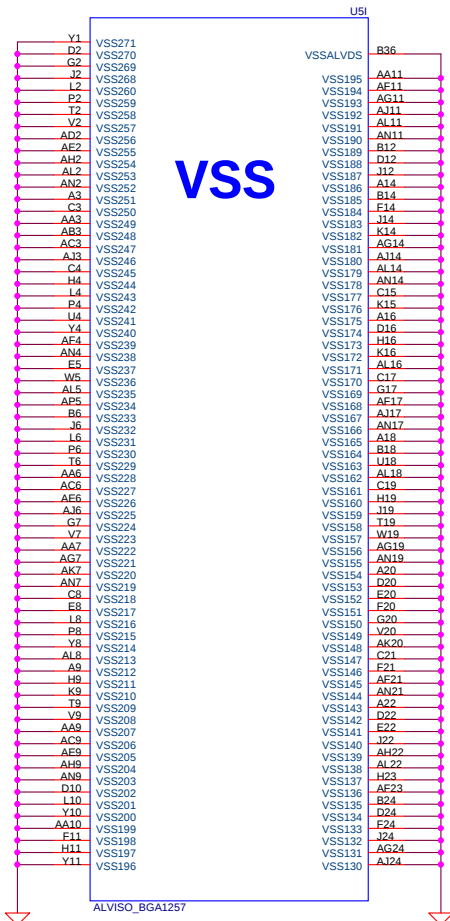
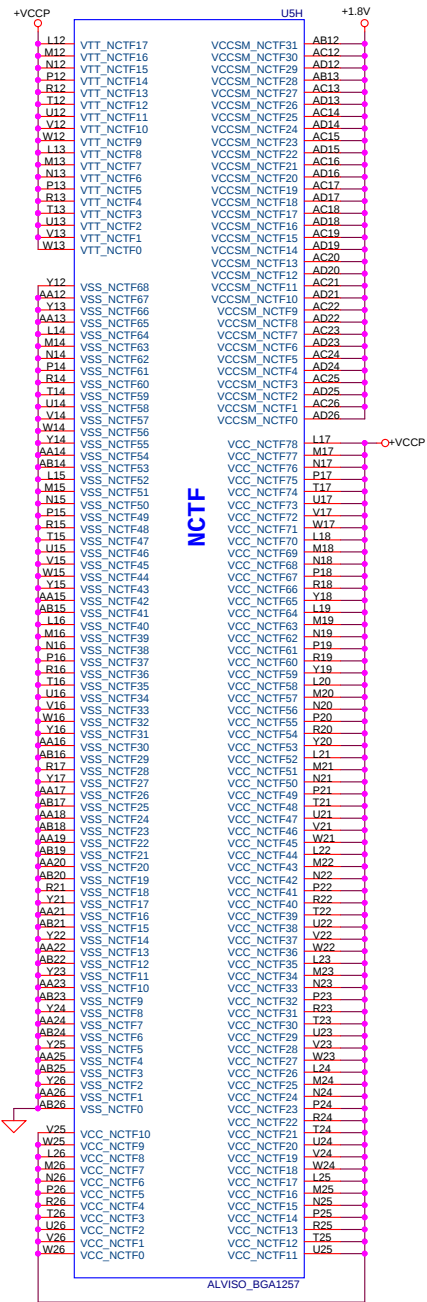


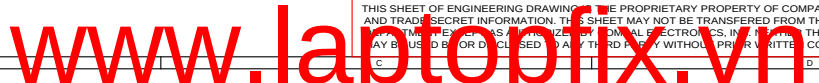
Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

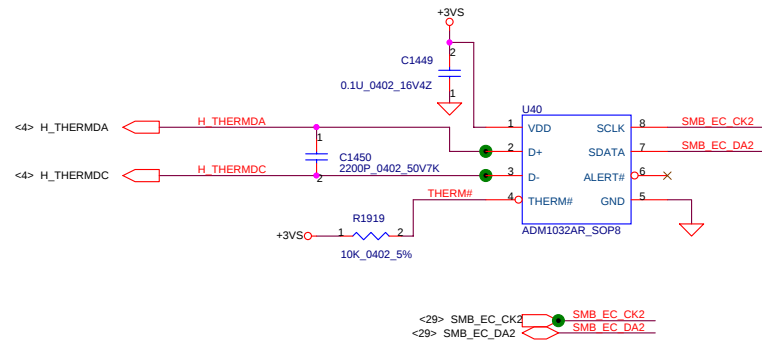
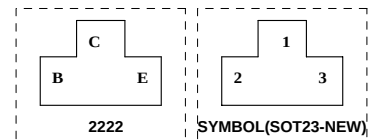
CRTDAC: Route caps within 250mil of Alvisto. Route FB within 3" of Alvisto.

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

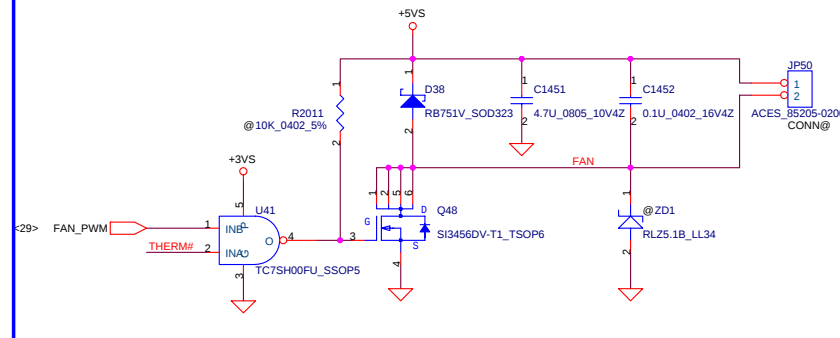




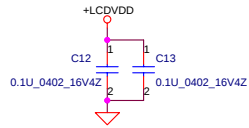




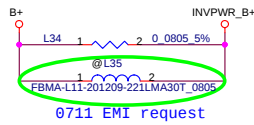
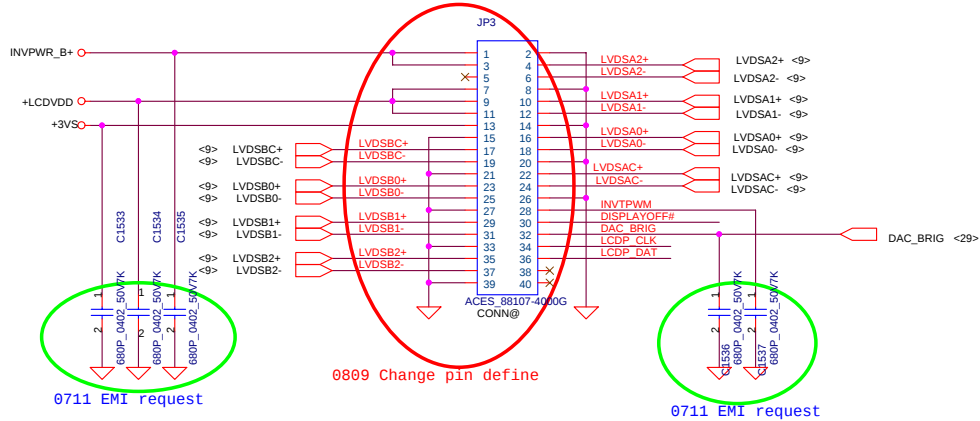
PWM Fan Control circuit



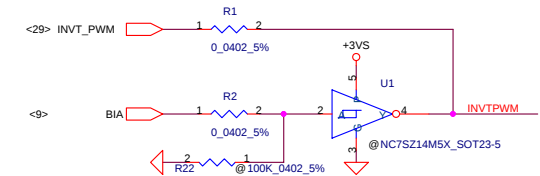
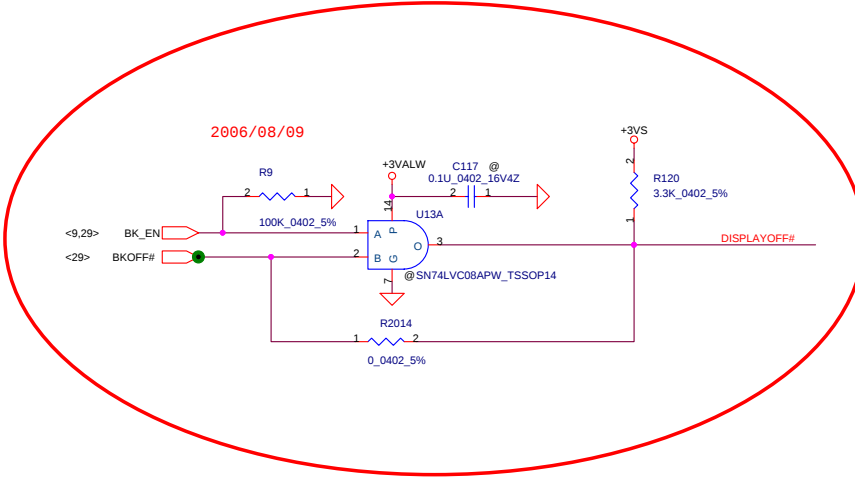
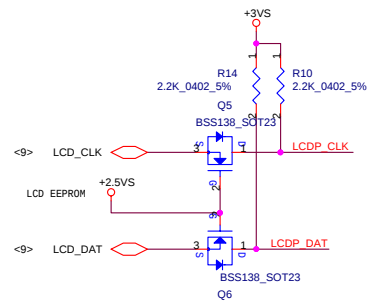
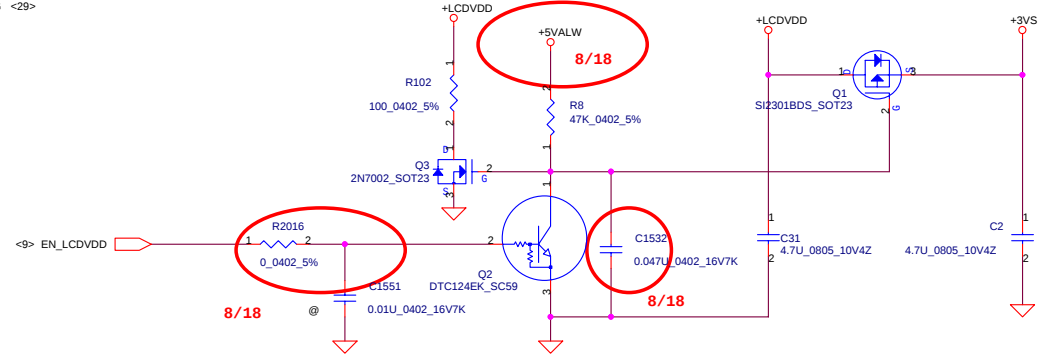
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Title	Thermal sensor and Fan
Document Number	LA-3361P
Date	Thursday, September 21, 2006
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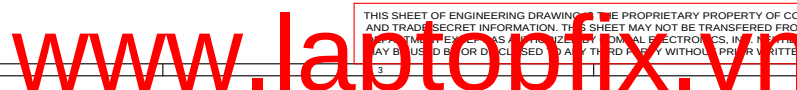
LVDS connector

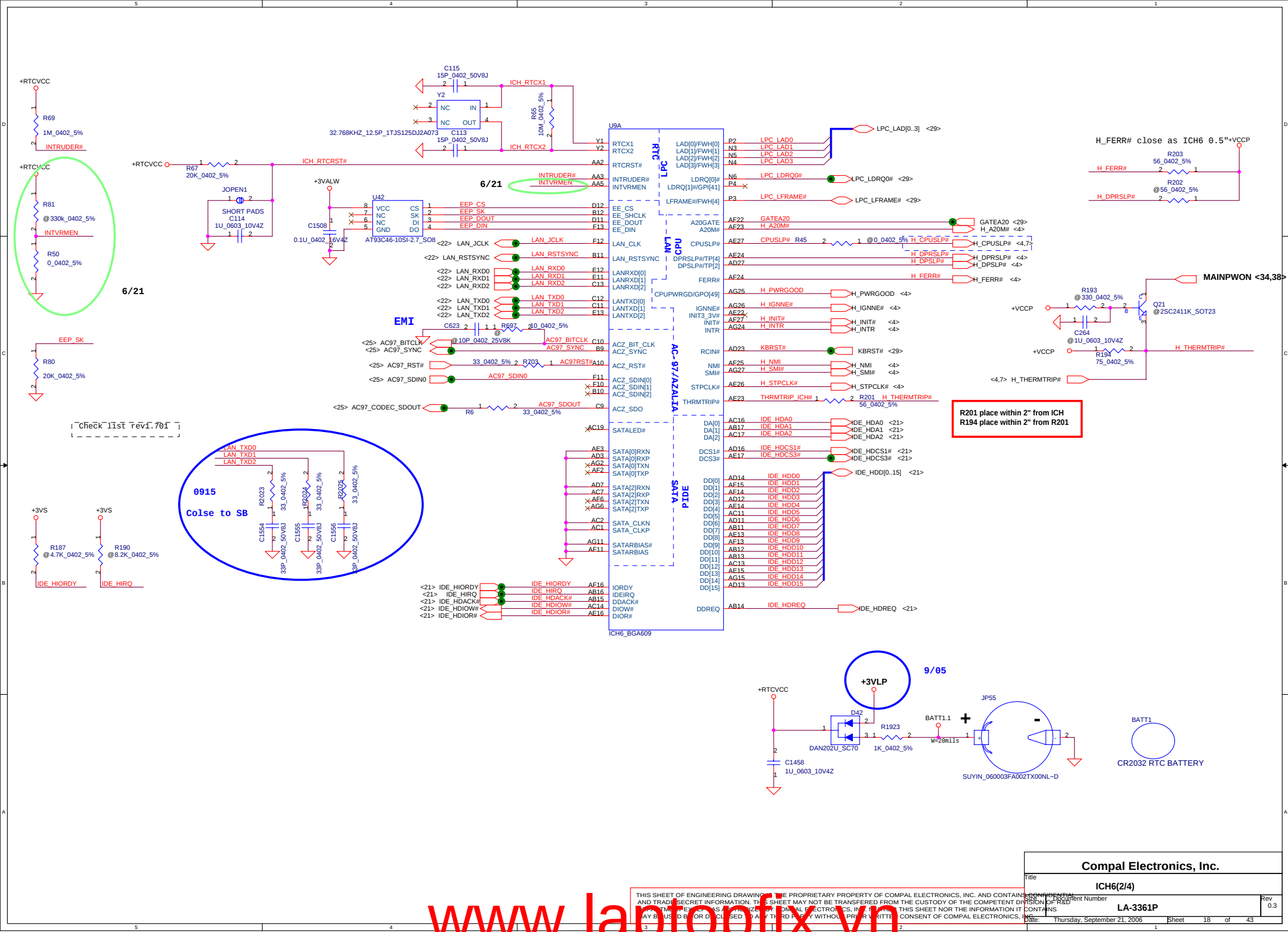


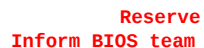
Aviso LCD/PANEL BD. CONN.



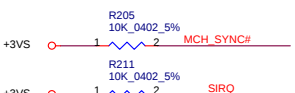
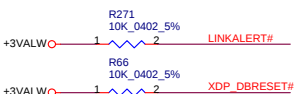
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LVDS connector	
LA-3361P	Rev 0.3
Thursday, September 21, 2006	Sheet 14 of 43



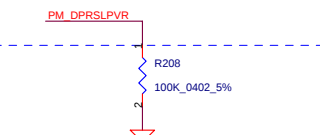




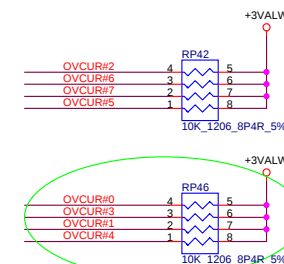
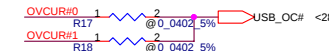
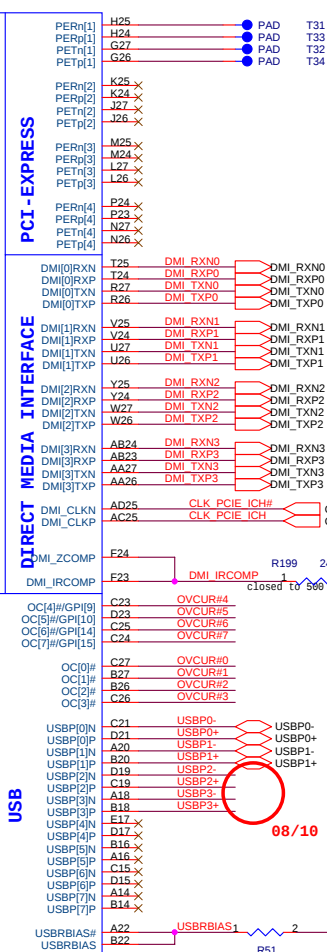
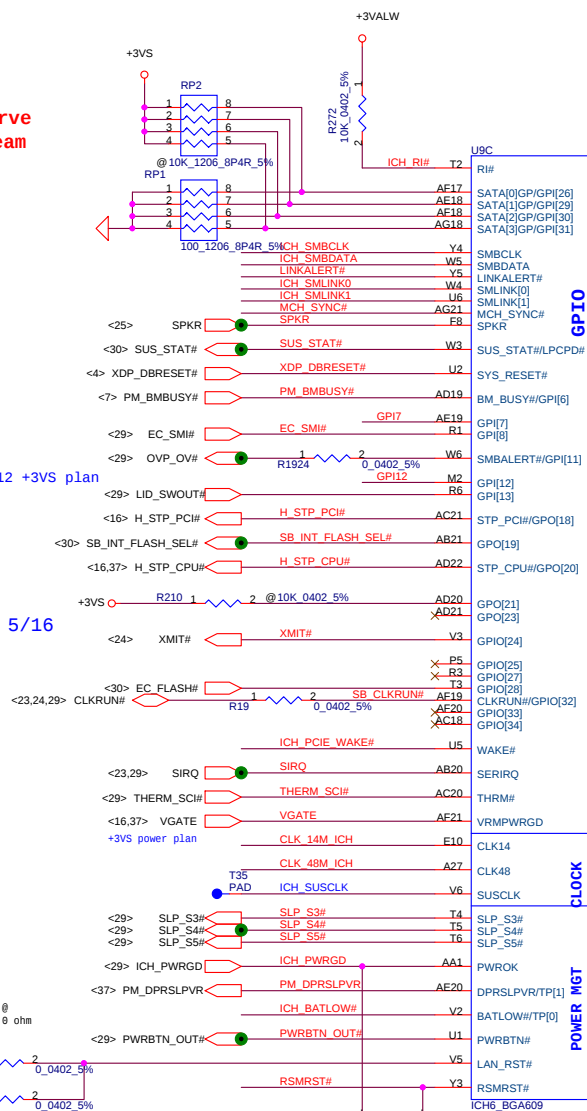
ICH6 VER1.5 GPI12 +3VS plan



8.2 k pull-up to Vcc3_3(CRB uses 10 k)

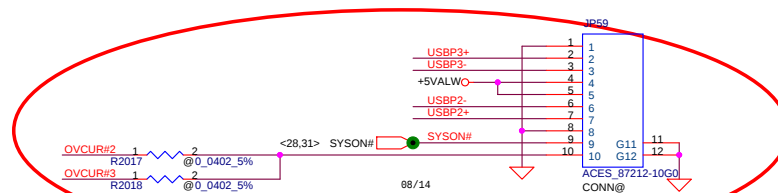


Signal has integrated pull-down in ICH
May need pulldown for DPRSLPVR in case
the ICH6m does not set this value in time
for boot.

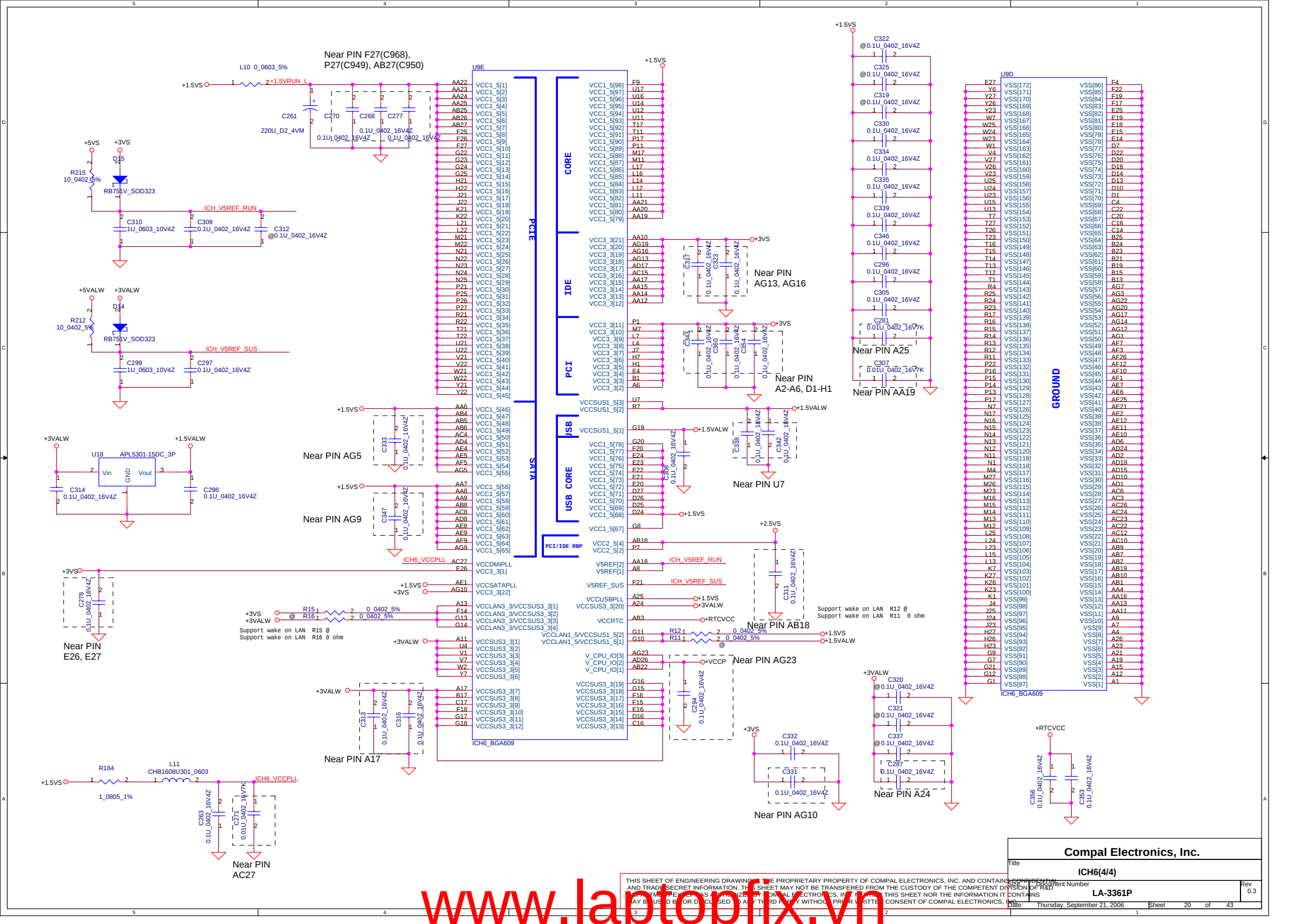


06/23 change R to RP

USBPN/USBPP impedance 45 Ohm

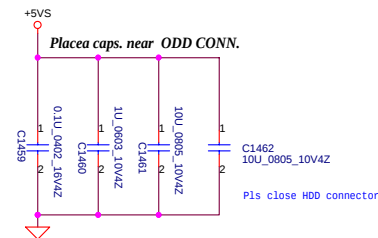
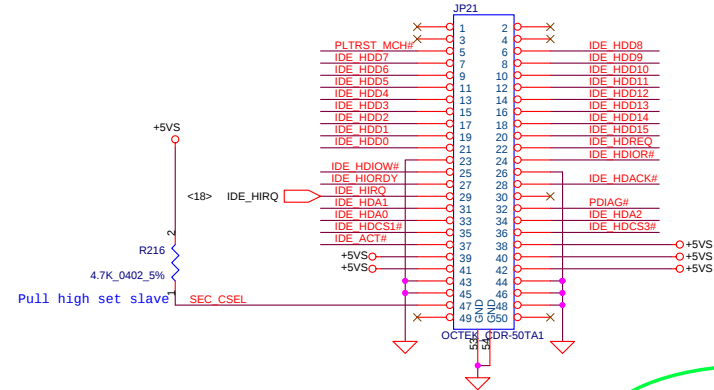
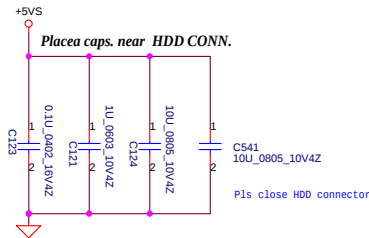
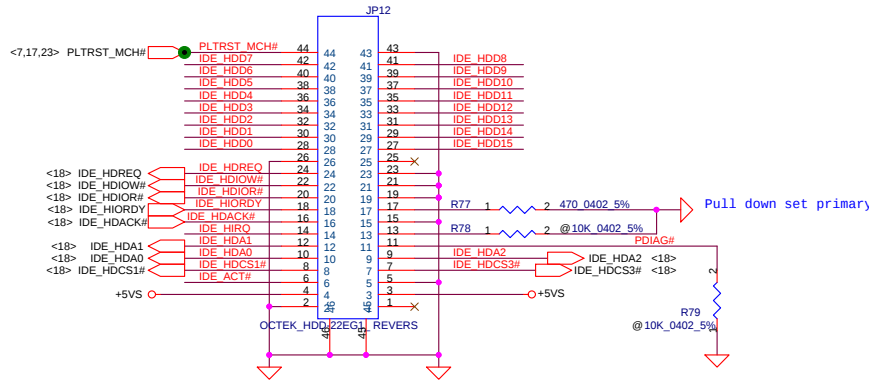


08/10 Add two USB port to subboard

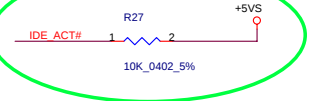


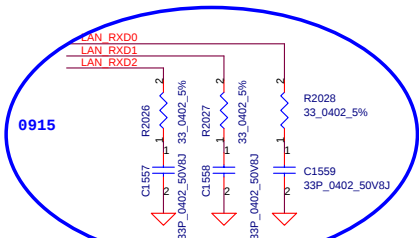
HDD Connector

CD-ROM Connector



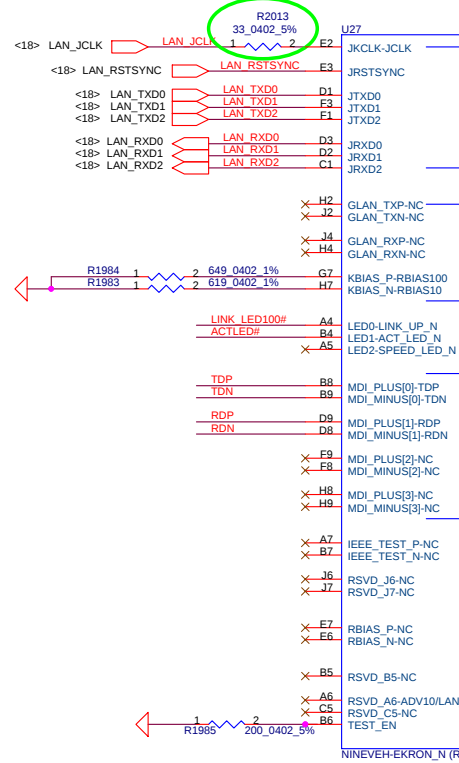
06/23



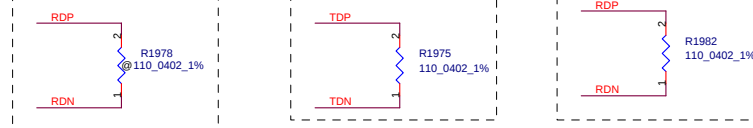


close to LAN chipset

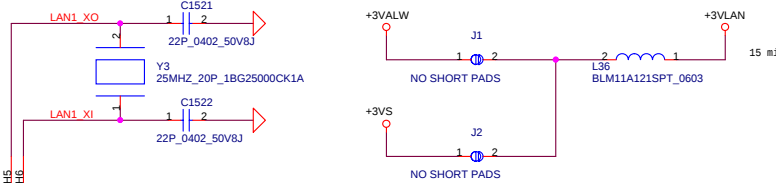
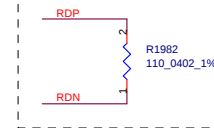
0718 Intel checklist recommend



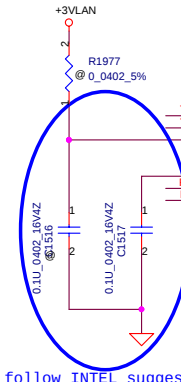
close to U25chip(Intel rule) close to U25chip(Intel rule)



close to U21

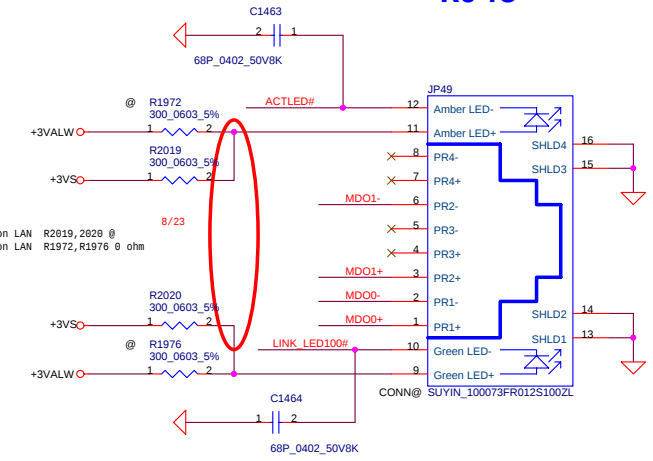


Support wake on LAN R2019, 2020 @
Support wake on LAN R1972, R1976 0 ohm

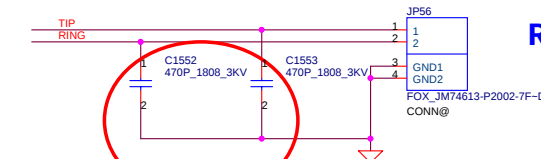


09/15 follow INTEL suggest

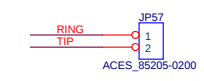
RJ45



RJ11

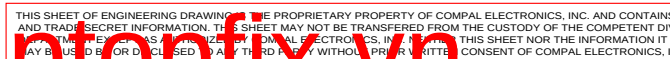
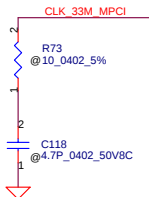


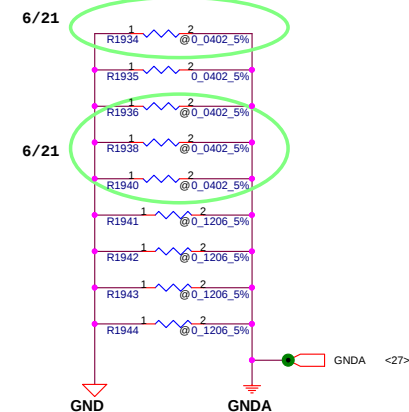
8/18 for EMI



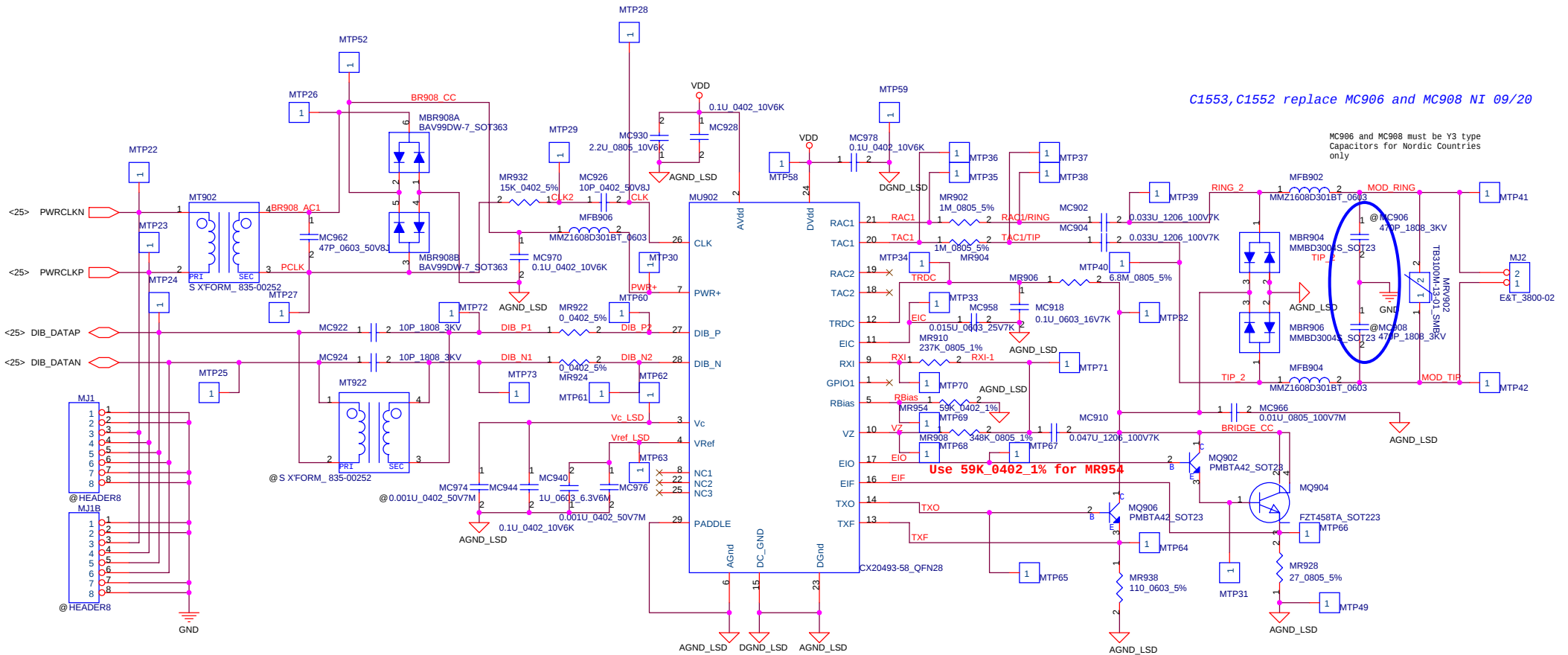
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Date: Thursday, September 21, 2006				Sheet 22 of 43	

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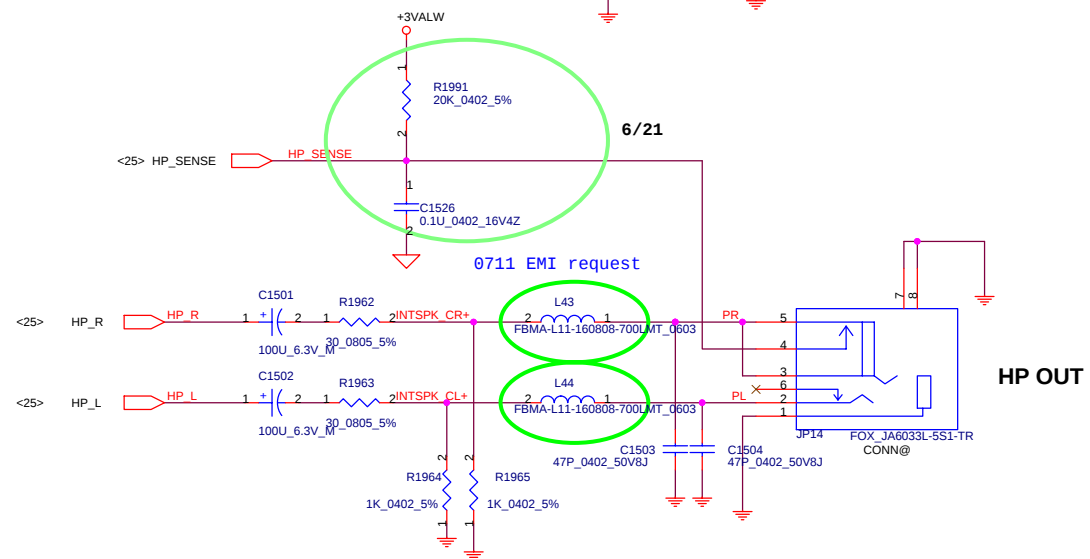
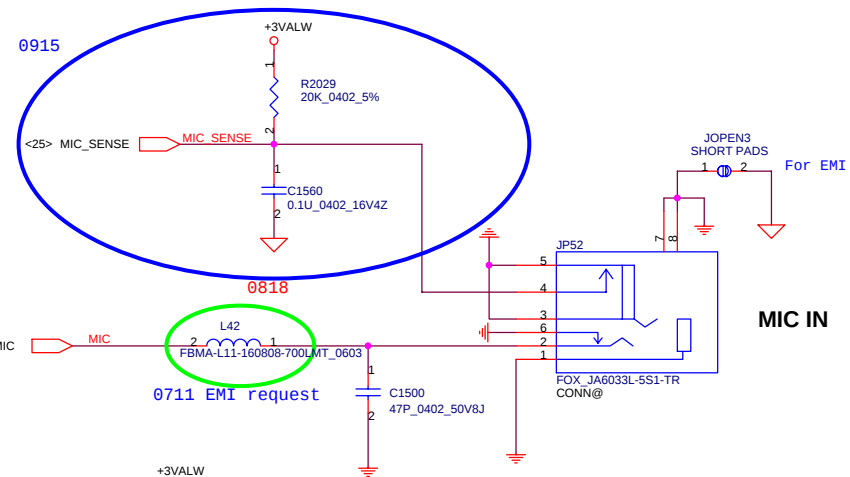
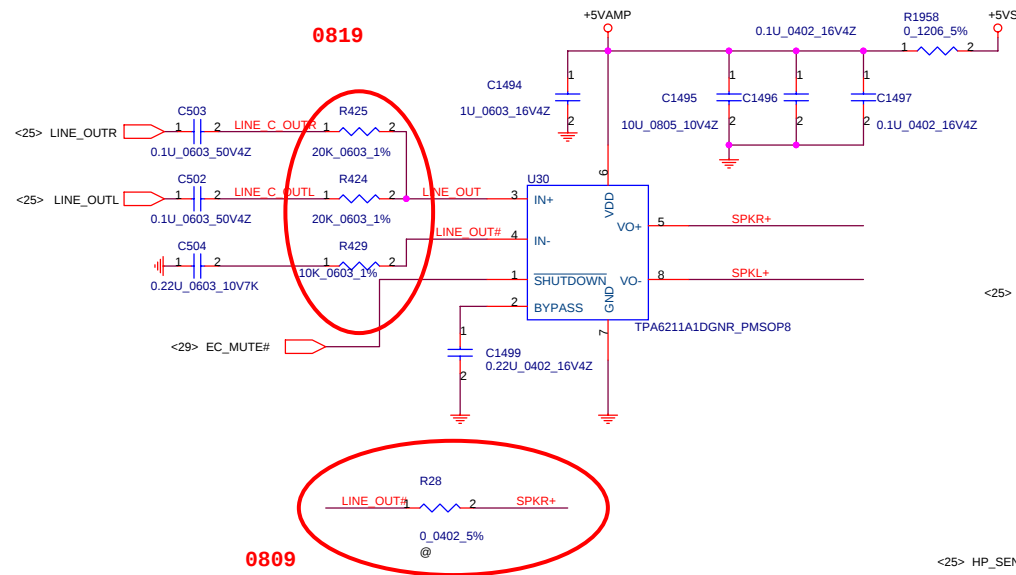




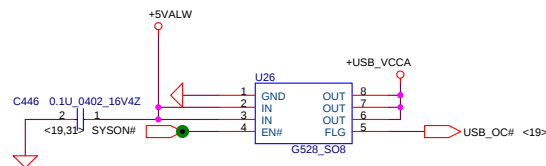
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				Date:	Thursday, September 21, 2006	Sheet 25 of 43



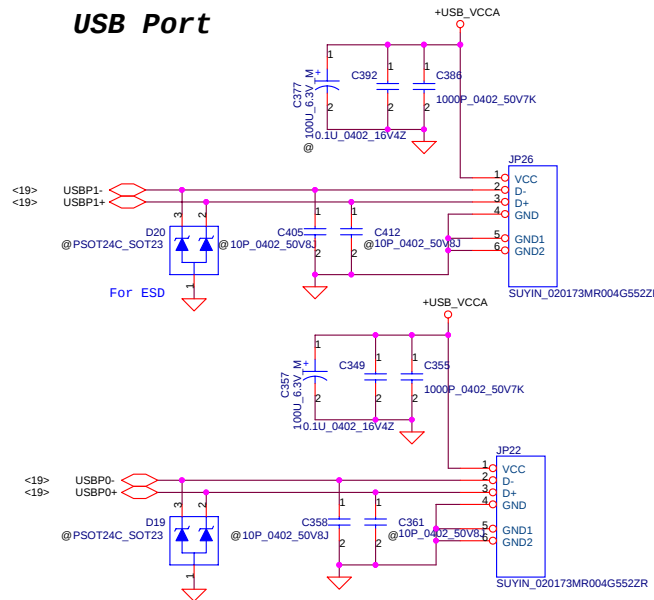
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Size Custom	Document Number	LA-3361P		
Date:	Thursday, September 21, 2006	Sheet	26	of 43



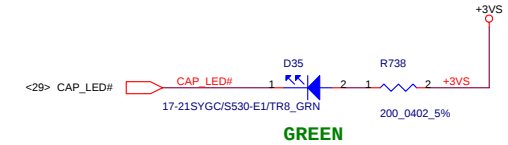
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				Document Number	LA-3361P
				Date	Thursday, September 21, 2006
				Sheet	27 of 43



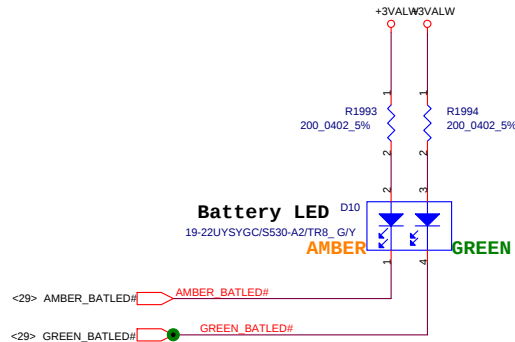
USB Port



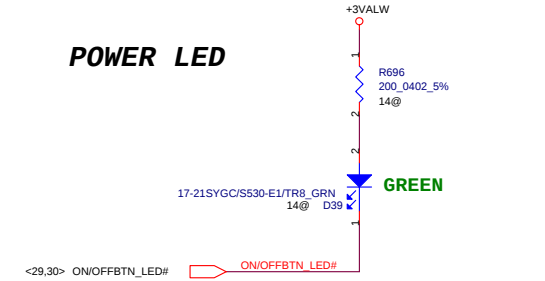
CAP LED



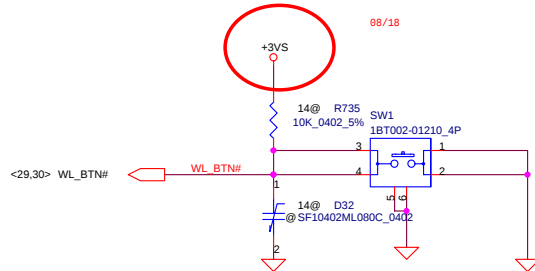
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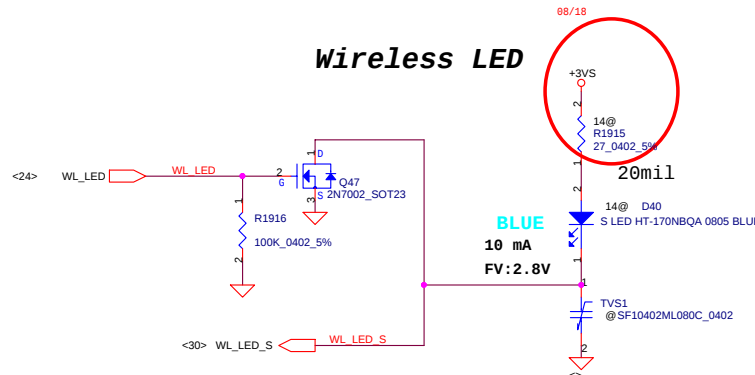
POWER LED



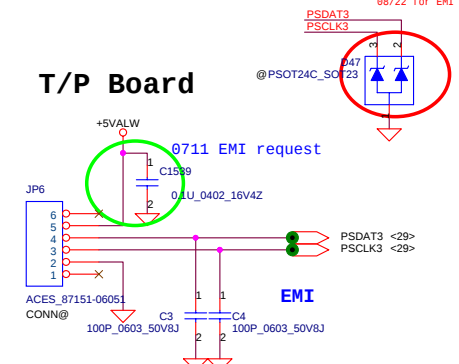
WL ON/OFF



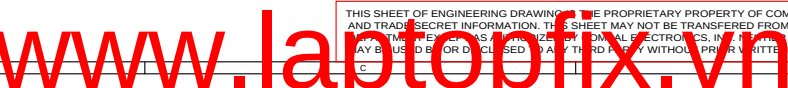
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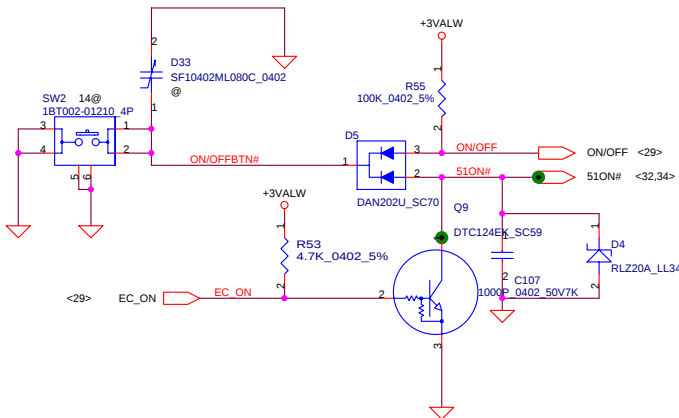
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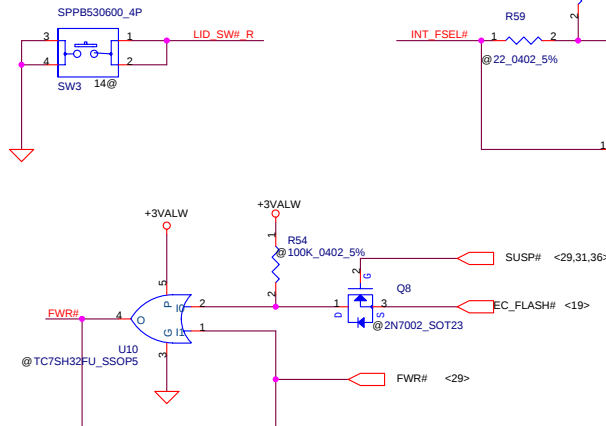
Compal Electronics, Inc.			
Title		Document Number	
USB Port		LA-3361P	
Date		Sheet	
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Power BTN ON/OFF Button



LID_SW

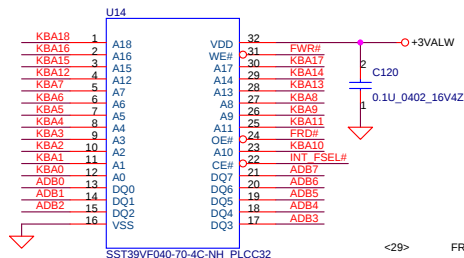


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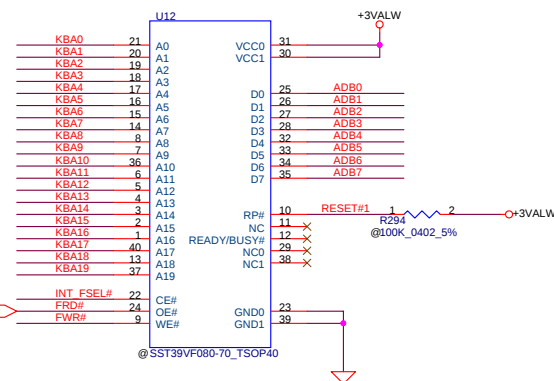
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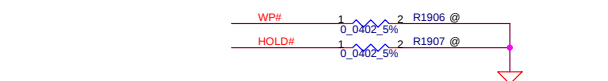
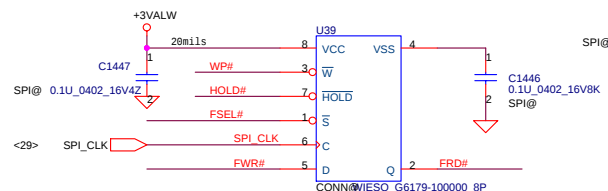
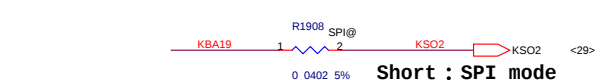
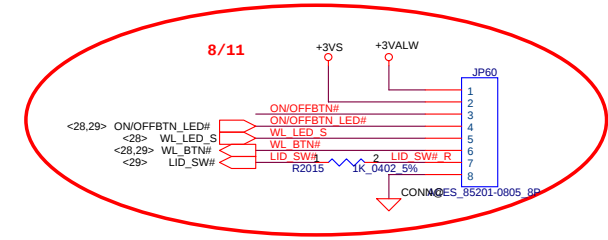
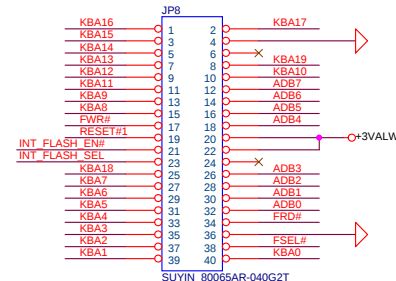
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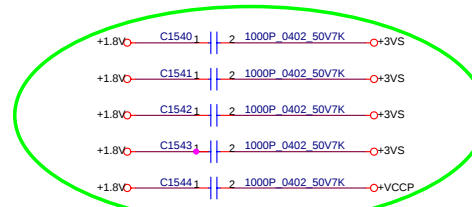
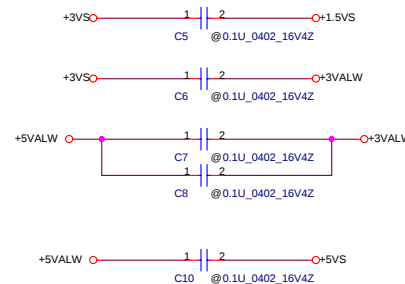
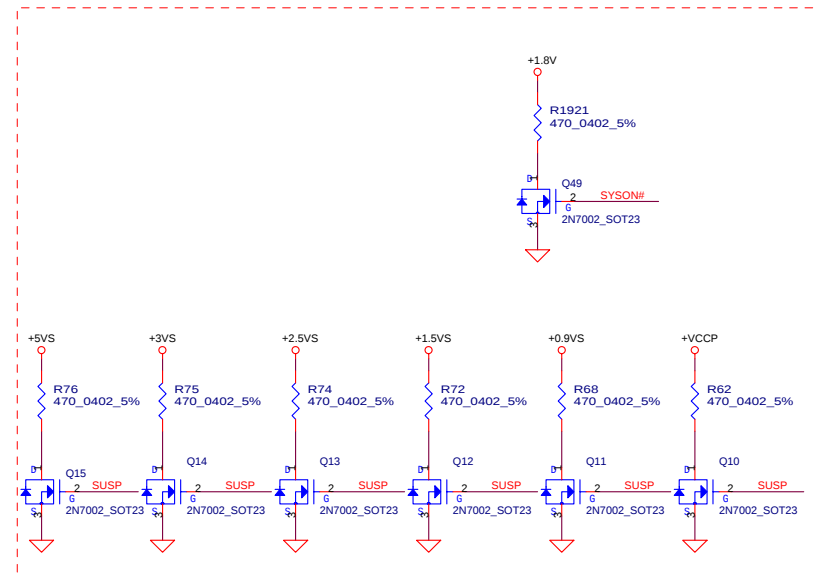
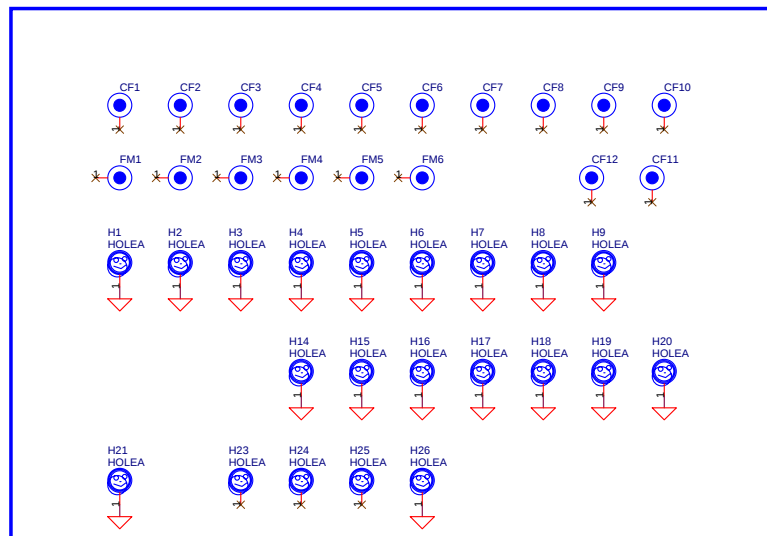
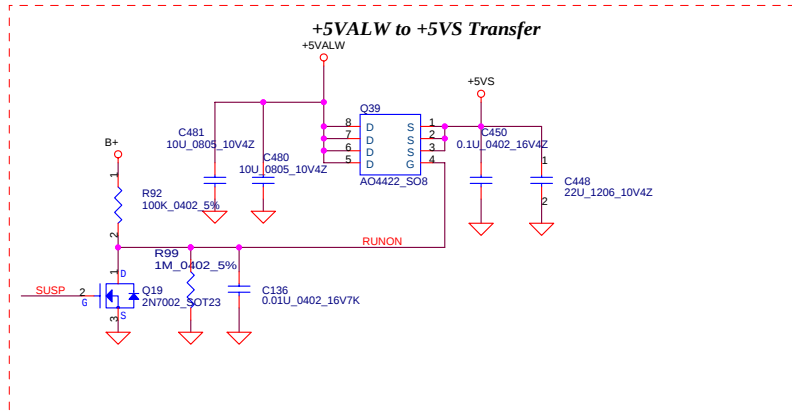
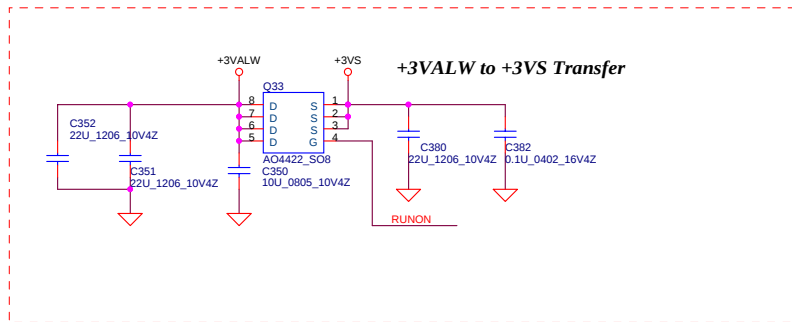


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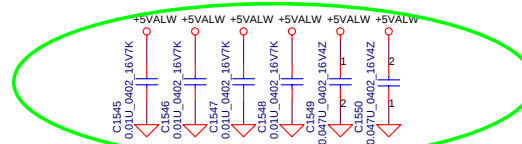


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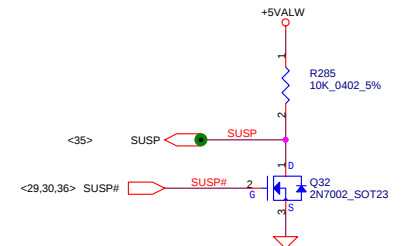
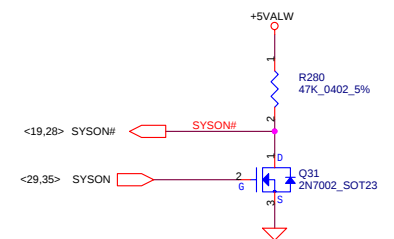
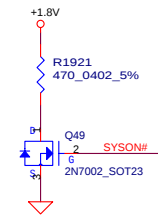




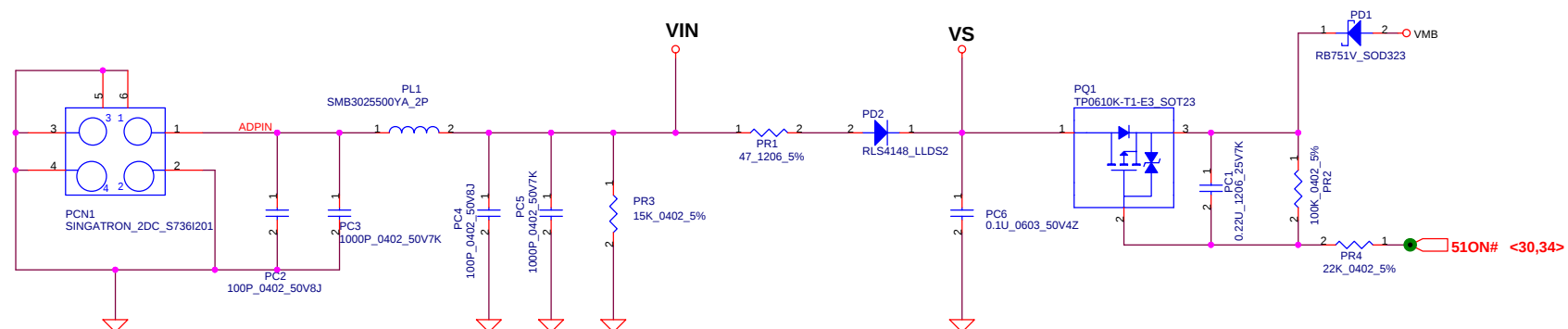
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7/11 EMI request

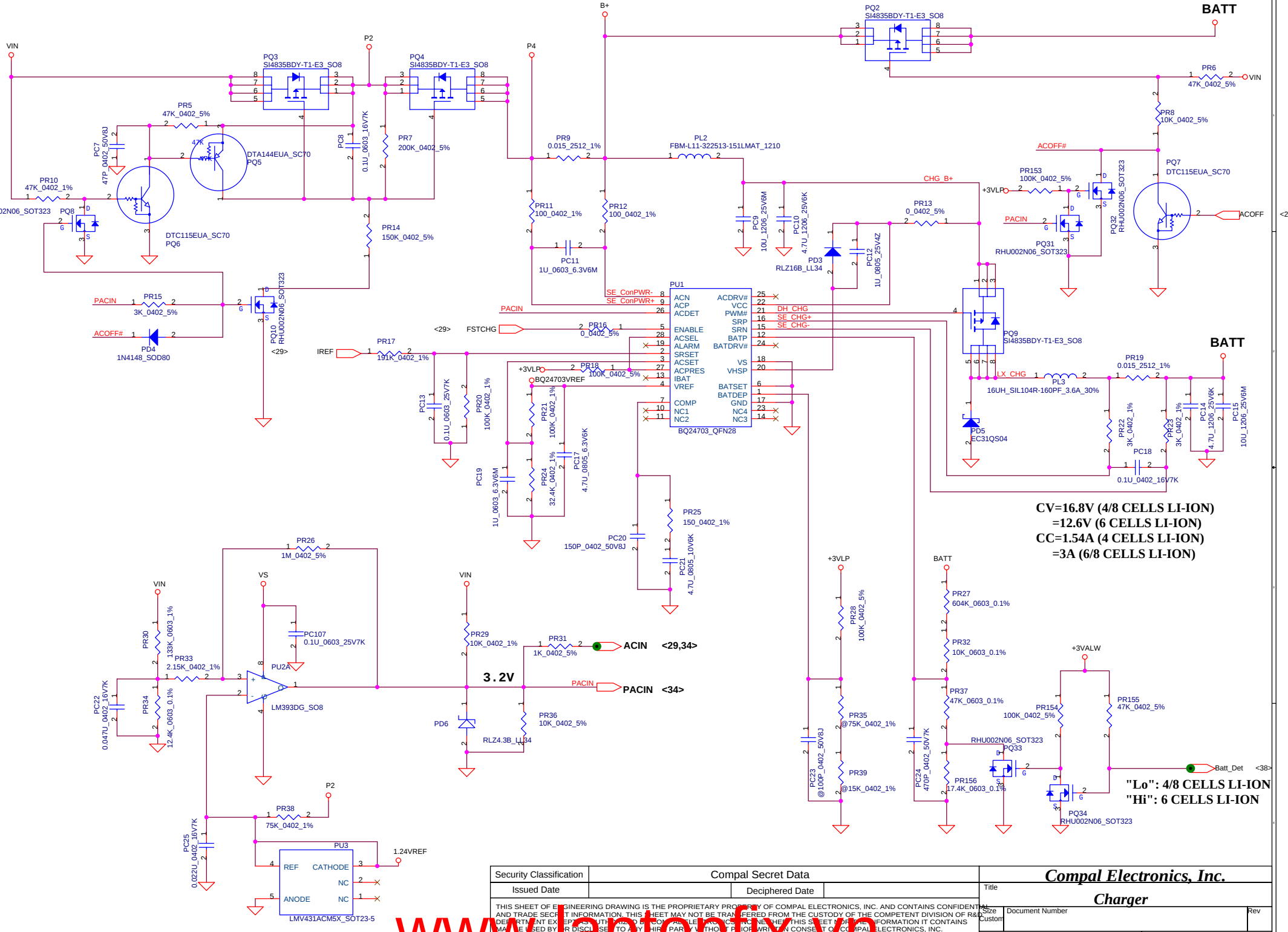


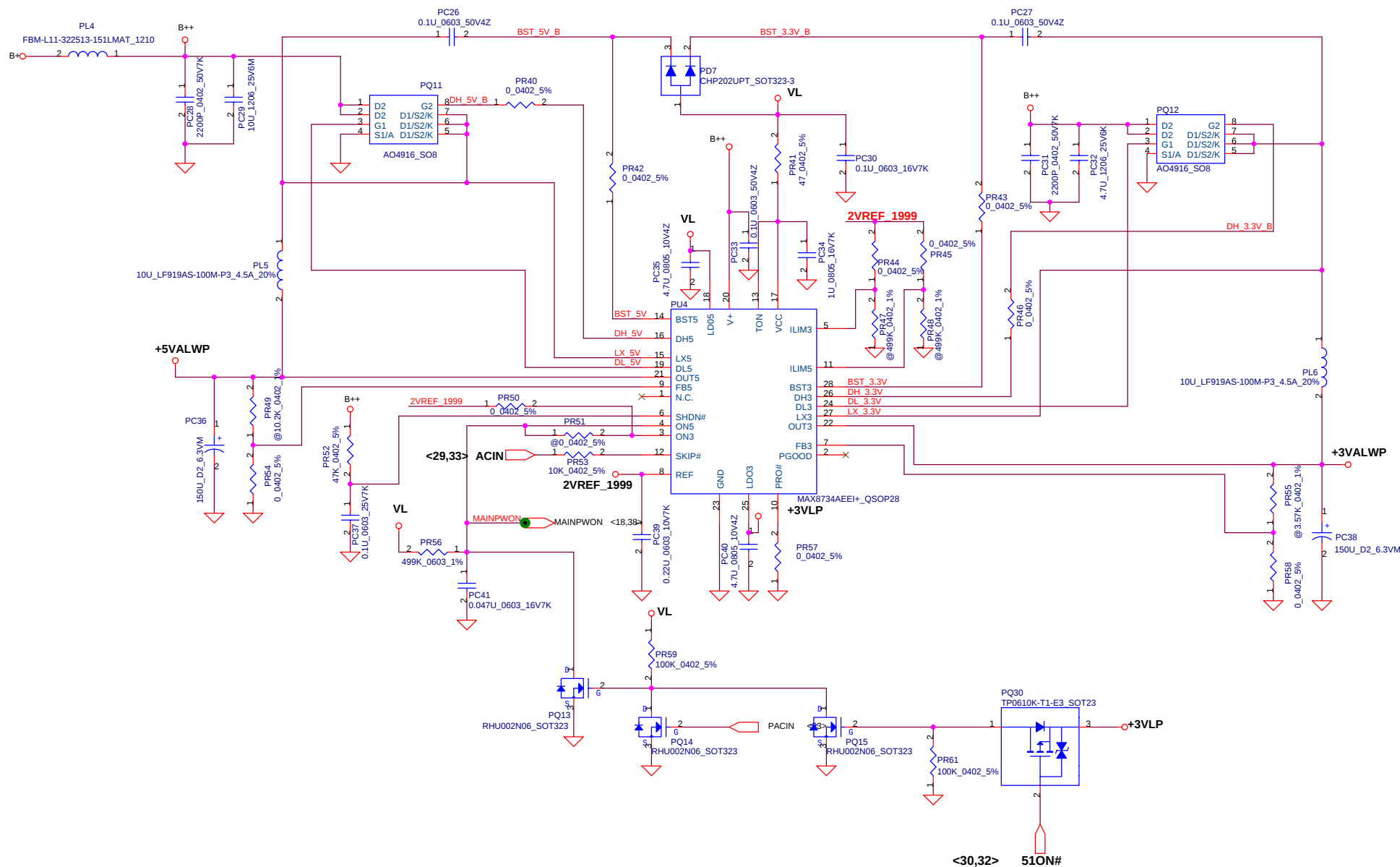
Compal Electronics, Inc.			
Title	POWER CONTROL		
Document Number	LA-3361P		
Rev	0.3		
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Security Classification		Compal Secret Data			
Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title	
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				<Doc>	
Date: Thursday, September 21, 2006				Sheet 32	of 43

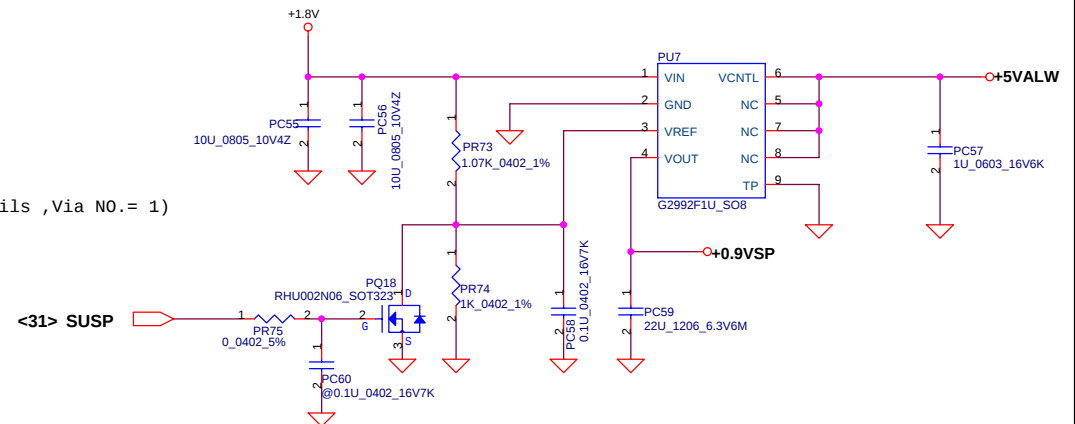
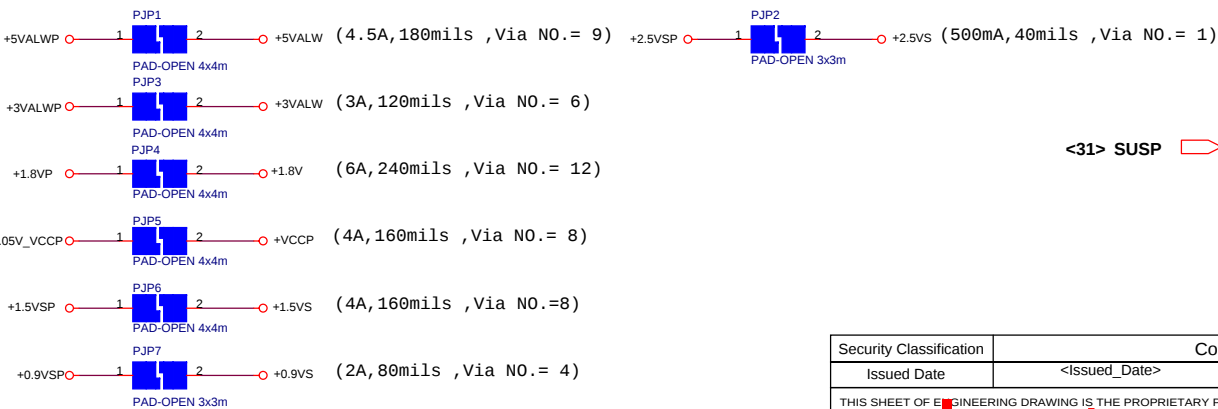
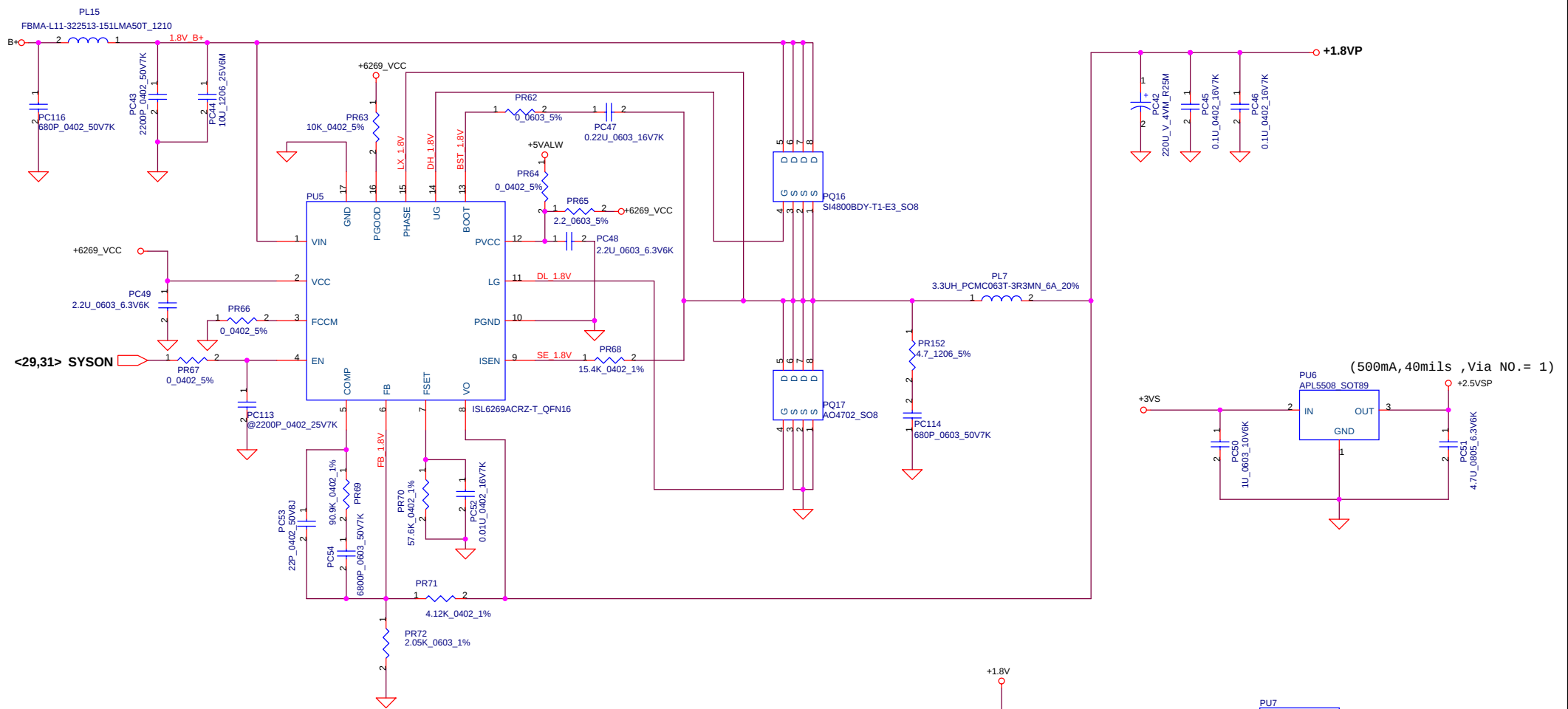
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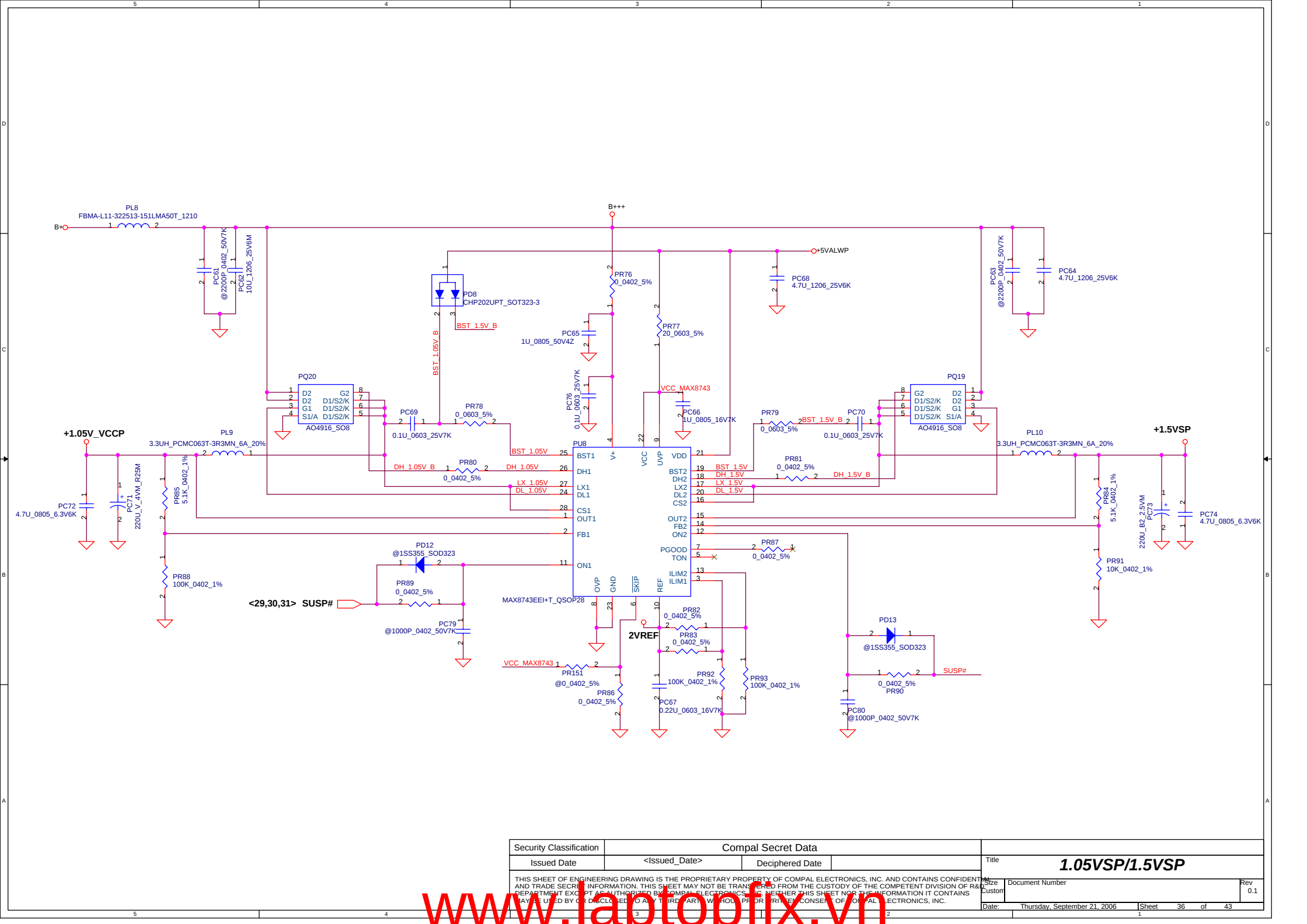


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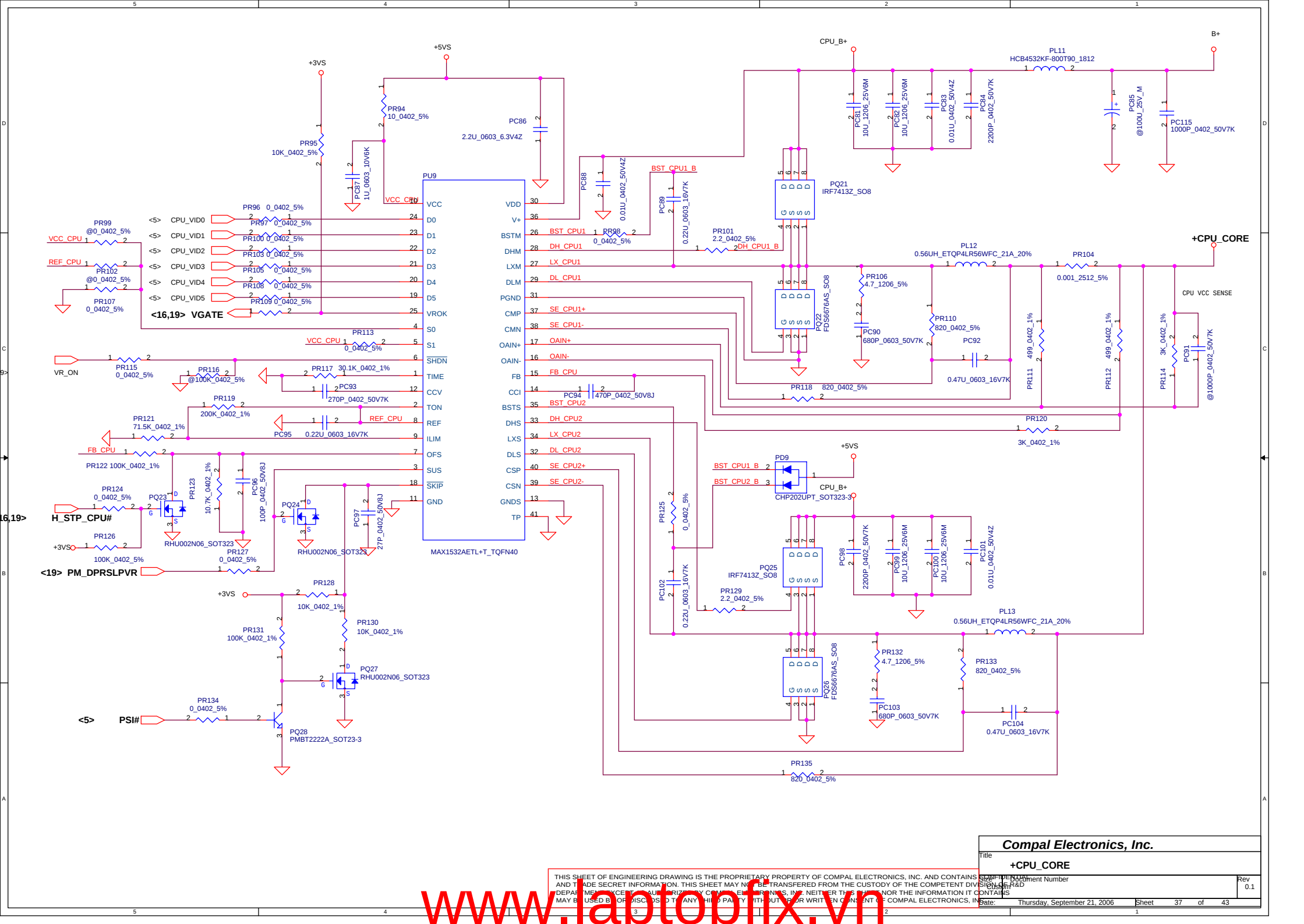
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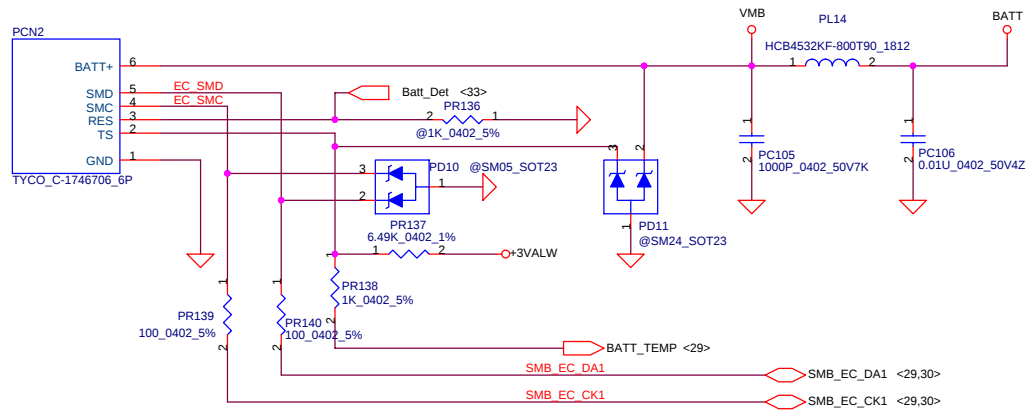
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Date: Thursday, September 21, 2006				Sheet	35 of 43



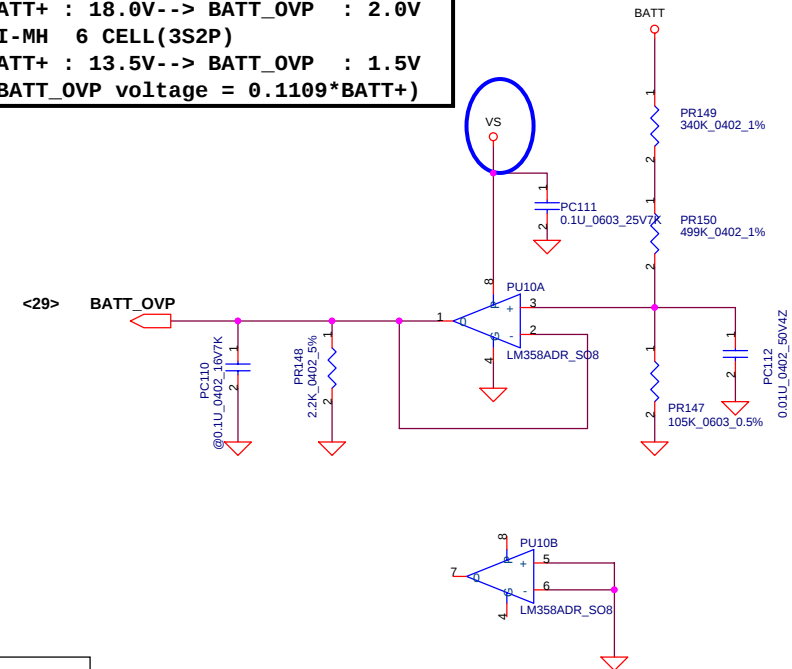
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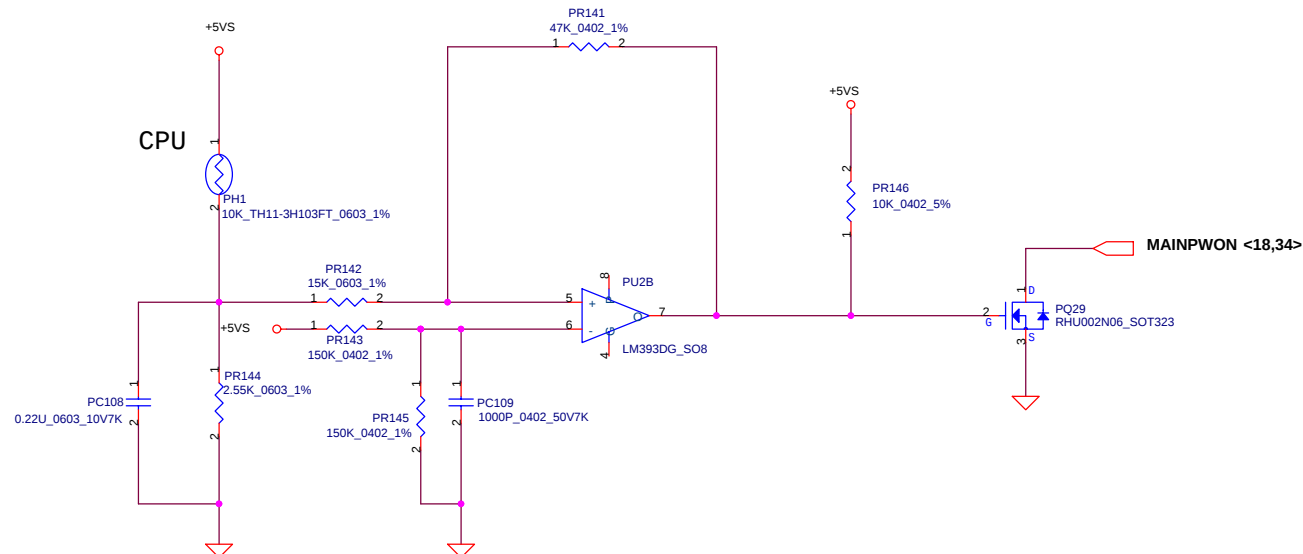
Compal Electronics, Inc.			
Title	+CPU_CORE		
Drawn By	PCB Design Number		
Check By	Rev		
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OVP voltage :
 LI-MH 4 CELL(4S1P)/ 8 CELL (4S2P)
 BATT+ : 18.0V--> BATT_OVP : 2.0V
 LI-MH 6 CELL(3S2P)
 BATT+ : 13.5V--> BATT_OVP : 1.5V
 (BATT_OVP voltage = 0.1109*BATT+)



PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 47 +-3 degree C



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Note	Phase
1			0.2	6	Change C94,C95,C286 from SGA20331D80 to SGA20331D20	Debug DB	
2		Change U31 to LF parts	0.2	25	Change U31 from SA204680000 to SA204680010	Debug DB	
3		LID switch material error	0.2	30	Change SW3 from SN511000300 to SN111000207	Debug DB	
4		CardBus controller material error	0.2	23	Change U38 from SA014100310 to SA014100130	Debug DB	
5		Un-install some bridge between AGND and DGND	0.2	25	Un-install R1934,R1936,R1938,R1940	Debug DB	
6		Let XMIT# match SW's GPIO definition	0.2	24	Delete Q46,R1913,R1914	Debug DB	
7		Modify Head phone sense's level	0.2	27	Delete R1990 ; Change C1526 to 0.1u 0402 cap ; Change R1991 to 20K resistor.	Debug DB	
8		Reserve for SB internal +1.5VALW regulator	0.2	18	Add R81 and R50	Debug DB	
9		HDD and ODD can't work at same time	0.2	21	Add R27 pull high	Debug DB	
10							
11		DB phase loss	0.2	23	JP54(PCMCIA connector) pin 71, pin72 connect to GND	Debug DB	
12		XMIT# Reserved pull high	0.2	24	Reserve R1913 pull high +3VALW		
13		DB phase error	0.2	17	Change RP43, RP44, RP45 package SIZE from 0804 to1206		
14		Cost down	0.2	19	ChangeR732, R733, R737, R739 to RP46		
15		Cost down	0.2	17	ChangeR277, R274, R265, R279 to RP47		
16		Cost down	0.2	17	ChangeR269, R268, R245, R262 to RP48		
17		Reserver a resistor for 2nd source Amp	0.2	27	Add R28 for 2nd source Amp		
18		Avoid DISPLAYOFF# error status to high	0.2	14	Change R120 to 47K and R9 to 4.7K		
19		Avoid DISPLAYOFF# error status to high	0.2	14	Remove R4, C1 and Add C2. Change pull-up RES R8 with +3VALW to Q1 gate net		
20		EMI Request	0.2	23	Change C641 from 0.1u to 680P, Add C1538(680p) for +3V_CB		
21		EMI Request	0.2	23	Change J4, J6 to bead L37, L38(SM010016810)		
22		EMI Request	0.2	31	Add C1540, C1541, C1542, C1543, C1544 for +1.8V cross plane		
23		EMI Request	0.2	14	Add C1533, C1534, C1535, C1536, C1537 for LVDS EMI Solution		
24		EMI Request	0.2	14	Change L35 from R to Bead		
25		EMI Request	0.2	25	Change R1946, R1945 to Bead L40, L41 and Add L39 For codec regulator		
26		EMI Request	0.2	27	Add C1492, C1493		
27		EMI Request	0.2	27	Change R1982, R1987, R1989 to Bead L42, L43, L44		
28							

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1		EMI Request	0.2	28	Add C1539(0.1u) for Touch Pad +5VALW		
2		EMI Request	0.2	22	Add C1516、 C1517 for LAN Transformer		
3		EMI Request	0.2	30	Add C1545、 C1546、 C1547、 C1548、 C1549、 C1550 for Cardbus reference +5VALW power plane to GND		
4		Change LCD pin define	0.2	14	Change LCD pin define		
5		Reserve ESD diode for SPEAKER	0.2	27	Reserve D45		
6		EMI Request	0.2	16	Change PJP14、 PJP15 to Bead		
7		Reserve a resistor to disable AMOM	0.2	25	Add R2012		
8		Place JKCLK series resistor with 2 inches of the 82566	0.2	22	Add R2013 The 33 ohm series resistor is required for signal integrity		
9		Add B channel from compatible with Others	0.3	9	Connect NB LVDS B Channel to LVDS connector		
10		Modify DISPLAYOFF# circuit	0.3	14	Connect BK_EN and BKOFF# to U13A gate to generate DISPLAYOFF#		
11		Let EC control BK_EN	0.3	29	Remove D28,D13 add R2014, Change R9 from 4.7Kohm to 100Kohm		
12		EC Reset dis-charge	0.3	29	Connect BK_EN from NB to EC pin33(GPIO15)		
13		EC Reset dis-charge	0.3	29	Add a DIODE D46 for EC reset discharge		
14		MotherBoard ID change to PV	0.3	29	R1996 install 1Kohm,R1997 install 2Kohm		
15		Change LVDS CONN pin assignment for compatible	0.3	14	Add LVDS Channel B from NB and change pin assignment		
16		Reserve two USB port connector	0.3	19	Add JP59,R2017,R2018		
17		Reserve bottom board connector	0.3	30	Add JP60,R2015		
18		Modify LVDS power circuit	0.3	14	Change Q3 pull high from +3VAL to +5VAL,Add R2016,C1551		
19		Delete MB standoff	0.3	31	Change C1532 from 0.01U to 0.047U		
20		Delete L39	0.3	25	Delete H22		
21		WL ON/OFF & Wireless LED pull high voltage	0.3	28	Delete L39		
22		EMI Request	0.3	22	Change pull high voltage form +5VS to +3VS;R1915 from 200 ohm to 27ohm		
23		Change amplifier gain	0.3	27	Add C1552,C1553		
24		Change value of RTC capacitor	0.3	18	Change R425,R424 from 34.8k to 20k; R429 from 16.2k to 10k		
25		EMI Request	0.3	28	Change C115,C113 from 18P to 15P		
26		Reserve +3VS for LAN connector LED	0.3	22	Reserve D47		
27		EMI Request	0.3	12	Add R2019,R2020		
28			0.3		Change C562,C563,C566,C567,C568 from 680P to 220P		

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	LAN signal measure fail on Intel site	Delete EMI capacitor	1.0	22	Change C1516,C1517 to NI		
2	WLAN LED work wrong	Add two resister to select WL_LED and XMIT#	1.0	24	Add R2021,R2022 ; R2022 NI ,R2021 0 ohm		
3		increase RTC battery life	1.0	18	D42 pin2 change power form +3VALW to +3VLP		
4	EMITest fail from LAN	Follow intel reference design	1.0	22	C1517 change form 0.01u to 0.1U and C1516 NI		
5	EMITest fail from LAN	Add parallel damping test is PASS but marging	1.0	18, 22			
6	MIC always on have noise	Add MIC_Sense pin to detect MIC plug in	1.0	25	R1954 change from 10k to 0 ohm		
7	MIC always on have noise	Add MIC_Sense pin to detect MIC plug in	1.0	27	Add R ? and C ? , MIC connector pin 3、 pin 5 connect to AGND		
8	M/B ID	Change to 3.3V for MV	1.0	29	R1997 Change to NI		
9	reduce S3 power consumption	Disable wake on LAN function	1.0	19 20 22	Change R16,R11R70 to NI;R15,R12,R71 0 hom		
10	AMON capacitor duplication	C1533,C1552 replace with MC906,MC908	1.0	26	Change MC906,MC908 NI		
11							
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Compal Electronics, Inc.

PIR

Document Number

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Version change list (P.I.R. List)

Power section

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Item	Reason for change	PG#	Modify List	Date	Phase
1	Fine tune the 1.8V OCP set-point as 7.5A (minimum continue load)	35	Change PR68 From SD034182280 (S RES 1/16W 18.2K +-1% 0402) To SD034154280 (S RES 1/16W 15.4K +-1% 0402)	2006/05/26	Before DB
2	Fine tune the charge current as 3A (maximum)	33	Change PR20 From SD034137380 (S RES 1/16W 137K +-1% 0402) To SD034100380 (S RES 1/16W 100K +-1% 0402)	2006/05/30	Before DB
3	Fine tune the AC detector set-point	33	Change PR26 From SD034681380 (S RES 1/16W 681K +-1% 0402) To SD028100480 (S RES 1/16W 1M +-5% 0402)	2006/05/30	Before DB
4	Fine tune the 1.05V OCP set-point as 8.125A (minimum continue load)	36	Change PR82 From SD034274180 (S RES 1/16W 2.74K +-1% 0402) To SD000009480 (S RES 1/16W 1.47K +-1% 0402) Change PR92 From SD034909280 (S RES 1/16W 90.9K +-1% 0402) To SD034499280 (S RES 1/16W 49.9K +-1% 0402)	2006/05/30	Before DB
5	Fine tune the 1.5V OCP set-point as 5A (minimum continue load)	36	Change PR83 From SD034274180 (S RES 1/16W 2.74K +-1% 0402) To SD000009480 (S RES 1/16W 1.47K +-1% 0402) Change PR93 From SD034909280 (S RES 1/16W 90.9K +-1% 0402) To SD034715280 (S RES 1/16W 71.5K +-1% 0402)	2006/05/30	Before DB
6	ID pin for 4 cells battery	38	Add PR136 SD028100180 (S RES 1/16W 1K +-5% 0402)	2006/05/30	Before DB
7	PL1 crack issue	32	As manufactory's comments, change the PL1 from multi-layer bead to beadcore	2006/07/13	DB
8	Modify the sequence of 3V/5V when DC mode	34	Connect the PQ30.1 from VS to +3VLP Change PC41 from 0.1u to 0.047u	2006/07/10	DB
9	The transient of +1.8V is fail	35	Change PR69 from 49.9K to 90.9K for transient	2006/07/12	DB
10	Due to the unstable of ISL6227, change the +1.5V/ +1.05V solution to MAX8743	36	Change the +1.5V/ +1.05V solution from ISL6227 to MAX8743, included all the related components.	2006/07/7	DB
11	For EMI's concern	35	Add PC116 (680pf)	2006/07/17	DB
12	For EMI's concern	37	PC115 (1000pf), PR106/PR132 (4.7ohm), and PC90/ PC103 (680pf)	2006/07/17	DB
13	Modify the sequence of 1.8V for S3 can't resume issue	35	Change connection of PR64.1 from +5VS to +5VALW	2006/08/02	SI
14	For 4 series/ 3 series battery selection, add circuit for changing charge voltage as 16.8V (4 series) or 12.6V (3 series)	33	Add PQ33, PQ34, PR154, PR155 and PR156	2006/08/10	SI
				Compal Electronics, Inc.	
				Title PWR PIR	
				Revision Number LA-3361	
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