

Compal Confidential

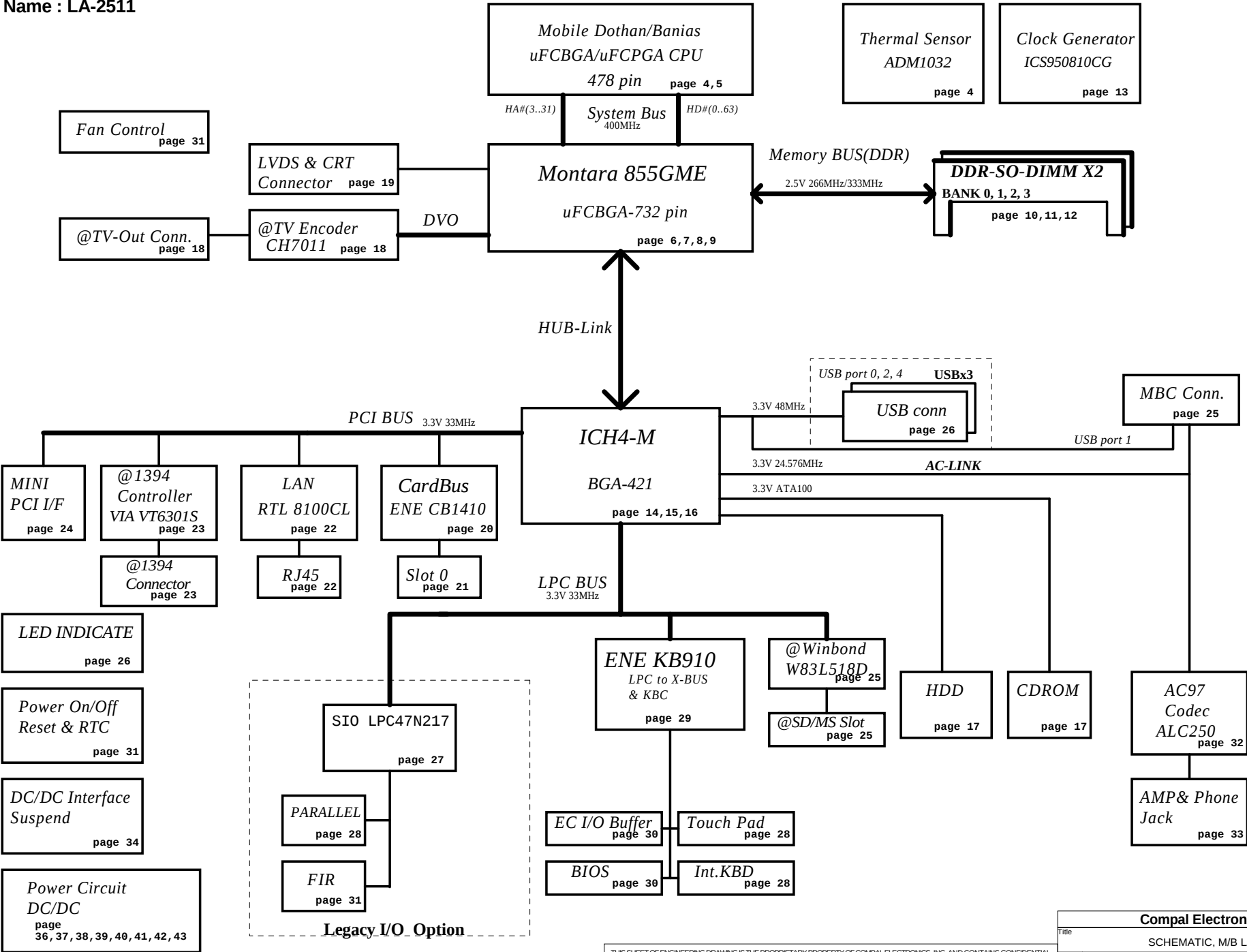
Schematics Document

Dothan/ Bantias uFCBGA/uFCPGA
Package
with Montara-GME Core Logic
REV: 0.1

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File Name : LA-2511



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
R368	100K +/- 5%			
Board ID	R361	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

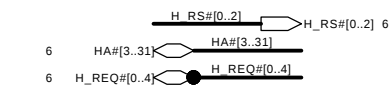
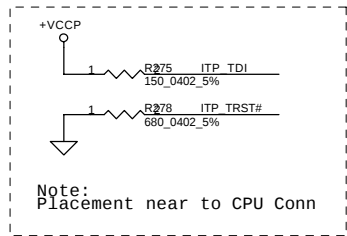
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	1.0
4	
5	
6	
7	

External PCI Devices

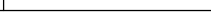
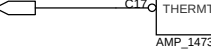
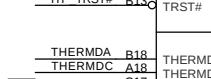
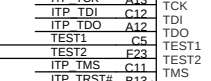
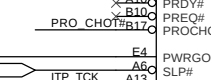
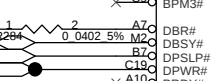
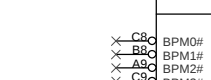
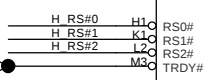
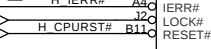
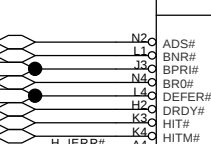
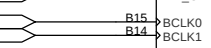
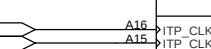
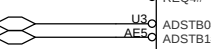
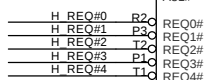
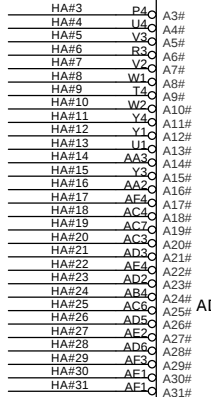
Device	IDSEL#	REQ#GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

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JP12A



Banias

ADDR GROUP

DATA GROUP

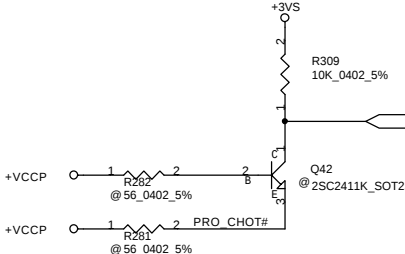
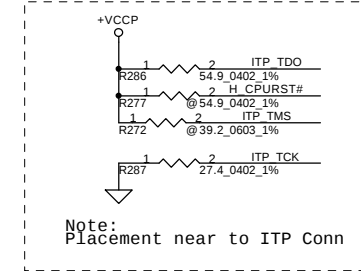
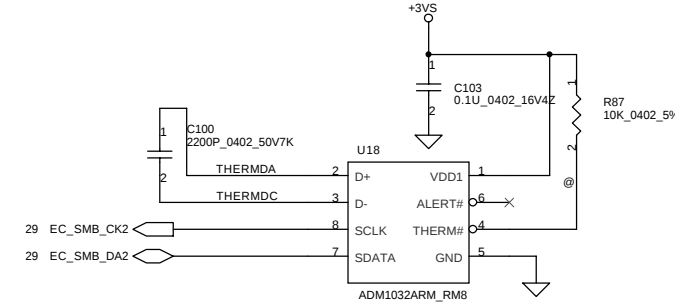
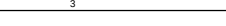
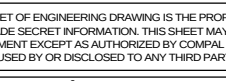
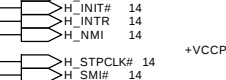
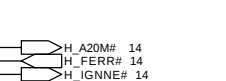
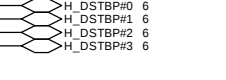
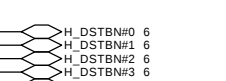
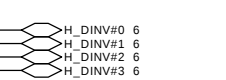
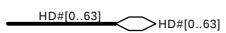
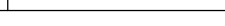
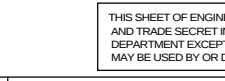
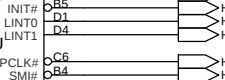
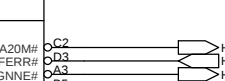
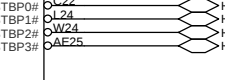
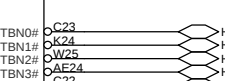
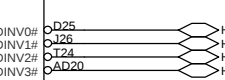
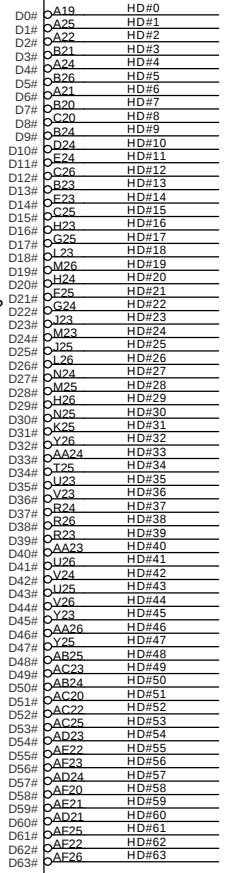
HOST CLK

CONTROL GROUP

MISC

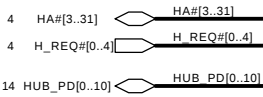
THERMAL DIODE

LEGACY CPU

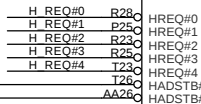
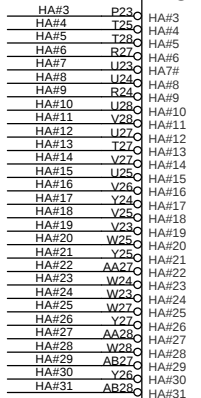


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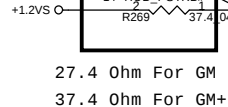
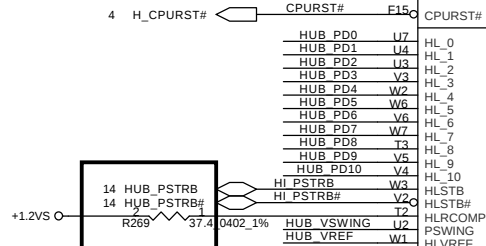
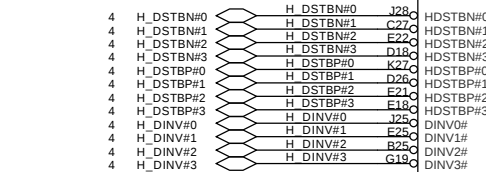
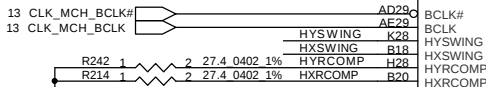
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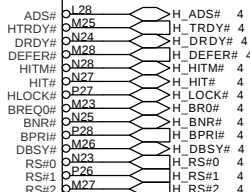
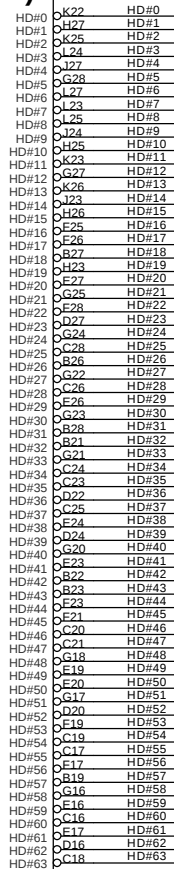
Montara-GM(L)



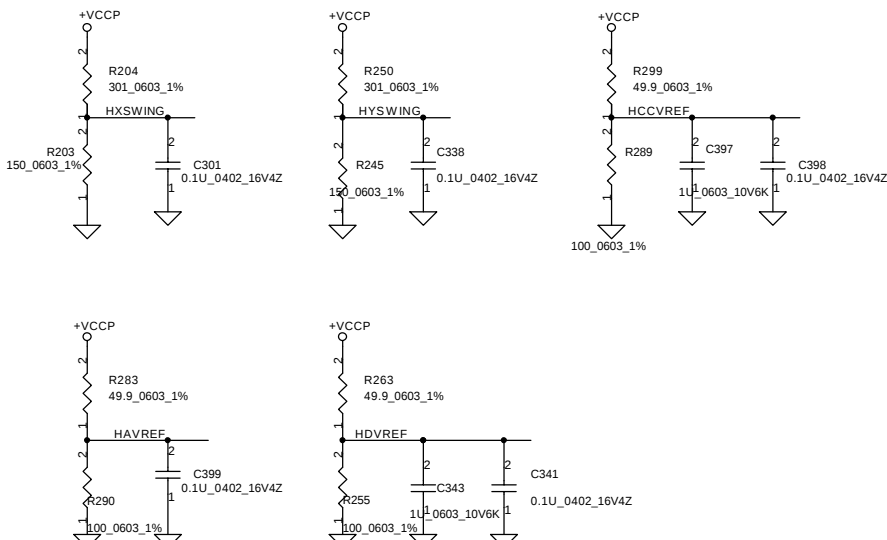
HOST



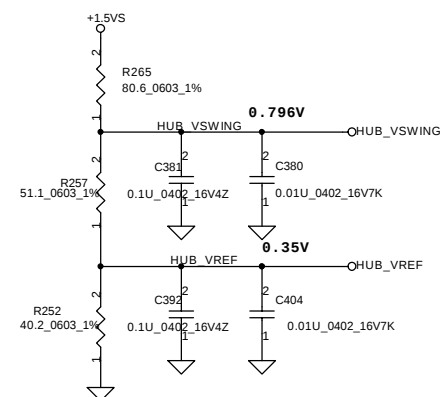
RG82G4350M_uFCBGA732



HOST REF VOLTAGE



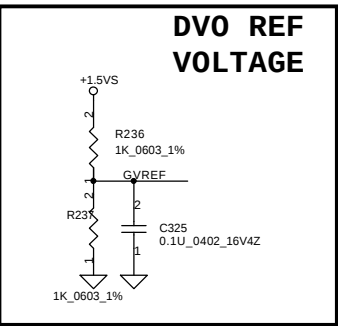
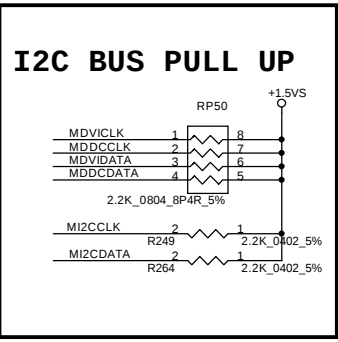
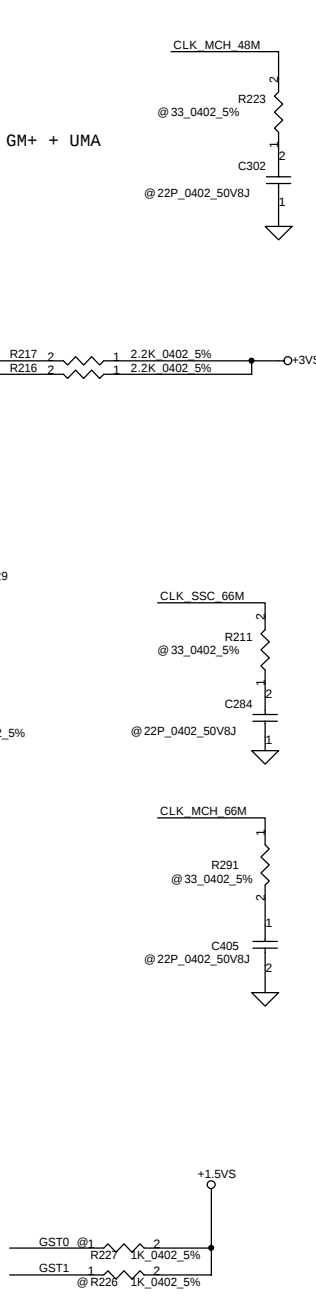
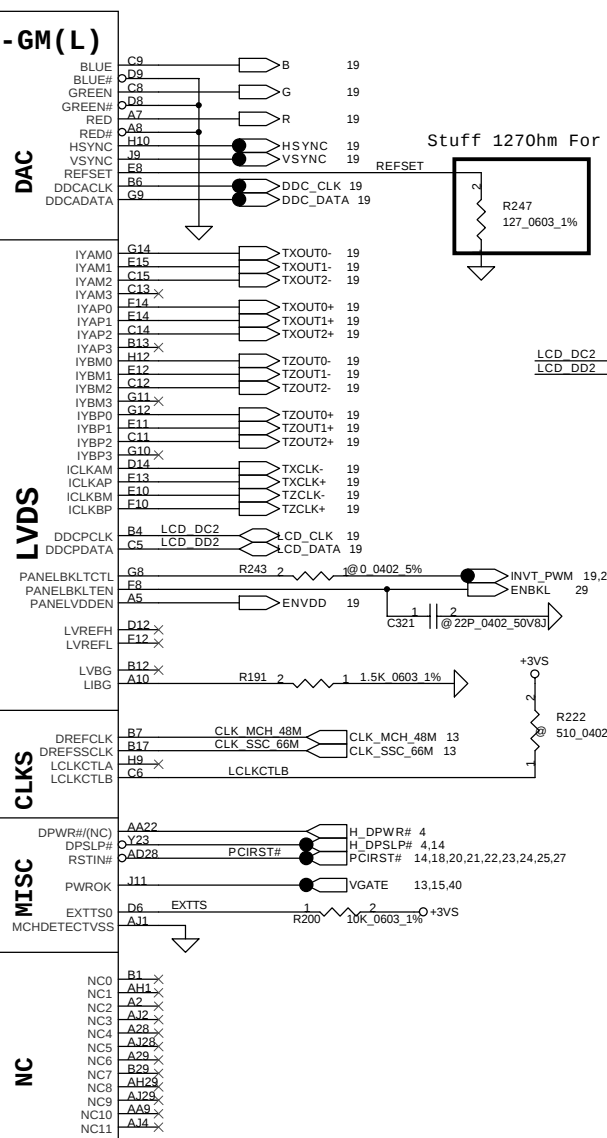
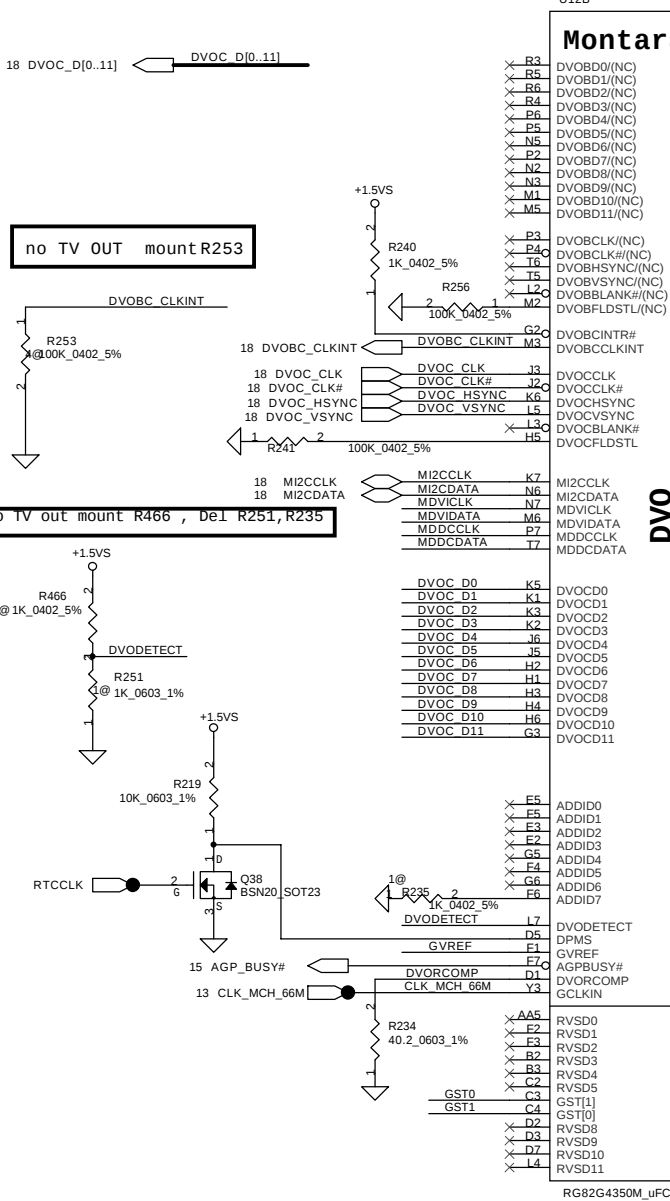
HUB I/F REF VOLTAGE



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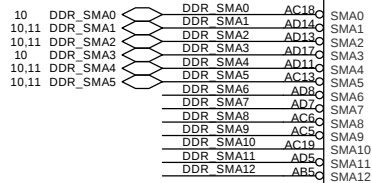
Starp pin list

LCLKCTLB: High for P4
N.C. for Banias(default low)
DVODETECT: Low to enable DVO
High to disable DVO

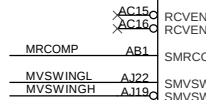
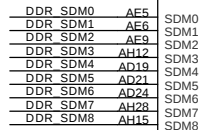
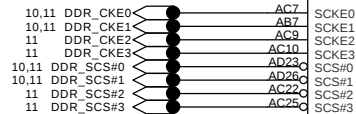
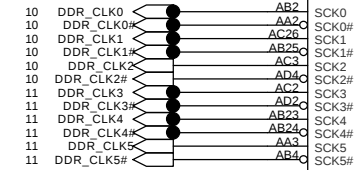
GST0	GST1	PSB/Sys Mem/ GFX Core
0	0	400/266/200 (default)
0	1	400/200/200
1	0	400/200/133

U12C

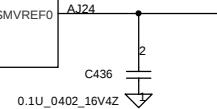
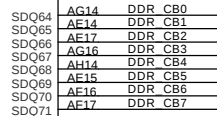
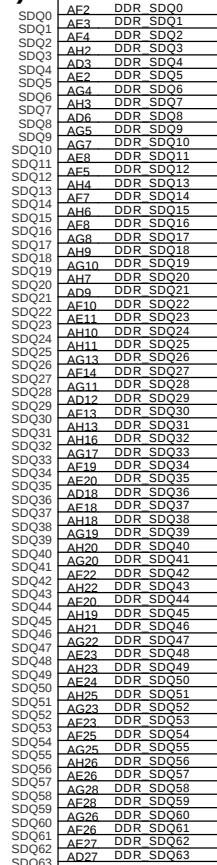
Montara-GM(L)



MEMORY

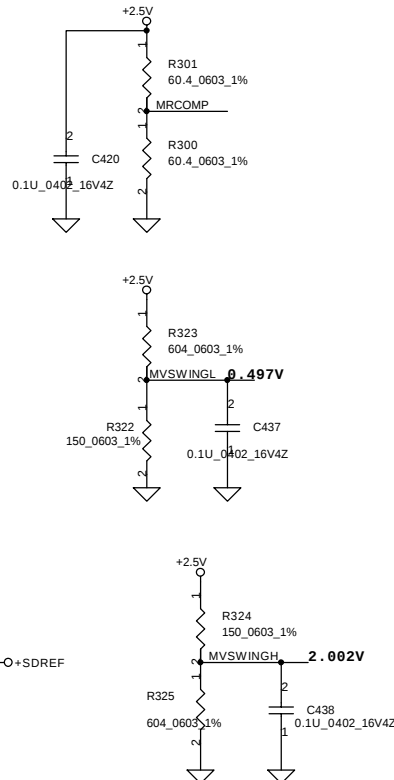


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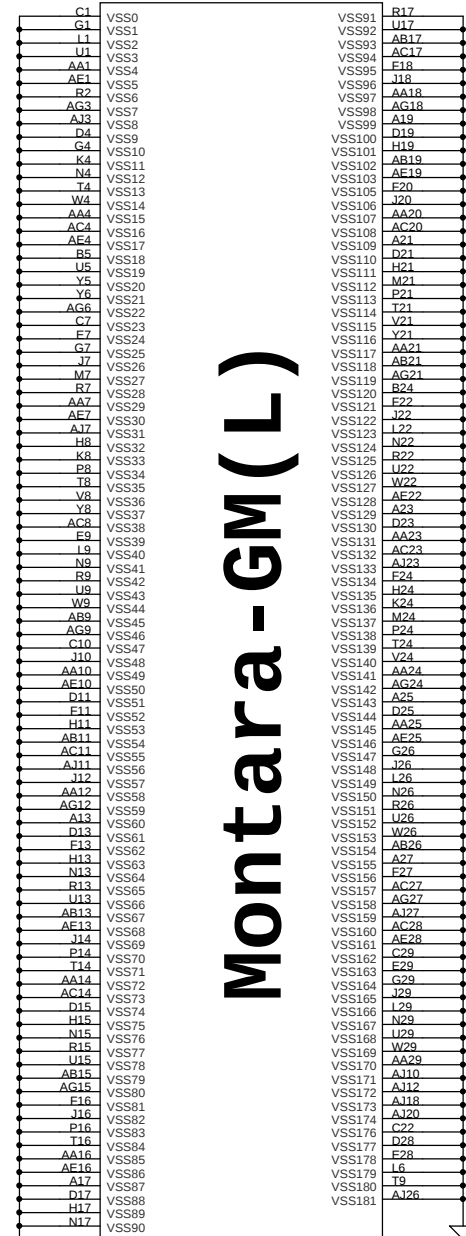


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DDR REF & SWING VOLTAGE



U12D

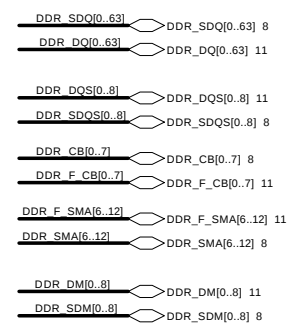
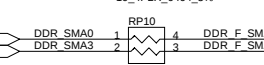


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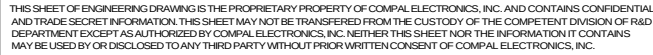
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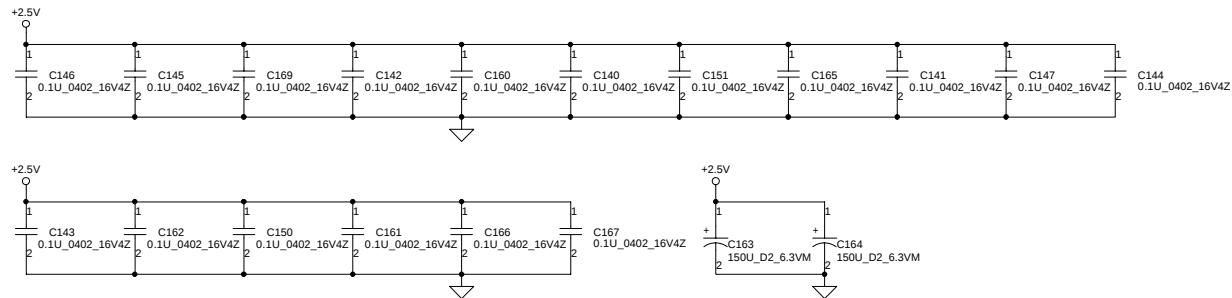
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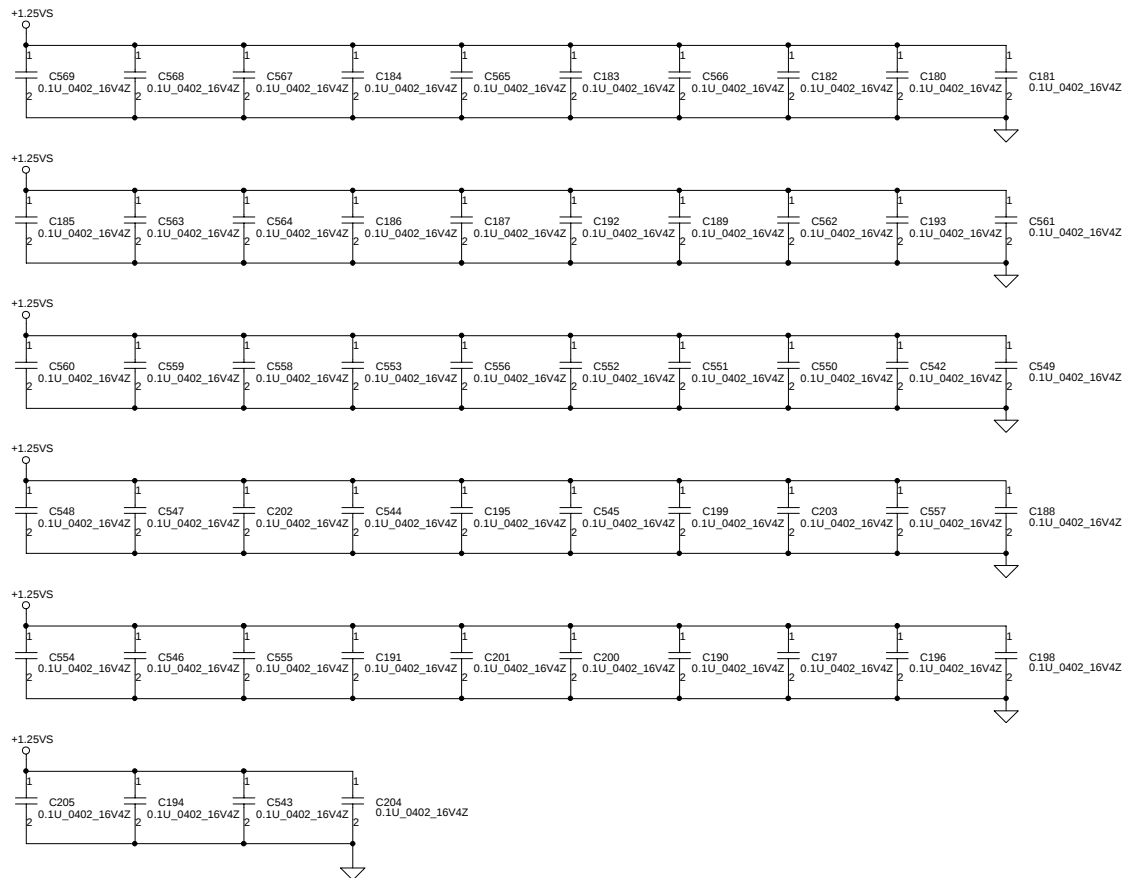
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Layout note :
Distribute as close as possible
to DDR-SODIMM.

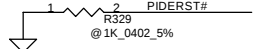
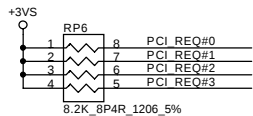
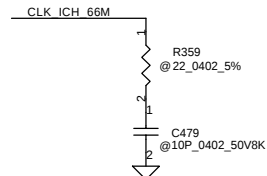
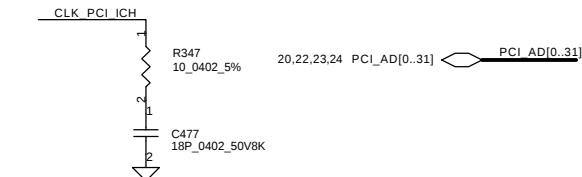


Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V

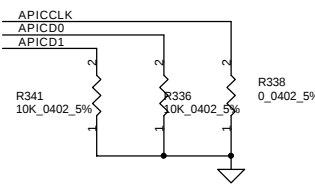
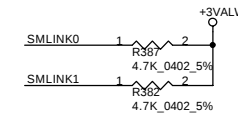
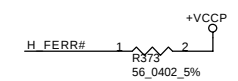
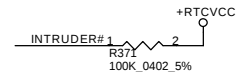
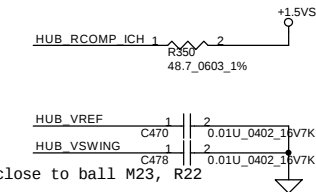
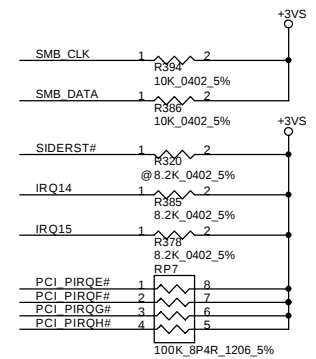
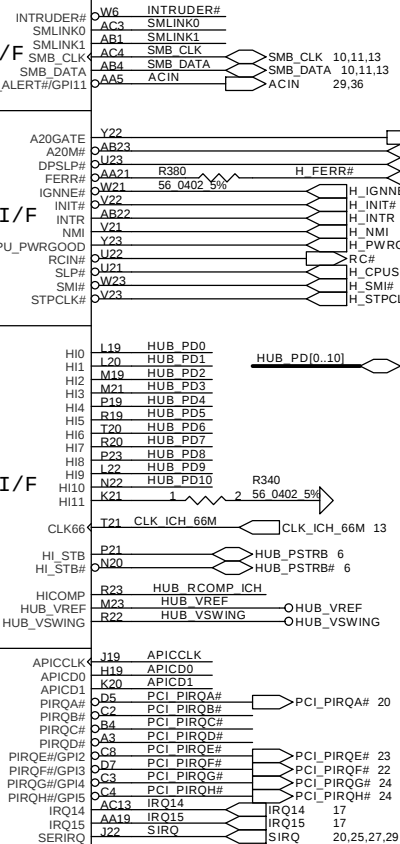
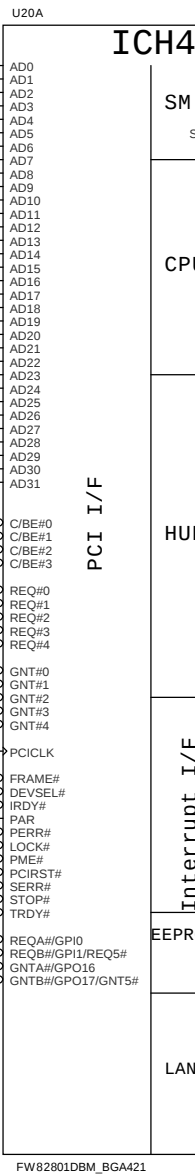
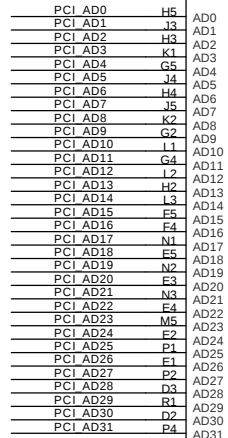
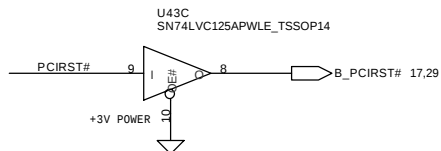
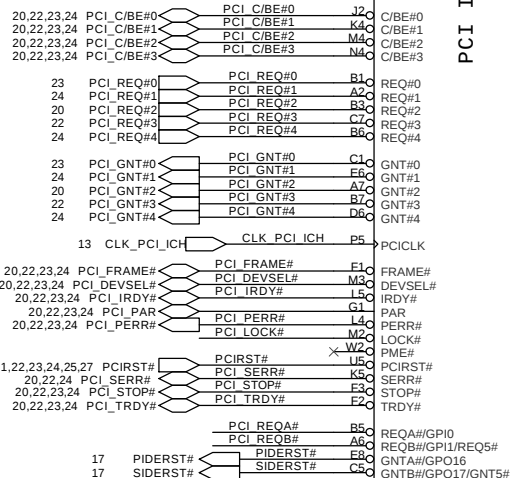
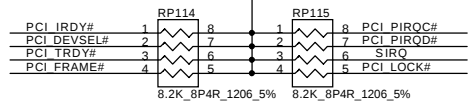
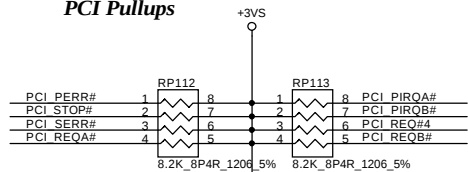


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PCI Pullups



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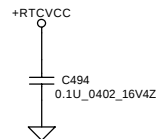
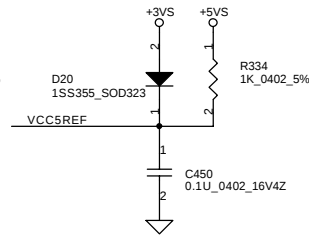
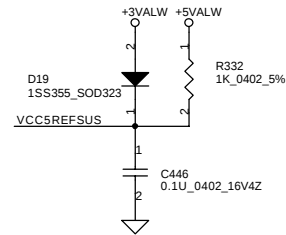
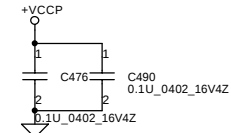
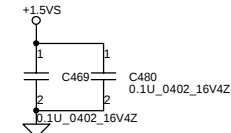
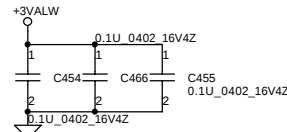
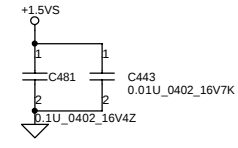
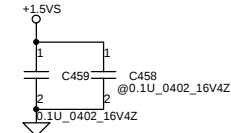
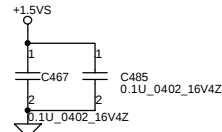
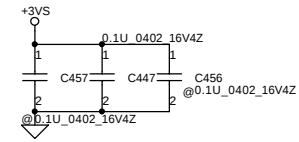
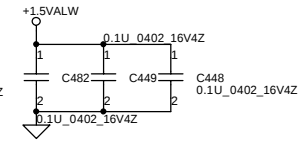
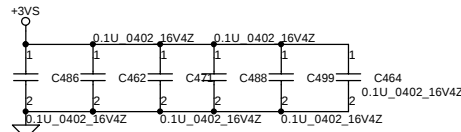
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U20C

ICH4

GND POWER

FW82801DBM_BGA421

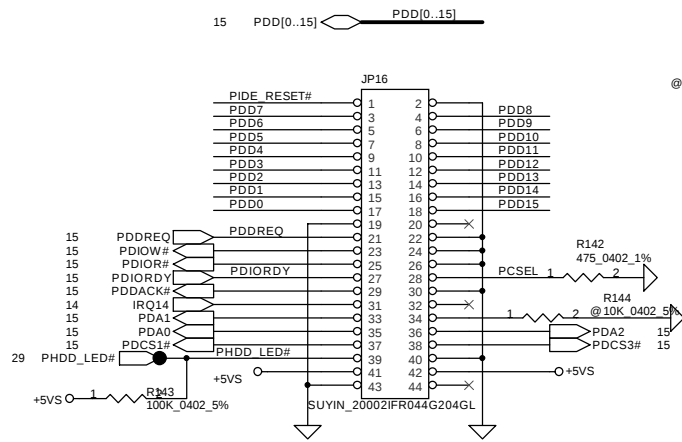


Compal Electronics, Inc.

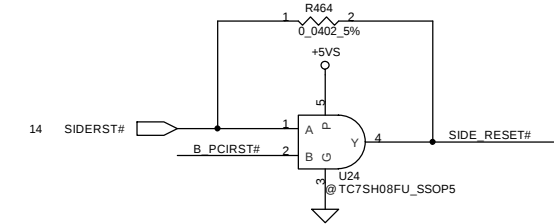
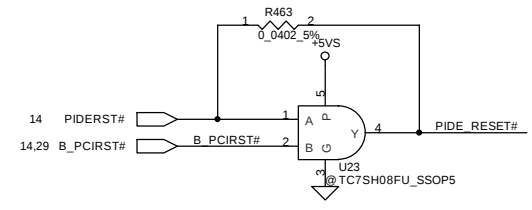
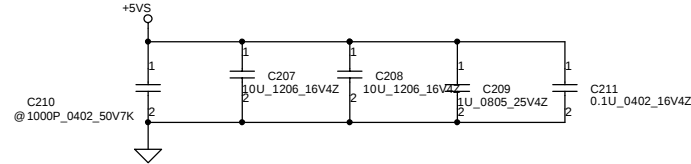
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HDD Connector

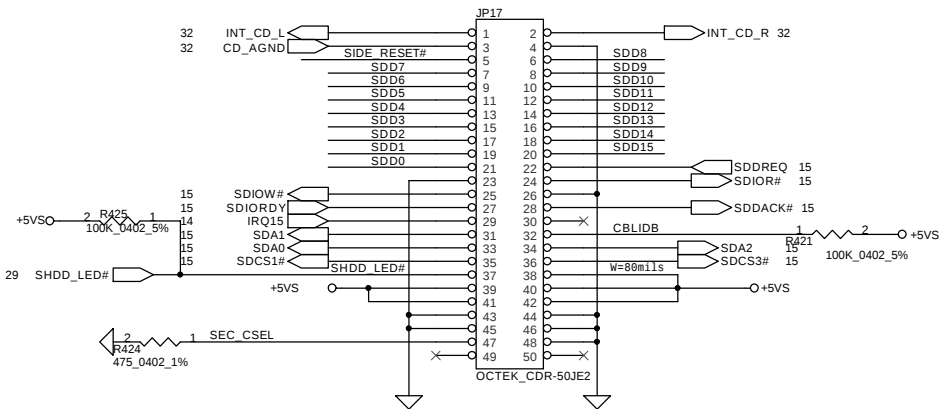


Placea caps. near HDD
CONN.

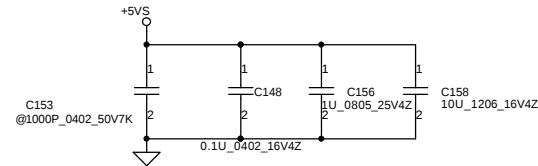


CD-ROM Connector

SDD[0..15] SDD[0..15] 15



Placea caps. near CDROM
CONN.



Compal Electronics, Inc.

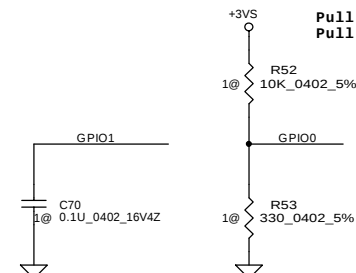
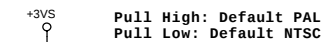
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Size Document Number 401313 Rev B

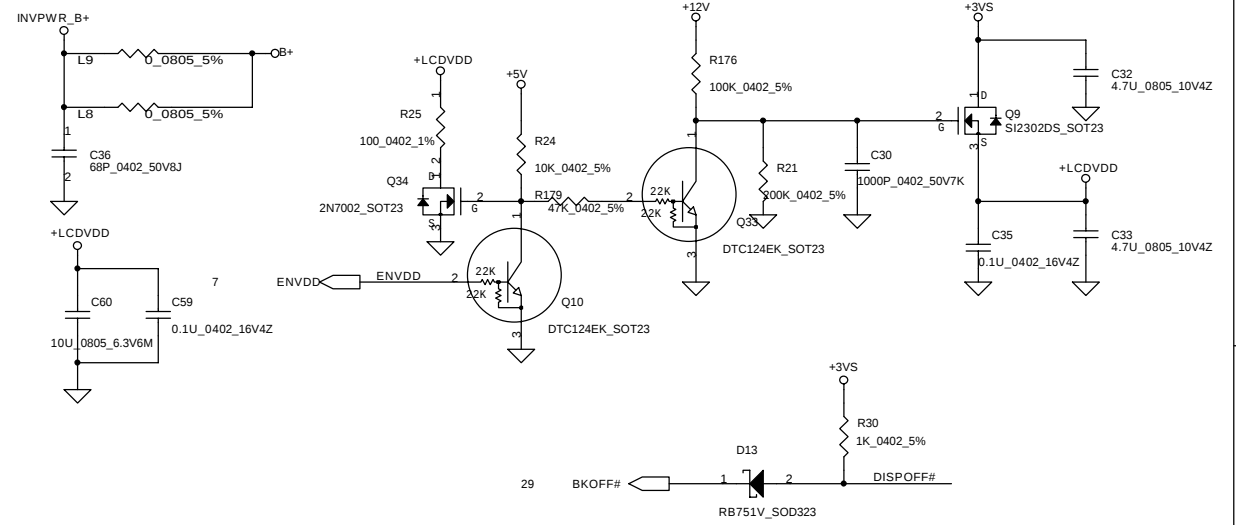
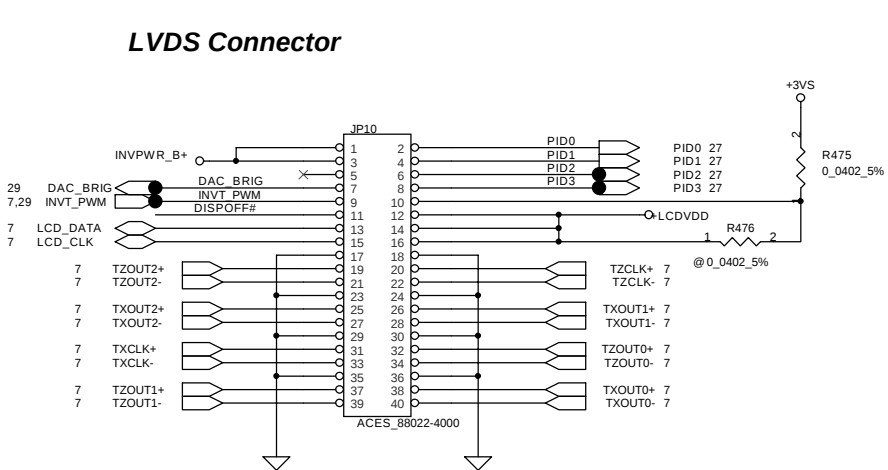
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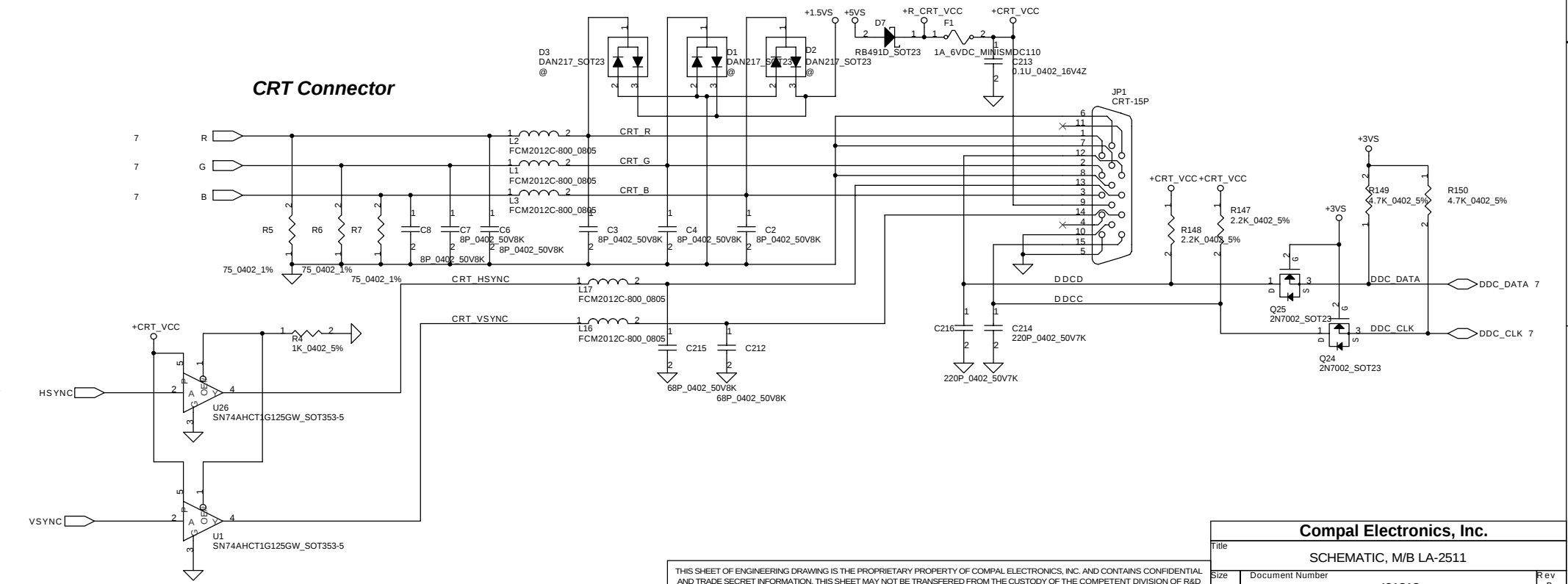
TV Encoder



LVDS Connector

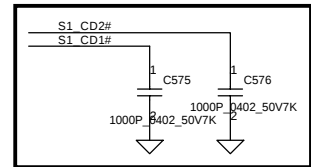


CRT Connector



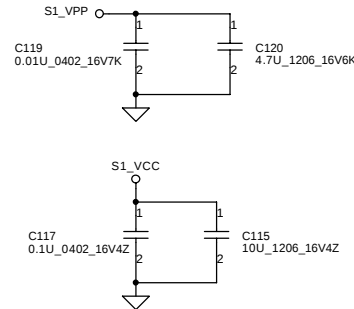
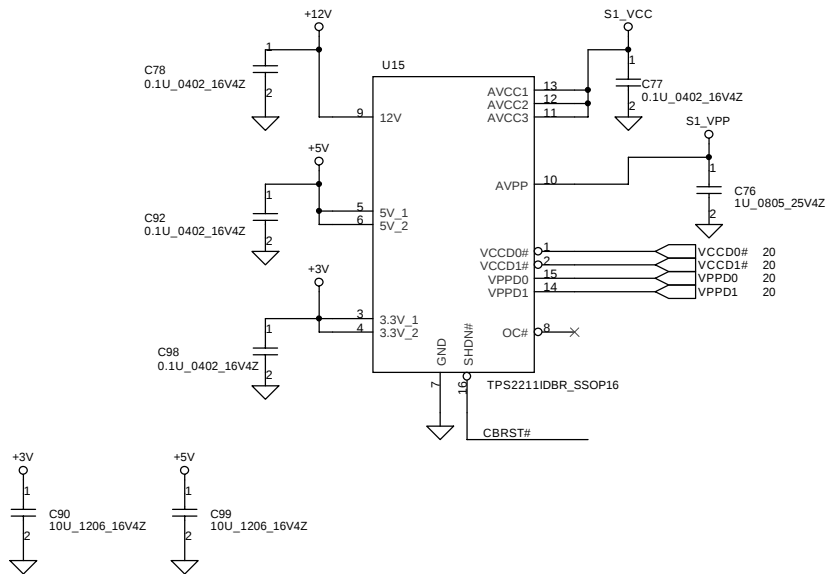
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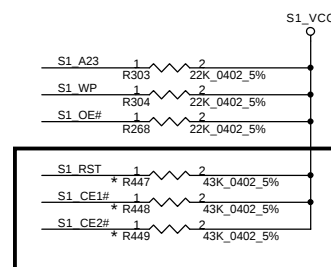
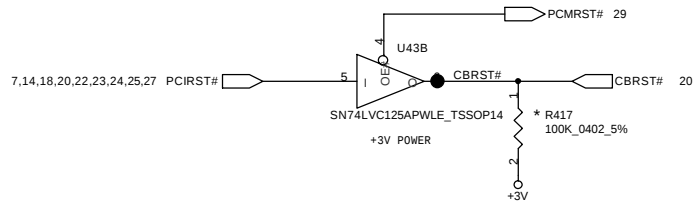
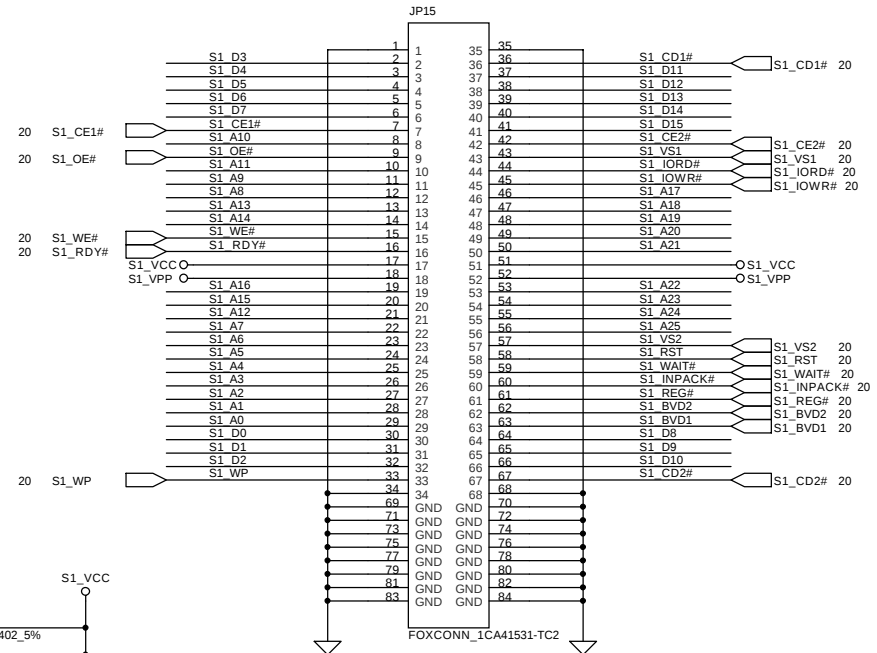


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PCMCIA Power Controller



CardBus Socket

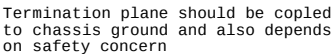


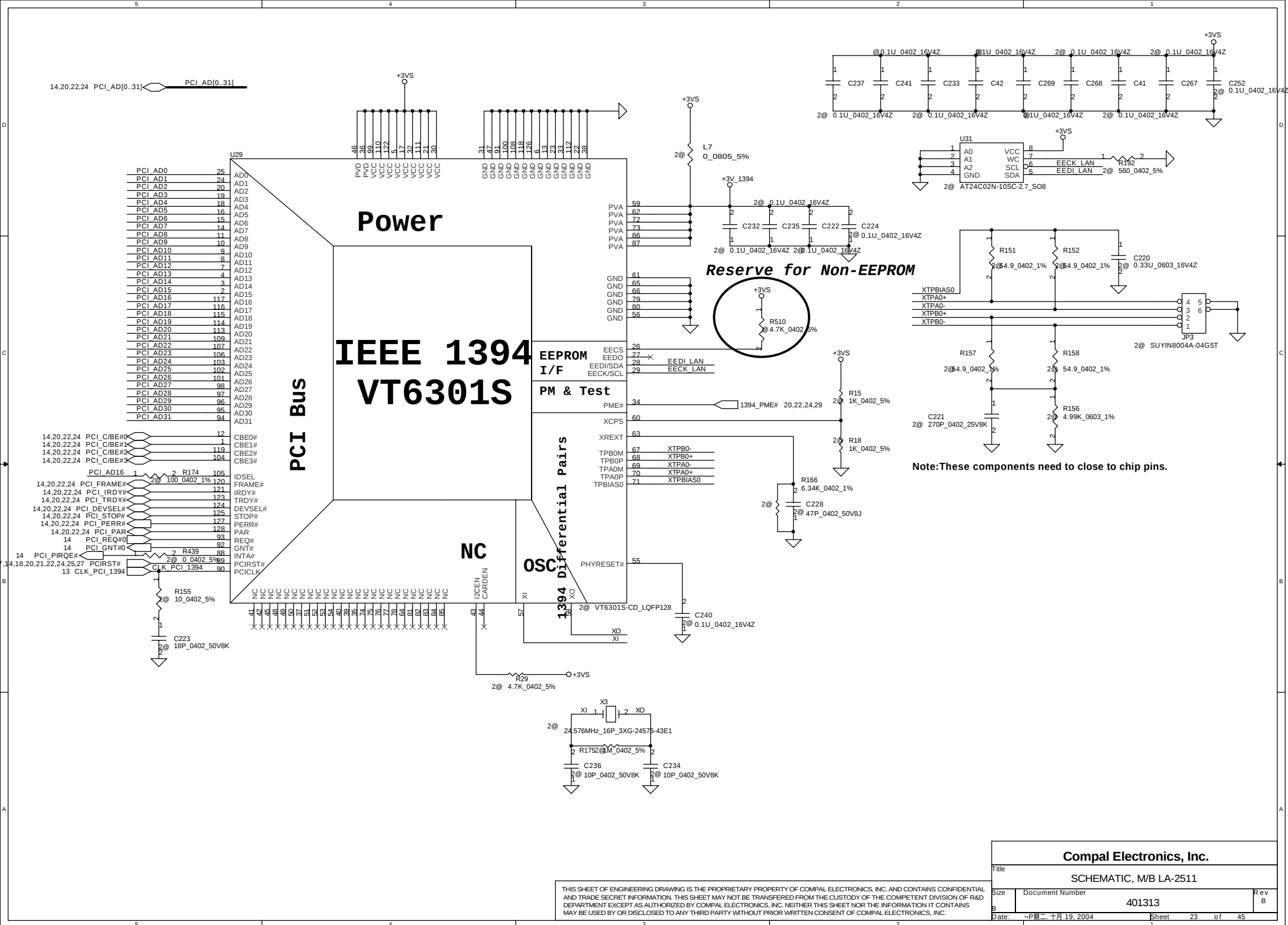
Reserve for CB1410 B0 Version

Compal Electronics, Inc.

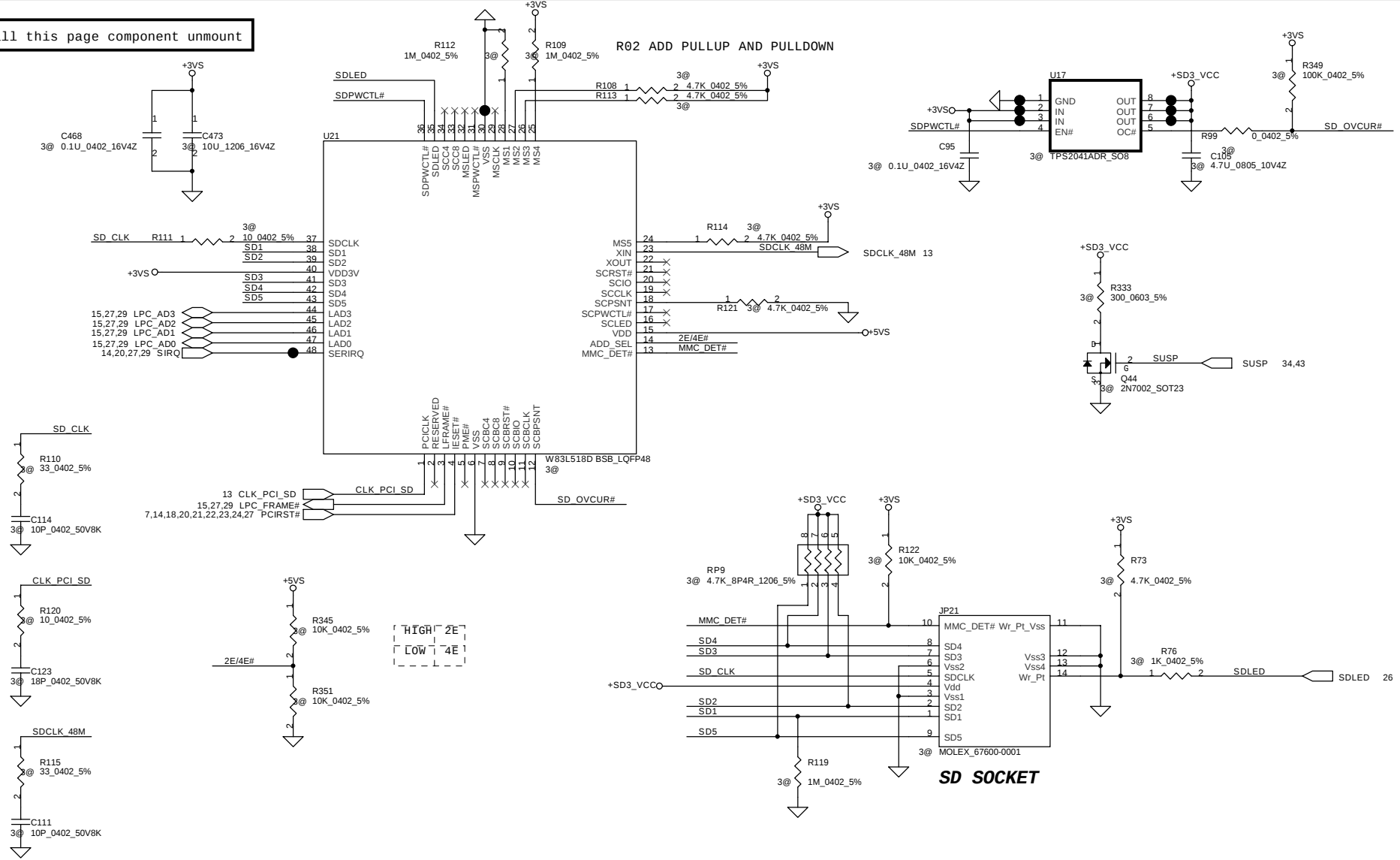
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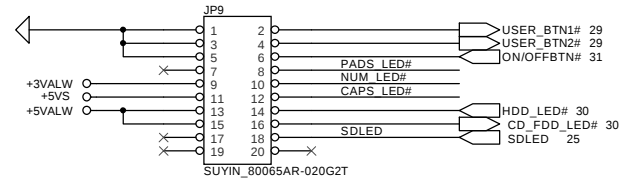
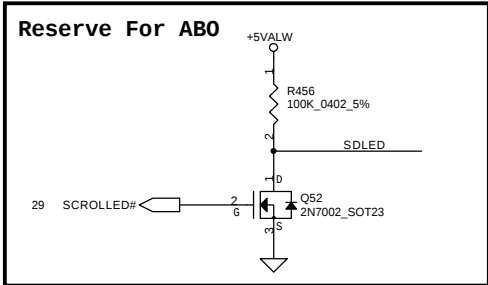
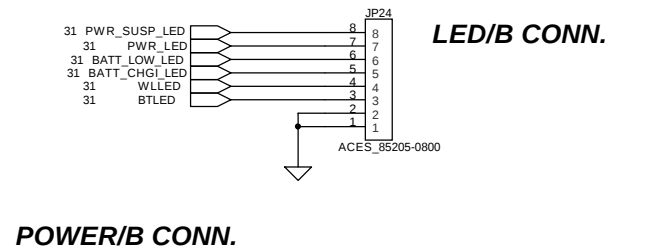
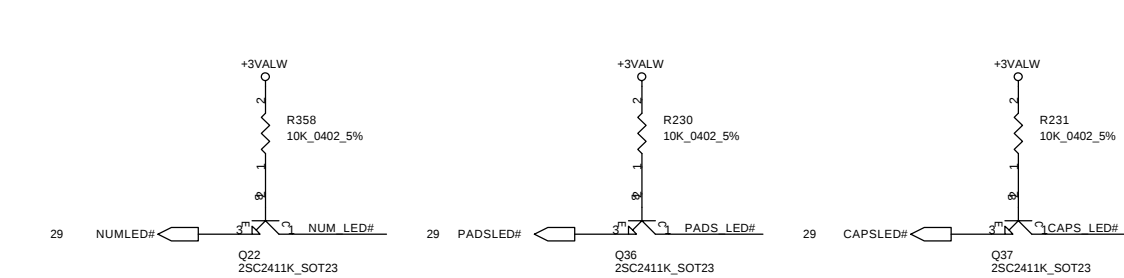
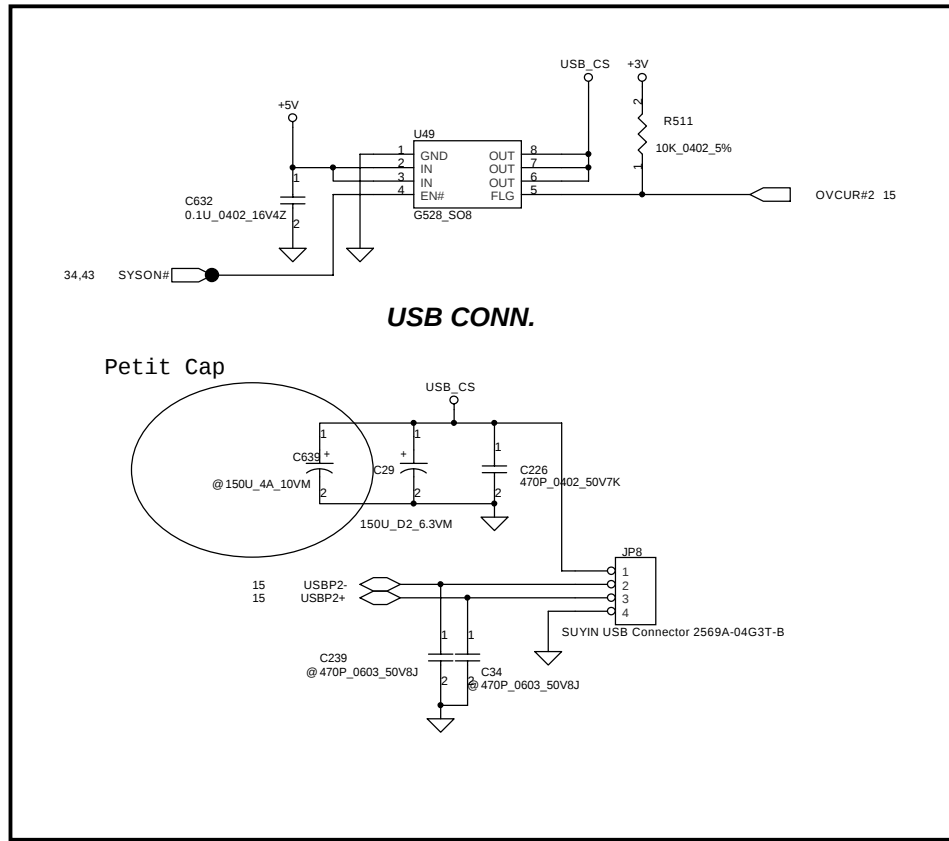
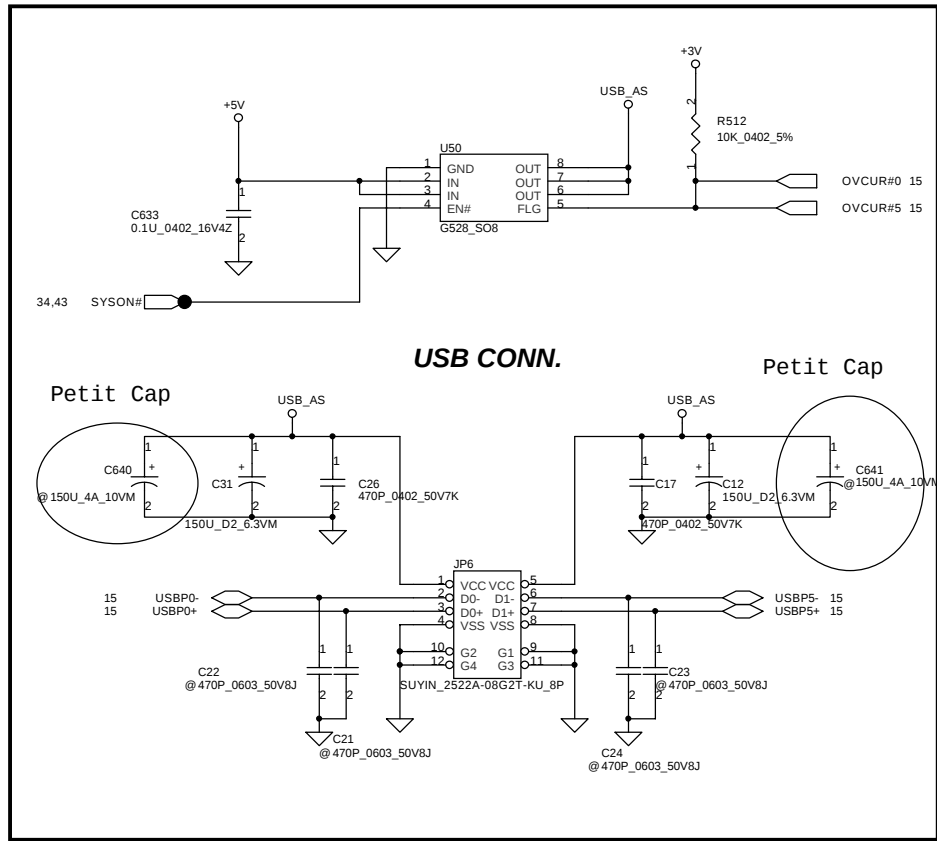
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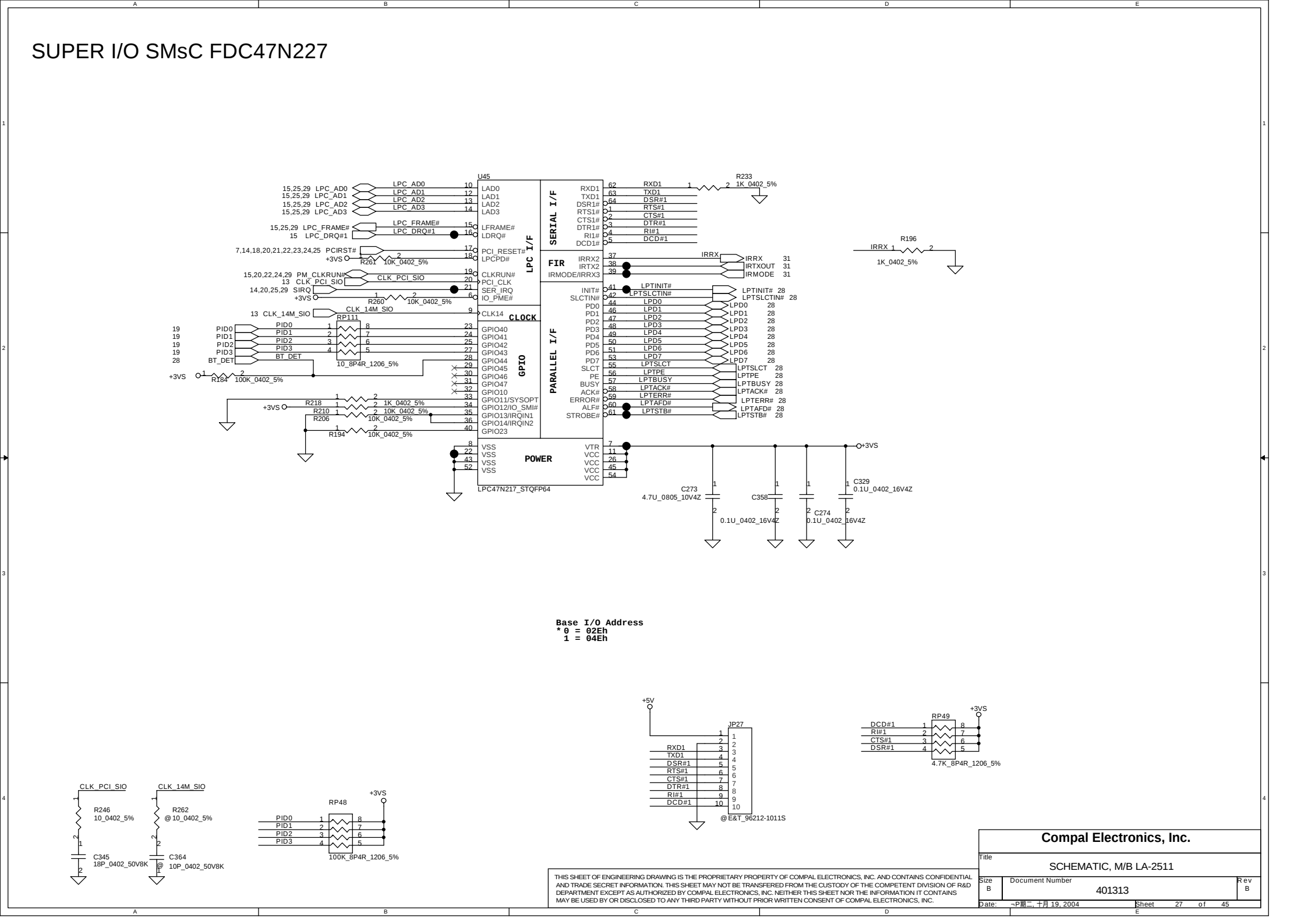
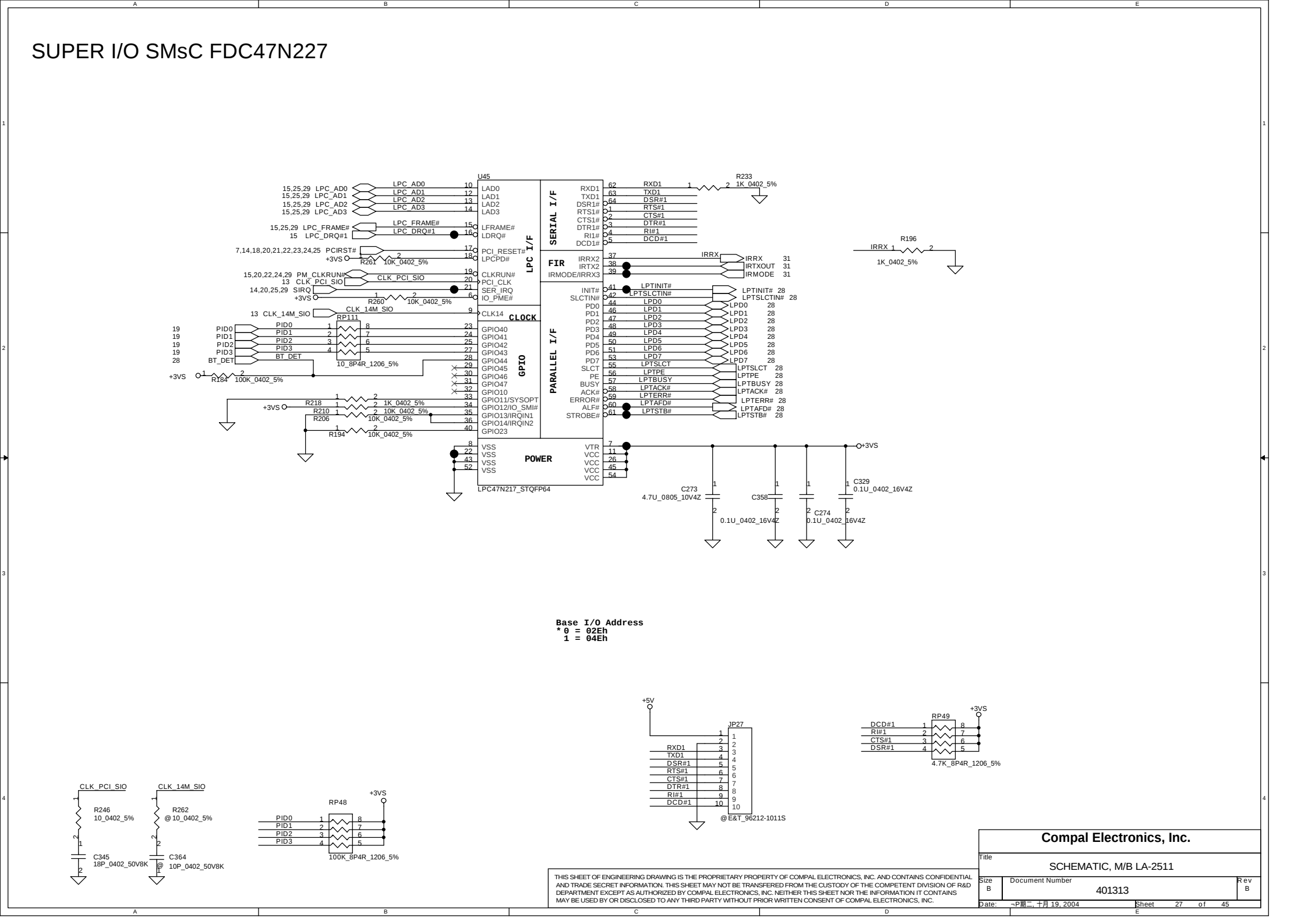
FOR ABO: all this page component unmount



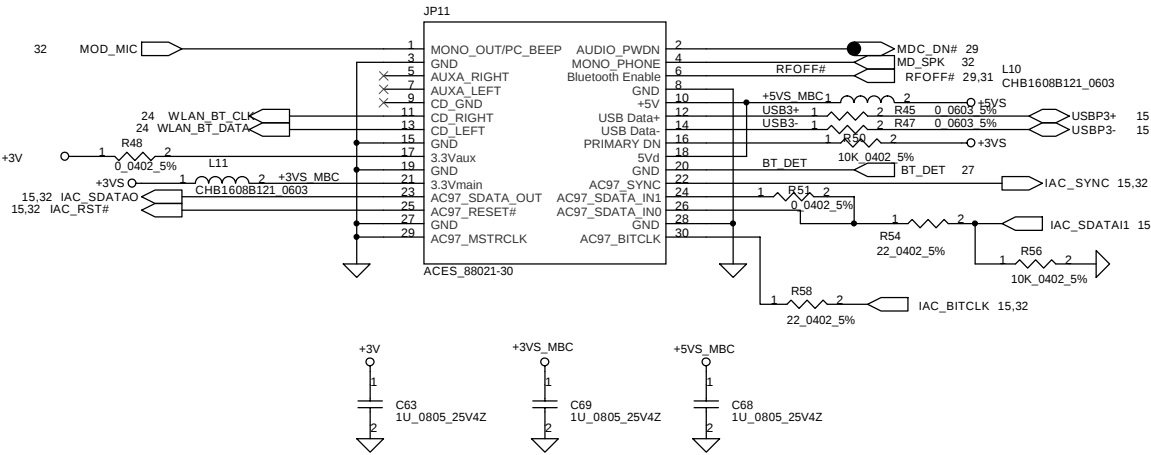


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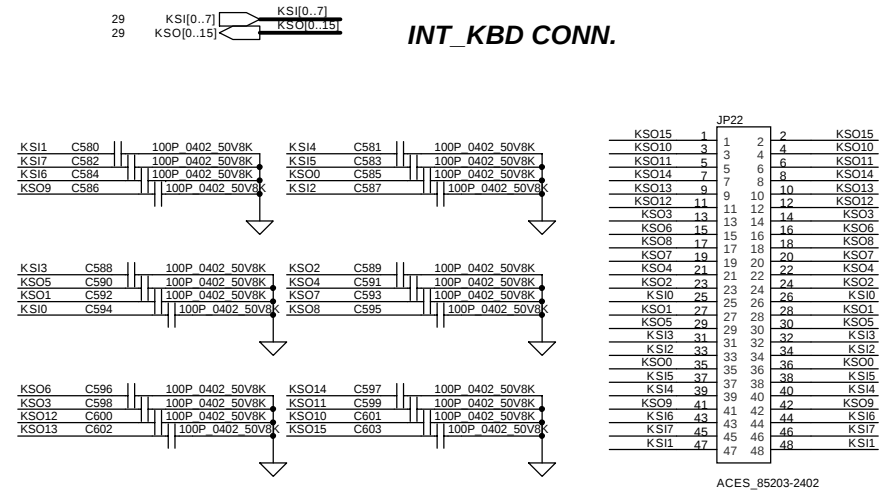
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MBC CONN.

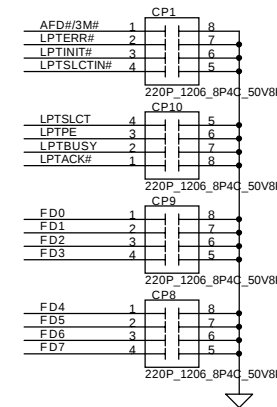
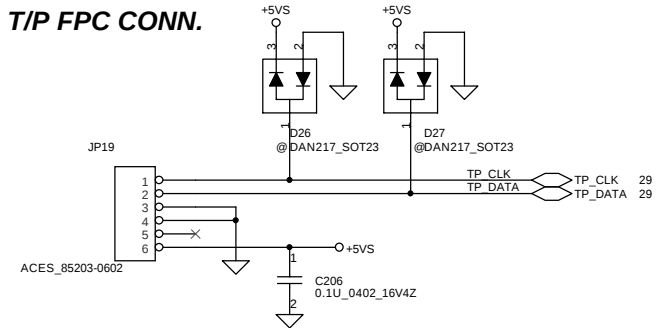


INT_KBD CONN.

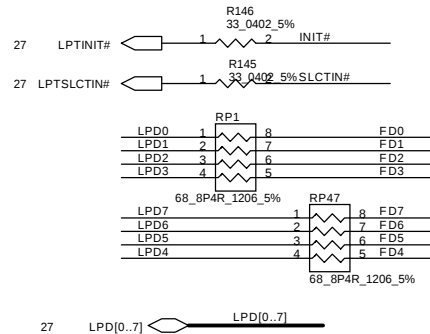
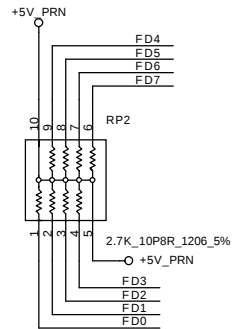
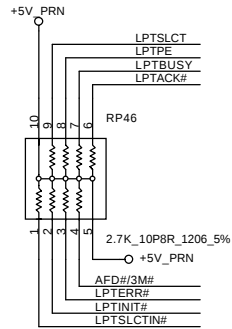
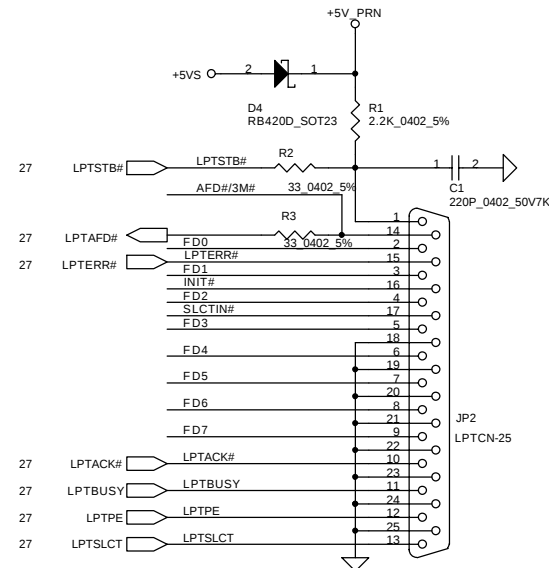


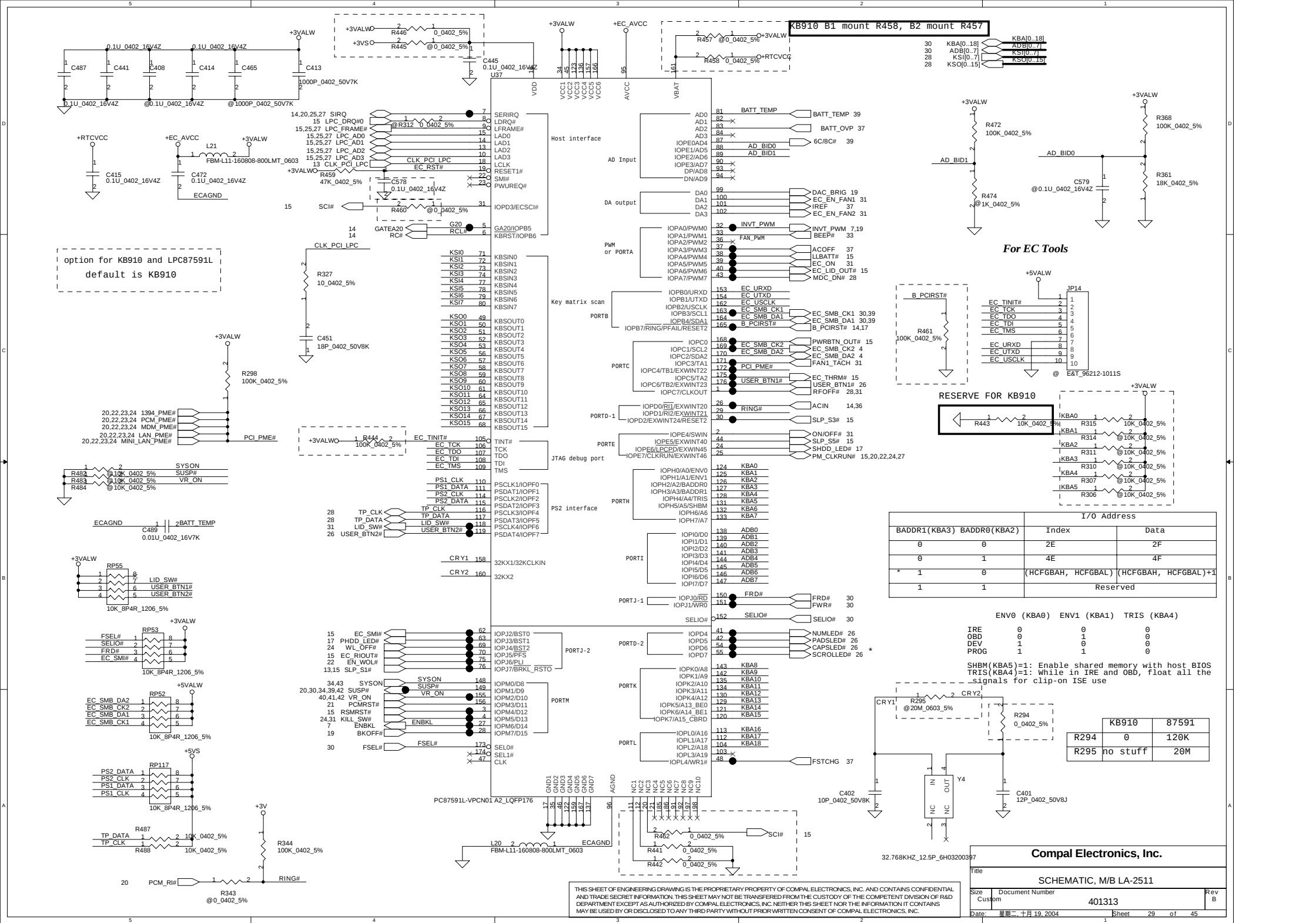
As close as possible to K/B connector

T/P FPC CONN.

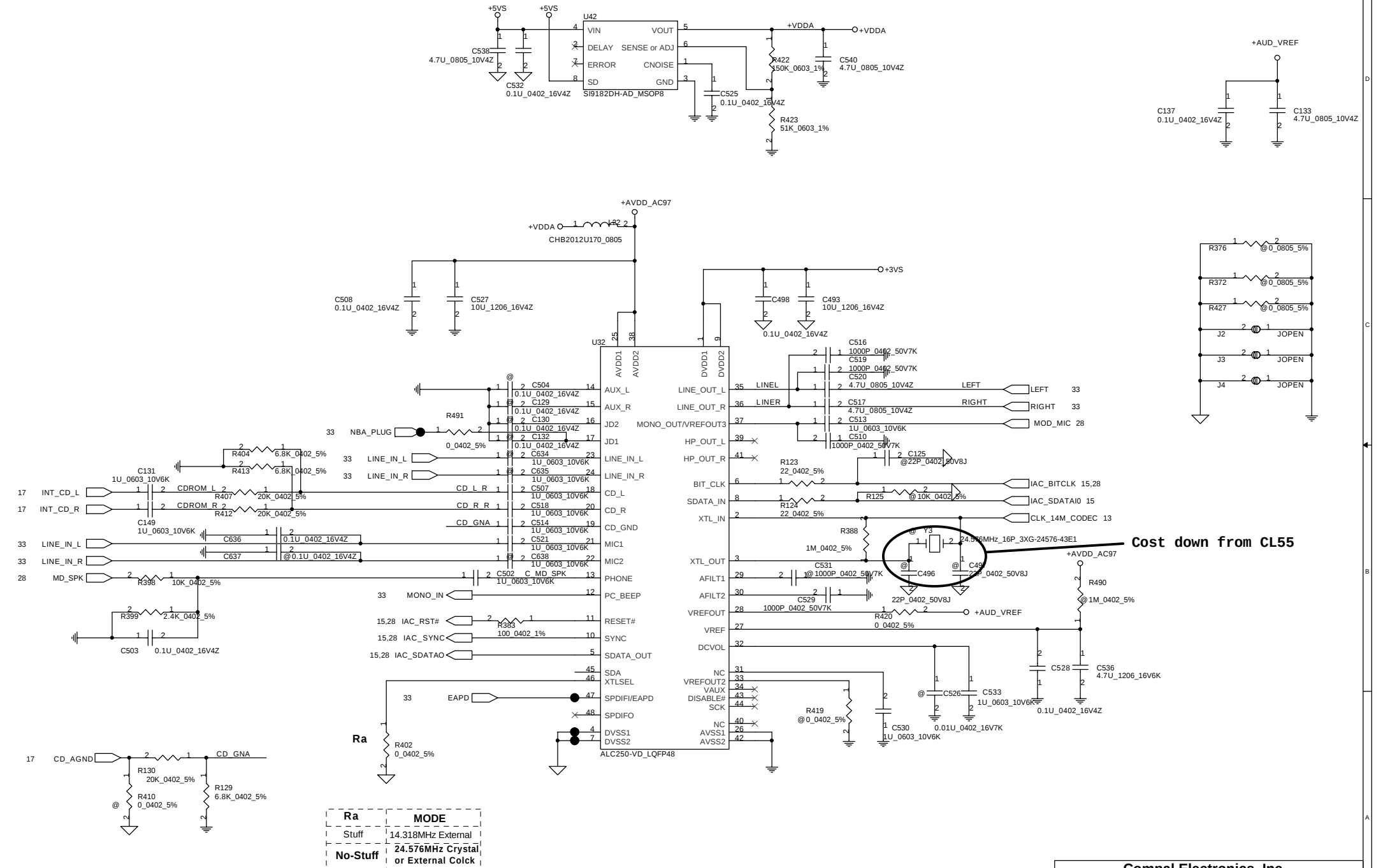


PARALLEL PORT





AC97 Codec



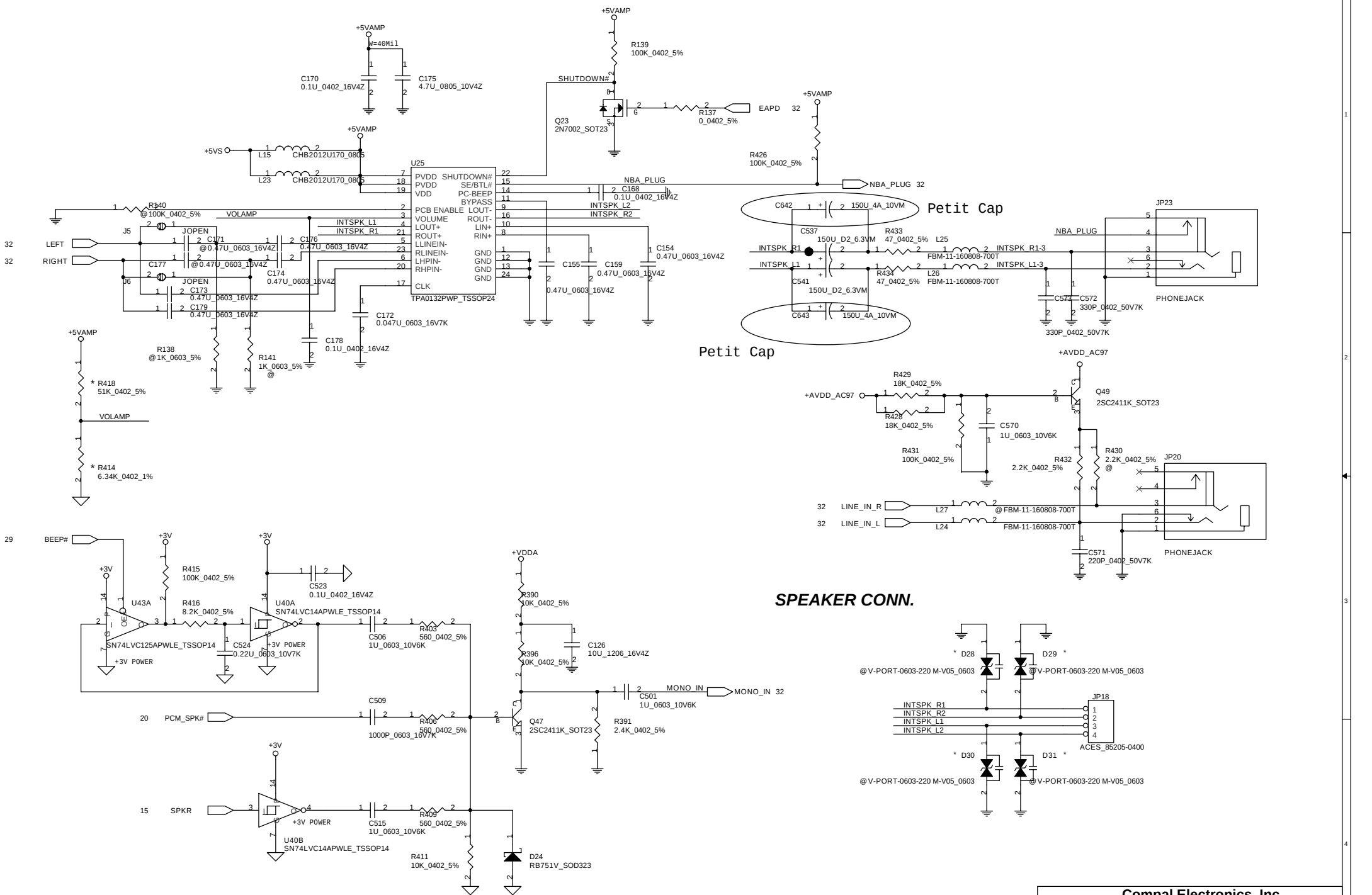
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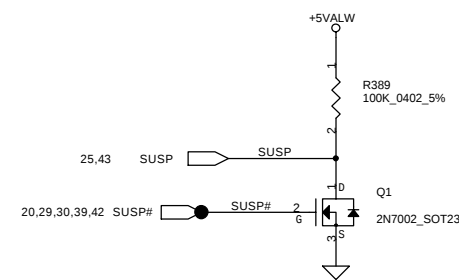
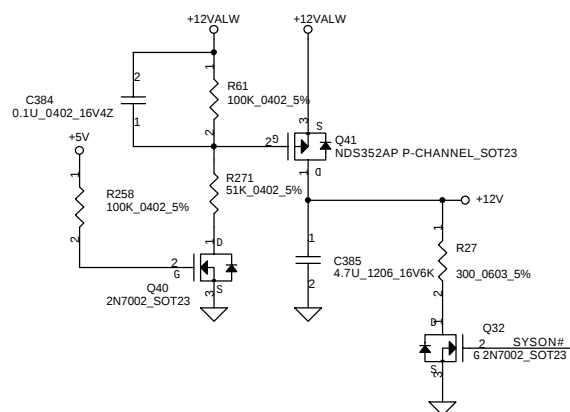
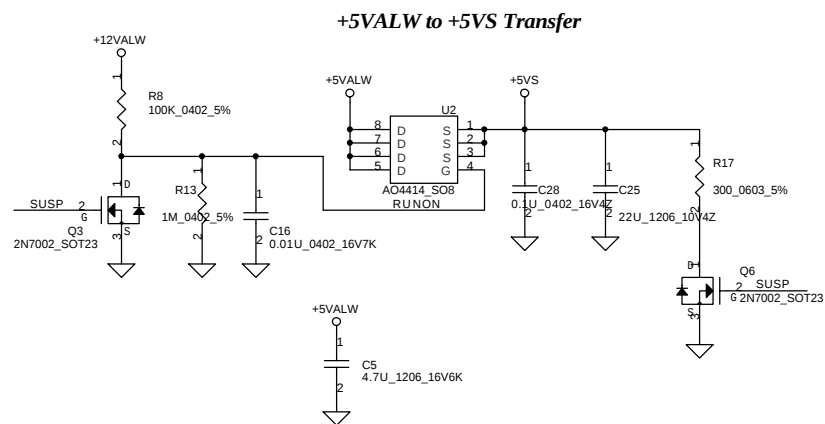
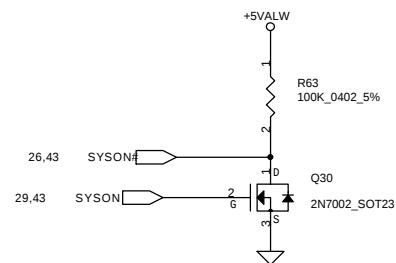
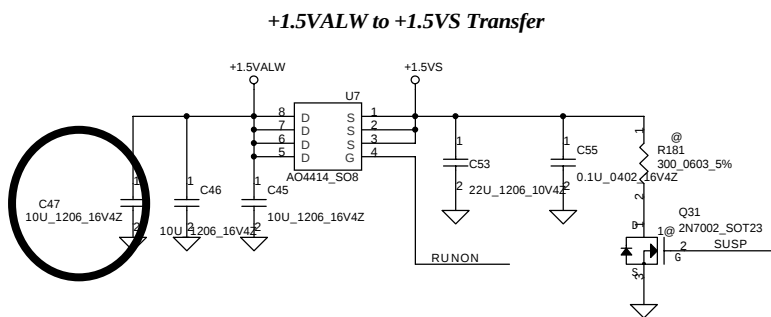
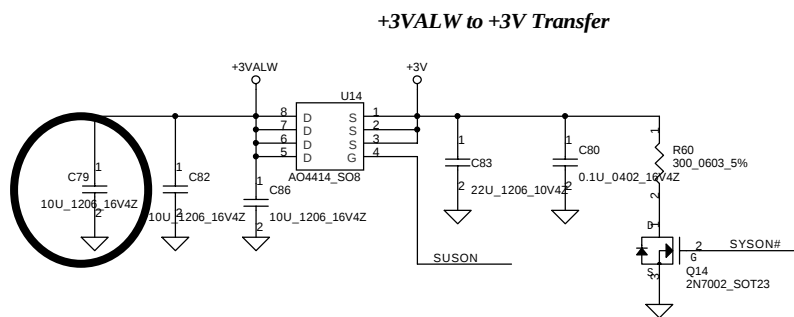
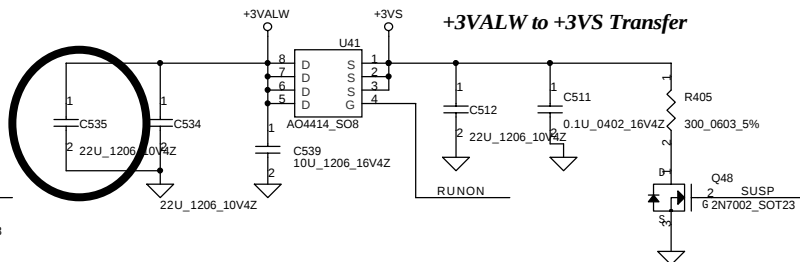
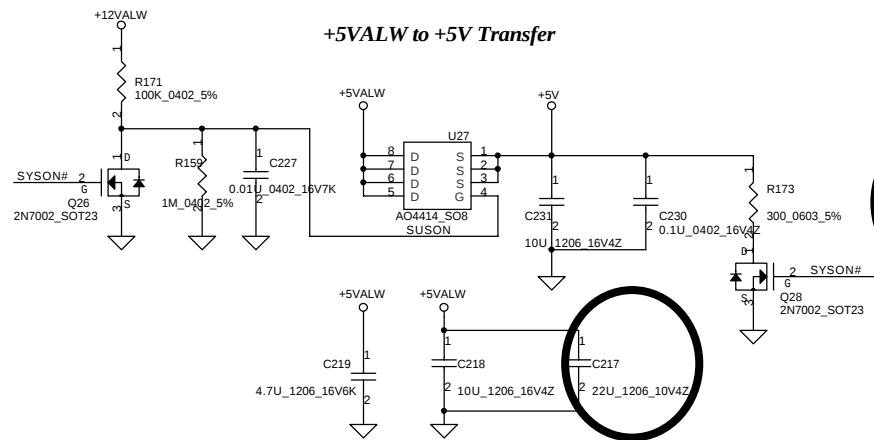
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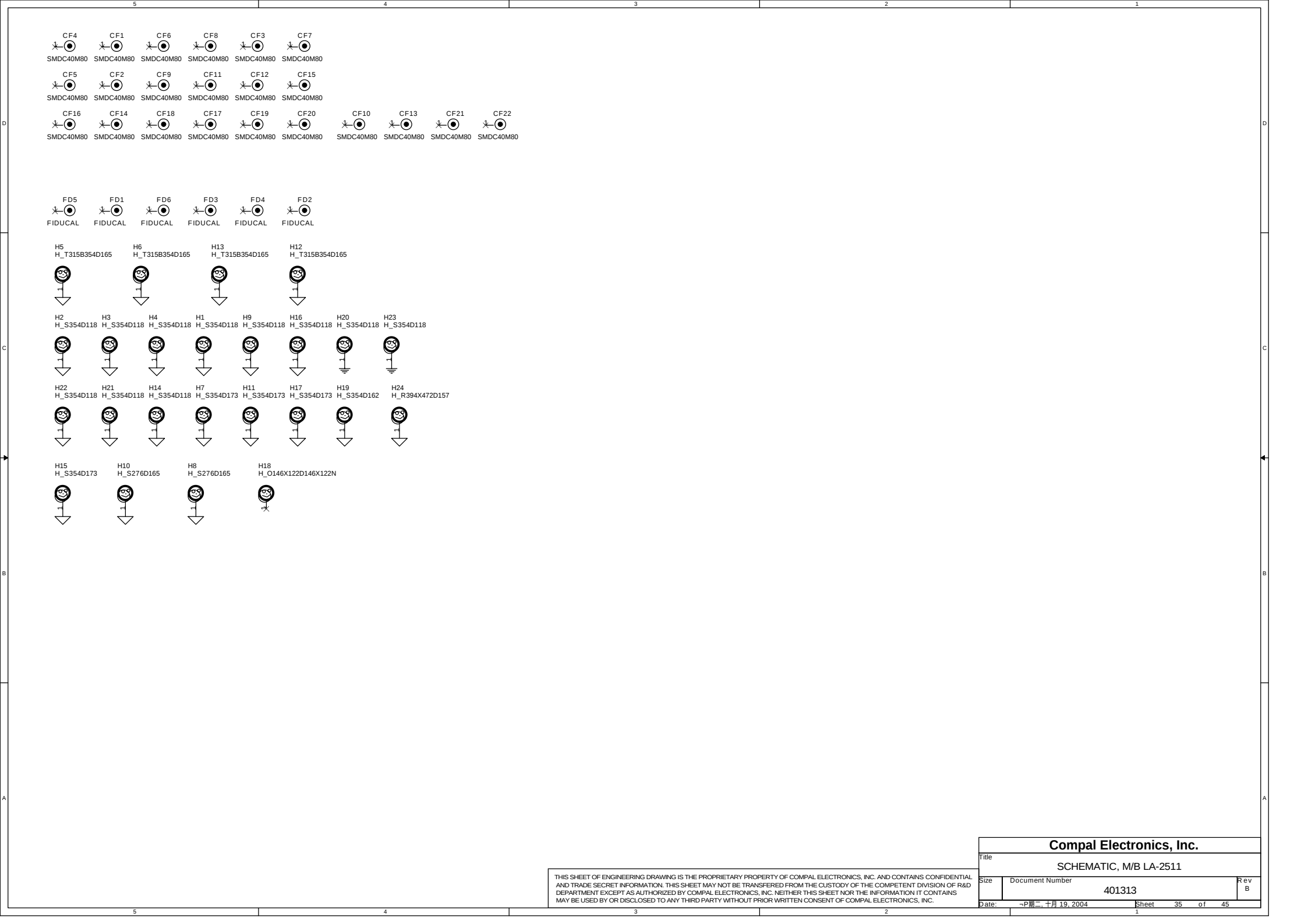
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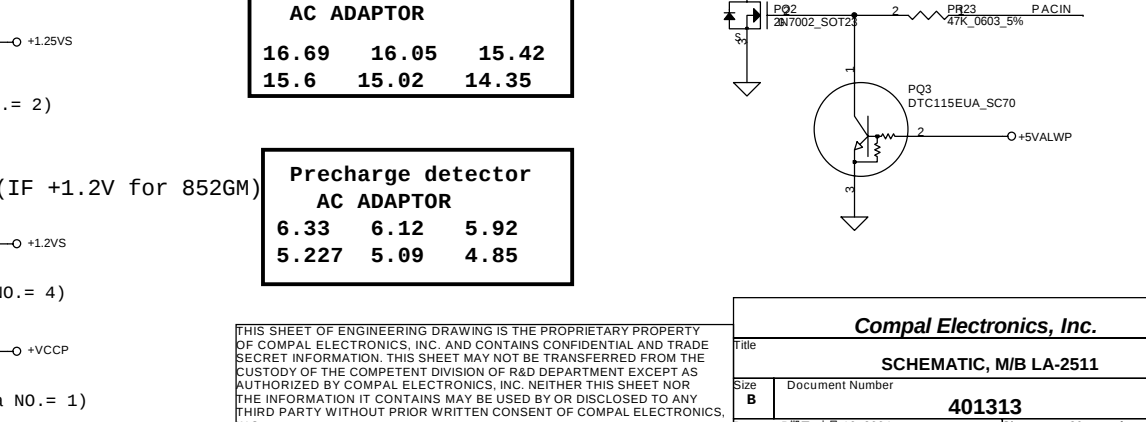
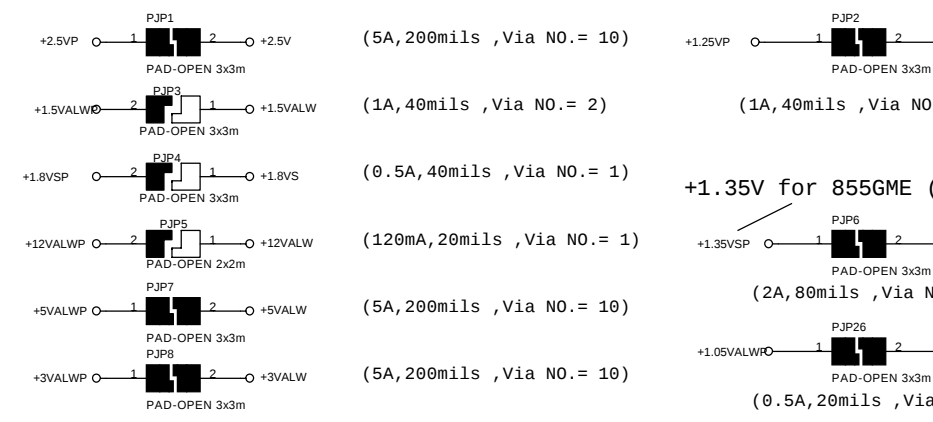
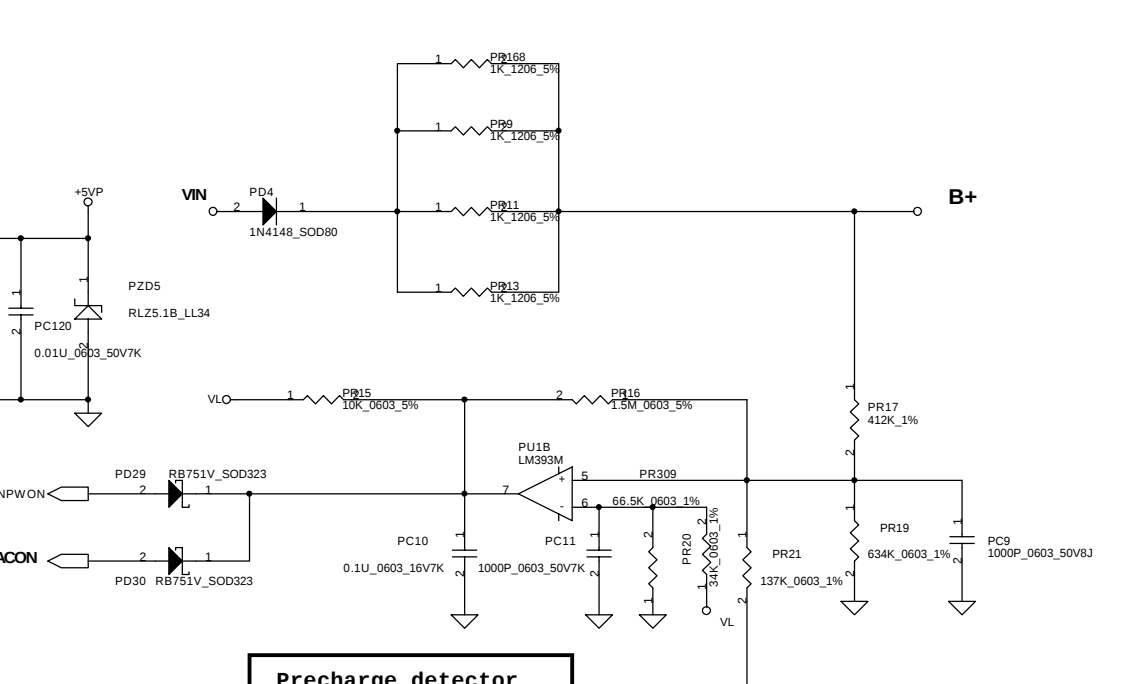
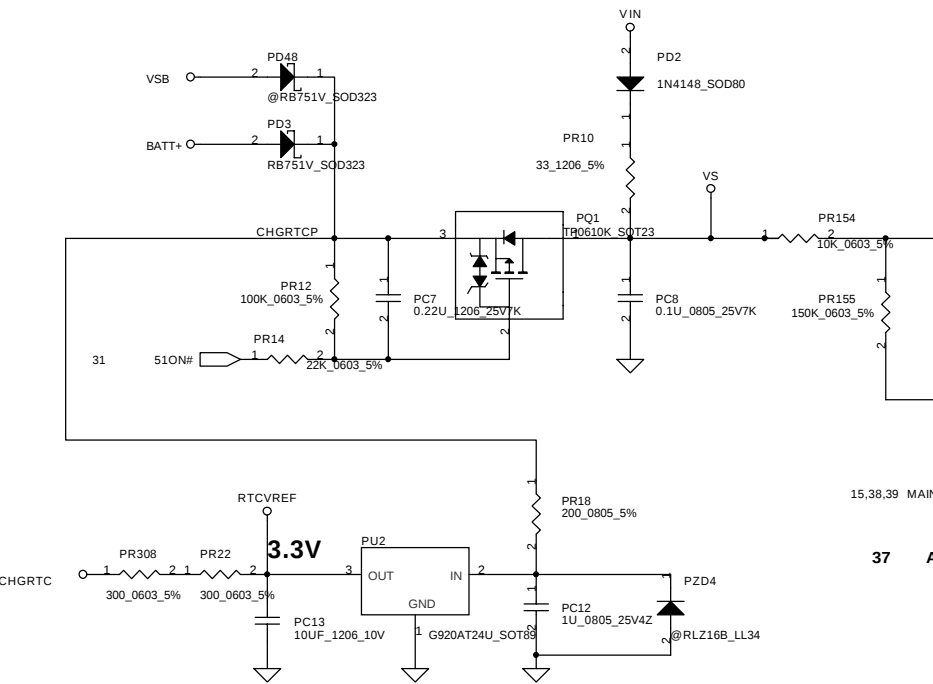
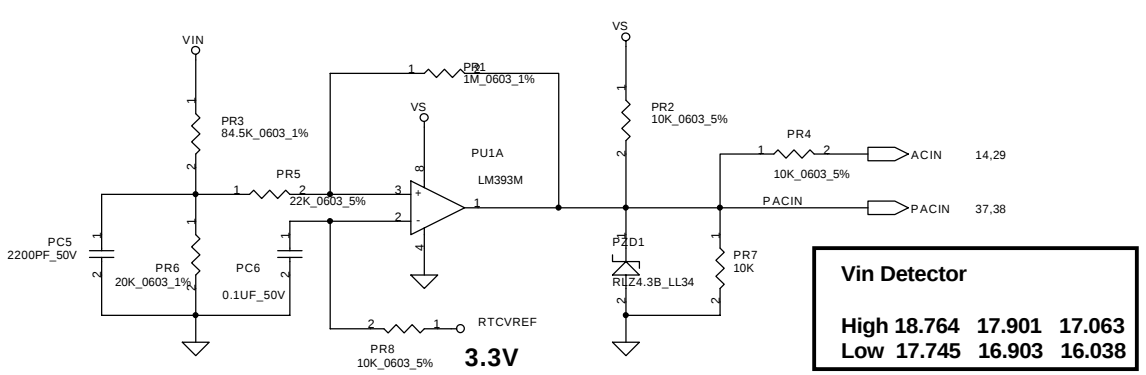
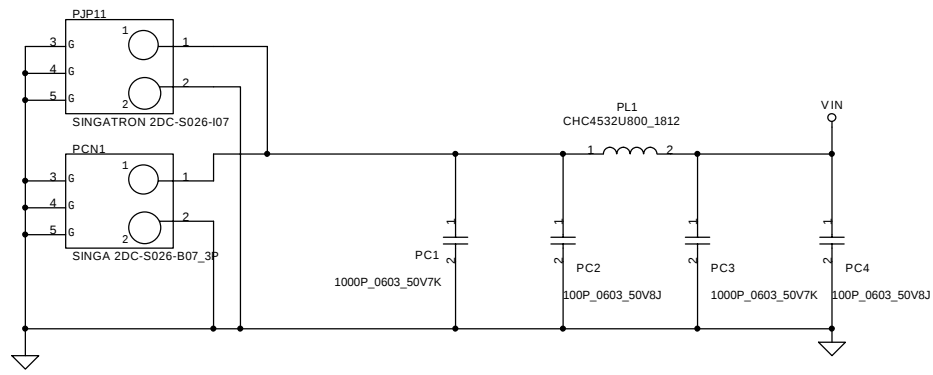
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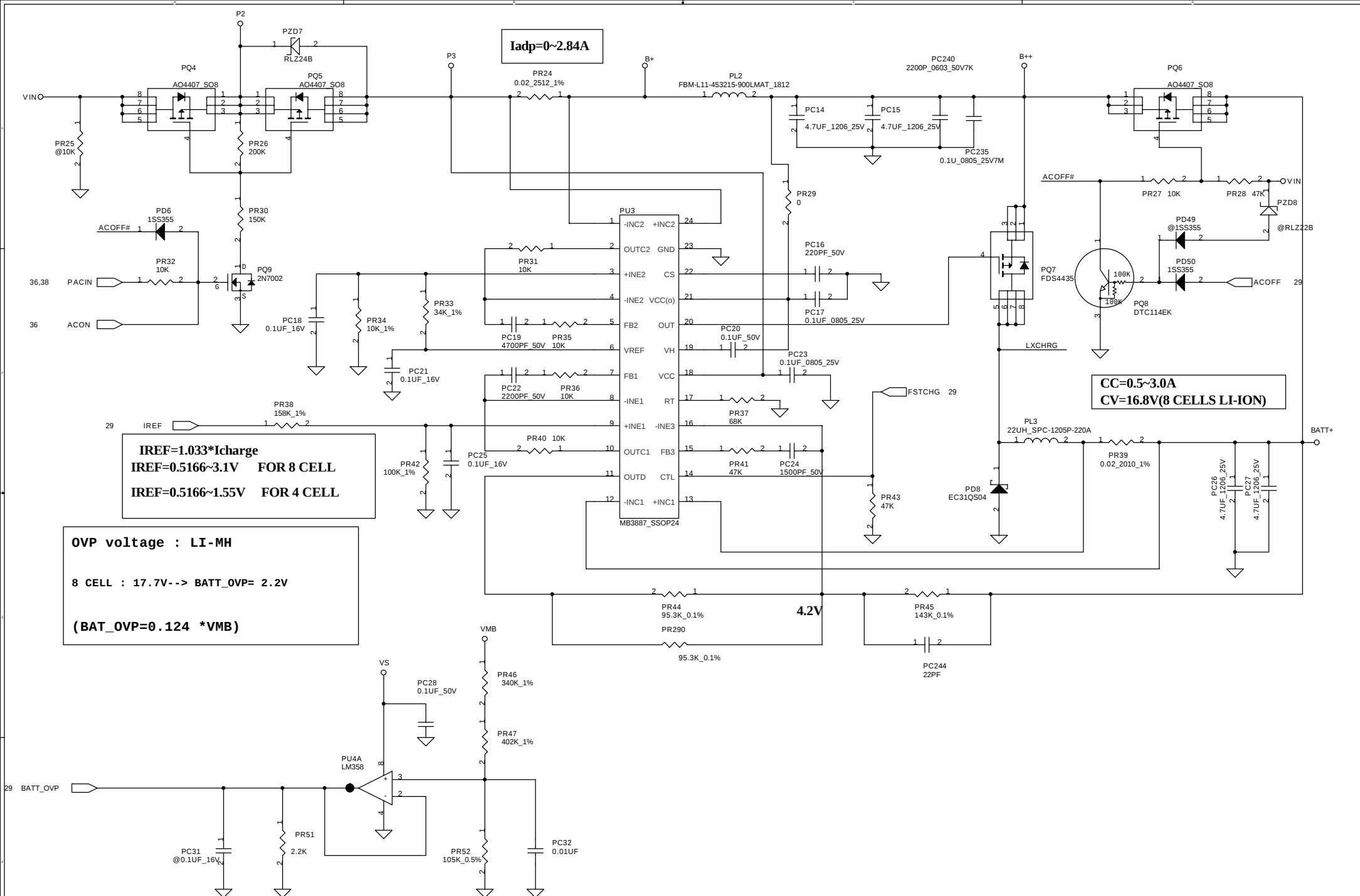


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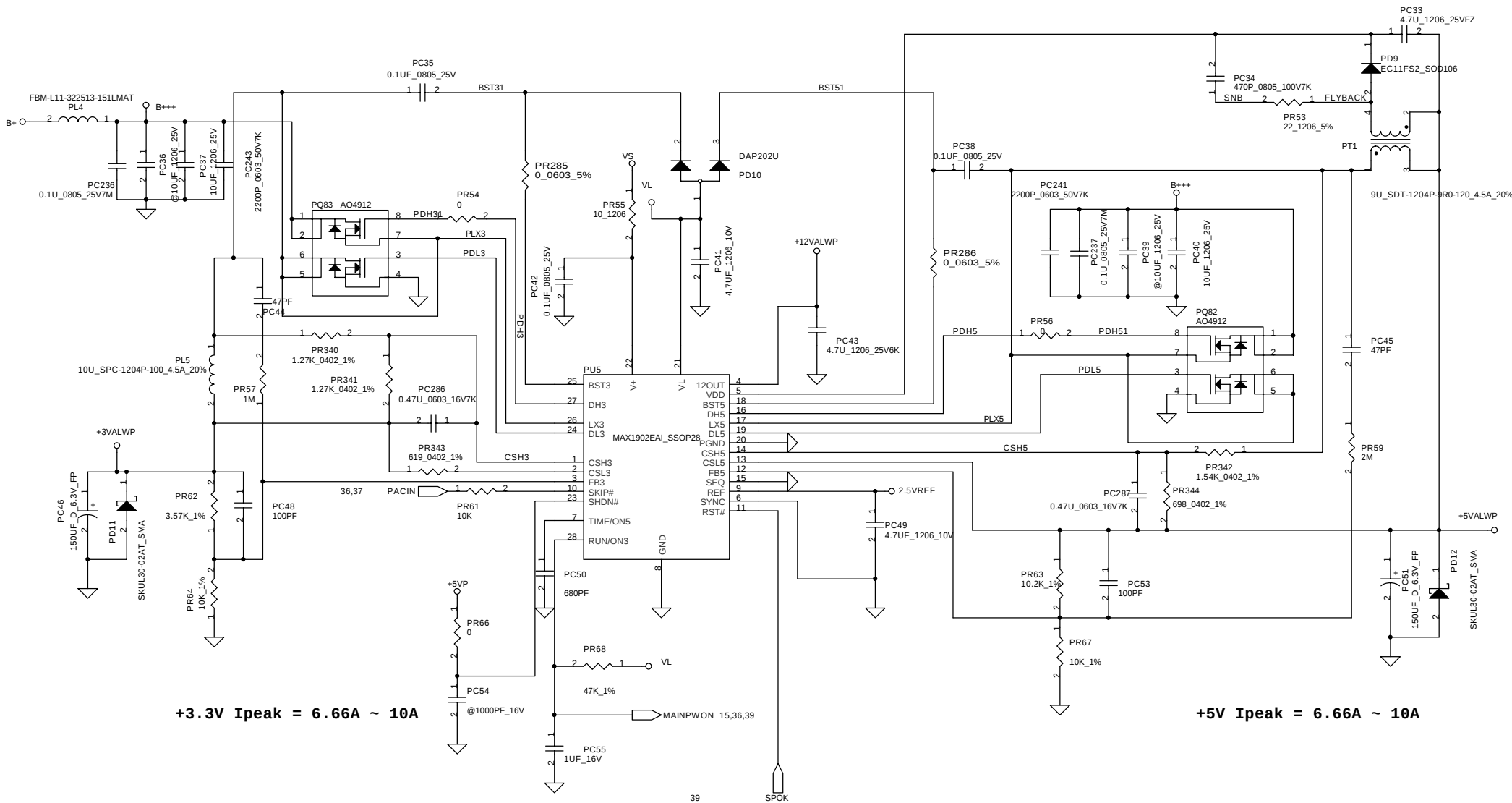


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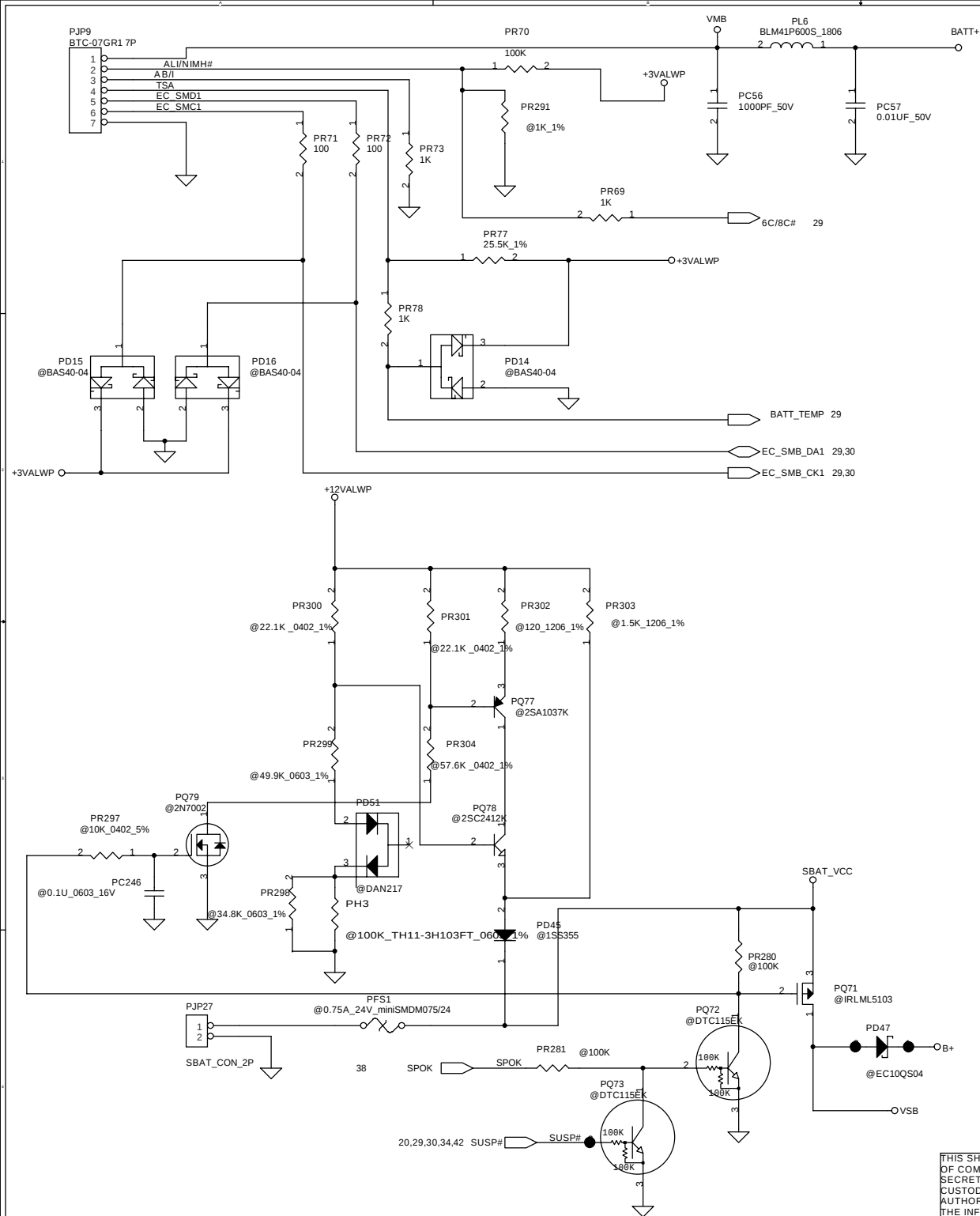
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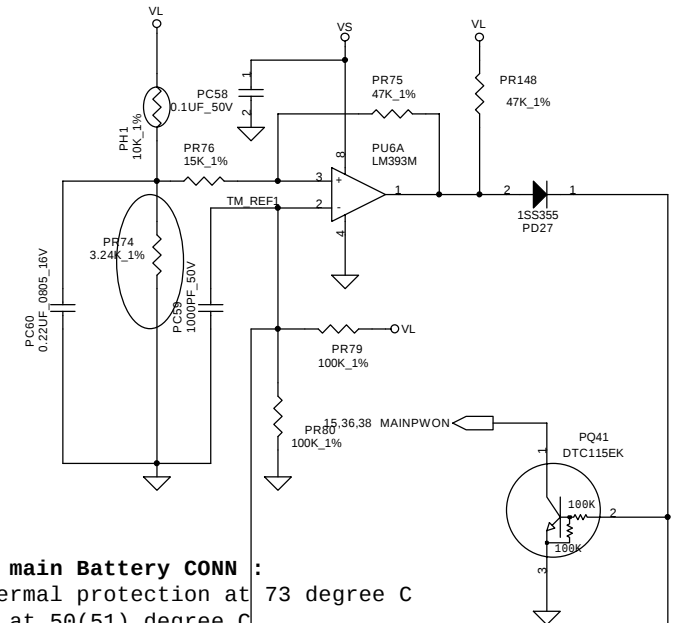


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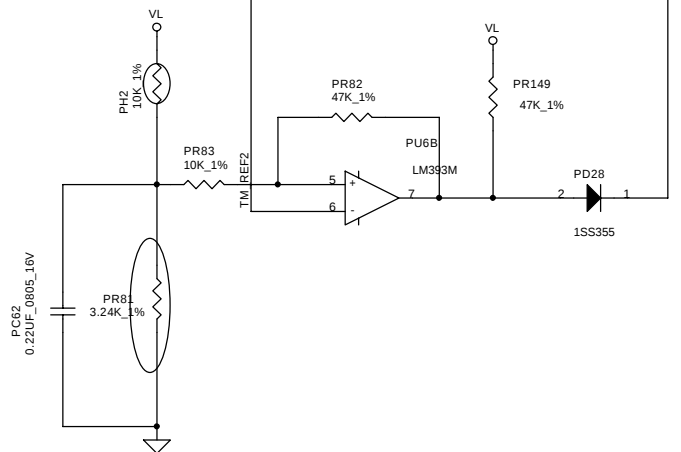
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PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C

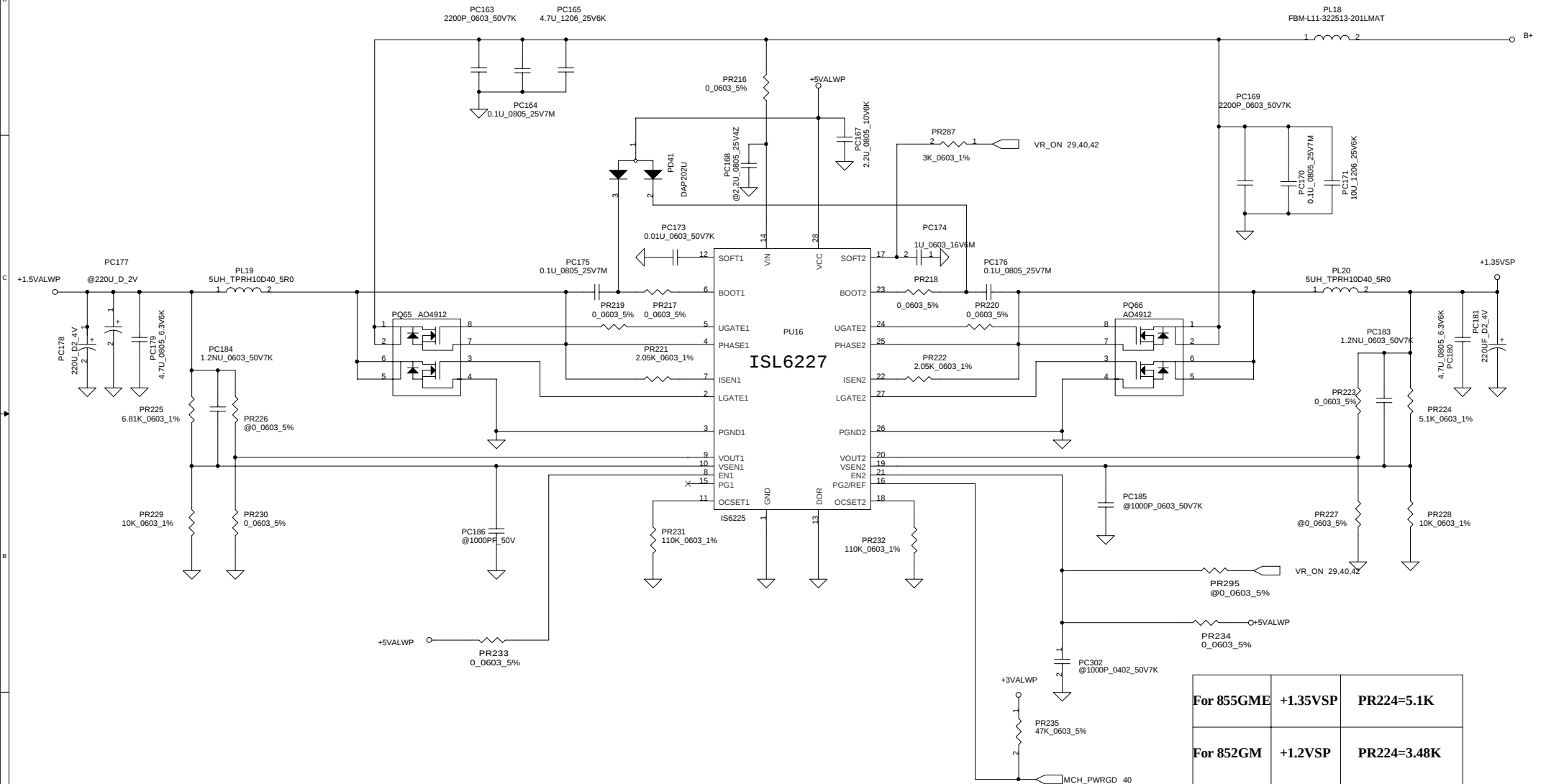


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+1.5VALWPV/+1.35VSP (GME)

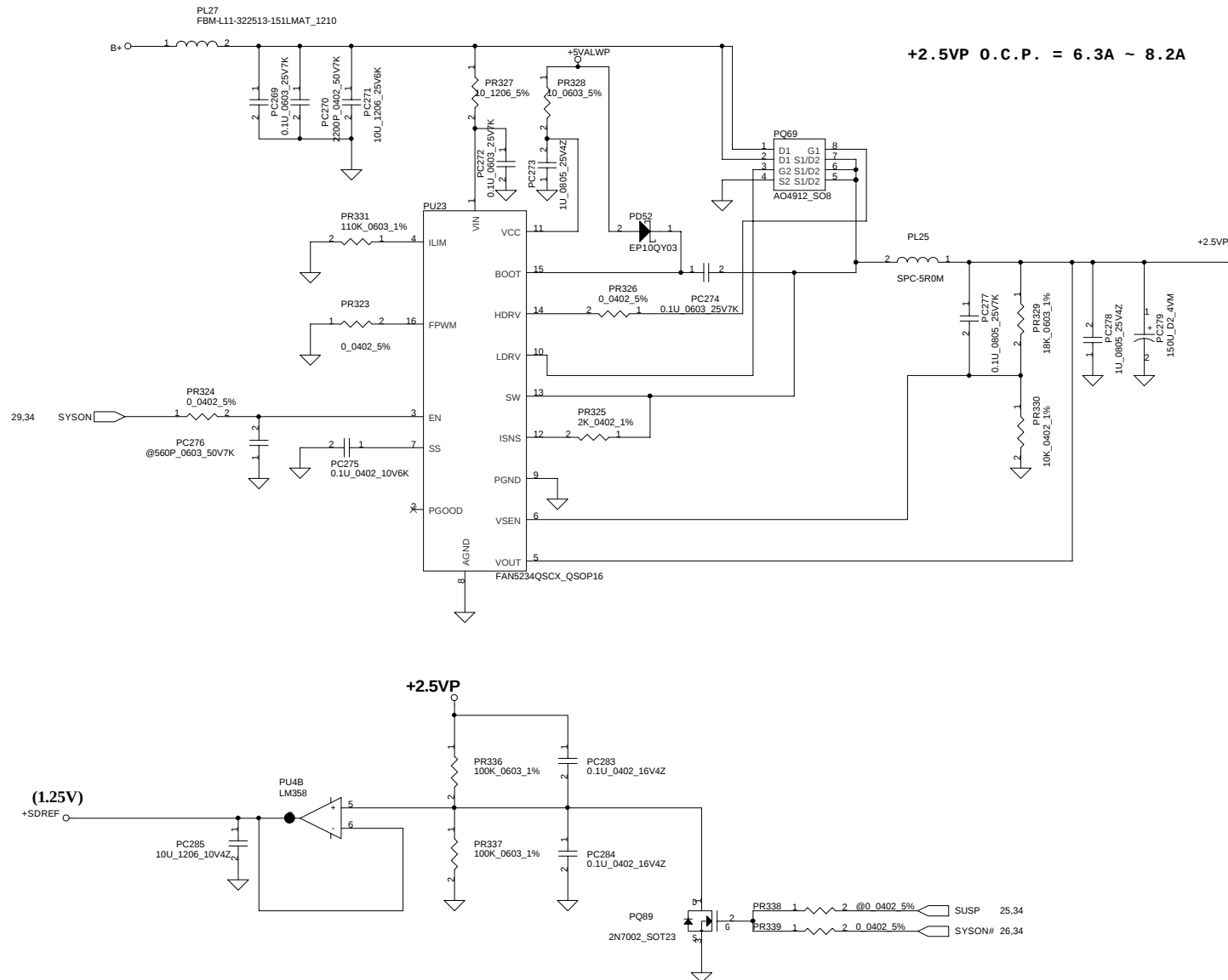
(IF +1.2V for 852GM)



For 855GME	+1.35VSP	PR224=5.1K
For 852GM	+1.2VSP	PR224=3.48K

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1		Modify 1.05VP voltage level		42	1. change PR314 to 402k		DVT
2		Change PU16(ISL6227) 135VSP power build from softstart build to enable build		41	1.delete PR287; change PC174 from 1u 0805 to 0.01u 0603;add PR295:0		DVT
3		To leave PC302 for 1.35VSP soft start time		41			DVT
4		Change PU16(ISL6227) 135VSP power build from enable build to softstart build due to the sequence		41	1.add PR287:1k ; change PC174 from 0.01u 0603 to 1u 0603;delete PR295:0;add PR234:0		DVT
5		change PU2 from S-81233SG(sot89) to G920AT24U(sot89)		36	1.delete PZD2;PZD4		PVT
6		MODIFY 1.35V RISE TIME			1CHANGE PR287 FROM 1K TO 3K		PVT
7		MODIFY 1.35V VOLTAGE LEVEL			1CHANGE PR224 FROM 3.48K TO 5.1K		PVT
8		CHANGE CPU CORE MOS			1.CHANGE PQ52/PQ56 from IR7811A to AO4408; CHANGE PQ54/PQ58 from SI4362 to AO4410;CHANGE PR349/PR370 FROM 0 TO 2.2		PVT
9		PQ1 MOS PHASE OUT			1CHANGE PQ1 FROM TP0610T TO TP0610K		PVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1	Delete R45,R47	EMI cost down	0.2	28			
2	Add R505,C627	Improve signal quality					
3							
4							
5							
6							
7							
8							
9							

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