

EAT20 (Sakhir 10GC)

LA-2492 Schematics Document

Intel Dothan / AlvisoPM / DDR-1 / ICH6-M / Select Bay

(nVIDIA NV43M & NV44M/ ATi M22 & M24)

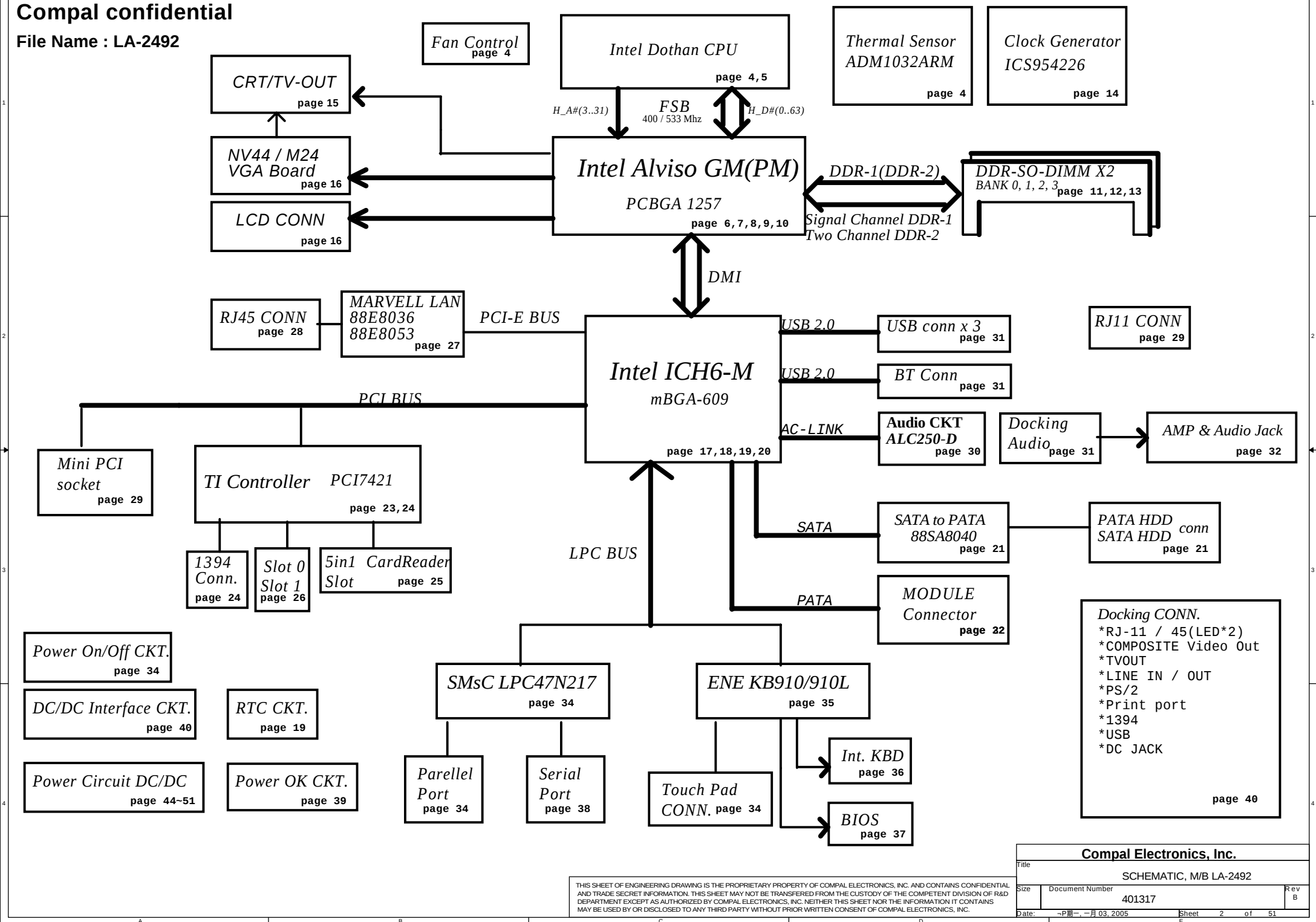
2004 / 12 / 22

Rev:1.0

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Title		
SCHEMATIC, M/B LA-2492		
Size	Document Number	Rev
	401317	B
Date:	~P圖一, 一月 03, 2005	Sheet 1 of 51
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File Name : LA-2492



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for Direct CD	ON	OFF	OFF
+5VMOD	5V switched power rail for Module Bay	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
1394	AD20	2	PIRQA/PIRQB
SD	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

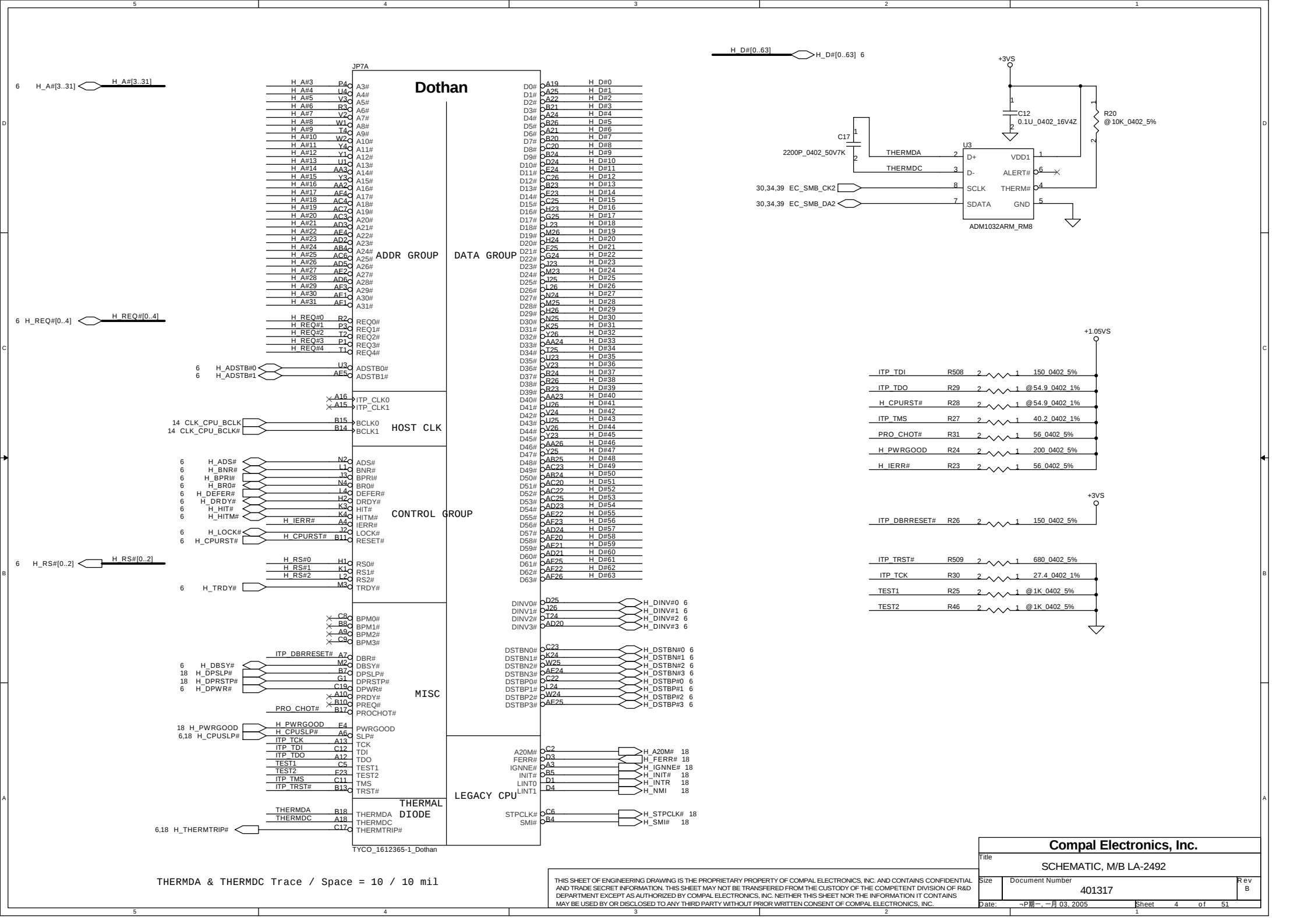
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1	NC
2	0.2
3	1.0
4	
5	
6	
7	

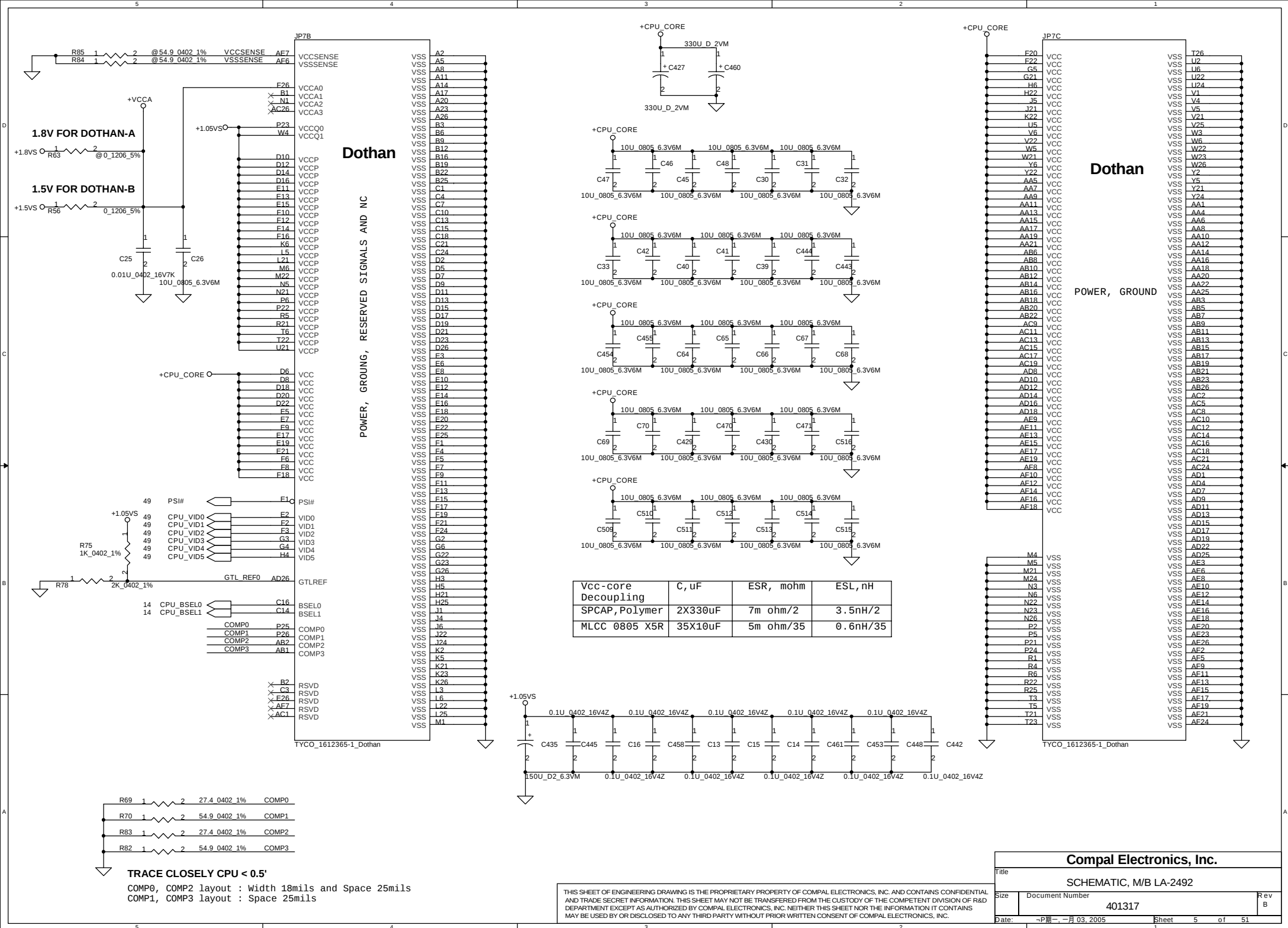
SKU ID Table

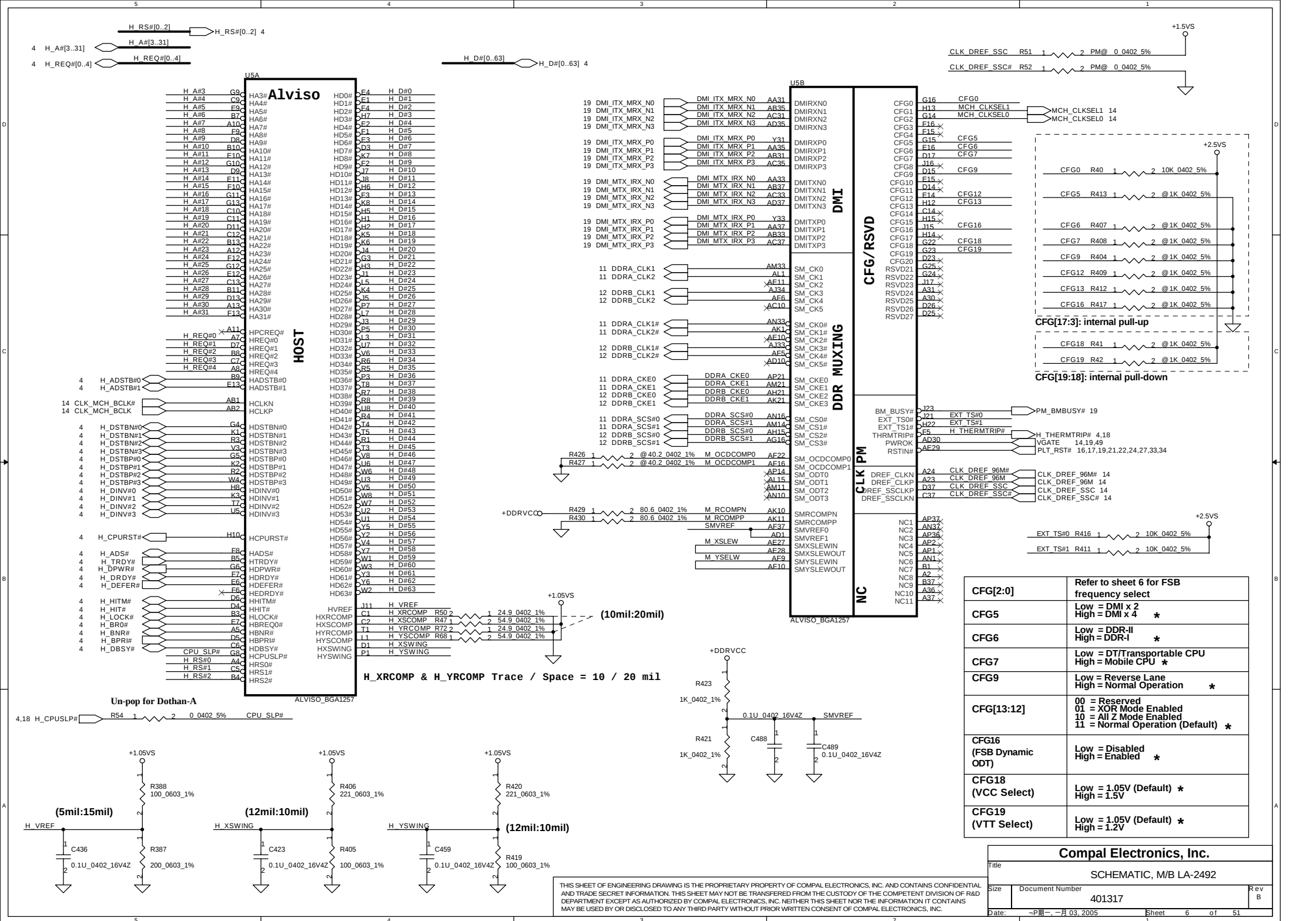
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		1-Button	3-Buttons	7-Buttons
0	10	1		0
1	10C	3	12	2
2	10G	5		4
3	10GC	7	13	6
4	10J	11		10
5				
6				

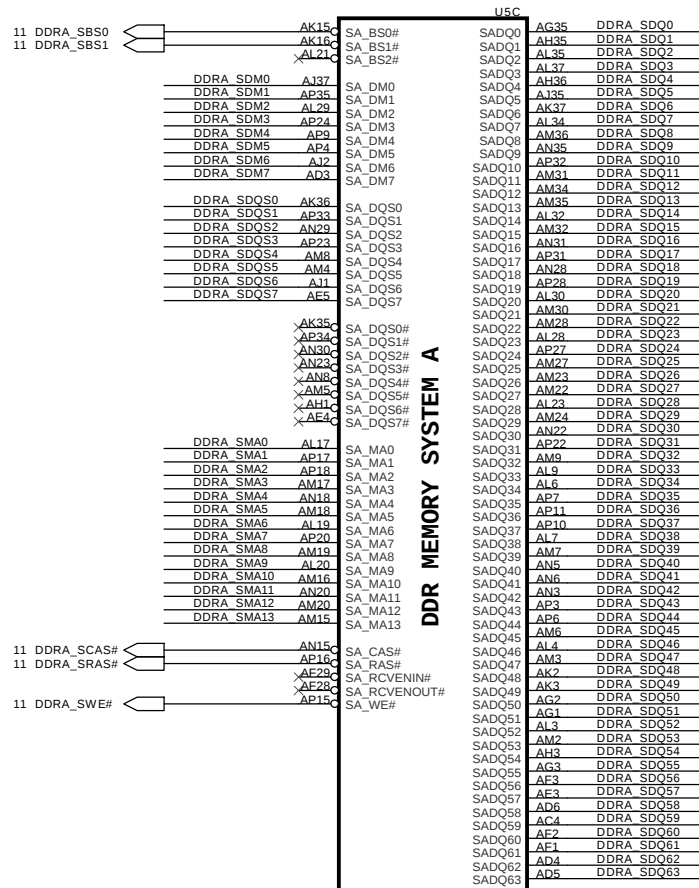
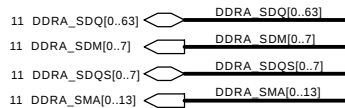
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Size	Document Number		Rev B
	401317		
Date:	~P開一, 一月 03, 2005		Sheet 3 of 51

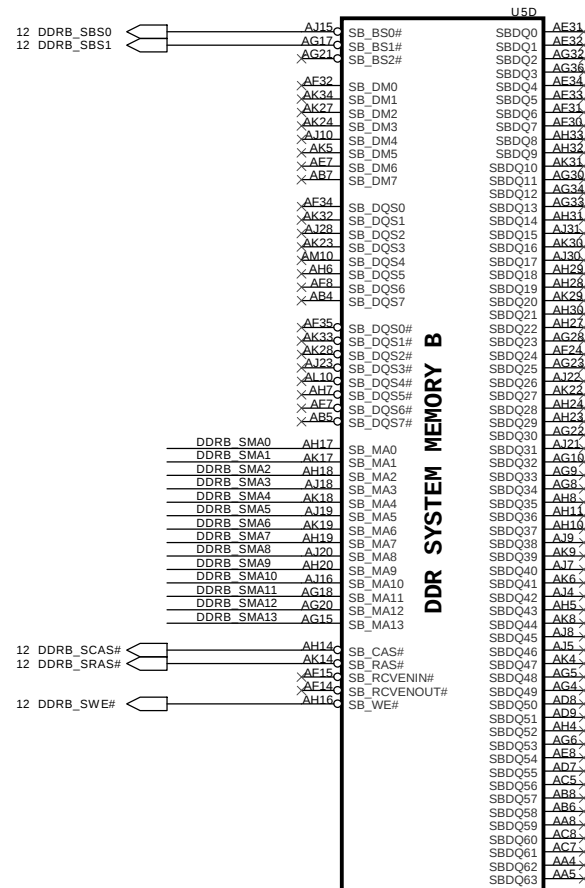








ALVISO_BGA1257



ALVISO_BGA1257

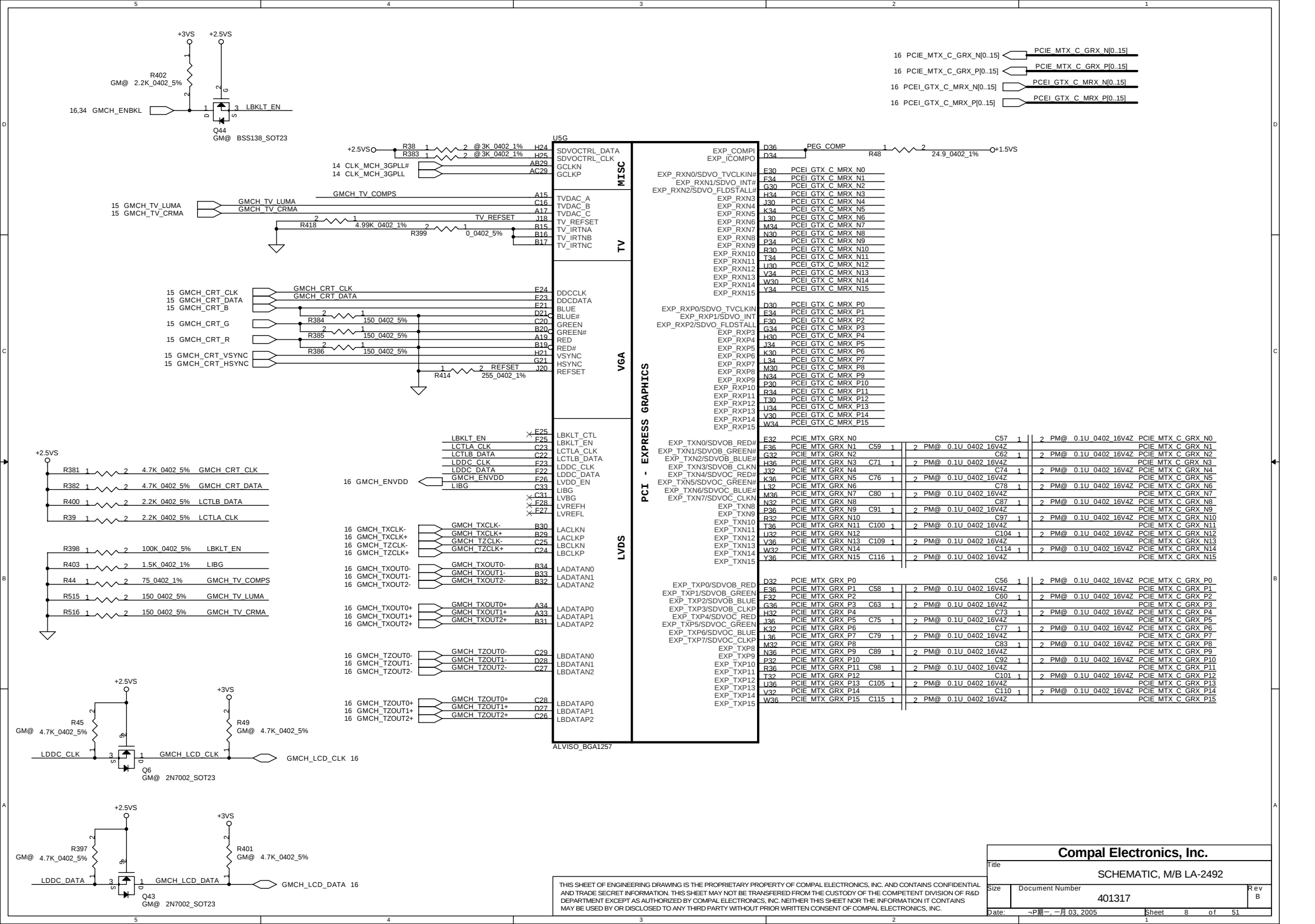
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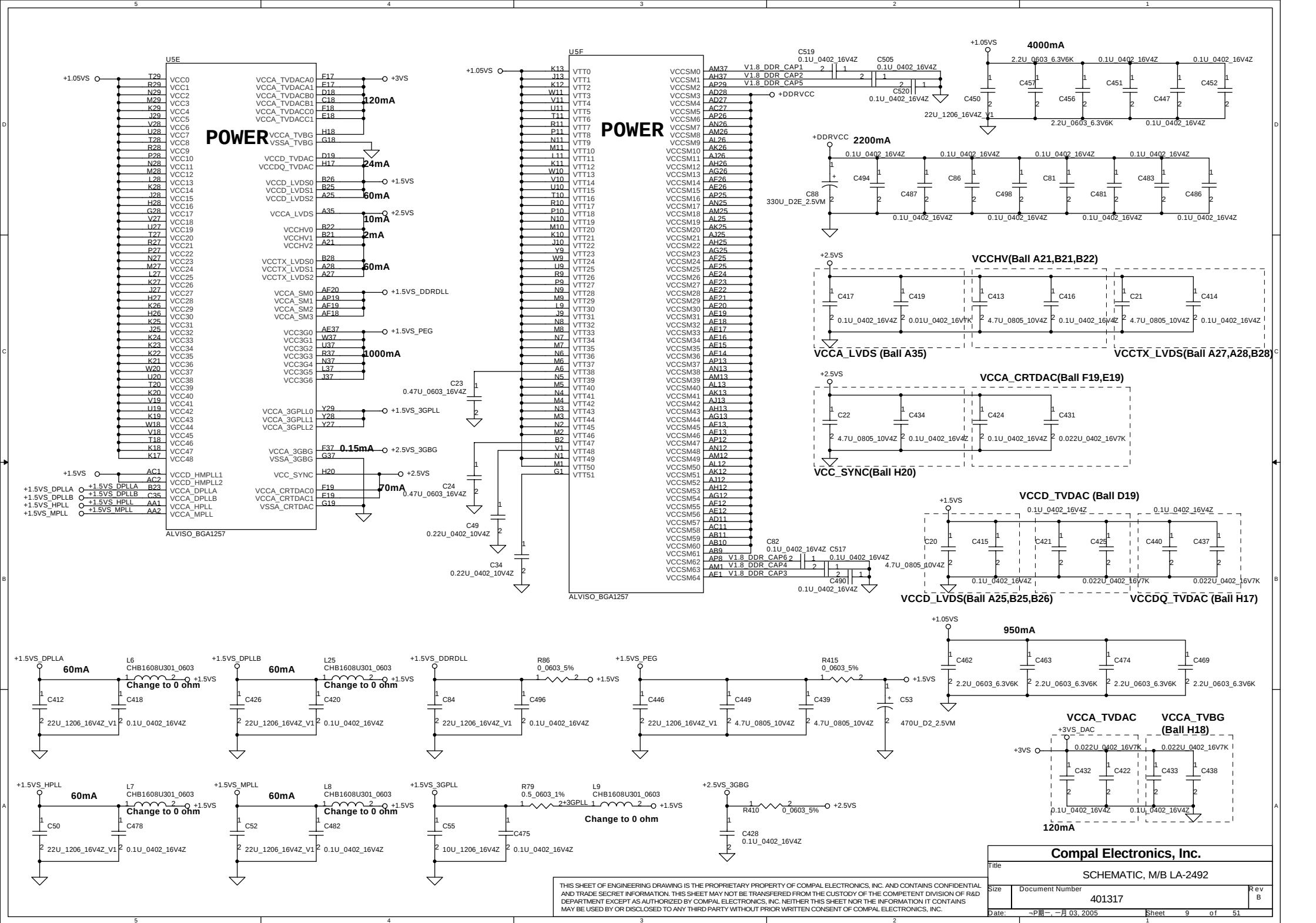
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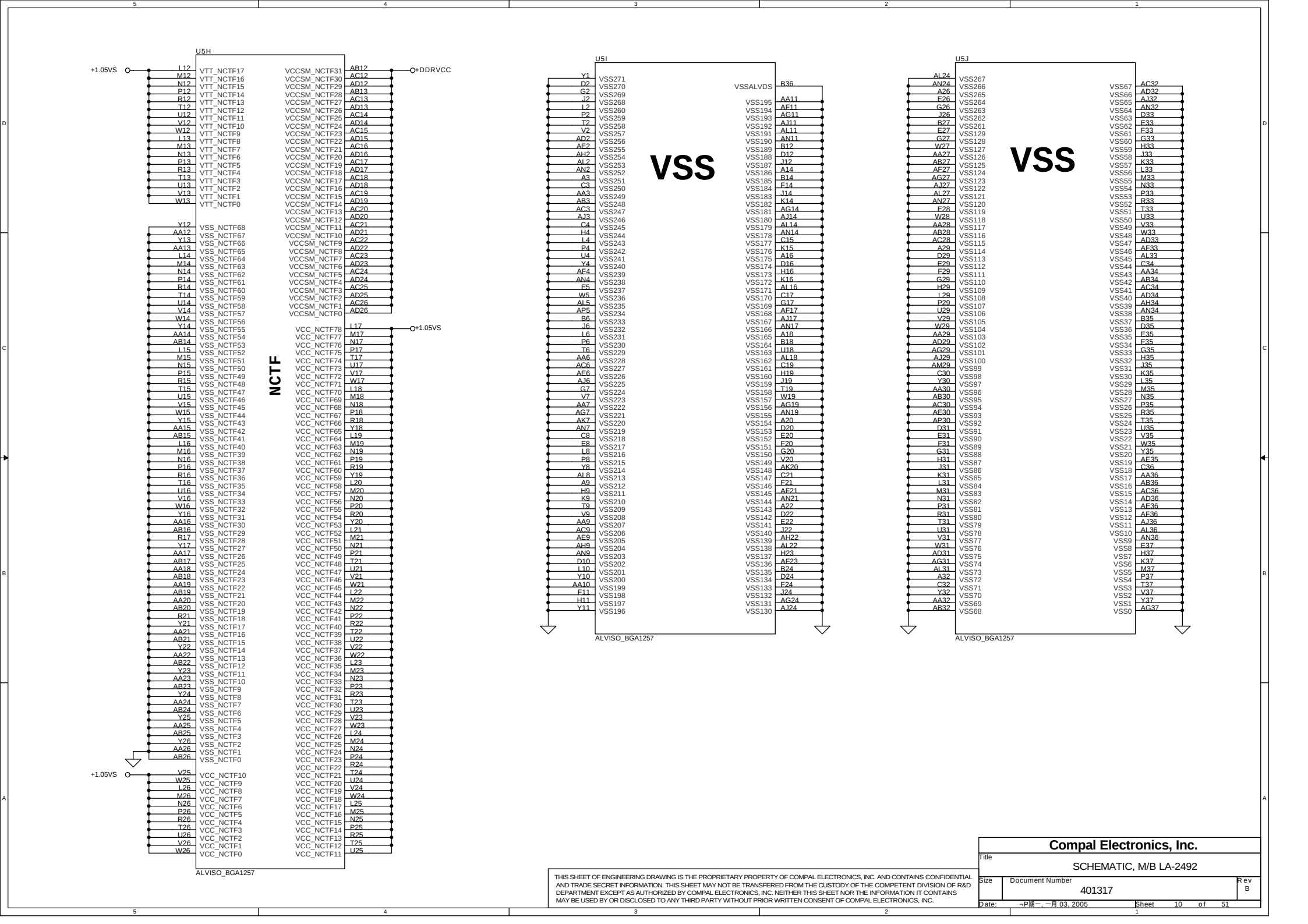
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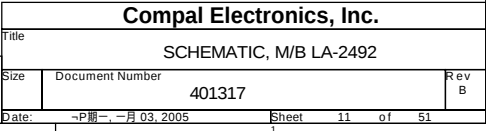
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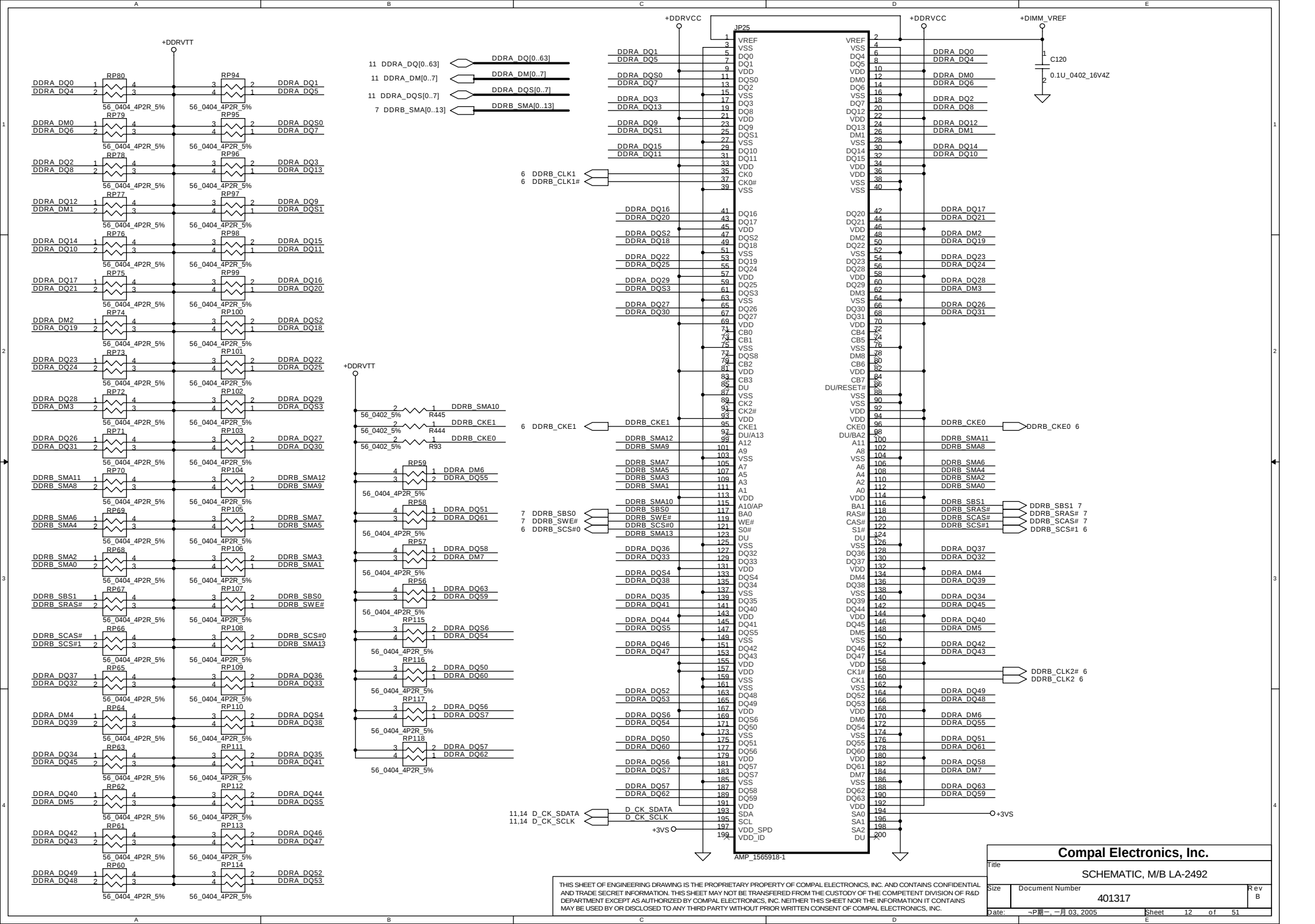
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Size	Document Number		401317	Rev B
Date:	~P 期一, 一月 03, 2005		Sheet 7 of 51	



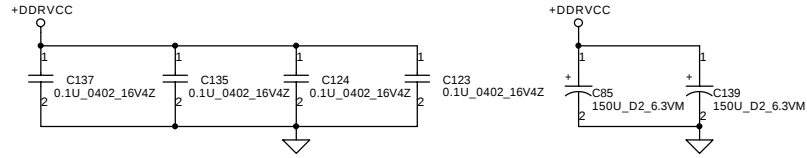
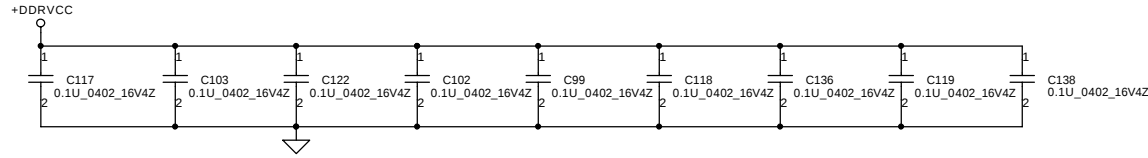




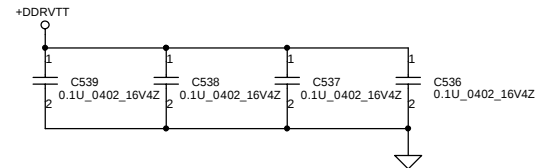
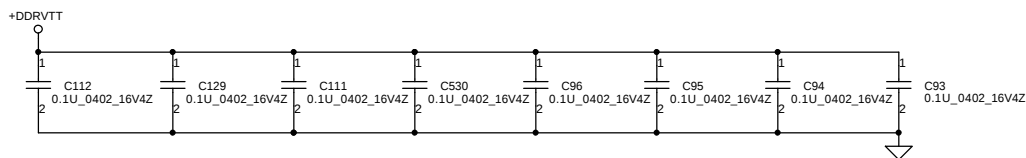
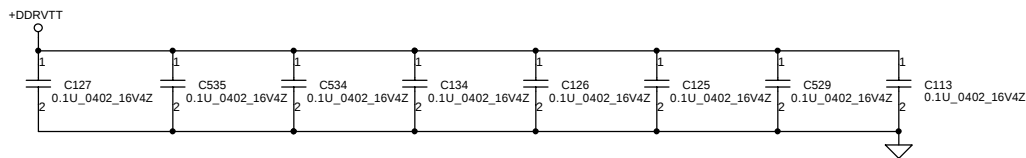
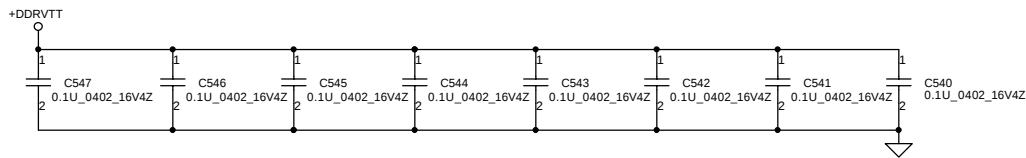
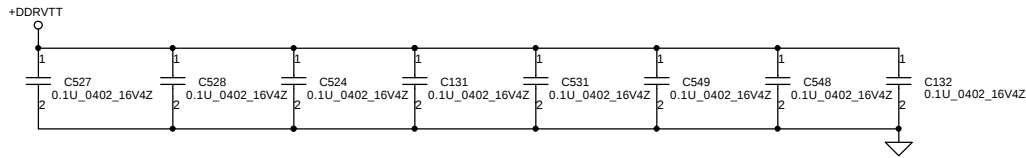
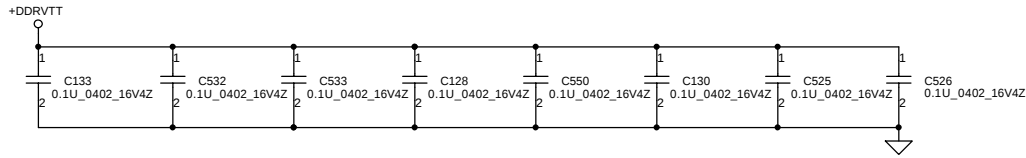




Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



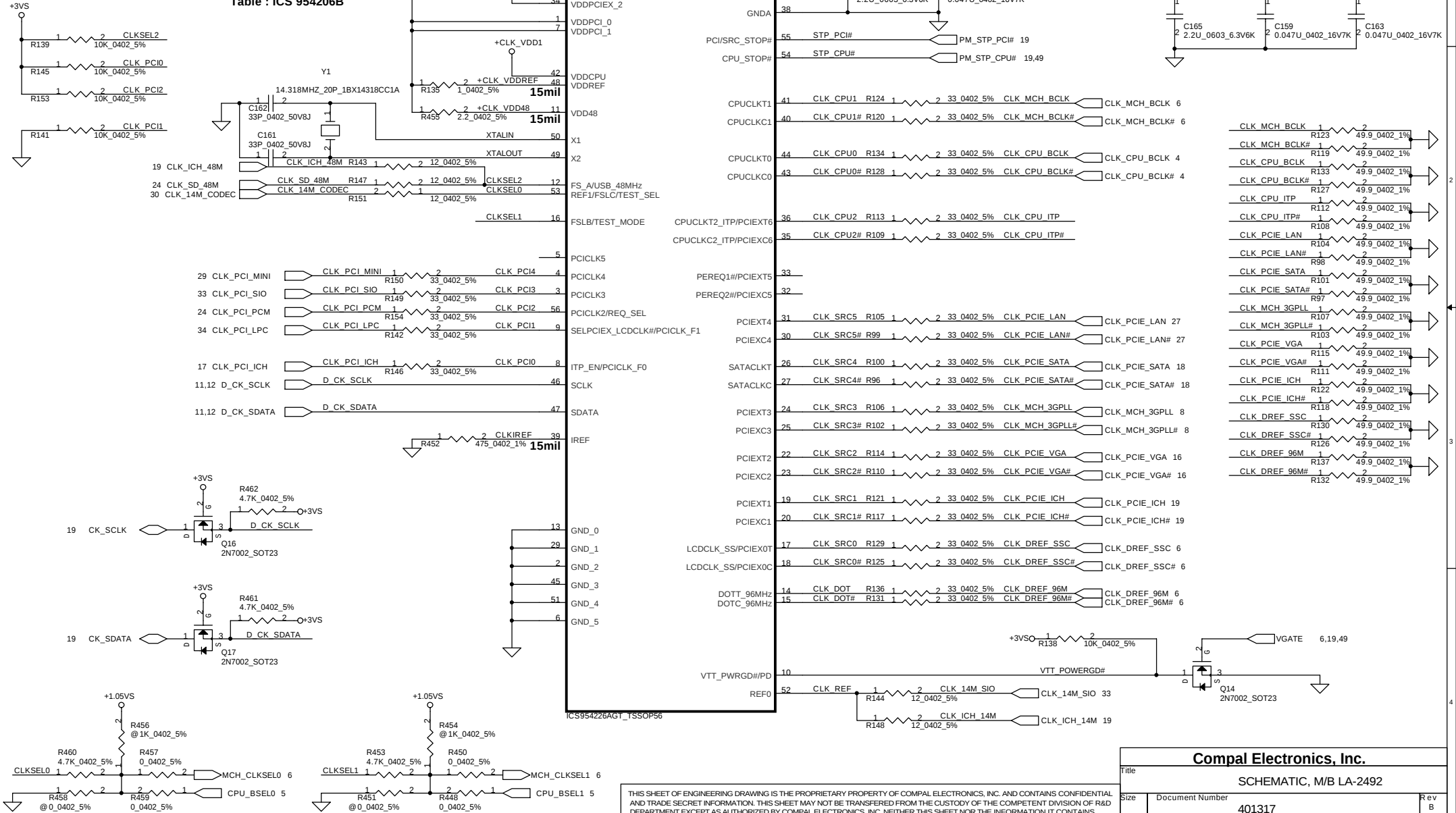
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Title			SCHEMATIC, M/B LA-2492
Size	Document Number		401317
Date	~P 周一, 一月 03, 2005		Sheet 13 of 51
		Rev	B

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

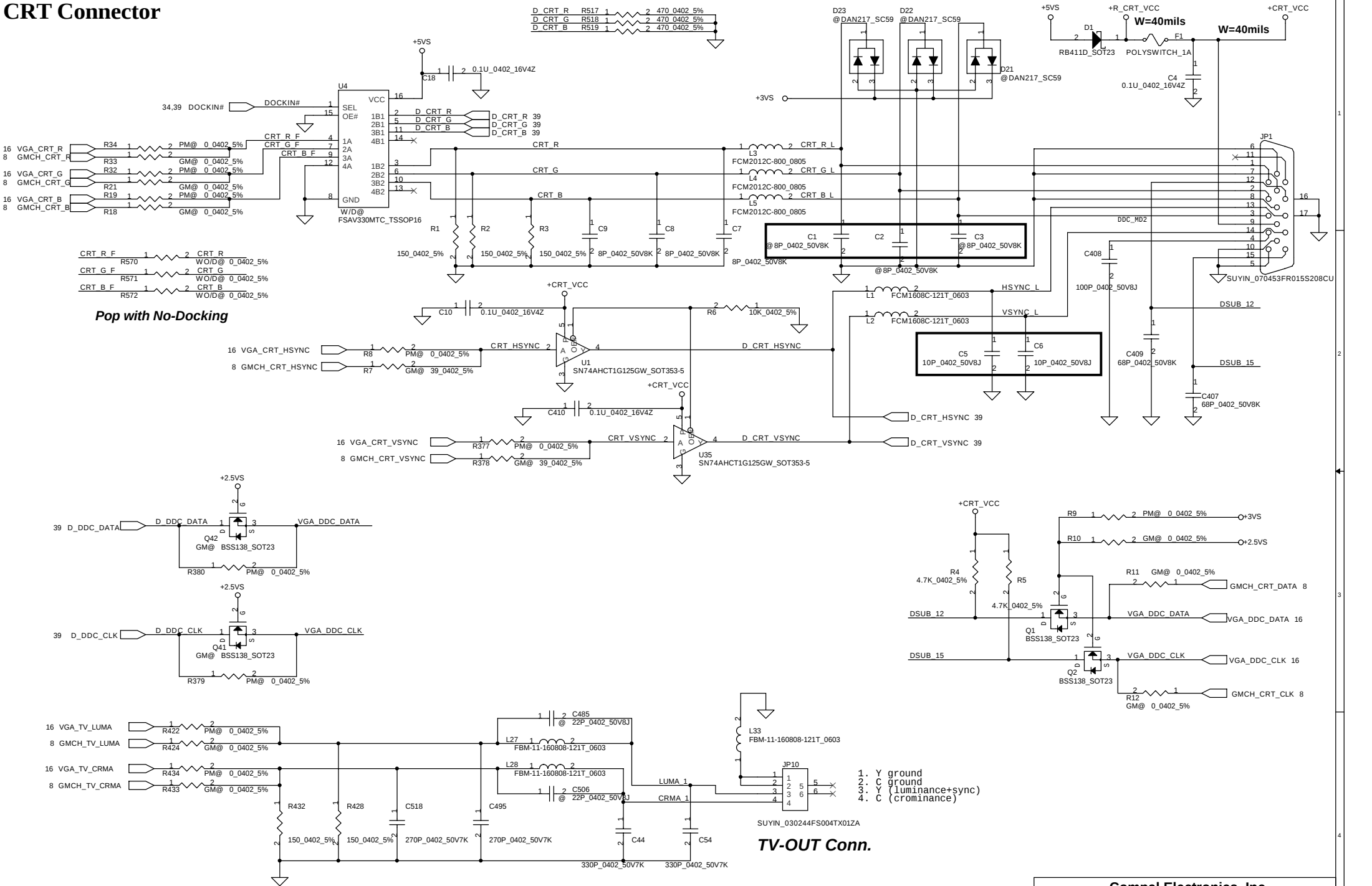
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Title		
SCHEMATIC, M/B LA-2492		
Size	Document Number	Rev
	401317	B
Date:	~月03, 2005	Sheet 14 of 51

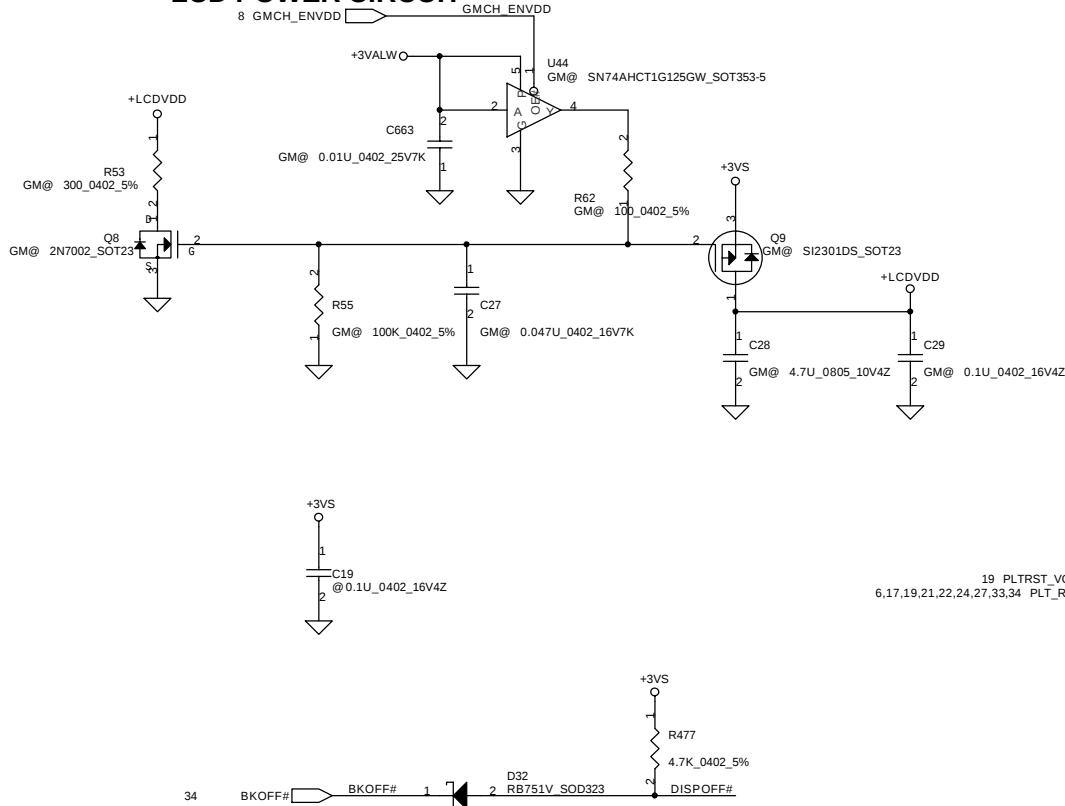
CRT Connector



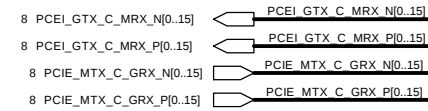
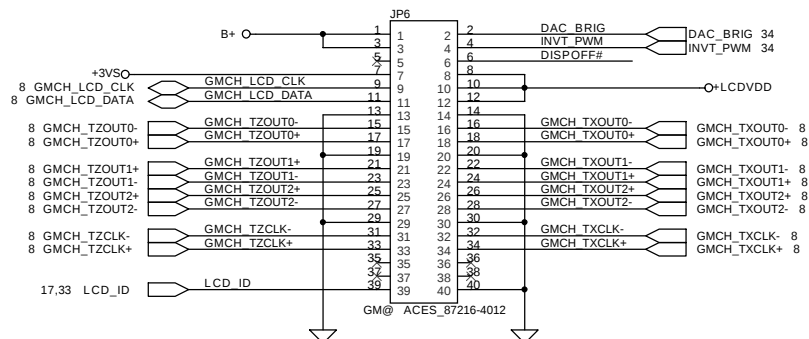
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Size	Document Number	Rev B
401317		
Date:	~P 十一月 03, 2005	Sheet 15 of 51

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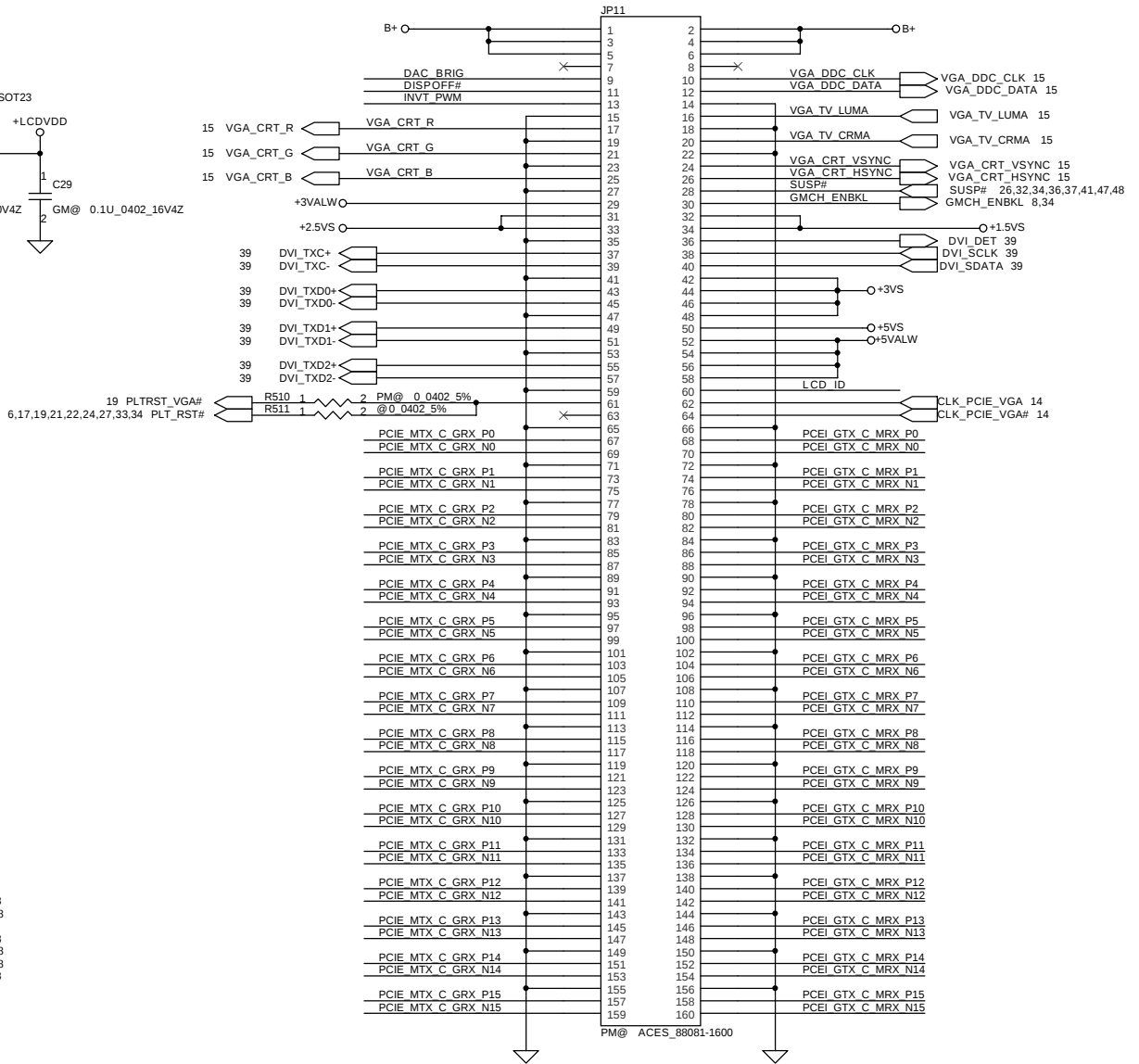
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



VGA BOARD Conn.



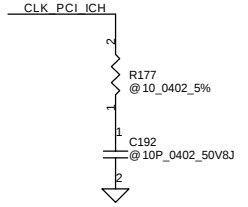
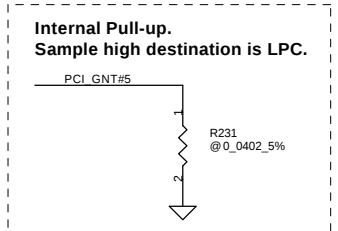
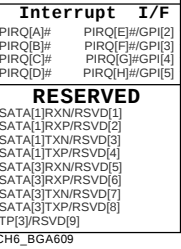
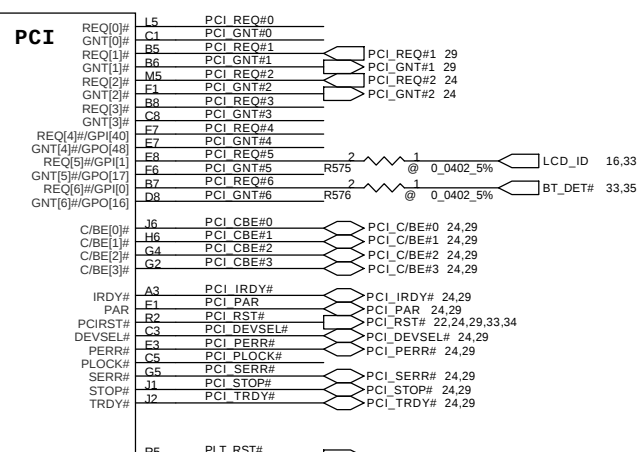
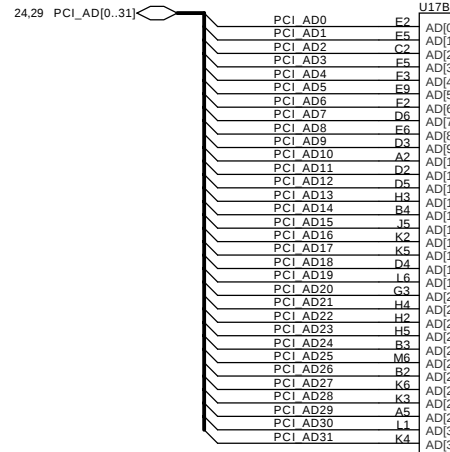
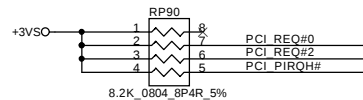
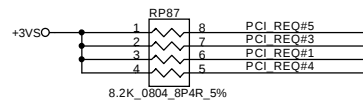
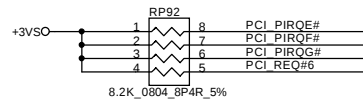
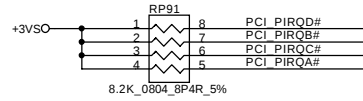
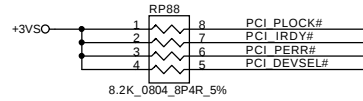
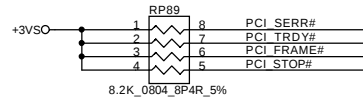
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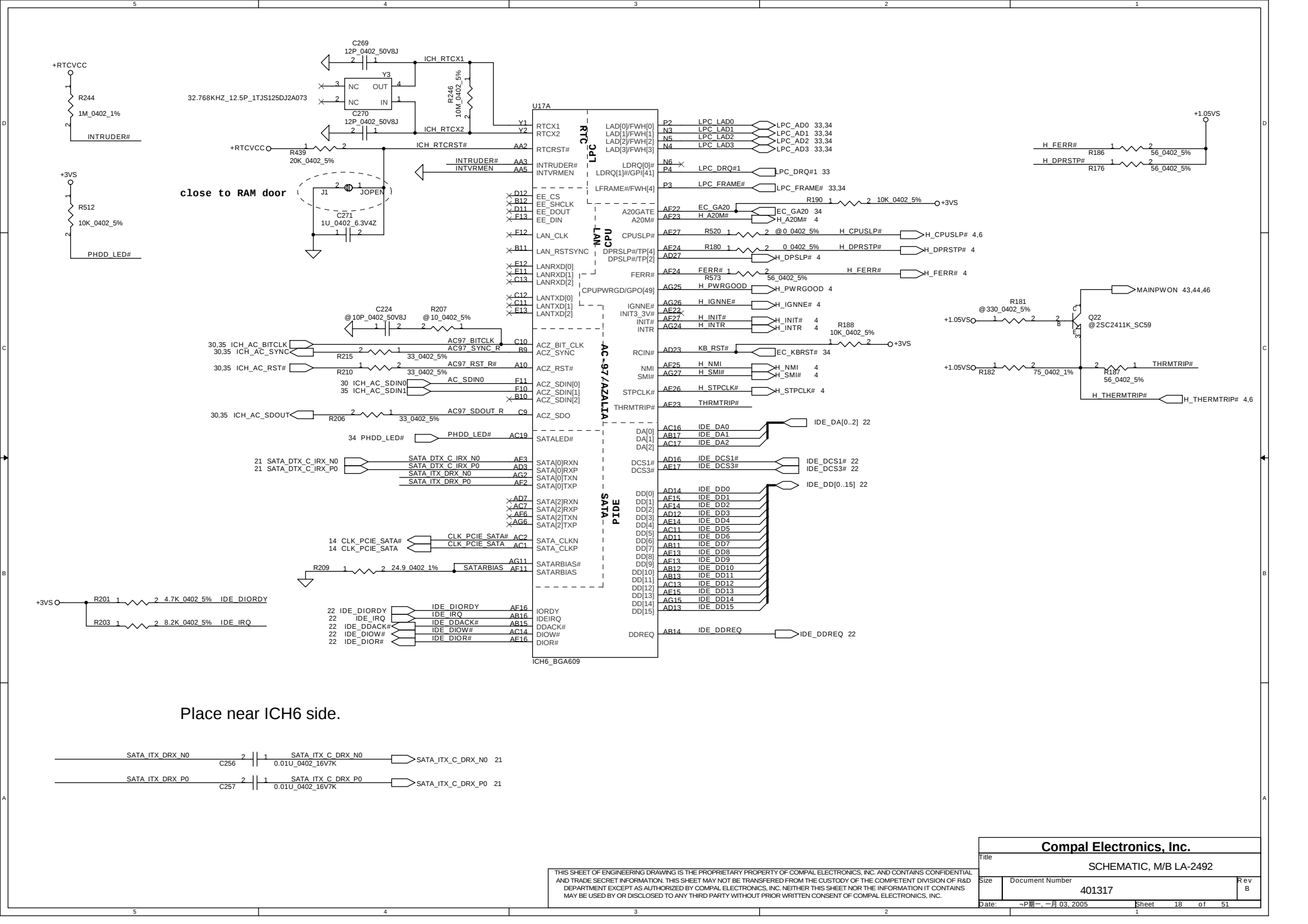
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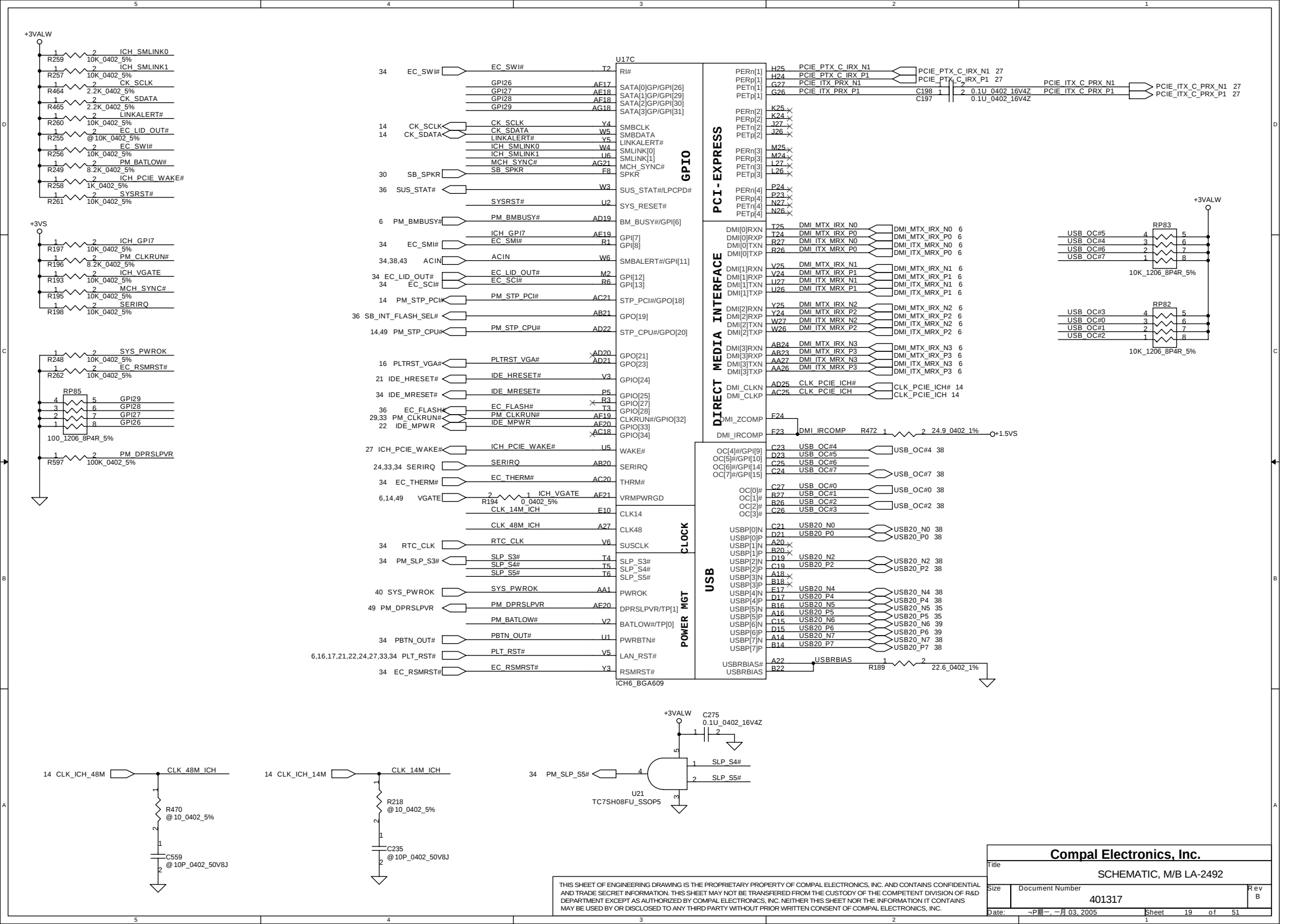
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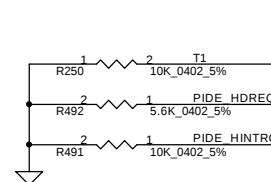
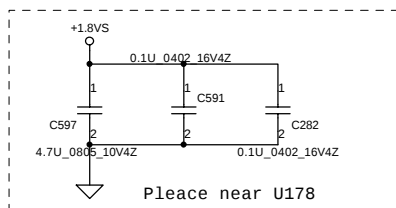
Date: ~P開一, 一月 03, 2005 Sheet 16 of 51

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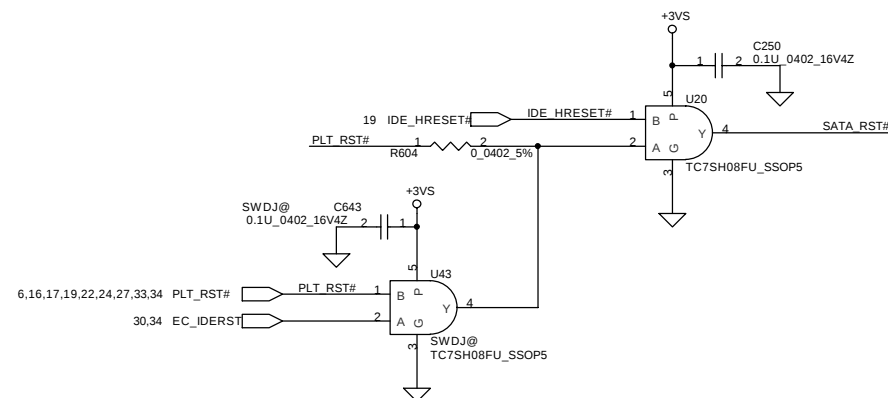
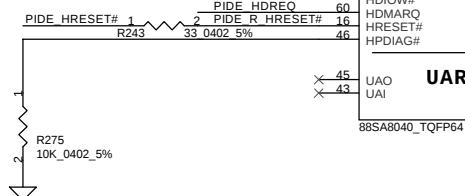
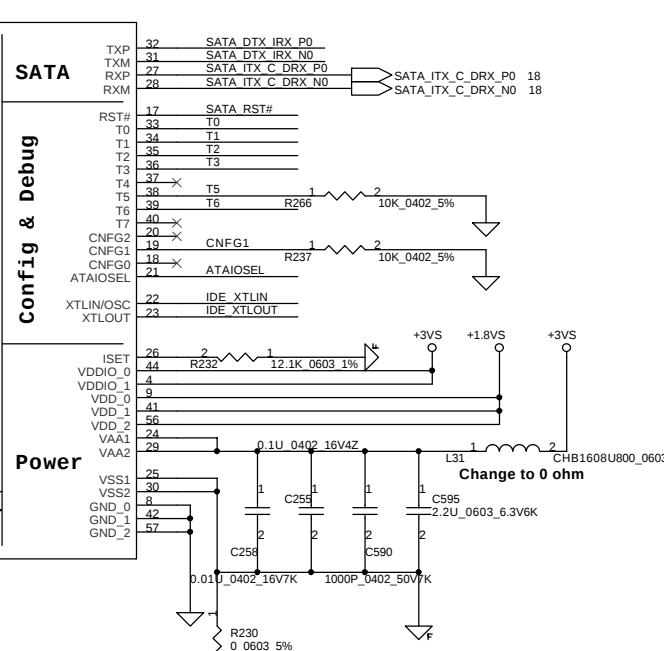




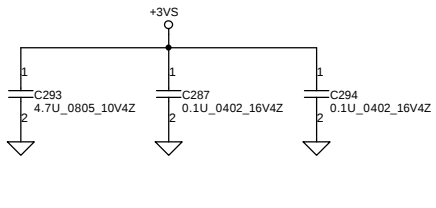


Sets maximum transfer rate and UDMA mode

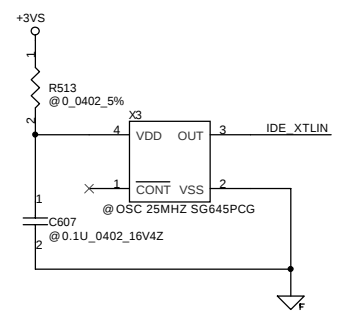
CNFG2 INT PD	CNFG1	CNFG0 INT PD	NOTE
0	0	0	Device Mode 100MB/s
0	0	1	Device Mode 133MB/s
0	1	0	Device Mode 150MB/s
1	0	0	Host Mode 100MB/s
1	0	1	Host Mode 133MB/s
1	1	0	Host Mode 150MB/s
0	1	1	Reserved
1	1	1	Reserved



Pinout diagram for the JP18 Molex 54782-4411 connector. The diagram shows two rows of pins. The top row (pins 1-20) includes PIDE HRESET#, PIDE HD7, PIDE HDD6, PIDE HDD5, PIDE HDD4, PIDE HDD3, PIDE HDD2, PIDE HDD1, PIDE HDD0, PIDE HDREQ, PIDE HDIOW#, PIDE HDIOR#, PIDE HDIORY, PIDE HDMACK#, PIDE HINTRQ, PIDE HDA1, PIDE HDA0, PIDE HCS0#, and a ground connection labeled '2 @ 10K 0402 5%'. The bottom row (pins 21-40) includes PIDE HDD8, PIDE HDD9, PIDE HDD10, PIDE HDD11, PIDE HDD12, PIDE HDD13, PIDE HDD14, PIDE HDD15, SEC CSEL R50, R50 R32, PIDE HDA2, PIDE HCS1#, and a +5VS connection. Pins 41-44 are also shown but not connected to any signal.



25MHz reference clock T[4:3] = 01



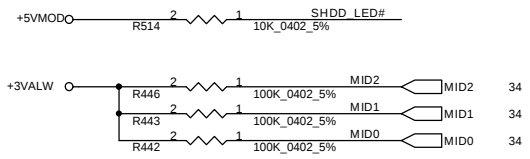
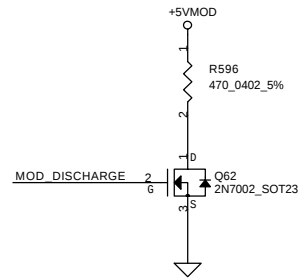
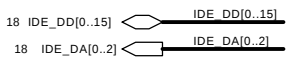
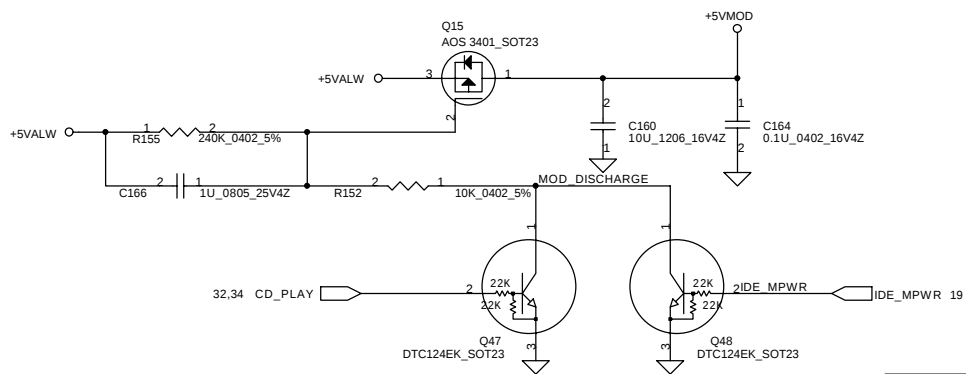
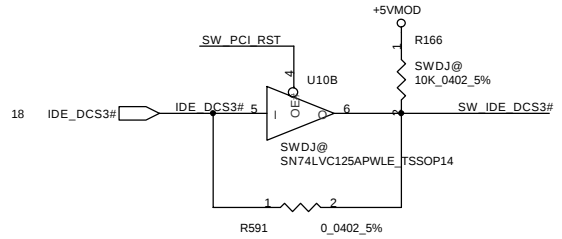
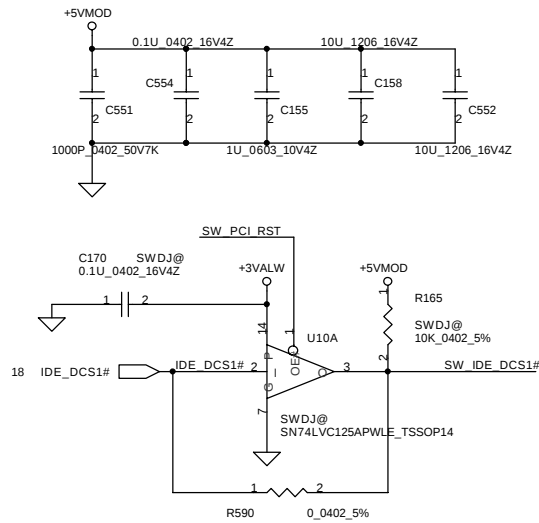
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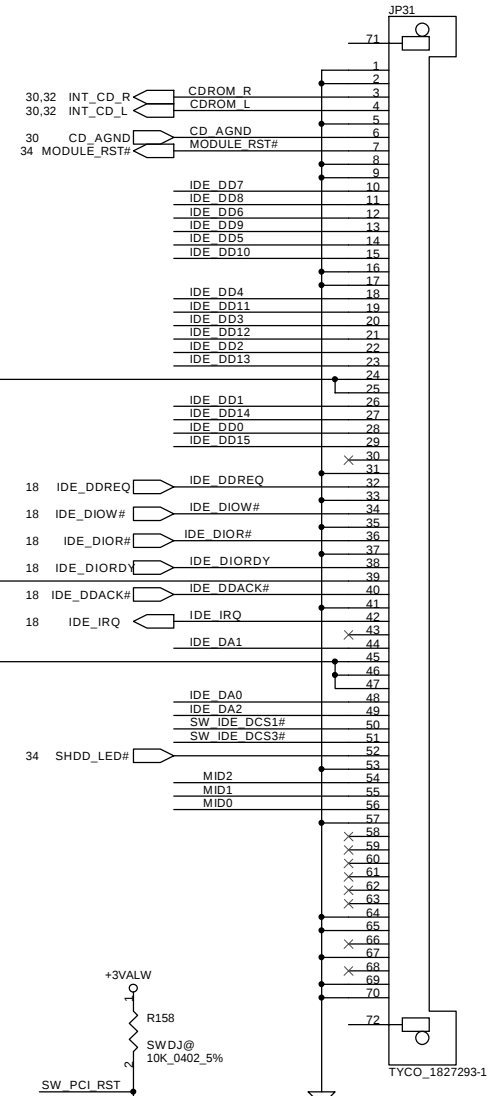
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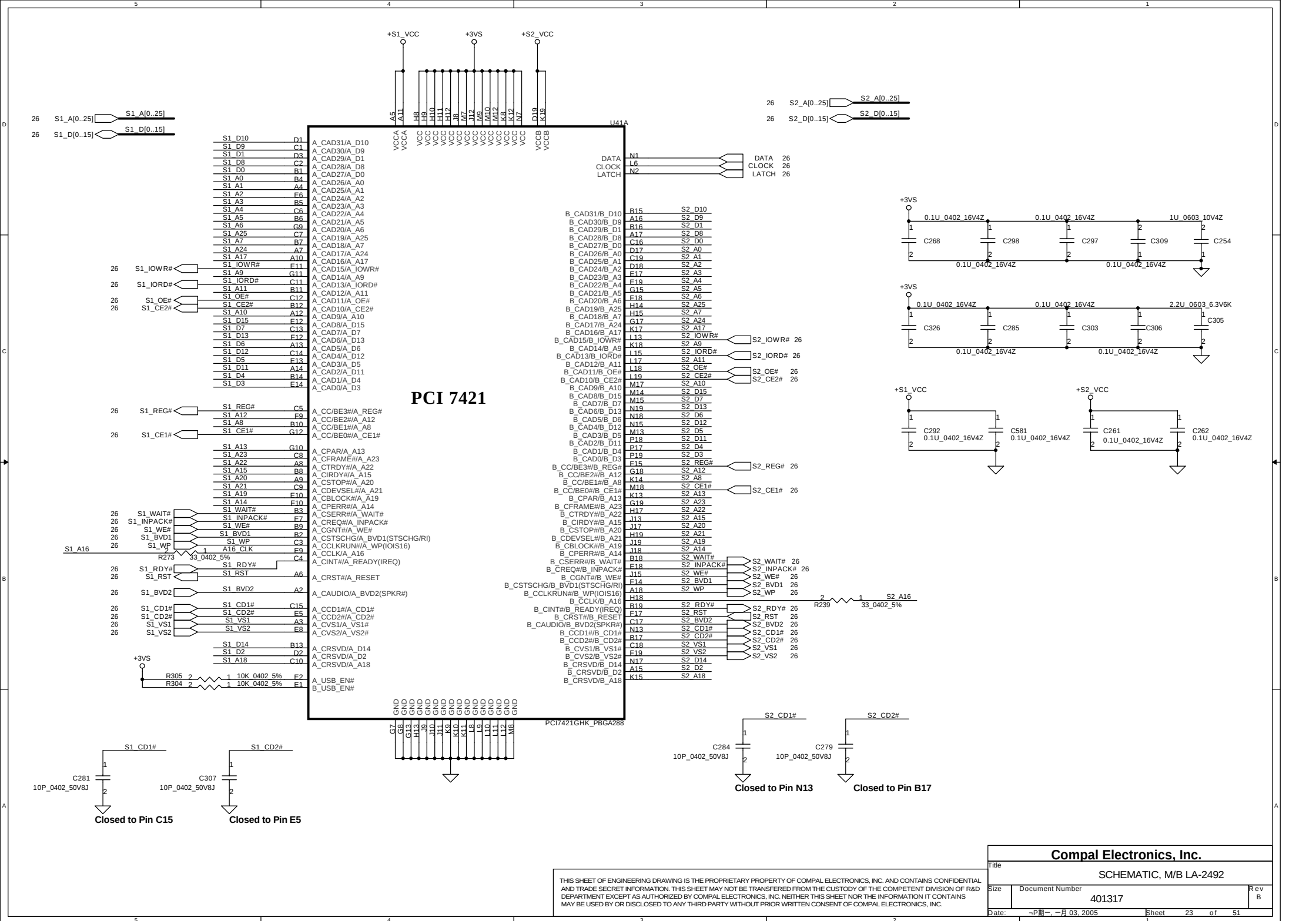


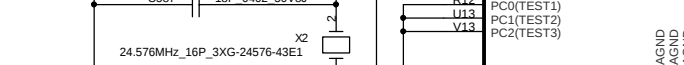
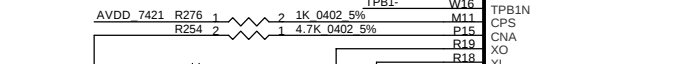
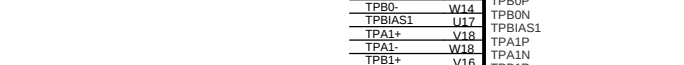
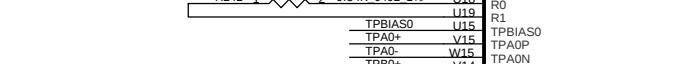
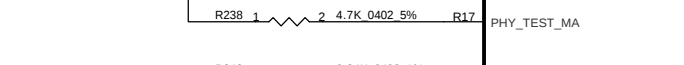
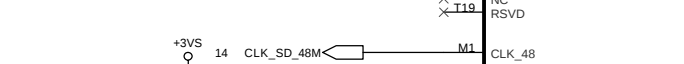
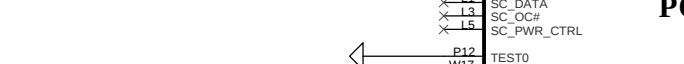
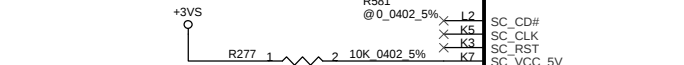
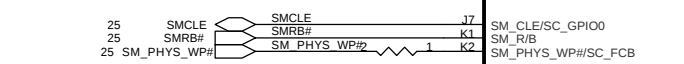
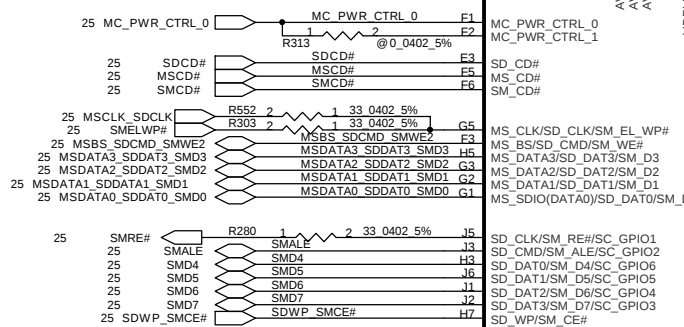
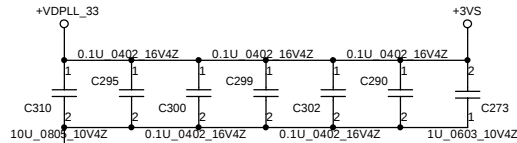
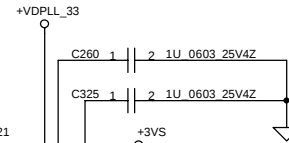
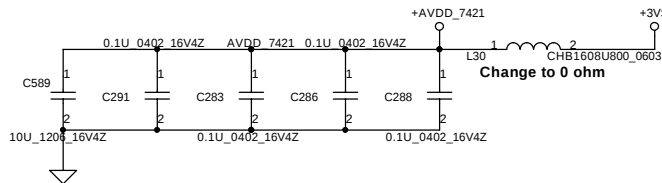
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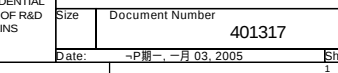
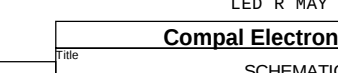
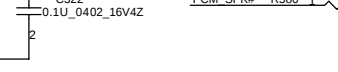
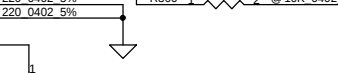
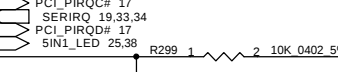
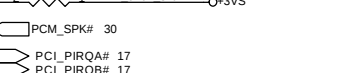
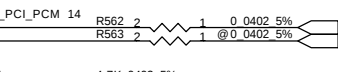
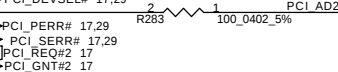
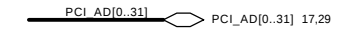
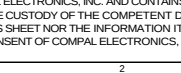
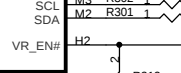
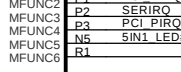
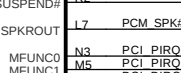
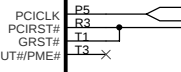
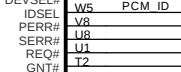
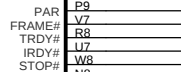
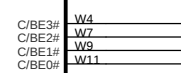
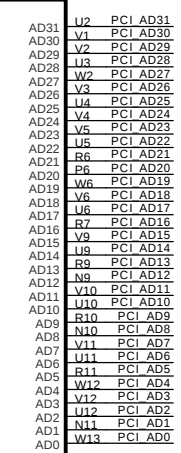
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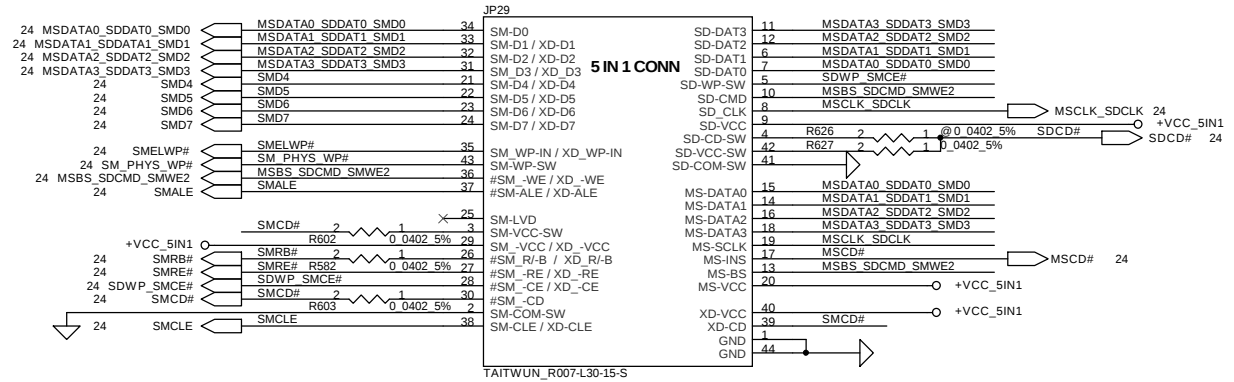
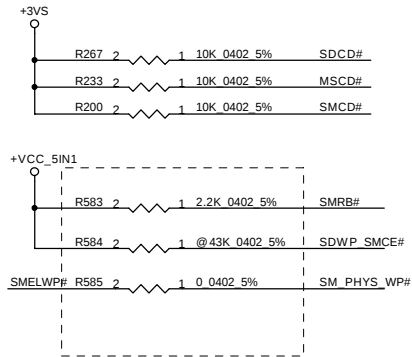


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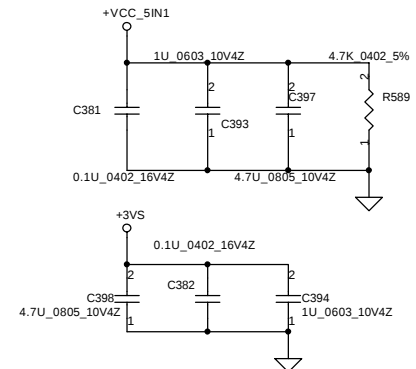
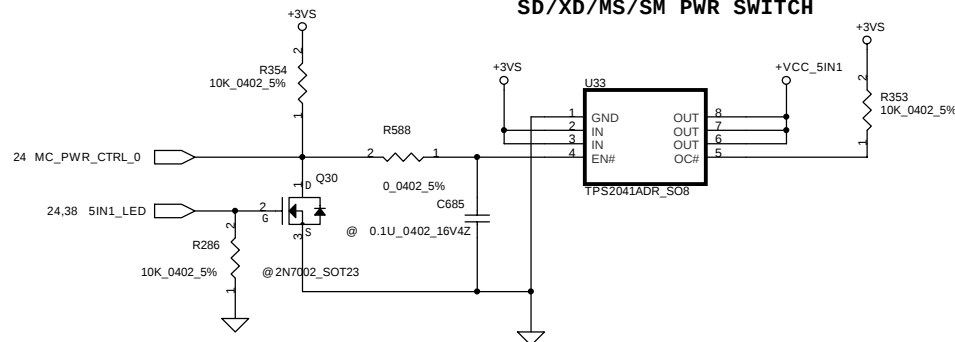
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Sheet		
24 of 51		
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5 in 1 CardReader Conn.



SD/XD/MS/SM PWR SWITCH



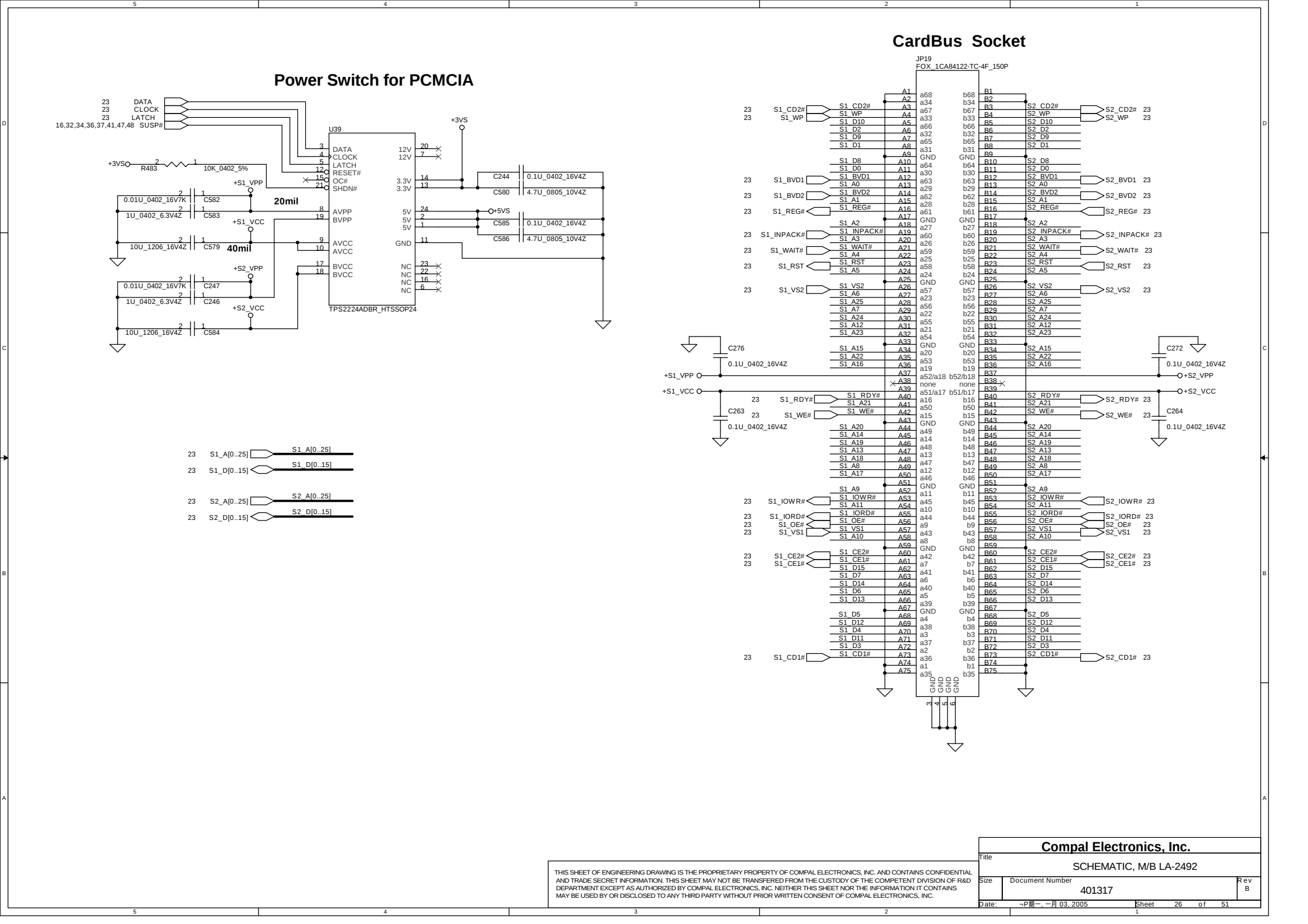
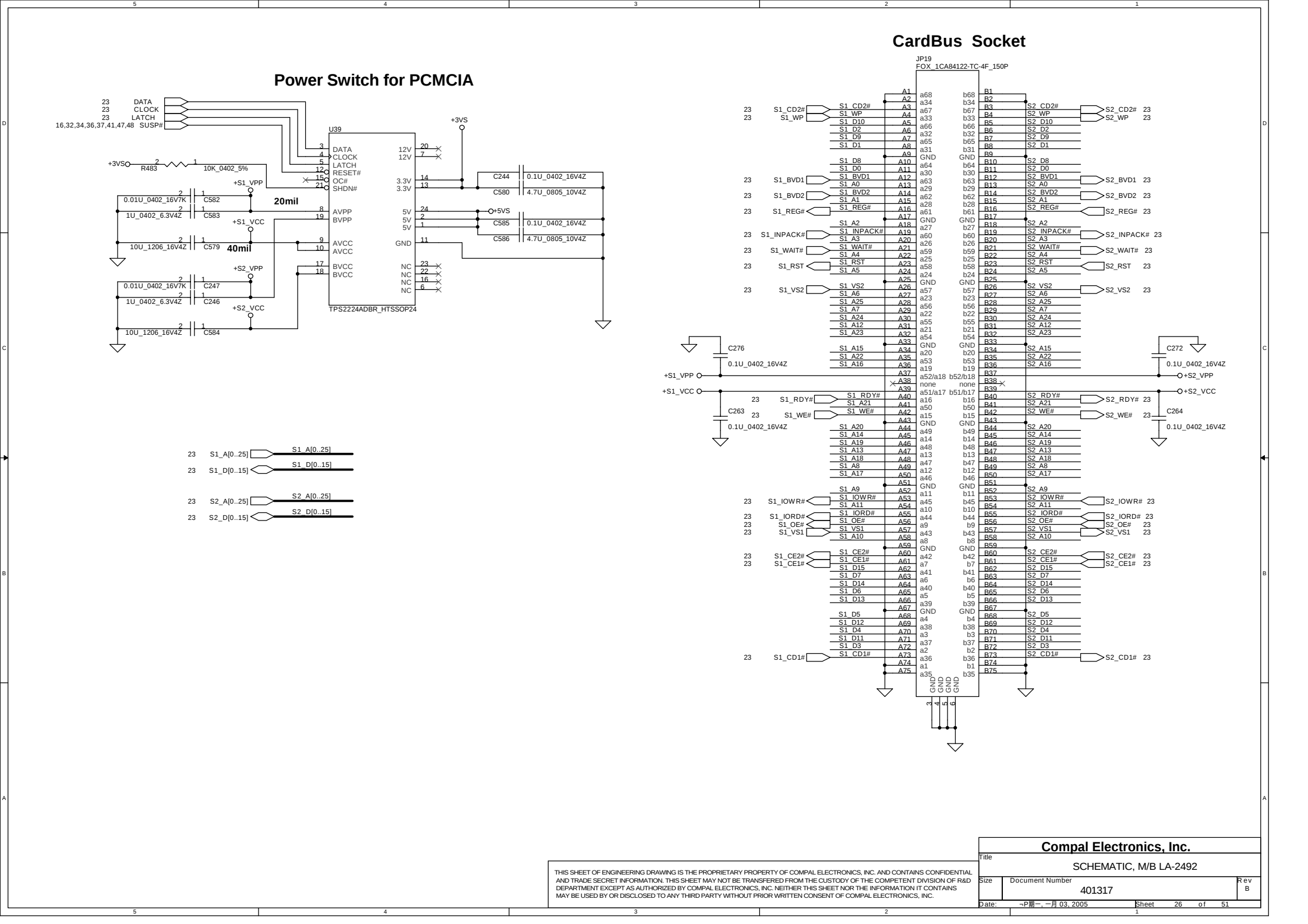
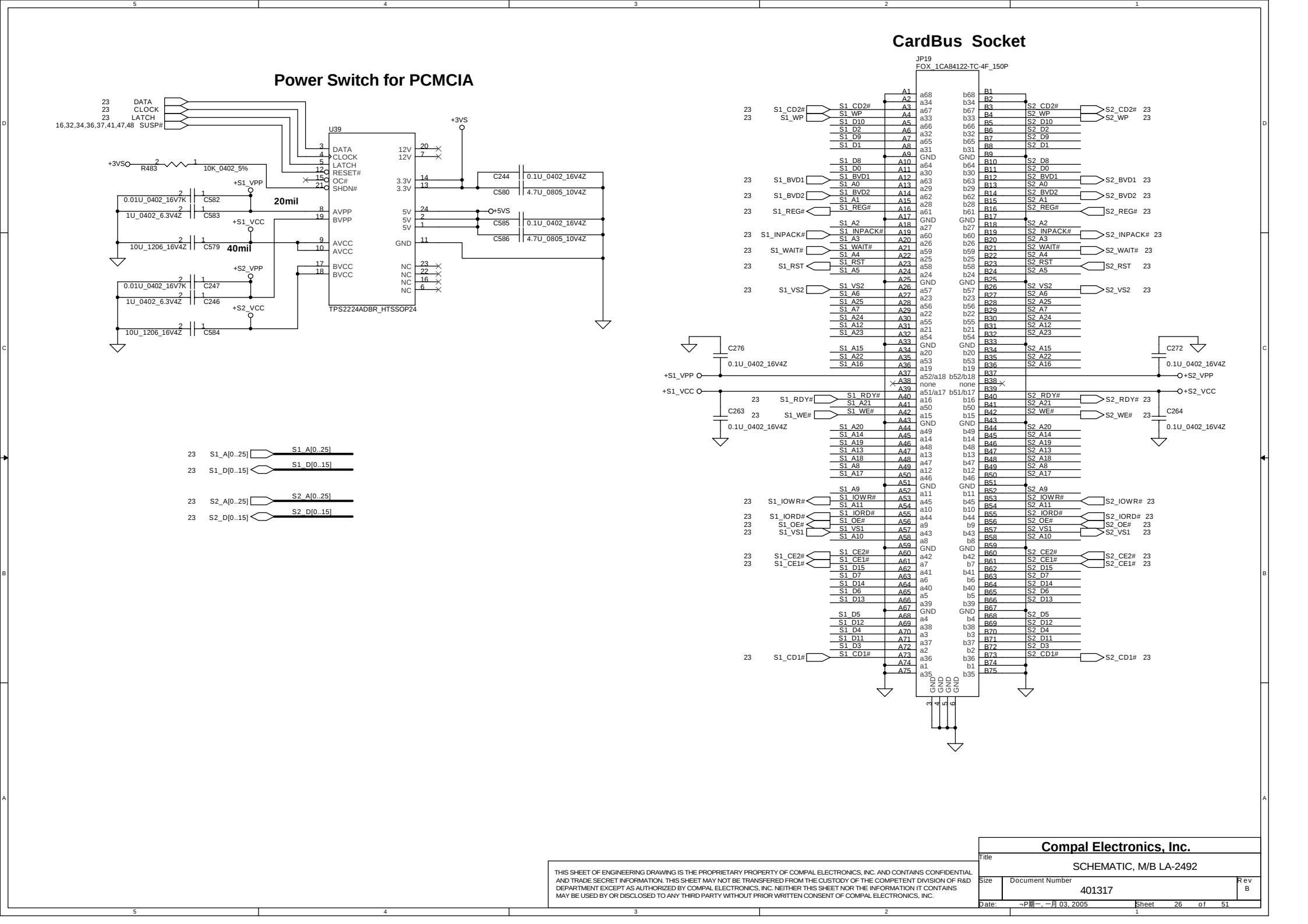
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Title SCHEMATIC, M/B LA-2492

Size Document Number 401317 Rev B

Date: ~P 一月 03, 2005 Sheet 25 of 51

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The schematic diagram illustrates the internal circuitry of a PCMCIA card, divided into two main functional blocks: the Power Switch for PCMCIA and the CardBus Socket.

Power Switch for PCMCIA: This section shows the power management circuitry. It includes a +3VSO input, a 10K_0402_5% resistor (R483), and several capacitors (C582, C583, C579, C247, C246, C584). The circuit is controlled by a TPS2224ADBR HTSSOP24 (U39) which manages the +S1_VPP, +S1_VCC, +S2_VPP, and +S2_VCC signals. The diagram also shows the connection of the PCMCIA data bus (DATA, CLOCK, LATCH, SUSP#) to the internal components.

CardBus Socket: This section shows the connection of the CardBus socket (JP19, FOX 1CA84122-TC-4F_150P) to the internal components. It includes a detailed pinout for the socket, showing the connection of various signals (S1_CD2#, S1_WP, S1_D10, S1_D9, S1_D8, S1_D0, S1_BVD1, S1_BVD2, S1_REG#, S1_INPACK#, S1_WAIT#, S1_RST, S1_VS2, S1_RDY#, S1_WE#, S1_IOWR#, S1_IORD#, S1_OE#, S1_VS1, S1_CE2#, S1_CE1#, S1_CD1#) to the internal components (A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75). The diagram also shows the connection of the CardBus data bus (S2_CD2#, S2_WP, S2_D10, S2_D9, S2_D8, S2_D0, S2_BVD1, S2_BVD2, S2_REG#, S2_INPACK#, S2_WAIT#, S2_RST, S2_VS2, S2_RDY#, S2_WE#, S2_IOWR#, S2_IORD#, S2_OE#, S2_VS1, S2_CE2#, S2_CE1#, S2_CD1#) to the internal components.

The diagram is a detailed technical drawing, likely a schematic, showing the internal circuitry of a PCMCIA card. It includes components like resistors (R483), capacitors (C244, C580, C585, C586, C276, C263, C272, C264), and integrated circuits (U39, TPS2224ADBR HTSSOP24). The diagram is divided into two main sections: "Power Switch for PCMCIA" and "CardBus Socket". The "Power Switch for PCMCIA" section shows the connection of the +3VSO input to the internal components, including the TPS2224ADBR HTSSOP24. The "CardBus Socket" section shows the connection of the CardBus socket (JP19) to the internal components, including the FOX 1CA84122-TC-4F_150P. The diagram also shows the connection of various signals (S1_CD2#, S1_WP, S1_D10, S1_D9, S1_D8, S1_D0, S1_BVD1, S1_BVD2, S1_REG#, S1_INPACK#, S1_WAIT#, S1_RST, S1_VS2, S1_RDY#, S1_WE#, S1_IOWR#, S1_IORD#, S1_OE#, S1_VS1, S1_CE2#, S1_CE1#, S1_CD1#) to the internal components. The diagram is a detailed technical drawing, likely a schematic, showing the internal circuitry of a PCMCIA card.

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The diagram is a detailed technical drawing, likely a schematic, showing the internal circuitry of a PCMCIA card. It includes components like resistors, capacitors, and integrated circuits (ICs) connected to various pins of the PCMCIA connector. The diagram is divided into two main sections: "Power Switch for PCMCIA" and "CardBus Socket". The "Power Switch for PCMCIA" section shows the connection of the PCMCIA power pins (DATA, CLOCK, LATCH, SUSP#) to the internal power switch circuitry, which includes a 3VSO input, a 10K_0402_5% resistor, and several capacitors (C582, C583, C579, C247, C246, C584). The "CardBus Socket" section shows the connection of the CardBus socket (JP19, FOX 1CA84122-TC-4F_150P) to the internal circuitry, including a detailed pinout for the socket and the connection of the CardBus data bus (DATA, CLOCK, LATCH, SUSP#) to the internal components. The diagram is a technical drawing, likely a schematic, showing the internal circuitry of a PCMCIA card.

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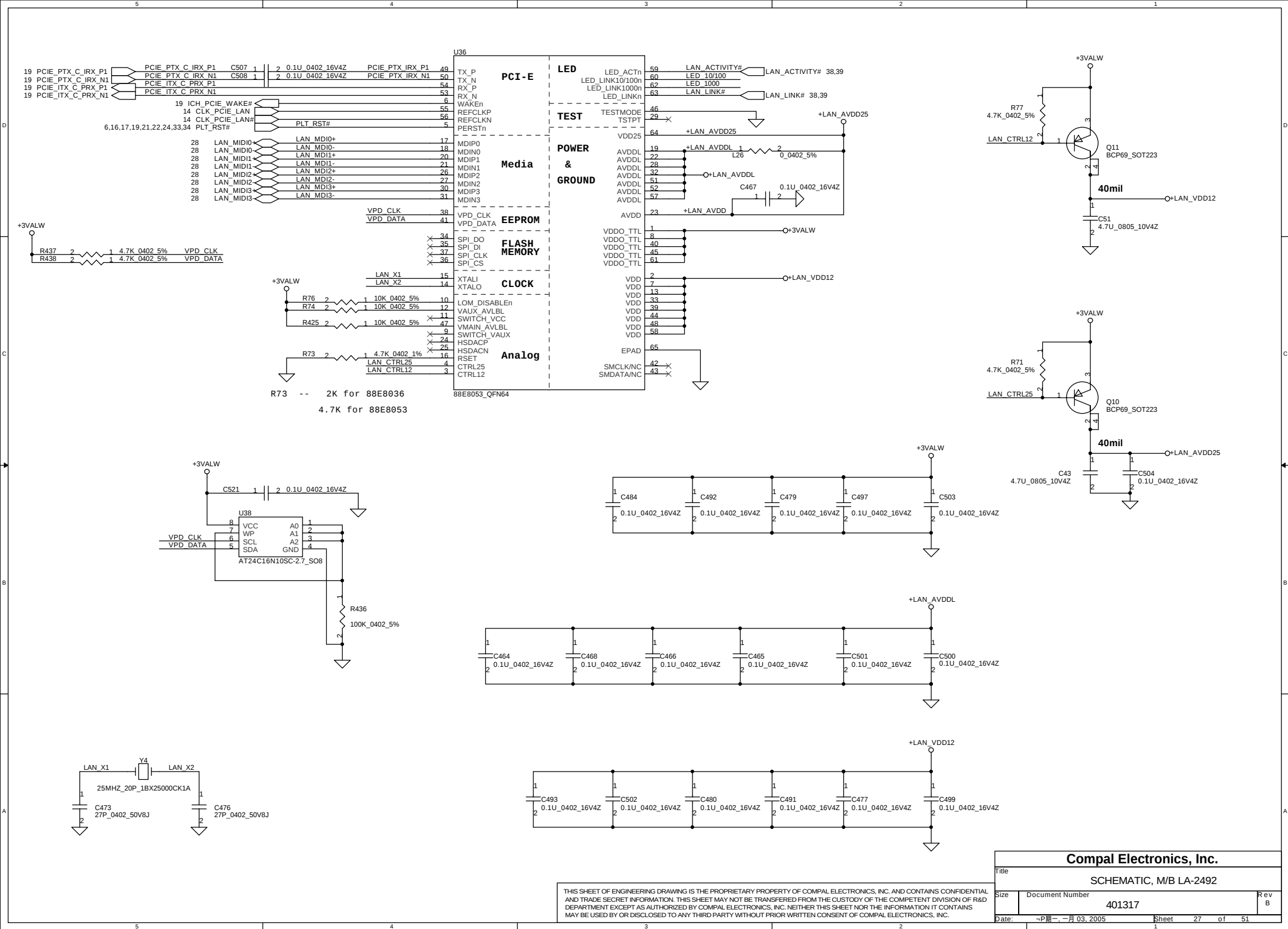
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Size	Document Number	Rev	
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Date:	~P開一, 一月 03, 2005	Sheet	26 of 51
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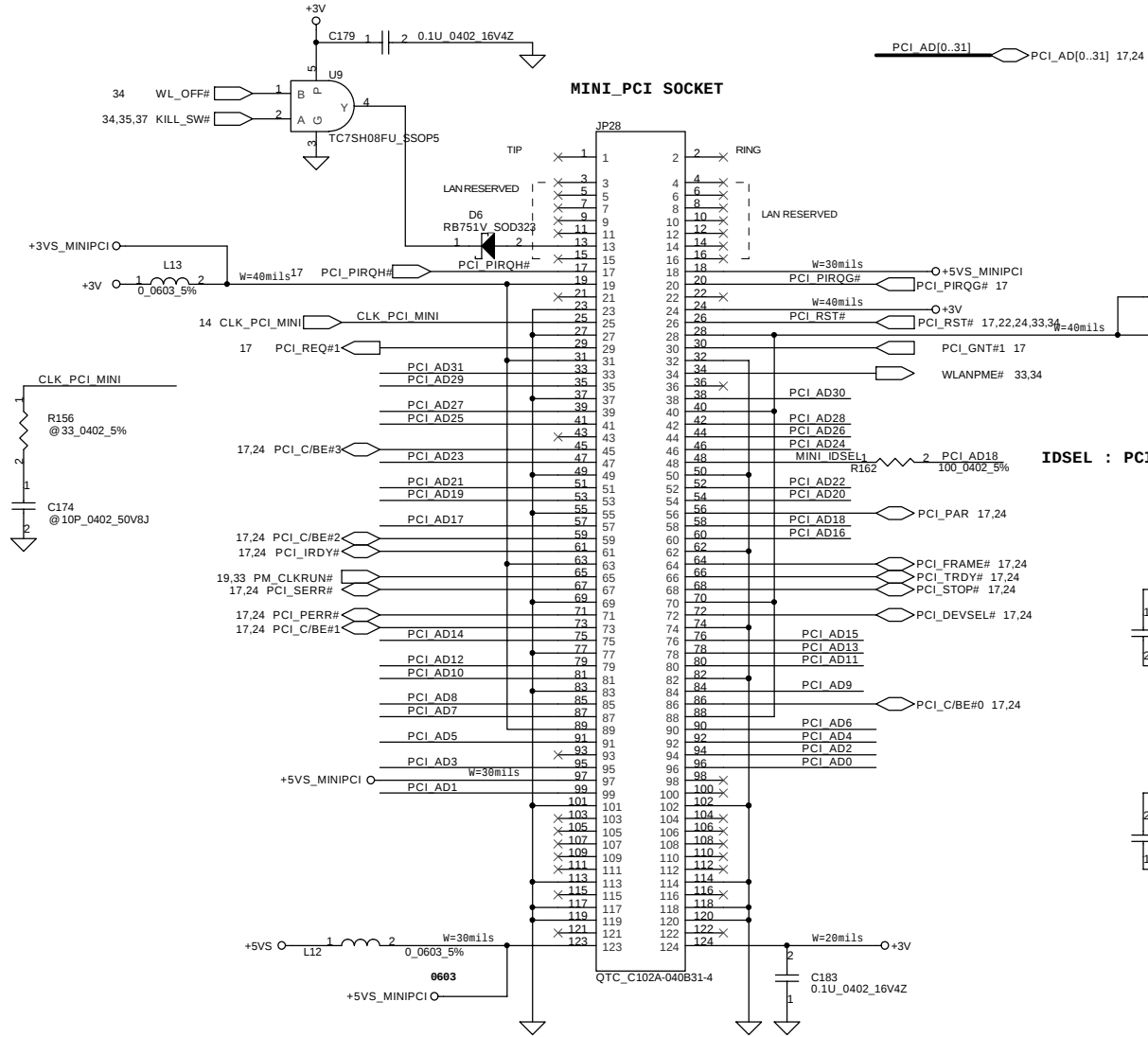
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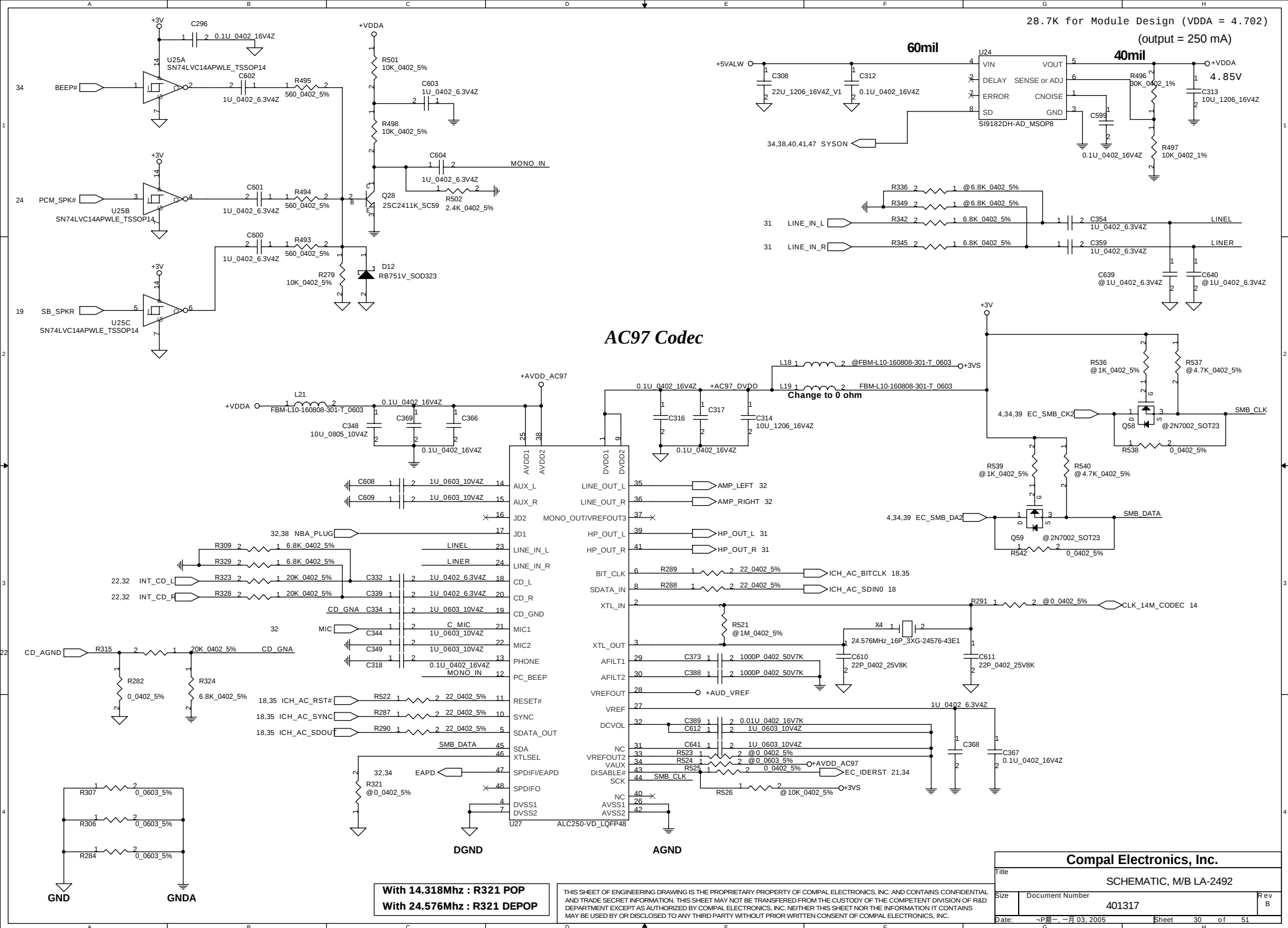




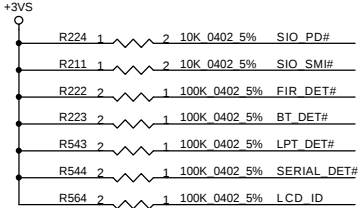
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Size	Document Number		Rev
	401317		B
Date:	~P 關一, 一月 03, 2005		Sheet 29 of 51

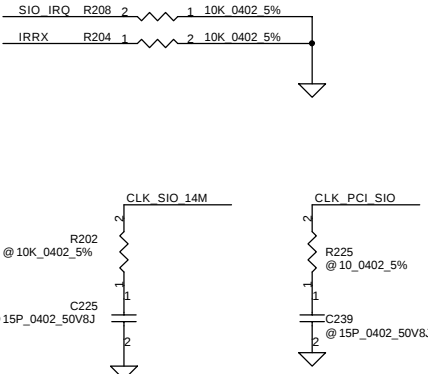
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SUPER I/O SMsC LPC47N217



LCD ID : High -- EDID
Low -- Panel ID



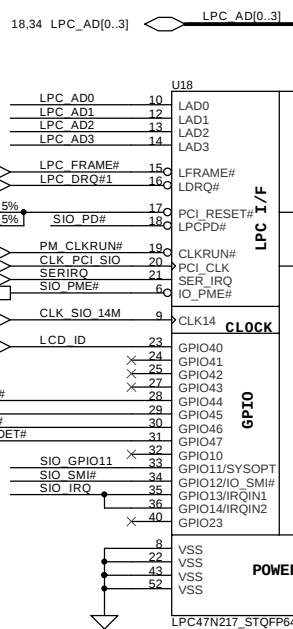
17,22,24,29,34 PCI_RST#
6,16,17,19,21,22,24,27,34 PLT_RST#

18,34 LPC_FRAME#
18 LPC_DRQ#1

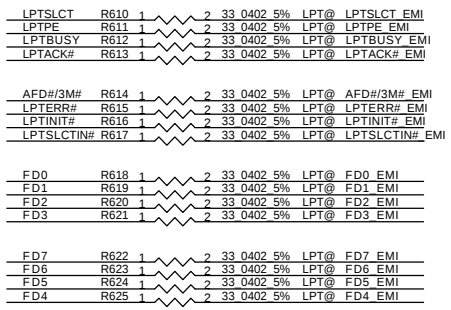
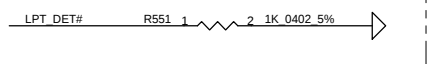
19,29 PM_CLKRUN#
14 CLK_PCI_SIO
19,24,34 SERIRQ
29,34 SIO_PME#

14 CLK_14M_SIO
16,17 LCD_ID

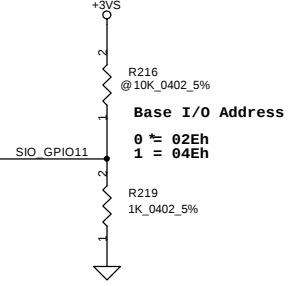
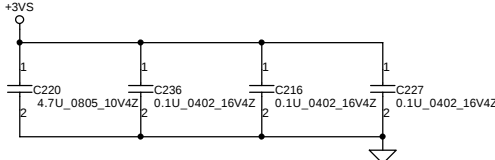
37 FIR_DET#
17,35 BT_DET#
38 SERIAL_DET#



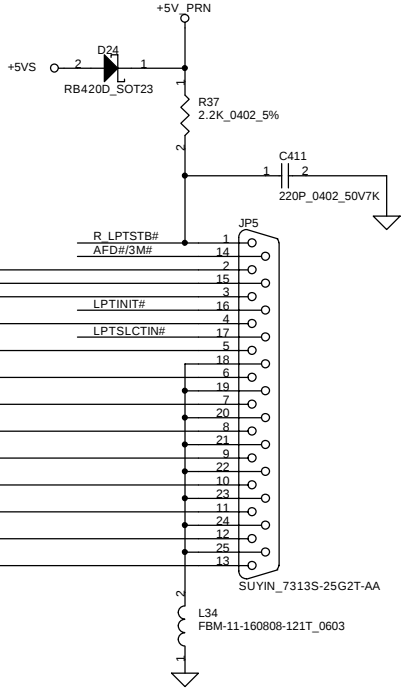
LPT Module
L: R POP LPT Enable
H: R De-POP LPT Disable



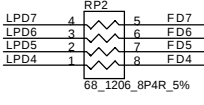
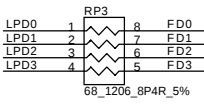
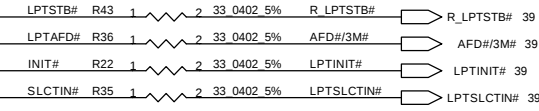
EMI Request for LPT ISSUE



Parallel Port

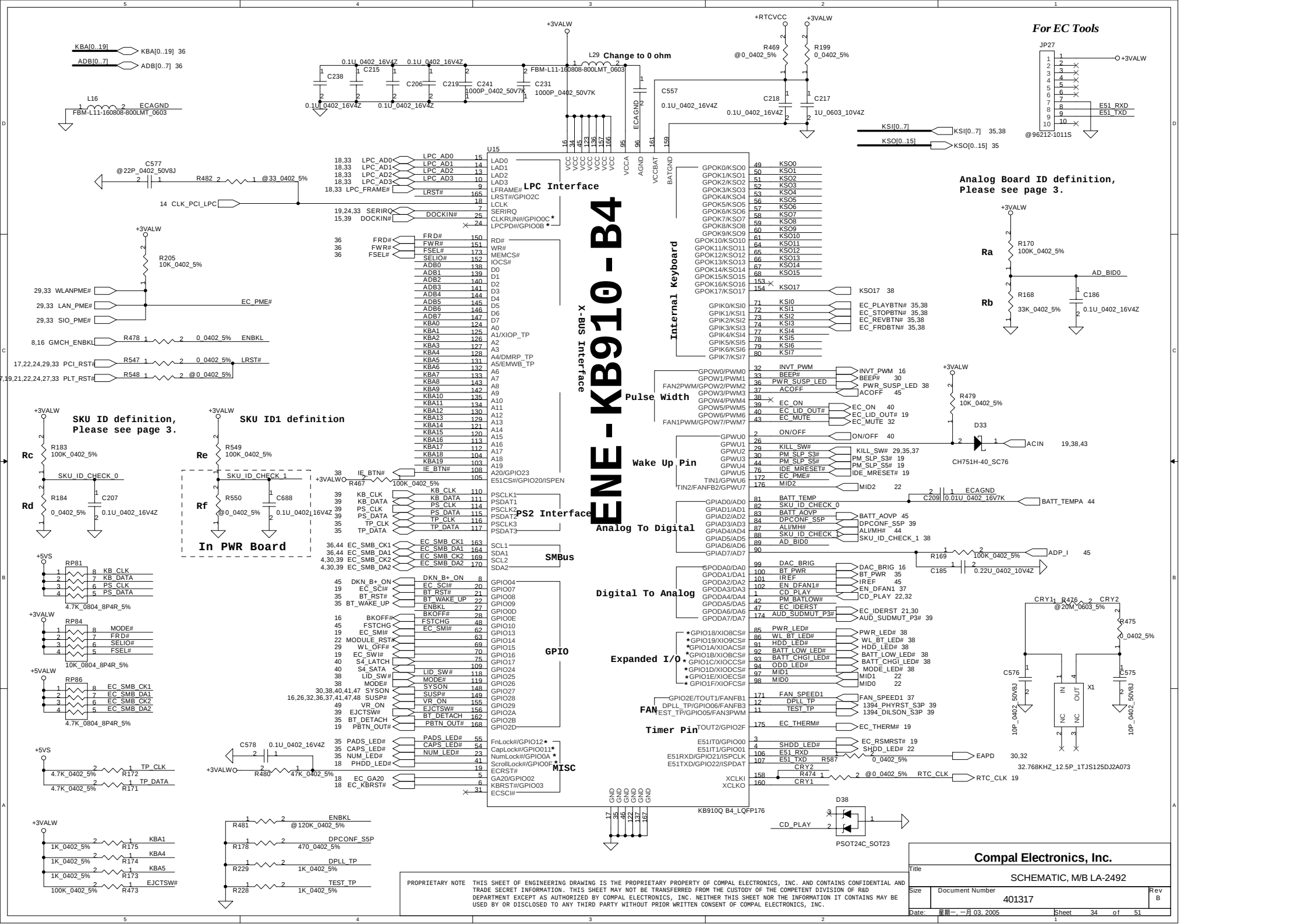


Close to Docking

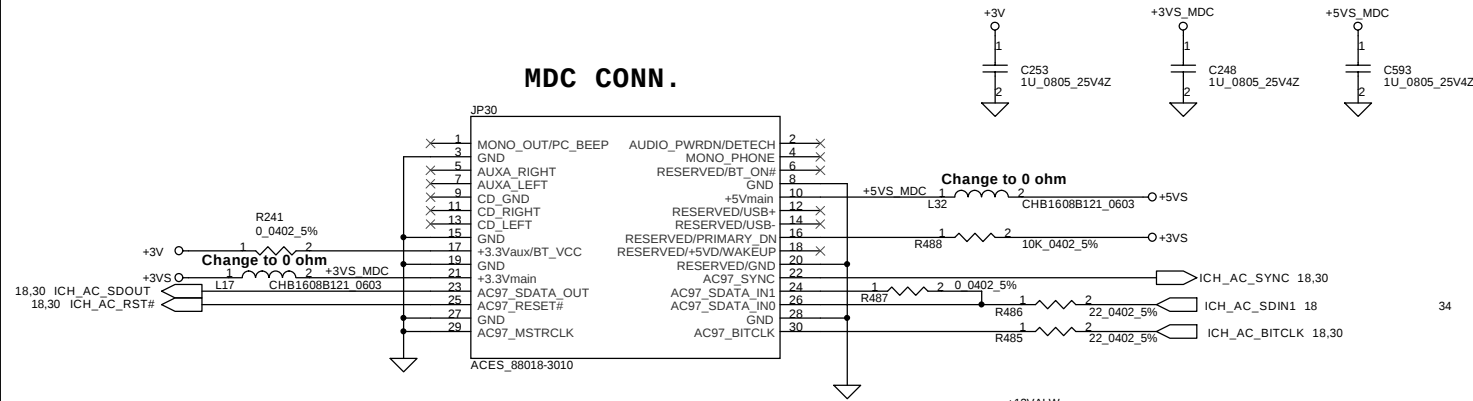


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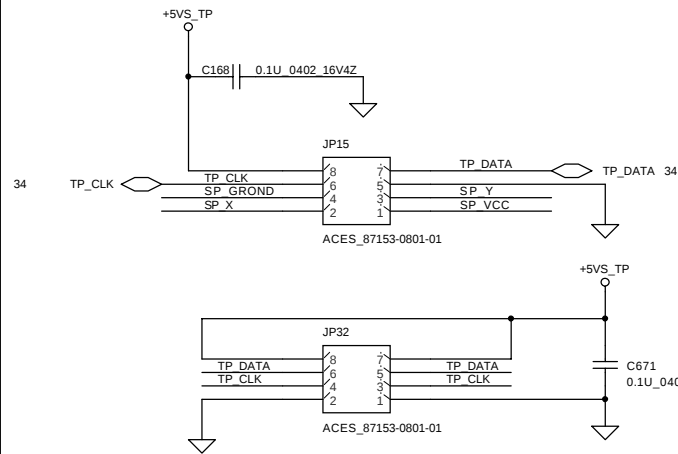
Compal Electronics, Inc.		
Title		
SCHEMATIC, M/B LA-2492		
Size	Document Number	Rev
	401317	B
Date:	~P 十一月 03, 2005	Sheet 33 of 51



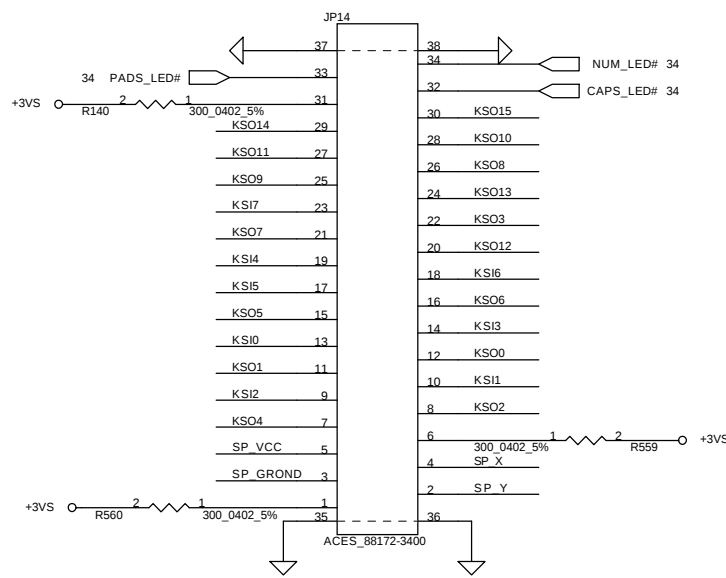
MDC CONN.



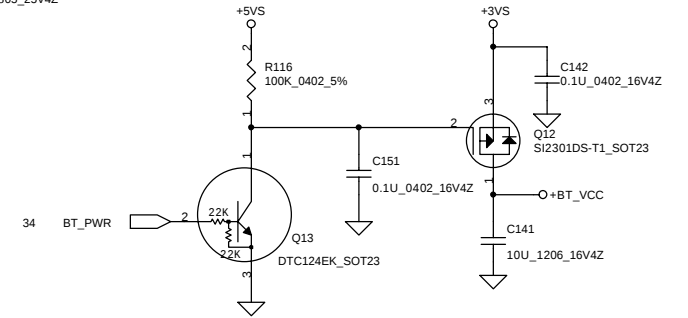
TP CONN.



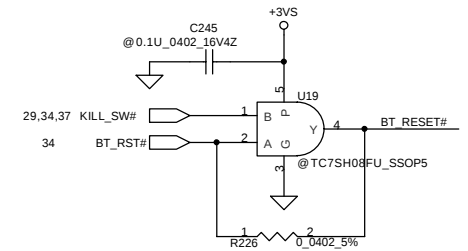
INT_KBD CONN.



BlueTooth Interface

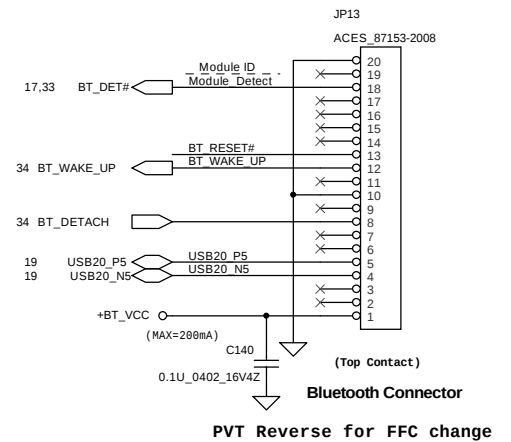


Module ID
Indication for polarity of reset
Reset input High Active -> Low,
Reset input Low Active -> Open



KSO7	C625	100P 0402 25V8K
KSO6	C626	100P 0402 25V8K
KSO5	C627	100P 0402 25V8K
KSO4	C628	100P 0402 25V8K
KSO3	C629	100P 0402 25V8K
KSI4	C630	100P 0402 25V8K
KSO2	C631	100P 0402 25V8K
KSO1	C632	100P 0402 25V8K
KSO0	C633	100P 0402 25V8K
KSI5	C634	100P 0402 25V8K
KSI6	C635	100P 0402 25V8K
KSI7	C636	100P 0402 25V8K
KSO8	C624	100P 0402 25V8K

KSO15	C613	100P 0402 25V8K
KSO14	C614	100P 0402 25V8K
KSO13	C615	100P 0402 25V8K
KSO12	C616	100P 0402 25V8K
KSI0	C617	100P 0402 25V8K
KSO11	C618	100P 0402 25V8K
KSO10	C619	100P 0402 25V8K
KSI1	C620	100P 0402 25V8K
KSI2	C621	100P 0402 25V8K
KSO9	C622	100P 0402 25V8K
KSI3	C623	100P 0402 25V8K
PADS_LED#	C682	100P 0402 25V8K
NUM_LED#	C683	100P 0402 25V8K
CAPS_LED#	C684	100P 0402 25V8K

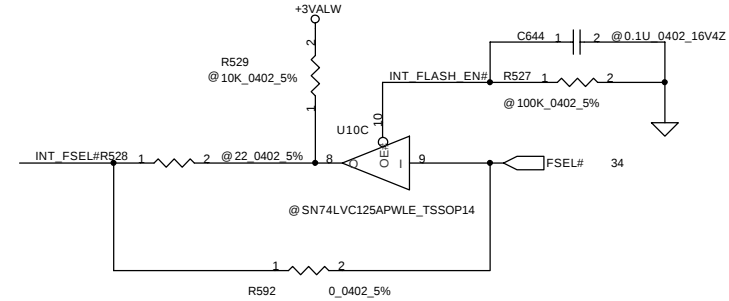
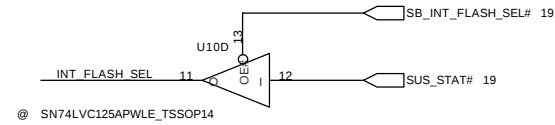


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SCHEMATIC, M/B LA-2492

Title	Size	Document Number	Rev
		401317	B
Date: ~P 開一、一月 03, 2005	Sheet	35 of 51	

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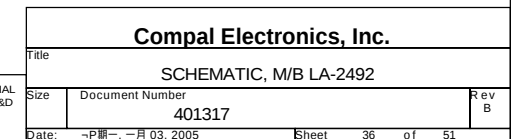


JP17

KBA16 1
 KBA15 2
 KBA14 3
 KBA13 4
 KBA12 5
 KBA11 6
 KBA9 7
 KBA8 8
 FWE# 9
 RESET# 10
 INT_FLASH_EN# 11
 INT_FLASH_SEL 12
 KBA18 13
 KBA7 14
 KBA6 15
 KBA5 16
 KBA4 17
 KBA3 18
 KBA2 19
 KBA1 20

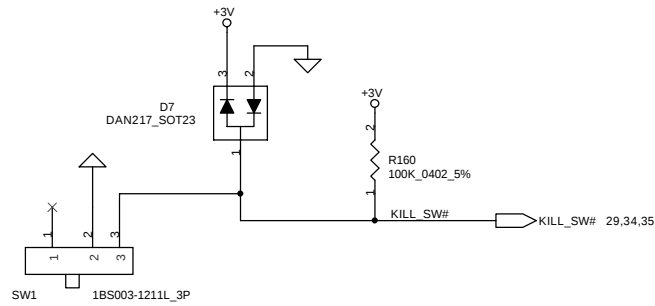
KBA17 21
 KBA19 22
 KBA10 23
 AD8 24
 AD6 25
 AD5 26
 AD4 27
 +3VALW 28
 AD3 29
 AD2 30
 AD1 31
 AD0 32
 FRD# 33
 FSEL# 34
 KBA0 35

@ SUYIN_80065AR-040G2T

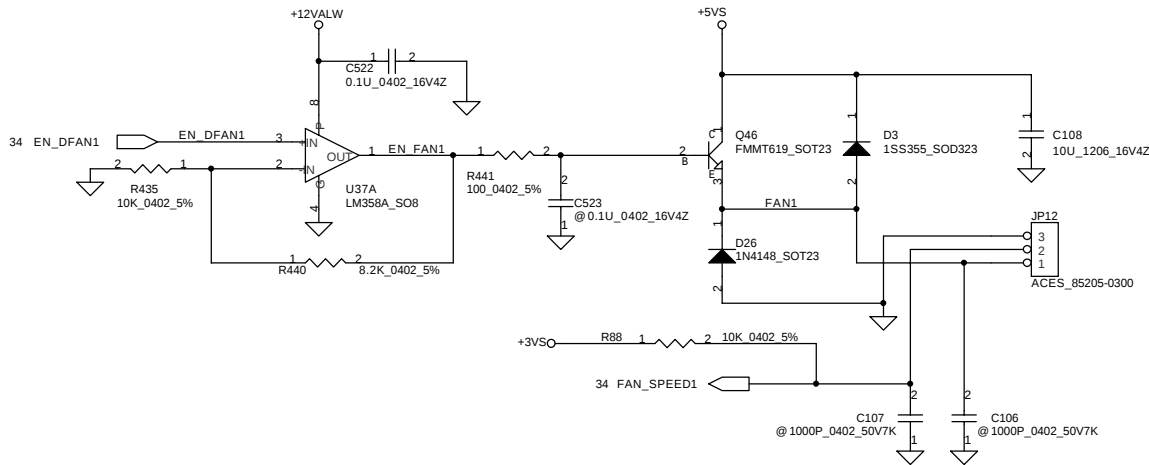


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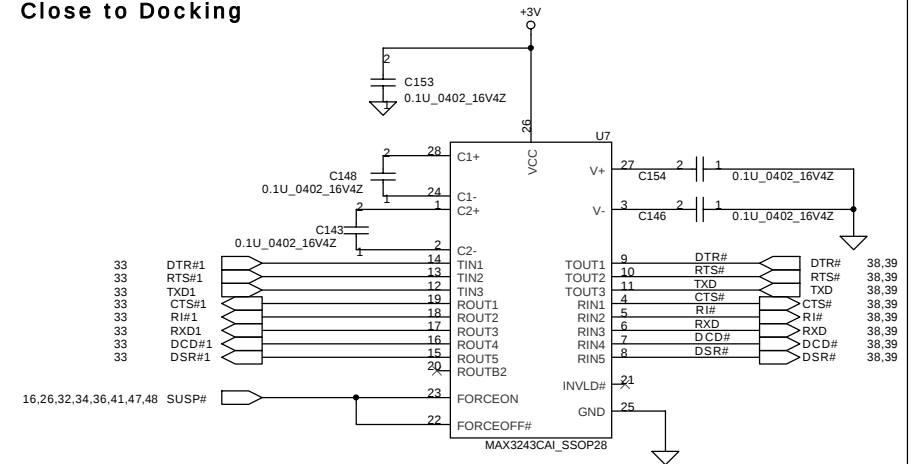
Kill SWITCH



FAN Conn



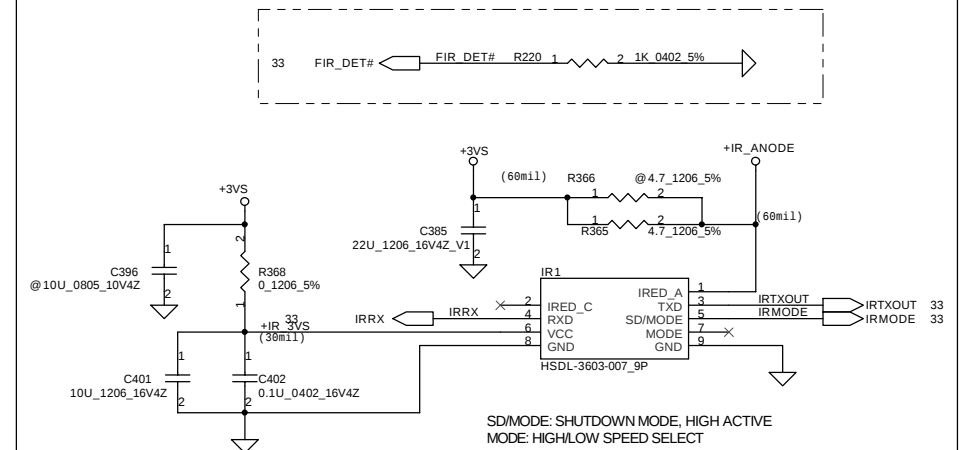
Close to Docking



No Docking and Serial Port -----> Del

FIR Module

L: R POP; FIR Enable
H: R De-POP; FIR Disable

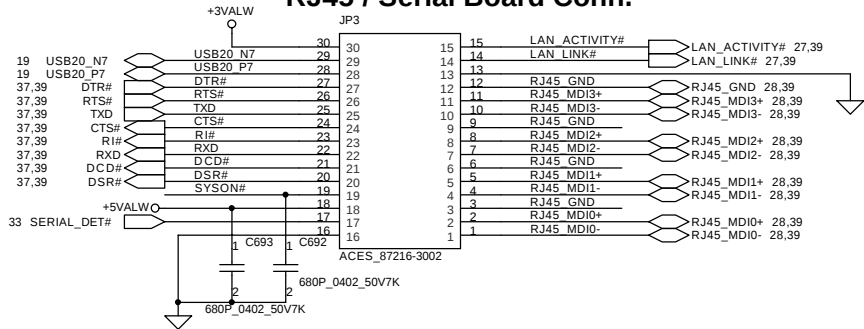


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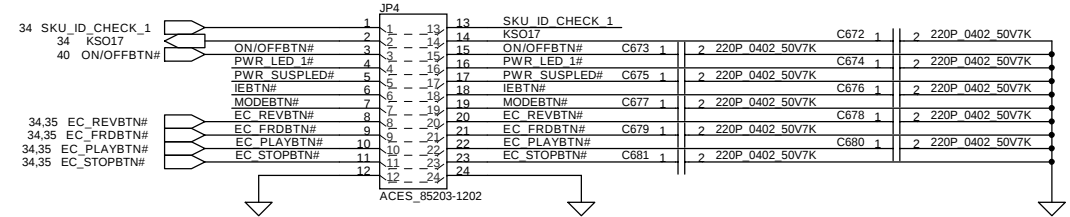
Title			
SCHEMATIC, M/B LA-2492			
Size	Document Number	Rev	
	401317	B	
Date:	~P 開一, 一月 03, 2005	Sheet	37 of 51

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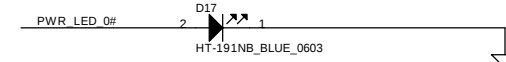
RJ45 / Serial Board Conn.



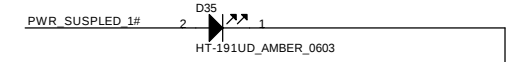
Power / LED Board Conn.



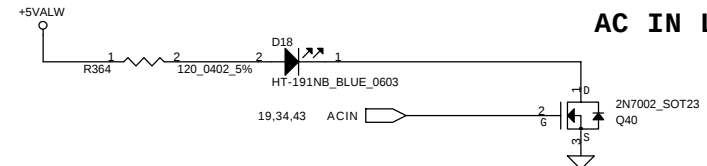
POWER/ON LED



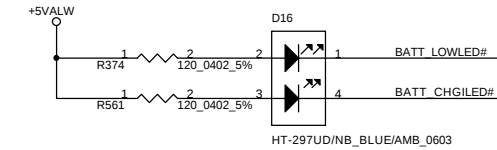
POWER/SUSP LED



AC IN LED



BATTERY CHG



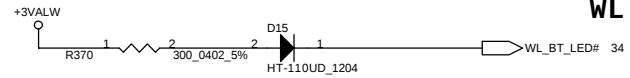
HDD LED



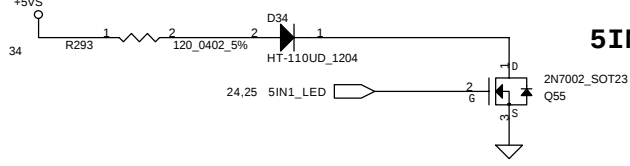
MODE LED



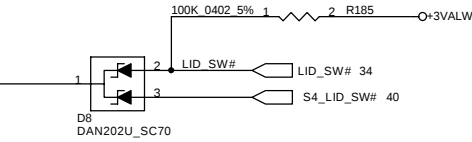
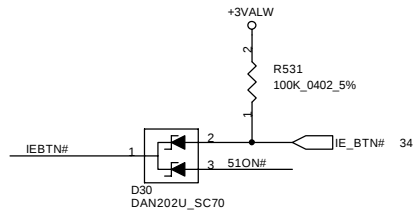
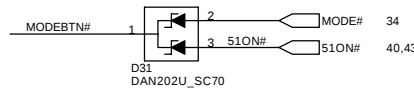
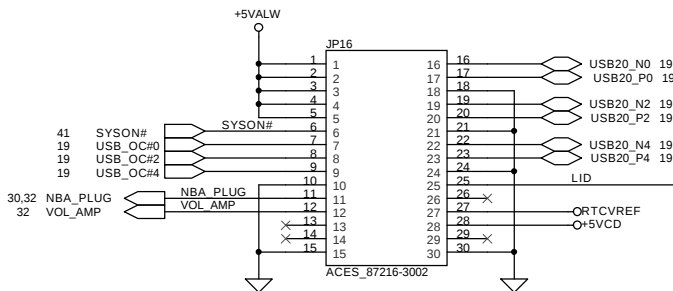
WL LED



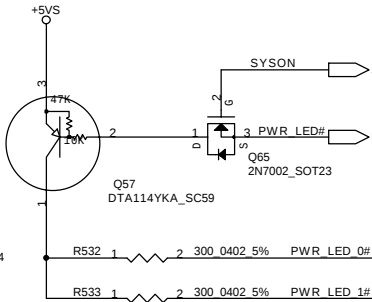
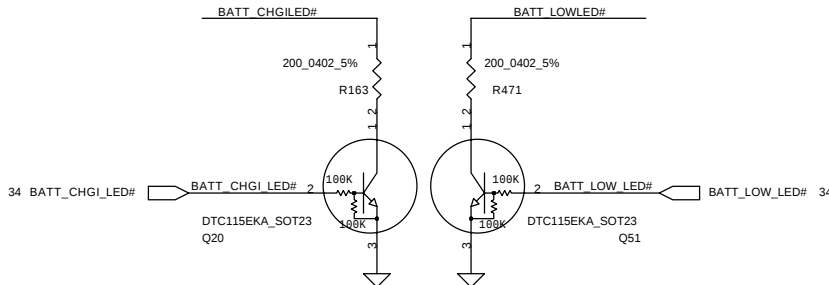
5IN1 LED



USB Board Conn.



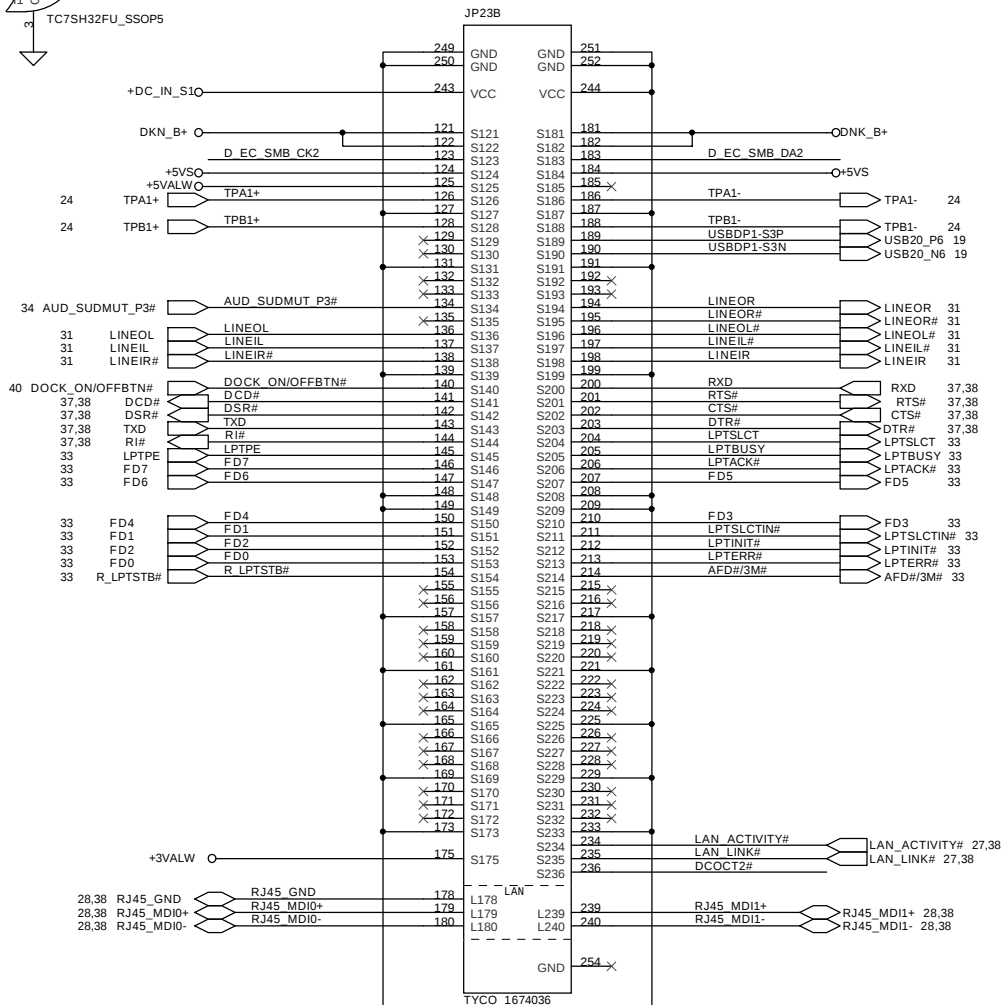
BATTERY CHG/LOW LED



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Title			SCHEMATIC, M/B LA-2492
Size			401317
Date			~P 册一, 一月 03, 2005
Sheet			38 of 51



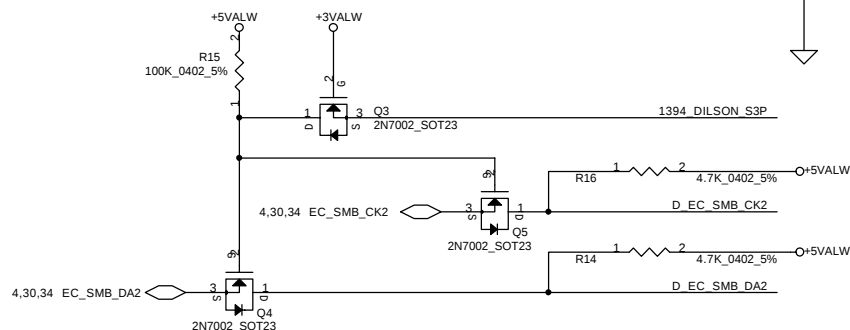
JP2

1
2
3
4

MDC1 RING

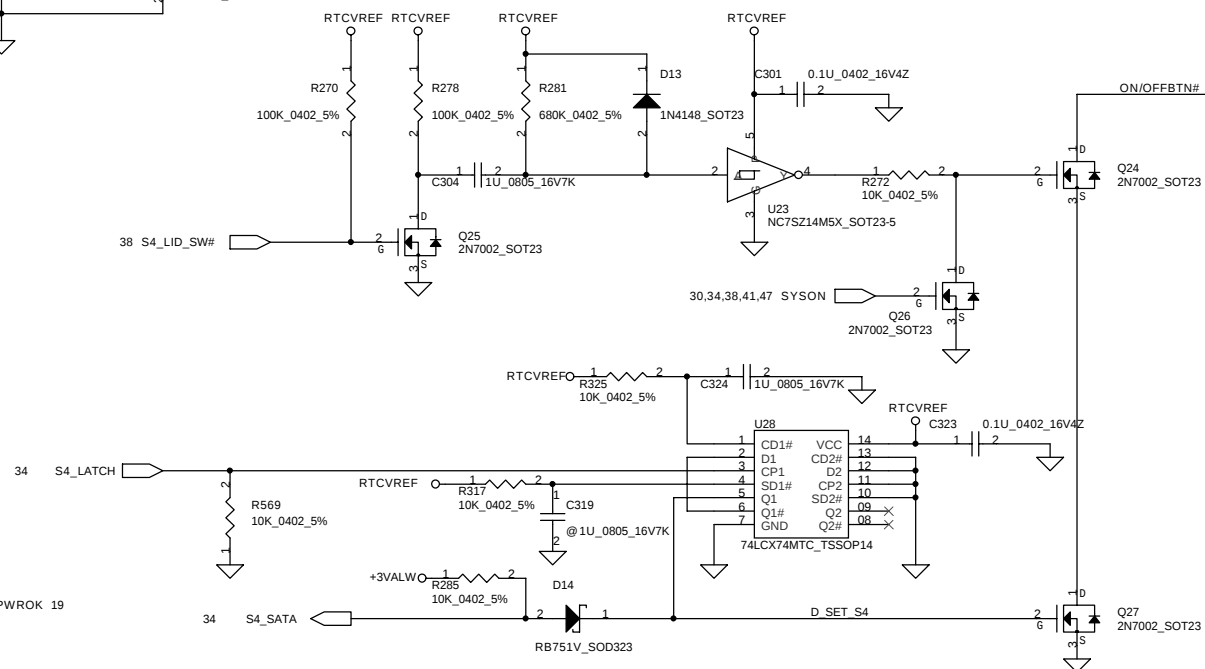
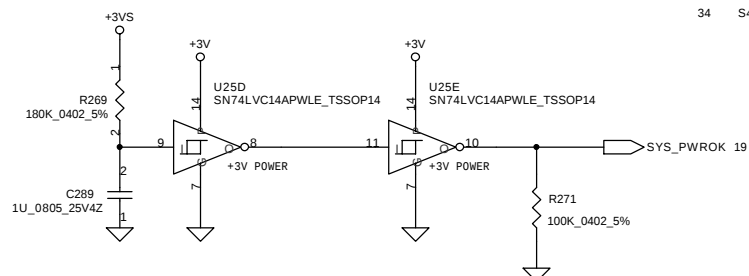
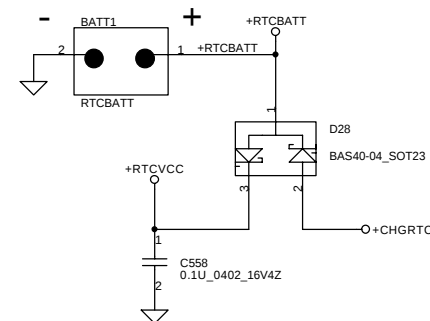
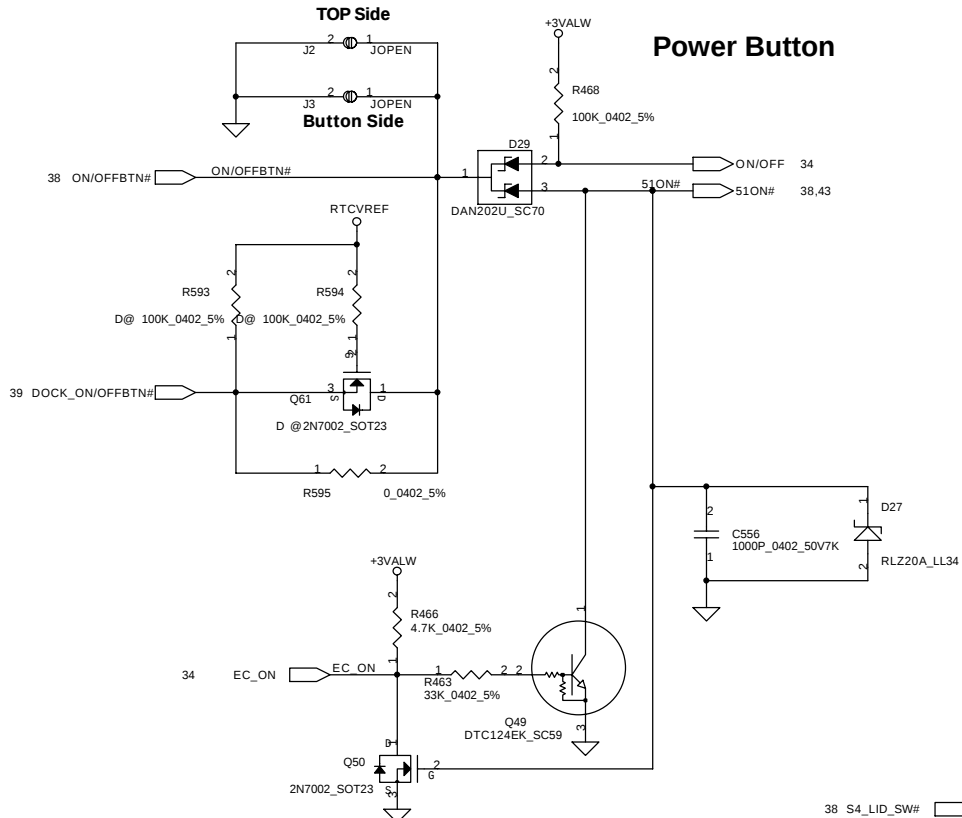
MDC2 TIP

ACES 85205-0400

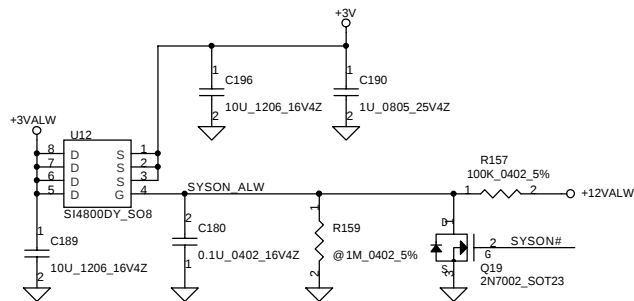


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Size	Document Number		Rev B
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Date:	~P期一,月03,2005	Sheet	39 of 51

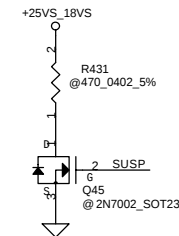
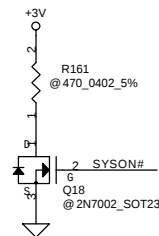
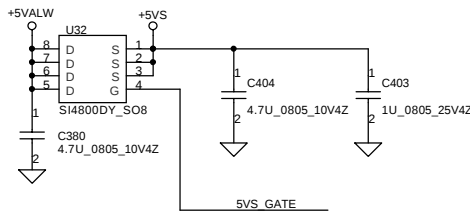
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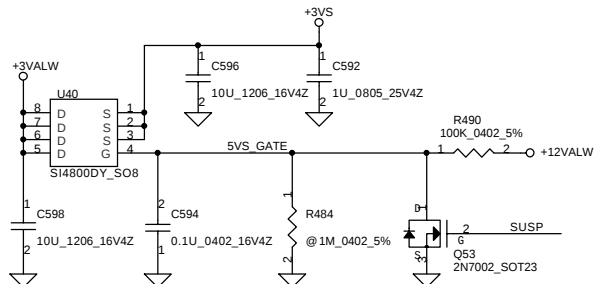
+3VALW TO +3V



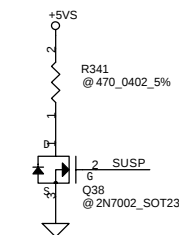
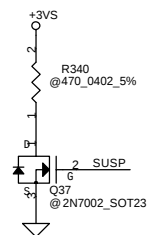
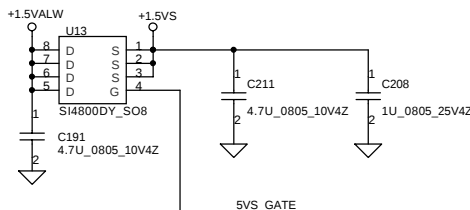
+5VALW TO +5VS



+3VALW TO +3VS

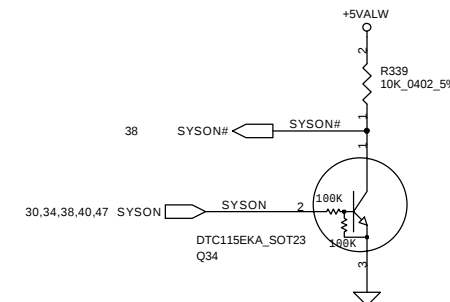
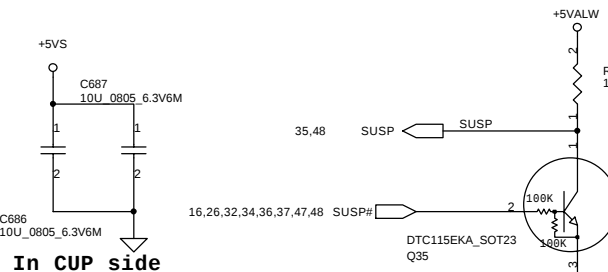
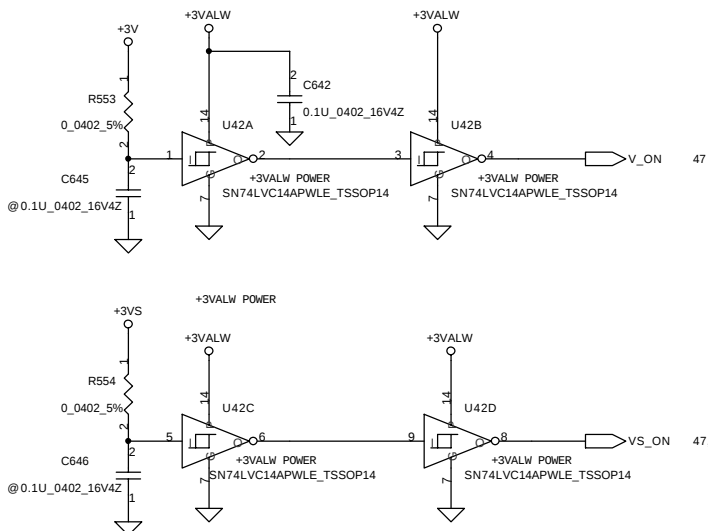
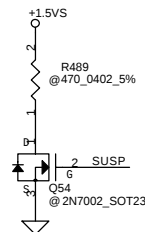
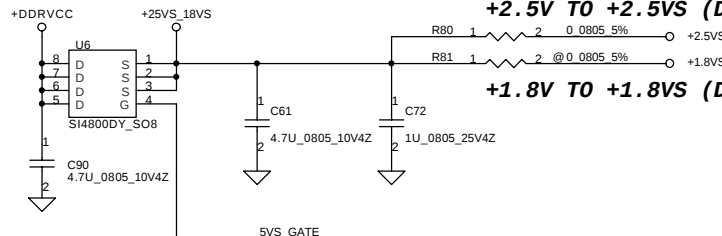


+1.5VALW TO +1.5VS



+2.5V TO +2.5VS (DDR1)

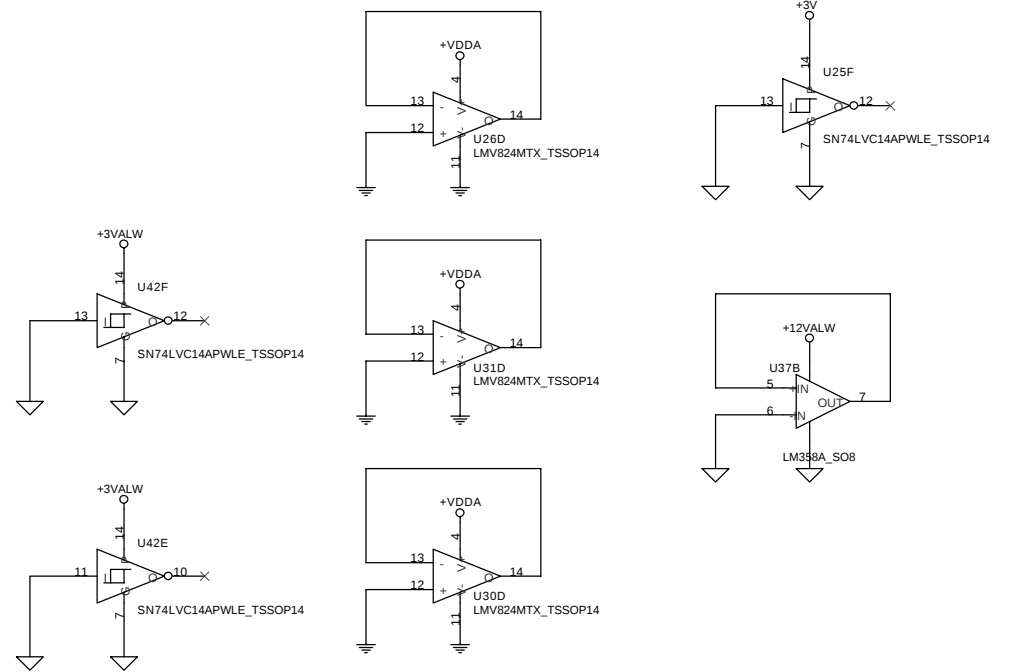
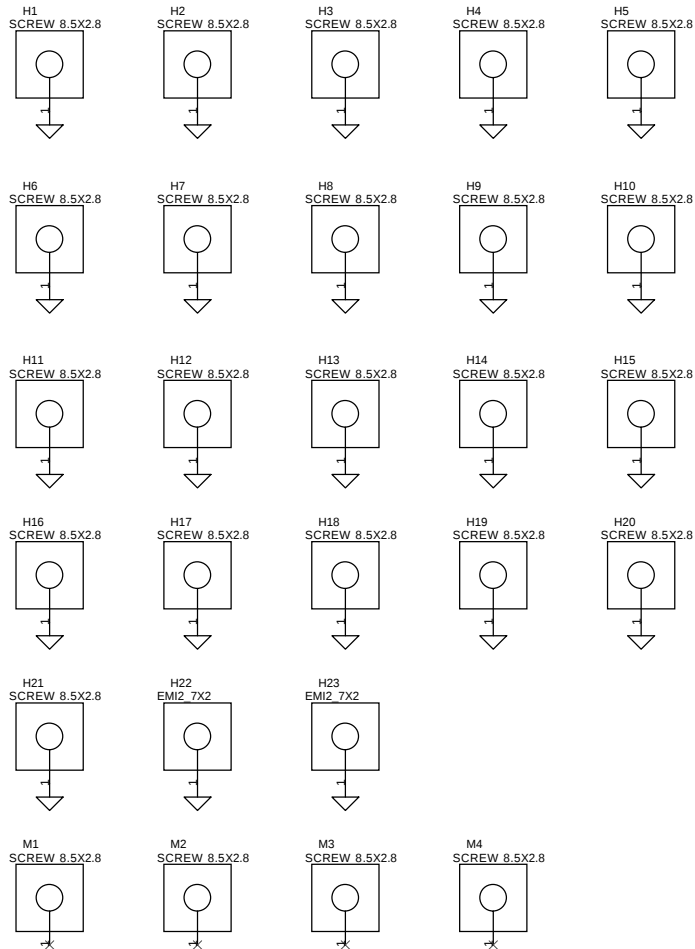
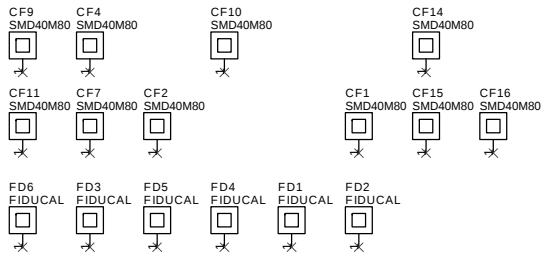
+1.8V TO +1.8VS (DDR2)



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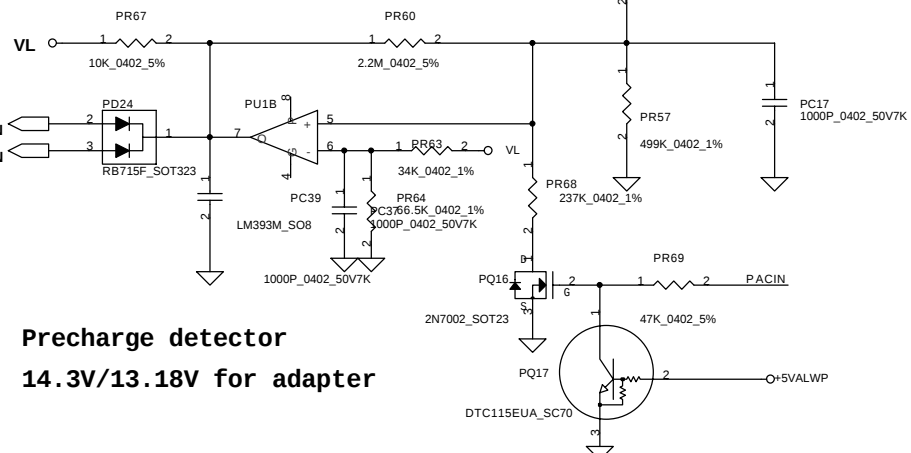
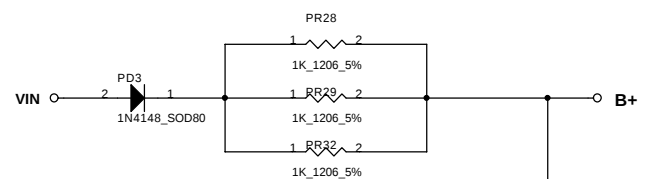
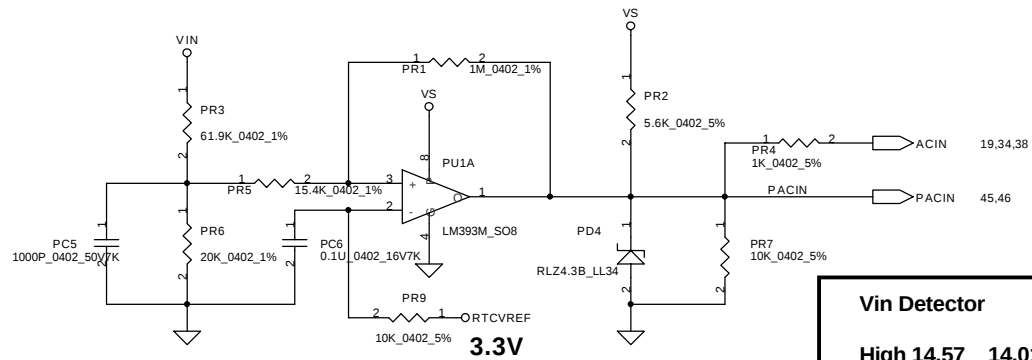
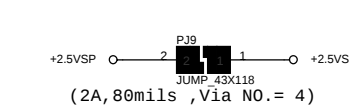
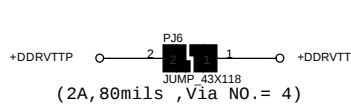
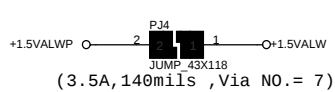
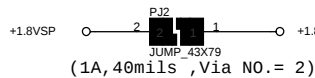
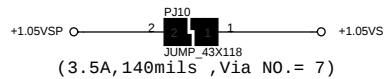
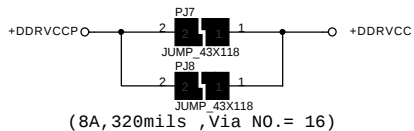
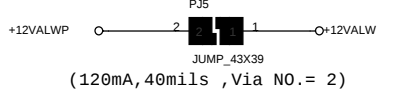
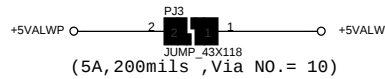
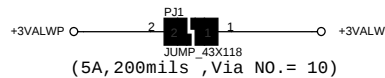
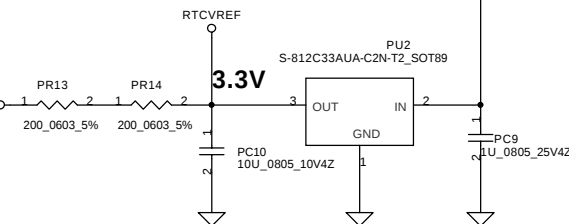
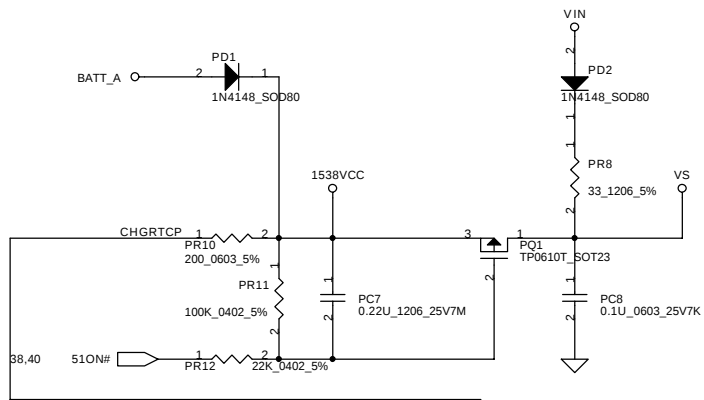
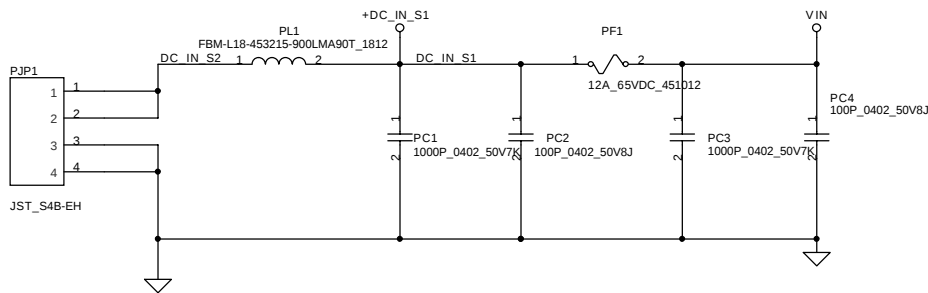
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Title			SCHEMATIC, M/B LA-2492		
Size	Document Number	401317			Rev
B					B
Date:	~P期一, 一月 03, 2005	Sheet	41	of	51



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Title			
SCHEMATIC, M/B LA-2492			
Size	Document Number		Rev
	401317		B
Date:	~P 期一, 一月 03, 2005		Sheet 42 of 51

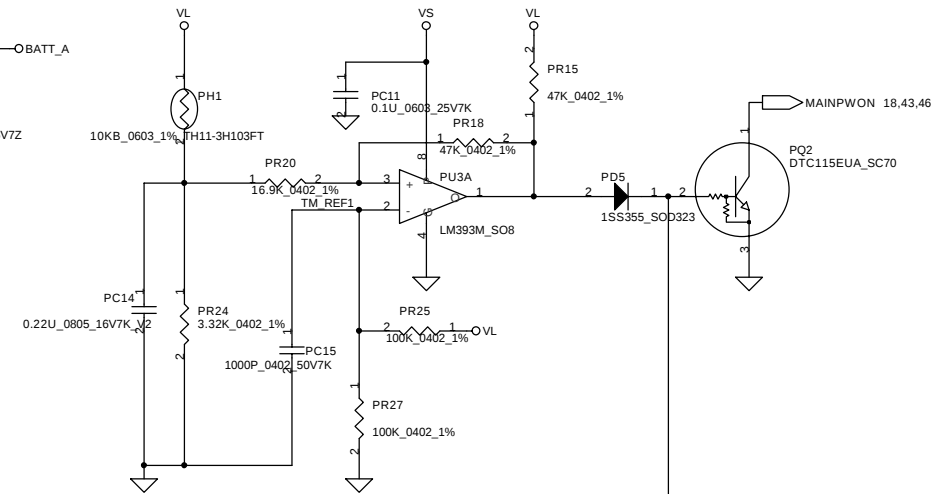
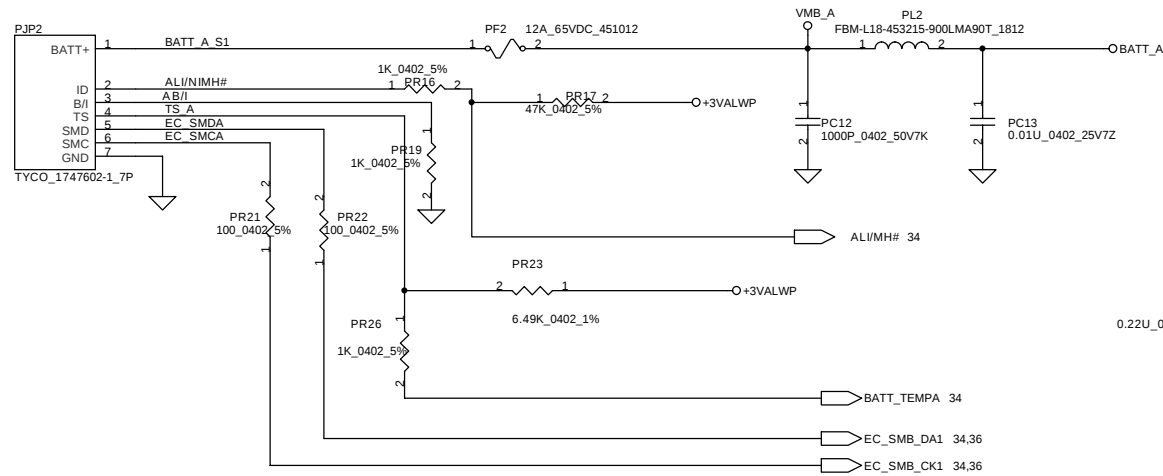


Precharge detector
14.3V/13.18V for adapter

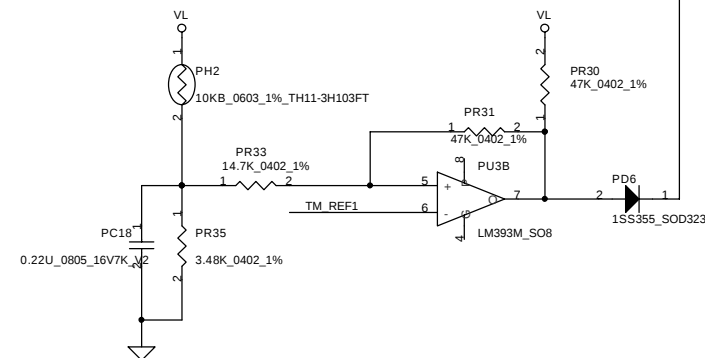
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Title			
SCHEMATIC, M/BLA-2492			
Size	Document Number		Rev
	401317		B
Date:	~P圖一, 一月 03, 2005		Sheet 43 of 51

PH1 under CPU botten side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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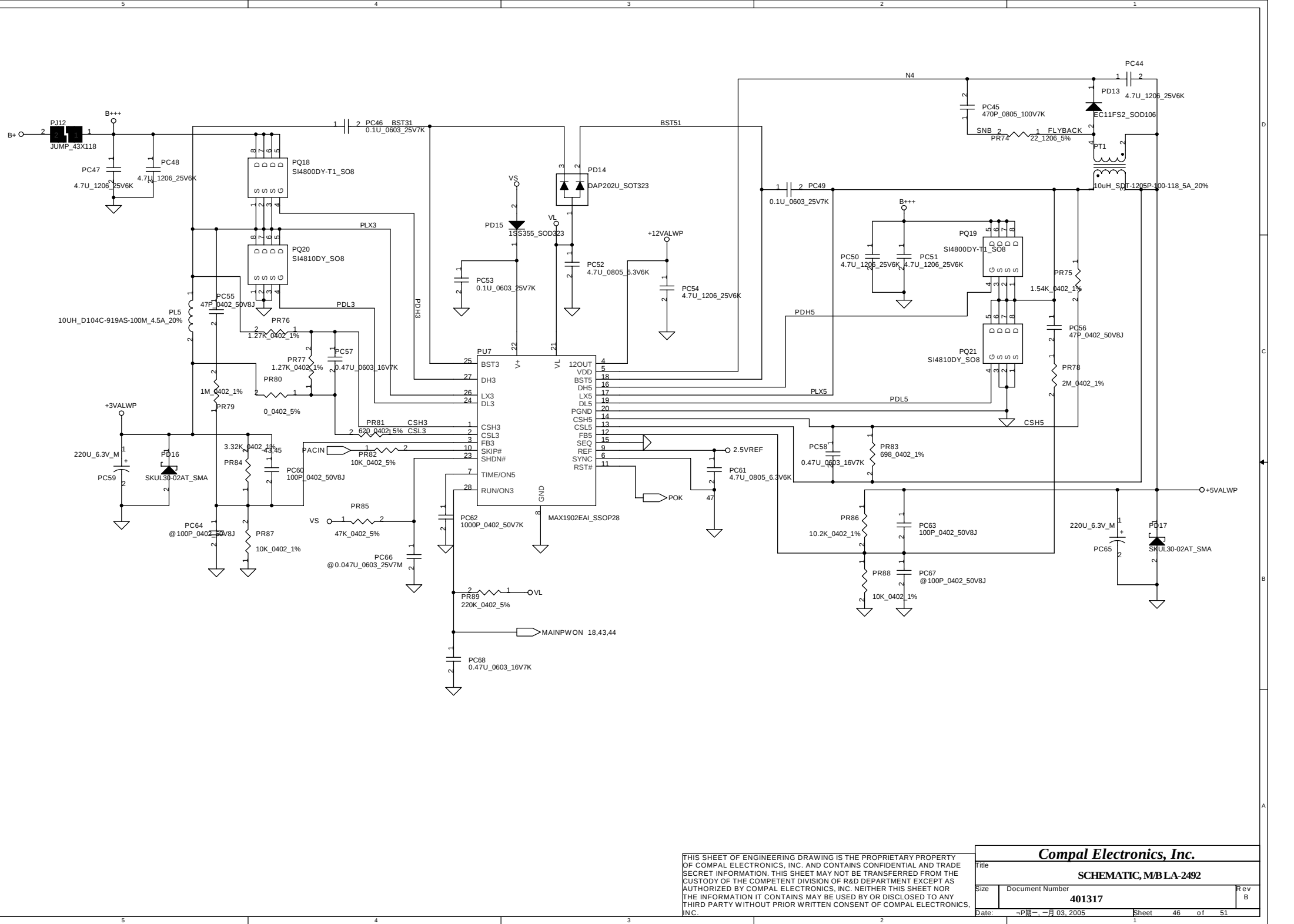
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Size	Document Number
	401317

Rev
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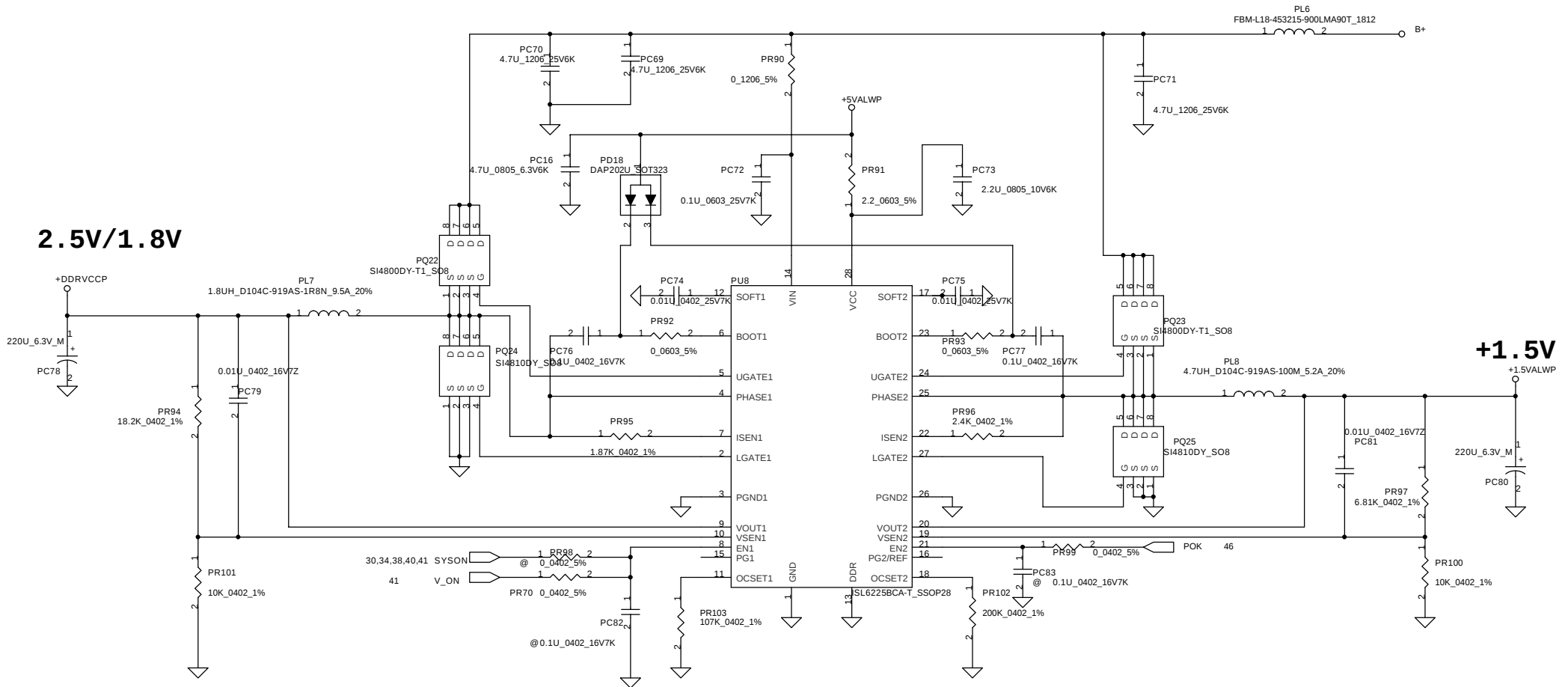
Date:	星期二, 一月 03, 2005	Sheet	44	of	51
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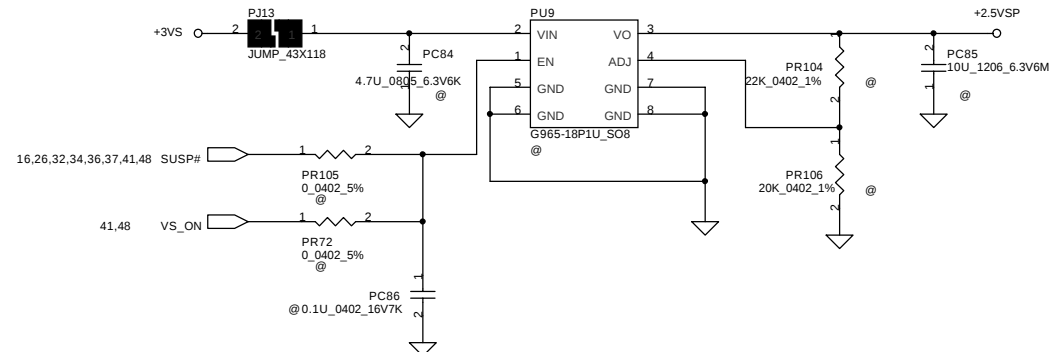
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Title			
SCHEMATIC, M/BLA-2492			
Size	Document Number		Rev
	401317		B
Date:	~P 周一, 一月 03, 2005		Sheet 46 of 51

2.5V/1.8V

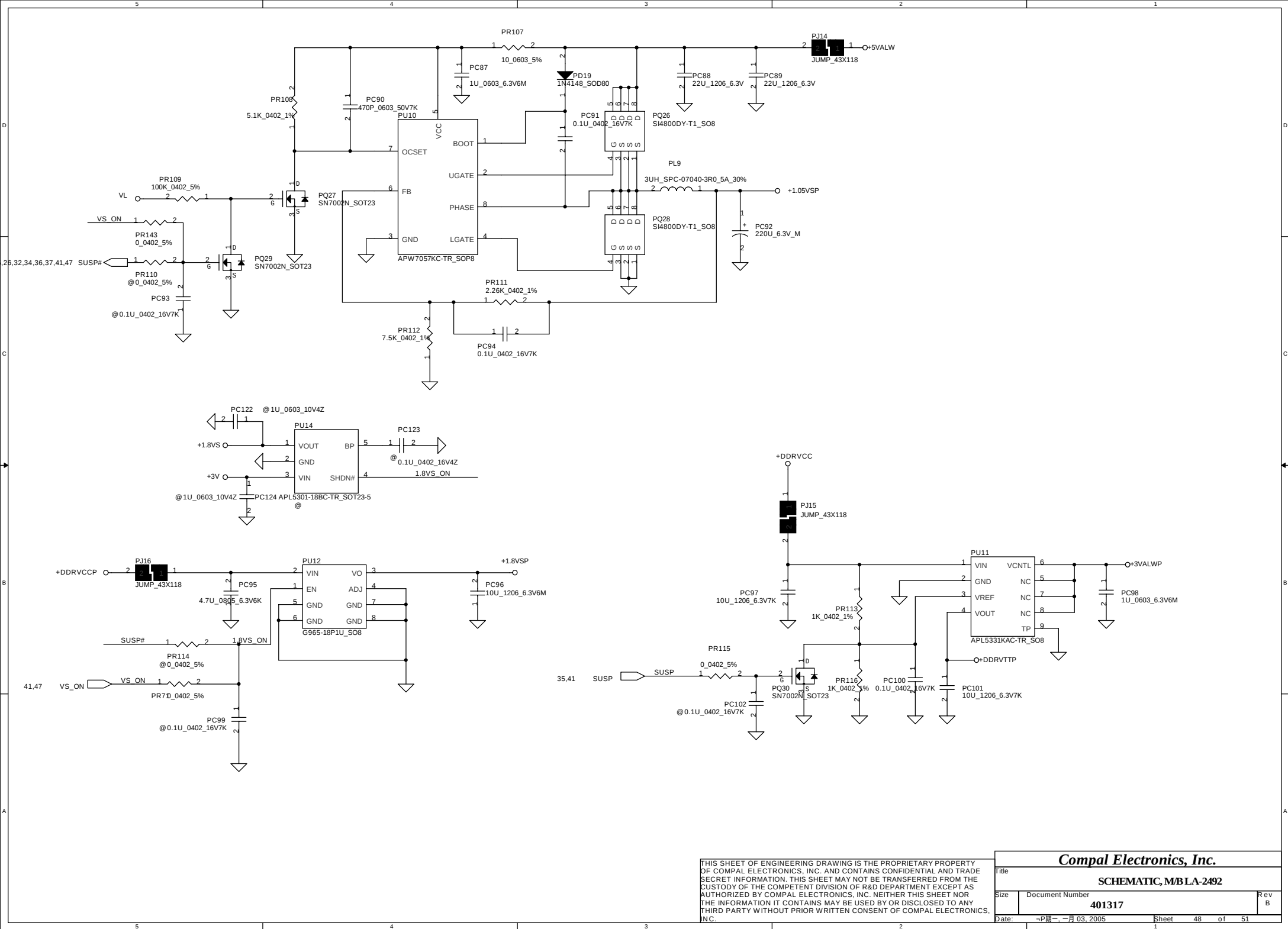


	PR94	UNPOP
DDRI	18.2K_0402_1% (2.5V)	PU9, PC84, PR105, PR104, PR106, PC85
DDRII	10K_0402_1% (1.8V)	PU12, PC95, PR114, PC96



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Title			
SCHEMATIC, M/BLA-2492			
Size	Document Number		Rev
	401317		B
Date:	~P版一、一月 03, 2005		Sheet 47 of 51



EAT10 PIR List

***** Rev:0.2 PIR List 2004/10/26 Writer by Sam Tsai *****

P04:Add @ in R28	Intel Recommend
P06:Add @ in C441, C427 D12,D9 C460 Change Value from 220U to 330U	Power Team testing OK
P12:+3VS change from JP25.196 to JP25.194	Intel Recommend
P15:New add R570, R571 & R572 New add L33 Del D2 & D25	RGB without Docking EMI EMI
P16:Change U44 from 7404 to 74125	LCDVDD Soft-Start
P18:New add R573 R439 Change Value from 180K to 20K C271 Change Value from 0.1U to 1U	Intel Recommend Intel Recommend Intel Recommend
P20:R214 Change Value from 1K to 10ohm	Intel Recommend
P22:New add @R , @R& Q	SwDJ testing
P24:New add R586 New add @R581	TI Recommend
P25:New add R582, R583, @R584, R585, R588, R589 & @C685	TI Recommend
P27:R73 Change Value from 4.99K to 4.7K	Marvwl1 Recommend
P31:R361 & R371 Change Value from 47K to 22K	Design Change
P33:New add R543, R544 P32:Modify C399 Net to SPKL+	Design Change
P33:New add L34 add@ in C647 ~ C662	EMI
P34:New add R587	Design Change
P35:New add JP32 & C671 New add C682 ~ C684 JP13 reverse	Design Change EMI Design Change
P36:New add	SwDJ testing
P37:Sw1 change to 1BS003-1211L_3P	Design Change
P38:Q52.3 change from +3VALW to +3V Q57.3 change from +5VALW to +5VS Lid Switch IC Power change from JP16.26 +3VALW to JP16.27 New add C672 ~ C681	Design Change RTCVREF EMI
P39:New add R574	Design Change
P40:Del D11	Design Change

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Title		SCHEMATIC, M/B LA-2492	
Size	Document Number		Rev
	401317		B
Date:	~P期一, 一月 03, 2005		Sheet 50 of 51

Version Change List (P. I. R. List) for Power Circuit

[illegible]

Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-2492			
Size	Document Number		Rev B
	401317		
Date:	星期二, 一月 03, 2005	Sheet	51 of 51

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