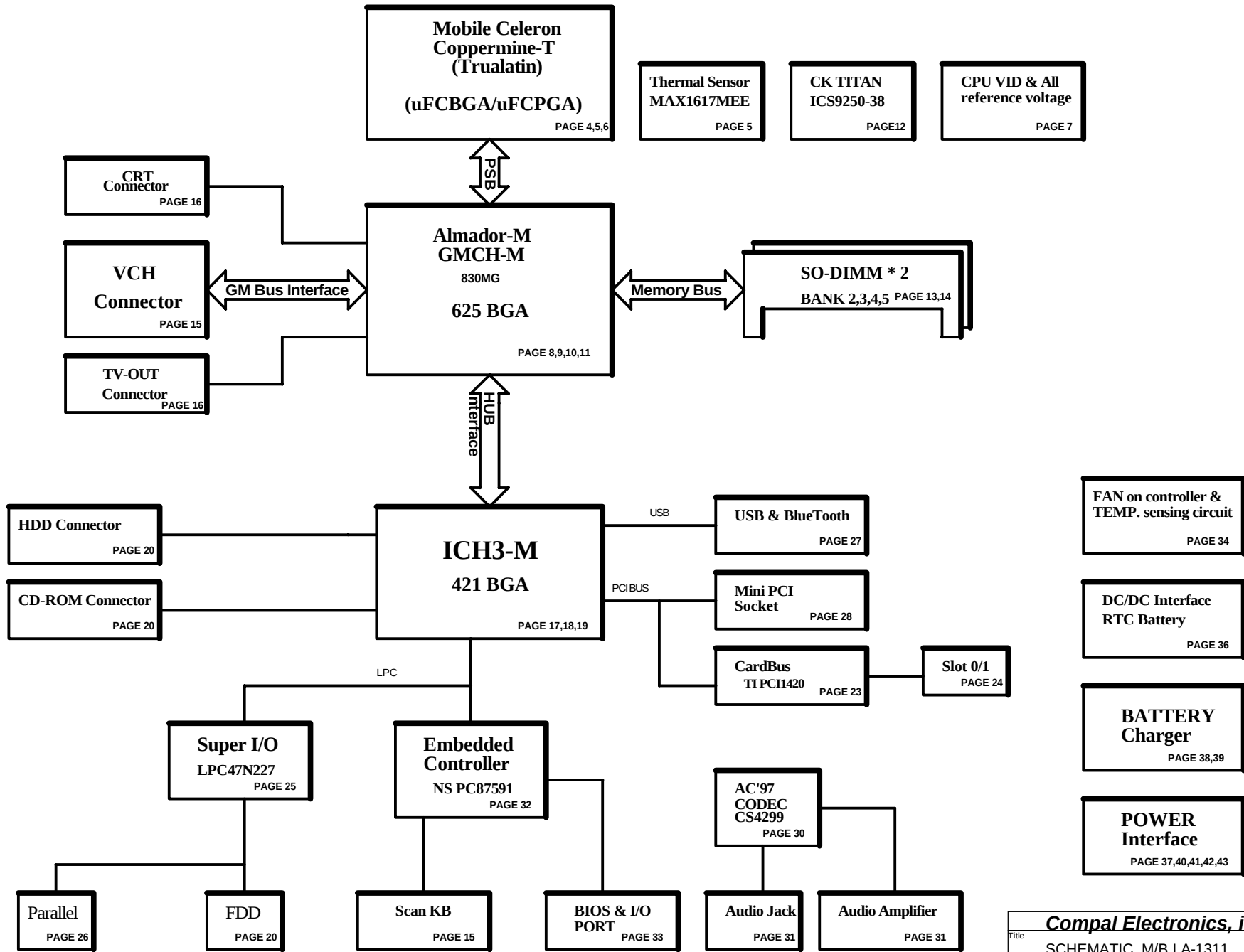


Model Name : ATW02

BLOCK DIAGRAM

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16(02)	1010 000X b	Smart Battery	0001 011X b
(24C04)	1011 000Xb	Docking	0011 011X b
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

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PIR

REV 0.1

Date	Page	Description
9/26	1	First time modify for remove OZ168

REV 0.2

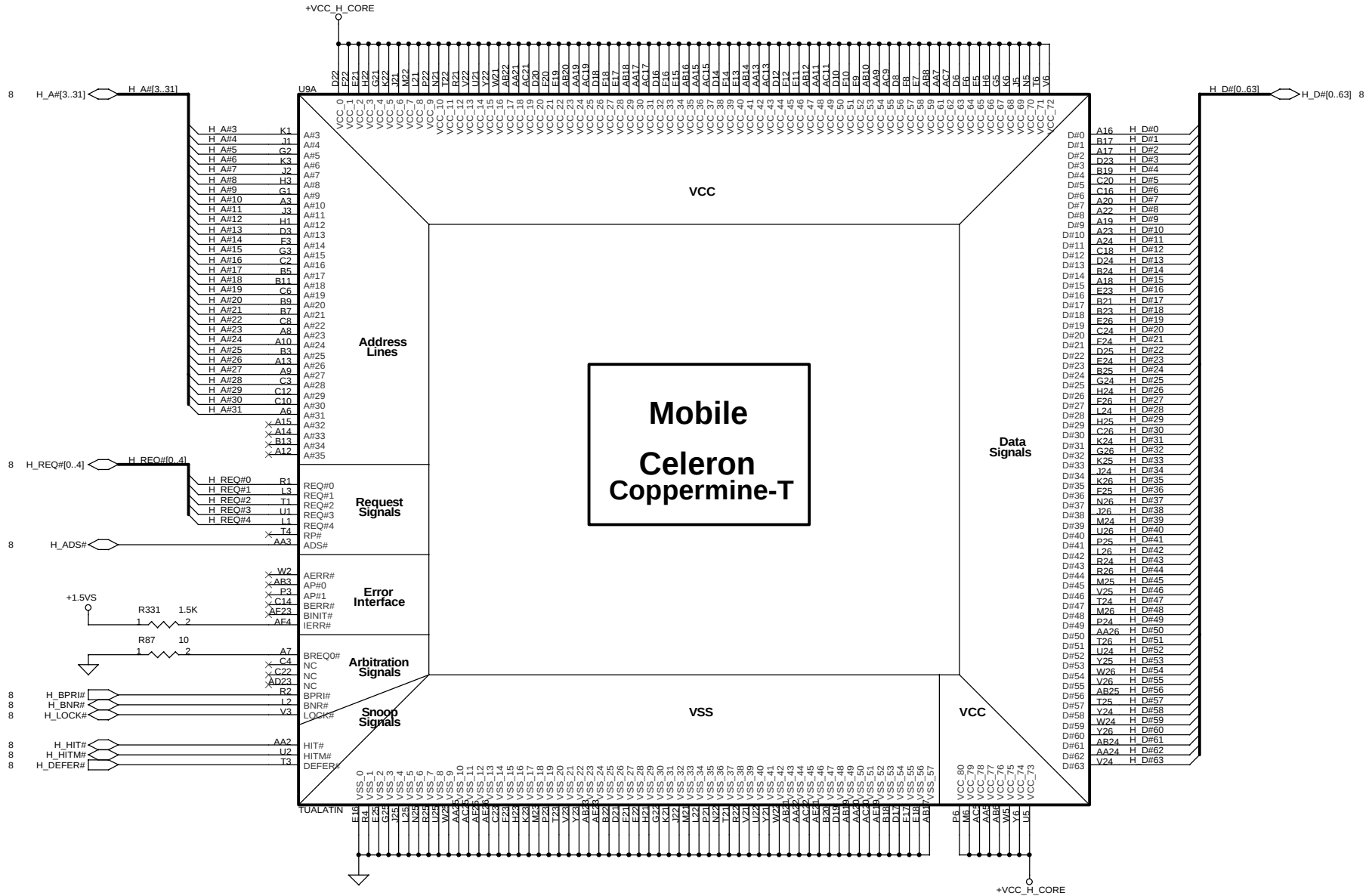
Date	Page	Description
10/23	16	Change R10 R12 R14 to 10Ohm
10/23	10	Change R229 to 255_1% Ohm
10/25	37 to 43	Integrate Power schematic rev0.4
10/29	35	Change H30 H31 H32 H33 H34 H35 H37 H38 Footprint to PAD_3_4X2_2MM
10/30	16	Remove @ on R199 R200 R201
10/30	26	Remove @ on R561
10/30	30	Remove @ on R81
10/30	23	Add @ on R473 C695
10/30	29	Add @ on R536
10/30	7	Add @ on R460 R461 U49
10/30	35	Delete H34
11/01	28	Remove @ on U61
11/01	7	Change R288 to 499_1% R291 to 1K_1%
11/05	12	Change R110 R111 from 330 to 1K
11/22	All	Version update to 1.0

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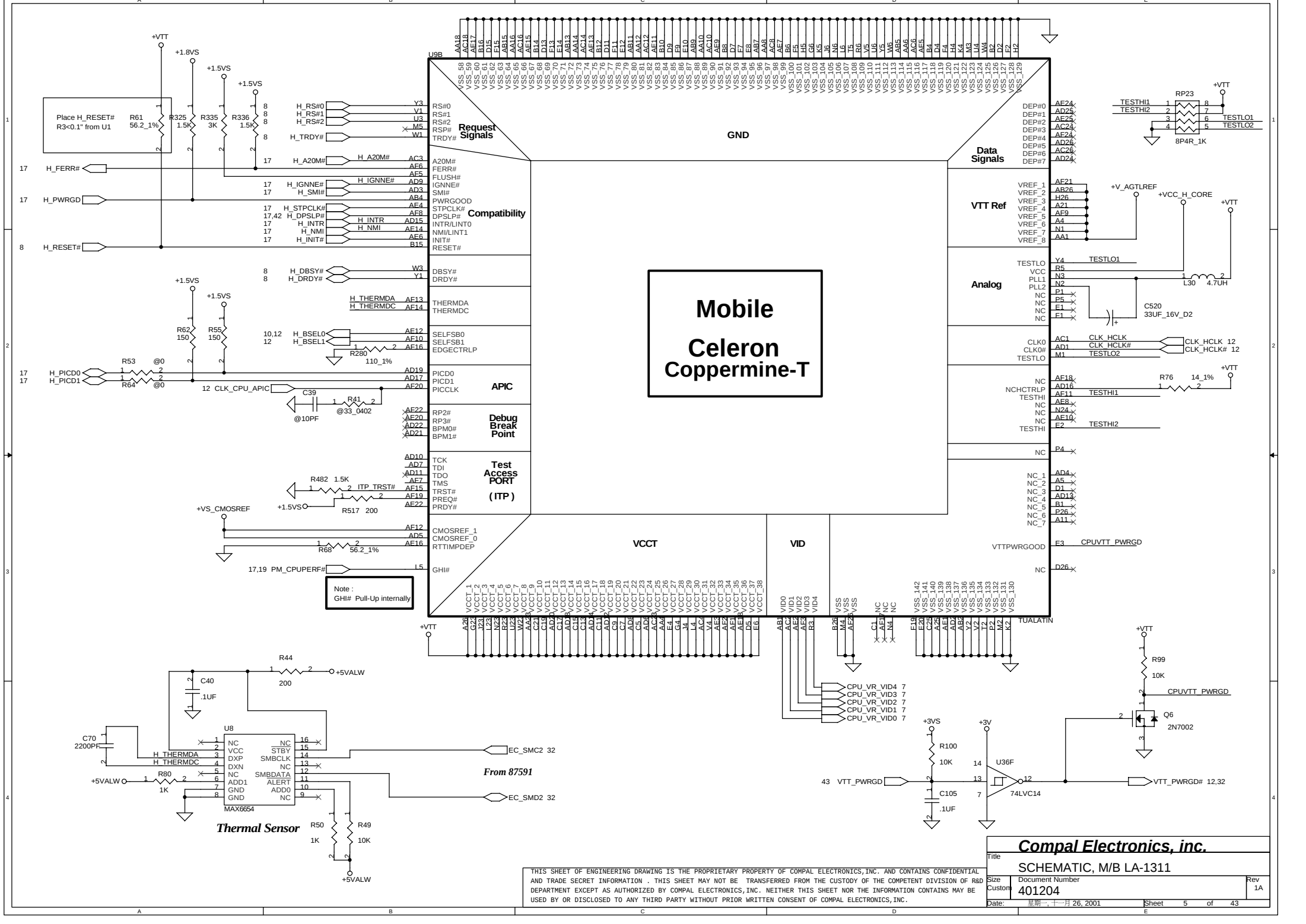
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Mobile
Celeron
Coppermine-T

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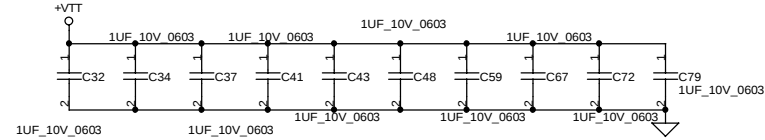
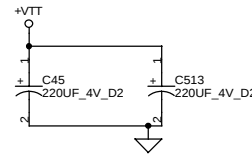
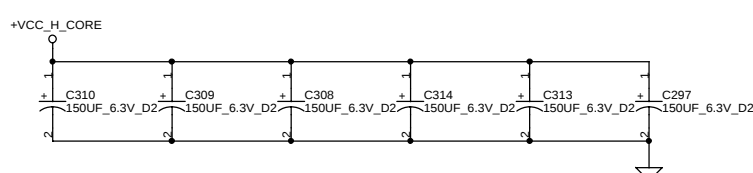
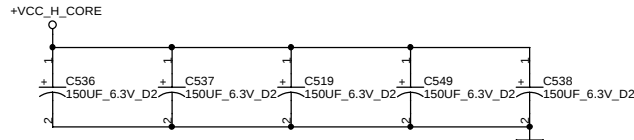
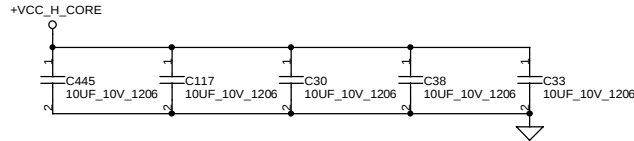
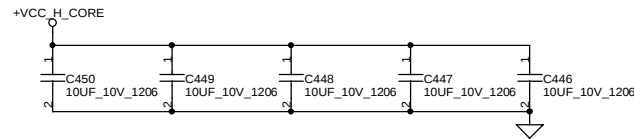
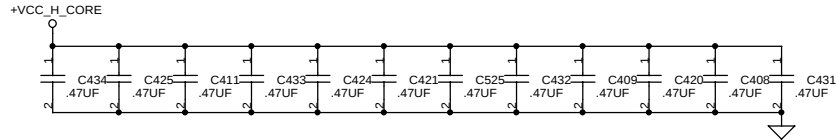
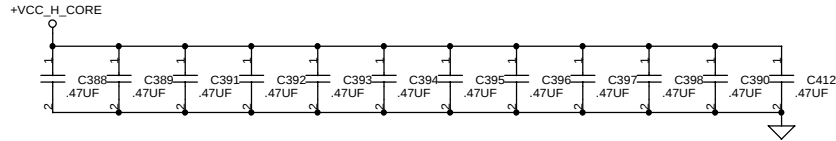
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Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

Layout note :

Place close to CPU,
Use 2 vias per PAD.



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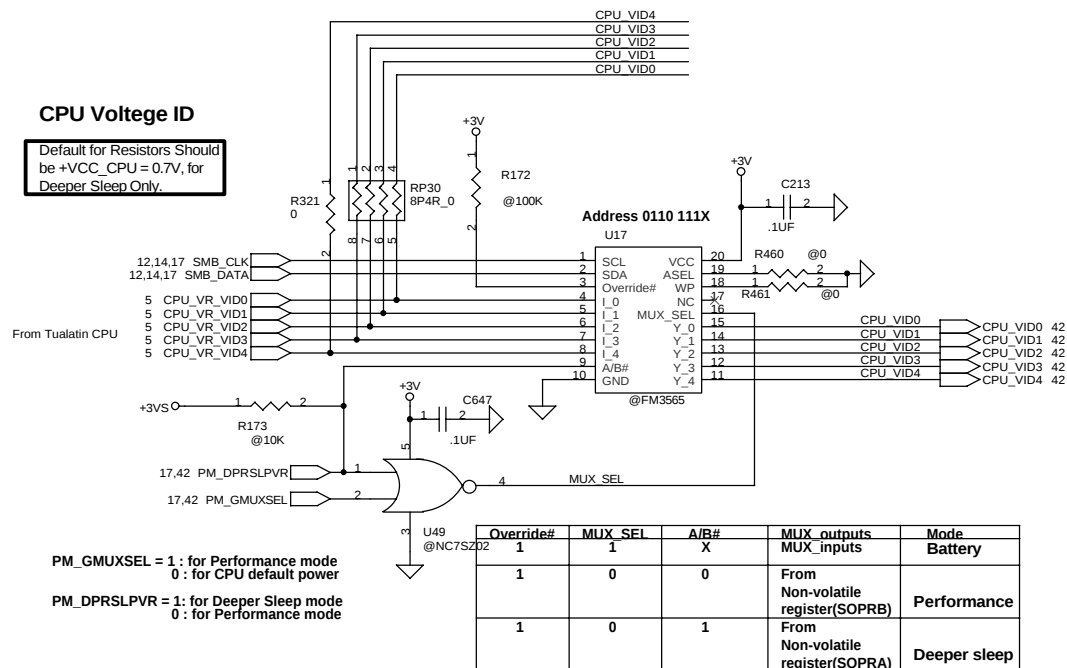
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Mount R321 and RP30 if without support SpeedStep

CPU Voltage ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



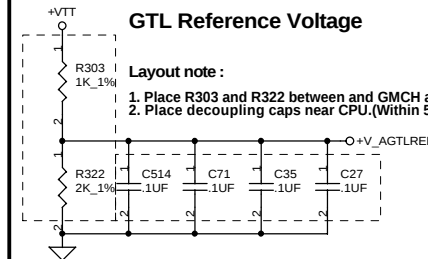
Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

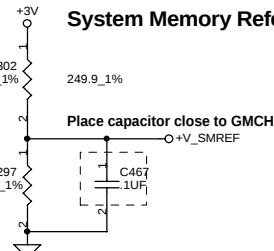
GTL Reference Voltage

Layout note :

1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)



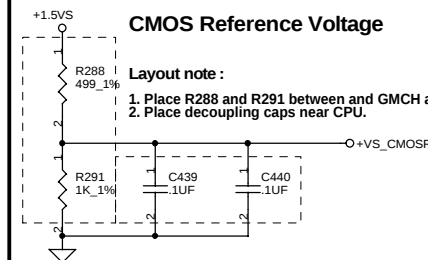
System Memory Reference



CMOS Reference Voltage

Layout note :

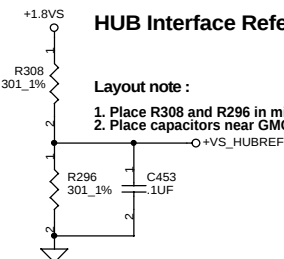
1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.



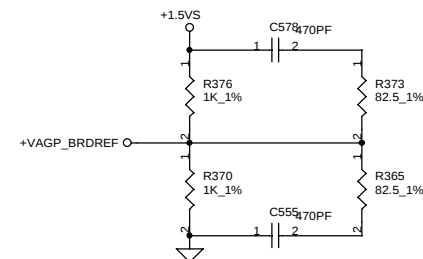
HUB Interface Reference

Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

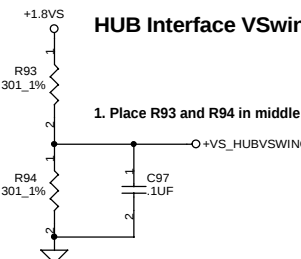


Place Reference Circuit near GMCH

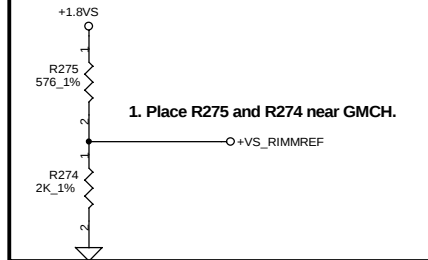


HUB Interface VSing Voltage

1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.



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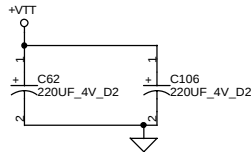
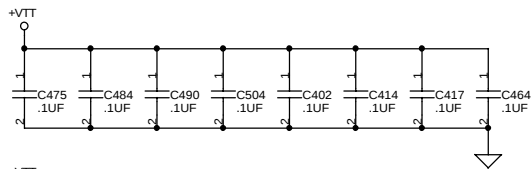
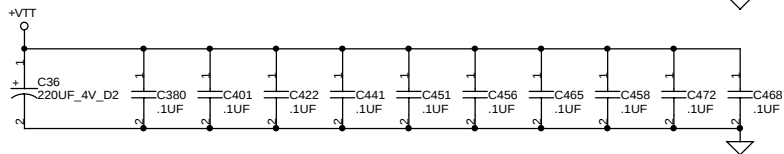
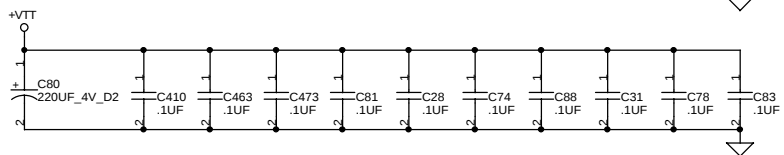
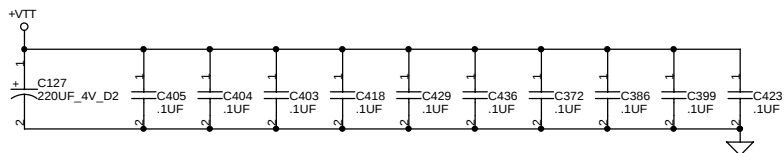
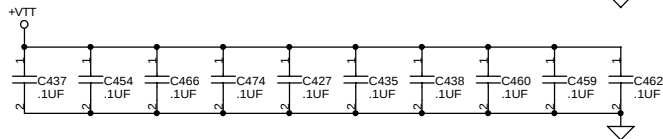
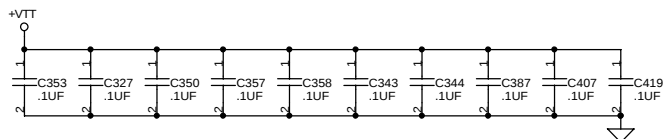
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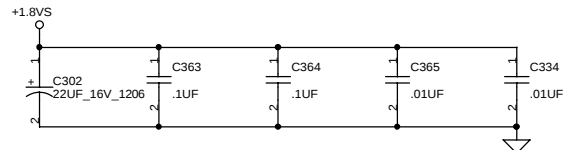
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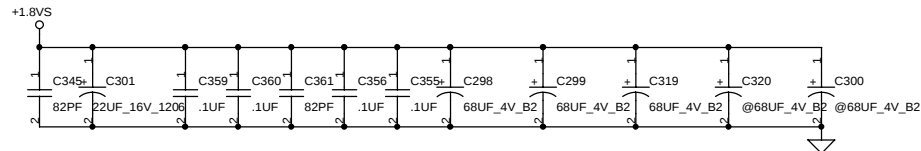
Layout note :
Distribute as close as possible
to GMCH Processor Quadrant .



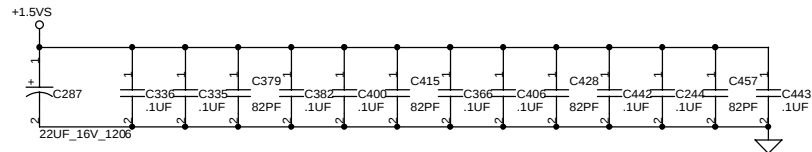
Layout note :
Distribute as close as possible
to VCCPCMOS_LM .



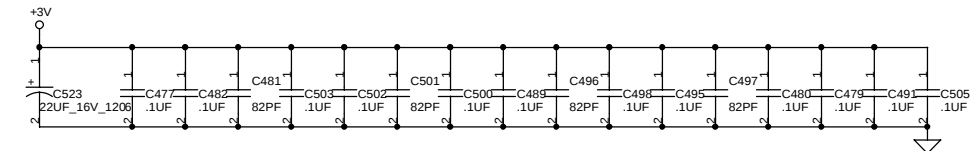
Layout note :
Distribute as close as possible
to GMCH Local Memory Quadrant .



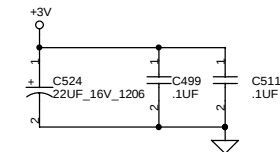
Layout note :
Distribute as close as possible
to GMCH AGP/DVO Quadrant .



Layout note :
Distribute as close as possible
to GMCH System Memory Quadrant .



Layout note :
Distribute as close as possible
to IO Quadrant .



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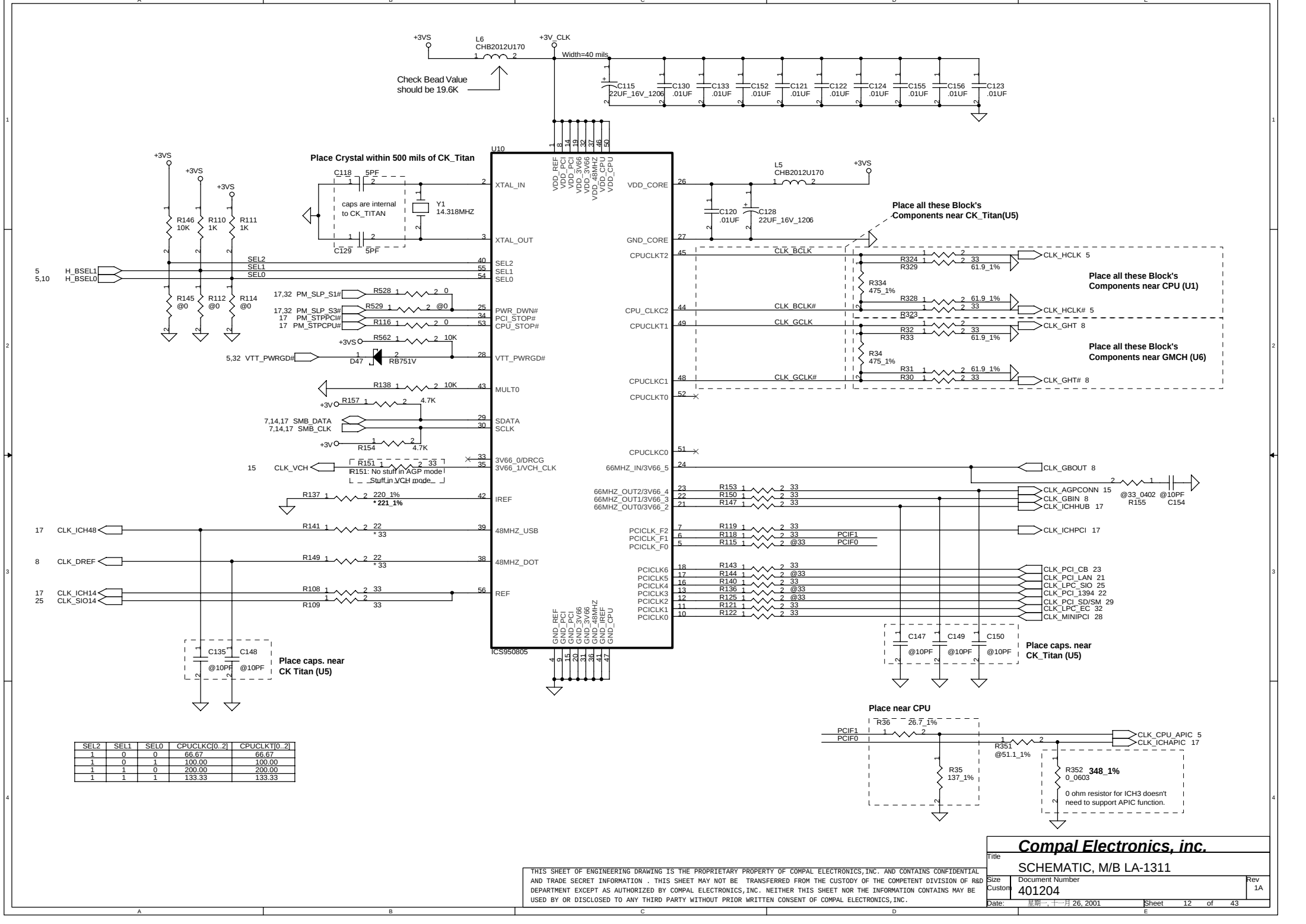
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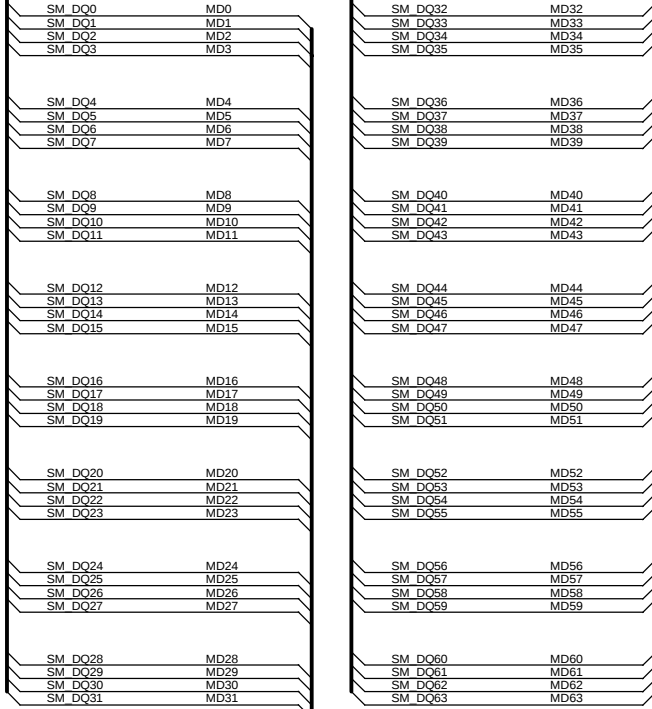


SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

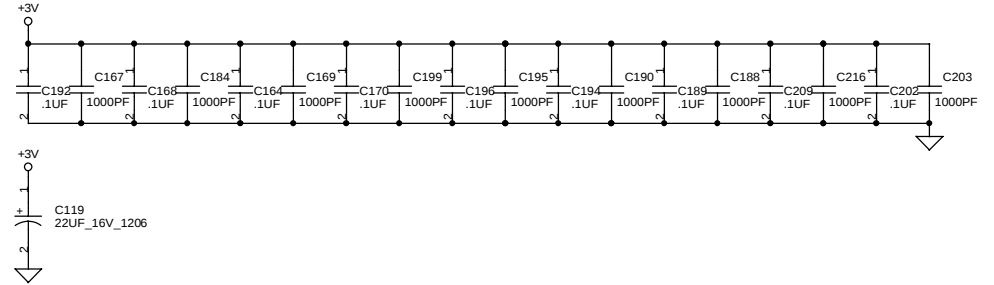
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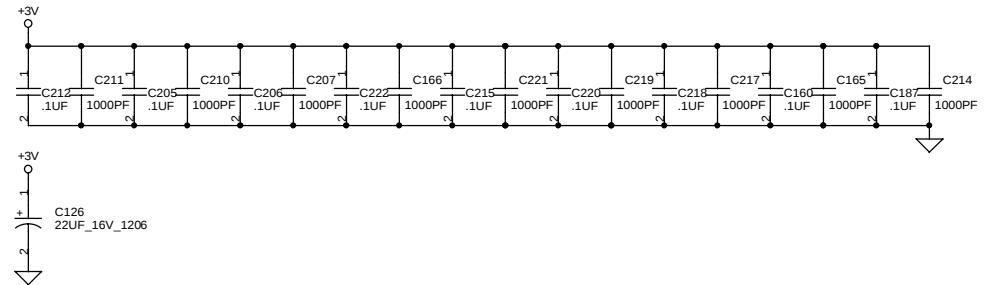
9,14 SM_DQ[0..63] MD[0..63] 9,14



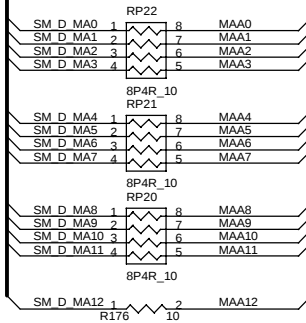
Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .



Layout note :
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



9 SM_D_MA[0..12] MAA[0..12] 14



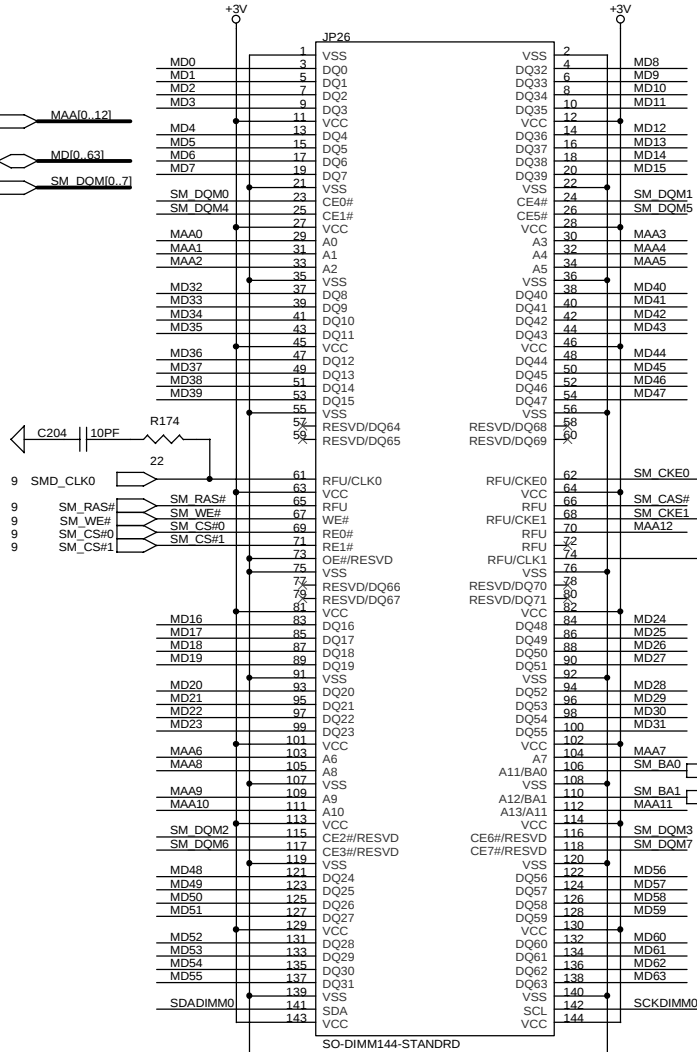
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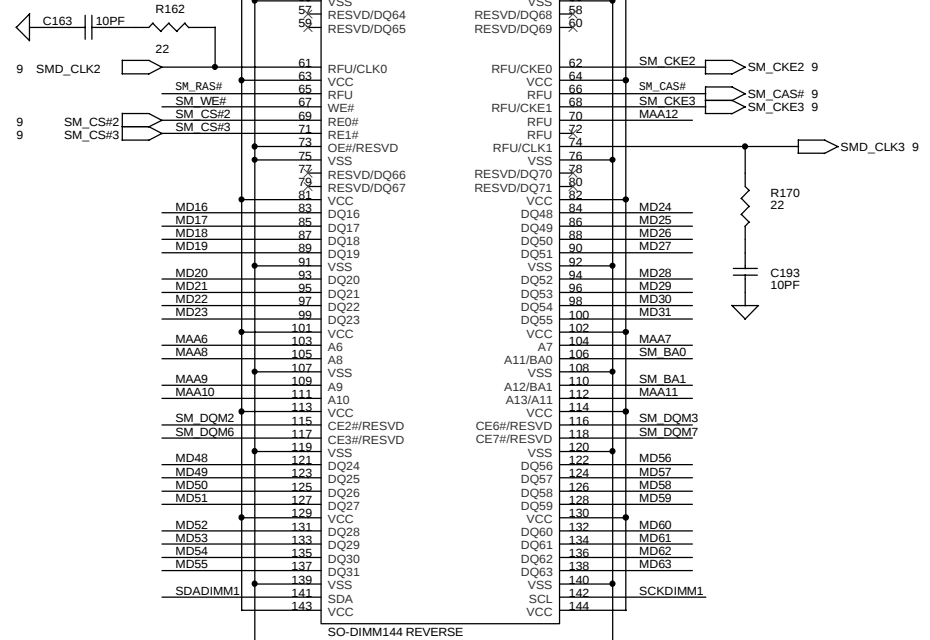
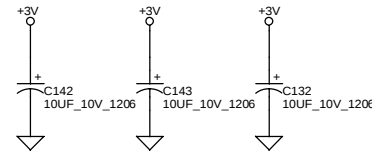
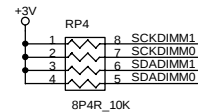
SO-DIMM 144 PINS RAM MODULE CONN. **BANK 0/1**

BANK 2/3

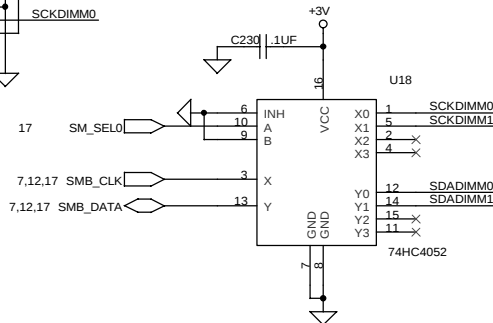
13 MAA[0..12] $\rightarrow$ MAA[0..12]
9 MD[0..63] $\rightarrow$ MD[0..63]
9 SM_DQM[0..7] $\rightarrow$ SM_DQM[0..7]



DIMM0



DIMM1



SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

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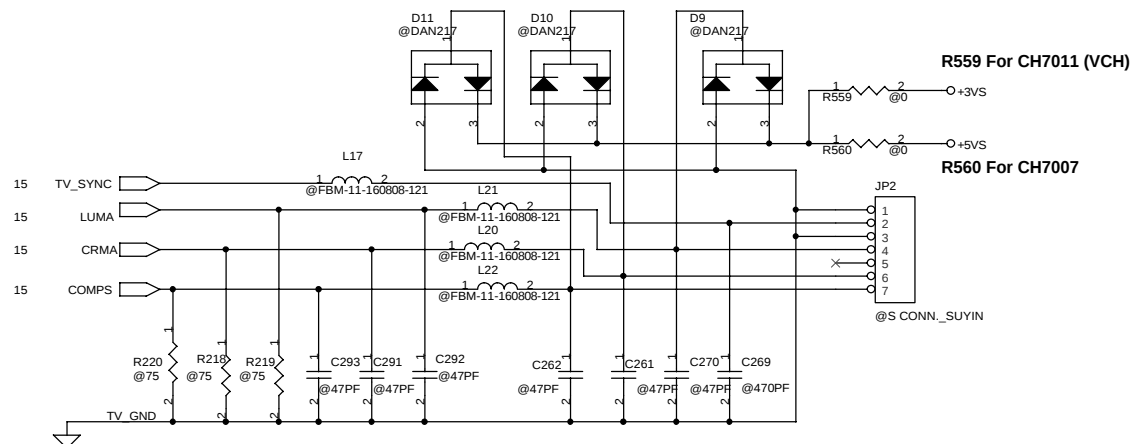
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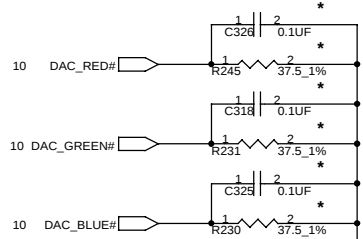
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TV_OUT CONN.

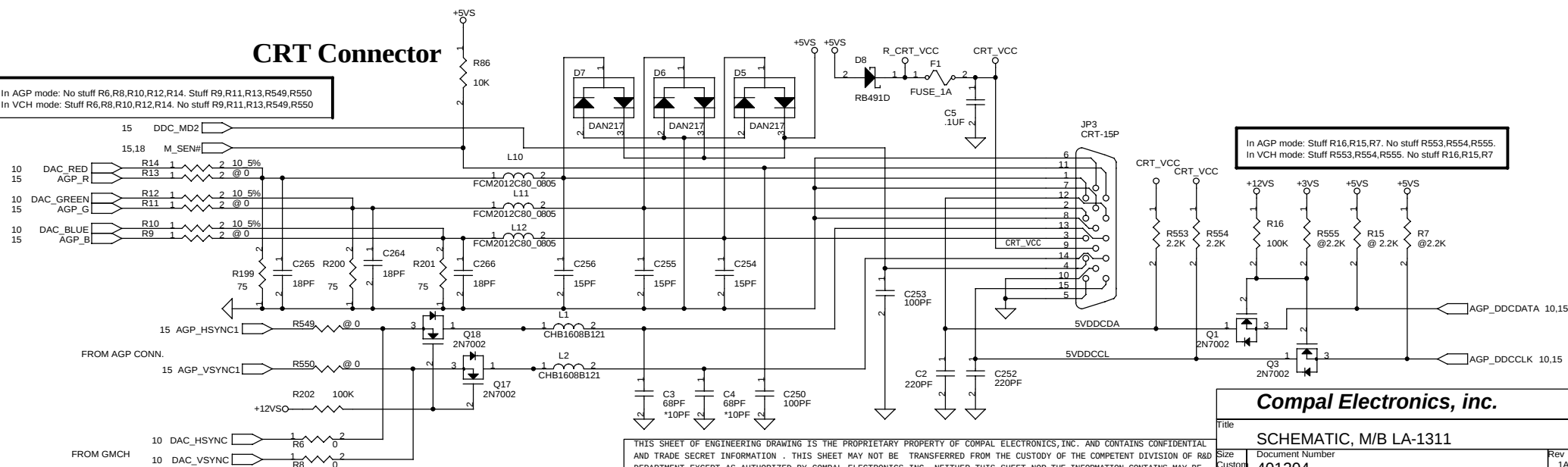


In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550



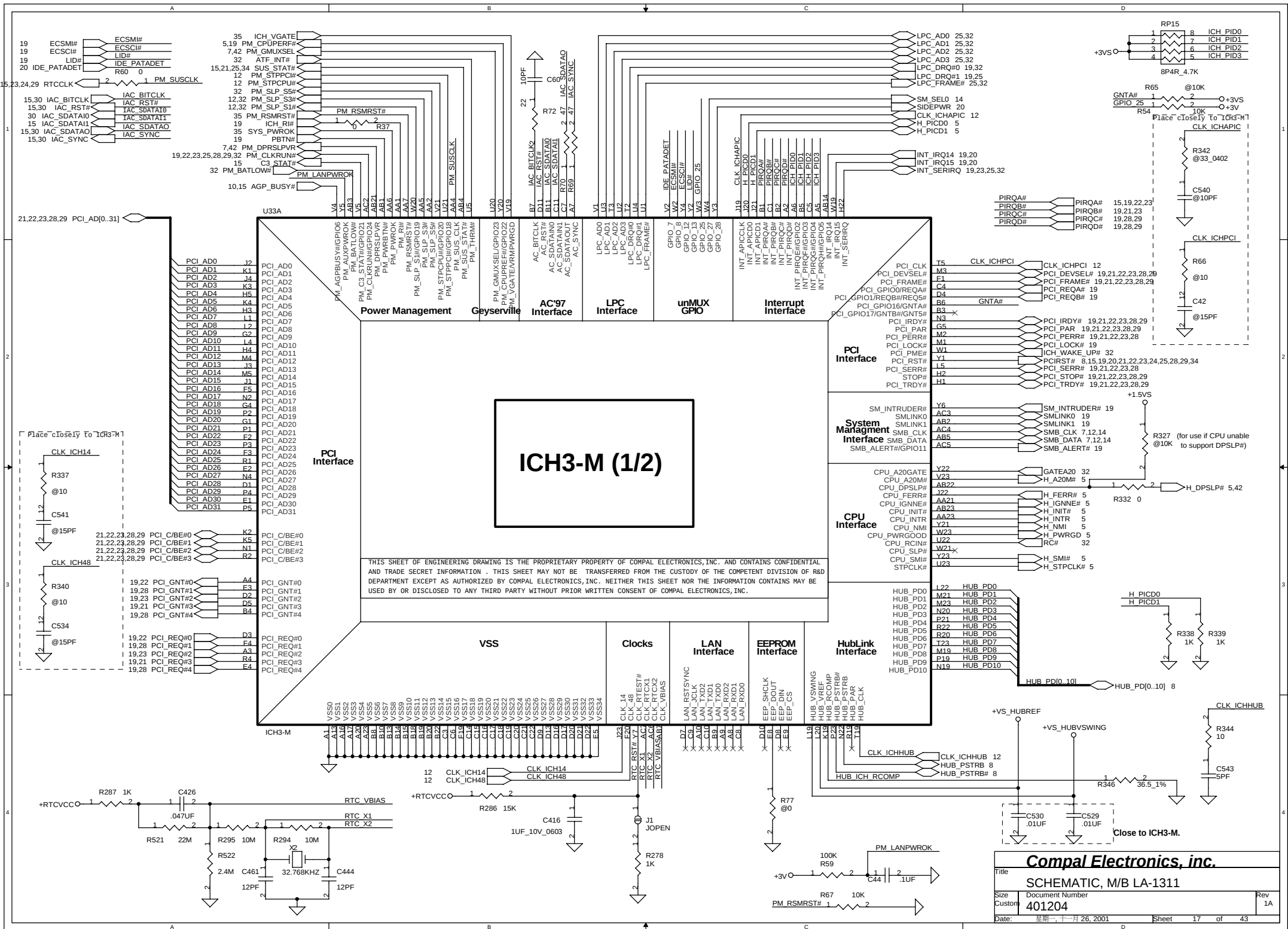
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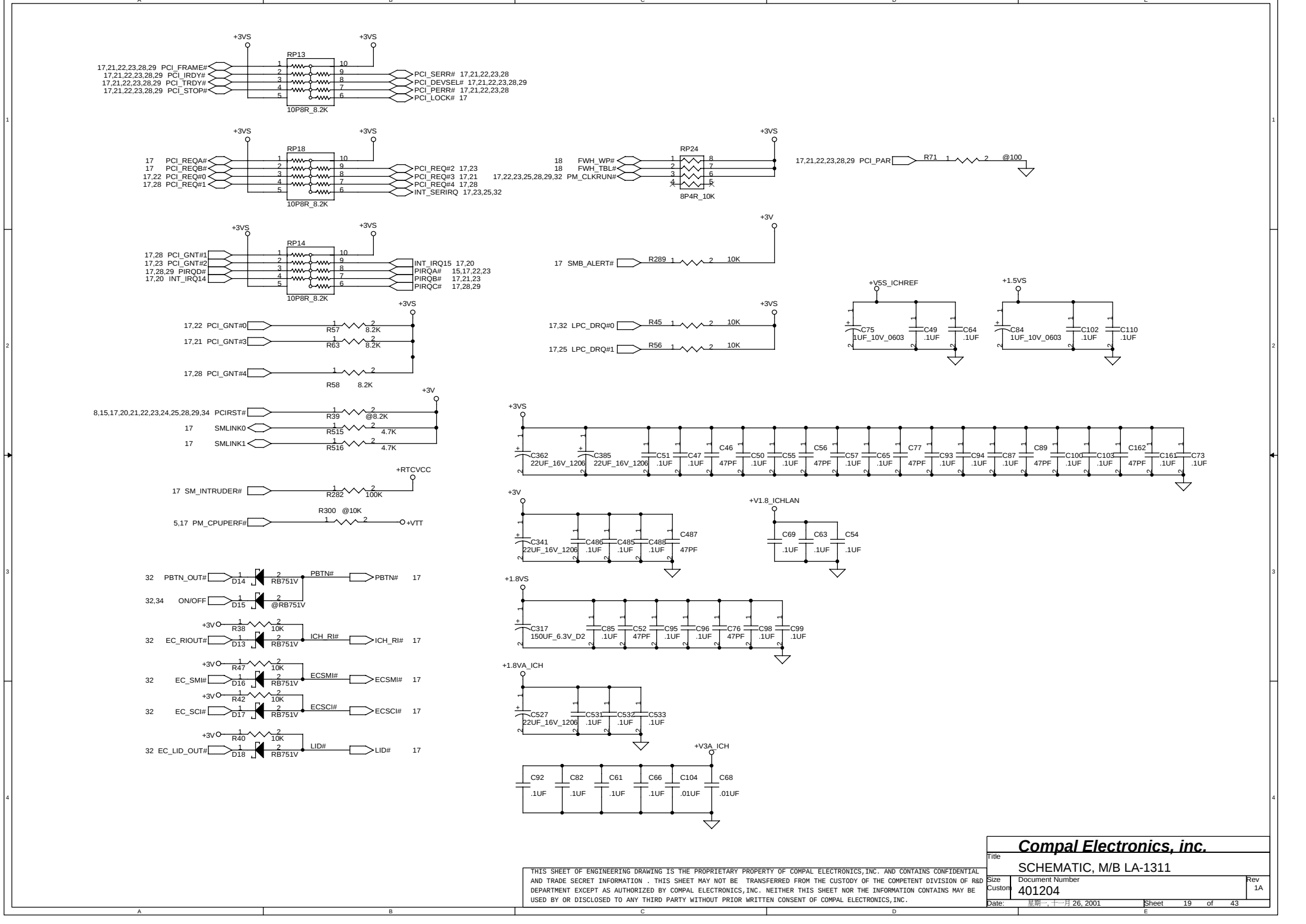
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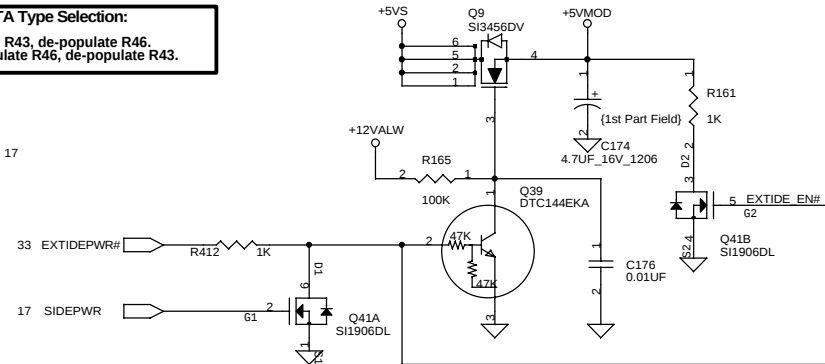
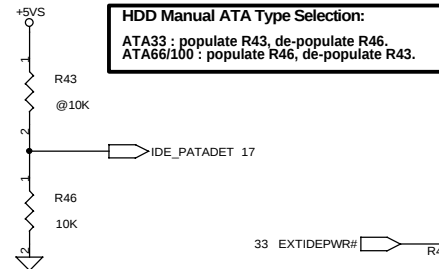
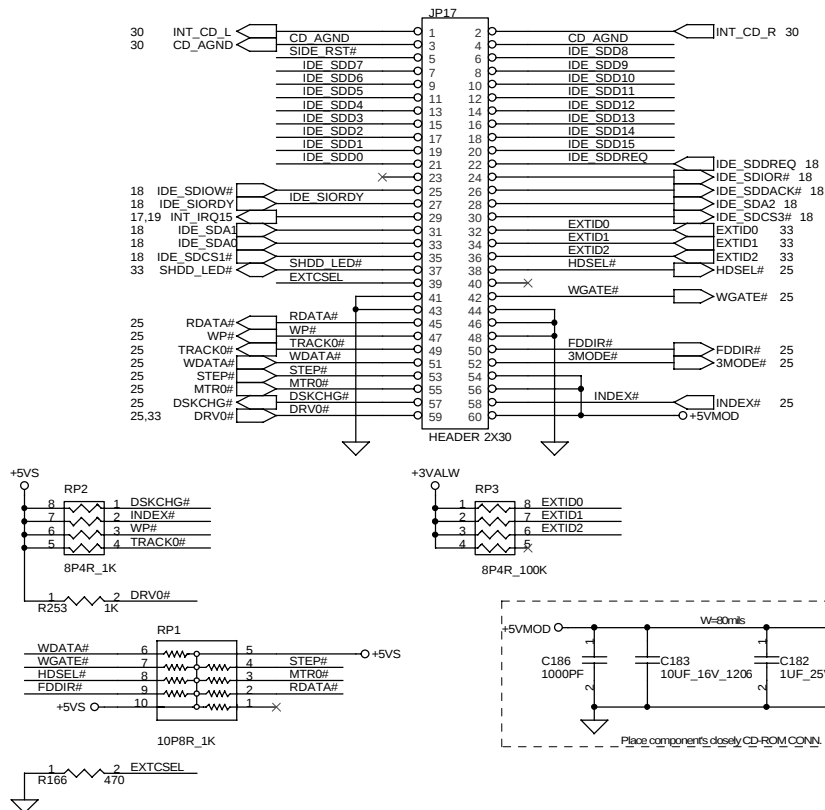
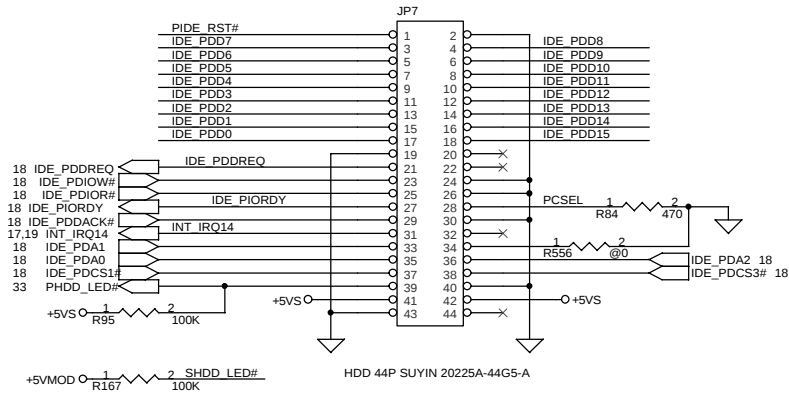
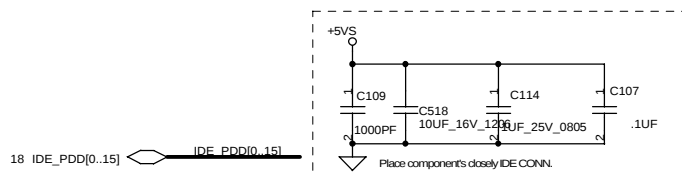
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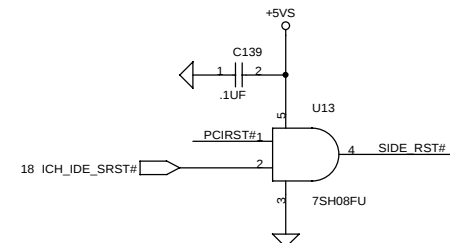
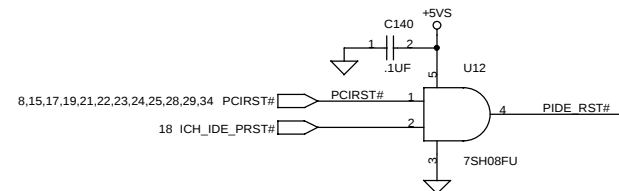
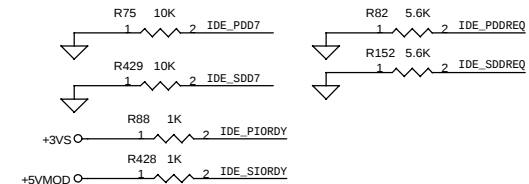




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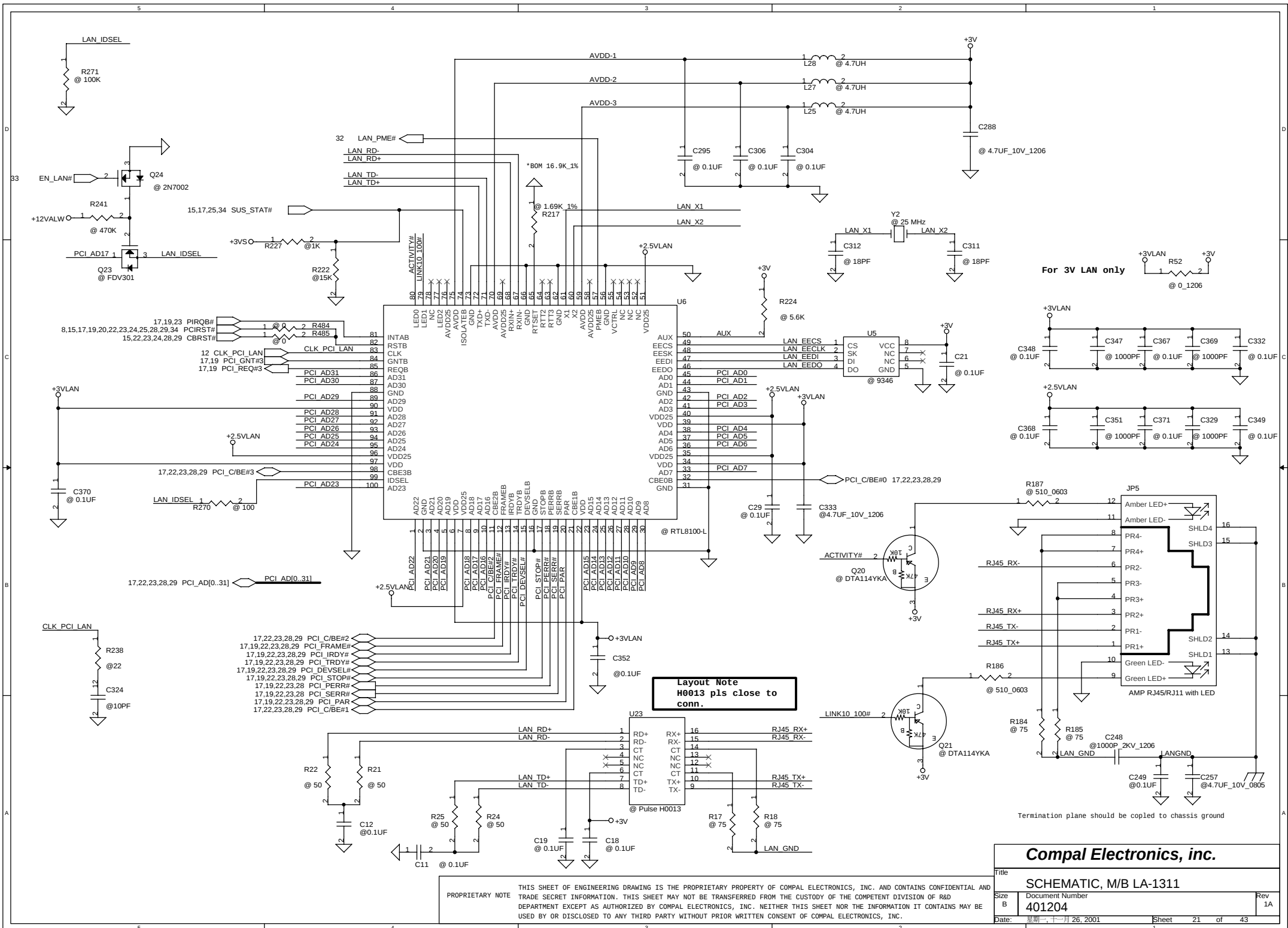


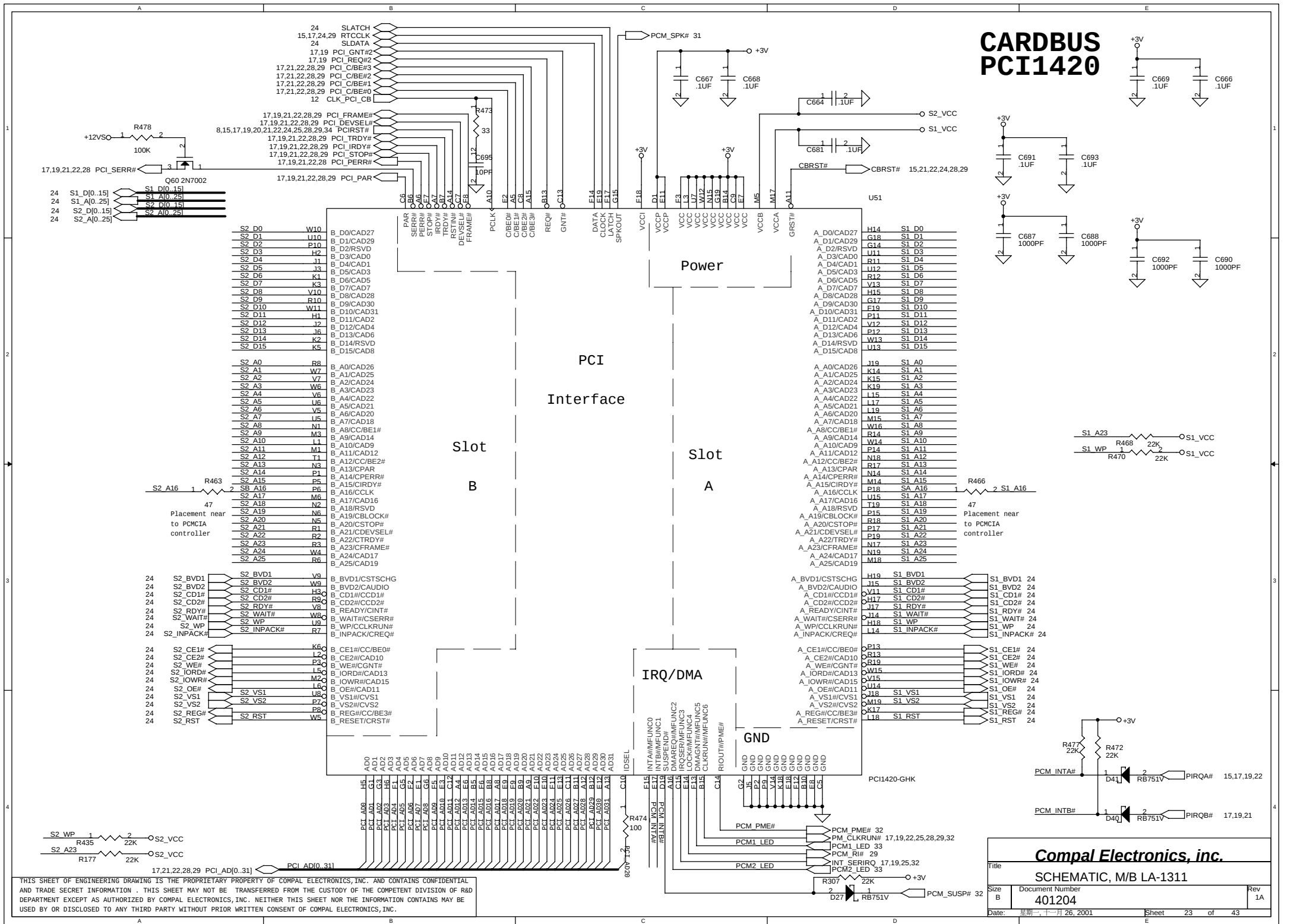
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VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V



Compal Electronics, inc.			
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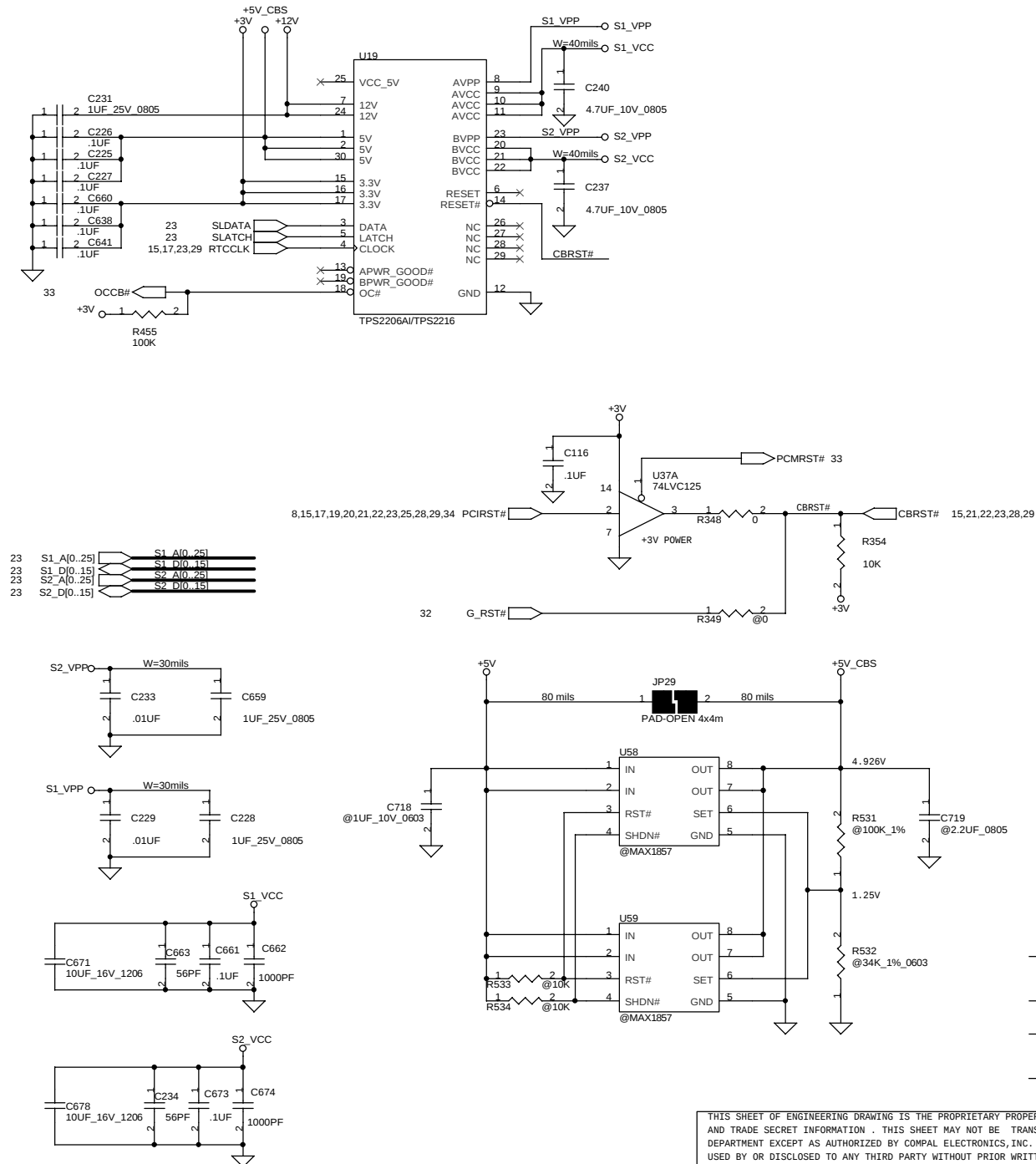
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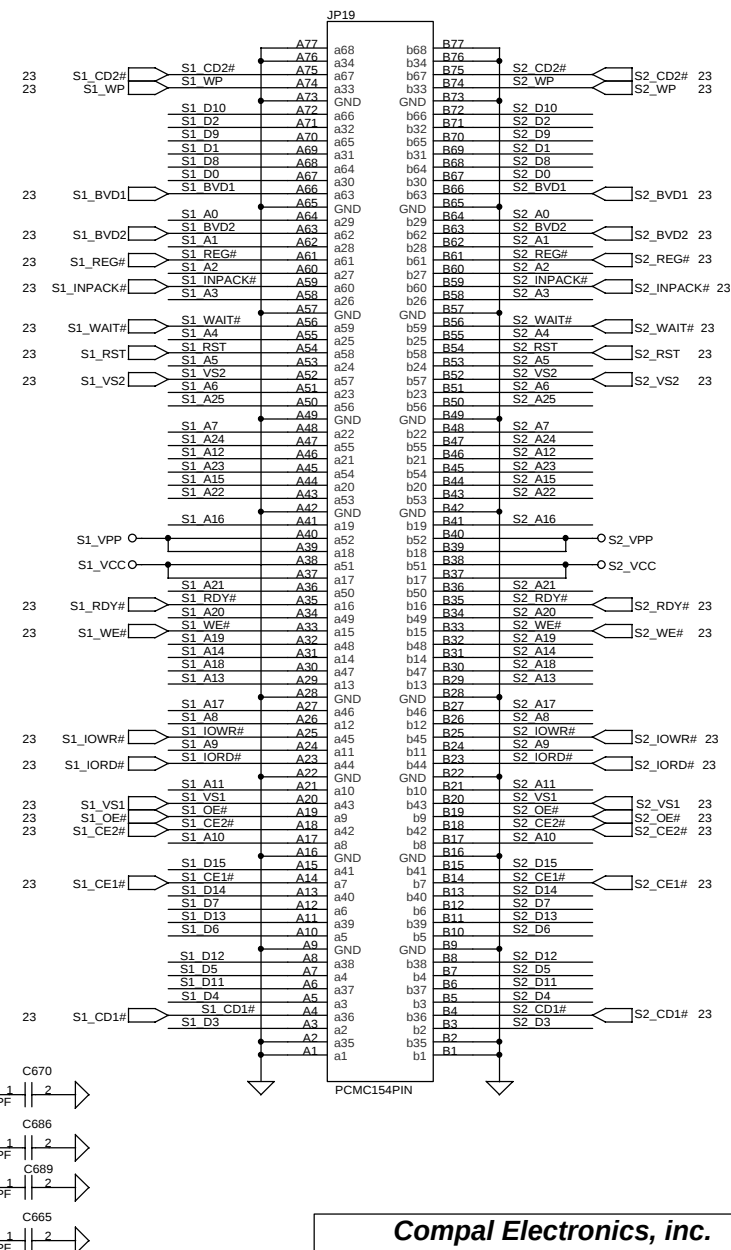


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PCMCIA POWER CTRL.



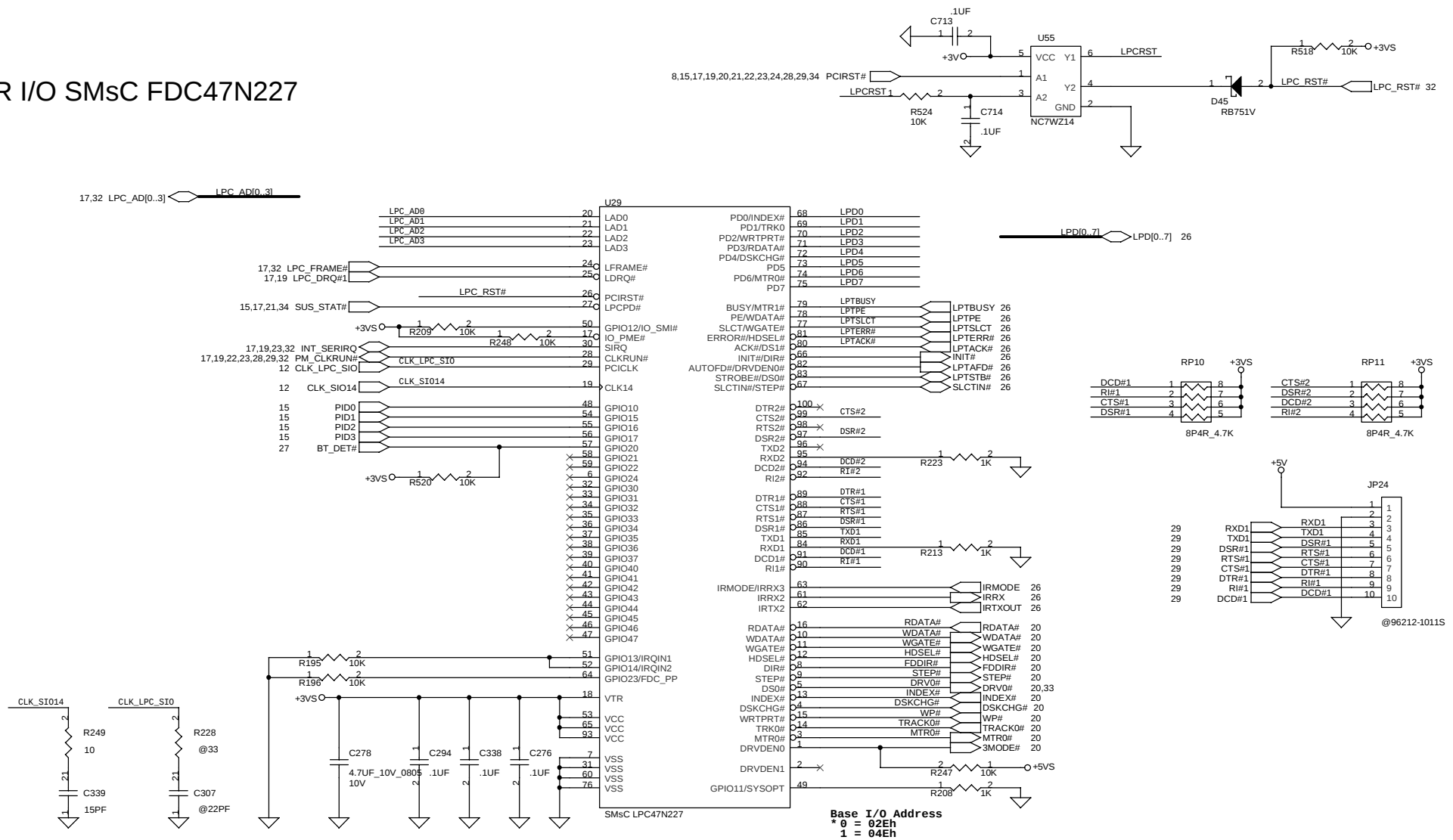
CARDBUS SOCKET



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SUPER I/O SMsC FDC47N227



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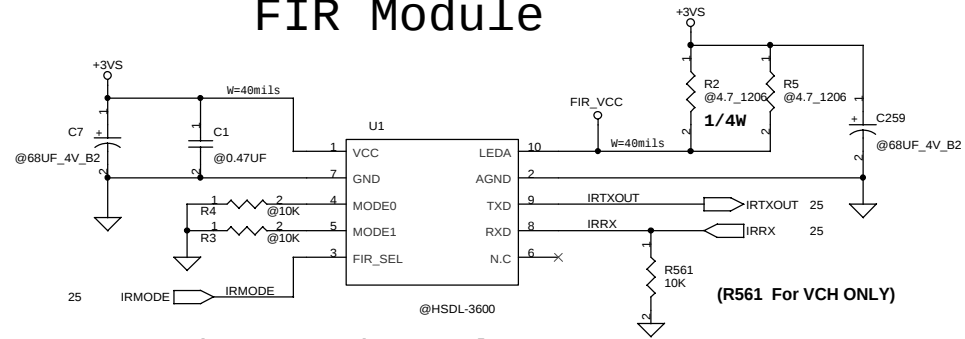
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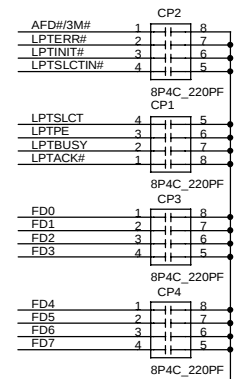
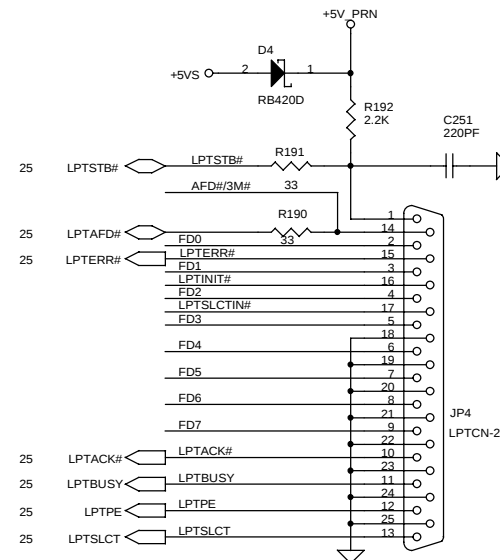
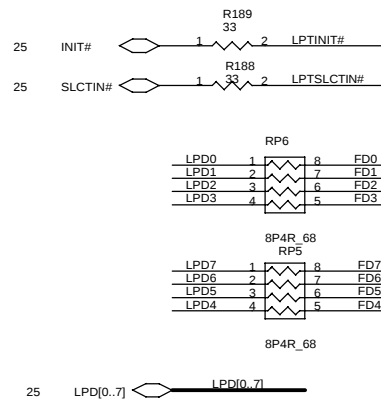
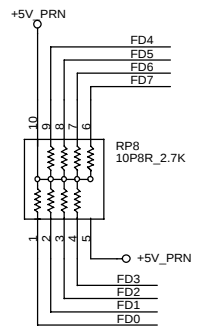
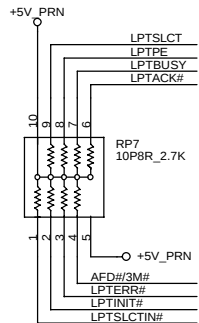
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FIR Module



The component's most place
cloely IRDA MODULE.

PARALLEL PORT

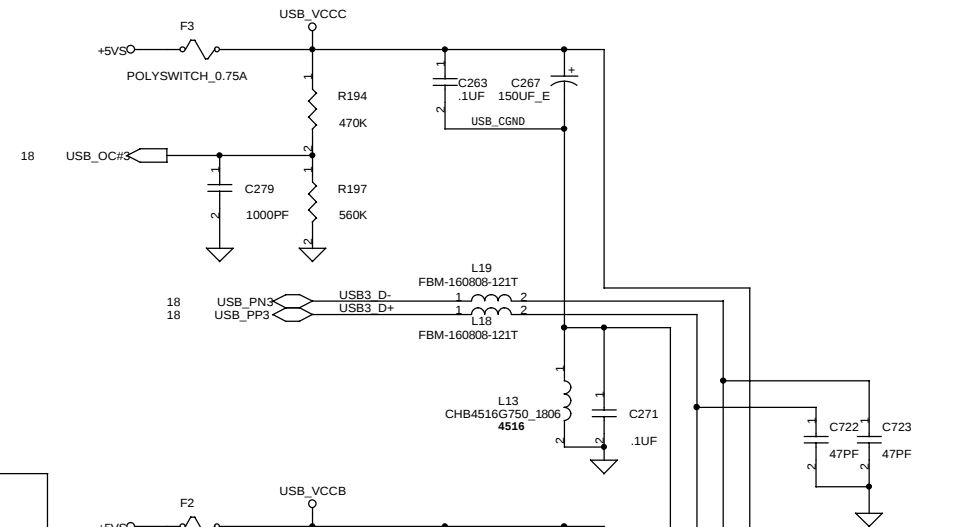
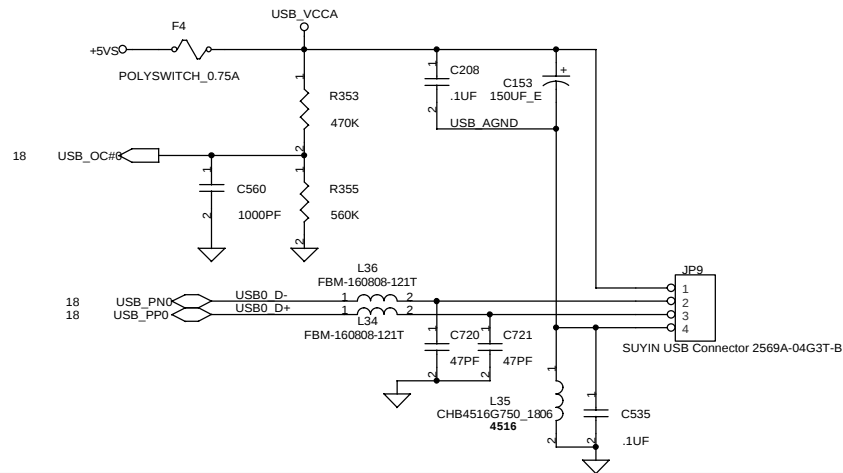


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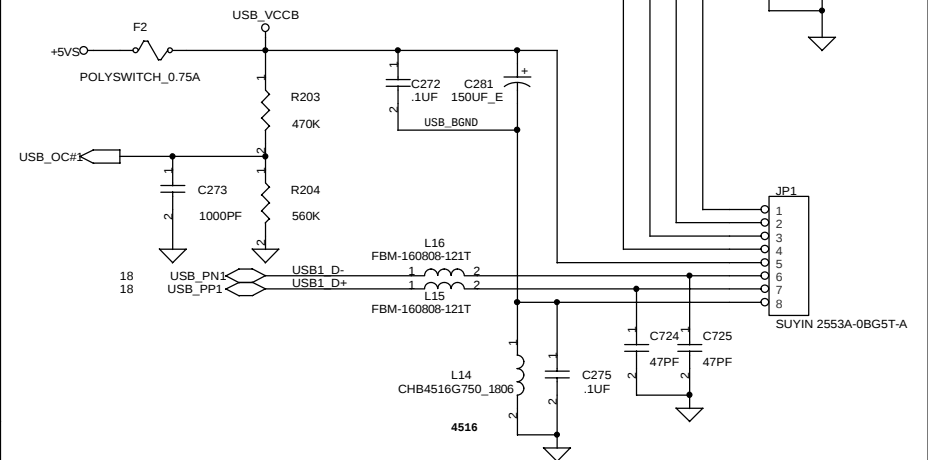
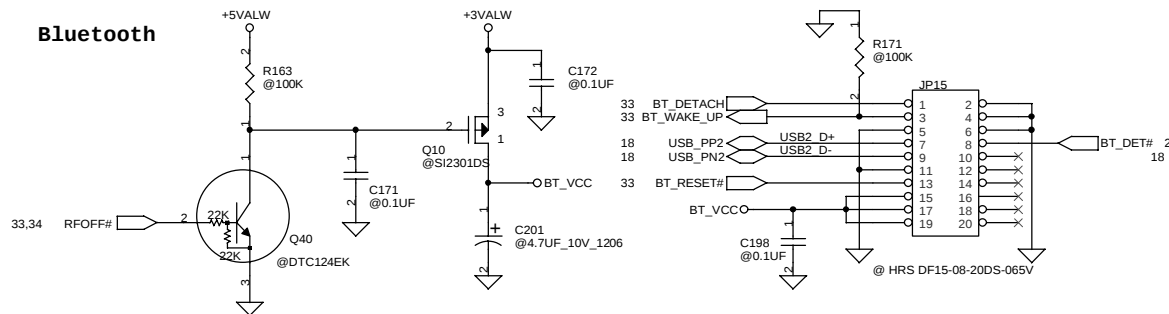
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USB PORT



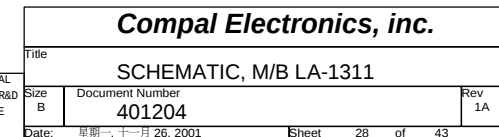
Bluetooth



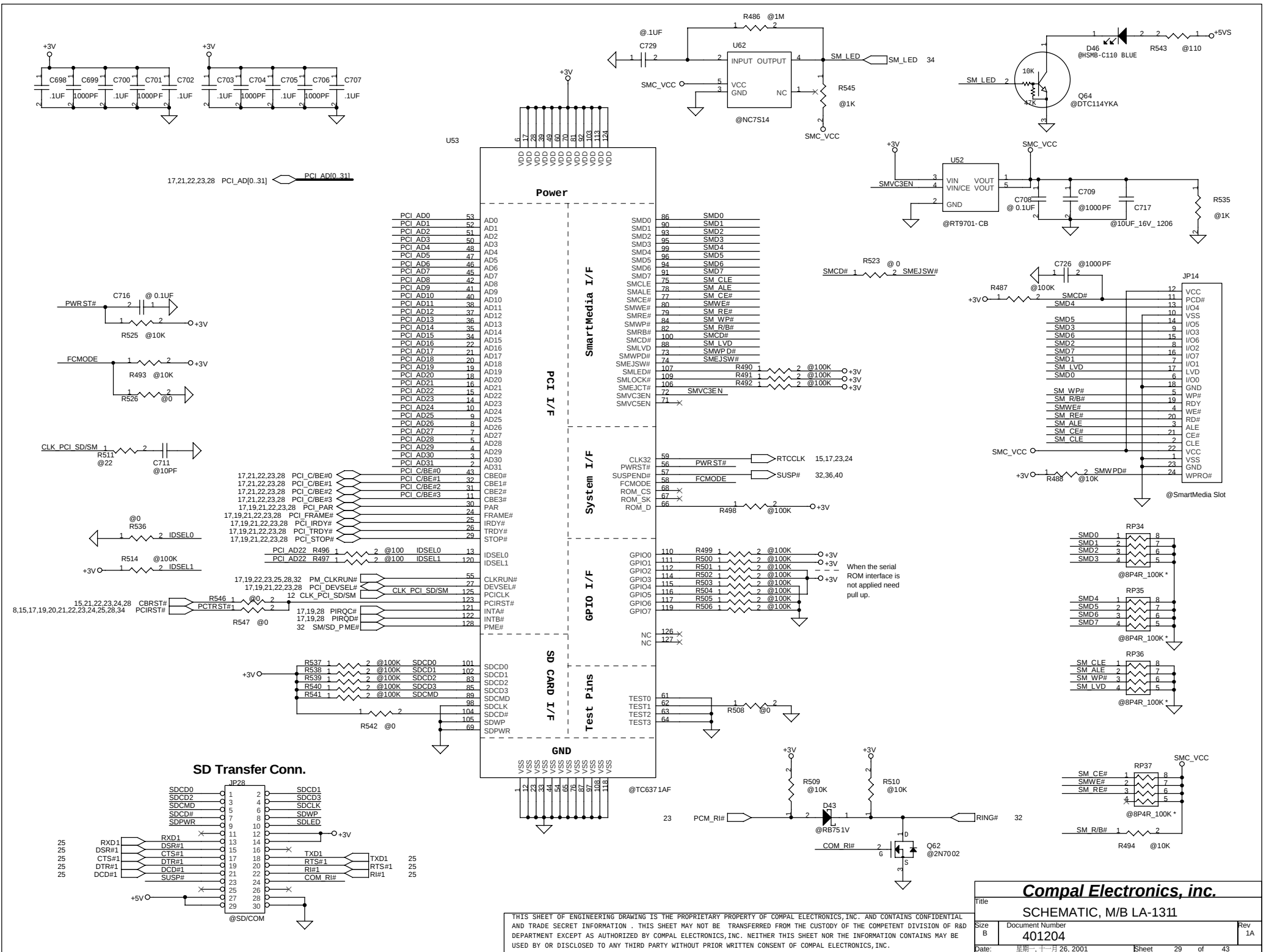
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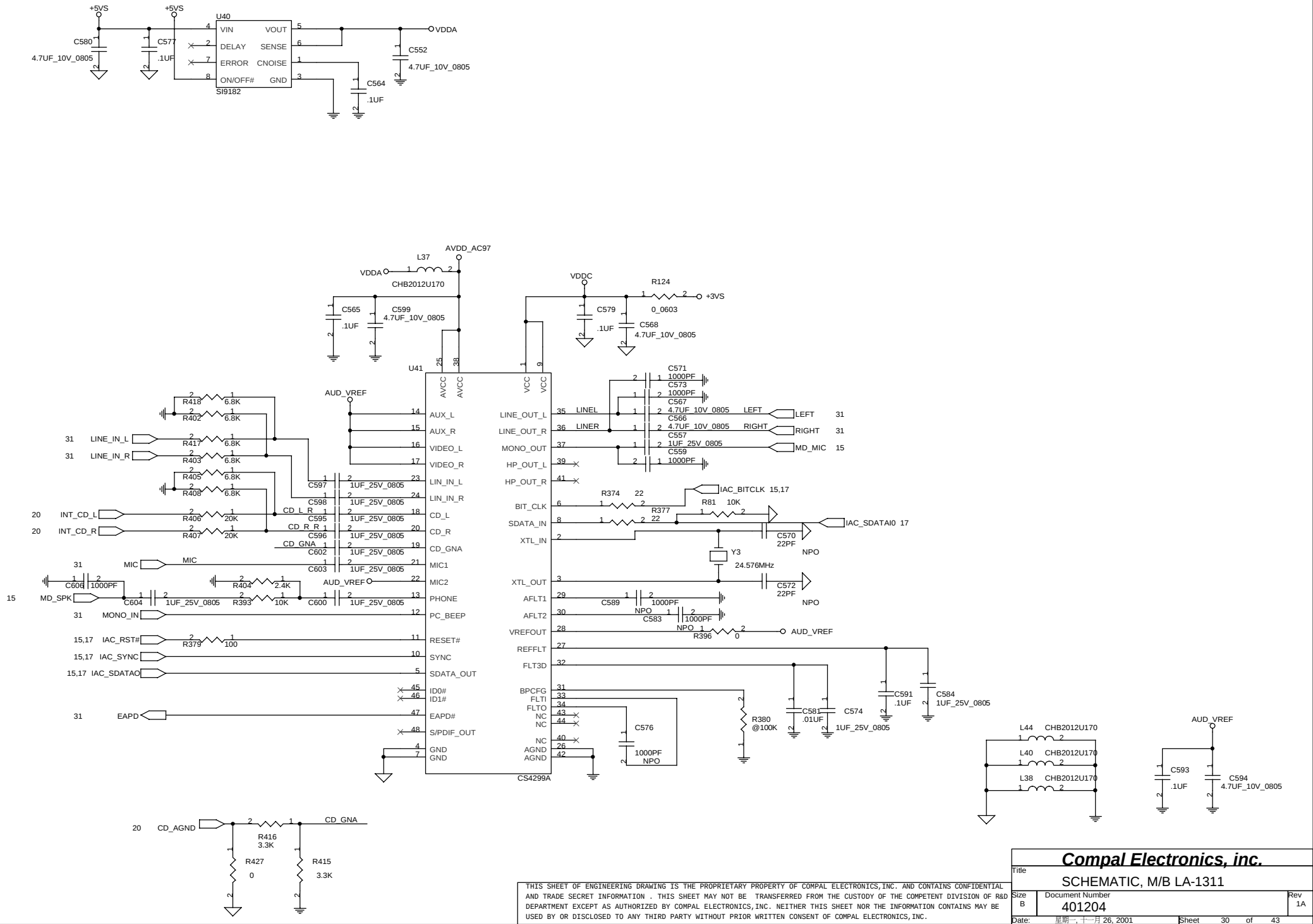
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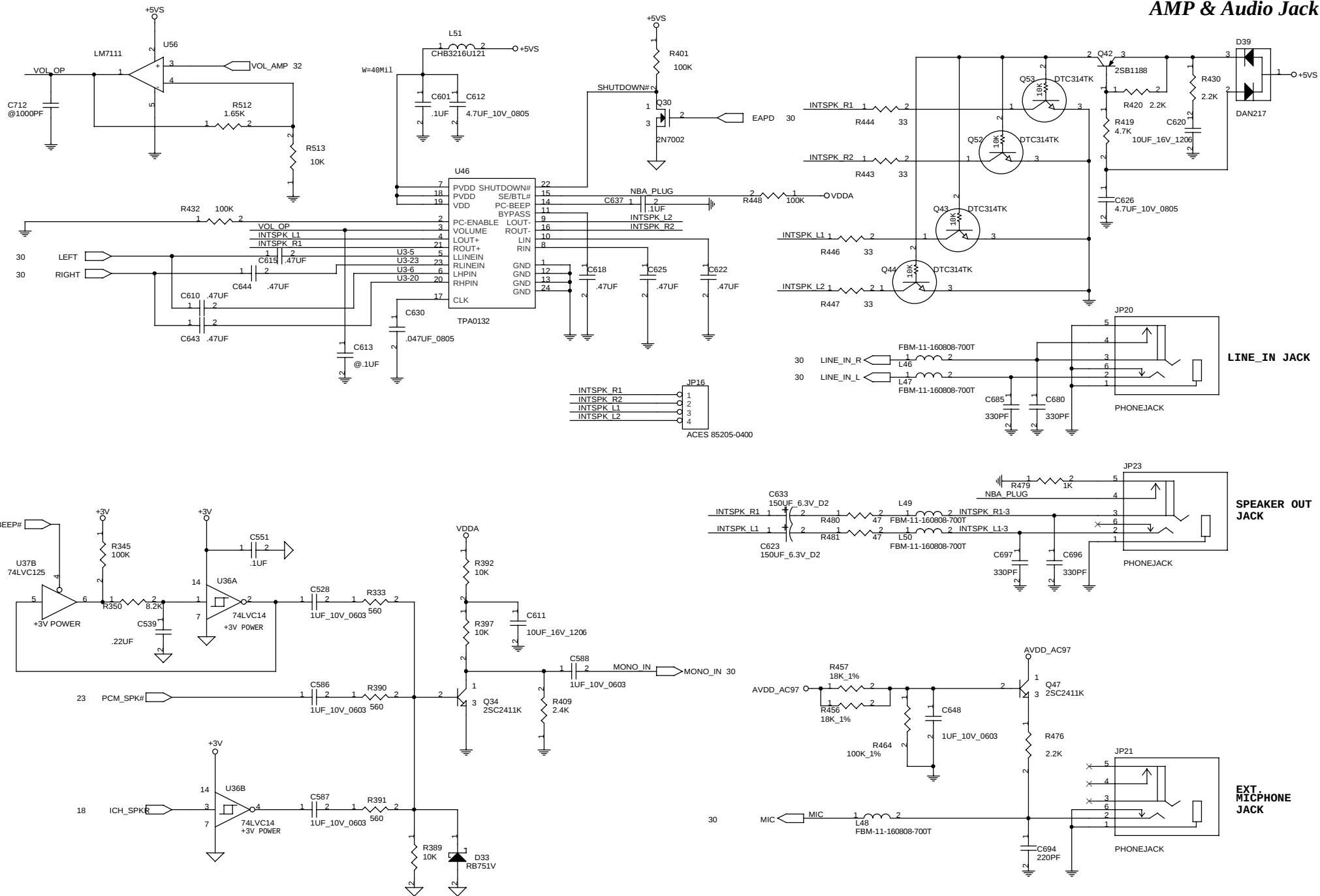
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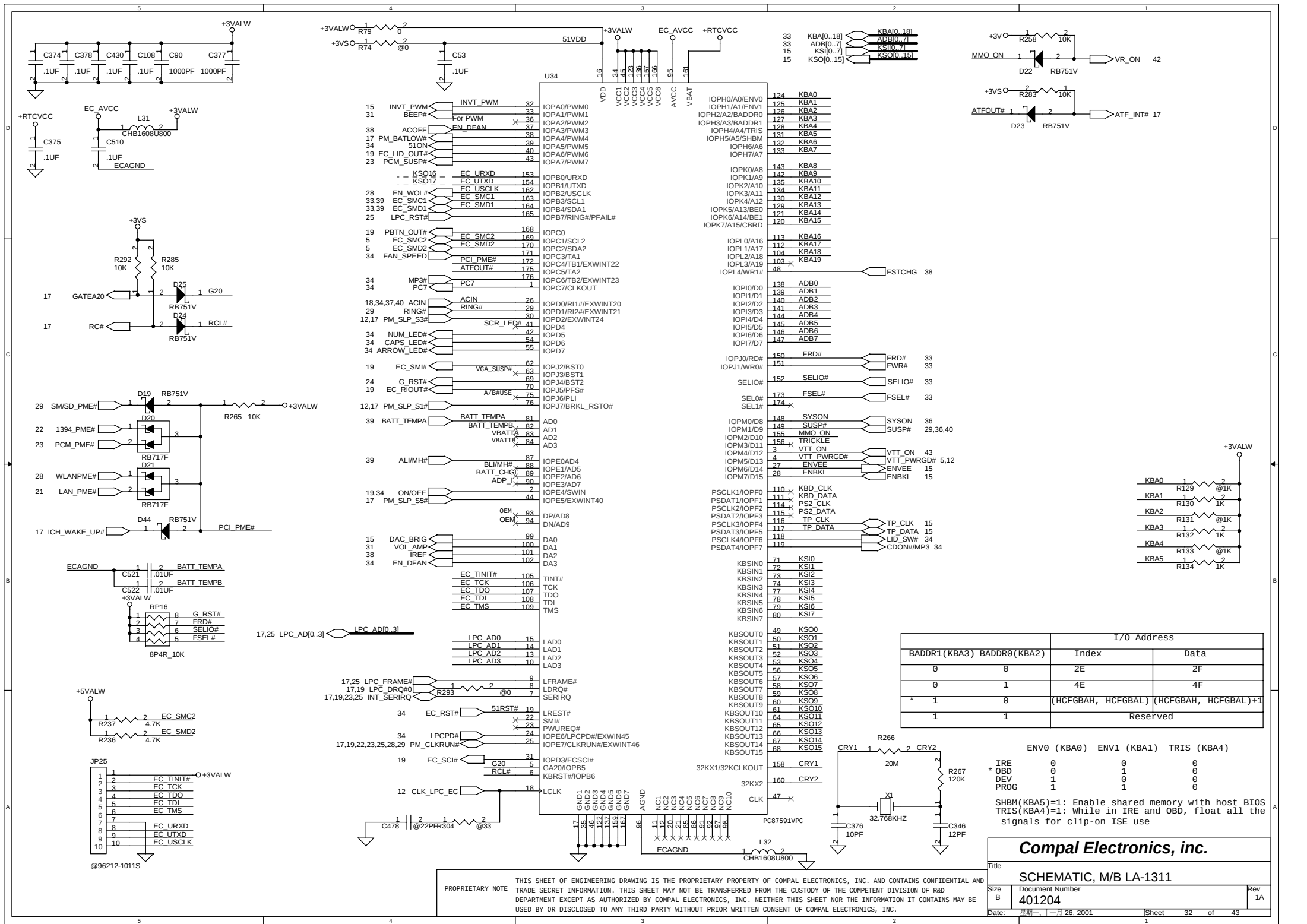
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AMP & Audio Jack



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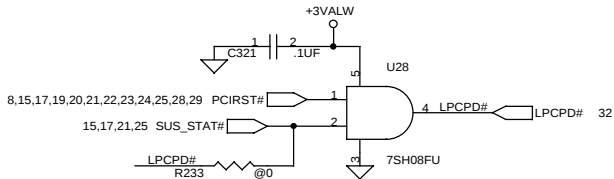
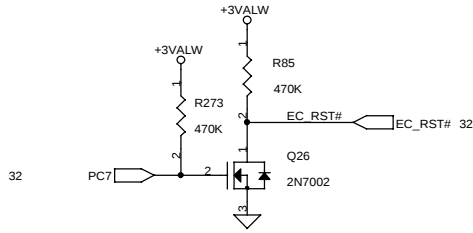
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BADDR1(KBA3) BADDR0(KBA2)		I/O Address	
		Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
1	1	Reserved	

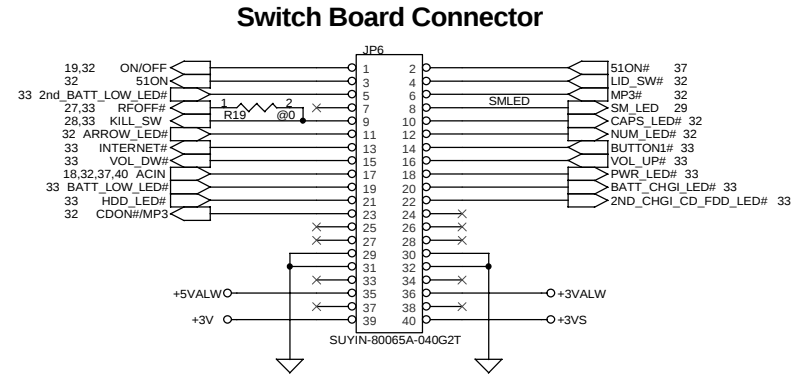
	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
* IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

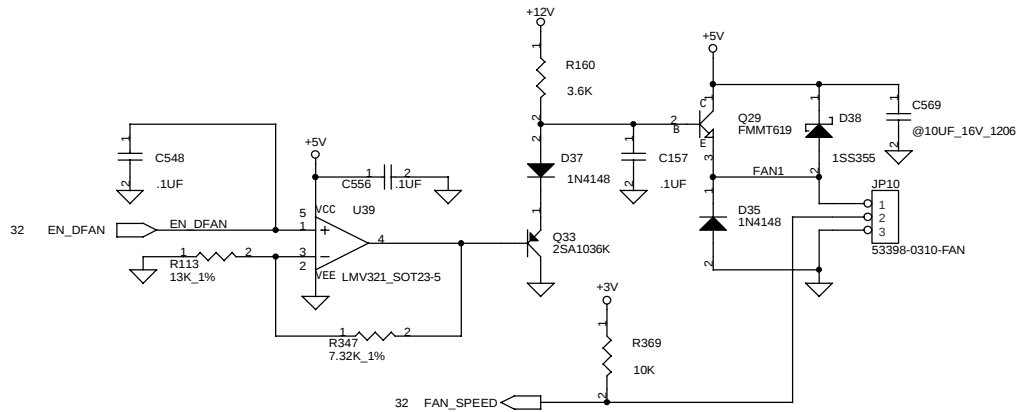
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For PC87591 REV 0.A Only



FAN CONN.



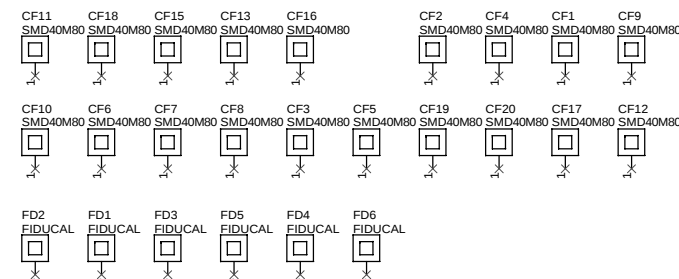
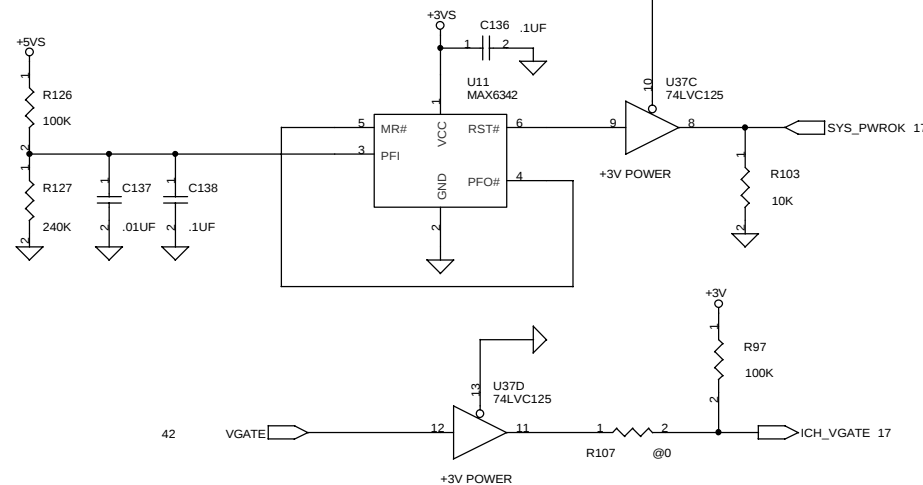
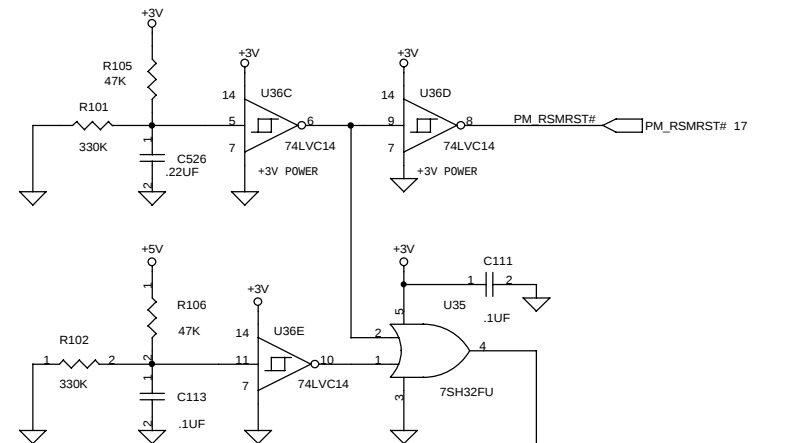
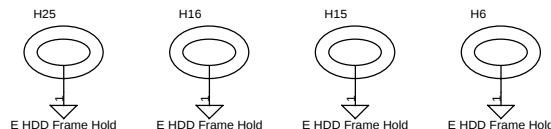
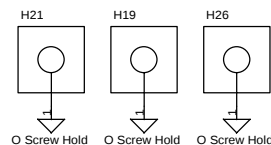
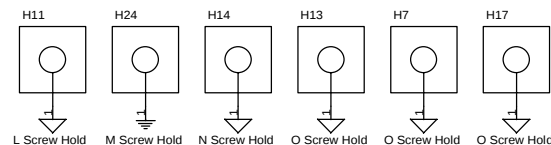
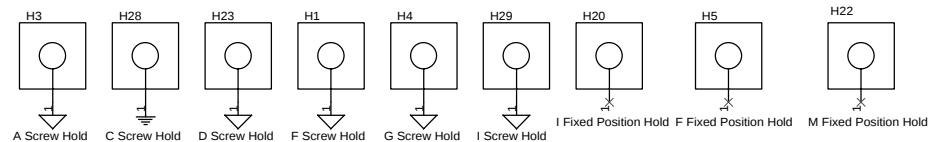
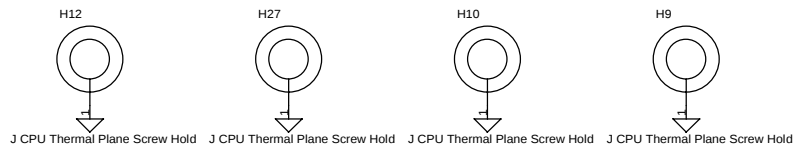
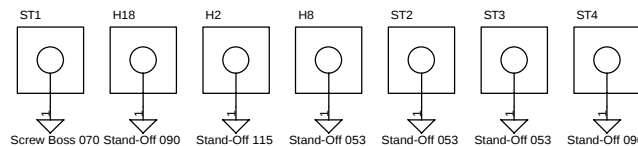
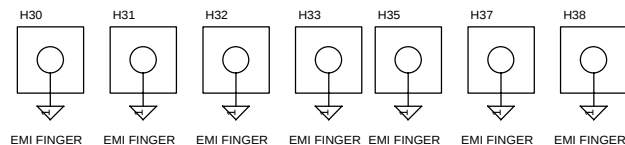
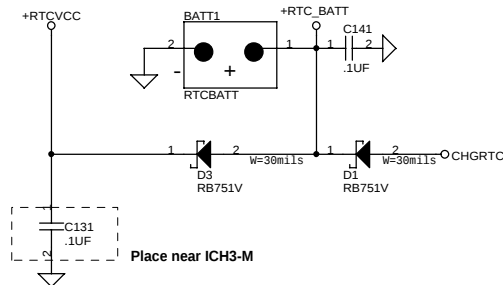
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RTC Batt. Connector

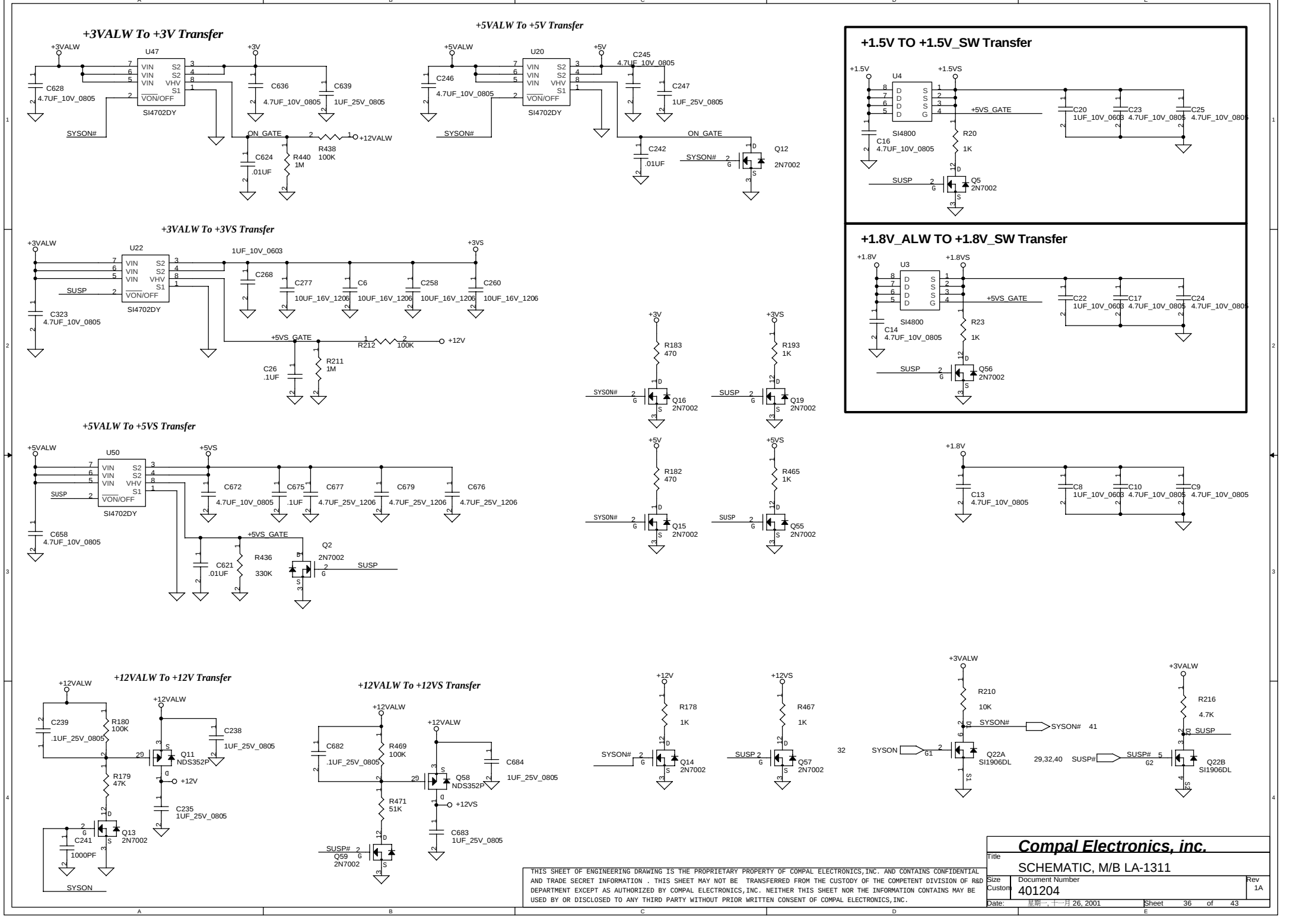


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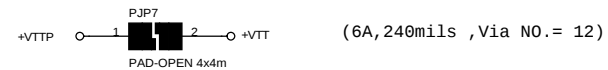
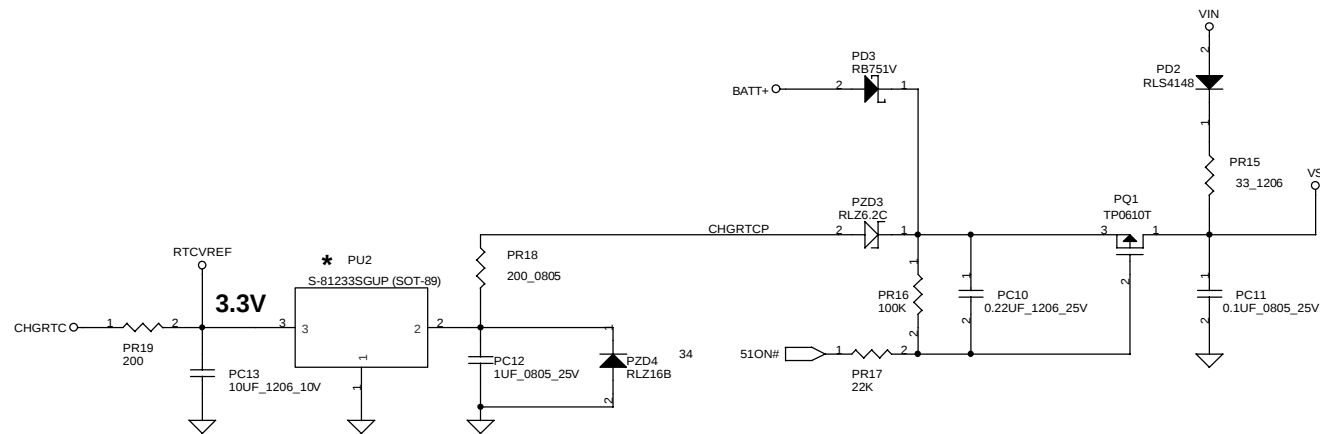
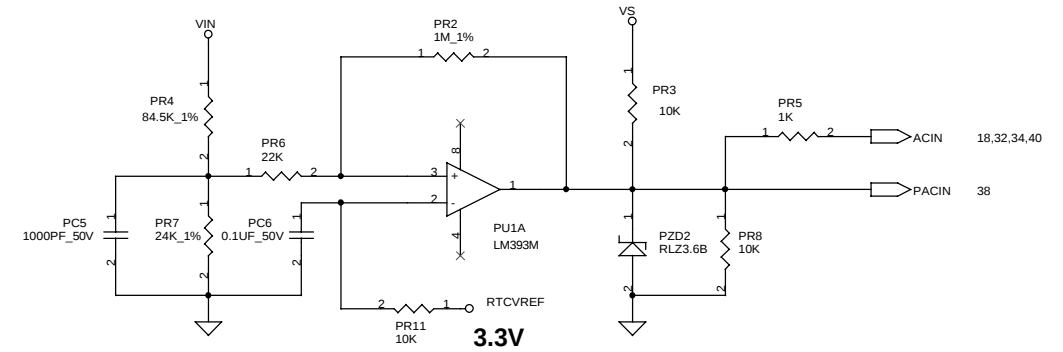
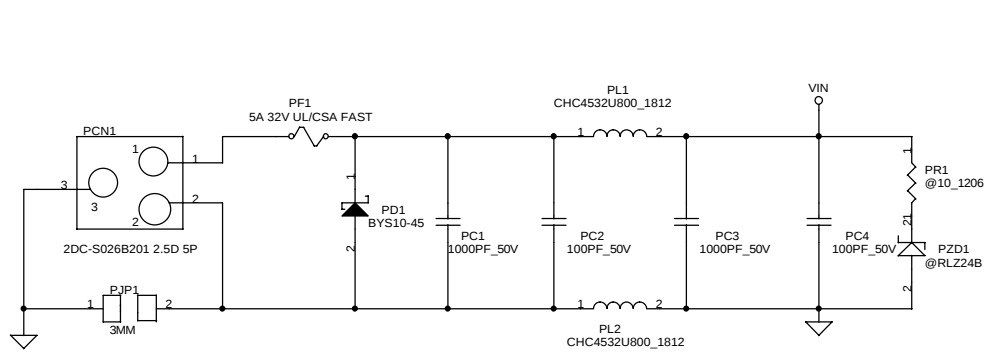
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Vin Detector				
High	16.265	15.526	14.808	V
Low	15.628	14.919	14.198	V

Vin Detector				
High	16.265	15.526	14.808	V
Low	15.628	14.919	14.198	V



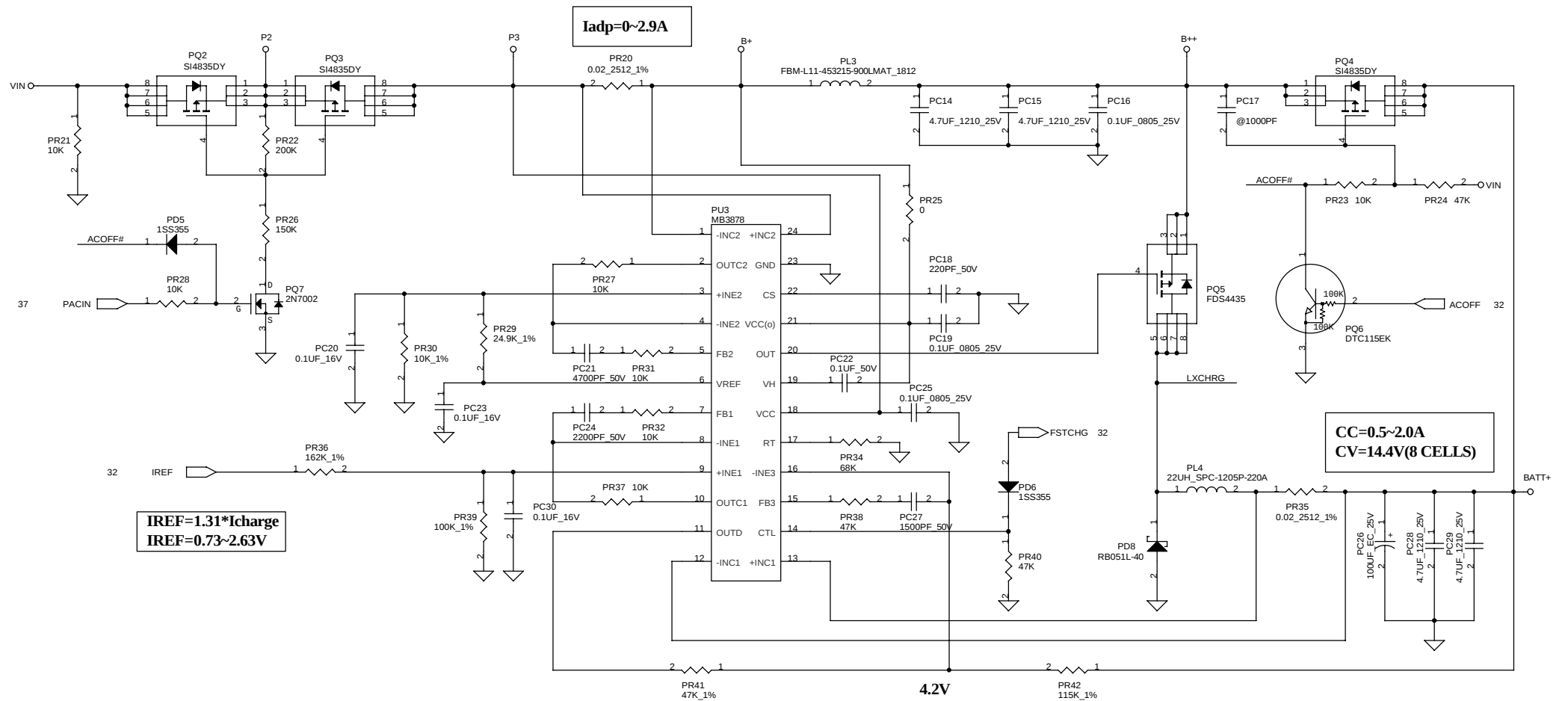
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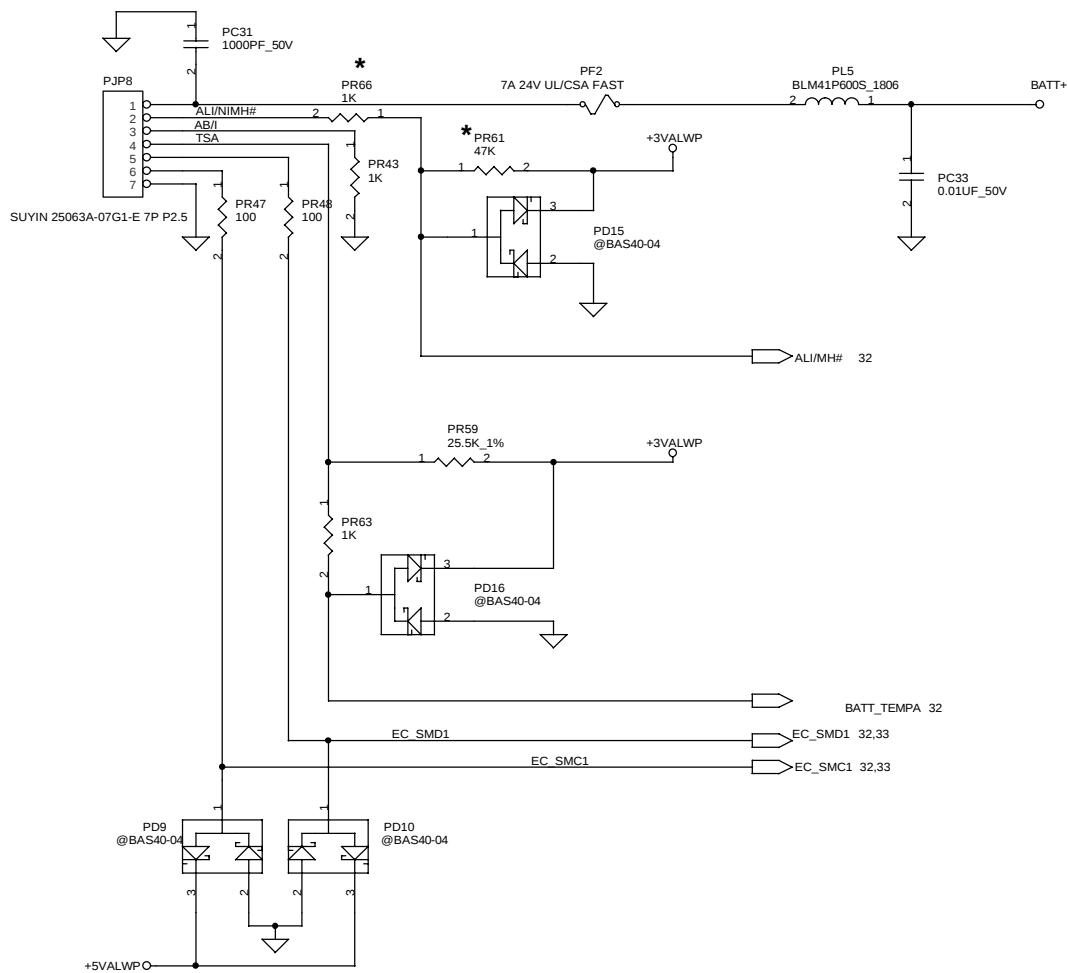


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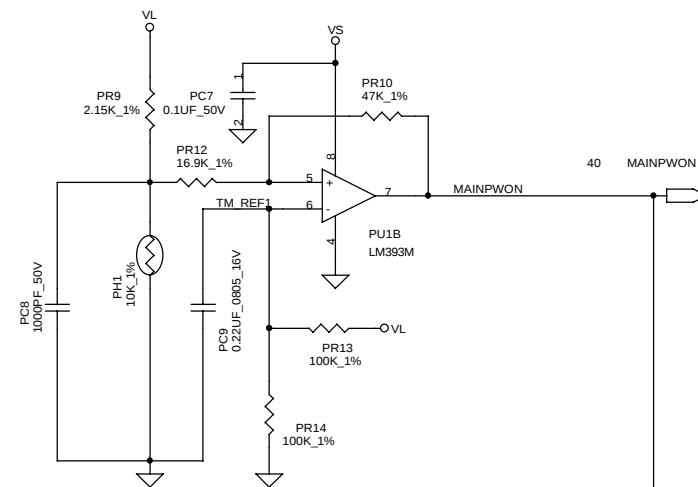
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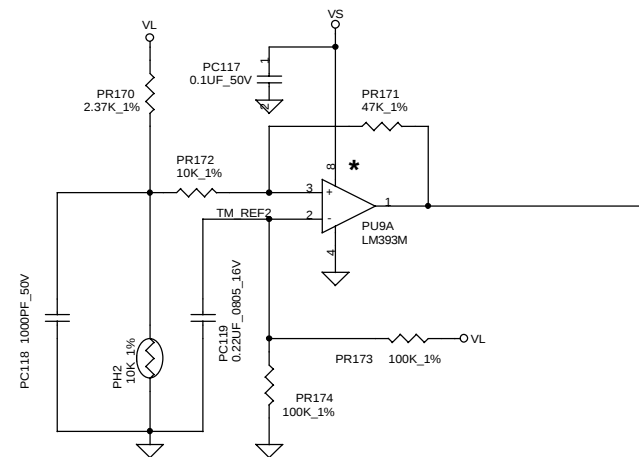
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PH1 under CPU botten side :
 CPU thermal protection at 82 degree C
 Recovery at 50(51) degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C

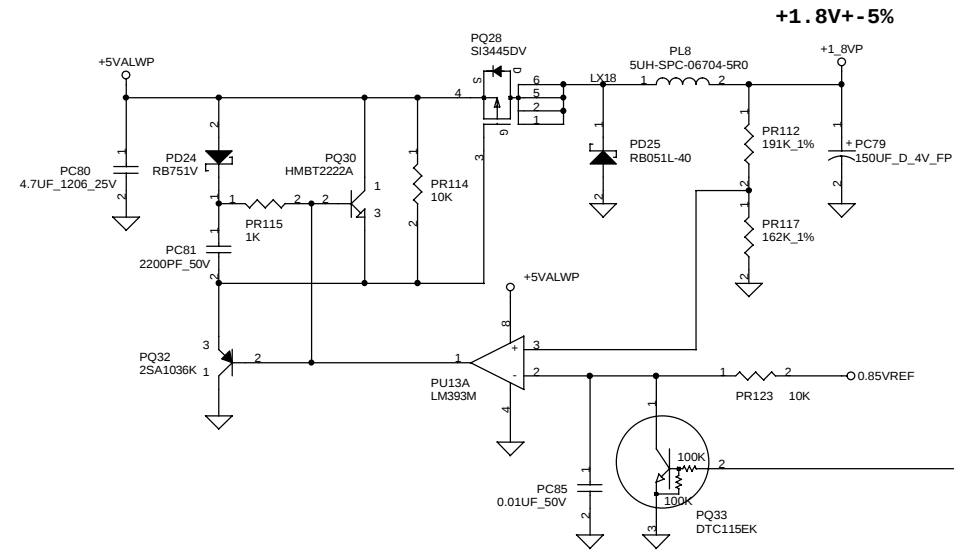
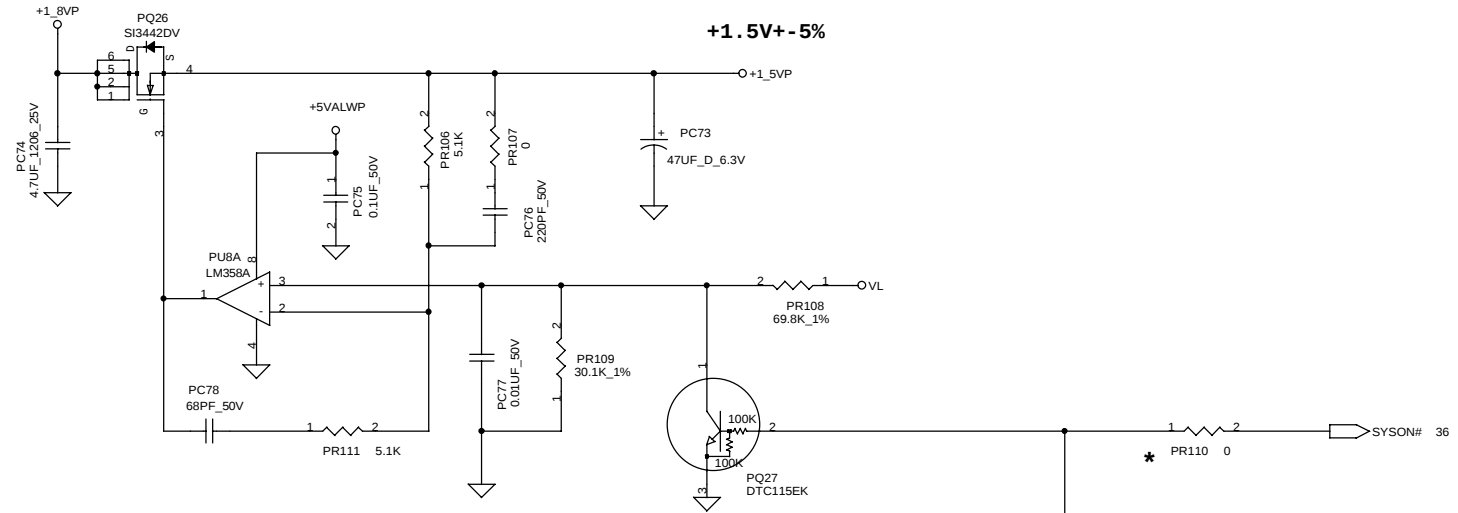


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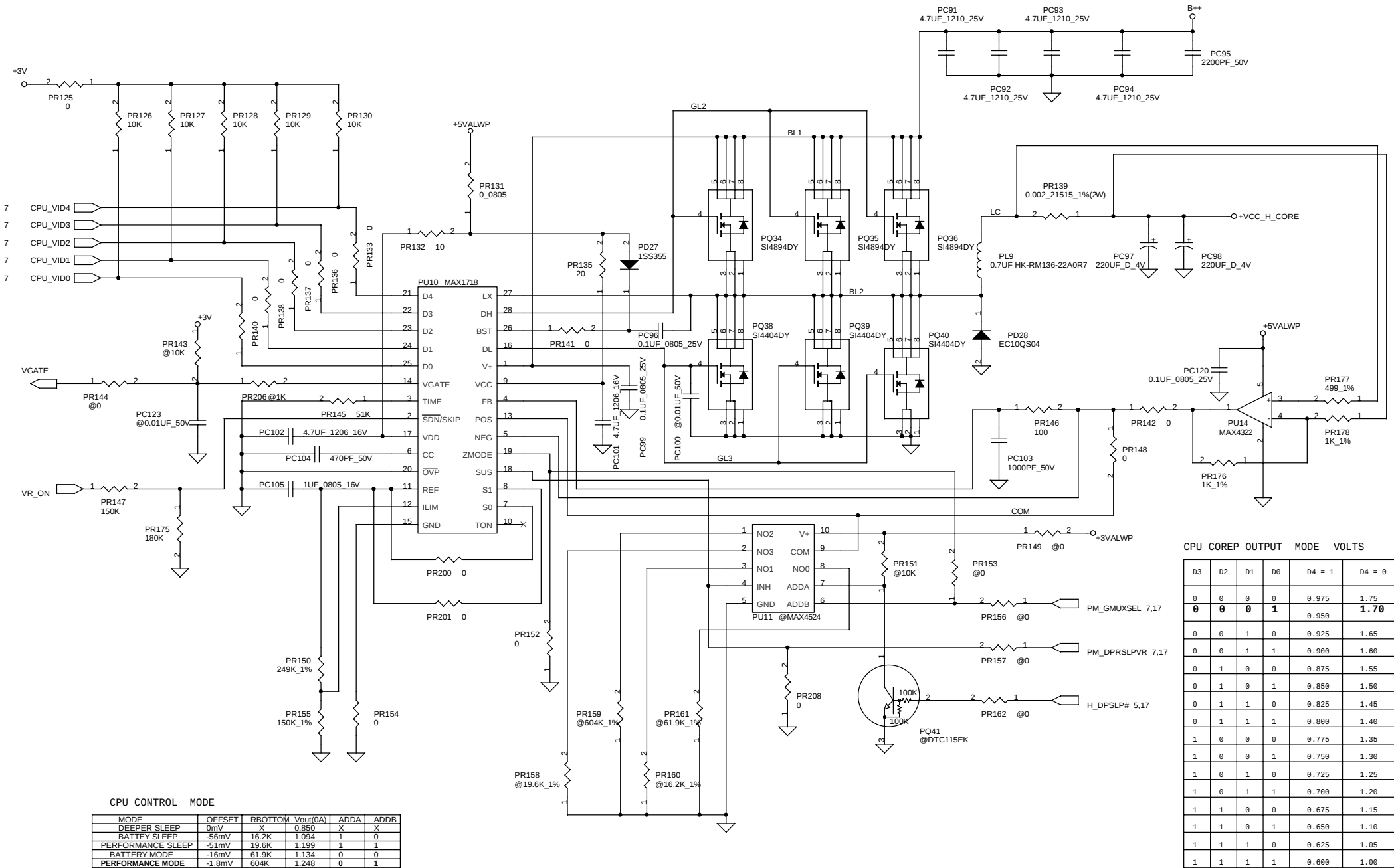
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