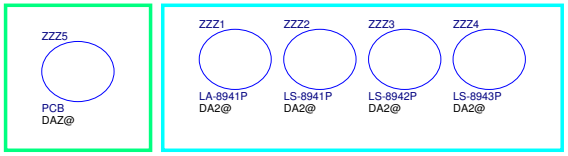
Compal Confidential

Model Name : Q1VZC
File Name :LA-8941P
BOM P/N:43



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Q1VZC M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-04-19

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

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Title: *Cover Page*

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 1 of 45

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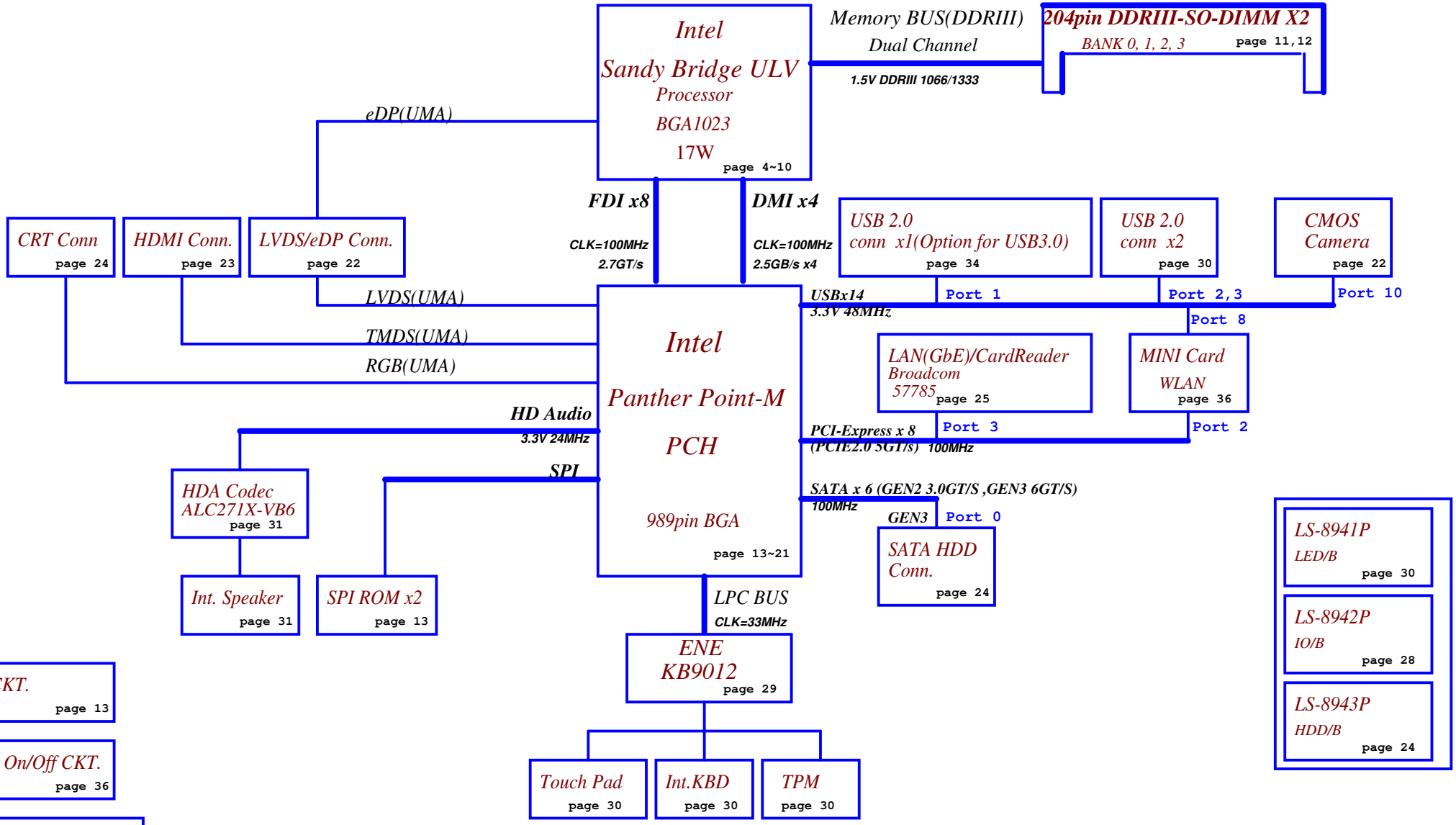
Model Name : Q1VZC
File Name :LA-8941P



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 2 of 45		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(STD)
ChannelB	DIMM0	B0	1010 010X	JDIMM2(REV)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Celeron 867	C867@
Pentium 977	P977@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

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Issued Date	2011/11/22	Deciphered Date	2012/11/22

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Title: Notes List

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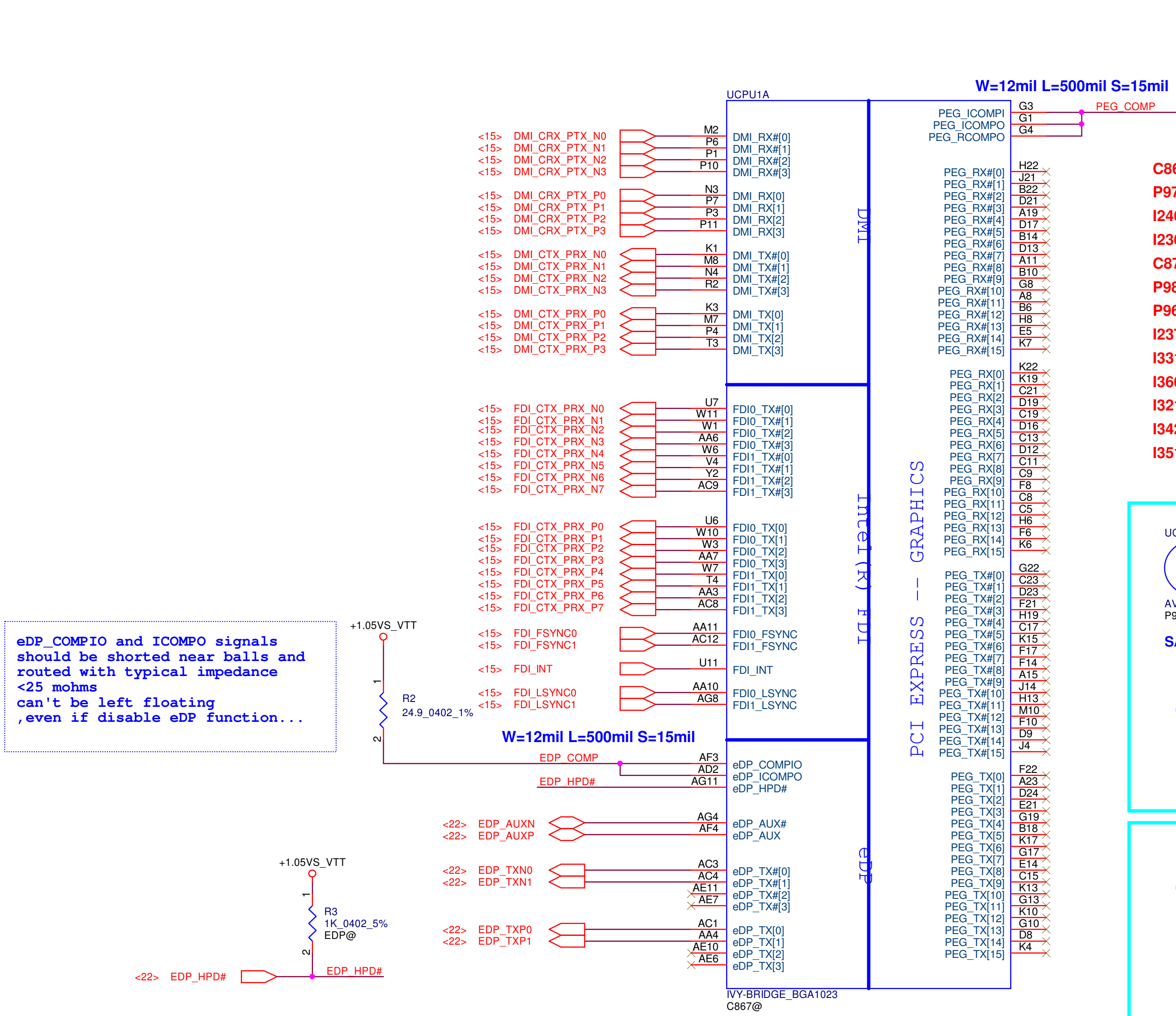
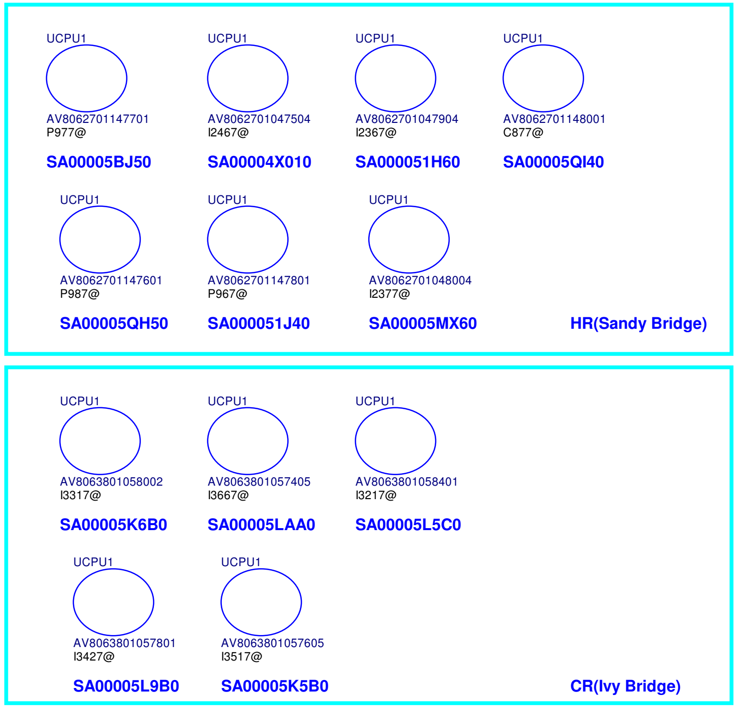
PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms



+1.05VS_VTT
R1
24.9_0402_1%
W=12mil L=500mil S=15mil
PEG_COMP
UCPU1A
PEG_ICOMPI G3
PEG_ICOMPO G1
PEG_RCOMPO G4
<15> DMI_CRX_PTX_N0 M2 DMI_RX#[0]
<15> DMI_CRX_PTX_N1 P6 DMI_RX#[1]
<15> DMI_CRX_PTX_N2 P1 DMI_RX#[2]
<15> DMI_CRX_PTX_N3 P10 DMI_RX#[3]
<15> DMI_CRX_PTX_P0 N3 DMI_RX[0]
<15> DMI_CRX_PTX_P1 P7 DMI_RX[1]
<15> DMI_CRX_PTX_P2 P3 DMI_RX[2]
<15> DMI_CRX_PTX_P3 P11 DMI_RX[3]
<15> DMI_CTX_PRX_N0 K1 DMI_TX#[0]
<15> DMI_CTX_PRX_N1 M8 DMI_TX#[1]
<15> DMI_CTX_PRX_N2 N4 DMI_TX#[2]
<15> DMI_CTX_PRX_N3 R2 DMI_TX#[3]
<15> DMI_CTX_PRX_P0 K3 DMI_TX[0]
<15> DMI_CTX_PRX_P1 M7 DMI_TX[1]
<15> DMI_CTX_PRX_P2 P4 DMI_TX[2]
<15> DMI_CTX_PRX_P3 T3 DMI_TX[3]
DMI
<15> FDI_CTX_PRX_N0 U7 FDI0_TX#[0]
<15> FDI_CTX_PRX_N1 W11 FDI0_TX#[1]
<15> FDI_CTX_PRX_N2 W1 FDI0_TX#[2]
<15> FDI_CTX_PRX_N3 AA6 FDI0_TX#[3]
<15> FDI_CTX_PRX_N4 W6 FDI1_TX#[0]
<15> FDI_CTX_PRX_N5 V4 FDI1_TX#[1]
<15> FDI_CTX_PRX_N6 Y2 FDI1_TX#[2]
<15> FDI_CTX_PRX_N7 AC9 FDI1_TX#[3]
<15> FDI_CTX_PRX_P0 U6 FDI0_TX[0]
<15> FDI_CTX_PRX_P1 W10 FDI0_TX[1]
<15> FDI_CTX_PRX_P2 W3 FDI0_TX[2]
<15> FDI_CTX_PRX_P3 AA7 FDI0_TX[3]
<15> FDI_CTX_PRX_P4 W7 FDI1_TX[0]
<15> FDI_CTX_PRX_P5 T4 FDI1_TX[1]
<15> FDI_CTX_PRX_P6 AA3 FDI1_TX[2]
<15> FDI_CTX_PRX_P7 AC8 FDI1_TX[3]
<15> FDI_FSYNC0 AA11 FDI0_FSYNC
<15> FDI_FSYNC1 AC12 FDI1_FSYNC
<15> FDI_INT U11 FDI_INT
<15> FDI_LSYNC0 AA10 FDI0_LSYNC
<15> FDI_LSYNC1 AG8 FDI1_LSYNC
Intel(R) FDI
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating
,even if disable eDP function...
+1.05VS_VTT
R2
24.9_0402_1%
W=12mil L=500mil S=15mil
EDP_COMP AF3 eDP_COMPIO
AD2 eDP_ICOMPO
EDP_HPD# AG11 eDP_HPD#
<22> EDP_AUXN AG4 eDP_AUX#
<22> EDP_AUXP AF4 eDP_AUX
<22> EDP_TXN0 AC3 eDP_TX#[0]
<22> EDP_TXN1 AC4 eDP_TX#[1]
AE11 eDP_TX#[2]
AE7 eDP_TX#[3]
<22> EDP_TXP0 AC1 eDP_TX[0]
<22> EDP_TXP1 AA4 eDP_TX[1]
AE10 eDP_TX[2]
AE6 eDP_TX[3]
eDP
+1.05VS_VTT
R3
1K_0402_5%
EDP@
<22> EDP_HPD# EDP_HPD#
PCI EXPRESS -- GRAPHICS
PEG_RX#[0] H22
PEG_RX#[1] J21
PEG_RX#[2] B22
PEG_RX#[3] D21
PEG_RX#[4] A19
PEG_RX#[5] D17
PEG_RX#[6] B14
PEG_RX#[7] D13
PEG_RX#[8] A11
PEG_RX#[9] B10
PEG_RX#[10] G8
PEG_RX#[11] A8
PEG_RX#[12] B6
PEG_RX#[13] H8
PEG_RX#[14] E5
PEG_RX#[15] K7
PEG_RX[0] K22
PEG_RX[1] K19
PEG_RX[2] C21
PEG_RX[3] D19
PEG_RX[4] C19
PEG_RX[5] D16
PEG_RX[6] C13
PEG_RX[7] D12
PEG_RX[8] C11
PEG_RX[9] C9
PEG_RX[10] F8
PEG_RX[11] C8
PEG_RX[12] C5
PEG_RX[13] H6
PEG_RX[14] F6
PEG_RX[15] K6
PEG_TX#[0] G22
PEG_TX#[1] C23
PEG_TX#[2] D23
PEG_TX#[3] F21
PEG_TX#[4] H19
PEG_TX#[5] C17
PEG_TX#[6] K15
PEG_TX#[7] F17
PEG_TX#[8] F14
PEG_TX#[9] A15
PEG_TX#[10] J14
PEG_TX#[11] H13
PEG_TX#[12] M10
PEG_TX#[13] F10
PEG_TX#[14] D9
PEG_TX#[15] J4
PEG_TX[0] F22
PEG_TX[1] A23
PEG_TX[2] D24
PEG_TX[3] E21
PEG_TX[4] G19
PEG_TX[5] B18
PEG_TX[6] K17
PEG_TX[7] G17
PEG_TX[8] E14
PEG_TX[9] C15
PEG_TX[10] K13
PEG_TX[11] G13
PEG_TX[12] K10
PEG_TX[13] G10
PEG_TX[14] D8
PEG_TX[15] K4
IVY-BRIDGE_BGA1023
C867@

C867@	Celeron 867	HR	1.3G	SA00005BH40(S IC AV8062701148901 SR0FK J1 1.3G ABO!)
P977@	Pentium 977	HR	1.4G	SA00005BJ50(S IC AV8062701147701 SR0FB J1 1.4G ABO!)
I2467@	i5-2467M	HR	1.6G	SA00004X010(S IC AV8062701047504 SR0D6 J1 1.6G ABO!)
I2367@	i3-2367M	HR	1.4G	SA000051H60(S IC AV8062701047904 SR0CV J1 1.4G ABO!)
C877@	Celeron 877	HR	1.4G	SA00005QI00(S IC AV8062701148001 QB35 J1 1.4G BGA)
P987@	Pentium 987	HR	1.5G	SA00005QH00(S IC AV8062701147601 QB31 J1 1.5G BGA)
P967@	Pentium 967	HR	1.3G	SA000051J40(S IC AV8062701147801 SR0FC J1 1.3G ABO!)
I2377@	i3-2377M	HR	1.5G	SA00005MX10(S IC AV8062701048004 QAXQ J1 1.5G BGA)
I3317@	i5-3317U	CR	1.7G	SA00005K650(S IC AV8063801058002 QC9E L1 1.7G BGA)
I3667@	i7-3667U	CR	2G	SA00005LA50(S IC AV8063801057405 QC9B L1 2G BGA 1023)
I3217@	i3-3217U	CR	1.8G	SA00005L530(S IC AV8063801058400 QC56 L0 1.8G ABO!)
I3427@	i5-3427U	CR	1.8G	SA00005L9A0(S IC AV8063801057801 SR0N7 L1 1.8G BGA)
I3517@	i7-3517U	CR	1.9G	SA00005K540(S IC AV8063801057605 QC9C L1 1.9G BGA)



UCPU1
AV8062701147701
P977@
SA00005BJ50
UCPU1
AV8062701047504
I2467@
SA00004X010
UCPU1
AV8062701047904
I2367@
SA000051H60
UCPU1
AV8062701148001
C877@
SA00005QI40
UCPU1
AV8062701147601
P987@
SA00005QH50
UCPU1
AV8062701147801
P967@
SA000051J40
UCPU1
AV8062701048004
I2377@
SA00005MX60
HR(Sandy Bridge)
UCPU1
AV8063801058002
I3317@
SA00005K6B0
UCPU1
AV8063801057405
I3667@
SA00005LAA0
UCPU1
AV8063801058401
I3217@
SA00005L5C0
UCPU1
AV8063801057801
I3427@
SA00005L9B0
UCPU1
AV8063801057605
I3517@
SA00005K5B0
CR(Ivy Bridge)

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Issued Date	2011/11/22	Deciphered Date	2012/11/22	Title: PROCESSOR(1/7) DMI,FDI,PEG

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0921 LVDS@->@

+1.05VS_VTT

CLK_CPU_DPLL# R4 2 LVDS@ 1 1K_0402_5%

CLK_CPU_DPLL R5 2 LVDS@ 1 1K_0402_5%

Checklist1.5 P.67 Graphis Disable Guide
eDP disable:
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PU 1K_5% to +1.05VS_VTT

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

<17> H_SNB_IVB# F49 PROC_SELECT#

C57 PROC_DETECT#

偵測CPU有無安裝

XBOX 三紅功能

T1 PAD@ H_CATERR# C49 CATERR#

follow Checklist 1.5

<18,29> H_PECI H_PECI A48 PECI

+1.05VS_VTT R7 2 1 62_0402_5%

R8 56_0402_5%

<29,35> H_PROCHOT# H_PROCHOT# 1 2 H_PROCHOT#_R C45 PROCHOT#

<18> H_THRMTRIP# D45 THERMTRIP#

UCPU1B

MISC

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

BCLK J3 H2 CLK_CPU_DMI <14> CLK_CPU_DMI# <14>

DPLL_REF_CLK AG3 CLK_CPU_DPLL CLK_CPU_DPLL <14>
DPLL_REF_CLK# AG1 CLK_CPU_DPLL# CLK_CPU_DPLL# <14>

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# <6>

SM_RCOMP[0] BF44 SM_RCOMP0 R9 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R10 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R11 2 1 200_0402_1%

DDR3 Compensation Signals

PRDY# N53
PREQ# N55

TCK L56 XDP_TCK @ PAD T2
TMS L55 XDP_TMS @ PAD T3
TRST# J58 XDP_TRST# @ PAD T4

TDI M60 XDP_TDI @ PAD T5
TDO L59 XDP_TDO @ PAD T6

DBR# K58 XDP_DBRESET# XDP_DBRESET# <15>

BPM#[0] G58
BPM#[1] E55
BPM#[2] E59
BPM#[3] G55
BPM#[4] G59
BPM#[5] H60
BPM#[6] J59
BPM#[7] J61

<15> H_PM_SYNC C48 PM_SYNC

<18> H_CPUPWRGD R13 1 2 H_CPUPWRGD_R B46 UNCOREPWRGOOD

UNCOREPWRGOOD:非CORE外的電OK

PM_DRAM_PWRGD_R BE45 SM_DRAMPWROK

SM_DRAMPWROK:DRAM power ok

BUF_CPU_RST# D44 RESET#

IVY-BRIDGE_BGA1023
C867@

C476 @ 2 1 H_CPUPWRGD_R 180P_0402_50V8J

12/22 Add(ESD request)

Follow DG 1.5& Tacoma_Fall2 1.0

reserve

C65 @ 2 1 0.1U_0402_16V4Z H_CPUPWRGD

R6 2 1 10K_0402_5%

Follow DG 1.5 & Tacoma_Fall2 1.0

Buffered reset to CPU

Use open drain logic gate:
+1.05VS_VTT PU pop 75ohm
series resister pop 43ohm

+3VS

C66 0.1U_0402_16V4Z

+1.05VS_VTT

R12 75_0402_5%

R14 0_0402_5%

R15 43_0402_1%

U1

<17> PLT_RST# PLT_RST# BUFO_CPU_RST# BUF_CPU_RST#

SN74LVC1G07DCKR_SC70-5

RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0

Use open drain logic gate:
+1.5V_CPU_VDDQ PU pop 200ohm
series resister pop 130ohm

+3VALW

C67 0.1U_0402_16V4Z

+1.5V_CPU_VDDQ

R16 200_0402_5%

U2

<15> SYS_PWROK

<15> PM_DRAM_PWRGD

PM_SYS_PWRGD_BUF

R18 130_0402_5%

PM_DRAM_PWRGD_R

MC74VHC1G09DFT2G_SC70-5

+3VS

XDP_DBRESET# R17 2 1 1K_0402_5%

Tacoma_Fall2 1.0 PU 1K +3VS
Check list 1.5 PU 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

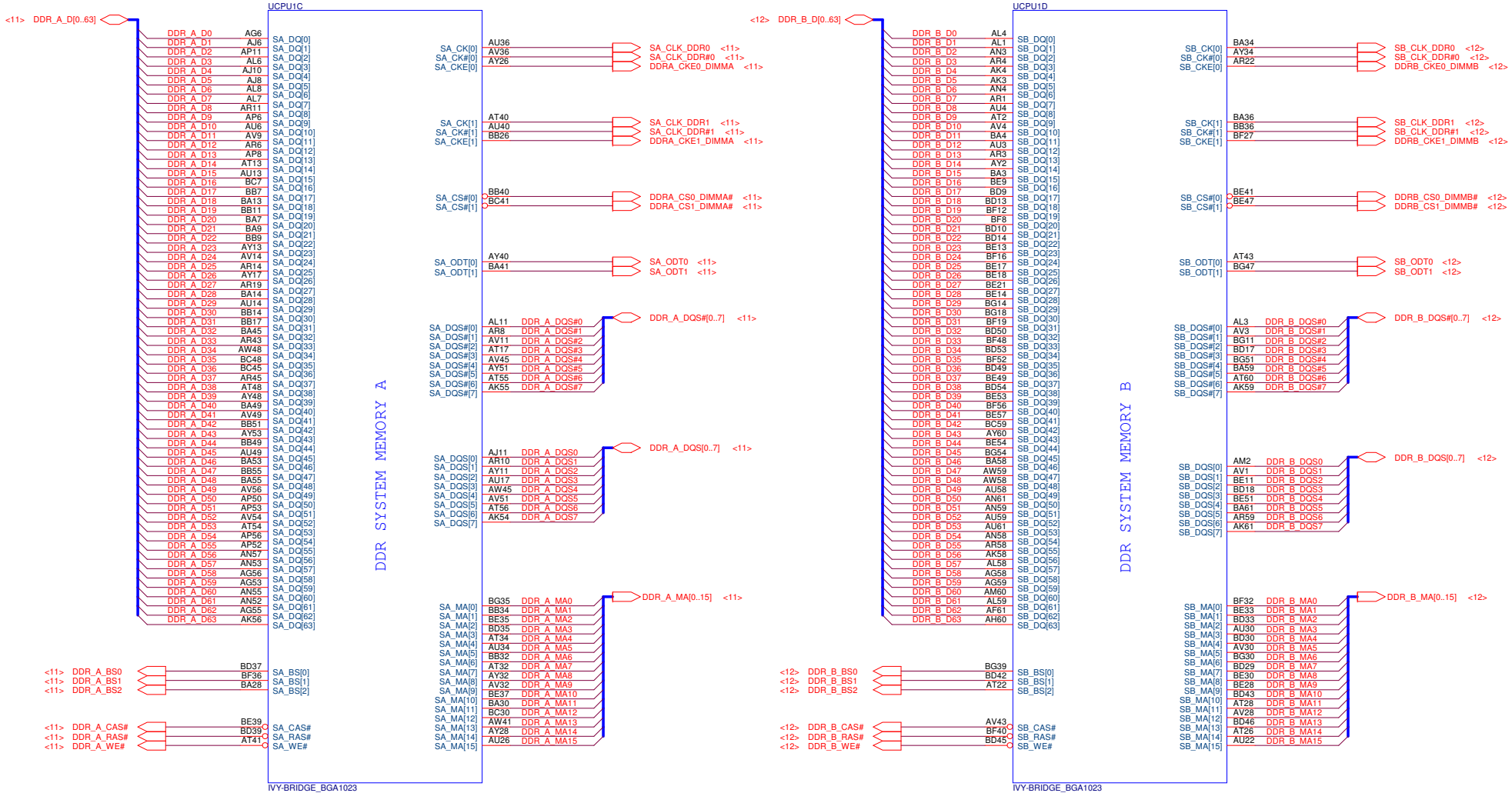
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

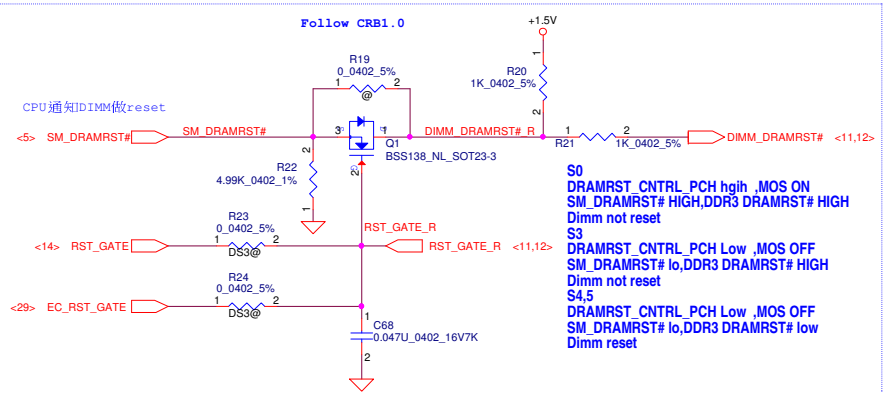
Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 5 of 45





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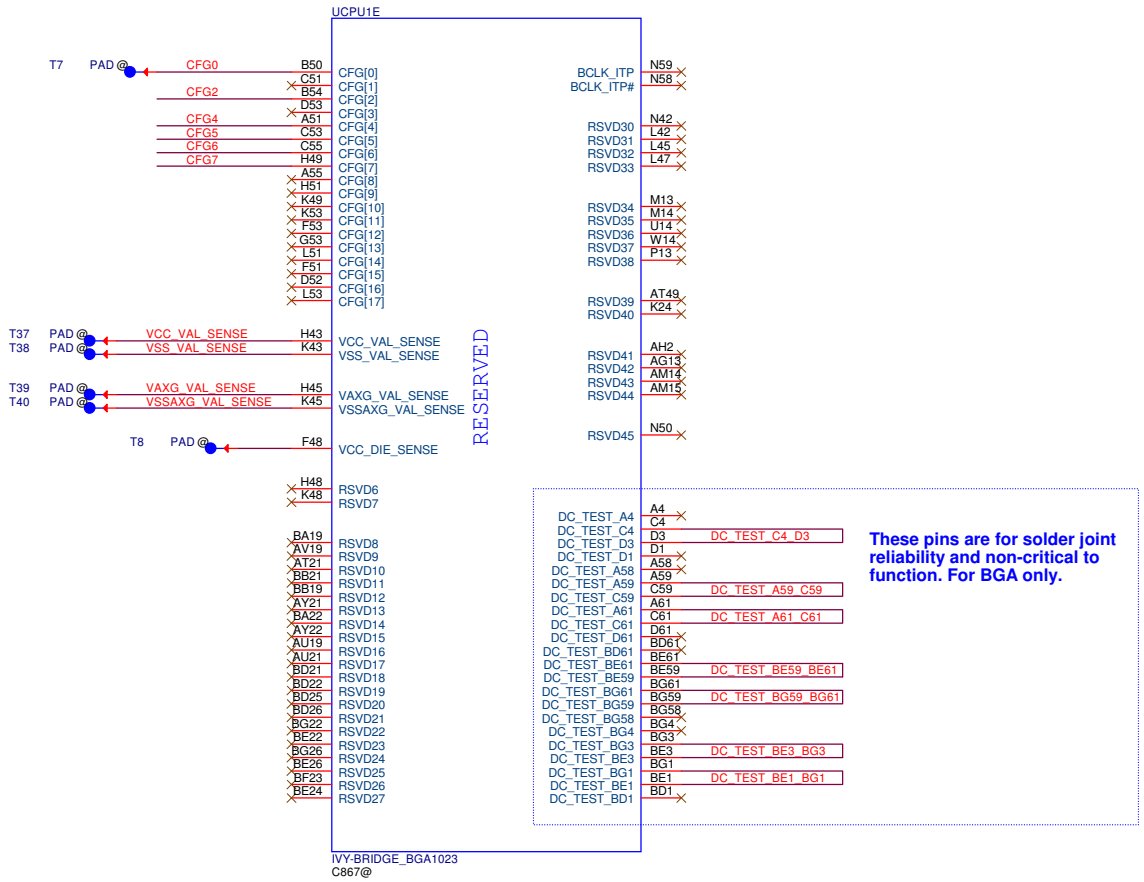
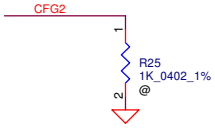
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: PROCESSOR(3/7) DDRIII			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 6 of 45		

CFG Straps for Processor

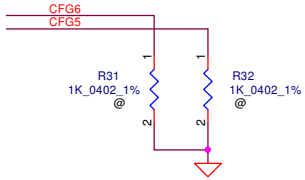


These pins are for solder joint reliability and non-critical to function. For BGA only.

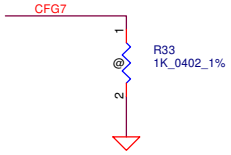


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

eDP enable	
CFG4	* 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express *10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 7 of 45

POWER

ULV type
DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F32
VCC[32] F34
VCC[33] F37
VCC[34] F38
VCC[35] F42
VCC[36] G42
VCC[37] H25
VCC[38] H26
VCC[39] H28
VCC[40] H29
VCC[41] H32
VCC[42] H34
VCC[43] H35
VCC[44] H37
VCC[45] H38
VCC[46] H40
VCC[47] J25
VCC[48] J26
VCC[49] J28
VCC[50] J29
VCC[51] J32
VCC[52] J34
VCC[53] J35
VCC[54] J37
VCC[55] J38
VCC[56] J40
VCC[57] J42
VCC[58] K26
VCC[59] K27
VCC[60] K29
VCC[61] K32
VCC[62] K34
VCC[63] K35
VCC[64] K37
VCC[66] K39
VCC[67] K42
VCC[68] L25
VCC[69] L28
VCC[70] L33
VCC[71] L36
VCC[72] L40
VCC[73] N26
VCC[74] N30
VCC[75] N34
VCC[76] N38

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

For PEG

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

+1.05VS_VTT
VCCIO50 W16
VCCIO51 W17

+3VS
R34 10K_0402_5% @
VCCIO_SEL
R35 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support		
BC22	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL
BC22 VCCIO_SEL

QUIET RAILS

VCCPQE[1] AM25
VCCPQE[2] AN22
+1.05VS_VTT
C69 1U_0402_6.3V6K

+1.05VS_VTT
R36 130_0402_5%

+1.05VS_VTT
R37 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43 H_CPU_SVIDCLK
VIDSOUT C44 H_CPU_SVIDDAT

R38 43_0402_1% SVID_ALERT# <41>
R39 0_0402_5% SVID_CLK <41>
R40 0_0402_5% SVID_DATA <41>

+CPU_CORE
R41 100_0402_1%

Place the PU resistors close to VR

SENSE LINES

VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R
R42 0_0402_5% VCCSENSE <41>
R43 0_0402_5% VSSSENSE <41>

R44 10_0402_5% +1.05VS_VTT
VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17
VSSIO_SENSE
VCCIO_SENSE <40>
R45 100_0402_1%
R46 10_0402_5%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

Check list 1.5

IVY-BRIDGE_BGA1023
C867@

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PROCESSOR(5/7) PWR,BYPASS		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 8 of 45		

POWER

UCPU1G

INTEL Recommend VAXG
2*470uF,6*22uF(0805) and 6*10uF(0603)
11*1U(0402)
PD0.8

+VGFX_CORE — DC 16A

VAXG[1] AA46
VAXG[2] AB47
VAXG[3] AB50
VAXG[4] AB51
VAXG[5] AB52
VAXG[6] AB53
VAXG[7] AB55
VAXG[8] AB56
VAXG[9] AB58
VAXG[10] AB59
VAXG[11] AC61
VAXG[12] AD47
VAXG[13] AD48
VAXG[14] AD50
VAXG[15] AD51
VAXG[16] AD52
VAXG[17] AD53
VAXG[18] AD55
VAXG[19] AD56
VAXG[20] AD58
VAXG[21] AD59
VAXG[22] AE46
VAXG[23] N45
VAXG[24] P47
VAXG[25] P48
VAXG[26] P50
VAXG[27] P51
VAXG[28] P52
VAXG[29] P53
VAXG[30] P55
VAXG[31] P56
VAXG[32] P61
VAXG[33] T48
VAXG[34] T58
VAXG[35] T59
VAXG[36] T61
VAXG[37] U46
VAXG[38] V47
VAXG[39] V48
VAXG[40] V50
VAXG[41] V51
VAXG[42] V52
VAXG[43] V53
VAXG[44] V55
VAXG[45] V56
VAXG[46] V58
VAXG[47] V59
VAXG[48] W50
VAXG[49] W51
VAXG[50] W52
VAXG[51] W53
VAXG[52] W55
VAXG[53] W56
VAXG[54] W61
VAXG[55] Y48
VAXG[56] Y61

GRAPHICS

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8

CR CheckList Rev1.5

+VGFX_CORE
R51 100_0402_5%
R52 100_0402_5%

<41> VCC_GFXSENSE
<41> VSS_GFXSENSE

VAXG_SENSE F45
VSSAXG_SENSE G45

SENSE LINES

1.2A

VCCPLL[1] BB3
VCCPLL[2] BC1
VCCPLL[3] BC4

1.8V RAIL

+1.8VS
Place BOT OUT Conn
C91 @ 220U_B2_2.5VM_R35
C92 1U_0402_6.3V6K
C93 1U_0402_6.3V6K

SGA00001700 S POLY C 220U
220U 2.5V M B2 ESR35 TPE H1.9

6A

VCCSA[1] L17
VCCSA[2] L21
VCCSA[3] N16
VCCSA[4] N20
VCCSA[5] N22
VCCSA[6] P17
VCCSA[7] P20
VCCSA[8] R16
VCCSA[9] R18
VCCSA[10] R21
VCCSA[11] U15
VCCSA[12] V16
VCCSA[13] V17
VCCSA[14] V18
VCCSA[15] V21
VCCSA[16] W20

SA RAIL

+VCCSA
Place TOP IN BGA
C94 330U_D2_2V_Y
C95 C96 C97 C98 C99 1U_0402_6.3V6K

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

Place BOT OUT BGA
C100 C101 C102 C103 C104 10U_0603_6.3V6M

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.8

IVY-BRIDGE_BGA1023
C867@

VREF

SM_VREF AY43 +V_SM_VREF

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU_VDDQ
R47 1K_0402_5%
R48 1K_0402_5%
C70 0.1U_0402_16V4Z

SA_DIMM_VREFDQ BE7
SB_DIMM_VREFDQ BG7

SA_DIMM_VREFDQ <11>
SB_DIMM_VREFDQ <12>

R49 1K_0402_1% @
R50 1K_0402_1% @

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
Check list1.5 P18 M1 default M3 no stuff

DDR3 - 1.5V RAILS

5A

VDDQ[1] AJ28
VDDQ[2] AJ33
VDDQ[3] AJ36
VDDQ[4] AJ40
VDDQ[5] AL30
VDDQ[6] AL34
VDDQ[7] AL38
VDDQ[8] AL42
VDDQ[9] AM33
VDDQ[10] AM36
VDDQ[11] AM40
VDDQ[12] AN30
VDDQ[13] AN34
VDDQ[14] AN38
VDDQ[15] AR26
VDDQ[16] AR28
VDDQ[17] AR30
VDDQ[18] AR32
VDDQ[19] AR34
VDDQ[20] AR36
VDDQ[21] AR40
VDDQ[22] AV41
VDDQ[23] AW26
VDDQ[24] BA40
VDDQ[25] BB28
VDDQ[26] BG33

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.8

Place TOP IN BGA
C71 C72 C73 C74 C75 C76 C77 C78 C79 C80 1U_0402_6.3V6K

Place BOT OUT BGA
C82 C83 C84 C85 C86 C87 C88 C89 10U_0603_6.3V6M

+1.5V_CPU_VDDQ
J1 JUMP_43X118 @
+1.5VS
C81 330U_D2_2V_Y

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

QUIET RAILS

VCCDQ[1] AM28
VCCDQ[2] AN26

+1.5V_CPU_VDDQ
C90 1U_0402_6.3V6K

SENSE LINES

VDDQ_SENSE BC43
VSS_SENSE_VDDQ BA43

VCCSA_SENSE U10
CPU EDS1.3 P.93
VCCSA_VID0 Must PD

VCCSA_SENSE <39>

VCCSA VID lines

VCCSA_VID[0] D48
VCCSA_VID[1] D49

H_VCCSA_VID0 <39>
H_VCCSA_VID1 <39>

R53 0_0402_5% @

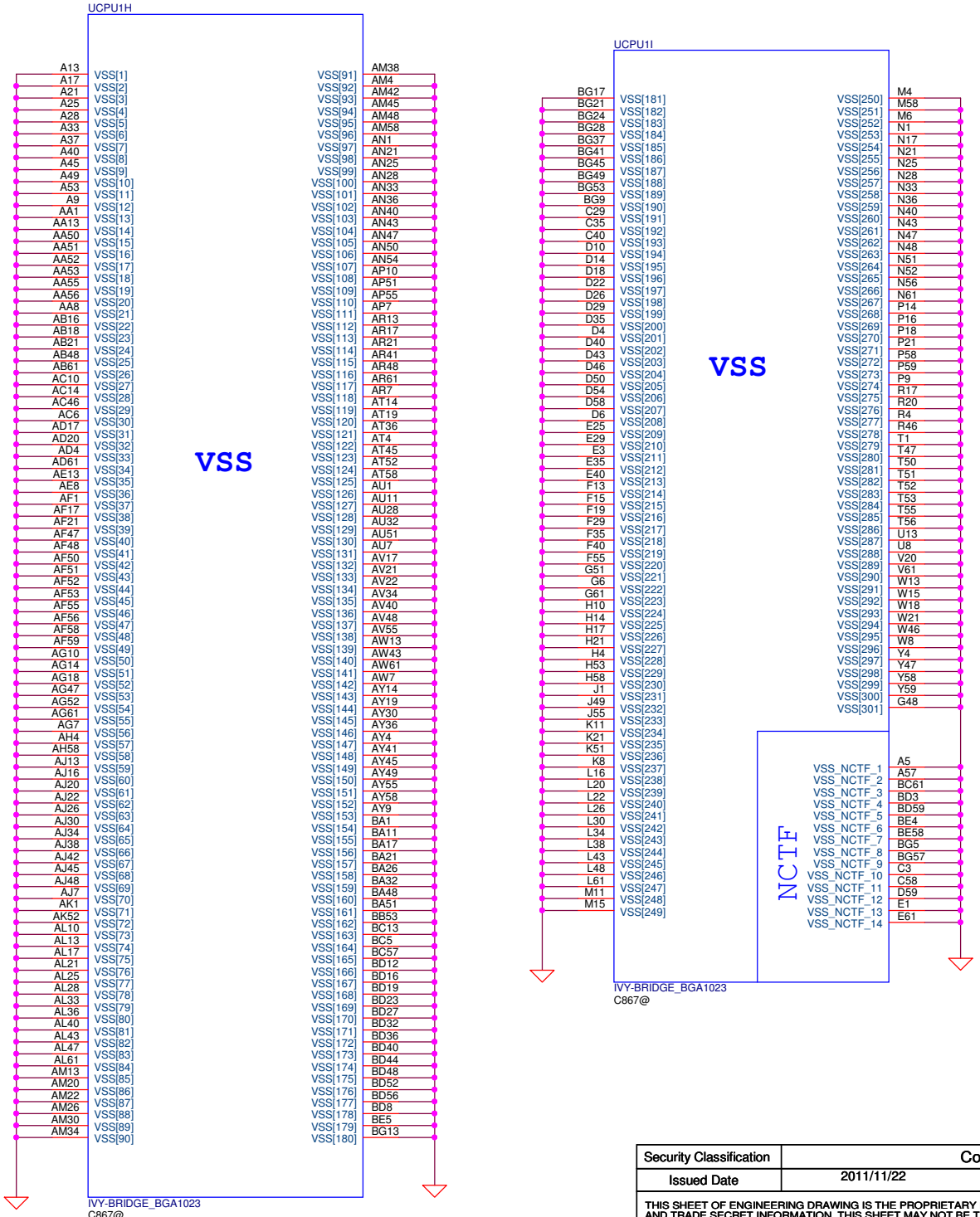
VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 9 of 45



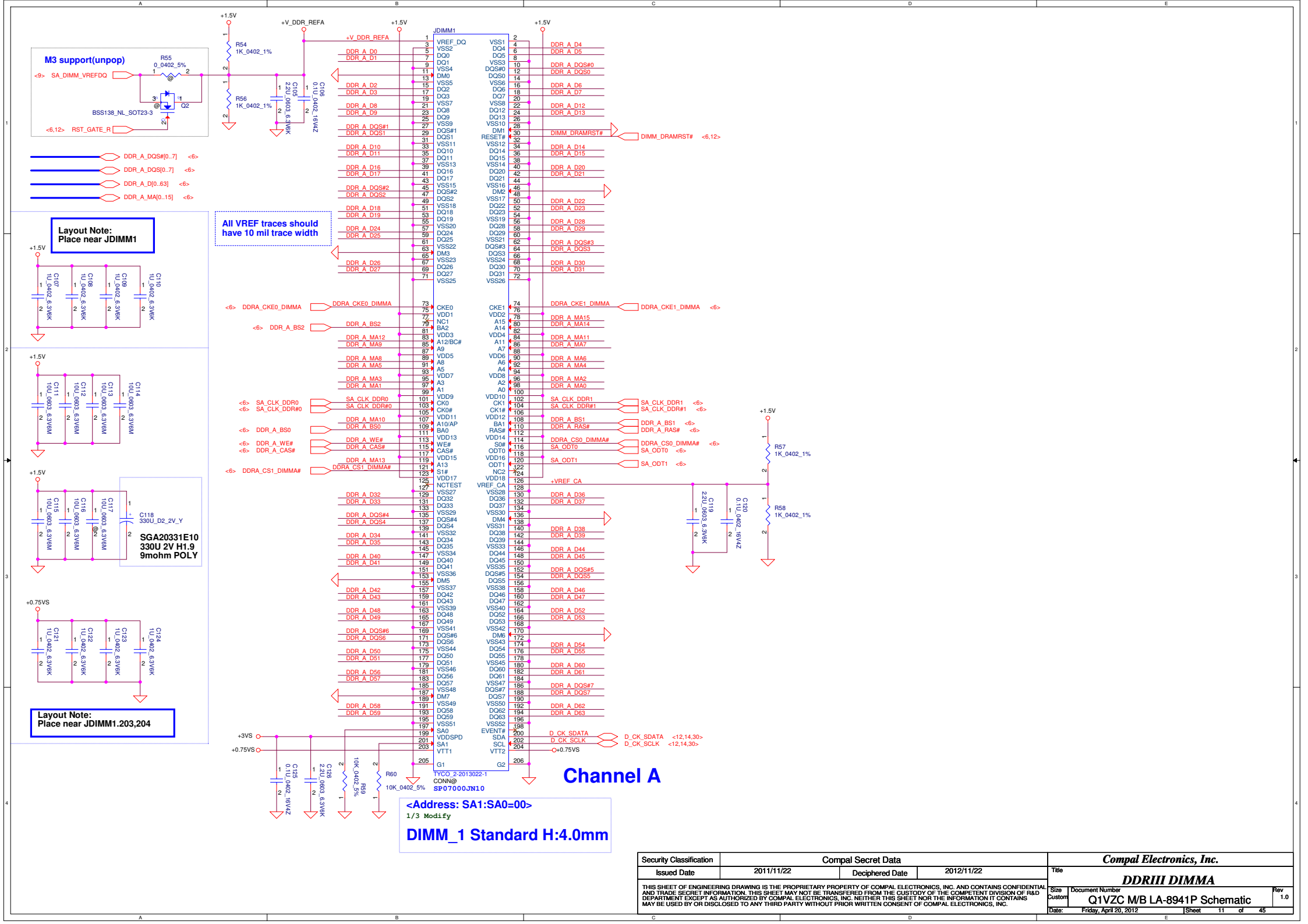
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

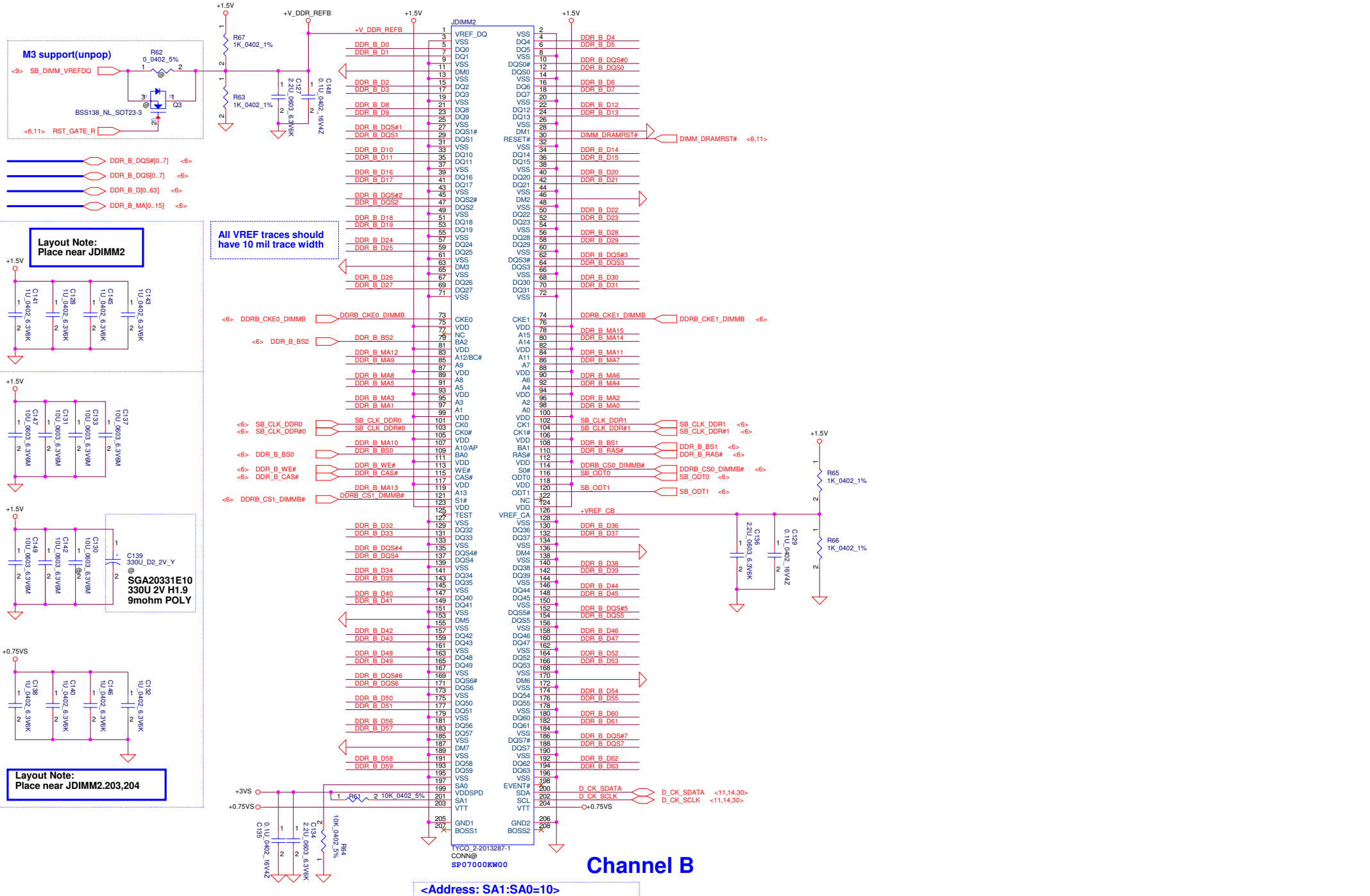
Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 10 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 11 of 45		



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet: 12 of 45		

RTCRST close RAM door J1

+RTCVCC
C163 1U_0603_10V6K
R74 0_0603_5%
R75 20K_0402_5%
R76 20K_0402_5%
PCH_RTCRST#
PCH_SRTCRST#
C164 1U_0603_10V6K
R77 0_0603_5%

+RTCVCC
R78 1M_0402_5% SM_INTRUDER#
R79 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R82 1K_0402_5% PCH_SPKR

HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+VCCSUS3_3
R84 1K_0402_5%
R83 0_0402_5%
HDA_SDOUT_PCH
<29> HDA_SDO

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disable (Default)
High = Enabled [Flash Descriptor Security Overide]

+VCCSUS3_3
R87 1K_0402_5% HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<31> HDA_BITCLK_AUDIO R88 33_0402_5% HDA_BITCLK_PCH
<31> HDA_SYNC_AUDIO R89 33_0402_5% HDA_SYNC_PCH_R
<31> HDA_RST_AUDIO# R92 33_0402_5% HDA_RST_PCH#
<31> HDA_SDOUT_AUDIO R95 33_0402_5% HDA_SDOUT_PCH

PCH_RTCX1
PCH_RTCX2
R107 10M_0402_5%
Y1 32.768KHZ_12.5PF_1TJF125DP1A000D
18P_0402_50V8J C167
C168 18P_0402_50V8J

U16 3/7 Add
BD82HM70
HM70@
SA00005MQ60

11/30 Add (EMI request)
HDA_BITCLK_AUDIO
C467 22P_0402_50V8J

Prevent back drive issue.
+5VS
Q4 BSS138_NL_SOT23-3
HDA_SYNC_PCH
R90 0_0402_5%
R93 1M_0402_5%

U16A

PCH_RTCX1	A20	RTCX1	RTC
PCH_RTCX2	C20	RTCX2	
PCH_RTCRST#	D20	RTCRST#	
PCH_SRTCRST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA
HDA_SYNC_PCH	L34	HDA_SYNC	
PCH_SPKR	T10	SPKR	
HDA_RST_PCH#	K34	HDA_RST#	
HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
HDA_SDOUT_PCH	A36	HDA_SDO	
	C36	HDA_DOCK_EN# / GPIO33	
	N32	HDA_DOCK_RST# / GPIO13	
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG
PCH_JTAG_TMS	H7	JTAG_TMS	
PCH_JTAG_TDI	K5	JTAG_TDI	
PCH_JTAG_TDO	H1	JTAG_TDO	
PCH_SPI_CLK	T3	SPI_CLK	SPI
PCH_SPI_CS0#	Y14	SPI_CS0#	
PCH_SPI_CS1#	T1	SPI_CS1#	
PCH_SPI_MOSI	V4	SPI_MOSI	
	U3	SPI_MISO	
PCH_SPI_MISO			

COUGARPOINT_FCBGA989
HM77@

FWH0 / LAD0	C38	LPC_AD0	LPC_AD0 <29,30>
FWH1 / LAD1	A38	LPC_AD1	LPC_AD1 <29,30>
FWH2 / LAD2	B37	LPC_AD2	LPC_AD2 <29,30>
FWH3 / LAD3	C37	LPC_AD3	LPC_AD3 <29,30>
FWH4 / LFRAME#	D36	LPC_FRAME#	LPC_FRAME# <29,30>
LDRQ0#	E36		
LDRQ1# / GPIO23	K36	PCH_GPIO23	
SERIRQ	V5	SERIRQ	SERIRQ <29,30>

SATA0RXN	AM3	SATA_PRX_DTX_N0	<24>
SATA0RXP	AM1	SATA_PRX_DTX_P0	<24>
SATA0TXN	AP7	SATA_PTX_DRX_N0	<24>
SATA0TXP	AP5	SATA_PTX_DRX_P0	<24>
SATA1RXN	AM10		
SATA1RXP	AM8		
SATA1TXN	AP11		
SATA1TXP	AP10		
SATA2RXN	AD7		
SATA2RXP	AD5		
SATA2TXN	AH5		
SATA2TXP	AH4		
SATA3RXN	AB8		
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11		
SATAICOMPI	Y10	SATA_COMP	R94 37.4_0402_1%
SATA3RCOMPO	AB12		
SATA3COMPI	AB13	SATA3_COMP	R97 49.9_0402_1%
SATA3RBIAS	AH1	RBIAS_SATA3	R99 750_0402_1%
SATALED#	P3	PCH_SATALED#	
SATA0GP / GPIO21	V14	PCH_GPIO21	
SATA1GP / GPIO19	P1	PCH_GPIO19	

SATA 6G
SATA

HDD1
12/1 Del
HM70 not support SATA for port1/port3
L=500mil S=15mil
+1.05VS_VTT
No use PU 10K +3VS
GPIO19 has internal Pull up

PCH_SPI_CLK_2 R96 33_0402_5%
PCH_SPI_CLK_1 R98 33_0402_5%
PCH_SPI_CS0#_1 R100 33_0402_5%
PCH_SPI_CS1#_2 R101 33_0402_5%
PCH_SPI_MOSI_2 R103 33_0402_5%
PCH_SPI_MOSI_1 R104 33_0402_5%
PCH_SPI_MISO_1 R105 33_0402_5%
PCH_SPI_MISO_2 R106 33_0402_5%

PAD T9 PCH_JTAG_TCK (R91 51_0402_5%)
PAD T10 PCH_JTAG_TMS
PAD T11 PCH_JTAG_TDI
PCH_JTAG_TDO

U17
+3VS
R109 3.3K_0402_5% SPI_WP1#
R108 3.3K_0402_5% SPI_HOLD1#
PCH_SPI_CS0#_1
PCH_SPI_CLK_1
PCH_SPI_MISO_1
PCH_SPI_MOSI_1
CS# WP# HOLD# GND VCC SCLK SI SO
MX25L3206EM2I-12G_SO8
SA000041P00

SPI ROM FOR ME (4MB)
Footprint 200mil

12/7 Change symbol of U18 from SA00000XT00 to SA000041O00
U18
+3VS
R111 3.3K_0402_5%
R112 3.3K_0402_5%
PCH_SPI_CS1#_2
PCH_SPI_MISO_2
SPI_WP2#
SPI_HOLD2#
PCH_SPI_CLK_2
PCH_SPI_MOSI_2
CS# SO WP# GND VCC HOLD# SCLK SI
MX25L8006EM2I-12G_SO8
SA000041O00

SPI ROM FOR ME (1MB)
Footprint 200mil

Reserve for EMI
PCH_SPI_CLK 33_0402_5% R110 C166 10P_0402_50V8J
11/30 Add
PCH_SPI_CLK_1 33_0402_5% R466 22P_0402_50V8J C465
PCH_SPI_CLK_2 33_0402_5% R467 22P_0402_50V8J C466

+RTCBATT
20mil
D1 BAS40-04_SOT23-3
+RTCVCC
20mil
+CHGRTC
C165 0.1U_0402_16V4Z
20mil

SERIRQ R80 10K_0402_5%
PCH_SATALED# R81 10K_0402_5%

+3VS
R230 10K_0402_5%
PCH_GPIO23
R234 1K_0402_5% @
R85 10K_0402_5%
PCH_GPIO21
R86 10K_0402_5% @

+3VS
R102 4.7K_0402_5%
PCH_GPIO19
Debug Port DG 1.2 PU 4.7K +3VS

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom
Document Number: Q1VZC M/B LA-8941P Schematic
Rev: 1.0
Date: Friday, April 20, 2012
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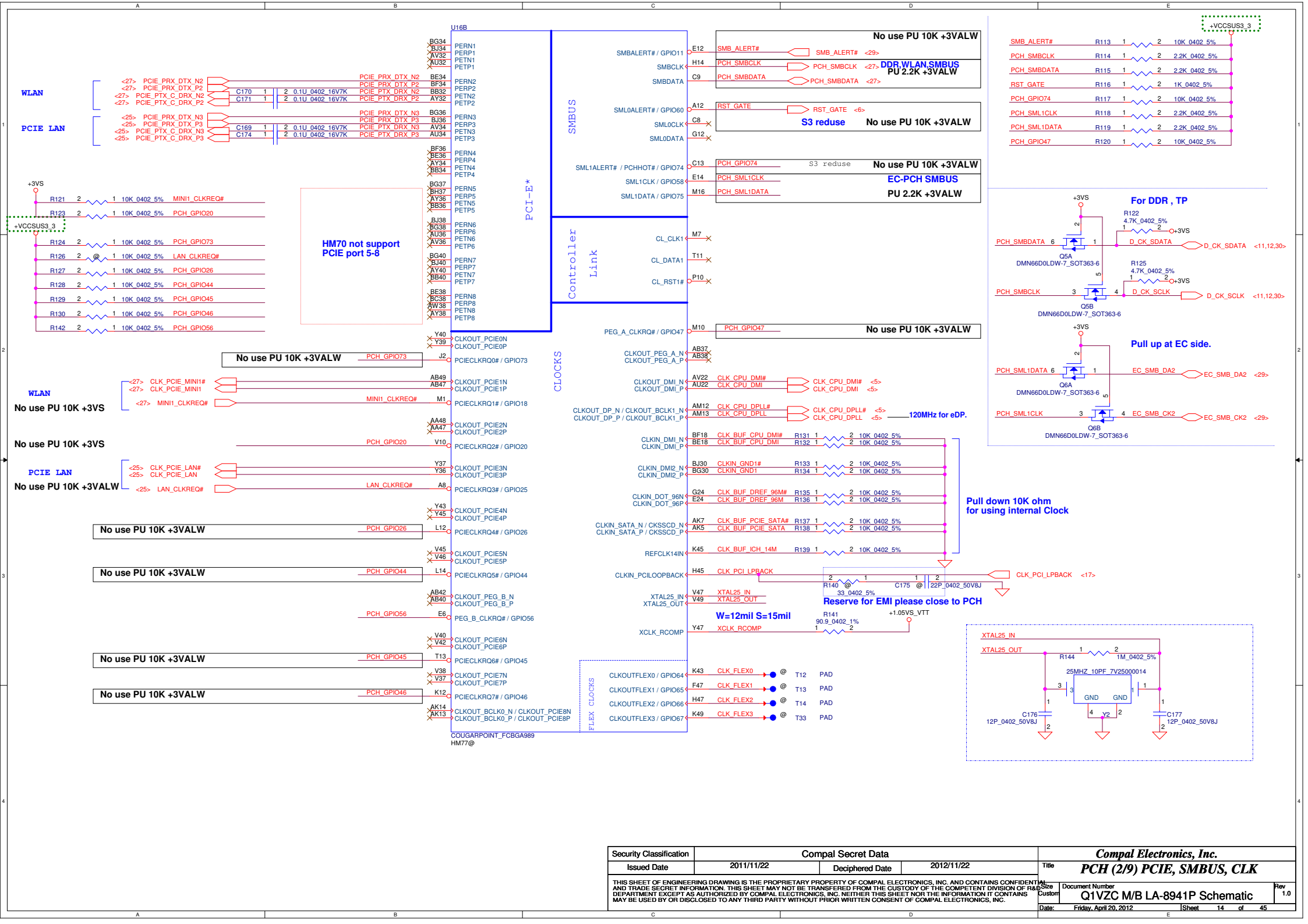
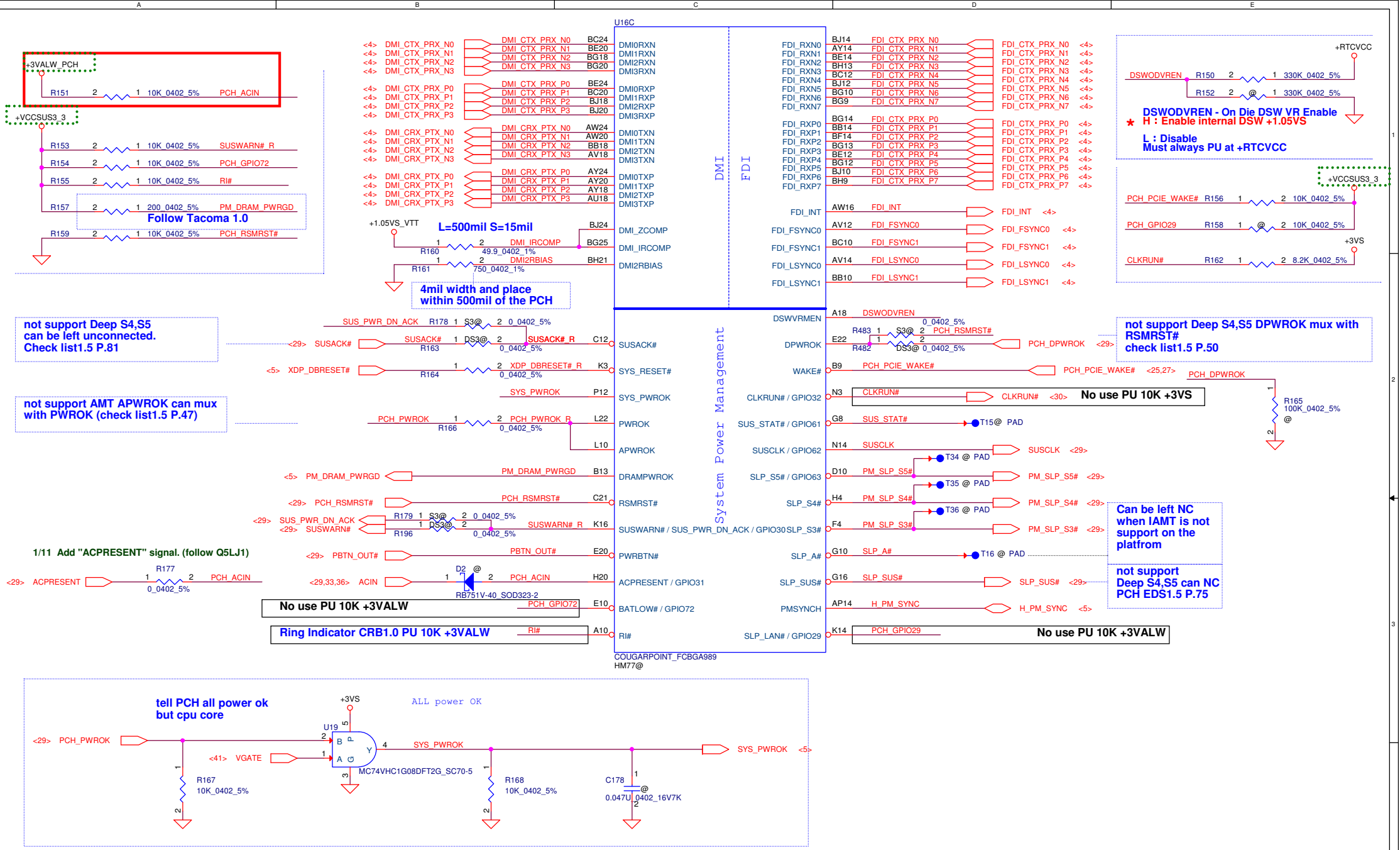


Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.	
Title	PCH (2/9) PCIE, SMBUS, CLK
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic
Rev: 1.0	
Date: Friday, April 20, 2012	Sheet 14 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title	PCH (3/9) DMI,FDI,PM		
Size	Document Number		Rev
Custom	Q1VZC M/B LA-8941P Schematic		1.0
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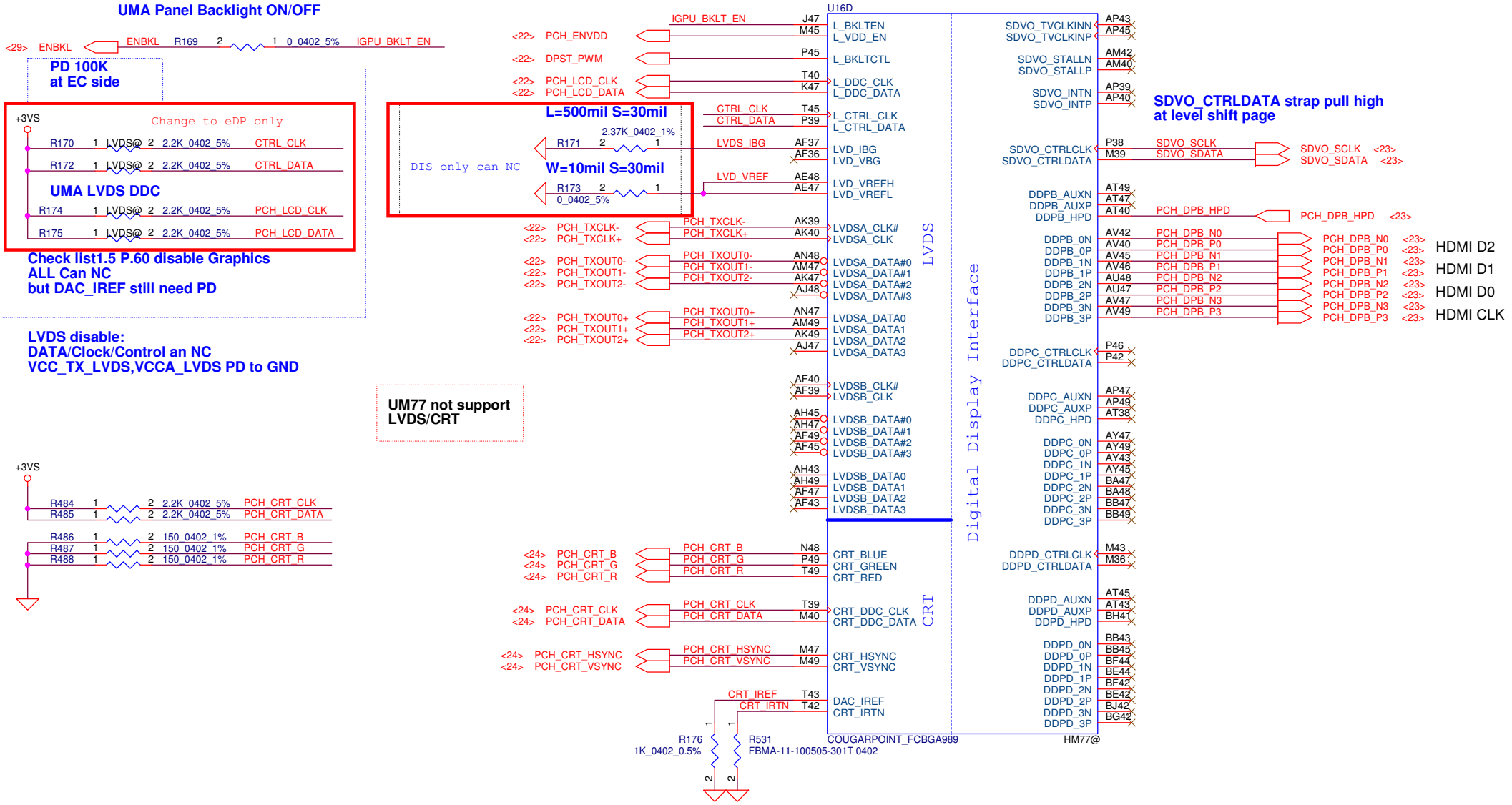


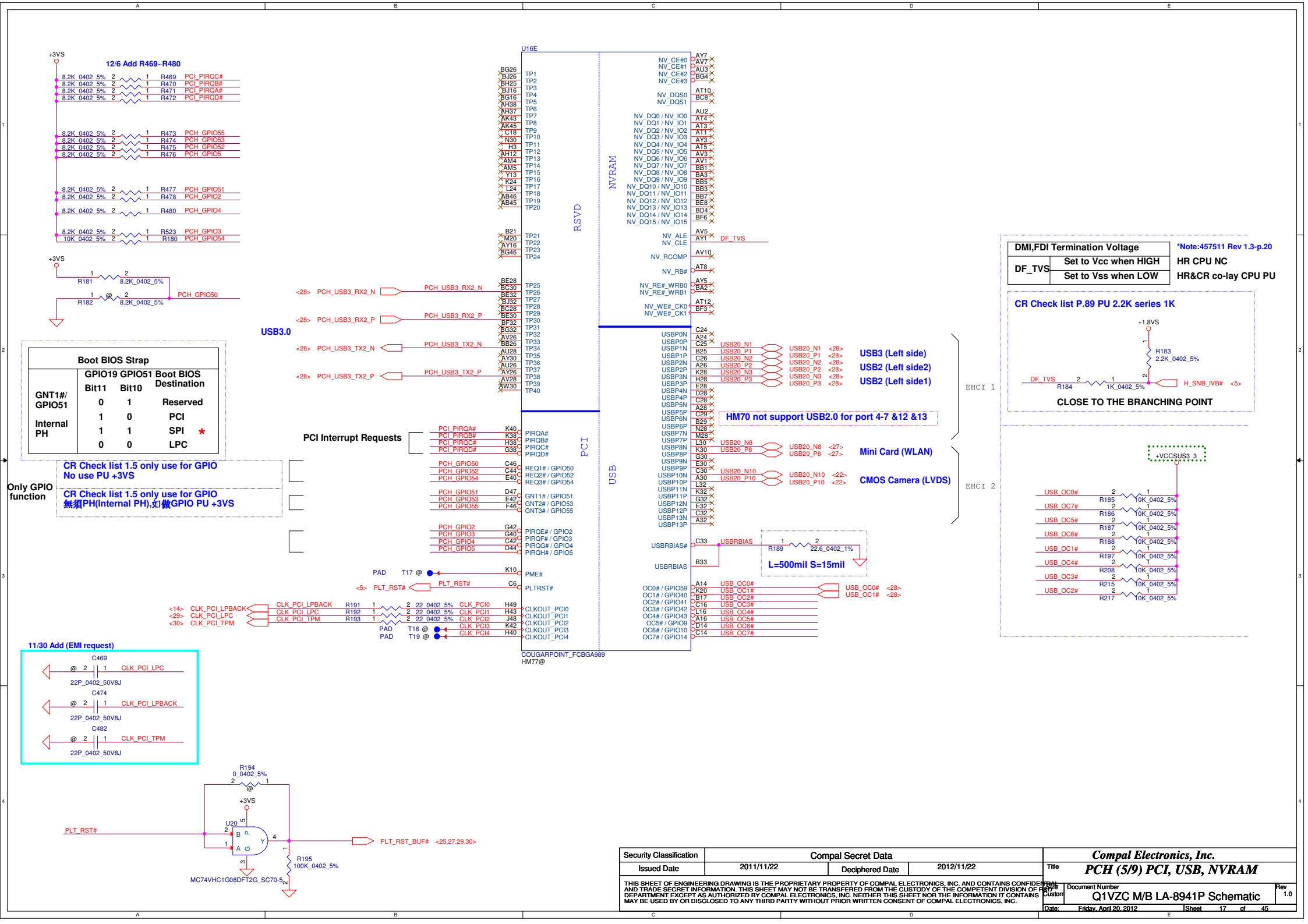
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

Date: Friday, April 20, 2012 Sheet 16 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+VCCSUS3_3

R202 4.7K_0402_5% — PCH_GPIO28

R205 1K_0402_5% — Debug Port DG 1.2 PU 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

R209 @ 10K_0402_5% PCH_GPIO27

+3VS

R211 200K_0402_5% PCH_GPIO36

+3VALW_PCH

R214 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled

+3VS

R216 10K_0402_5% PCH_GPIO0
R218 10K_0402_5% PCH_GPIO1
R219 10K_0402_5% PCH_GPIO6
R220 10K_0402_5% PCH_GPIO16
R221 10K_0402_5% PCH_GPIO17
R522 10K_0402_5% PCH_GPIO38 — 12/13 Add
R222 10K_0402_5% PCH_GPIO34
R223 10K_0402_5% PCH_GPIO48
R225 10K_0402_5% PCH_GPIO49

+VCCSUS3_3

R227 10K_0402_5% PCH_GPIO12
R228 1K_0402_5% EC_LID_OUT#
R232 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.

CRB1.0 PU 10K to +3VALW

+VCCSUS3_3

R224 10K_0402_5% PCH_GPIO24
R226 @ 10K_0402_5%

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

No use PU 10K +3VS	PCH_GPIO0	T7
No use PU 10K +3VS	PCH_GPIO1	A42
No use PU 10K +3VS	PCH_GPIO6	H36
No use PU 10K +3VS <29> EC_SCI#	EC_SCI#	E38
No use PU 10K +3VALW <29> EC_SMI#	EC_SMI#	C10
No use PU +3VALW	PCH_GPIO12	C4
No use PU +3VALW <29> EC_LID_OUT#	EC_LID_OUT#	G2
No use PU +3VS	PCH_GPIO16	U2
No use PU +3VS	PCH_GPIO17	D40
No use PU 10K +3VS RAM flag	PCH_GPIO22	T5
No use PU +3VALW DDR3/DDR3L	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	E16
No use PU 10K +3VALW	PCH_GPIO28	P8
No use PU 10K +3VS BT ON/OFF	PCH_GPIO34	K1
No use can NC PAD T20 @	PCH_GPIO35	K4
Can't PU	PCH_GPIO36	V8
Can't PU PAD T21 @	PCH_GPIO37	M5
No use PU 10K +3VS	PCH_GPIO38	N2
No use PU 10K +3VS RAM flag	PCH_GPIO39	M3
No use PU 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3
No use PU +3VALW	PCH_GPIO57	D6

11/21 EDP@->POP

LVDS/eDP	GPIO71
LVDS	1
eDP	0

+3VS

R198 10K_0402_5% LVDS@ — PCH_GPIO71
R201 10K_0402_5% EDP@
R199 10K_0402_5% @ — PCH_GPIO69
R203 10K_0402_5%
R200 10K_0402_5%@ — PCH_GPIO70
R204 10K_0402_5%

U16F

BMBUSY# / GPIO0 — T7
TACH1 / GPIO1 — A42
TACH2 / GPIO6 — H36
TACH3 / GPIO7 — E38
GPIO8 — C10
LAN_PHY_PWR_CTRL / GPIO12 — C4
GPIO15 — G2
SATA4GP / GPIO16 — U2
TACH0 / GPIO17 — D40
SCLOCK / GPIO22 — T5
GPIO24 / MEM_LED — E8
GPIO27 — E16
GPIO28 — P8
STP_PCI# / GPIO34 — K1
GPIO35 — K4
SATA2GP / GPIO36 — V8
SATA3GP / GPIO37 — M5
SLOAD / GPIO38 — N2
SDATAOUT0 / GPIO39 — M3
SDATAOUT1 / GPIO48 — V13
SATA5GP / GPIO49 — V3
GPIO57 — D6

TACH4 / GPIO68 — C40 PCH_GPIO68
TACH5 / GPIO69 — B41 PCH_GPIO69
TACH6 / GPIO70 — C41 PCH_GPIO70
TACH7 / GPIO71 — A40 PCH_GPIO71

GPIO

CPU/MISC

A20GATE — P4
PECI — AU16 PCH_PECI_R 0_0402_5% R207 — H_PECI <5,29>
RCIN# — P5 EC_KBRST# — EC_KBRST# <29>
PROCPWRGD — AY11 — H_CPUPWRGD <5>
THRMTRIP# — AY10 PCH_THRMTRIP#_R R210 390_0402_5% — H_THRMTRIP# <5>
INIT3_3V# — T14

+3VS

R206 10K_0402_5% — GATEA20 <29>

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

NC_1 — AH8
NC_2 — AK11
NC_3 — AH10
NC_4 — AK10
NC_5 — P37

TS_VSS1~4
PD to GND

+3VS

EC_KBRST# R212 10K_0402_5%
PCH_GPIO68 R213 10K_0402_5%

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49

VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

NCTF

9/15 Layout request remove Test point They will route by itself

9/15 Layout request remove Test point They will route by itself

COUGARPOINT_FCBGA989
HM77@

+3VS

R229 10K_0402_5% — PCH_GPIO39
R233 10K_0402_5% @
R231 10K_0402_5% — PCH_GPIO22
R235 10K_0402_5% @

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

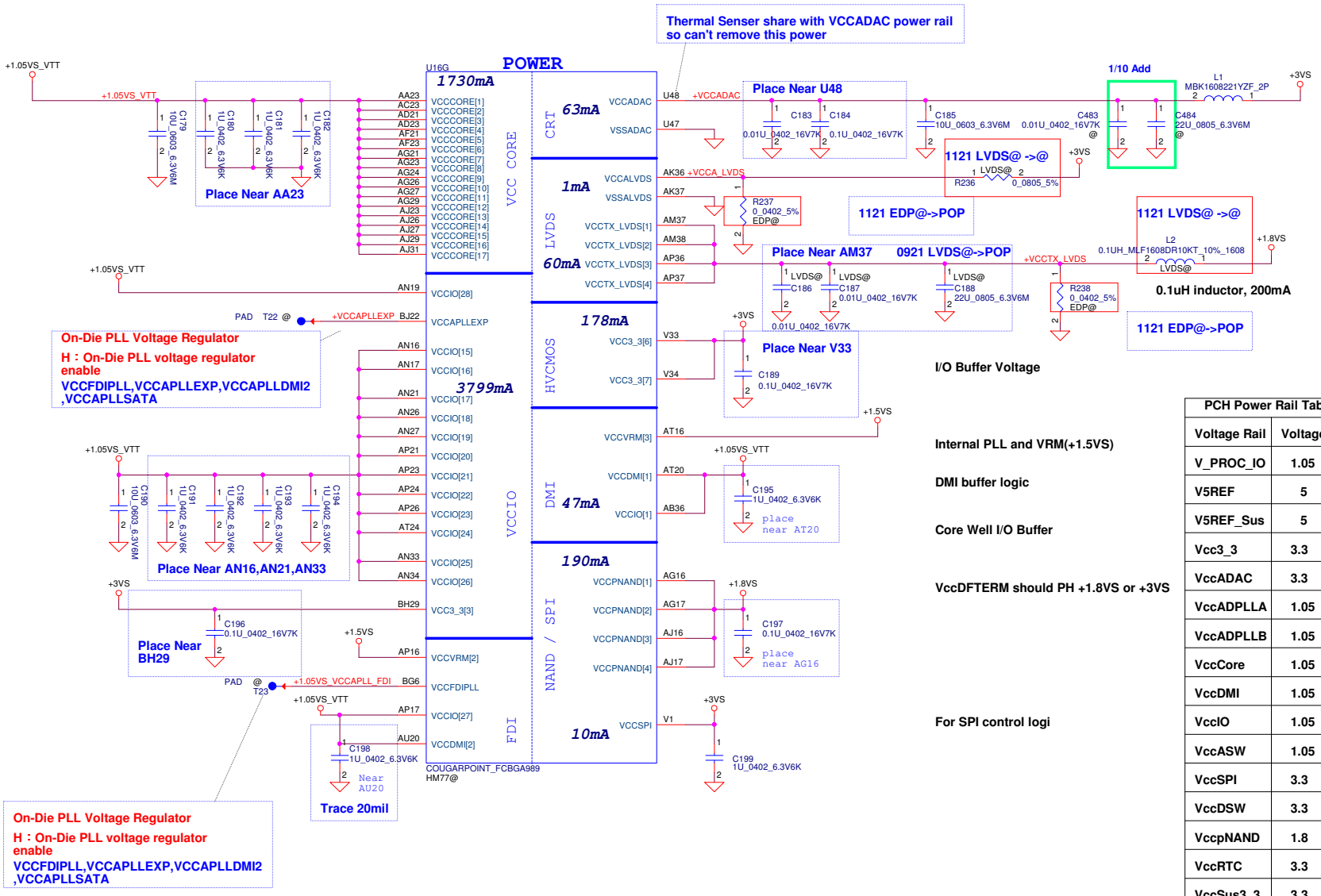
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 18 of 45



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Buffer Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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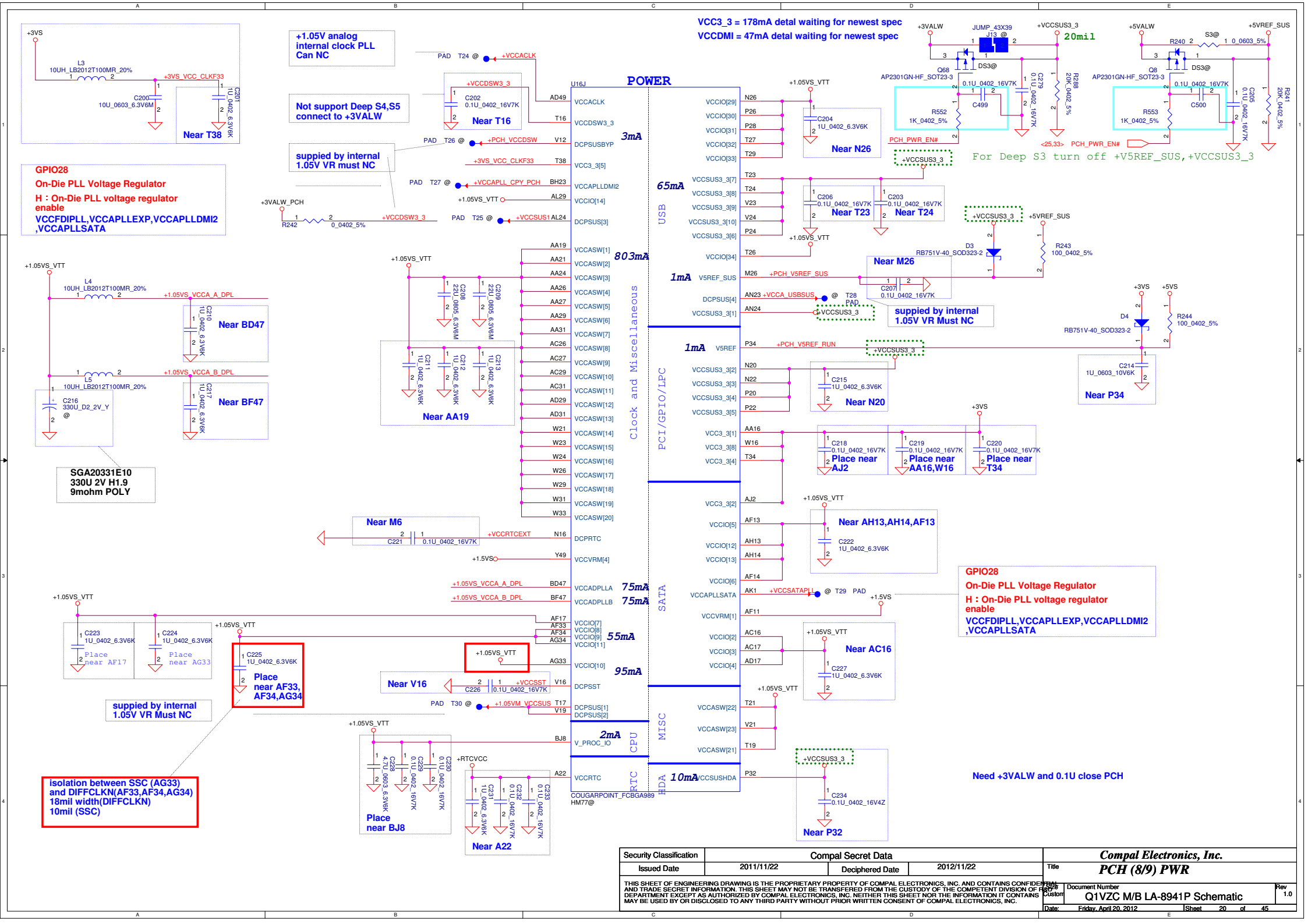
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.			
Title: PCH (7/9) PWR			
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 19 of 45		


VCC3_3 = 178mA detal waiting for newest spec
VCCDMI = 47mA detal waiting for newest spec
POWER
+1.05V analog internal clock PLL Can NC
Not support Deep S4,S5 connect to +3VALW
suppied by internal 1.05V VR must NC
GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA
SGA20331E10
330U 2V H1.9
9mohm POLY
isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)
For Deep S3 turn off +V5REF_SUS,+VCCSUS3_3
Need +3VALW and 0.1U close PCH
U16J
COUGARPOINT_FCBGA989
HM77@
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
Compal Electronics, Inc.
PCH (8/9) PWR
Q1VZC M/B LA-8941P Schematic
Rev 1.0
Friday, April 20, 2012
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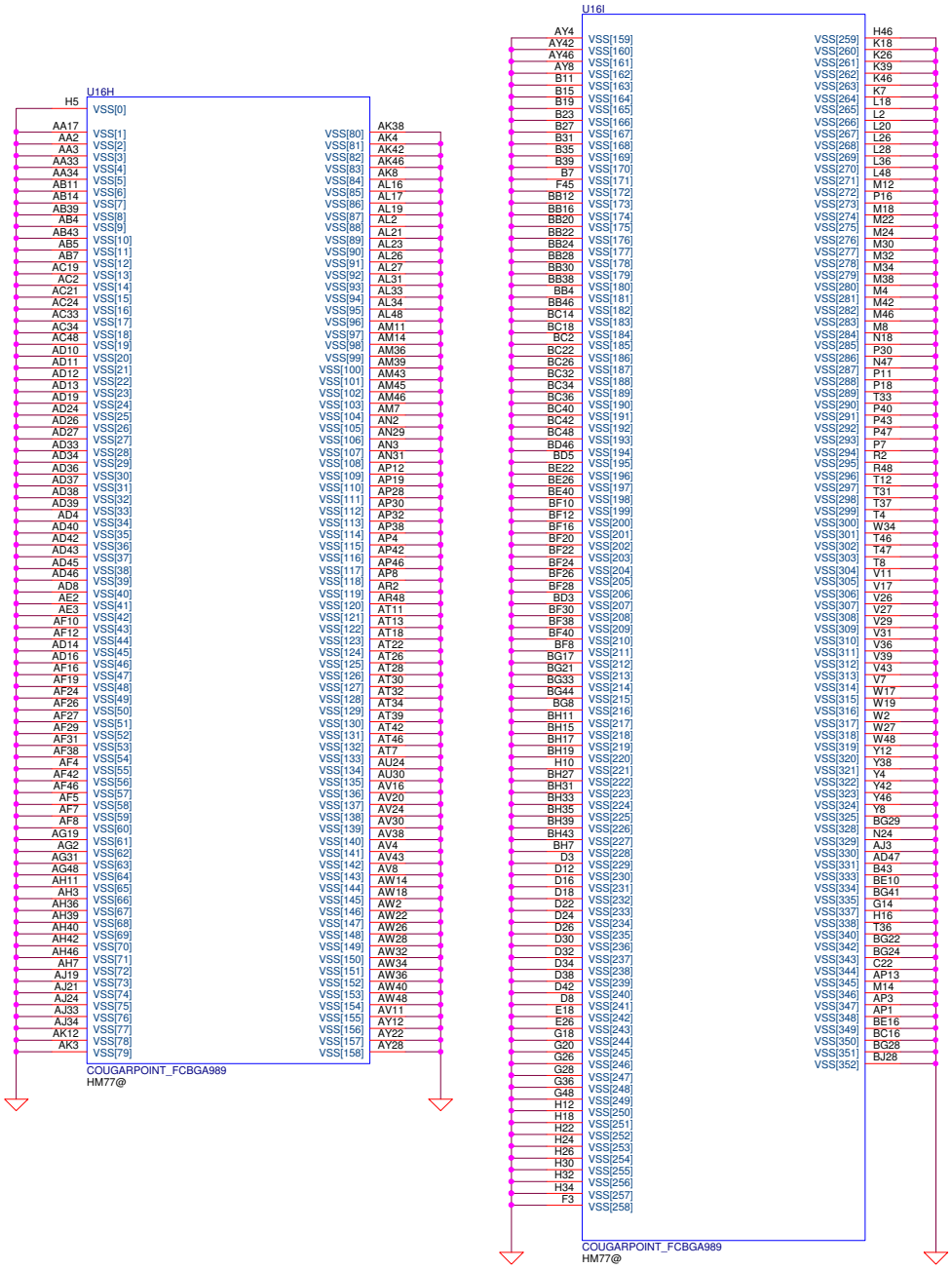
Security Classification
Compal Secret Data
Issued Date 2011/11/22
Deciphered Date 2012/11/22



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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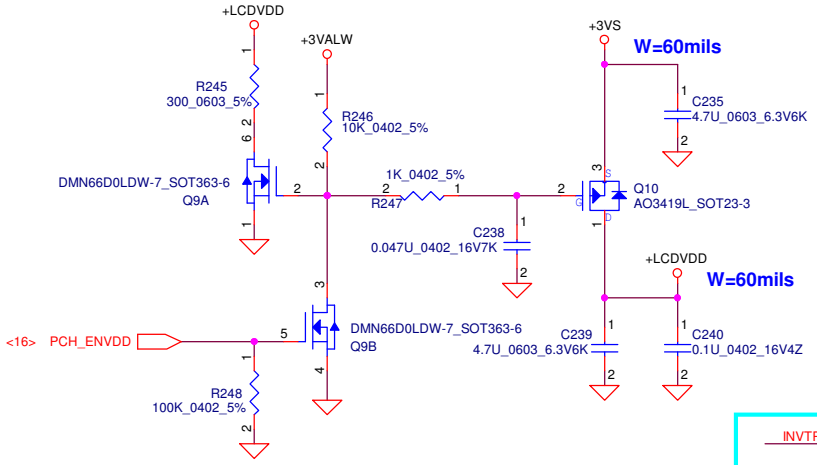
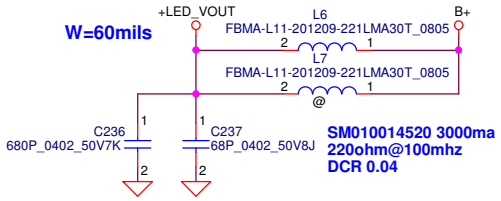
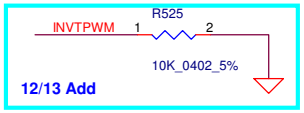
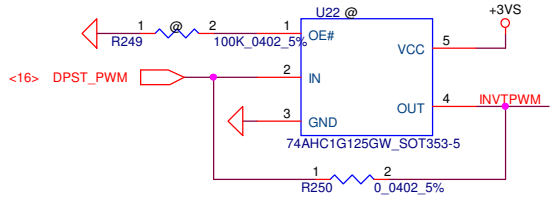
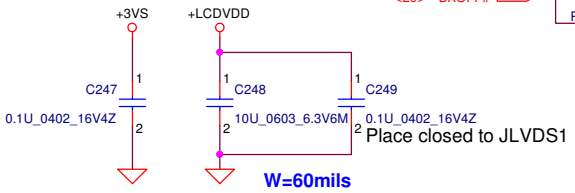
LCD POWER CIRCUIT



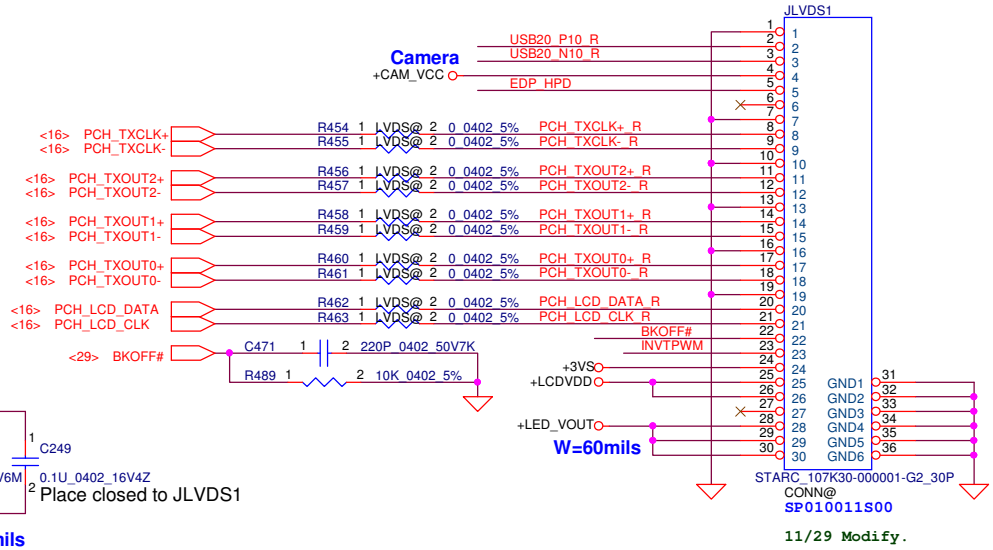


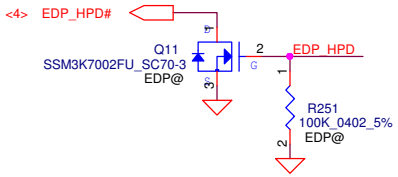




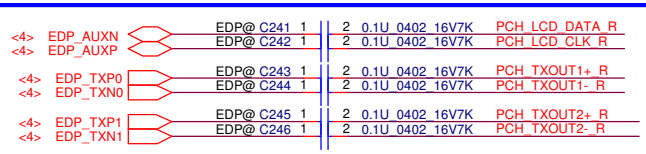


LCD/LED PANEL Conn.

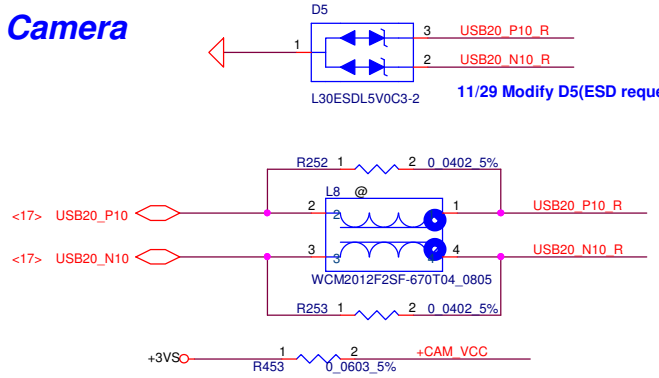




eDP



Camera



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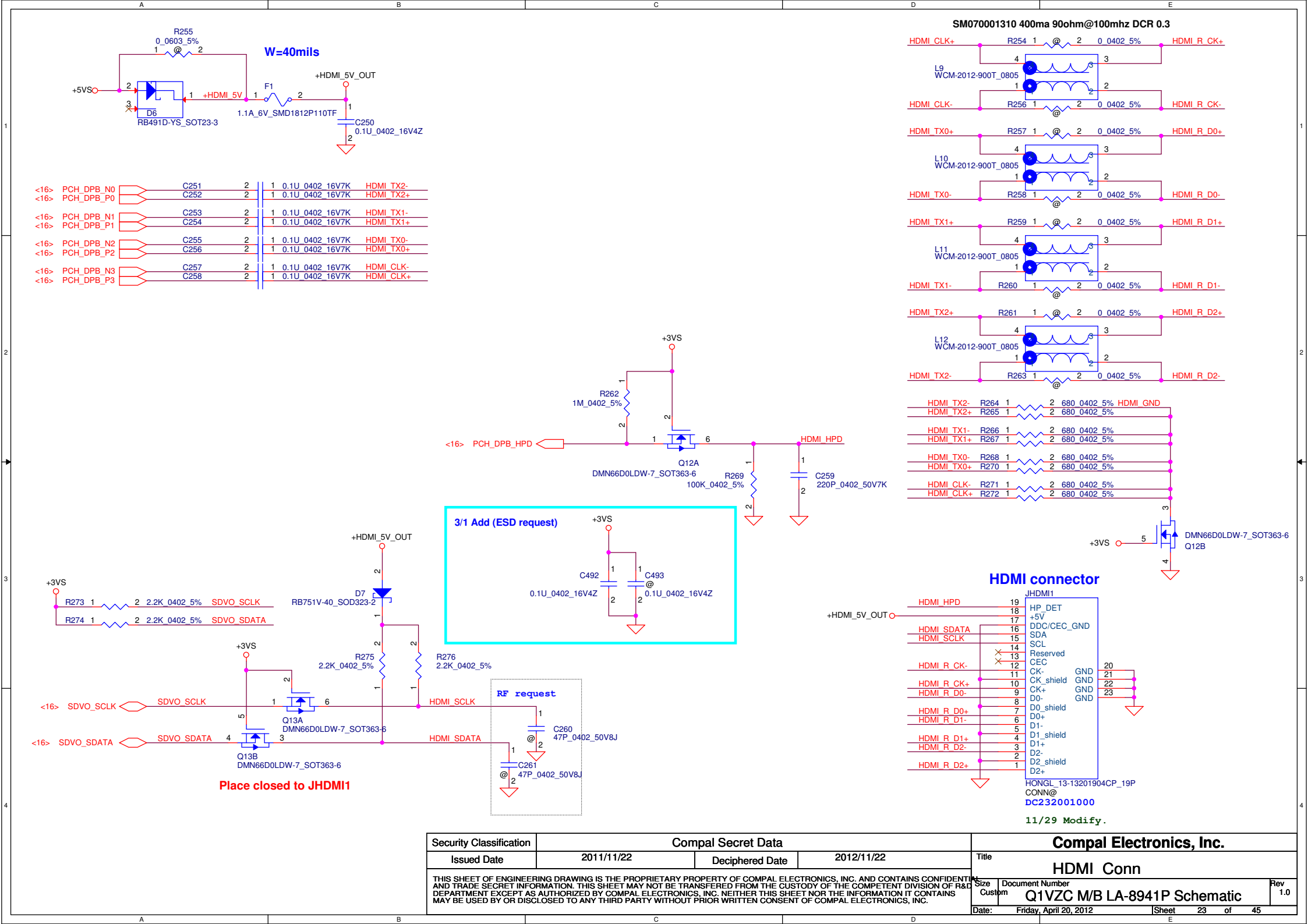
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: LVDS&eDP

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 22 of 45



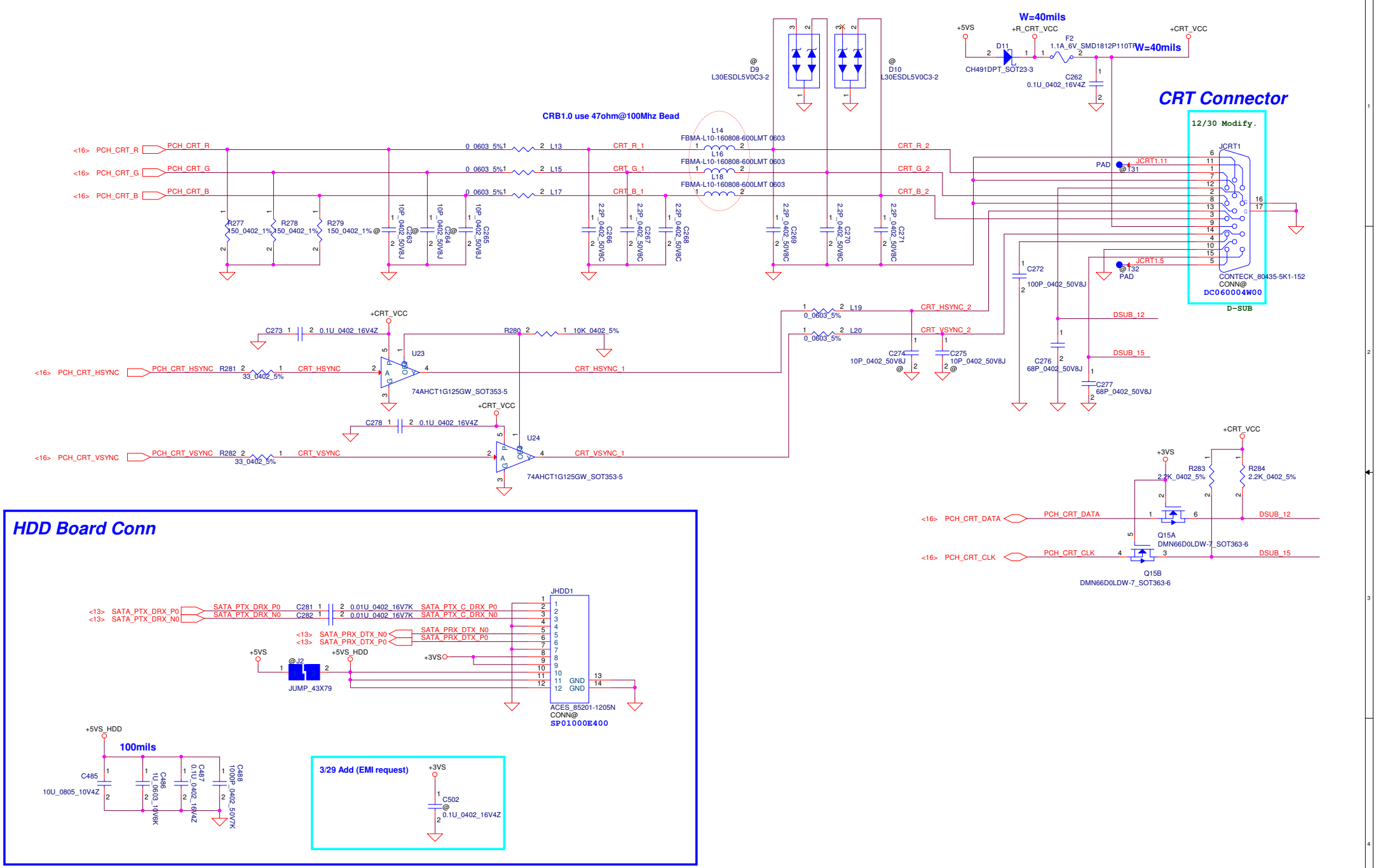
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: HDMI Conn

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

Date: Friday, April 20, 2012 Sheet 23 of 45



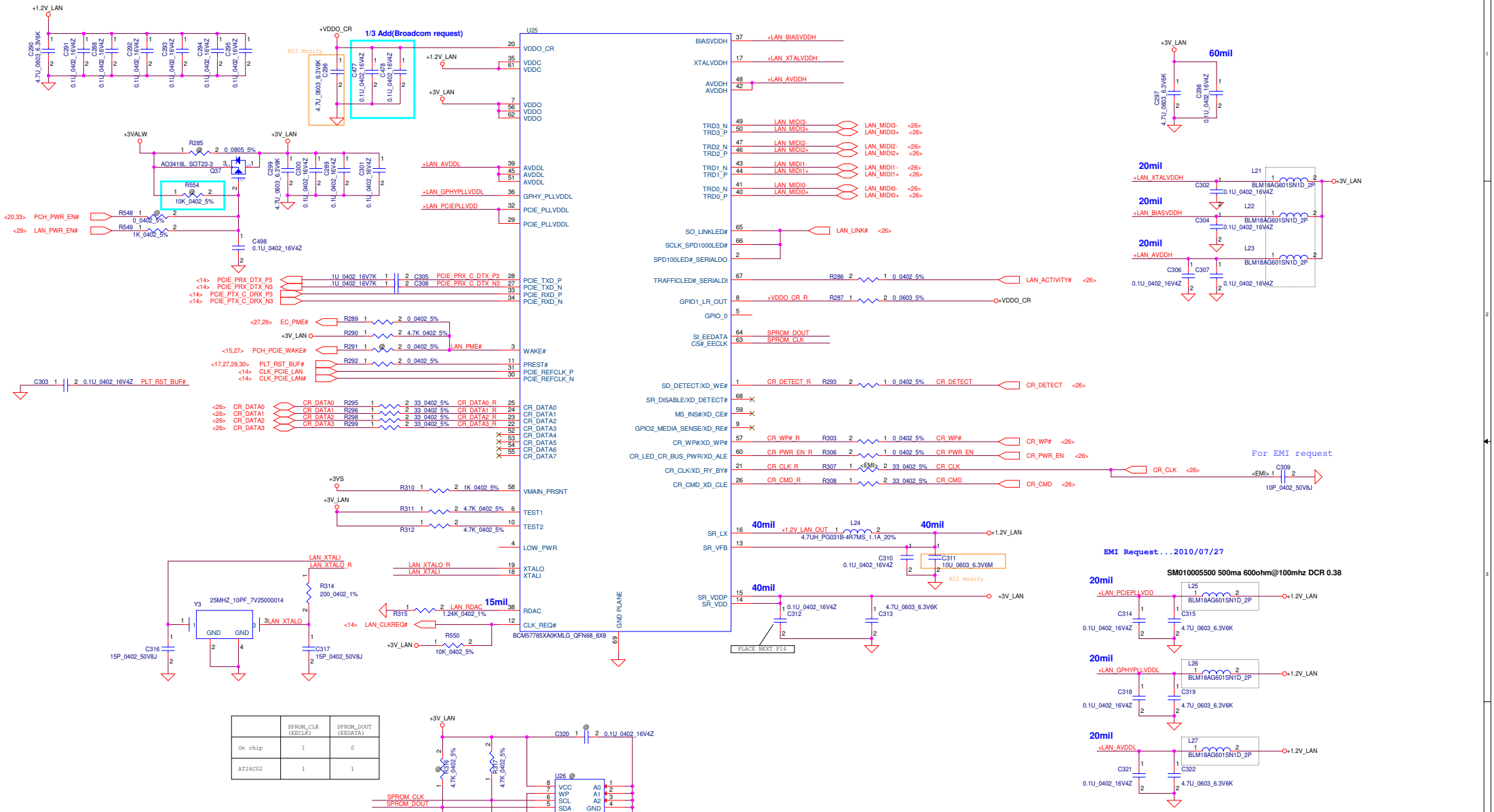
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: CRT&HDD Connector

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 24 of 45


+1.2V_LAN
+VDDO_CR
1/3 Add(Broadcom request)
U25
+3VALW
+3V_LAN
60mil
20mil
EMI Request...2010/07/27
SM010005500 500ma 600ohm@100mhz DCR 0.38
For EMI request
40mil
15mil
PLACE NEXT P14
GND PLANE
BCM57785XA0KMLG_QFN68_8X8
AT24C04BN-SH-T_SO8
SA00004QG00
25MHZ_10PF_7V25000014
BLM18AG601SN1D_2P
4.7UH_PG031B-4R7MS_1.1A_20%
SPROM_CLK (EECLK)
SPROM_DOUT (EEDATA)
On chip
AT24C02
Security Classification
Compal Secret Data
Issued Date
2011/11/22
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2012/11/22
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LAN Boardcom 57785
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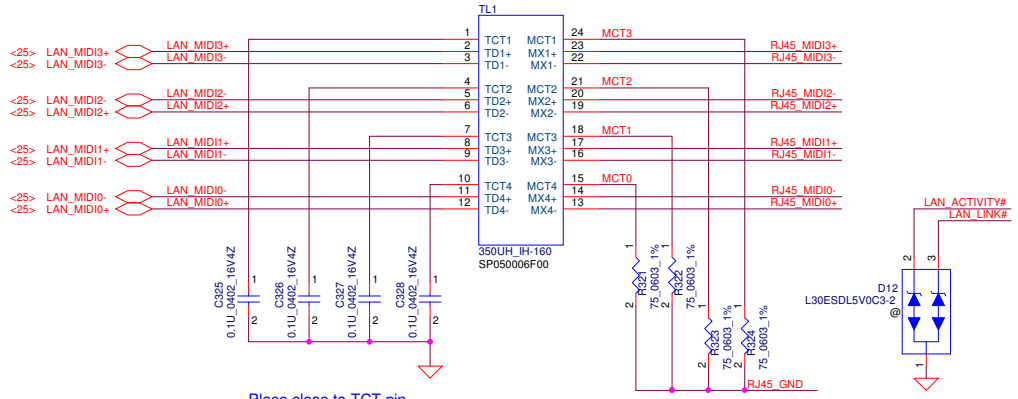
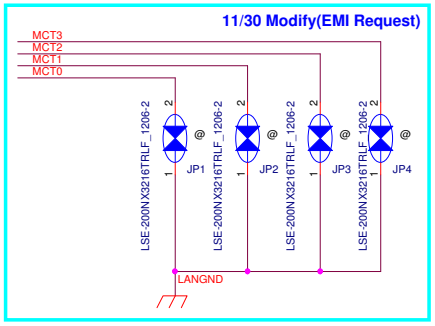
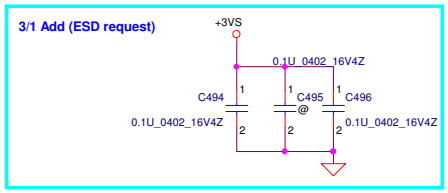
BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

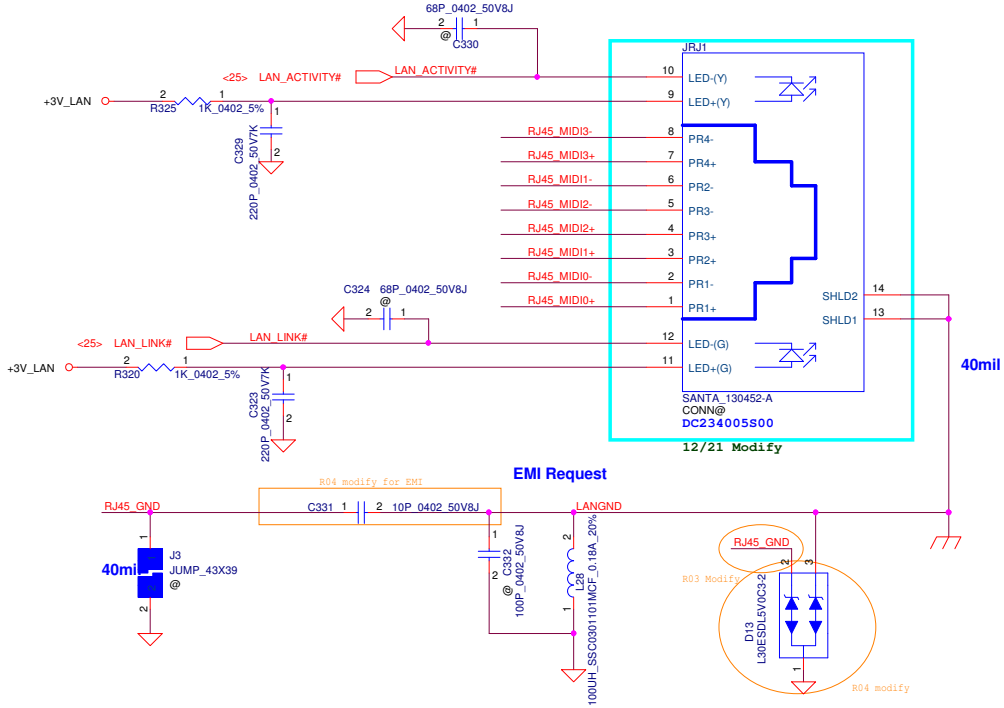
LAN Connector

C474,C475 and D14
ME interefer,do not pop!!

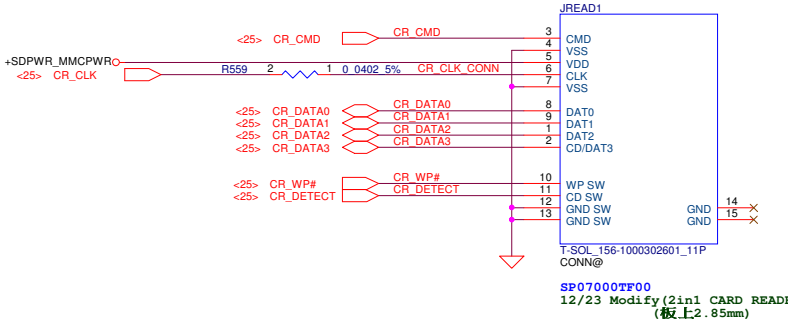


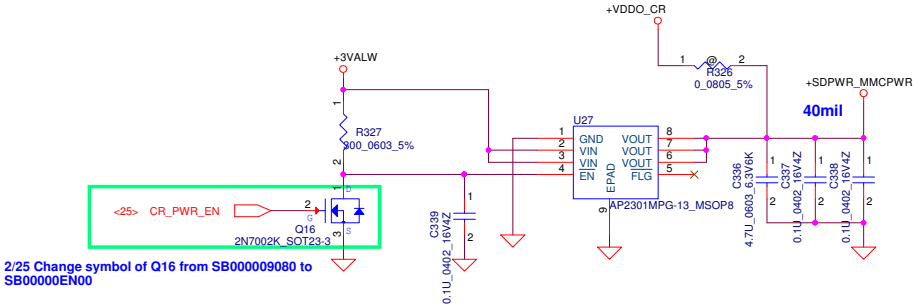


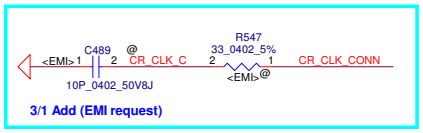


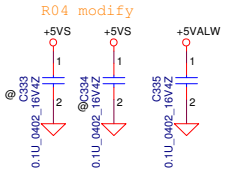


Card Reader Connector









Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: Card Reader

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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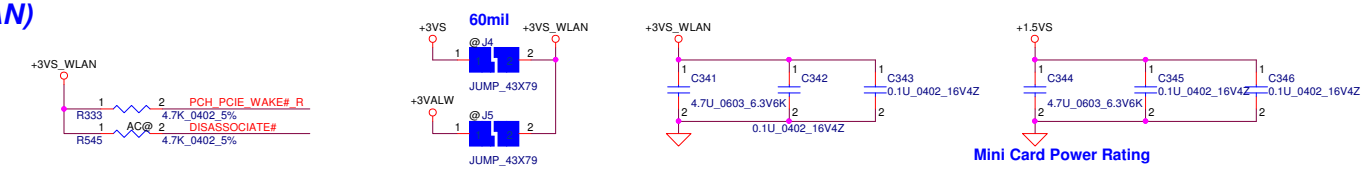
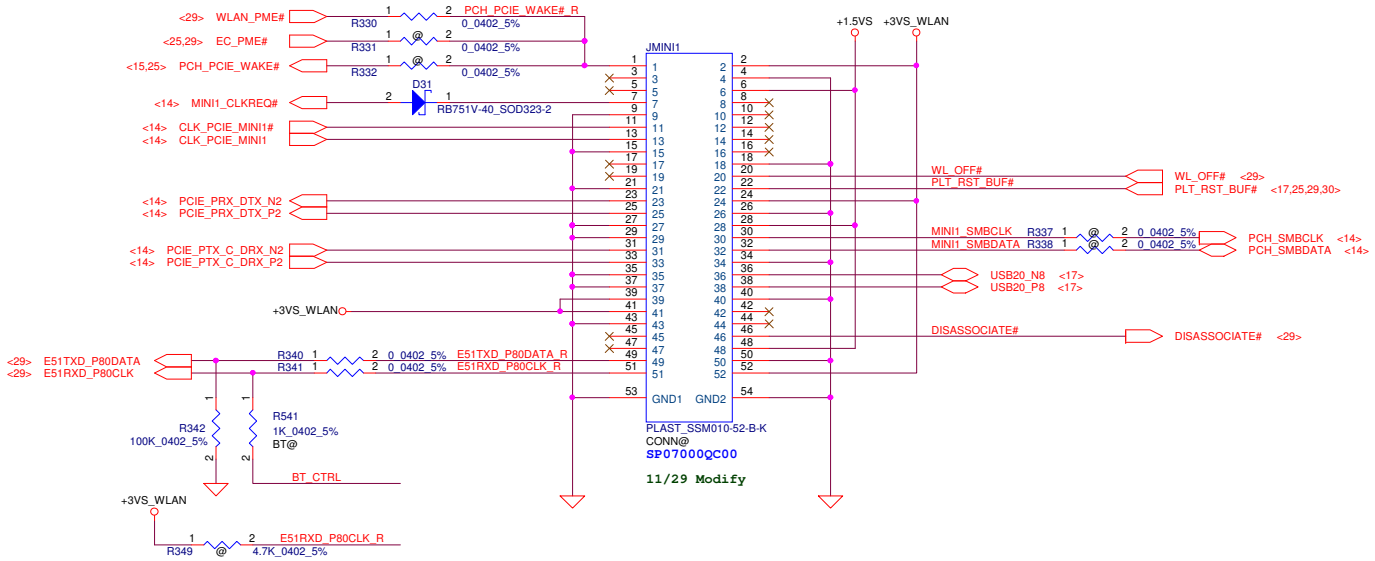
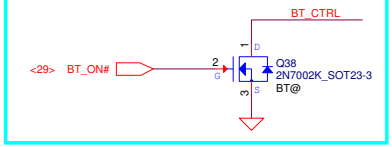
MINI CARD(Wireless LAN)

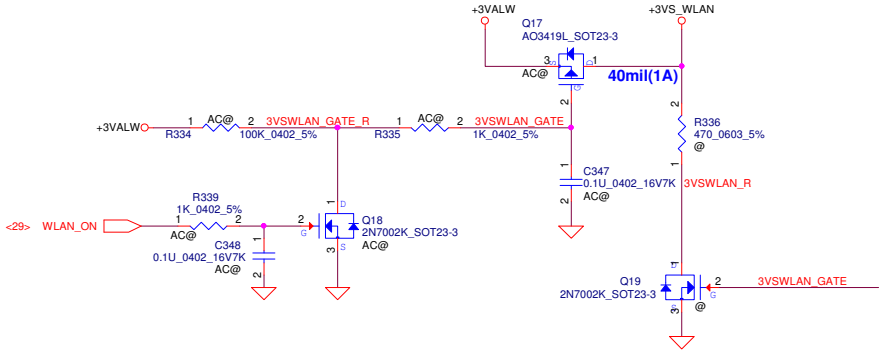




WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H





Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: MINI CARD (WLAN)

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

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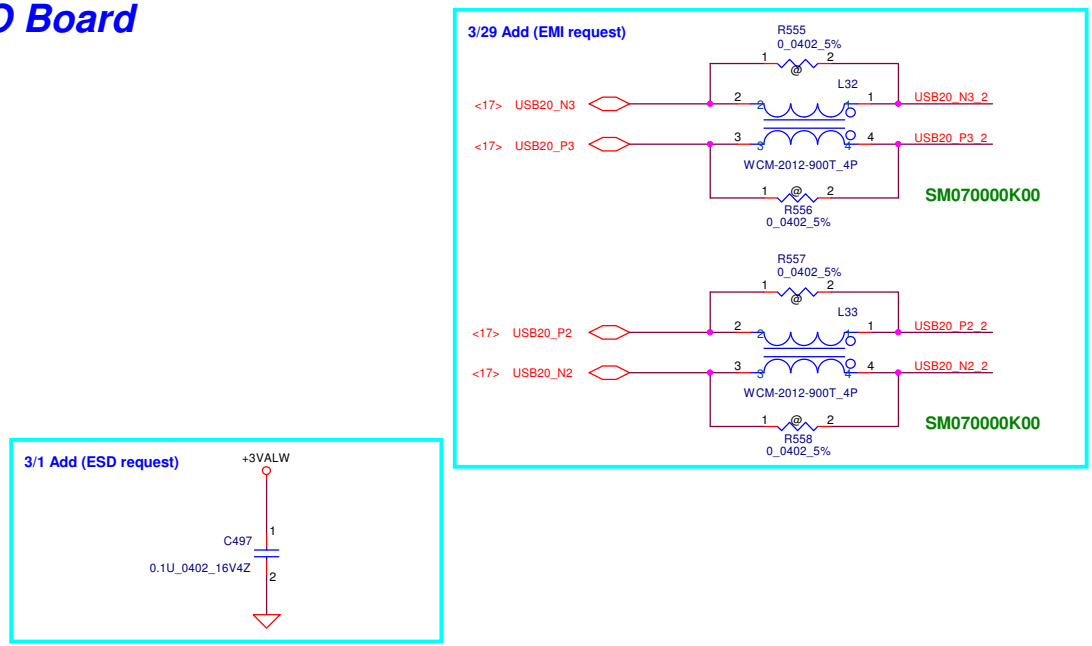
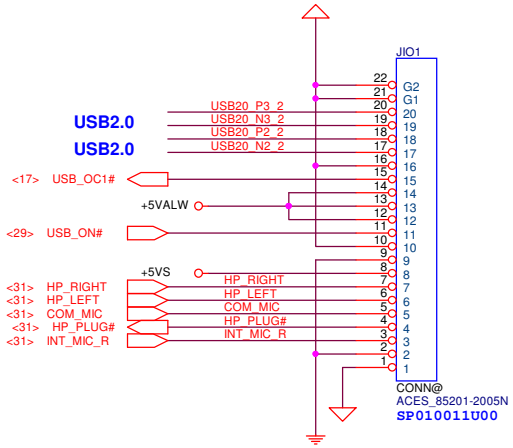
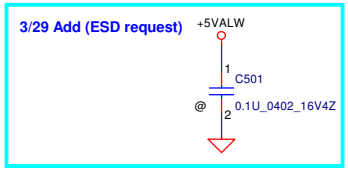
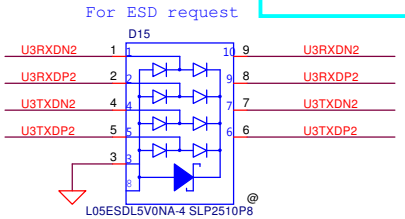
IO Board

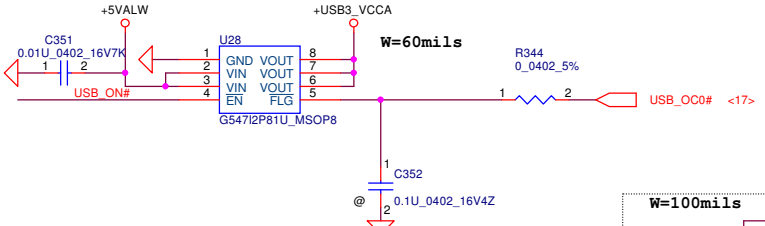


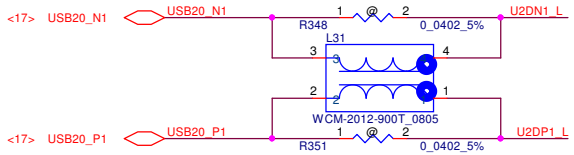


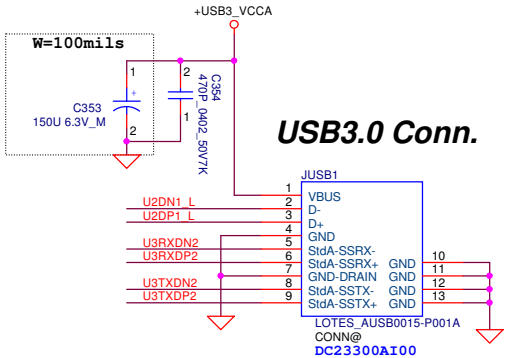
USB3.0

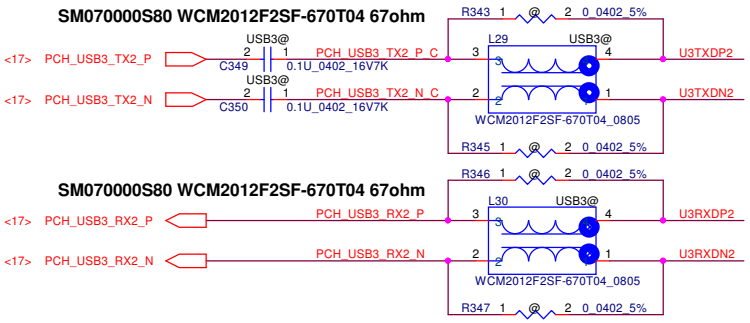


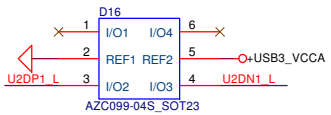












Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Title	IO Board & USB3.0		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
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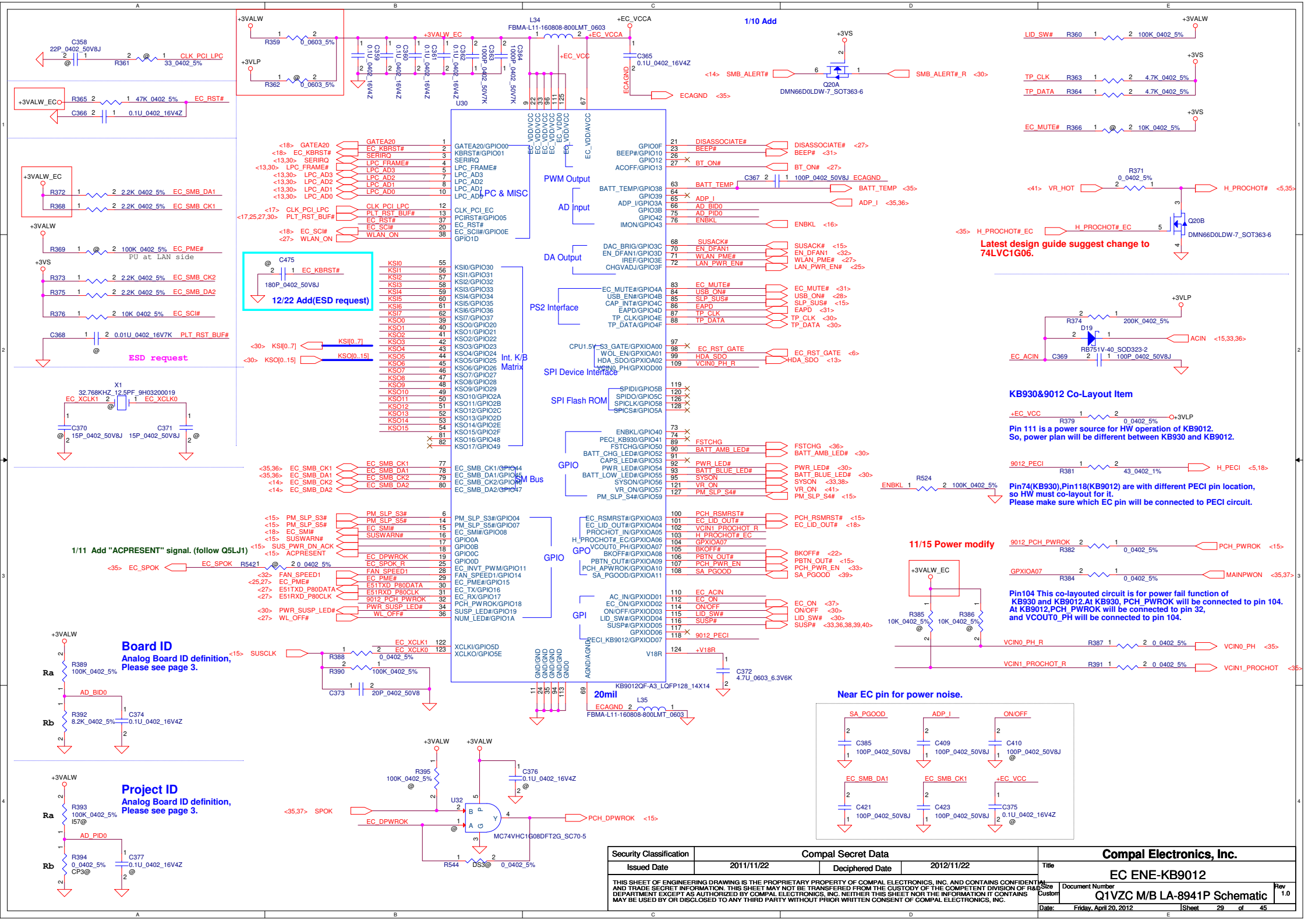
1/10 Add
1/11 Add "ACPRESENT" signal. (follow Q5LJ1)
11/15 Power modify
Latest design guide suggest change to 74LVC1G06.
12/22 Add(ESD request)
ESD request
KB930&9012 Co-Layout Item
Pin 111 is a power source for HW operation of KB9012.
So, power plan will be different between KB930 and KB9012.
Pin74(KB930),Pin118(KB9012) are with different PECI pin location, so HW must co-layout for it.
Please make sure which EC pin will be connected to PECI circuit.
Pin104 This co-layouted circuit is for power fail function of KB930 and KB9012.At KB930, PCH_PWROK will be connected to pin 104.
At KB9012,PCH_PWROK will be connected to pin 32,
and VCOUT0_PH will be connected to pin 104.
Near EC pin for power noise.
Board ID
Analog Board ID definition,
Please see page 3.
Project ID
Analog Board ID definition,
Please see page 3.
20mil
KB9012QF-A3_LQFP128_14X14
MC74VHC1G08DFT2G_SC70-5
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
LPC & MISC
SMB Bus
Int. K/B Matrix
Compal Electronics, Inc.
EC ENE-KB9012
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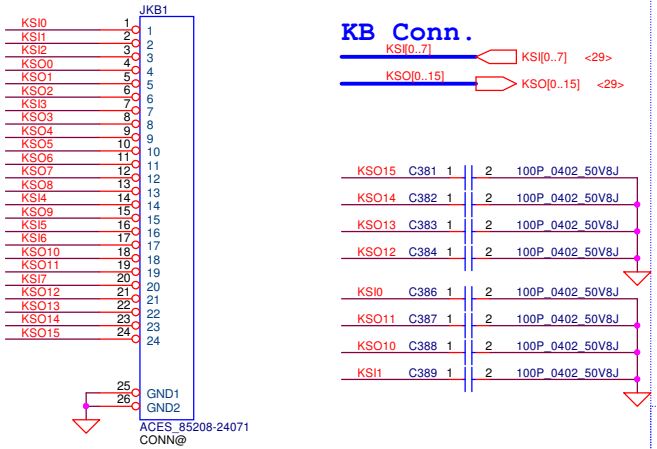
KB Conn.



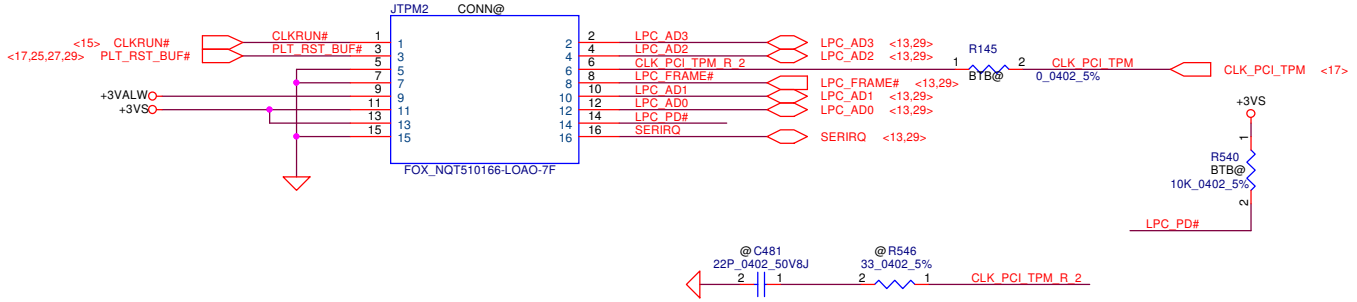
12/30 Modify.

KSI[0..7] KSI[0..7] <29>

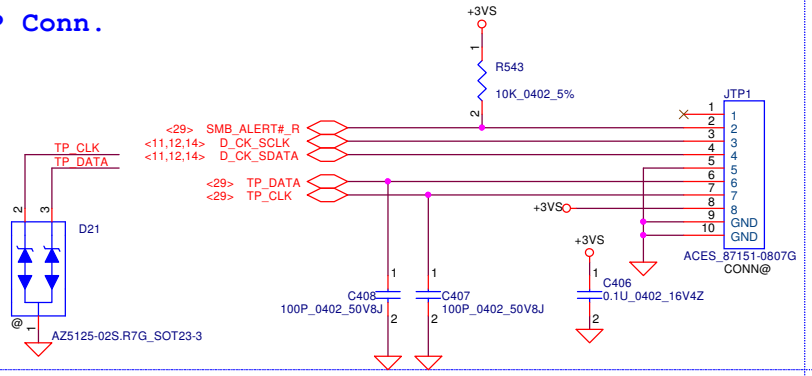
KSO[0..15] KSO[0..15] <29>

KSO15	C381	1	2	100P_0402_50V8J
KSO14	C382	1	2	100P_0402_50V8J
KSO13	C383	1	2	100P_0402_50V8J
KSO12	C384	1	2	100P_0402_50V8J
KSI0	C386	1	2	100P_0402_50V8J
KSO11	C387	1	2	100P_0402_50V8J
KSO10	C388	1	2	100P_0402_50V8J
KSI1	C389	1	2	100P_0402_50V8J
KSI2	C390	1	2	100P_0402_50V8J
KSO9	C392	1	2	100P_0402_50V8J
KSI3	C394	1	2	100P_0402_50V8J
KSO8	C396	1	2	100P_0402_50V8J
KSO0	C400	1	2	100P_0402_50V8J
KSI5	C398	1	2	100P_0402_50V8J
KSI6	C402	1	2	100P_0402_50V8J
KSI7	C404	1	2	100P_0402_50V8J
KSO7	C391	1	2	100P_0402_50V8J
KSO6	C393	1	2	100P_0402_50V8J
KSO5	C395	1	2	100P_0402_50V8J
KSO4	C397	1	2	100P_0402_50V8J
KSO3	C401	1	2	100P_0402_50V8J
KSI4	C399	1	2	100P_0402_50V8J
KSO2	C403	1	2	100P_0402_50V8J
KSO1	C405	1	2	100P_0402_50V8J

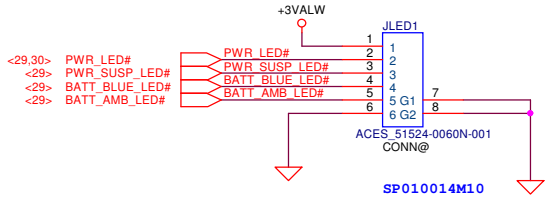
TPM



TP Conn.

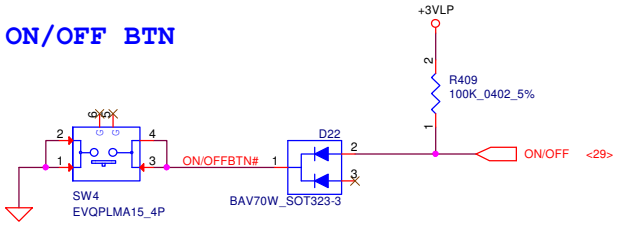


LED Board

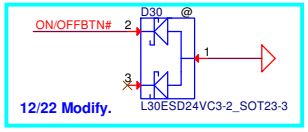


01/12 Change to ACES_51524-0060N-001 .

ON/OFF BTN

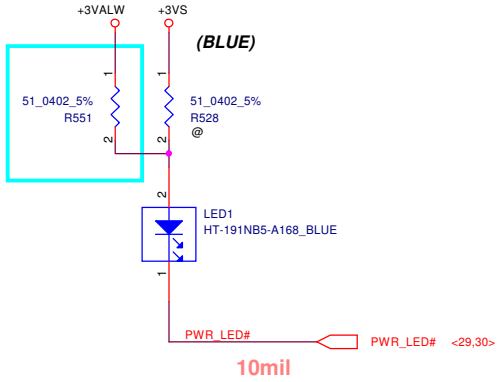


For power button ESD request



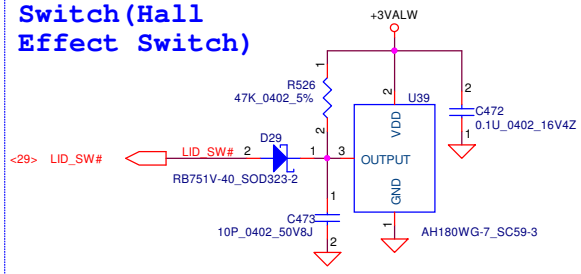
12/22 Modify.

Power LED



10mil

Lid Switch(Hall Effect Switch)



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: TP/IO Port/ KB CONN/TPM

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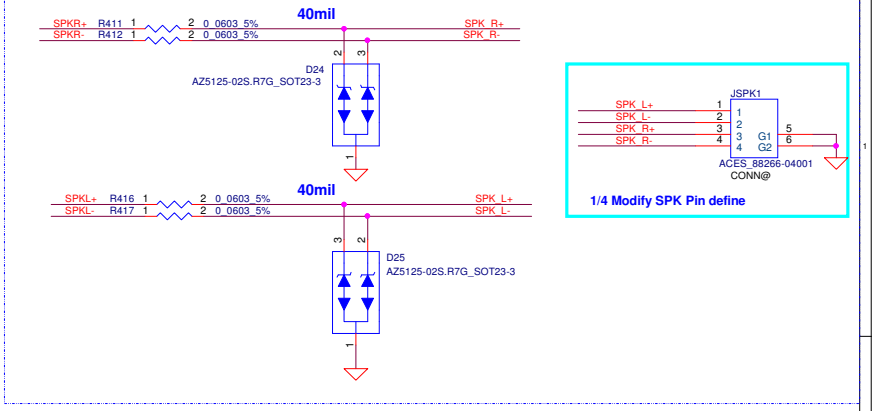
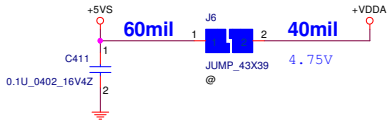
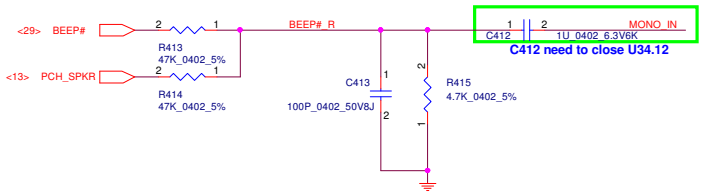
HD Audio Codec

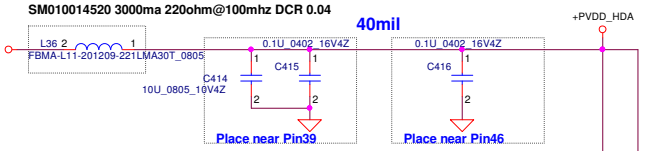
Int. Speaker Conn.

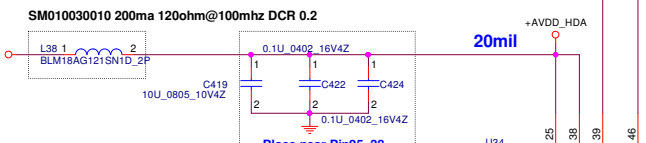


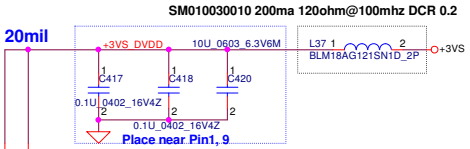


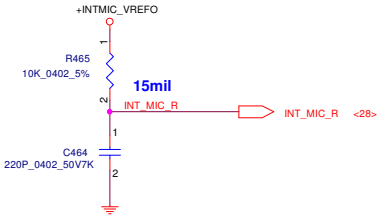
(output = 300 mA)

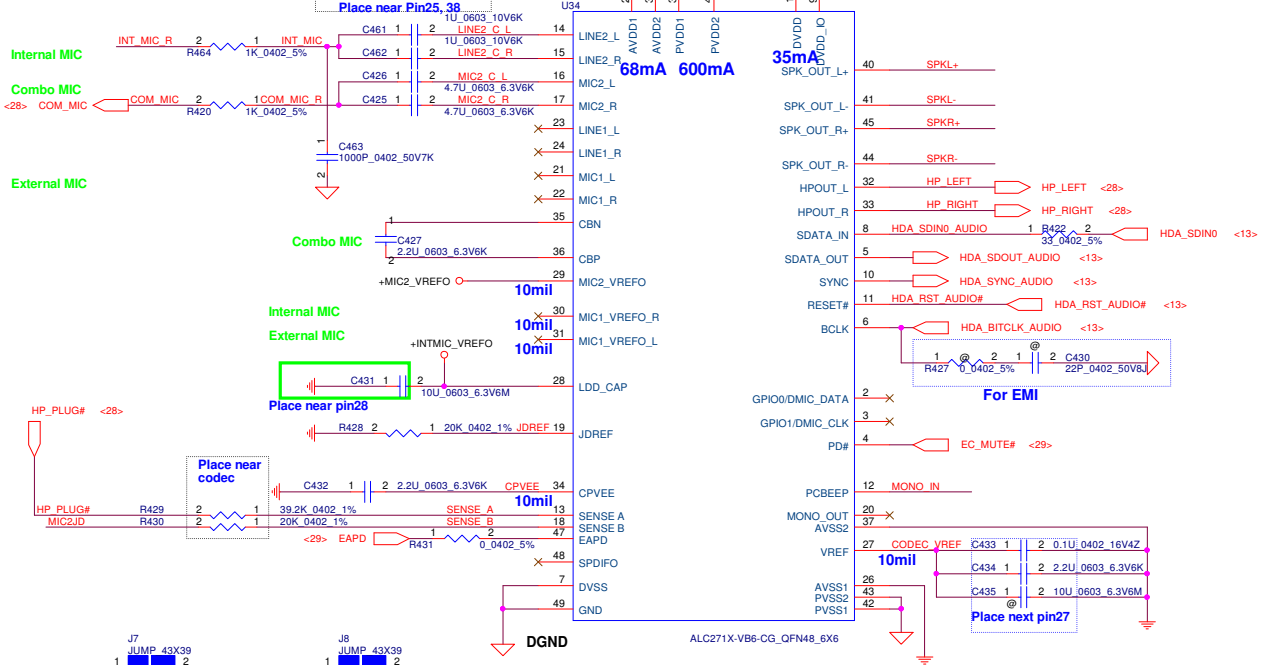


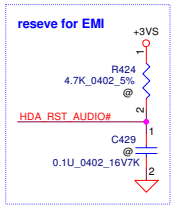


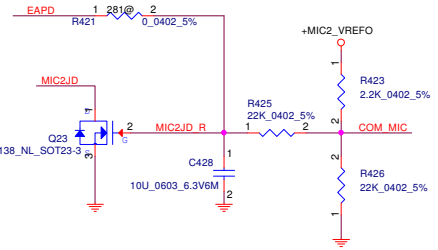


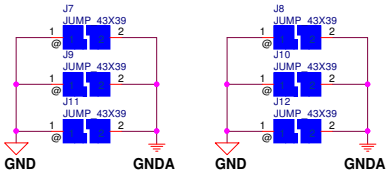












Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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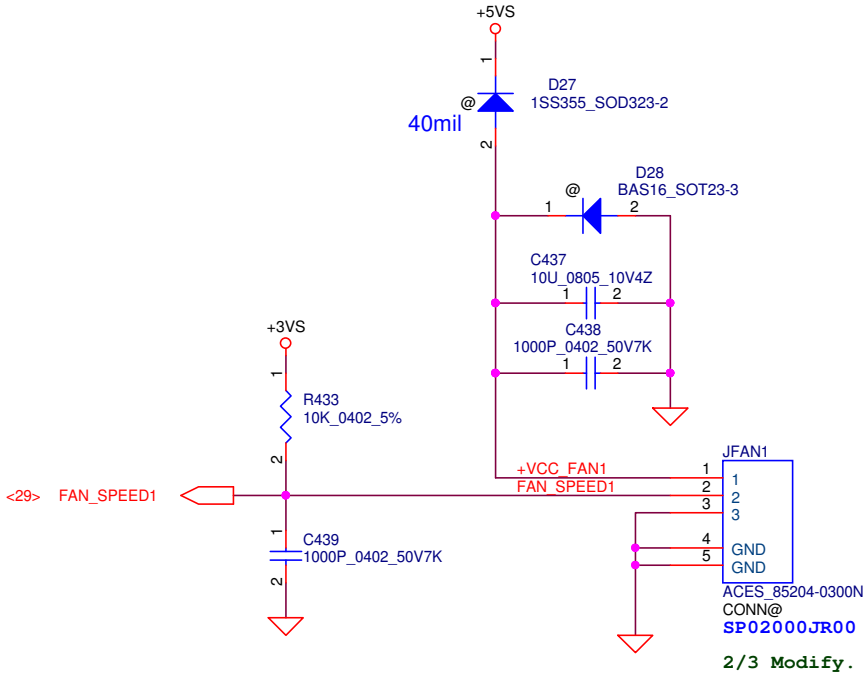
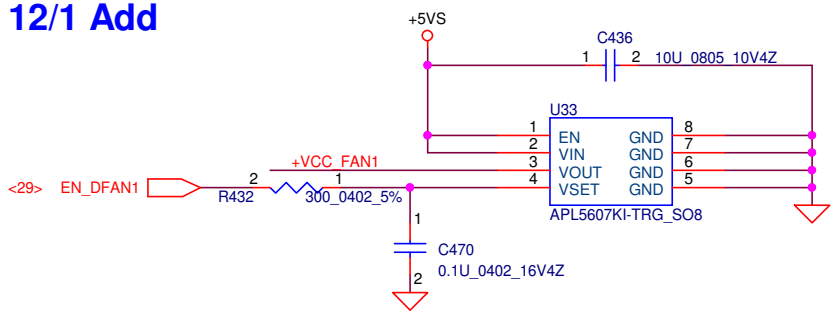
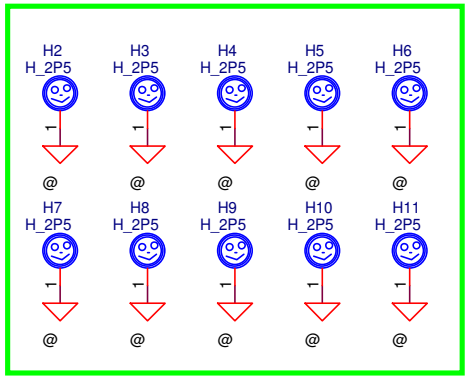
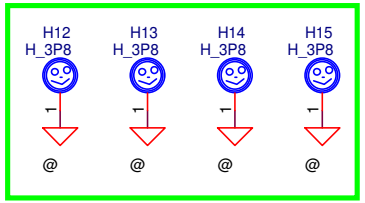
FAN1 Conn



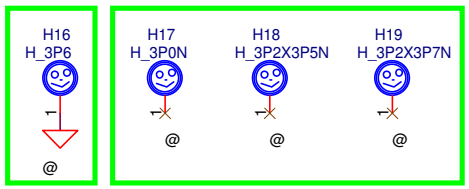
12/1 Add

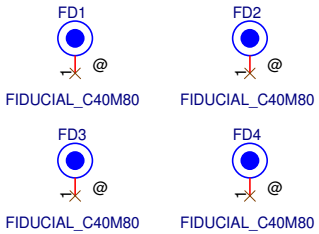






CPU support plate





Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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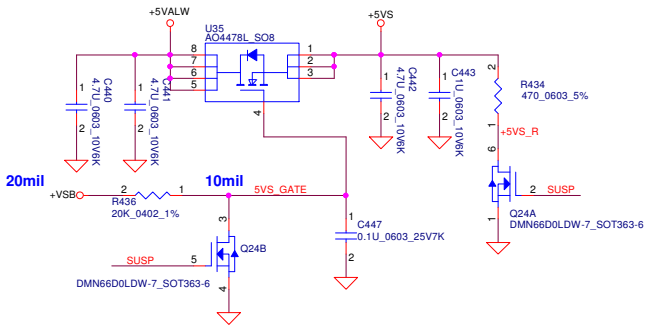
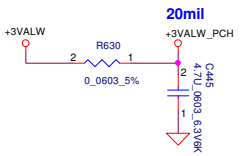
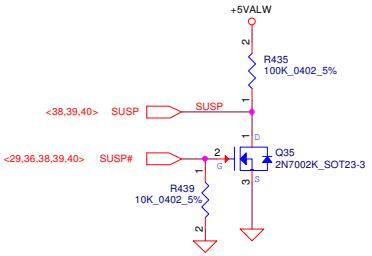
+5VALW TO +5VS

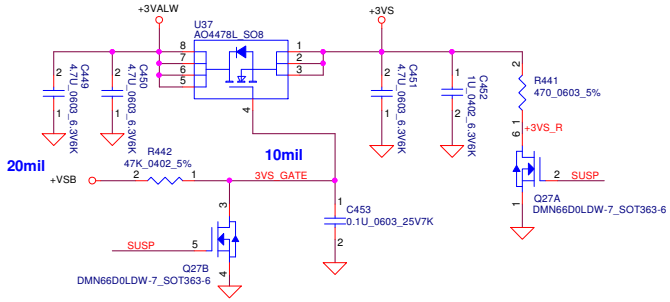


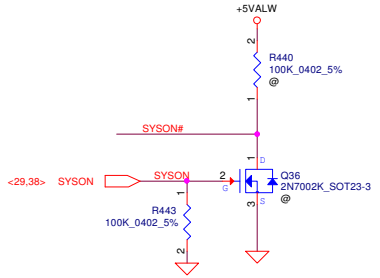
+3VALW to +3VALW_PCH(PCH AUX Power)



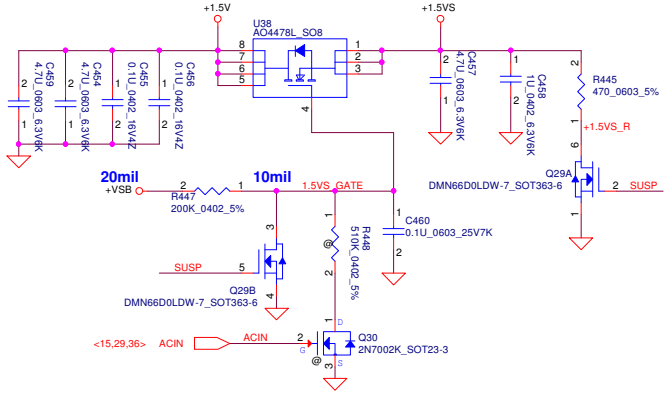


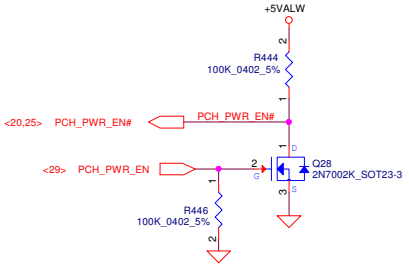
+3VALW TO +3VS

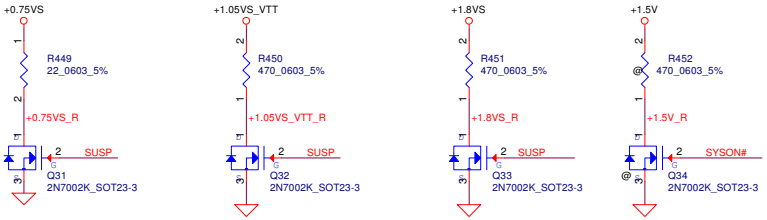




+1.5V to +1.5VS







Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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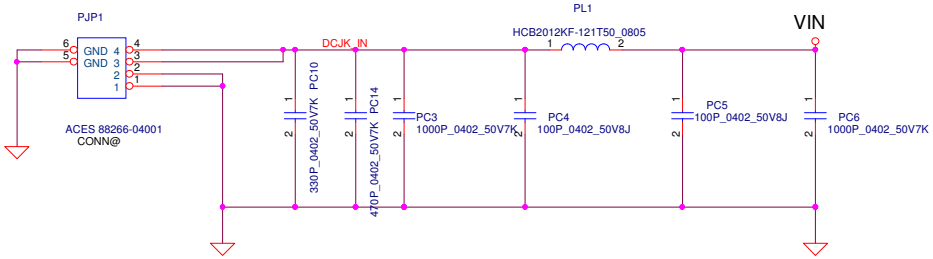

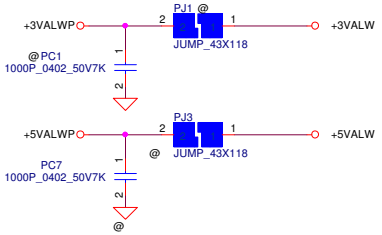

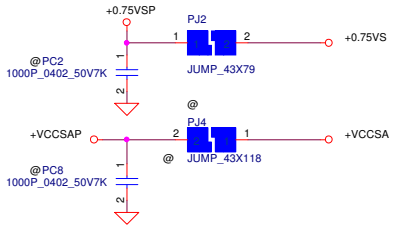

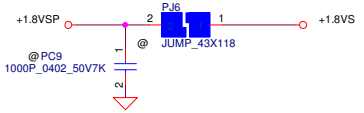

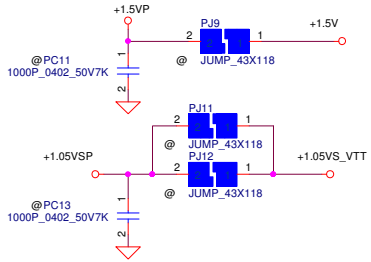

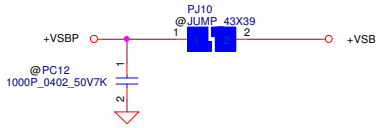

Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	Q1VZC M/B LA-8941P Schematic	1.0

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footprint :SUYIN_200275MR008G15QZR_8P-T
PN:DC040007N10 SOCKET BATT C200275MR008G15QZR 8P W/FORK

@

PJP2

SUYIN_200275GR008G16MZR

<40,41>
VMB

PJ5 @
JUMP_43X118

<40,41>
BATT+

PC66 1000P_0402_50V7K
PC67 0.01U_0402_25V7K

PR58 100_0402_1%
PR59 100_0402_1%
PR60 1K_0402_5%
PR62 6.49K_0402_1%
PR65 1K_0402_1%

EC_SMDA
EC_SMCA
TH
BI+

EC_SMB_DA1 <29,36>
EC_SMB_CK1 <29,36>
+3VALW
<5,29> H_PROCHOT#
BATT_TEMP <29>

VL
PC65 0.1U_0603_25V7K

+EC_VCCA
PR78 12.4K_0402_1%
PR63 CS@ 5.62K_0402_1%
ADP_I <29,36>
VCIN0_PH <29>
VCIN1_PROCHOT <29>

@PR61 21K_0402_1%
@PR64 100K_0402_1%
@PR66 9.53K_0402_1%
PU3 @
VCC TMSNS1
GND RHYST1
~OT1 TMSNS2
~OT2 RHYST2
G718TM1U_SOT23-8
MAINPWON

+3VLP
PR67 @ 100K_0402_1%
@PQ32 2N7002KW_SOT323-3
@PR68 28.7K_0402_1%
PH1 100K_0402_1%_NCP15WF104F03RC
@PR80 0_0402_5%
PR81 0_0402_5%
PR79 10K_0402_1%
<29> ECAGND

SD034100280 10K OHM

<29> H_PROCHOT#_EC

PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

PQ19 BSS84LT1G_SOT23-3
B+
+VSBP
PR70 100K_0402_1%
PC68 0.22U_0603_25V7K
PC69 0.1U_0603_25V7K
PR71 22K_0402_1%

<29> EC_SPOK
VL
PR72 100K_0402_1%
PR73 1K_0402_5%
<29,37> SPOK
PQ20 2N7002KW 1N SOT323-3
PC71 1U_0402_6.3V6K

+3VALW
@ PC70 0.1U_0603_25V7K
@PR74 10K_0402_1%
@PR75 10K_0402_1%
@PU4
VCC TMSNS1
GND RHYST1
OT1 TMSNS2
OT2 RHYST2
G718TM1U_SOT23-8
PH2_R
@PR77 47K_0402_1%
@PH2 100K_0402_1%_NCP15WF104F03RC
@PR76 100K_0402_1%
<29,37> MAINPWON

For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W

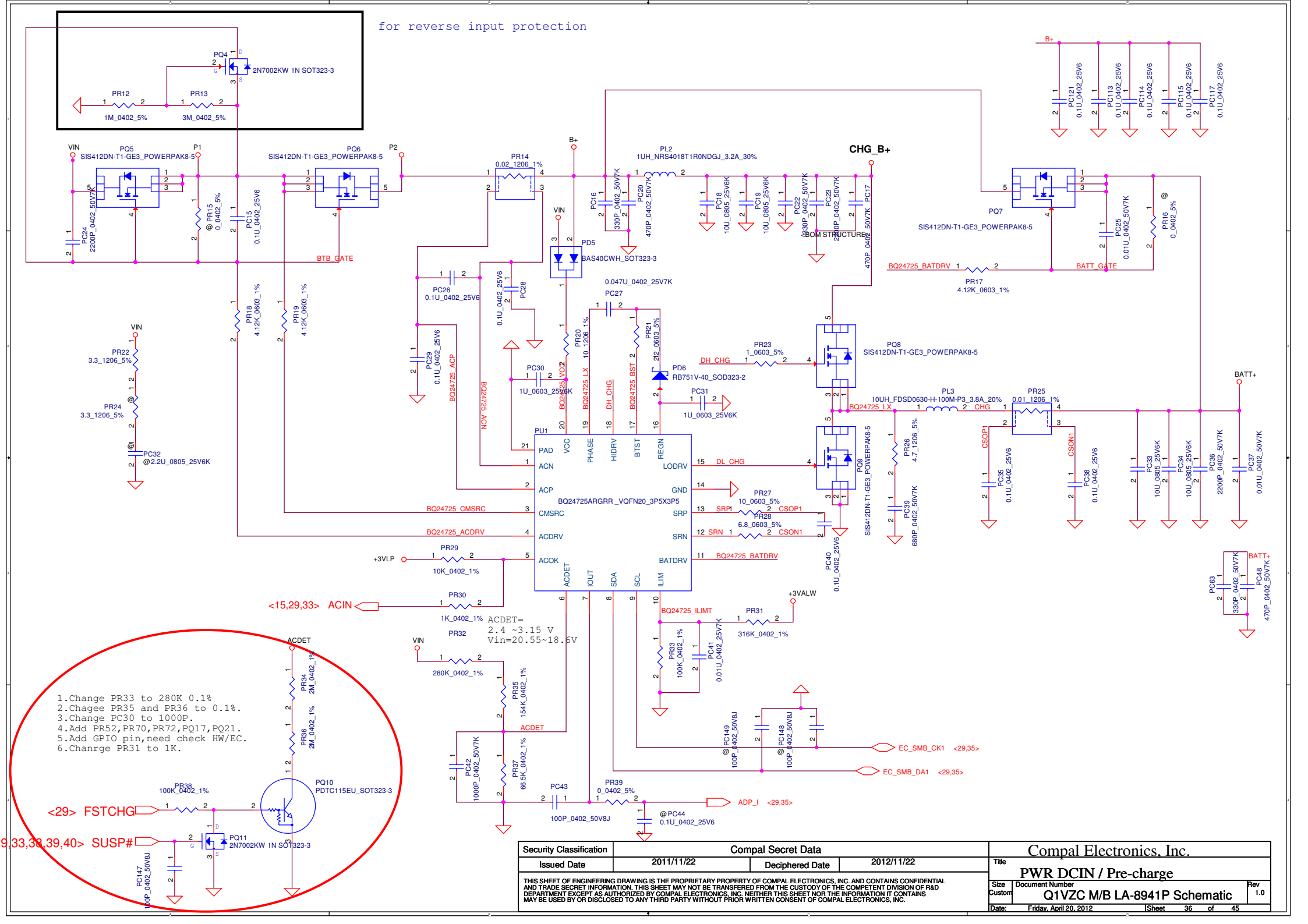
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 35 of 45



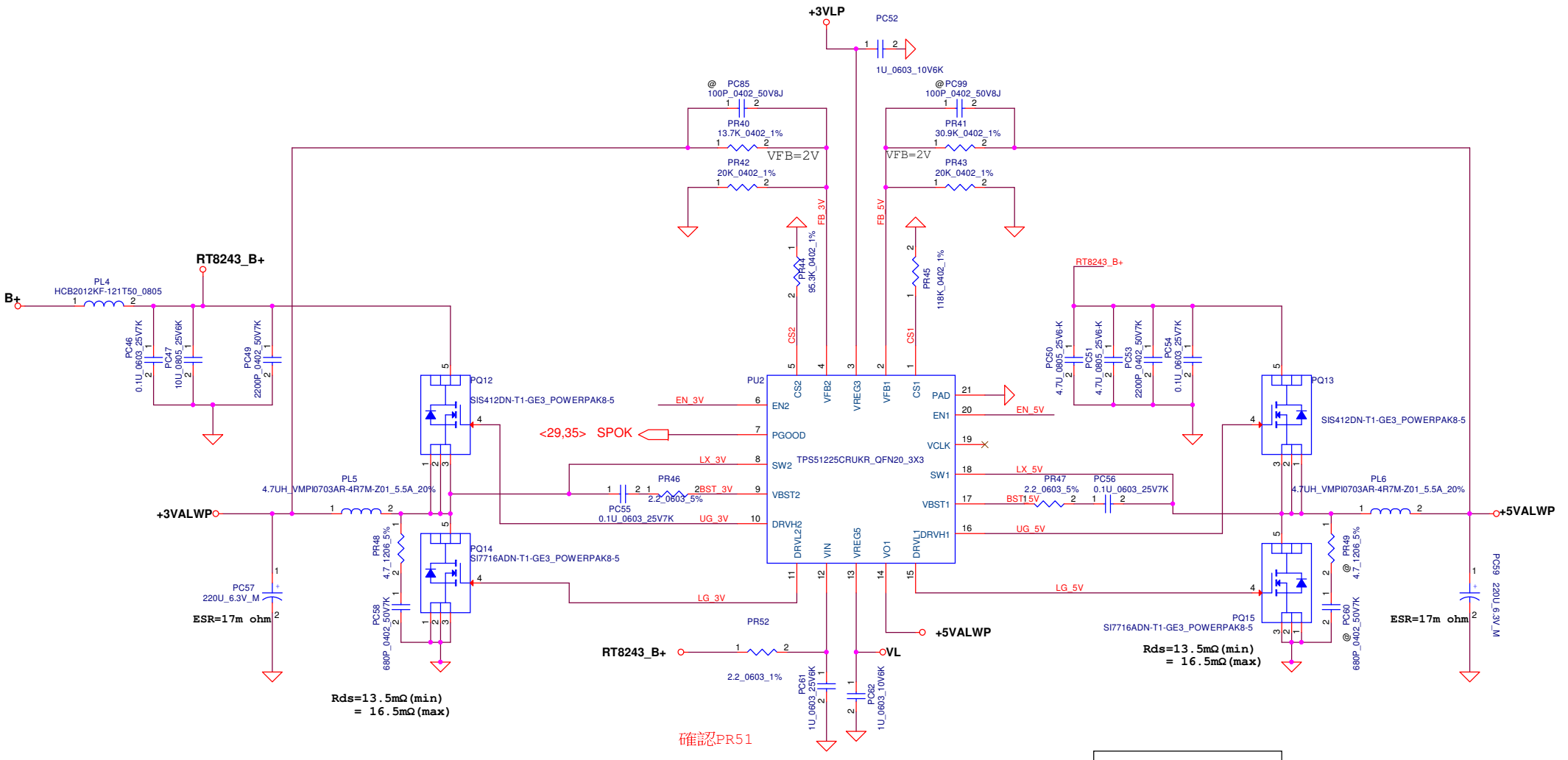
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 36 of 45



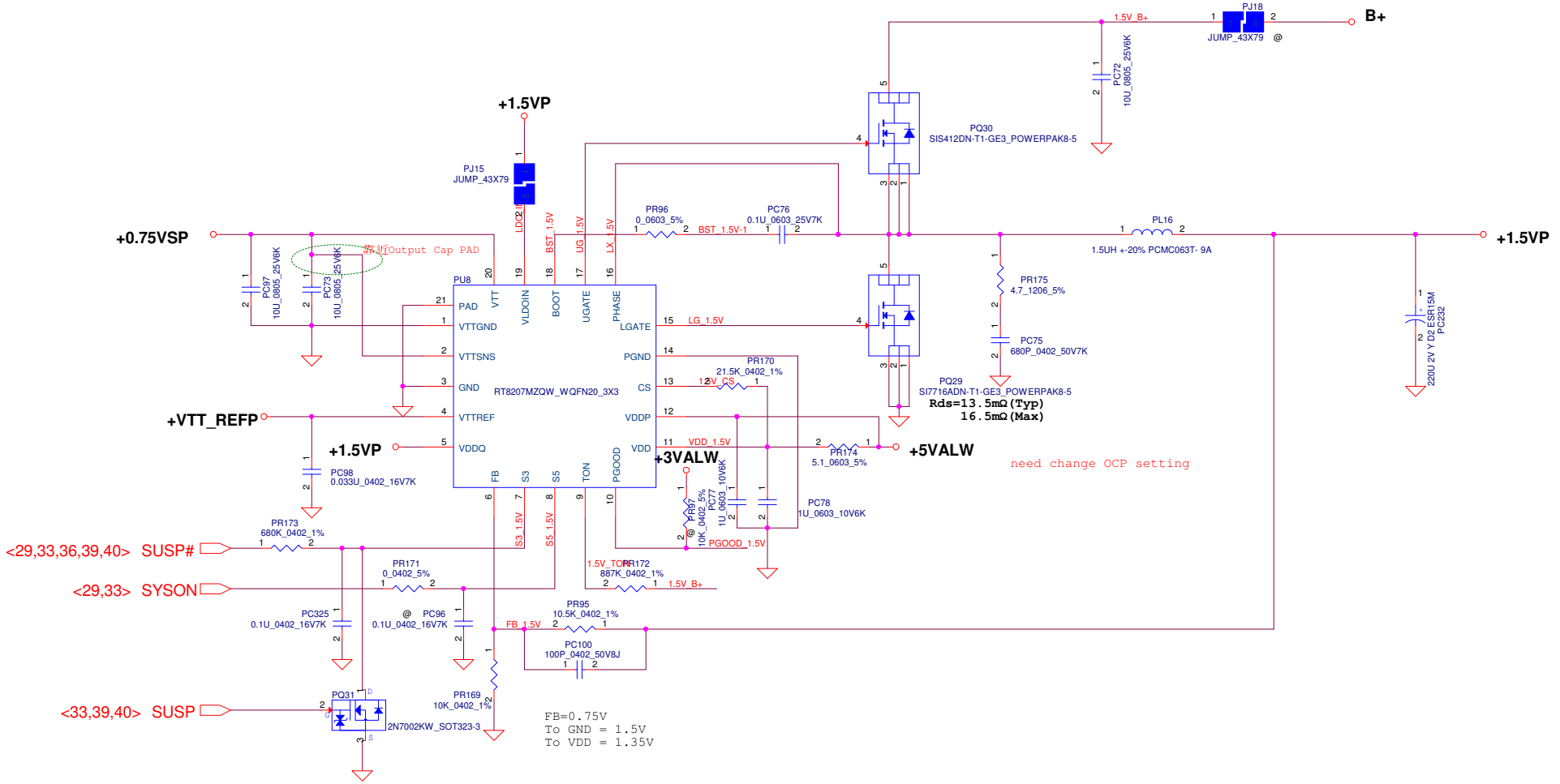
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 37 of 45



STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

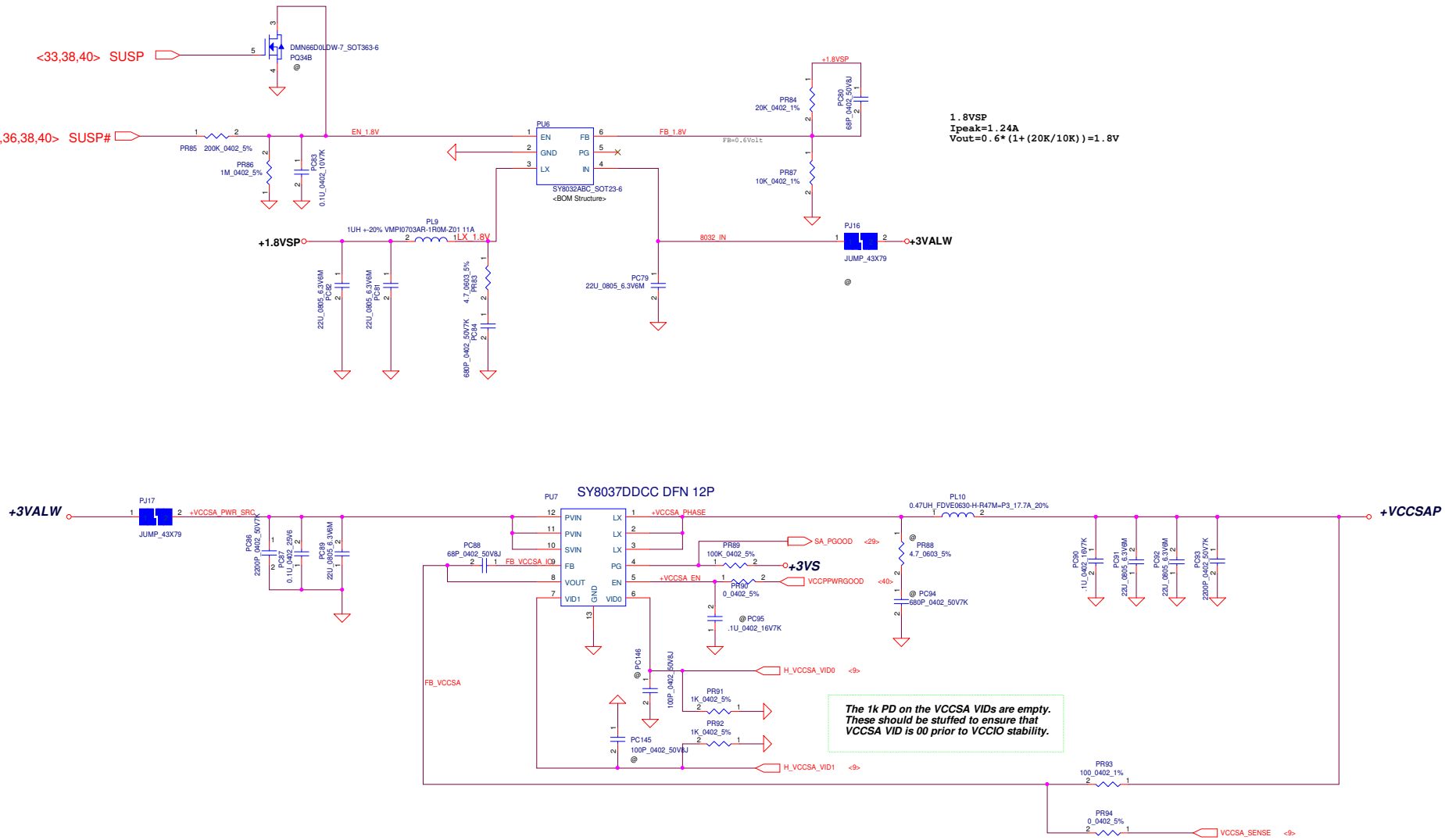
<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10.5K)=1.52V
Fsw=286K to 200KHz

Cout ESR=17m ohm Rdson(max)=16.5 mohm Rdson(typ)=13.5 mohm.
Ipeak=12 A, Imax=8.4A, Iocp=14.4A

Delta I=((Vin-Vo)*(Vo/Vin))/(L*Fsw)=2.195A
=>1/2Delta I=1.099A

Iocpmax=((21.5K*11uA)/0.0135)+0.5 delta I= A
Iocpmin=((21.5K*9uA)/(0.0165))+0.5 delta I=15.6A

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/22	Deciphered Date	2012/11/22
Title	PWR-+1.5VP		
Size: Custom	Document Number: Q1VZC M/B LA-8941P Schematic		Rev: 1.0
Date: Friday, April 20, 2012	Sheet 38 of 45		



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout(ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

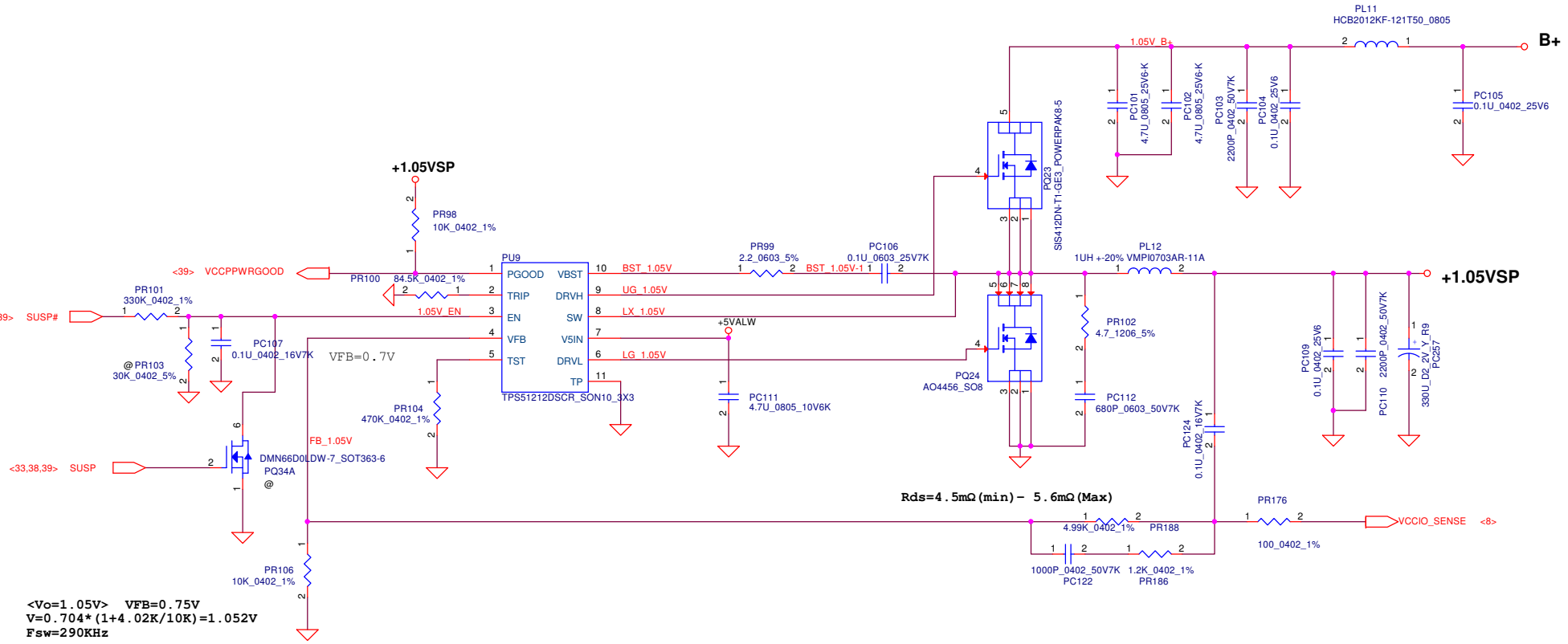
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 39 of 45



<Vo=1.05V> VFB=0.75V
V=0.704*(1+4.02K/10K)=1.052V
Fsw=290KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.06A

Iocpmax=((15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A

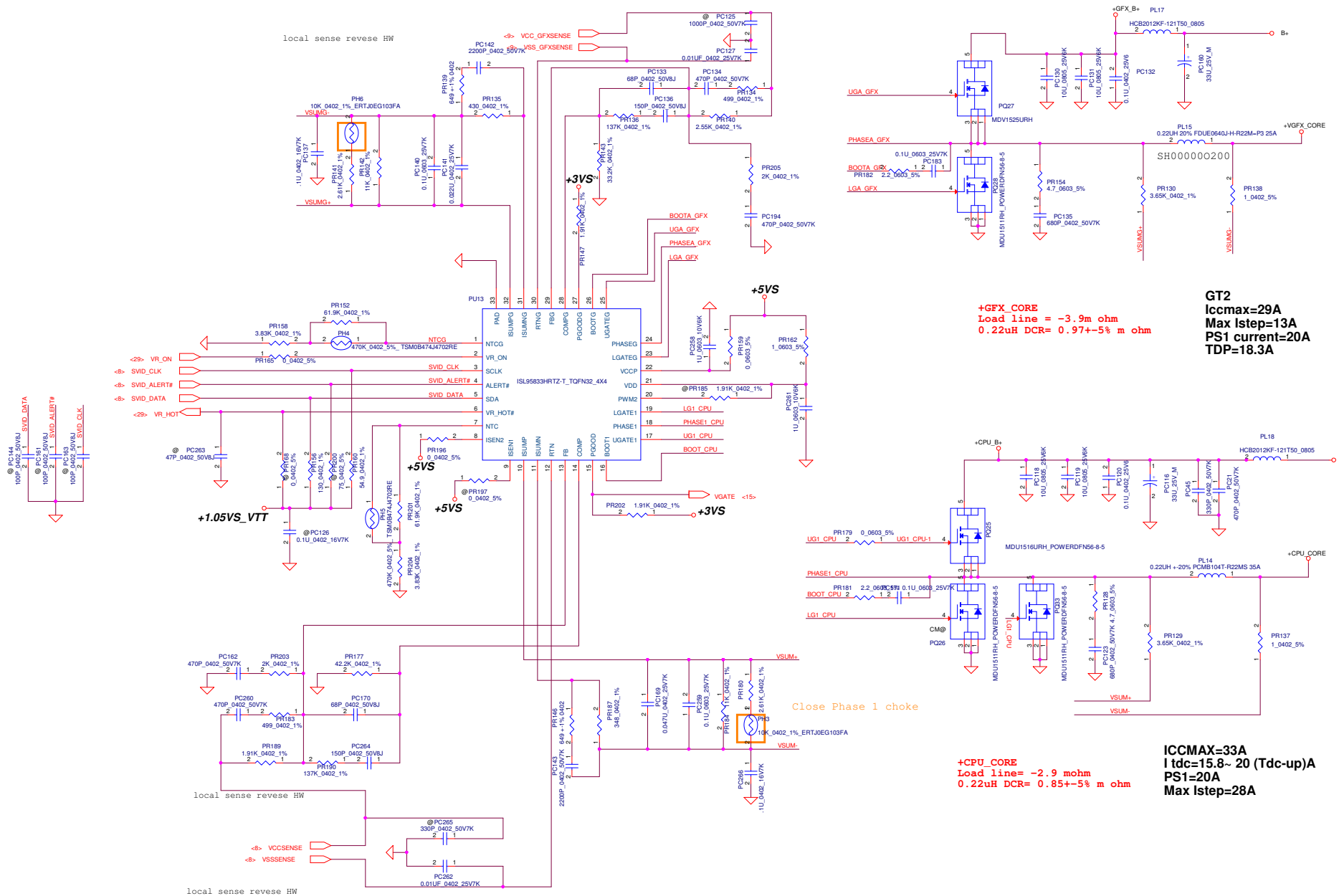
Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 40 of 45



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/22	Deciphered Date 2012/11/22	Title CPU/GFX_CORE

Size	Document Number	Q1VZC M/B LA-8941P Schematic	Rev 1.0
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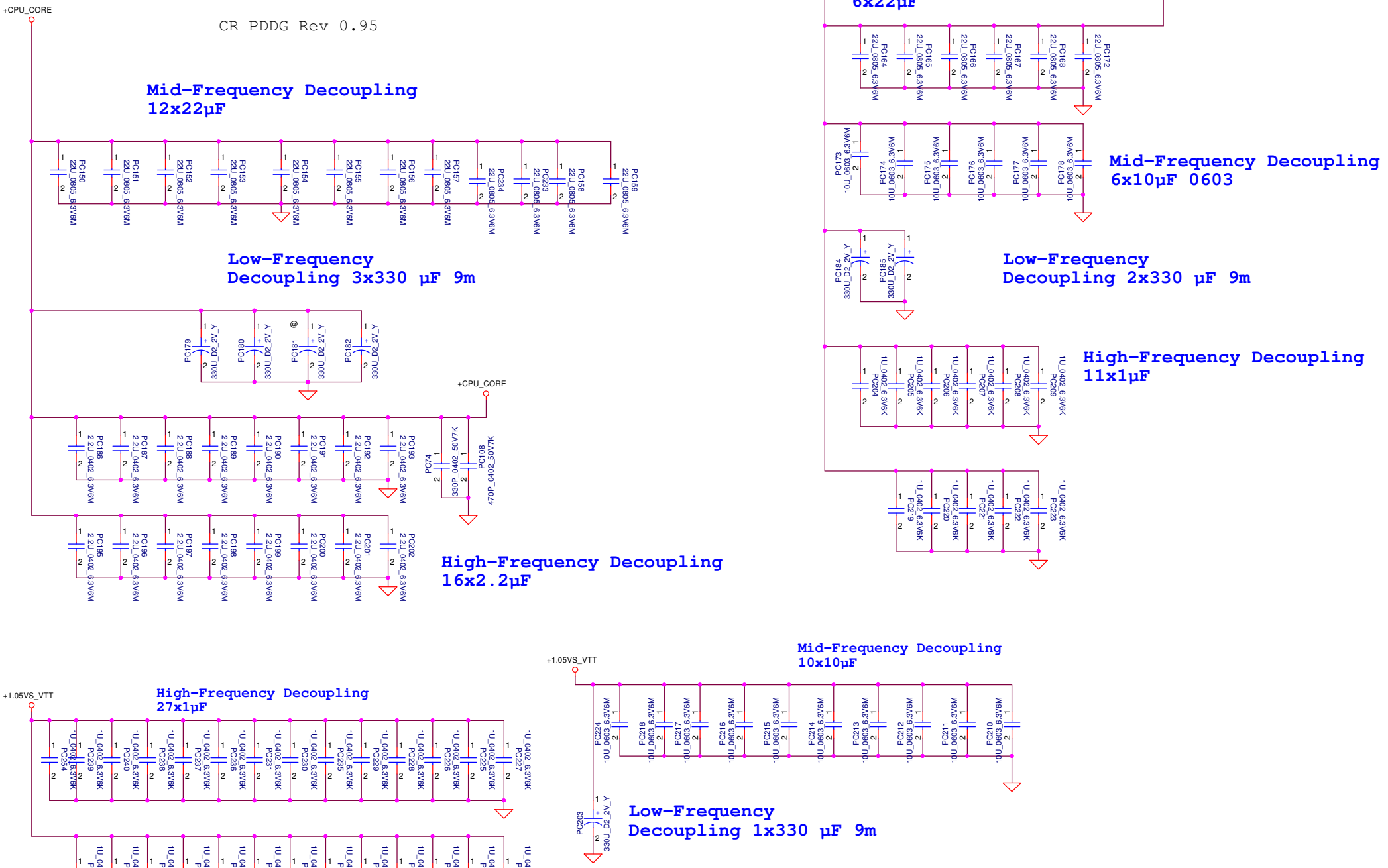
CR PDDG Rev 0.95



Security Classification	Compal Secret Data		
Issued Date	2011/11/22	Deciphered Date	2012/11/22

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

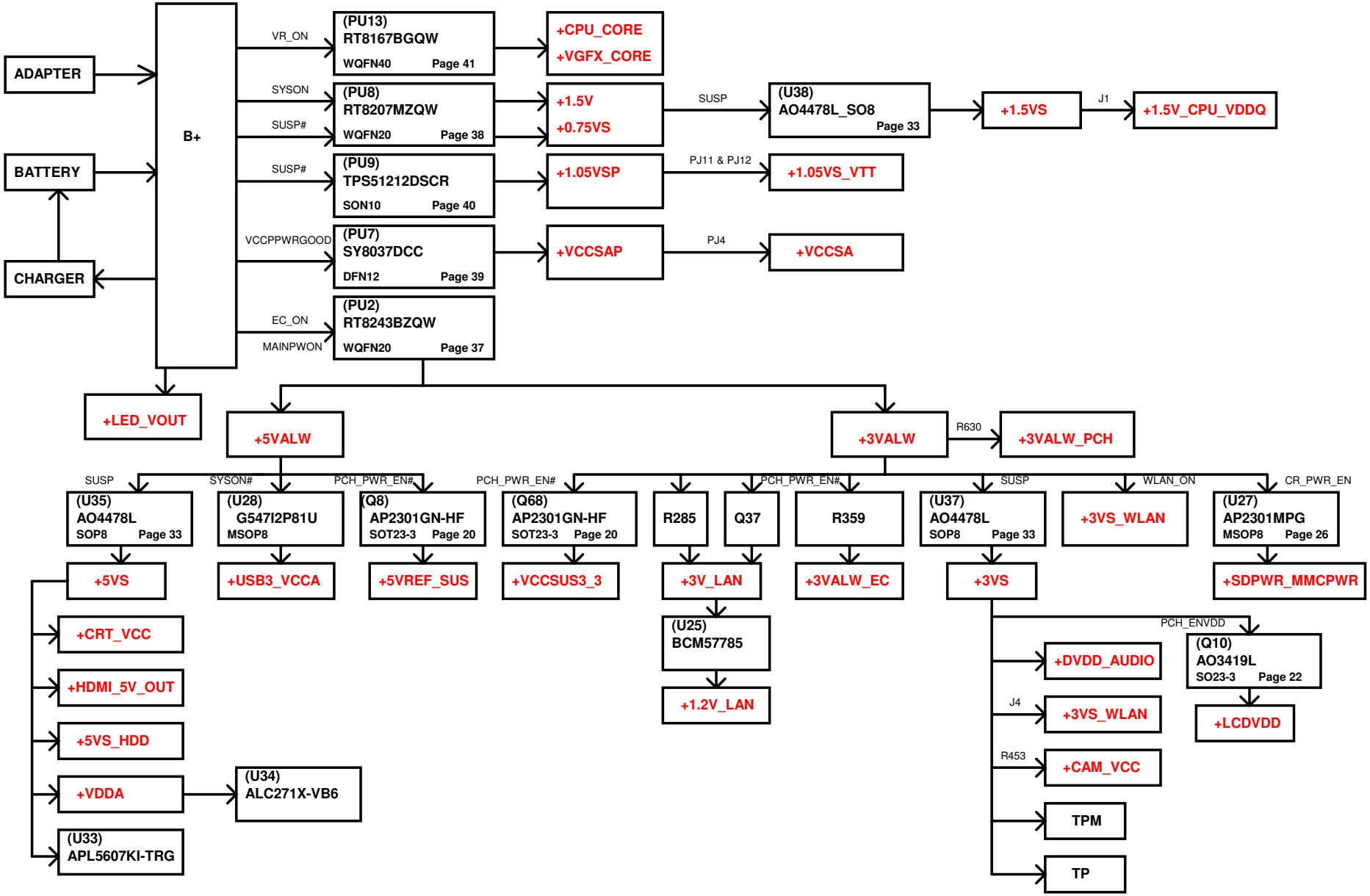
Size | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 42 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.1			2010/12/29	
2			0.1	---		2010/12/29	
3						2011/02/08	
4						2011/02/08	
5						2011/02/08	
6				---		2011/02/08	
7				---		2011/02/16	
8				---		2011/05/13	PVT2
9				---		2011/05/13	PVT2
10				---		2011/05/13	PVT2
11				---		2011/05/13	PVT2
12						2011/05/13	PVT2
13							
14							
15							

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0
Date: Friday, April 20, 2012 | Sheet 43 of 45



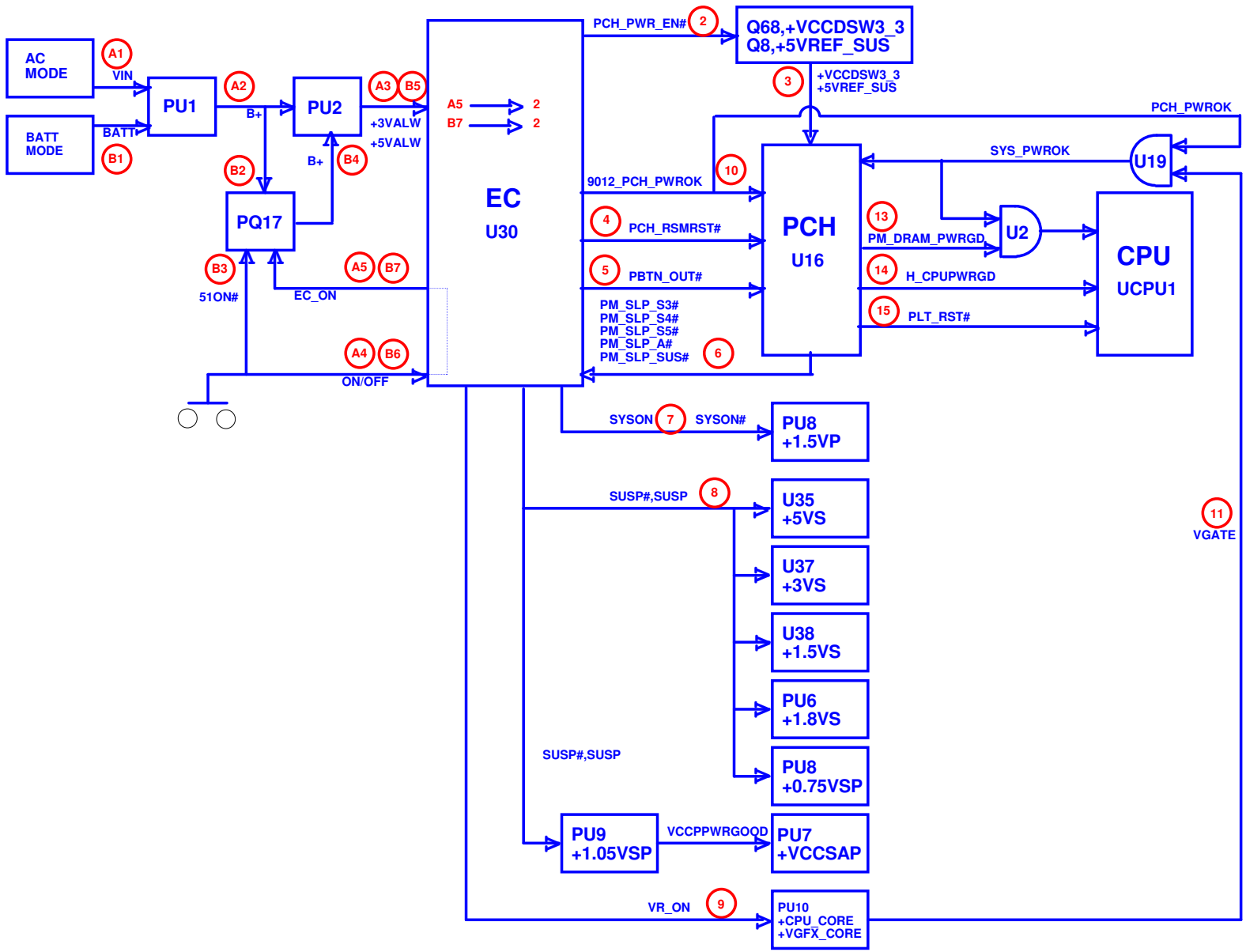
Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: Power Rail

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 44 of 45



Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: Q1VZC M/B LA-8941P Schematic | Rev: 1.0

Date: Friday, April 20, 2012 | Sheet 45 of 45