

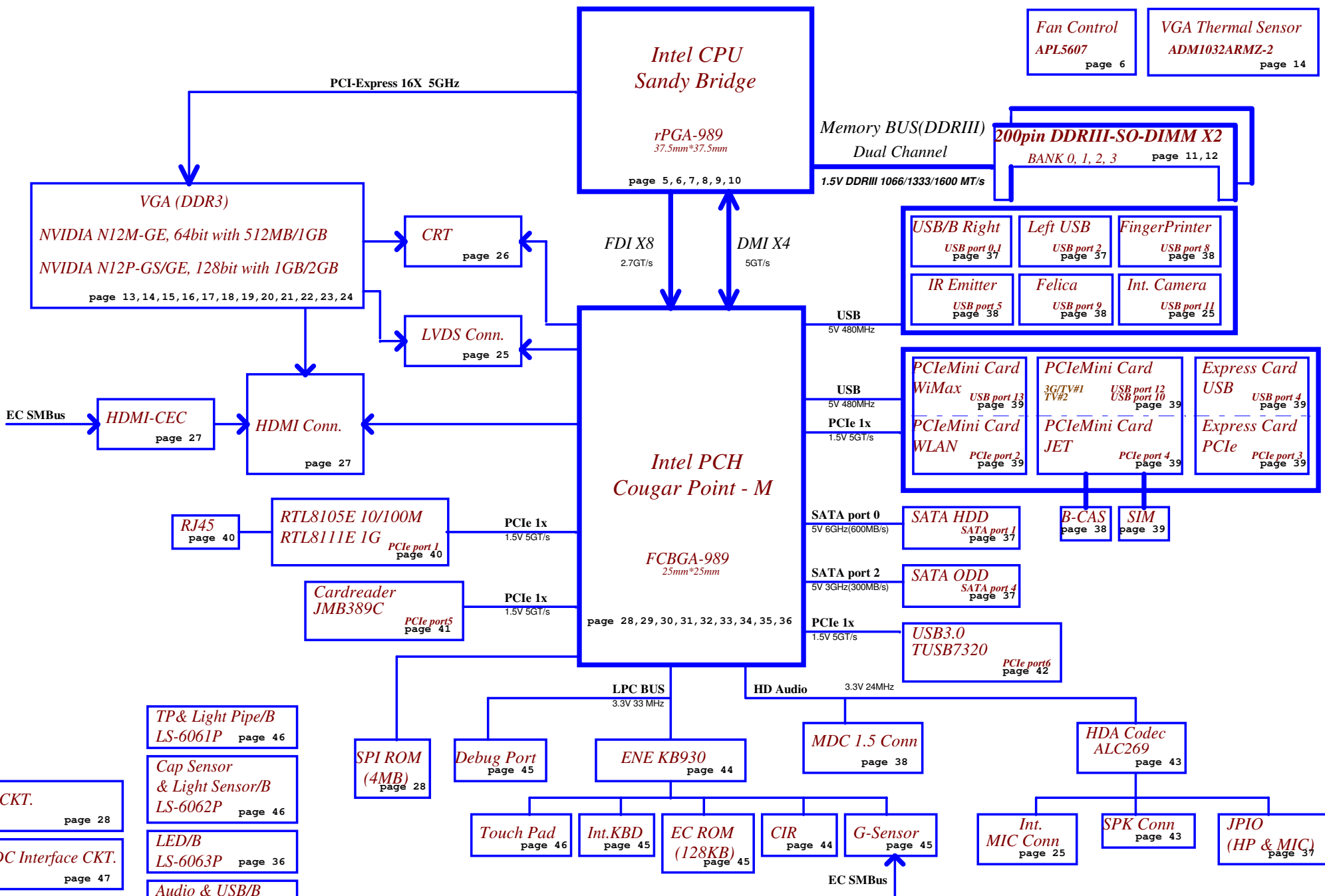
PHQAA

Marseille 10R/10RG

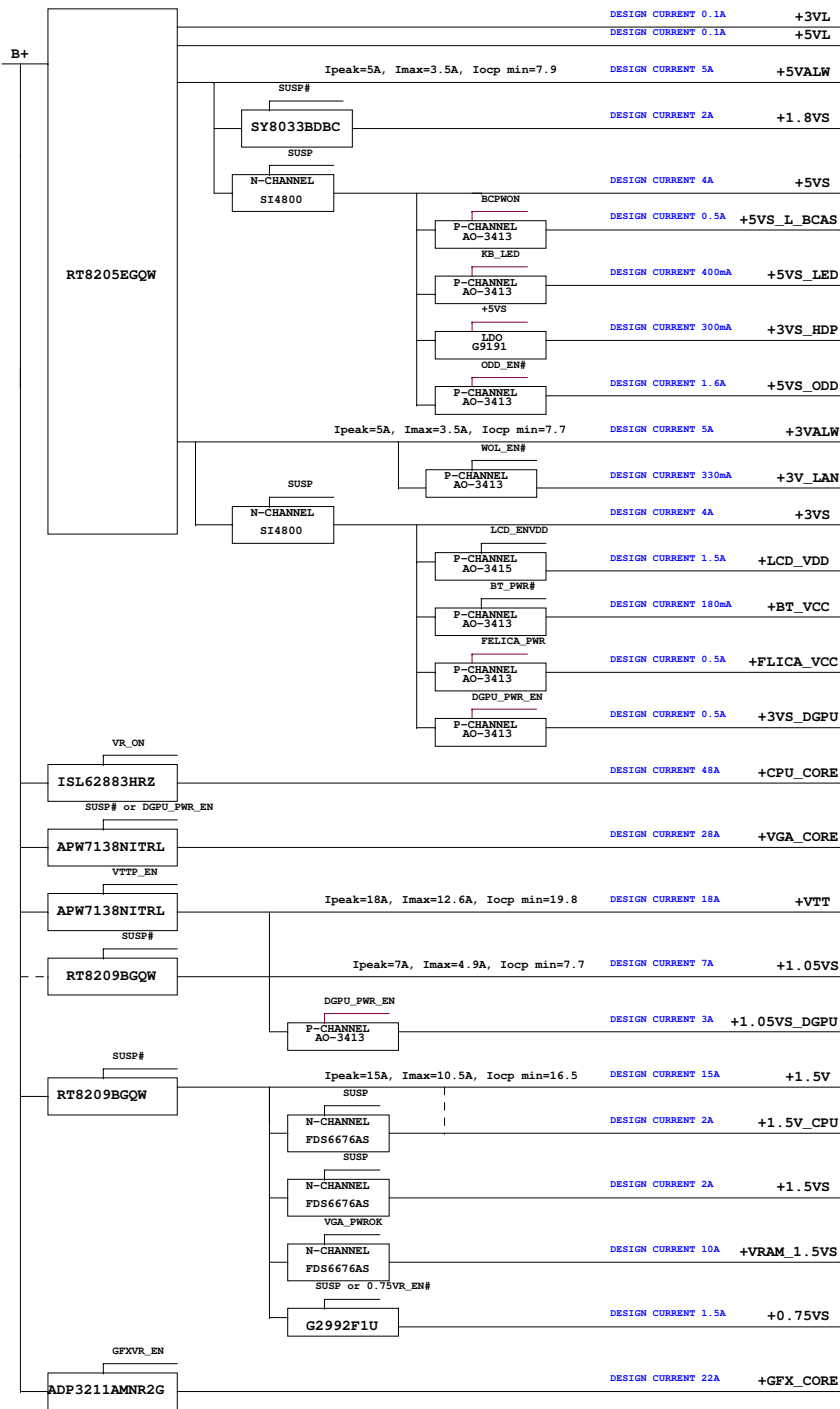
LA-6831P REV 0.1 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2010-07-05 Rev 0.1

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA (OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

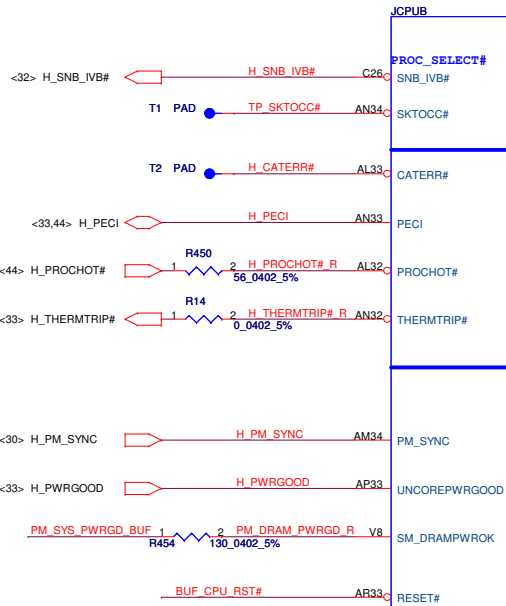
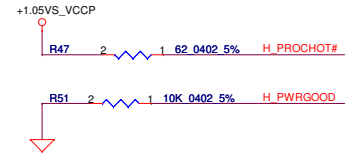
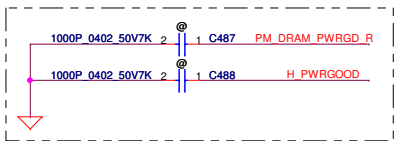
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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100 MHz

A28 CLK CPU DMI
A27 CLK CPU DMI#

CLK_CPU_DMI <29>
CLK_CPU_DMI# <29>

120 MHz

A16 CLK CPU DPLL
A15 CLK CPU DPLL#

DPLL_REF_SSCLK
DPLL_REF_SSCLK#

BCLK
BCLK#

SM_DRAMRST#

SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]

AK1 SM_RCOMP 0 R1437 2 140 0402 1%
A5 SM_RCOMP 1 R1439 2 25.5 0402 1%
A4 SM_RCOMP 2 R1439 2 200 0402 1%

DDR3 Compensation Signals
Layout Note: Place these resistors near Processor

PRDY#
PREQ#

AP28 XDP PRDY# R R1 1 2 0 0402 5%
AP27 XDP PREQ# R R2 1 2 0 0402 5%

TCK
TMS
TRST#

AR26 XDP TCK R R4 1 2 0 0402 5%
AR27 XDP TMS R R6 1 2 0 0402 5%
AP30 XDP TRST# R R7 1 2 0 0402 5%

TDI
TDO

AR28 XDP TDI R R8 1 2 0 0402 5%
AP26 XDP TDO R R10 1 2 0 0402 5%

DBR#

AL35 XDP DBRSET# R R11 1 2 0 0402 5%

BPM#(0)
BPM#(1)
BPM#(2)
BPM#(3)
BPM#(4)
BPM#(5)
BPM#(6)
BPM#(7)

AT28 XDP BPM#0 R R12 1 2 0 0402 5%
AR29 XDP BPM#1 R R13 1 2 0 0402 5%
AR30 XDP BPM#2 R R15 1 2 0 0402 5%
AT30 XDP BPM#3 R R18 1 2 0 0402 5%
AP32 XDP BPM#4 R R19 1 2 0 0402 5%
AR31 XDP BPM#5 R R20 1 2 0 0402 5%
AT31 XDP BPM#6 R R21 1 2 0 0402 5%
AR32 XDP BPM#7 R R23 1 2 0 0402 5%

XDP BPM#0
XDP BPM#1
XDP BPM#2
XDP BPM#3
XDP BPM#4
XDP BPM#5
XDP BPM#6
XDP BPM#7

R24 1 2 0 0402 5%
R25 1 2 0 0402 5%
R26 1 2 0 0402 5%
R27 1 2 0 0402 5%

CFG12 <10>
CFG13 <10>
CFG14 <10>
CFG15 <10>

Close to CPU side

R38 1 2 0 0402 5%

XDP DBRSET# <30>

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

XDP DBRSET#

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XDP DBRSET#

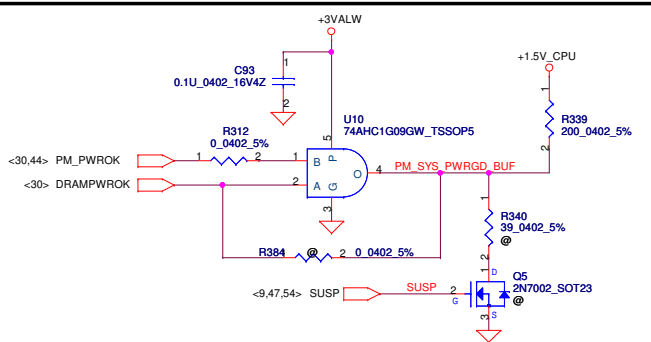
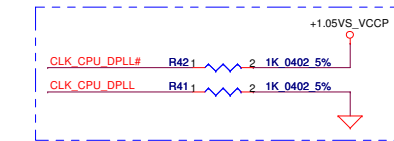
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XDP DBRSET#

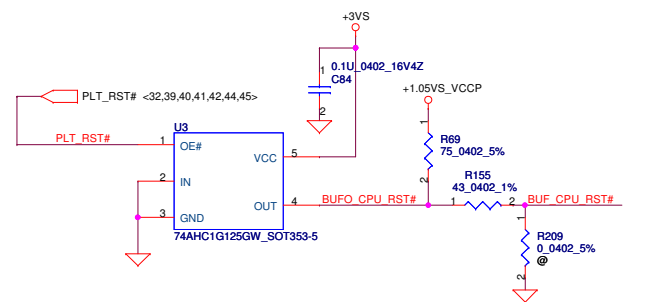
XDP DBRSET#

XDP DBRSET#

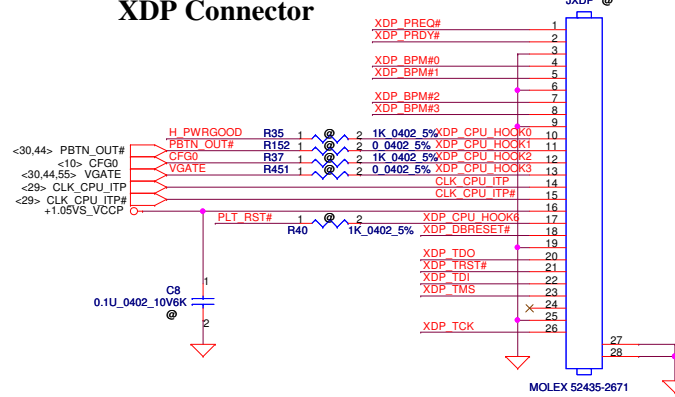
Stuff R41 and R42 if do not support eDP



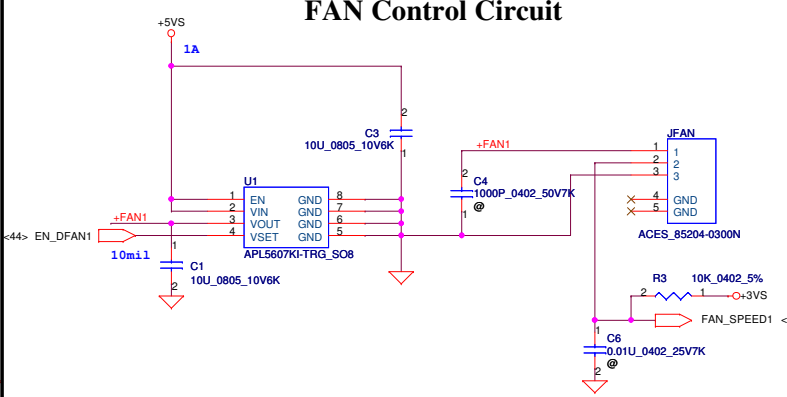
Buffered Reset to CPU



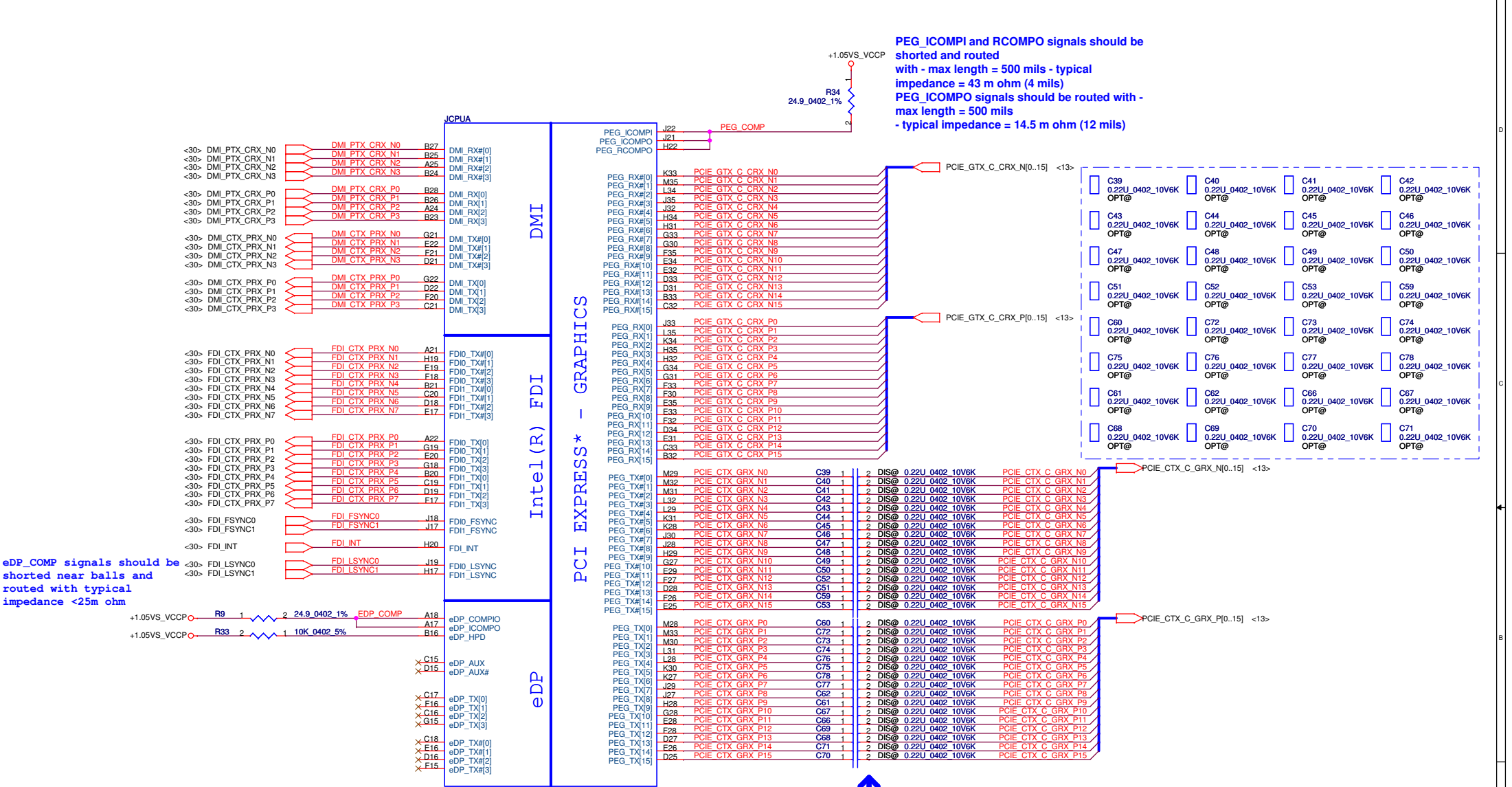
XDP Connector



FAN Control Circuit



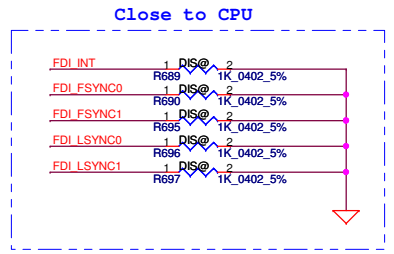
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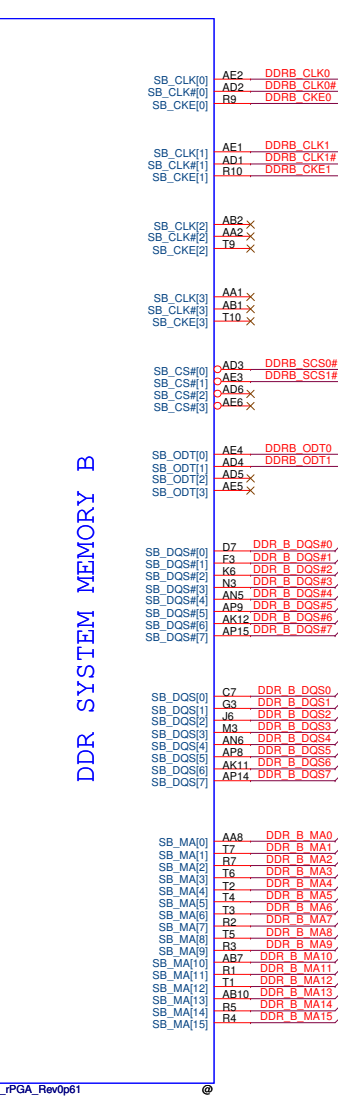
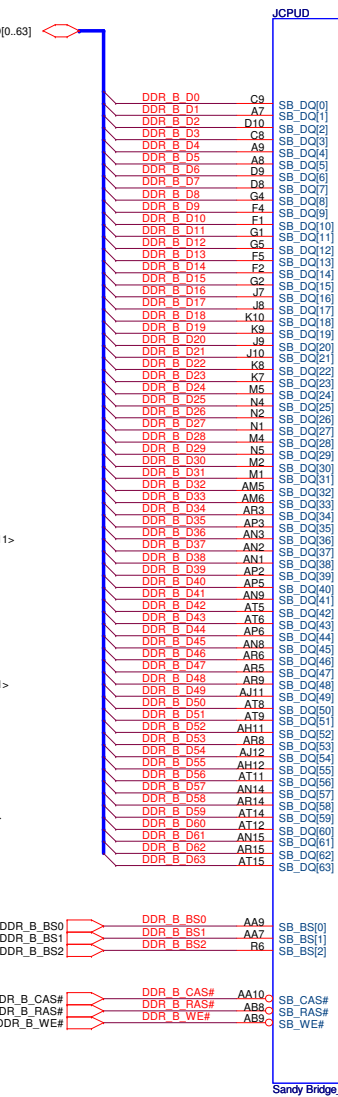
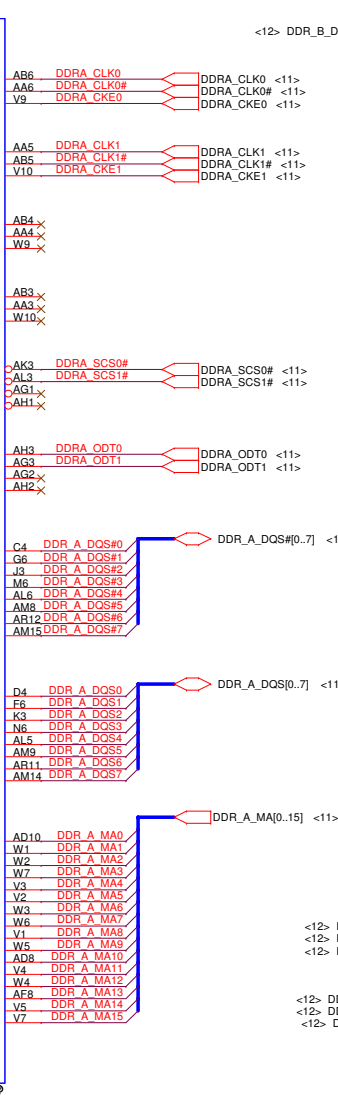
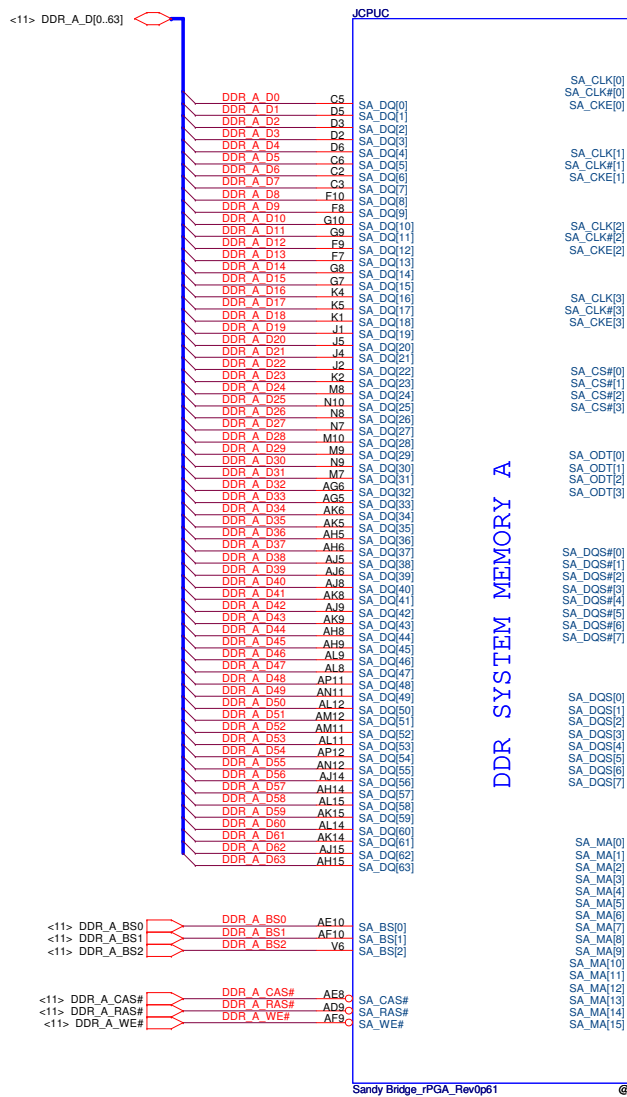
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

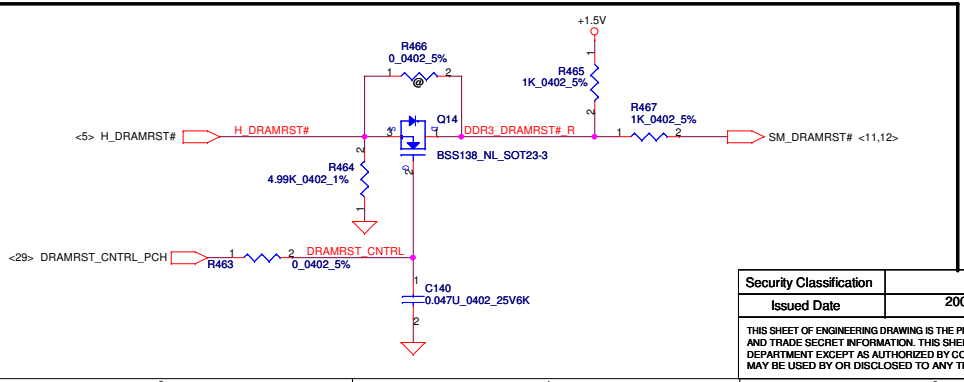


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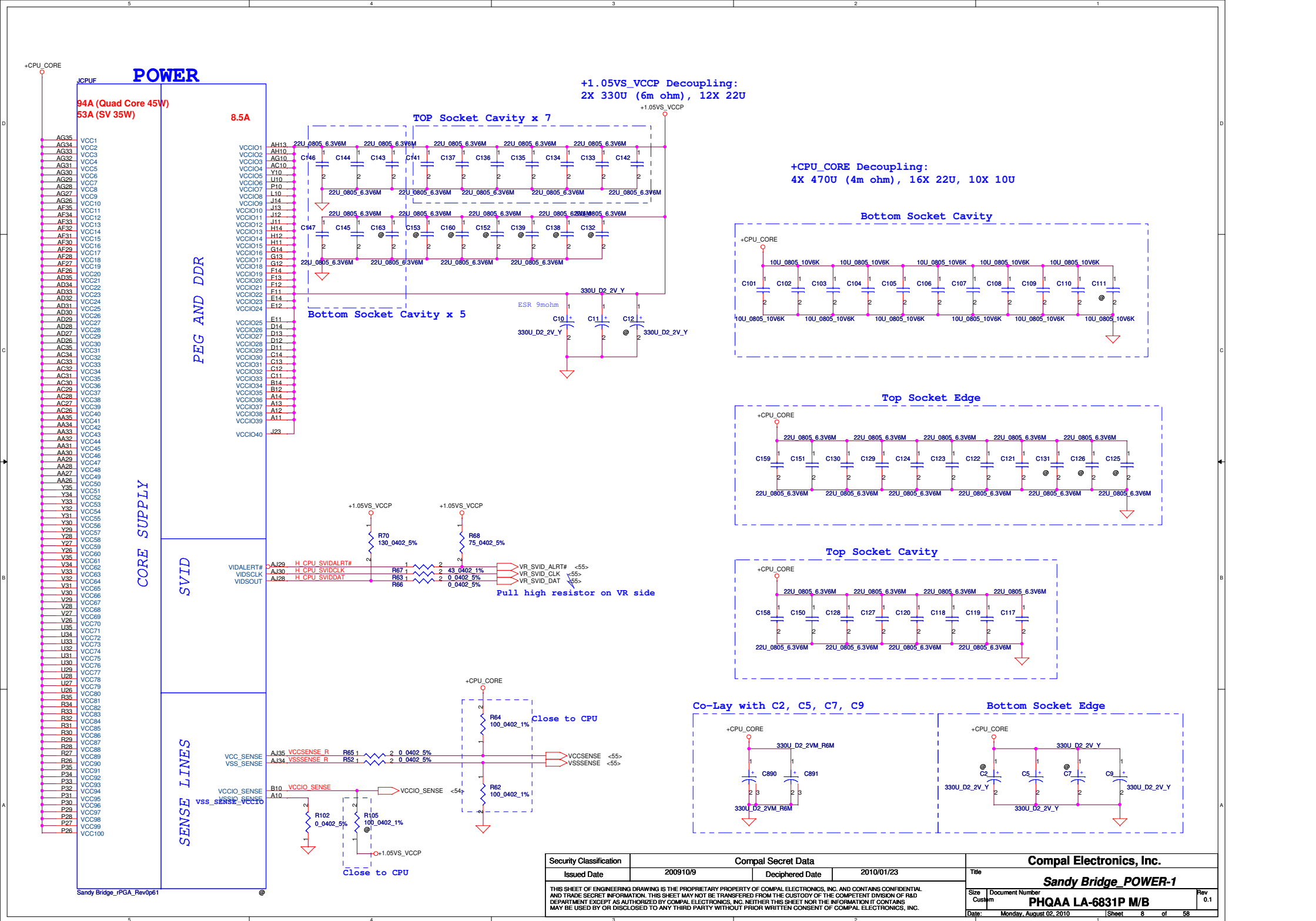


DDR SYSTEM MEMORY A

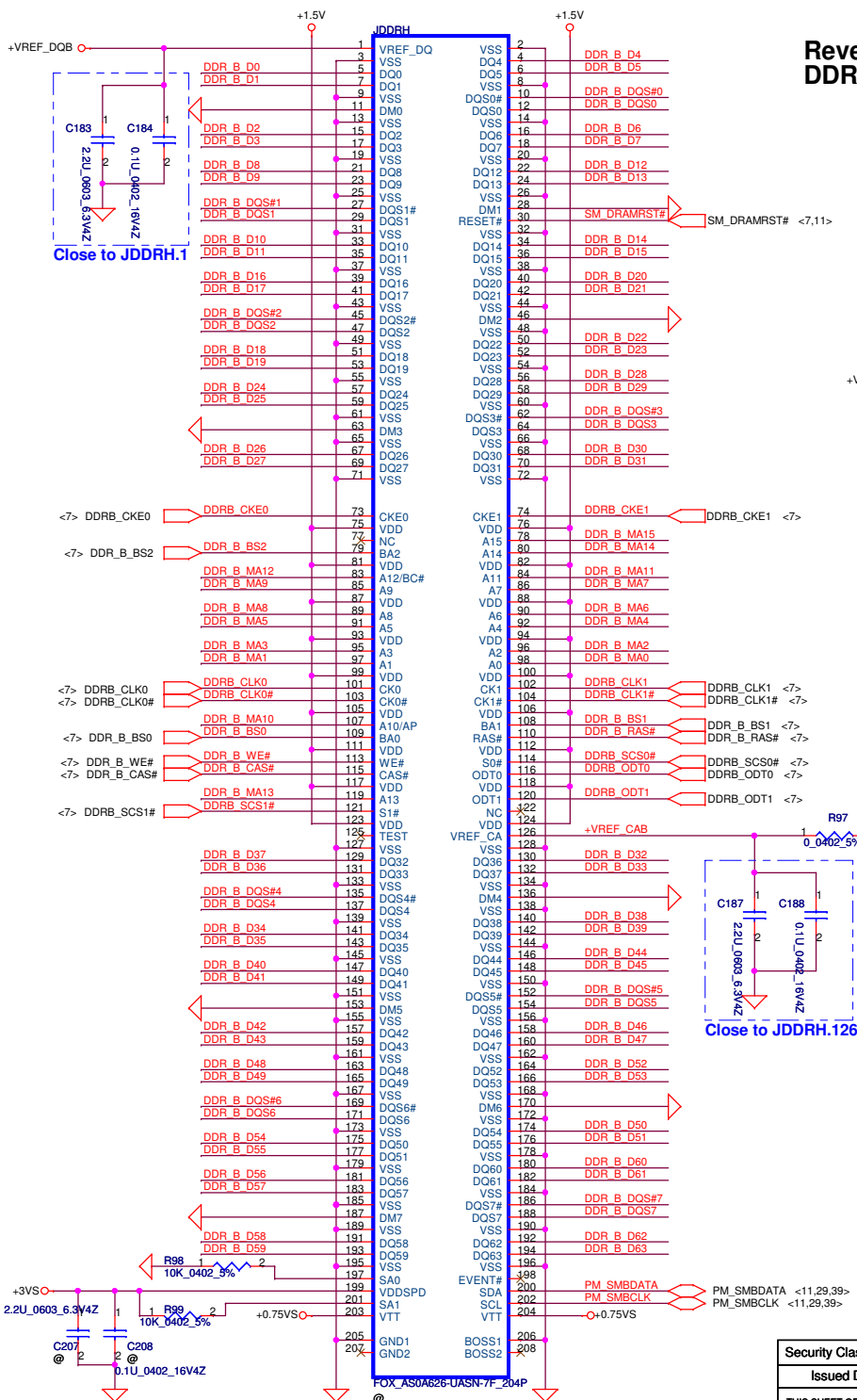
DDR SYSTEM MEMORY B



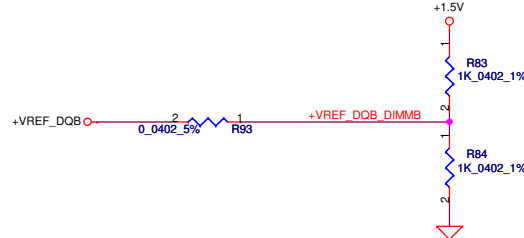
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Reverse Type DDR3 SO-DIMM B



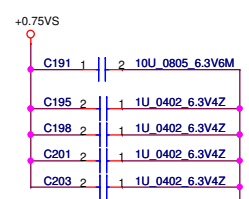
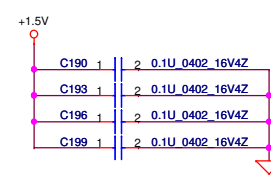
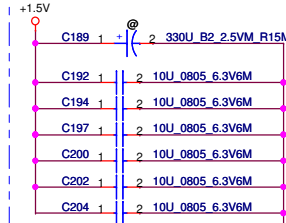
DDR_B_DQS#[0..7] <7>
DDR_B_DQS[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_MA[0..15] <7>



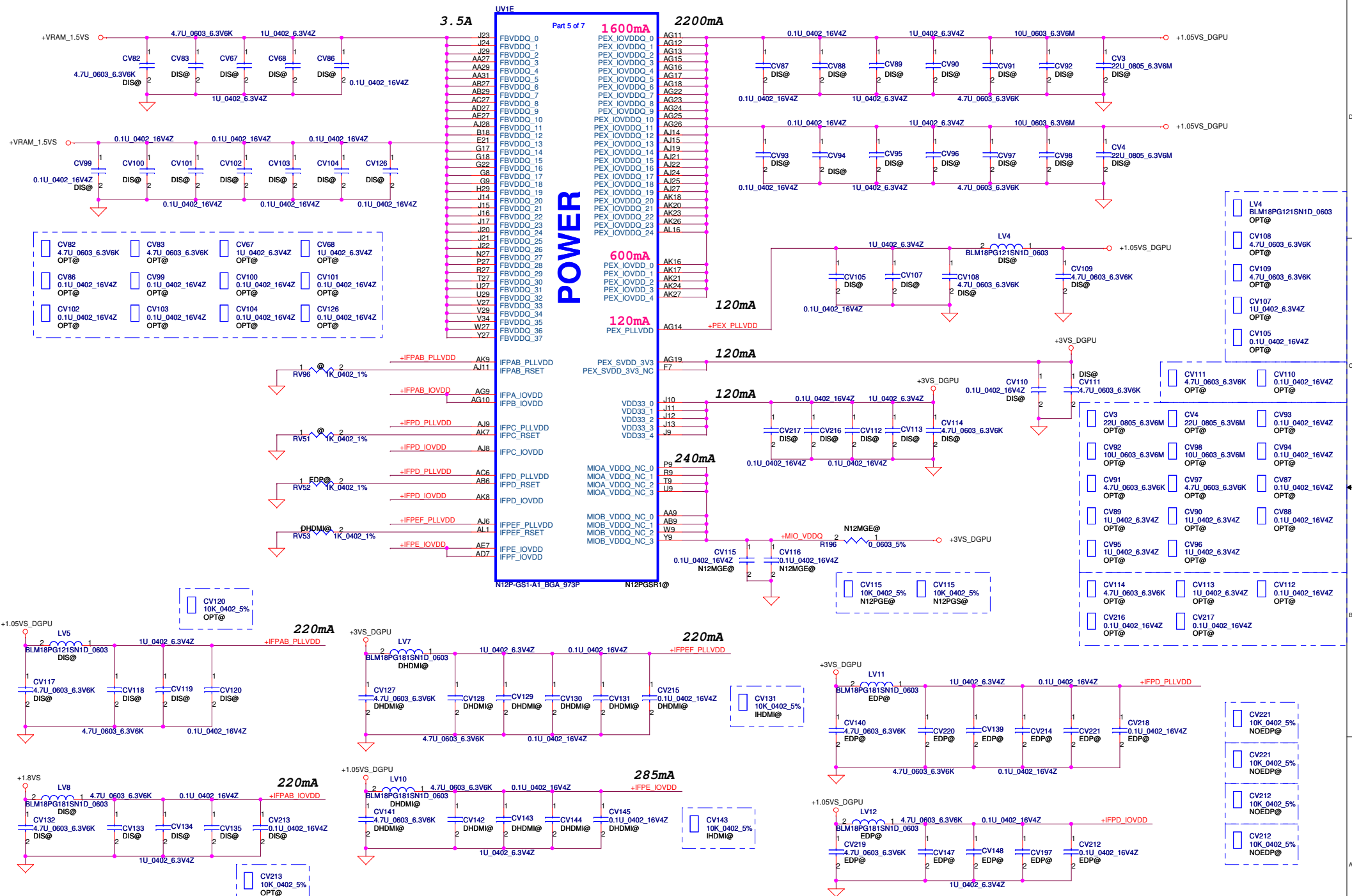
Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204



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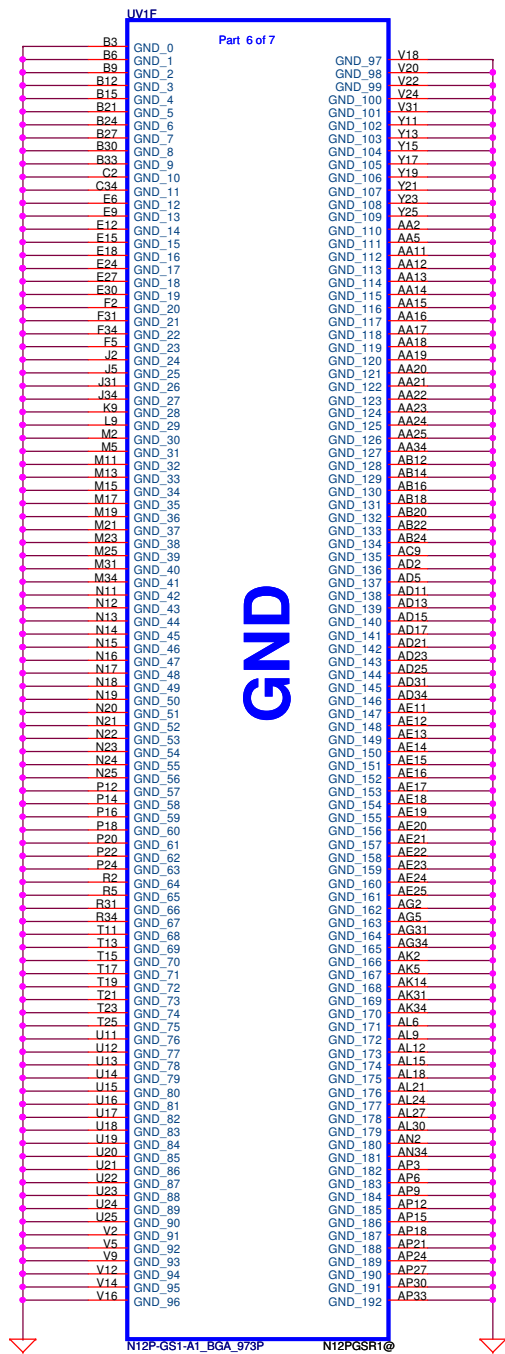
VGA_POWER

PHQAA LA-6831P M/B

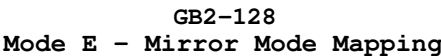
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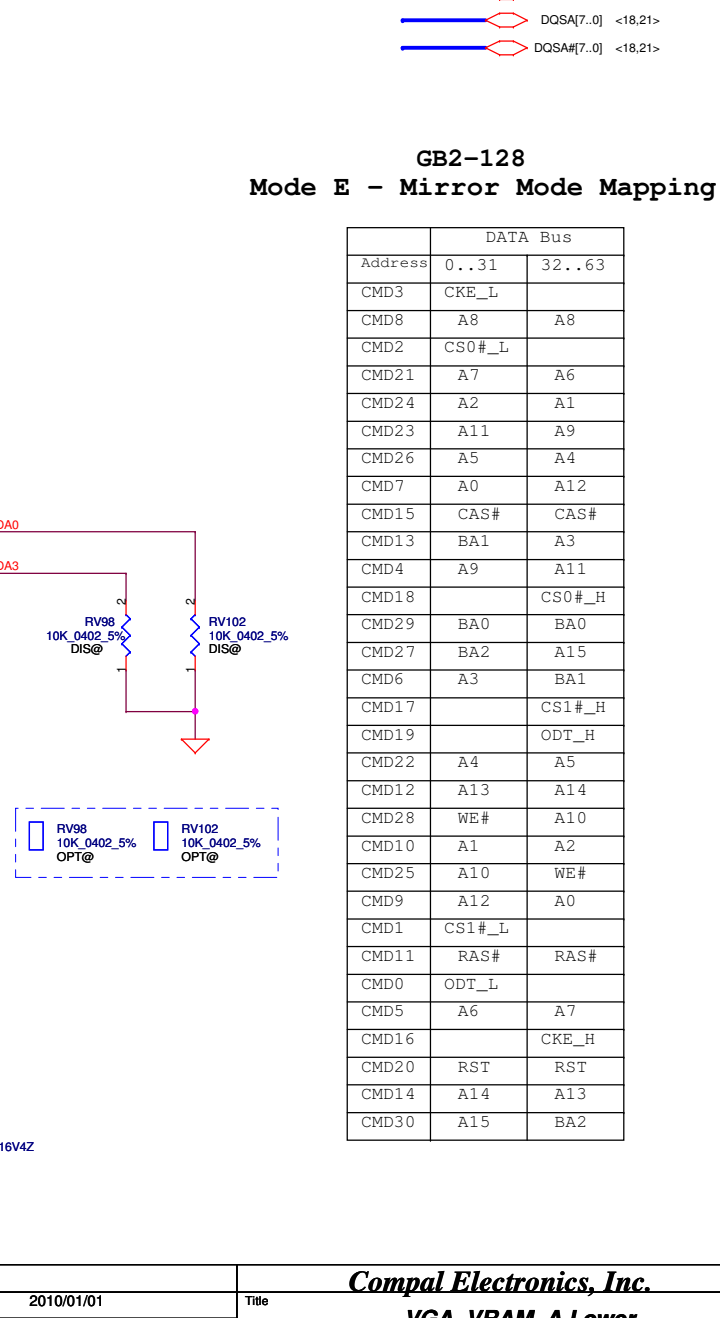
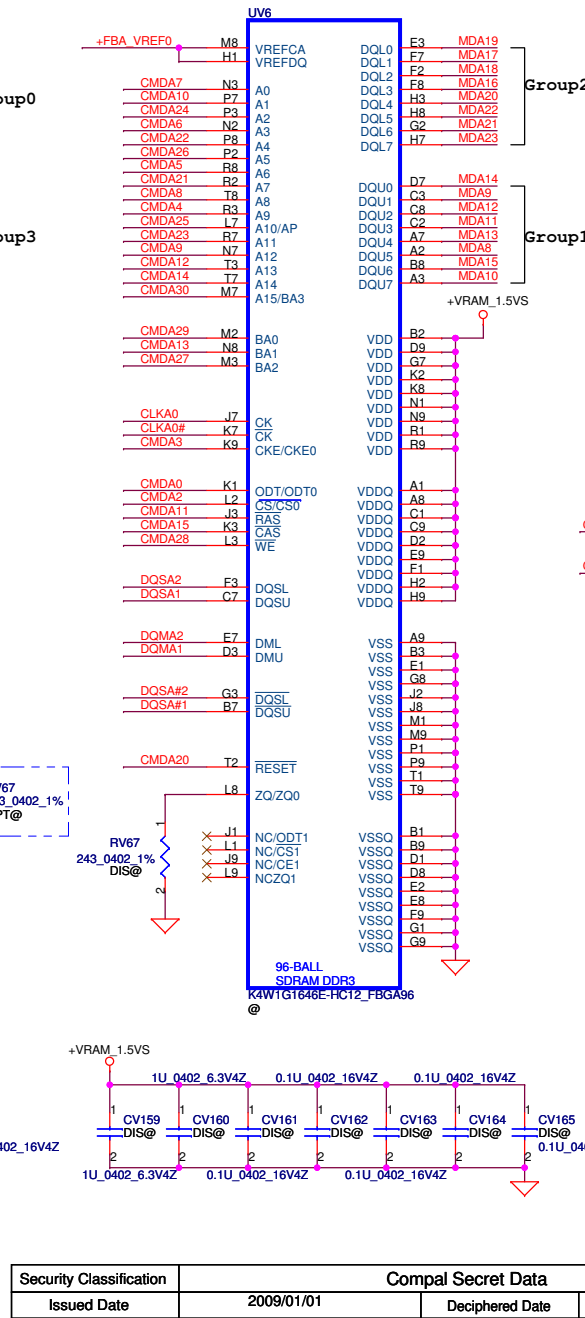
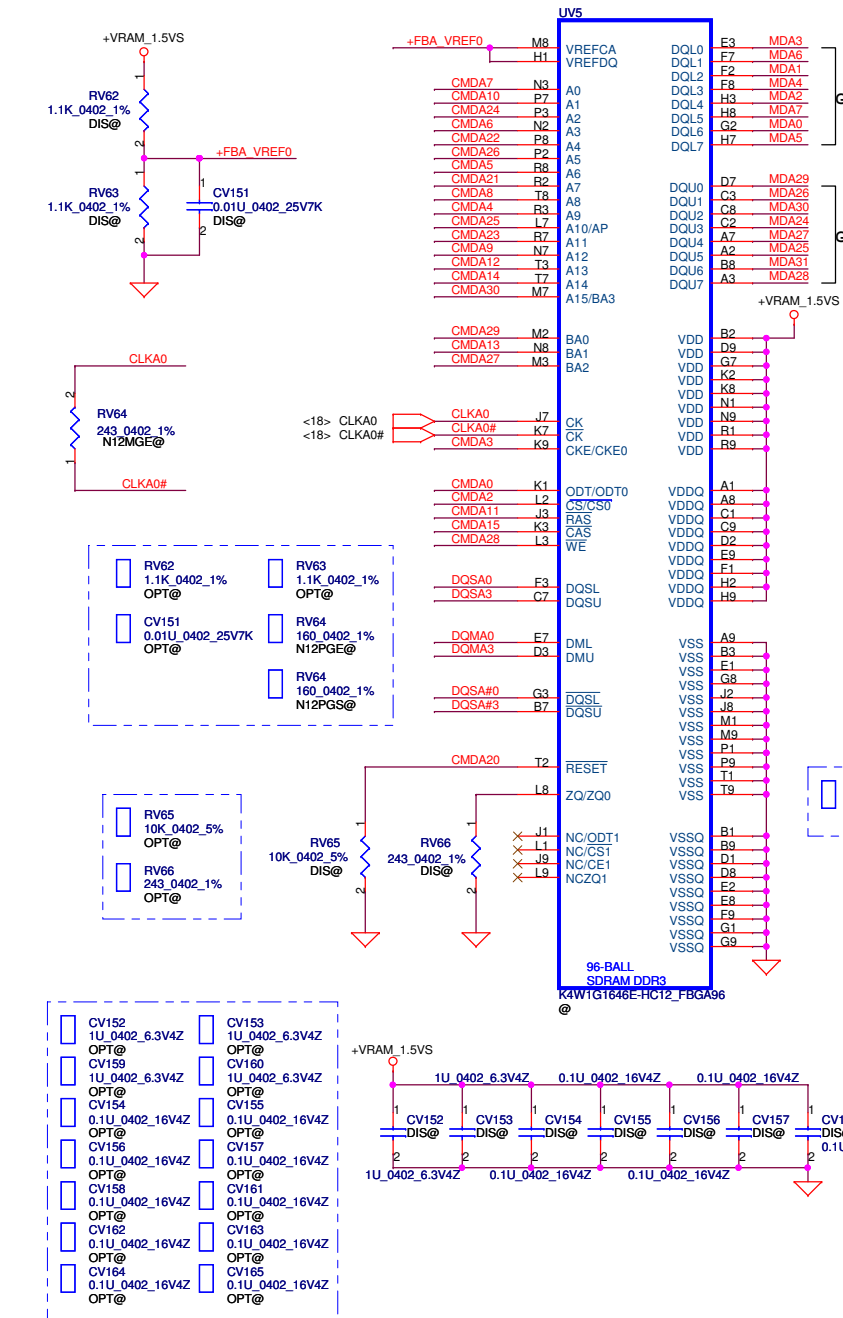
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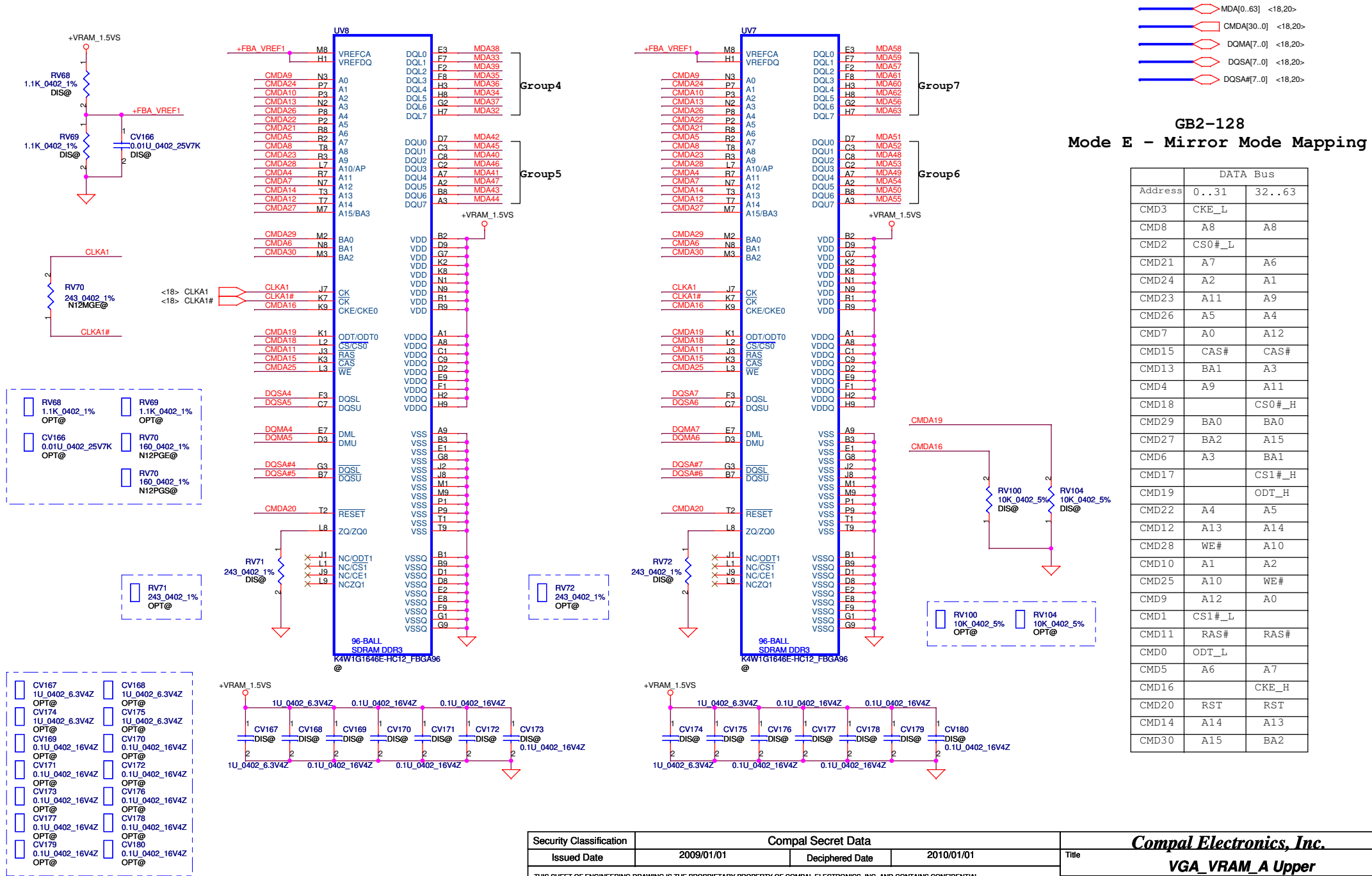
Memory Partition A - Lower 32 bits



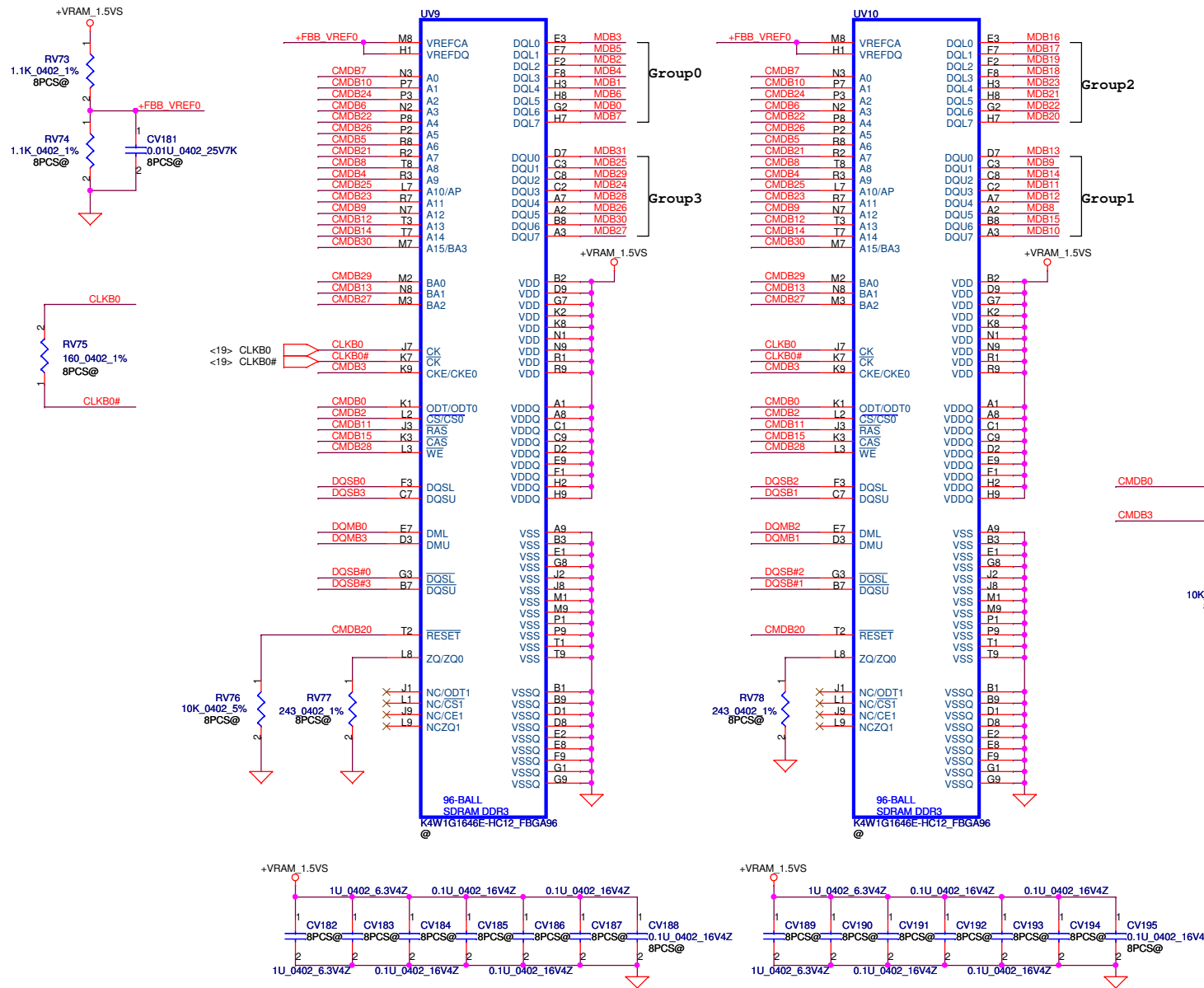
GB2-128
Mode E - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Memory Partition A - Upper 32 bits



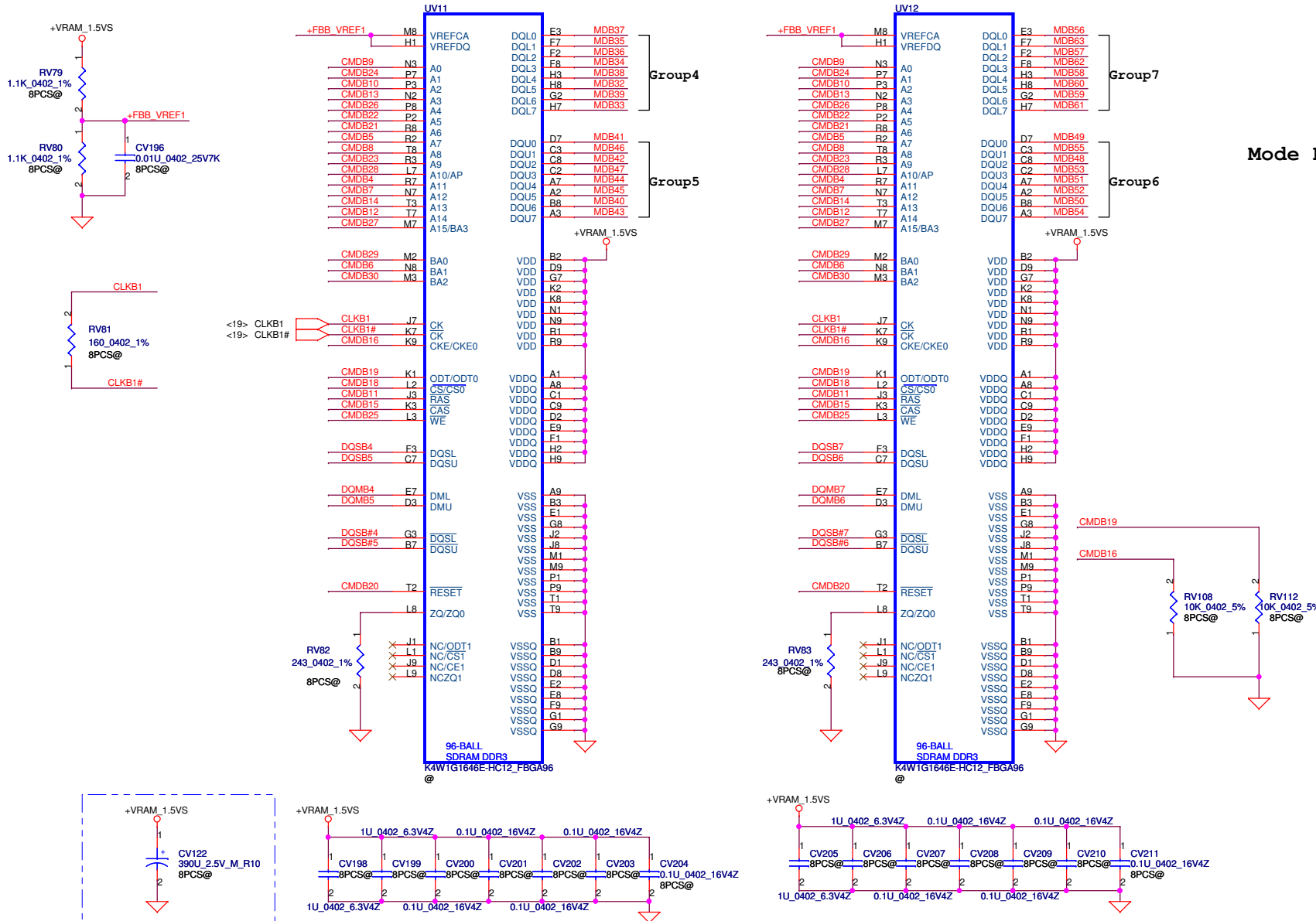
Memory Partition C - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

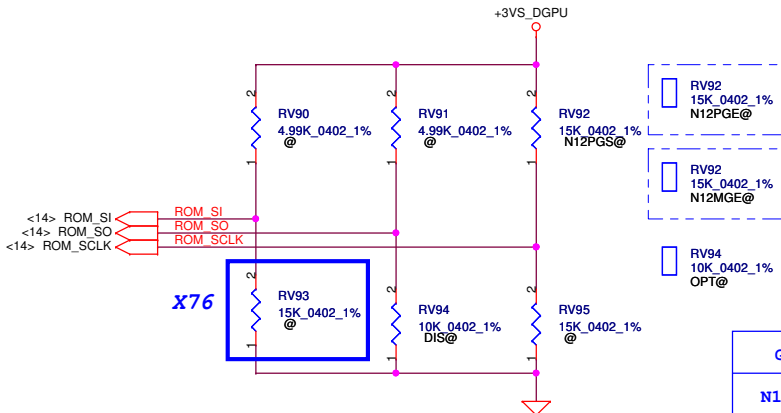
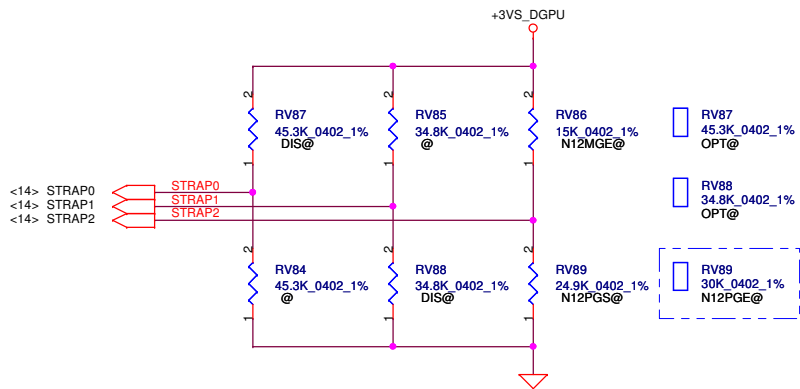
Memory Partition C - Upper 32 bits



- MD[0..63] <19,22>
- CMDB[30..0] <19,22>
- DOMB[7..0] <19,22>
- DQSB[7..0] <19,22>
- DQSB# [7..0] <19,22>

GB2-128
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K
	1G	0010	PD 15K
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K
	1G	0011	PD 20K

SD034150280

SD034200280

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

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					Date:	Monday, August 02, 2010	Sheet 24 of 58

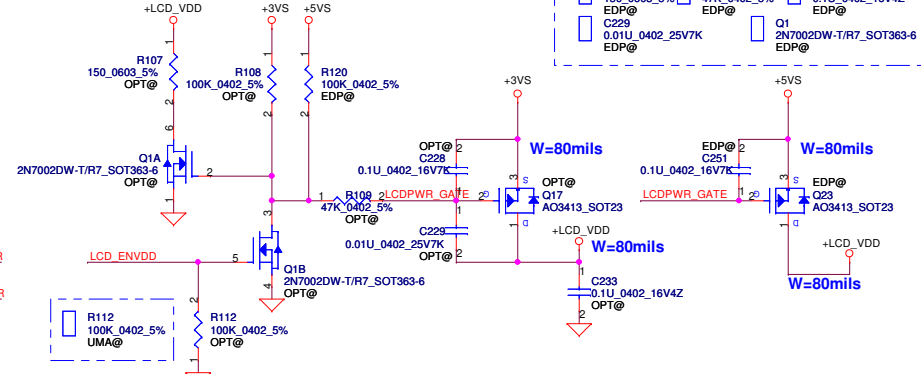
Compal Electronics, Inc.

VGA_MSIC

PHQAA LA-6831P M/B

Signal	Pin	Function	Supply	Current	Notes
<31> LCD_TXOUT0+	R262	OPT0_2	0.0402	5%	LVDS_TXOUT0+
<31> LCD_TXOUT0-	R263	OPT0_2	0.0402	5%	LVDS_TXOUT0-
<31> LCD_TXOUT1+	R265	OPT0_2	0.0402	5%	LVDS_TXOUT1+
<31> LCD_TXOUT1-	R264	OPT0_2	0.0402	5%	LVDS_TXOUT1-
<31> LCD_TXOUT2+	R298	OPT0_2	0.0402	5%	LVDS_TXOUT2+
<31> LCD_TXOUT2-	R277	OPT0_2	0.0402	5%	LVDS_TXOUT2-
<31> LCD_TXCLK+	R297	OPT0_2	0.0402	5%	LVDS_TXCLK+
<31> LCD_TXCLK-	R296	OPT0_2	0.0402	5%	LVDS_TXCLK-
<31> LCD_EDID_CLK	R300	OPT0_2	0.0402	5%	LVDS_EDID_CLK
<31> LCD_EDID_DATA	R299	OPT0_2	0.0402	5%	LVDS_EDID_DATA
<31> PCH_PWM	R332	OPT0_2	0.0402	5%	LED_PWM
<31> UMA_ENVDD	R350	OPT0_2	0.0402	5%	LCD_ENVDD
<31> UMA_ENBKL	R357	OPT0_2	0.0402	5%	EC_ENBKL <44>

Figure 10 shows the EMI filter circuit for USB20_P11 and USB20_N11. The circuit includes a WCM-2012-900T_0B05 filter component. The input signals are USB20_P11 and USB20_N11, which are connected to the filter's input terminals. The filter's output terminals are connected to the USB20_P11 and USB20_N11 signals. The filter is labeled with 'CAM@ 2' and 'R96 0.0402_5%'.



<14>	VGA_TXOUT0+		1	DIS0	2	R331	0	0402_5%	LVDS_TXOUT0+
<14>	VGA_TXOUT0-		1	DIS0	2	R309	0	0402_5%	LVDS_TXOUT0-
<14>	VGA_TXOUT1+		1	DIS0	2	R317	0	0402_5%	LVDS_TXOUT1+
<14>	VGA_TXOUT1-		1	DIS0	2	R315	0	0402_5%	LVDS_TXOUT1-
<14>	VGA_TXOUT2+		1	DIS0	2	R308	0	0402_5%	LVDS_TXOUT2+
<14>	VGA_TXOUT2-		1	DIS0	2	R302	0	0402_5%	LVDS_TXOUT2-
<14>	VGA_TXCLK+		1	DIS0	2	R305	0	0402_5%	LVDS_TXCLK+
<14>	VGA_TXCLK-		1	DIS0	2	R304	0	0402_5%	LVDS_TXCLK-
<13>	VGA_EDID_CLK		1	DIS0	2	R314	0	0402_5%	LVDS_EDID_CLK
<13>	VGA_EDID_DATA		1	DIS0	2	R310	0	0402_5%	LVDS_EDID_DATA
<13>	VGA_BL_PWM		1	DIS0	2	R349	0	0402_5%	LED_PWM
<13>	VGA_ENVDD		1	DIS0	2	R356	0	0402_5%	LCD_ENVDD
<13>	VGA_ENBKL		1	DIS0	2	R358	0	0402_5%	EC_ENBKL

[illegible]

Signal	Pin	Function	Value	Frequency	Source
<14> VGA_TZOUT0+	R500	1 30 @	2	0.0402 5%	LVDS_TZOUT0+
<14> VGA_TZOUT0-	R501	1 30 @	2	0.0402 5%	LVDS_TZOUT0-
<14> VGA_TZOUT1+	R502	1 30 @	2	0.0402 5%	LVDS_TZOUT1+
<14> VGA_TZOUT1-	R503	1 30 @	2	0.0402 5%	LVDS_TZOUT1-
<14> VGA_TZOUT2+	R504	1 30 @	2	0.0402 5%	LVDS_TZOUT2+
<14> VGA_TZOUT2-	R505	1 30 @	2	0.0402 5%	LVDS_TZOUT2-
<14> VGA_TZCLK+	R507	1 30 @	2	0.0402 5%	LVDS_TZCLK+
<14> VGA_TZCLK-	R508	1 30 @	2	0.0402 5%	LVDS_TZCLK-

LVDS TZOUT0+
 LVDS TZOUT0-
 LVDS TZOUT1+
 LVDS TZOUT1-
 LVDS TZOUT2+
 LVDS TZOUT2-
 LVDS TZCLK+
 LVDS TZCLK-

+5VSWLW

IO#	IO Name	IO#	IO Name	IO#	IO Name	IO#	IO Name	IO#	IO Name
<14>	VGA_EDP_TX0+	C880	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT0+		
<14>	VGA_EDP_TX0-	C881	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT0-		
<14>	VGA_EDP_TX1+	C882	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT1+		
<14>	VGA_EDP_TX1-	C883	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT1-		
<14>	VGA_EDP_TX2+	C884	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT2+		
<14>	VGA_EDP_TX2-	C885	EDP@	1	0.1U_0402_16V7K	LVDS	TZOUT2-		
<14>	VGA_EDP_TX3+	C886	EDP@	1	0.1U_0402_16V7K	LVDS	TZCLK+		
<14>	VGA_EDP_TX3-	C887	EDP@	1	0.1U_0402_16V7K	LVDS	TZCLK-		
<14>	VGA_EDP_AUX	C888	EDP@	1	0.1U_0402_16V7K	LVDS	EDID_CLK		
<14>	VGA_EDP_AUX	C889	EDP@	1	0.1U_0402_16V7K	LVDS	EDID_DATA		

Close to LVDS1 Connector

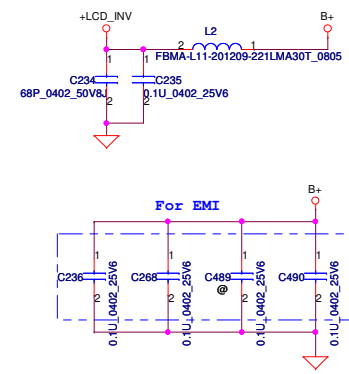
Close to LVDS Connector

The diagram illustrates the internal wiring of the ACES_87242-3001-09 camera module. It shows the connection between the camera's pins and the board's components. Key components include a USB20 P11 R connector, LVDS TXOUT0+/-, TXOUT1+/-, TXOUT2+/-, TXCLK+/-, and TXCLK- signals. The camera's internal components include a CAM@ 0.1U_0402_16V4Z, a D84 @ connector, a PACDN042Y3R_SOT23-3, and a NCD30@ 0.0402_5% resistor. The board's components include a USB20 P11 R connector, LVDS TXOUT0+/-, TXOUT1+/-, TXOUT2+/-, TXCLK+/-, and TXCLK- signals. The board's internal components include a CAM@ 0.1U_0402_16V4Z, a D84 @ connector, a PACDN042Y3R_SOT23-3, and a NCD30@ 0.0402_5% resistor. The board's external components include a USB20 P11 R connector, LVDS TXOUT0+/-, TXOUT1+/-, TXOUT2+/-, TXCLK+/-, and TXCLK- signals.

Pin connection diagram for the JLVDS1 component:

- Pin 1: LVDS_TZOUT0+
- Pin 2: LVDS_TZOUT0-
- Pin 3: LVDS_TZOUT1+
- Pin 4: LVDS_TZOUT1-
- Pin 5: LVDS_TZOUT2+
- Pin 6: LVDS_TZOUT2-
- Pin 7: LVDS_TZCLK+
- Pin 8: LVDS_TZCLK-
- Pin 9: +5VALW
- Pin 10: Ground
- Pin 11: GND1
- Pin 12: GND2

Component: JLVDS1
ACES 87213-1000N ©



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OPTIMUS

<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

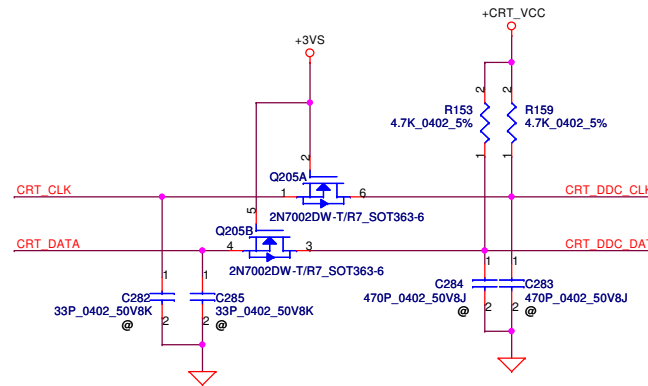
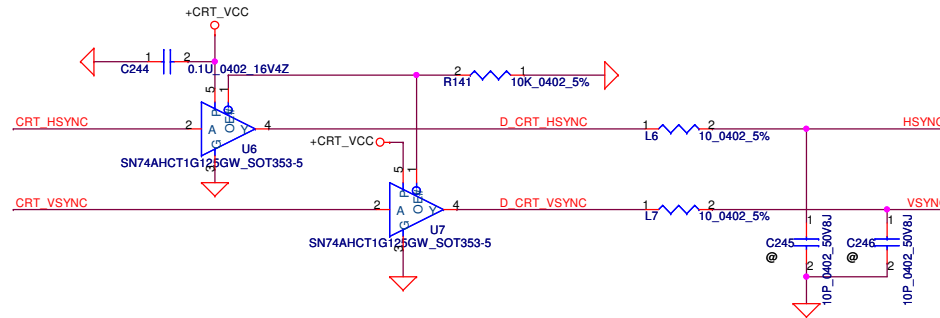
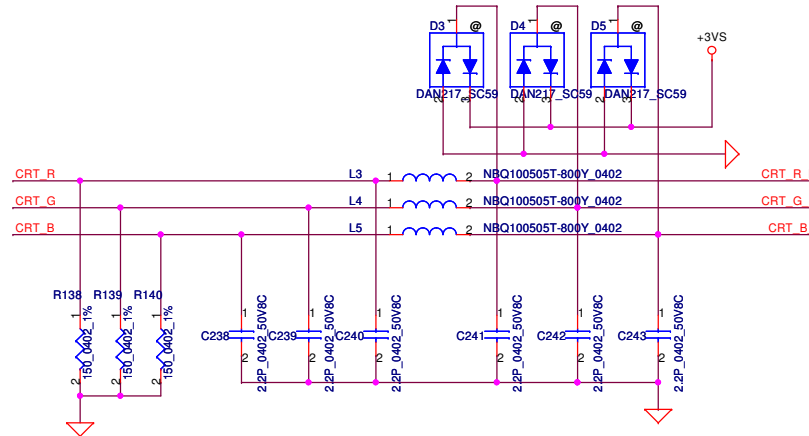
Close to CRT Connector

R200 0.0402_5% UMA@	R204 0.0402_5% UMA@	R211 0.0402_5% UMA@
R213 0.0402_5% UMA@	R235 0.0402_5% UMA@	R236 0.0402_5% UMA@
R261 0.0402_5% UMA@		

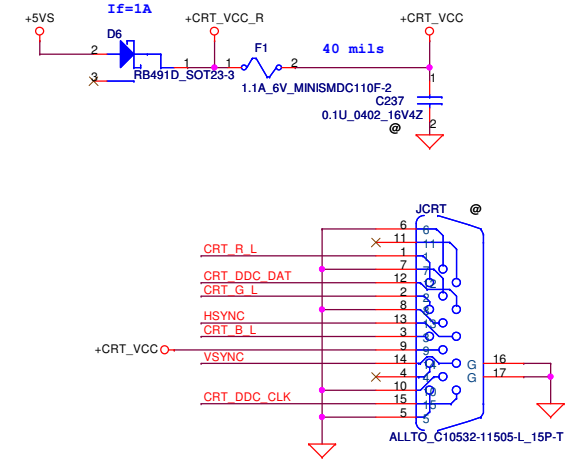
DISCRETE

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<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector

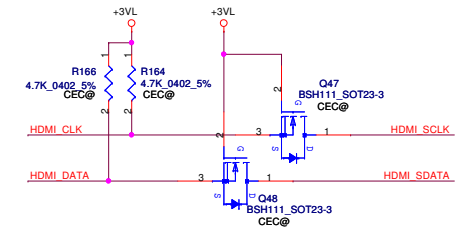
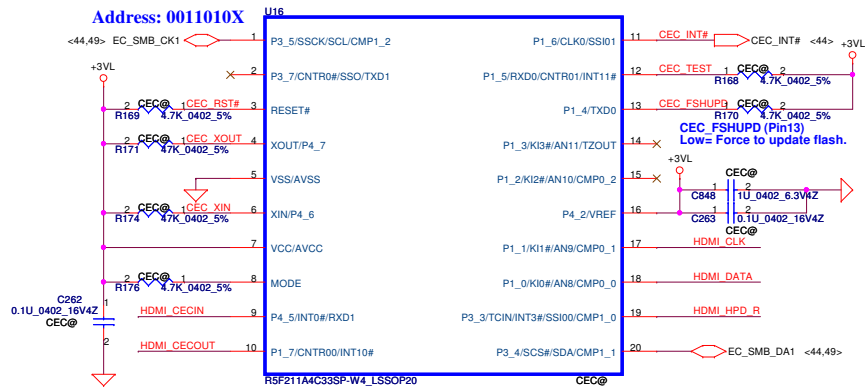
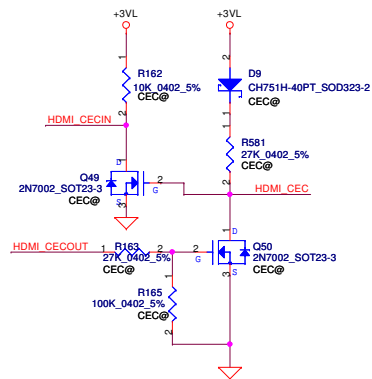


CRT CONNECTOR



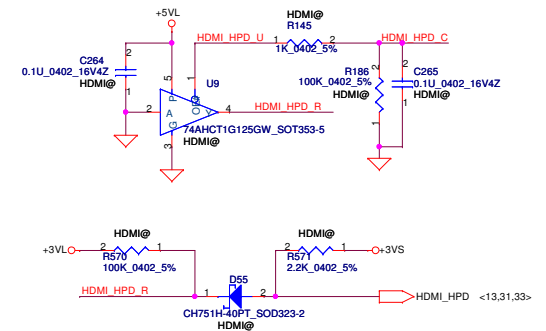
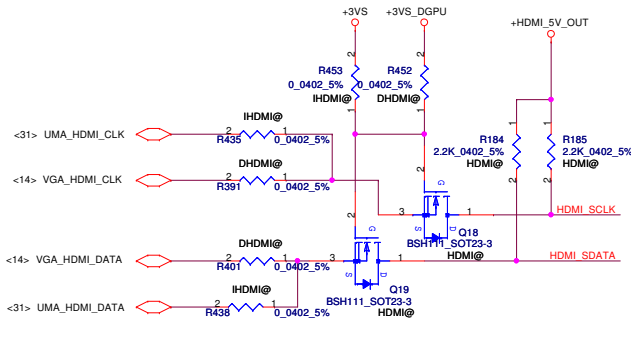
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HDMI CEC Controller



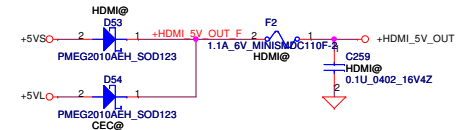
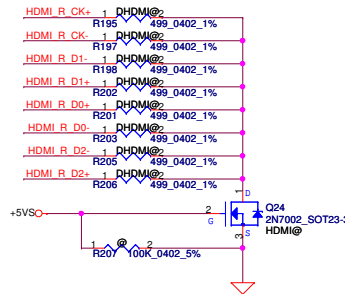
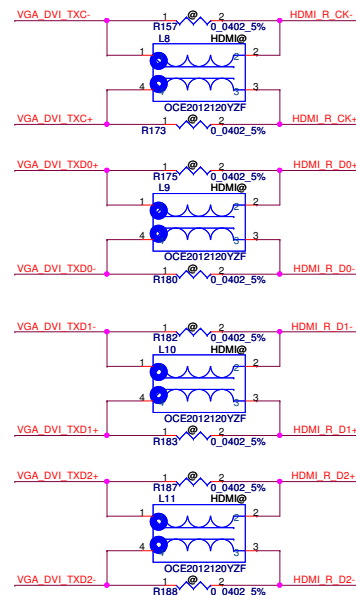
For DISCRETE

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<14>	VGA_HDMI_CLK-		CV293	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXC-
<14>	VGA_HDMI_TX0+		CV294	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD0+
<14>	VGA_HDMI_TX0-		CV297	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD0-
<14>	VGA_HDMI_TX1+		CV299	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD1+
<14>	VGA_HDMI_TX1-		CV298	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD1-
<14>	VGA_HDMI_TX2+		CV295	1	2	0.1U_0402_16V7K_DHDMI@	VGA_DVI_TXD2+
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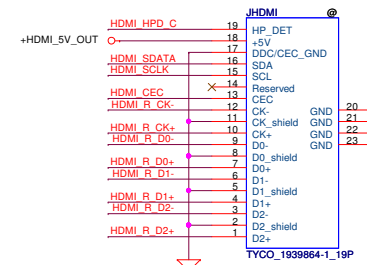


For Optimus

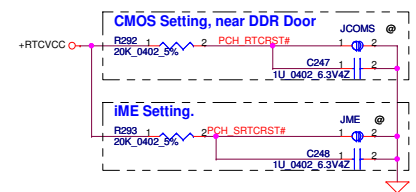
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<31> UMA_HDMI_TX0+	CV306	1	2	0.1U_0402_16V7K IHDM1@	VGA_DVI_TXD0
<31> UMA_HDMI_TX0-	CV302	1	2	0.1U_0402_16V7K IHDM1@	VGA_DVI_TXD0-
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HDMI Connector

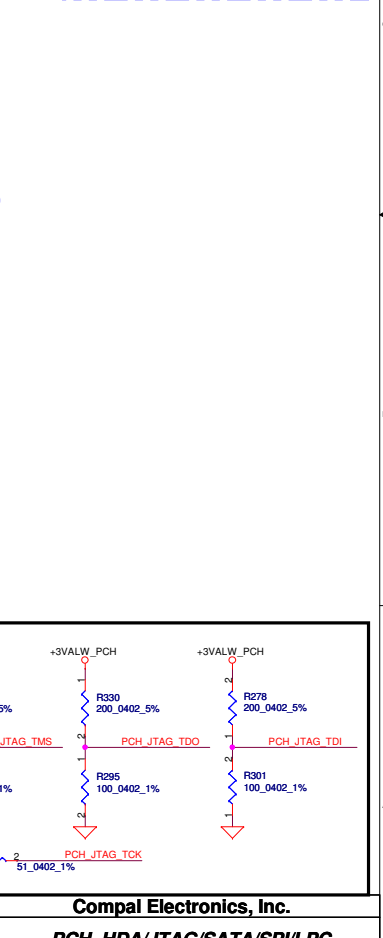
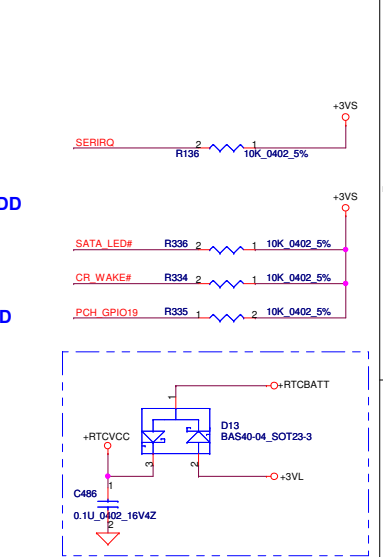
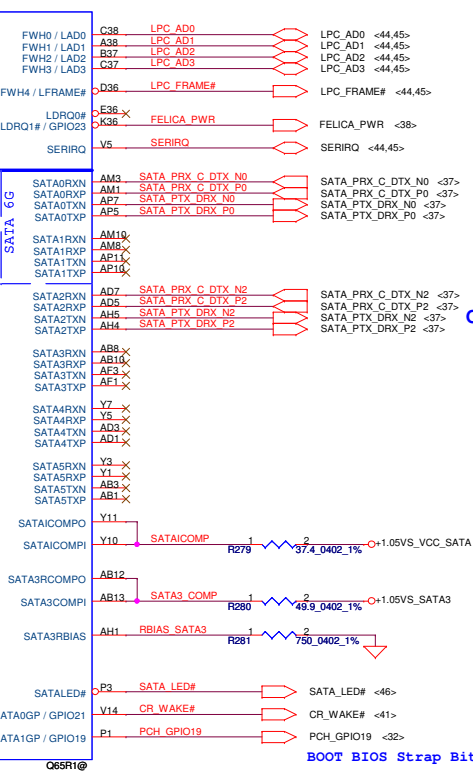
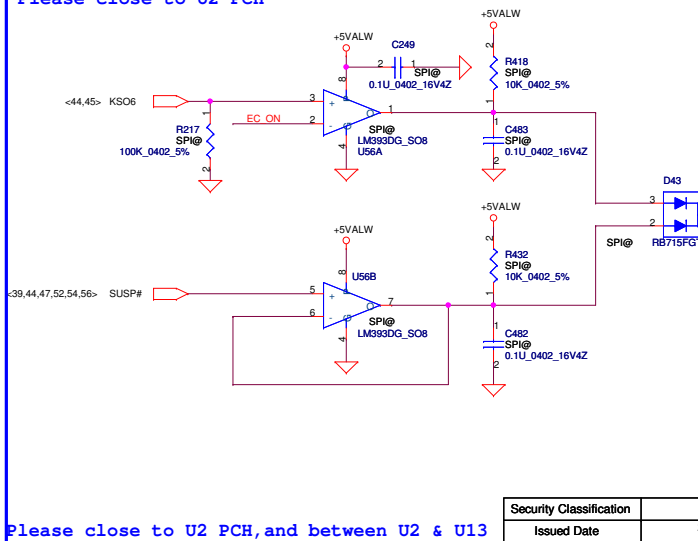
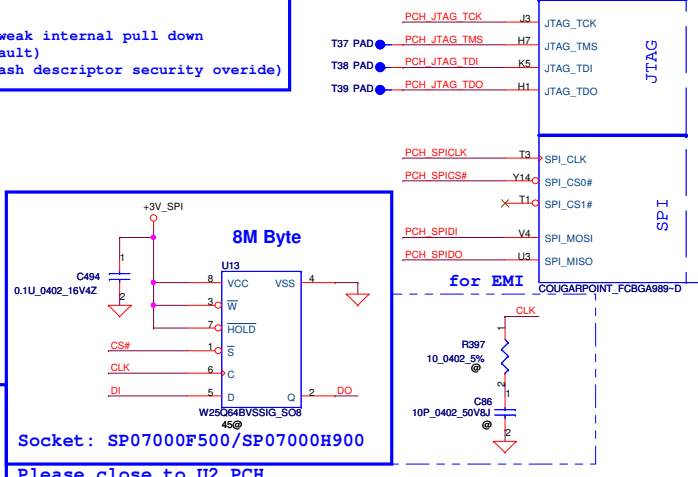
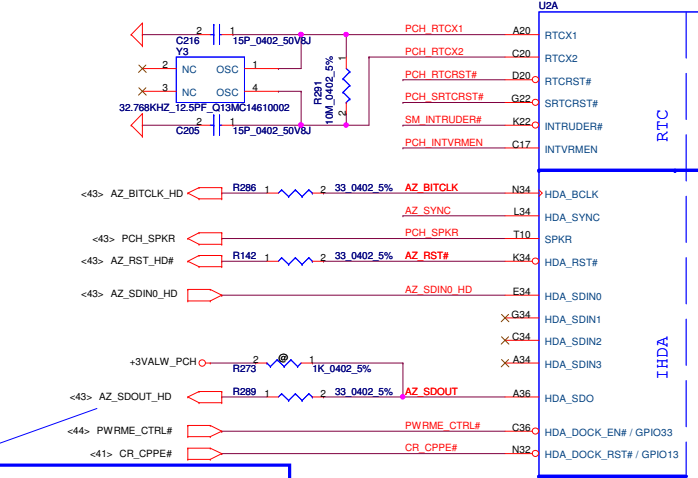
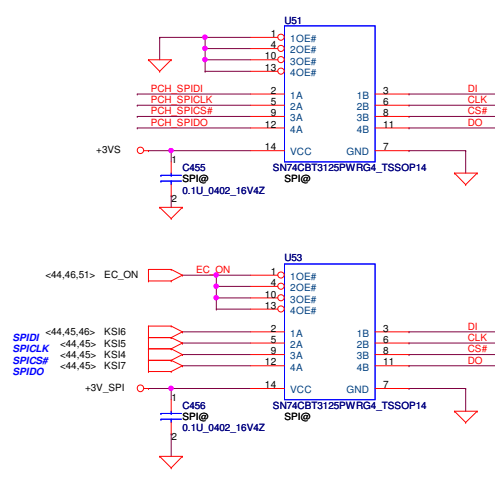
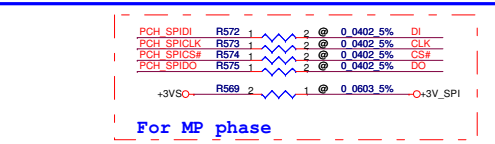
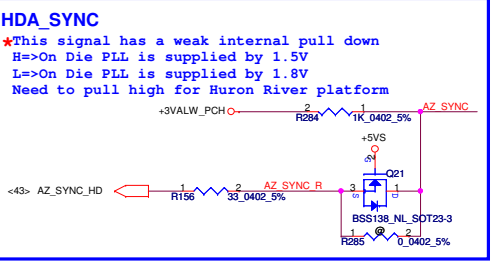
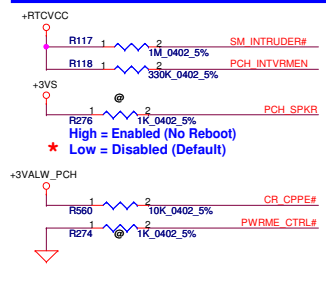


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				Size	Document Number	Rev
				PHQAA LA-6831P M/B 0.1		
Date: Monday, August 02, 2010				Sheet	27	of 58

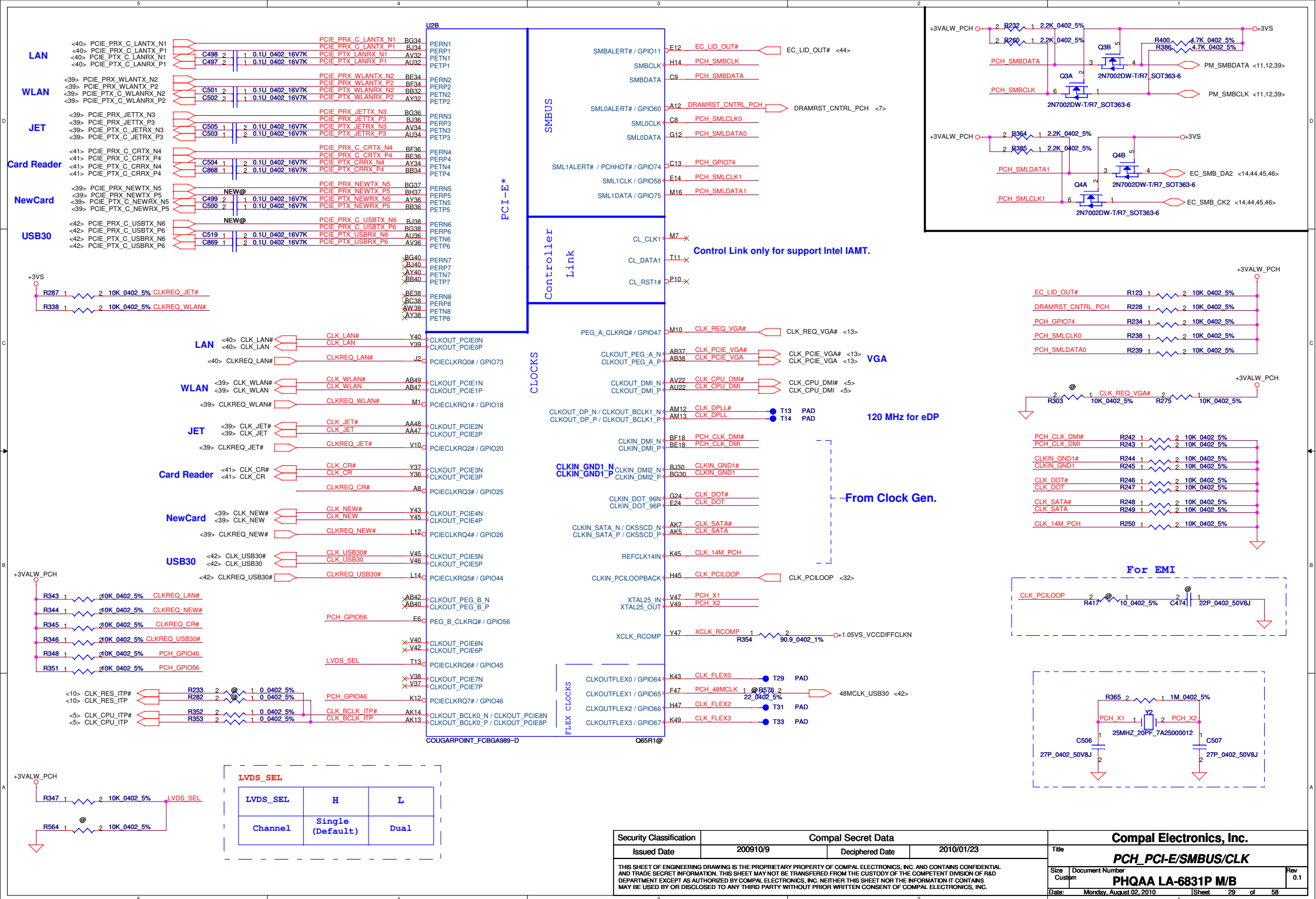


Integrated SUS 1.05V VRM Enable

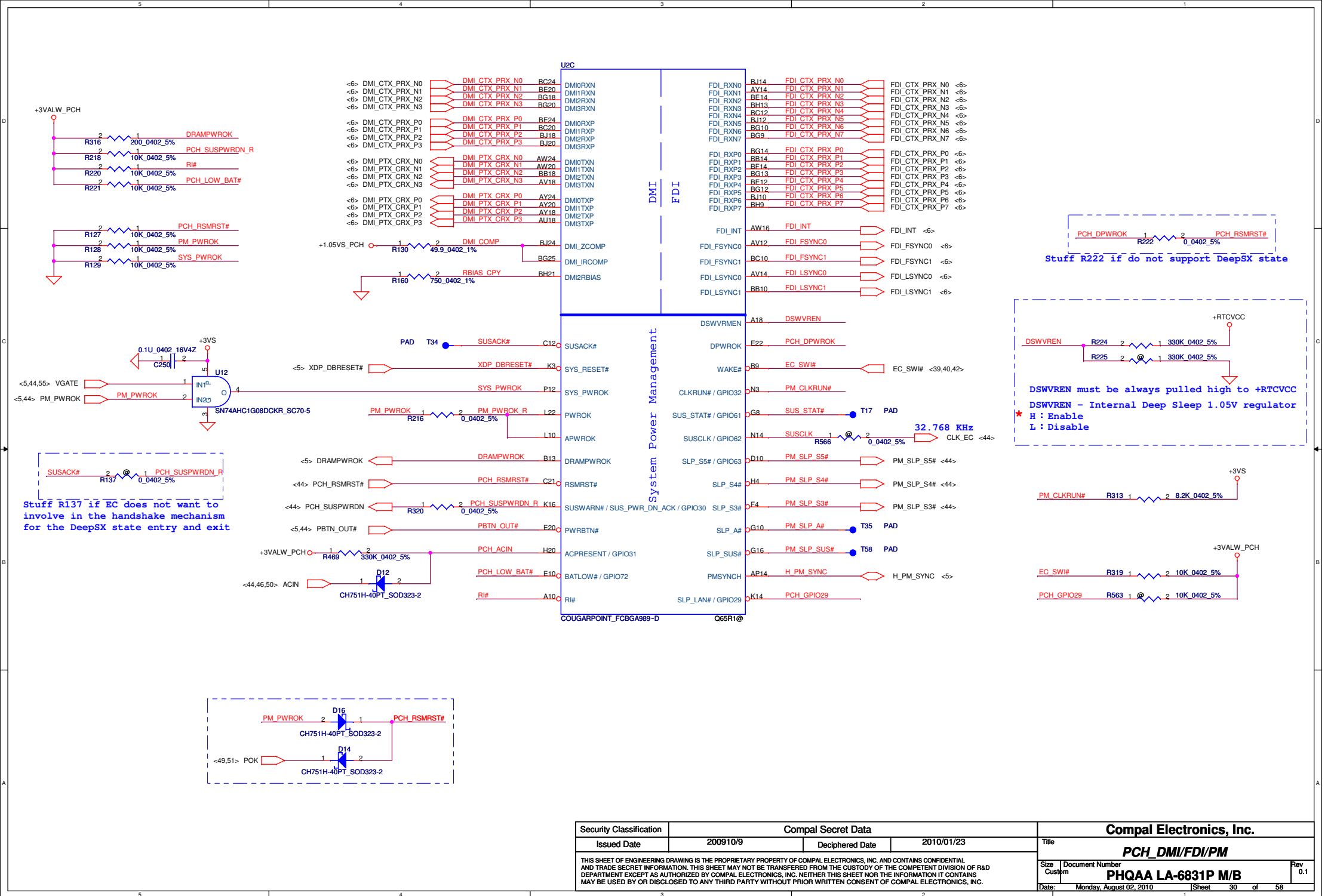
PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

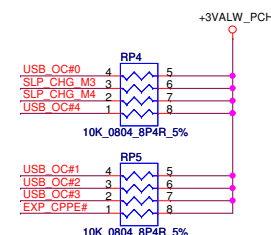
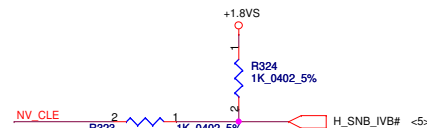
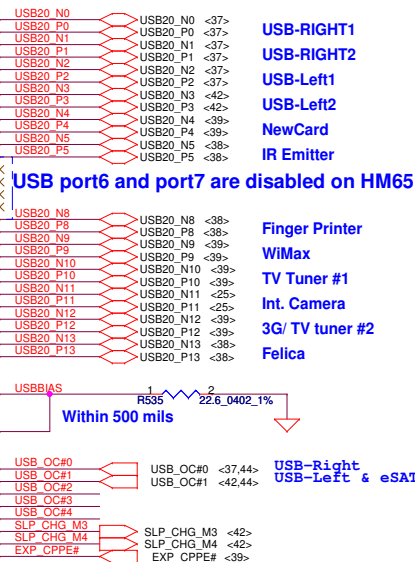
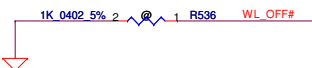
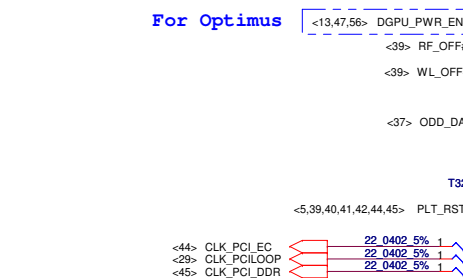


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				Custom	PHQAA LA-6831P M/B
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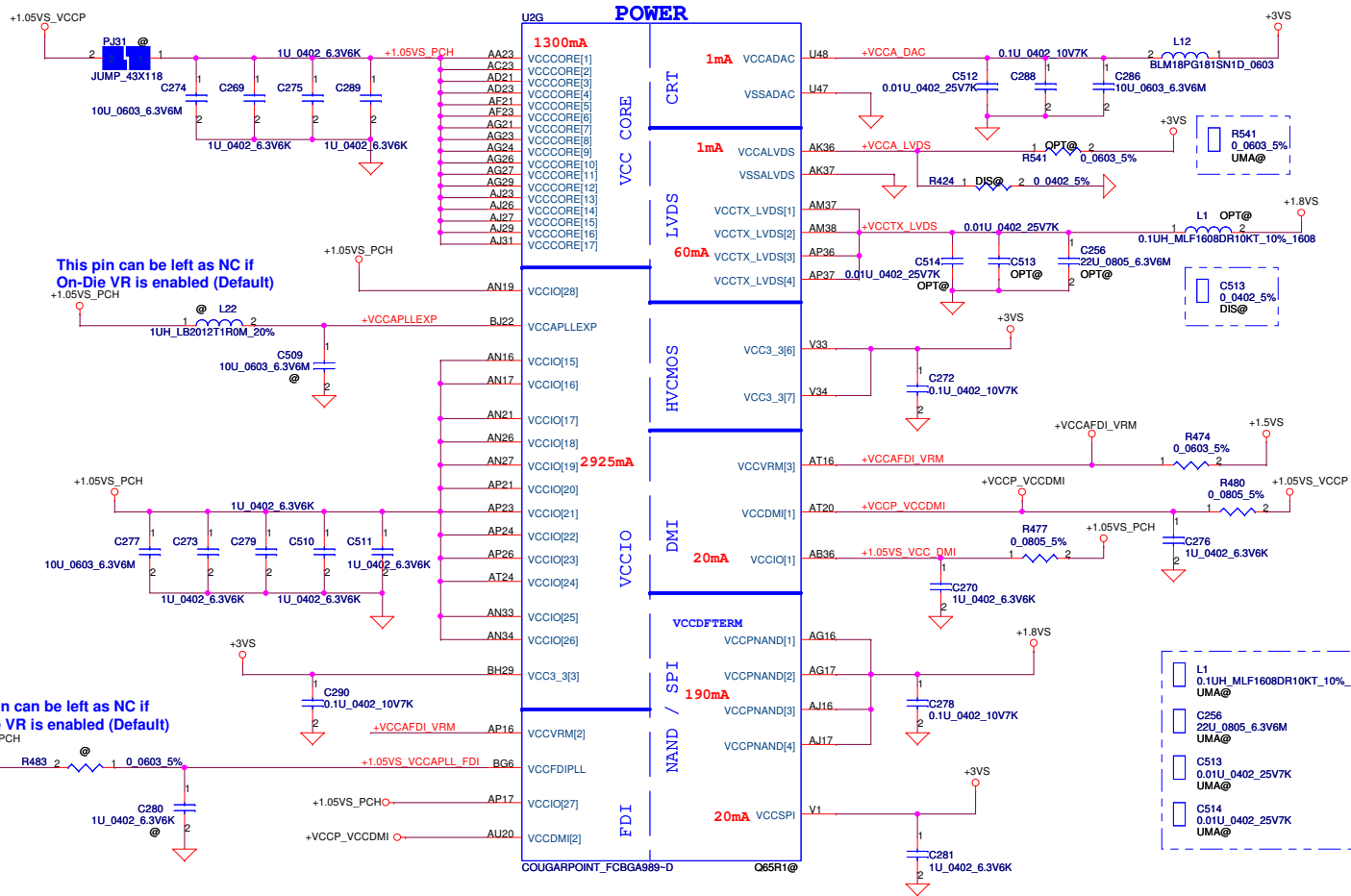
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title		
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				Size Document Number Custom PHQAA LA-6831P M/B		
				Date: Monday, August 02, 2010 Sheet 29 of 58 Rev 0.1		



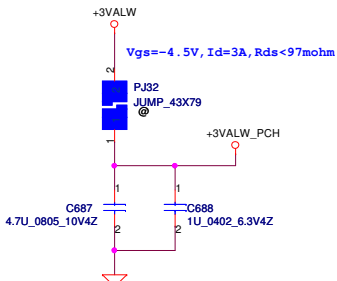


A16 Swap Override Strap	
WL_OFF#	★ Low= A16 swap override Enable High= A16 swap override Disable

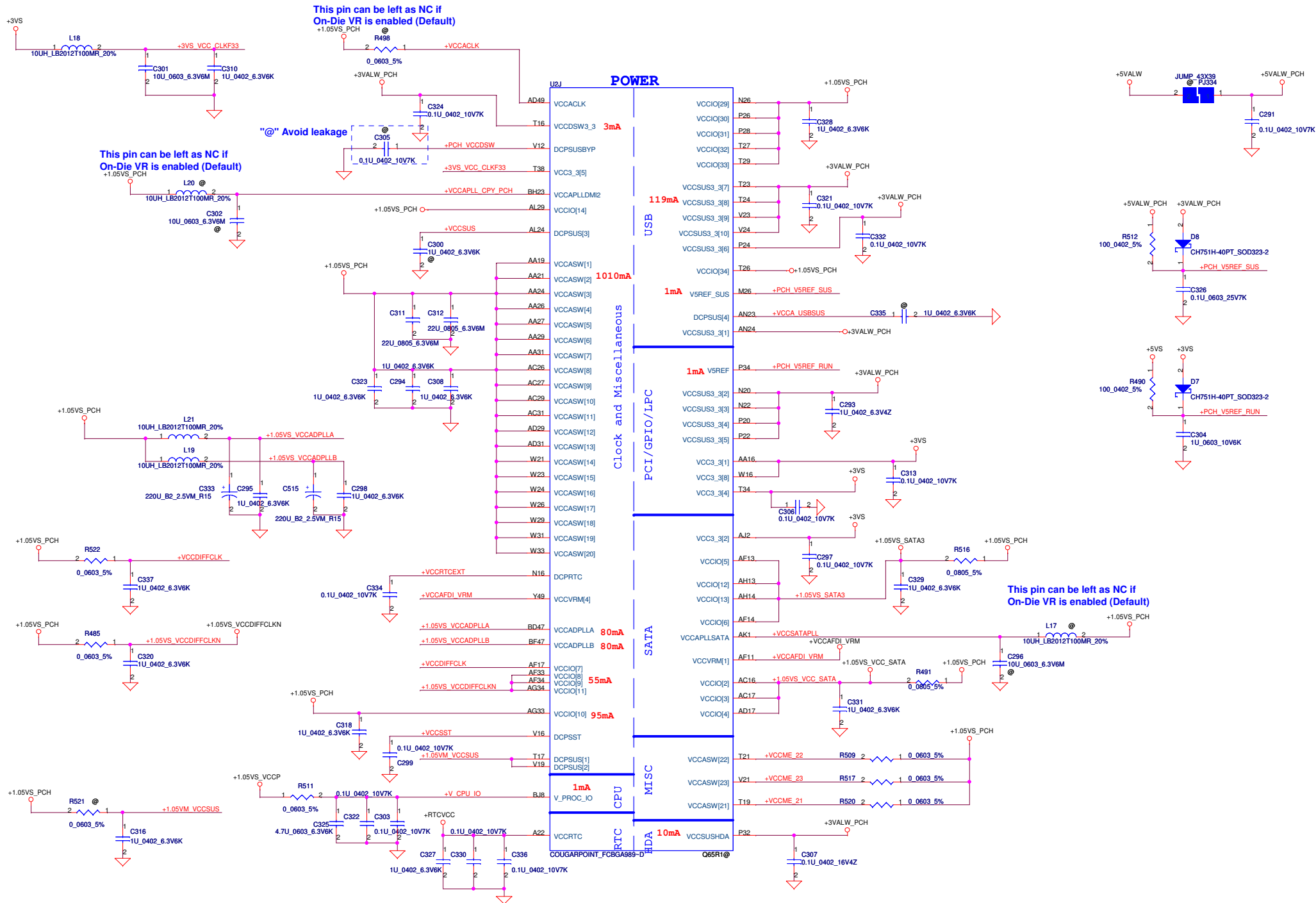
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Issued Date	200910/9	Deciphered Date	2010/01/23	Title	PCH_PCI/USB/NAND
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				Document Number	0.1
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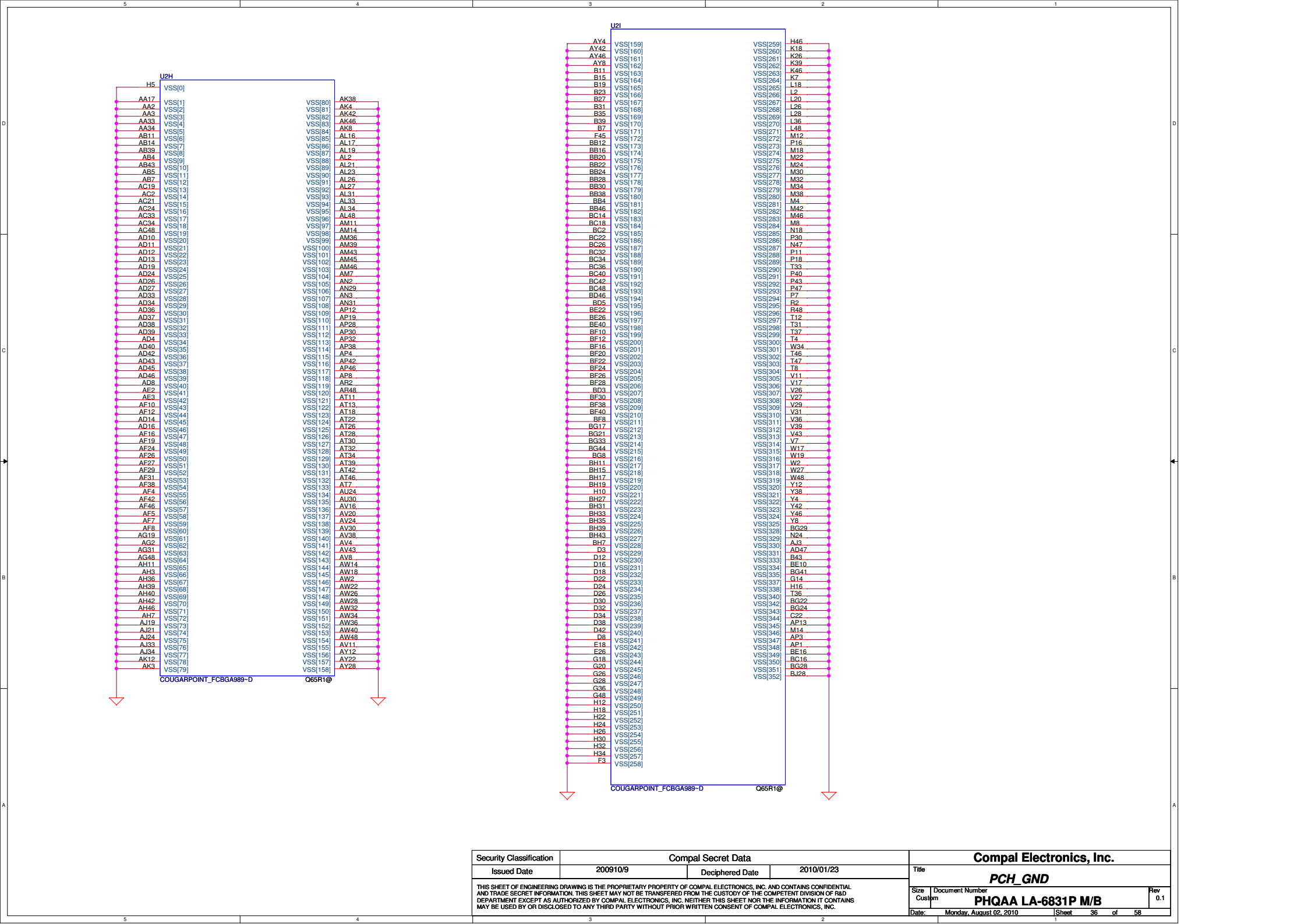
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



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				Custom	PHQAA LA-6831P M/B	0.1
				Date	Monday, August 02, 2010	Sheet 34 of 58

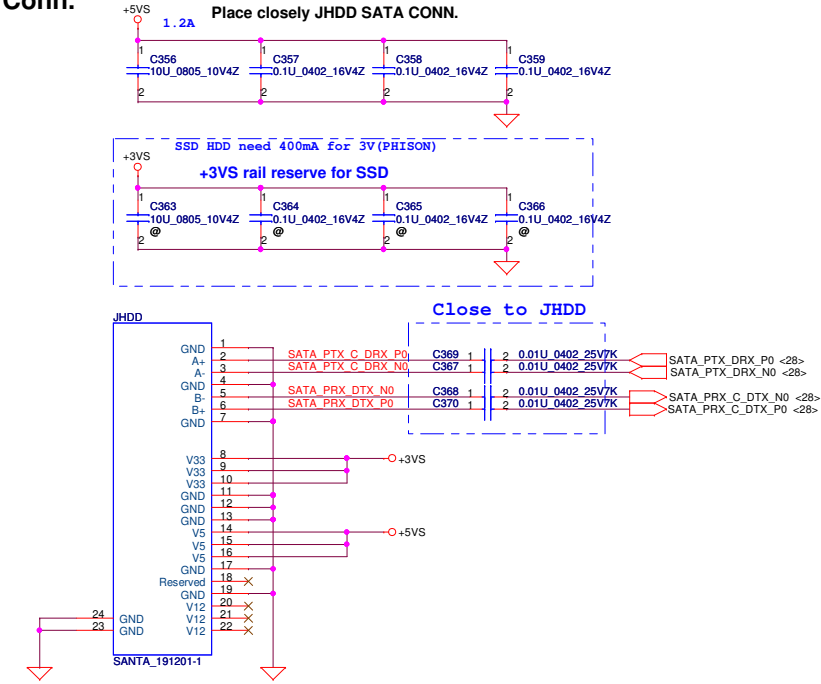


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Size	Document Number	Rev		Date	
Custom	PHQAA LA-6831P M/B	0.1		Monday, August 02, 2010	
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1		35		58	

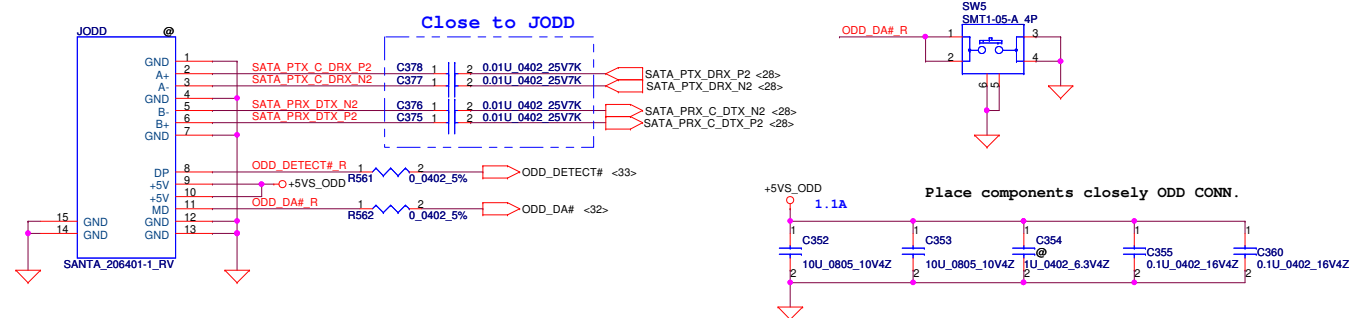


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Size		Document Number		Rev	
Custom		PHQAA LA-6831P M/B		0.1	
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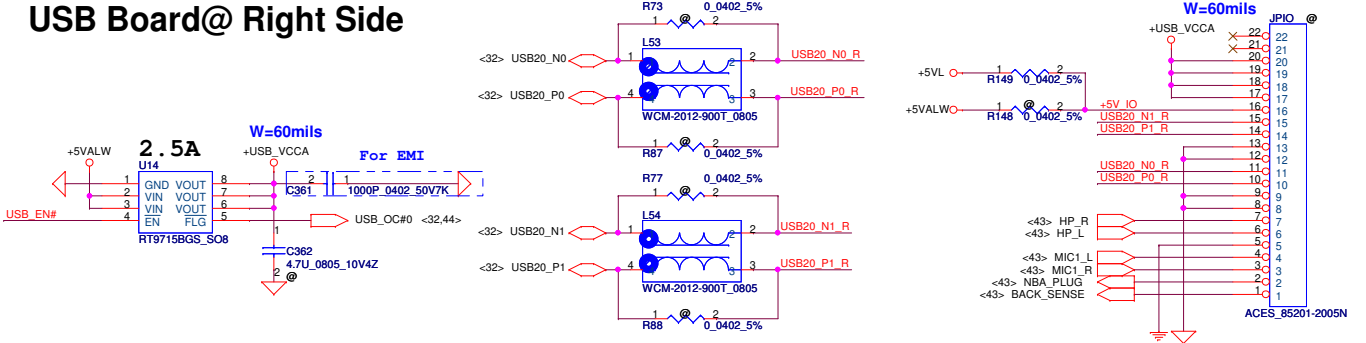
SATA HDD Conn.



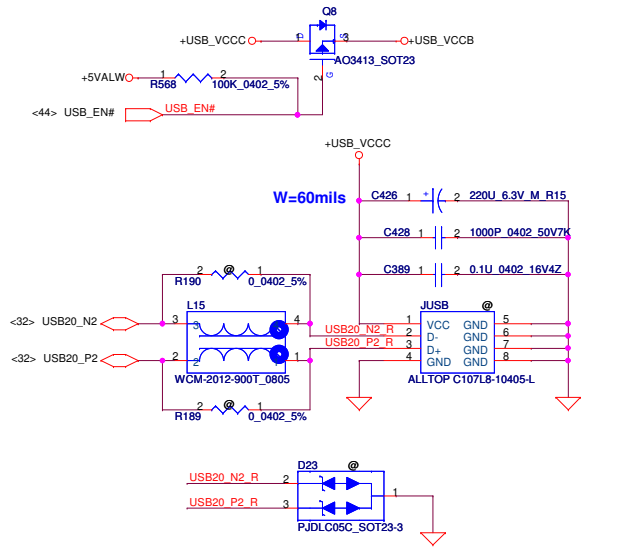
SATA ODD Conn



USB Board@ Right Side

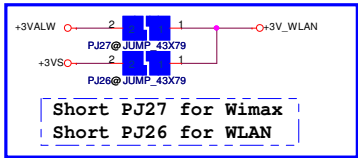


USB Board@ Left Side



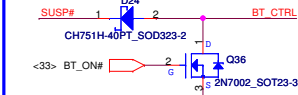
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Issued Date	200910/9	Deciphered Date	2010/01/23	SATA-HDD/ODD/USB	
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Slot 1 Half PCIe Mini Card-WLAN/ WiMax



	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

**If +3V_WLAN is +3VS, please remove D24



For isolate Intel Rainbow Peak and Compal Debug Card.

WLAN WIFI

WiMax

LED WIMAX#

WIMAX#

FOX_AS08226-S40N-7F

3VALW_CARD

Imax = 0.275A

3VS_CARD

Imax = 1.35A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

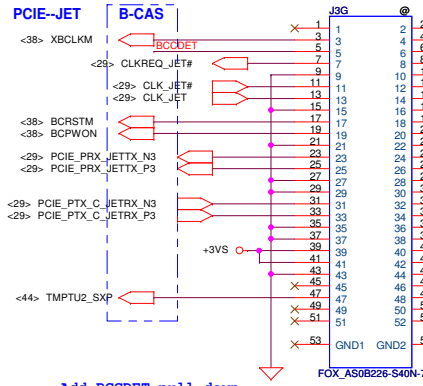
Imax = 0.75A

3VS_CARD

Imax = 0.75A

1.5VS_CARD

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET



Add BCCDET pull down

BCCDET

R307

470_0402_5%

FOX_AS08226-S40N-7F

3VALW_CARD

Imax = 0.275A

3VS_CARD

Imax = 1.35A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

3VS_CARD

Imax = 0.75A

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Imax = 0.75A

3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

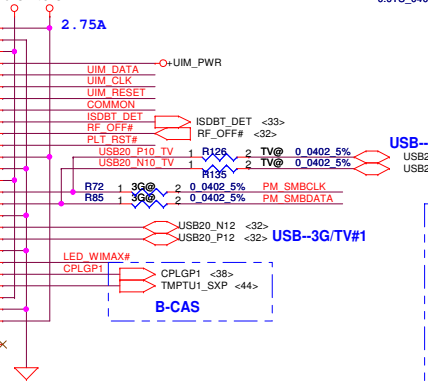
3VS_CARD

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Imax = 0.75A

3VALW_CARD



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BCCDET

R307

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1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

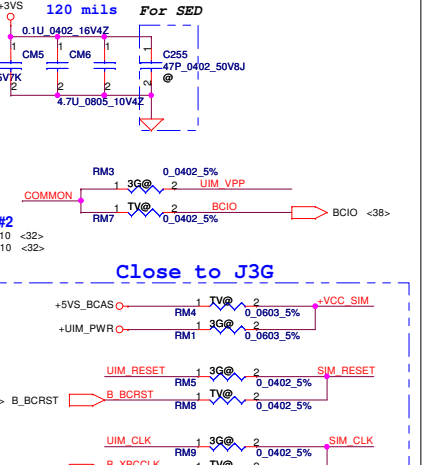
3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD



Add BCCDET pull down

BCCDET

R307

470_0402_5%

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Imax = 0.75A

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Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

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Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

3VALW_CARD

Imax = 0.75A

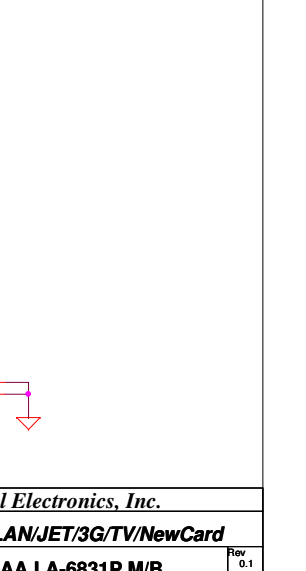
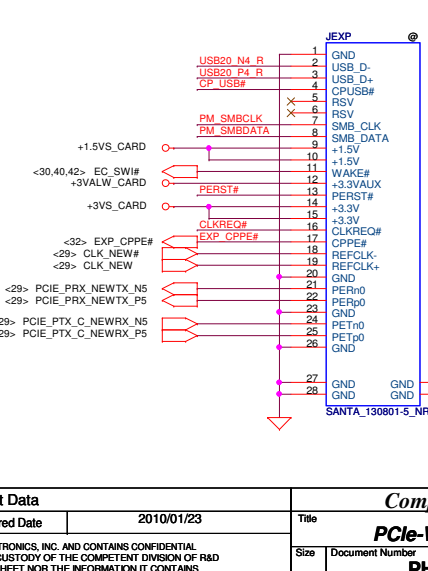
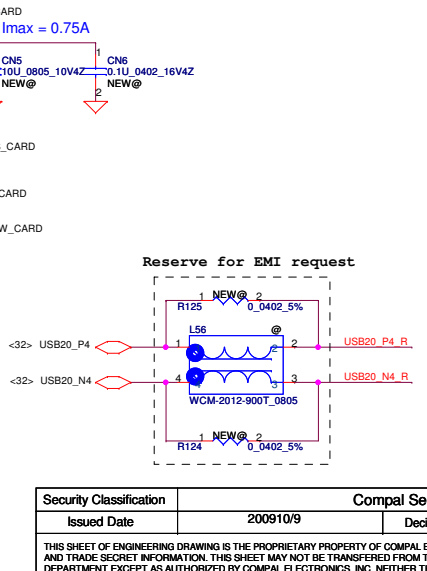
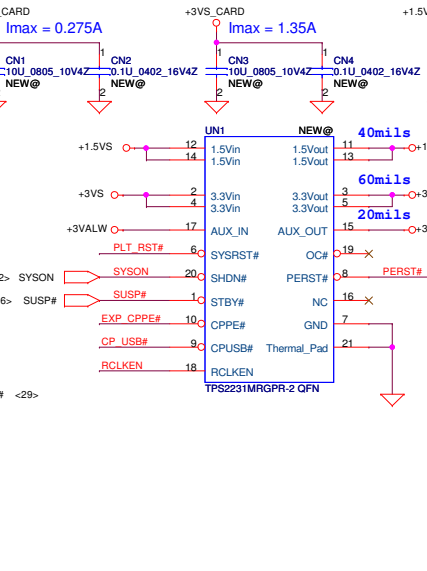
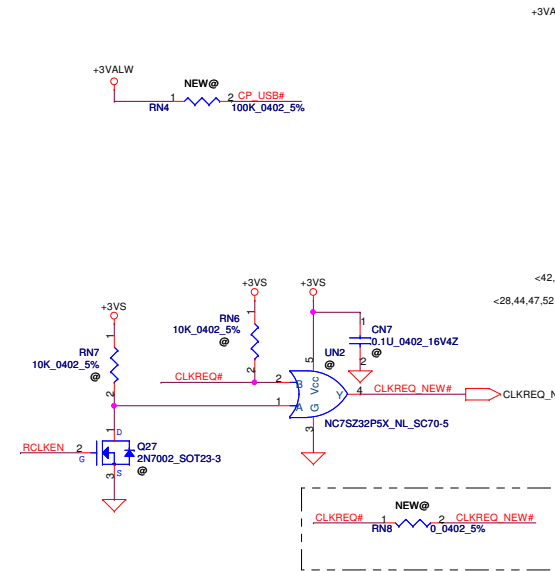
3VS_CARD

Imax = 0.75A

1.5VS_CARD

Imax = 0.75A

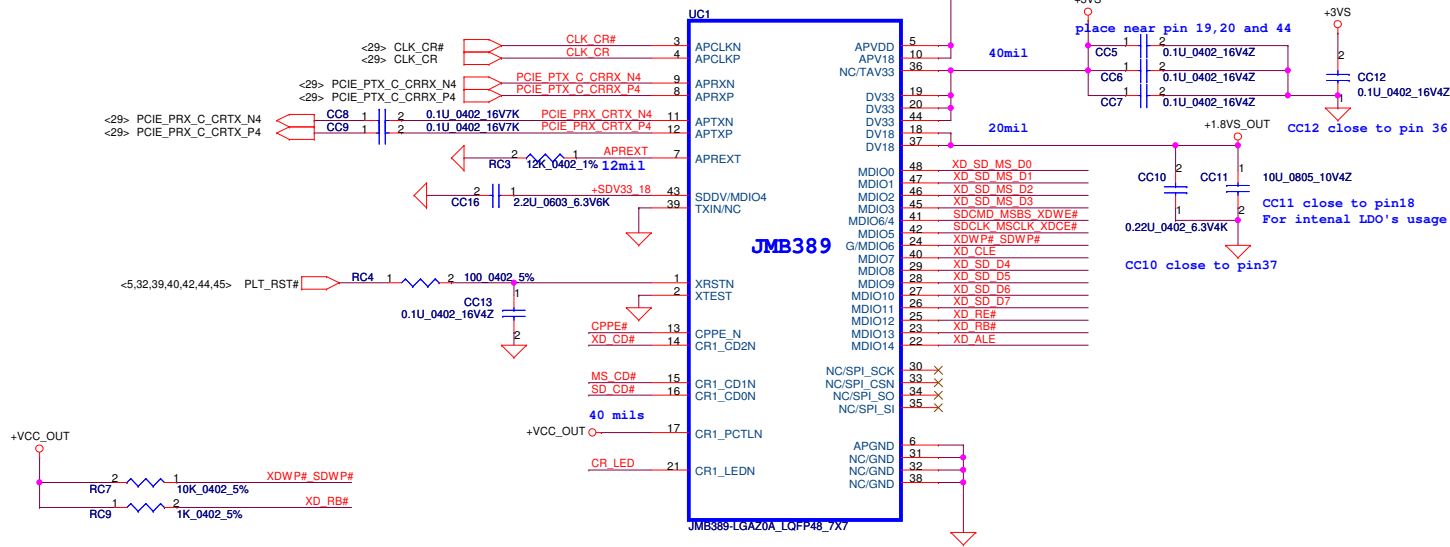
3VALW_CARD



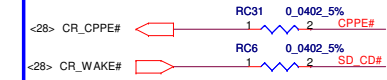
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CC16 close to pin43
For internal LDO in SD3.0

JMB389C

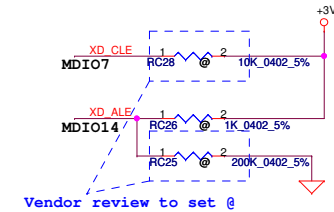


D3E mode

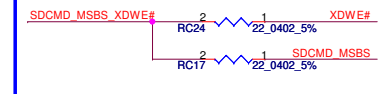


Power On Strapping setting

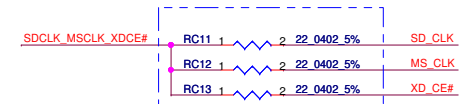
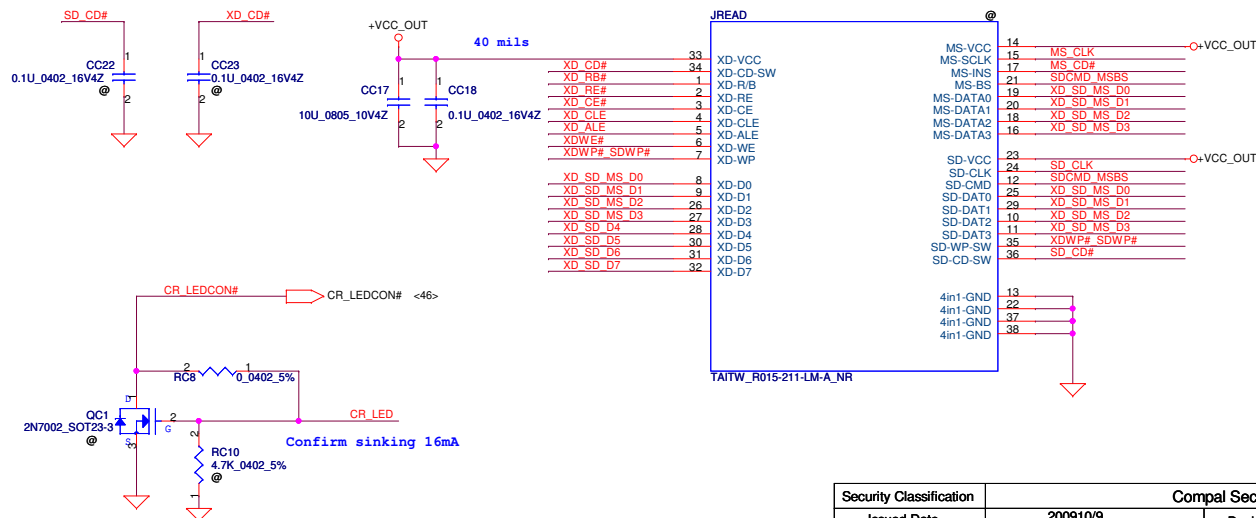
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★



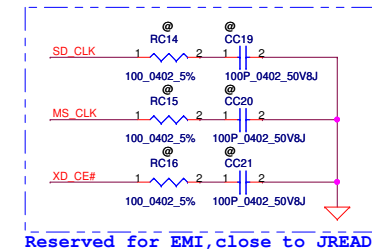
Add RC24 and RC17 close to UC1 for xD issue



5 in 1 Card Reader

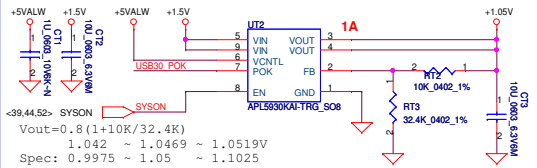


Reserved for EMI,close to UC1.42



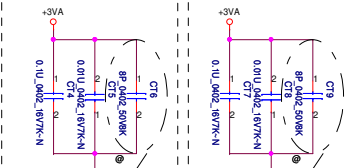
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Compal Electronics, Inc.				PCle-CardReader JMB389
Size Custom				Document Number PHQAA LA-6831P M/B
Date: Monday, August 02, 2010				Sheet 41 of 58

+1.5V to +1.05V Transfer

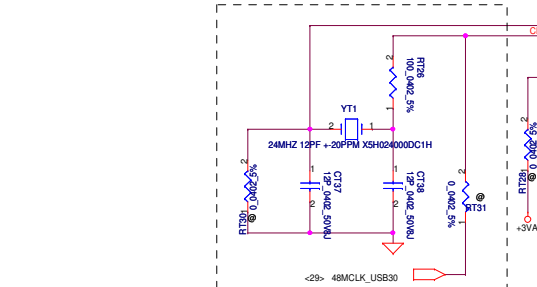
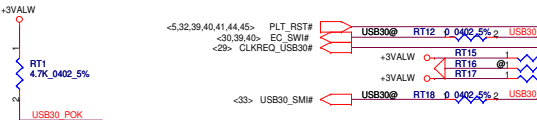
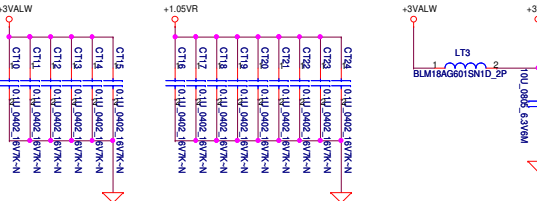


Close to U102.D7

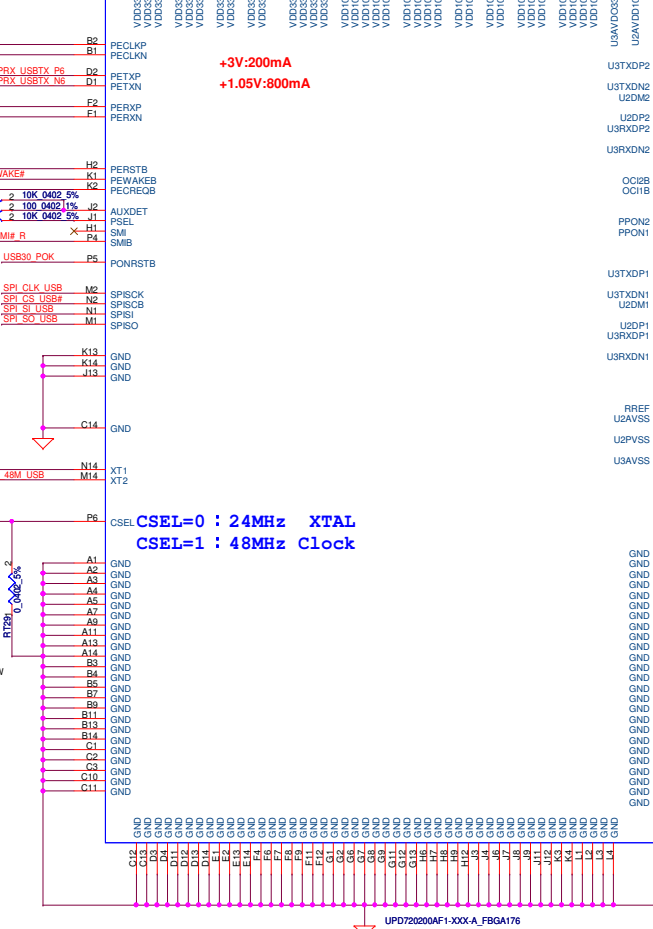
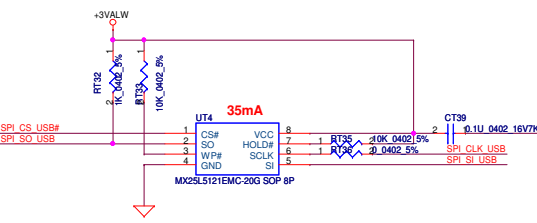
Close to U102.P13



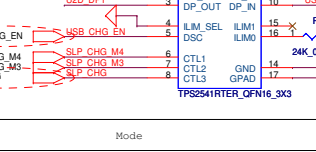
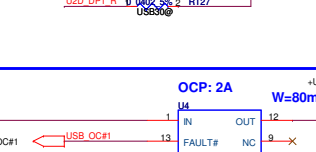
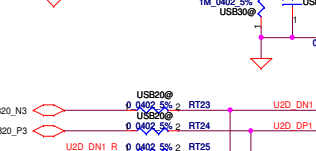
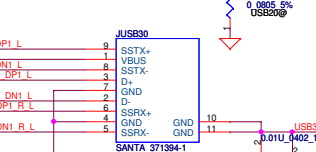
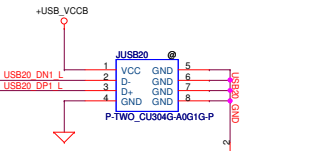
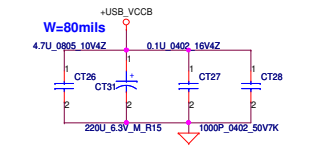
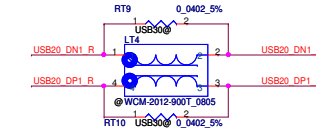
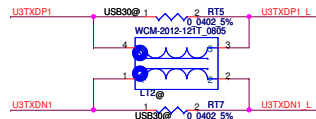
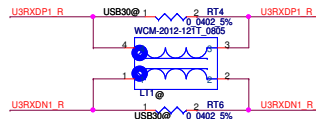
Follow Vendor recommend.



Place as close as possible to U102.N14 and U102.M14

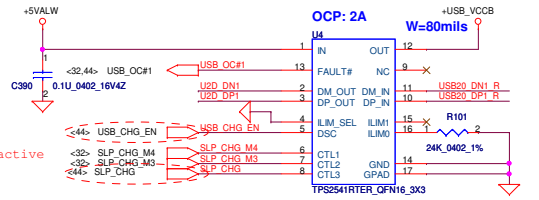


Close to U137.6

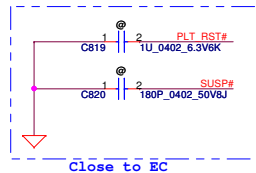
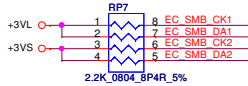
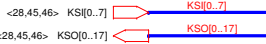
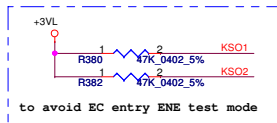
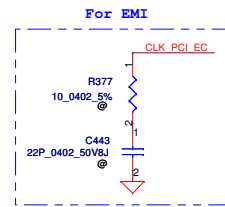


USB Sleep & Charge Auto-Mode

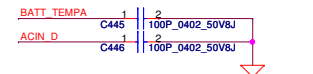
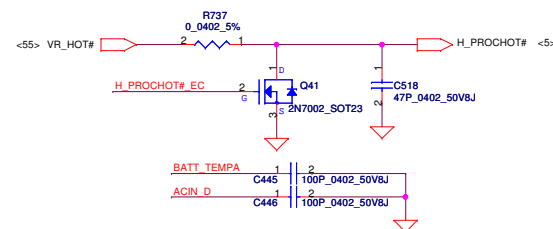
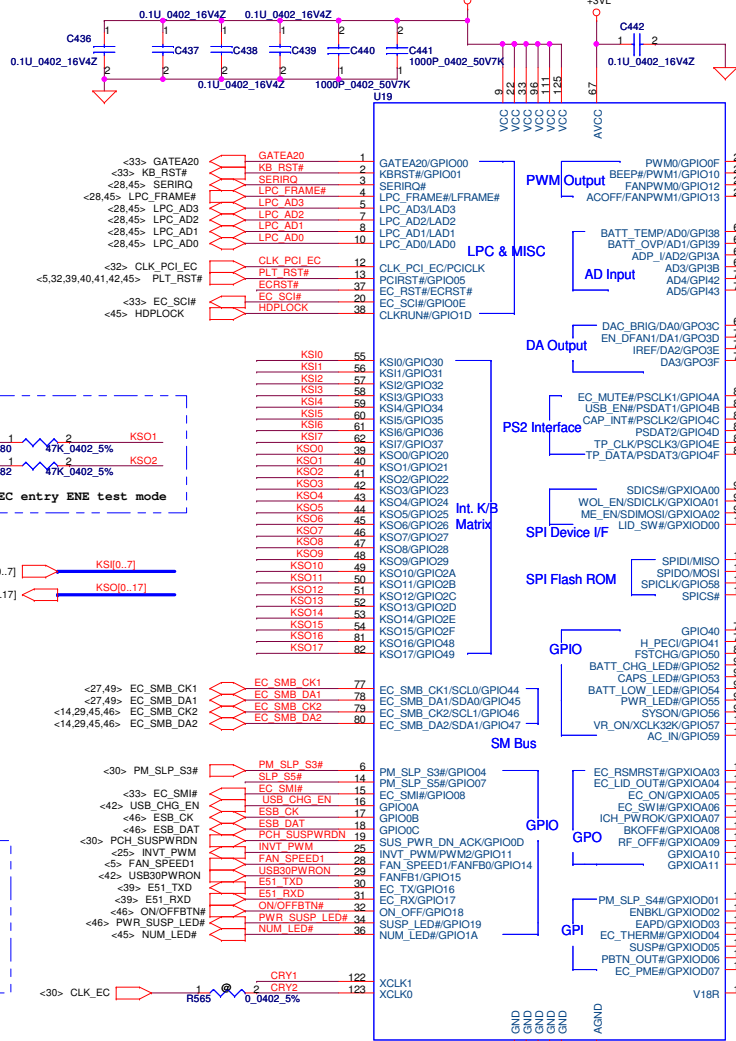
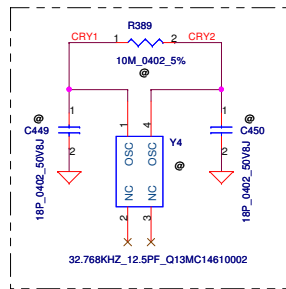
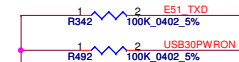
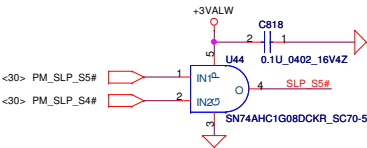
07/08/2010
Need EC to set these signals to high active
SLP_CHG, USB_CHG_EN



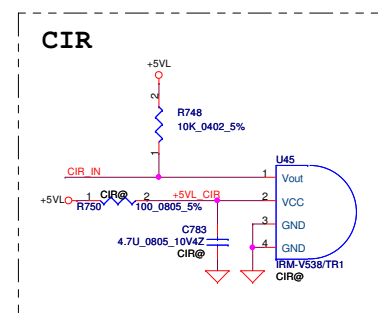
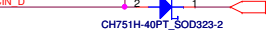
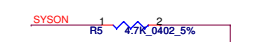
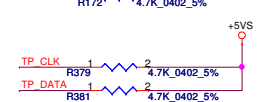
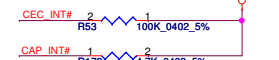
SLP_CHG_M4	SLP_CHG_M3	SLP_CHG	Mode
0	0	X(1)	Dedicated Charging Port, Auto-detect
0	1	X(1)	Dedicated Charging Port, BC Specification 1.1 Only (Mode 3)
1	0	X(1)	Dedicated Charging Port, Apple Only (Mode 4)
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1



Close to EC

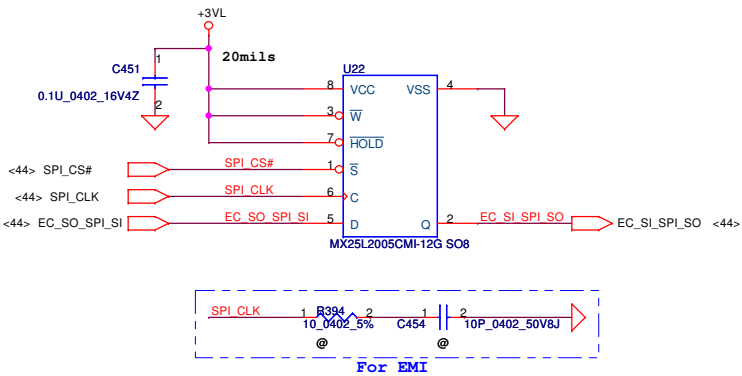


TV tuner temperature

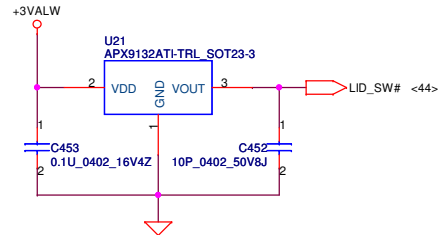


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32.768KHZ_12.5PF_Q13MC14610002		PHQAA LA-6831P M/B		44	0.1
Monday, August 02, 2010		Sheet		44	of 58

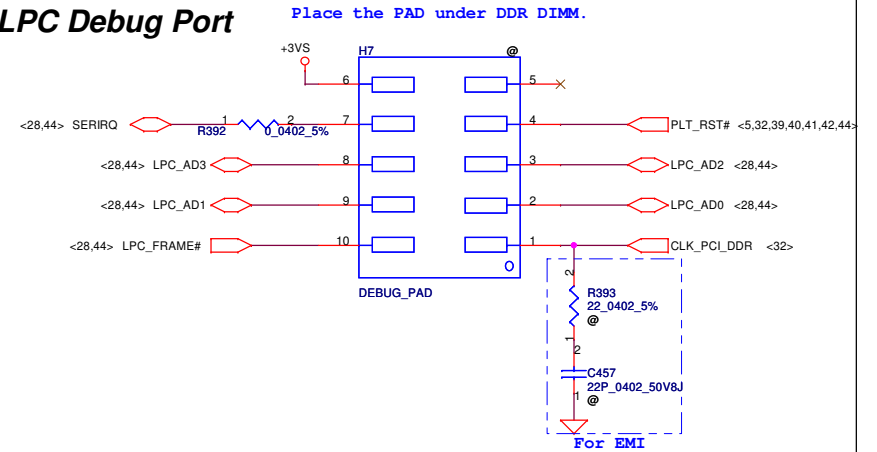
SPI Flash (256KB)



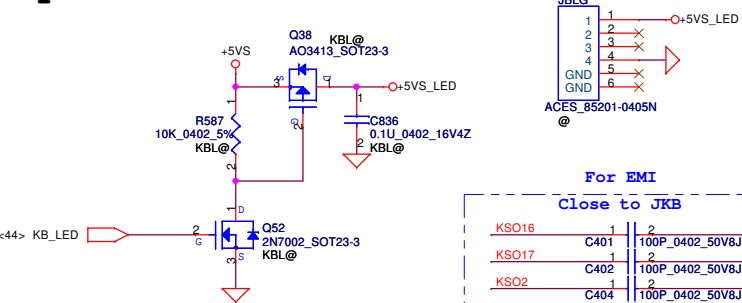
Lid SW



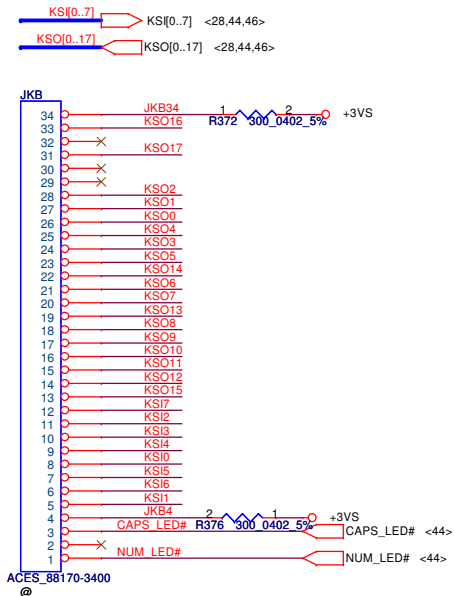
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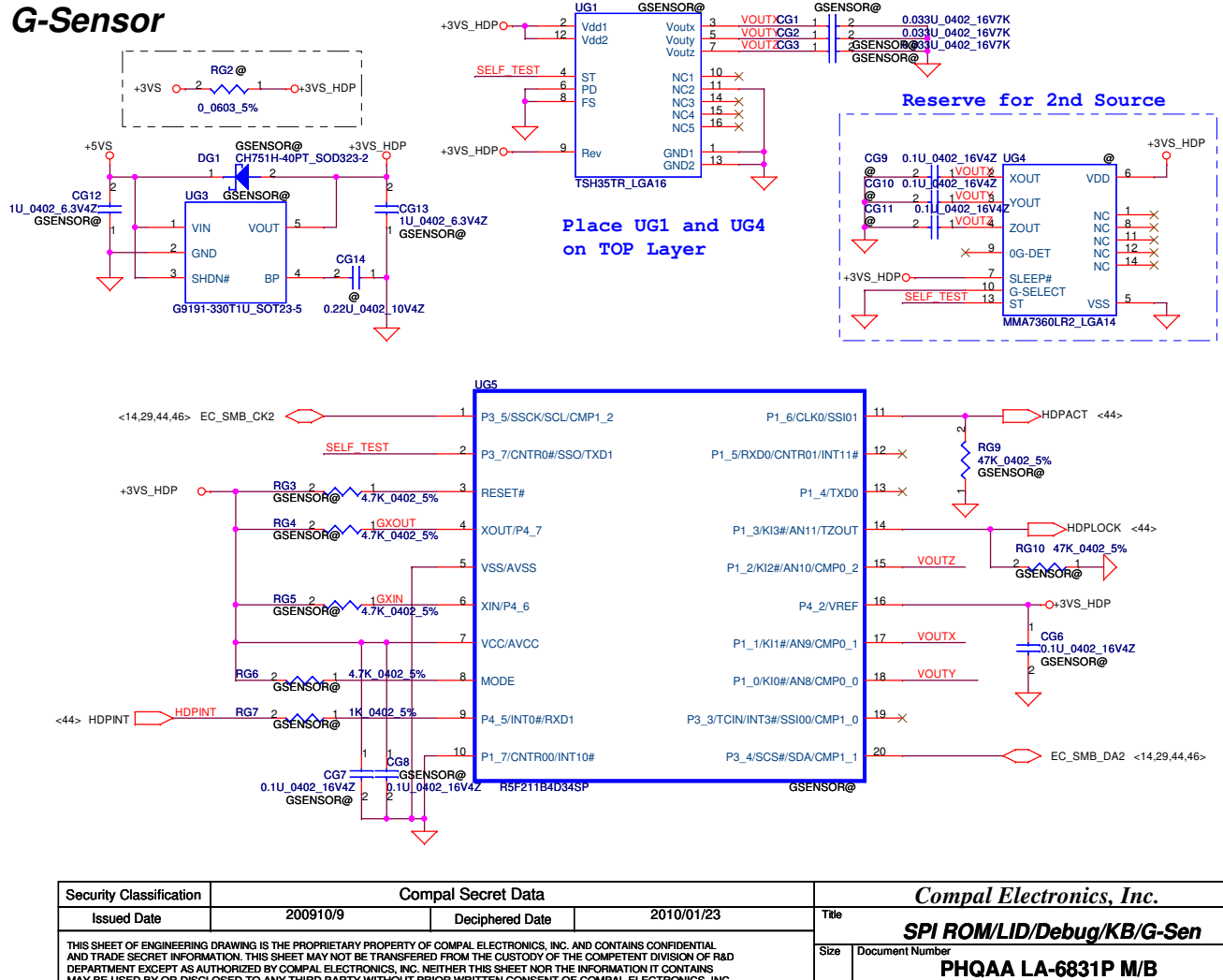
Keyboard LED



KEYBOARD CONN.

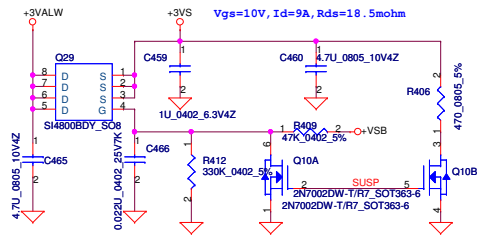


G-Sensor

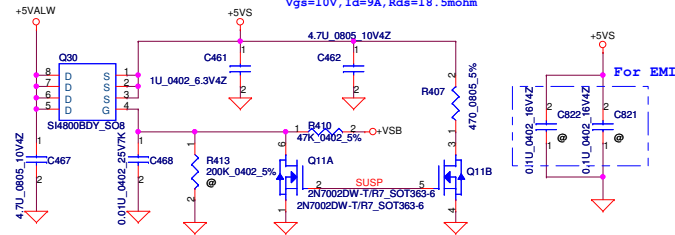


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Size	Document Number	PHQAA LA-6831P M/B		Rev
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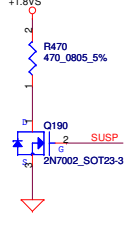
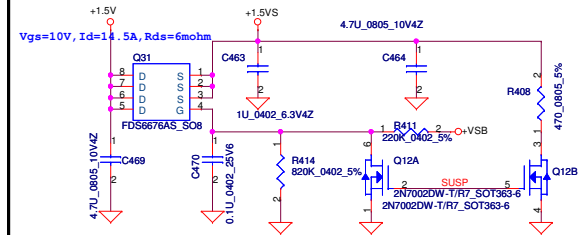
+3VALW TO +3VS



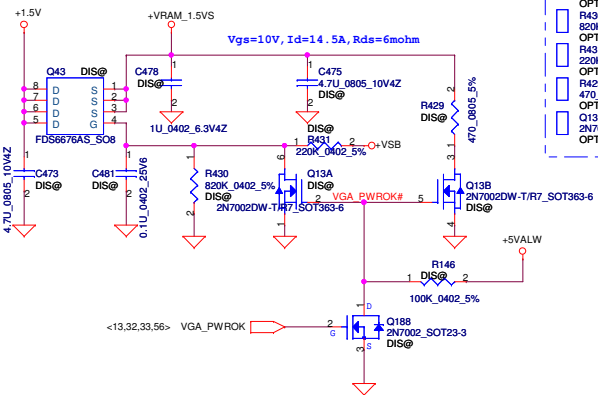
+5VALW TO +5VS



+1.5V to +1.5VS

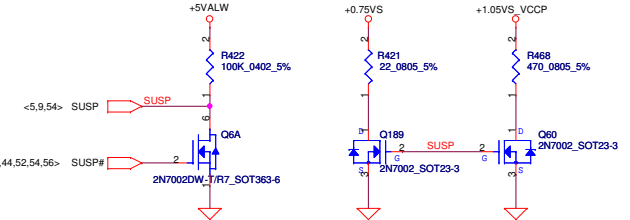
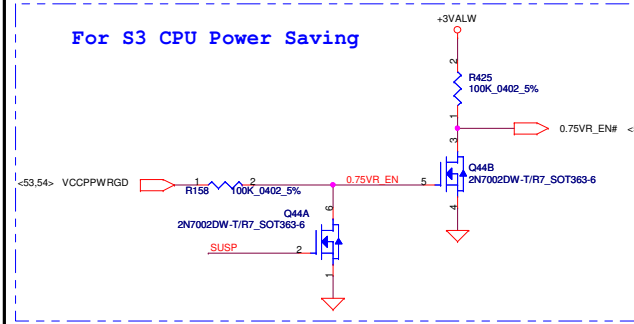


+1.5V to +VRAM_1.5VS

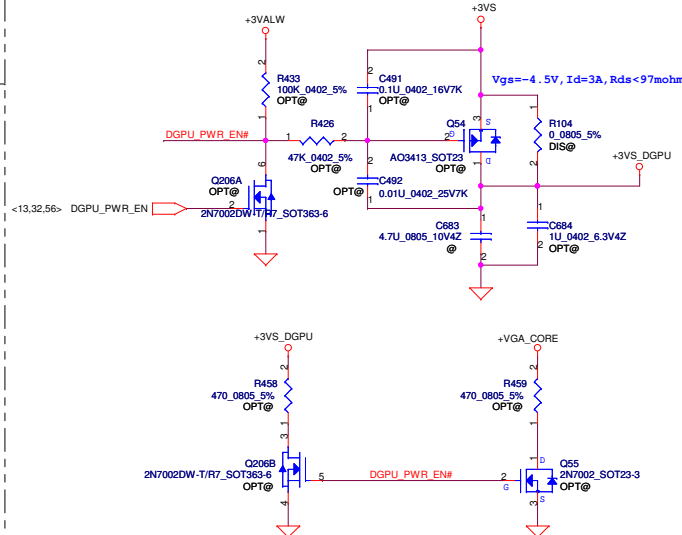


Q43	FDS6676AS_S08	C473	4.7U_0805_10V4Z
Q481	OPT@	C479	1U_0402_6.3V4Z
Q481	OPT@	C475	4.7U_0805_10V4Z
R430	820K_0402_5%	C475	4.7U_0805_10V4Z
R431	220K_0402_5%	R146	100K_0402_5%
R429	470_0805_5%	Q188	2N7002_SOT23-3
Q13	2N7002DW-T/R7_SOT363-6	Q188	2N7002_SOT23-3
Q13	2N7002DW-T/R7_SOT363-6	Q188	2N7002_SOT23-3

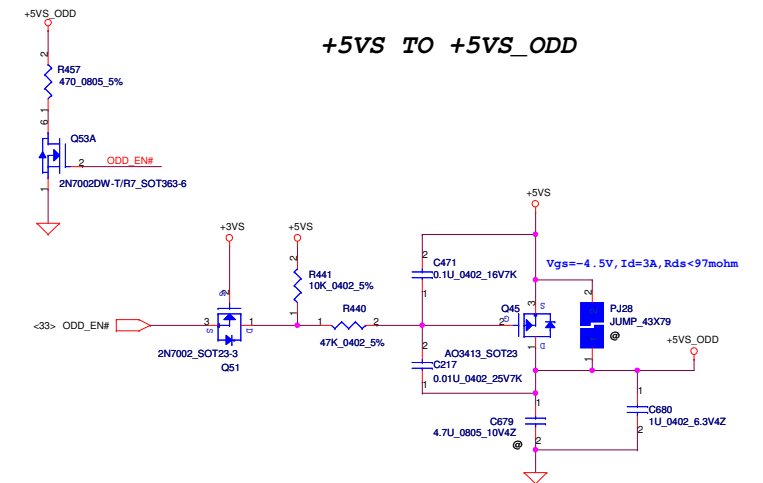
For S3 CPU Power Saving



+3VS to +3VS_DGPU

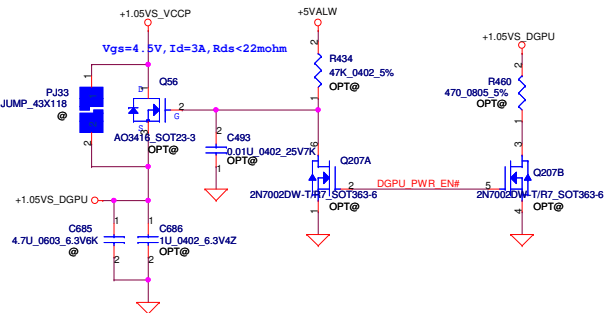


+5VS TO +5VS_ODD



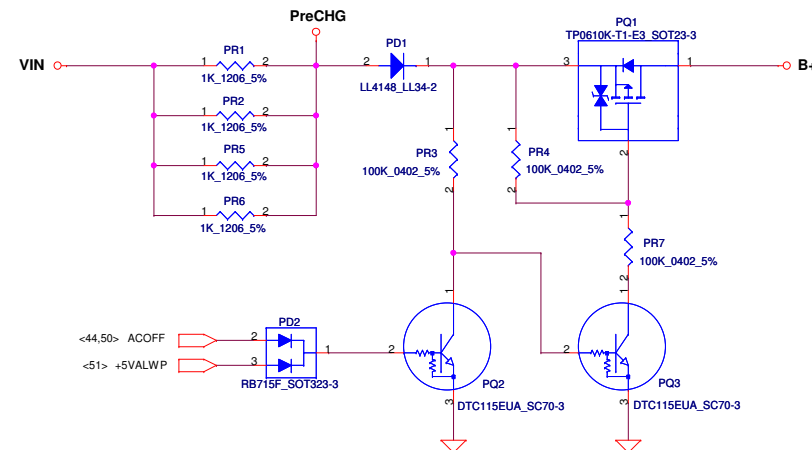
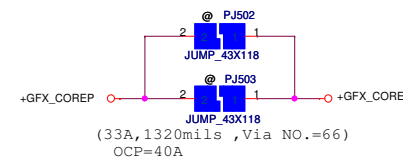
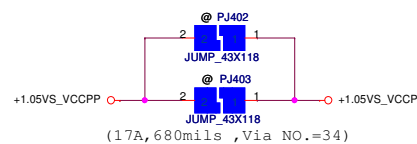
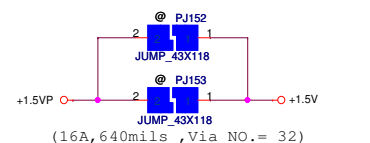
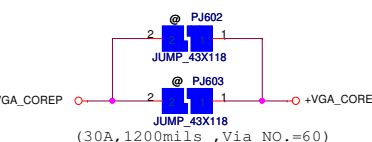
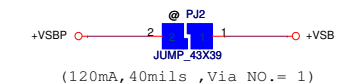
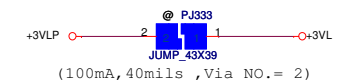
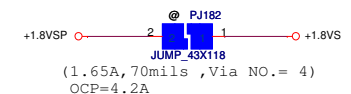
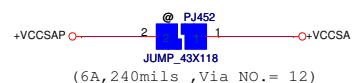
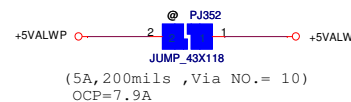
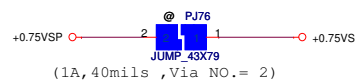
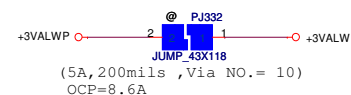
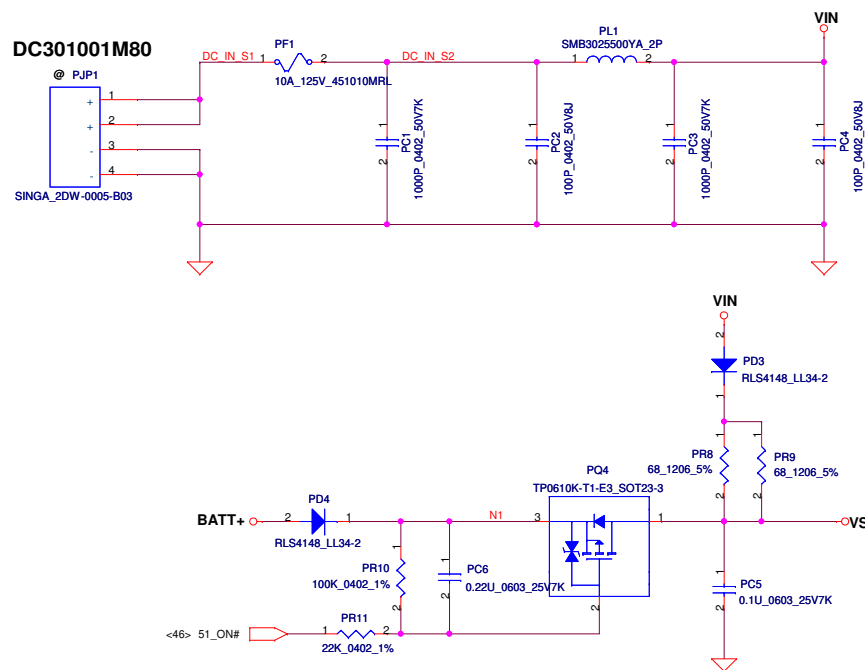
+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs

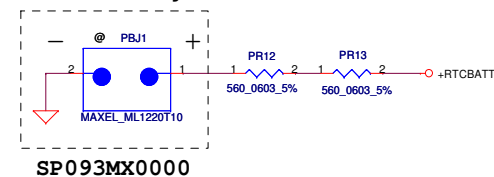


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Title			
DC-DC INTERFACE			
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DC301001M80



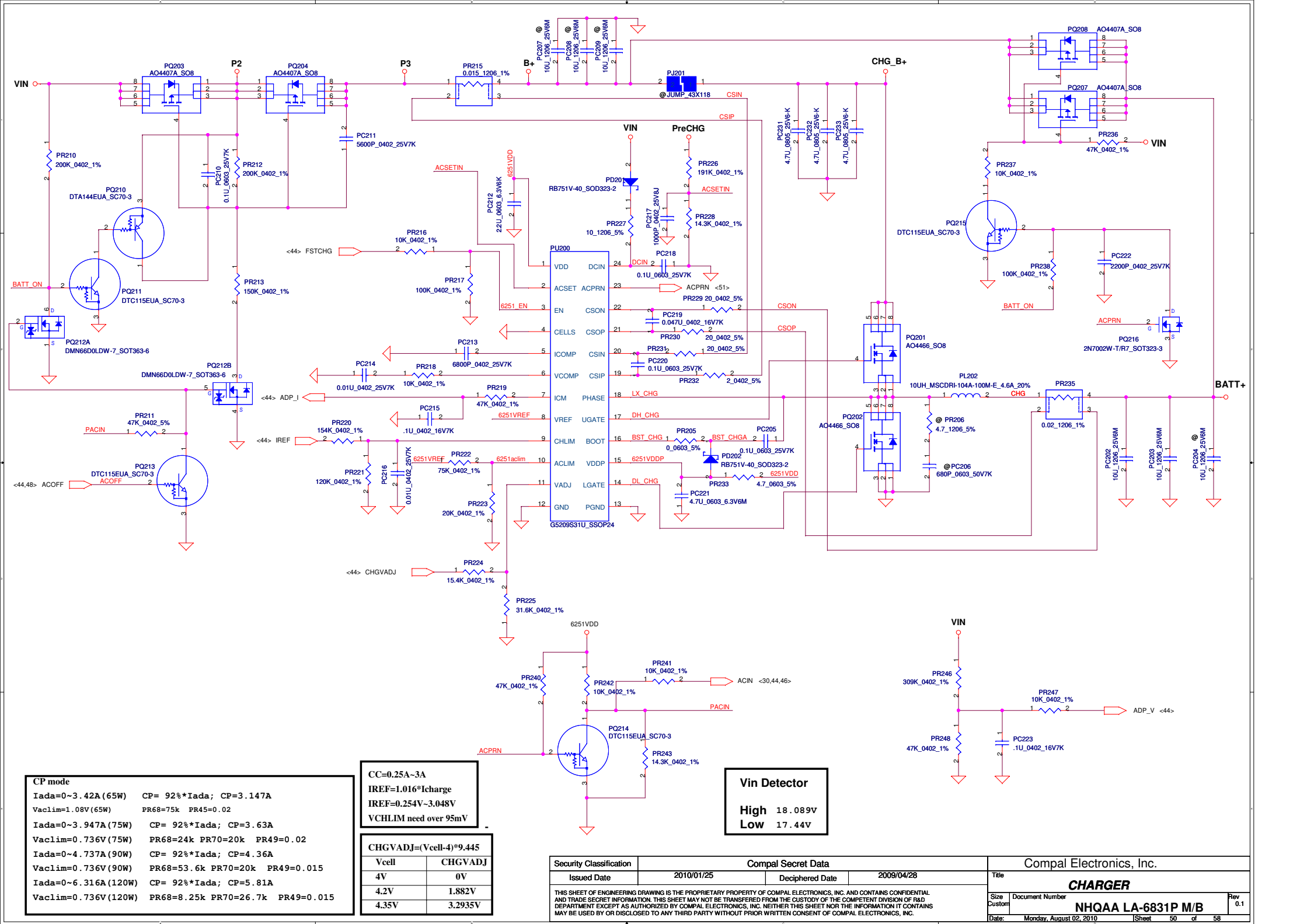
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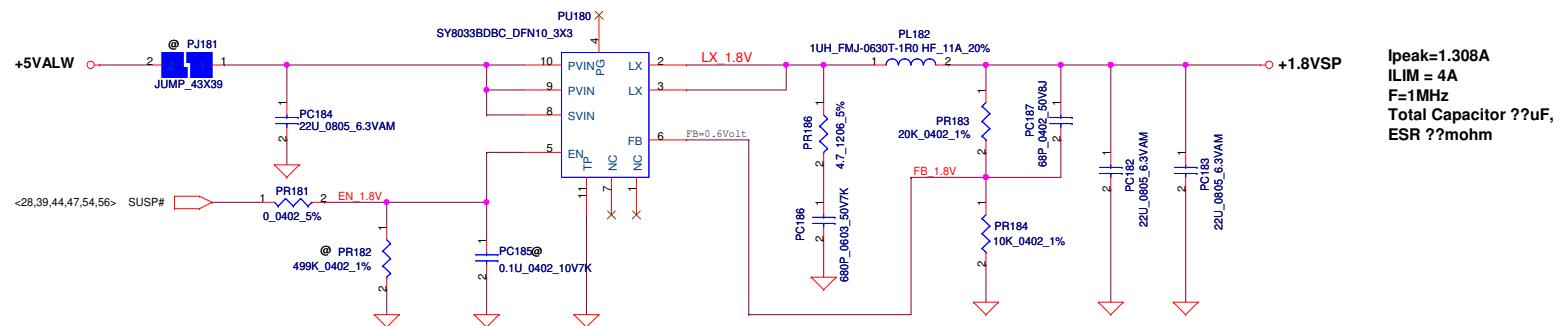
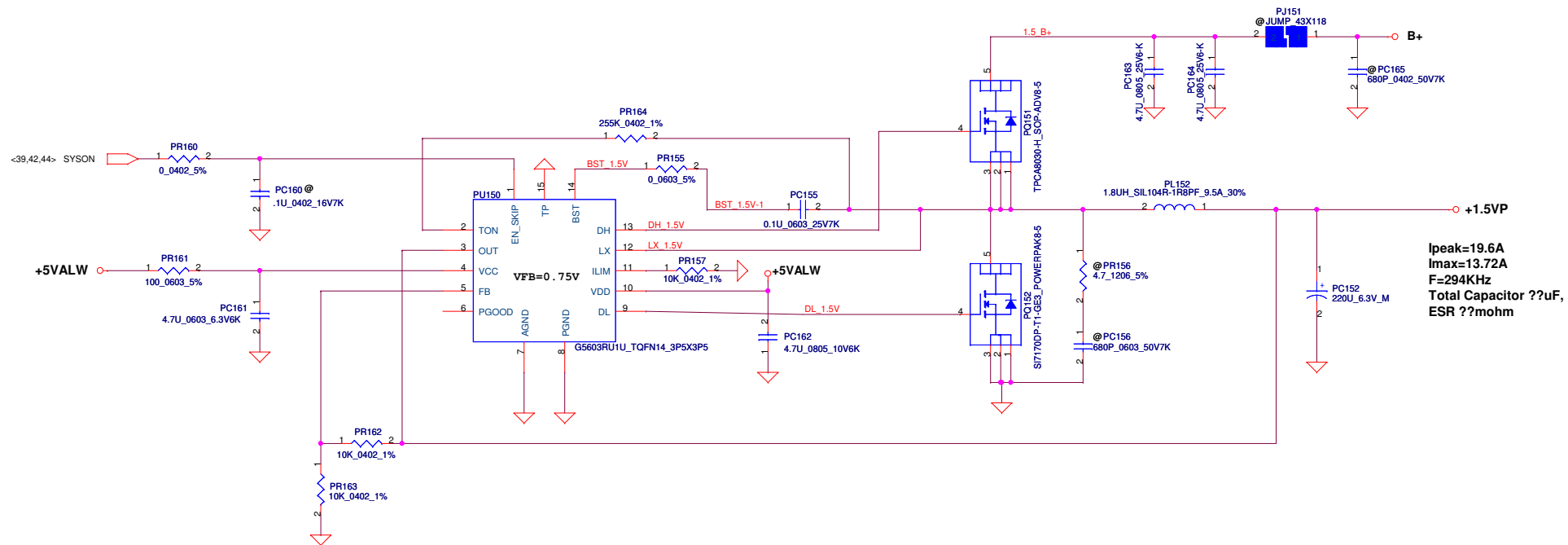


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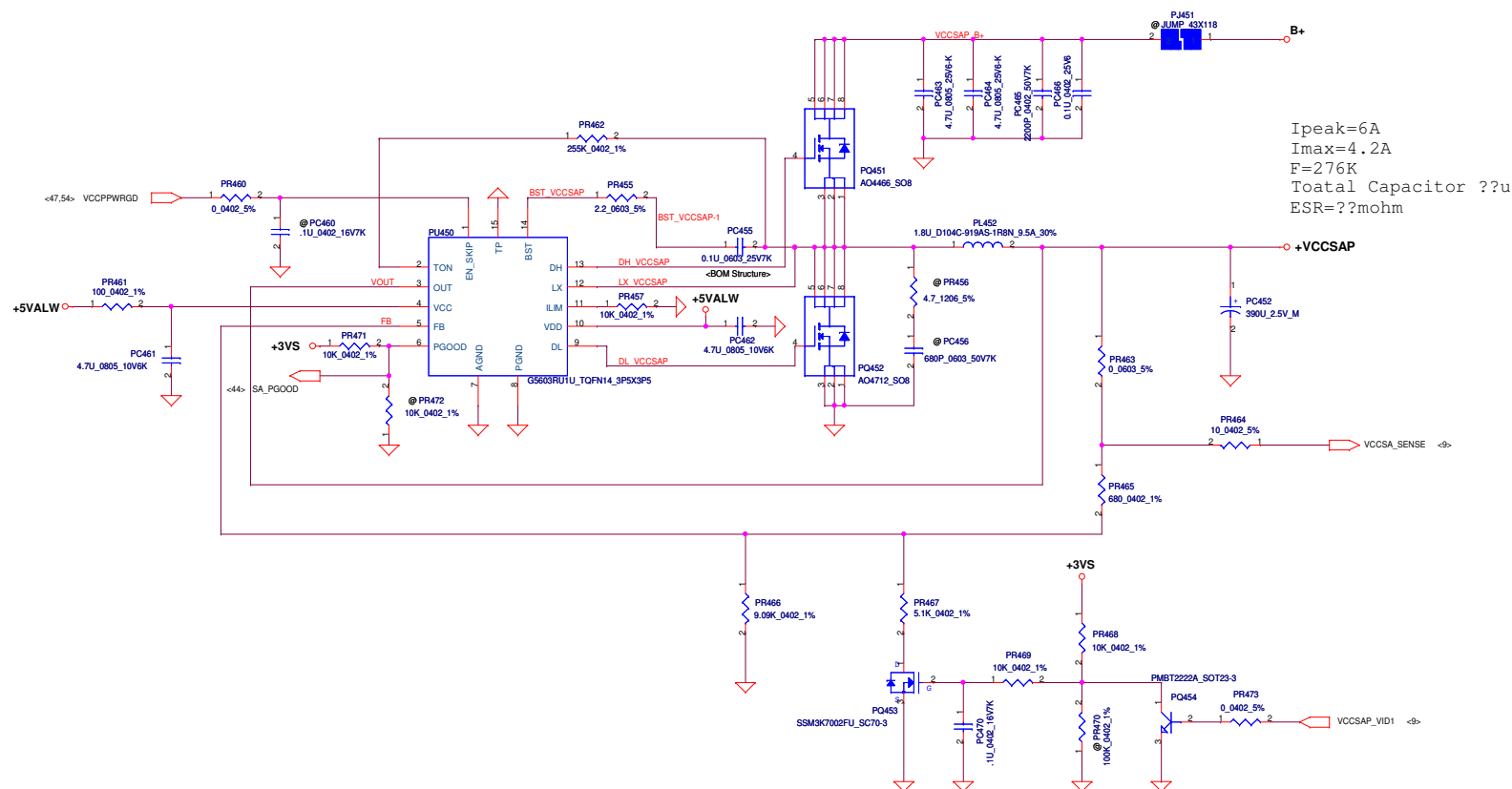
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L-->H	15.39V	15.88V	16.39V

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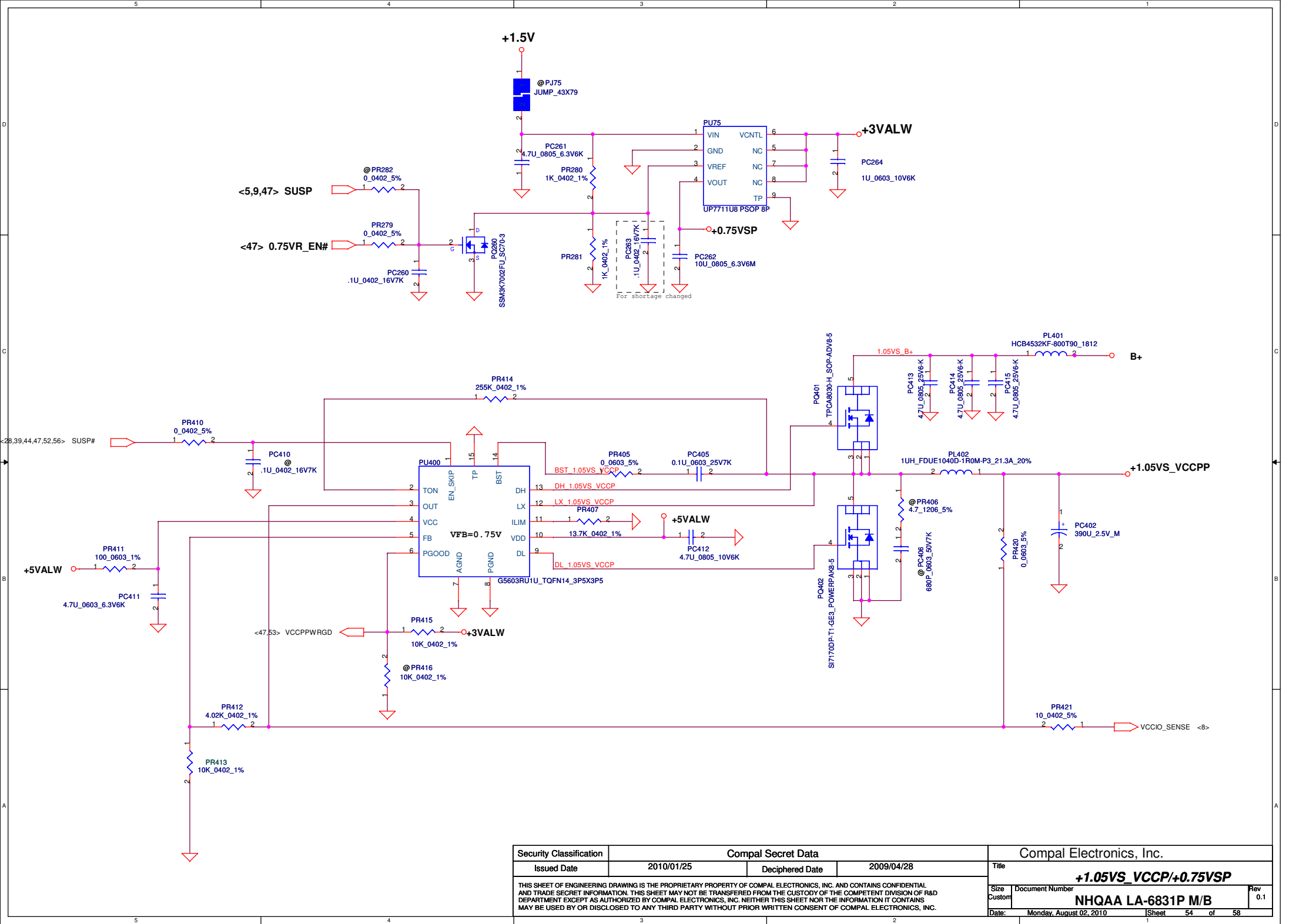


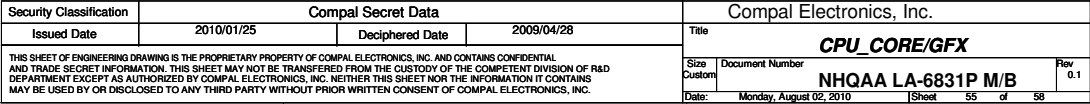


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VID1	+VCCSAP
1	0.8V
0	0.9V





HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30
NO DATE PAGE MODIFICATION LIST

PURPOSE

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	

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				Size	Document Number		Rev
					NHQAA LA-6831P M/B		0.1
				Date:	Monday, August 02, 2010	Sheet	57