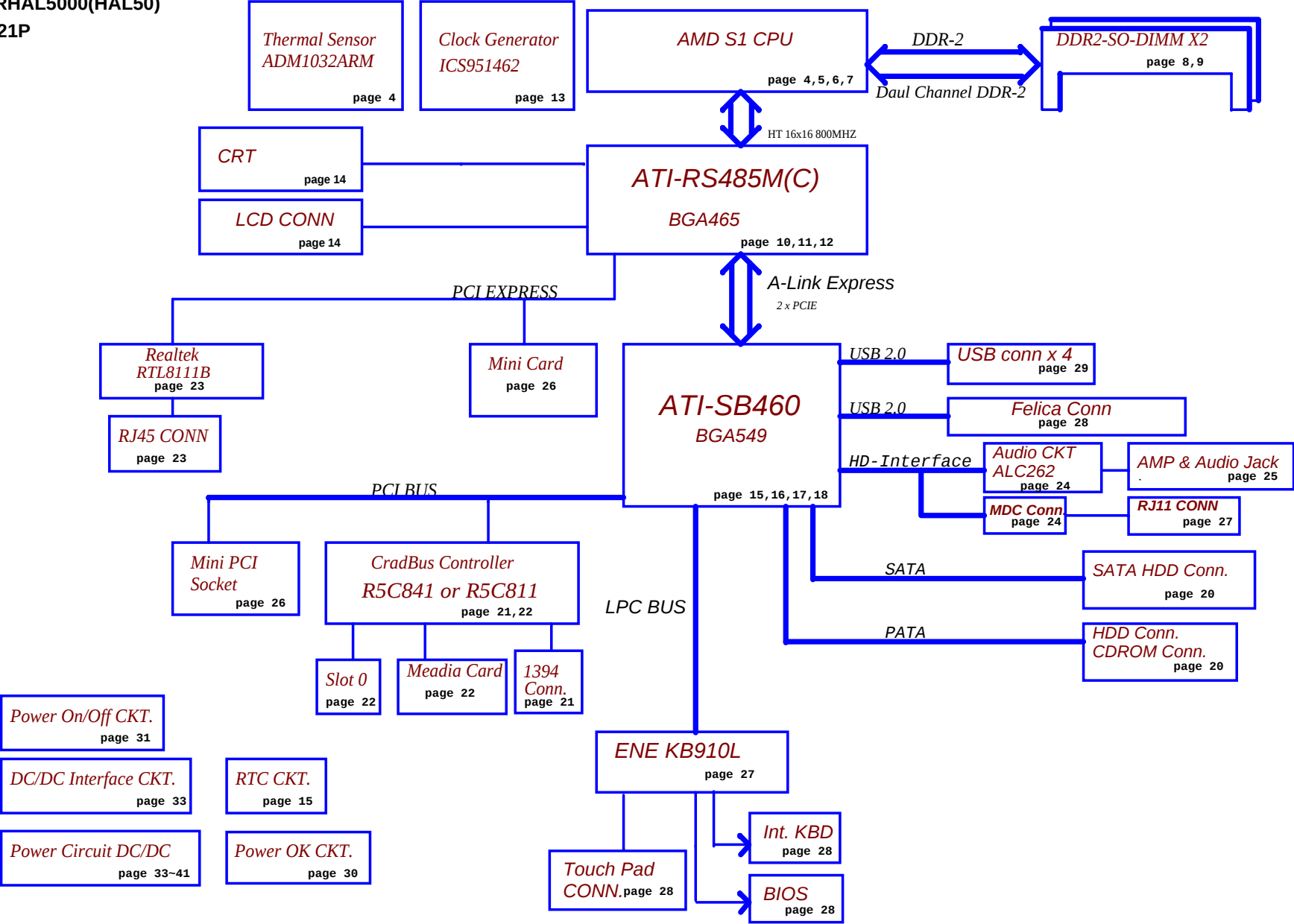


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Schematics Document
AMD/S1/ATI RS485M(C)/SB460
2005 / 12 / 30 Rev:0.1

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				Date: Friday, January 06, 2006	Sheet 1 of 43



Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG
Mini-PCI	AD22	1	PIRQF/PIRQG

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	1001 110X b?
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

Device	Address
Clock Generator (ICS 951462AGT)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

Board ID Table for AD channel

BOARD ID Table

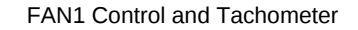
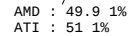
BTO Option Table

[illegible]

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				LA-3221P	0.1	
				Date:	Friday, January 06, 2006	Sheet 3 of 43

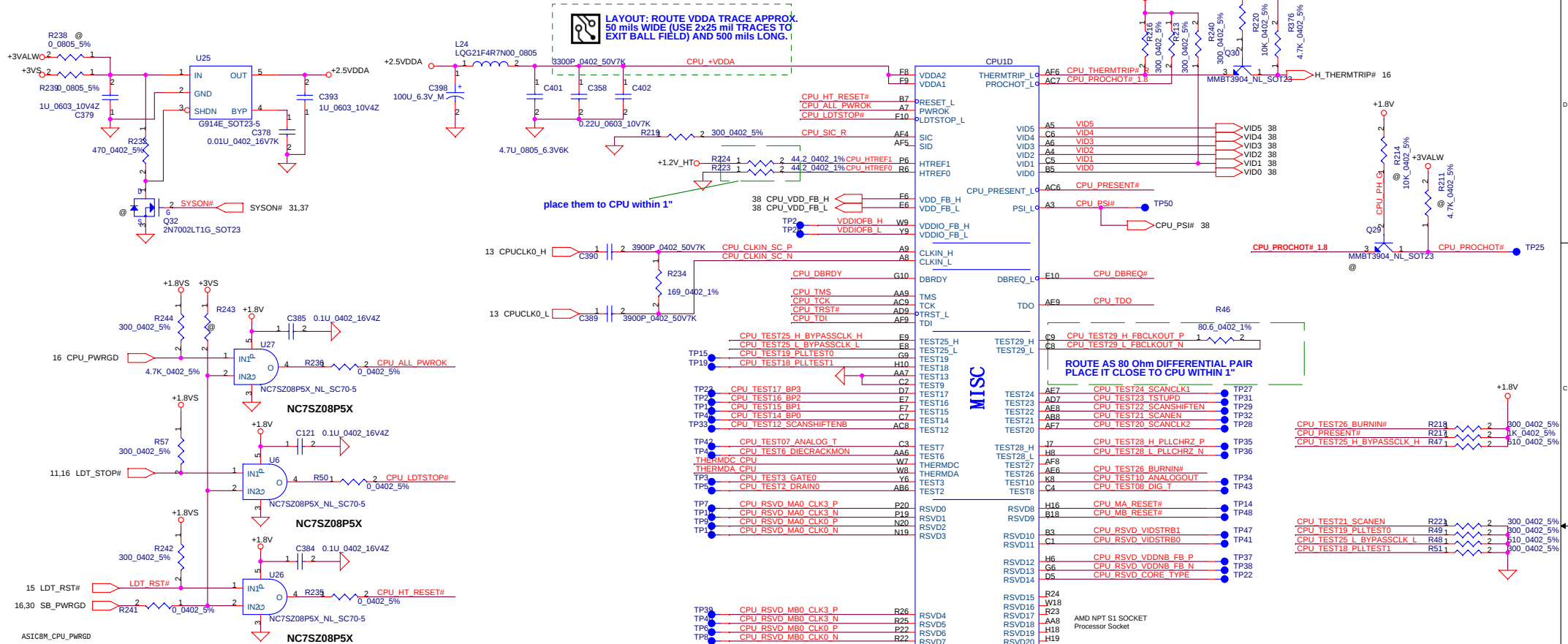


VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

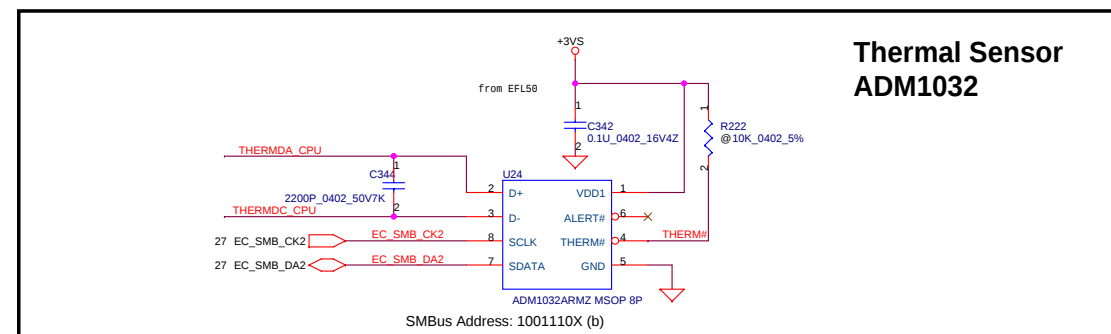
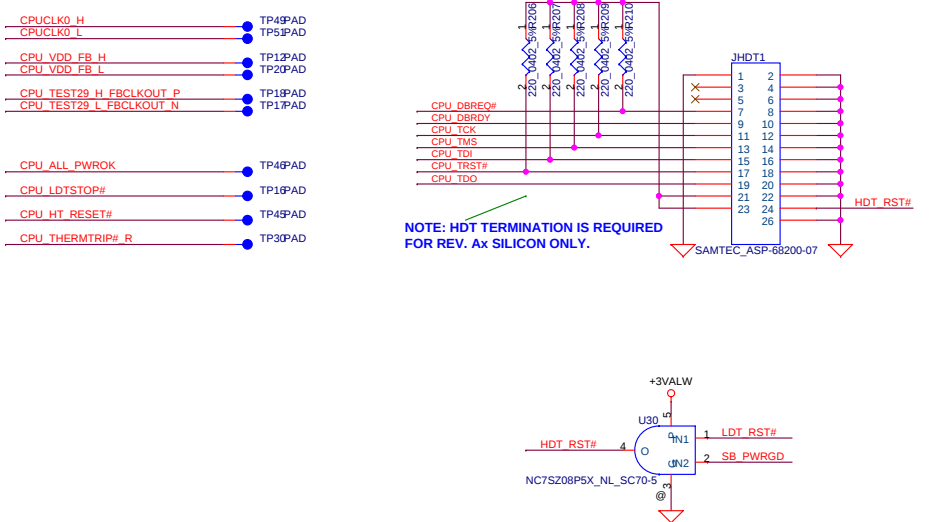


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				Custody	LA-3221P	0.1	
				Date	Friday, January 06, 2006	Sheet	4 of 43

ATHLON Control and Debug

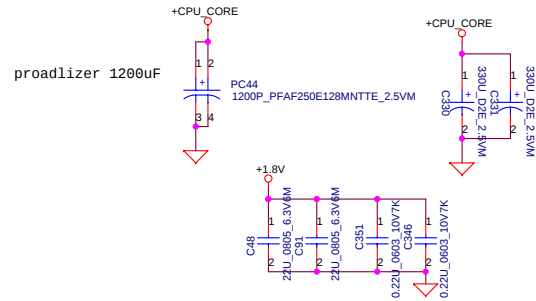


HDT Connector

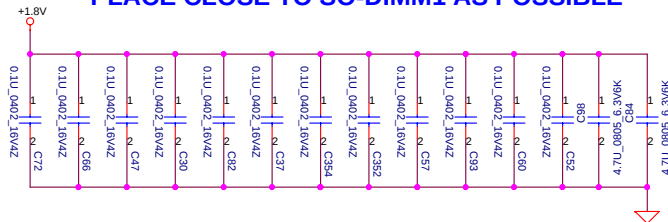


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				LA-321P	0.1
				Date: Friday, January 06, 2006	Sheet 6 of 43

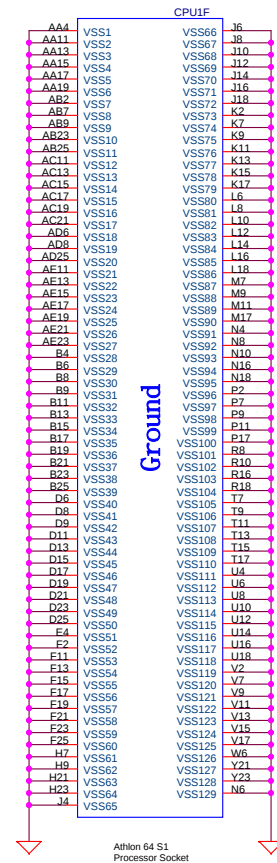
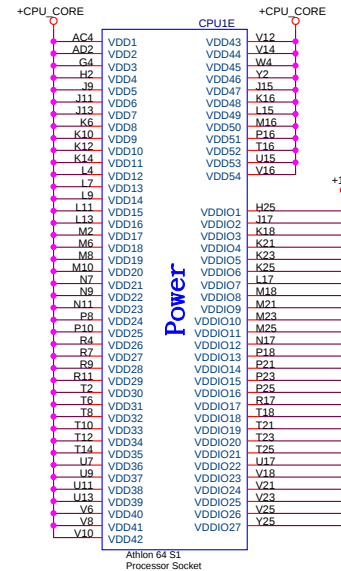
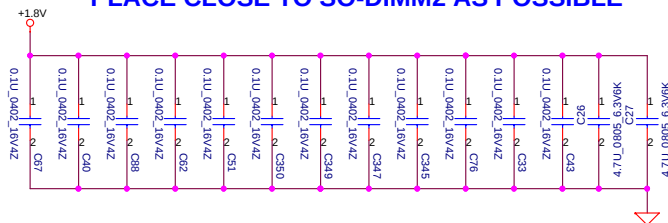
BOTTOMSIDE DECOUPLING



PLACE CLOSE TO SO-DIMM1 AS POSSIBLE

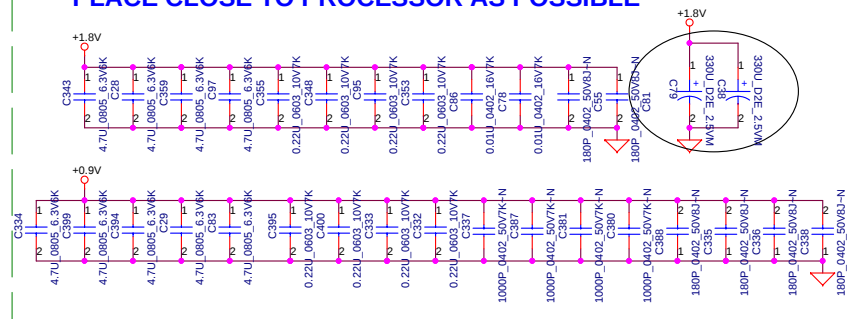


PLACE CLOSE TO SO-DIMM2 AS POSSIBLE

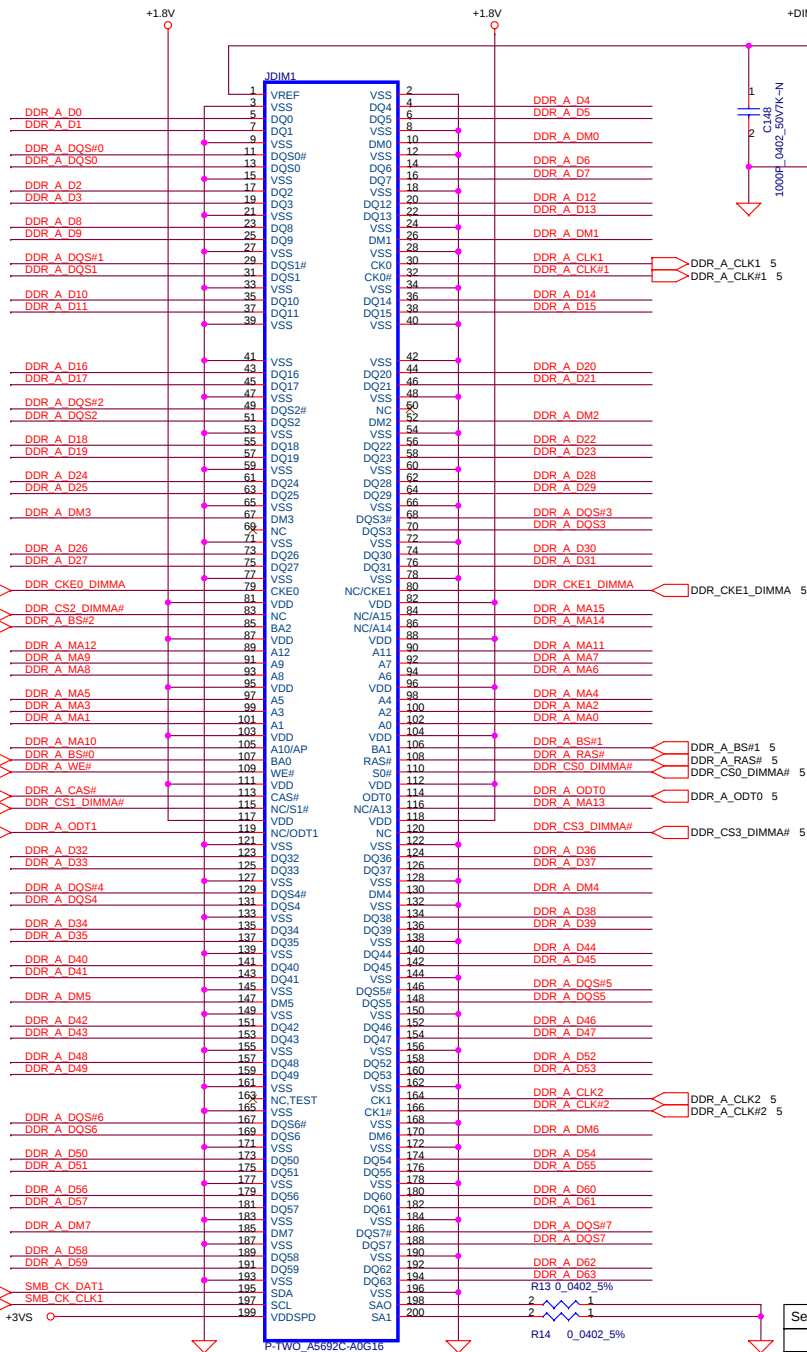


DECOUPLING BETWEEN PROCESSOR AND DIMMs

PLACE CLOSE TO PROCESSOR AS POSSIBLE



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				Doc Number	LA-3221P
				Rev	0.1
Date	Friday, January 06, 2006		Sheet	7	of 43



9.13.16.26 SMB_CK_DAT1
9.13.16.26 SMB_CK_CLK1

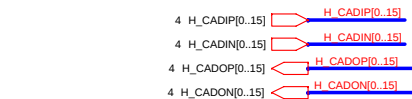
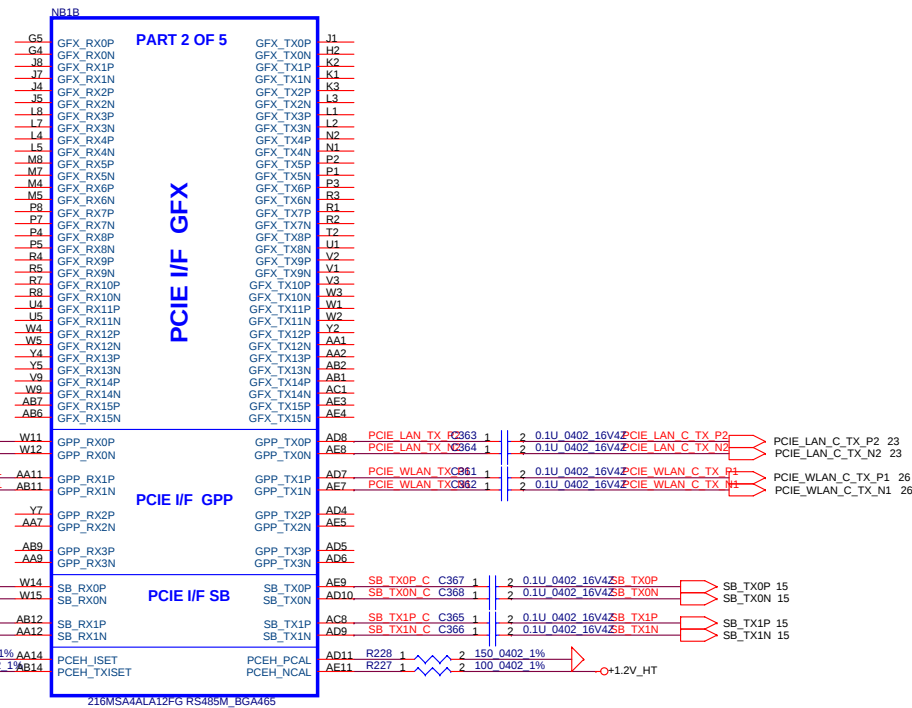
SMB CK DAT1
SMB CK CLK1

+3VS

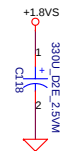
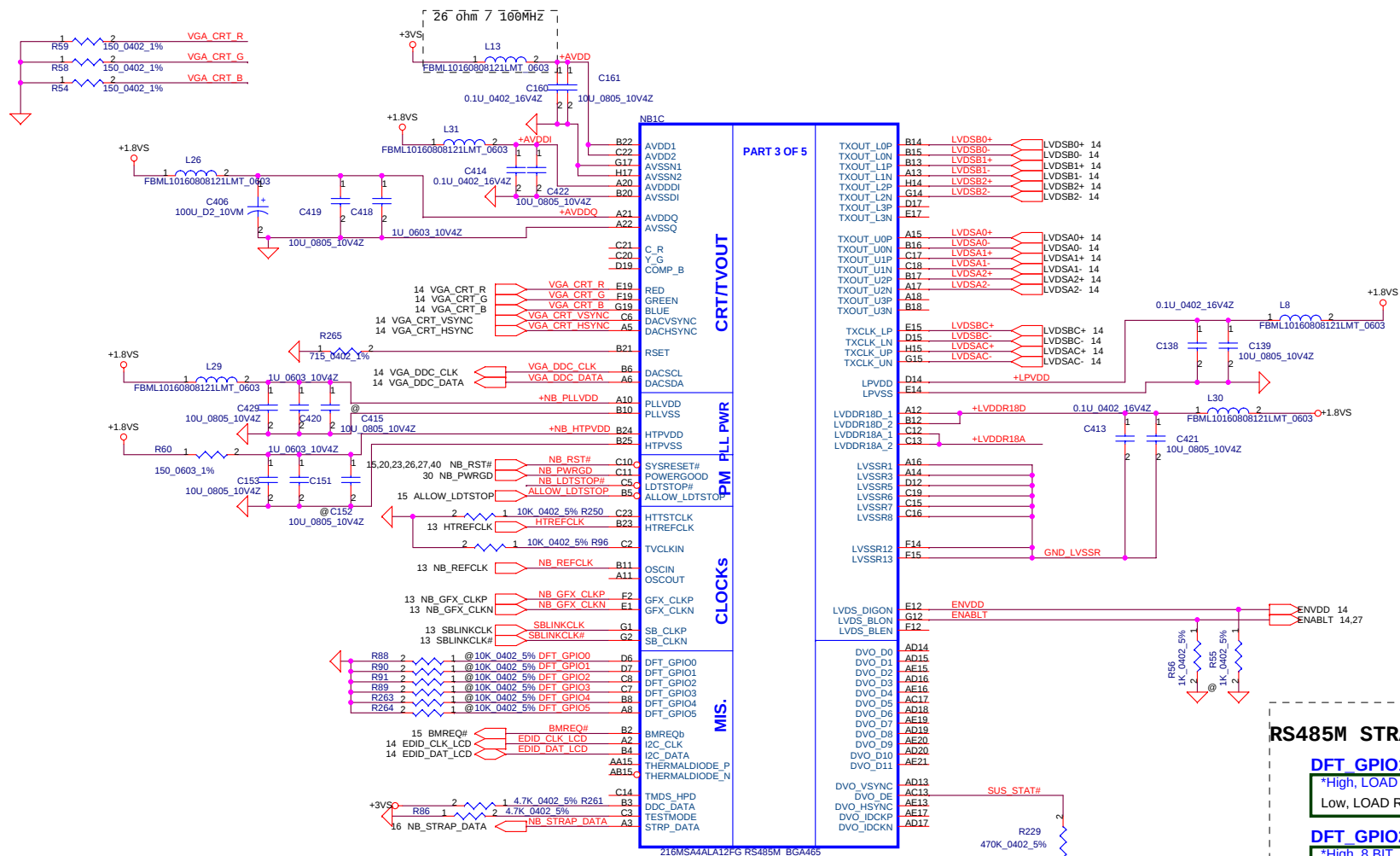
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R14 0_0402_5%

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								DDR2 SO-DIMM I	
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						LA-3221P		0.1	
						Date:		Friday, January 06, 2006	
						Sheet		8 of 43	



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				Date	Friday, January 06, 2006	Sheet 10 of 43



RS485M STRAPS(Internal pull up)

DFT GPIO1:LOAD ROM STRAPS

*High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE

DFT GPIO2:HT LINK WIDTH

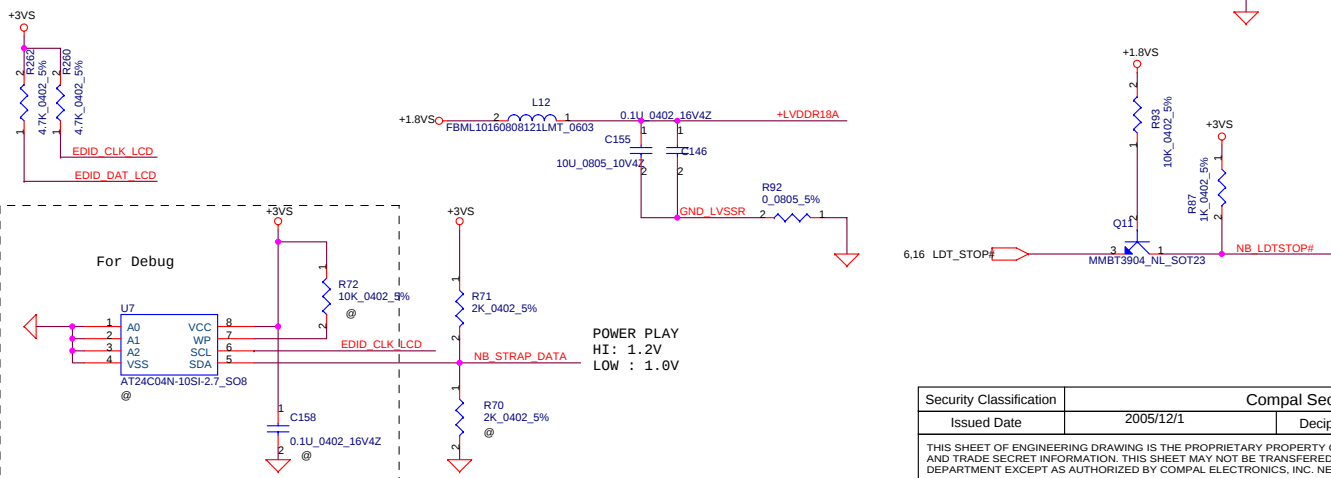
*High, 8 BIT
Low,RESERVED

DFT GPIO3,4:HT LINK FREQ

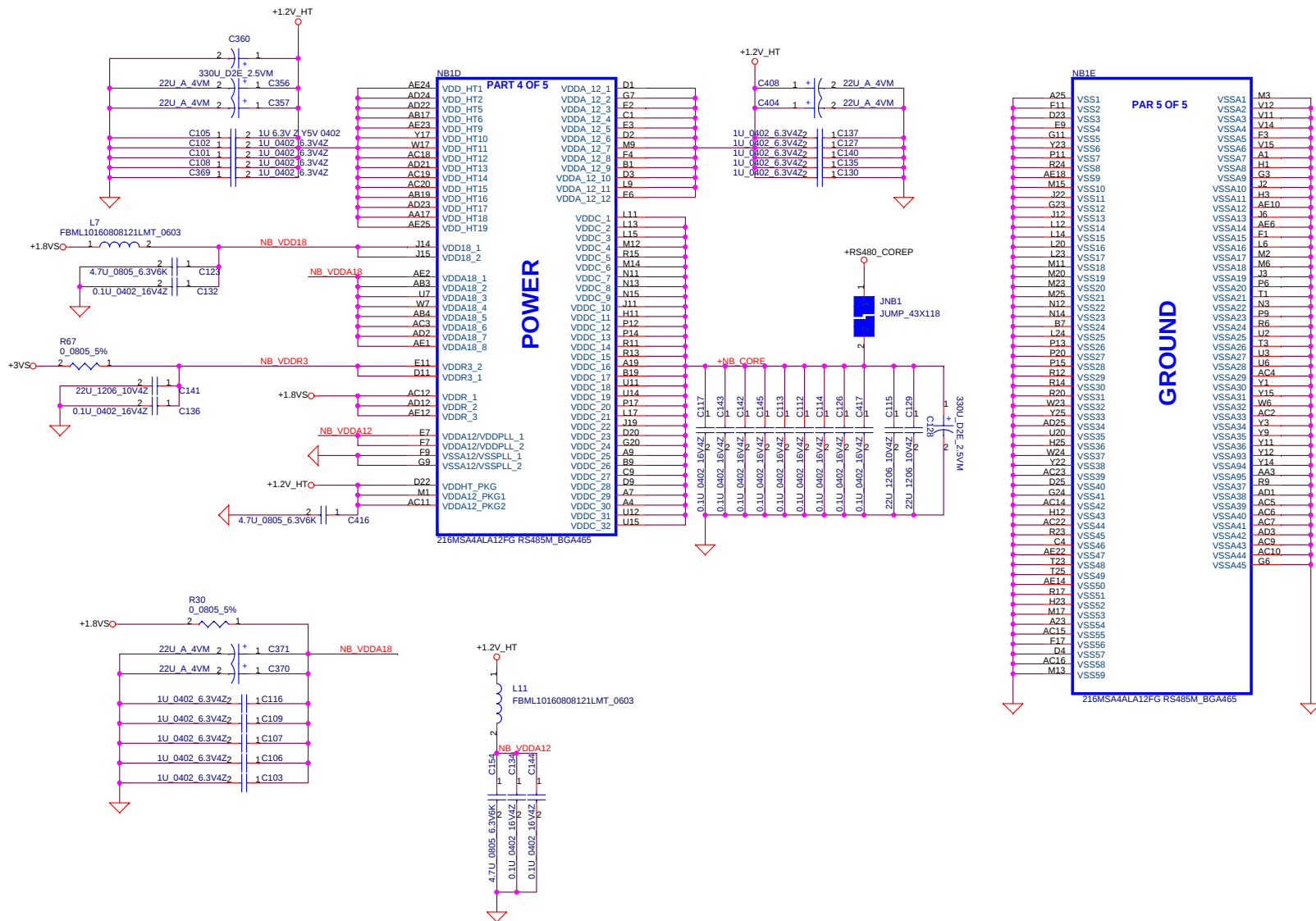
GPI04	GPI03	DESCRIPTION
0	0	RESERVED
0	1	RESERVED
1	0	RESERVED
1	1	200MHZ

DFT GPIO5:LOAD MEM STRAPS

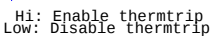
*High, LOAD MEM STRAP DISABLE
Low, LOAD MEM STRAP ENABLE



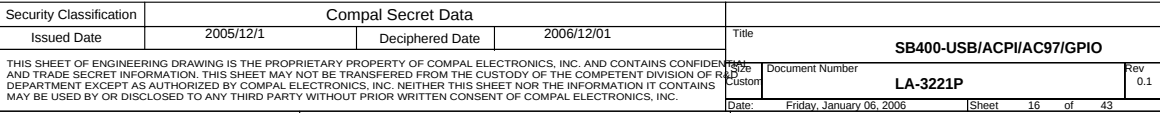
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Issued Date	2005/12/1	Deciphered Date	2006/12/01	RS480M VIDEO_IF/CLOCK GEN	
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				LA-3221P	0.1
Date: Friday, January 06, 2006		Sheet 11		of 43	

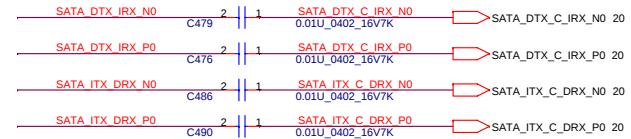
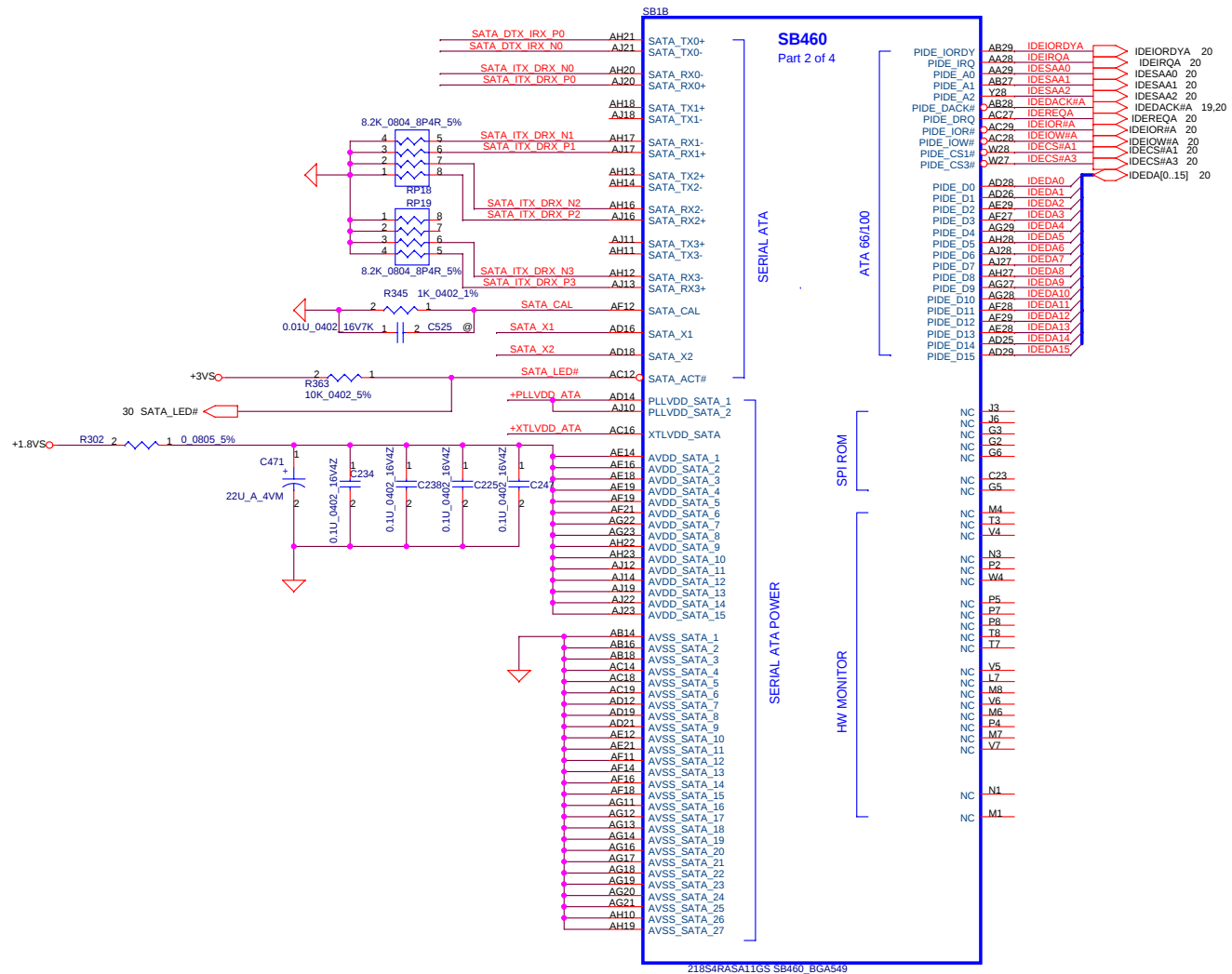
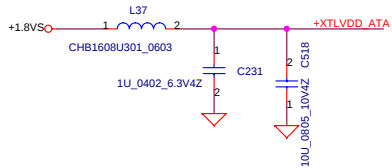
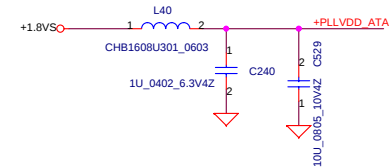
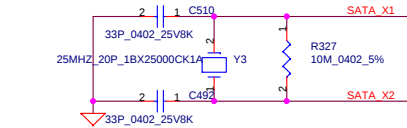


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				LA-3221P	0.1
Date: Friday, January 06, 2006				Sheet 12	of 43



Page Size Custom	Document Number LA-3221P	Rev 0.1
Date: Friday, January 06, 2006		Sheet 15 of 43



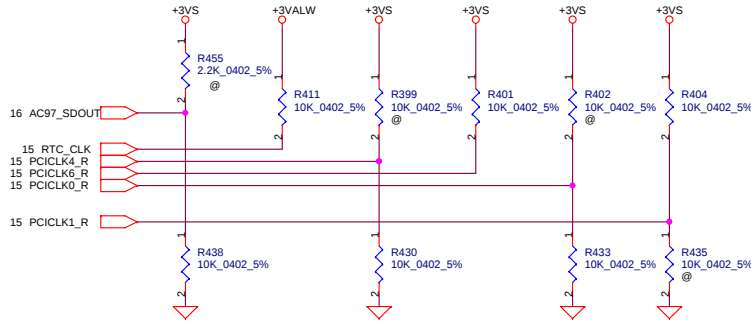


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								SB400-IDE/SATA	
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								Document Number	LA-3221P
Date: Friday, January 06, 2006								Sheet	17 of 43



REQUIRED STRAPS

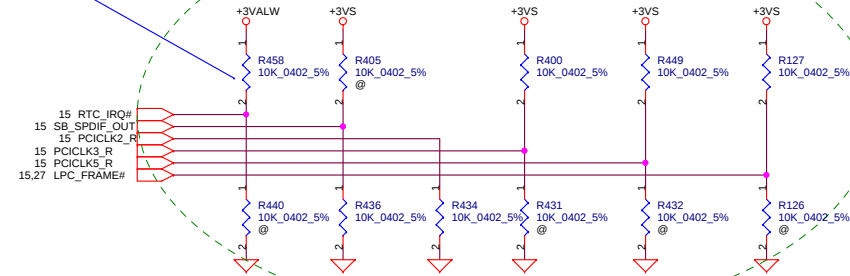
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	AC97_SDOUT	RTC_CLK	PCICLK4_R	PCICLK6_R	PCICLK1_R	PCICLK0_R
PULL HIGH	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM DEFAULT	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	

NOTE: R751 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB600
TO KEEP THE INPUT FROM FLOATING.

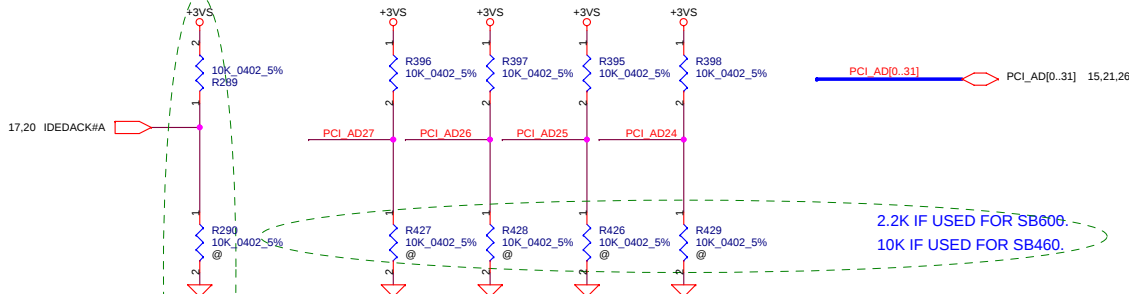
SB460 ONLY



	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

DEBUG STRAPS

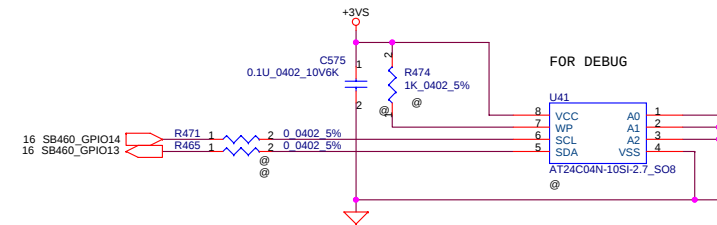
SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#A	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

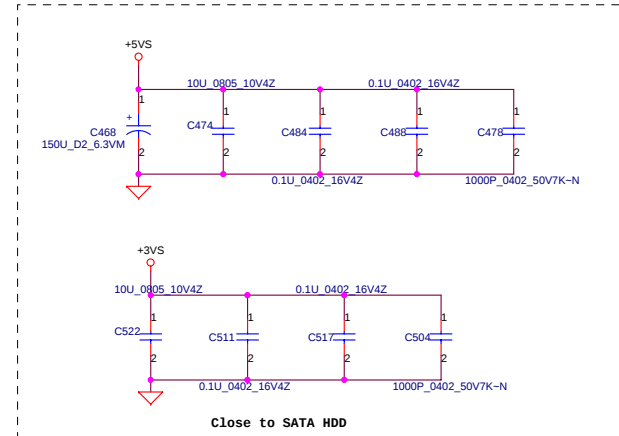
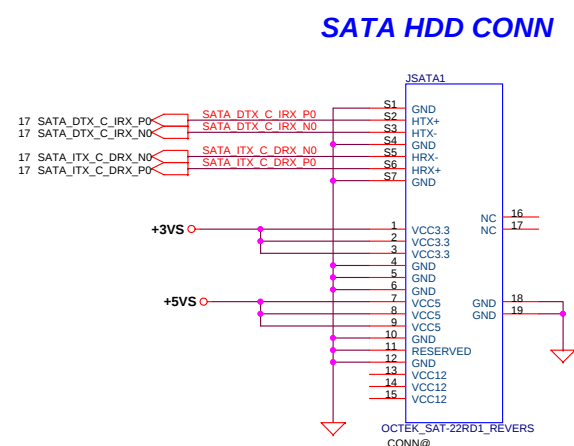
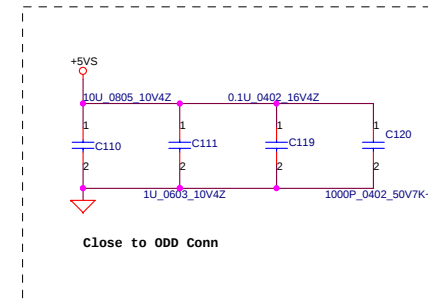
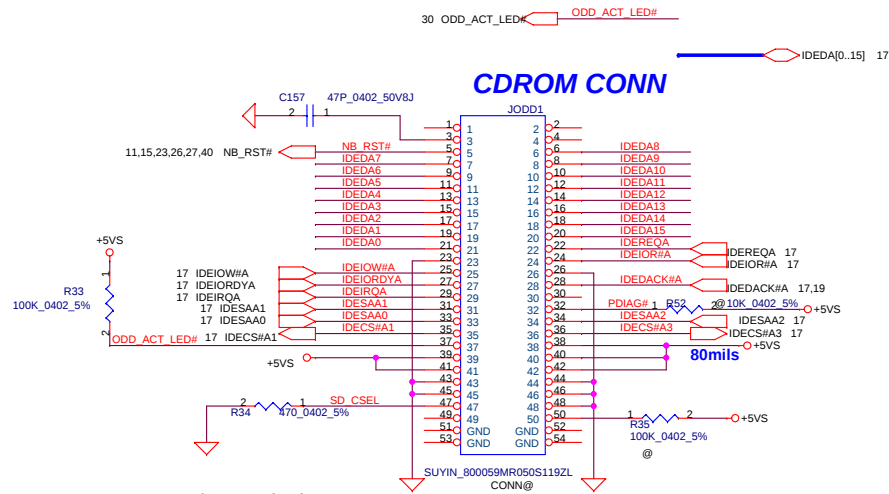
SB460 ONLY

OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

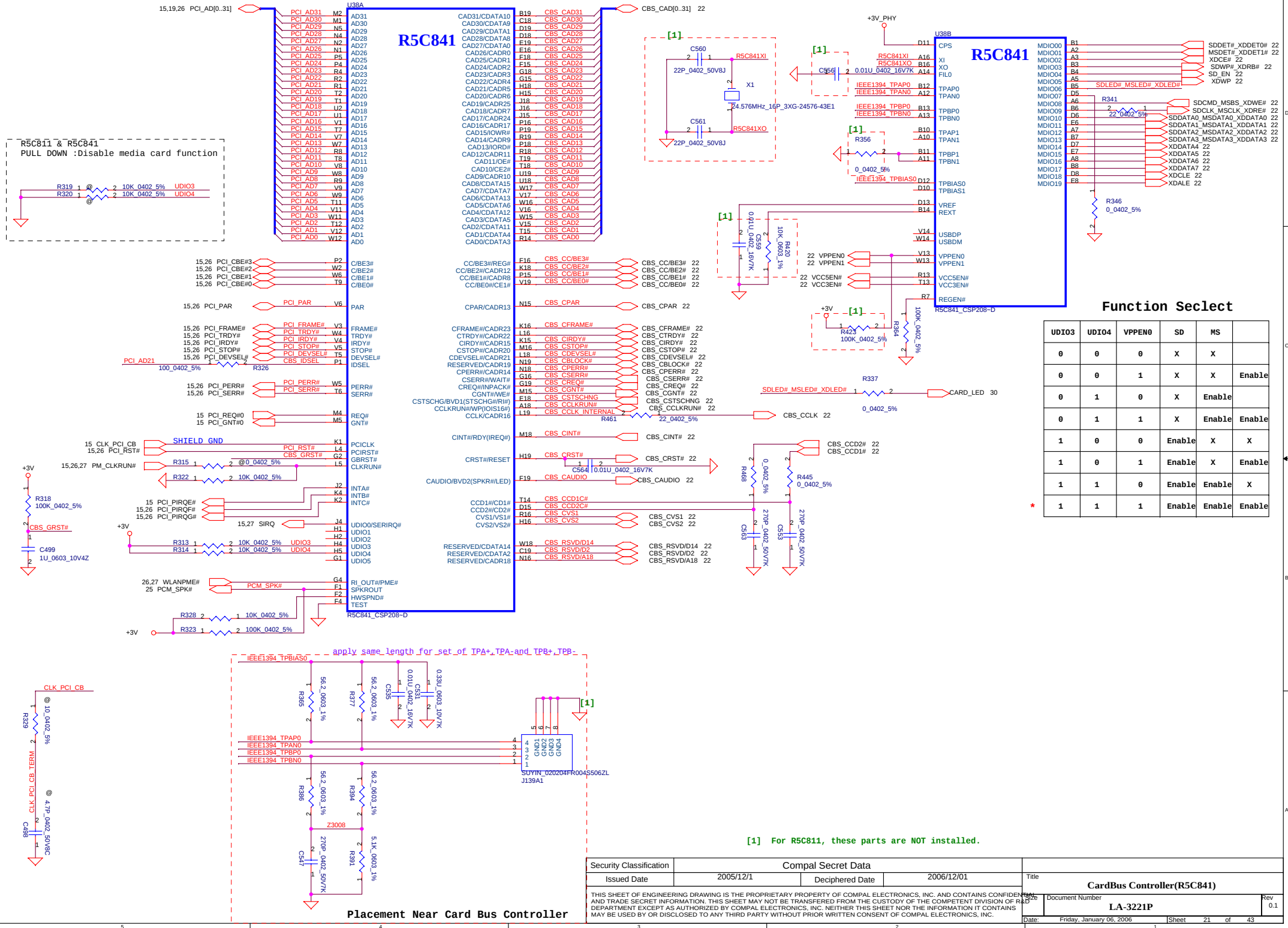


SB PCIE EEPROM STRAPS

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				LA-3221P	0.1
				Date: Friday, January 06, 2006	Sheet 19 of 43

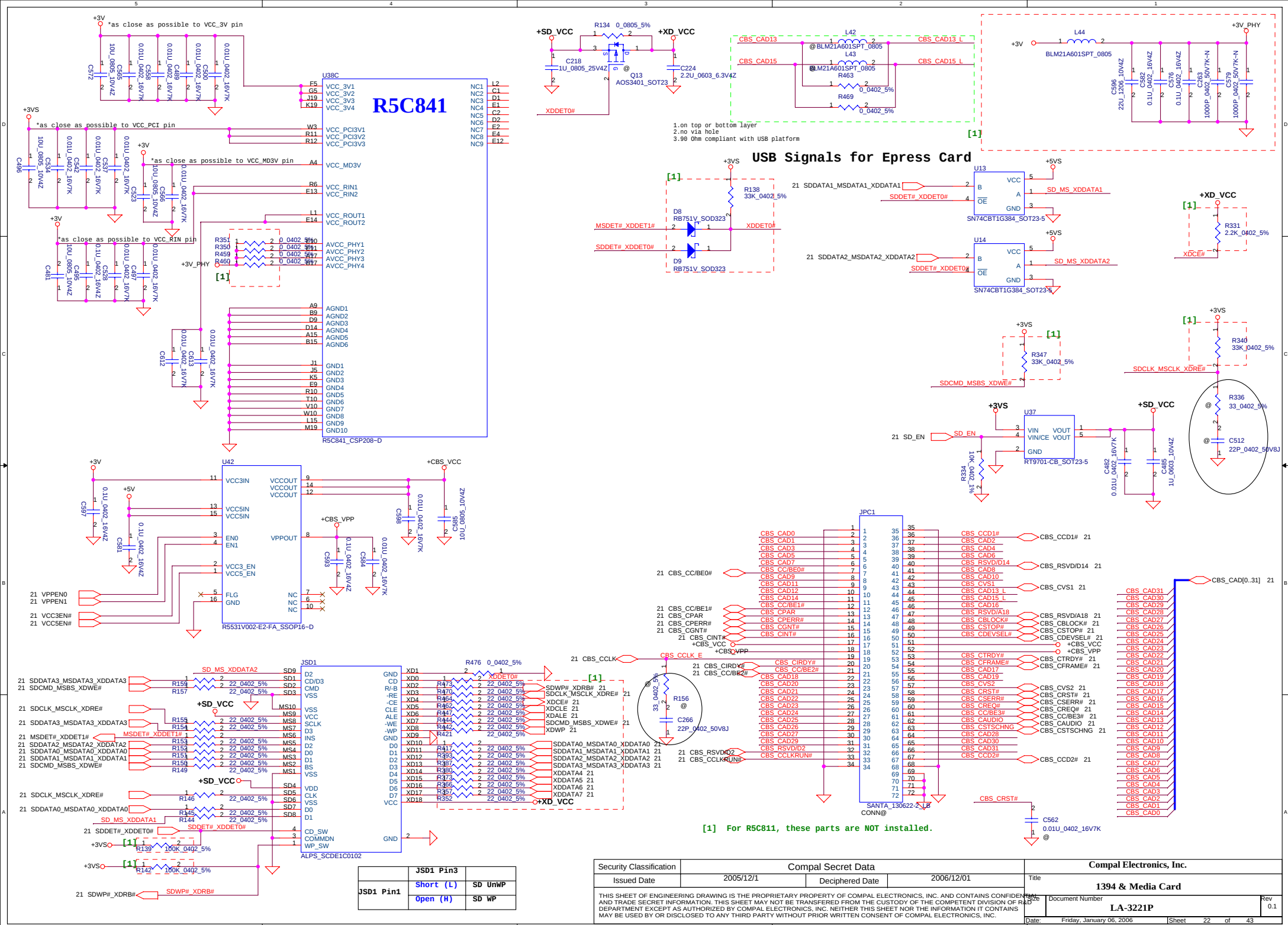


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				LA-3221P	0.1
				Friday, January 06, 2006	Sheet 20 of 43

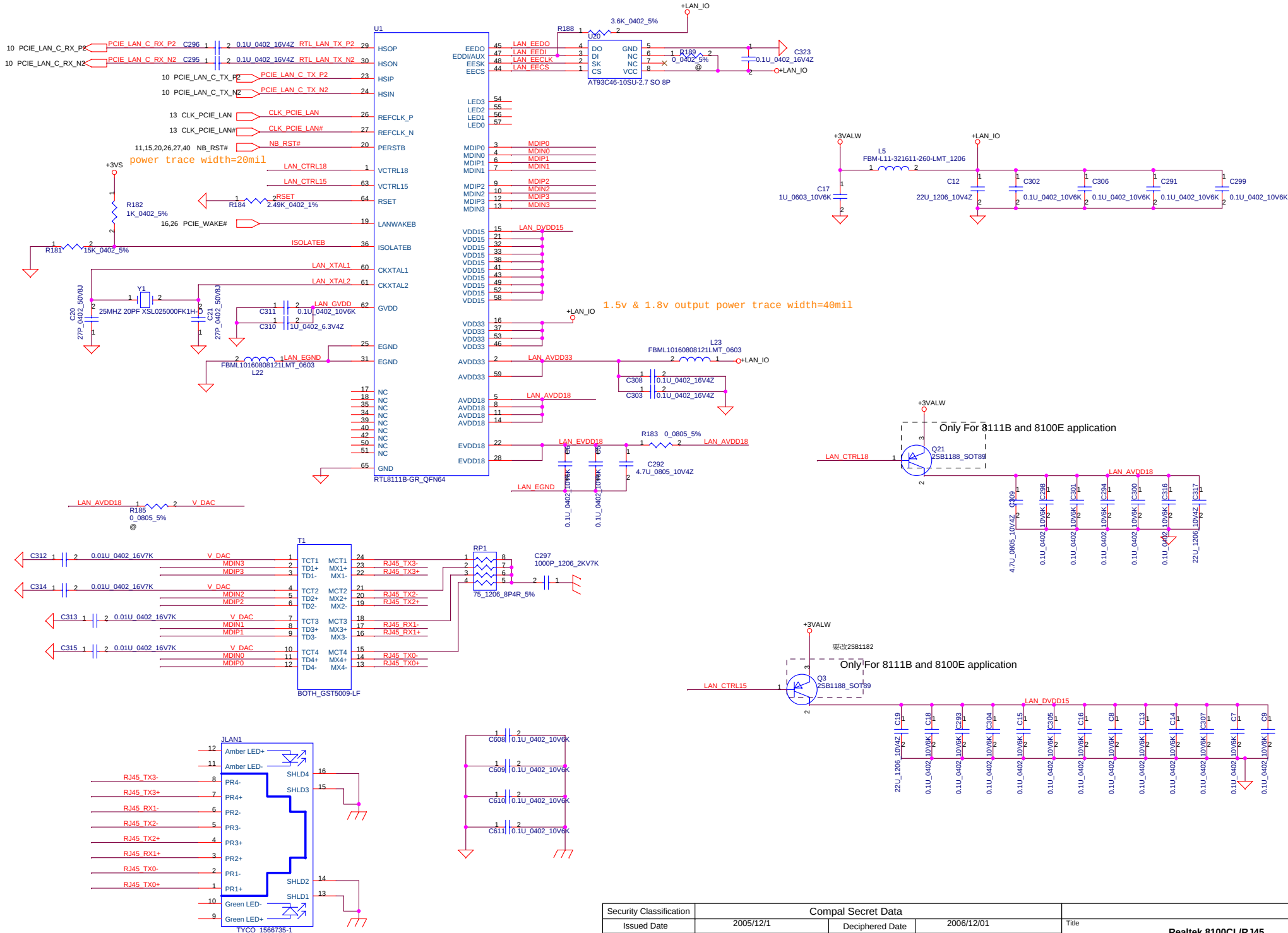


Function Select					
UDIO3	UDIO4	VPPEN0	SD	MS	
0	0	0	X	X	
0	0	1	X	X	Enable
0	1	0	X	Enable	
0	1	1	X	Enable	Enable
1	0	0	Enable	X	X
1	0	1	Enable	X	Enable
1	1	0	Enable	Enable	X
1	1	1	Enable	Enable	Enable

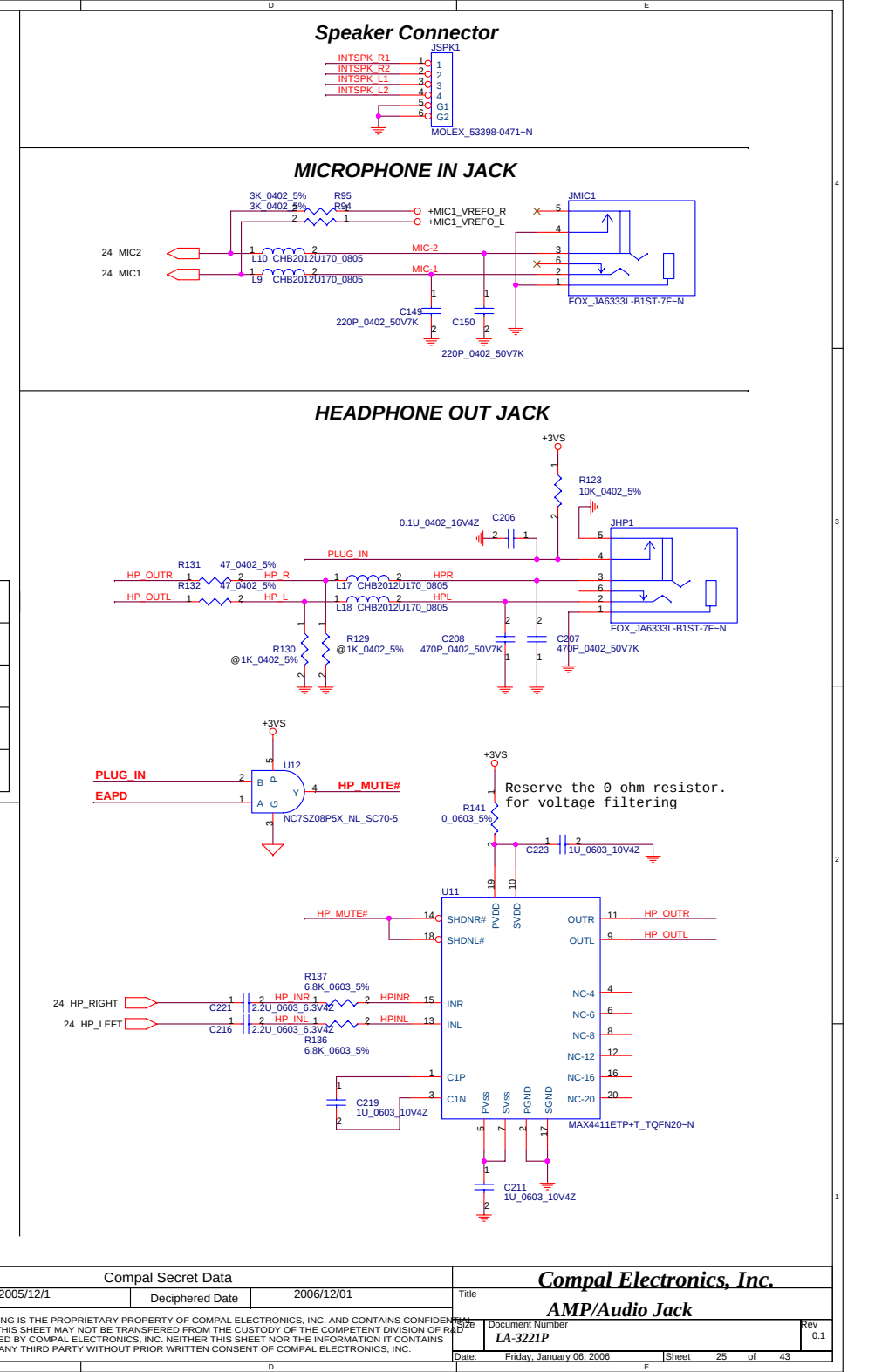
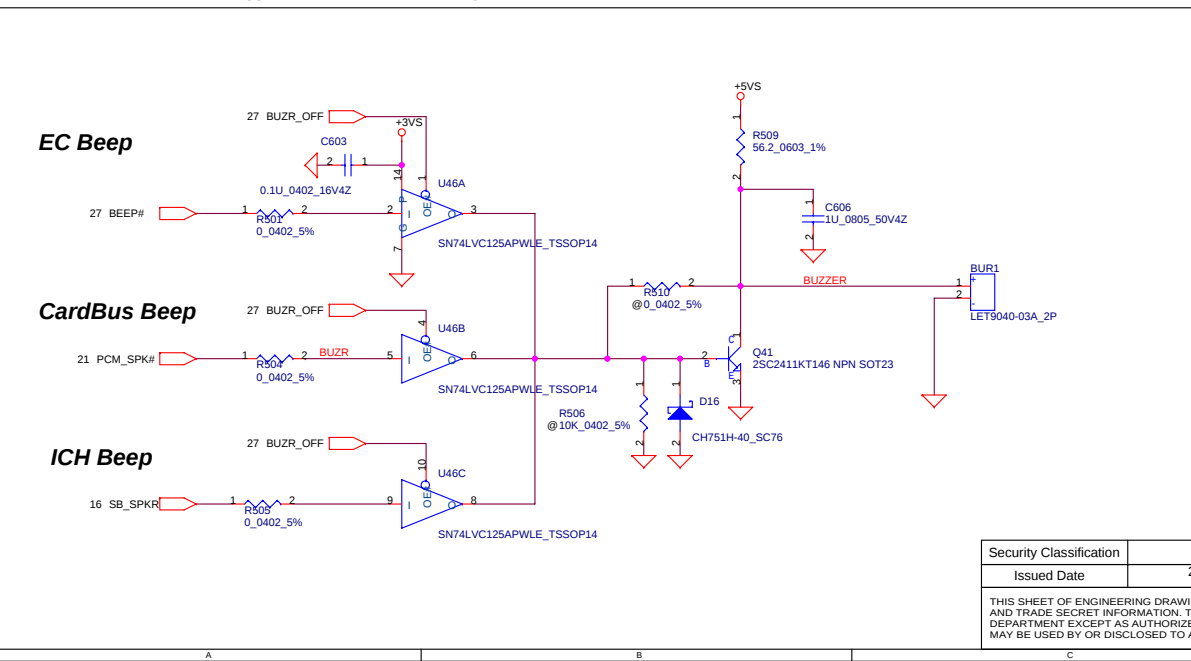
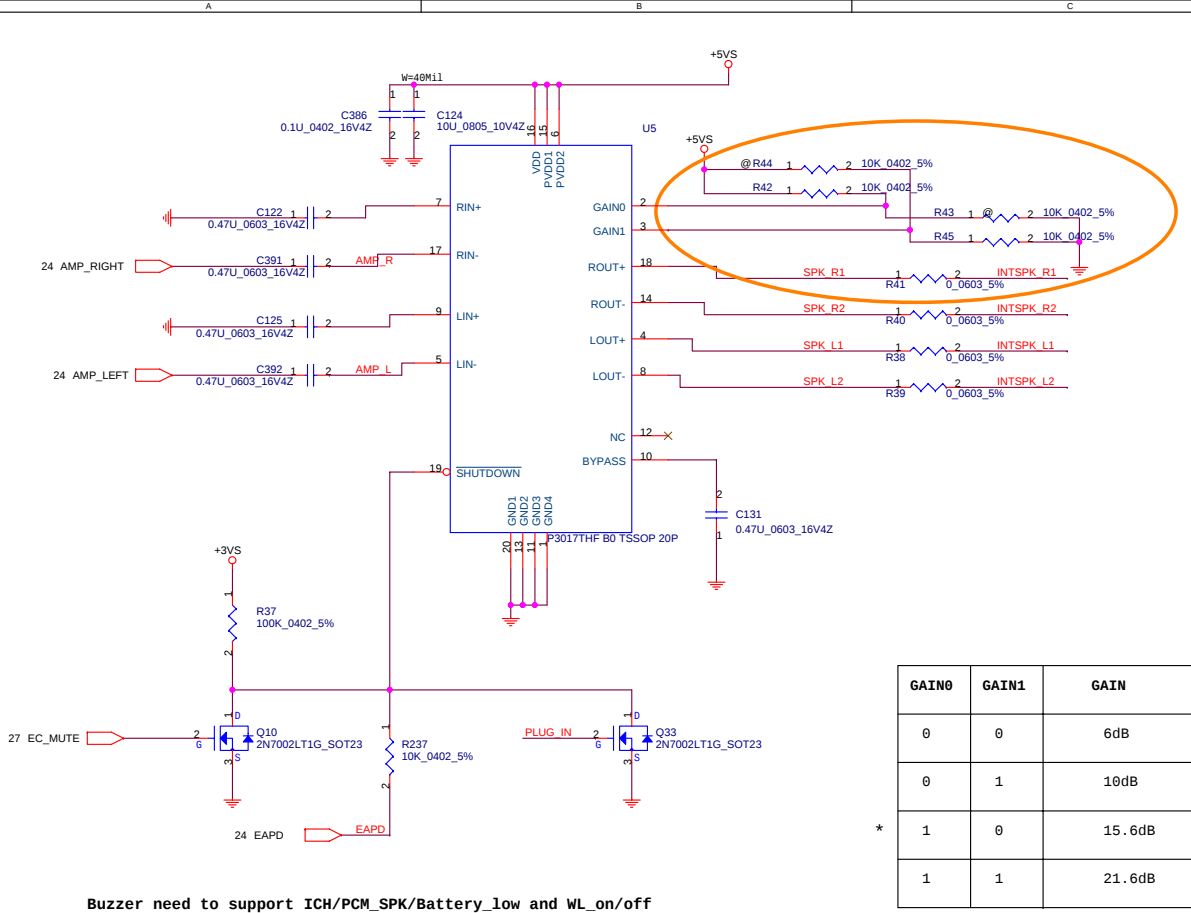
[1] For R5C811, these parts are NOT installed.

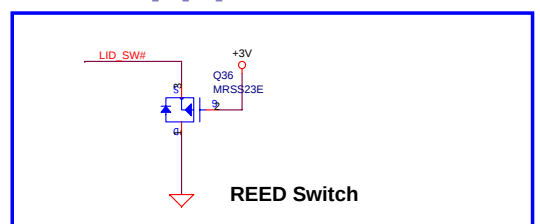
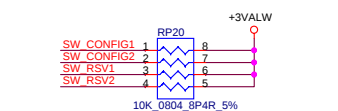
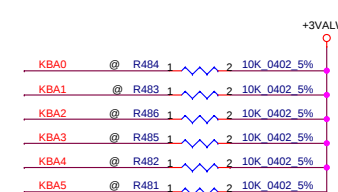
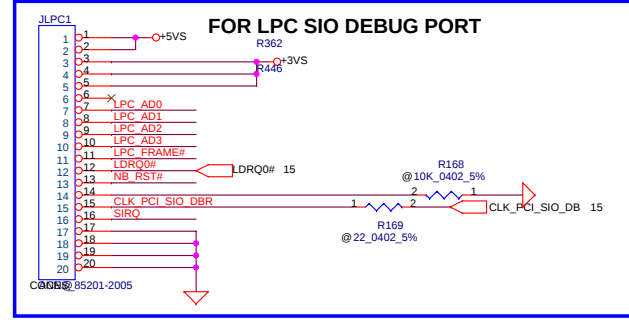
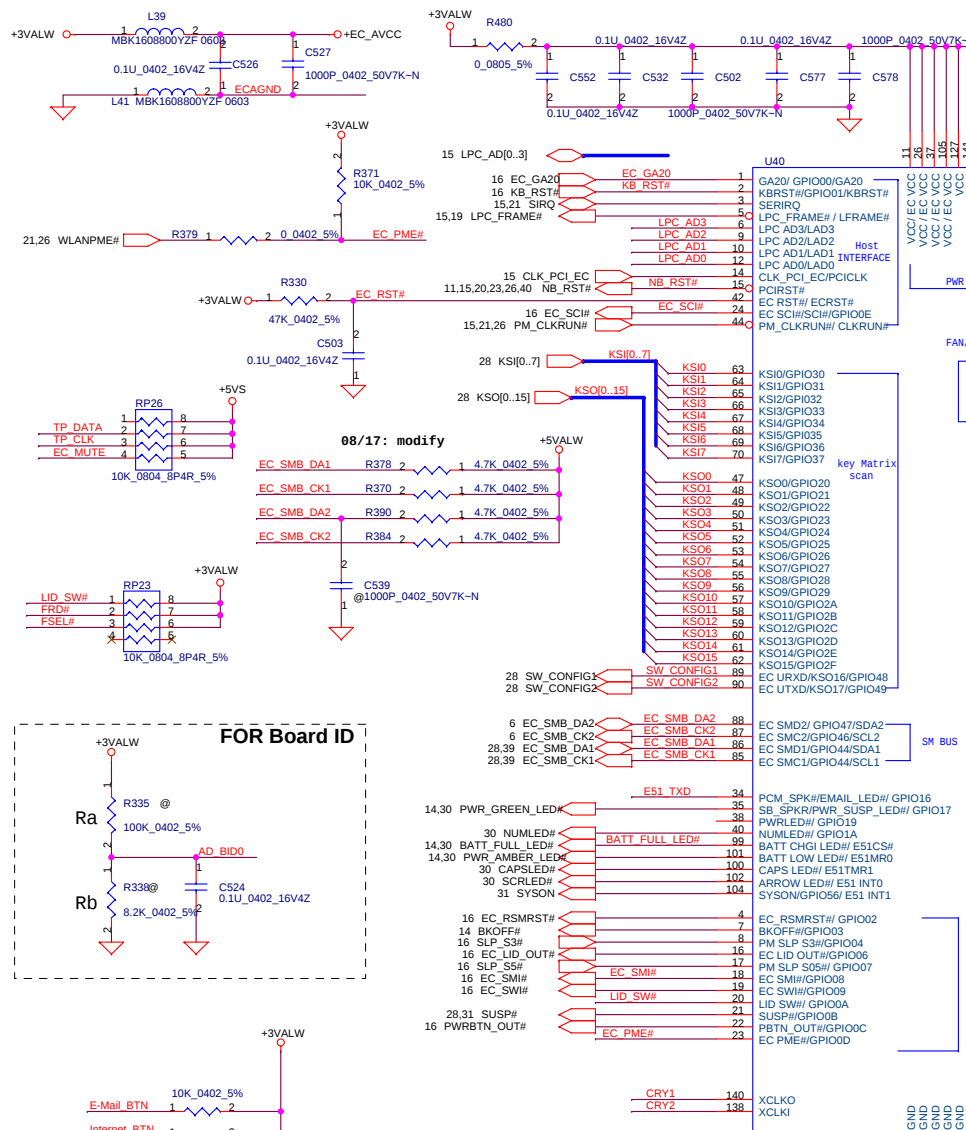


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						Docu		Document Number		LA-3221P		Rev	
						Date:		Friday, January 06, 2006		Sheet		22 of 43	
												0.1	

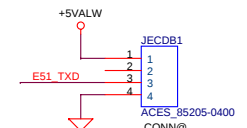
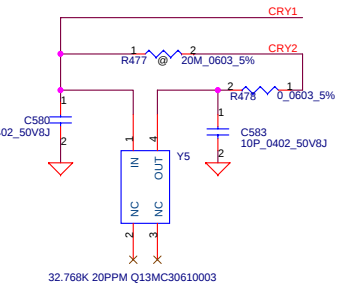
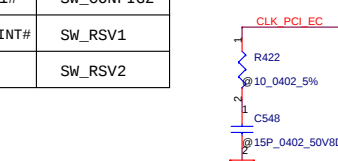


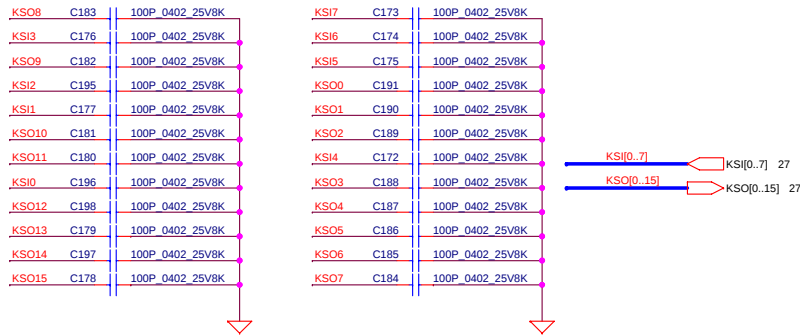
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Issued Date				2005/12/1				2006/12/01			
Deciphered Date				2006/12/01				Realtek 8100CL/RJ45			
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Document Number				LA-3221P				Rev 0.1			
Sheet				23				of 43			



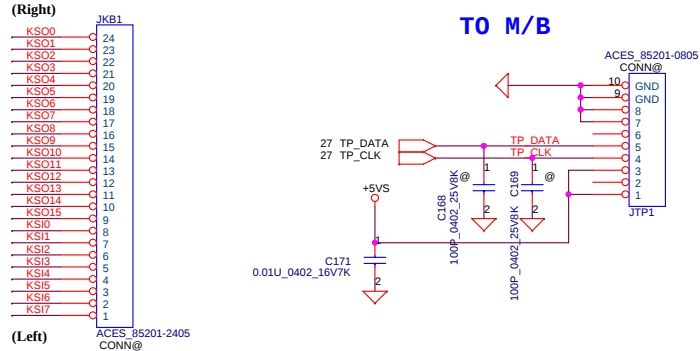


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KBSEL1#	SW_CONFIG2
FINGERPRINT#	SW_RSV1
	SW_RSV2

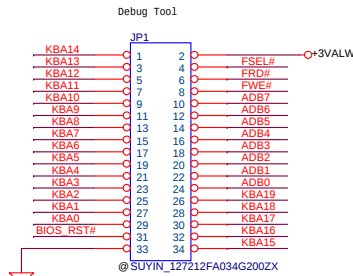
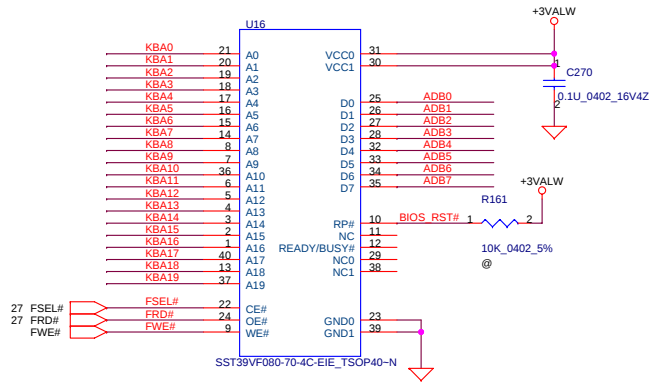
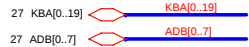




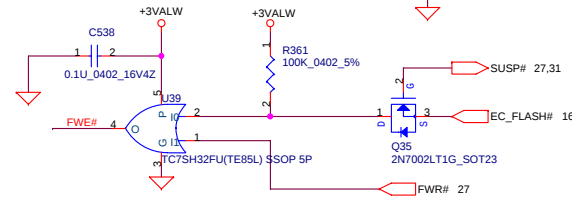
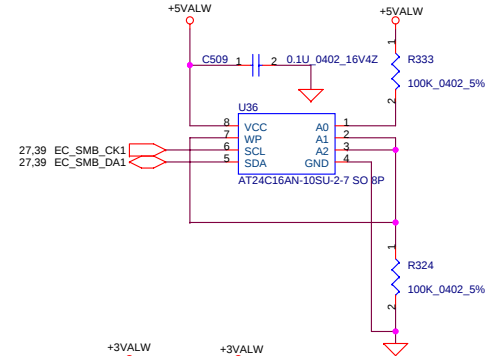
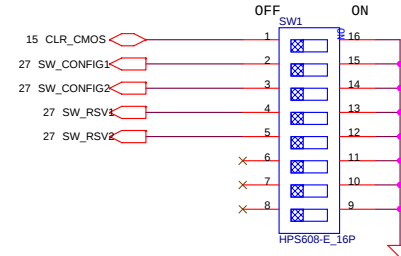
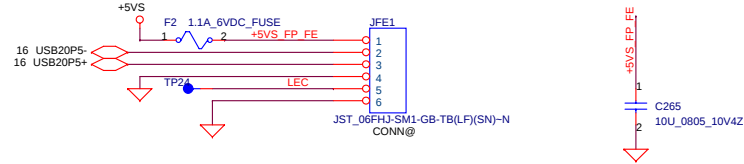
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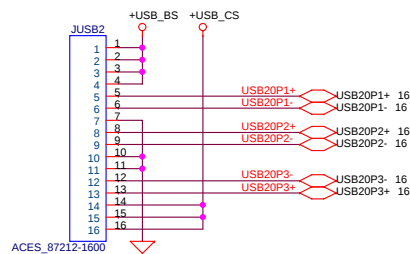
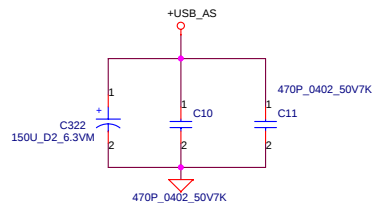
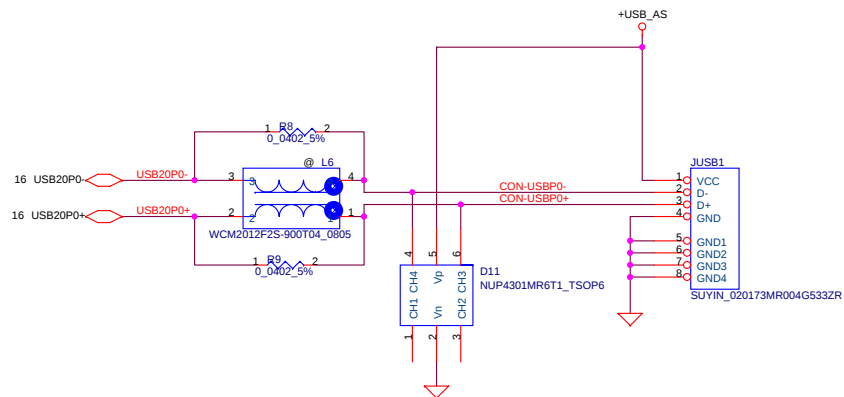
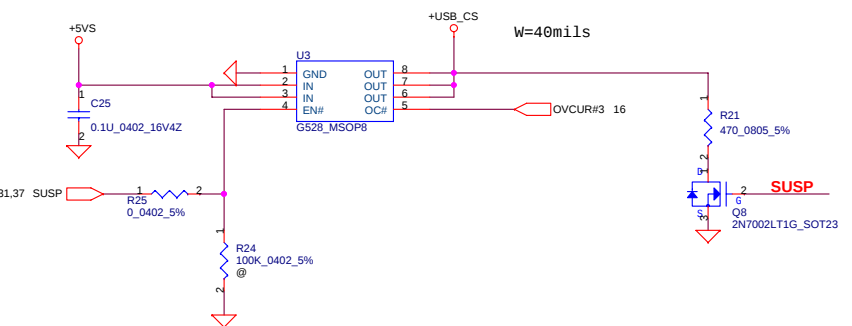
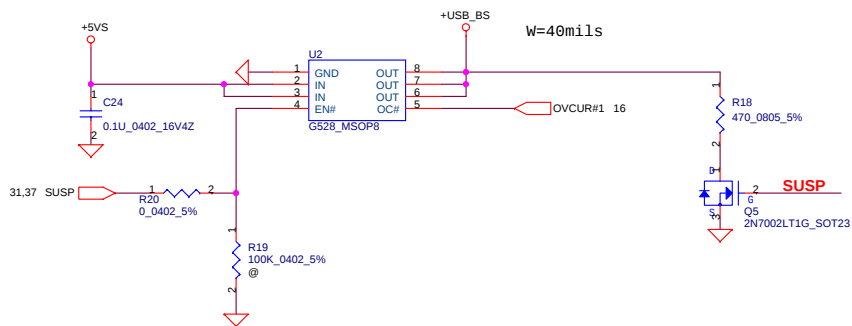
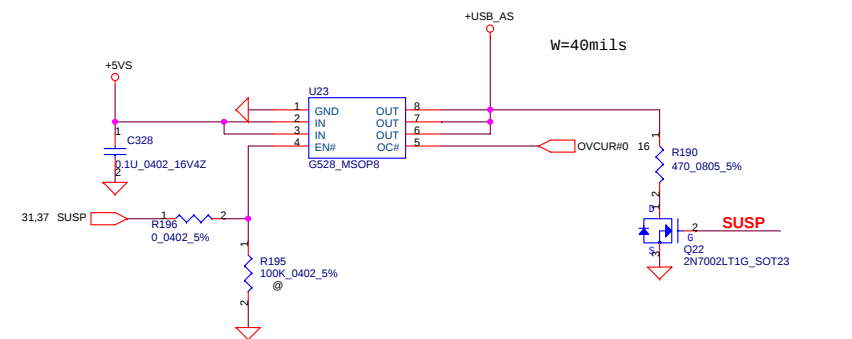
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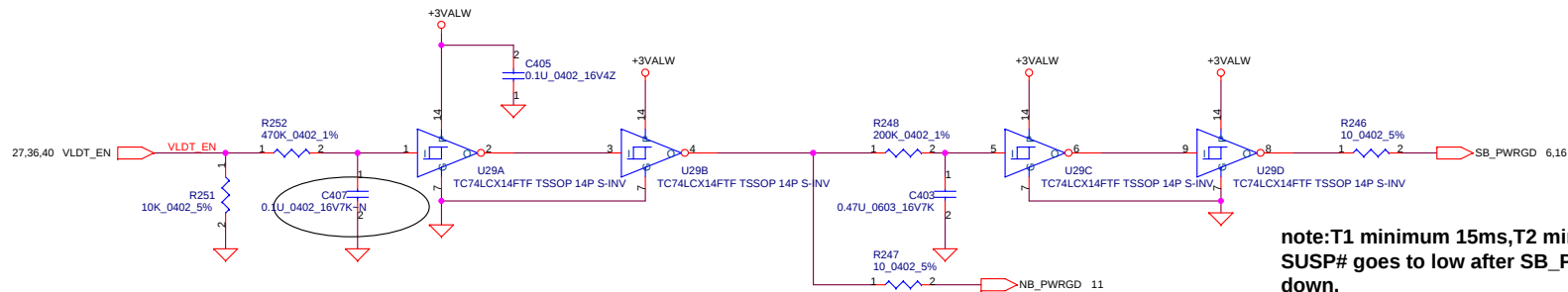
Felica Conn



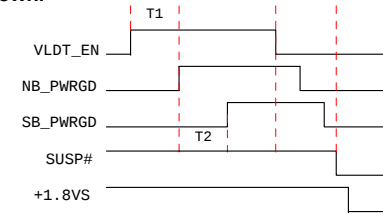
Security Classification	Compal Secret Data			Title	
Issued Date	2005/12/1	Deciphered Date	2006/12/01	MDA/BT/KBD/TP Conn	
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				LA-3221P	0.1
Date:				Friday, January 06, 2006	Sheet 28 of 43



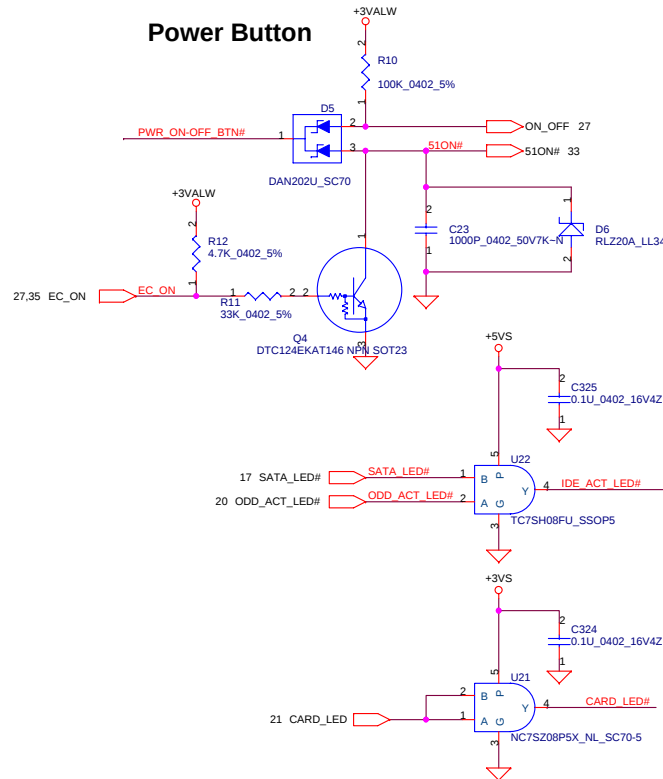
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2006/12/01				Title				USB Port			
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LA-3221P				0.1				Date			
Friday, January 06, 2006				Sheet				29 of 43			



note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



Power Button

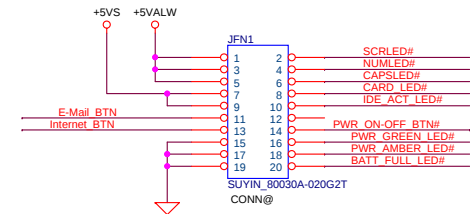


27 SCRLD#
27 NUMLED#
27 CAPSLED#

27 E-Mail_BTN
27 Internet_BTN

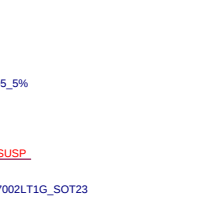
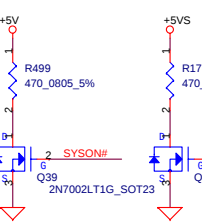
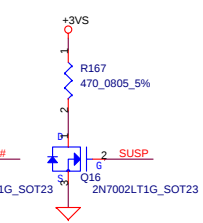
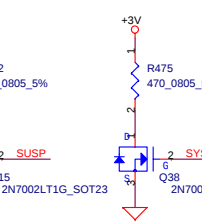
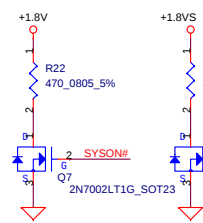
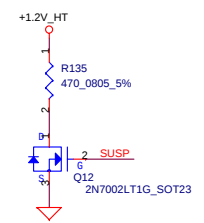
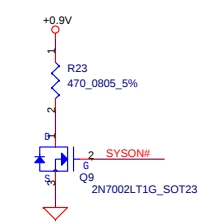
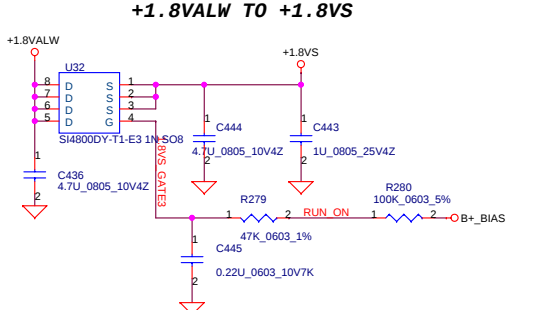
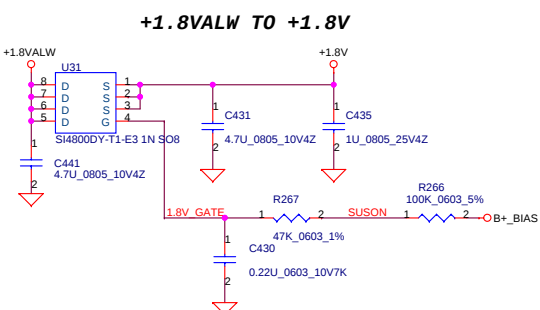
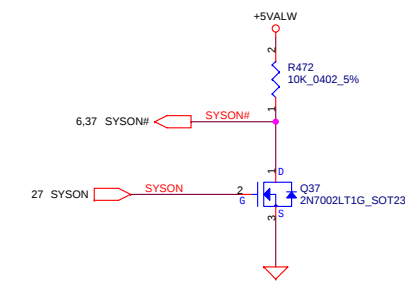
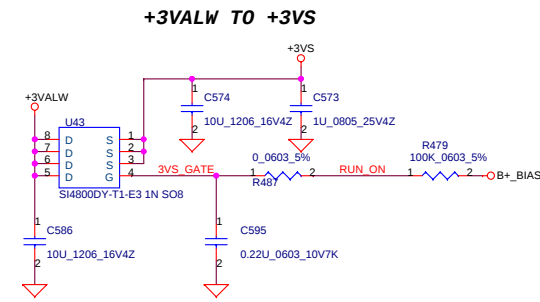
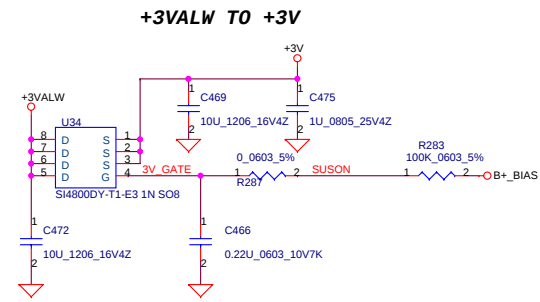
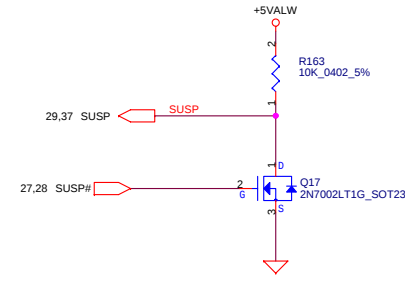
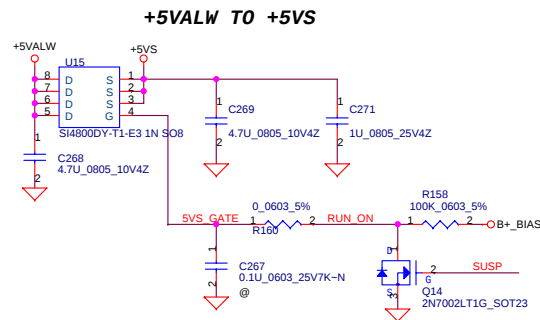
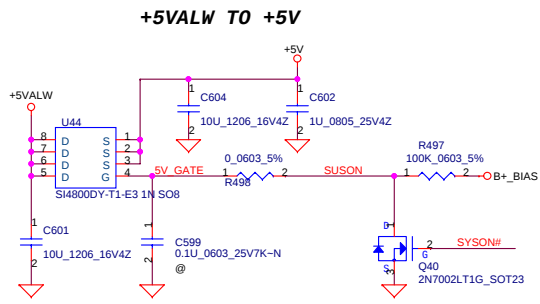
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14.27 PWR_AMBER_LED#

14.27 BATT_FULL_LED#

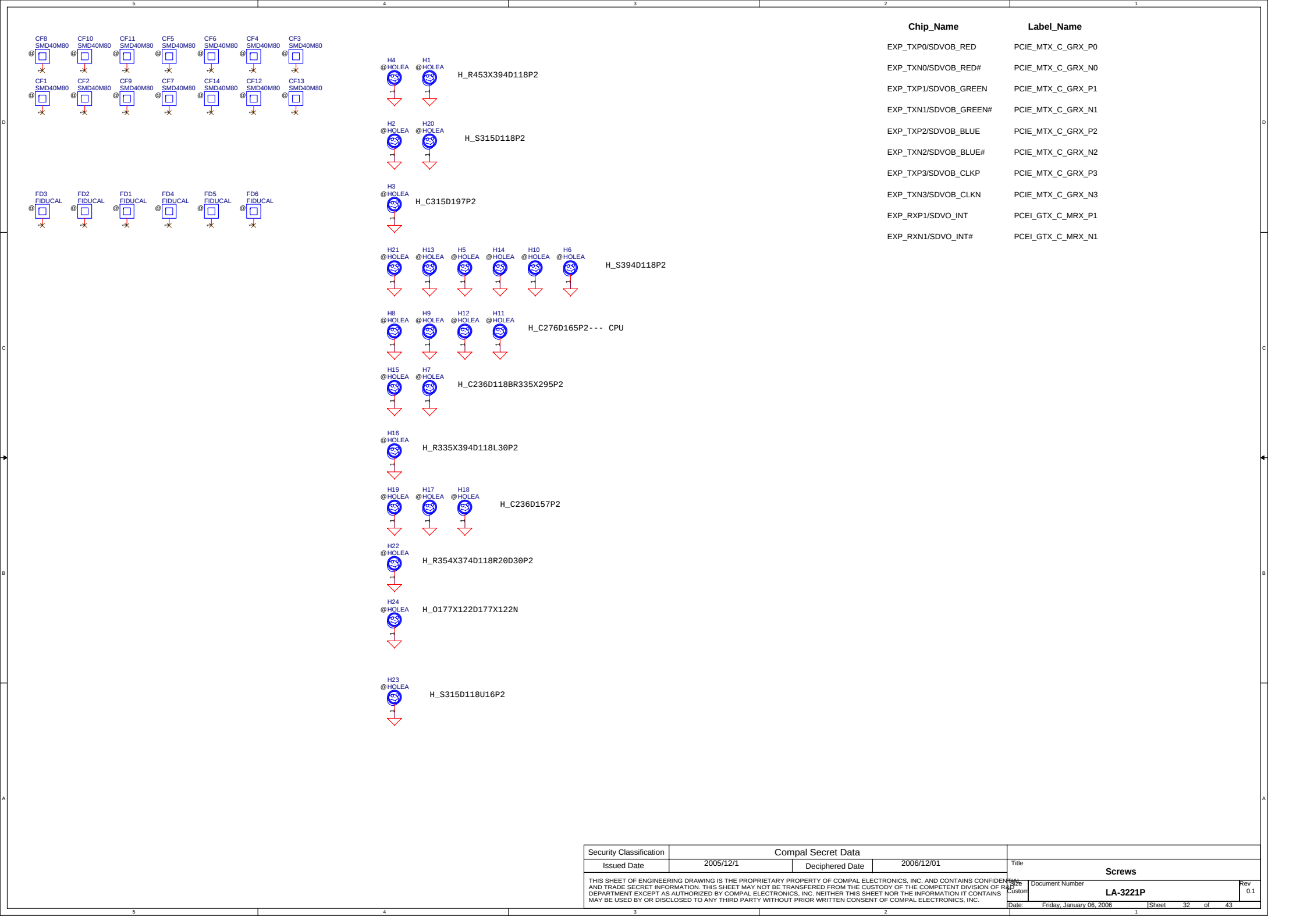


E-Mail_BTN @C625 100P_0402_25V8K
Internet_BTN @C621 100P_0402_25V8K
SCRLD# @C617 100P_0402_25V8K
NUMLED# @C615 100P_0402_25V8K
CAPSLED# @C618 100P_0402_25V8K
CARD_LED# @C624 100P_0402_25V8K
IDE_ACT_LED# @C619 100P_0402_25V8K
PWR_ON-OFF_BTN# @C623 100P_0402_25V8K
PWR_GREEN_LED# @C614 100P_0402_25V8K
PWR_AMBER_LED# @C622 100P_0402_25V8K
BATT_FULL_LED# @C616 100P_0402_25V8K

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				PWR_OK/BTN			
				Document Number		Rev	
				LA-3221P		0.1	
				Date:		Friday, January 06, 2006	
				Sheet		30 of 43	

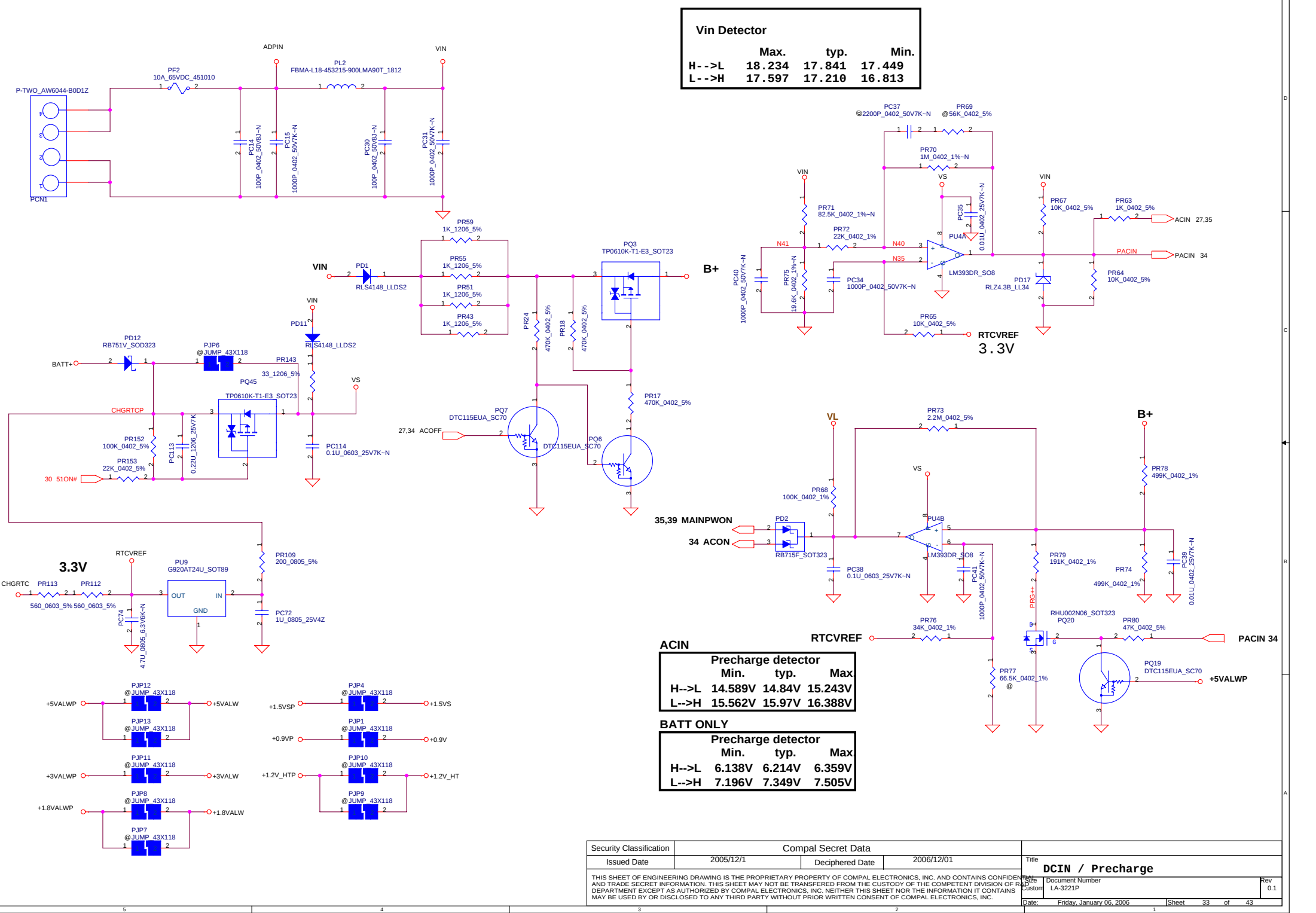


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				LA-3221P	0.1
Date: Friday, January 06, 2006				Sheet	31 of 43



Chip_Name	Label_Name
EXP_TXP0/SDVOB_RED	PCIE_MTX_C_GRX_P0
EXP_TXN0/SDVOB_RED#	PCIE_MTX_C_GRX_N0
EXP_TXP1/SDVOB_GREEN	PCIE_MTX_C_GRX_P1
EXP_TXN1/SDVOB_GREEN#	PCIE_MTX_C_GRX_N1
EXP_TXP2/SDVOB_BLUE	PCIE_MTX_C_GRX_P2
EXP_TXN2/SDVOB_BLUE#	PCIE_MTX_C_GRX_N2
EXP_TXP3/SDVOB_CLKP	PCIE_MTX_C_GRX_P3
EXP_TXN3/SDVOB_CLKN	PCIE_MTX_C_GRX_N3
EXP_RXP1/SDVO_INT	PCEI_GTX_C_MRX_P1
EXP_RXN1/SDVO_INT#	PCEI_GTX_C_MRX_N1

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Issued Date	2005/12/1	Deciphered Date	2006/12/01	Screws	
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				Friday, January 06, 2006	0.1
				Sheet 32 of 43	



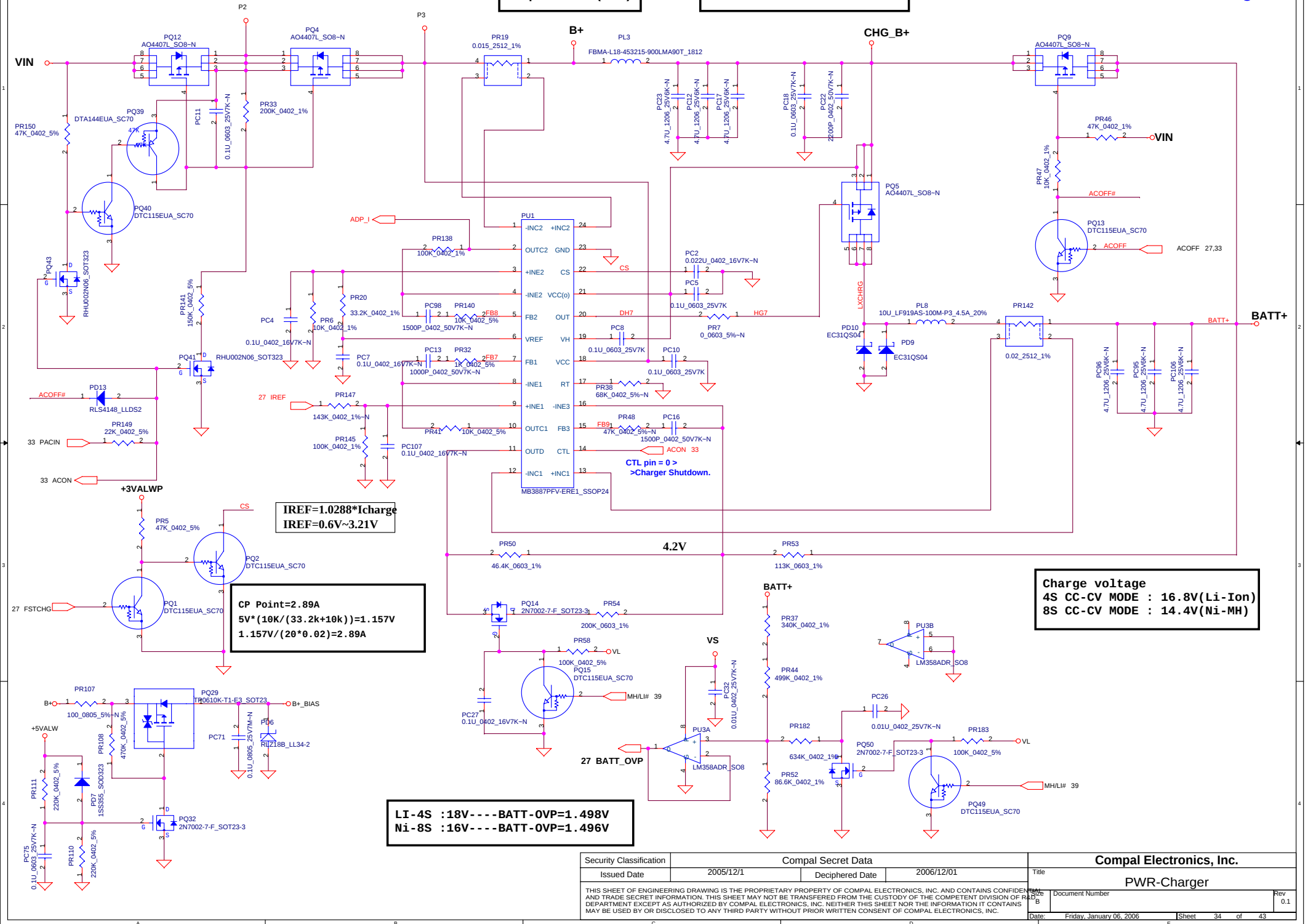
Vin Detector			
	Max.	typ.	Min.
H-->L	18.234	17.841	17.449
L-->H	17.597	17.210	16.813

ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

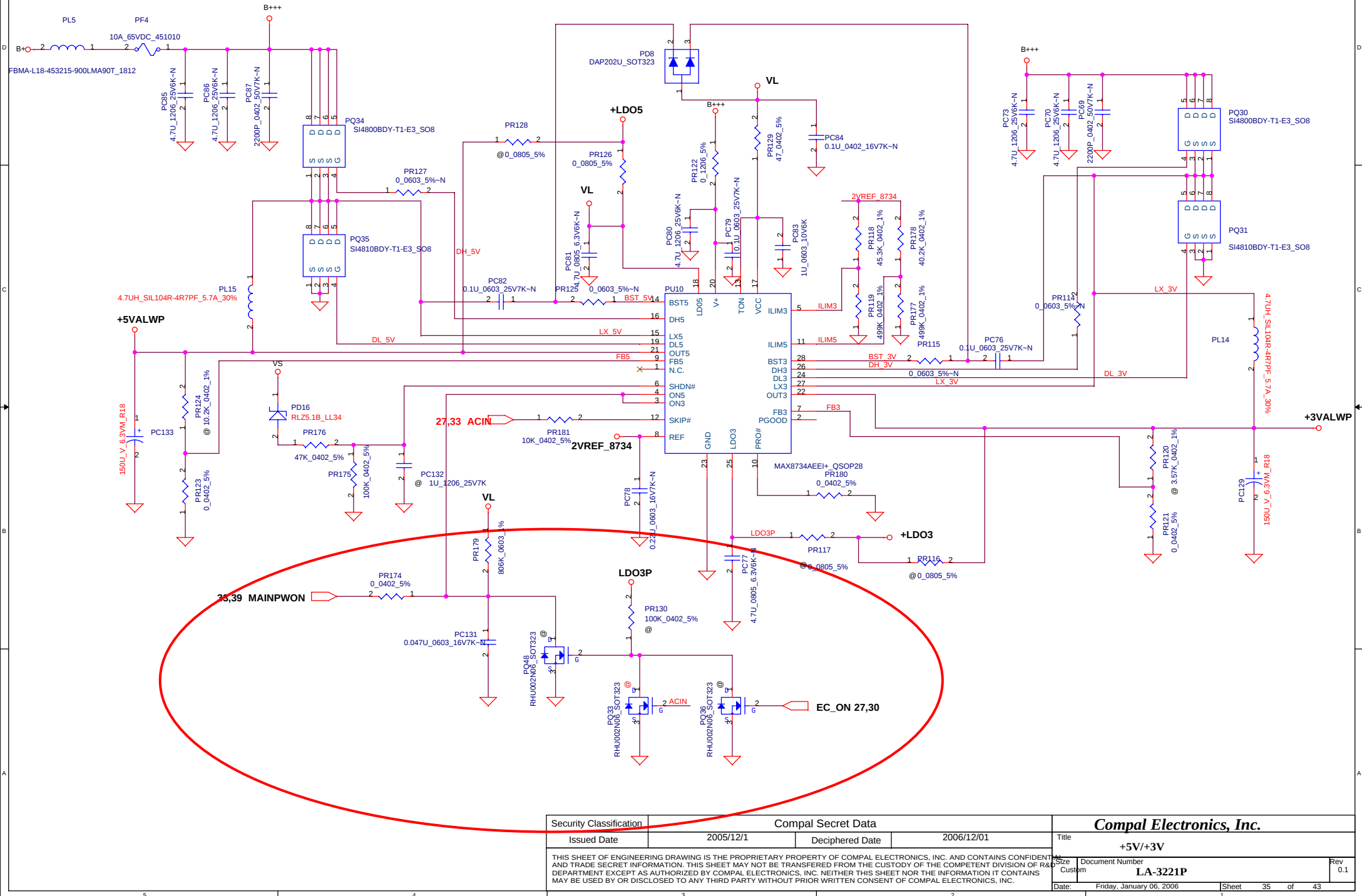
BATT ONLY			
Precharge detector			
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

$$I_{adp}=0\sim 3.16A(60W)$$

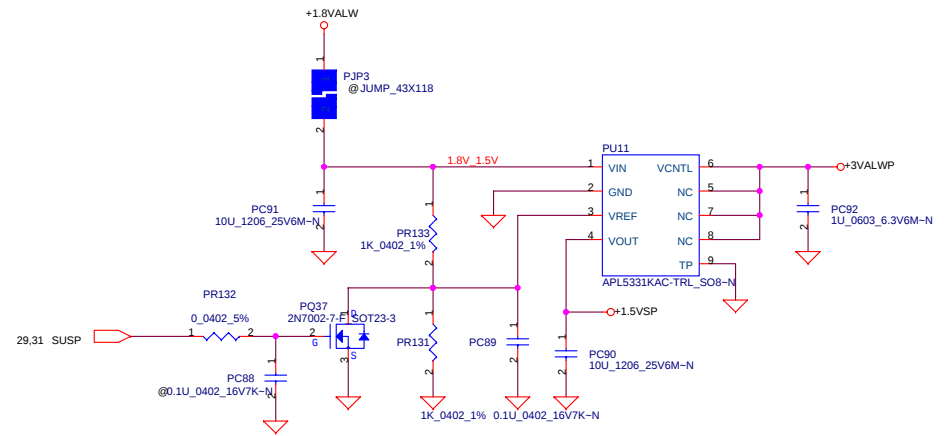
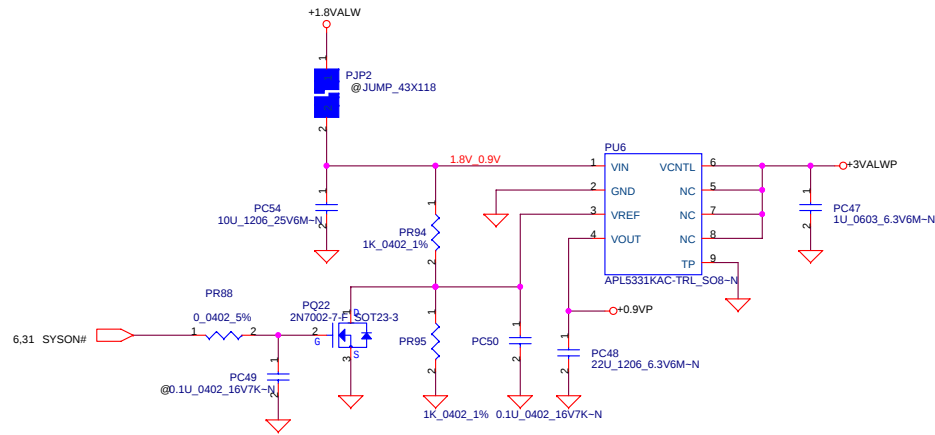
$$F_{osc}=14100/R_t=14100/47=300KHz$$



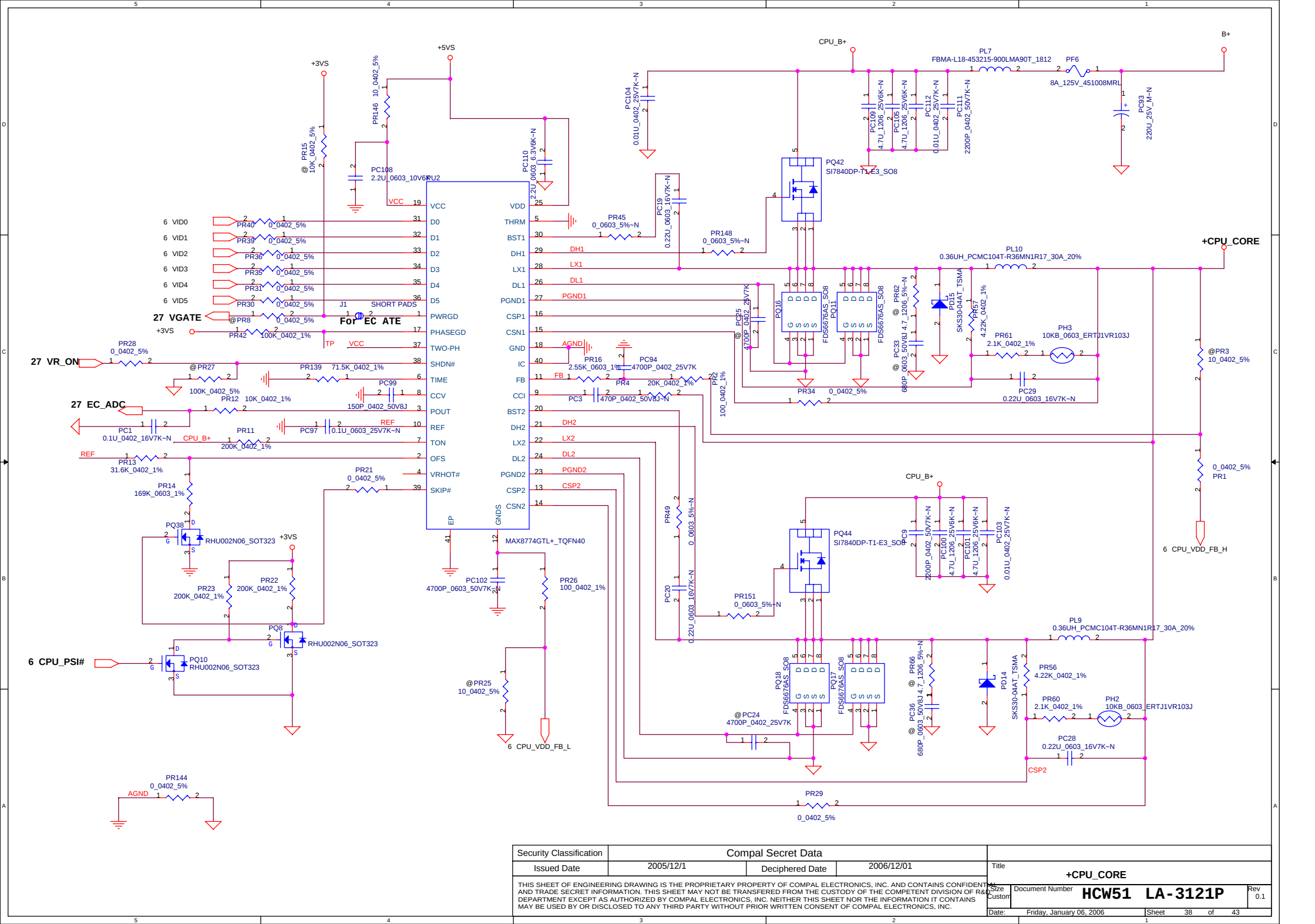
+3.3VALWP/+5VALWP



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				Date	Friday, January 06, 2006
				Sheet	35 of 43
				Rev	0.1

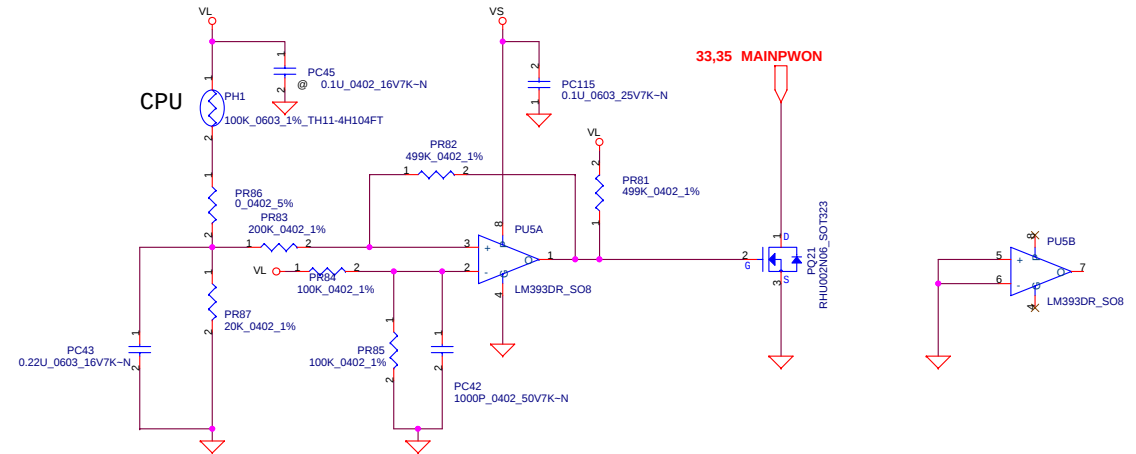
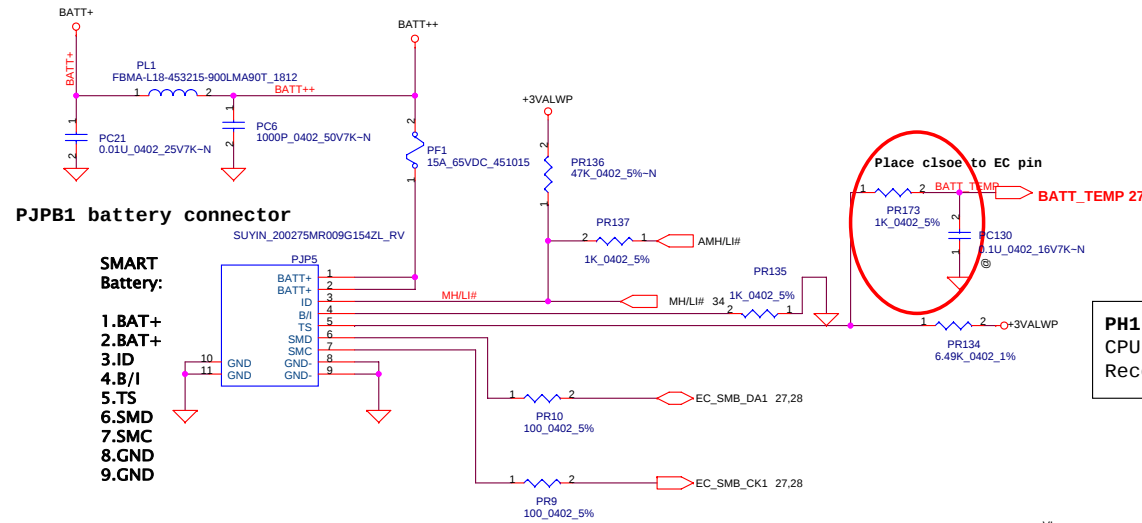


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Date: Friday, January 06, 2006				Sheet 37 of 43



Security Classification		Compal Secret Data			
Issued Date	2005/12/1	Deciphered Date	2006/12/01	Title	+CPU_CORE
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				Date: Friday, January 06, 2006	Sheet 38 of 43

Battery Connect/OTP



Security Classification	Compal Secret Data			Title
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Date:	Friday, January 06, 2006	Sheet	39 of 43	

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							
5							
6							
7							
8							
10							
11							
12							
13							
14							
15							
16							
17							

Next: PR238, PC202, PQ56, PD42, PJP21

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Compal Electronics, Inc.			
Title EE-PIR			
Drawing Number LA-3221P		Rev 0.1	
Date: Friday, January 06, 2006		Sheet 41 of 43	

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		CPU bypass Cap change to Proadlizer 1200uF.		7			
2		Change Felica connector package.		28	From 4pin change to 6 pin.		
3		Change R536 value.		24	R536 change to 10K ohm		
4		Change net (WLAN_ACT) from pin 3 to pin46.		26	Add R516, R538		
5		RS485MC only support 2 lane PCI-E		10,15	A-LINK 4X---->2X Change PCI-E port 2,3 ---->0,1		
6		Part reference rename for layout		All	Part reference change		
7		To support WOL on S3/S4/S5		23	Change the power rail from +3V to +3VALW.		
8		Change R185 BOM structure		23			
9							

