SHANGHAI 100
BTK20 LA-1521 Schematics Document

REV 1.0A
PVT2

INTEL Mobile P4 uFCBGA/uFCPGA Northwood Celeron
MCH-M(845MZ) + ICH3-M + M6-C(16MB VRAM)

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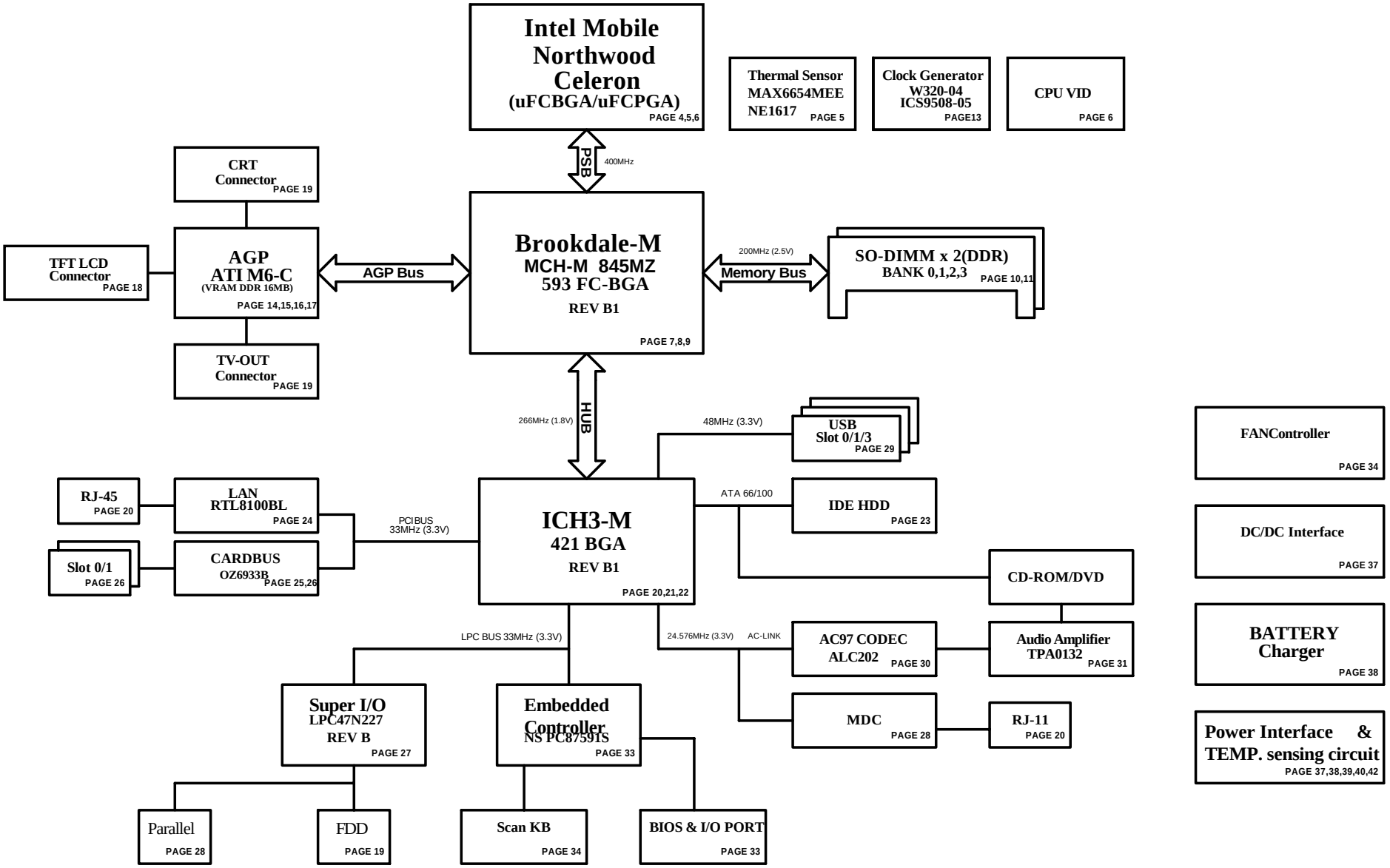
SHANGHAI 100
BTK20 LA-1521 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON*" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB

EC SM Bus1 address

Device	Address
Smart Battery	0001 011Xb
EEPROM(24C16/02)	1010 000Xb
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX6654MEE	1001 110Xb
Smart Battery	0001 011Xb
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1 (EVT/DVT PHASE)

Date	Page	Description
07/06 2002	07	ADD R441,R442 AND C622 FOR "+AGP_REF"
07/06 2002	14	Change R137 Pin2 power name from "+AGP_NBREF" to "+AGP_VGAREF" for can't boot issue.
07/06 2002	16	Change R181 Pin2 power plane from "+2.5V" to "+2.5V_VGA" for leakage.
07/06 2002	17	DEL R43,R255,R40 and J1.
07/06 2002	24	ADD Q47 FOR LAN POWER "+2.5VLAN". ADD Q48 and Q49 FOR LAN Layout Rule.
07/06 2002	27	JP8 Pin25 Create "FDD_READY#" for W/O FDD (GI BTO).
07/06 2002	30	Change R122 to 10K, R121 to 2.4K for MDC Noise. Change R340 to 100K_1%, R347 to 33K_1% for Back-Grand Noise. Change R159 to 0, C220 to 0 for Vendor(Realtek) Recommend.
07/06 2002	32	ADD R443, JP22 FOR EC JTAG Connector.
07/06 2002	34	Change JP5 form 20pins to 26pins type.
07/06 2002	36	DEL R352,R277,R243,R287,R301 and R355.
07/06 2002	37	Change PR15 pin2 power name form "+2.5VREF" to "2.5REF"
07/12 2002	05	ADD Q50,Q51,Q52,R445 and R446 for "H_THERMTRIP#" Function.
07/12 2002	39	ADD PF3 for "NA" of Battery type.
07/12 2002	33	Update EC BOARD ID: 001 for PVT1.(Remove R331, Add R327)

REV 0.2 (PVT1 PHASE)

Date	Page	Description
07/26 2002	05	Improved Q50,Q51,Q52,R445 and R446 for "H_THERMTRIP#" Function. Change R446 pin1 power from "+5VS" to "+CPU_CORE" Change R445 pin1 power from "+5VS" to "+5V"
07/26 2002	24	Update BOM by DEL Q47, ADD R106 for LAN unstable.
07/26 2002	33	Update EC BOARD ID: 011 for PVT2.(Remove R325, Add R324)

REV 1.0

Date	Page	Description
07/30 2002	33	Update EC BOARD ID Description :EC_BID2 <-> EC_BID0.

REV 1.0A (PVT2 PHASE)

Date	Page	Description

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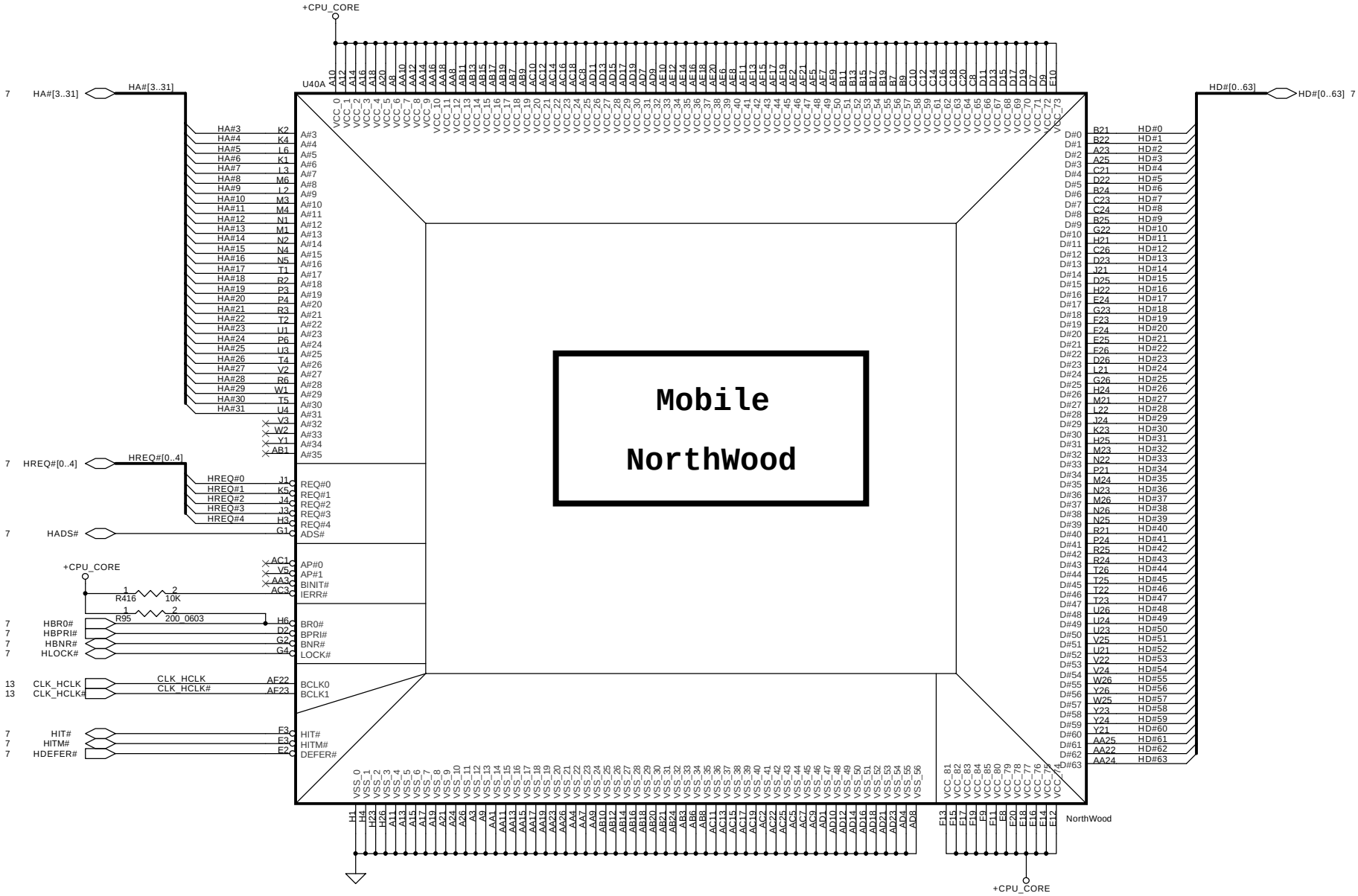

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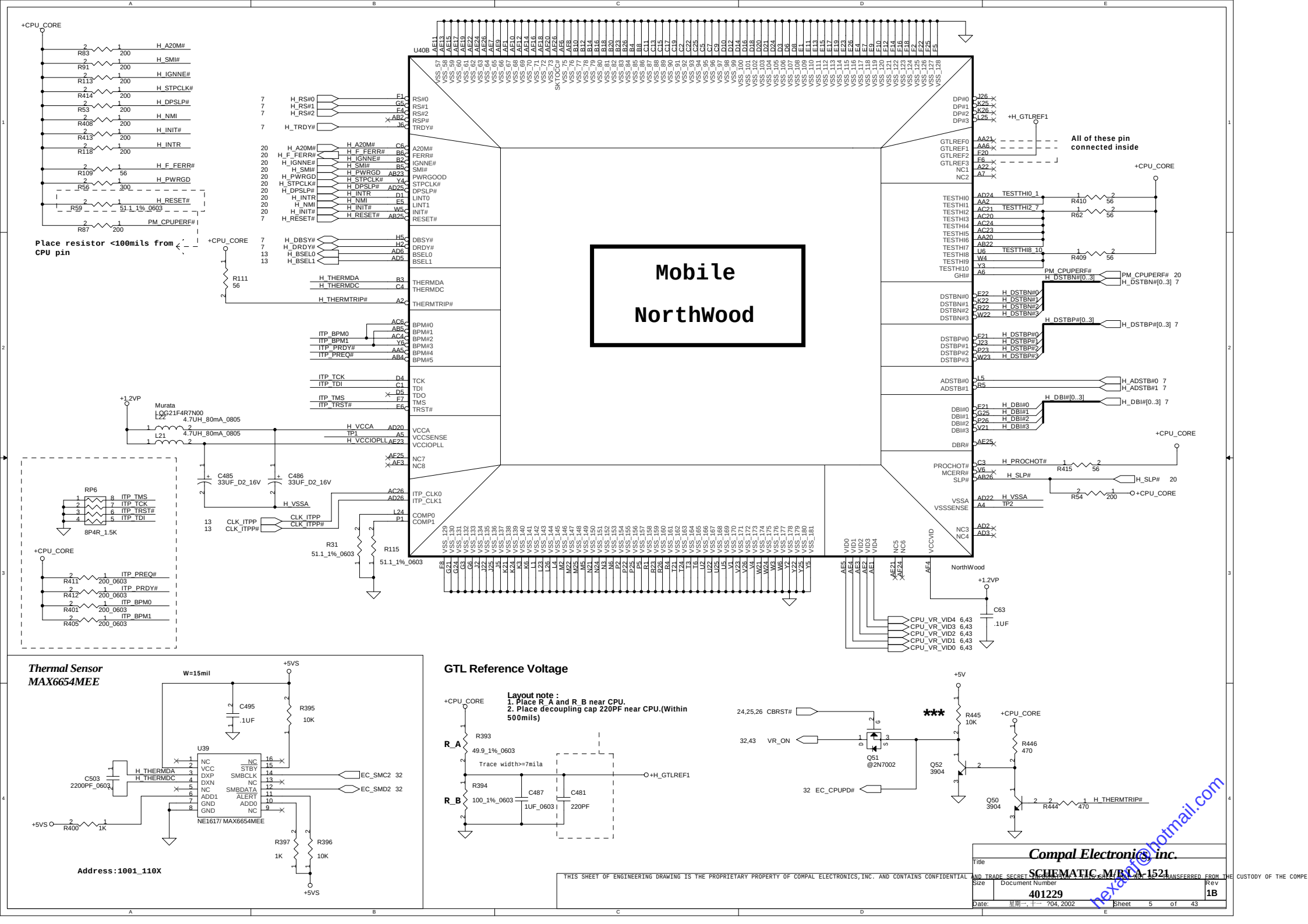

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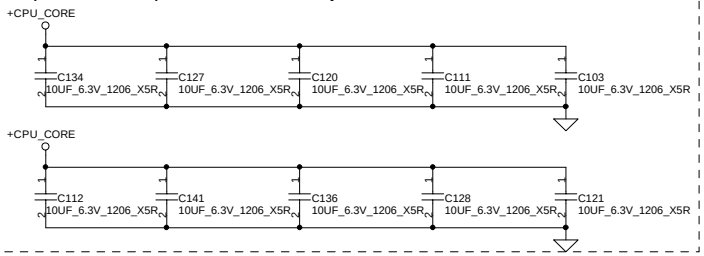
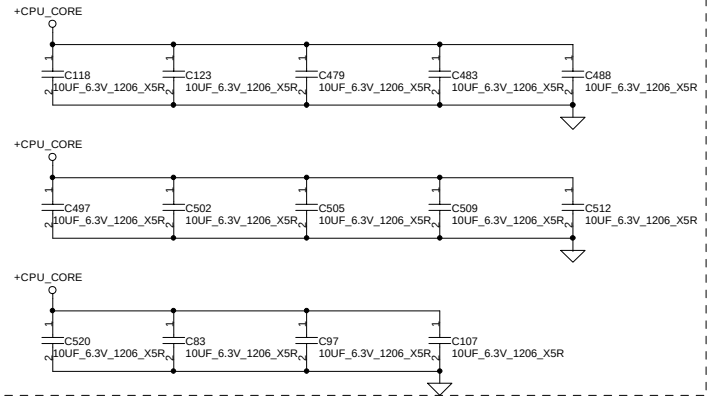
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

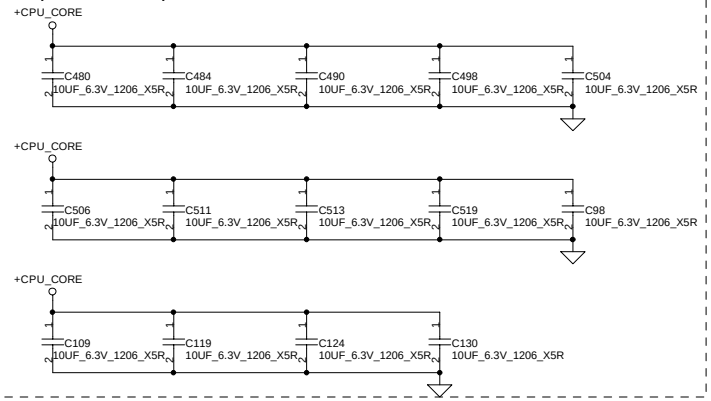
Please place these cap in the socket cavity area



Please place these cap on the socket north side



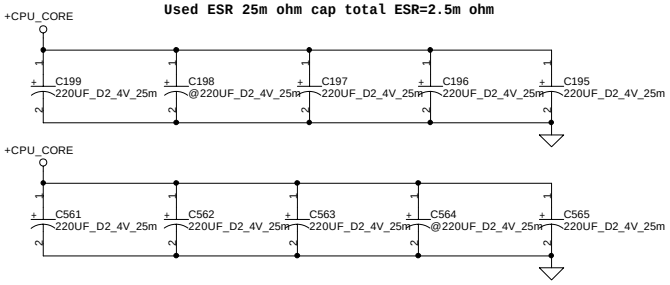
Please place these cap on the socket south side

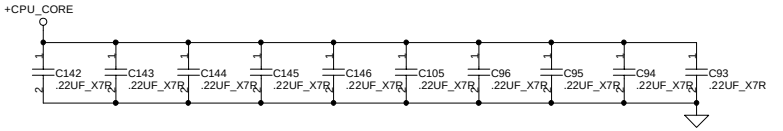


Layout note :

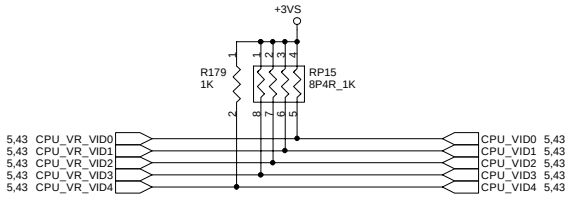
Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm





CPU Voltage ID



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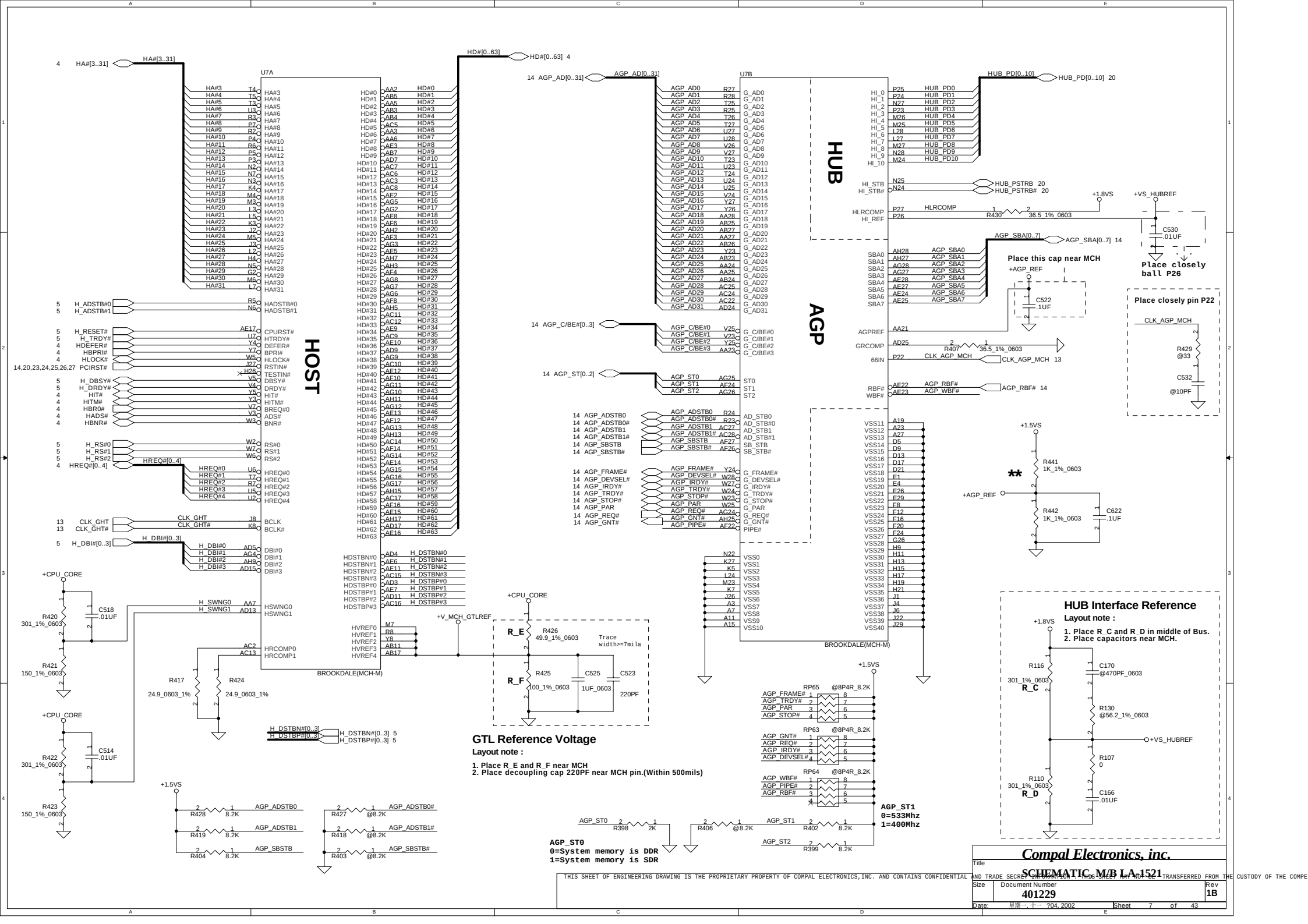

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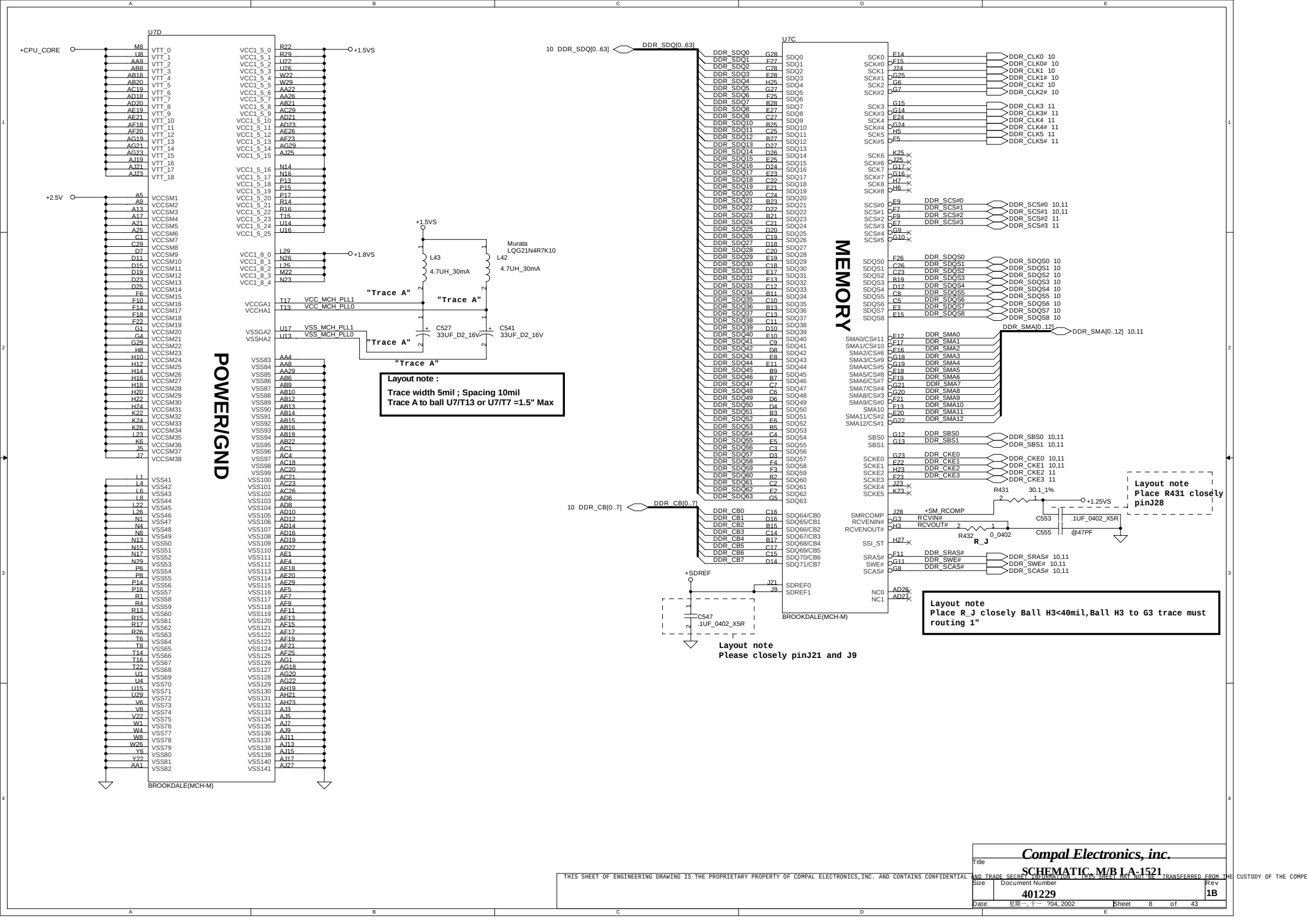

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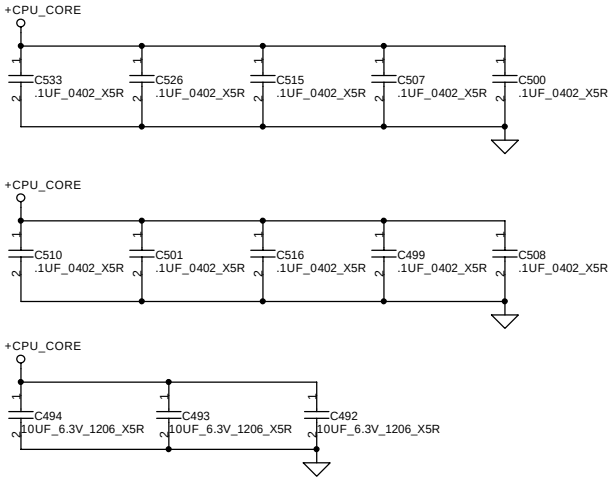
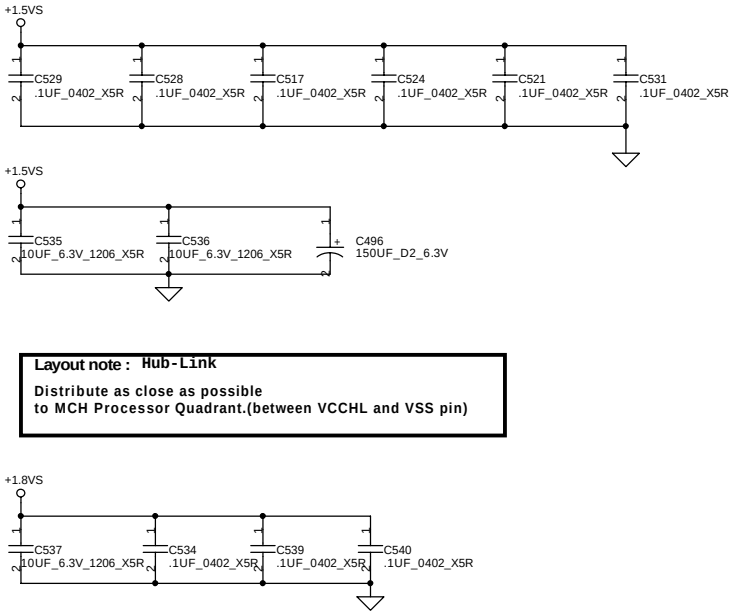
Layout note : Processor system bus

Distribute as close as possible to MCH Processor Quadrant.(between VTTFSB and VSS pin)



Layout note : AGP/CORE

Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)

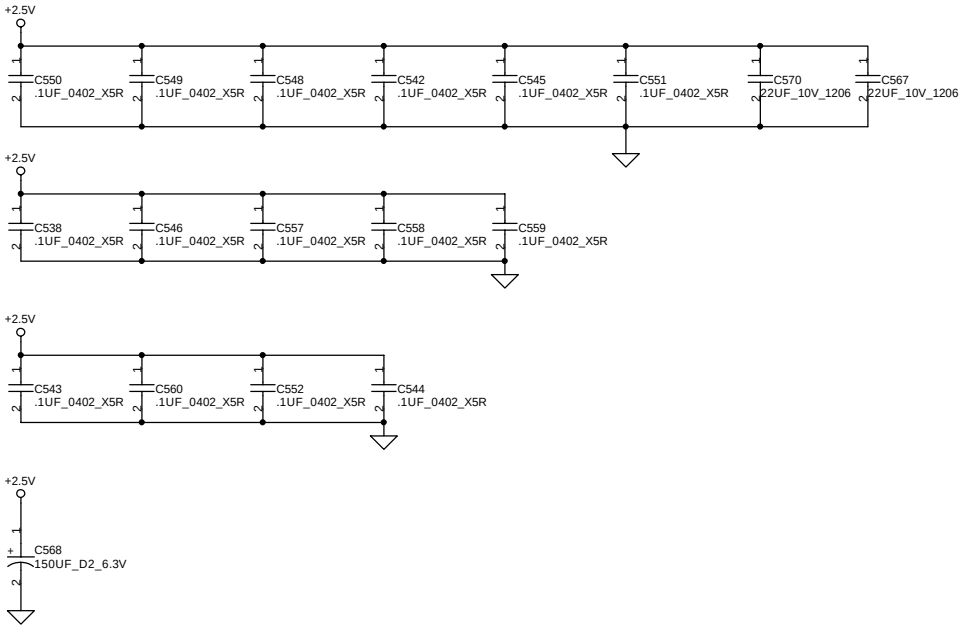


Layout note : Hub-Link

Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)

Layout note : DDR Memory interface

Distribute as close as possible to MCH Processor Quadrant.(between VCCSM and VSS pin)



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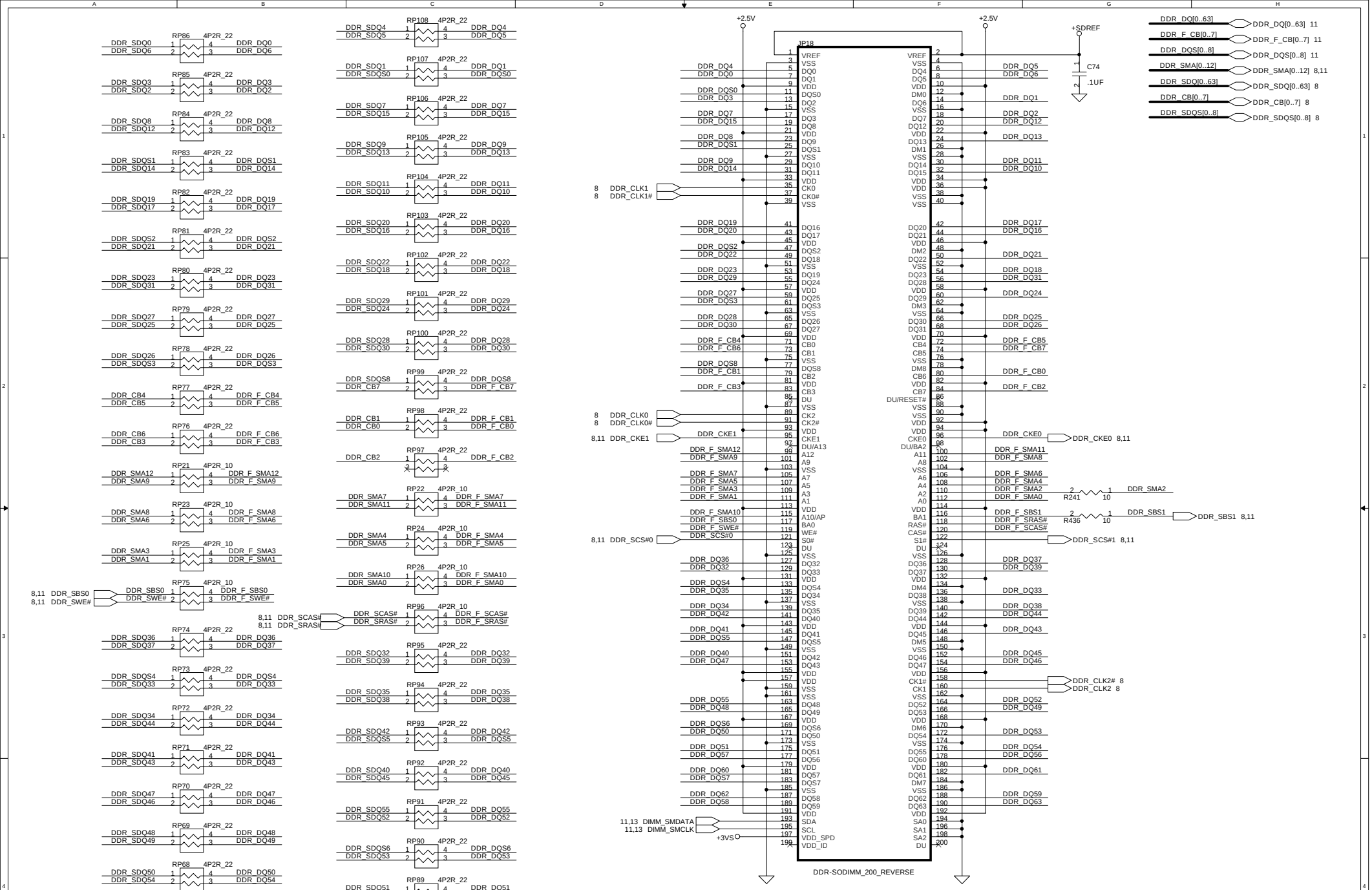

DIMM0 REVERSE H:5.2mm

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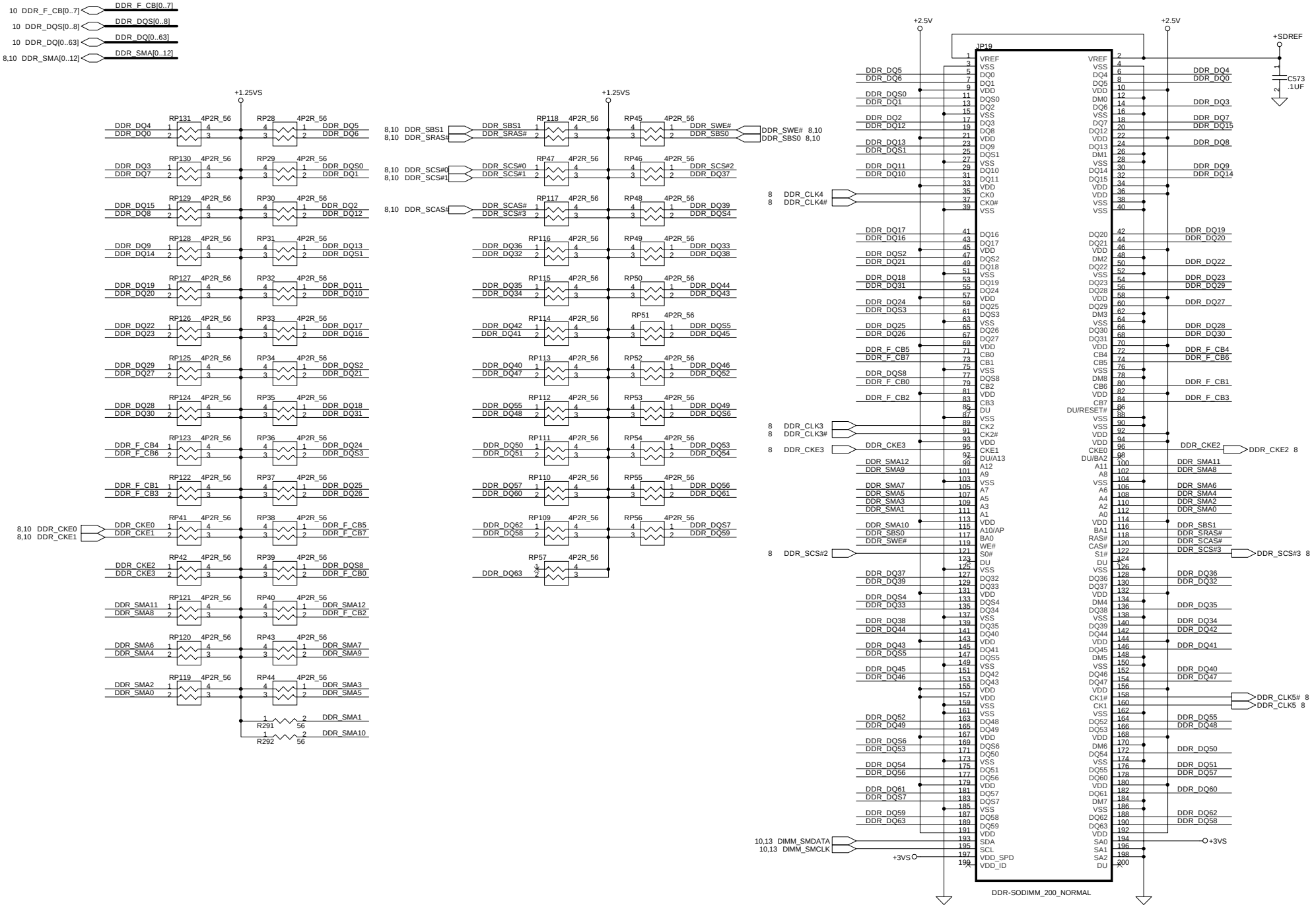

DIMM1 NORMAL H:9.2mm

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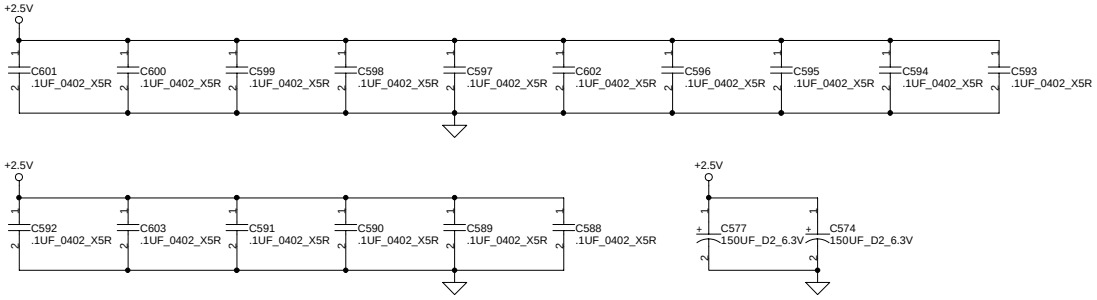
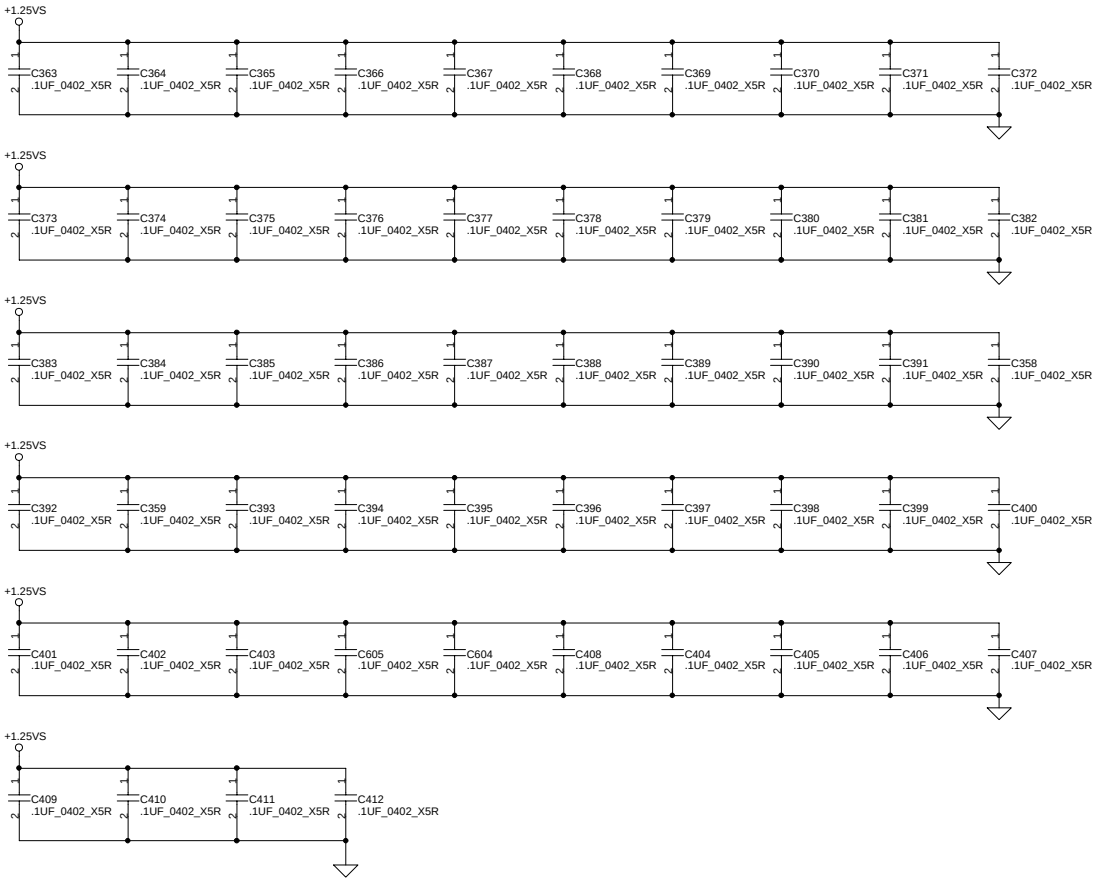
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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SEL1	SEL0	Function
0	0	66Mhz Host CLK
* 0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK

MULT0	Iref
0	5.00mA
1	2.32mA

+3V_CLK = 40mils

+3VS_VDD48M = 10mils

Place Crystal within 500 mils of CK_Titan

caps are internal to CK_TITAN

Y3 14.318MHZ

Please closely pin42

or ICS 9508-05

Place caps. near CK_Titan (U10)

Place resistor near RD1,RD2 ;Trace<=400mils

Place resistor near RD3, RD4 ;Trace<=400mils

Place resistor near RD5, RD6 ;Trace<=400mils

Q19 2N7002

Q20 2N7002

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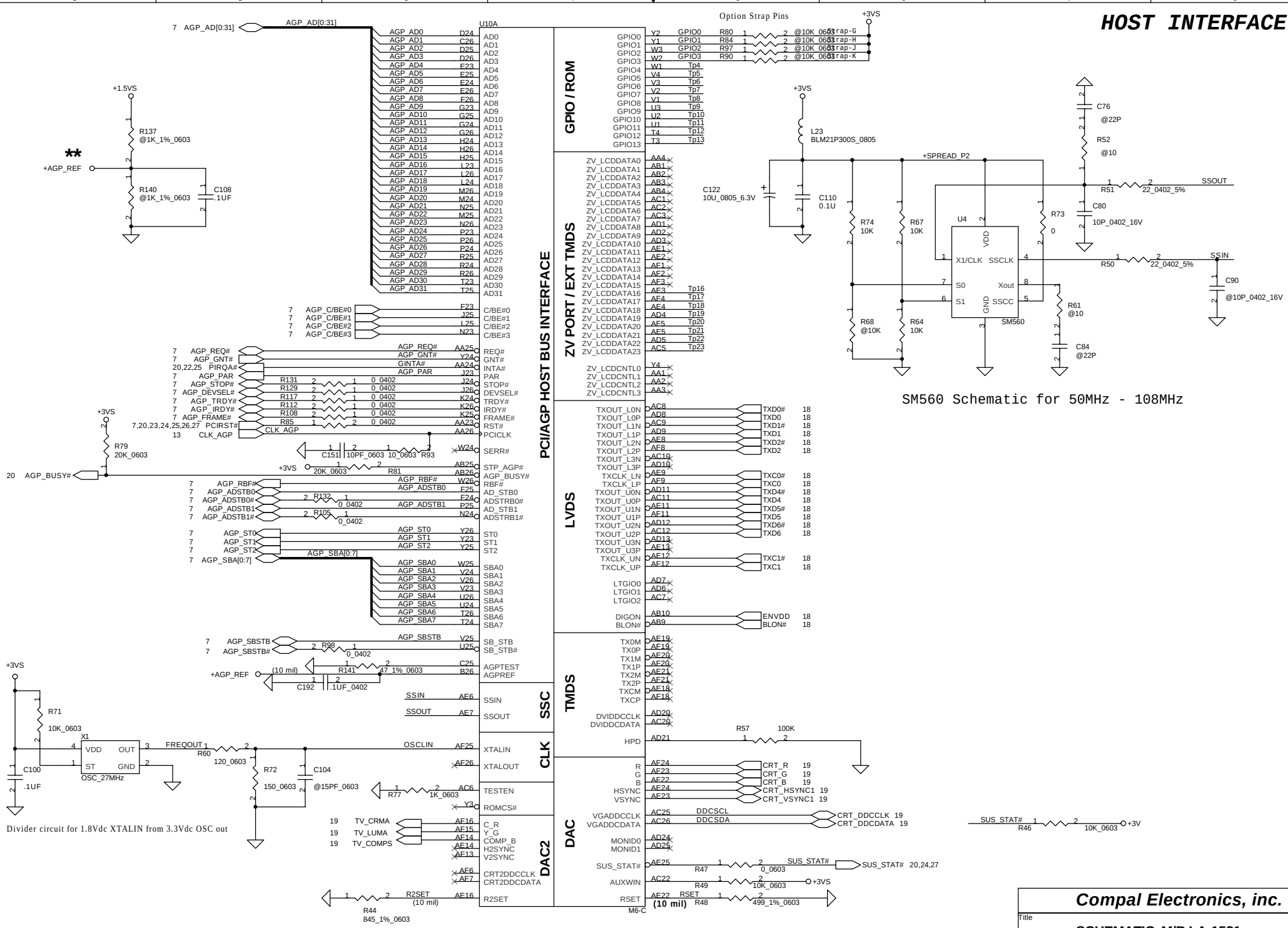
HOST INTERFACE



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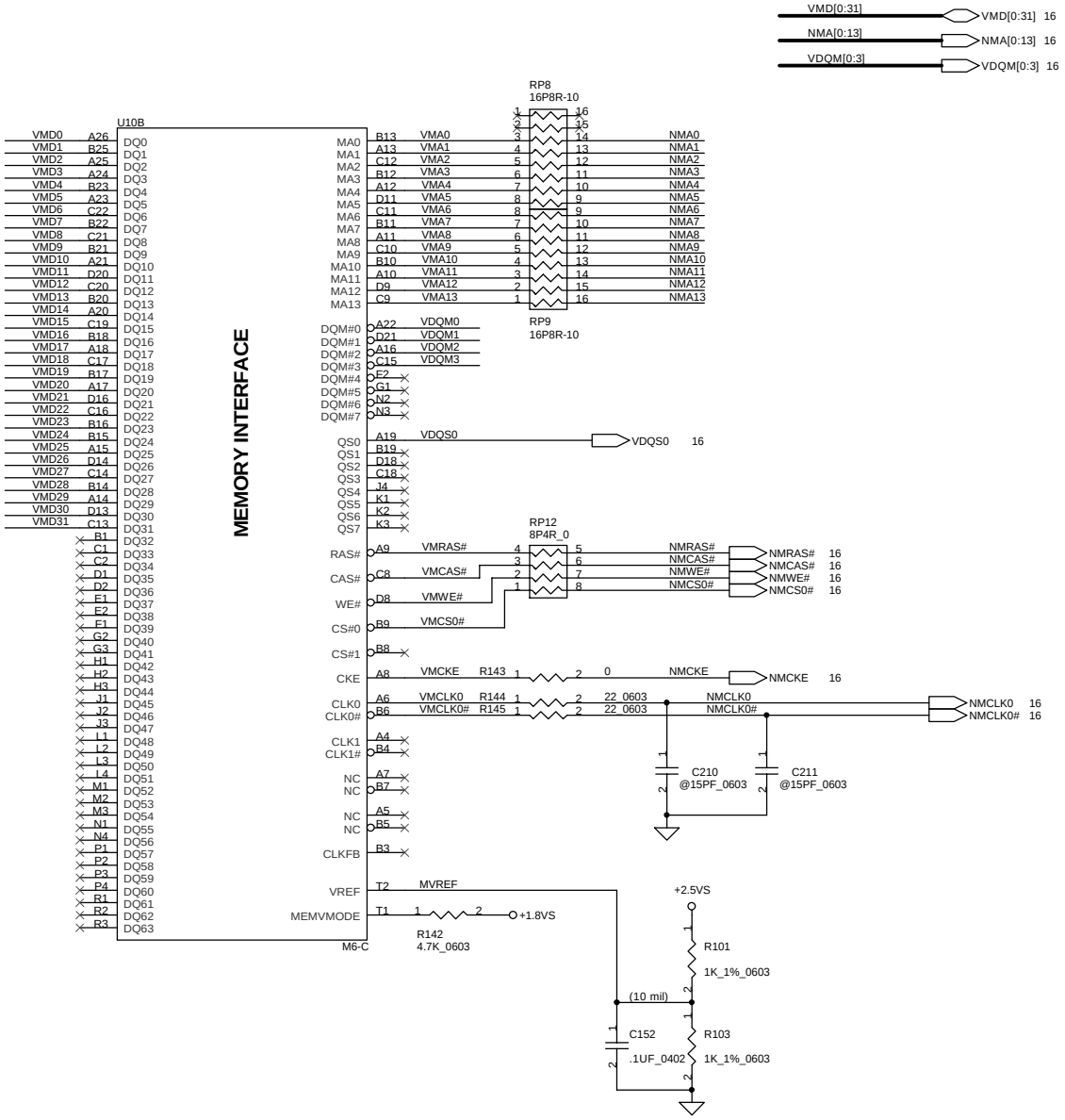
MEMORY INTERFACE



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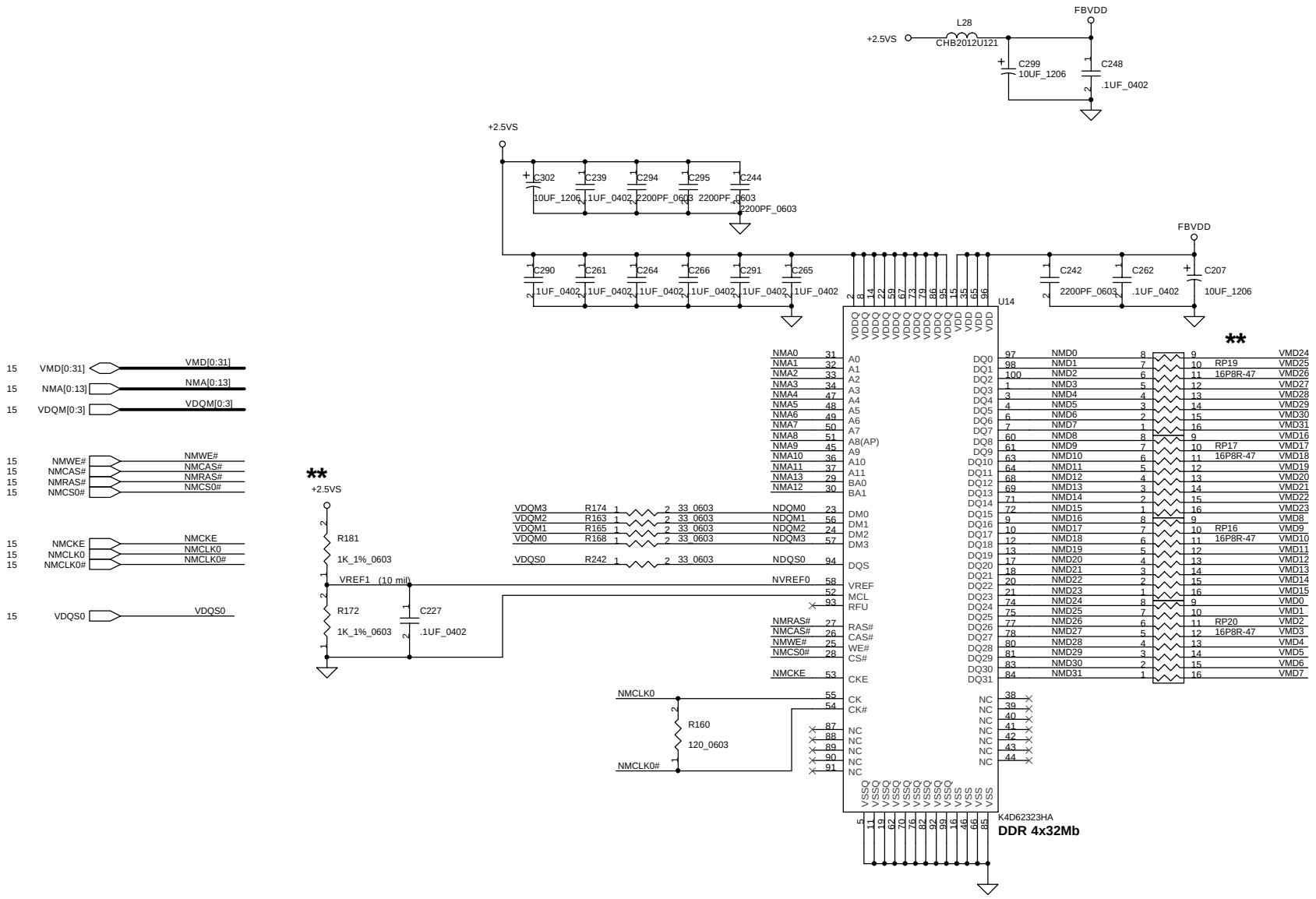
DDR SDRAM 4X32Mb



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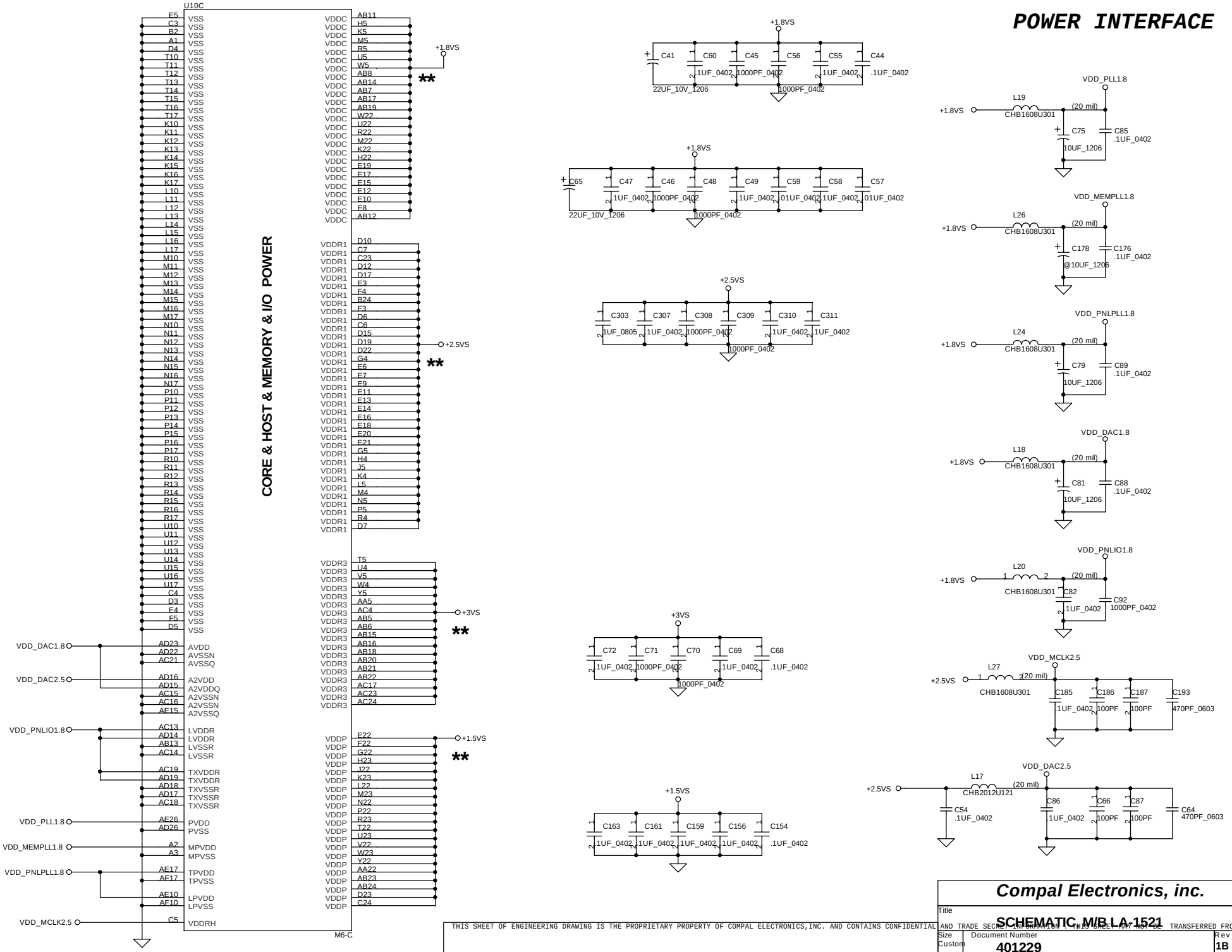
POWER INTERFACE



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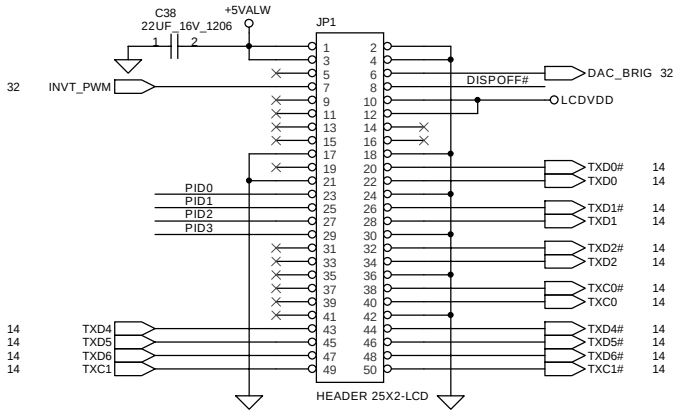
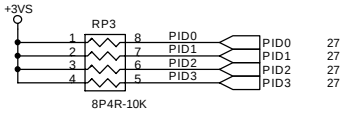
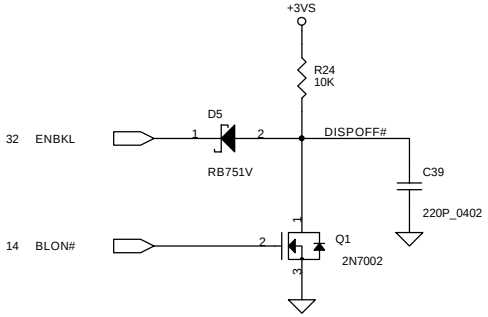
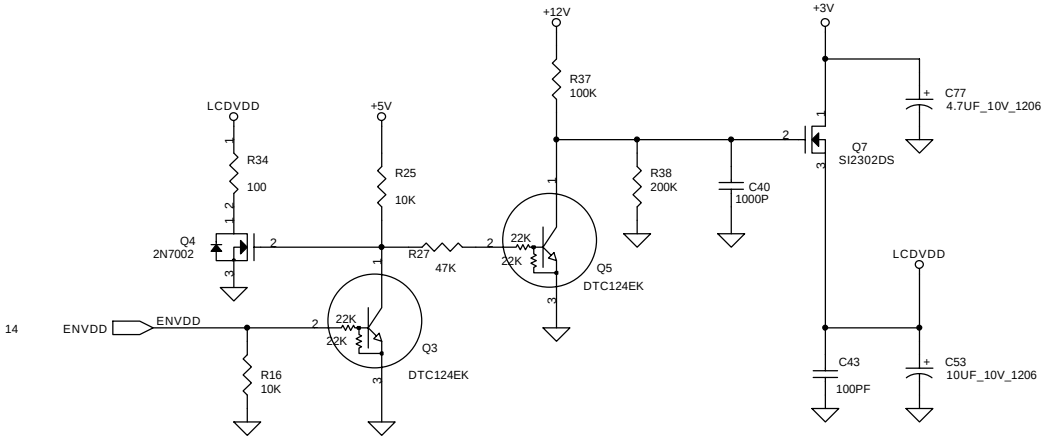
LVDS Connector









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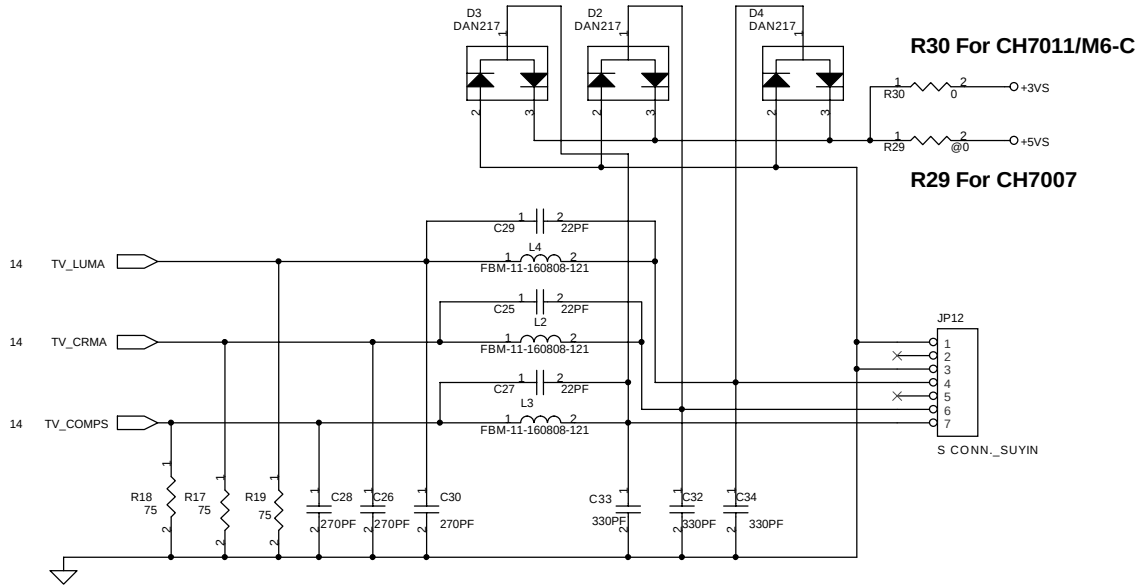
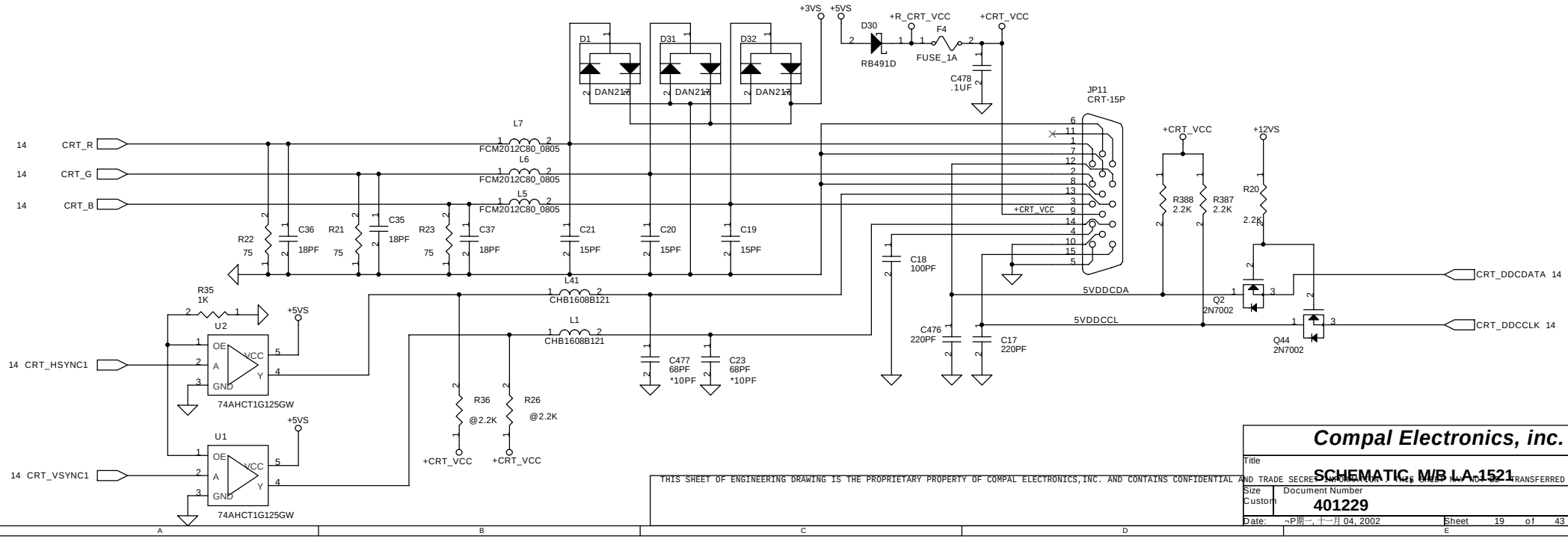
TV_OUT CONNECTOR



CRT CONNECTOR



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ICH3-M (1/2)

Power Management

Geyserville

AC'97 Interface

LPC Interface

unMUX GPIO

Interrupt Interface

PCI Interface

System Managment Interface

CPU Interface

VSS

Clocks

LAN Interface

EEPROM Interface

HubLink Interface

HUB Interface VSwing Voltage

1. Place R_G and R_H in middle of Bus.

HUB Reference Voltage

Place R_K and R_L Closely ICH3

Place closely to ICH3

Close to ICH3-M.

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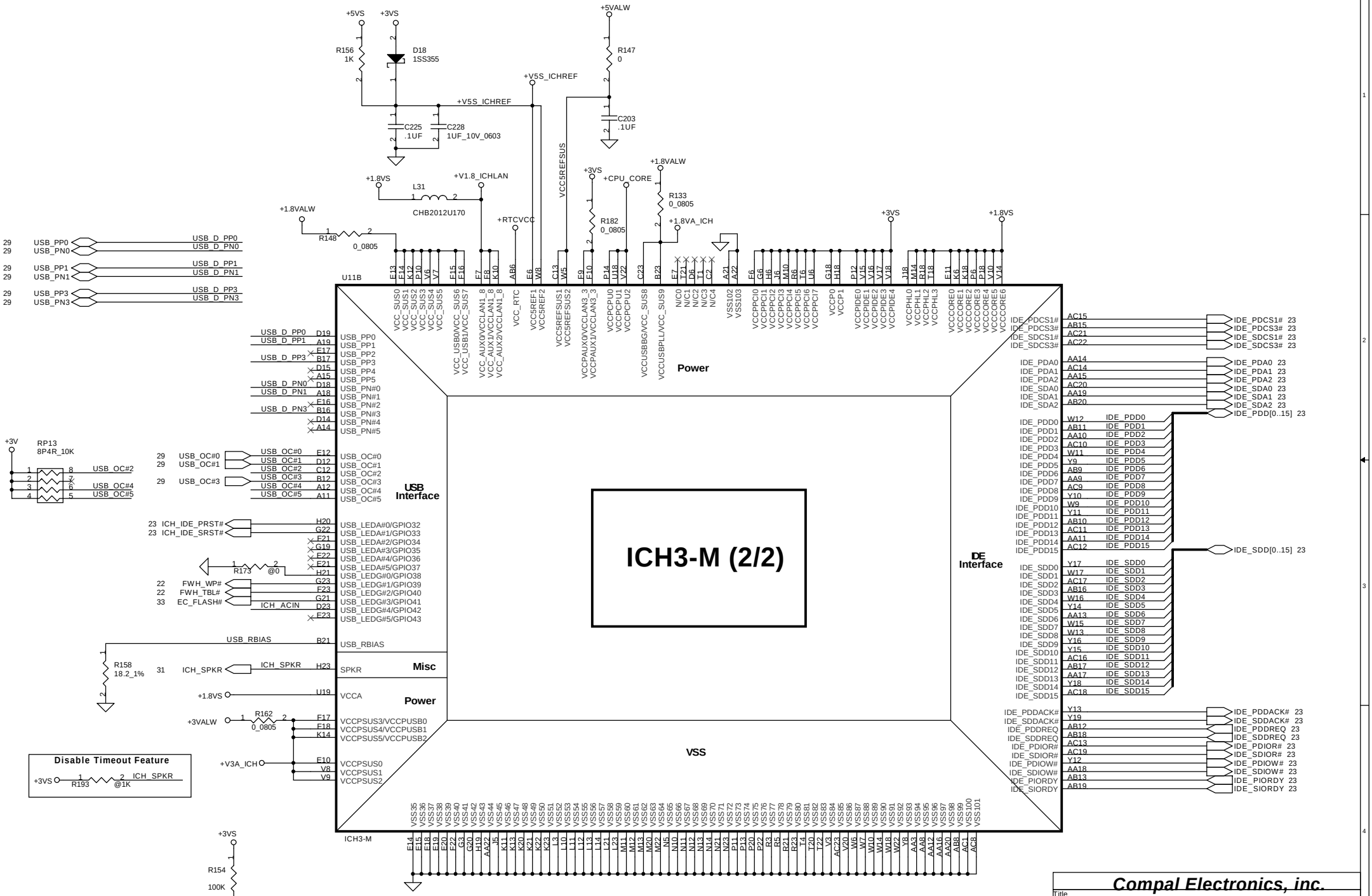

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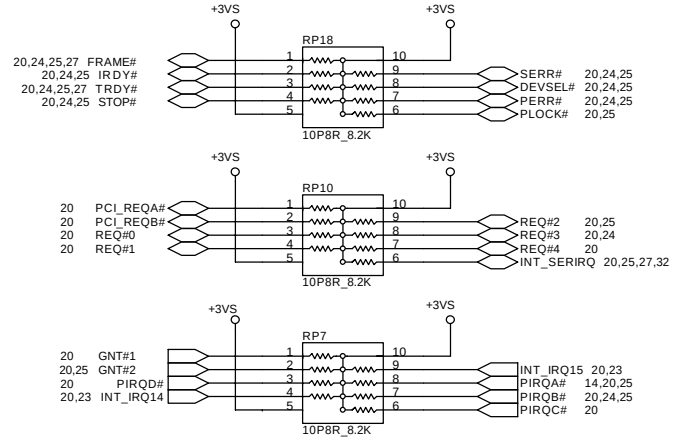
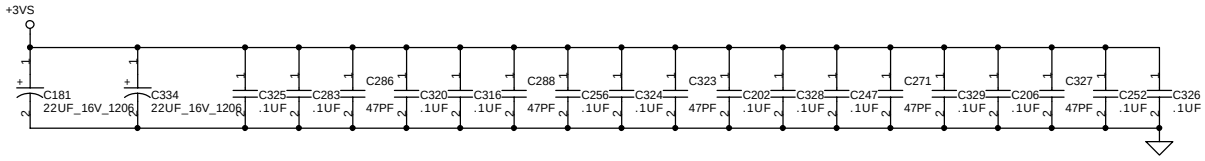
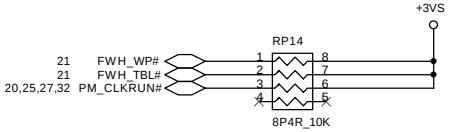
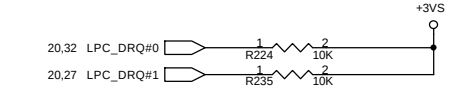
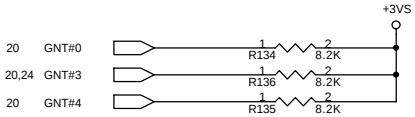
+3VS PULL-UP/BY-PASS



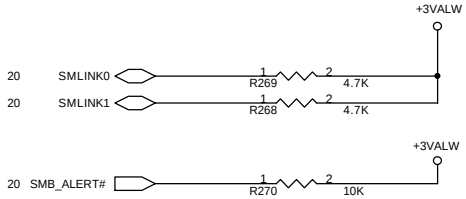


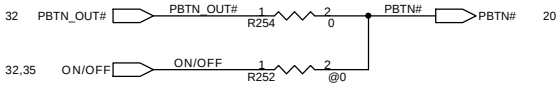


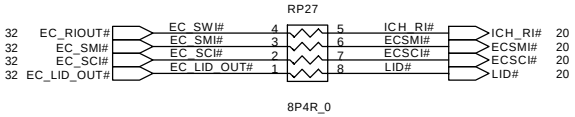


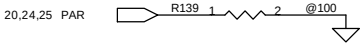


+3VALW PULL-UP

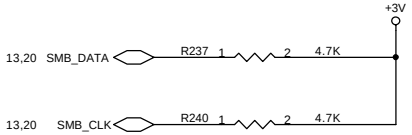






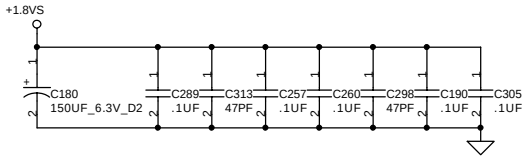


+3V PULL-UP/BY-PASS

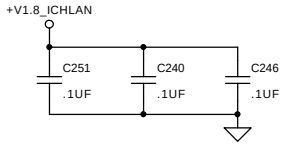


+RTCVCC PULL-UP

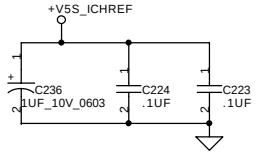
+1.8SV BY-PASS



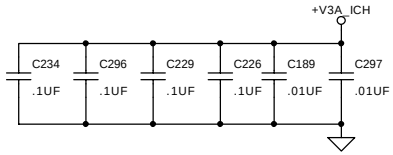
+V1.8S_ICHLAN BY-PASS



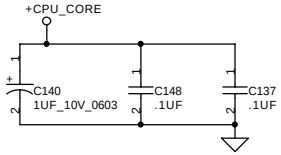
+V5S_ICHREF BY-PASS



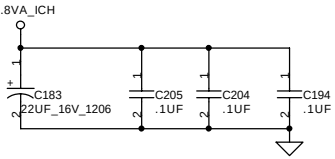
+V3A_ICH BY-PASS



+CPU_CORE BY-PASS



+1.8VA_ICH BY-PASS



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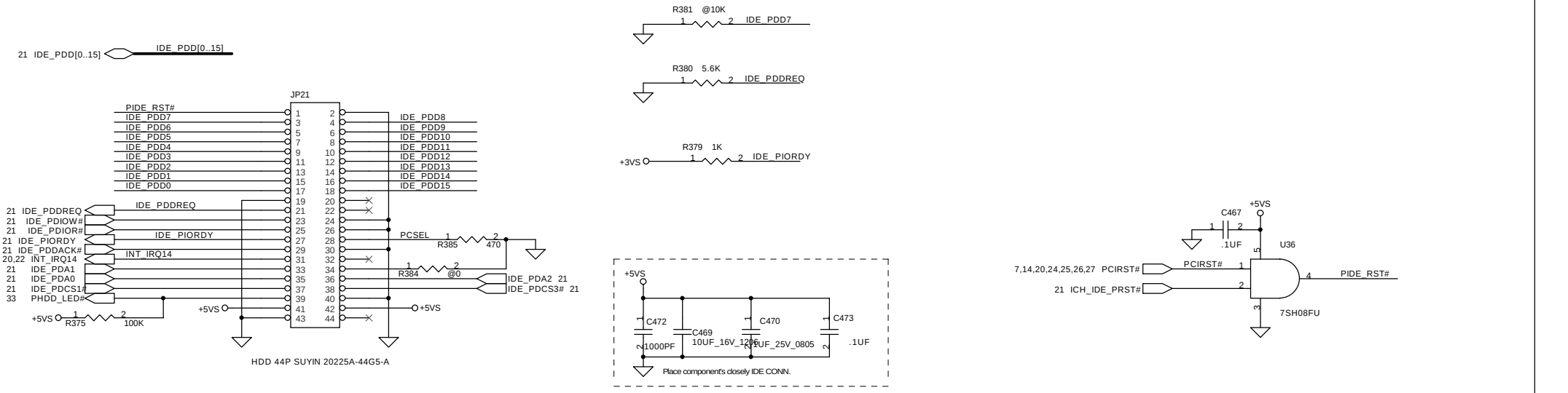
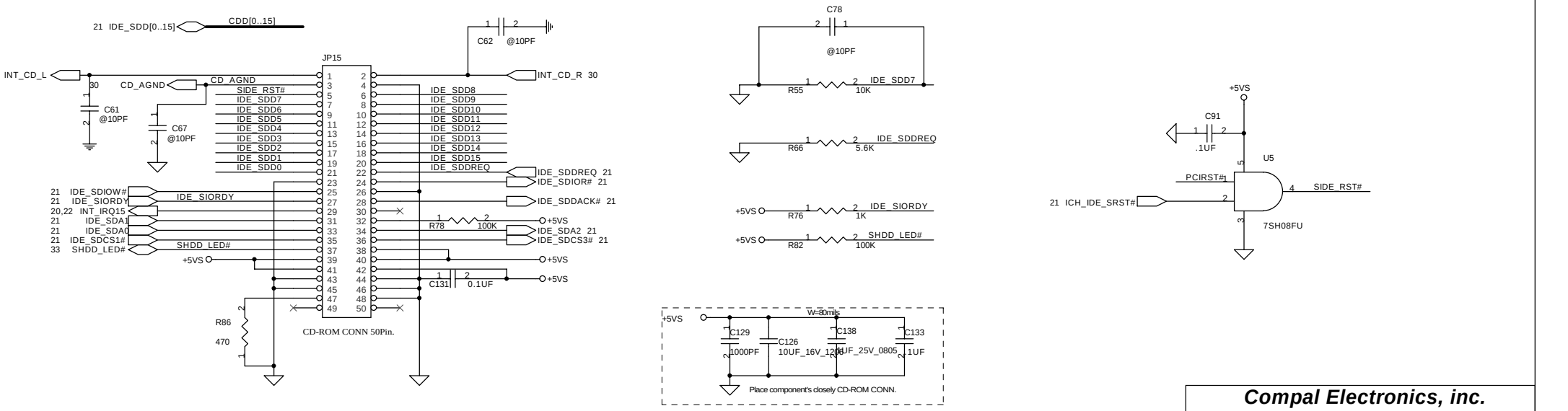
IDE Module CONN.



CD-ROM Module CONN.



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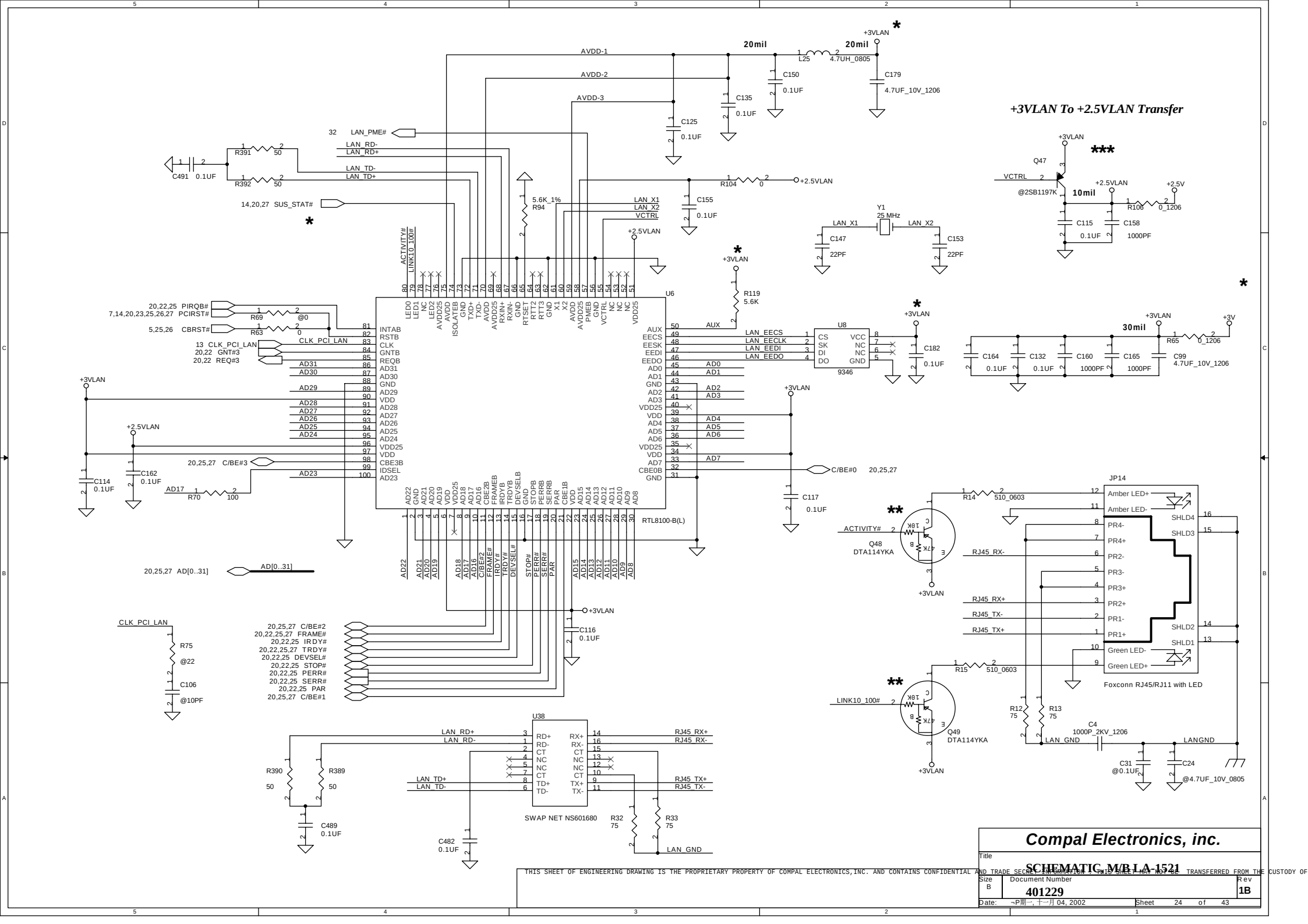

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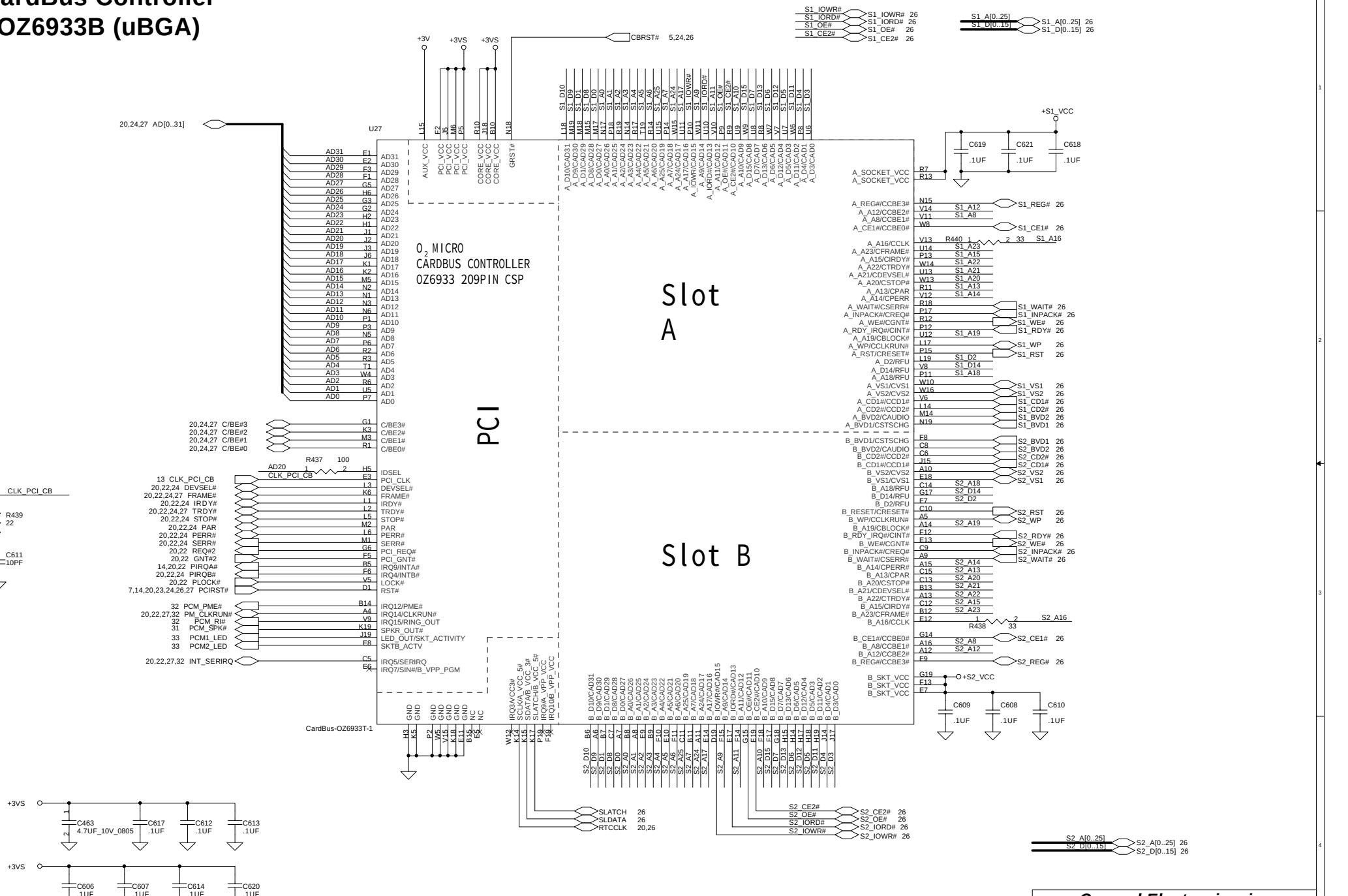
CardBus Controller
OZ6933B (uBGA)



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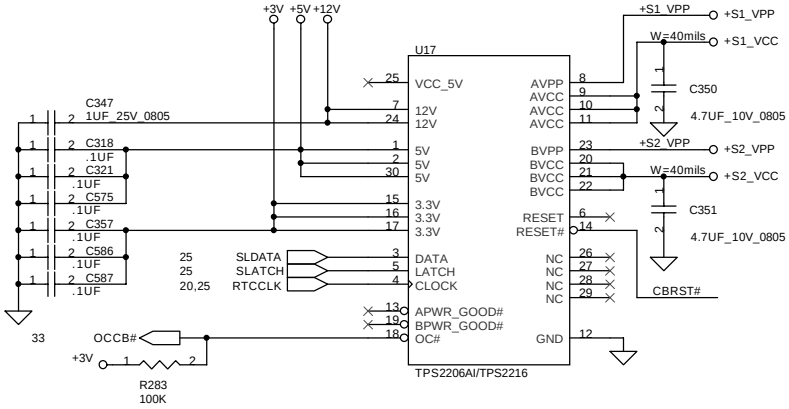
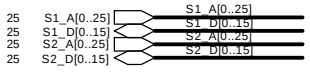
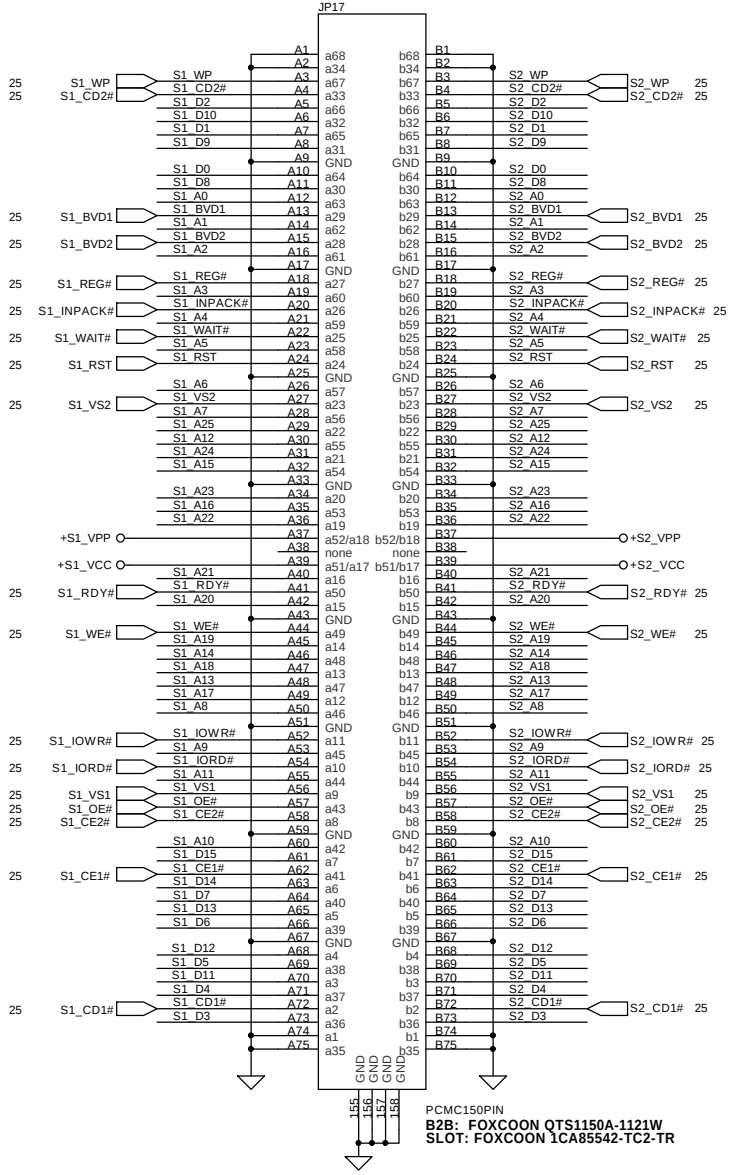
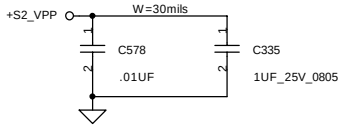
PCMCIA POWER CTRL.

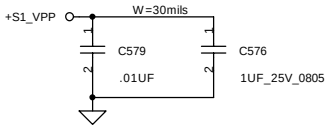


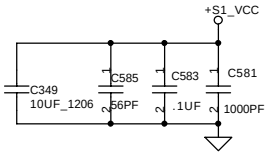


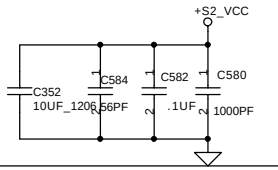
CARDBUS SOCKET

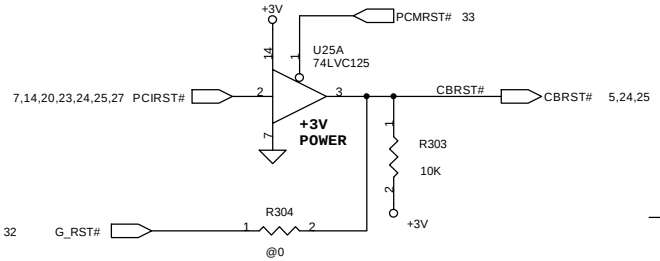


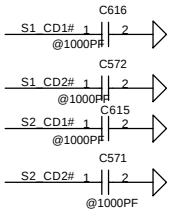












PCMC150PIN
B2B: FOXCOON QTS1150A-1121W
SLOT: FOXCOON 1CA85542-TC2-TR

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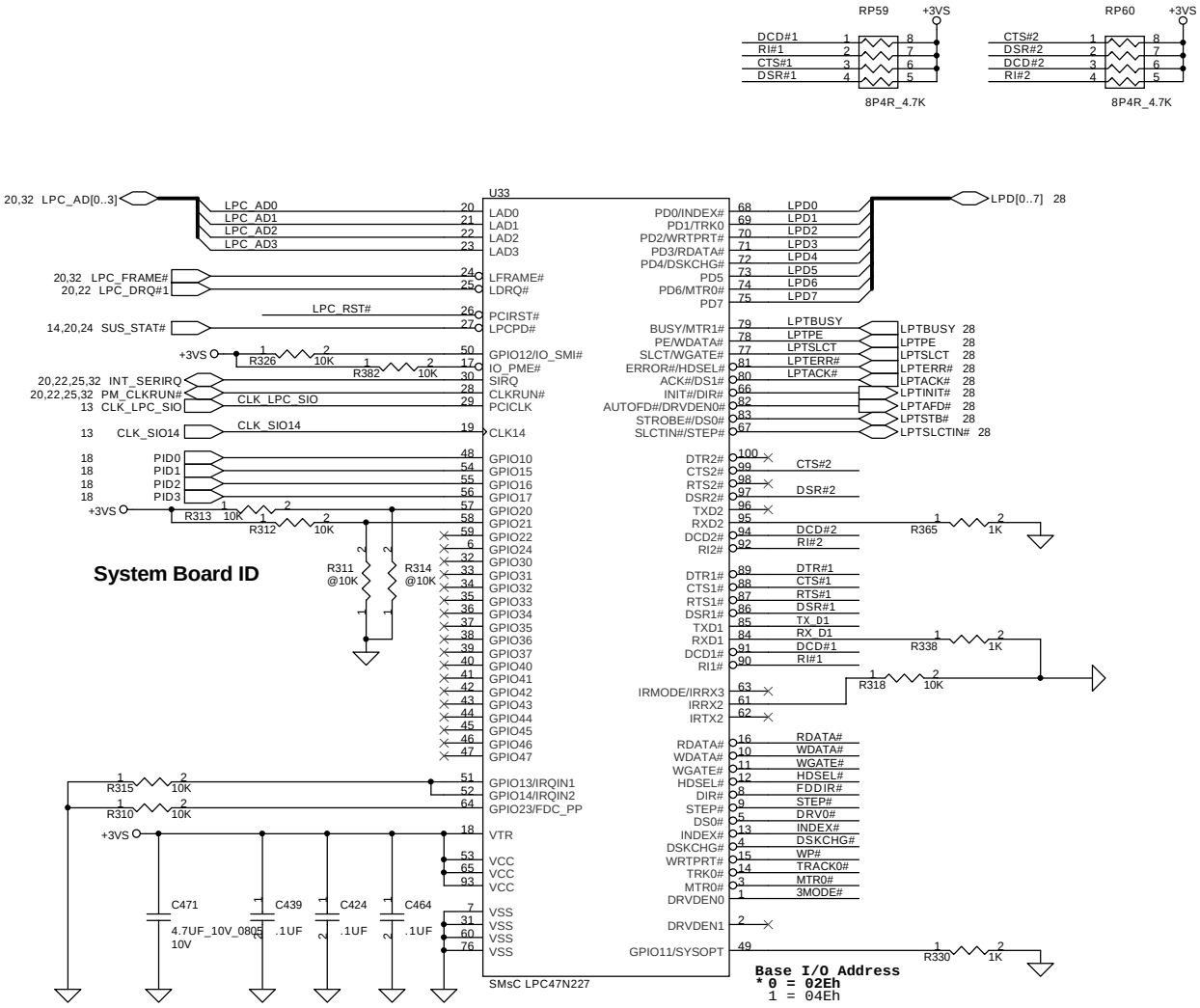
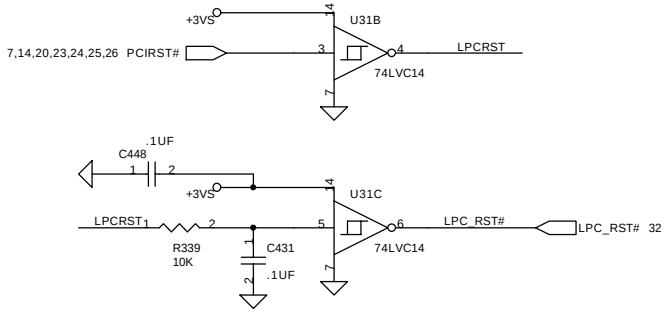
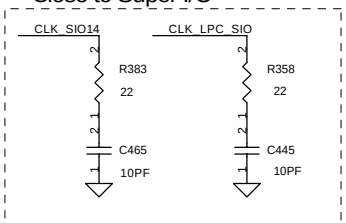
SUPER I/O SMsC FDC47N227



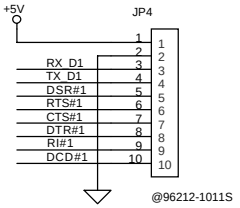


PROPRIETARY NOTE

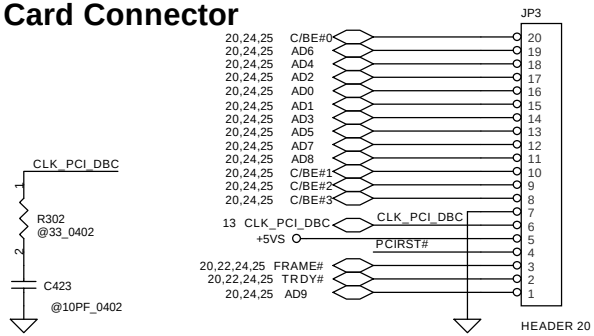
Close to Super I/O



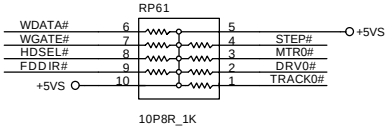
ACPI Debug Connector

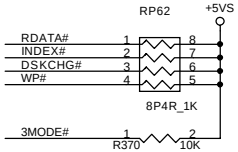


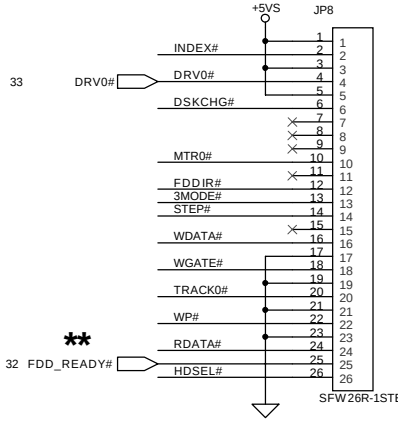
Port 80 Debug Card Connector

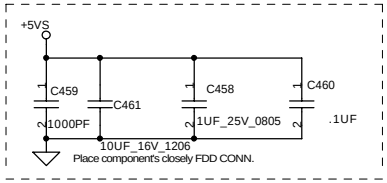


Floppy Connector









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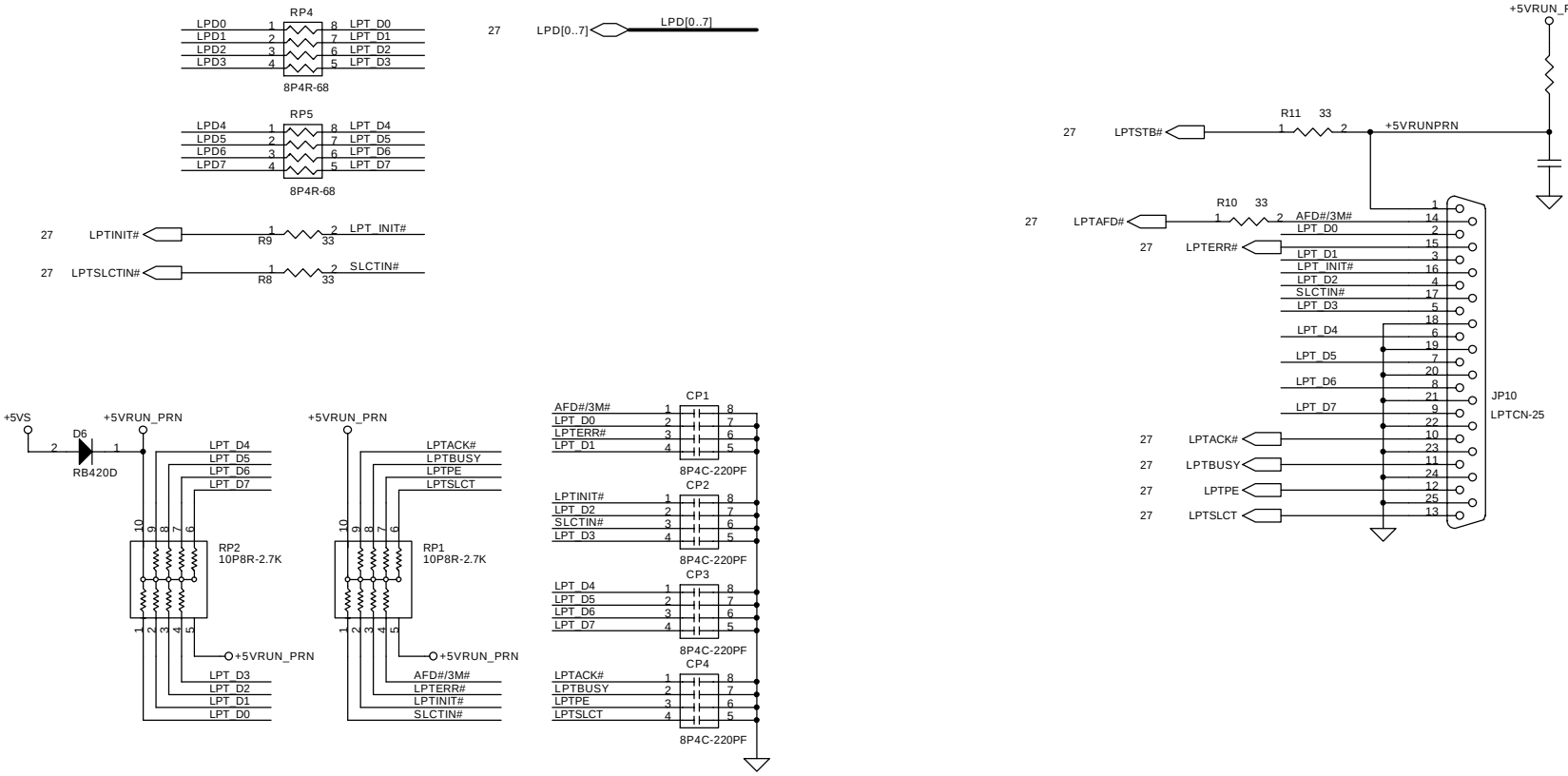
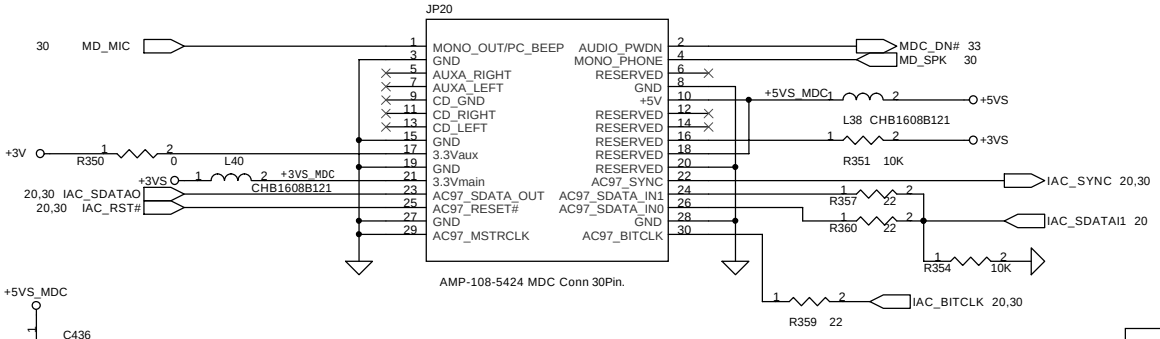
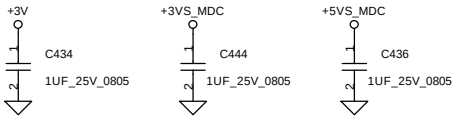
Parallel Port



MDC Connector

MDC CONN.





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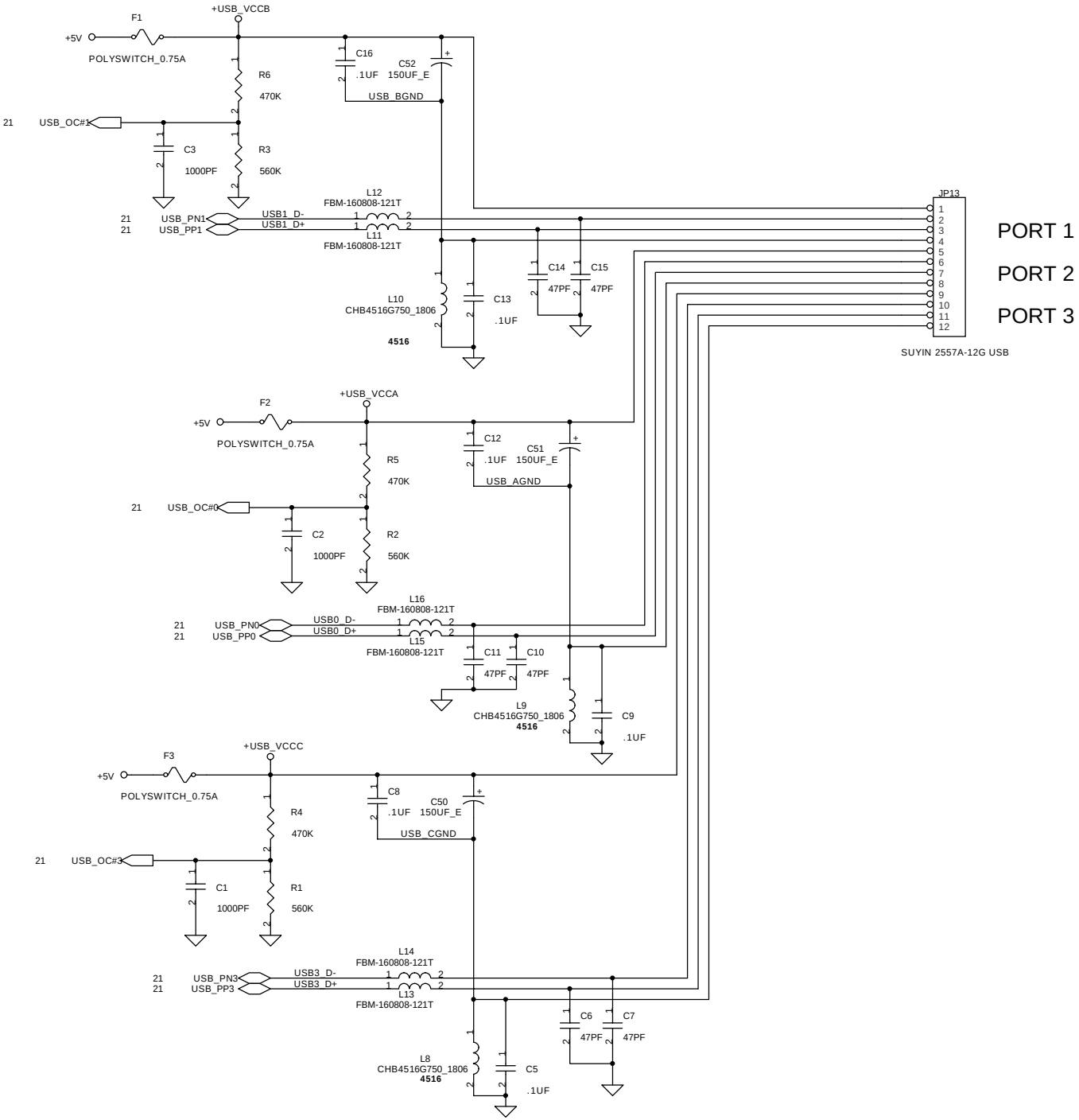
USB Port



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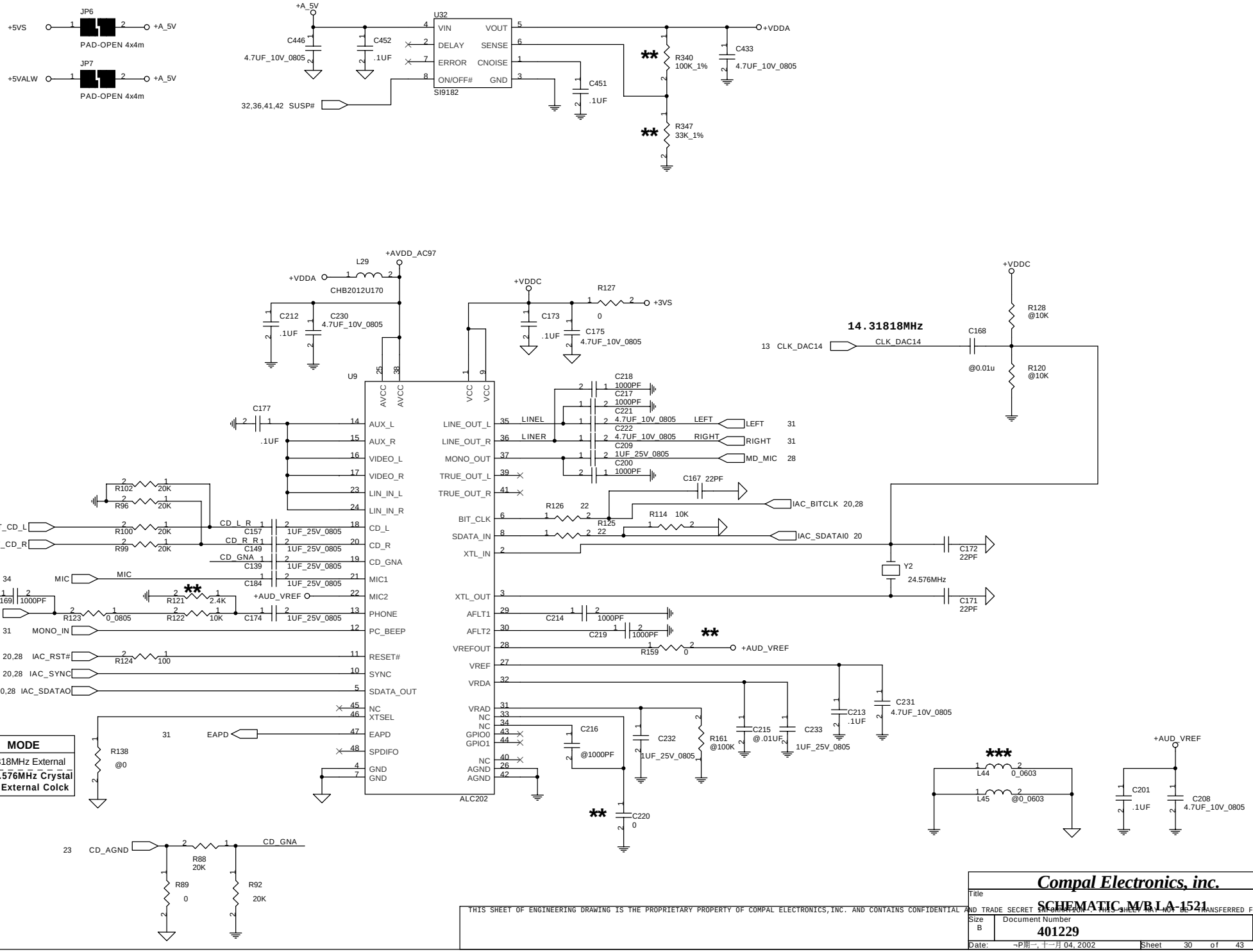
AC97 Audio Codec



R138	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

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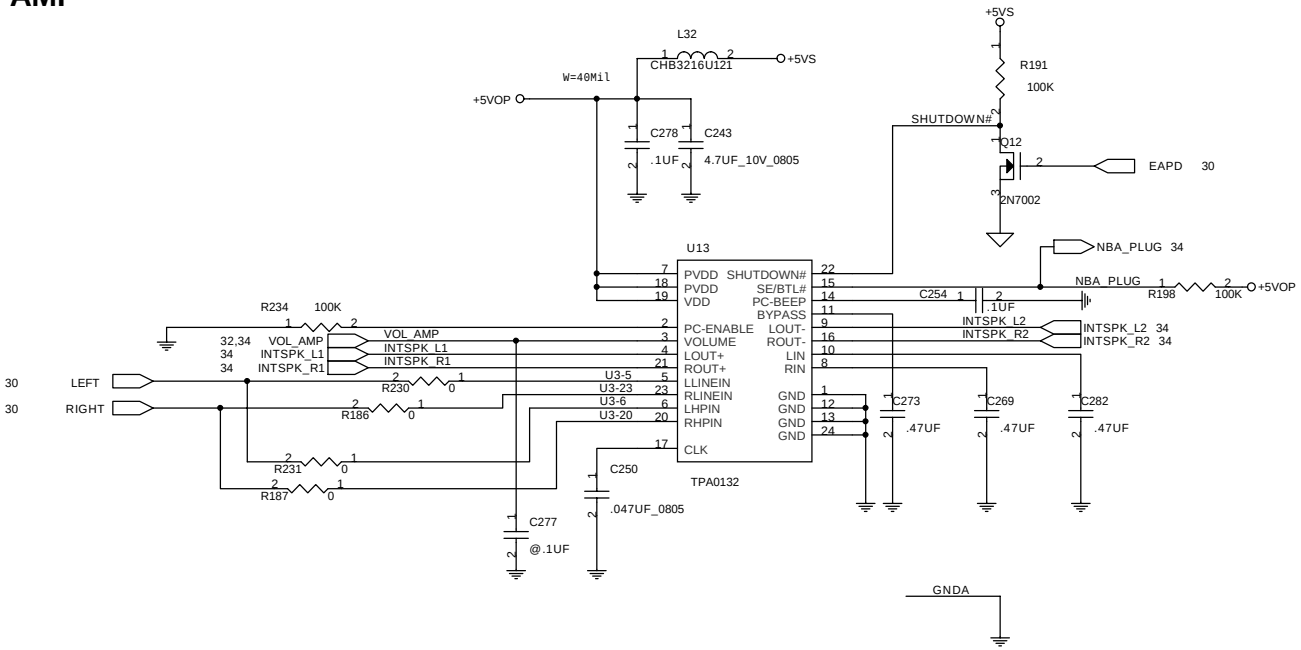
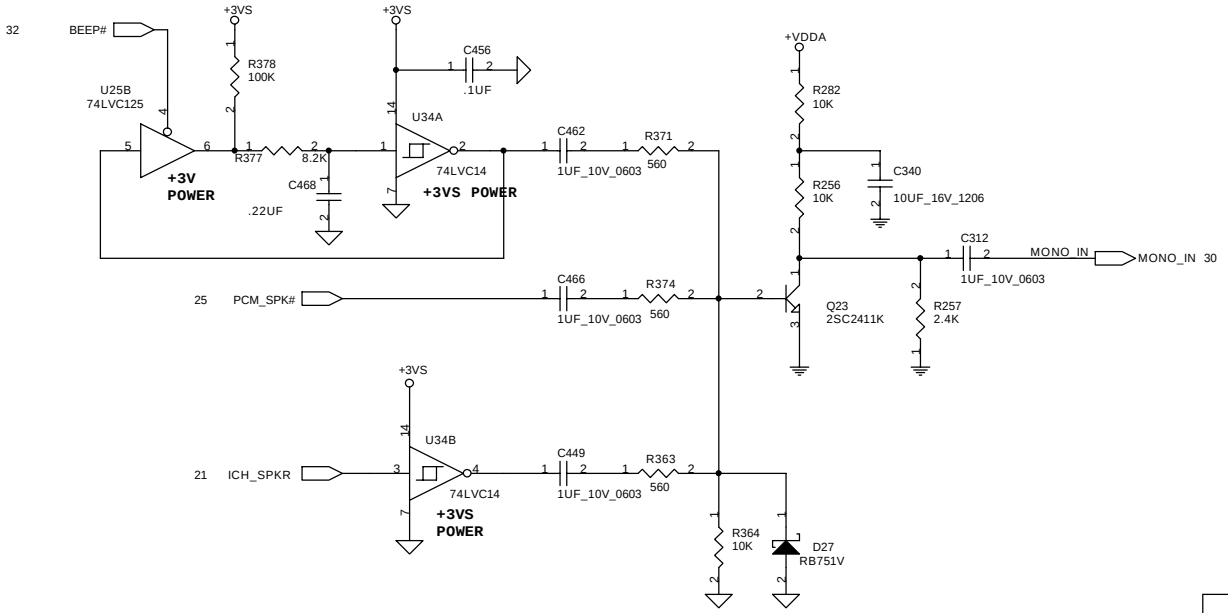
Audio AMP



System Sound



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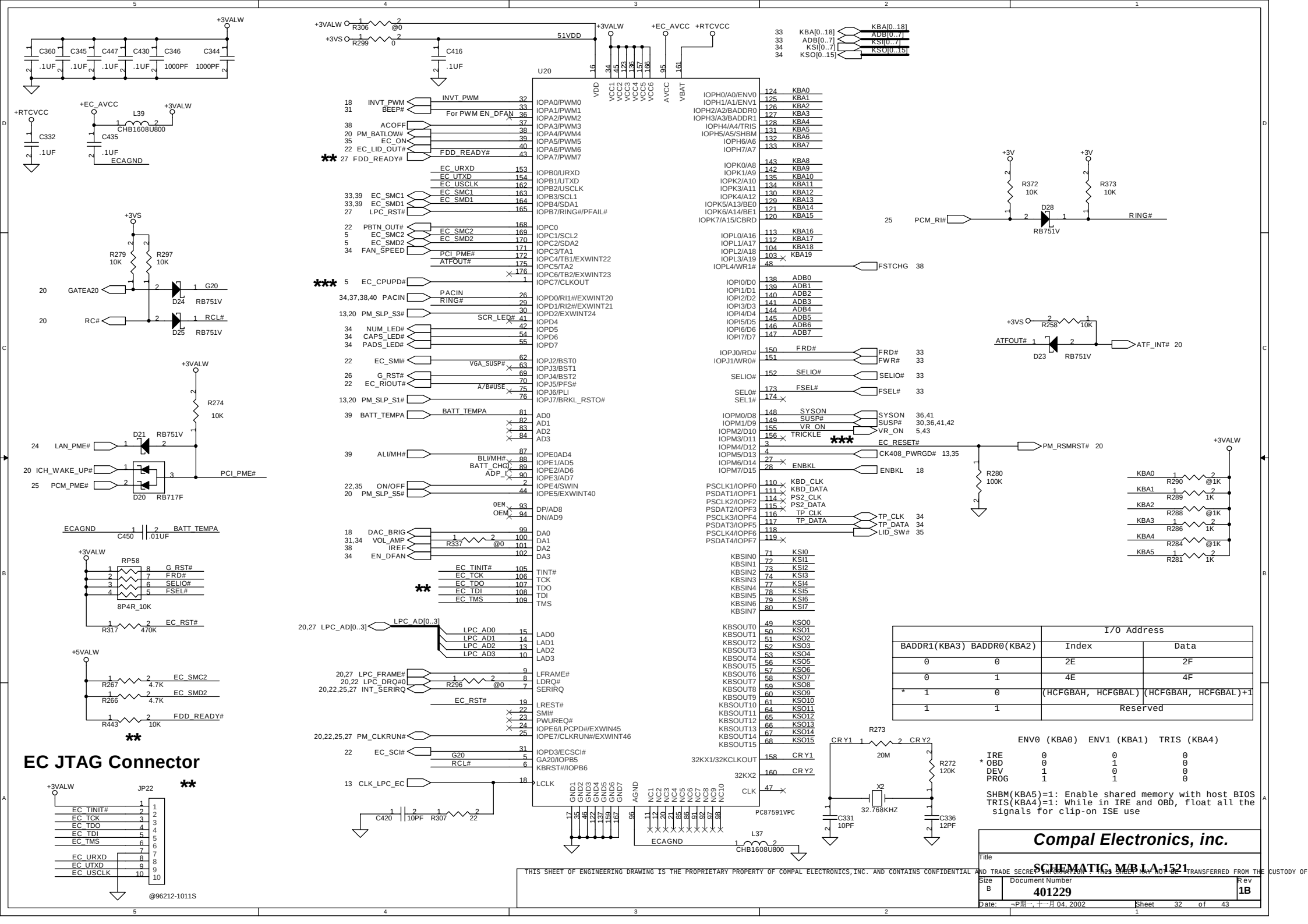

	I/O Address	
BADDR1(KBA3) BADDR0(KBA2)	Index	Data
0 0	2E	2F
0 1	4E	4F
* 1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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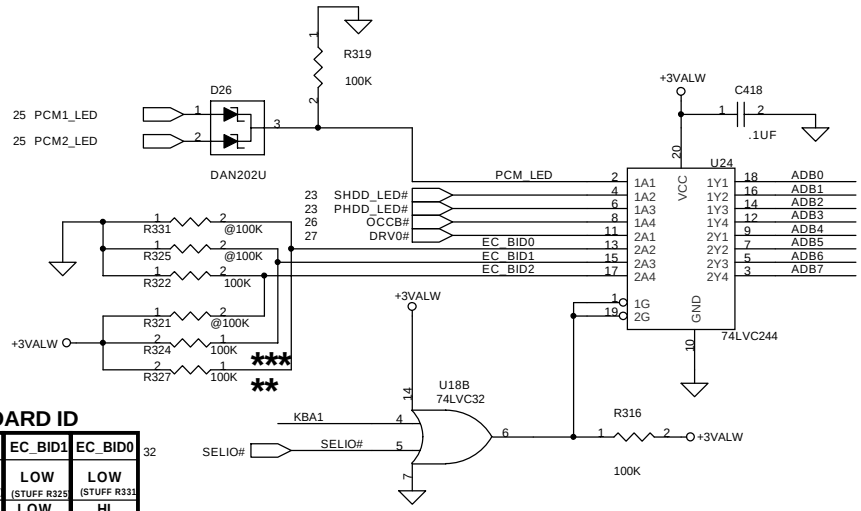
EXT I/O PORT

INPUT PORT



EC BOARD ID

	EC_BID2	EC_BID1	EC_BID0
EVT DVT (REV 0.1)	LOW (STUFF R322)	LOW (STUFF R325)	LOW (STUFF R331)
PVT1 (REV 0.2)	LOW (STUFF R322)	LOW (STUFF R325)	HI (STUFF R324)
PVT2 (REV 1.0)	LOW (STUFF R322)	HI (STUFF R324)	HI (STUFF R323)

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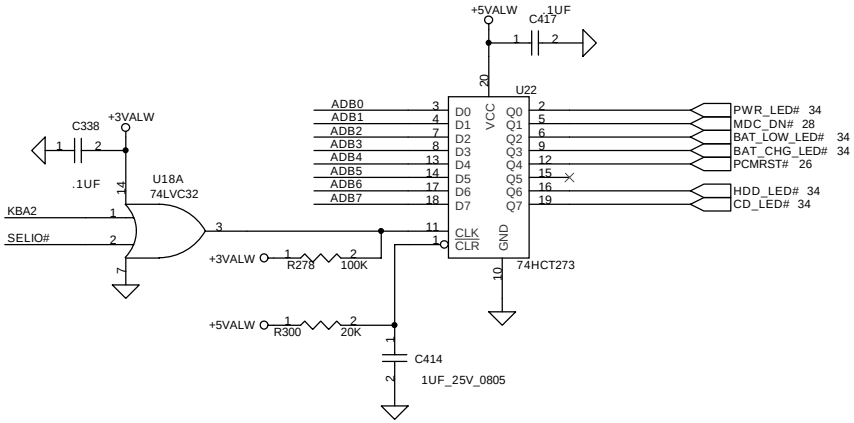
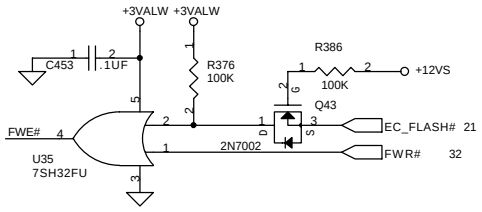
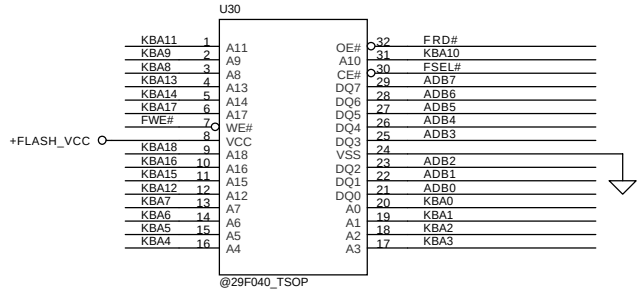
✱Pre-MP

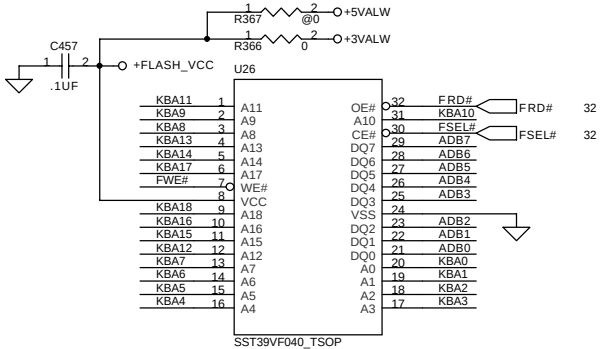
OUTPUT PORT



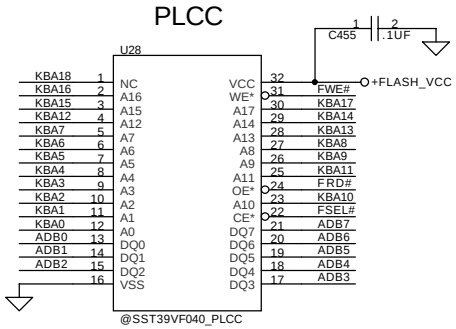
SYSTEM BIOS



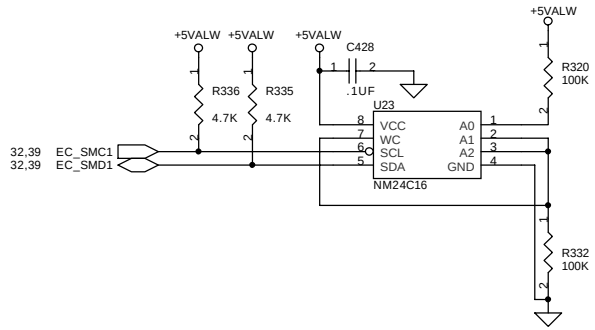




PLCC



SMBUS EEPROM



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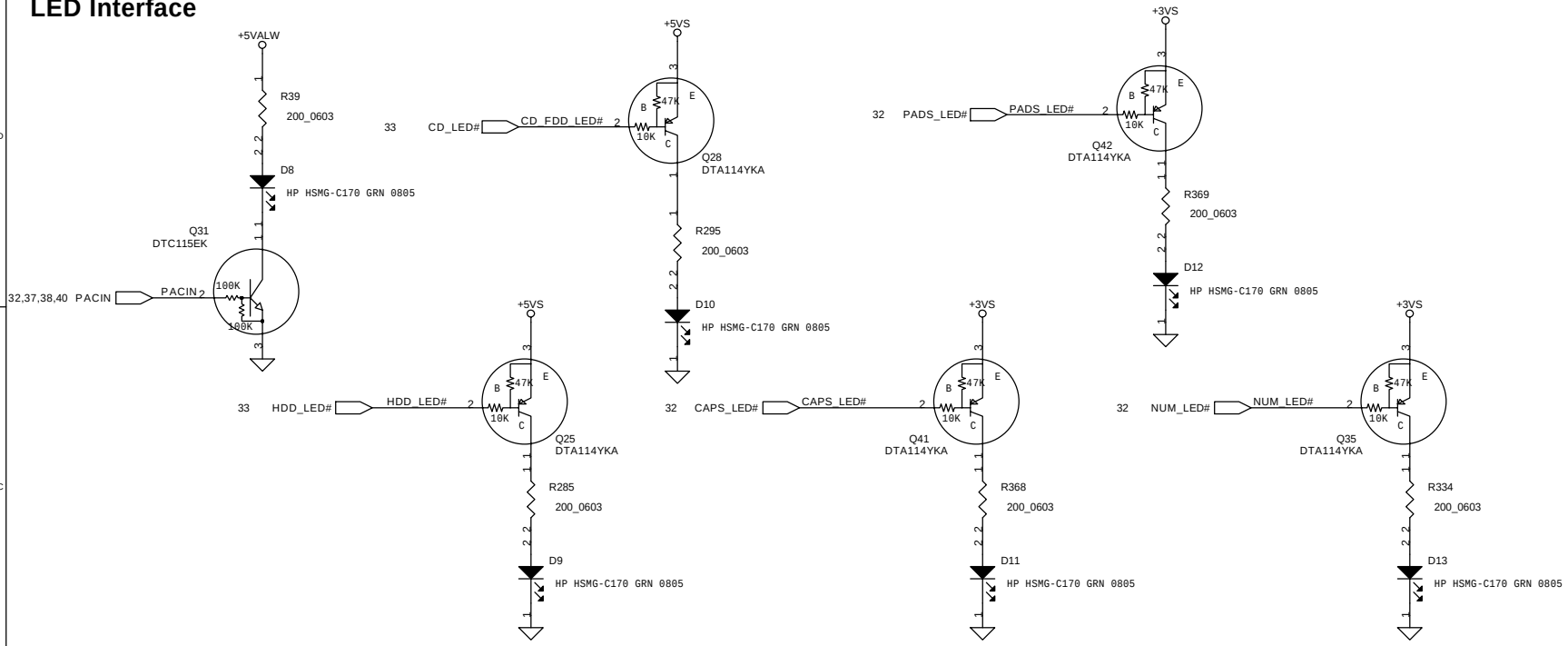
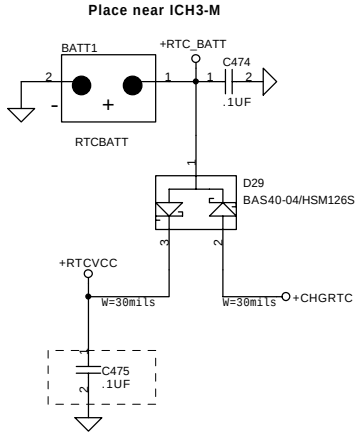
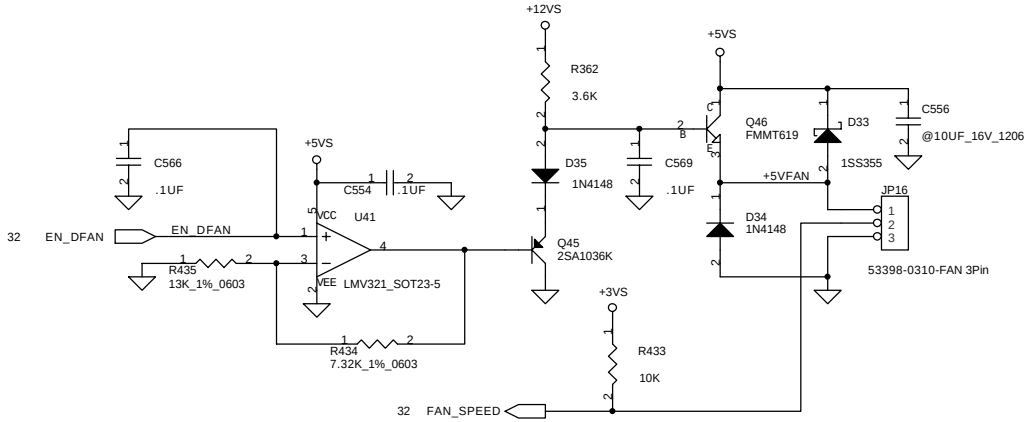
LED Interface



RTC Batt.

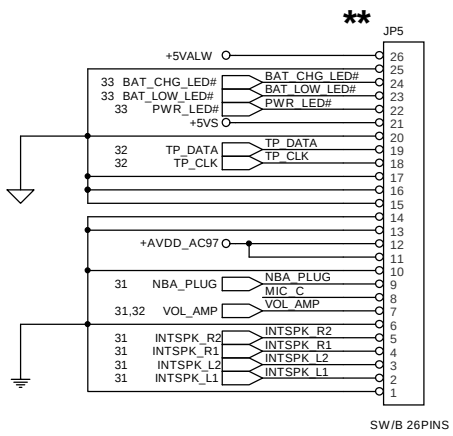


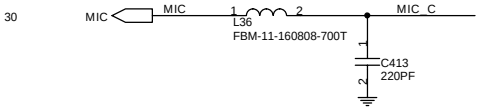
FAN Connector



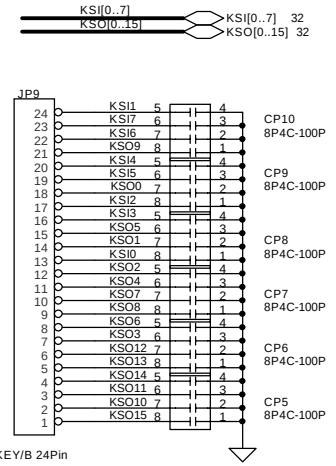
System Connector

Switch Board Connector





Int. Keyboard Connector



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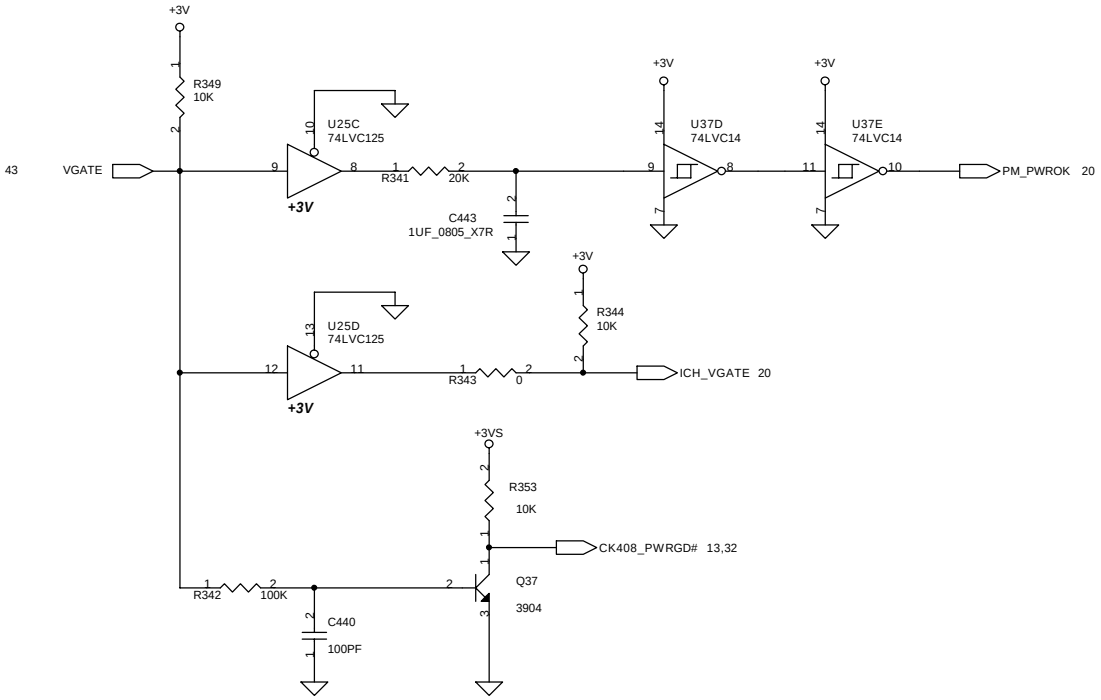
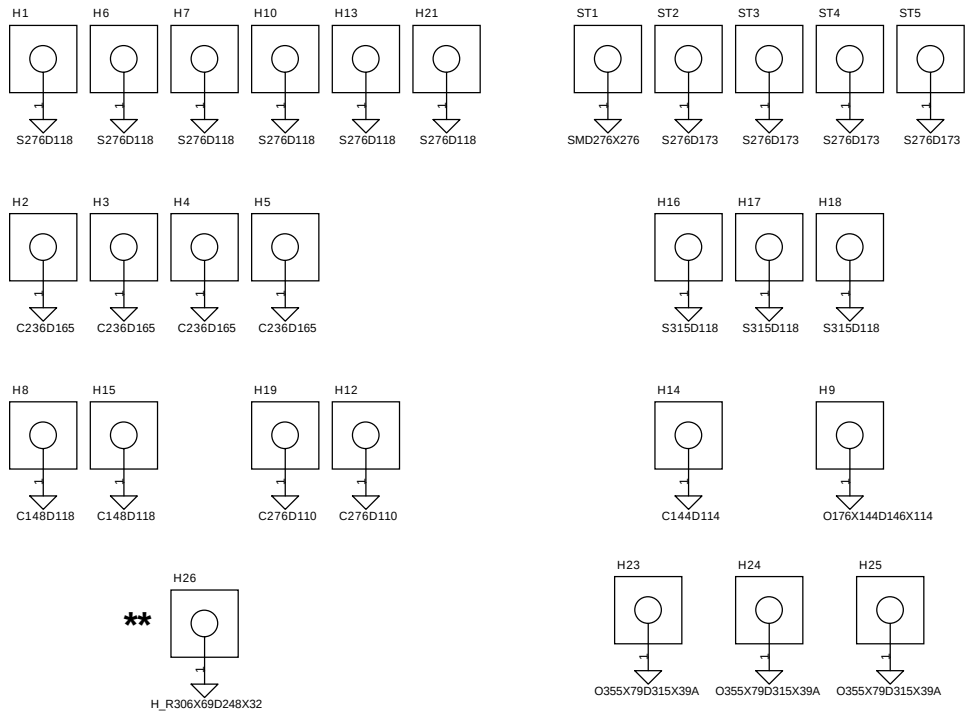
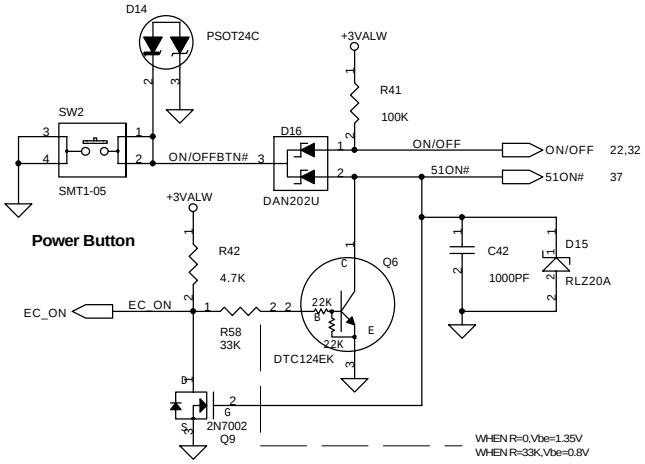
Power Good Circuit



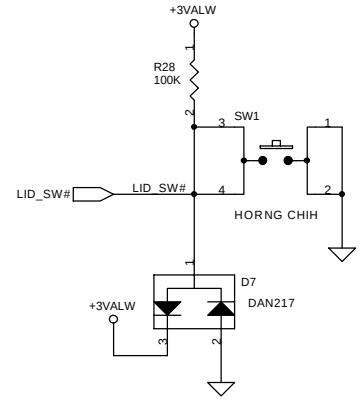
Screw Hole



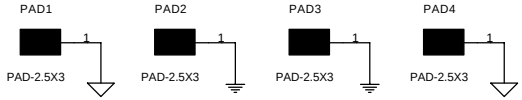
SW for Power Button



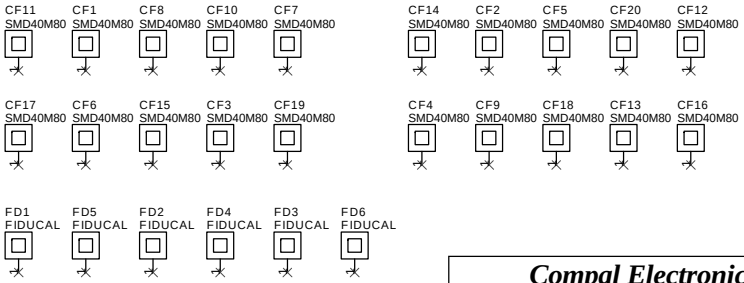
LID Switch



EMI CLIP PAD



Fiducial Mark



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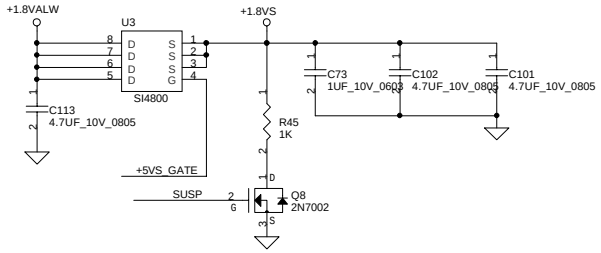
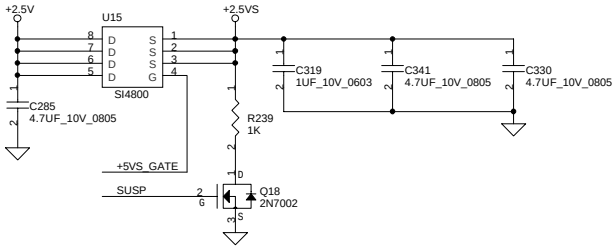
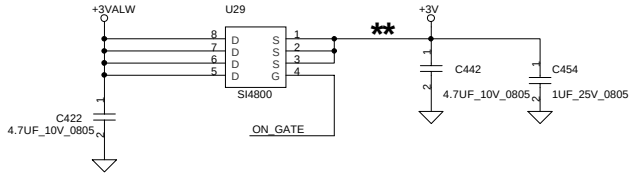
+1.8VALW To +1.8VS Transfer



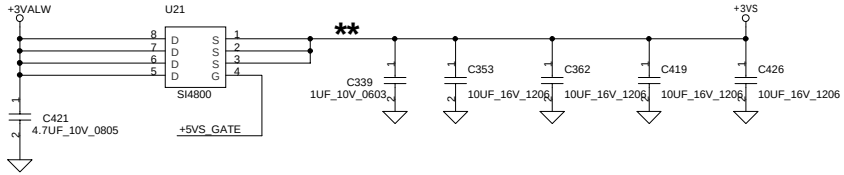
+2.5V To +2.5VS Transfer



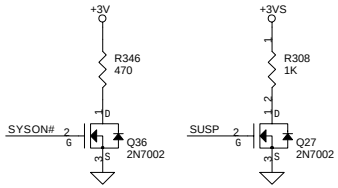
+3VALW To +3V Transfer



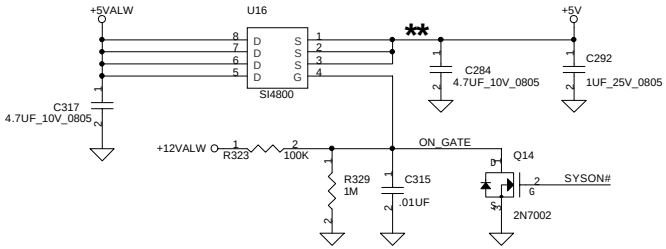
+3VALW To +3VS Transfer



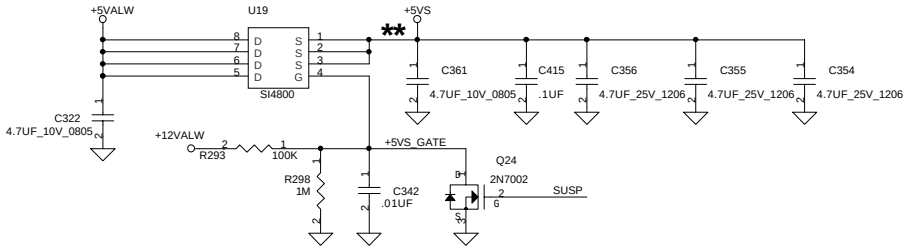
+3V & +3VS Discharge



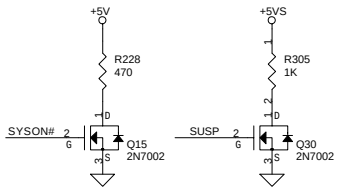
+5VALW To +5V Transfer



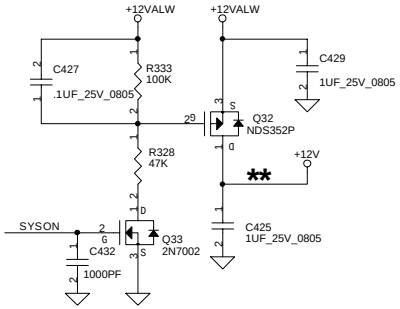
+5VALW To +5VS Transfer



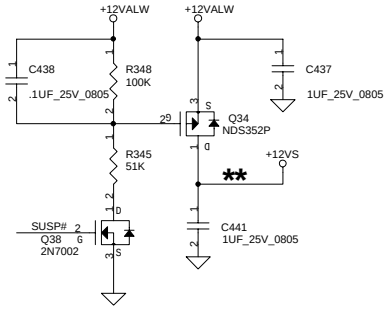
+5V & +5VS Discharge



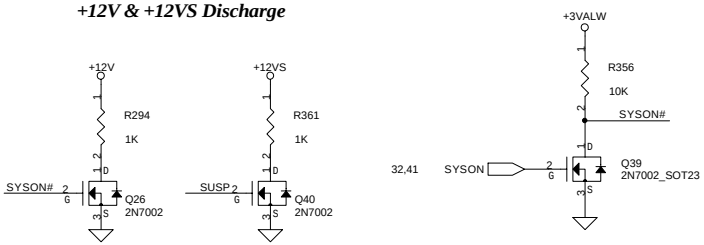
+12VALW To +12V Transfer



+12VALW To +12VS Transfer



+12V & +12VS Discharge



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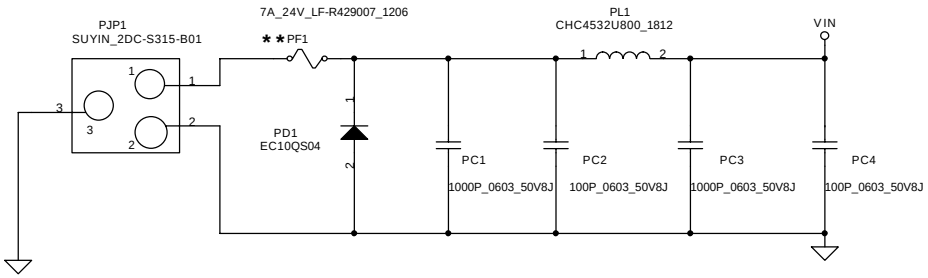
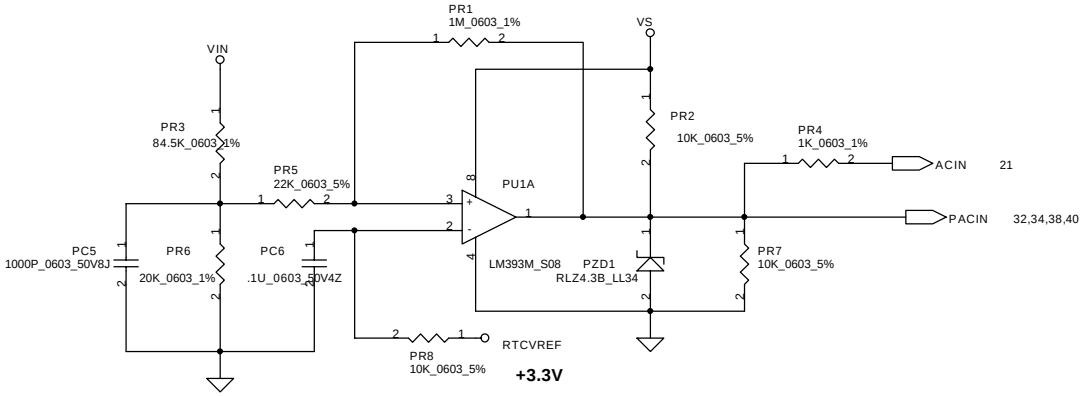
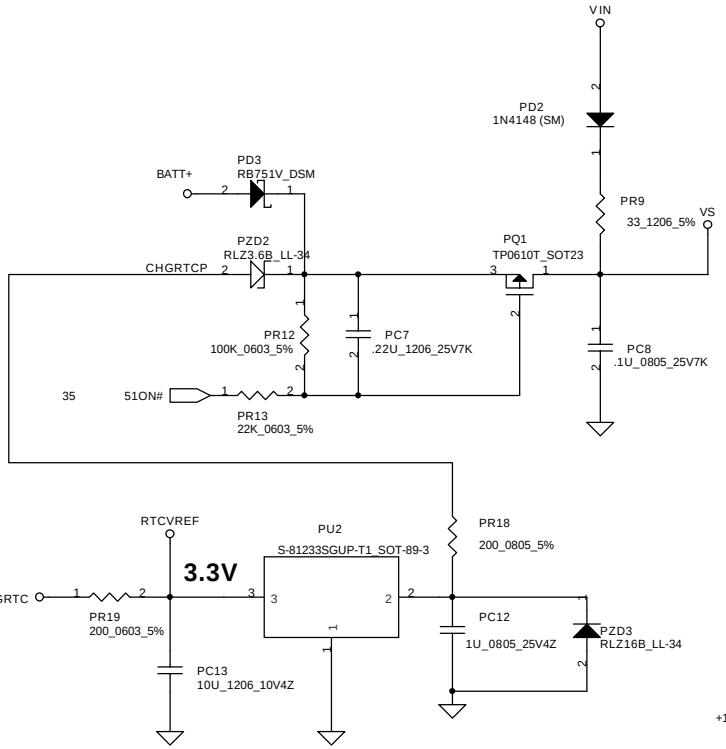
Vin Detector

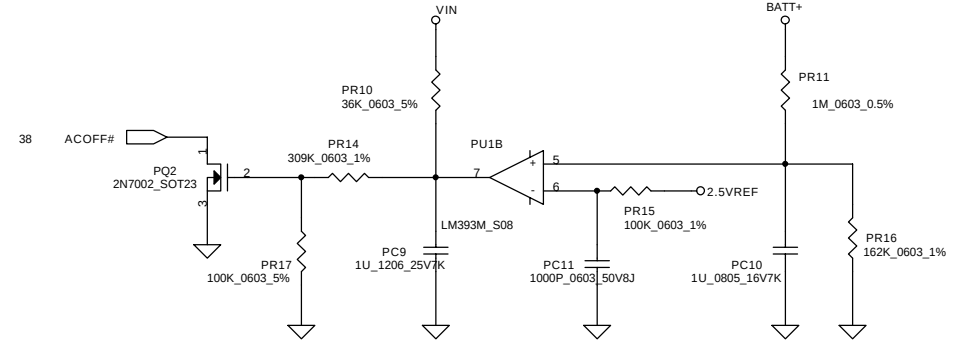
High	**18.764**	**17.901**	**17.063**
Low	**17.745**	**16.903**	**16.038**

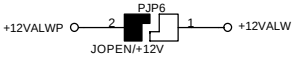






8 Cells LI-ION BAT Charger OVP : 18.059V

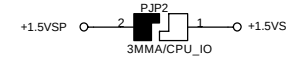




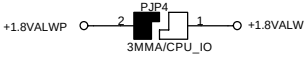
(120mA,20mils ,Via NO.= 1)

(5A,200mils ,Via NO.= 10)

(5A,200mils ,Via NO.= 10)



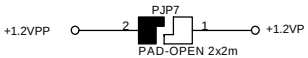
(1.5A,60mils ,Via NO.= 3)



(3A,120mils ,Via NO.= 6)

(6A,240mils ,Via NO.= 12)

(3A,120mils ,Via NO.= 6)



(300mA,40mils ,Via NO.= 2)

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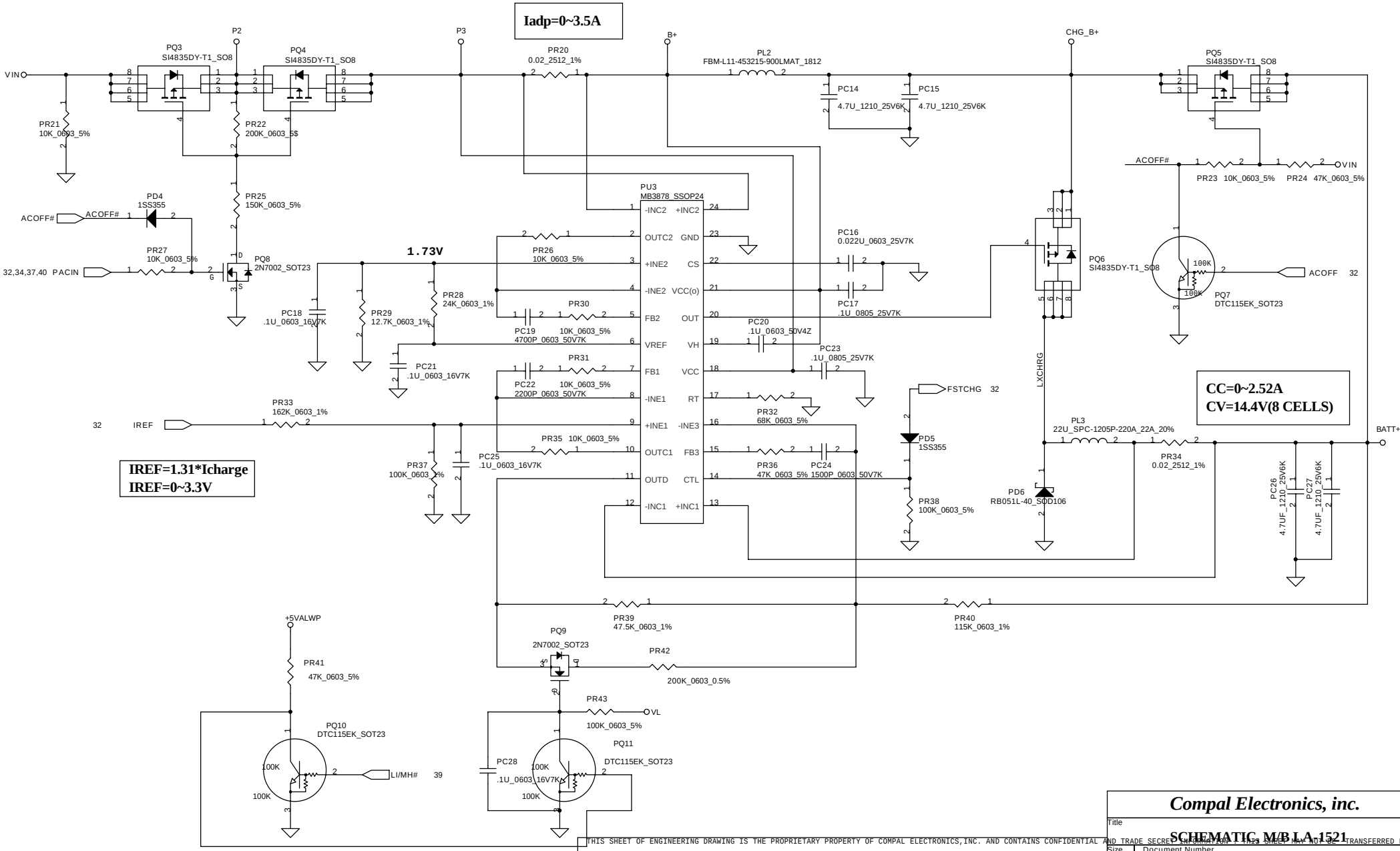

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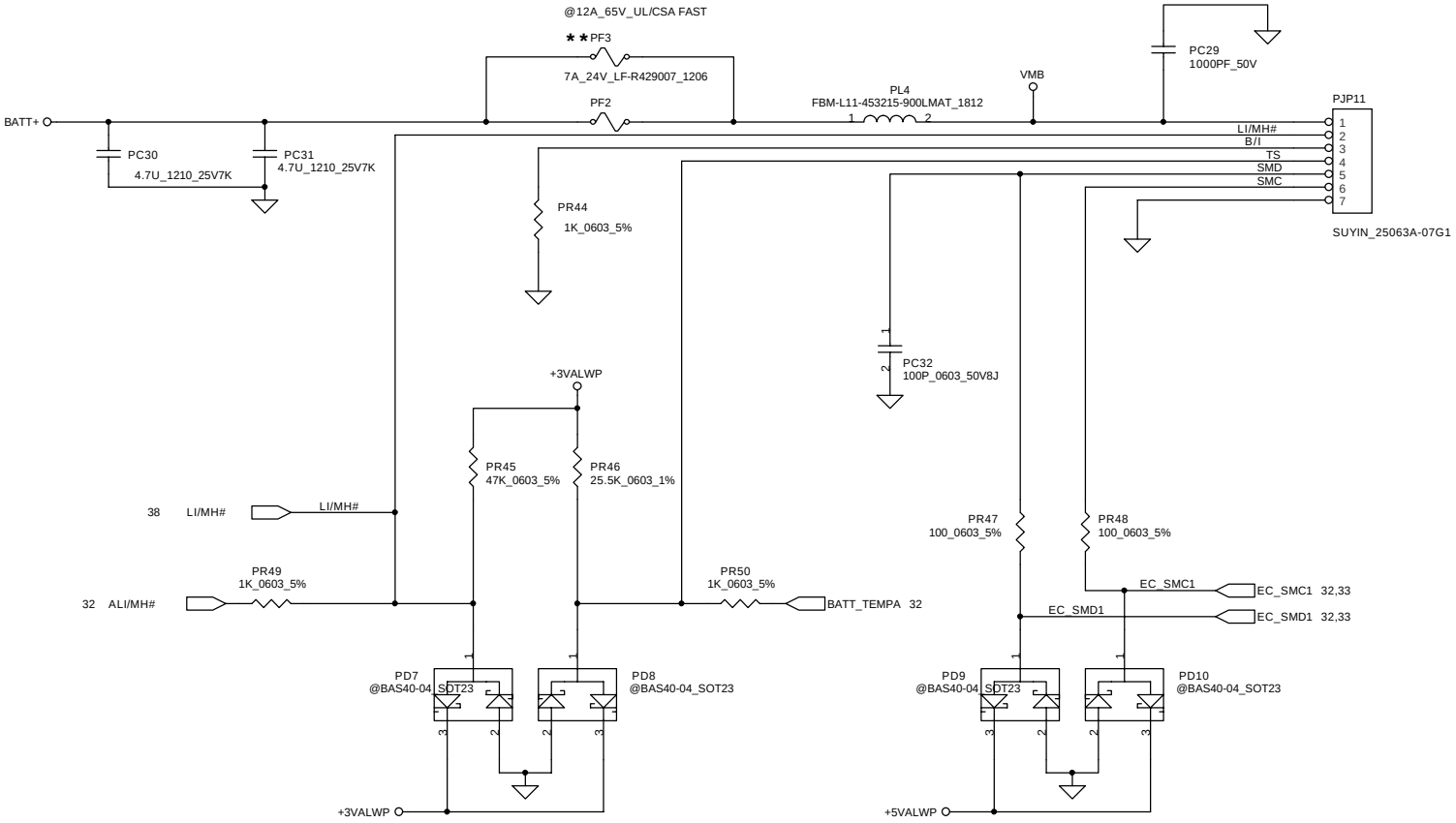

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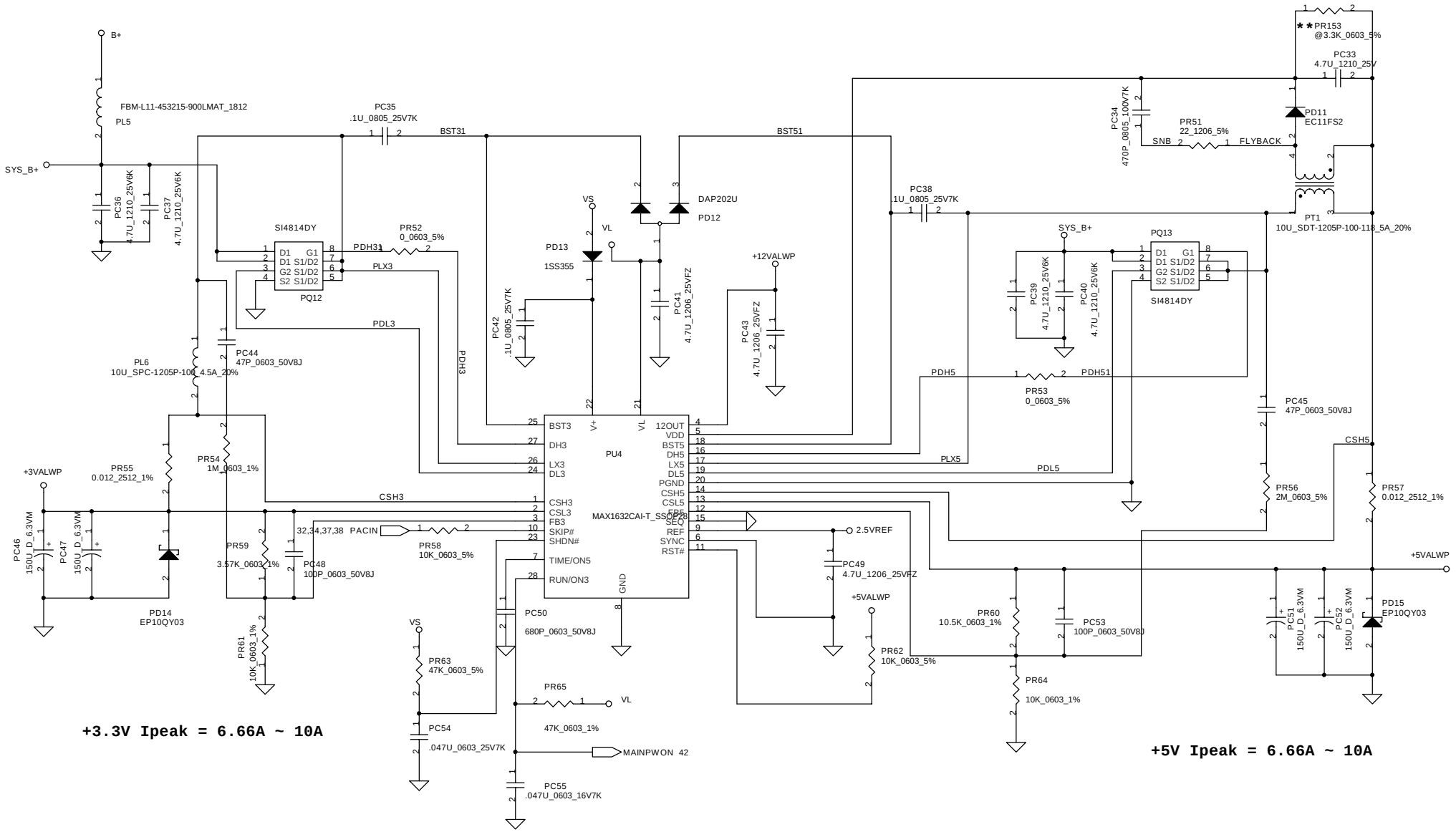

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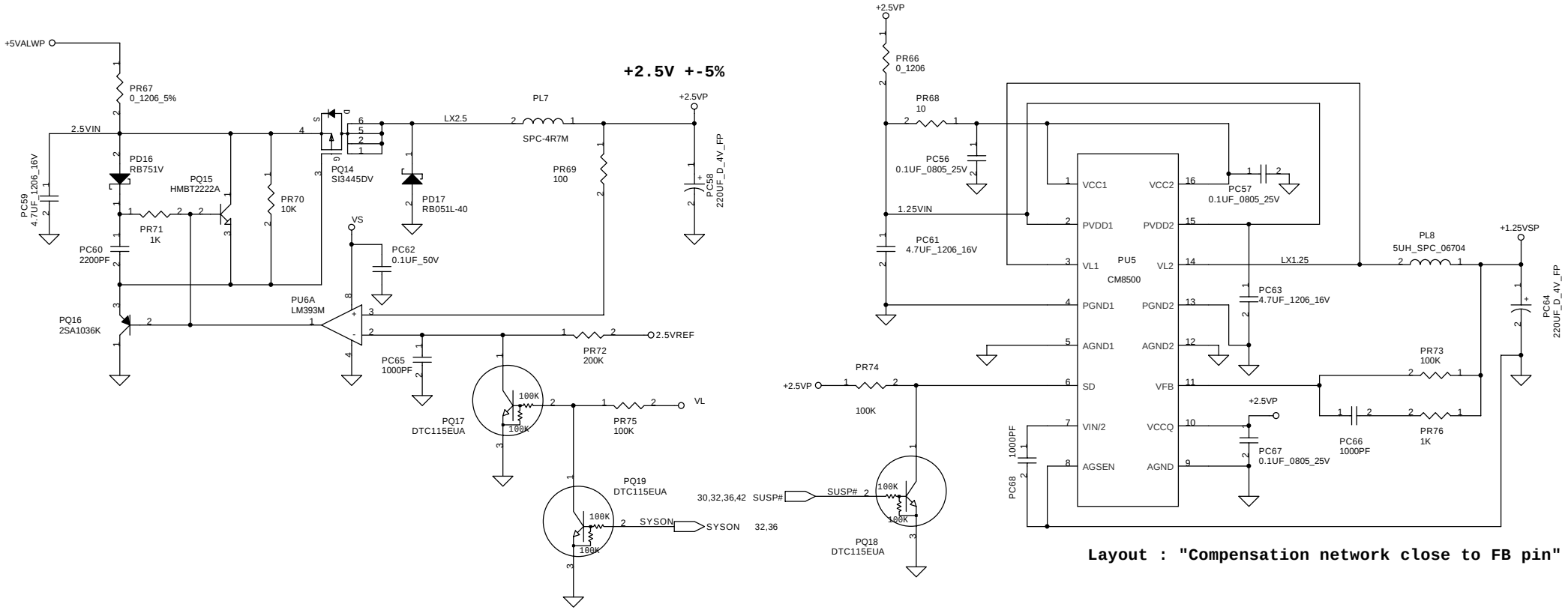

Layout : "Compensation network close to FB pin"

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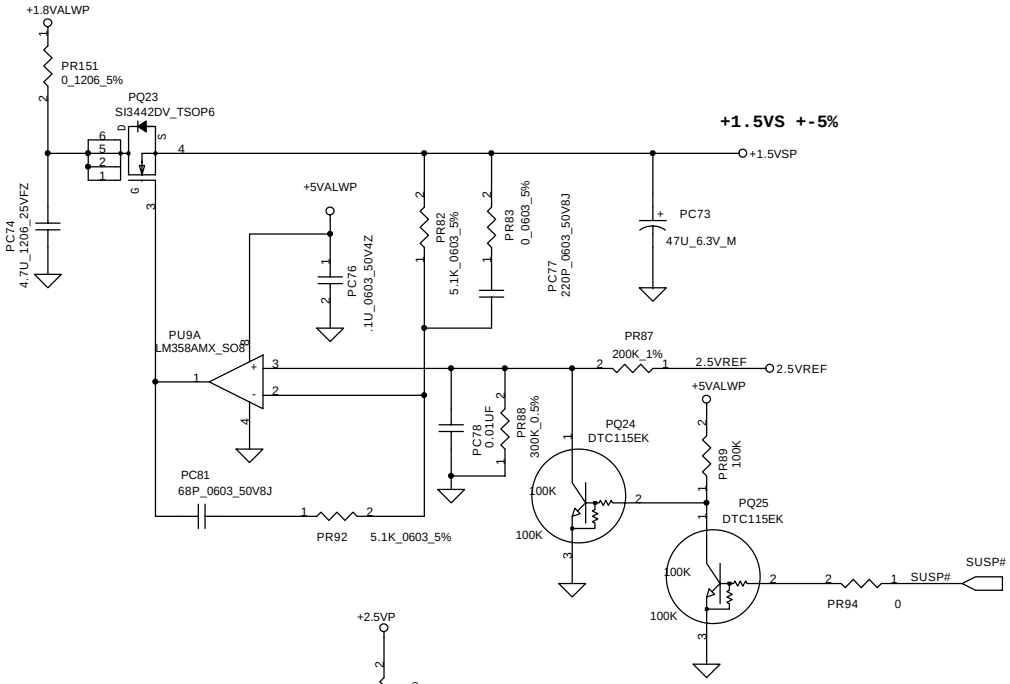
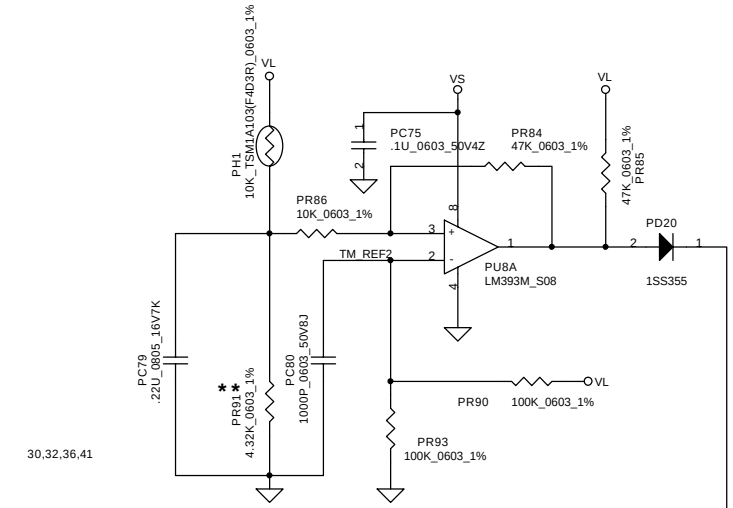
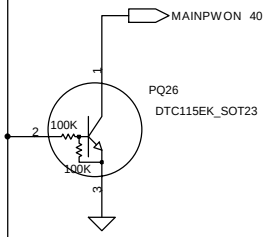
PH1 near main Battery CONN :
BAT. thermal protection at 65 degree C
Recovery at 40(41) degree C

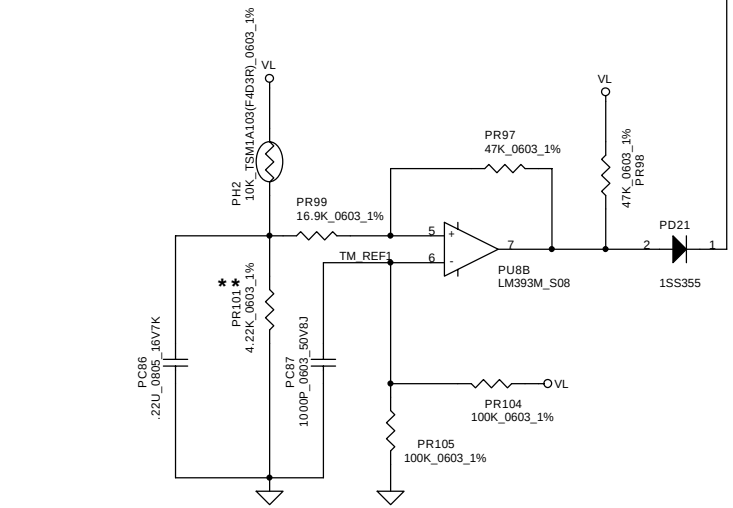


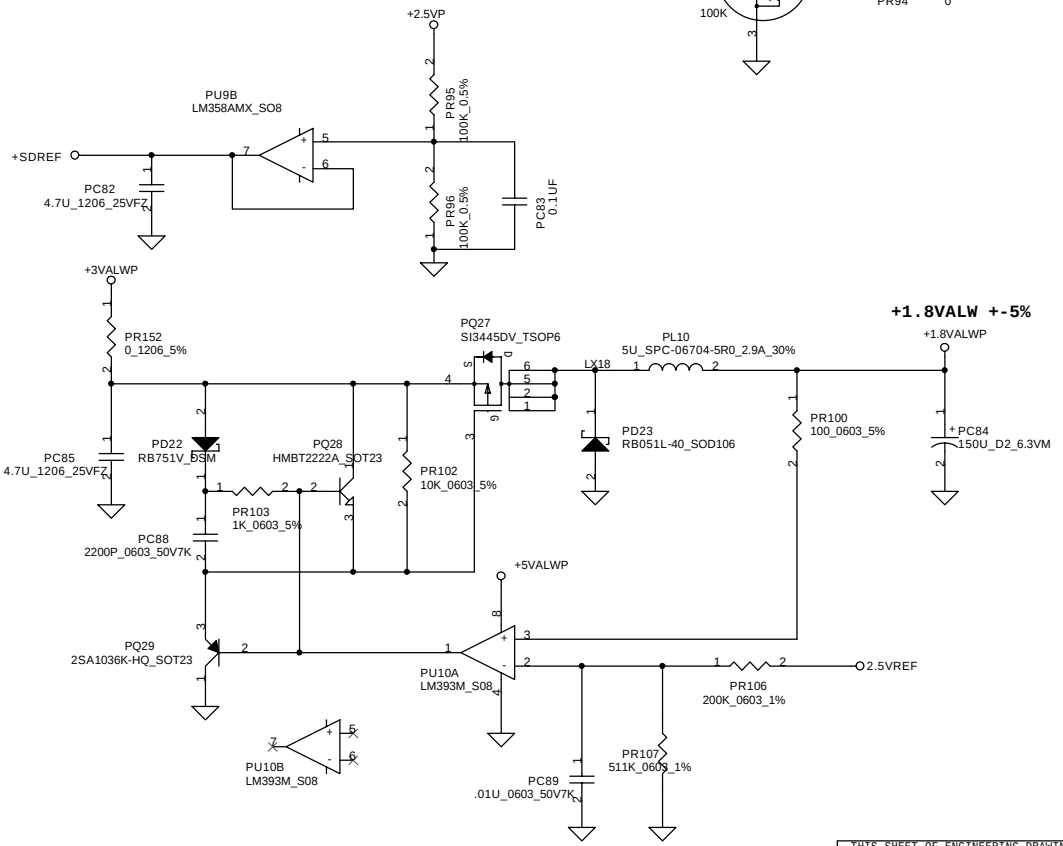


30,32,36,41



PH2 under CPU botten side :
CPU thermal protection at 76 degree C
Recovery at 37 degree C





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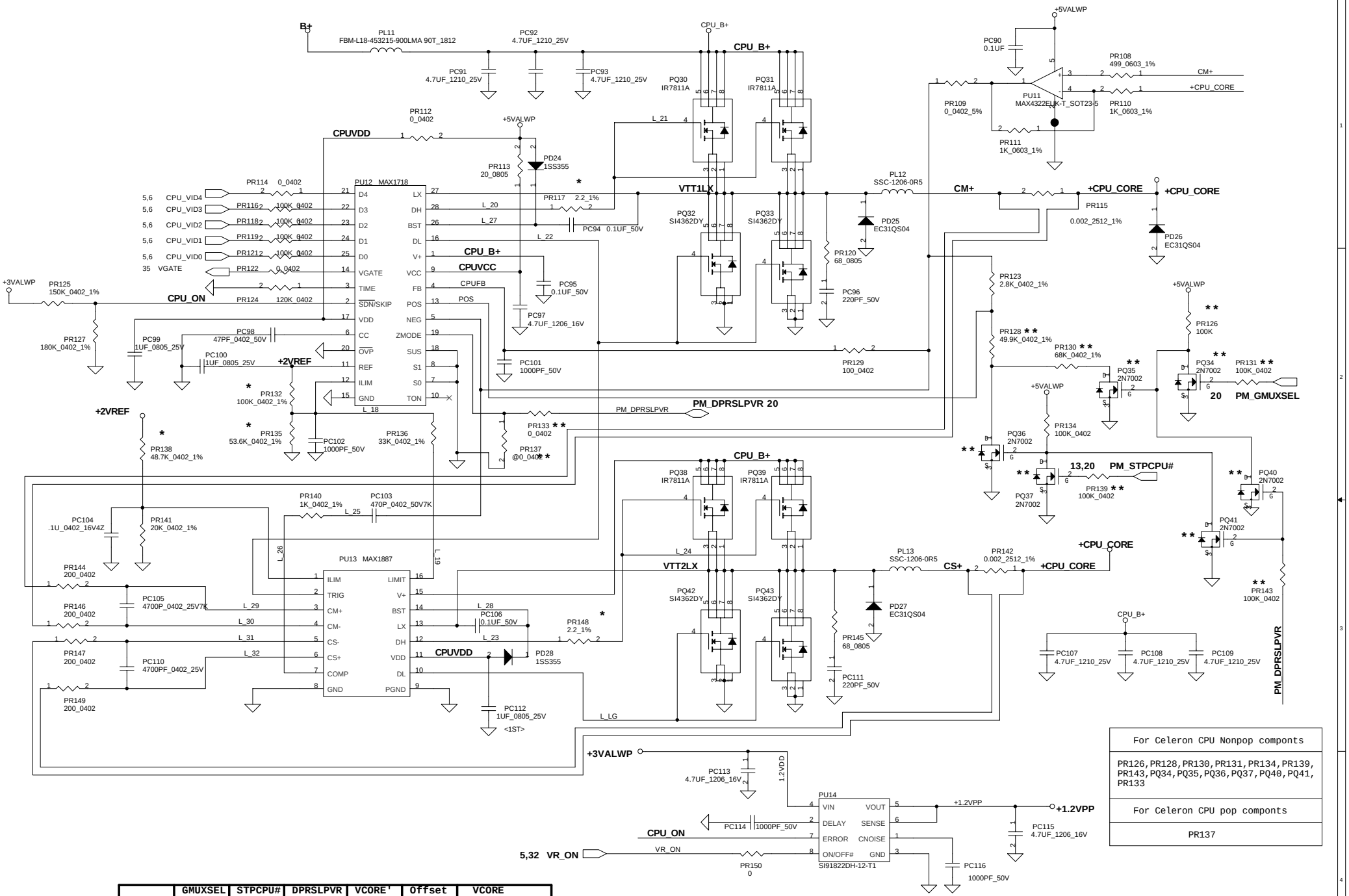

	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

For Celeron CPU Nonpop components
PR126,PR128,PR130,PR131,PR134,PR139, PR143,PQ34,PQ35,PQ36,PQ37,PQ40,PQ41, PR133
For Celeron CPU pop components
PR137

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