

Schematics Document
LA-1381 REV0.5
uFCBGA/uFCPGA Northwood with
Brookdale chipset(845MP/MZ+ICH3-M)

BOM 記號

DT@ SKU W/Desktop CPU 要打
M@ SKU W/Mobile CPU 要打
LAN@ SKU W/LAN 要打
1394@ SKU W/1394 controller 要打
S@ SKU W/TVOUT 要打
FIR@ SKU W/FIR module 要打
MDC@ SKU W/MODEM module 要打
DK@ SKU W/DOCKING 要打
SD@ SKU W/SD CARD 要打
BT@ SKU W/Bluetooth module 要打
MLED@ SKU Media LED supper 要打
SUB@ SKU W/SUBWOOFER 要打

PCB Layer
Structure:
TOP
GND1
IN1
IN2
VCC
IN3
GND2
BOT

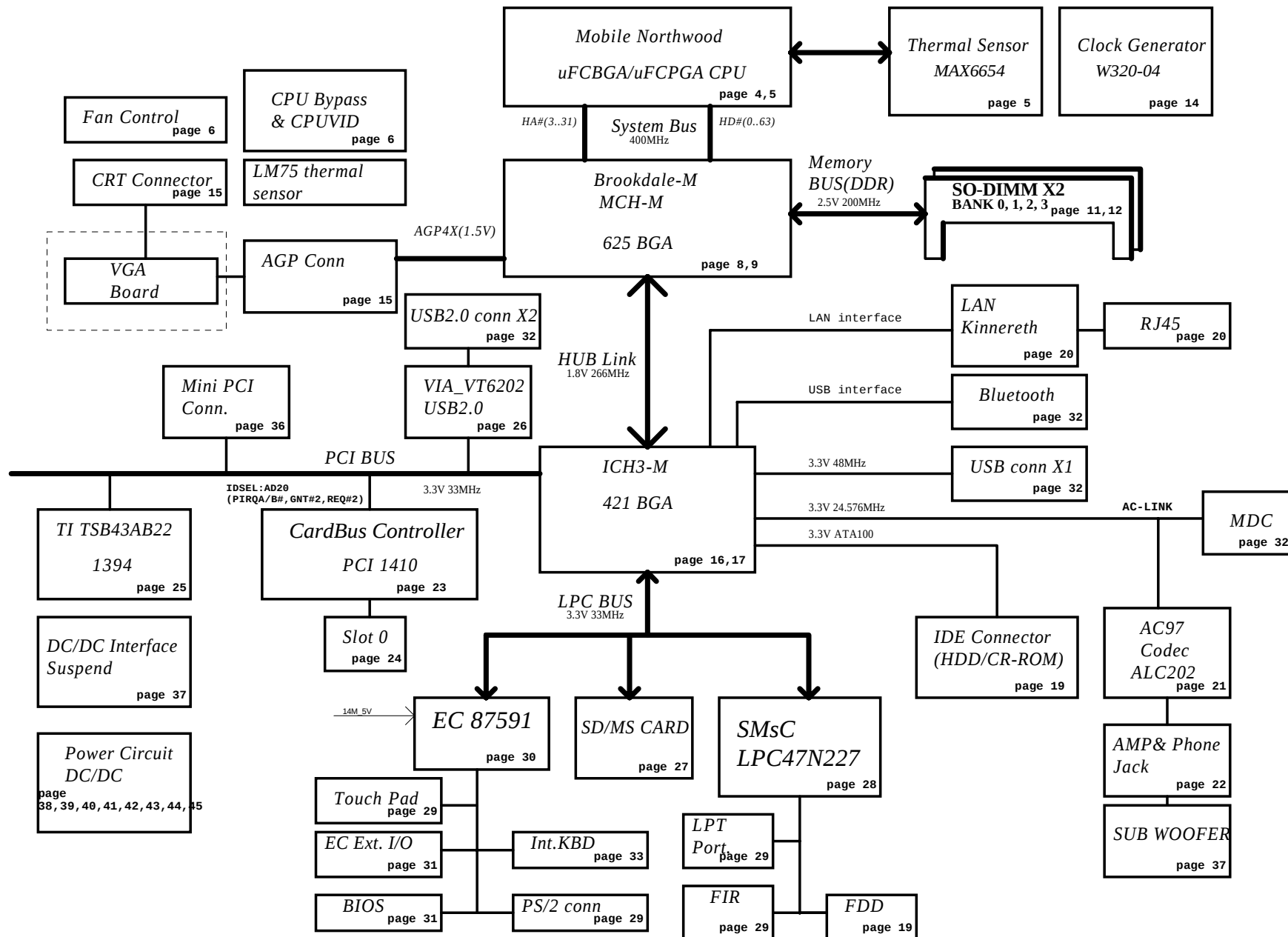
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Compal confidential

Model Name : APL11

File Name : LA-1381



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Power Managment table

Signal State	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	NB Chip Rev	SB Chip Rev

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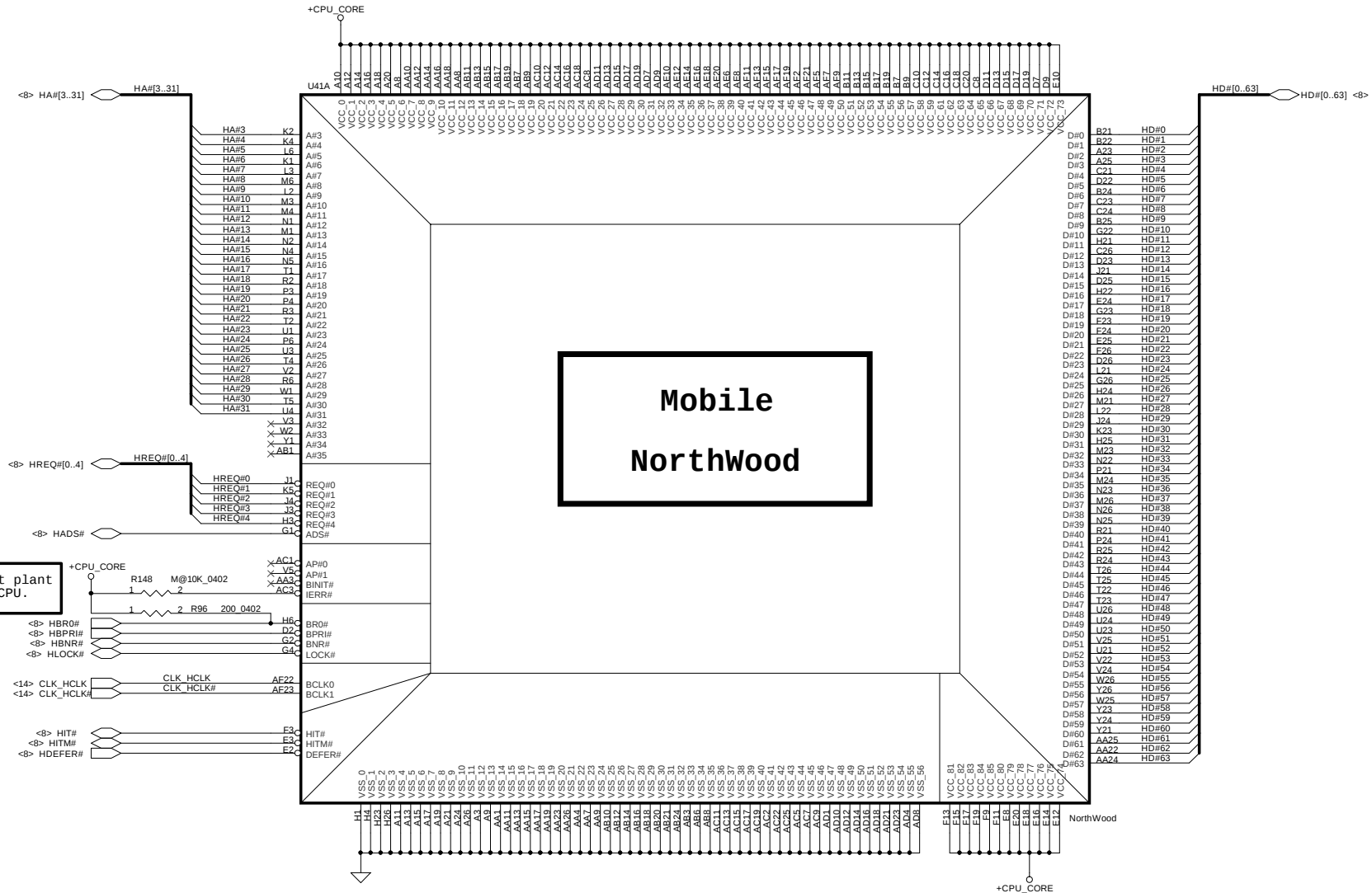
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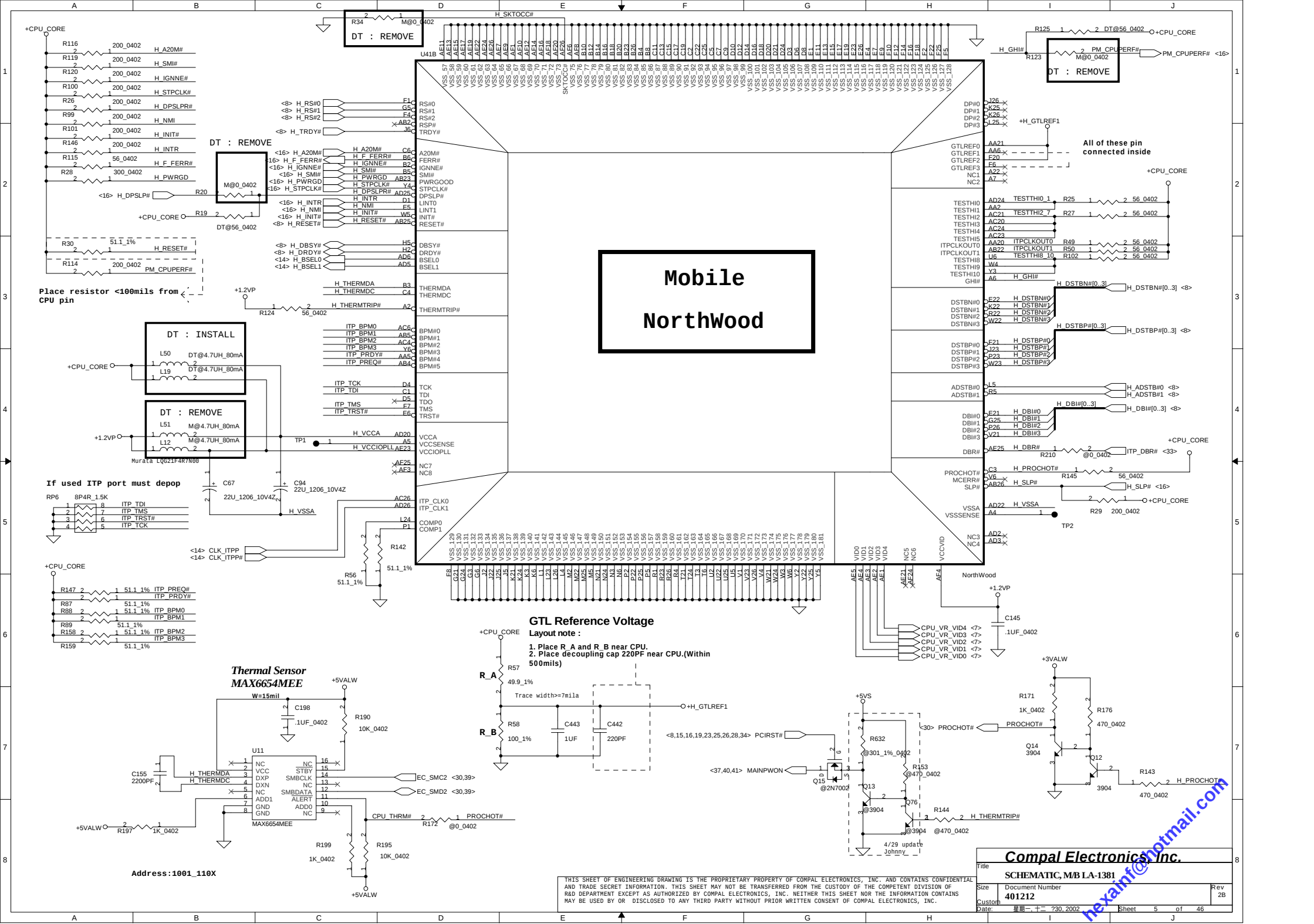
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hexainf@hotmail.com

Mobile NorthWood





Place close to CPU, Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

Three circuit diagrams are shown, each representing a power plane connection for a +CPU_CORE. Each diagram shows a series of capacitors connected between the power plane and a common ground (indicated by a triangle symbol).

- Diagram 1 (Top):** Shows a series of capacitors C80, C92, C104, C428, and C118. Each capacitor is labeled with its value: 10UF, 6.3V, 1206_X5R.
- Diagram 2 (Middle):** Shows a series of capacitors C128, C61, C59, C57, and C56. Each capacitor is labeled with its value: 10UF, 6.3V, 1206_X5R.
- Diagram 3 (Bottom):** Shows a series of capacitors C429, C430, C423, and C53. Each capacitor is labeled with its value: 10UF, 6.3V, 1206_X5R.

Three circuit diagrams are shown, each representing a different configuration for connecting a CPU_CORE to a common ground through a series of capacitors. Each diagram consists of a top rail connected to CPU_CORE and a bottom rail connected to ground. Capacitors are connected between the rails at various points.

- Diagram 1 (Top):** Shows a top rail connected to CPU_CORE and a bottom rail connected to ground. Capacitors are connected between the rails at various points. The capacitors are labeled with their values and part numbers: C123 (10UF_6.3V_1206_X5R), C115 (10UF_6.3V_1206_X5R), C159 (10UF_6.3V_1206_X5R), C116 (10UF_6.3V_1206_X5R), and C448 (10UF_6.3V_1206_X5R).
- Diagram 2 (Middle):** Shows a top rail connected to CPU_CORE and a bottom rail connected to ground. Capacitors are connected between the rails at various points. The capacitors are labeled with their values and part numbers: C447 (10UF_6.3V_1206_X5R), C83 (10UF_6.3V_1206_X5R), C495 (10UF_6.3V_1206_X5R), C174 (10UF_6.3V_1206_X5R), and C175 (10UF_6.3V_1206_X5R).
- Diagram 3 (Bottom):** Shows a top rail connected to CPU_CORE and a bottom rail connected to ground. Capacitors are connected between the rails at various points. The capacitors are labeled with their values and part numbers: C176 (10UF_6.3V_1206_X5R), C426 (10UF_6.3V_1206_X5R), C427 (10UF_6.3V_1206_X5R), and C55 (10UF_6.3V_1206_X5R).

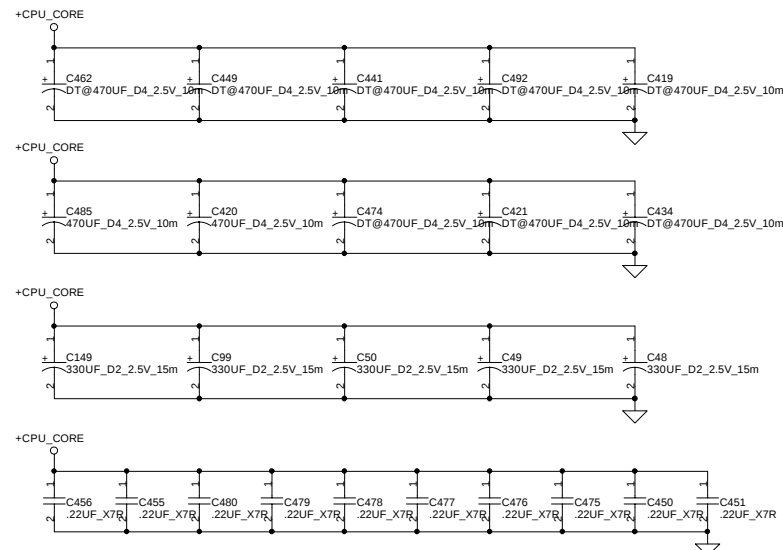
PAD1

 1

PAD-2.5X3

Place close to CPU power and ground pin as possible (<1inch)

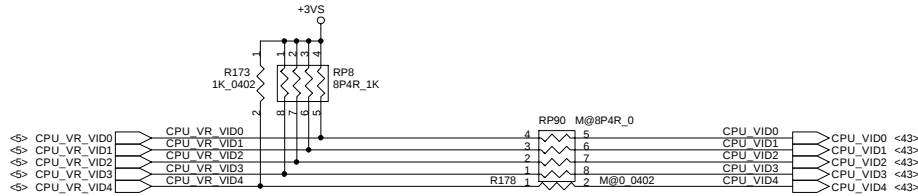
For Mobile's CPU:
ESR total=1.875m ohm
C total=2590uF

[illegible][illegible]

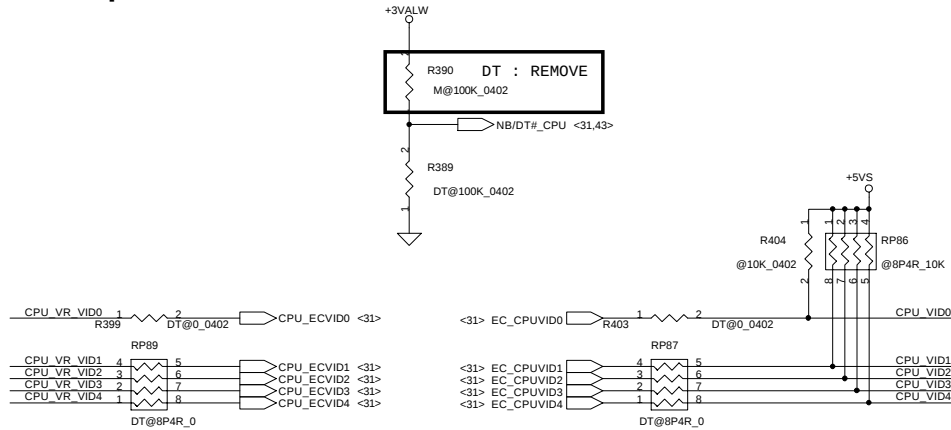
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For Mobile CPU

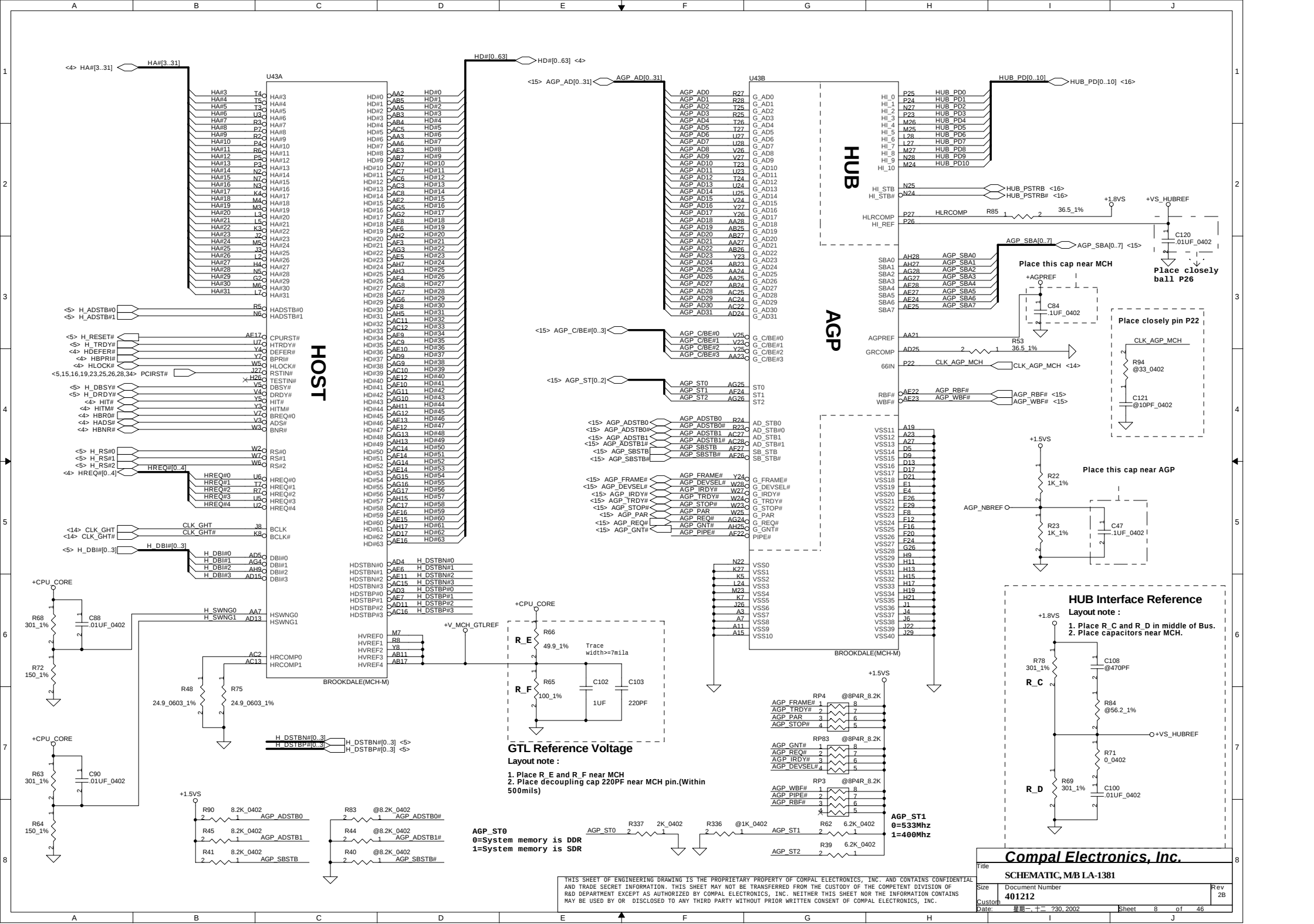


For Desktop CPU

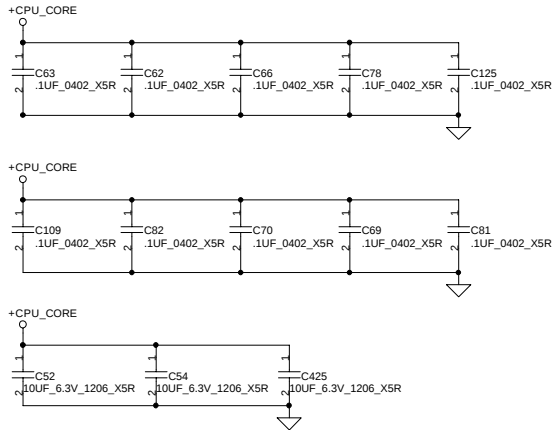


	Mobil CPU					Destop CPU				
NB/DT_CPU	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	1	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	0	1	X	X	X	X	X
0.775V	1	1	0	1	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off						1	1	1	1	1

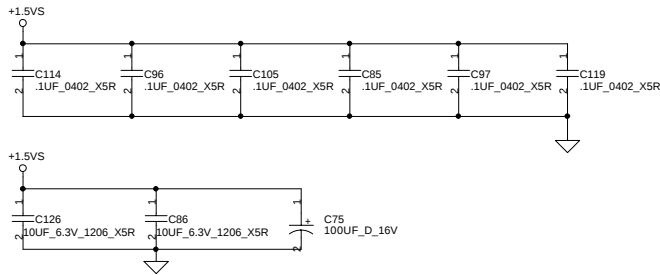
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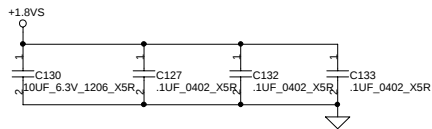
Layout note : Processor system bus
Distribute as close as possible
to MCH Processor Quadrant.(between VTTFSB and VSS pin)



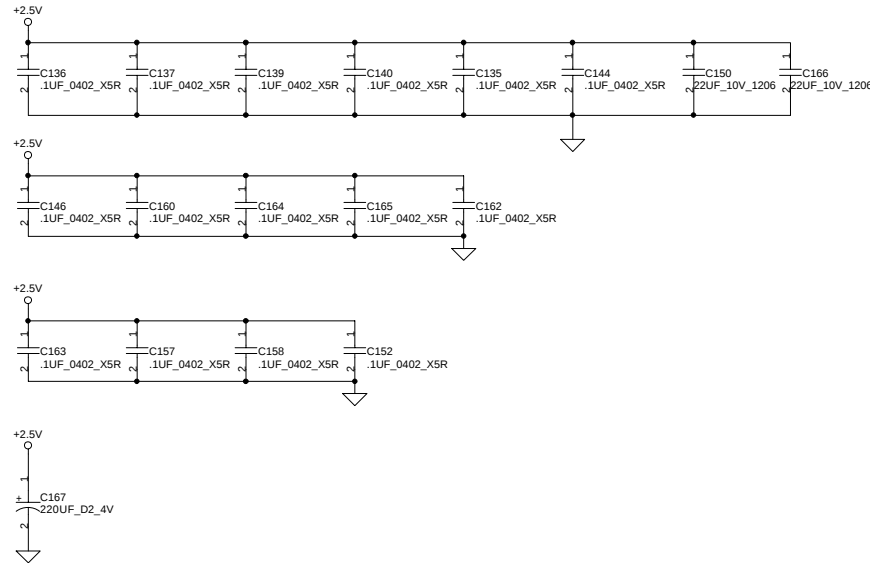
Layout note : AGP/CORE
Distribute as close as possible
to MCH Processor Quadrant.(between VCCAGP/VCCCORE
and VSS pin)



Layout note : Hub-Link
Distribute as close as possible
to MCH Processor Quadrant.(between VCCHL and VSS pin)



Layout note : DDR Memory interface
Distribute as close as possible
to MCH Processor Quadrant.(between VCCSM and VSS pin)

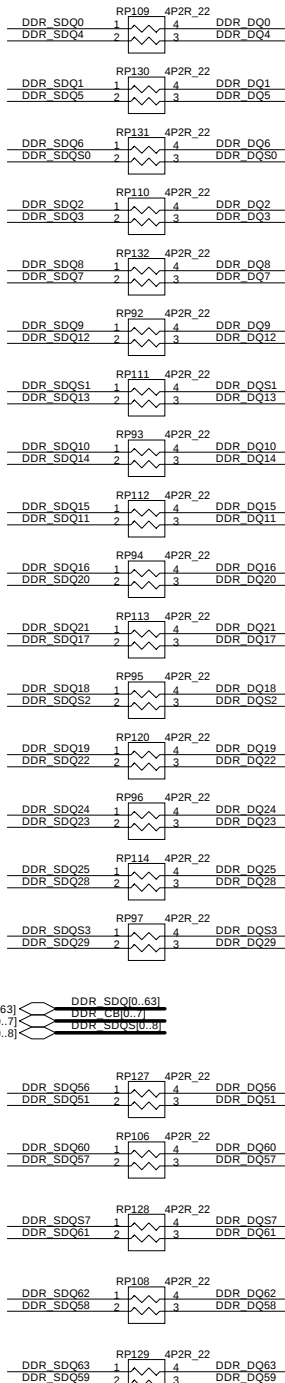


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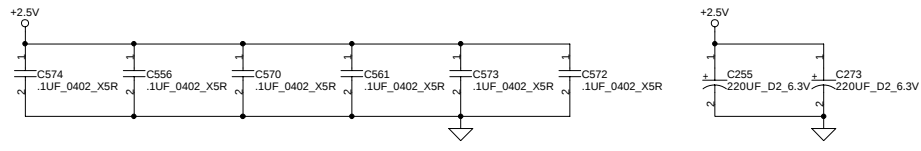
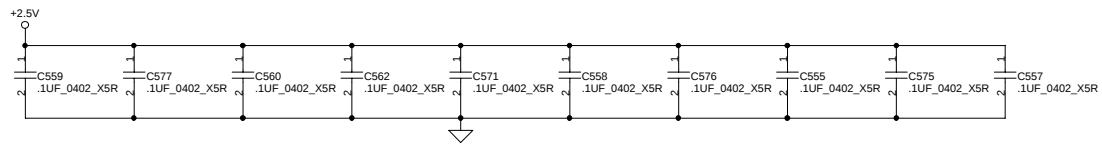
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Layout note

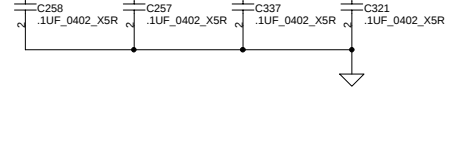
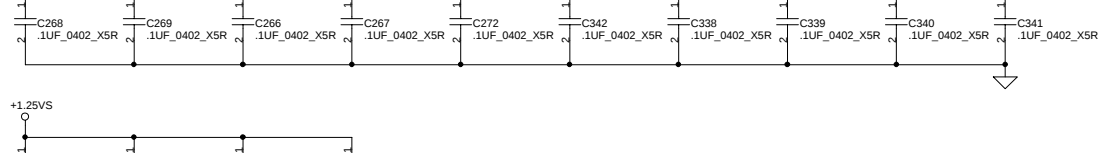
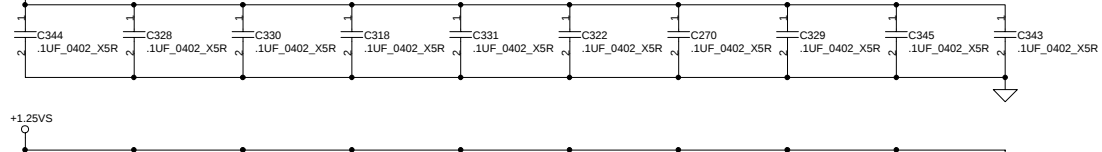
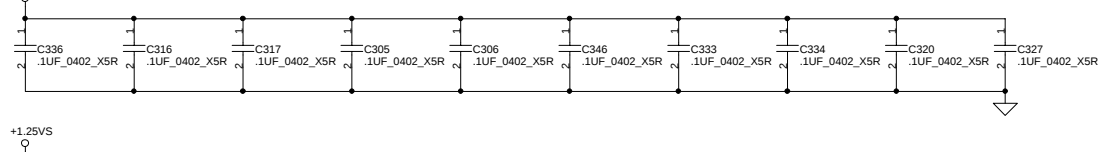
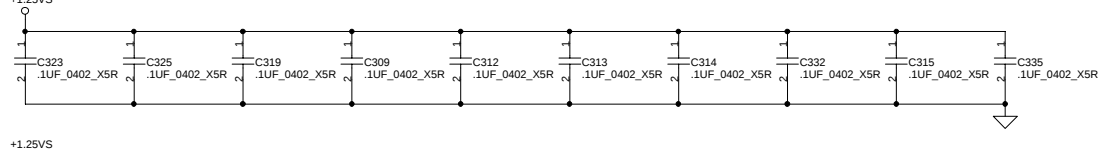
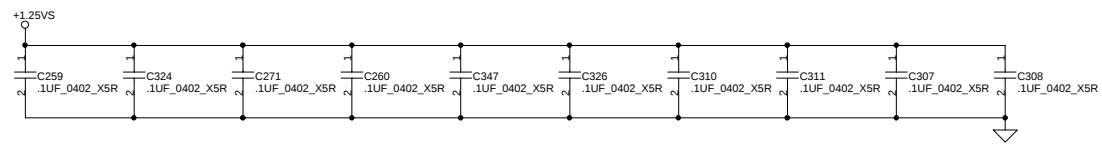
Place these resistor
closely DIMM0,
all trace length<750mil



Layout note :
Distribute as close as possible
to DDR-SODIMM.



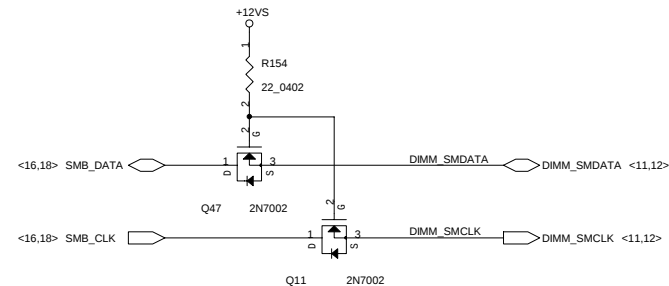
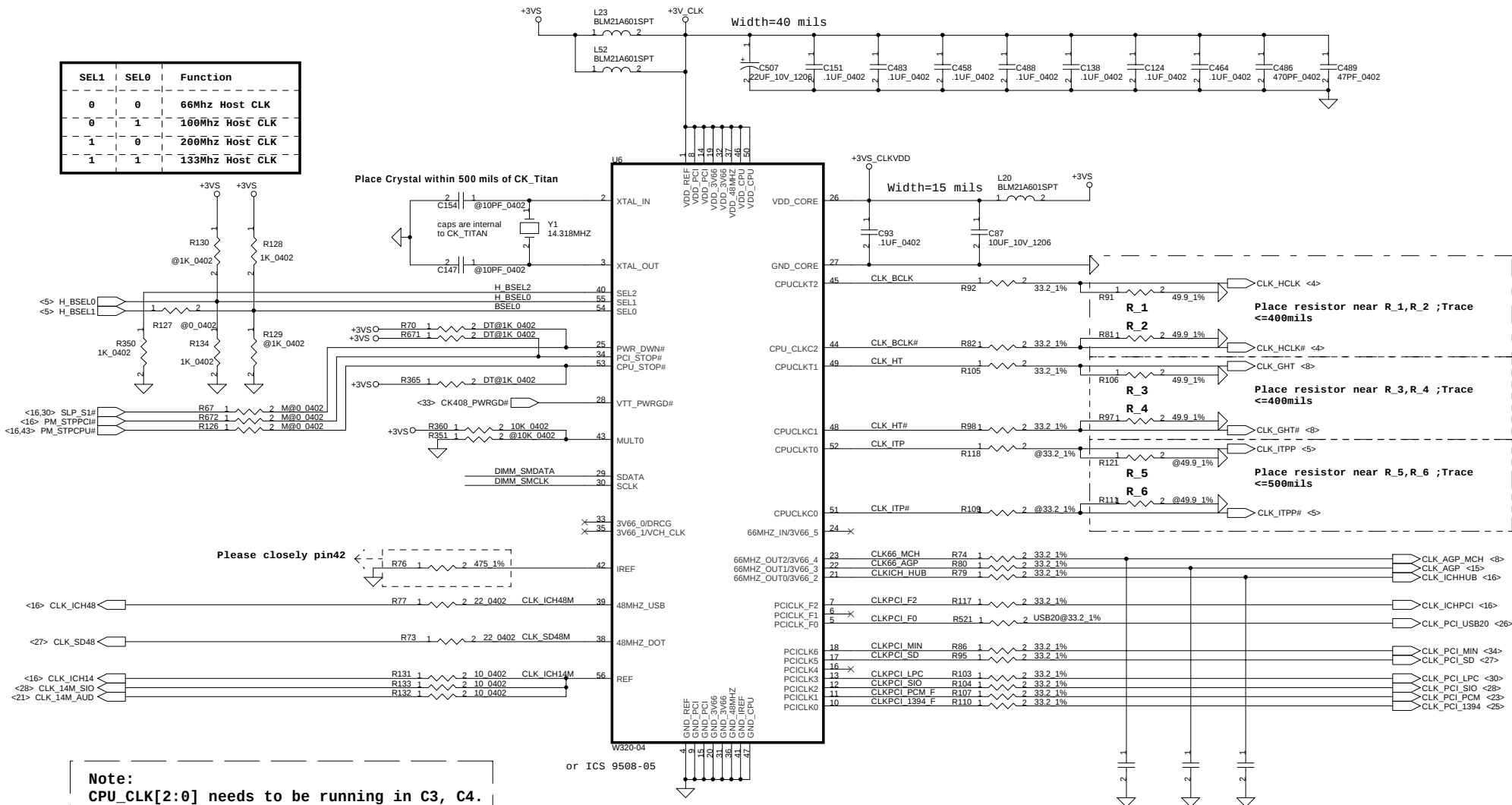
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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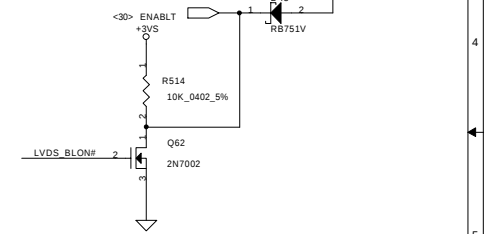
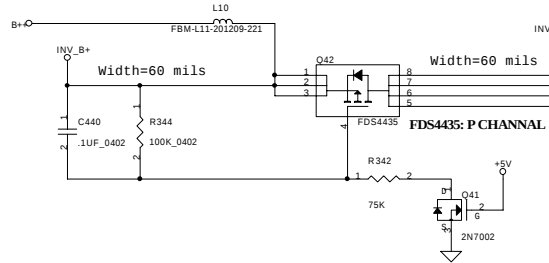
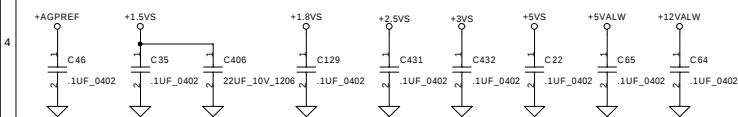
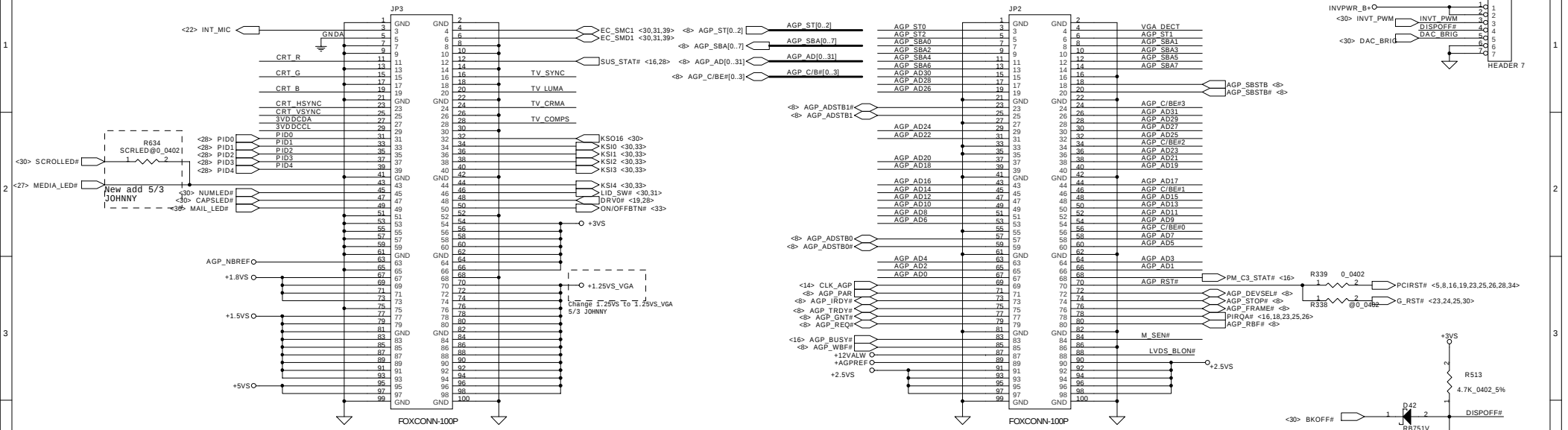
SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



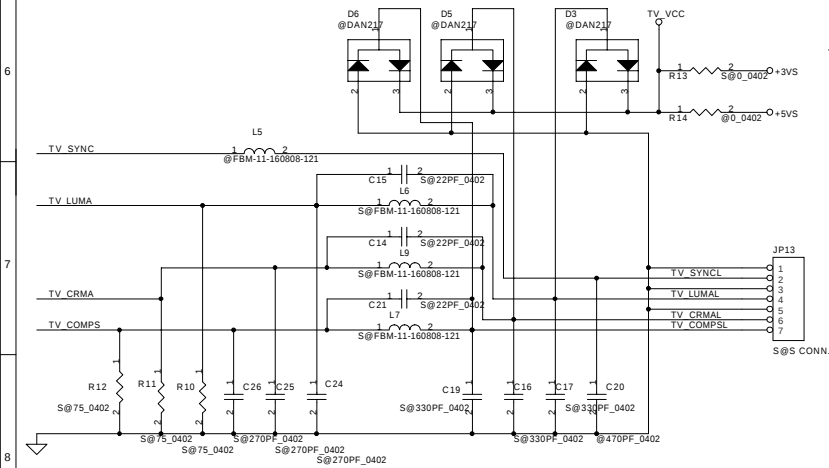
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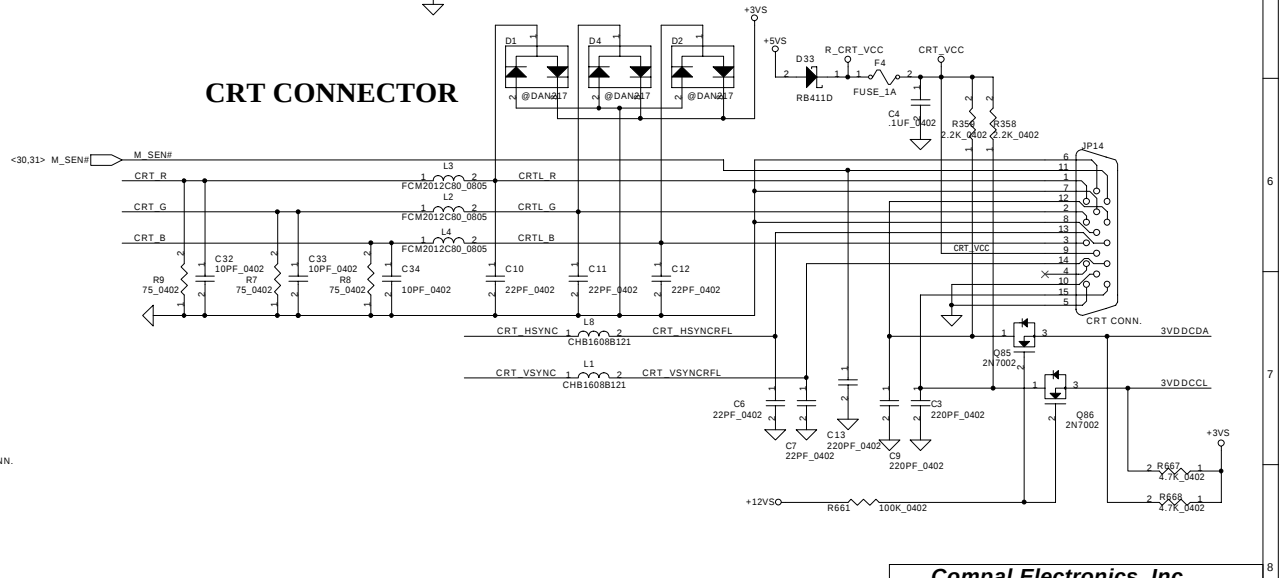
AGP 100X2 Pin connector

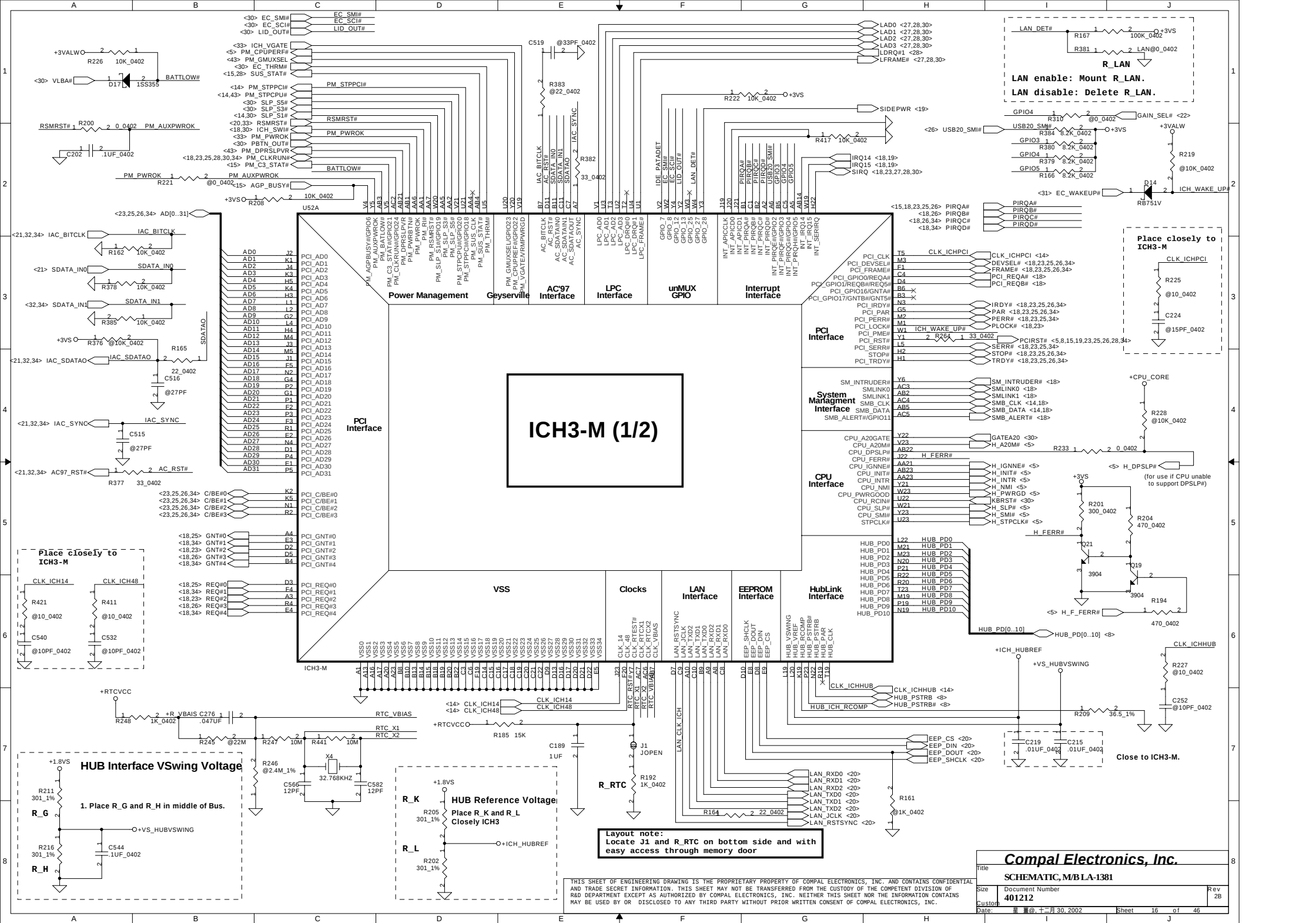


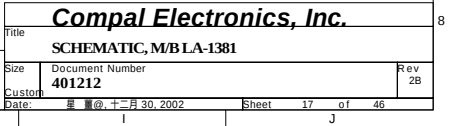
TV_OUT CONNECTOR

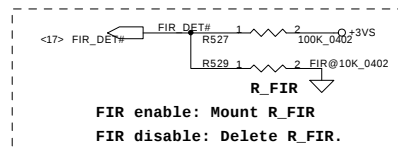
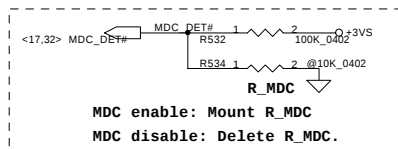
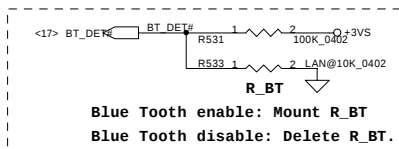
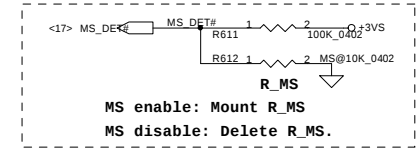
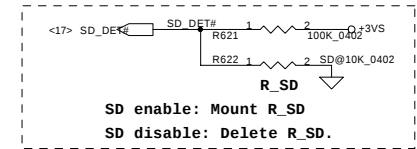
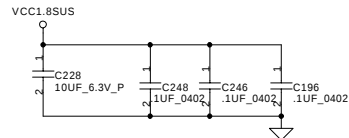
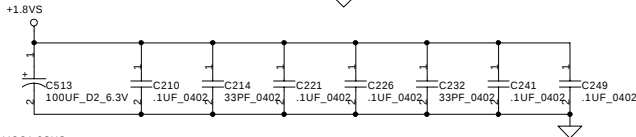
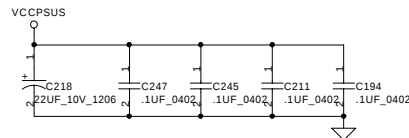
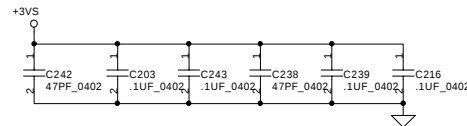
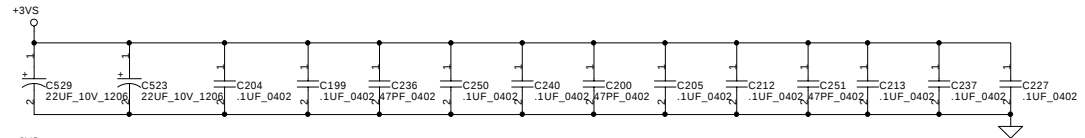
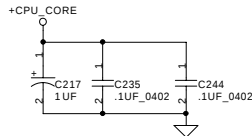
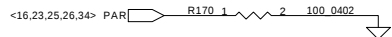
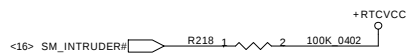
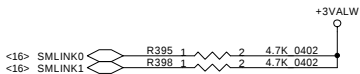
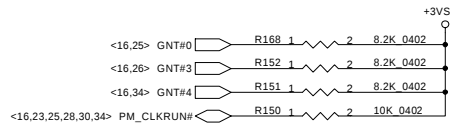
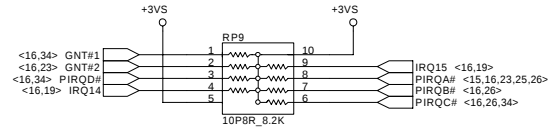
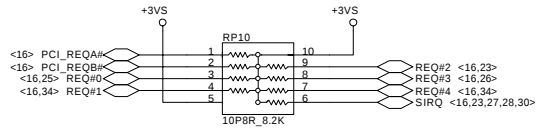
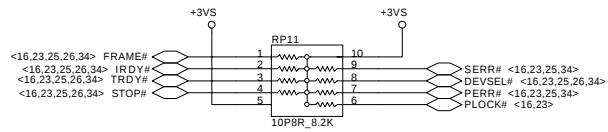


CRT CONNECTOR





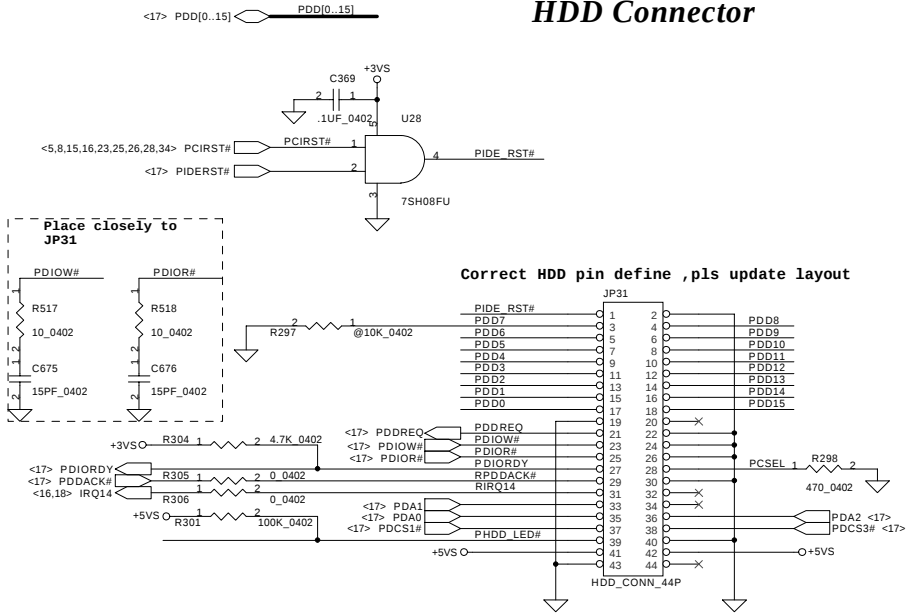




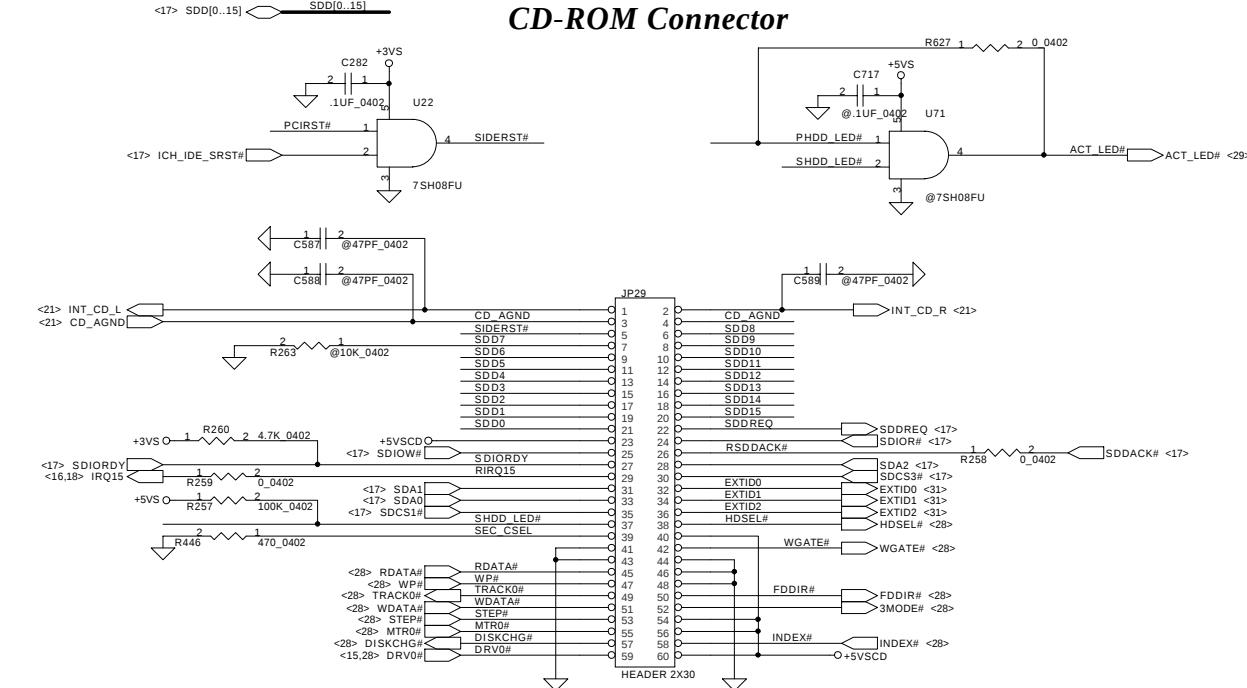
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HDD Connector



CD-ROM Connector



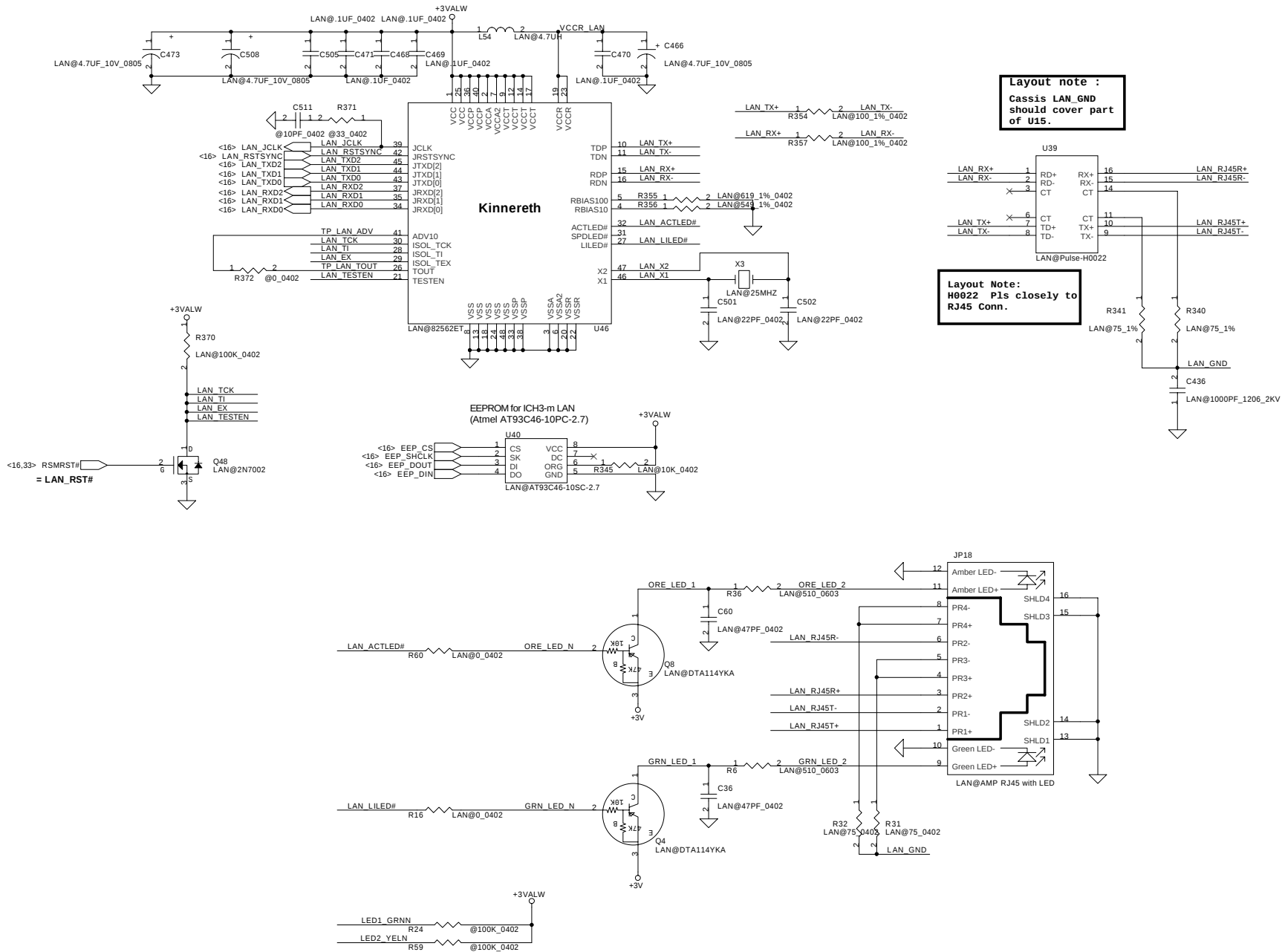
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FDD	0	0	0
CD-ROM	0	0	1
LS-120	0	1	0
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NONE	1	1	1

Compal Electronics, Inc.

SCHEMATIC, MBLA-1381

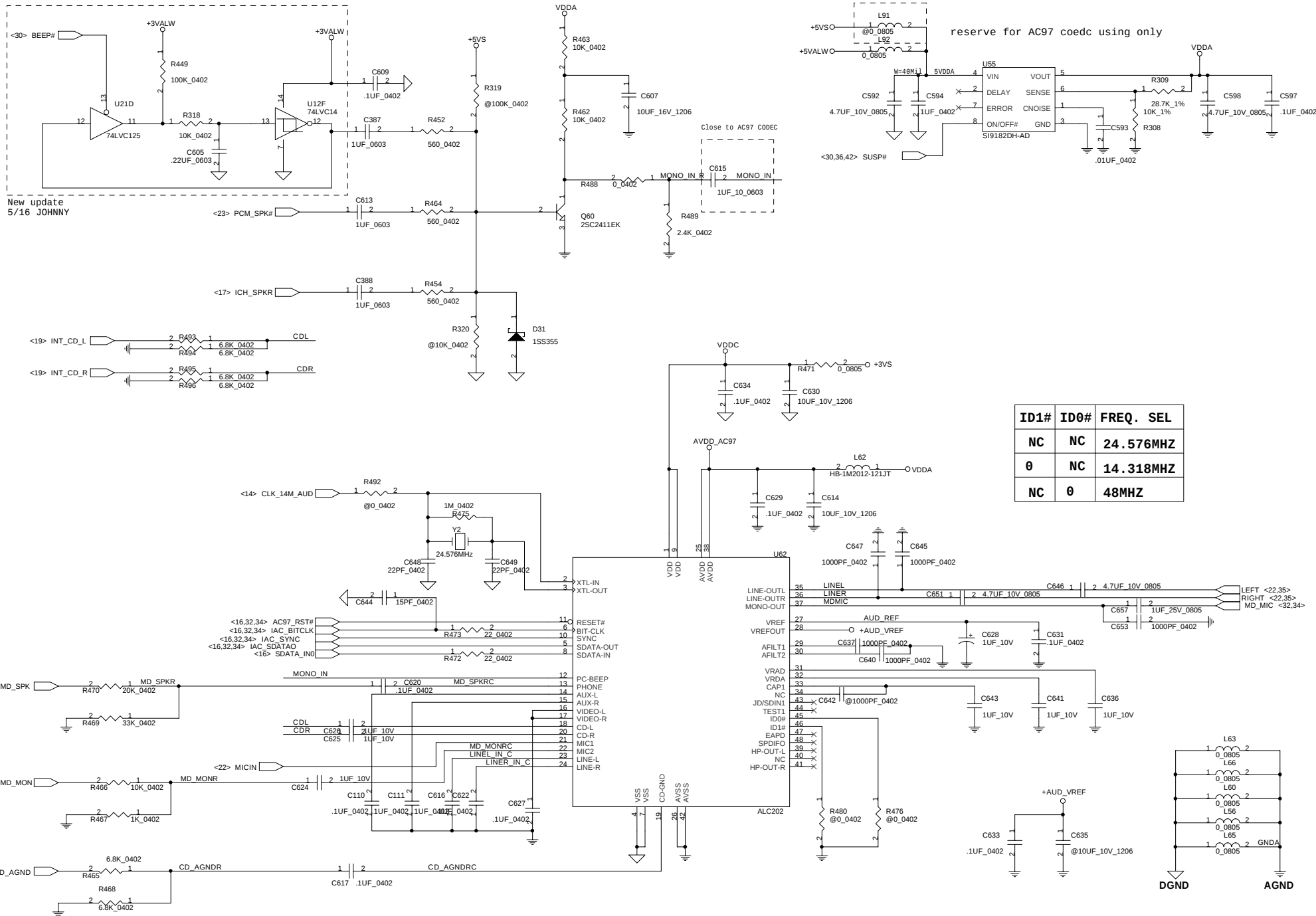
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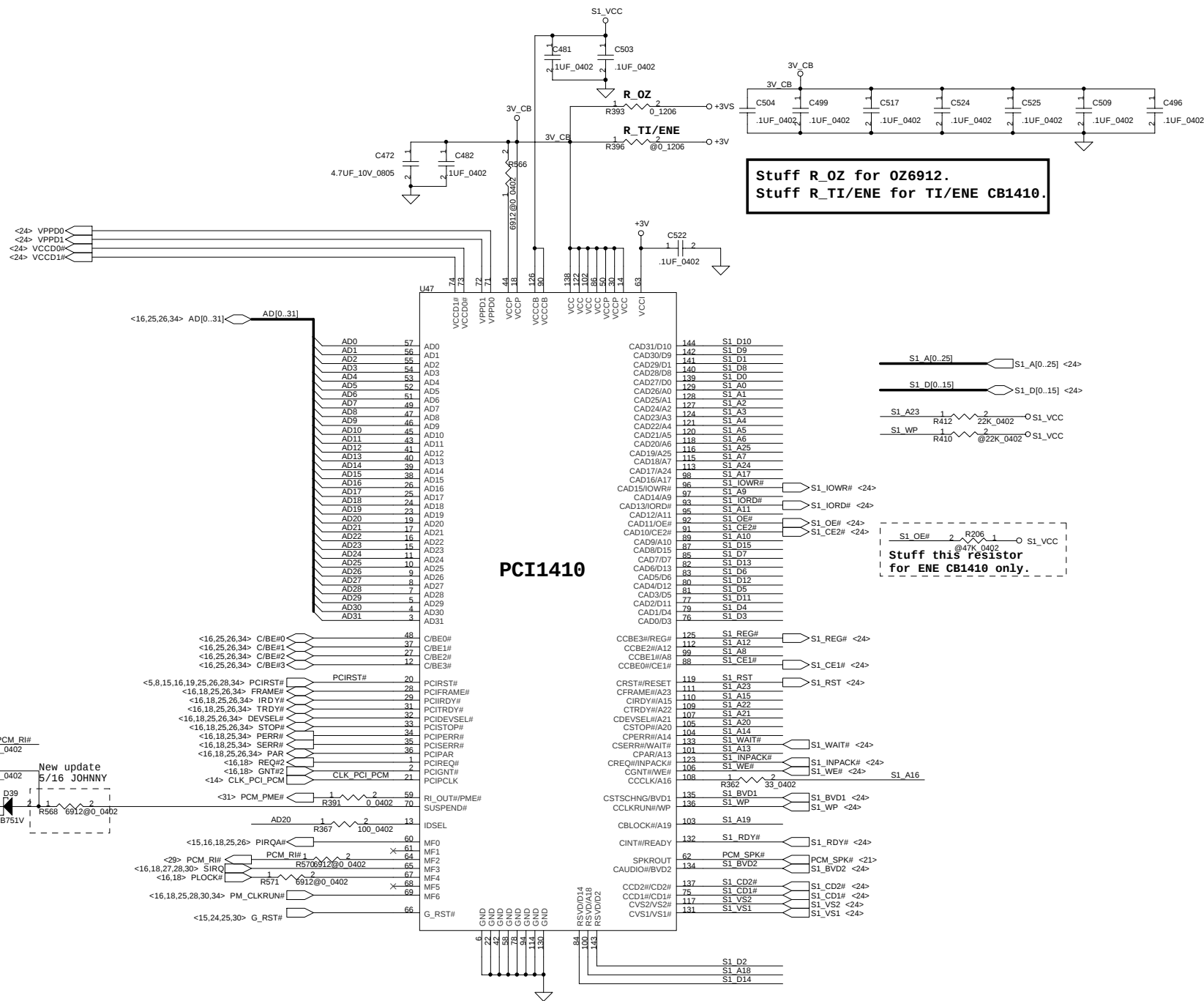
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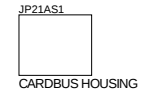
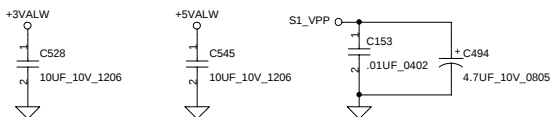
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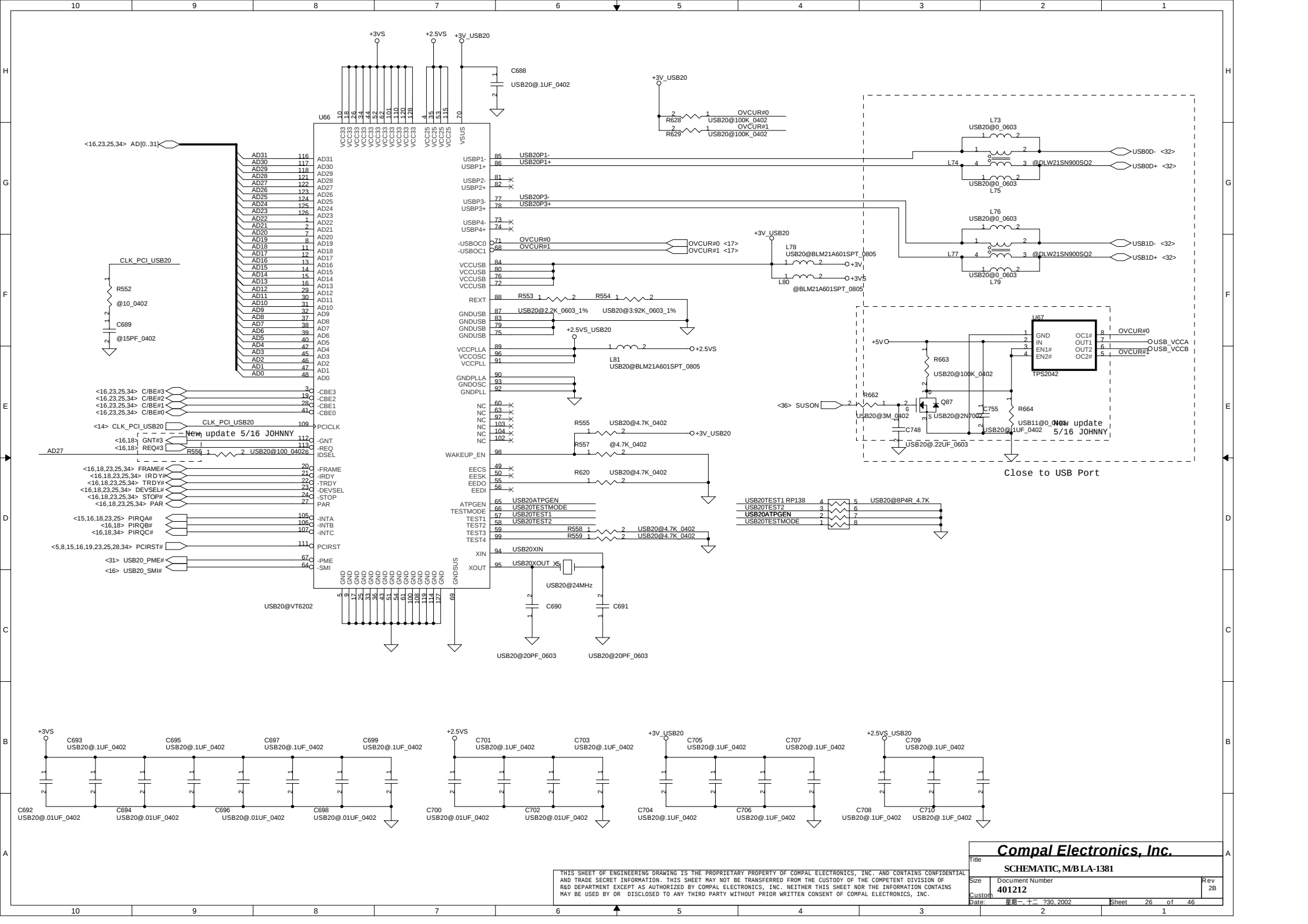


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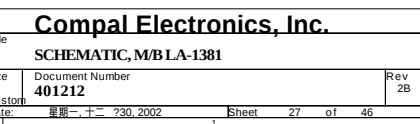






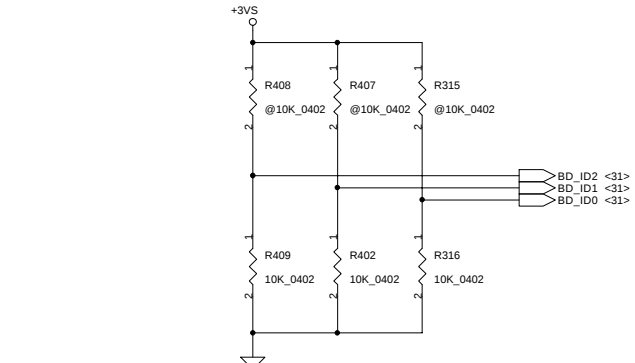
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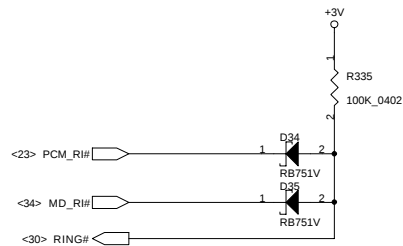
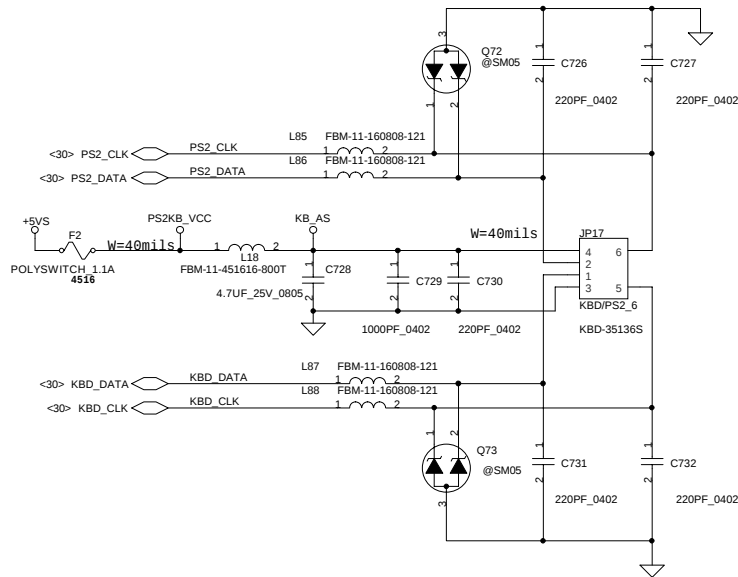
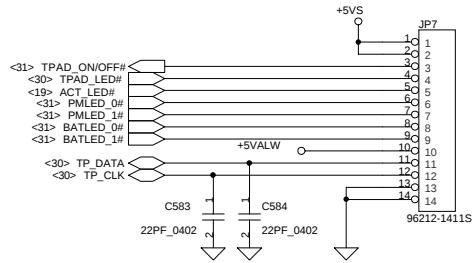
BOARD ID



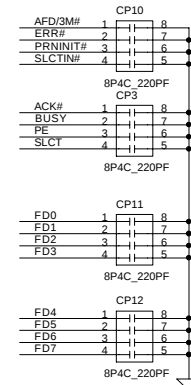
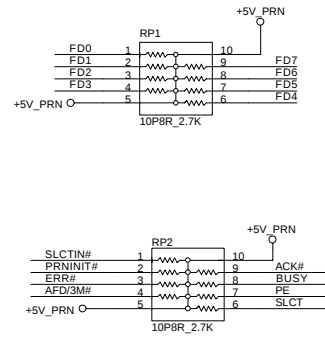
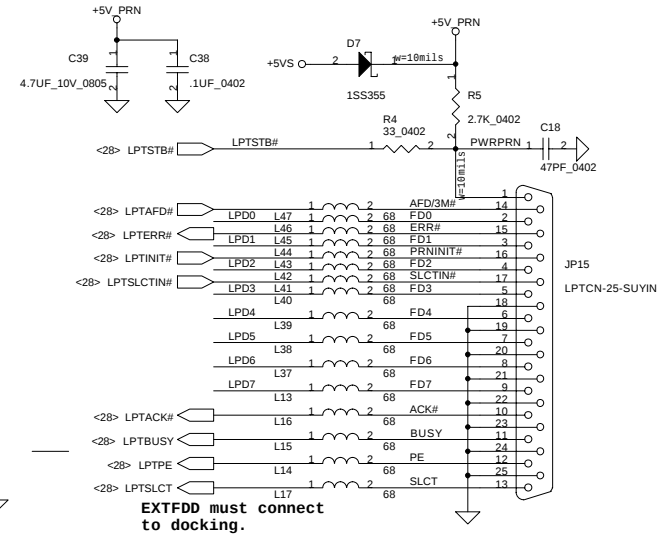
The schematic diagram illustrates the 80486 system bus architecture. It features three 80486 processors (RP141, RP91, and RP85) and a 10B8P 1K memory module. The bus is connected to a 10B8P 1K memory module. The bus is connected to a 10B8P 1K memory module. The bus is connected to a 10B8P 1K memory module. The bus is connected to a 10B8P 1K memory module.

[illegible]

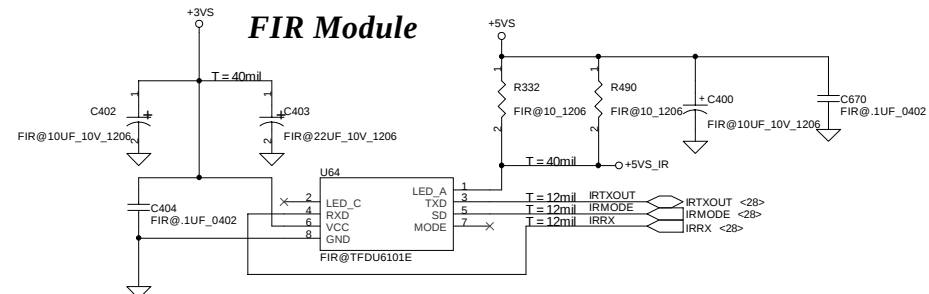
Touch Pad & Status LED Conn.



Parallel Port

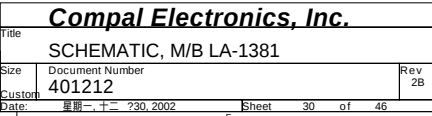


FIR Module

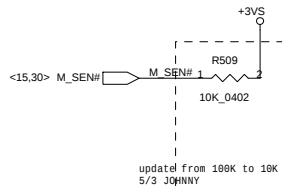
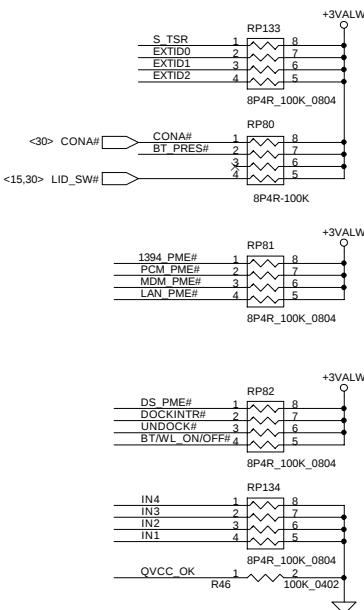
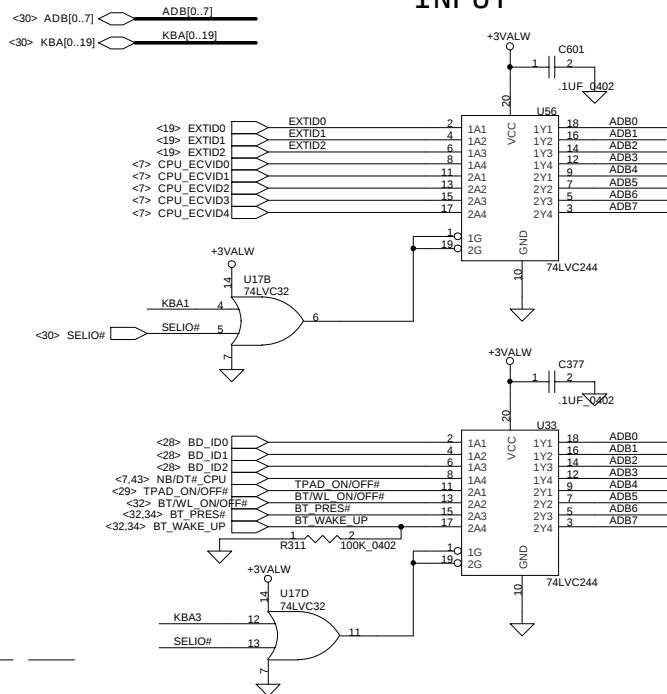


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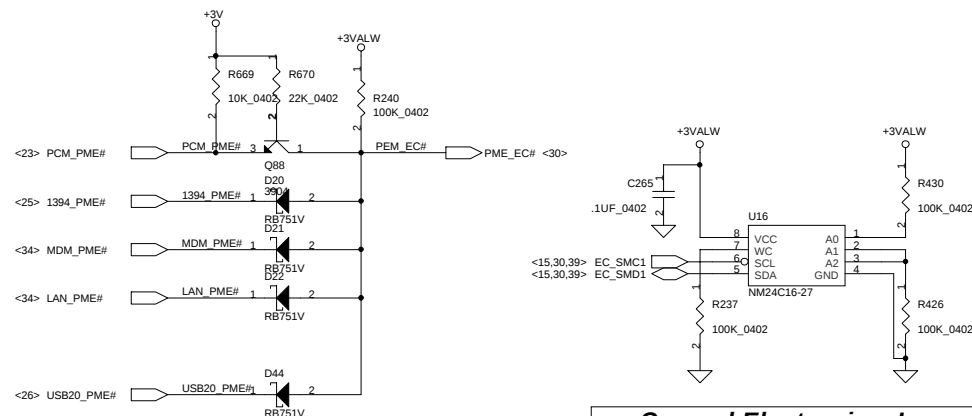
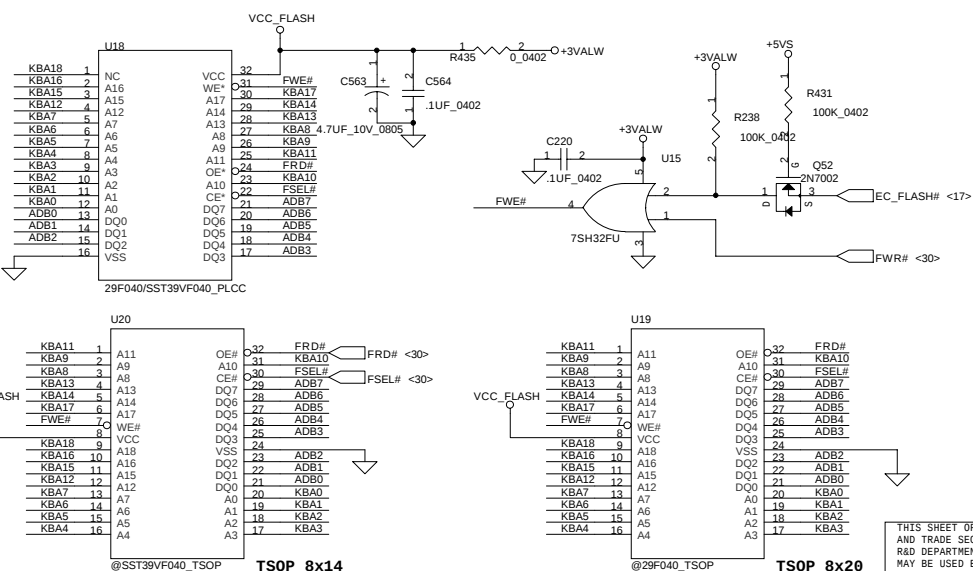
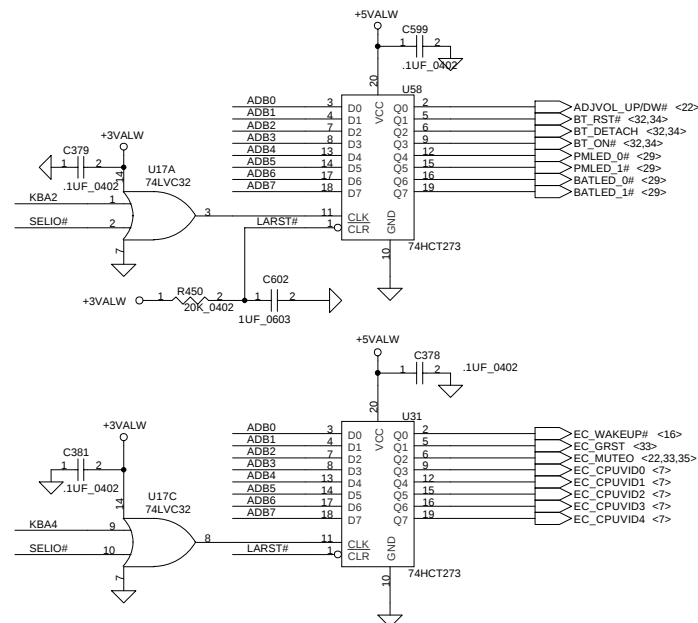
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INPUT



OUTPUT



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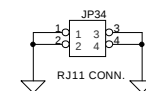
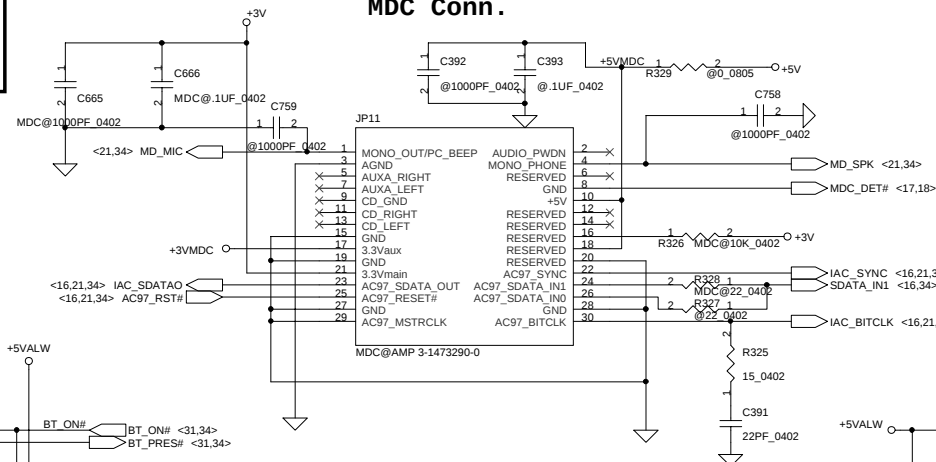
Compal Electronics, Inc.

SCHEMATIC, M/B LA-1381

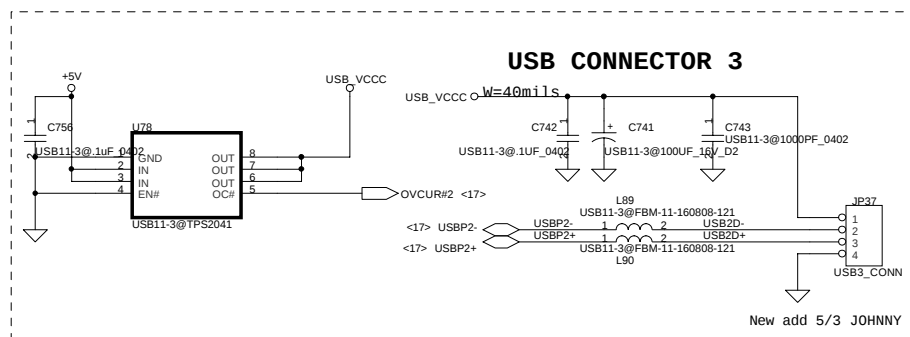
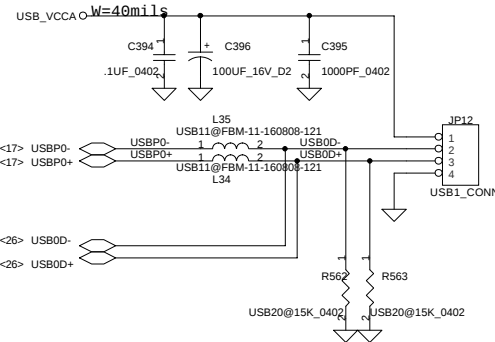
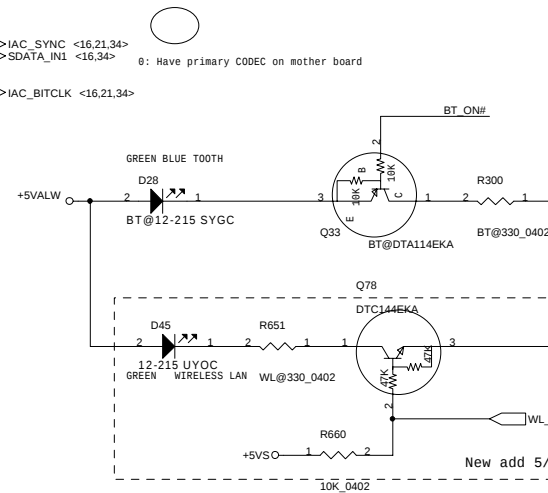
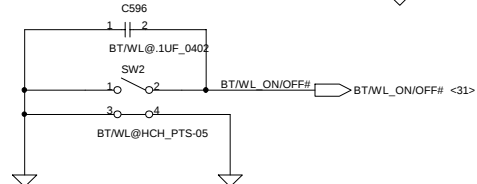
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Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem



Bluetooth Connector



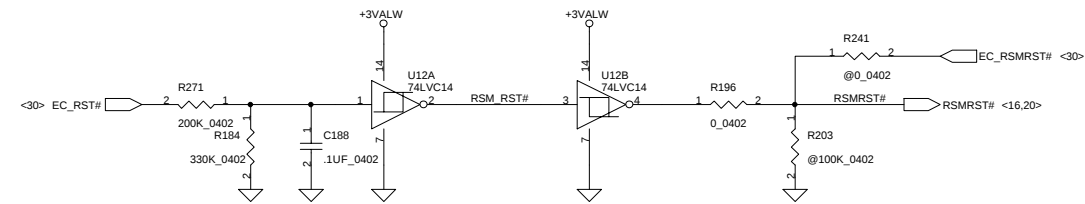
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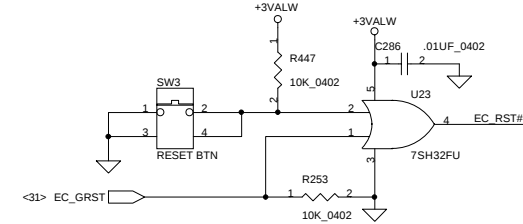
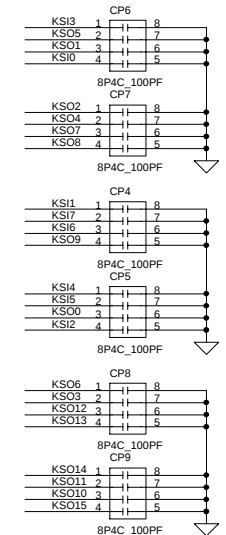
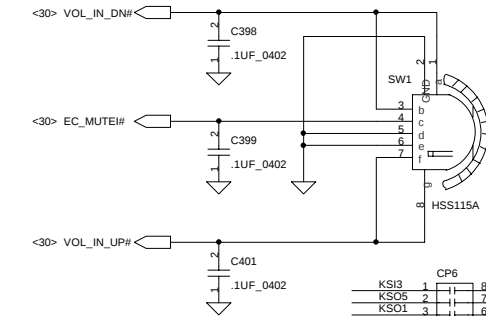
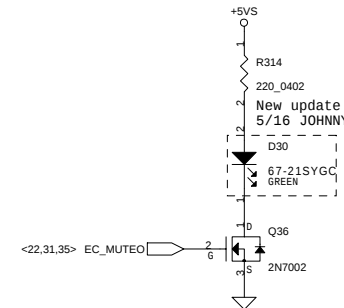
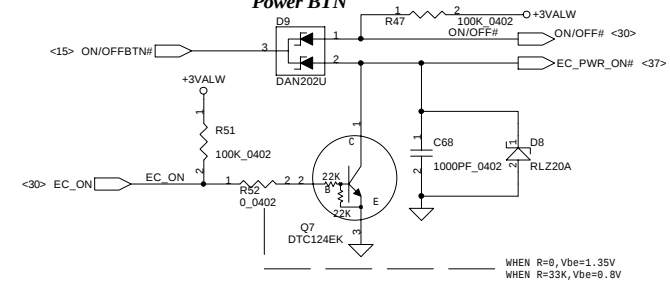
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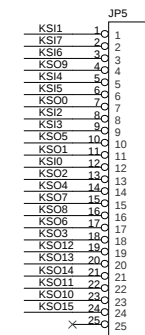
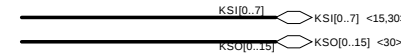
Power ON Circuit



Reset Button

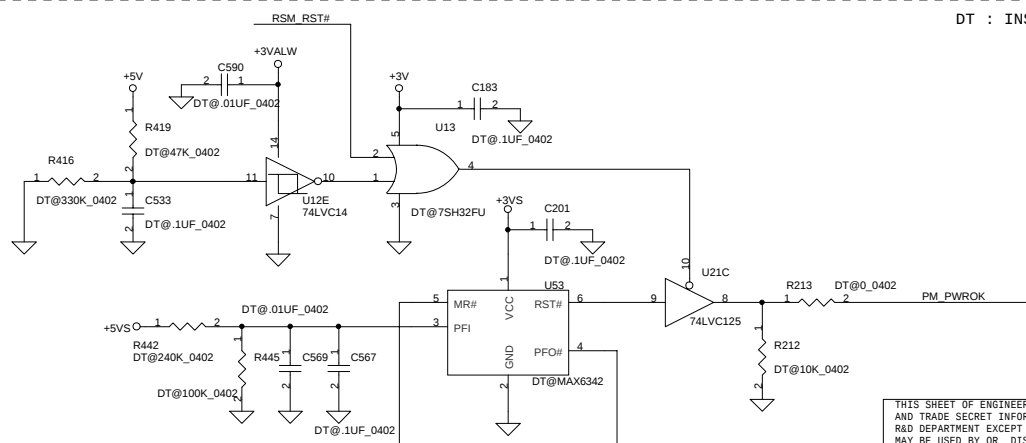
**Power BTN**

INT_KBD CONN.



INT_KB_CONN

DT : INSTALL



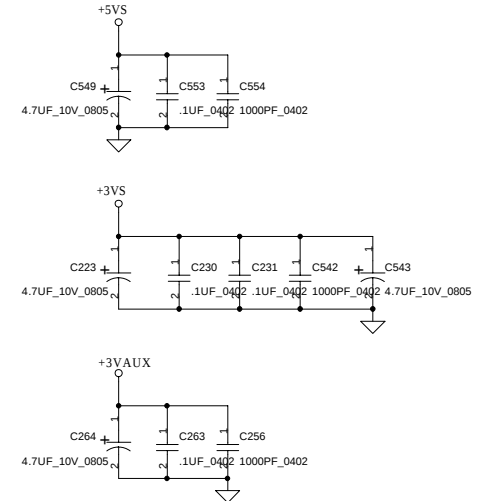
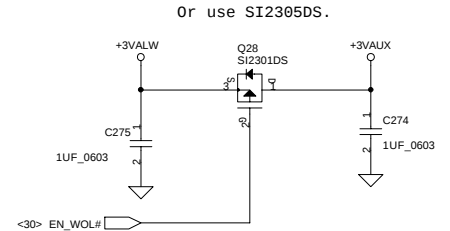
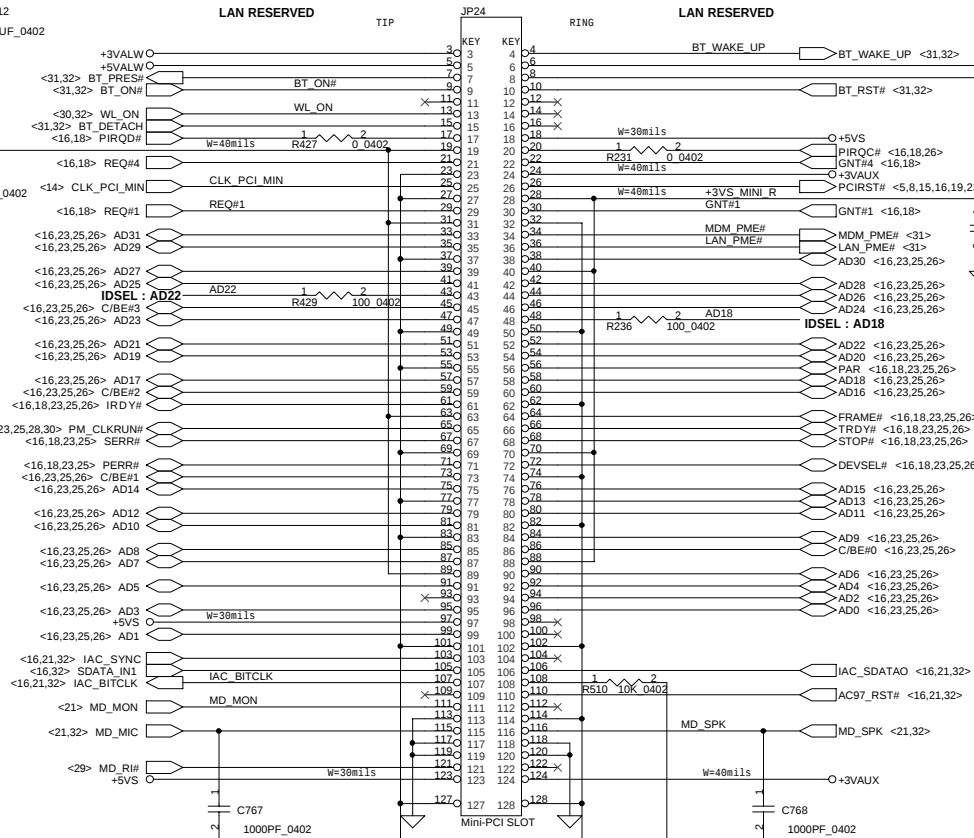
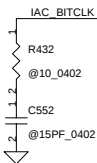
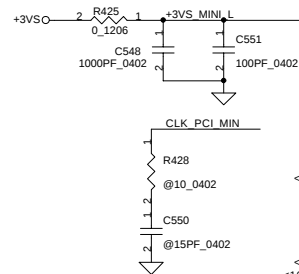
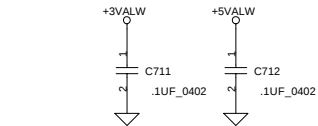
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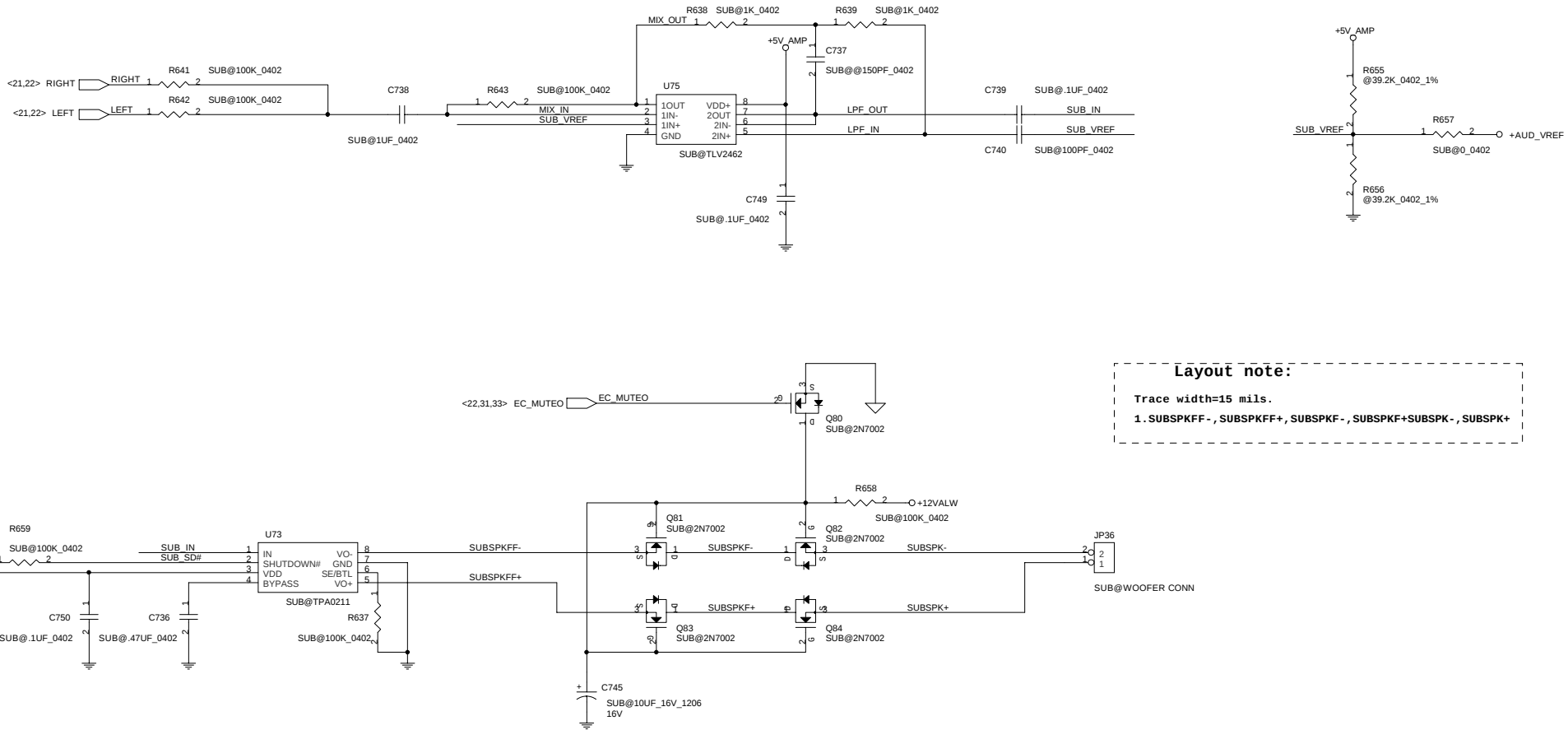
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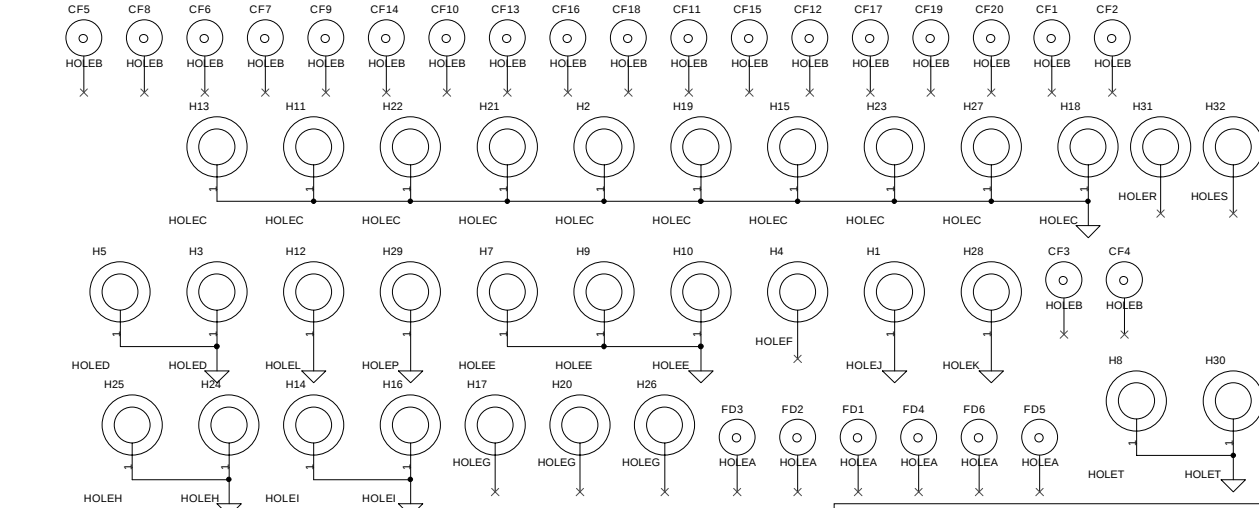
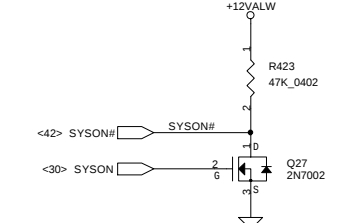
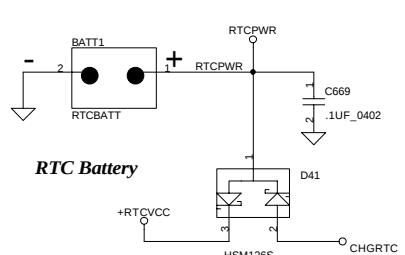
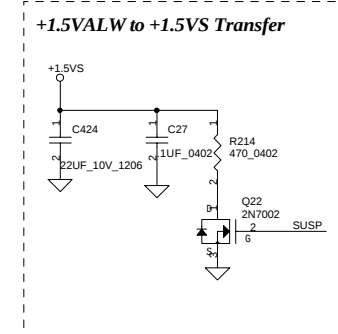
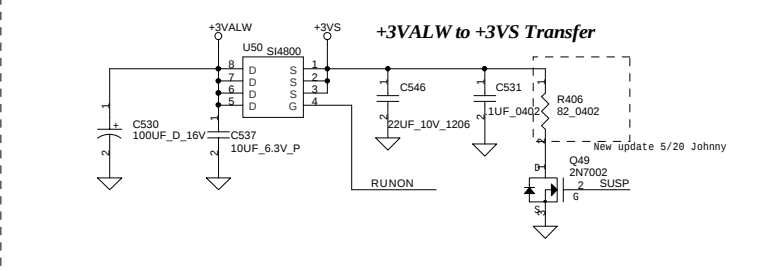
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Layout note:
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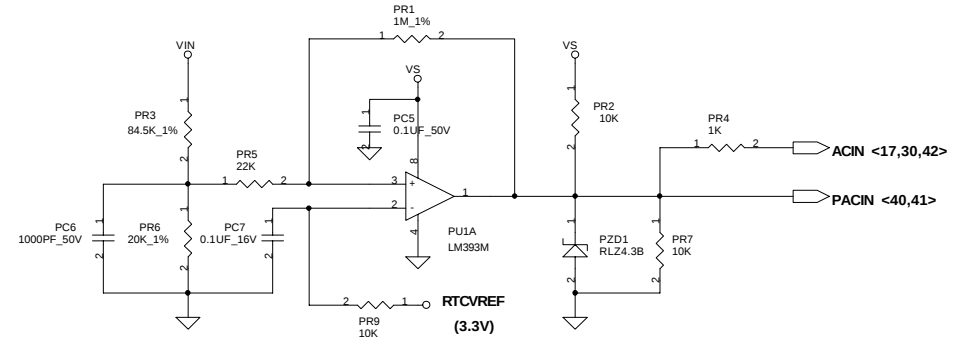
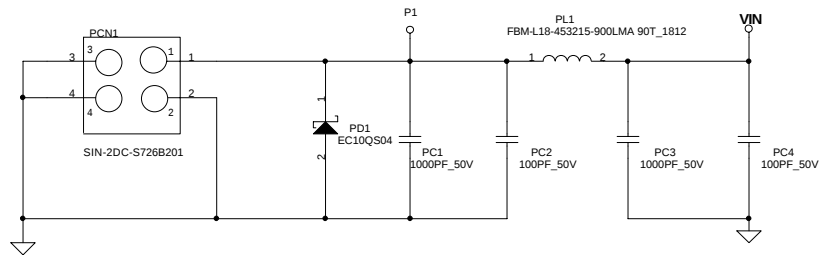
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Vin Detector

High 18.784 17.901 17.077 V
Low 17.877 17.043 16.195 V

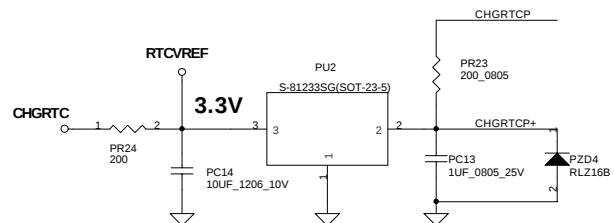
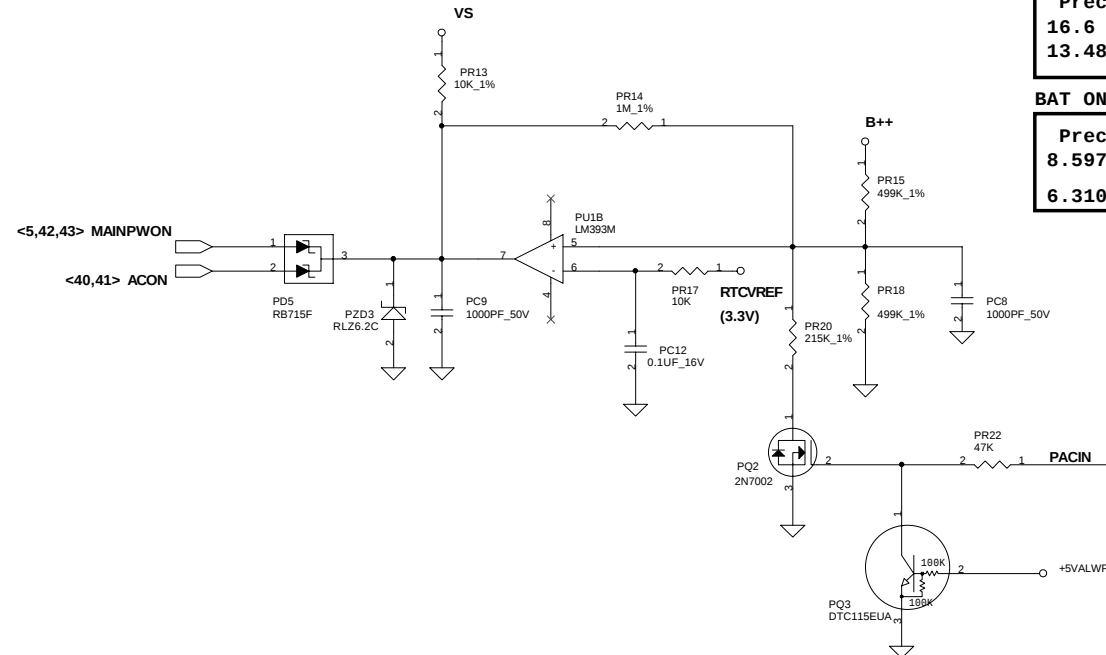
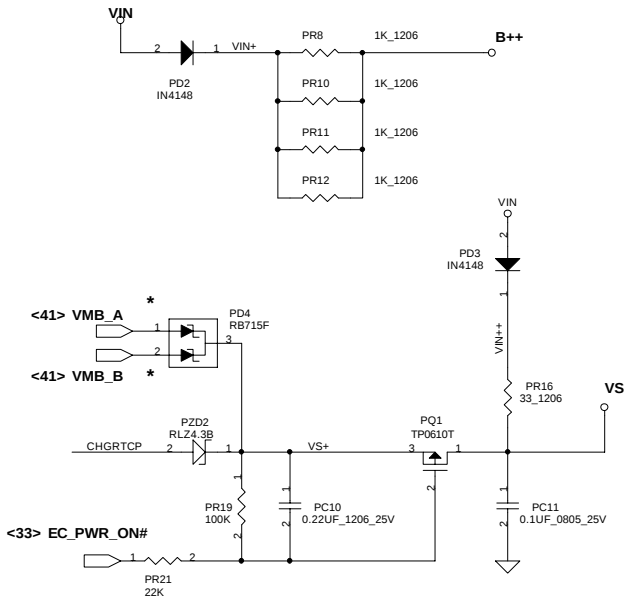


ACIN

Precharge detector		
16.6	15.9	15.2
13.48	12.93	12.09

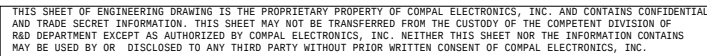
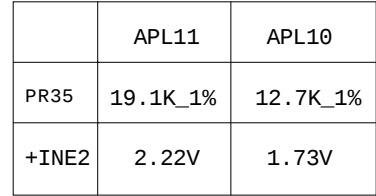
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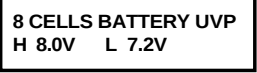
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8.597	8.247	7.904
6.310	6.101	5.683



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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

+1.25V+ -5%

M7C
+1.25VS_VGA

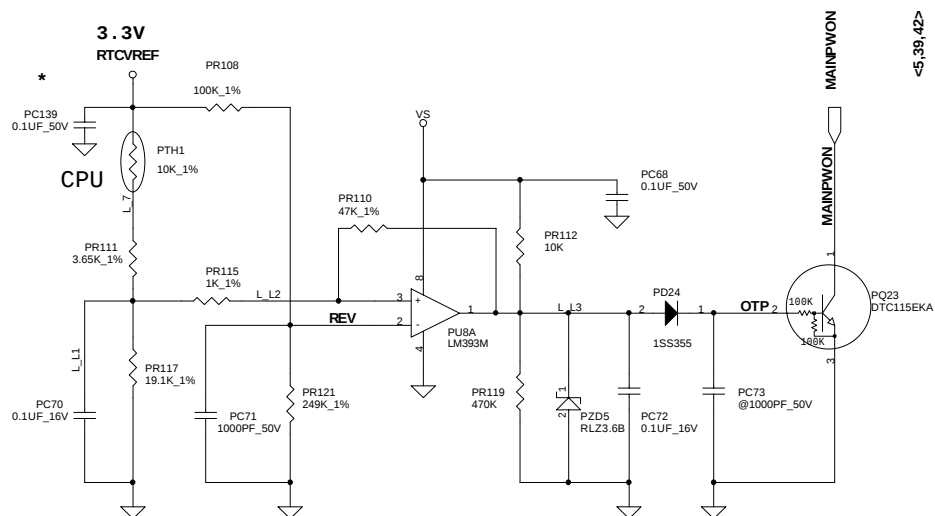
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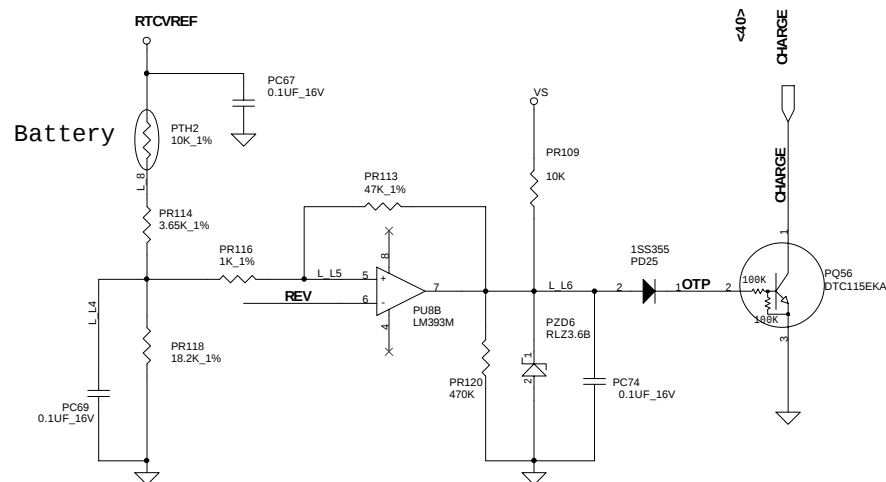
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PTH1 under CPU botten side :
CPU thermal protection at 84(85)+-3 degree C
Recovery at 36(37)+-3 degree C



PTH2 near main Battery CONN :
BAT. thermal protection at 90(91)+-3 degree C
Recovery at 39(40)+-3 degree C



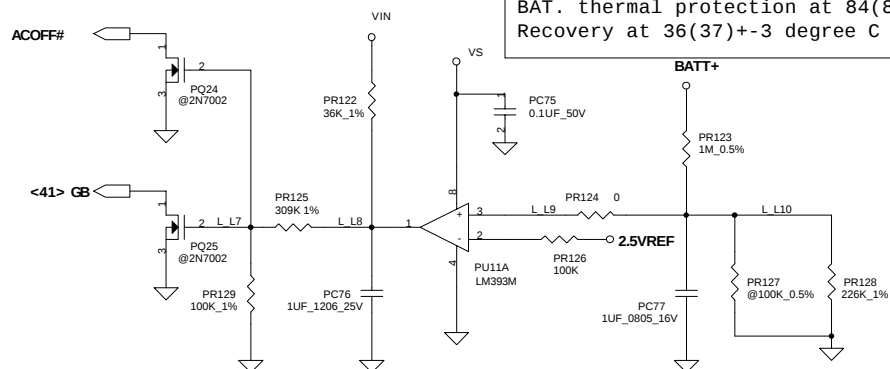
BATTERY Charger OVP : 13.56V

APL10 PR117 18.7K

PTH1 under CPU botten side :
CPU thermal protection at 87(88)+-3 degree C
Recovery at 37(38)+-3 degree C

APL10 PR118 19.1K

PTH2 near main Battery CONN :
BAT. thermal protection at 84(85)+-3 degree C
Recovery at 36(37)+-3 degree C



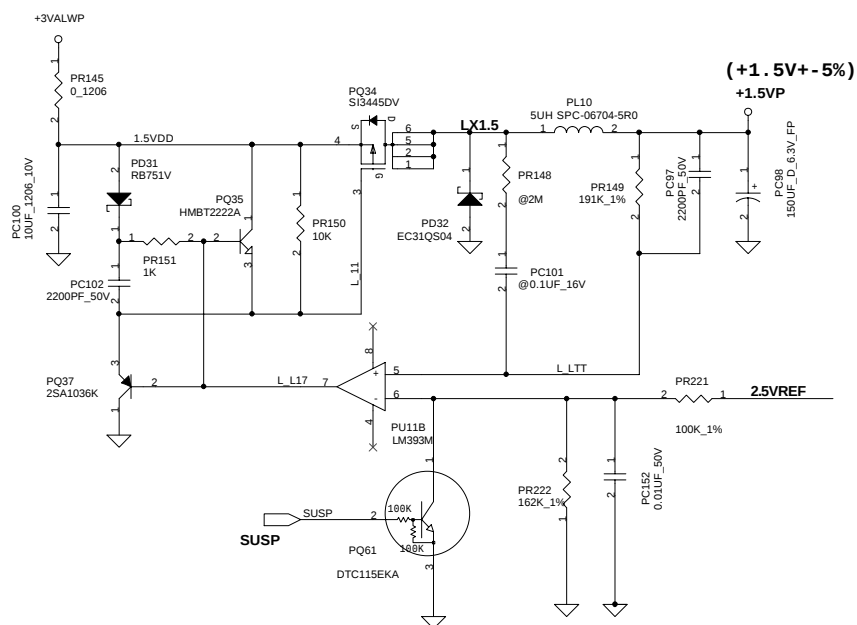
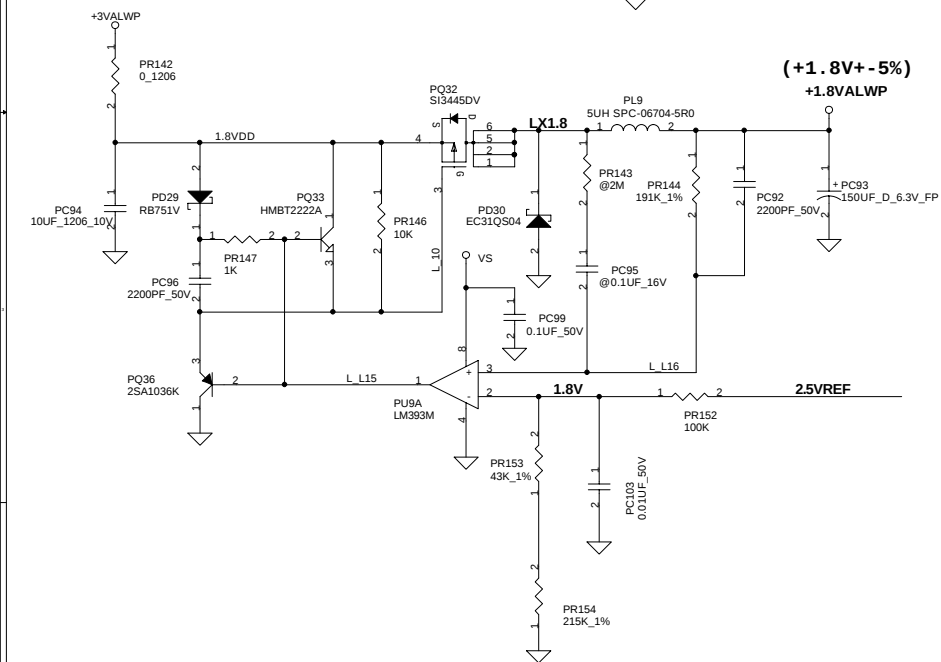
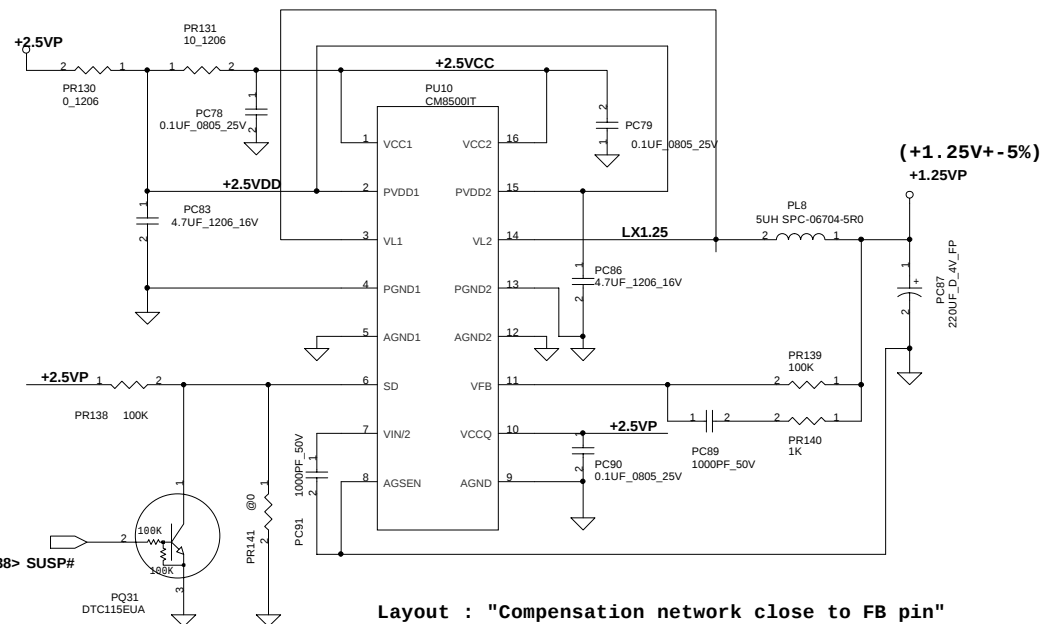
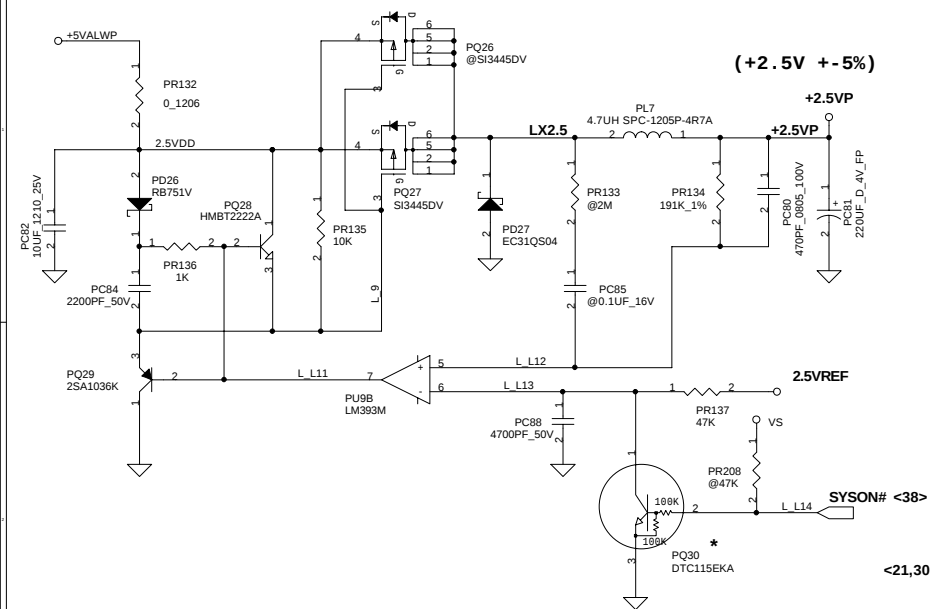
Please refer to Page. 45

APL10 nonpop components for cpu_core

PU15;PQ51;PQ52;PQ54;PQ55;PD39;PD38;PL14;PC130;
PC132;PC133;PC131;PC134;PC135;PC129;PC128;
PR193;PR194;PR196;PR199;PR197;PR192;PR195;
PR200;PR198, PR223

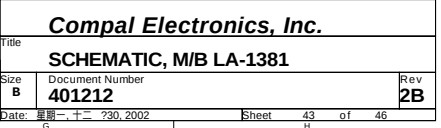
APL11 nonpop components for mobile

PR171, PR172, PQ42, PR177, PQ43, PQ44, PR207, PR184,
PQ49, PR204, PQ59, PR205, PQ50



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	GMUXSEL	STPCPU#	DPRSLPVR	VCORE1	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.2309V
BM	0	1	0	1.20V	2.6%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	B.Ver #	Phase
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Footprint error	4	Change R96 footprint to 0402	0.2
			5	Change RP6 footprint to 0402	
			7	Change RP8, RP86, RP87, RP89 and RP90 footprint to 0402	
			27	Change RP91 footprint to 0402	
2		Power saving	6	Change C190.1, R292.2, R434.2 and U27.8 connect from +12VALW to +12VS	0.2
				Change D16.1, D13.1, Q23.1 and Q24.1 connect from +5VALW to +5VS	
				Change R433.1 and R220.1 connect from +3V to +3VS	
3		No design requirement	7	Delete U10 and C178	0.2
			17	Delete RP7	
			21	Delete C621 and C623	
			22	Delete J8, C611, C612, L55 and L57	
4		No requirement for VGA board	15	Change JP3.48 net from EC_PWR_ON# to N.C.	0.2
5		Divider circuit for U62(AC97 CODEC ALC201)	21	Add R503, R504, R507 and R508 6.8K	0.2
6		Lost connected net for L59	22	Connect L59.2 to LINECL_OUT_L	0.2
7		Modify Base I/O Address for U48(SUPER I/O SMsC LPC47N227)	27	Change R491 value from 10K_0402 to @10K_0402	0.2
				Change R135 value from @10K_0402 to 10K_0402	
8		Solve Touch Pad no function issue	30	Change RP82.3 net from TPAD_ON/OFF# to N.C.	0.2
9		Prevent power leakage	30	Change RP80.3 net from M_SEN# to N.C.	0.2
				Add R509 100K pull-high to +3VS for M_SEN#	
10		Modify bright of D28	31	Change Q33.3 net from +3VALW to+5VALW	0.2
11		Solve D28 can't work issue	31	Relayout for D28	0.2
12		Solve USB2 no function issue	31	Relayout for JP19	0.2
13		Solve power on fail issue	32	Delete R183	0.2
				Change R271 from 0_0402 to 68K_0402	
14		Modify net name for SW1	32	Exchange VOL_IN_UP# and VOL_IN_DN#	0.2
15		BIOS request for MDC	35	Add R510 10K pull-down to GND for JP24.108	0.2
16		Modify USB application	17	Change R157.1 net from OVCUR#0 to OVCUR#5	0.2
				Change R160.1 net from OVCUR#1 to OVCUR#3	
				Change R169.1 net from OVCUR#2 to OVCUR#4	
			31	Change L26.1 net from USBP1+ to USBP3+	
				Change L27.1 net from USBP1- to USBP3-	
				Add F5, C671, C672, C673, C674, R511, R512, L67, L68 and JP32	

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
17		For M.E. request	15	Add JP33, R513, R514, D42, D43 and Q62	0.2
				Change JP3.8, JP3.10, JP3.94, JP3.96, JP2.84 and JP2.86 net to N.C.	
				Change JP3.98 net from INVPWR_B+ to LVDS_BLON#	
			31	Add JP34	
			32	Change JP5 for new connector	
18		Discharge circuit for +12VS and +2.5VS	36	Add R515, R516, Q63 and Q64	0.2
19		For USB2.0 can't fast speed	26	Change L73,L75,L76,L79 to 0.0603	0.3
20		Signal H_THERMTRIP# Design change	5	U66 pin112 connector change to GNT#3,pin113 connector change to REQ#3	
21		Remove serial port connector	28	Add R632 and Q76	0.3
			29	Change VL to +SVS	
			35	Add R633 and RP141	0.3
				Cancel U4,C40,C1,C414,C415,C416,CP1,CP2,JP16	
				Update JP20 pin151,152,101,102,103,104,105,106 Name	
				Add net R1A0	
22		Change M_SEN# R509 from 100K_0402 to 10K_0402	31	Change R509 from 100K_0402 to 10K_0402	0.3
23		For schematic R568 711@ error	23	Change R568 711@0_0402 to 6912@0_0402	0.3
24		BT LED SPEC update	32	Change D28 to new part	0.3
				Add WL_LED	
25		Add sub-woofer solution	22	Add SUB@	0.3
26		Add USB1.1 port	32	Add USB3 port	0.3
27		Add Fan EMI solution	6	Add C751/C752/C753/C754/C746/C747/C234	0.3
28		EC add MAIL_LED#	30	Change U24_pin162 to MAIL_LED#	0.3
				Add U24_pin24 EC_MUTE1#	
29		Change audio amp power source	22	Change +5VALW to VDDA	0.3
30		Change CD_AGND connect to AGND	21	Change from GND to GNDA	0.3
31		711 option cancel	23,27	Del 711@	0.4
32		Add EMI request(FAN)	6	Add C222/C754/C753/C747 and change C746 to 220P	0.4
33		Add EMI request(HDD)	19	Add R517/R518/C675/C676	0.4
34		SD control vender recommend	27	R149 change to 1M/Add 4.7K pull-down	0.4
35		circuit update	30	JP27 pin10 change to MAIL_LED#	0.4
36		Add capacitance for audio noise	32,35,36	Add C758/C759/C760/C761/C762/C763/C764/C765/C766/C767/C768	0.4
37		Add POWER VGATE recommend	33	Add R665/C757	0.4
38		Change ACL201 to ACL202	21	Change CLK input to 14MHZ	0.4
39		Add crystal for ALC202	21	Add Y2,R475,C468,C469 Del R492,R480	0.5
40		Power noise issue	30	Change C366 to @	0.5
41		Customer request	32	Change D45 to Green LED	0.5

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