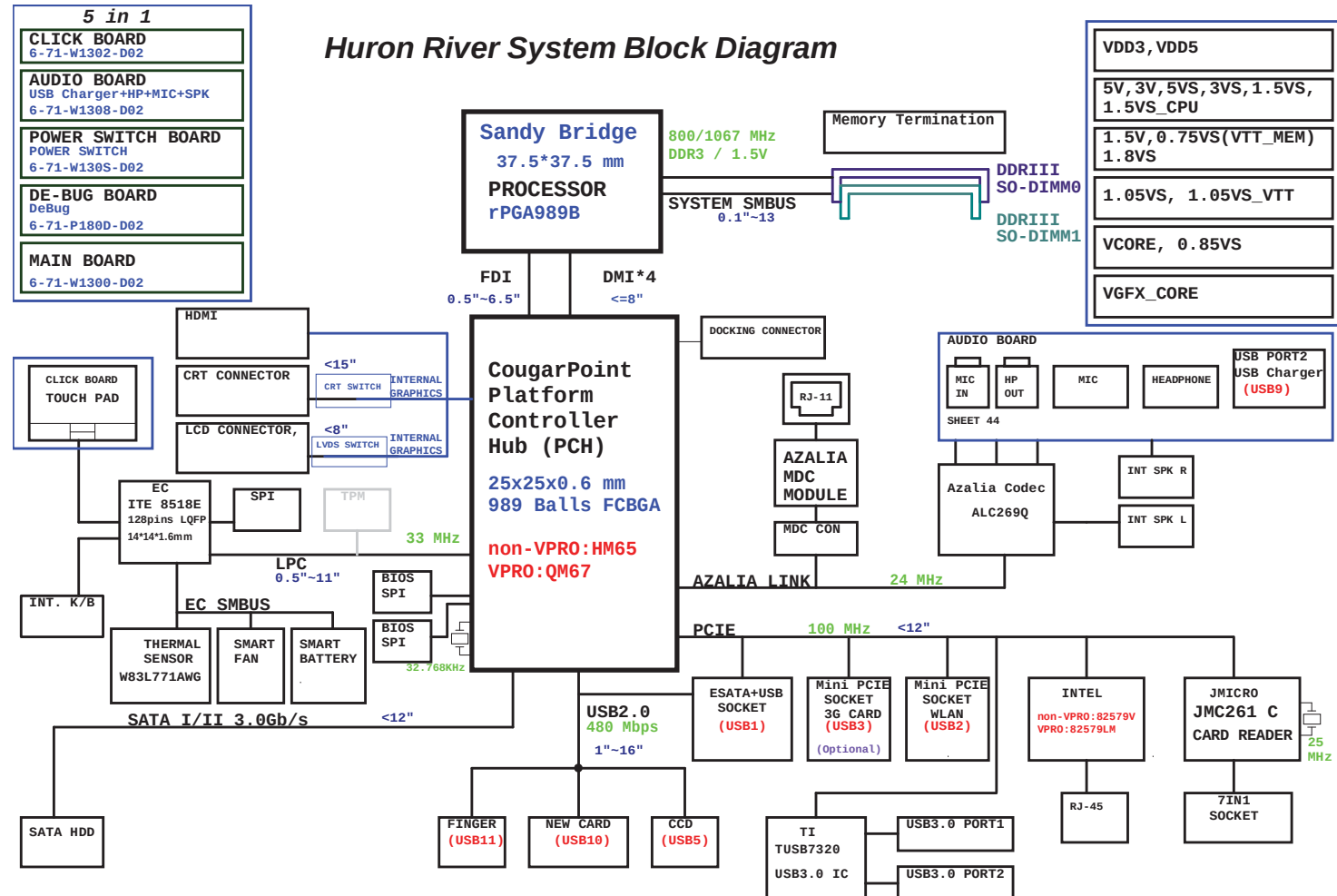
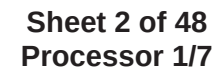


System Block Diagram



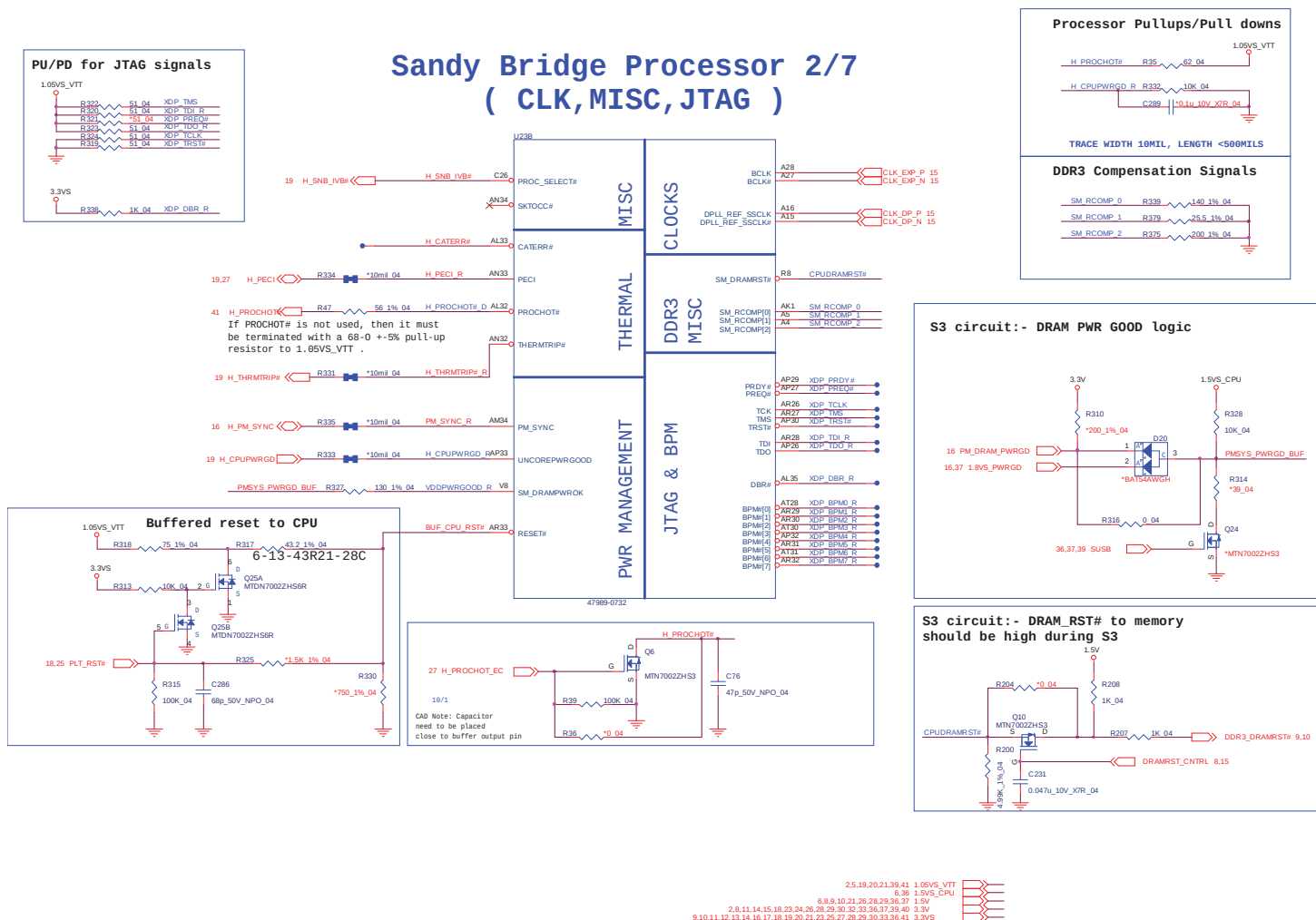
Sheet 1 of 48
System Block
Diagram

Sandy Bridge Processor 1/7 (DMI,PEG,FDI)



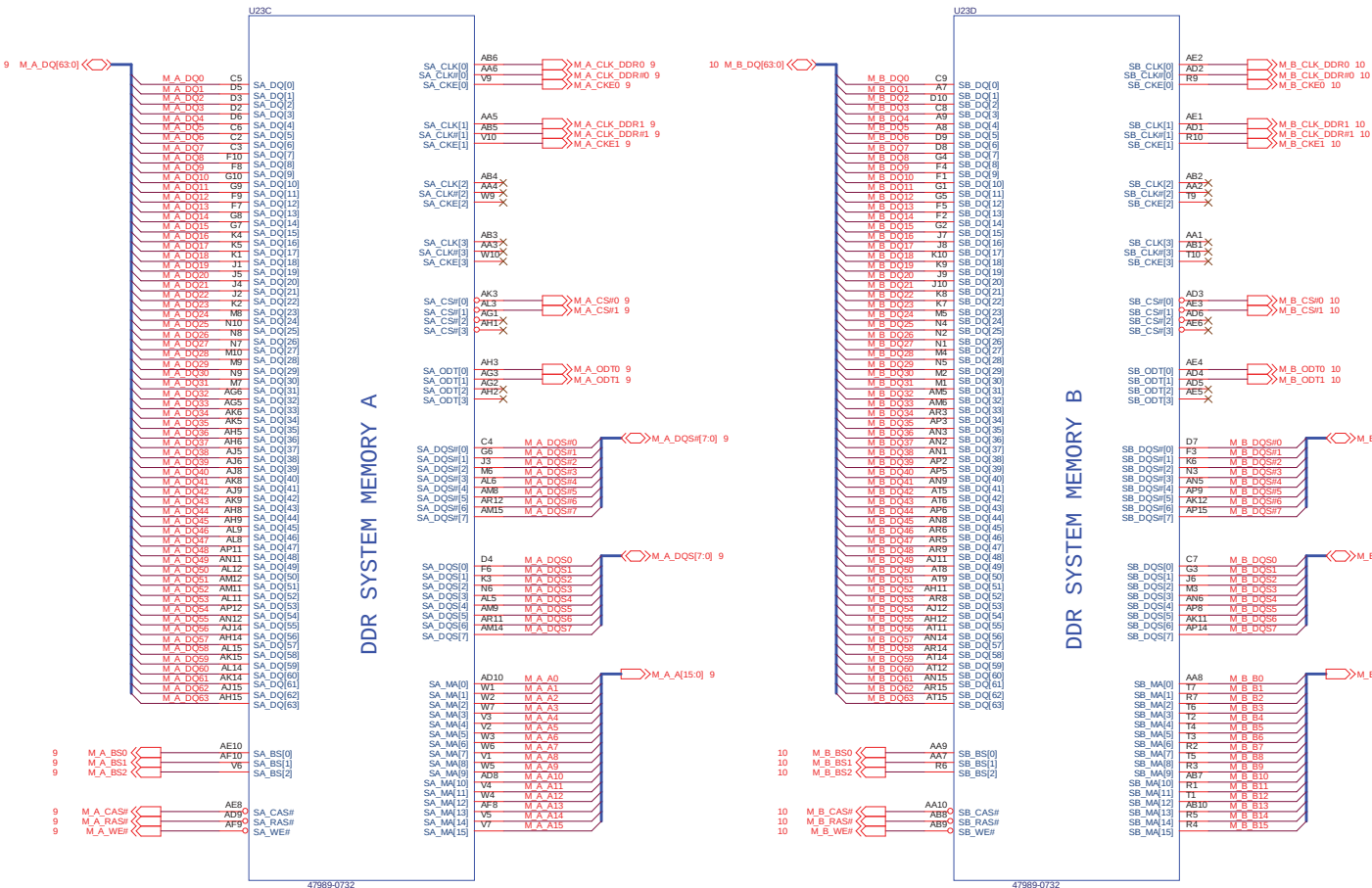
Processor 2/7

Sheet 3 of 48
Processor 2/7



Processor 3/7

Sandy Bridge Processor 3/7 (DDR3)

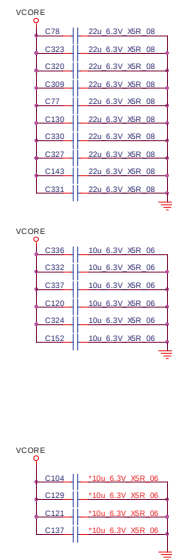
Sheet 4 of 48
Processor 3/7

Processor 4/7

Sandy Bridge Processor 4/7

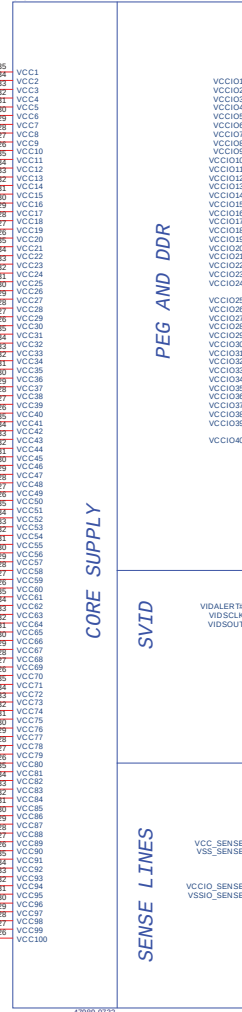
PROCESSOR CORE POWER

ICCMAX Maximum Processor SV 48

Sheet 5 of 48
Processor 4/7

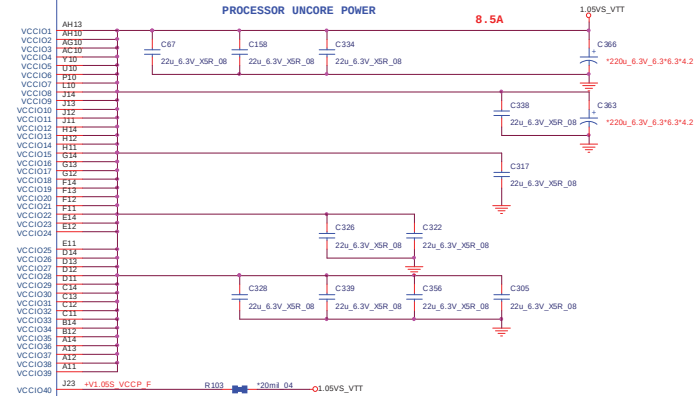
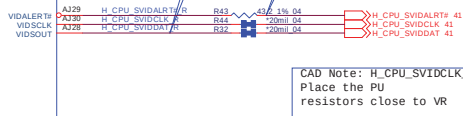
B.Schematic Diagrams

POWER

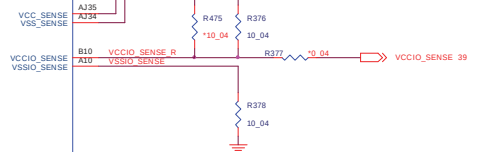


47989-0732

PROCESSOR UNCORE POWER

CAD Note: H_CPU_SVIDALRT#_R, H_CPU_SVIDDAT_R
Place the PU resistors close to CPU

SVID Signals

41.42 VCORE
2.3.19.20.21.39.41 1.05V_VTT

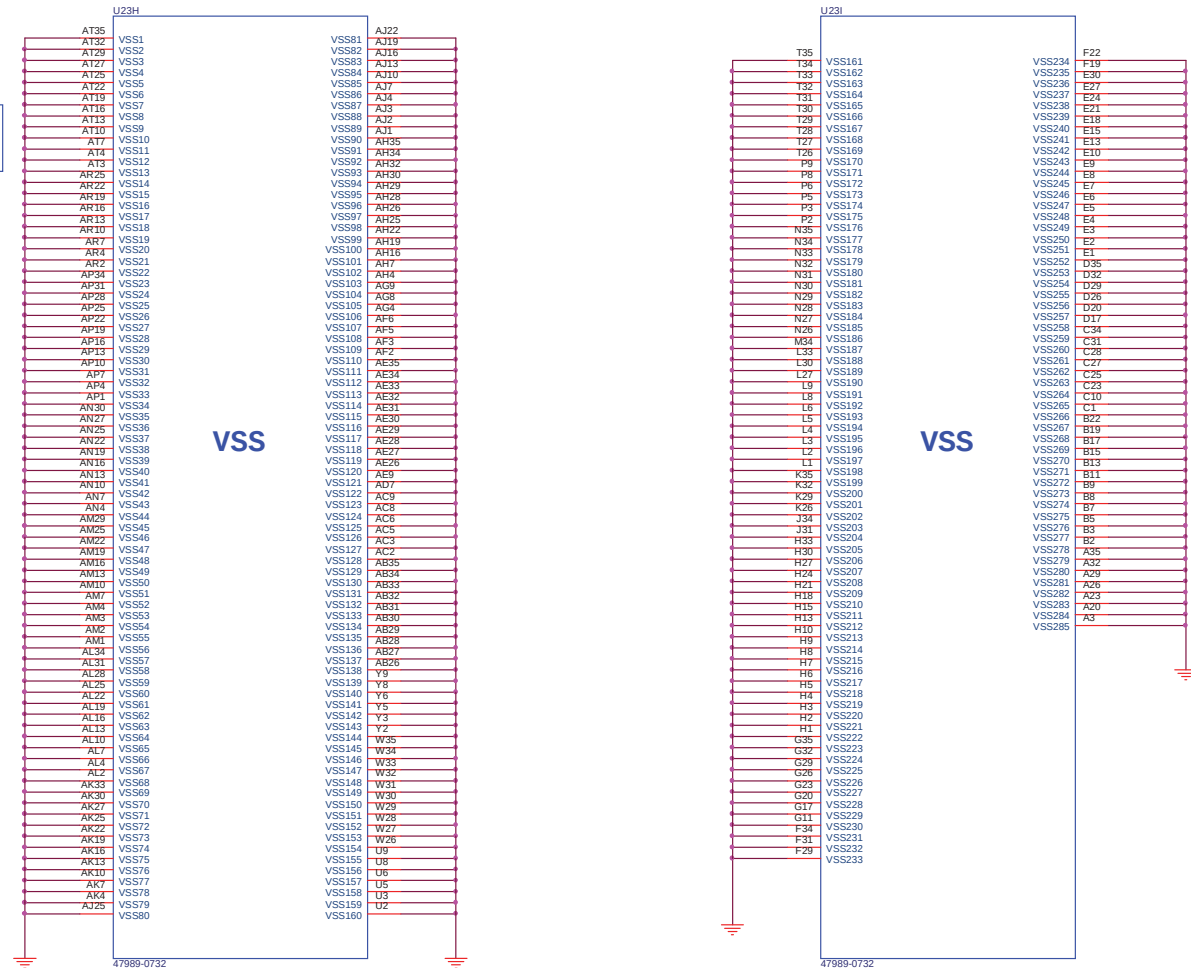
Processor 6/7

Sandy Bridge Processor 6/7 (GND)

CAD Note: 0 ohm resistor
should be placed close
to CPU

Sheet 7 of 48
Processor 6/7

B.Schematic Diagrams



Processor 7/7

Sandy Bridge Processor 7/7
(RESERVED)

CFG Straps for Processor

PEG Static Lane Reversal - CF62 is for the 16x

CFG2 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed

CFG2 R40 *1K_04

Display Port Presence Strap

CFG4 1: (Default) Disabled; No Physical Display Port attached to Embedded Display Port
0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 R31 *1K_04

PCIe Port Bifurcation Straps

CFG[6:5] 11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

CFG5 R41 *1K_04

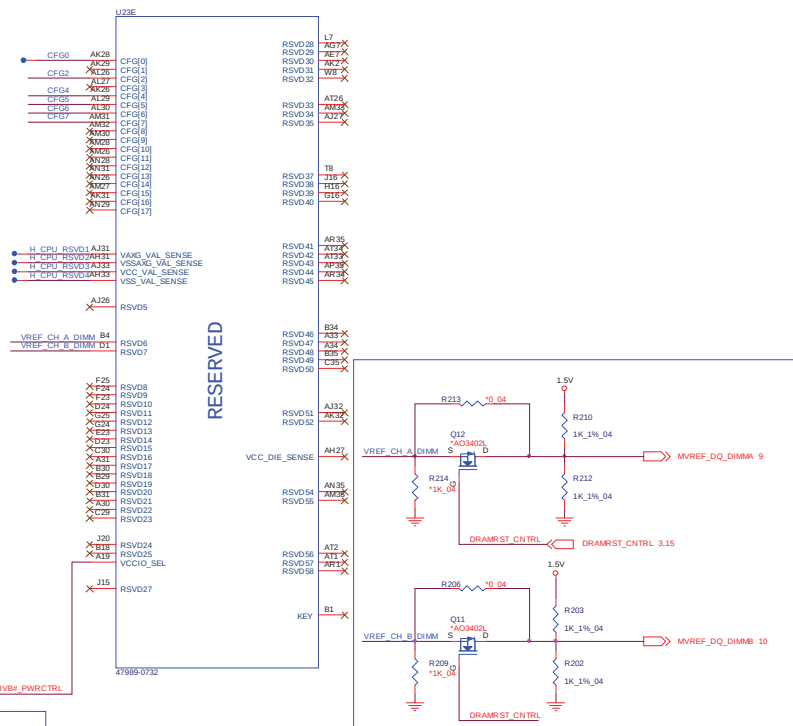
CFG6 R45 *1K_04

PEG DEFER TRAINING

CFG7 1: (Default) PEG Train immediately following xRESETB de assertion
0: PEG Wait for BIOS for training

CFG7 R46 *1K_04

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

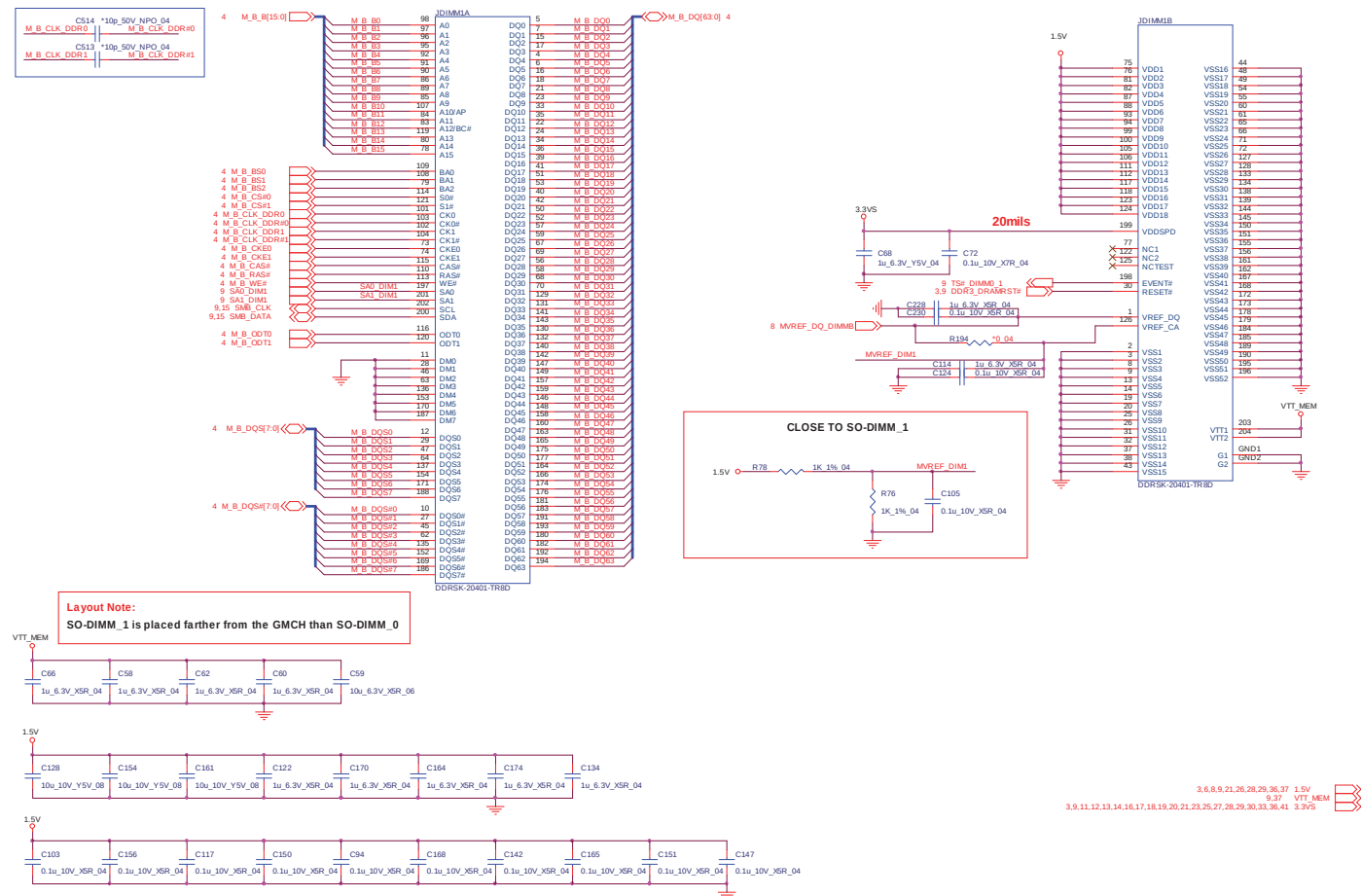


3.6, 9, 10, 21, 26, 29, 29, 36, 37, 1.5V
2.3, 11, 14, 15, 18, 23, 24, 26, 28, 29, 30, 32, 33, 36, 37, 39, 40, 3.3V

Sheet 8 of 48
Processor 7/7

SO-DIMM B

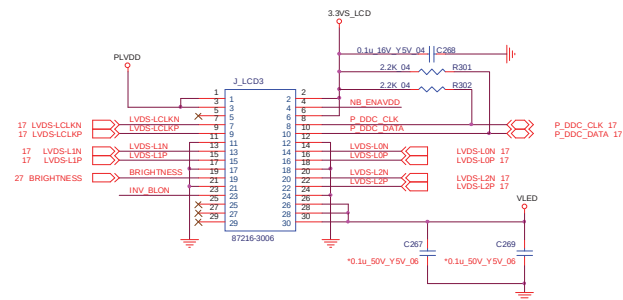
CHANGE TO STANDARD



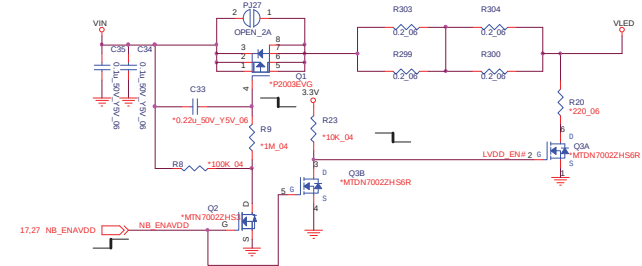
Schematic Diagrams

LVDS, INVERTER

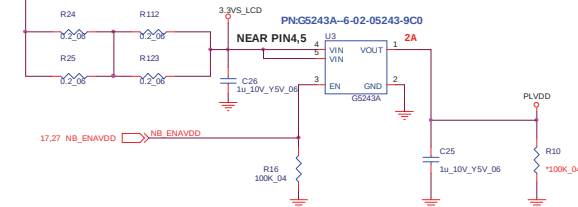
PANEL CONNECTOR



LED PANEL (LVDS Dual Channel).

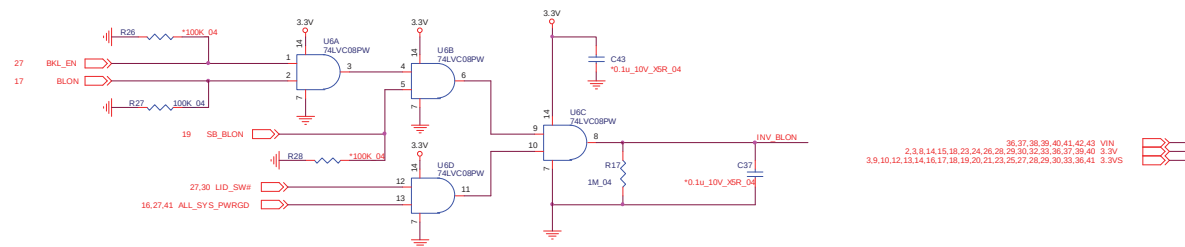


LCD Power Switch G5243A



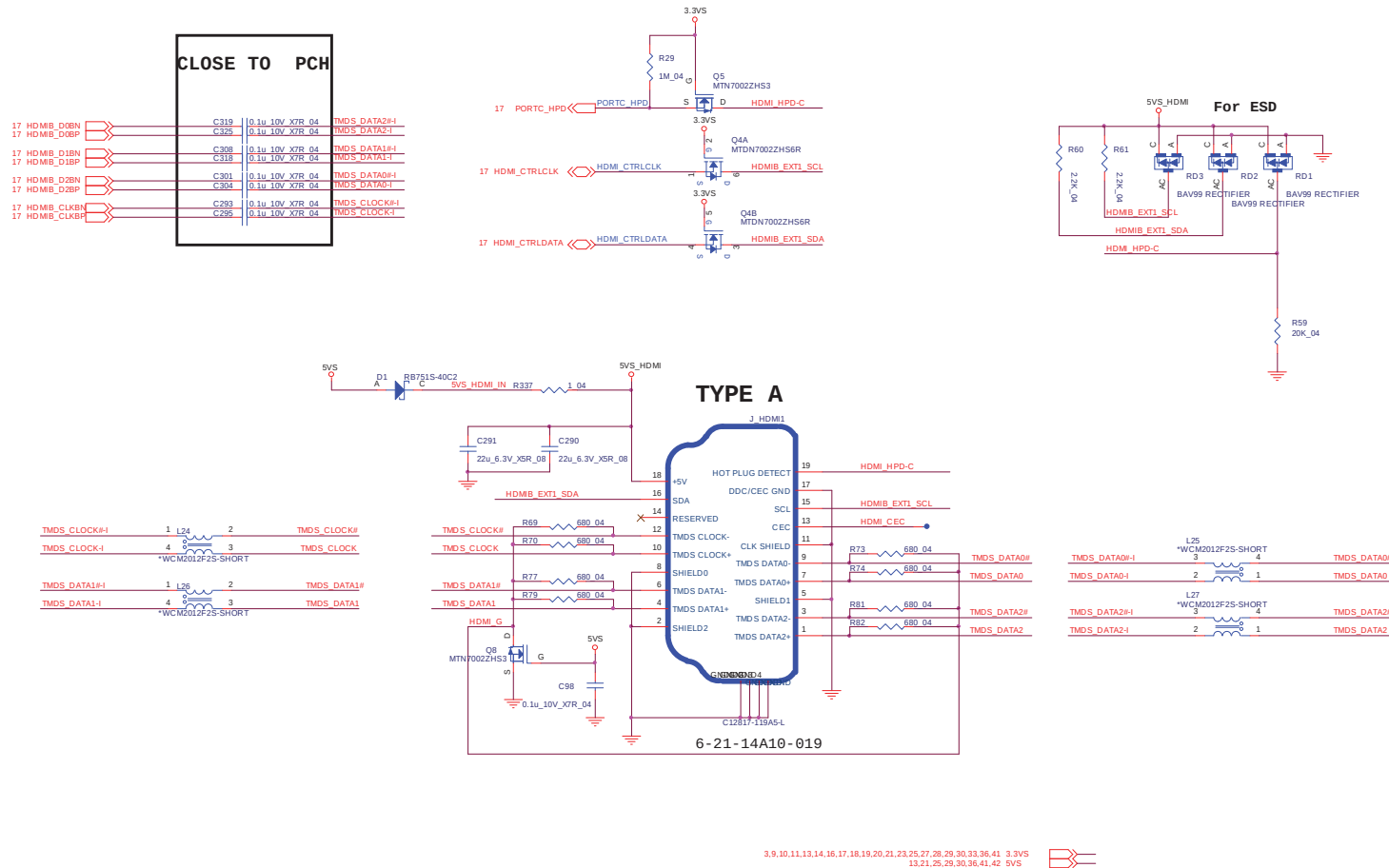
? 40pin connector? , ? ? 30pin connector? ? ? ? pin pad? ? ? ?

INVERTER CONNECTOR



HDMI

HDMI PORT

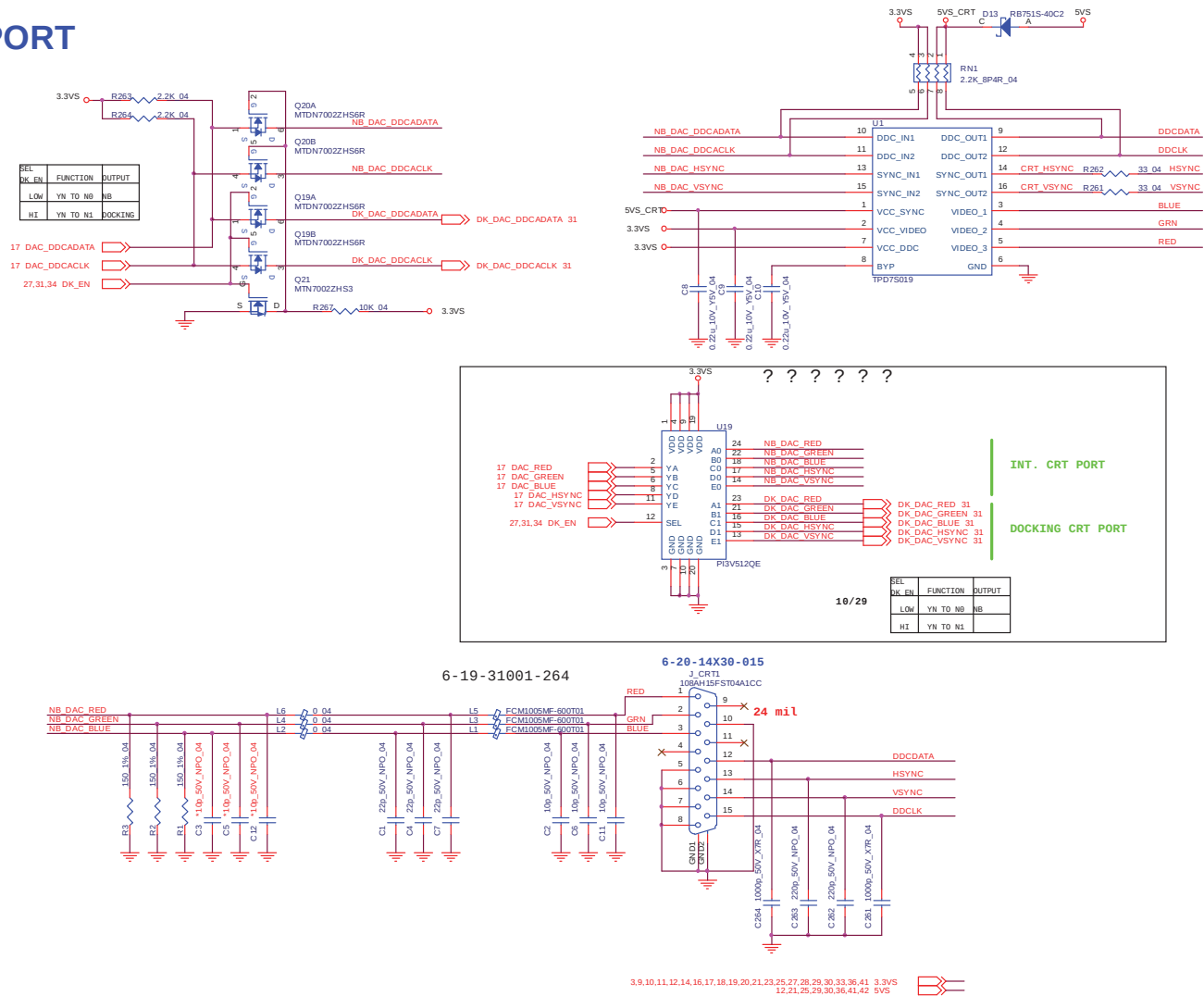


Sheet 12 of 48
HDMI

Schematic Diagrams

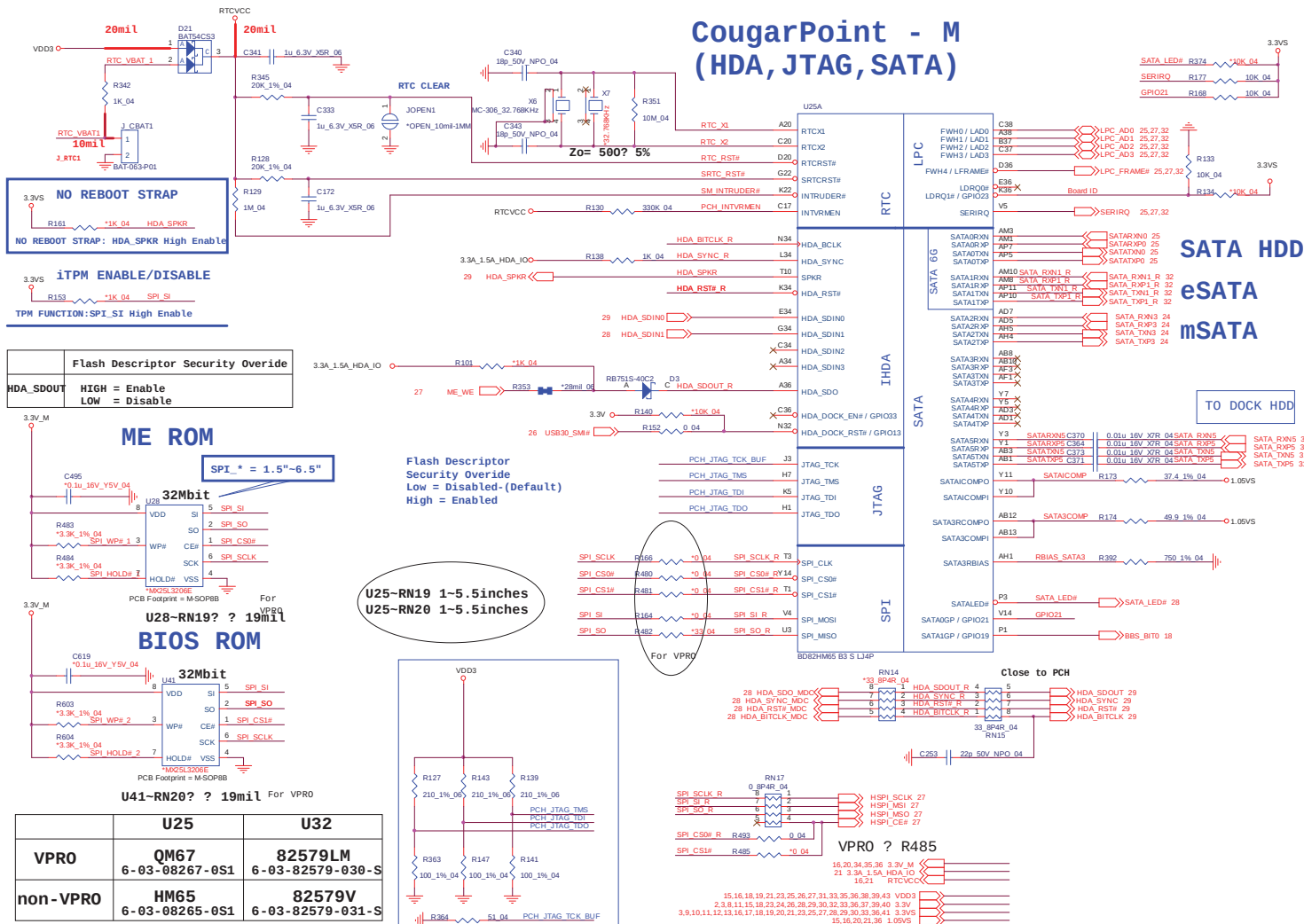
CRT

CRT PORT



Sheet 13 of 48
CRT

Cougar Point M 1/9



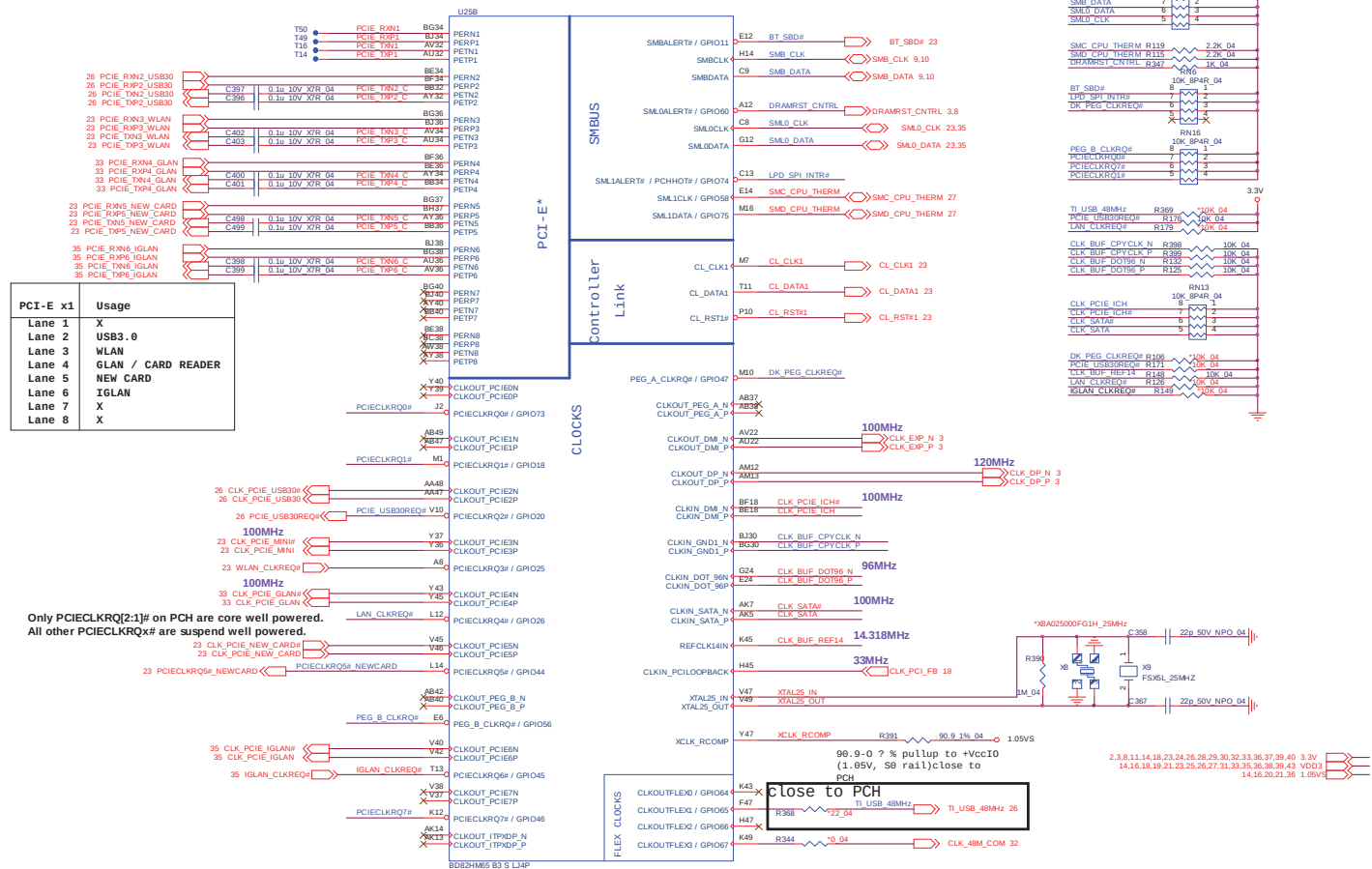
Sheet 14 of 48
Cougar Point M 1/9

B.Schematic Diagrams

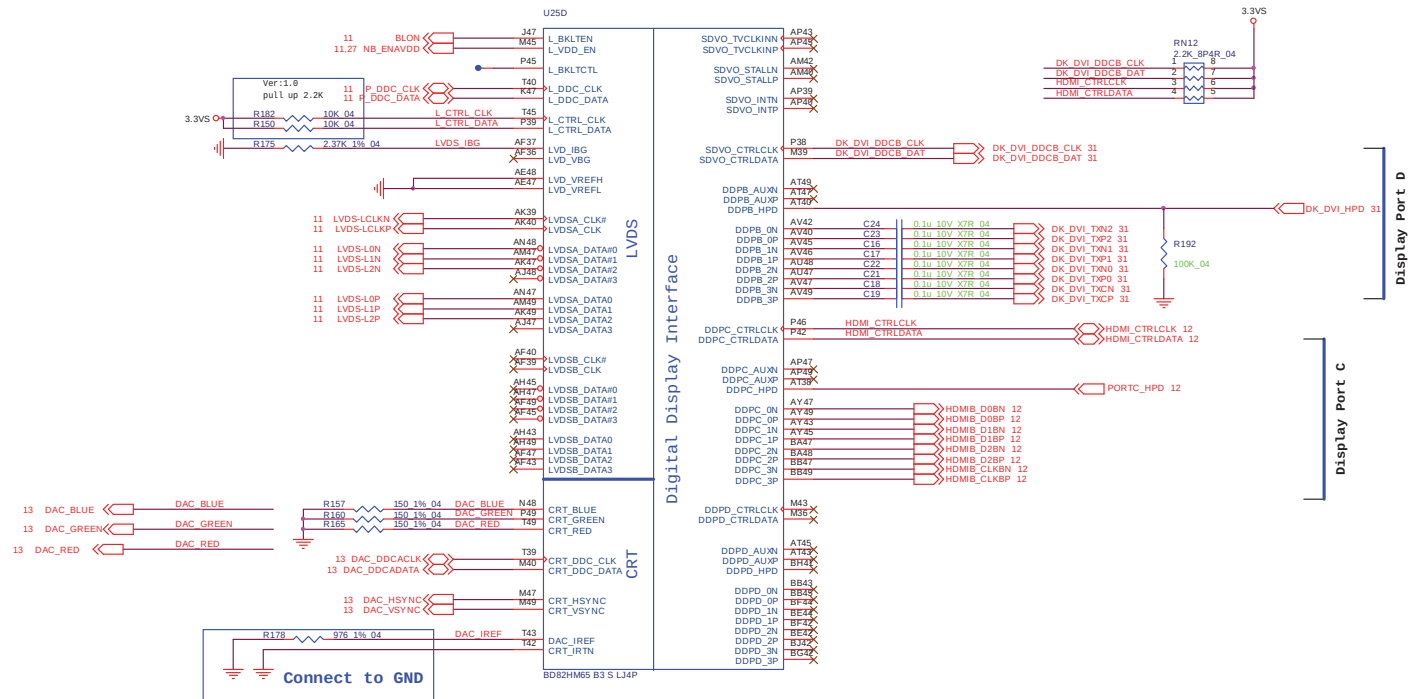
Sheet 15 of 48
Cougar Point M 2/9

PCI-E x1	Usage
Lane 1	X
Lane 2	USB3.0
Lane 3	WLAN
Lane 4	GLAN / CARD READER
Lane 5	NEW CARD
Lane 6	IGLAN
Lane 7	X
Lane 8	X

Only PCIECLKRQ[2:1]# on PCH are core well powered.
All other PCIECLKRQx# are suspend well powered.



Cougar Point M 4/9

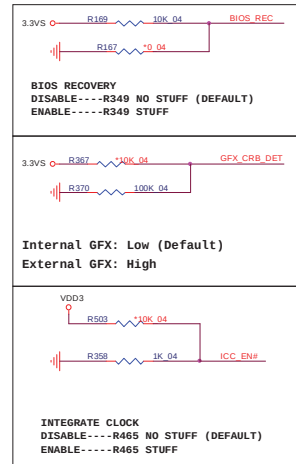
CougarPoint -M
(LVDS, DDI, CRT)Sheet 17 of 48
Cougar Point M 4/9

12,13,21,25,29,30,36,41,42 5V5
3,9,10,11,12,13,14,16,18,19,20,21,23,25,27,28,29,30,33,36,41 3.3V5

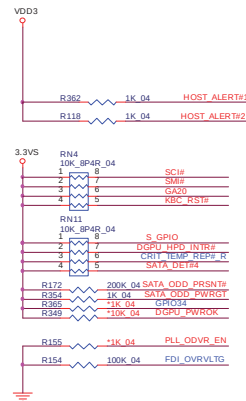
Sheet 18 of 48
Cougar Point M 5/9



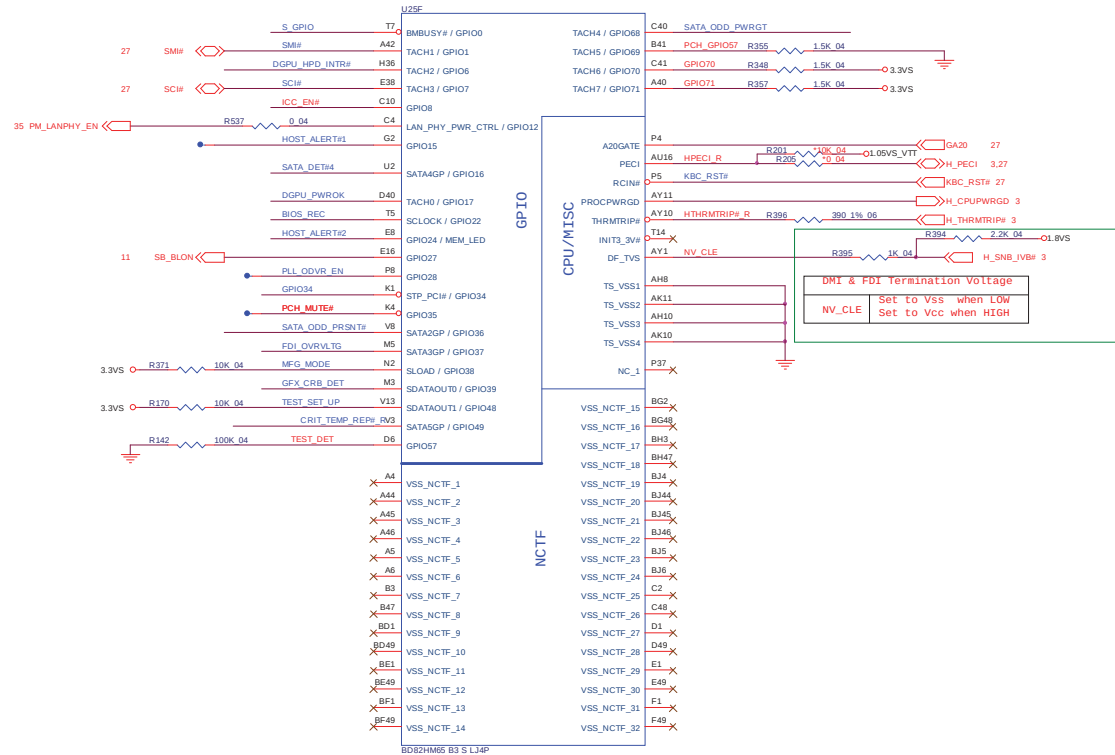
Cougar Point M 6/9



Sheet 19 of 48
Cougar Point M 6/9

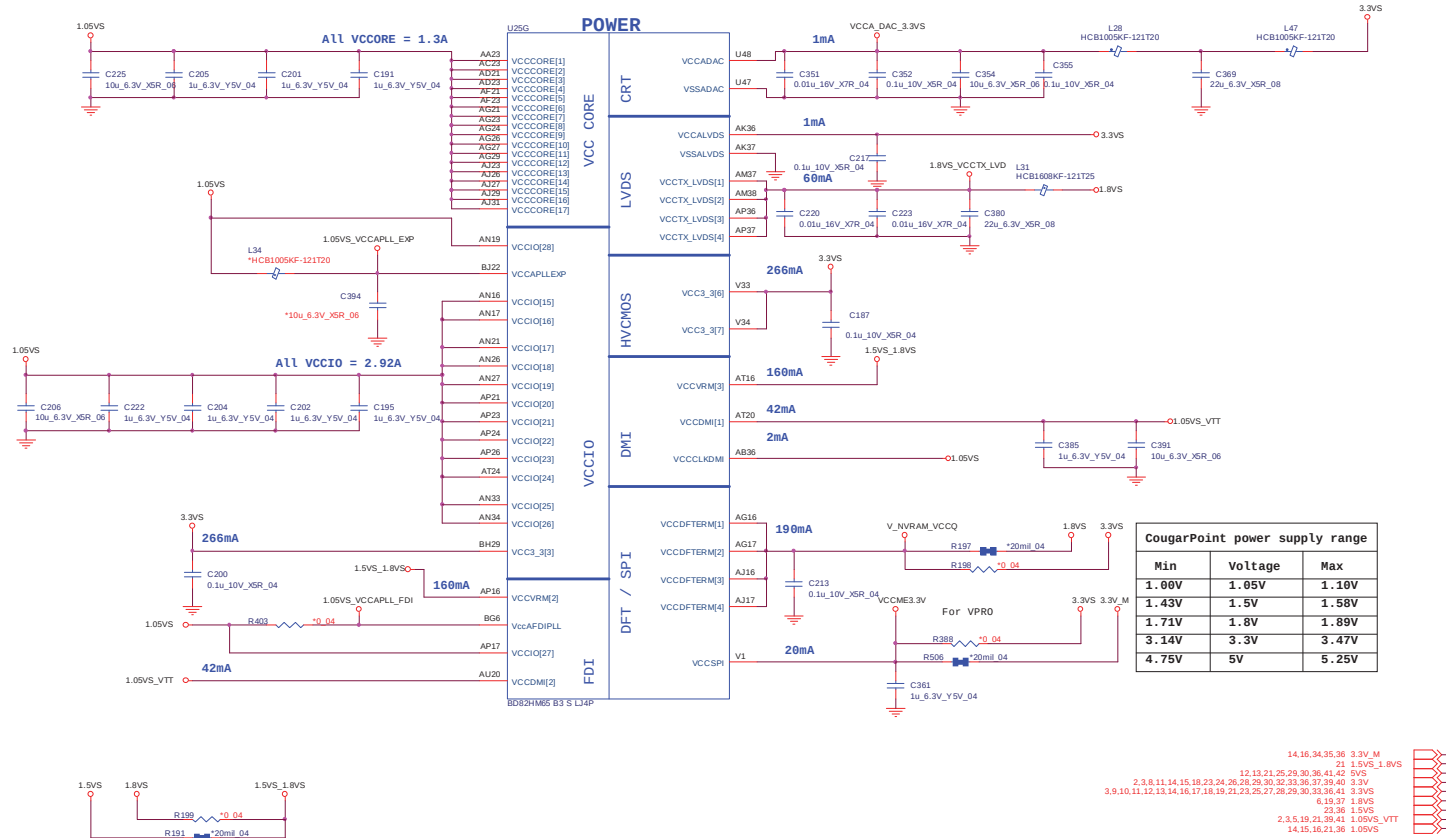


CougarPoint - M (GPIO, VSS_NCTF, RSVD)



Cougar Point M 7/9

CougarPoint -M (POWER)



Sheet 20 of 48
Cougar Point M 7/9

Cougar Point M 8/9

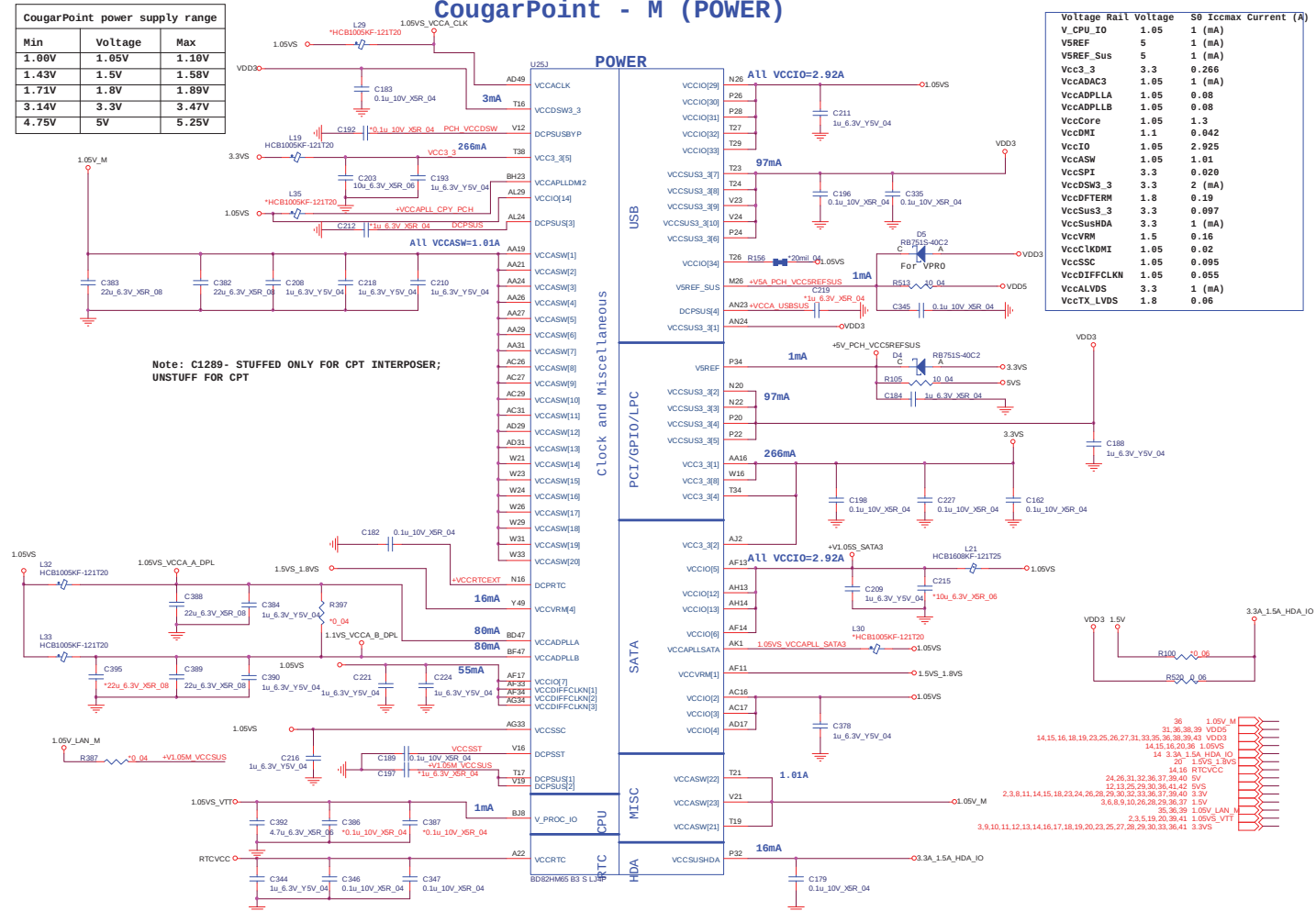
CougarPoint power supply range			
Min	Voltage	Max	
1.00V	1.05V	1.10V	
1.43V	1.5V	1.58V	
1.71V	1.8V	1.89V	
3.14V	3.3V	3.47V	
4.75V	5V	5.25V	

CougarPoint - M (POWER)

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_CPU_IO	1.05	1 (mA)
VSREF	5	1 (mA)
VSREF_Sus	5	1 (mA)
Vcc3_3	3.3	0.266
VccADAC3	1.05	1 (mA)
VccADPLLA	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPT	3.3	0.020
VccDSW3_3	3.3	2 (mA)
VccDFTERM	1.8	0.19
VccSus3_3	3.3	0.097
VccSusHDA	3.3	1 (mA)
VccVRM	1.5	0.16
VccLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	2.3	1 (mA)
VccTX_LVDS	1.8	0.06

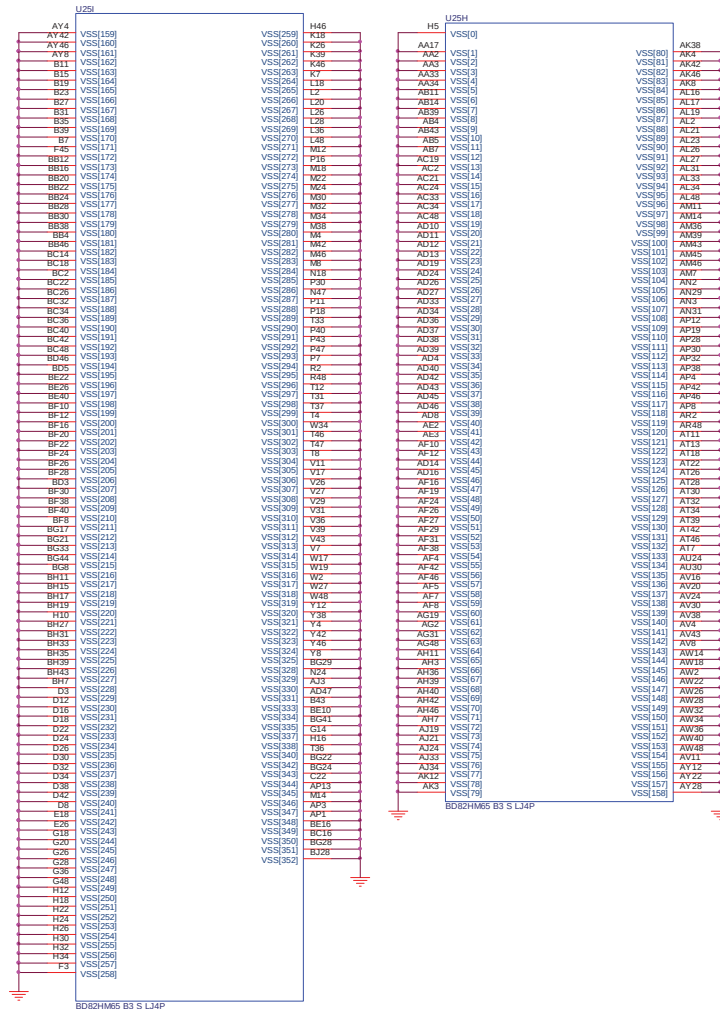
Sheet 21 of 48
Cougar Point M 8/9

B.Schematic Diagrams



Cougar Point M 9/9

CougarPoint -M (GND)



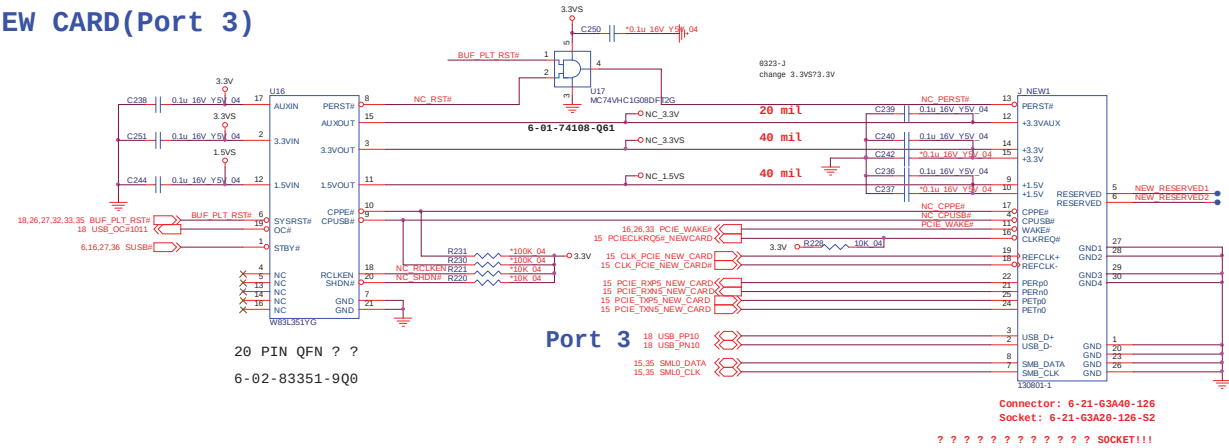
Sheet 22 of 48
Cougar Point M 9/9

B.Schematic Diagrams

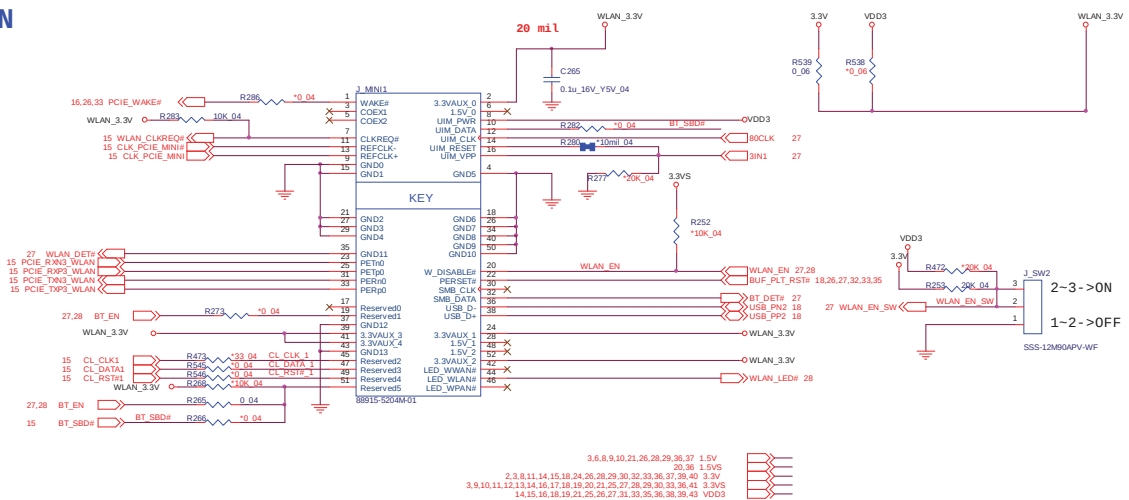
Schematic Diagrams

NEW CARD, MINI PCIE

NEW CARD(Port 3)

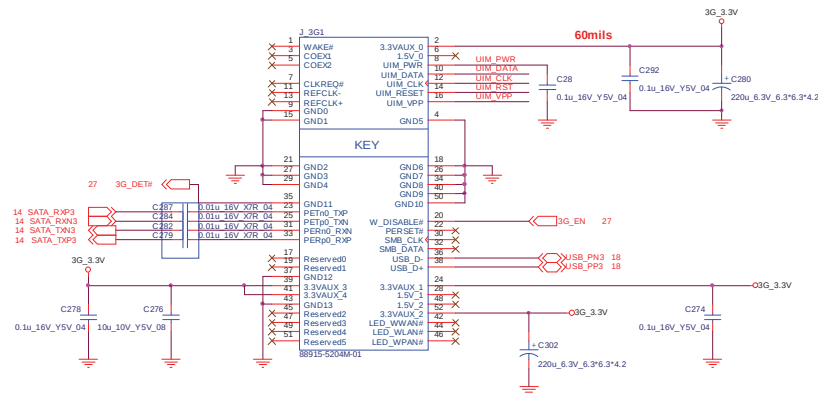


MINI CARD WLAN

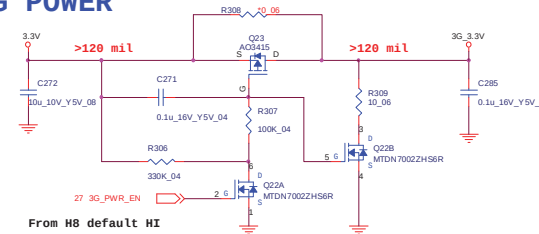


CCD, 3G

MINI CARD 3G(Port 6)

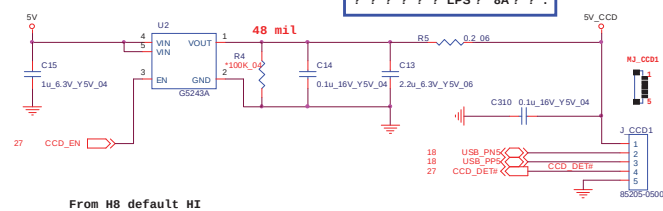


3G POWER



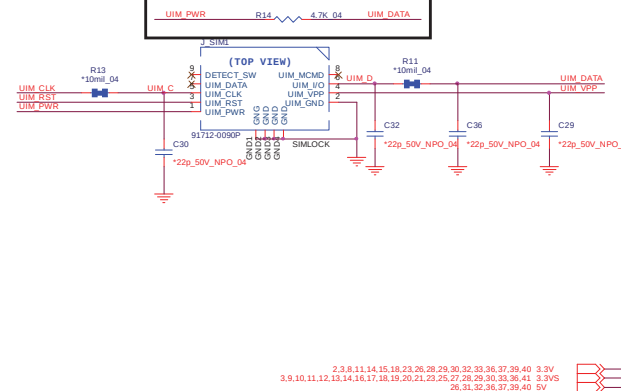
Sheet 24 of 48
CCD, 3G

CCD



SIM CONN

8mil



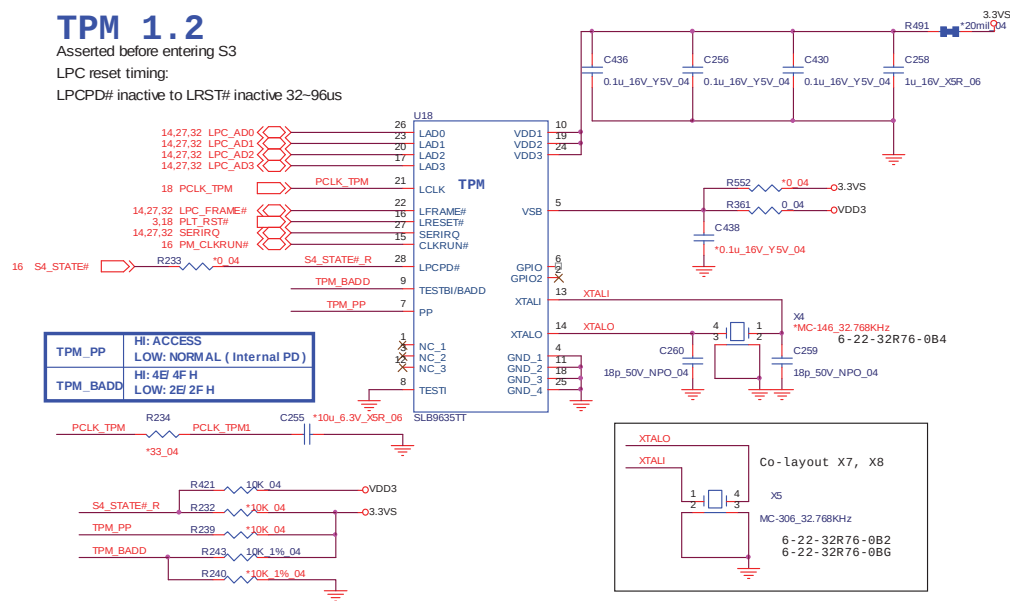
TPM, SATA HDD

TPM 1.2

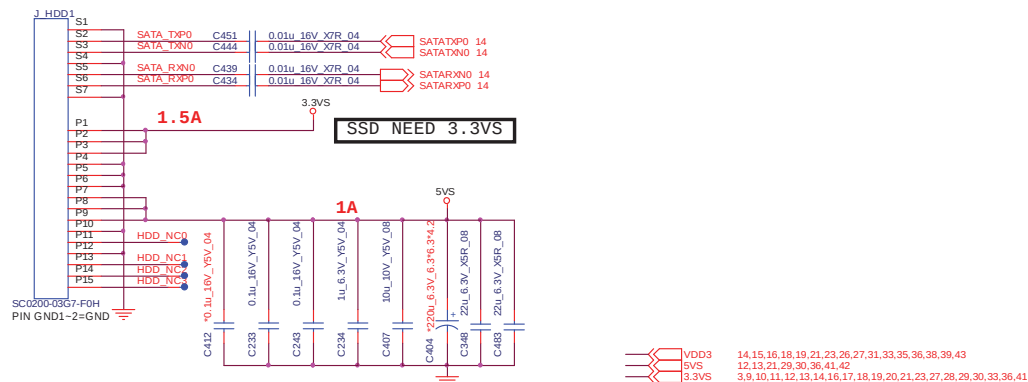
Asserted before entering S3

LPC reset timing:

LPCPD# inactive to LRST# inactive 32~96us



SATA HDD



The image shows a complex PCB layout for a USB3.0 interface. The layout includes a USB3.0 PHY, a USB3.0 Hub, and a USB3.0 Connector. The layout is populated with various components, including resistors, capacitors, and a USB3.0 Hub (TUSB7320). The layout also includes a table for USB3.0 Layout Guidelines and a table for USB3.0 Connector Pinout.

USB3.0 Layout Guidelines:

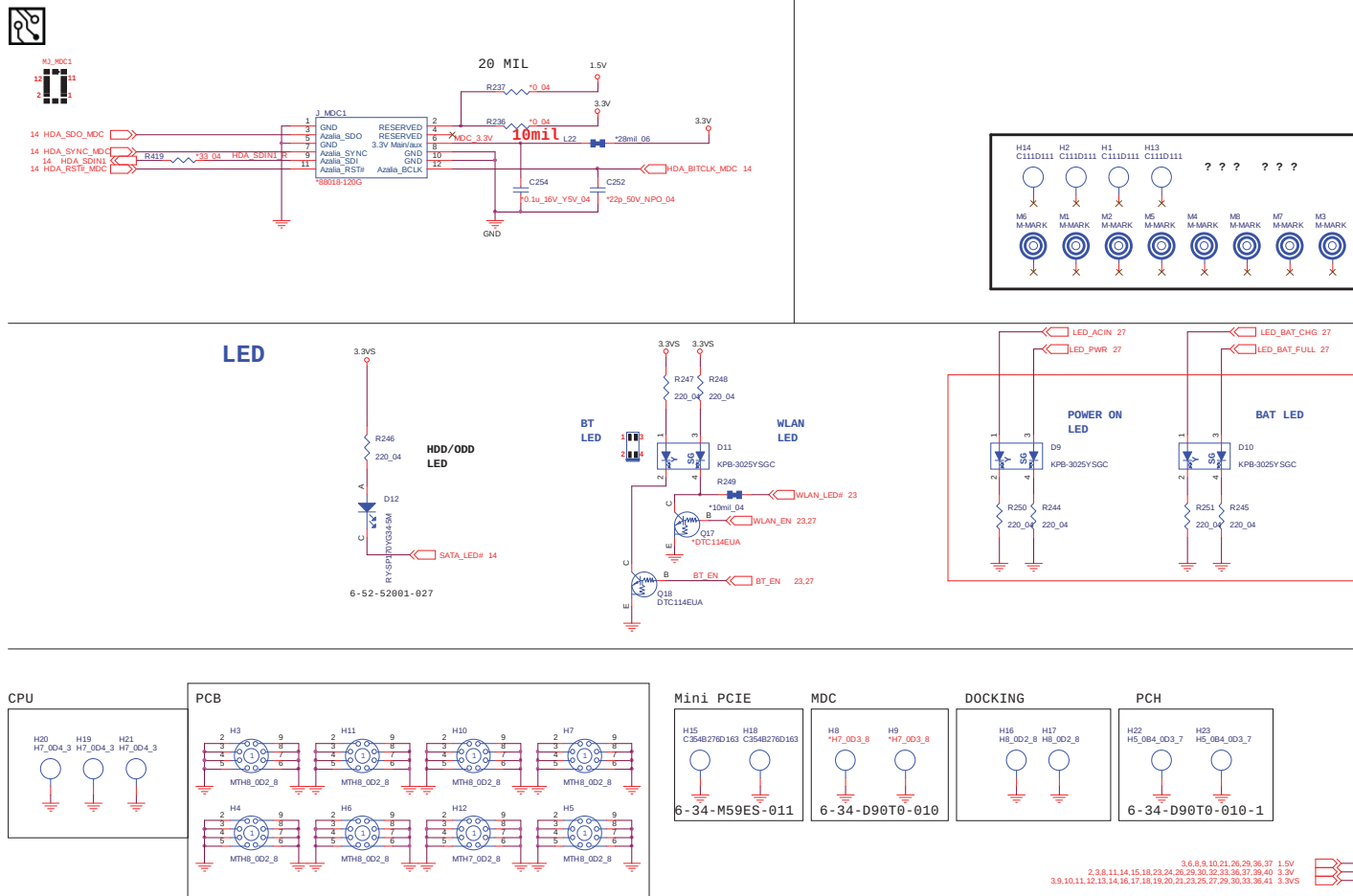
- USB3.0 Differential trace impedance: 90ohm
- Differential pairs The USB3.0 the total trace skew less than 5 mils.
- IC pad to USB Connector total length < 4"(Max)
- USB3.0 Capacitor 0.1u-10V_X7R_04 Close to Connector.
- PCie Differential Impedance 85 ohm.
- PCie For transmitter and receiver the total trace length: 1"(Min)--6"(Max).
- PCie Number of vias 4via hole(Max).
- PCie clock Differential impedance 90 ohm.
- PCie Differential pairs and pairs spacing 20mils, with Other trace spacing 25mils.
- Power Trace width=20mils, Spacing=80 mils.

USB3.0 Connector Pinout:

Pin	Signal	Standard
1	USBS1_1	Standard
2	USBS1_2	Standard
3	USBS1_3	Standard
4	USBS1_4	Standard
5	USBS1_5	Standard
6	USBS1_6	Standard
7	USBS1_7	Standard
8	USBS1_8	Standard
9	USBS1_9	Standard
10	USBS1_10	Standard
11	USBS1_11	Standard
12	USBS1_12	Standard
13	USBS1_13	Standard
14	USBS1_14	Standard
15	USBS1_15	Standard
16	USBS1_16	Standard
17	USBS1_17	Standard
18	USBS1_18	Standard
19	USBS1_19	Standard
20	USBS1_20	Standard
21	USBS1_21	Standard
22	USBS1_22	Standard
23	USBS1_23	Standard
24	USBS1_24	Standard
25	USBS1_25	Standard
26	USBS1_26	Standard
27	USBS1_27	Standard
28	USBS1_28	Standard
29	USBS1_29	Standard
30	USBS1_30	Standard
31	USBS1_31	Standard
32	USBS1_32	Standard
33	USBS1_33	Standard
34	USBS1_34	Standard
35	USBS1_35	Standard
36	USBS1_36	Standard
37	USBS1_37	Standard
38	USBS1_38	Standard
39	USBS1_39	Standard
40	USBS1_40	Standard
41	USBS1_41	Standard
42	USBS1_42	Standard
43	USBS1_43	Standard
44	USBS1_44	Standard
45	USBS1_45	Standard
46	USBS1_46	Standard
47	USBS1_47	Standard
48	USBS1_48	Standard
49	USBS1_49	Standard
50	USBS1_50	Standard
51	USBS1_51	Standard
52	USBS1_52	Standard
53	USBS1_53	Standard
54	USBS1_54	Standard
55	USBS1_55	Standard
56	USBS1_56	Standard
57	USBS1_57	Standard
58	USBS1_58	Standard
59	USBS1_59	Standard
60	USBS1_60	Standard
61	USBS1_61	Standard
62	USBS1_62	Standard
63	USBS1_63	Standard
64	USBS1_64	Standard
65	USBS1_65	Standard
66	USBS1_66	Standard
67	USBS1_67	Standard
68	USBS1_68	Standard
69	USBS1_69	Standard
70	USBS1_70	Standard
71	USBS1_71	Standard
72	USBS1_72	Standard
73	USBS1_73	Standard
74	USBS1_74	Standard
75	USBS1_75	Standard
76	USBS1_76	Standard
77	USBS1_77	Standard
78	USBS1_78	Standard
79	USBS1_79	Standard
80	USBS1_80	Standard
81	USBS1_81	Standard
82	USBS1_82	Standard
83	USBS1_83	Standard
84	USBS1_84	Standard
85	USBS1_85	Standard
86	USBS1_86	Standard
87	USBS1_87	Standard
88	USBS1_88	Standard
89	USBS1_89	Standard
90	USBS1_90	Standard
91	USBS1_91	Standard
92	USBS1_92	Standard
93	USBS1_93	Standard
94	USBS1_94	Standard
95	USBS1_95	Standard
96	USBS1_96	Standard
97	USBS1_97	Standard
98	USBS1_98	Standard
99	USBS1_99	Standard
100	USBS1_100	Standard

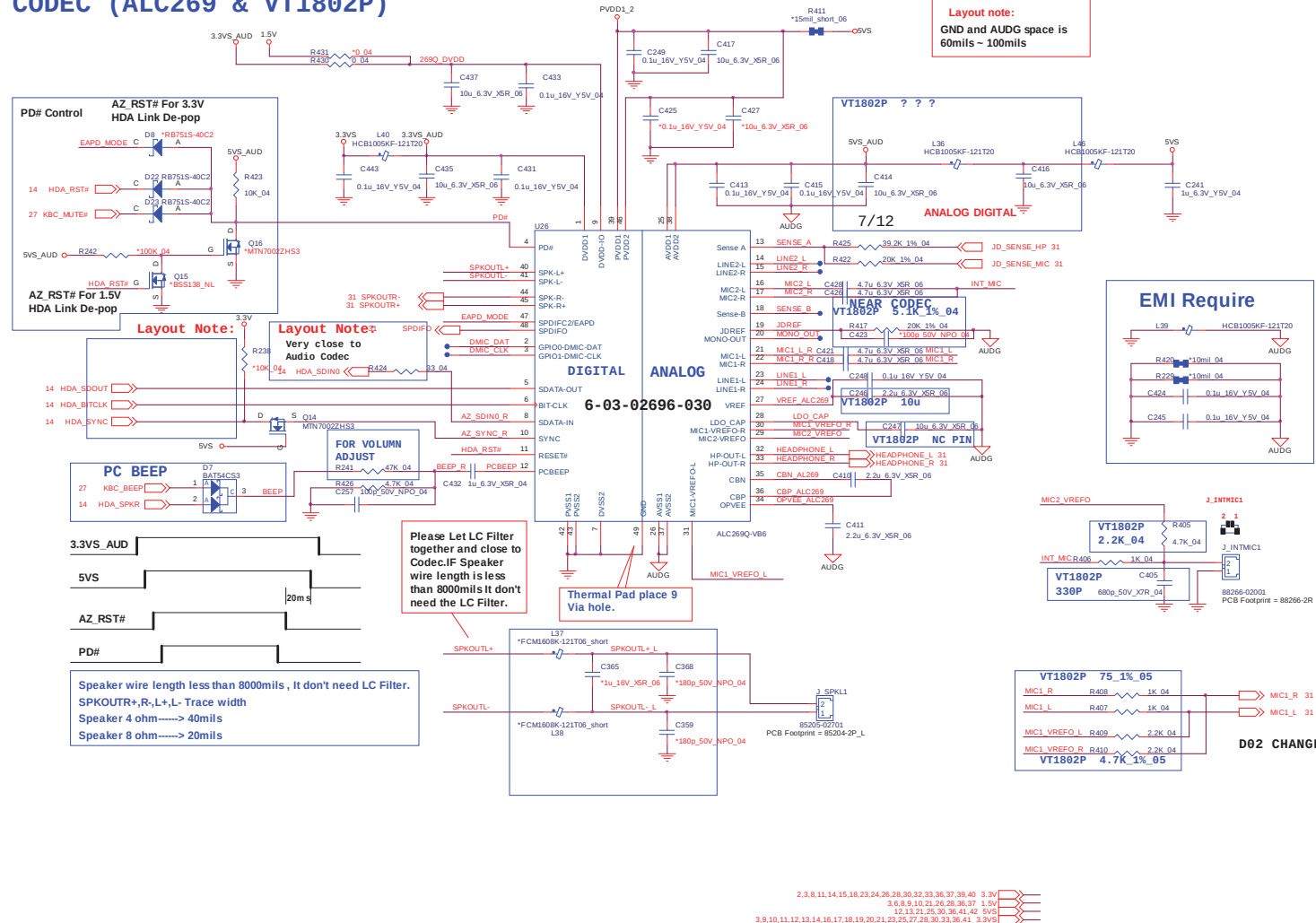
TI TUSB7320 USB3.0 B - 27

LED, MDC

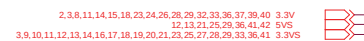
Sheet 28 of 48
LED, MDC

AUDIO CODEC ALC269Q

CODEC (ALC269 & VT1802P)

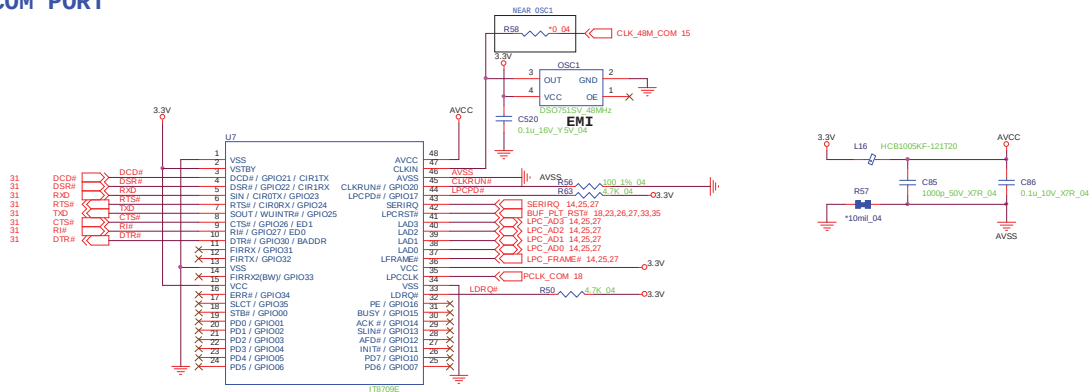


FAN CONTROL



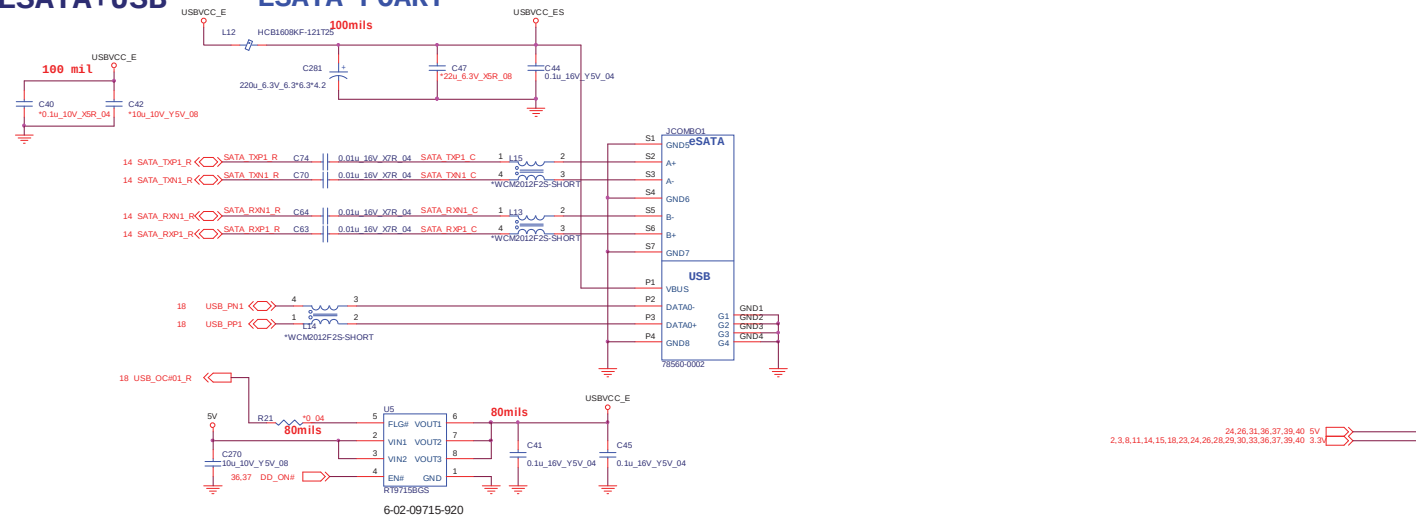
COM PORT, ESATA+USB

Docking COM PORT



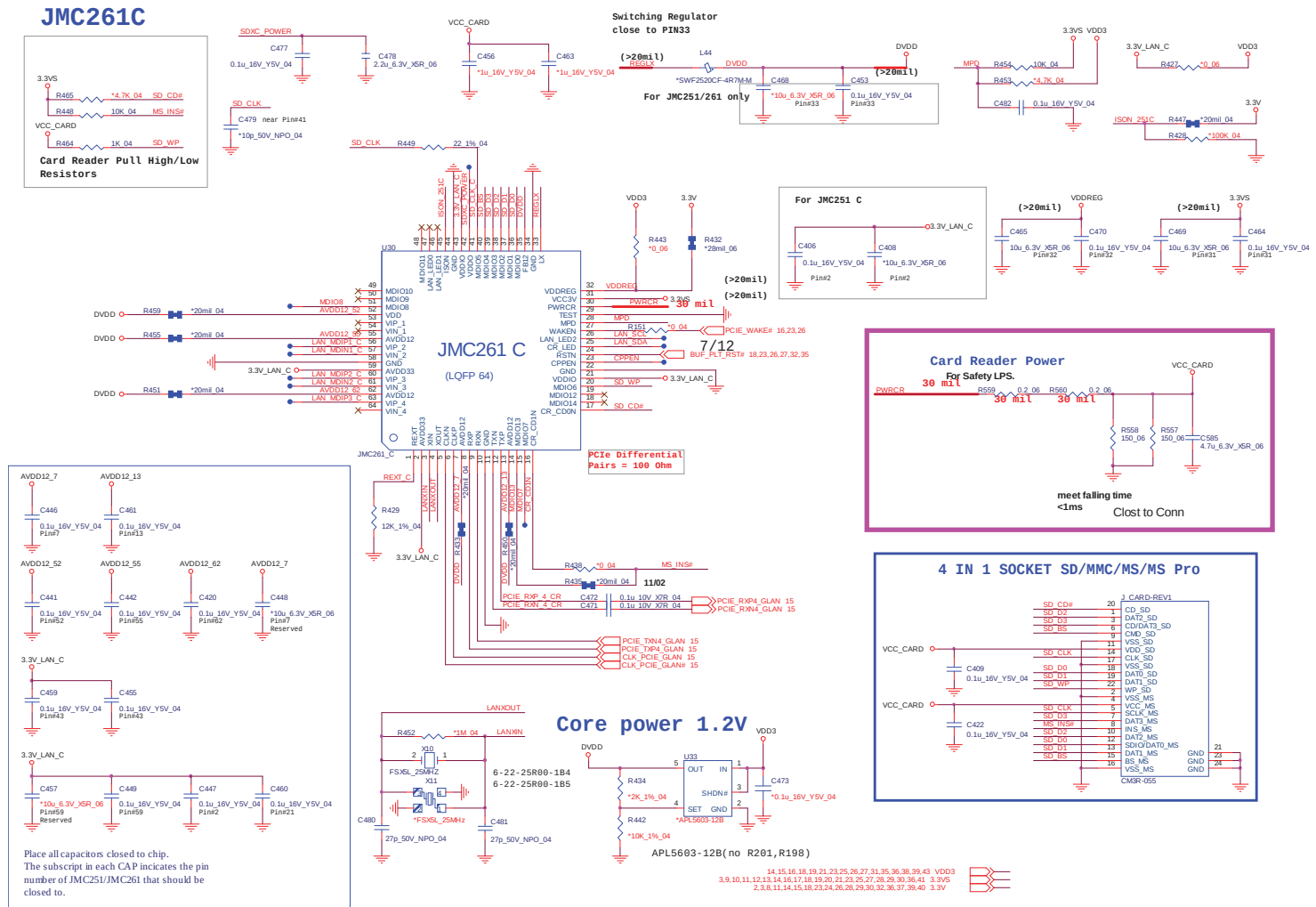
Sheet 32 of 48
COM PORT,
ESATA+USB

ESATA+USB



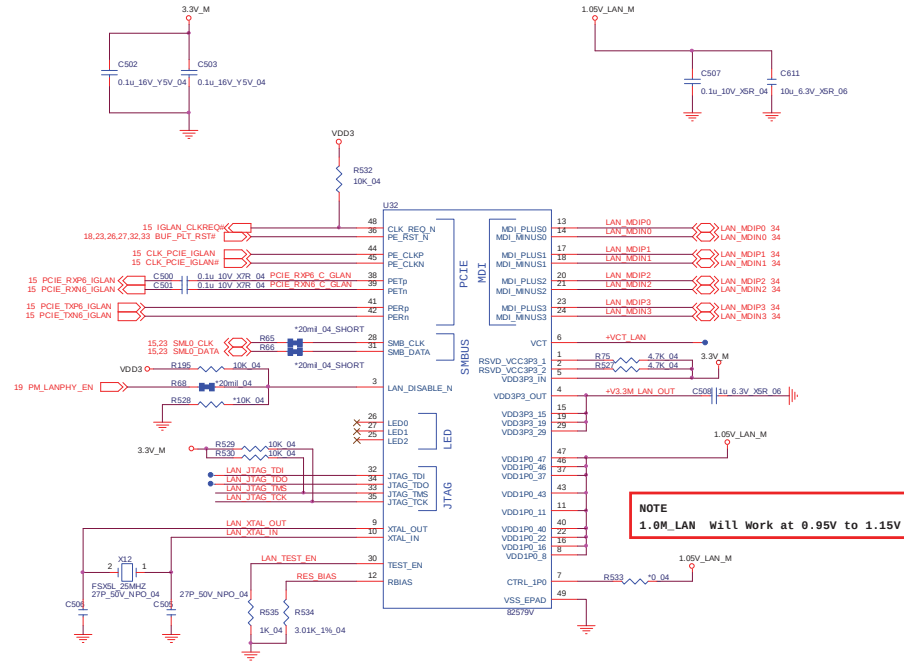
CARD READER JMC261C

Sheet 33 of 48
CARD READER
JMC261C



INTEL LAN82579LM

Sheet 35 of 48
INTEL
LAN82579LM

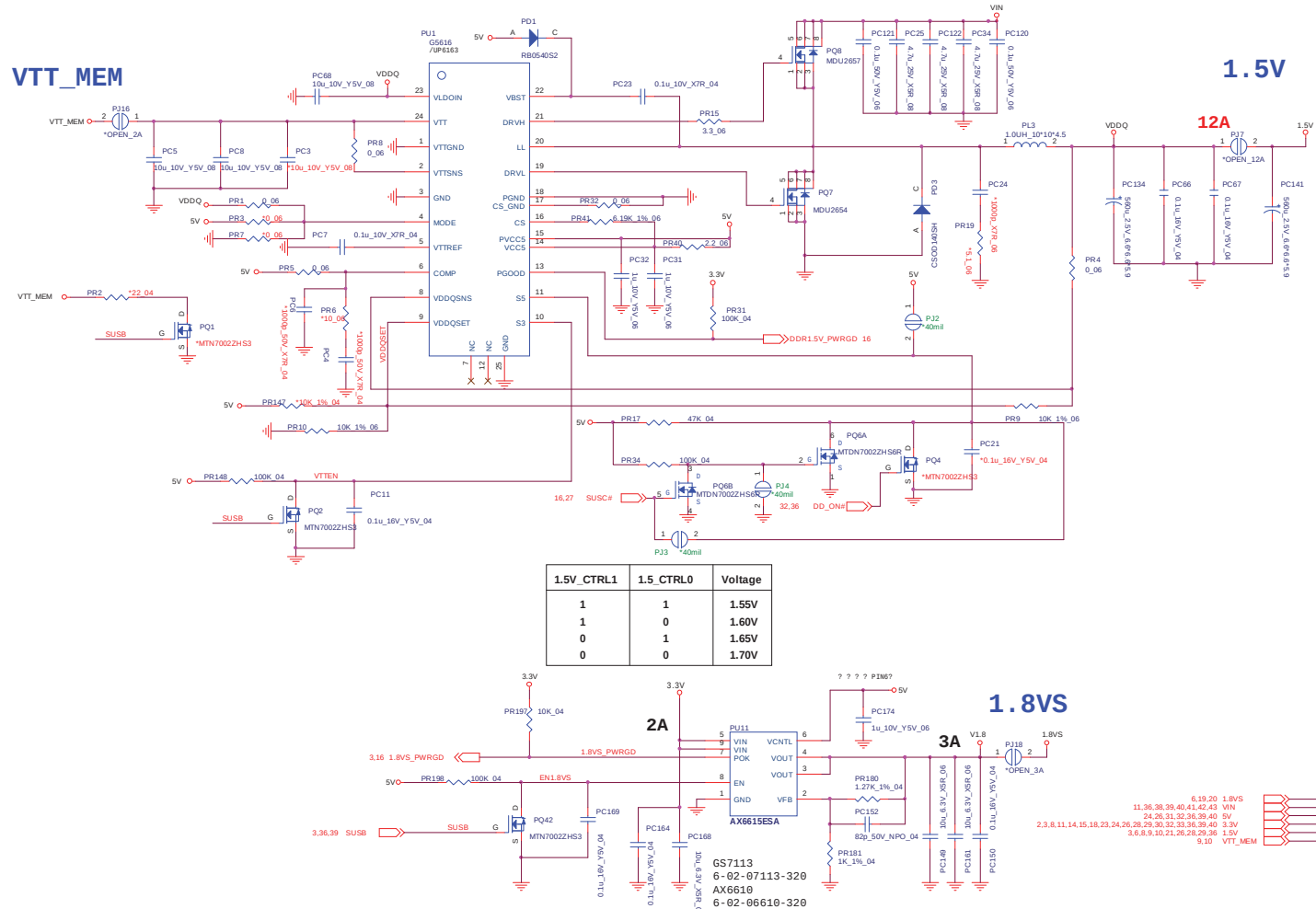


	U25	U32	U28	U41	U27
VPRO	QM67 6-03-08267-0S1	82579LM 6-03-82579-030-S6	MX25L3206E 6-04-25320-490	MX25L3206E 6-04-25320-490	PM25LD010C-SCE 6-04-25010-A91
non-VPRO	HM65 6-03-08265-0S1	82579V 6-03-82579-031-S	NI	NI	MX25L3206E 6-04-25320-490

21,36,39 1.05V_LAN_M
14,16,20,34,36 3.3V_M
14,15,16,18,19,21,23,25,26,27,31,33,36,38,39,43 VDD3

Schematic Diagrams

Power 1.5V/0.75V,1.8VS

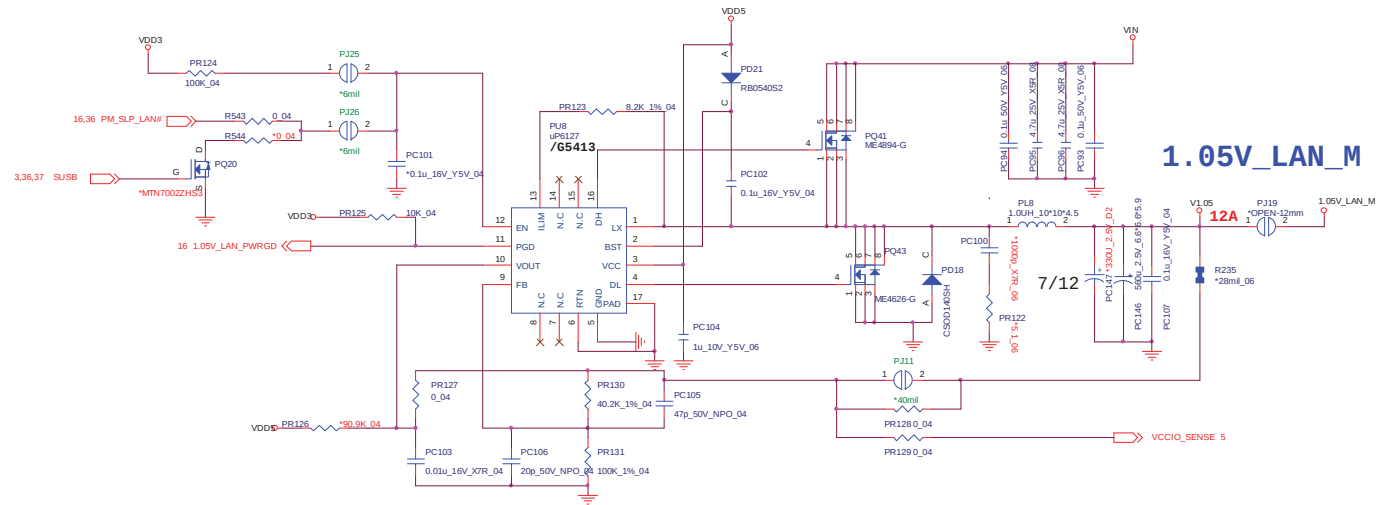


Sheet 37 of 48
Power 1.5V/
0.75V,1.8VS

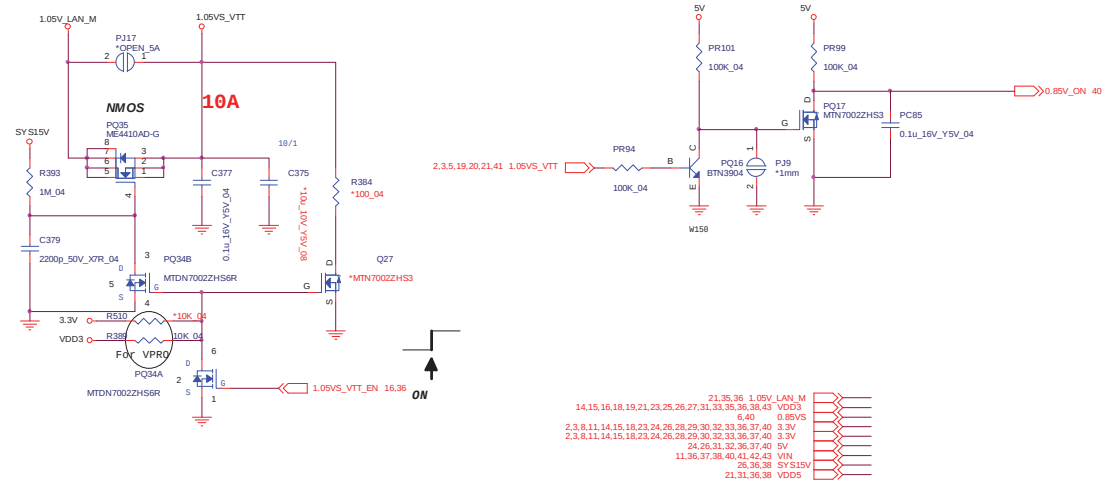
Schematic Diagrams

POWER 1.05V LAN M

Sheet 39 of 48
POWER 1.05V LAN
M

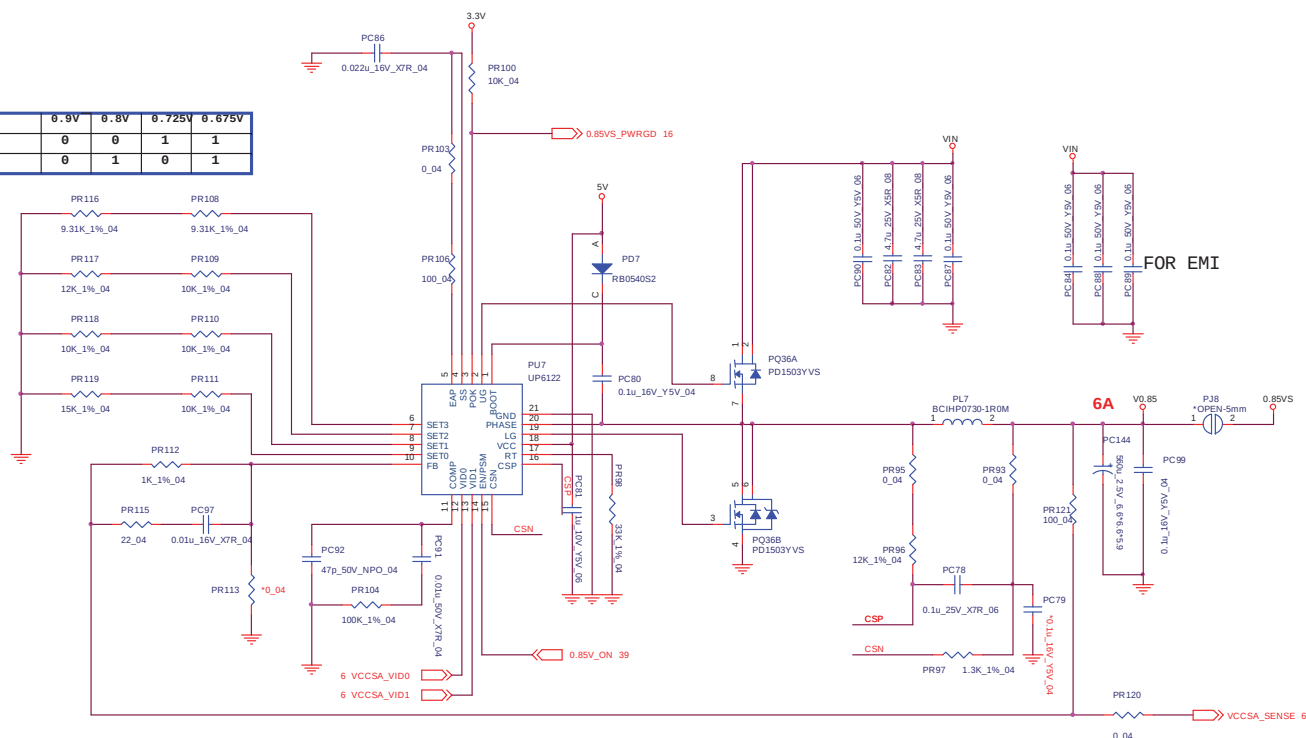


1.05VS_VTT



POWER 0.85VS

	0.9V	0.8V	0.725V	0.675V
VCCSA_VID0	0	0	1	1
VCCSA_VID1	0	1	0	1



Sheet 40 of 48
POWER 0.85VS

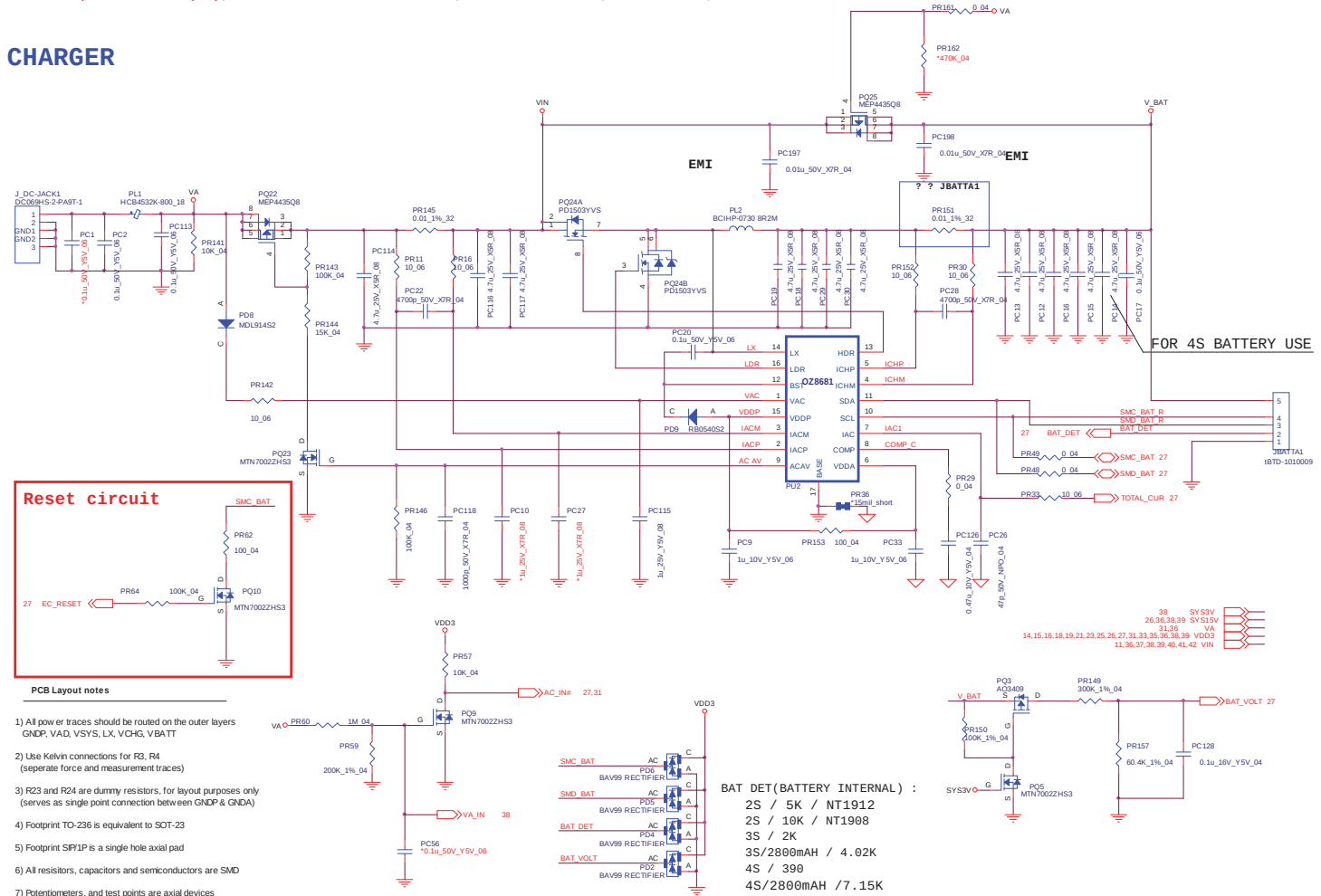
VCORE_2



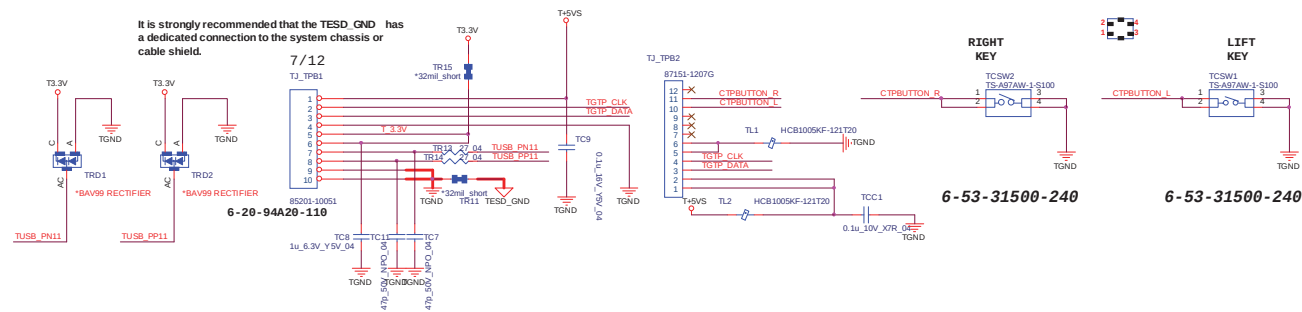
CHARGE, DC IN

? Adapter ? ? 120W(?), ? ? ? ? ? ? ? 2PCS MOSFET, 180W~220W : 3PCS , 300W: 4PCS , 360W: 5PCS

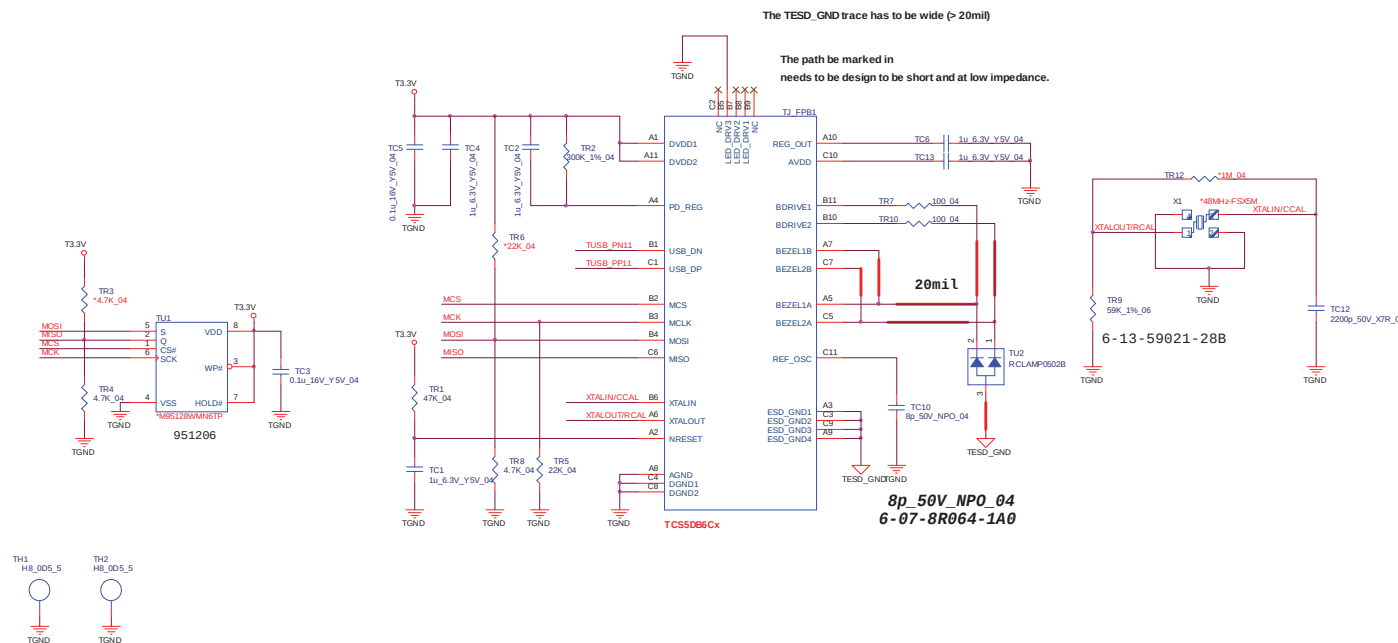
CHARGER

Sheet 43 of 48
CHARGE, DC IN

CLICK BOARD/ FG



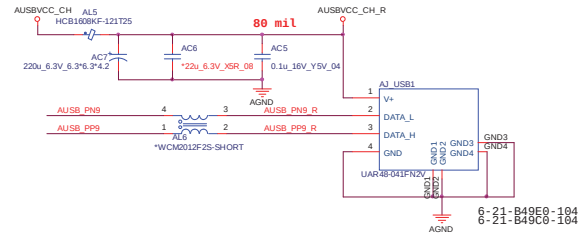
Sheet 44 of 48
CLICK BOARD/ FG



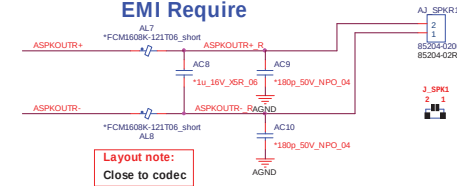
Schematic Diagrams

AUDIO BOARD/ USB, HP, MIC

USB PORT



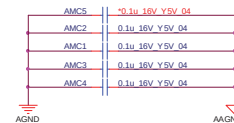
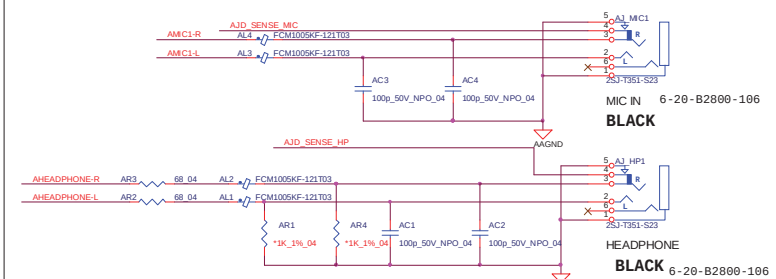
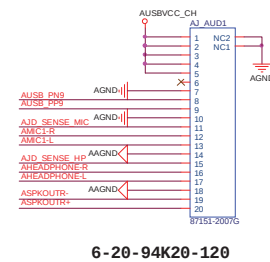
EMI Require



TO M/B

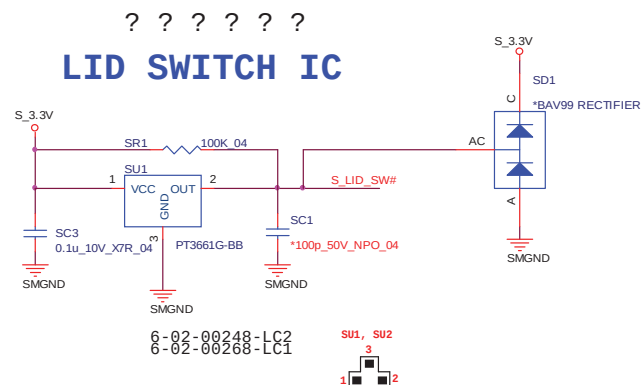
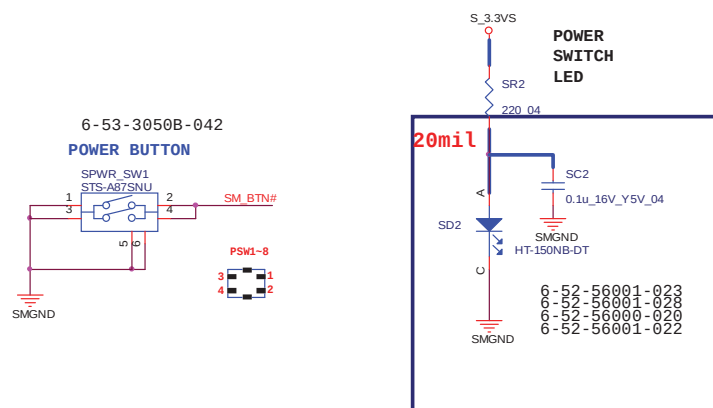
AUDIO JACK

Sheet 45 of 48
AUDIO BOARD/
USB, HP, MIC

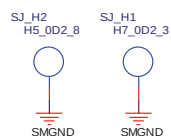
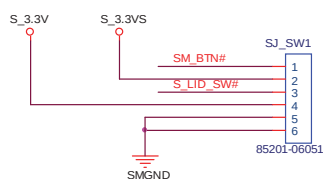


POWER SWITCH

POWER SW & LED & HOT KEY



Sheet 46 of 48
POWER SWITCH



80 PORT DEBUG RD111

Sheet 47 of 48
DEBUG BOARD

