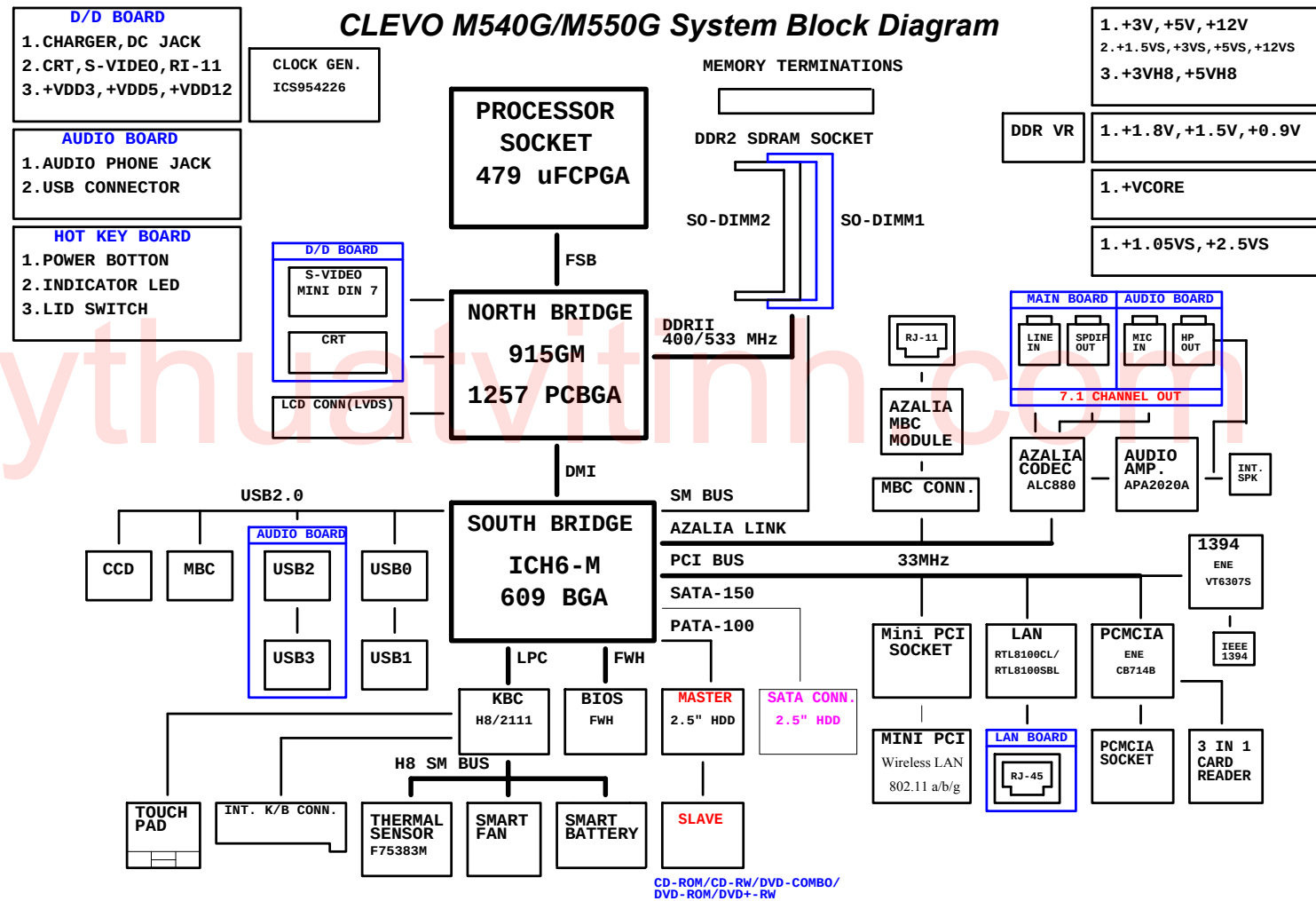
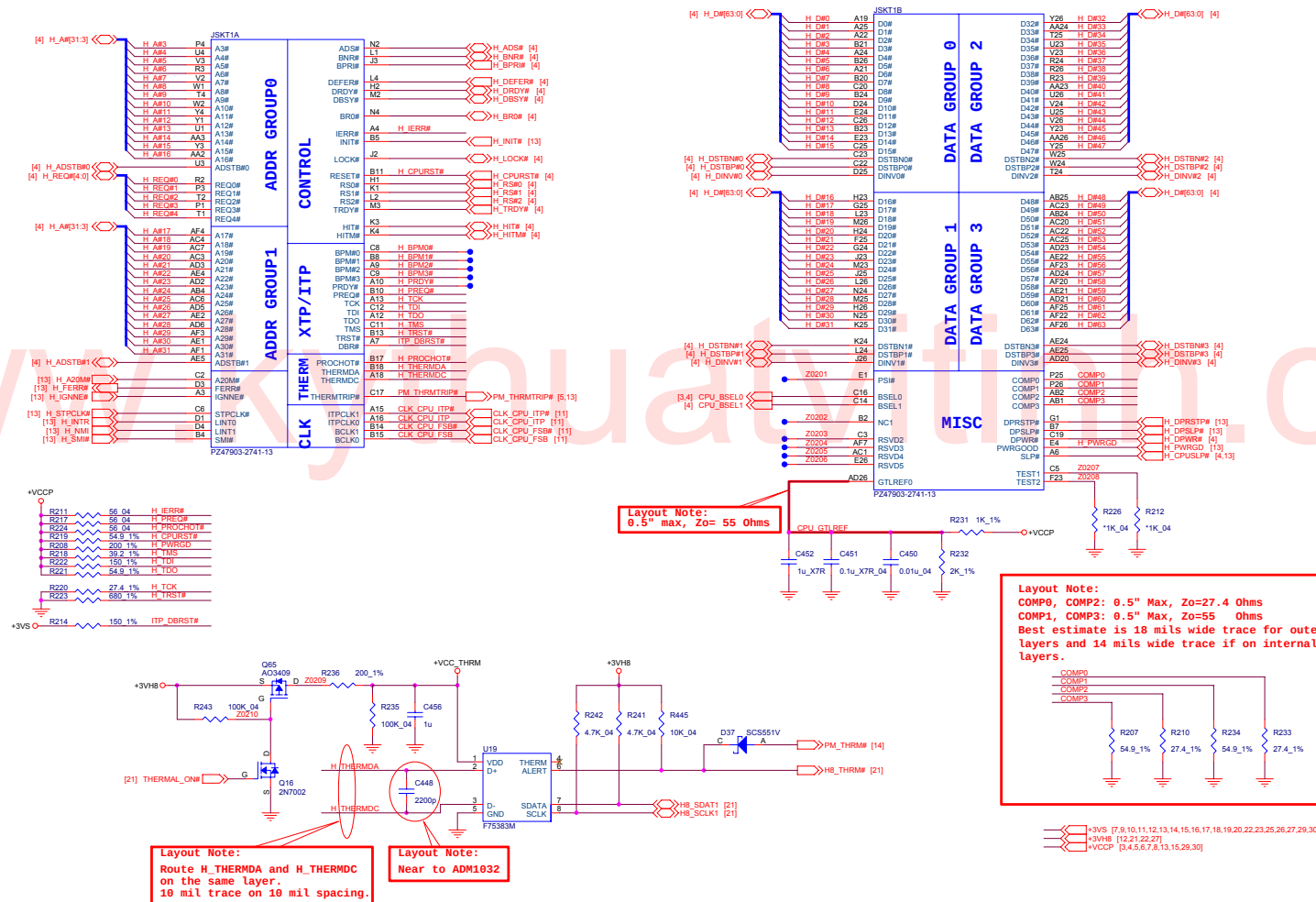


System Block Diagram



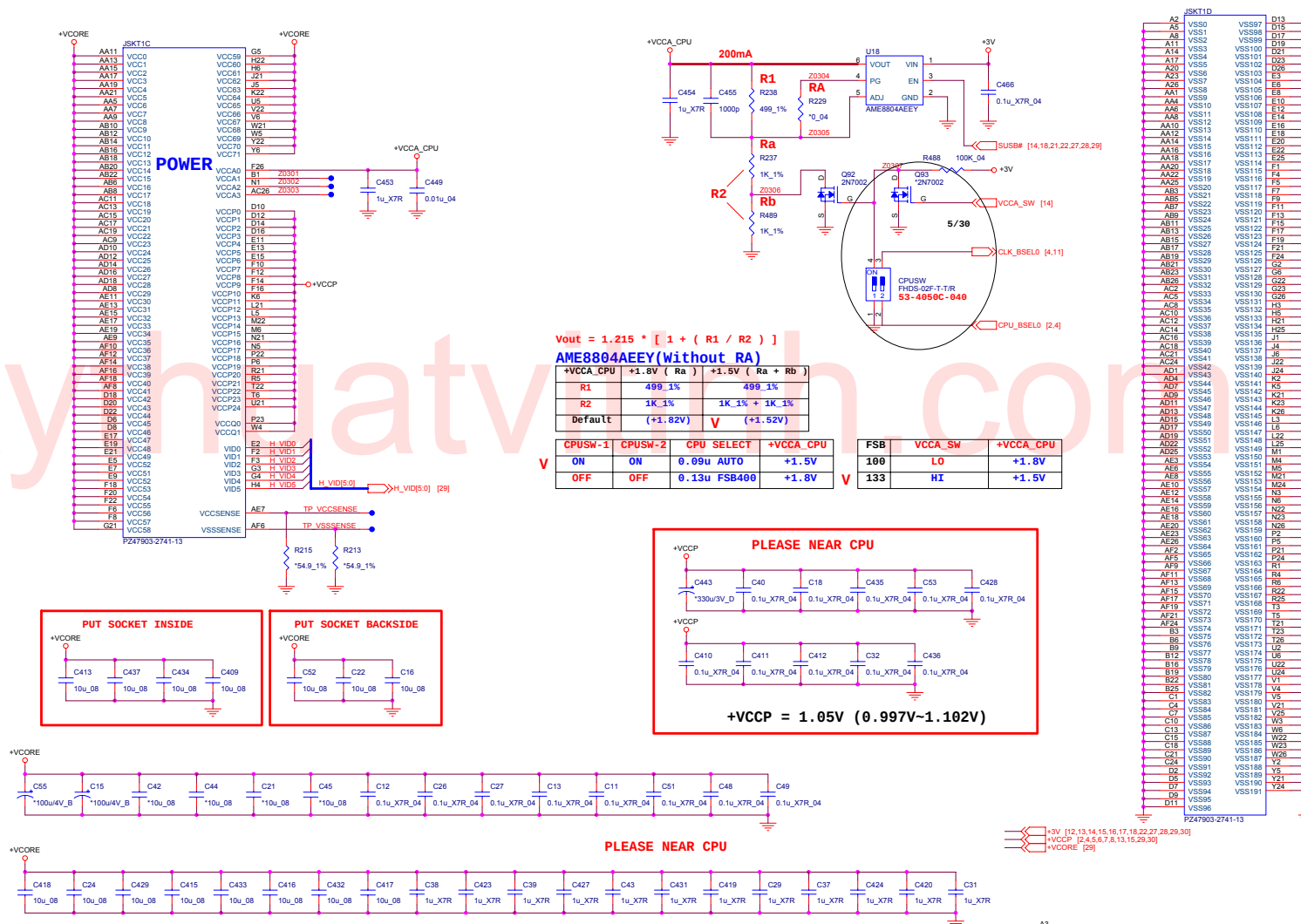
Sheet 1 of 40
System Block
Diagram

DOTHAN 1/2

Sheet 2 of 40
DOTHAN 1/2

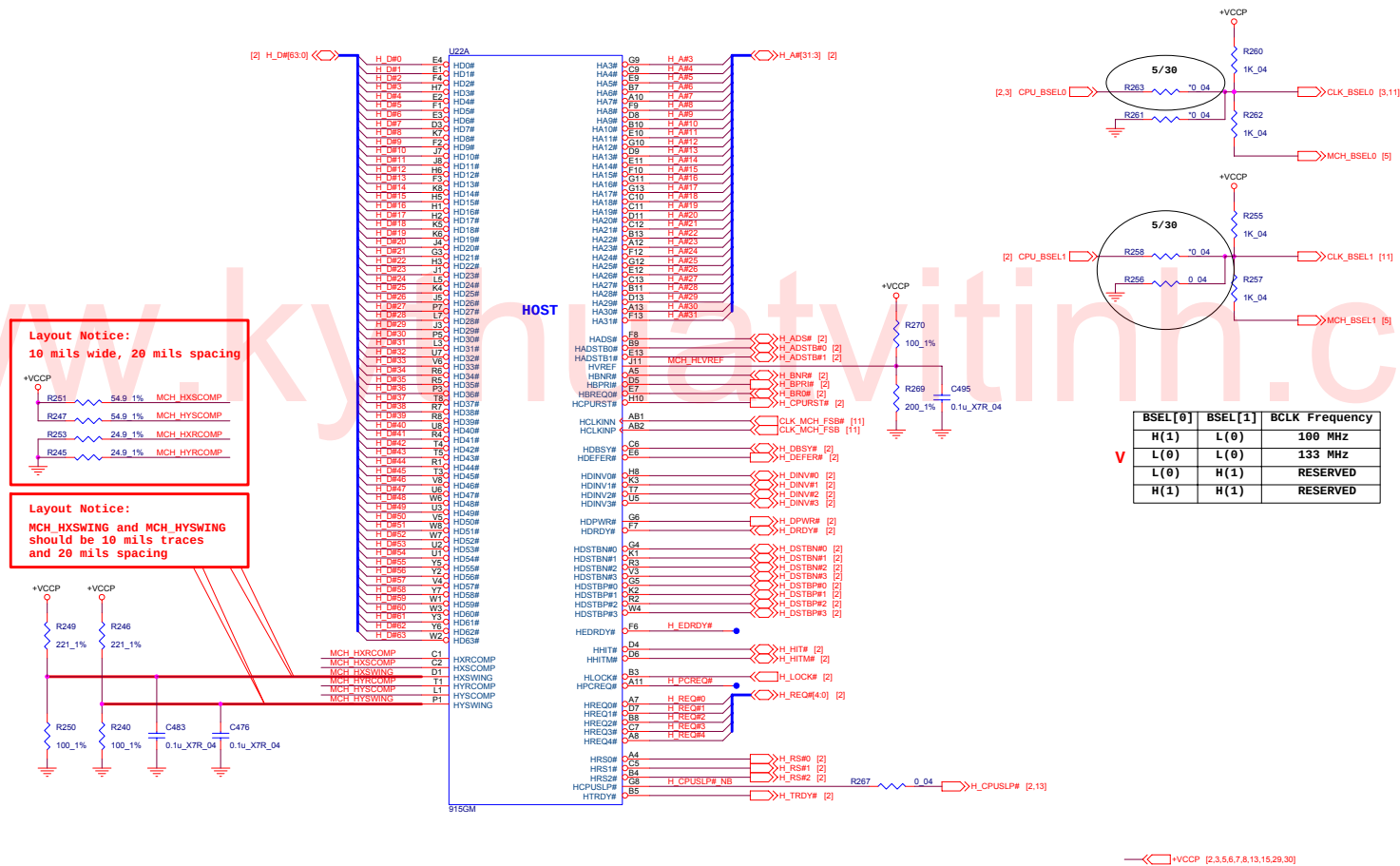
B.Schematic Diagrams

Sheet 3 of 40
DOTHAN 2/2



Schematic Diagrams

915GM 1/5



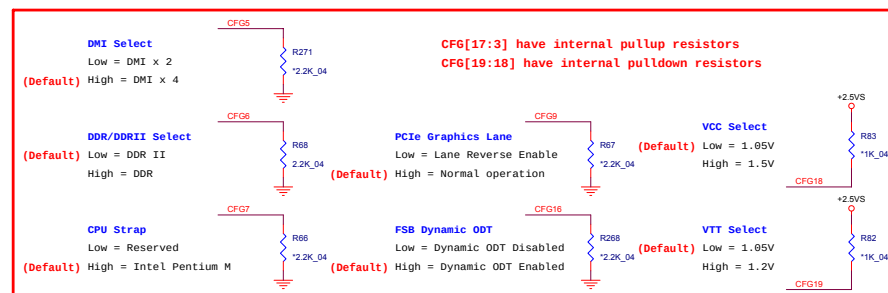
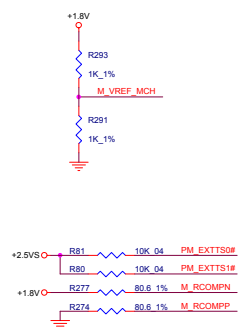
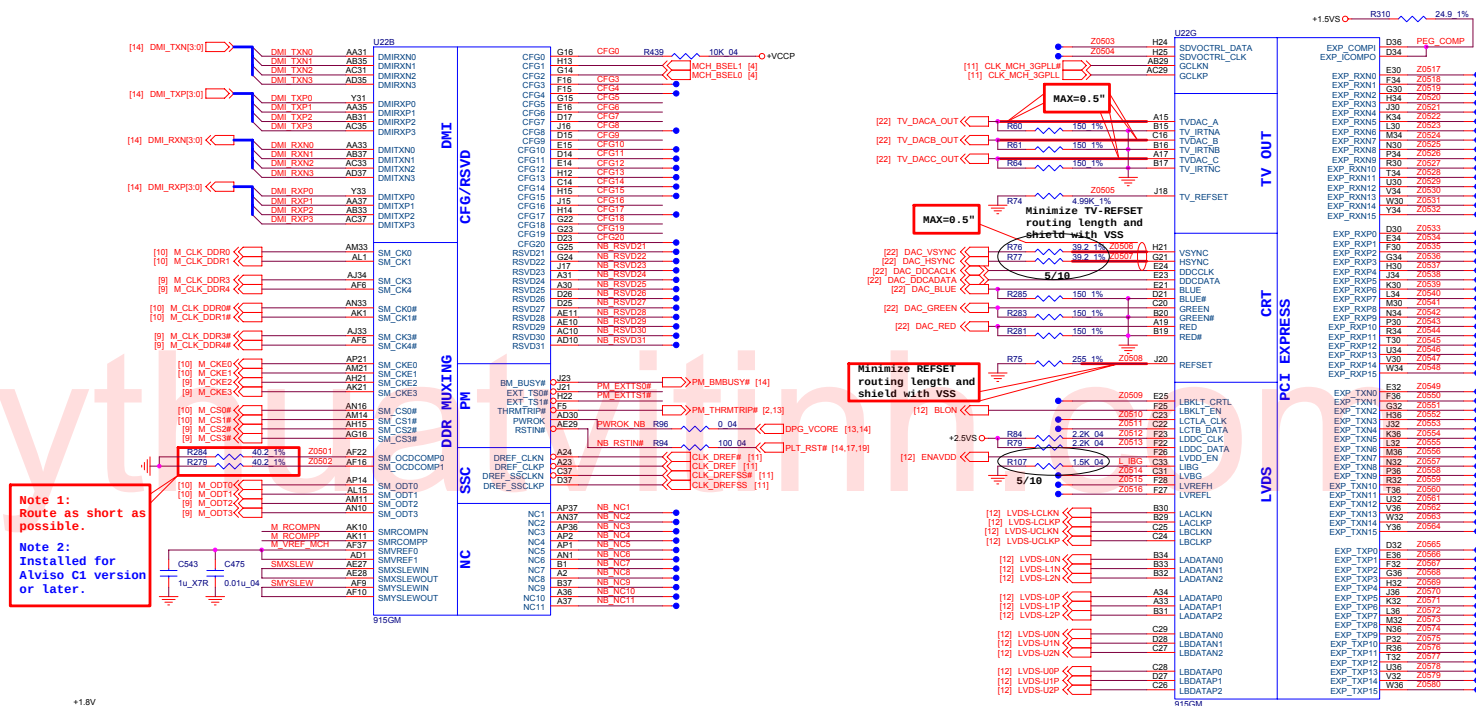
Sheet 4 of 40
915GM 1/5

B. Schematic Diagrams

915GM 2/5

B.Schematic Diagrams

Sheet 5 of 40
915GM 2/5



CFG9:PCIe Graphics Lane

NOTE: Ohlone CRB is strapped for PCI-E lane reversal for ease of routing. If in integrated GFX mode, need to use lane-reversal ADD2 add-in card since SDVO if does not support lane reversal.

 +1.5VS [7,14,15,27]
 +1.8V [7,8,9,10,28]
 +2.5VS [7,12,15,22,30]
 +VCCP [2,3,4,6,7,8,13,15,29,30]

B.Schematic Diagrams

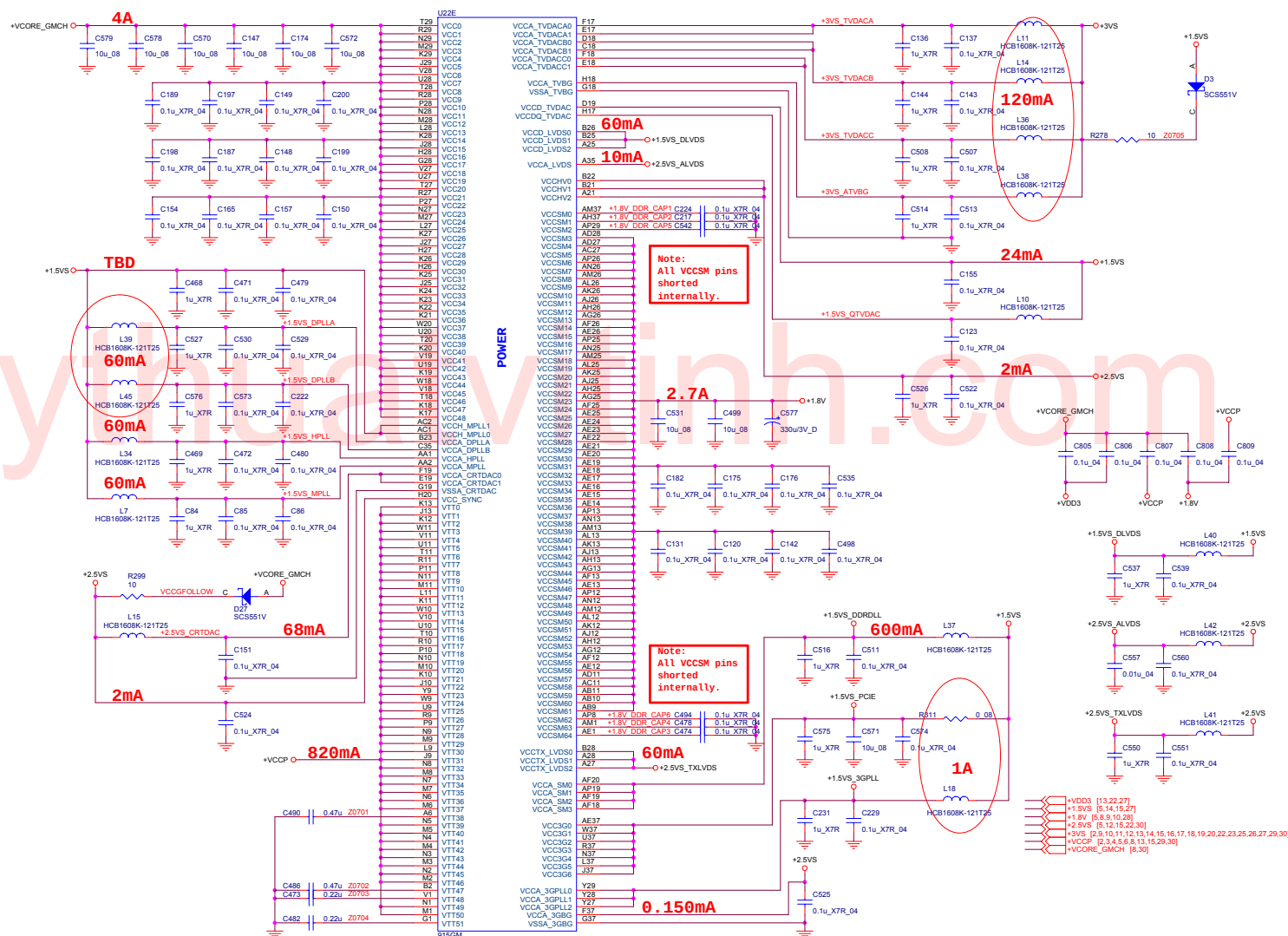
Sheet 6 of 40
915GM 3/5



915GM 4/5

B. Schematic Diagrams

Sheet 7 of 40
915GM 4/5



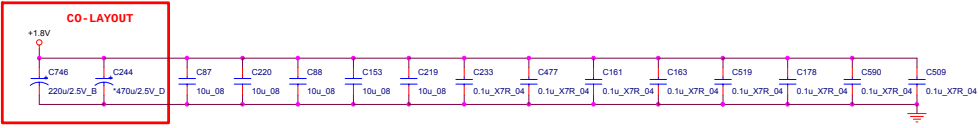
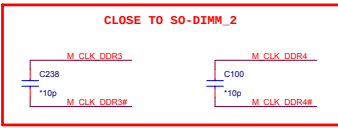
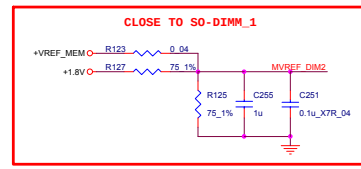
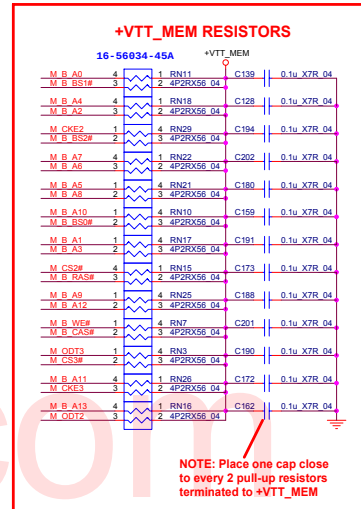
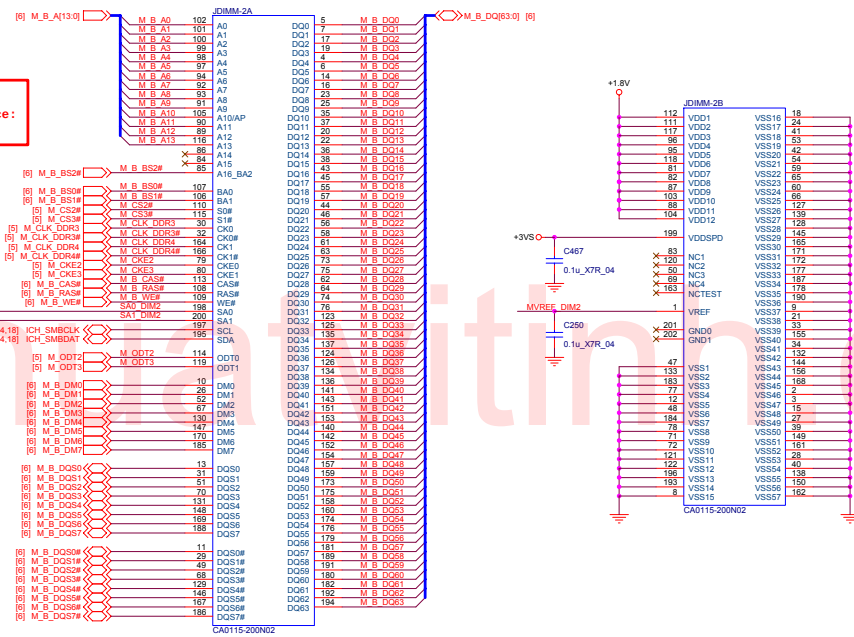
Schematic Diagrams

DRII SO-DIMM 2

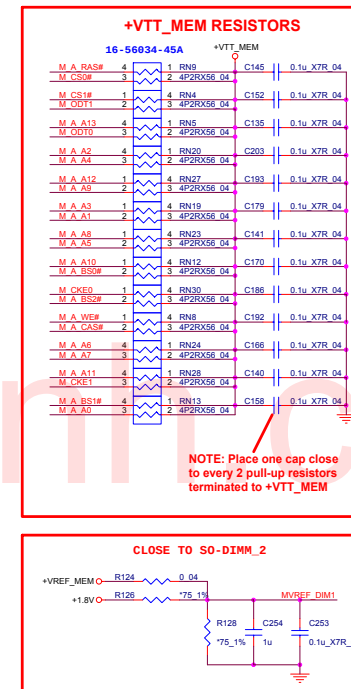
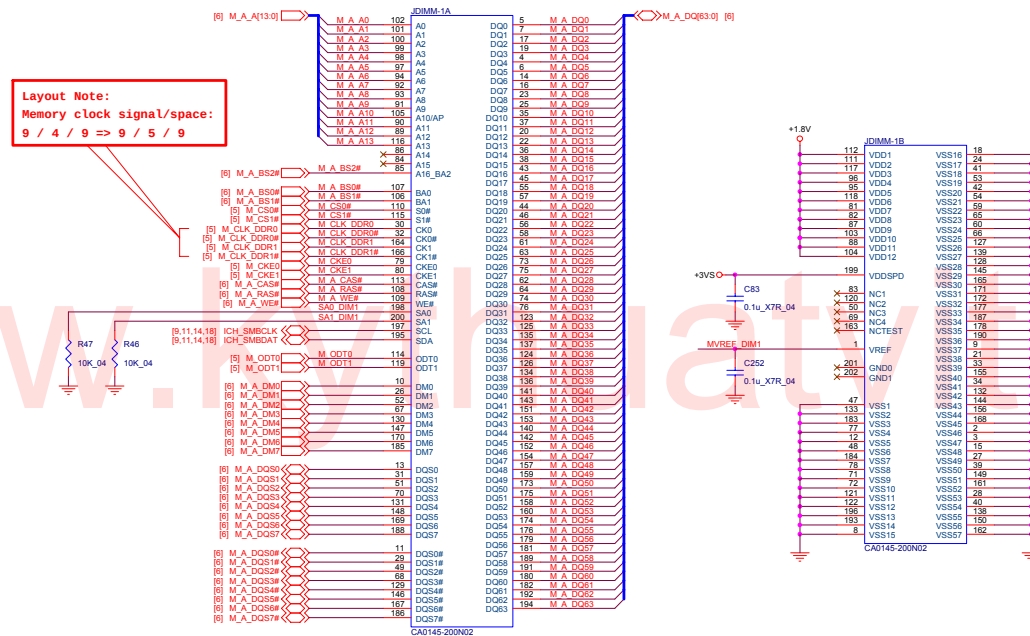
SO-DIMM 2

Sheet 9 of 40
DRII SO-DIMM 2

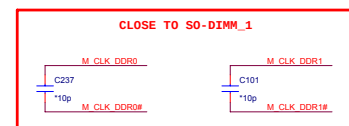
Layout Note:
Memory clock signal/space:
9 / 4 / 9 => 9 / 5 / 9



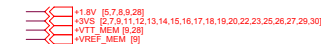
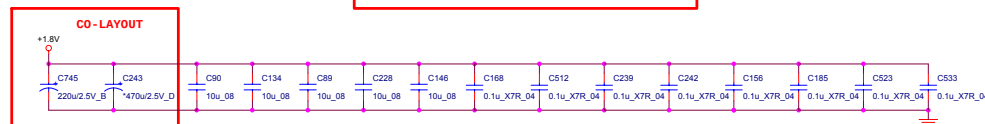
SO-DIMM 1



Sheet 10 of 40
DDRII SO-DIMM 1



NOTE:
SO-DIMM_1 is placed farther from
the GMCH than SO-DIMM_2

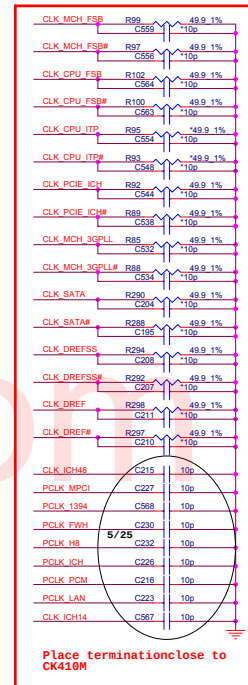
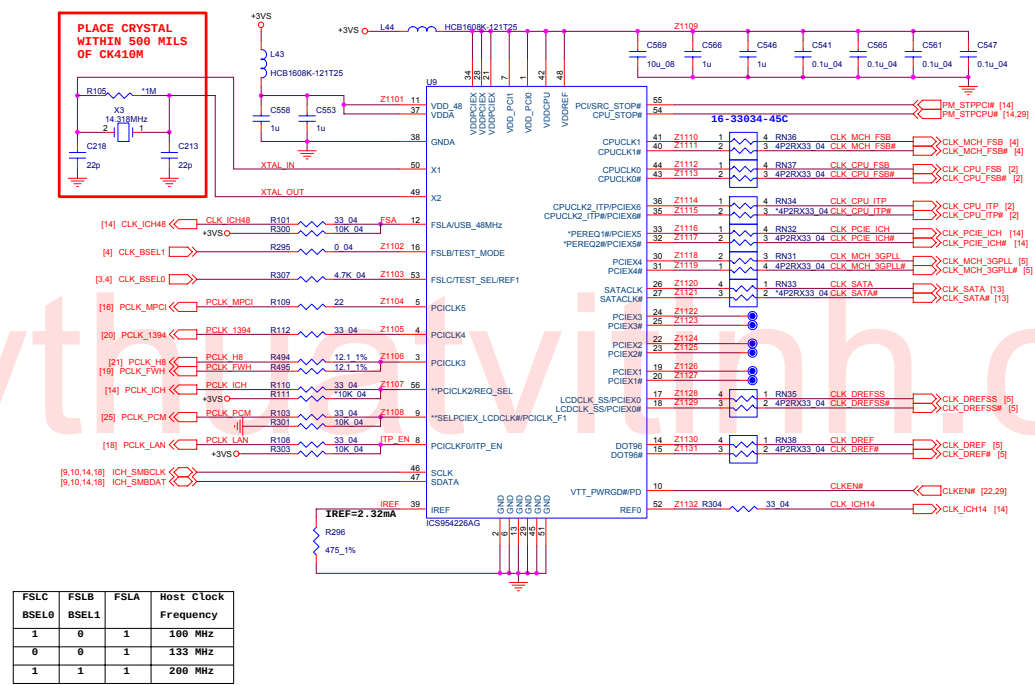


Schematic Diagrams

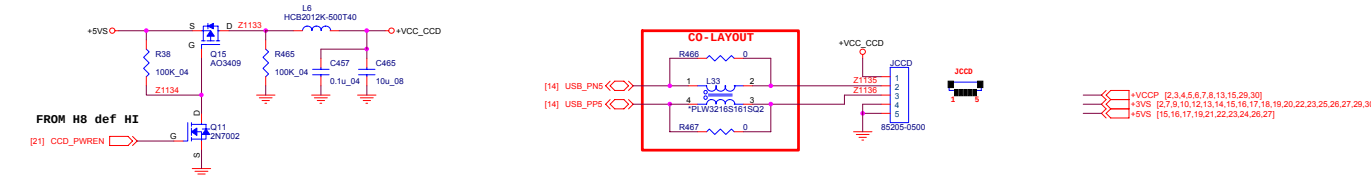
CLOCK GENERATOR, CCD

CLOCK GENERATOR

Sheet 11 of 40
CLOCK
GENERATOR, CCD



CCD



Schematic Diagrams

The schematic diagram illustrates the power supply circuit for the LCD module. A +3VS input is connected to a network of resistors (RN46, RN45, Z1203) and capacitors (CLCDI03, CLCDI02, CLCDI00). The output is connected to the LCD03, LCD02, and LCD00 pins of the LCD module.

Panel ID Select		Coaxial Cable		
TYPE	PANEL MODEL	JLCB-39(GP1024)	JLCB-29(GP1027)	JLCB-28(GP102)
15" XGA	AU B15XSG01	0 (GND)	0 (GND)	0 (GND)
15" XGA	CPT CLAA150X061	0 (GND)	0 (GND)	0 (GND)
15" SXGA+	AU B15SPB03	1 (NC)	0 (GND)	0 (GND)
15" SXGA+	CPT CLAA150PB03	1 (NC)	0 (GND)	0 (GND)
14" WXGA	Hydis HT140WX1-100	0 (GND)	1 (NC)	0 (GND)
14" WXGA	AU B140EW01	0 (GND)	1 (NC)	0 (GND)
14" WXGA	SANSUNG LTN140W1-L01	0 (GND)	1 (NC)	0 (GND)

FAN CONTROL

4/29

R508 4.99K_1% Z1212 1 3
R509 10K_1% 1 3
C776 0.1uF_04 1 2
U44 LMV331
FAN_ON

5/20

D44 1N4148 A 1
R10 100K_04 1 2
R11 2.2K_04 1 2
Z1210 1 2
Z1211 1 2
+VDD5
C778 10uF_08 1 2
C779 10uF_08 1 2
C780 10uF_08 1 2
C781 10uF_08 1 2
C782 10uF_08 1 2
C783 10uF_08 1 2
C784 10uF_08 1 2
C785 10uF_08 1 2
C786 10uF_08 1 2
C787 10uF_08 1 2
C788 10uF_08 1 2
C789 10uF_08 1 2
C790 10uF_08 1 2
C791 10uF_08 1 2
C792 10uF_08 1 2
C793 10uF_08 1 2
C794 10uF_08 1 2
C795 10uF_08 1 2
C796 10uF_08 1 2
C797 10uF_08 1 2
C798 10uF_08 1 2
C799 10uF_08 1 2
C800 10uF_08 1 2

4/29

Q45 AO3409 G 1
D17 SC5851V 1 2
Z1212 1 2
C394 100uF_6.3V_B 1 2
+VDD5
+3VHB
FAN_SEN

4/29

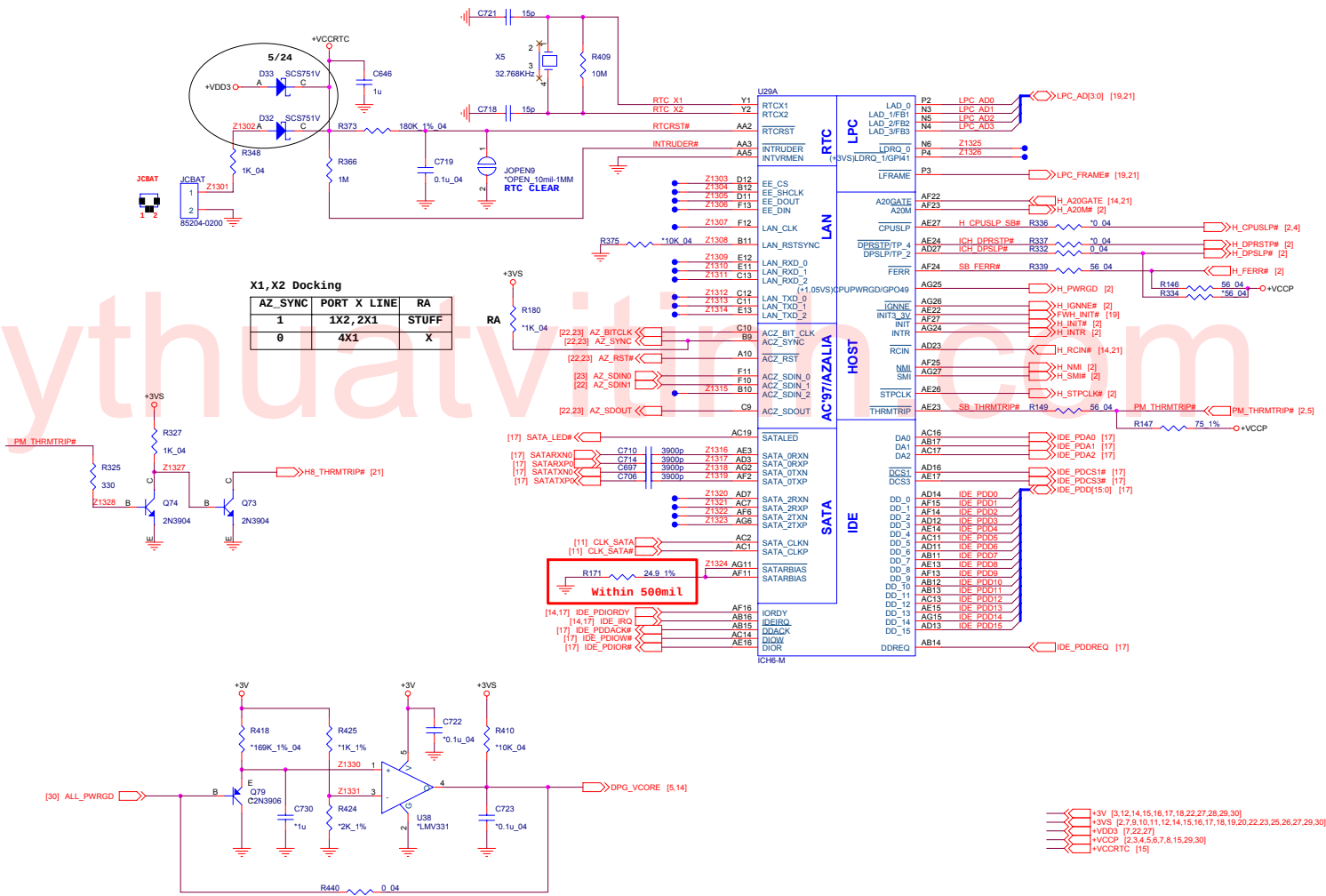
R1 4.7K_04 1 2
D1 1 2
+3VHB
FAN_SEN

Legend:

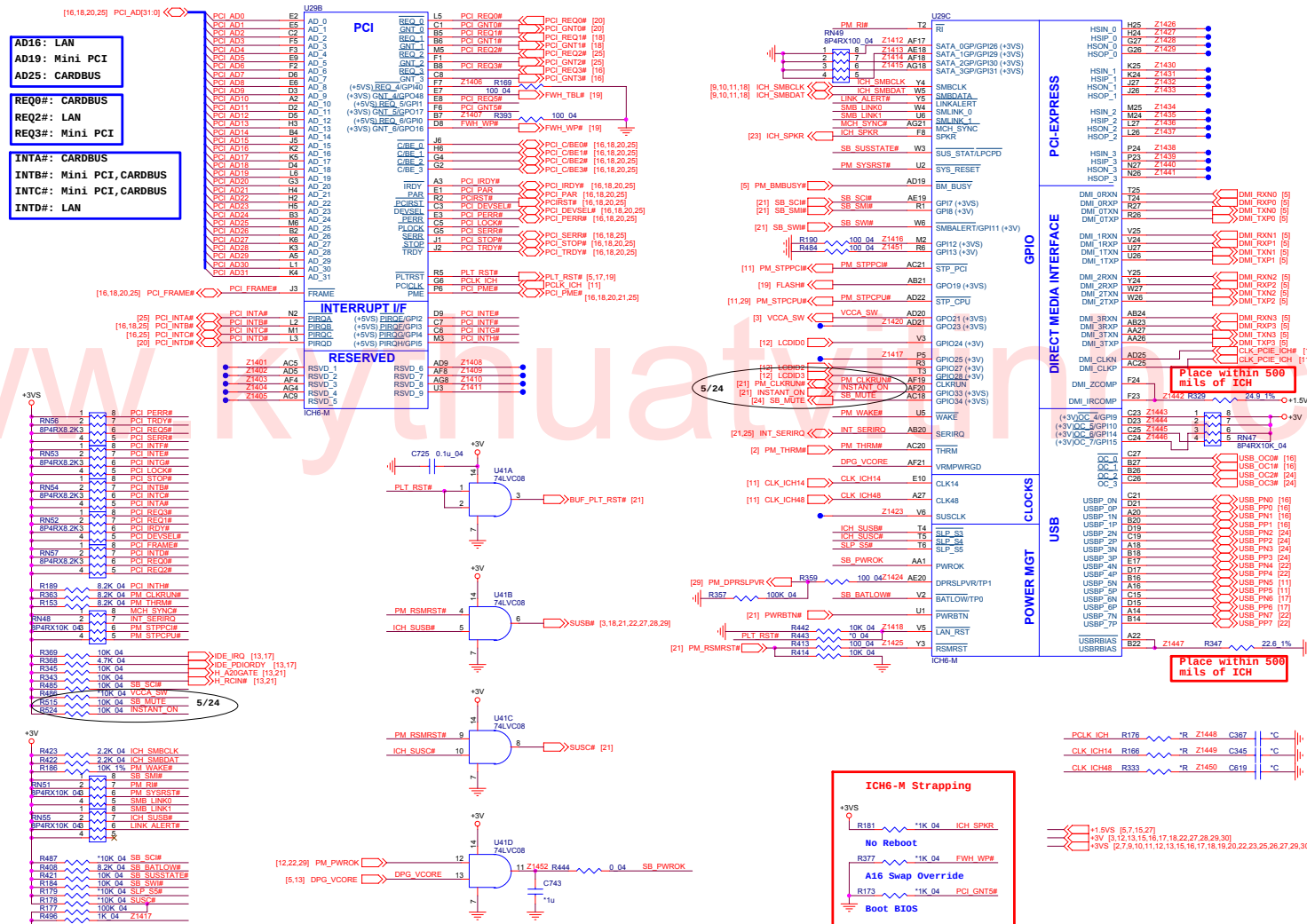
- +2.6V5 [5,7,15,22,30]
- +3V [3,13,14,15,16,17,18,22,27,28,29,30]
- +5V [2,7,8,10,11,13,14,15,16,17,18,19,20,22,23,25,26,27,29,30]
- +5VHB [2,21,22,27]
- +5VHB [19,21,27]
- +12V5 [28,27]
- +VDD5 [22,27,28,29]
- +VIN [1,2,27,28,29,30]

ICH6-M 1/3

Sheet 13 of 40
ICH6-M 1/3

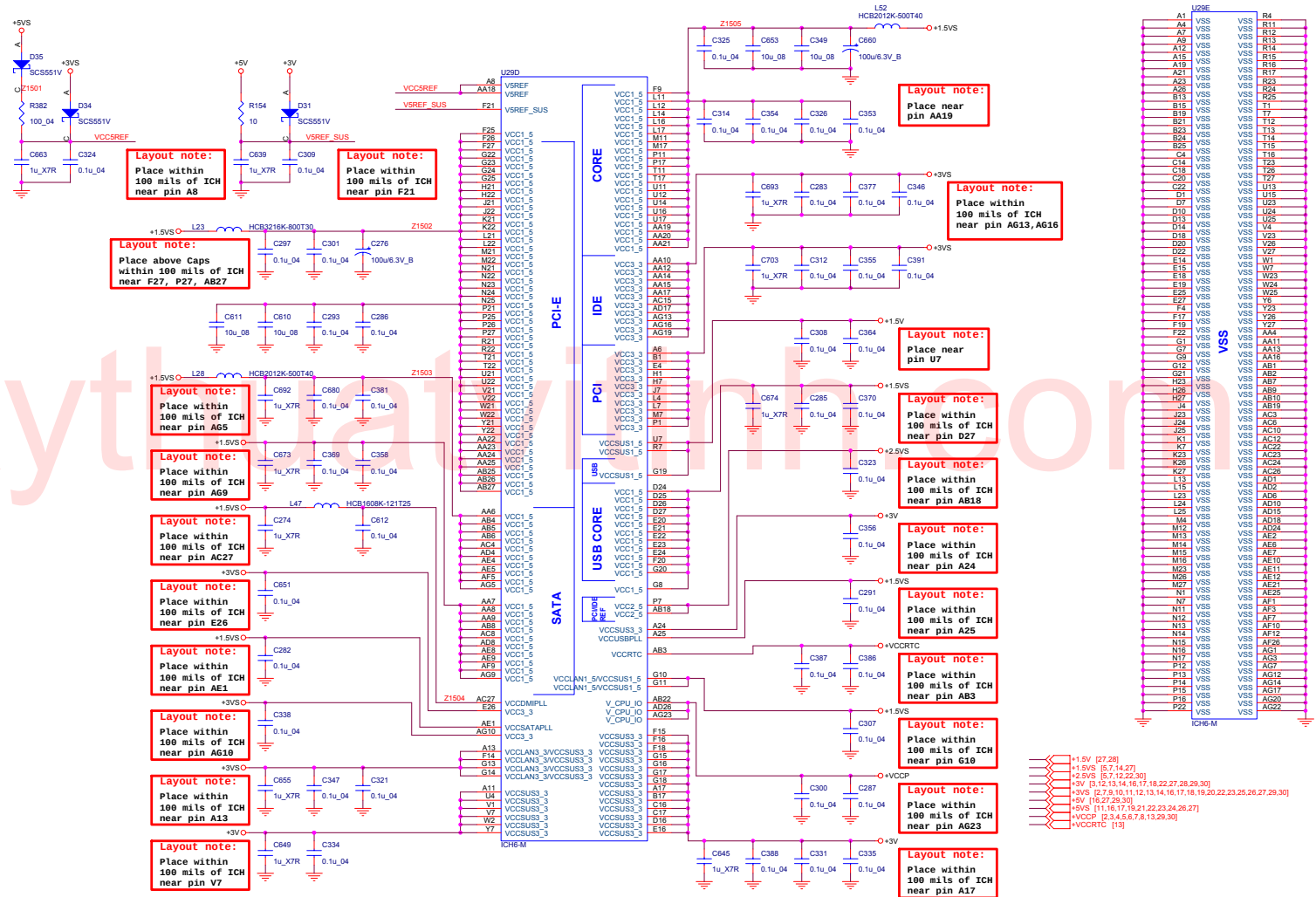


ICH6-M 2/3 B - 15

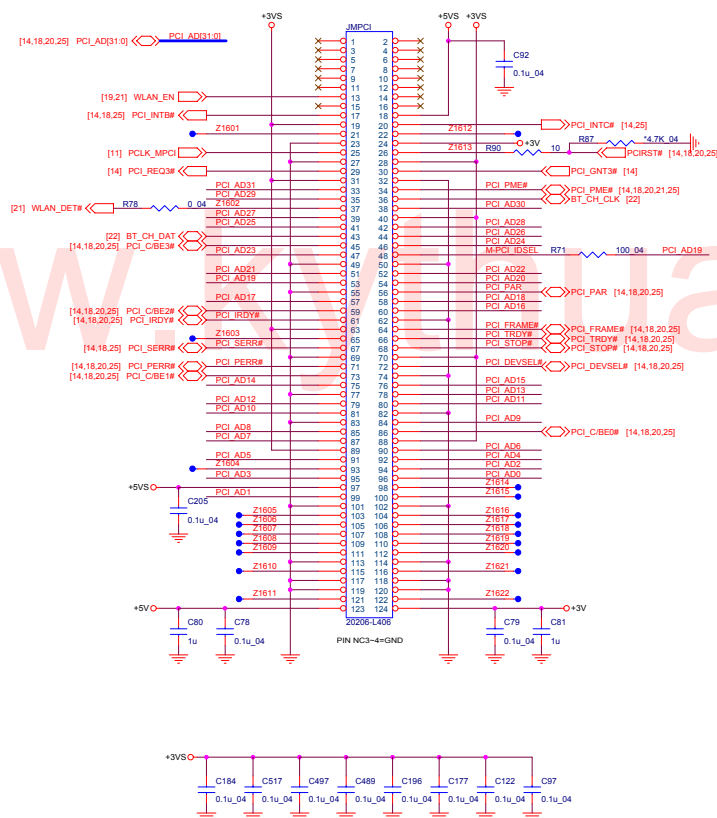


ICH6-M 3/3

Sheet 15 of 40
ICH6-M 3/3



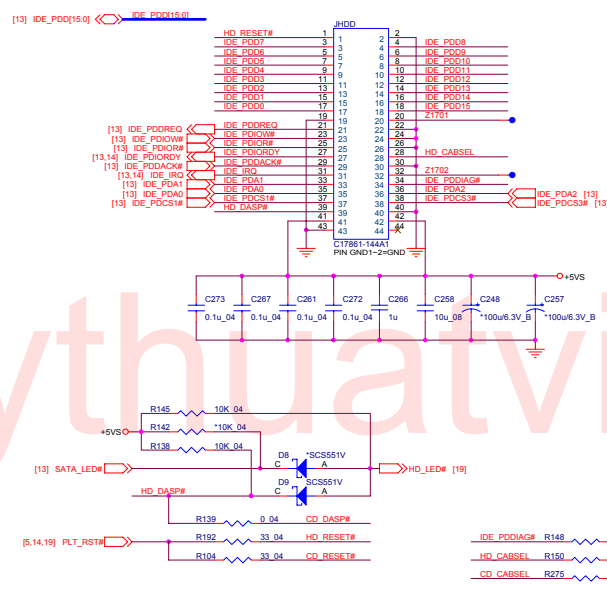
MINI PCI



The schematic diagram illustrates the USB interface circuit for the STM32F103C8T6. It features two USB connectors, JUSB1 and JUSB2, each with a USB04R0MX module. JUSB1 is connected to +VCCUSB0 and GND, while JUSB2 is connected to +VCCUSB1 and GND. Both modules are connected to the STM32F103C8T6 via USB pins. The circuit also includes a 5V regulator (U3) and various passive components like resistors (R27, R32, R36, R35), capacitors (C66, C72, C74, C76, C54, C57, C77, C82), and inductors (L2, L4, L5, L8).

Sheet 16 of 40
MINI PCI, USB2.0* 2

HDD



The schematic diagram illustrates the USB to UART bridge circuit. It features a USB connector (J24) connected to a USB to UART bridge IC (C1243N-15A1). The IC is connected to a microcontroller (U1) via a 4-pin header (J1). The microcontroller is connected to a USB connector (J23) and a UART connector (J2). The circuit includes various capacitors (C506, C503, C169, C164, C181, C510, C540, C552) and a 5V supply (O+5VS).

INT_CD_R & CD_GND & INT_CD_L must parallel routing to Audio Codec. The space must be equal.

To AUDIO CODEC

Signal:Space = 1:2

Signal:Space = 1:1

Signal:Space = 1:1

Signal:Space = 1:2

Other Signal

CD_R

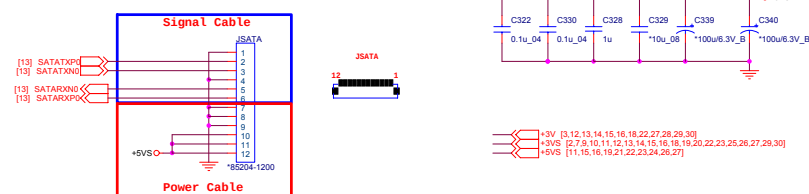
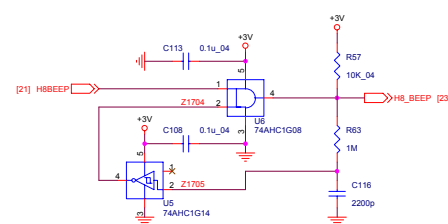
CD_G

CD_L

Other Signal

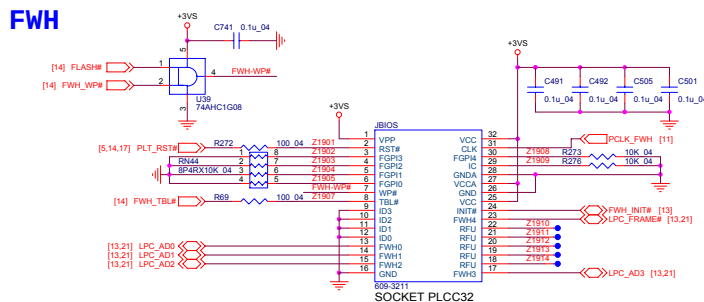
From CD-ROM

SATA HDD

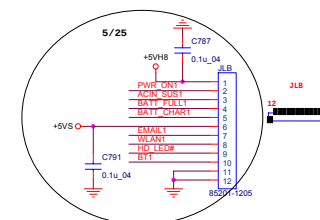


B.Schematic Diagrams

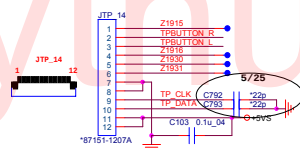
FWH



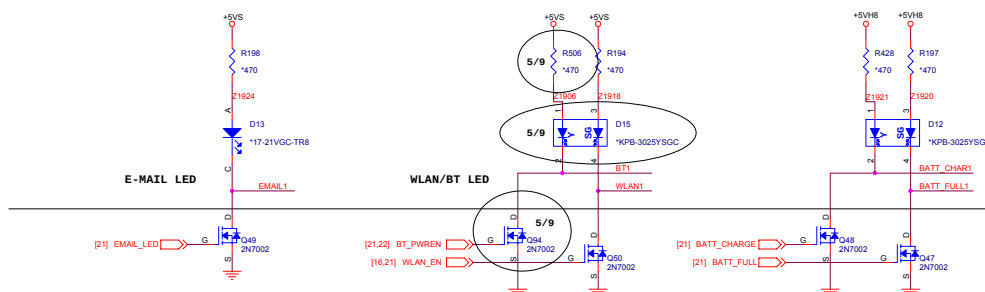
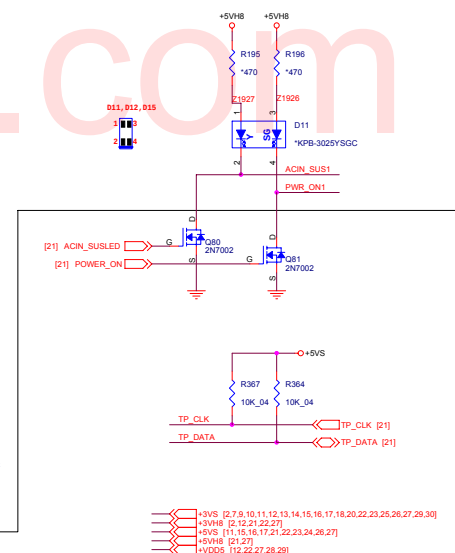
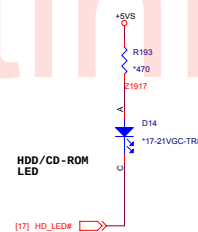
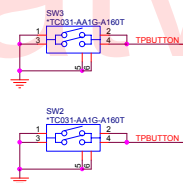
FOR M550G

**FOR M540G**

Sheet 19 of 40
FWH, TOUCH PAD,
LED

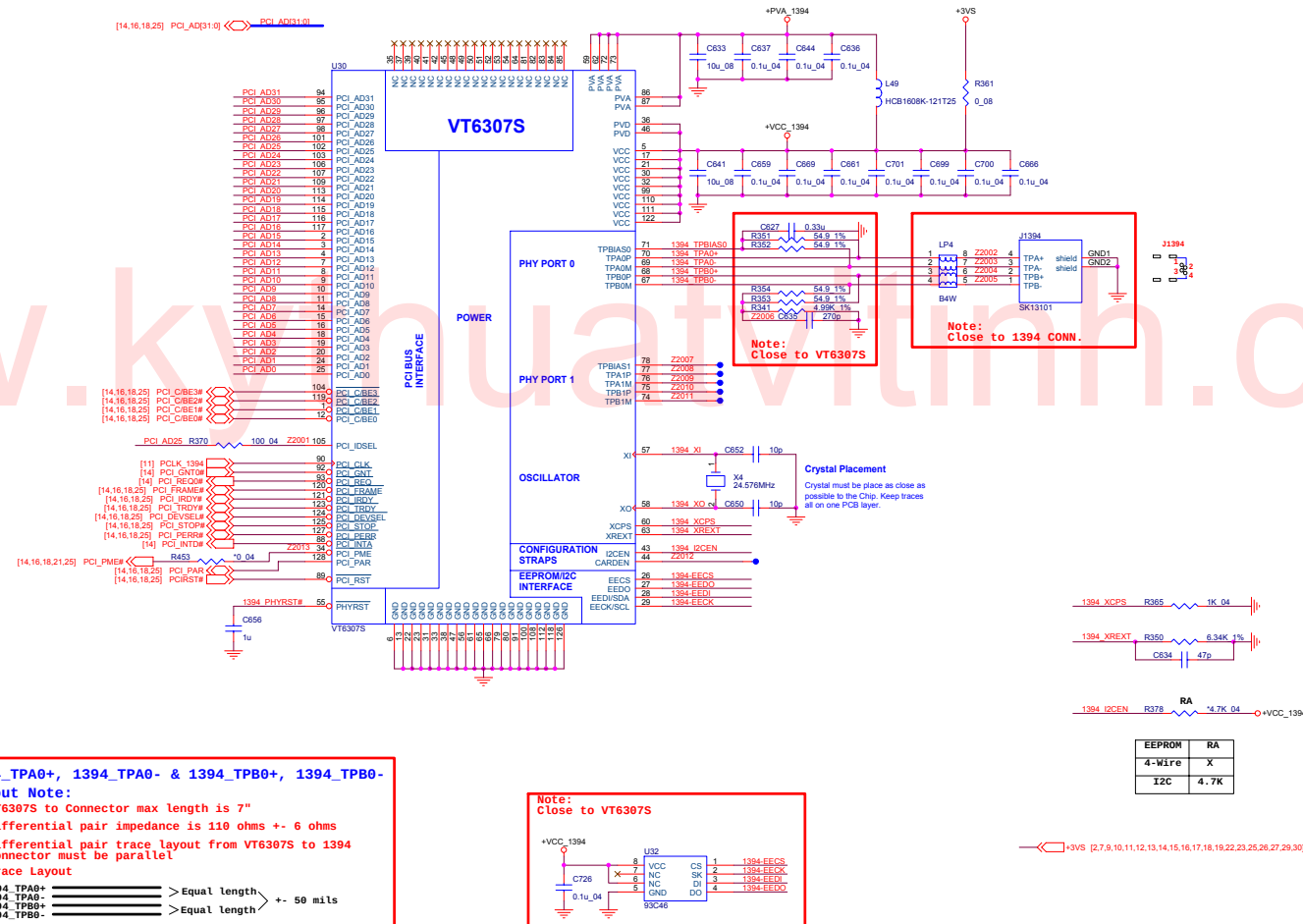


VENDOR	PART NUMBER
Synaptics	
E-LAN	800409-5102



IEEE 1394 VT6307S

IEEE1394



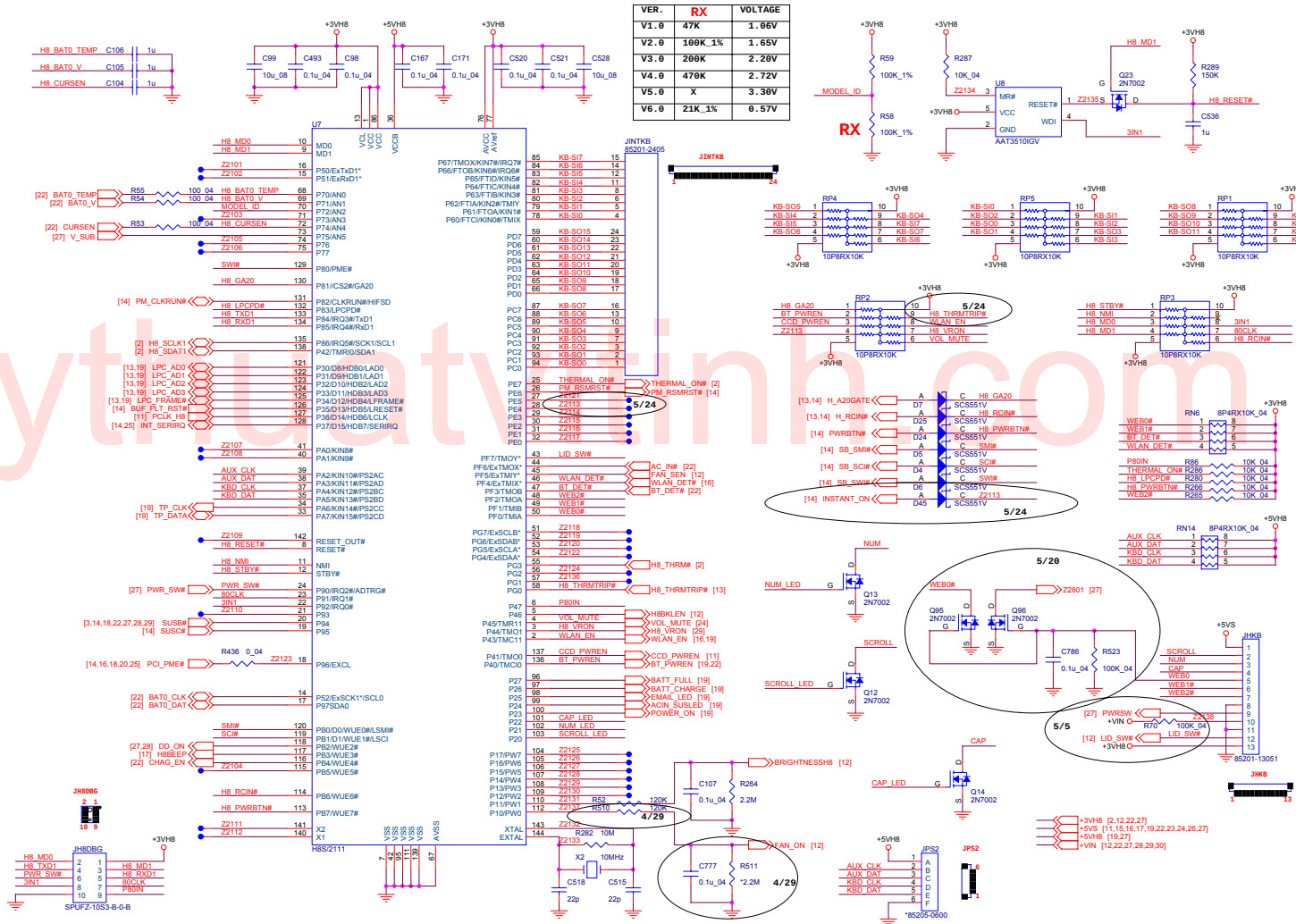
Sheet 20 of 40
IEEE 1394 VT6307S

B. Schematic Diagrams

Schematic Diagrams

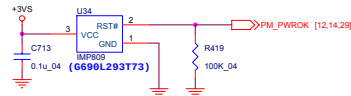
H8/2111

Sheet 21 of 40
H8/2111

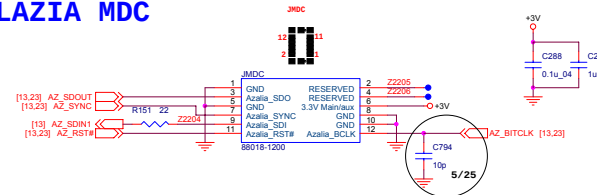


MDC, USB BT, PWRGD, DDB CON

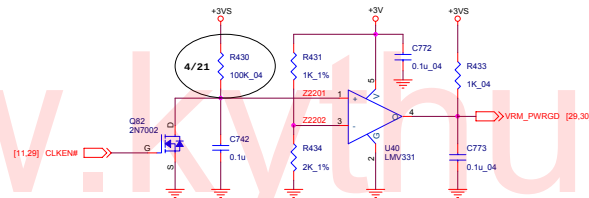
POWER OK



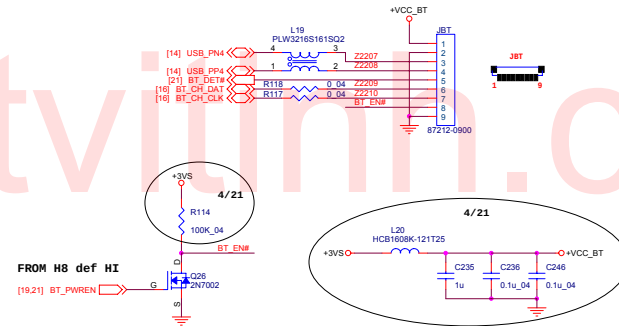
ALAZIA MDC



VCORE PWRGD



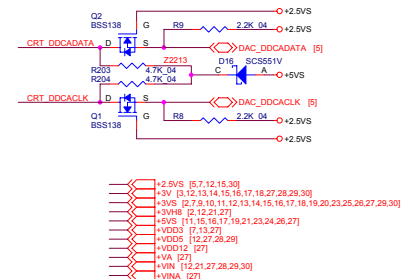
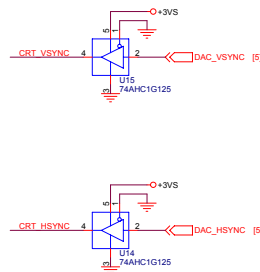
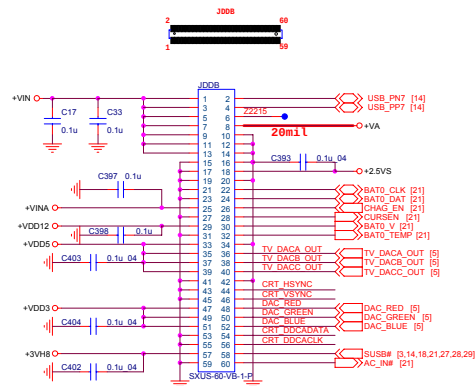
USB BLUETOOTH



Sheet 22 of 40
MDC, USB BT,
PWRGD, DDB CON

B.Schematic Diagrams

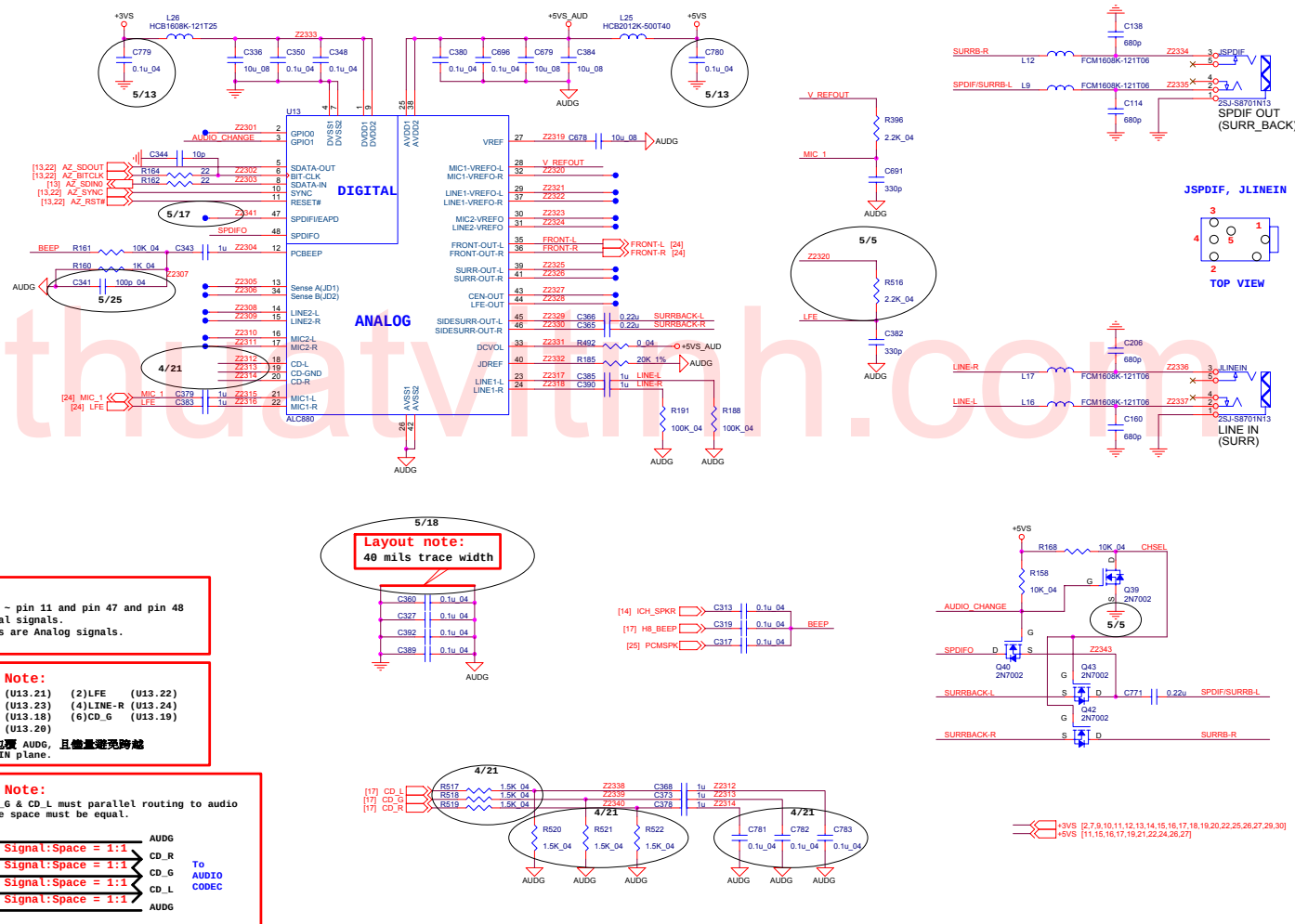
TO MULTI-FUNCTION BOARD



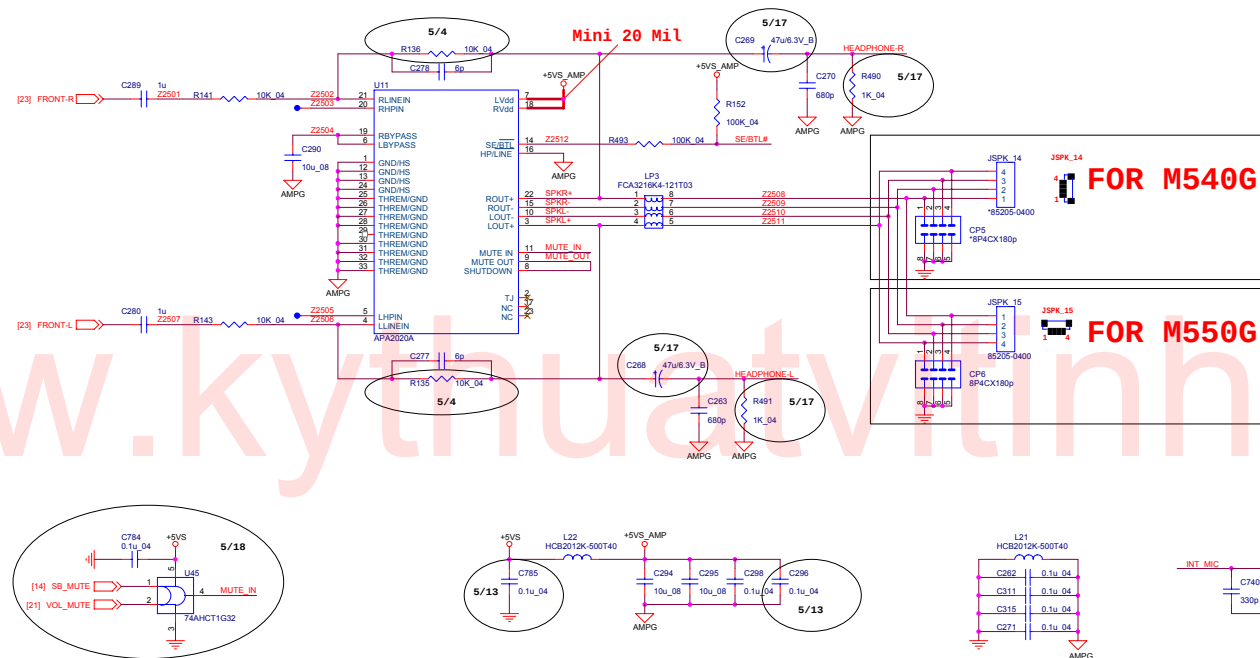
AZALIA CODEC ALC880

B. Schematic Diagrams

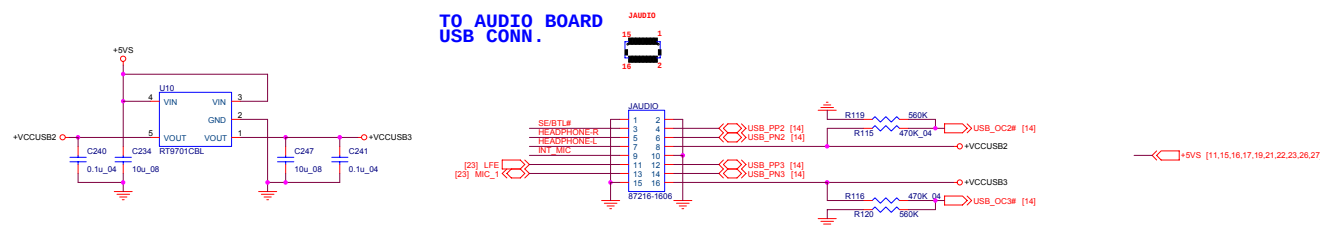
Sheet 23 of 40
AZALIA CODEC
ALC880



AUDIO AMP, USB2.0* 2

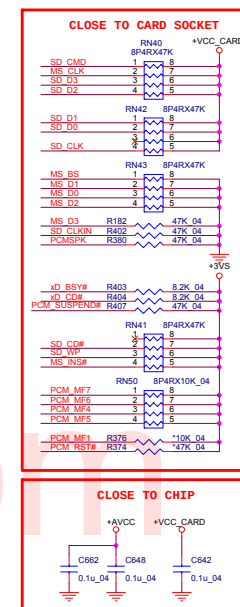
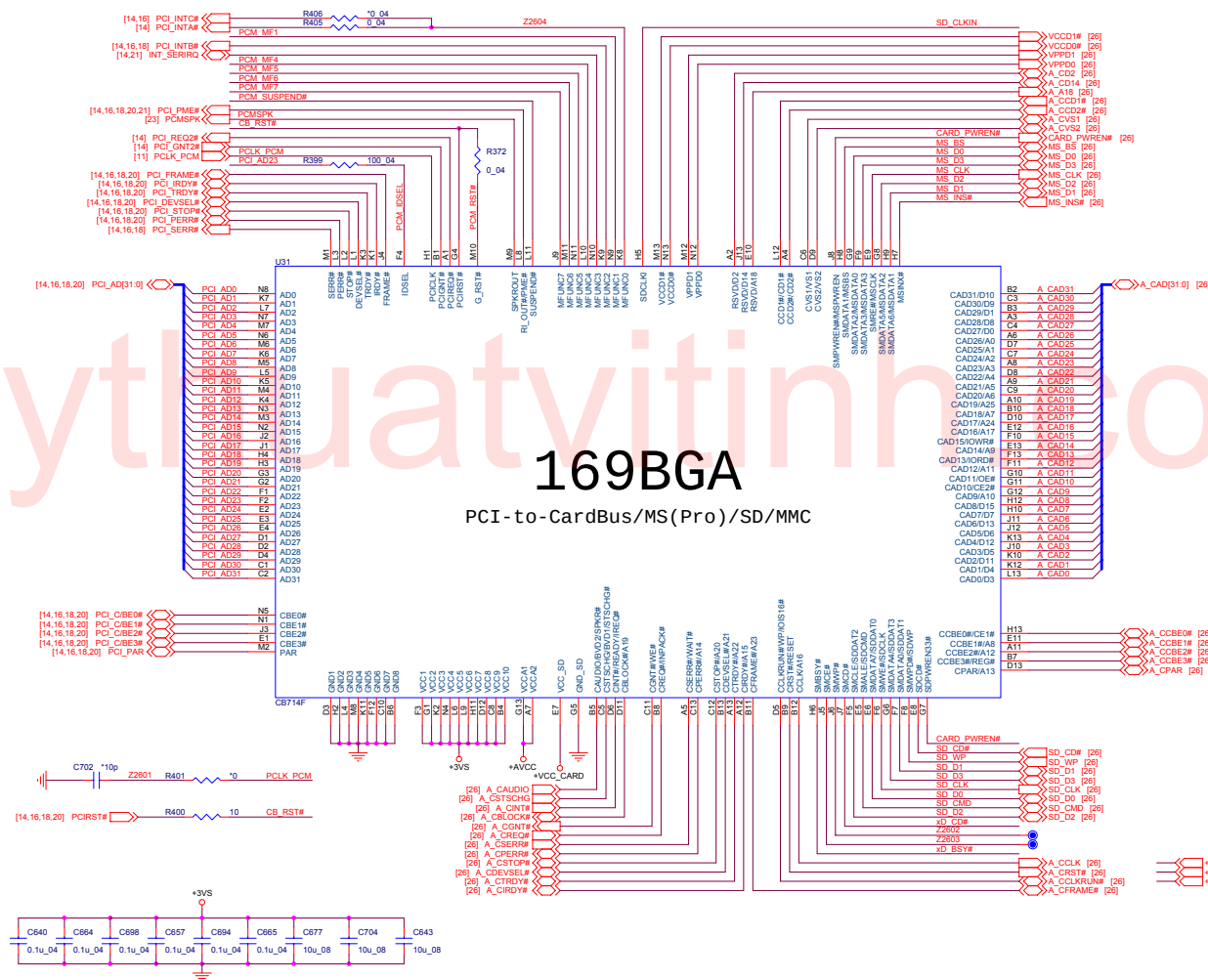


Sheet 24 of 40
AUDIO AMP, USB*
2



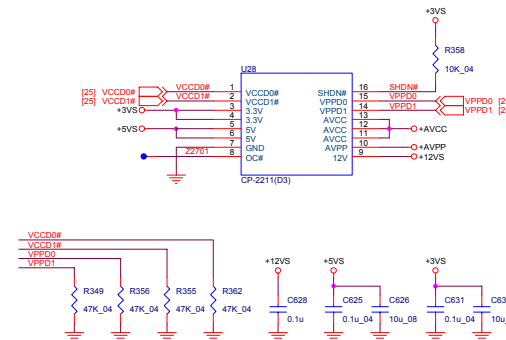
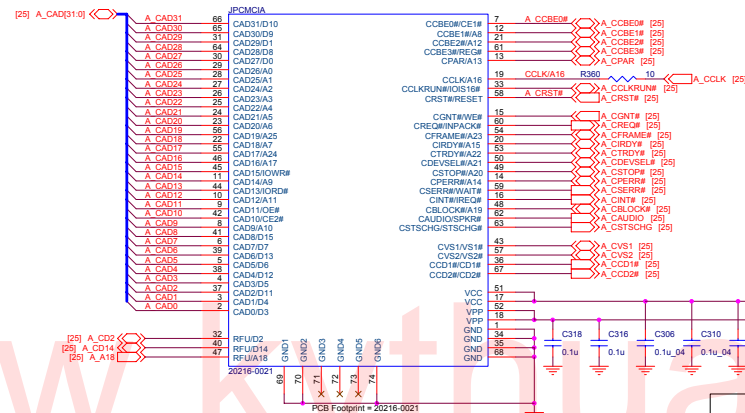
169BGA

PCI-to-CardBus/MS(Pro)/SD/MMC



PCM SOCKET, 3 IN 1 SOCKET

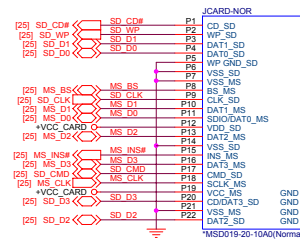
CARDBUS SOCKET



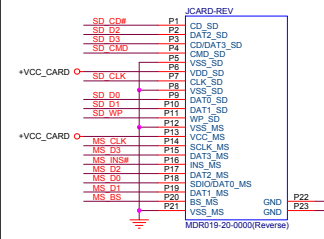
Sheet 26 of 40
PCM SOCKET, 3 IN
1 SOCKET

3 IN 1 SOCKET SD/MMC/MS(Pro)

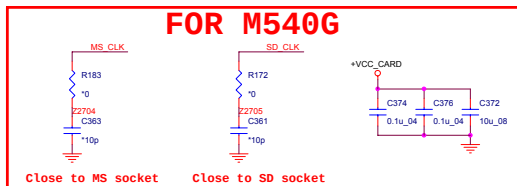
FOR M540G



FOR M550G

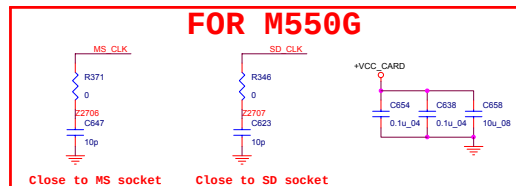


FOR M540G



Close to MS socket Close to SD socket

FOR M550G

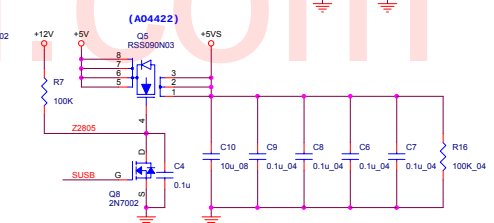
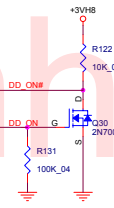
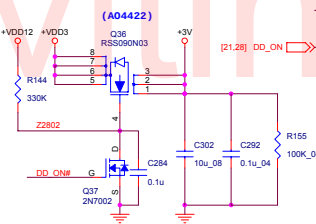
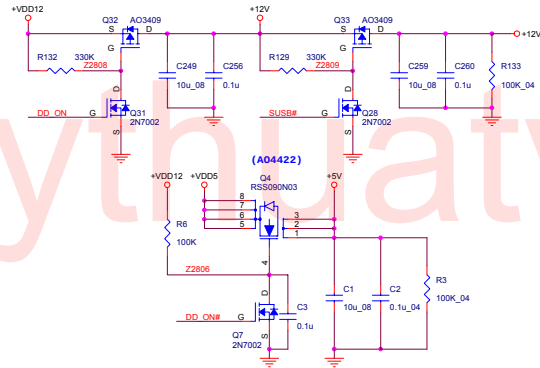
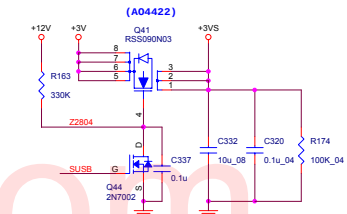
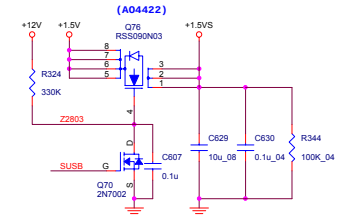
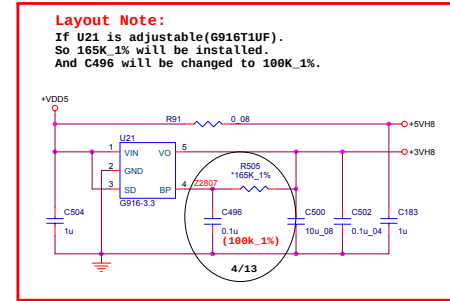
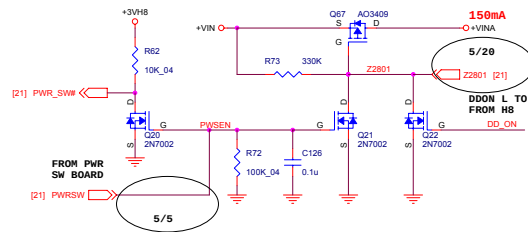


Close to MS socket Close to SD socket

+3VS [2,7,9,10,11,12,13,14,15,16,17,18,19,20,22,23,25,27,29,30]
+5VS [1,15,16,17,19,21,22,23,24,27]
+12VS [12,27]
+VCC [25]
+VCC_CARD [25]

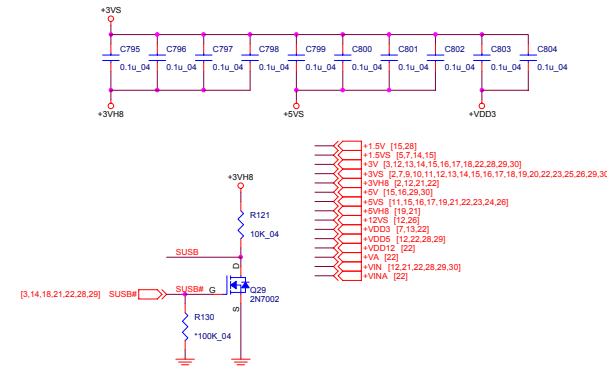
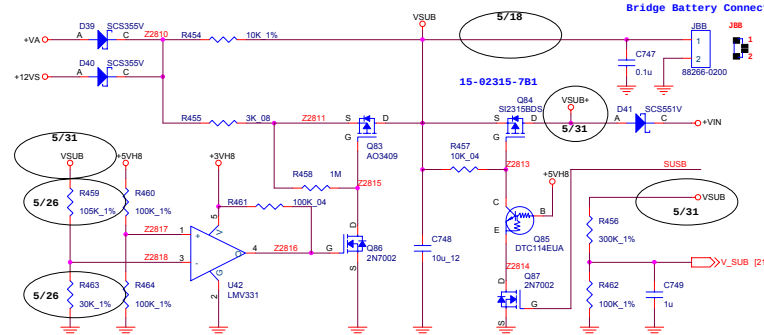
SYSEYEM POWER, BRIDGE BATT

Sheet 27 of 40
SYSTEM POWER,
BRIDGE BATT

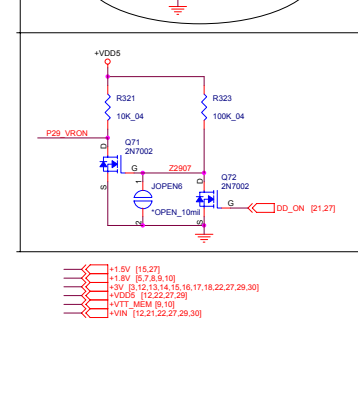
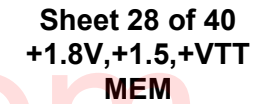


BRIDGE BATTERY

FOR M550G



+1.8V, +0.9V

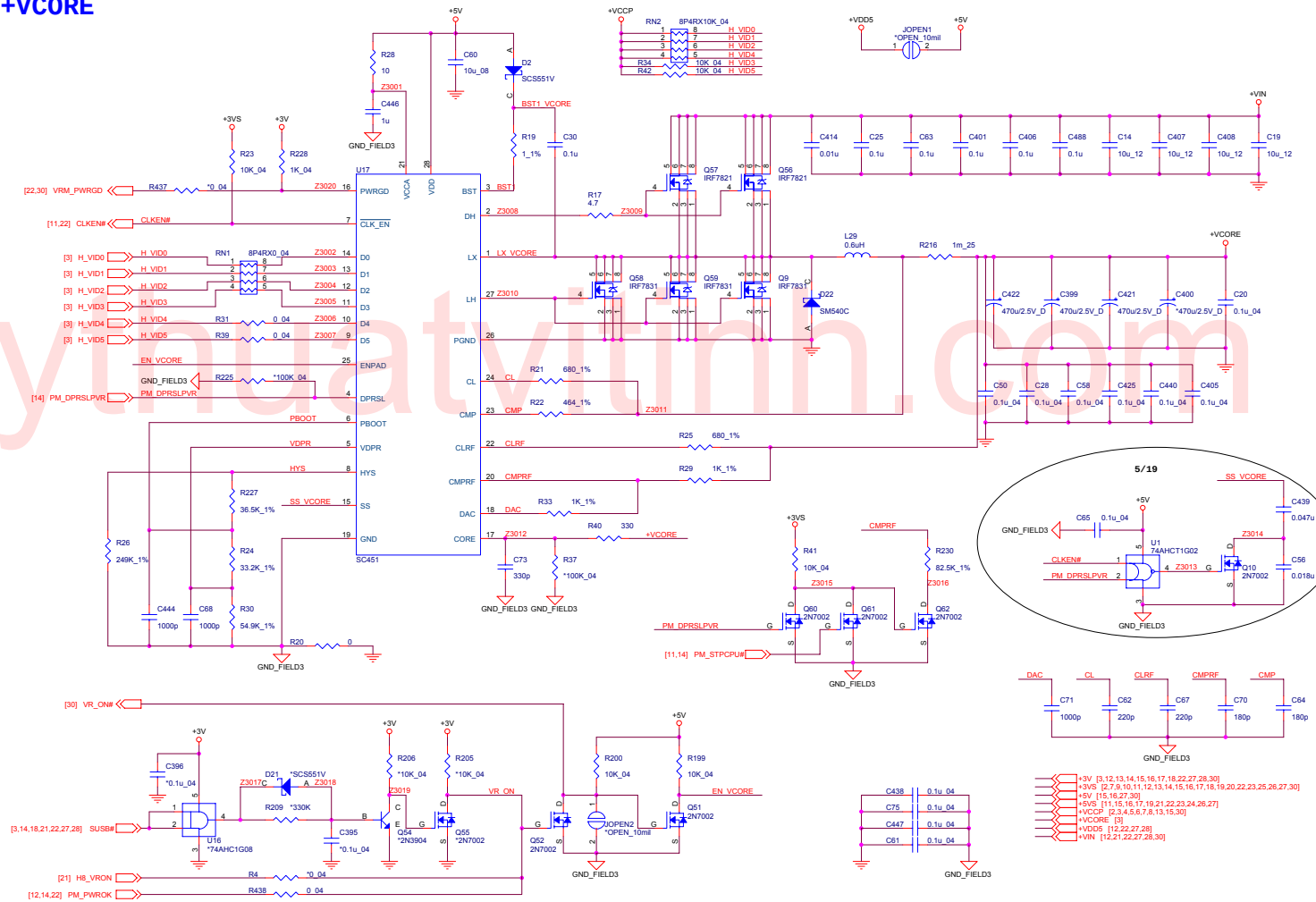


Schematic Diagrams

+VCORE

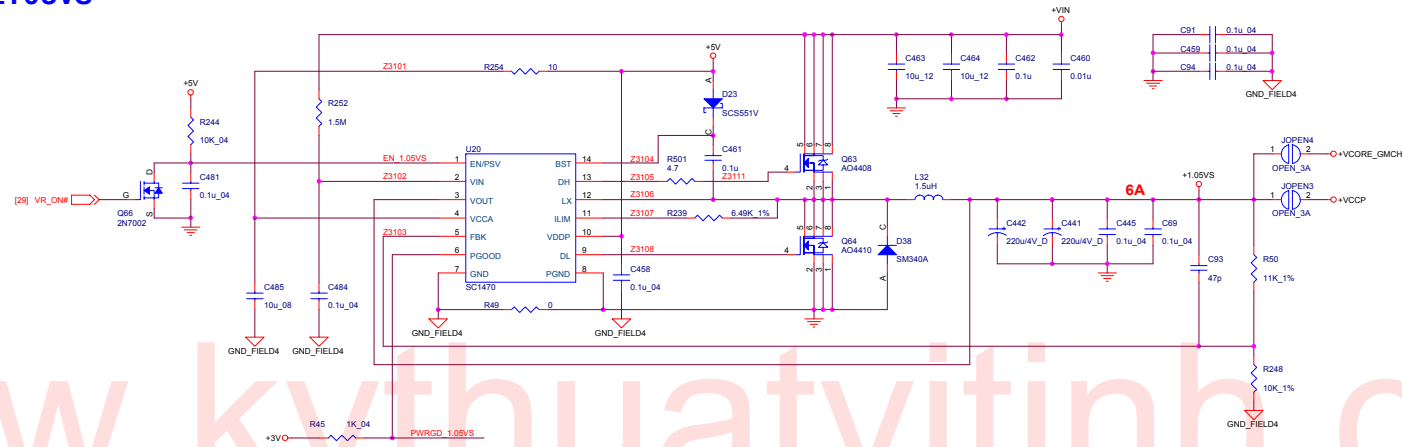
Sheet 29 of 40
+VCORE

+VCORE



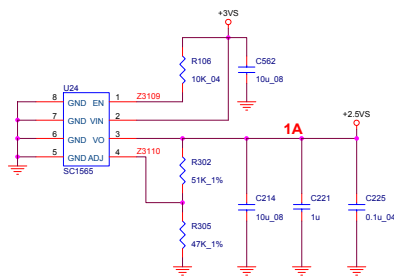
+1.05VS, +2.5VS

+1.05VS

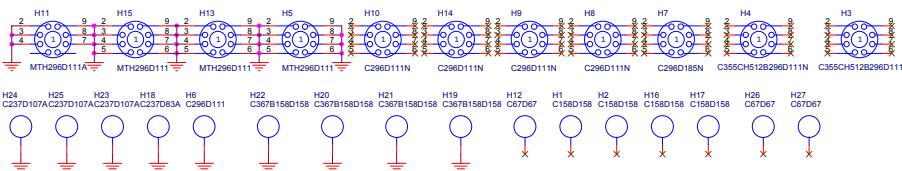
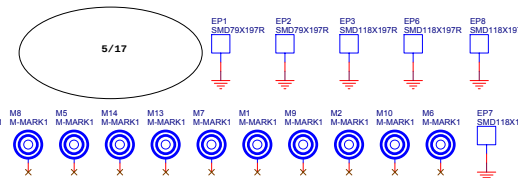


Sheet 30 of 40
+1.05VS, +2.5VS

+2.5VS

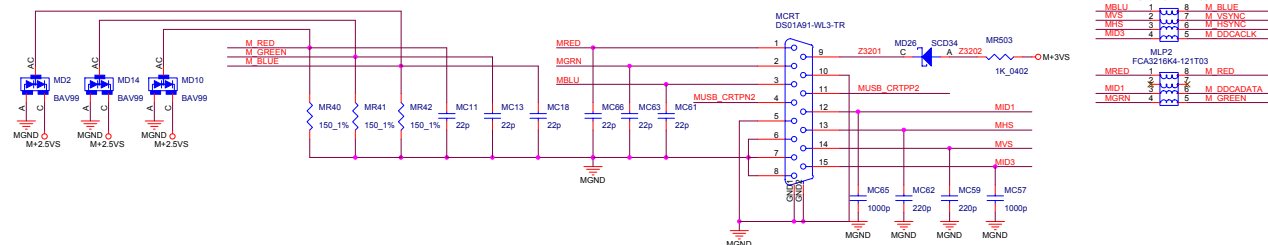


- +5V [5,7,12,15,22]
- +3V [3,12,13,14,15,16,17,18,22,27,28,29]
- +1.05VS [2,7,9,10,11,12,13,14,15,16,17,18,19,20,22,23,25,26,27,29]
- +5V [15,16,27,29]
- +VCCP [2,3,4,5,6,7,8,13,15,29]
- +VCCORE_GMCH [17,8]
- +VIN [12,21,22,27,28,29]

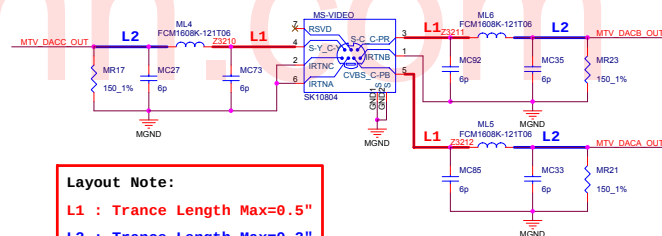
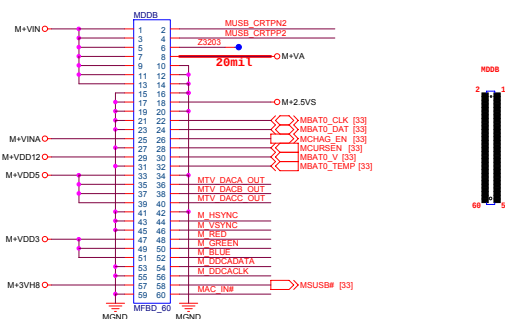
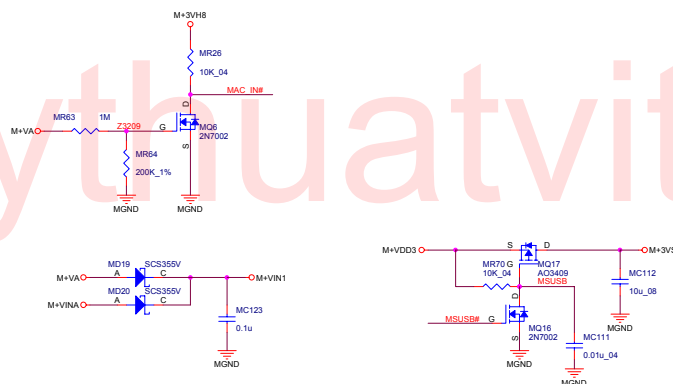


B.Schematic Diagrams

CRT



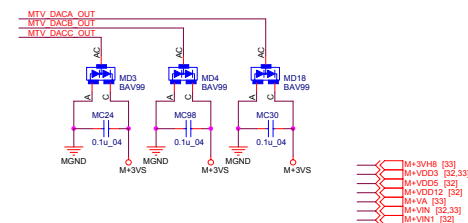
Sheet 31 of 40
D/D BD (CRT, S-
VIDEO, RJ-11)



Layout Note:

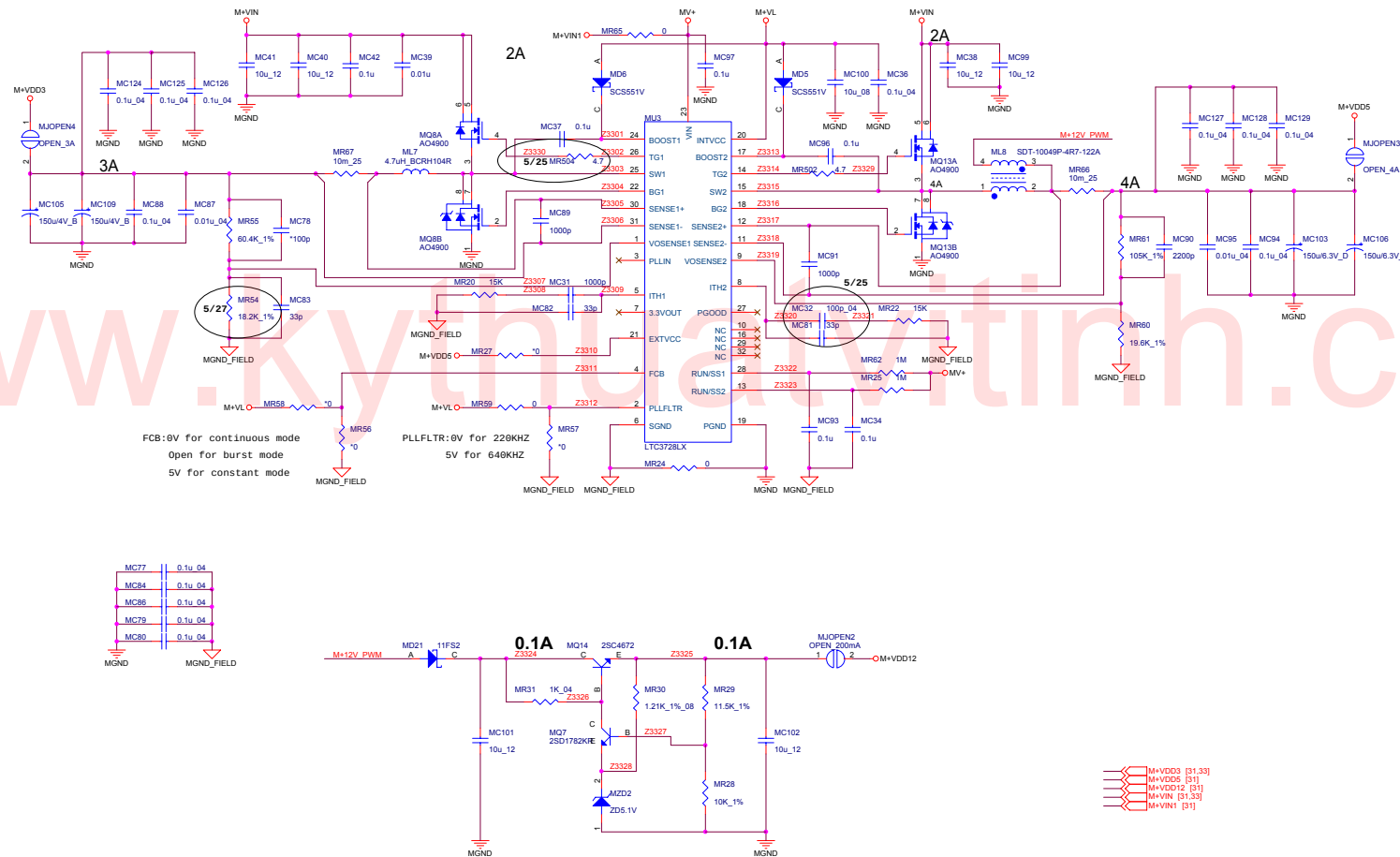
L1 : Trance Length Max=0.5"

L2 : Trance Length Max=0.2"



D/D BD (+VDD3, +VDD5, +VDD12)

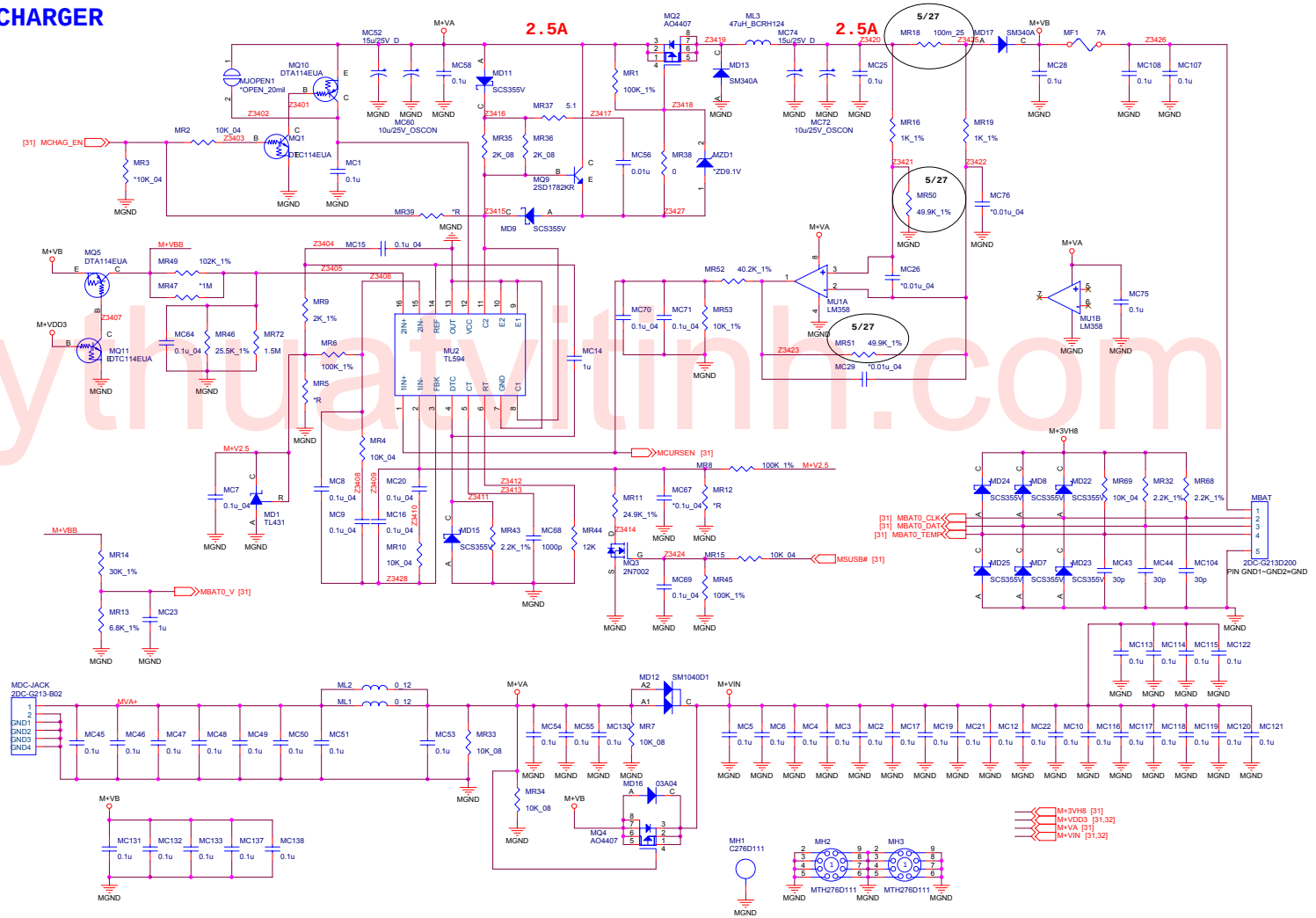
+VDD3, +VDD5, +VDD12



Sheet 32 of 40
D/D BD (+VDD3,
+VDD5, +VDD12)

D/D BD (CHARGER, DC IN)

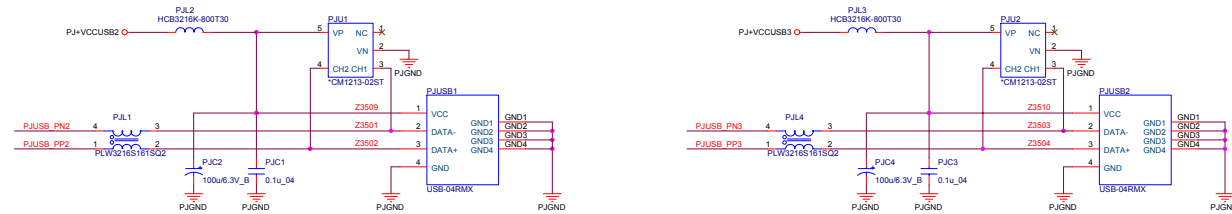
CHARGER



Sheet 33 of 40
D/D BD (CHARGER,
DC IN)

AUDIO BD (PHONE JACK, USB)

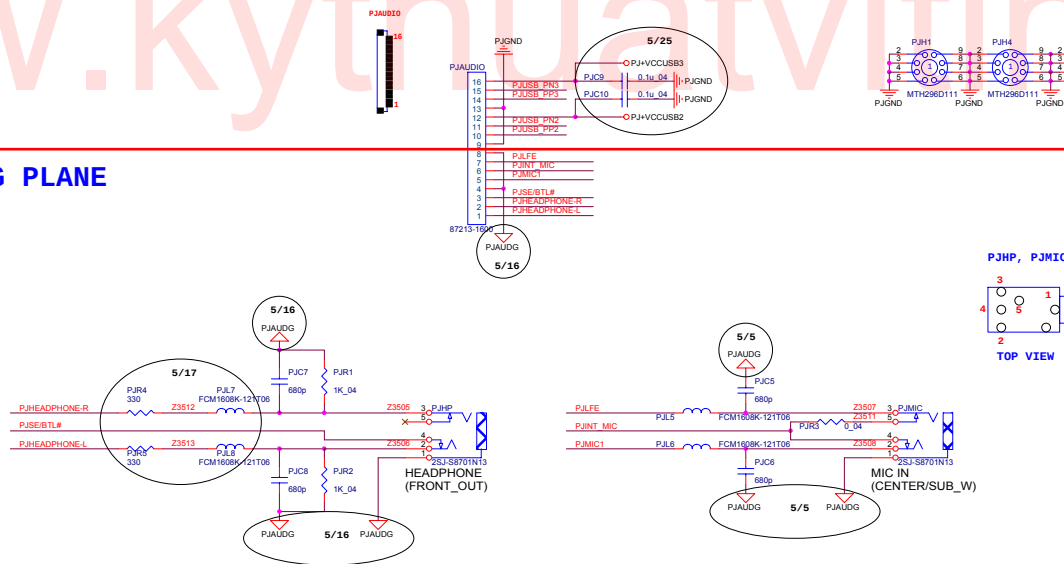
DIGITAL PLANE



Sheet 34 of 40
AUDIO BD (PHONE JACK, USB)

B.Schematic Diagrams

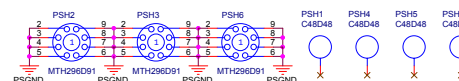
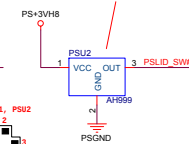
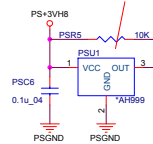
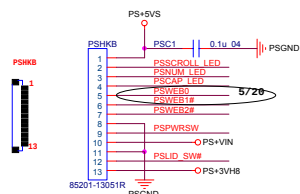
ANALOG PLANE



Sheet 35 of 40
HOT KEY BD (HOT
KEY, LED)



FOR M540G



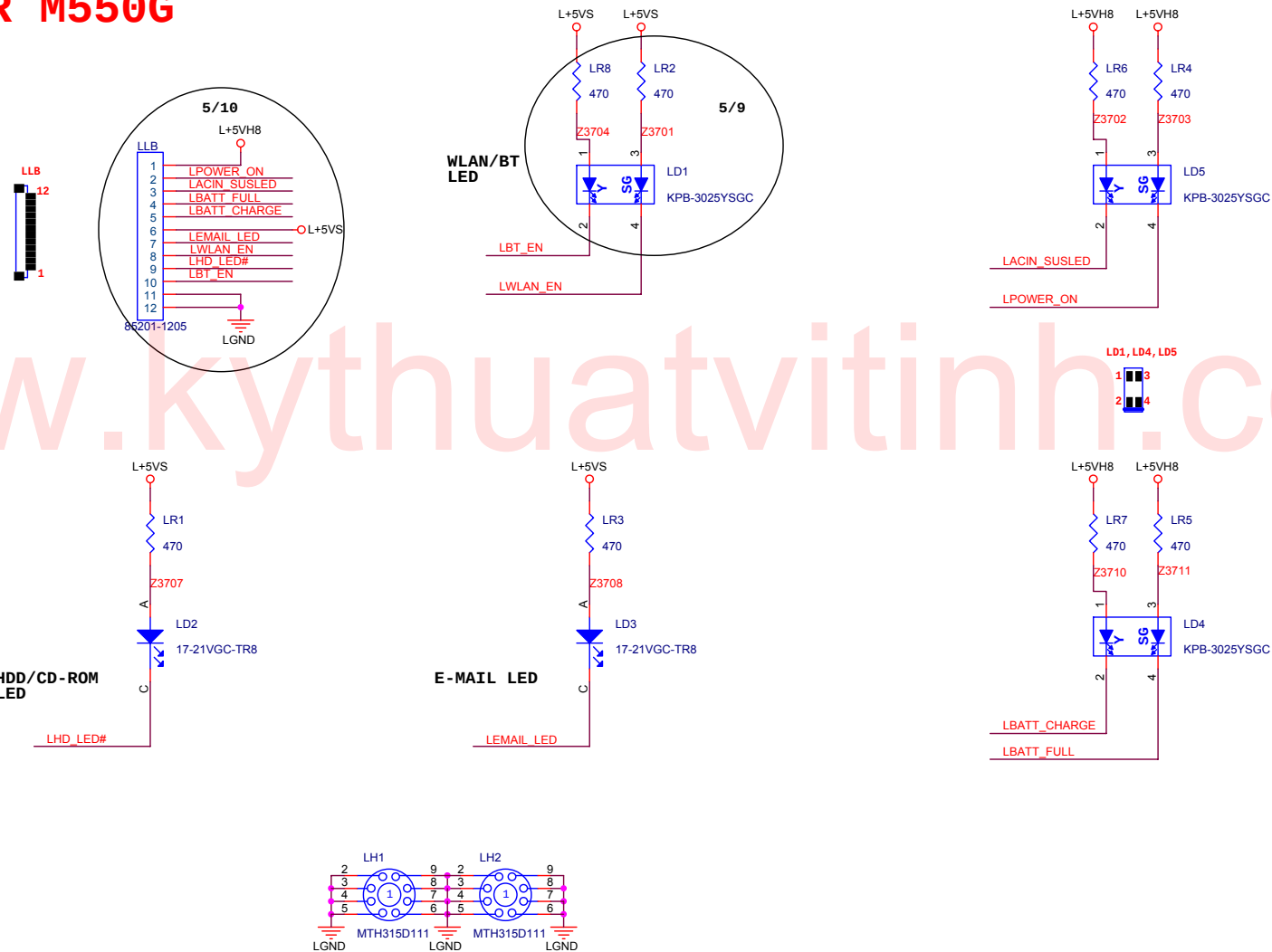
	LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8	MR SENSOR
M540G	X	X	X	V	V	V	X	V	PSU1
M550G	V	V	V	X	X	X	V	X	PSU2

	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
M540G	X	V	X	V	X	V	X	V
M550G	V	X	V	X	V	X	V	X

CLEVO CO. 藍天電腦	
Title	[35]HOT KEY BD(HOT KEY,LED)
Size A3	Document Number 71-M55GS-003
Date	3117 Tuesday, May 31, 2005
	Sheet 35 of 30

LED BOARD

FOR M550G

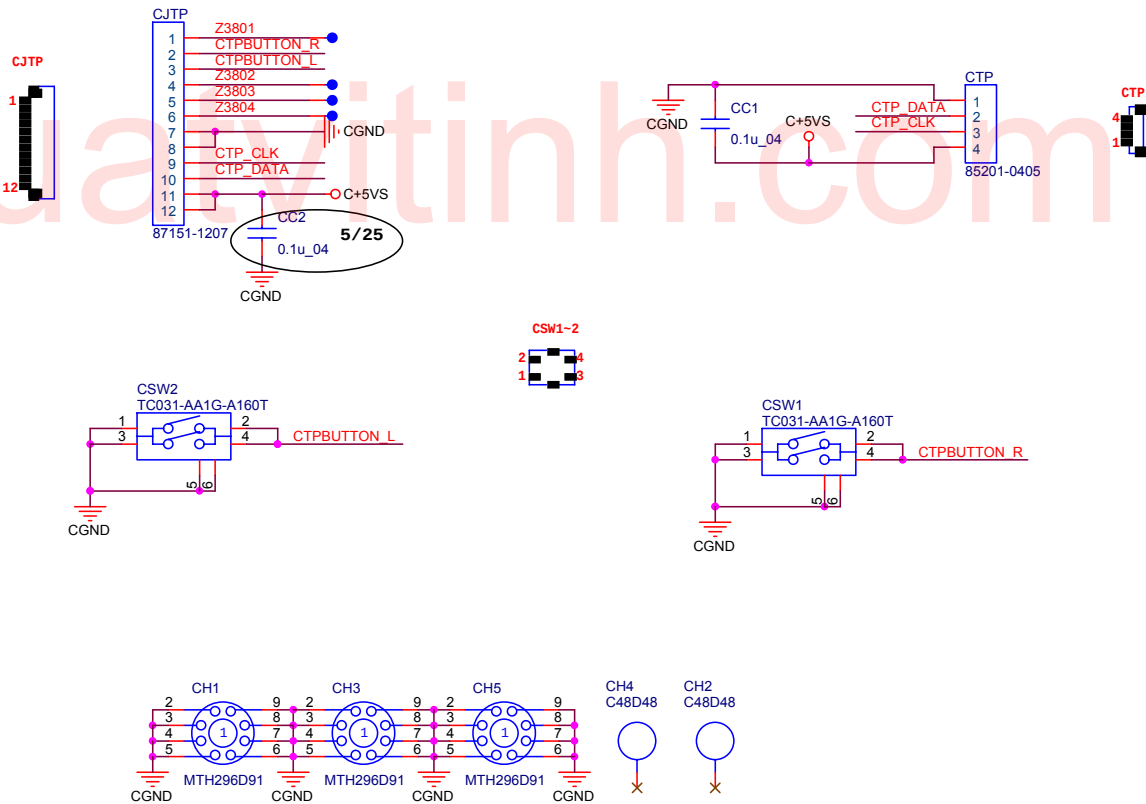


Sheet 36 of 40
LED BOARD

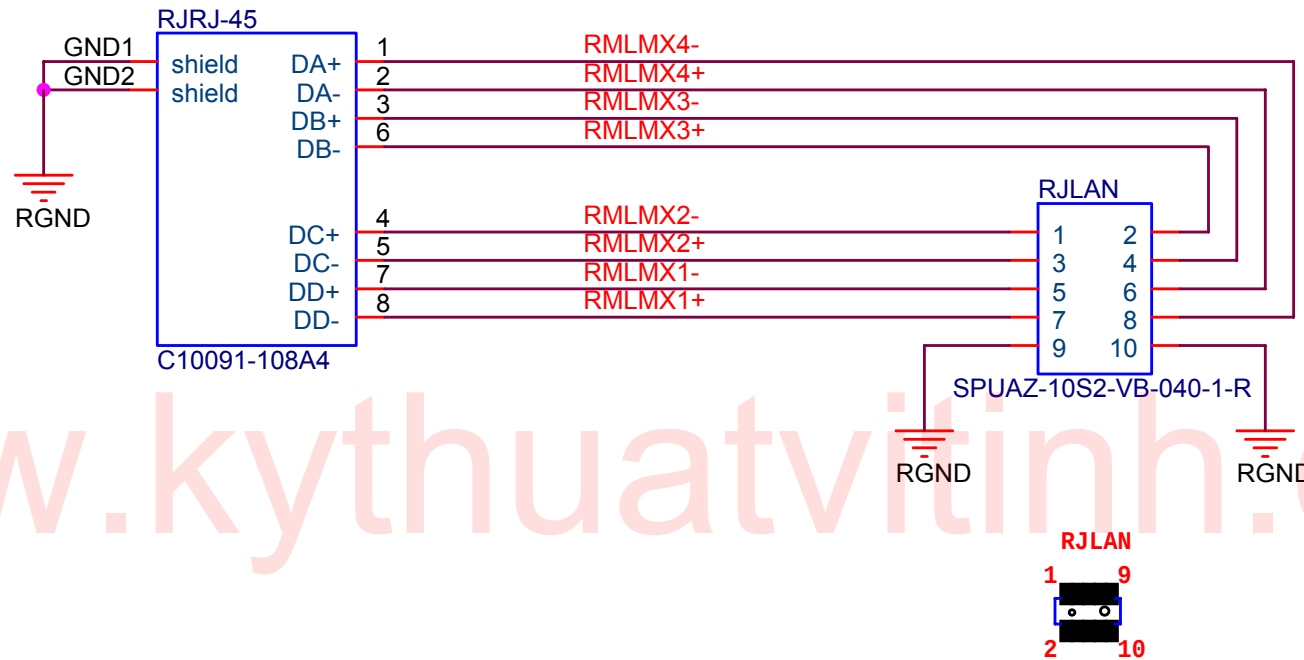
CLICK BOARD
FOR M550G

VENDOR	PART NUMBER
Synaptics	
E-LAN	800409-5102

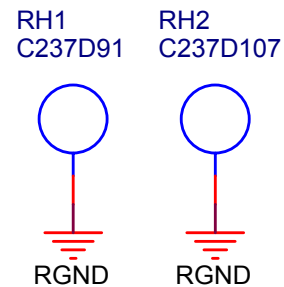
Sheet 37 of 40
CLICK BOARD



RJ-45 BOARD



Sheet 38 of 40
RJ-45 BOARD



USB DONGLE BOARD

