

CLEVO Tigerhill- Pineview System Block Diagram

AC-IN, CHARGER

SHEET 16

14.318 MHz

Colck Generator

SLG8SP510T

17.1mm*8.1mm*1.2mm
TSSOP 64PIN

SHEET 7

DDR2 One Channel

1GB & 2GB

Memory Termination

DDRII SO-DIMM0

SHEET 6

VDD3, VDD5

SHEET 18

3.3V, 5V, 3VS, 5VS

SHEET 17

1.05VS, 1.5VS

SHEET 20

1.8V, 0.9VS(VTT_MEM)

SHEET 19

VCORE

SHEET 21

Intel
Pineview 45nm

C0/C1/C2/C3/C4

PROCESSOR

FCBGA 559 pin

22mm*22mm*2.35mm

SHEET 2, 3, 4, 5

667MT/s

X2-GEN1

10 Gbits/s

DMI

<=8"

SOUTH BRIDGE

Tiger Point

360 MMAP

17mm*17mm*1.06mm

SHEET 8, 9, 10, 11

SYSTEM SMBUS

0.1"~13

AZALIA LINK

24 MHz

PCIE 100 MHz

<12"

CLICK BOARD
TOUCH PAD
SHEET 15

32.768 KHz

EC

ITE 8502E

128pins LQFP

14*14*1.6mm

SHEET 15

INT. K/B

SHEET 15

LPC ROM

SHEET 15

EC SMBUS

THERMAL SENSOR

EMC1402

SHEET 2

SMART FAN

SHEET 12

SMART BATTERY

SHEET 16

SATA I/II 3.0Gb/s

<12"

USB2.0 480 Mbps

1"~16"

SATA HDD

SHEET 13

(USB2)
Port_2

SHEET 13

(USB7)
CCD

SHEET 24

USB0
Port_0

SHEET 24

USB1
Port_1

SHEET 24

Mini Card

WLAN

Bluetooth(USB5)

SHEET 13

JMC251/ JMC261

LAN

CARD READER

SHEET 23

RJ-45

SHEET 23

Card Reader

Socket

SHEET 23

SHEET 14
MIC IN
HP OUT

Azalia Codec

RealTek

ALC272

48pins QFN

9*9*1.6mm

SHEET 14

INT SPK R

SHEET 14

INT SPK L

SHEET 14

INT MIC

SHEET 14

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Title			
[01]BLOCK DIAGRAM			
Size	Document Number	Rev	
A3	6-7P-M1104-001	6-71-M1100-D01	
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(1)
LVDS Clock & Data Signal Group
Zdiff = 90 Ohm ±10%
signal / space : 4 / 5 mils
length < 7850 mils

(1)

(2)
LVDS Control Signal Group
LBKLT_CTL, LBKLT_EN, LVDD_EN
Zo = 50 Ohm ±10%
signal : 5 mils
length < 6000 mils

PINE_VIEW_M

CPU

4 OF 6

Thermal IC

LAYOUT NOTE:

Place near GTLREF's pin
Zo = 50 Ohm ±15%
Signal : 5 mils
length < 500 mils

LAYOUT NOTE:

GTLREF MAX trace length of
500 mils and 5 mils spacing

PROCHOT# must be terminated with a 56-Ω,
pull-up resistor to VCCP even if it is not used.

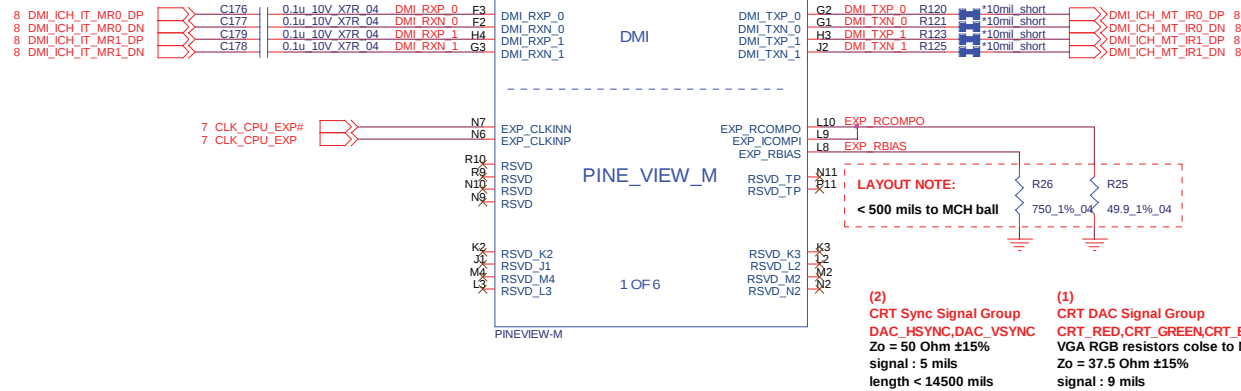
8,10,11,12,13,15,17,19 3.3V
3,5,6,7,8,9,10,11,12,13,14,15,17,20,21 3.3VS
5,7,9,10,11,20 1.05VS

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Title			
[02]PINEVIEW CPU 1/4			
Size	Document Number	Rev	
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DMI Signal Group

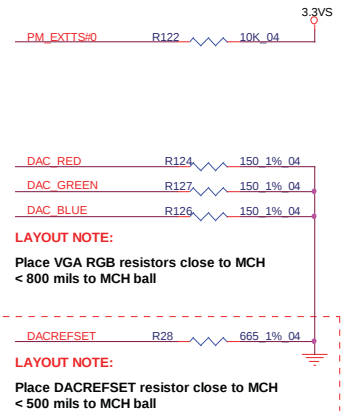
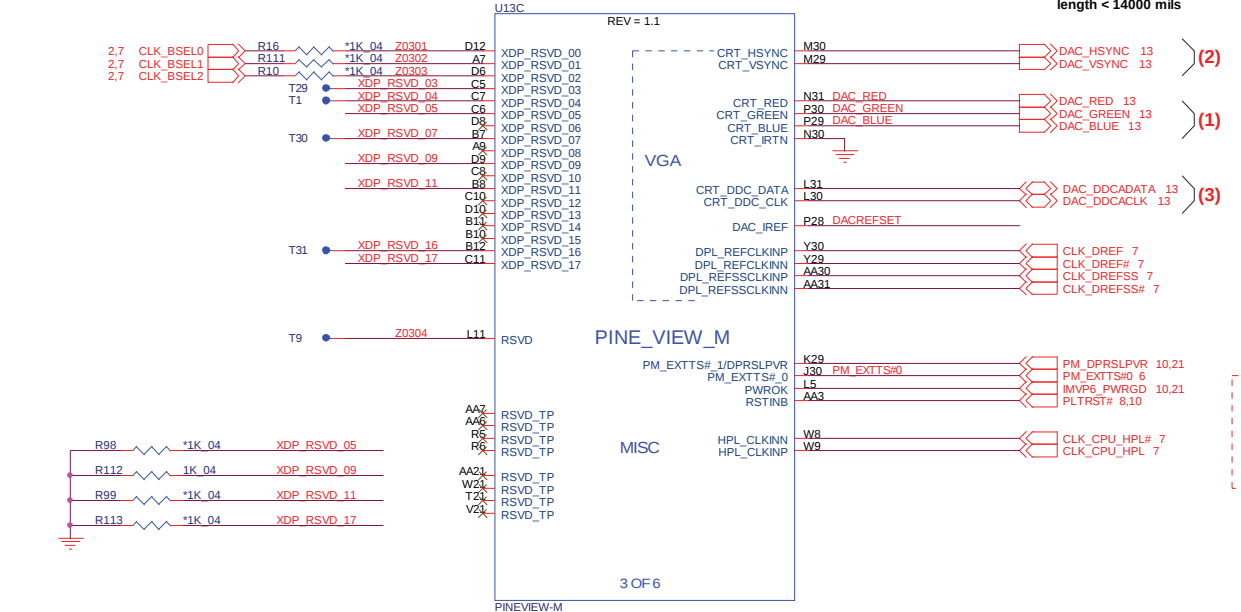
Zdiff = 85 Ohm ±10%
signal / space : 6 / 6 mils
length < 6400 mils



(2) CRT Sync Signal Group
DAC_HSYNC, DAC_VSYNC
Zo = 50 Ohm ±15%
signal : 5 mils
length < 14500 mils

(1) CRT DAC Signal Group
CRT_RED, CRT_GREEN, CRT_BLUE
VGA RGB resistors close to MCH ball
Zo = 37.5 Ohm ±15%
signal : 9 mils
length < 800 mils
Two VGA RGB resistors between
Zo = 50 Ohm ±15%
signal : 5 mils
length < 14000 mils

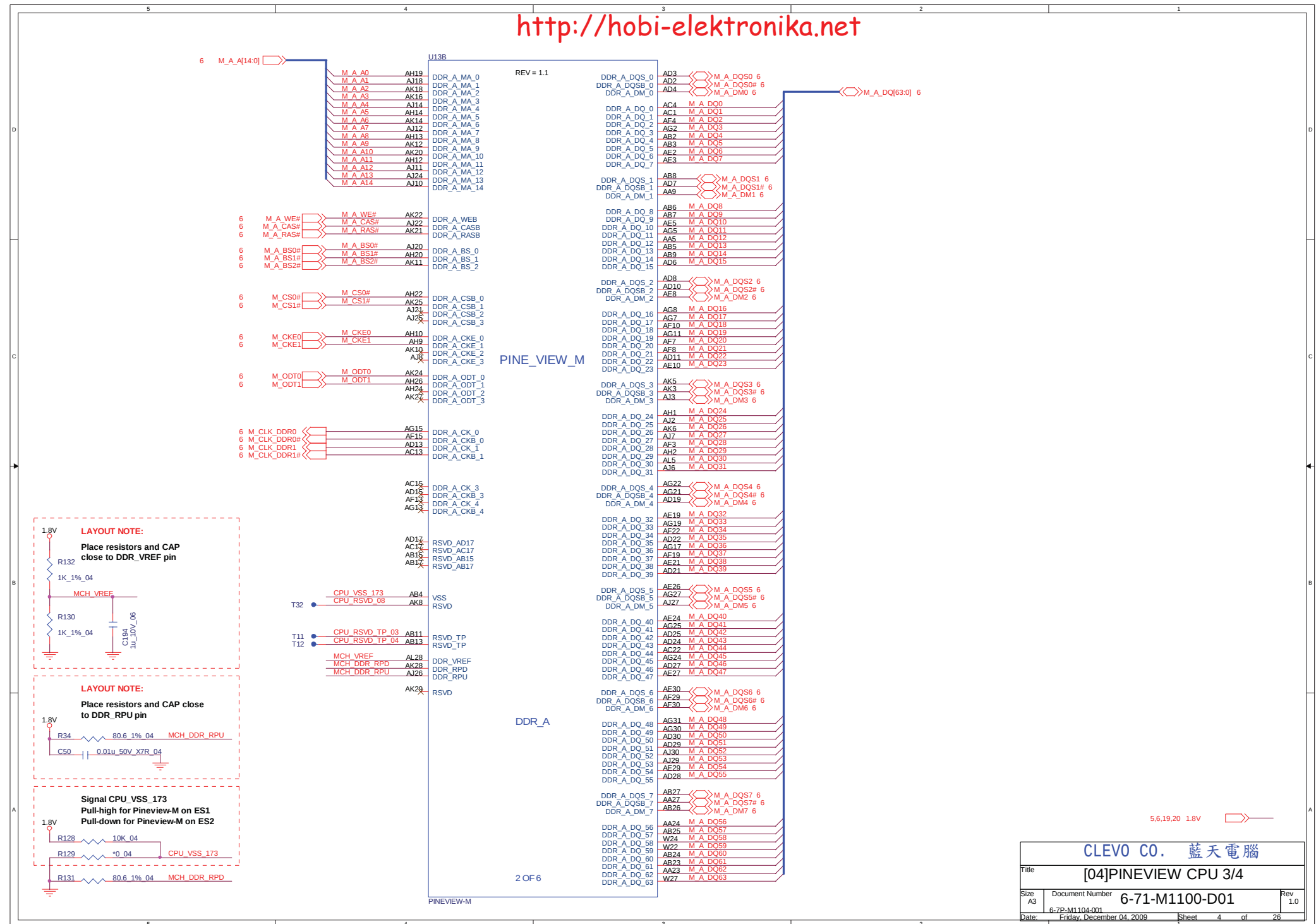
(3) CRT Control Signal Group
CRT_DDC_CLK, CRT_DDC_DATA
Zo = 50 Ohm ±15%
signal : 5 mils
length < 15100 mils

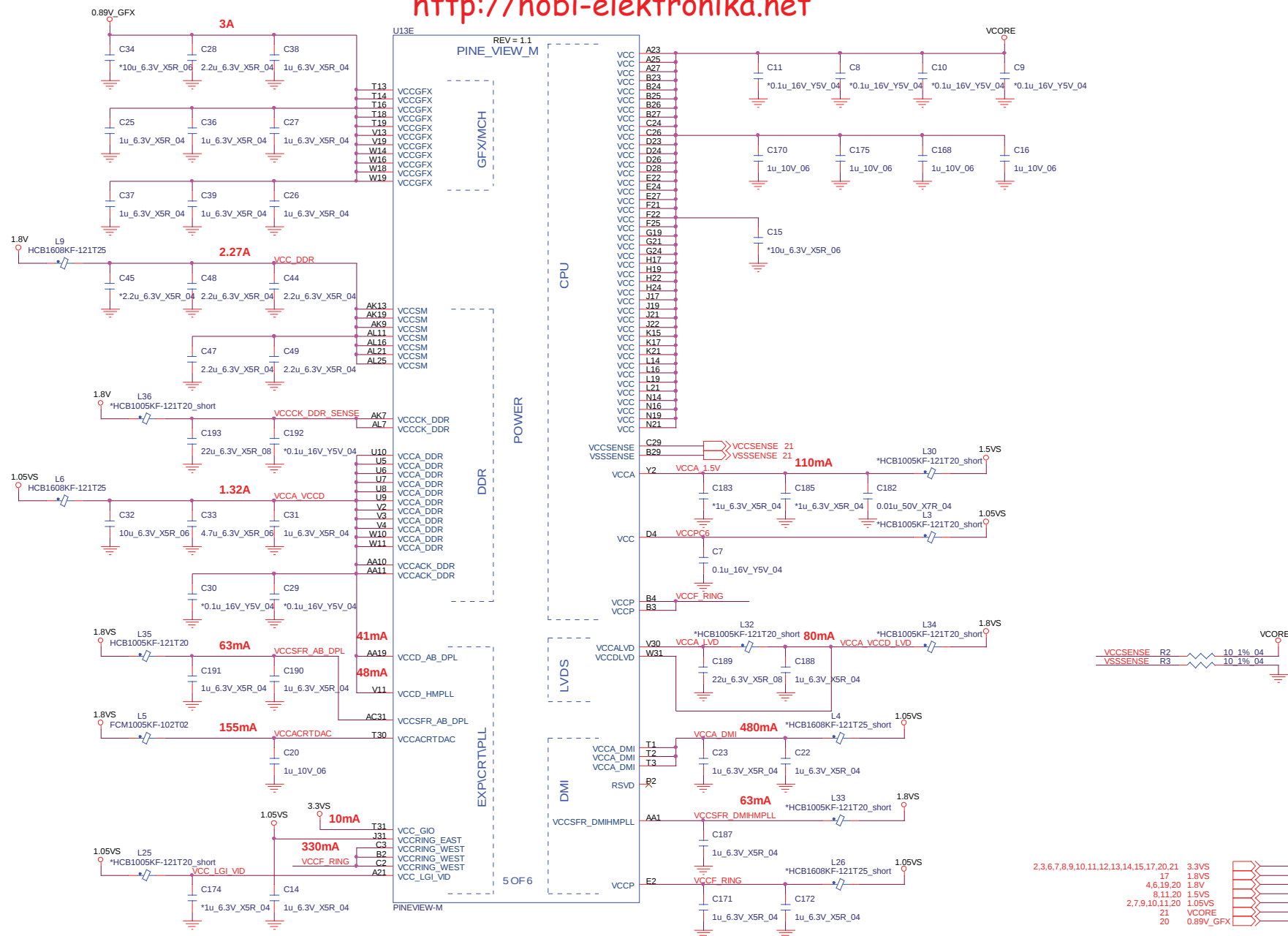


2,5,6,7,8,9,10,11,12,13,14,15,17,20,21 3.3VS

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Title			[03]PINEVIEW CPU 2/4	
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A3	6-71-M1100-001	6-71-M1100-D01		
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Title			
[05]PINEVIEW CPU 4/4			
Size	Document Number	Rev	
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SO-DIMM 0

<http://hobi-elektronika.net>

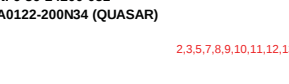
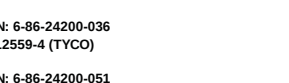
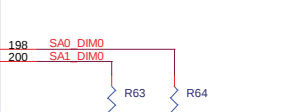
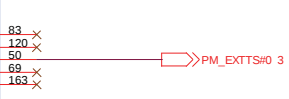
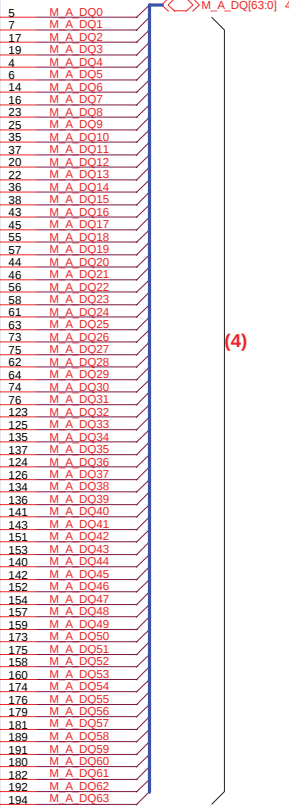
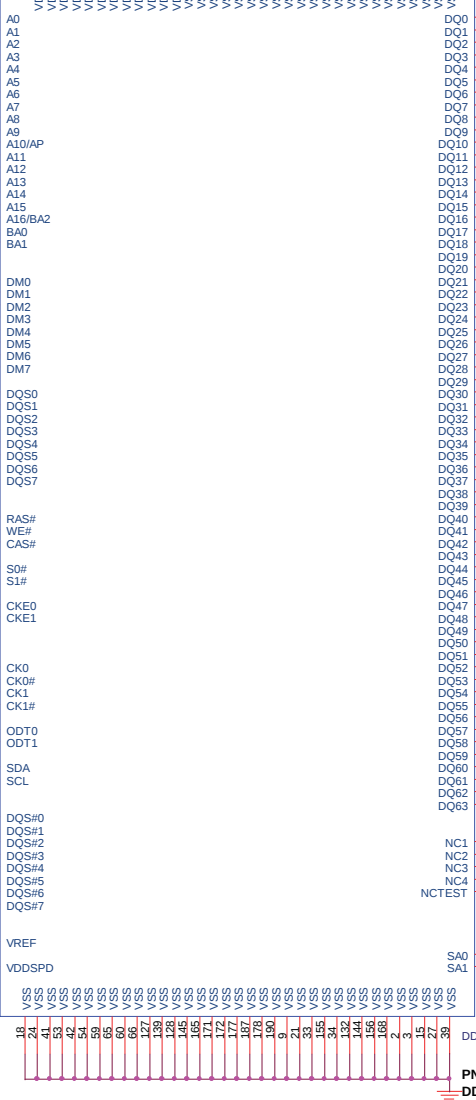
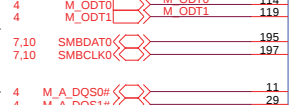
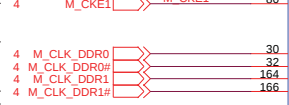
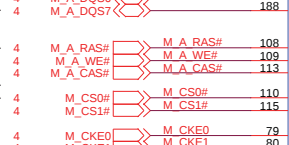
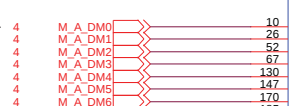
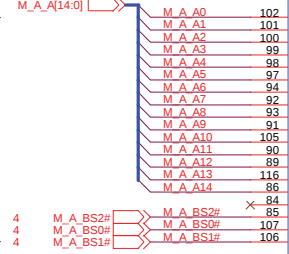
(3)
DDR2 Command Signal Group
MA[14:0], BS[2:0],
RAS#, CAS#, WE#
Zo = 37 Ohm ±10%
signal : 9.5 mils
length < 3500 mils

(4)
DDR2 Data Signal Group
DQ[63:0], DM[7:0]
Zo = 37 Ohm ±10%
signal : 9.5 mils
length < 4000 mils

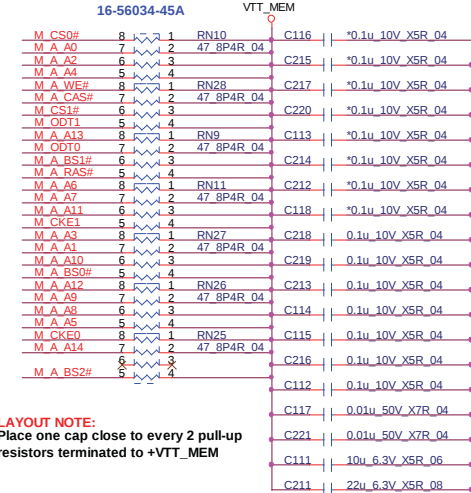
(5)
DDR2 Data Strobes Signal Group
DQS[7:0], DQS[7:0]#
Zdiff = 85 Ohm ±10%
signal / space : 5 / 5.5 mils
length < 4000 mils

(1)
DDR2 Clocks Signal Group
CK[1:0], CK# [1:0]
Zdiff = 65 Ohm ±12%
signal / space : 9 / 5 mils
length < 4000 mils

(2)
DDR2 Control Signal Group
CS#[1:0], CKE[1:0], ODT[1:0]
Zo = 37 Ohm ±10%
signal : 9.5 mils
length < 3500 mils



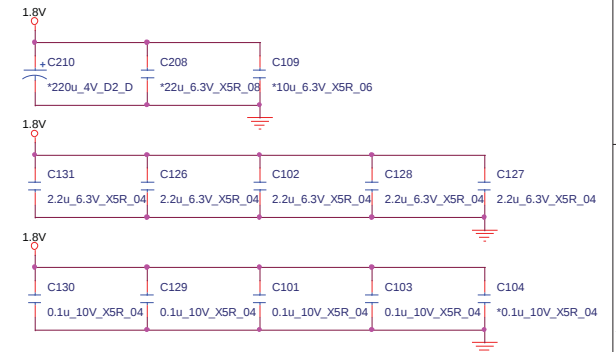
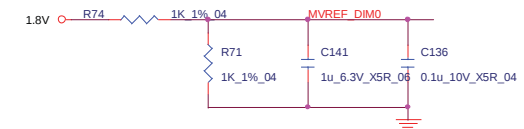
+VTT_MEM RESISTORS



LAYOUT NOTE:
Place one cap close to every 2 pull-up
resistors terminated to +VTT_MEM

LAYOUT NOTE:

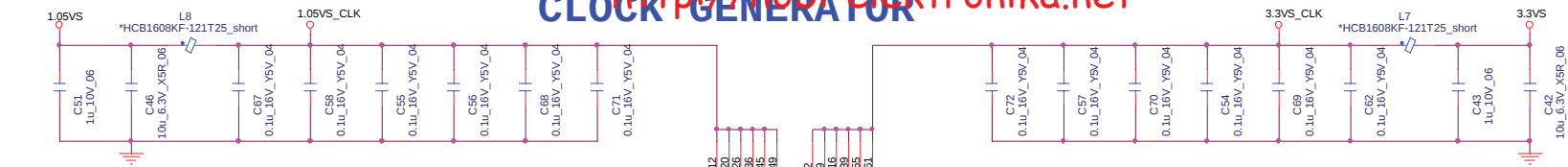
Place resistors and CAP close to SO-DIMM_0



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[06]DDR2 SO-DIMM_0

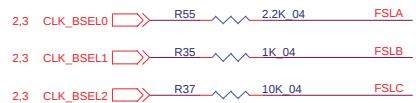
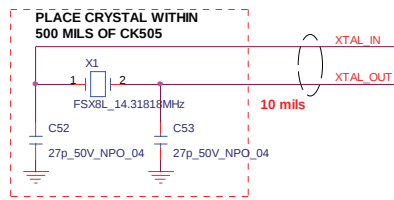
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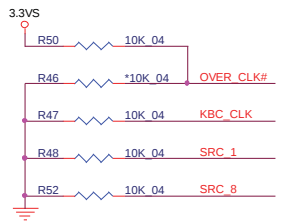
Zo = 55 Ohm ±15%
signal : 4 mils

Zo = 50 Ohm ±15%
signal : 5 mils

Zdiff = 92 Ohm ±10%
signal / space : 4 / 5.5 mils



FSLC BSEL2	FSLB BSEL1	FSLA BSEL0	Host Clock Frequency
---	---	---	CPU_SEL
0	1	1	166 MHz



PN: 6-02-08510-EL0
SLG8SP510T

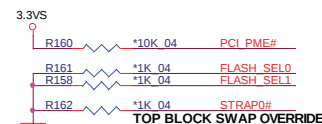
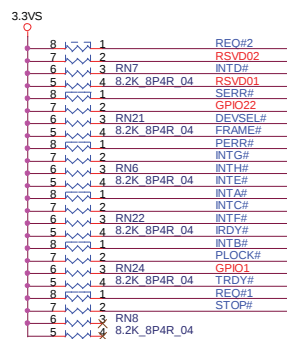
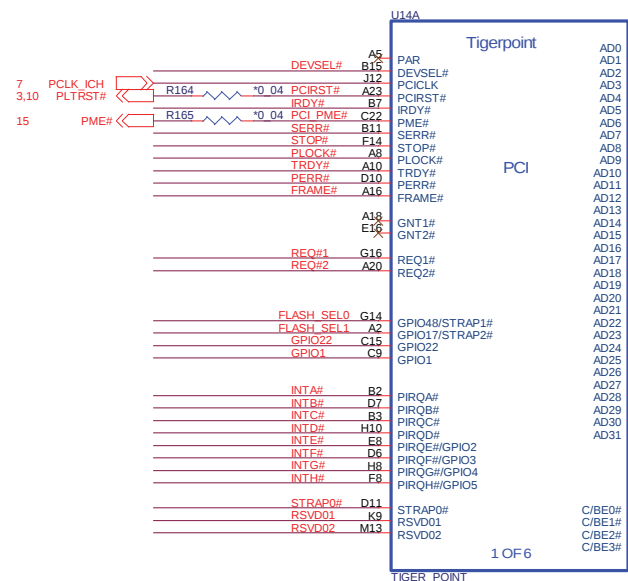
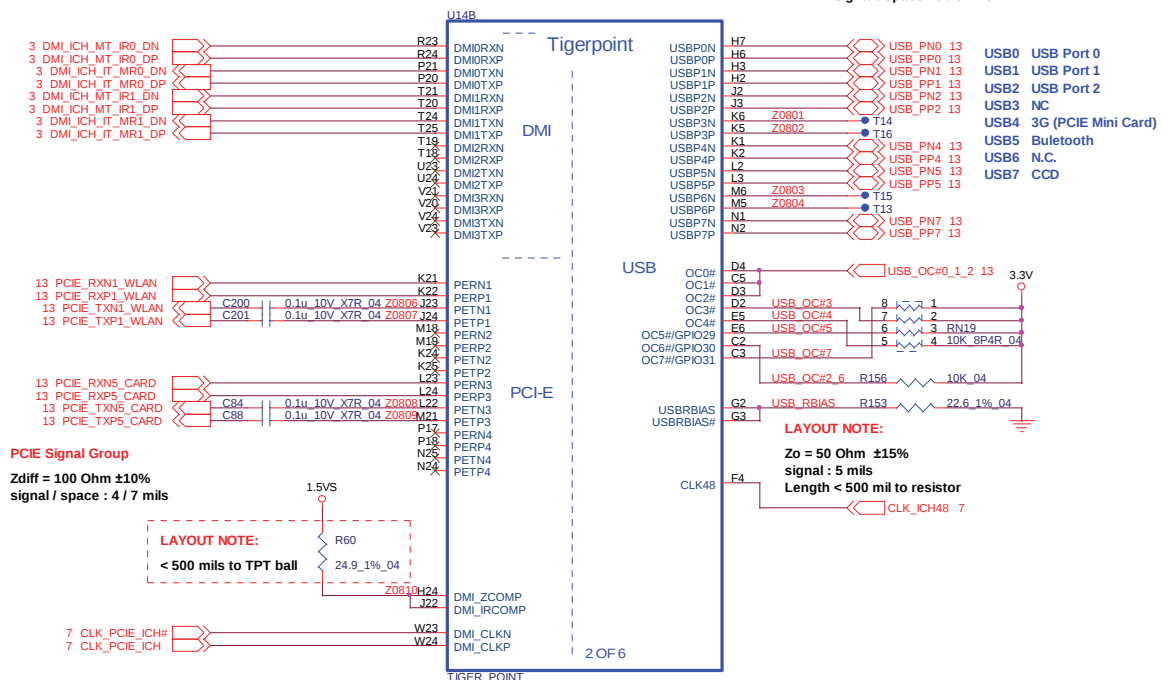
PN: 6-02-87560-EL0
RTM875T-606-VD-GRT

2,3,5,6,8,9,10,11,12,13,14,15,17,20,21 3.3VS
2,5,9,10,11,20 1.05VS

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Title [07]CLOCK GENERATOR			
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USB Signal Group

Zdiff = 90 Ohm ±15%
signal / space : 5 / 6 mils

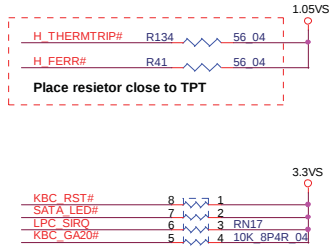


FLASH_SEL1 GPIO17/STRAP2#	FLASH_SEL0 GPIO48/STRAP1#	MODE
0	1	SPI
1	0	PCI
1	1	LPC

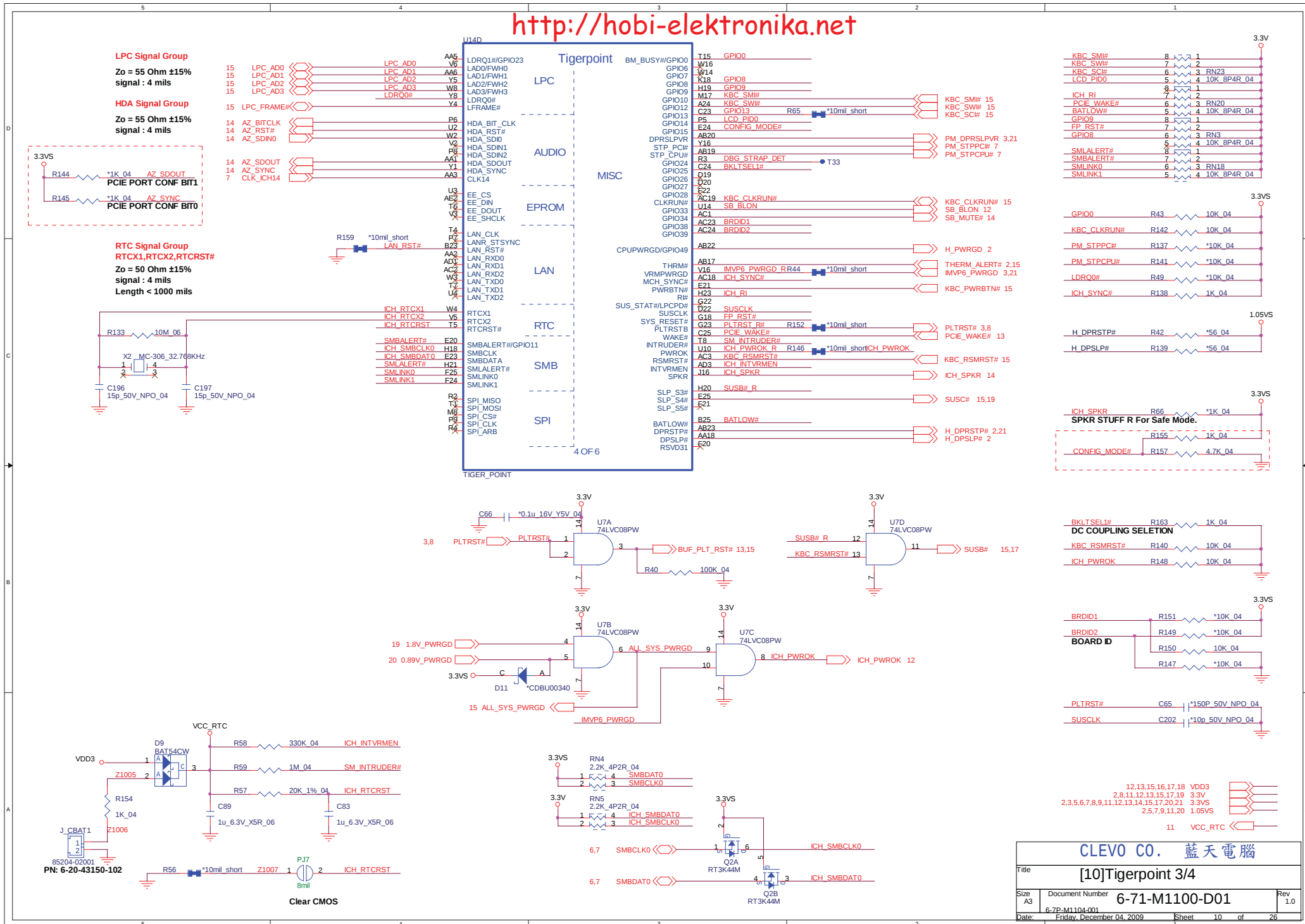
2,10,11,12,13,15,17,19 3.3V
2,3,5,6,7,9,10,11,12,13,14,15,17,20,21 3.3V
5,11,20 1.5V

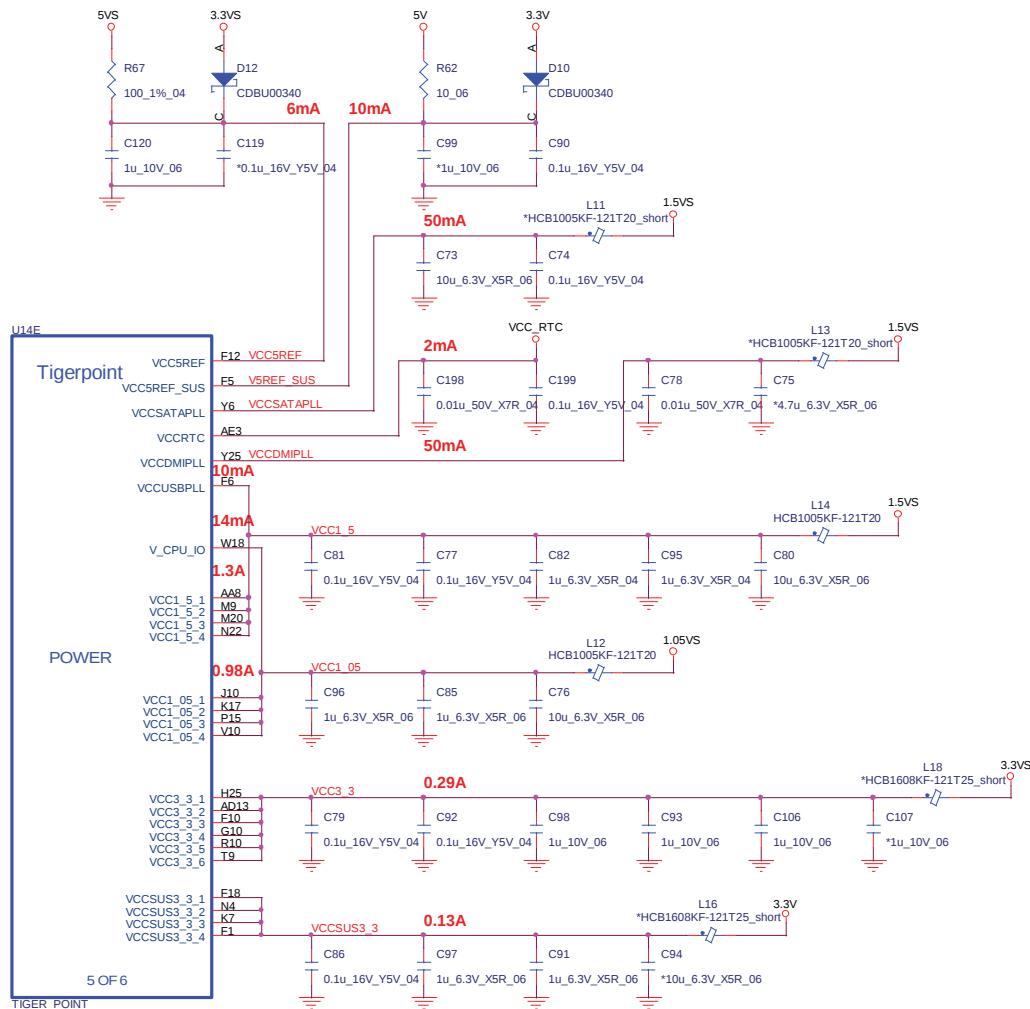
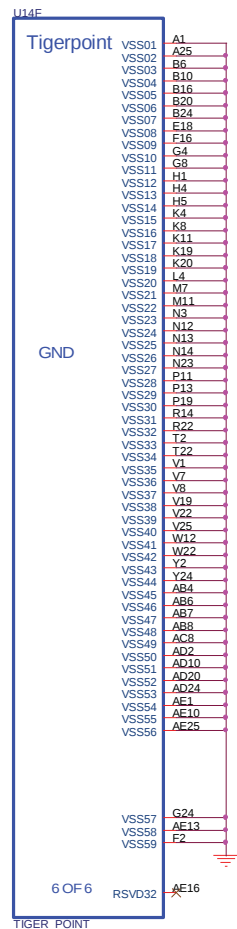
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Title [08]Tigerpoint 1/4		
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Title [09]Tigerpoint 2/4			
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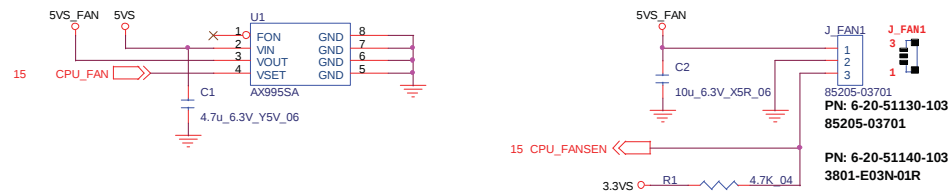
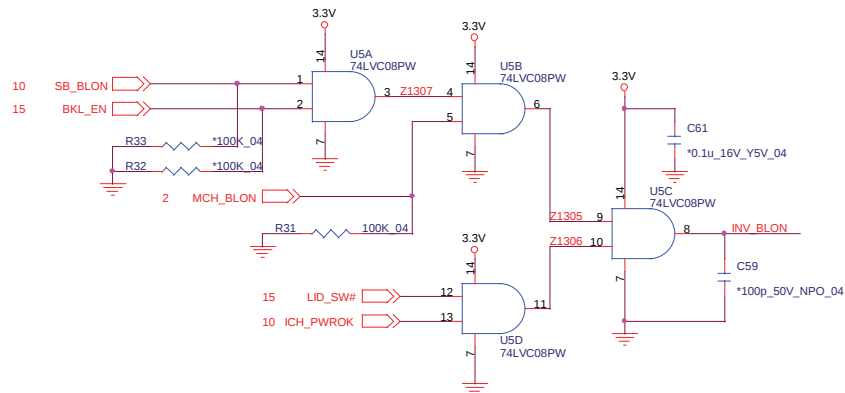


13,17,18,19,20,21 5V
12,13,14,15,17 5V
2,8,10,12,13,15,17,19 3.3V
2,3,5,6,7,8,9,10,12,13,14,15,17,20,21 3.3V
5,8,20 1.5V
2,5,7,9,10,20 1.05V
10 VCC_RTC

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Title [11]Tigerpoint 4/4		
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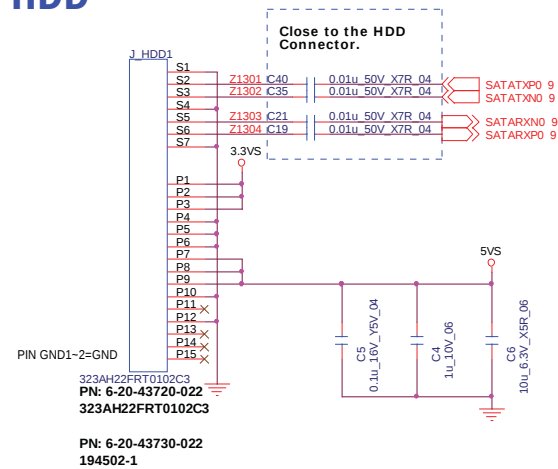
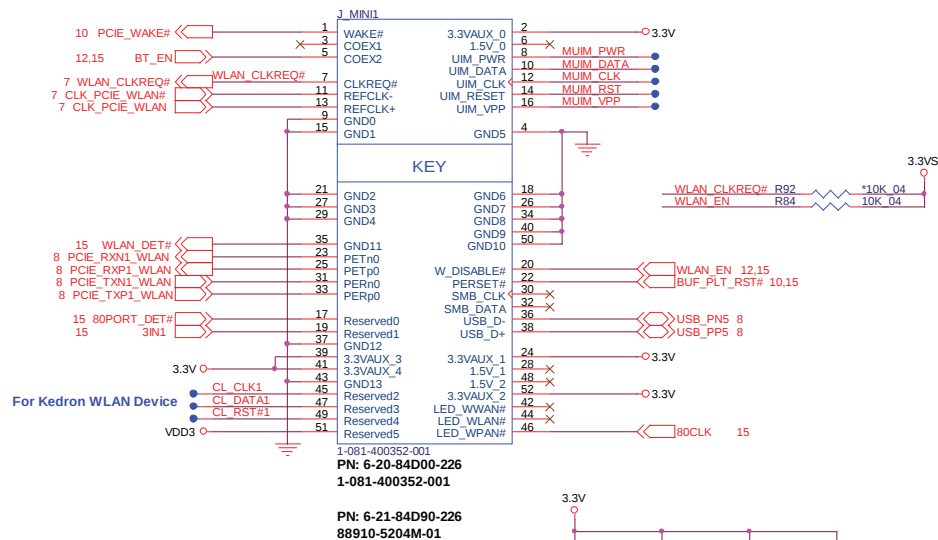


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Title [12]PANEL,LED,FAN			
Size A3	Document Number 6-7P-M1104-001	6-71-M1100-D01	Rev 1.0
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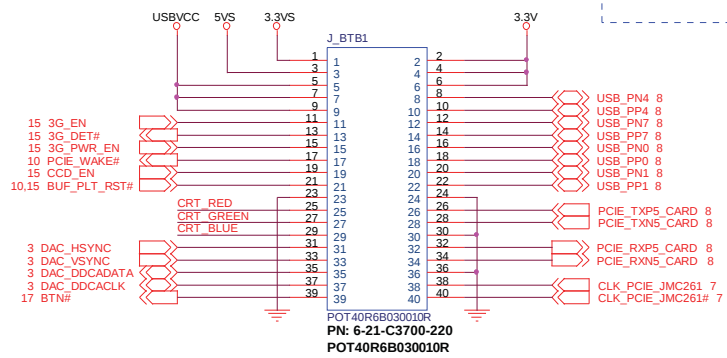
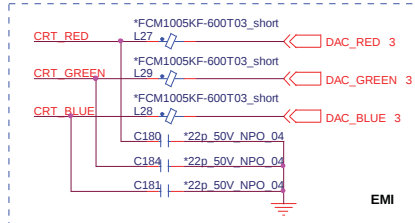
MINI-PCIE CARD AND Debug Port

<http://hobi-elektronika.net>

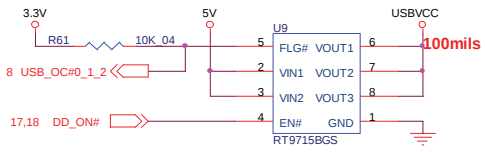
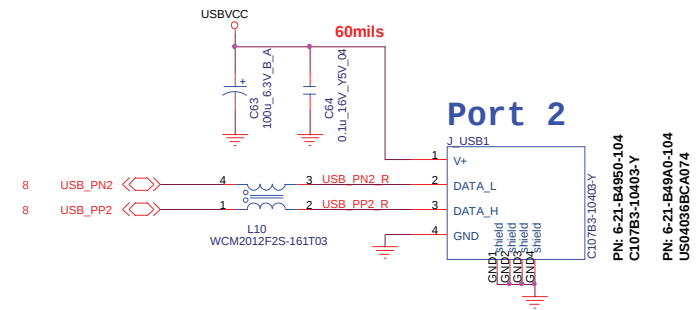
SATA HDD



CONN. FOR CONT TO CR/B

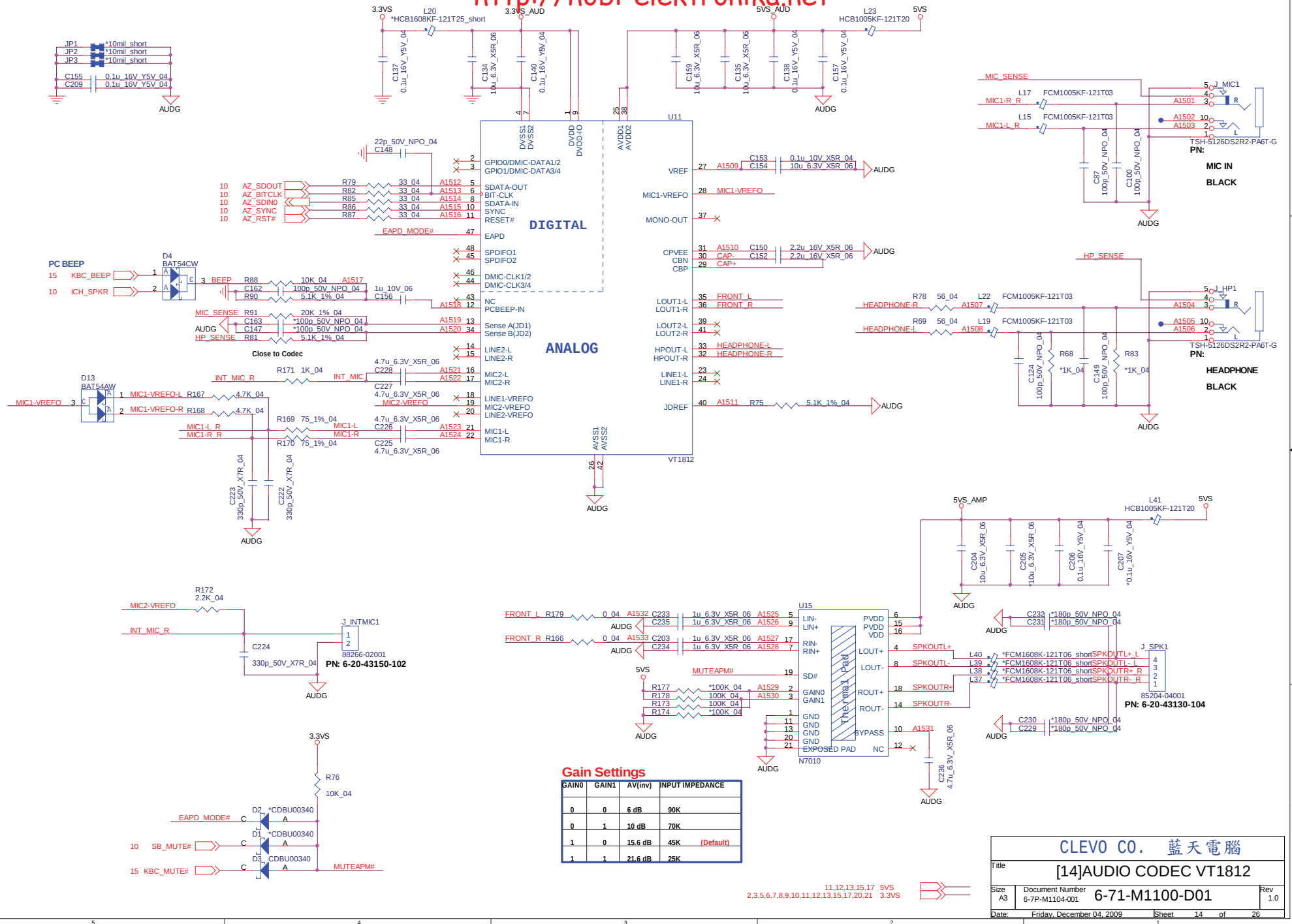


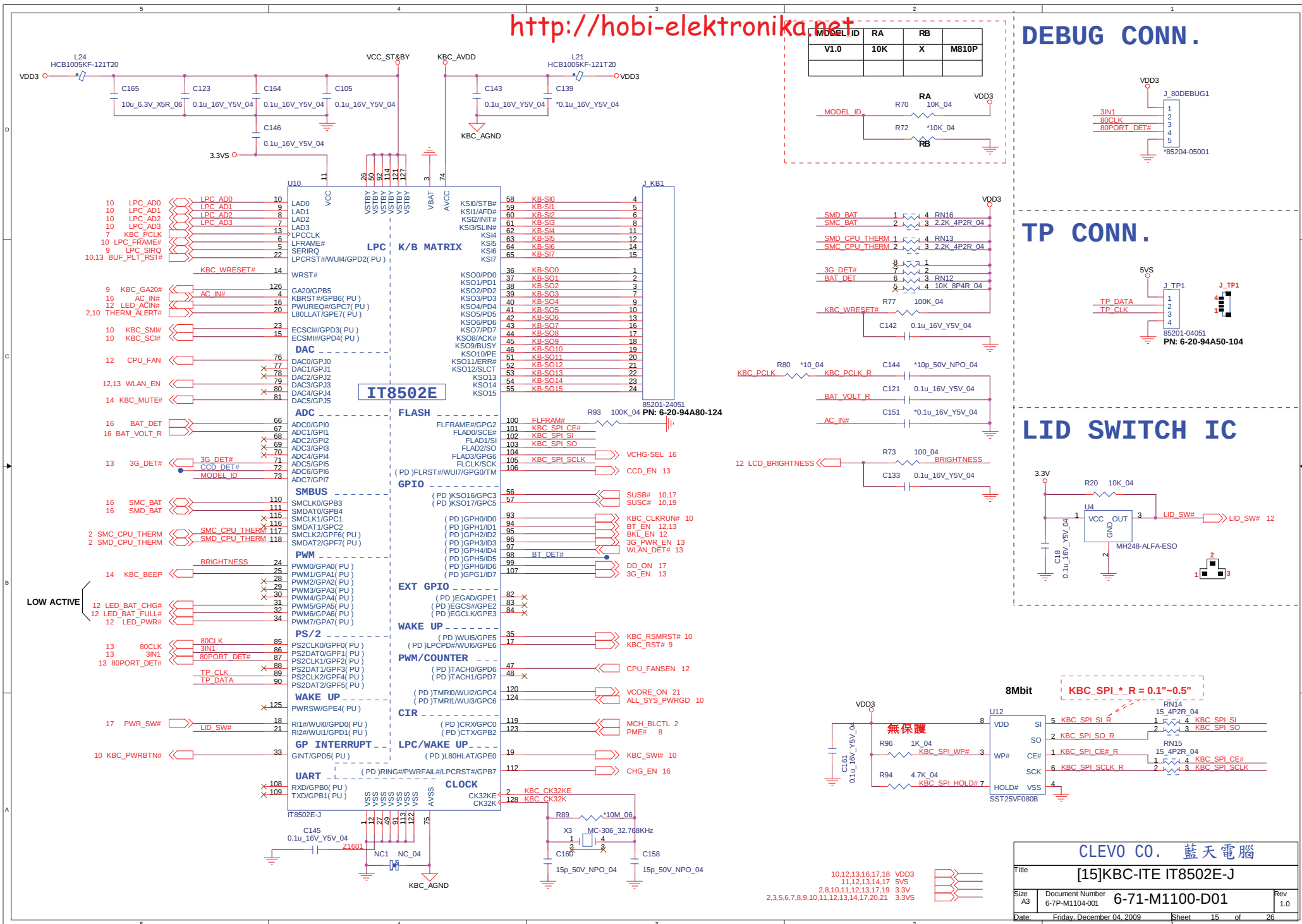
USB PORT_2

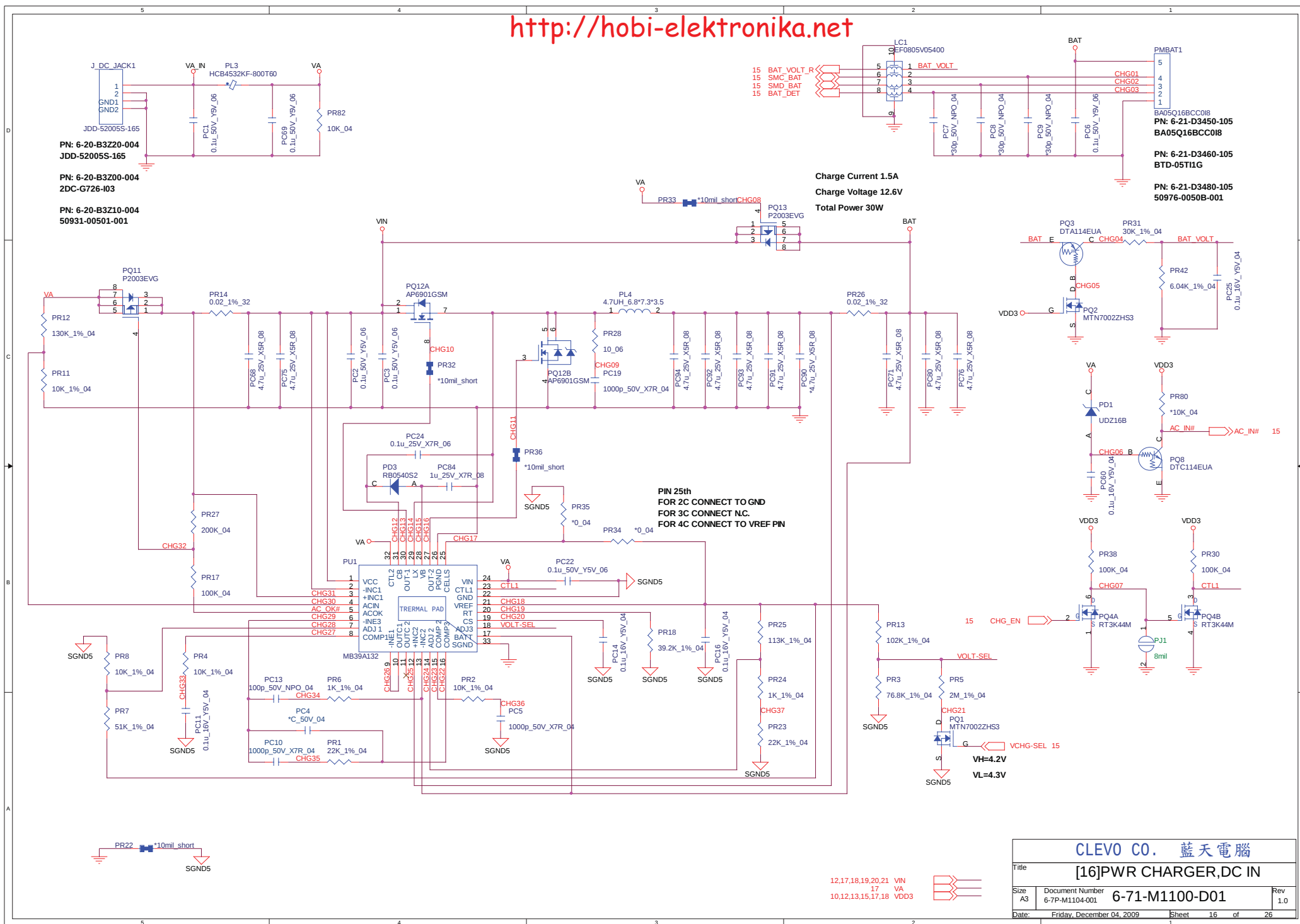


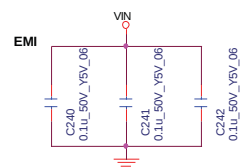
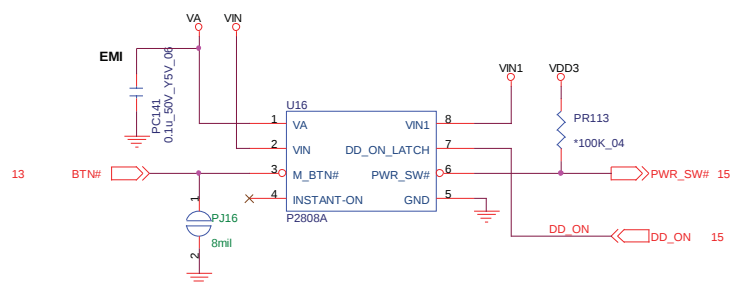
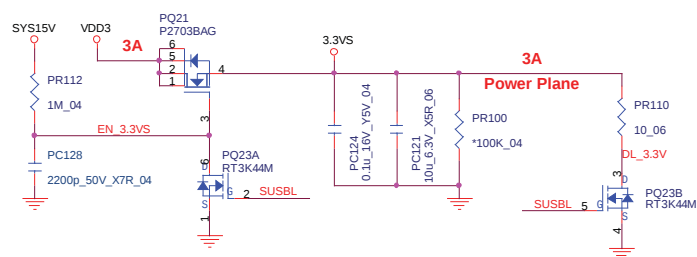
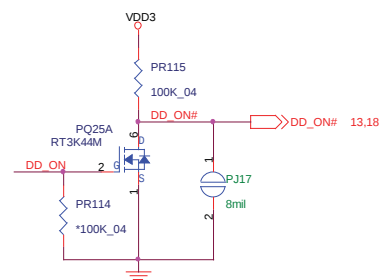
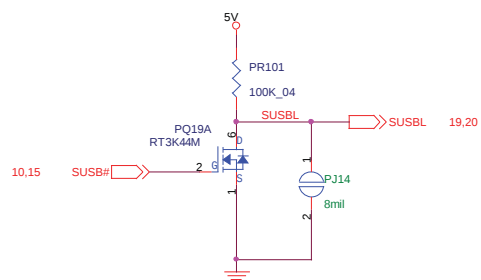
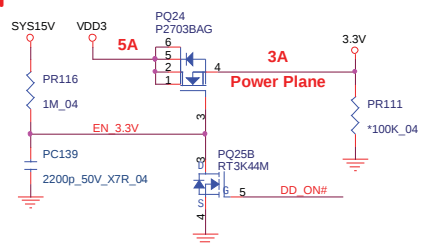
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Title			
[13]USB,WLAN,HDD			
Size	Document Number	Rev	
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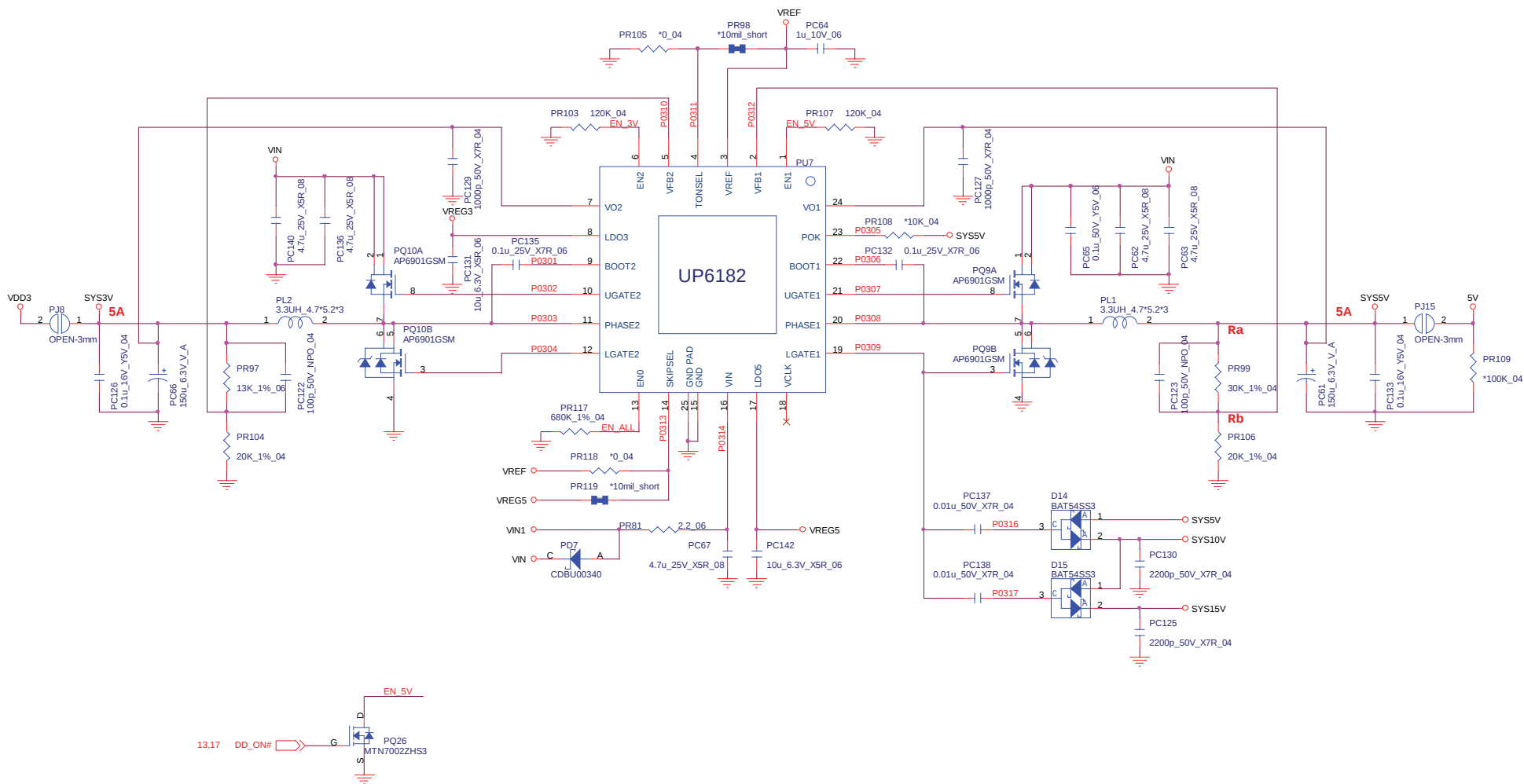






12,16,18,19,20,21	VN	
18	VN1	
16	VA	
18	SYS15V	
11,13,18,19,20,21	5V	
10,12,13,15,16,18	VDD3	
4,5,6,19,20	1.8V	
2,8,10,11,12,13,15,19	3.3V	
11,12,13,14,15	5VS	
2,3,5,6,7,8,9,10,11,12,13,14,15,20,21	3.3VS	
5	1.8VS	

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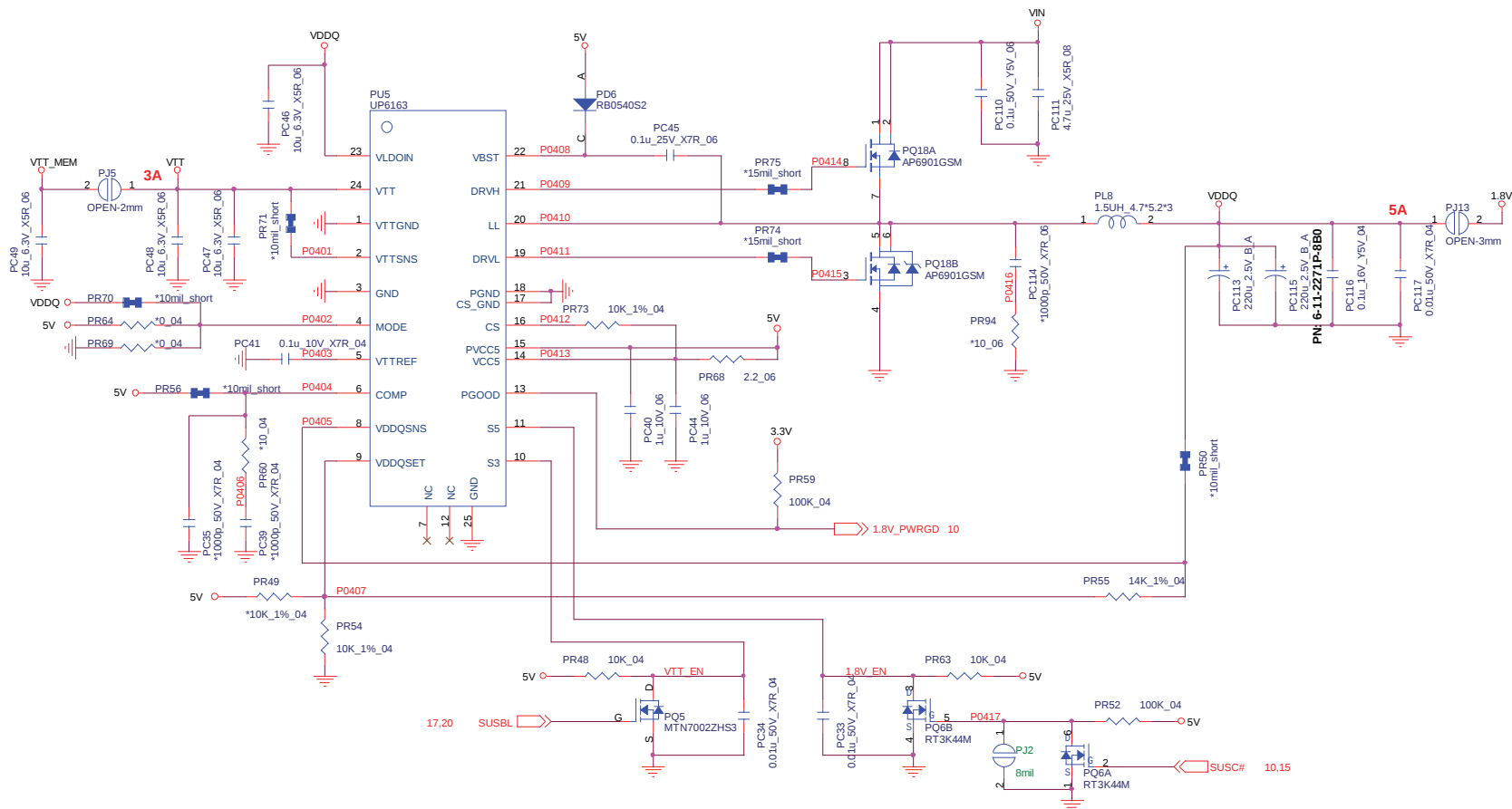
12,16,17,19,20,21 VIN
17 VIN1
17 SYS15V
11,13,17,19,20,21 5V
10,12,13,15,16,17 VDD3

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Title [18]PWR VDD3,5V,SYS15V

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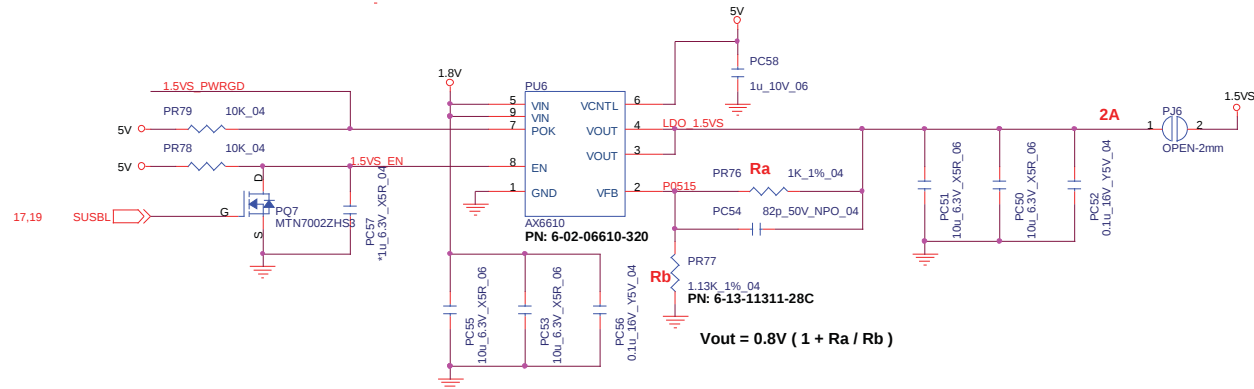
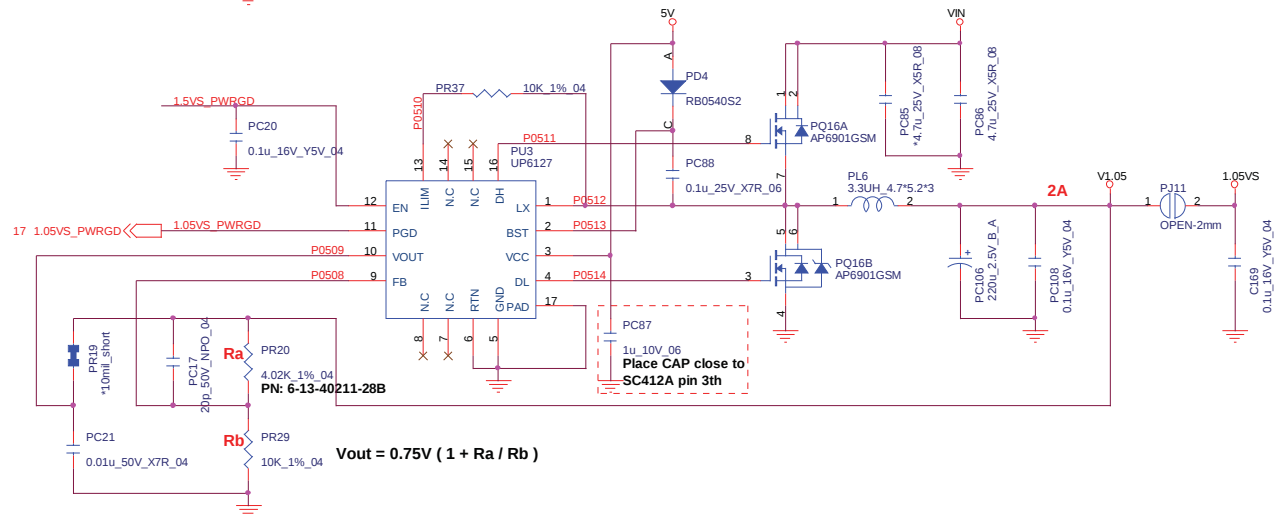
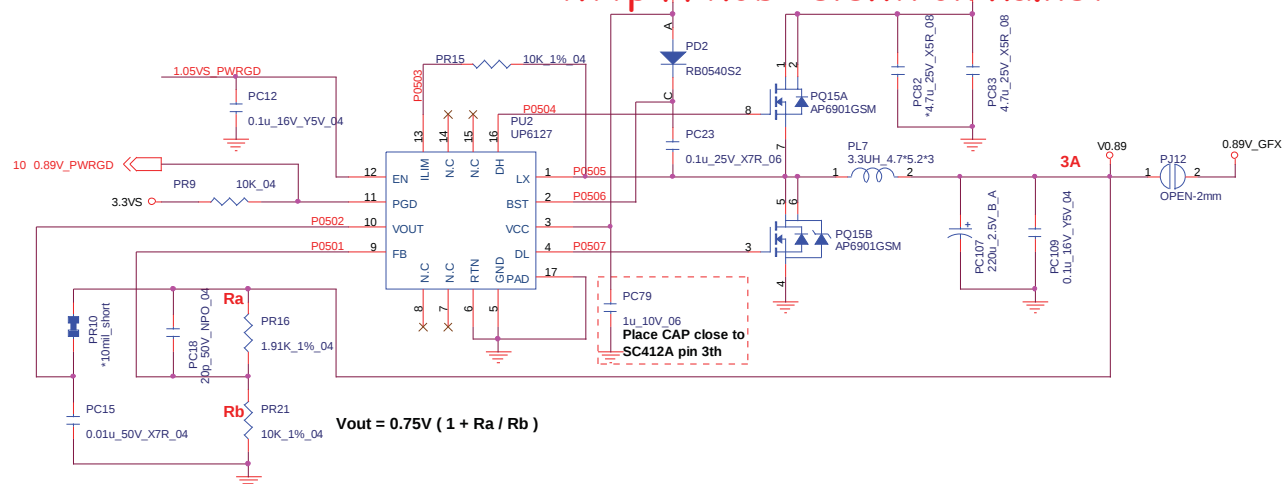
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12,16,17,18,20,21 VIN
11,13,17,18,20,21 5V
2,8,10,11,12,13,15,17 3.3V
4,5,6,20 1.8V
6 VTT_MEM

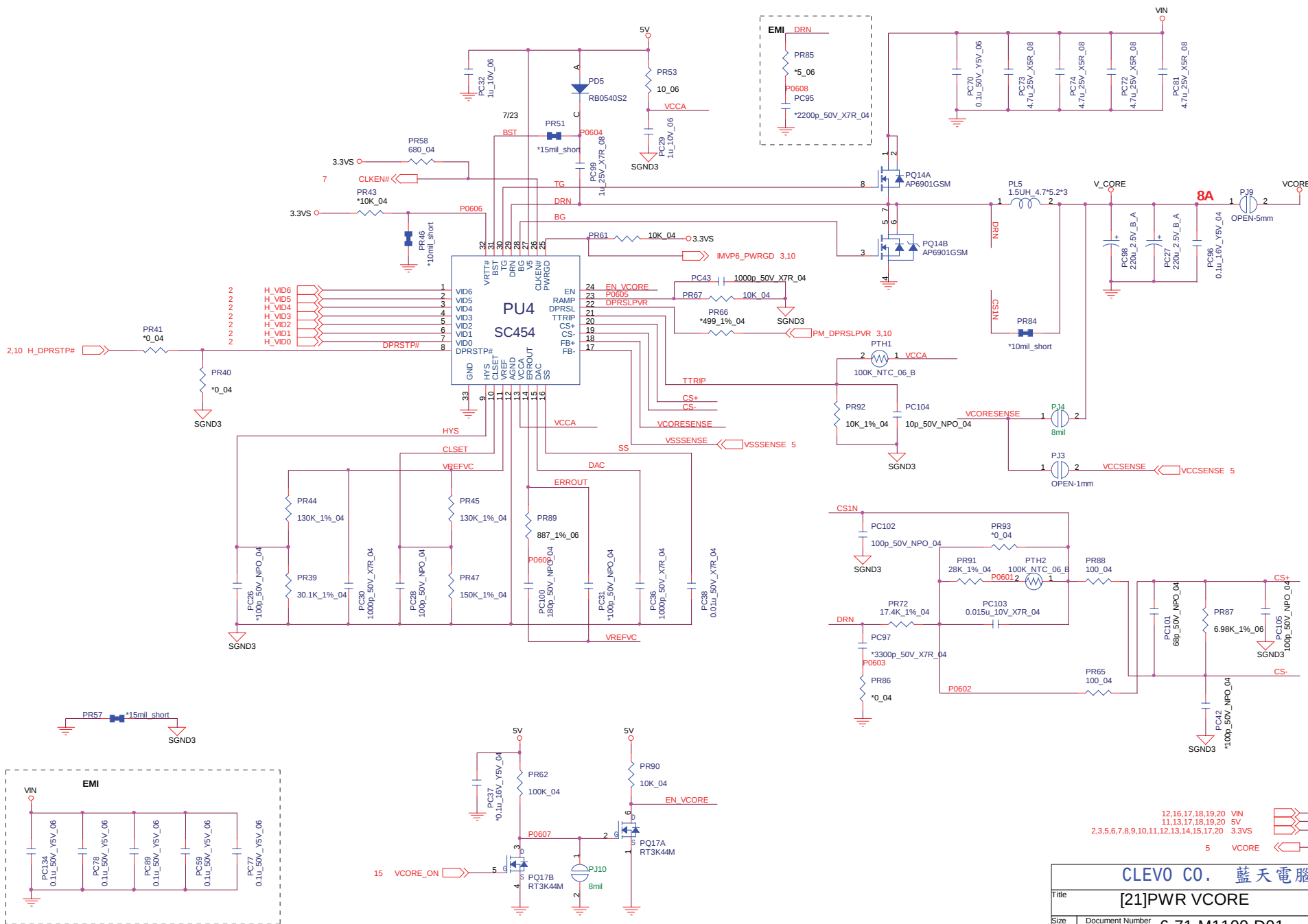
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Title [19]PWR 1.8V,0.9V			
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- 12,16,17,18,19,21 VIN
- 11,13,17,18,19,21 5V
- 11,12,13,14,15,17 5V
- 2,8,10,11,12,13,15,17,19 3.3V
- 2,3,5,6,7,8,9,10,11,12,13,14,15,17,21 3.3V
- 4,5,6,19 1.8V
- 2,5,7,9,10,11 1.05VS
- 5,8,11 1.5VS
- 5 0.89V_GFX

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Title [20]PWR 0.89V,1.05VS,1.5VS			
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12,16,17,18,19,20 VIN
11,13,17,18,19,20 5V
2,3,5,6,7,8,9,10,11,12,13,14,15,17,20 3.3VS
5 Vcore

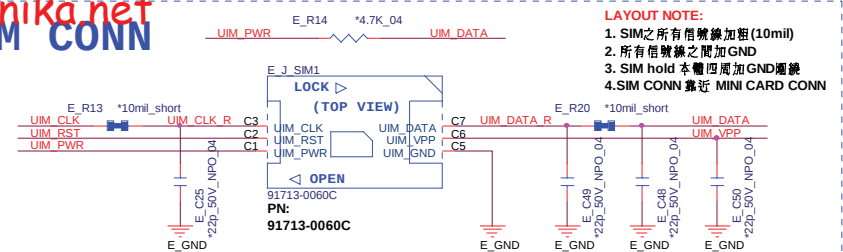
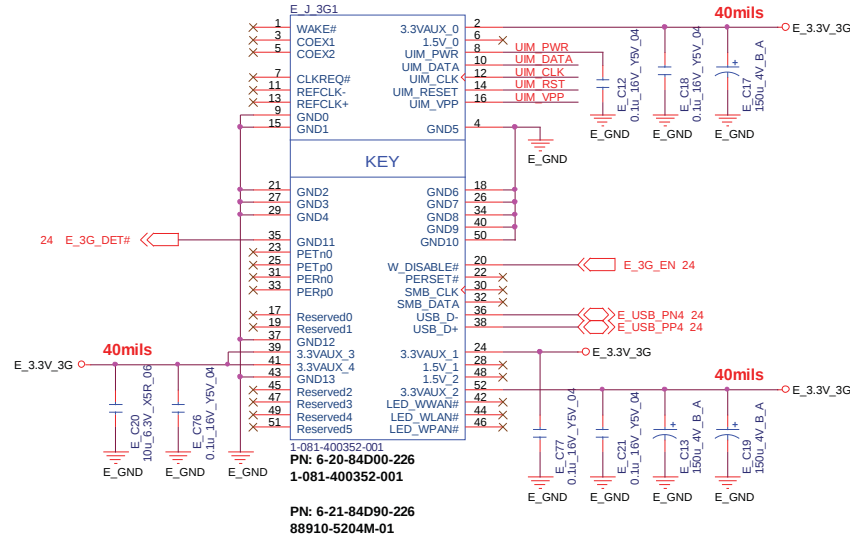
CLEVO CO. 藍天電腦

Title				[21]PWR VCORE			
Size A3		Document Number 6-7P-M1104-001		6-71-M1100-D01		Rev 1.0	
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3G CARD

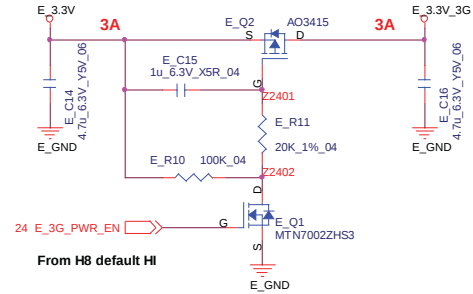
<http://hobi-elektronika.net>

SIM CONN



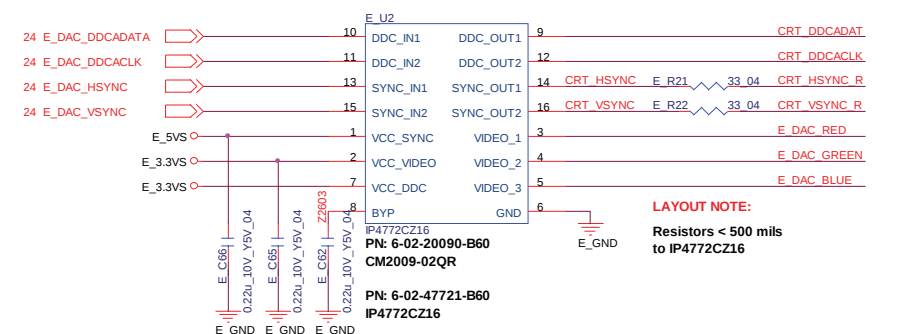
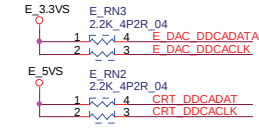
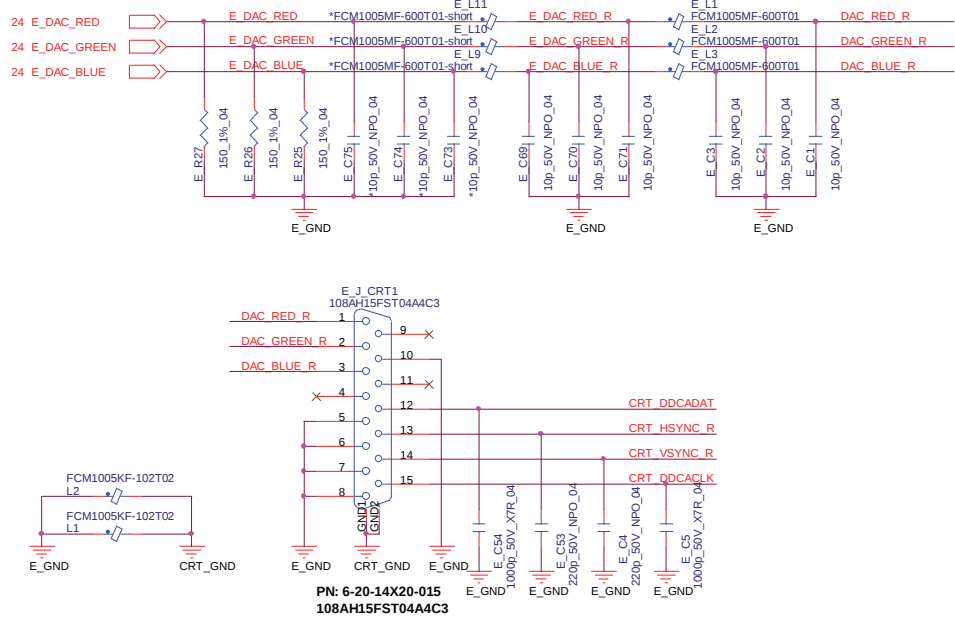
- LAYOUT NOTE:**
1. SIM之所有信號線加粗(10mil)
 2. 所有信號線之間加GND
 3. SIM hold 本電路增加GND通線
 4. SIM CONN 靠近 MINI CARD CONN

3G POWER



CRT

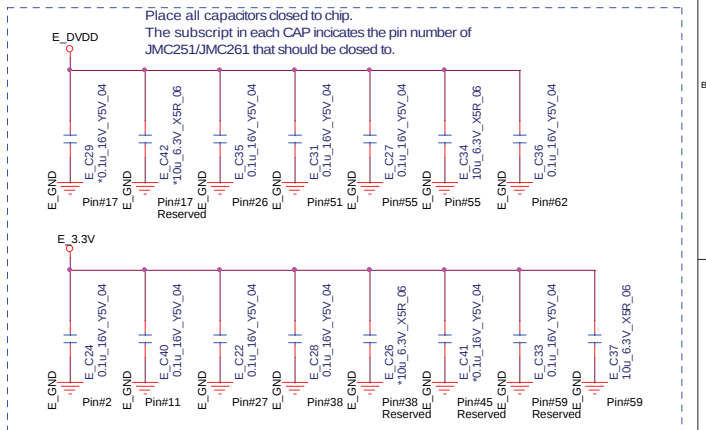
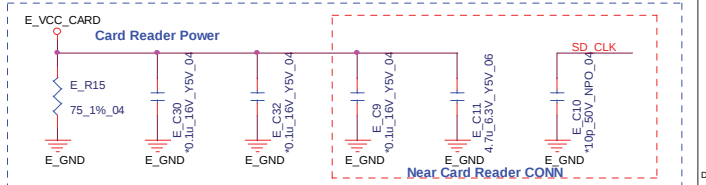
CRT DAC Signal Group
CRT_RED, CRT_GREEN, CRT_BLUE
 VGA RGB resistors colse to Connector
 $Z_0 = 55 \text{ Ohm} \pm 15\%$
 signal : 4 mils
 length < 500 mils



- LAYOUT NOTE:**
1. Resistor < 500 mils to IP4772CZ16

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Title [22]3G CARD,CRT			
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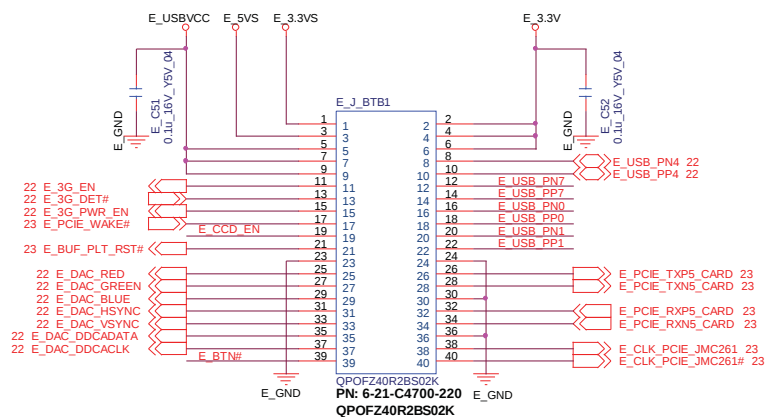


Title				[23]LAN,CARD READER(JMB261)			
Size	Document Number					Rev	
A3	6-71-M1101-D01					1.0	
6-7P-M1104-001							
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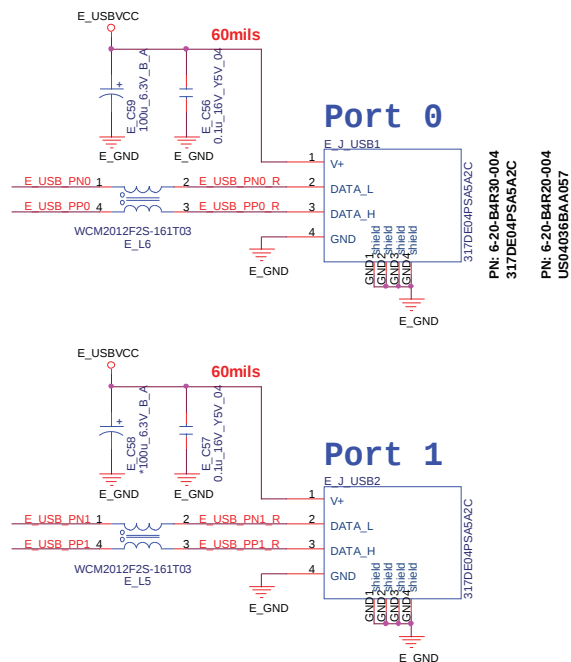
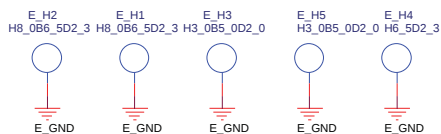
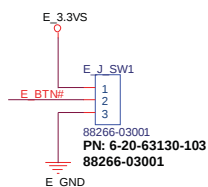
CONN. FOR CONT TO M/B

<http://hobi-elektronika.net>

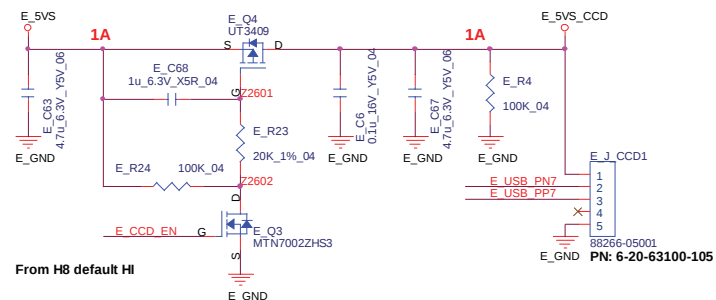
USB PORT_0&1



POWER SW CONN.

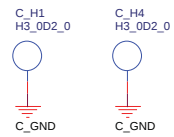
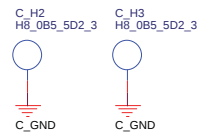
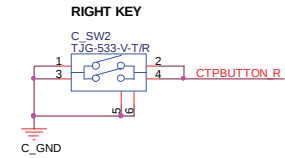
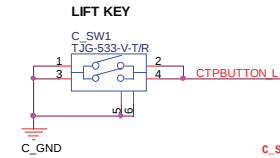
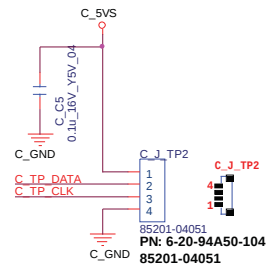
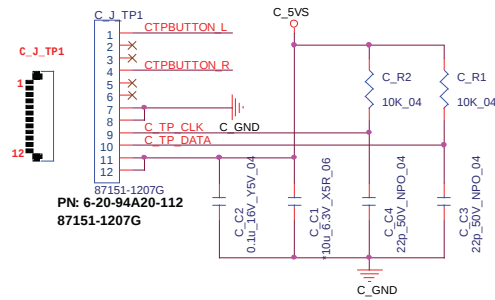


CCD CONN.

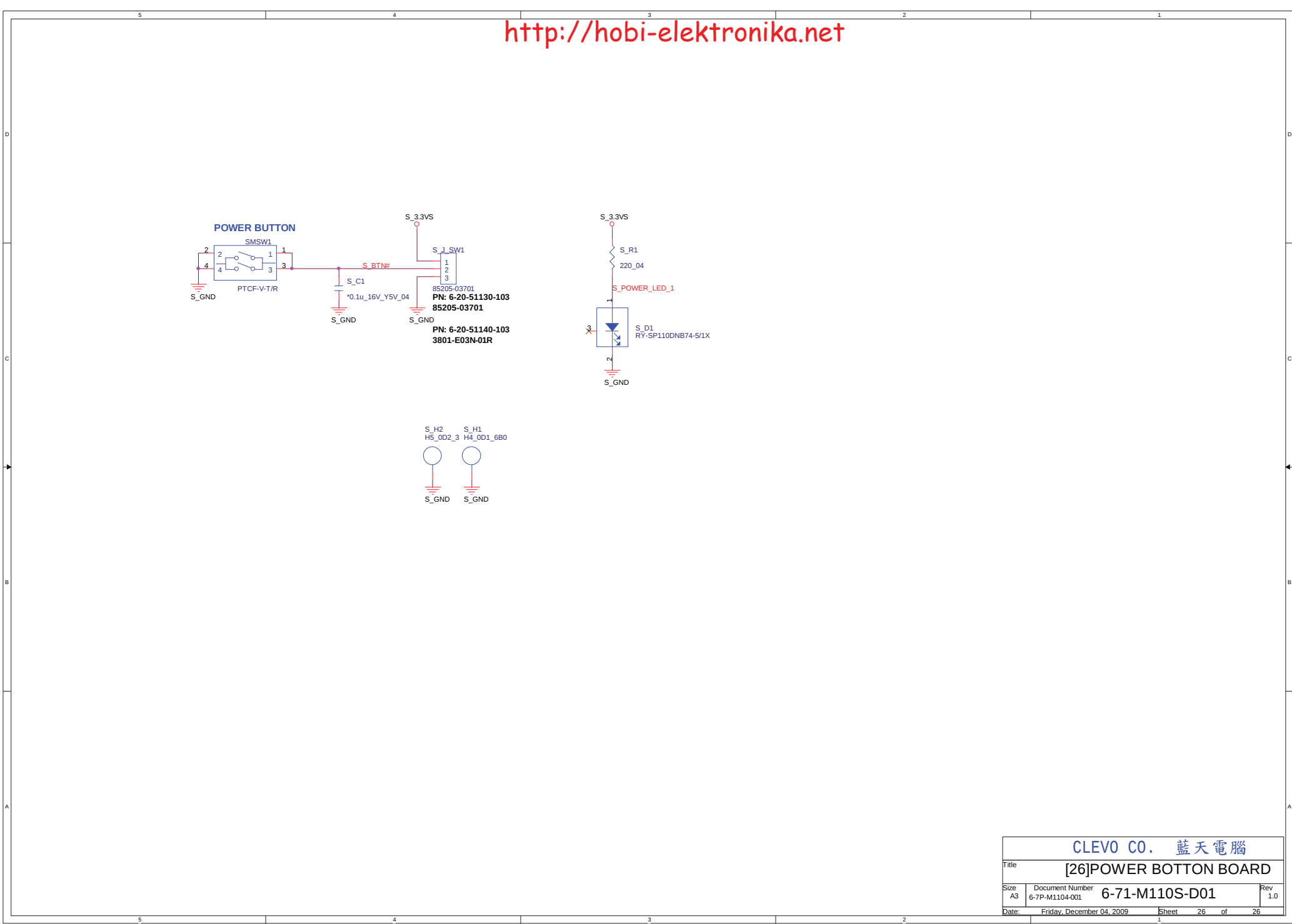


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Title			
[24]USB,CCD,PWR SW			
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Title [25]CLICK BOARD			
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POWER BUTTON

SMSW1
PTCF-V-T/R

S_GND

S_3.3VS

S_BTN#

S_C1
*0.1u_16V_Y5V_04

S_GND

S_3.3VS

S_R1
220_04

S_POWER_LED_1

S_D1
RY-SP110DNB74-5/1X

S_GND

S_H2
H5_0D2_3

S_GND

S_H1
H4_0D1_6B0

S_GND

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Title [26]POWER BOTTON BOARD			
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