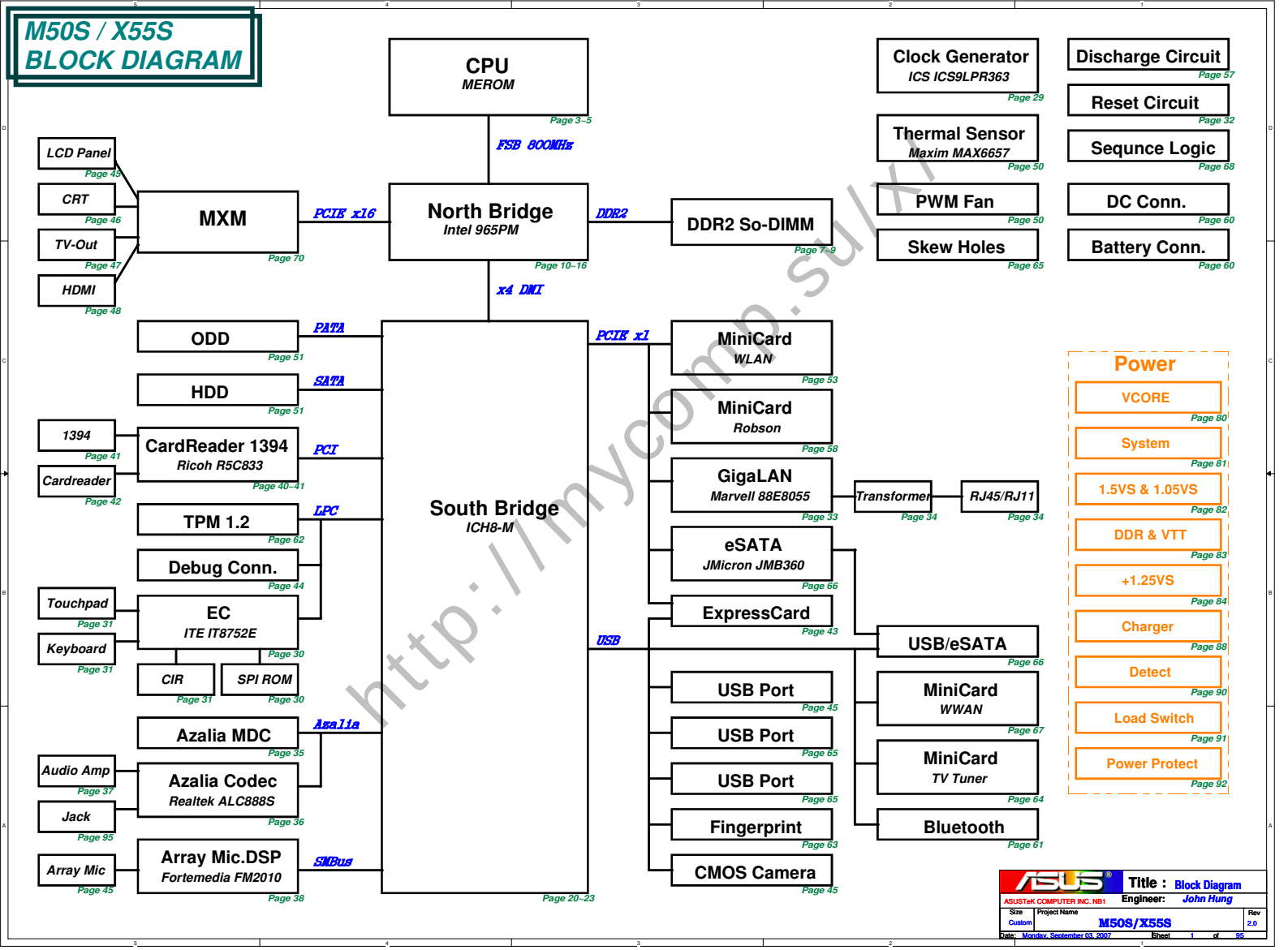
M50S / X55S BLOCK DIAGRAM



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 1 of 95		

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPIO8	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPIO1/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPIO12	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPIO2/GPIO14		
AE20	STP_PCI#/GPIO15	STP_PCI#	I/O
AJ14	DPRSLPVR/GPIO16	PM_DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPIO18		
AJ10	GPIO19/SATA1GP		
AE11	GPIO20	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPIO0/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8752E GPIO SETTING

Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
29	PWM1/GPA1	CHG_LED_UP#	O
32	PWM2/GPA2		
33	PWM3/GPA3		
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
36	PWM6/GPA6		
38	PWM7/GPA7		
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
139	CTX0/GPB2		
124	SMCLK0/GPB3	SMB0_CLK	I/O
125	SMDAT0/GPB4	SMB0_DAT	I/O
142	GA20/GPB5	A20GATE	O
4	KBRST#/GPB6	RC_IN#	O
126	GPB7	PM_RSMRST#	O
133	CRX0/GPC0	CRX0	I
129	SMCLK1/GPC1	SMB1_CLK	I/O
130	SMDAT1/GPC2	SMB1_DAT	I/O
64	GPC3	PM_PWRBTN#	O
136	WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	WUI3/GPC6	BAT1_IN_OC#	I
20	GPC7	RFON_SW#	I
22	WUI0/GPD0	PWRLIMIT#	I
25	WUI1/GPD1	PM_SUSC#	I
26	WUI4/GPD2	BUF_PLT_RST#	I
27	ECSCI#/GPD3	EXT_SCI#	O
19	GPD4	EXT_SMI#	O
37	GPD5	LCD_BACKOFF#	O
53	TACH0 / GPD6	FAN0_TACH	I
54	GPD7		
23	GPE0	VSUS_ON	O
94	GPE1	SUSC_EC#	O
95	GPE2	SUSB_EC#	O
96	GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	GPE6	LID_SW#	I
24	GPE7	INSTANT_ON#	I
97	PS2CLK0/GPF0		
98	PS2DAT0/GPF1	COLOREN#	I
99	PS2CLK1/GPF2	MARATHON#	I
100	PS2DAT1/GPF3	DISTP#	I
101	PS2CLK2/GPF4	TP_CLK	I/O
102	PS2DAT2/GPF5	TP_DAT	I/O
131	SMCLK2/GPF6	THRO_CPU	O
132	SMDAT2/GPF7	TP_LED	O
118	WUI7/GPG0		
121	GPG1	PM_SUSB#	I
112	GPG2		
116	GPG6		

Pin	Pin Name	Signal Name	Type
105	CLKRUN#/GPH0	PM_CLKRUN#	I/O
106	CRX1/GPH1	3G_ON#	O
107	CTX1/GPH2	3G_LED_ON#	O
108	GPH3	BAT_LEARN	I/O
109	GPH4		
110	GPH5	NUM_LED	O
111	GPH6	CAP_LED	O
74	ADC0/GPI0	NV_OVERT#	I
75	ADC1/GPI1	SUS_PWRGD	I
76	ADC2/GPI2	ALL_SYS_PWRGD	I
77	ADC3/GPI3	CPU_PWRGD	I
78	ADC4/GPI4	PWR_MON	I
79	ADC5/GPI5	ALS_D4	I
80	ADC6/GPI6		
81	ADC7/GPI7		
84	DAC0/GPJ0	EC_CLK_EN	
85	DAC1/GPJ1	PM_PWROK	
86	DAC1/GPJ2		
87	DAC1/GPJ3		
88	DAC1/GPJ4		
89	DAC1/GPJ5		
15	GPK0		
16	GPK1		
17	GPK2		
18	GPK3		
48	GPK4		
49	GPK5		
62	GPK6		
63	GPK7		
90	GPL0		
91	GPL1		
92	GPL2		
93	GPL3		
119	GPL4		
120	GPL5		
134	GPL6		
135	GPL7		

965GM/PM co-layout option:

965PM

Change:
- U1001 to 965PM, U3601 to ALC888S
- R1213~R1219 to 0ohm
- C1406, C1501~C1504, C1506~C1507, C1510, C1514 to 0ohm

Mount:
- D4801~D4803
- F4801
- J4801, J7001
- H7001~H7004
- Q4801
- R1112~R1117, R1203~R1212, R1502, R2910, R3618~R3620, R4801~R4804
- RX2901~RX2902, RX4801~RX4810
- CX1201~CX1232

Un-mount:
- R1202, R1401~R1403, R1501, R1503~R1505, R2909, R3621, R7001~R7008
- RN7001~RN7011
- RNX1201, RNX2901, RNX2915
- L1501~L1505
- C1404~C1405, C1407~C1409, C1505, C1509, C1511~C1513
- CE1404, CE1501~CE1503

965GM

Change:
- U1001 to 965GM
- R1213~R1218 to 150ohm
- R1219 to 1.3Kohm

Un-mount:
- D4801~D4803
- F4801
- J4801, J7001
- H7001~H7004
- Q4801
- R1112~R1117, R1203~R1212, R1502, R2910, R3618~R3620, R4801~R4804
- RX2901~RX2902, RX4801~RX4810
- CX1201~CX1232

Mount:
- R1202, R1401~R1403, R1501, R1503~R1505, R2909, R3621, R7001~R7008
- RN7001~RN7011
- RNX1201, RNX2901, RNX2915
- L1501~L1505
- C1404~C1409, C1501~C1507, C1509~C1514
- CE1404, CE1501~CE1503

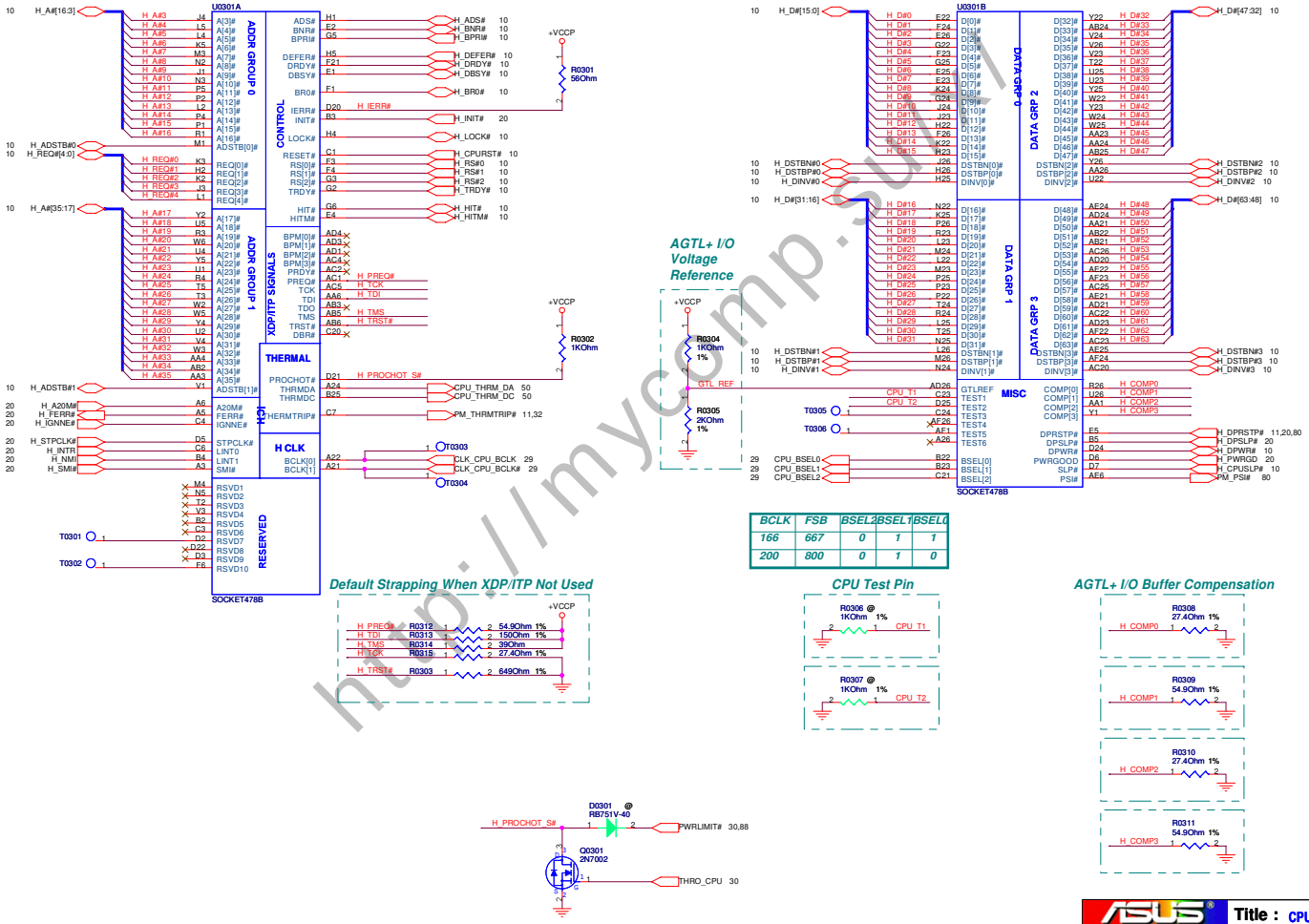
ASUSTeK COMPUTER INC. NB1

Title : System Setting

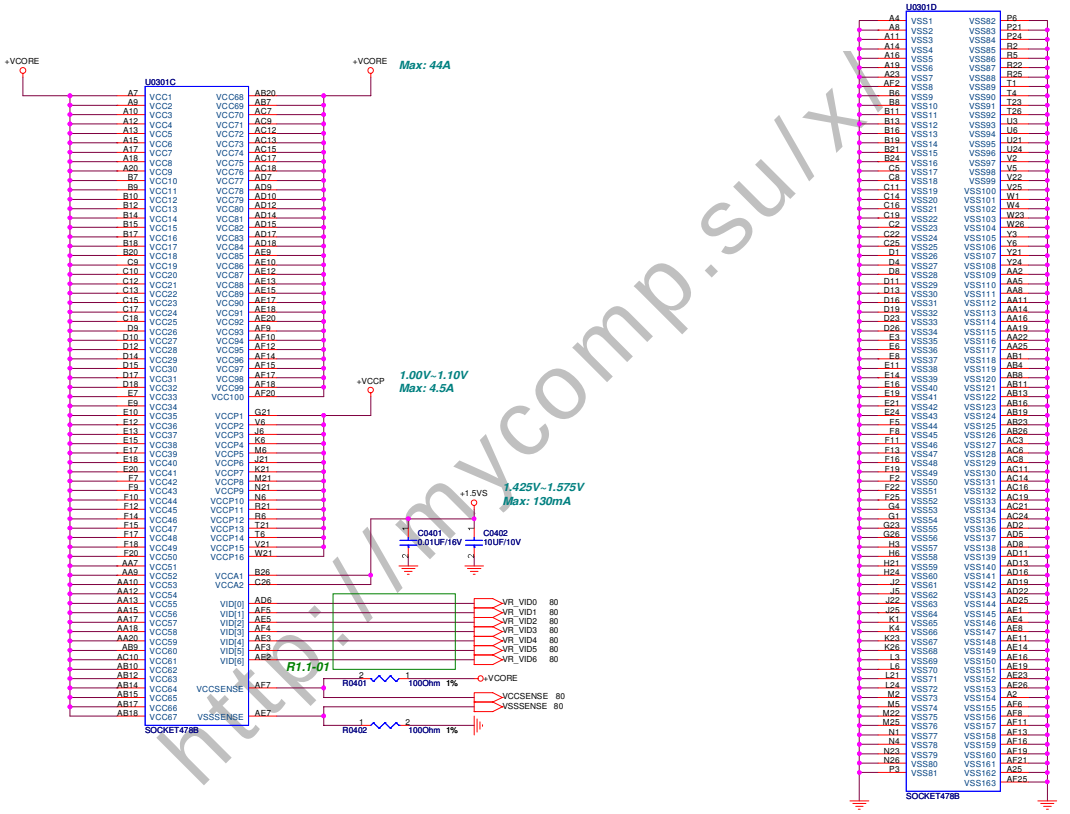
Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0

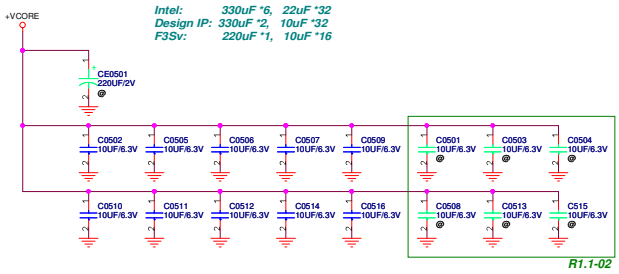
Date: Monday, September 03, 2007 Sheet 2 of 95

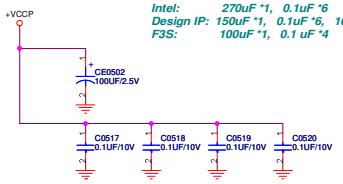


Title :	CPU_Merom(Host)	
ASUSTeK COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 3 of 95	



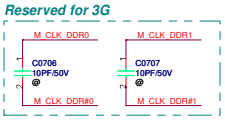
ASUSTeK COMPUTER INC. NB1	Title : CPU_Merom(PWR)		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 4 of 55		



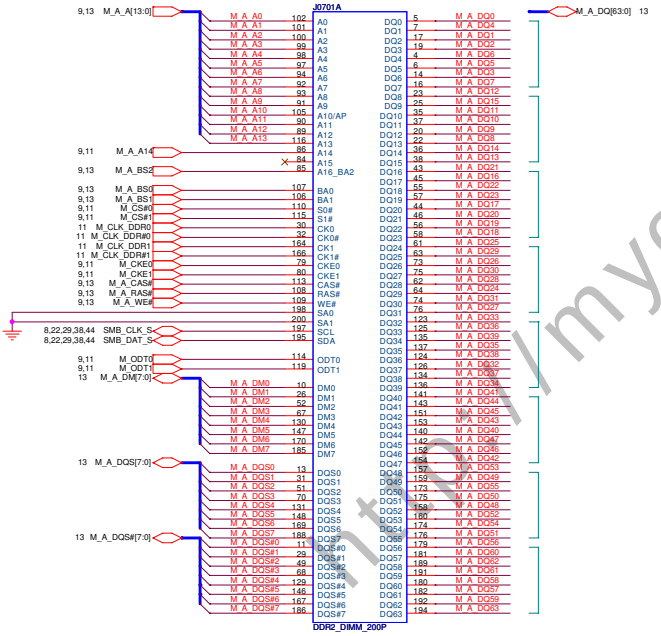


ASUSTeK COMPUTER INC. NB1	Title : CPU_Capacitors	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 5 of 95	

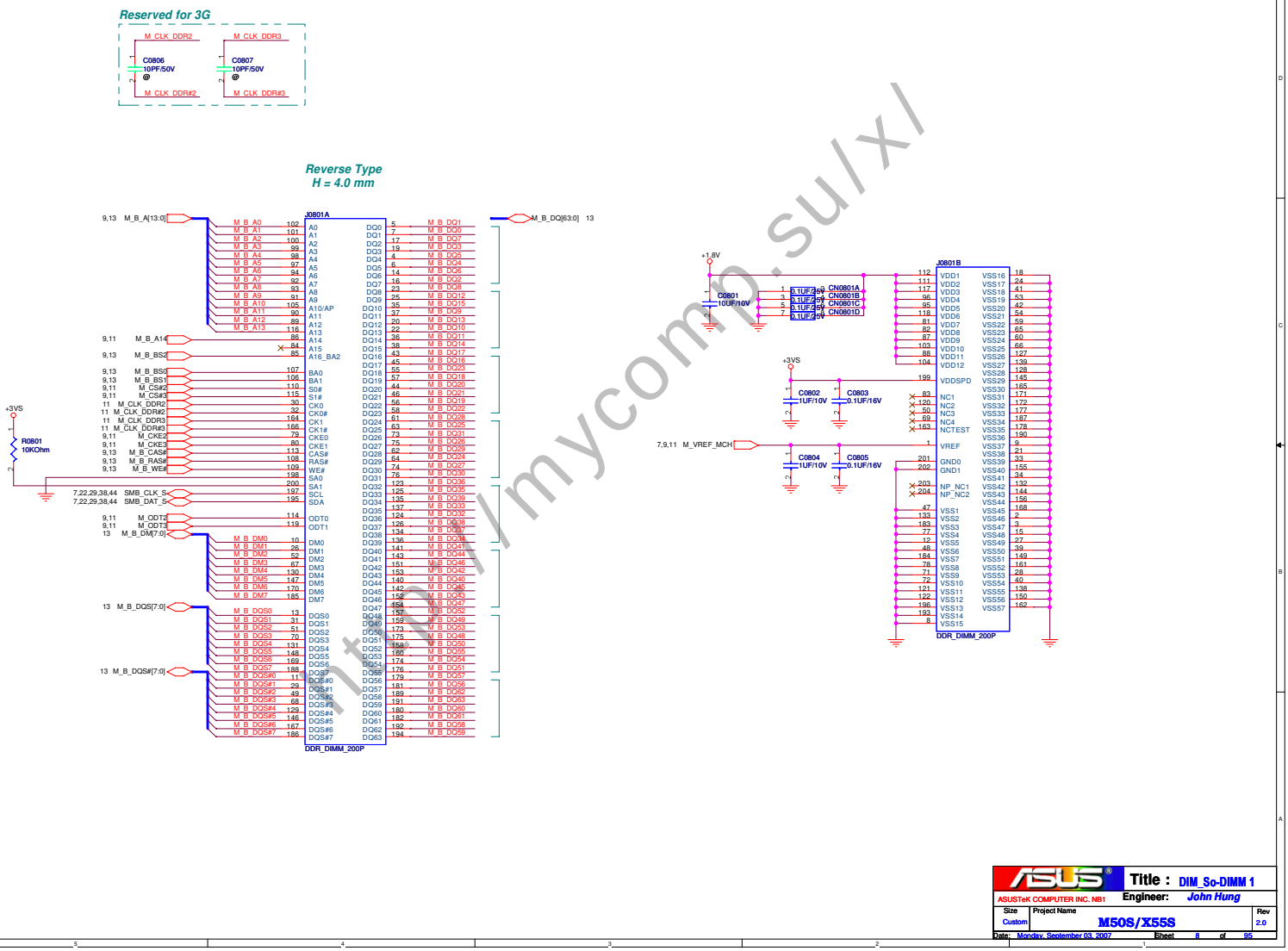
ASUSTeK COMPUTER INC. NB1	Title : CPU-****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 6 of 95		



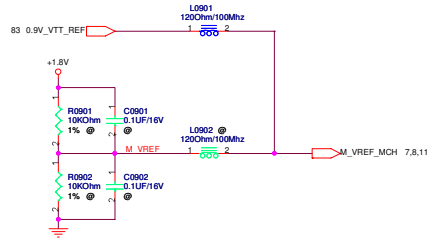
Reverse Type
H = 9.2 mm

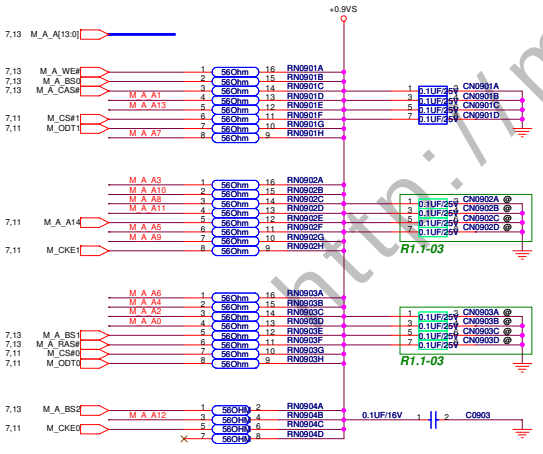


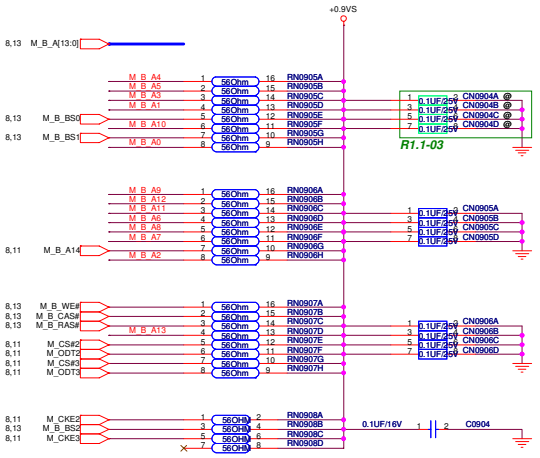
ASUSTeK COMPUTER INC. NB1	Title : DIM_So-DIMM 0		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 7 of 95		



ASUSTeK COMPUTER INC. NB1	Title : DIM_So-DIMM 1	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 8 of 95	



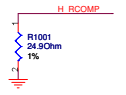




ASUSTeK COMPUTER INC. NB1	Title : DIM_DDR2 Termination	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 9 of 95	

FSB RCOMP

For Calibrating the FSB I/O Buffer

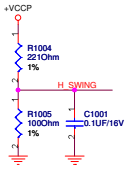


FSB SCOMP

For Slew Rate Compenssation on the FSB

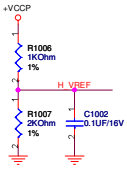
FSB Voltage Swing

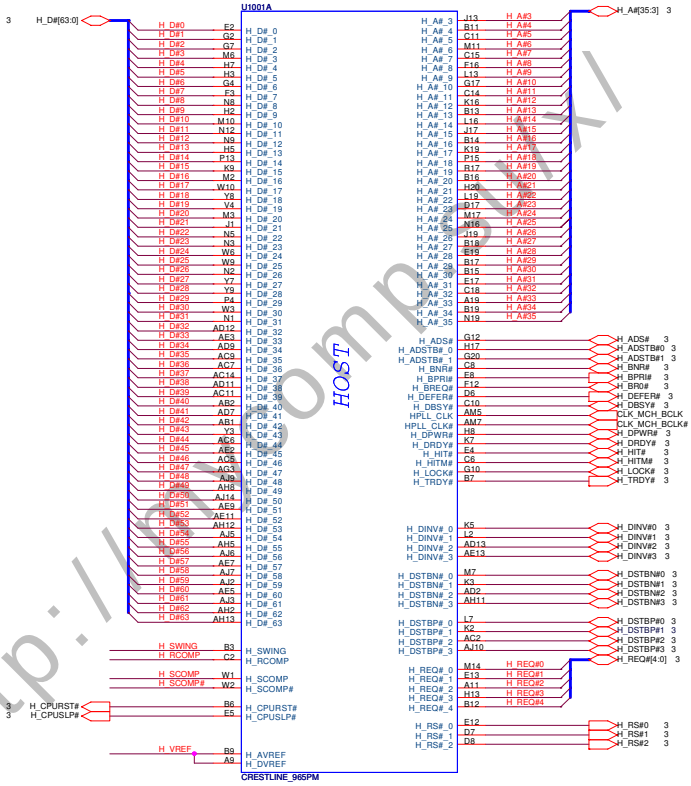
For Providing a Reference Voltage to The FSB RCOMP circuits



FSB VREF

For Providing Reference Voltage for FSB Signals





ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(Host)	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 10 of 95	

CFG5 : DMI Strap
0 = DMI x2
1 = DMI x4 (D)

CFG7 : CPU Strap
0 = Reserved
1 = Mobile CPU (D)

CFG9 : PCIE Graphic Lane
0 = Reverse Lane
1 = Normal Operation (D)

R1101 @ 4.02KOHM 1% — MCH_CFG9

CFG[13:12] : GMCH Test Mode
00 = Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

CFG16 : FSB Dynamic ODT
0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

CFG18: Core Voltage
0 = 1.05V (D)
1 = 1.5V

CFG19 : DMI Lane Reversal
0 = Normal Operation (D)
1 = Lanes Reversed

+3VS — R1102 @ 4.02KOHM 1% — MCH_CFG19

CFG20 : Concurrent SDVO / PCIe
0 = Only one is operational (D)
1 = operate simultaneous

U1001B

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 — C1101 0.1UF/16V

RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29 RSVD30 RSVD31

SA_MA_14 SB_MA_14 RSVD34 RSVD35 RSVD36 LVDSA_DATA#_3 LVDSA_DATA_3 RSVD39 RSVD40 RSVD41 RSVD42 RSVD43 RSVD44 RSVD45

M_A_A14 (7,9) M_B_A14 (8,9)

CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

MCH_BSEL0 (29) MCH_BSEL1 (29) MCH_BSEL2 (29)

T1101 T1102 T1103 T1104 T1105 T1106 T1107 — MCH_CFG9 — MCH_CFG19

PM_BM_BUSY# (22, 3,20,80) H_DPRSTP# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

PM_EXTTS#0 PM_EXTTS#1 — PM_PWROK (22,30) — BUF_PLT_RST# (21,30,33,38,43,51,53,58,62,66,70) — R1103 100Ohm — PM_THRMTRIP# (3,32) (22,80)

+3VS — RN1101A PM_EXTTS#0 — RN1101B PM_EXTTS#1 — RN1101C MCH_CLKREQ# — RN1101D (10KOhm)

NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16

CRESTLINE_965PM

DDR MUXING

SM_CK_0 SM_CK_1 SM_CK_3 SM_CK_4 — M_CLK_DDR0 7, M_CLK_DDR1 7, M_CLK_DDR2 8, M_CLK_DDR3 8

SM_CK#_0 SM_CK#_1 SM_CK#_3 SM_CK#_4 — M_CLK_DDR#0 7, M_CLK_DDR#1 7, M_CLK_DDR#2 8, M_CLK_DDR#3 8

SM_CKE_0 SM_CKE_1 SM_CKE_3 SM_CKE_4 — M_CKE0 7,9, M_CKE1 7,9, M_CKE2 8,9, M_CKE3 8,9

SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 — M_CS#0 7,9, M_CS#1 7,9, M_CS#2 8,9, M_CS#3 8,9

SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 — M_ODT0 7,9, M_ODT1 7,9, M_ODT2 8,9, M_ODT3 8,9

SM_RCOMP SM_RCOMP# — SM_RCOMP SM_RCOMP#

SM_RCOMP_VOH SM_RCOMP_VOL — SM_RCOMP_VOH SM_RCOMP_VOL

SM_VREF_0 SM_VREF_1 — M_VREF_MCH 7,8,9

CLK

DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# — CLK_DREF 29, CLK_DREF# 29, CLK_DREFSS 29, CLK_DREFSS# 29

PEG_CLK PEG_CLK# — CLK_MCH_3GPLL 29, CLK_MCH_3GPLL# 29

DMI

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 — DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 — DMI_TXN[3:0] 21

DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 — DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3 — DMI_TXP[3:0] 21

DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 — DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3 — DMI_RXN[3:0] 21

DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 — DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3 — DMI_RXP[3:0] 21

GRAPHICS VID

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VR_EN

MISC

CL_CLK CL_DATA CL_PWROK CL_RSTB CL_VREF — CL_CLK0 22, CL_DATA0 22, PM_PWROK, CL_RST#0 22, CL_VREF_MCH

SDVO_CTRL_CLK SDVO_CTRL_DATA CLK_REQ# ICH_SYNC# — SDVO_CTRL_CLK SDVO_CTRL_DATA MCH_CLKREQ# — MCH_ICH_SYNC# 22

TEST_1 TEST_2 — R1104 20KOhm 1%

+1.8V — R1105 20Ohm 1% — SM_RCOMP — R1106 20Ohm 1% — SM_RCOMP#

+1.8V — R1107 1KOhm 1% — SM_RCOMP_VOH — C1102 0.01UF/16V, C1103 1UF/10V — R1108 3.01KOhm 1% — SM_RCOMP_VOL — C1104 0.01UF/16V, C1105 1UF/10V — R1109 1KOhm 1%

M_VREF_MCH — C1106 0.1UF/16V, C1107 0.1UF/16V

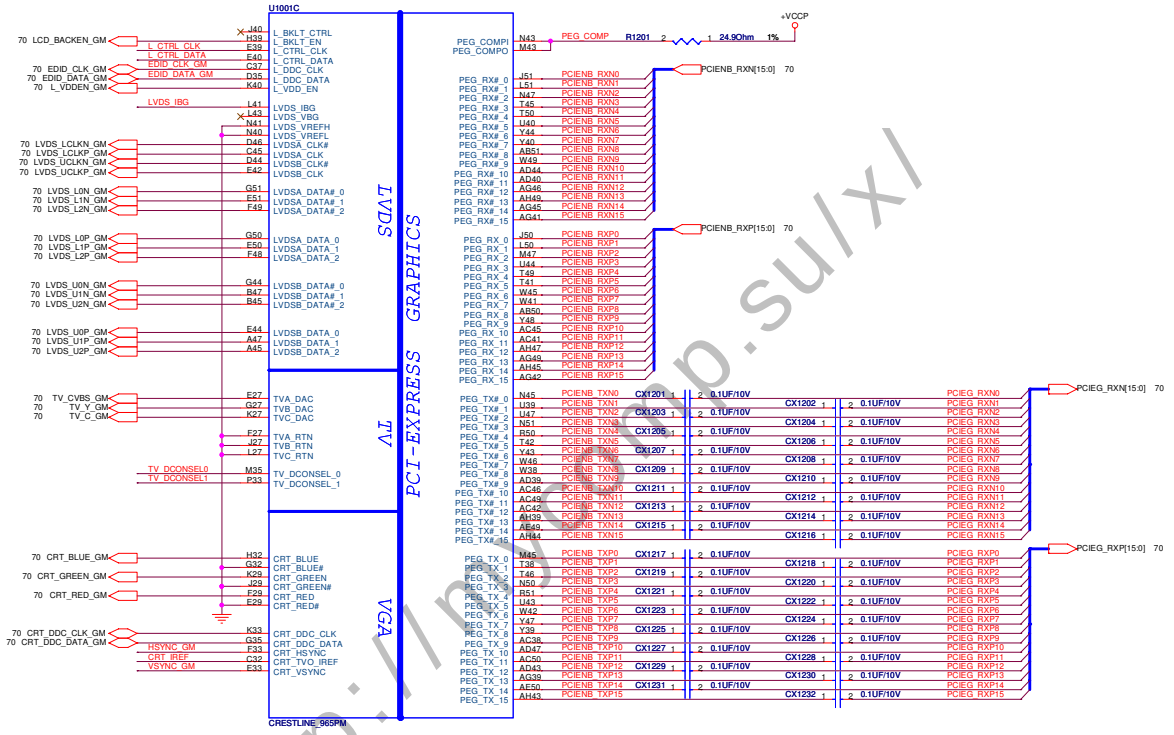
+1.25VS — R1110 1KOhm 1% — CL_VREF_MCH — C1108 0.1UF/16V — R1111 392OHM 1%

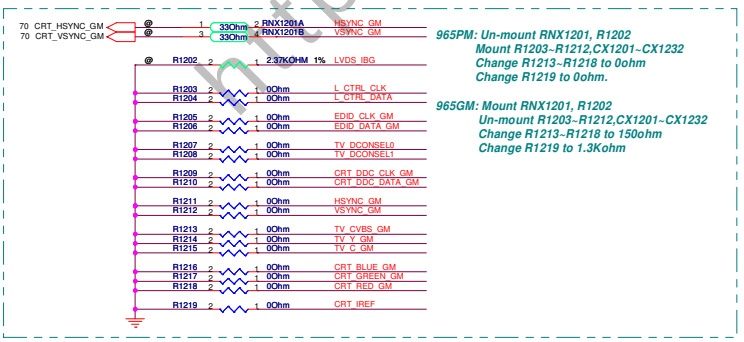
Option for 965PM/GM
965PM: Mount R1112~R1117
965GM: Un-mount R1112~R1117

CLK_DREF R1112 0Ohm
CLK_DREF# R1113 0Ohm
CLK_DREFSS R1114 0Ohm
CLK_DREFSS# R1115 0Ohm
SDVO_CTRL_CLK R1116 0Ohm
SDVO_CTRL_DATA R1117 0Ohm

ASUSTeK COMPUTER INC. NB1

Title : NB_965PM(DMI/CFG)
Engineer: John Hung
Size: Custom
Project Name: M50S/X55S
Rev: 2.0
Date: Monday, September 03, 2007
Sheet 11 of 95

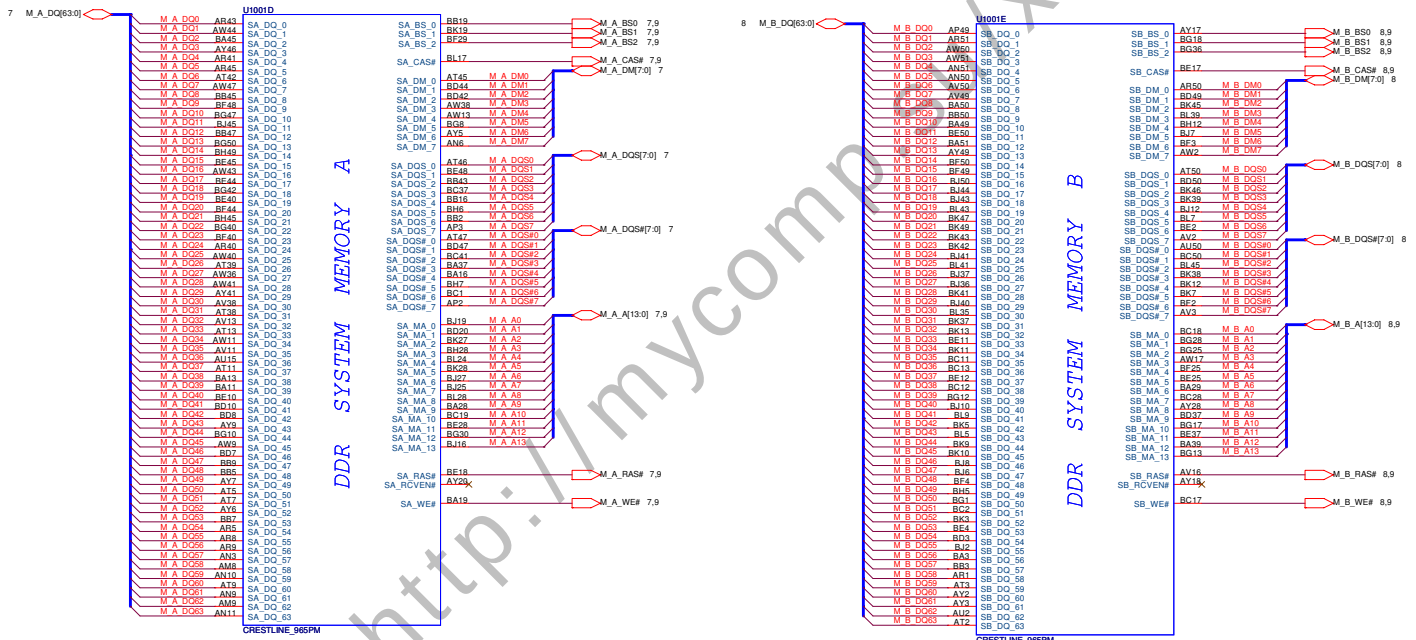




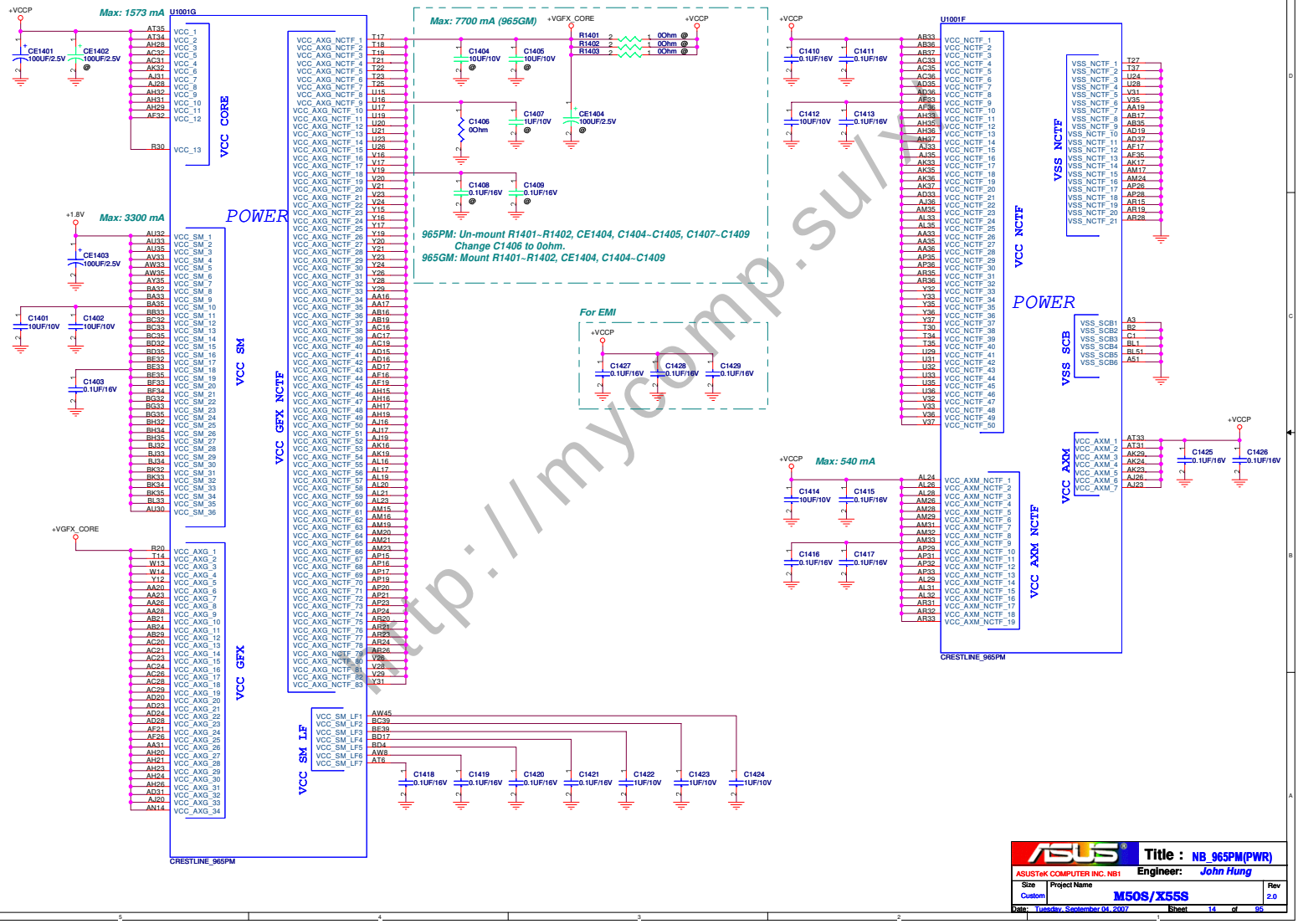
965PM: Un-mount RNX1201, R1202
Mount R1203~R1212,CX1201~CX1232
Change R1213~R1218 to 0ohm
Change R1219 to 0ohm.

965GM: Mount RNX1201, R1202
Un-mount R1203~R1212,CX1201~CX1232
Change R1213~R1218 to 150ohm
Change R1219 to 1.3Kohm

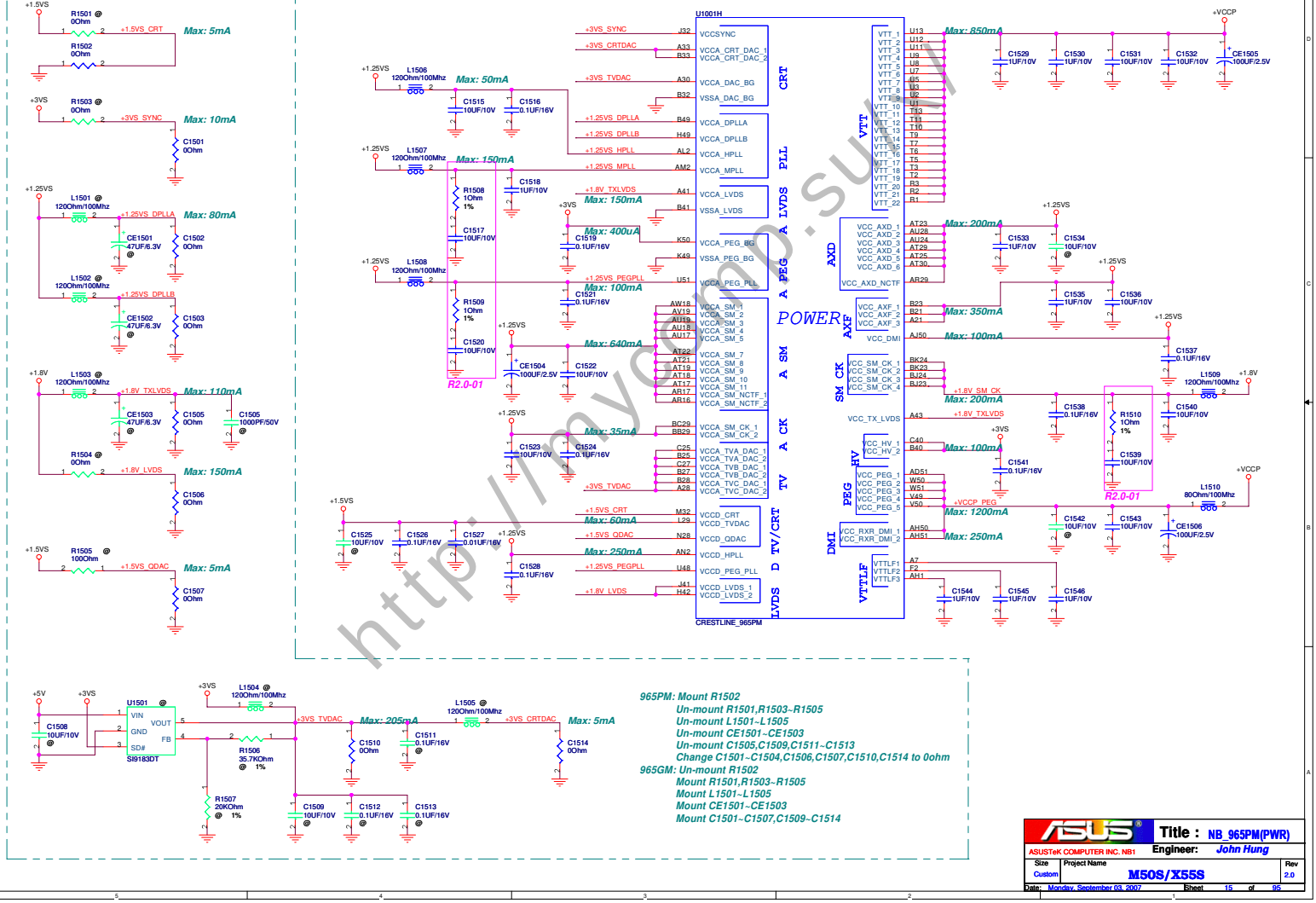
ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(GFX)		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 12 of 95		



ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(DDR2)		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 13 of 95		

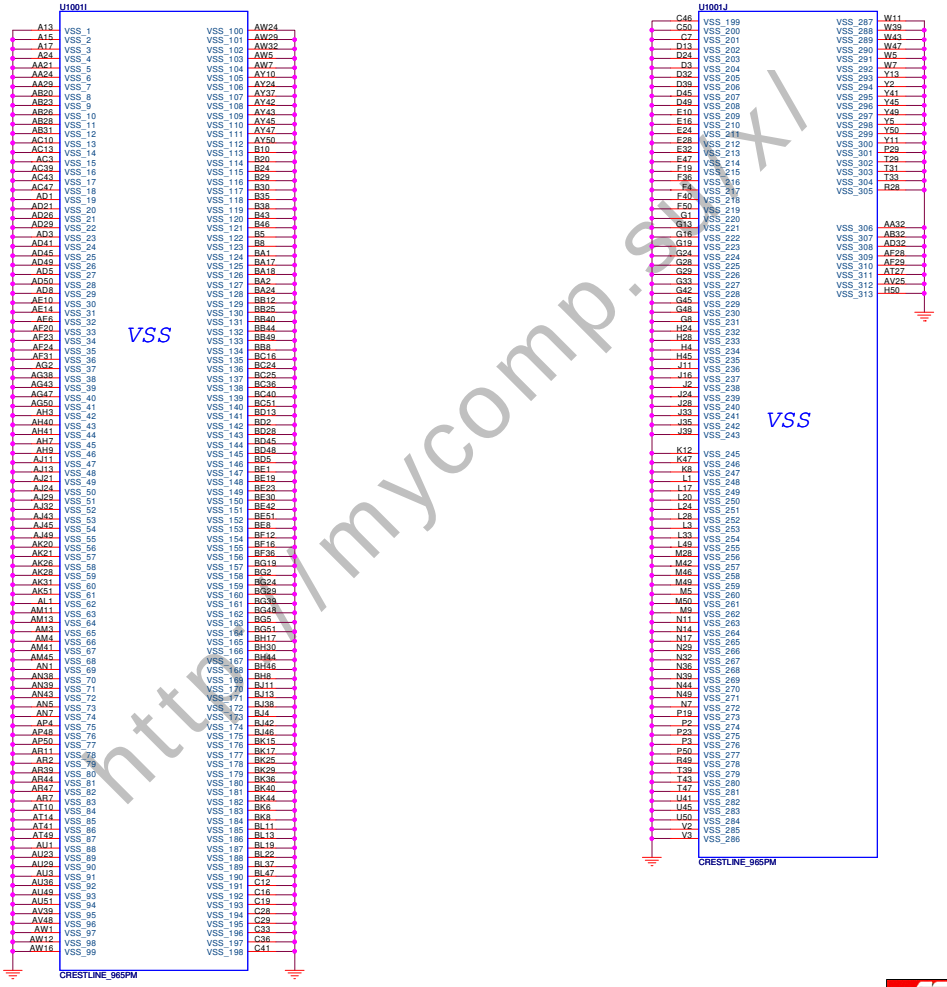


ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(PWR)		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Tuesday, September 04, 2007	Sheet 14 of 95		



965PM: Mount R1502
Un-mount R1501,R1503~R1505
Un-mount L1501~L1505
Un-mount CE1501~CE1503
Un-mount C1505,C1509,C1511~C1513
Change C1501~C1504,C1506,C1507,C1510,C1514 to 0ohm
965GM: Un-mount R1502
Mount R1501,R1503~R1505
Mount L1501~L1505
Mount CE1501~CE1503
Mount C1501~C1507,C1509~C1514

ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(PWR)	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 15 of 95	



ASUSTeK COMPUTER INC. NB1	Title : NB_965PM(GND)		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 16 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 17 of 95		

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 18 of 95	

Main Board

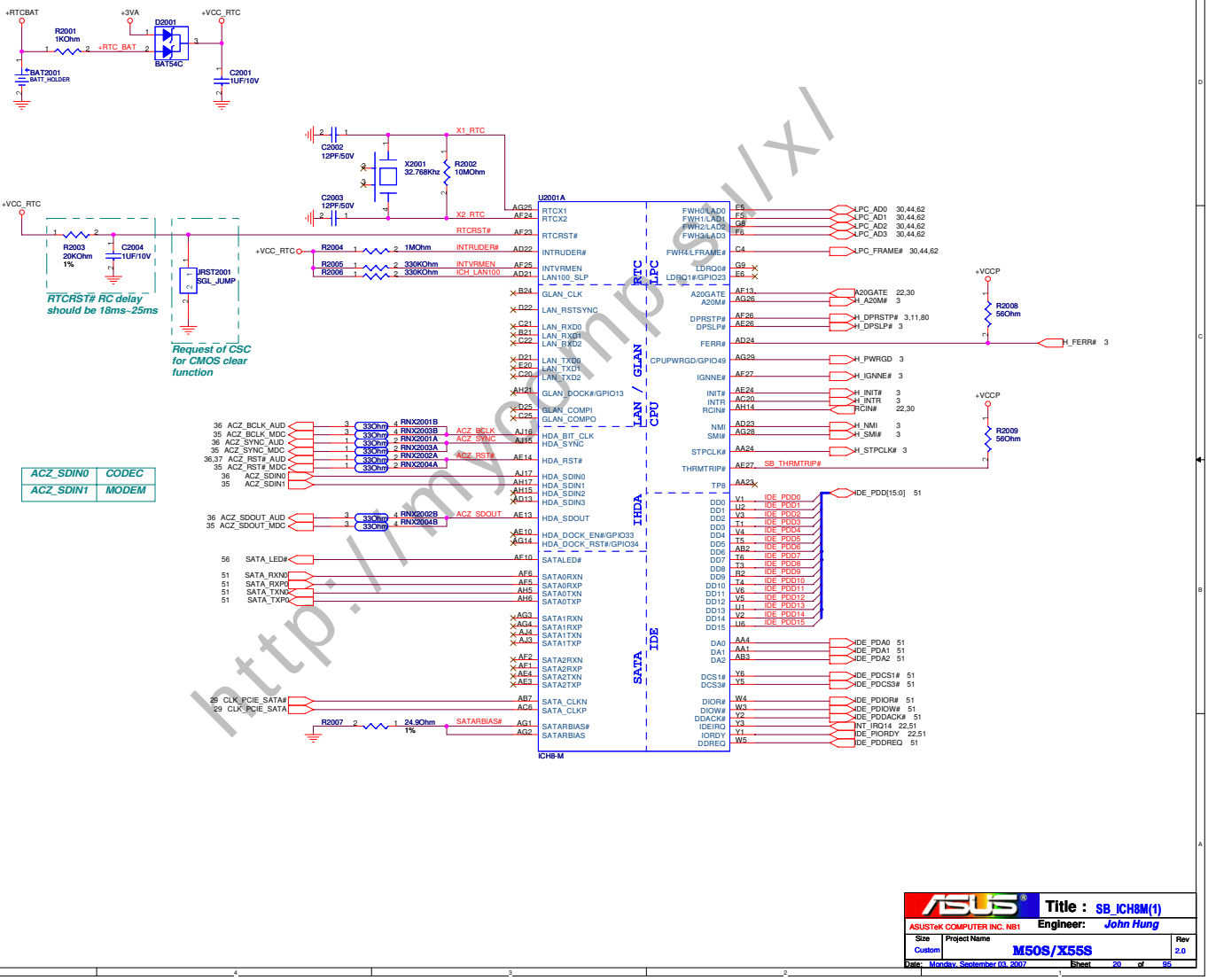
Title : MEM_****

ASUSTeK COMPUTER INC. NB1

Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0

Date: Monday, September 03, 2007 Sheet 19 of 95



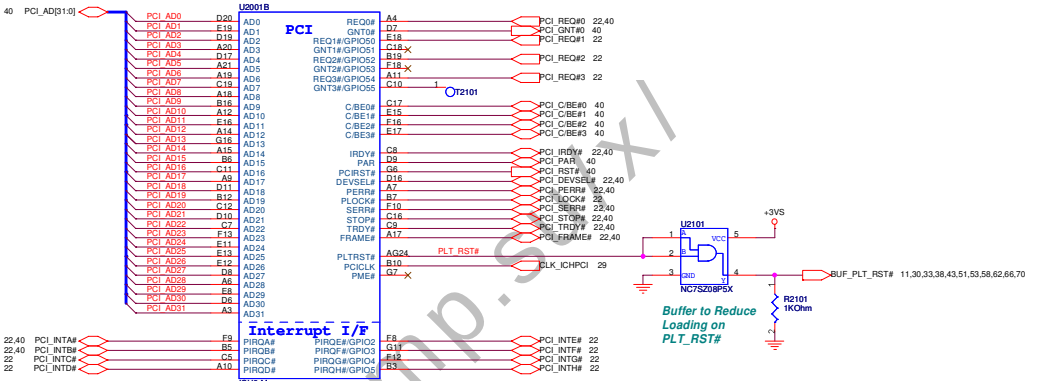
Title : SB_ICH8M(1)		
ASUSTeK COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 20 of 95	

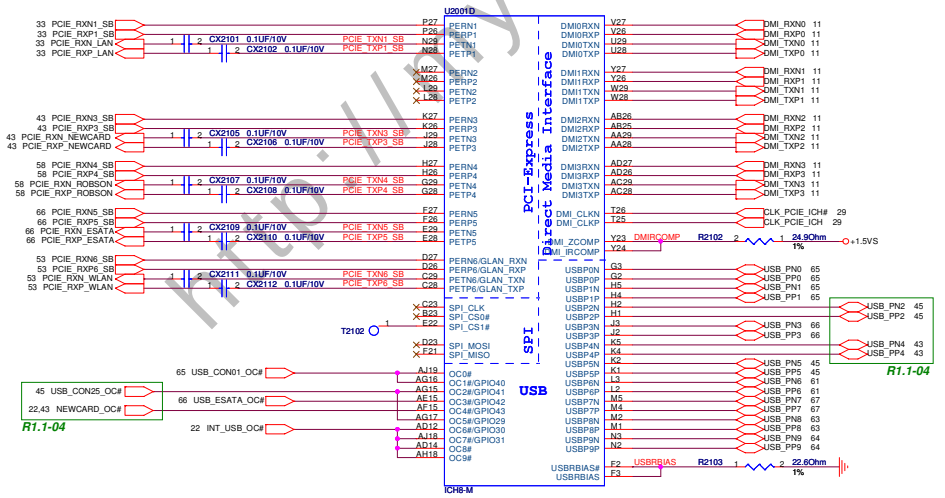
ICH_TP3, ACZ_SDOUT : XOR Chain Entrance Strap
- 00 = Reserved
- 01 = Enter XOR Chain
- 10 = Normal Operation (D)
- 11 = Set PCIe Port Config Bit 1

GNT0#, SPI_CS1 : ICH8 Boot BIOS Select
- 00 = Reserved
- 01 = SPI
- 10 = PCI
- 11 = LPC (D)

GNT2# : PCIe Port Configuration 2(Port 5/6)
- 0 = Port 5 (x2)
- 1 = Port 5 (x1), Port 6(x1) (D)

GNT3# : A16 Swap override strip
- 0 = Enable
- 1 = Default (D)





USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	eSATA/USB
USB 4	NewCard
USB 5	Camera
USB 6	Bluetooth
USB 7	3G Card
USB 8	Fingerprint
USB 9	TV Tuner

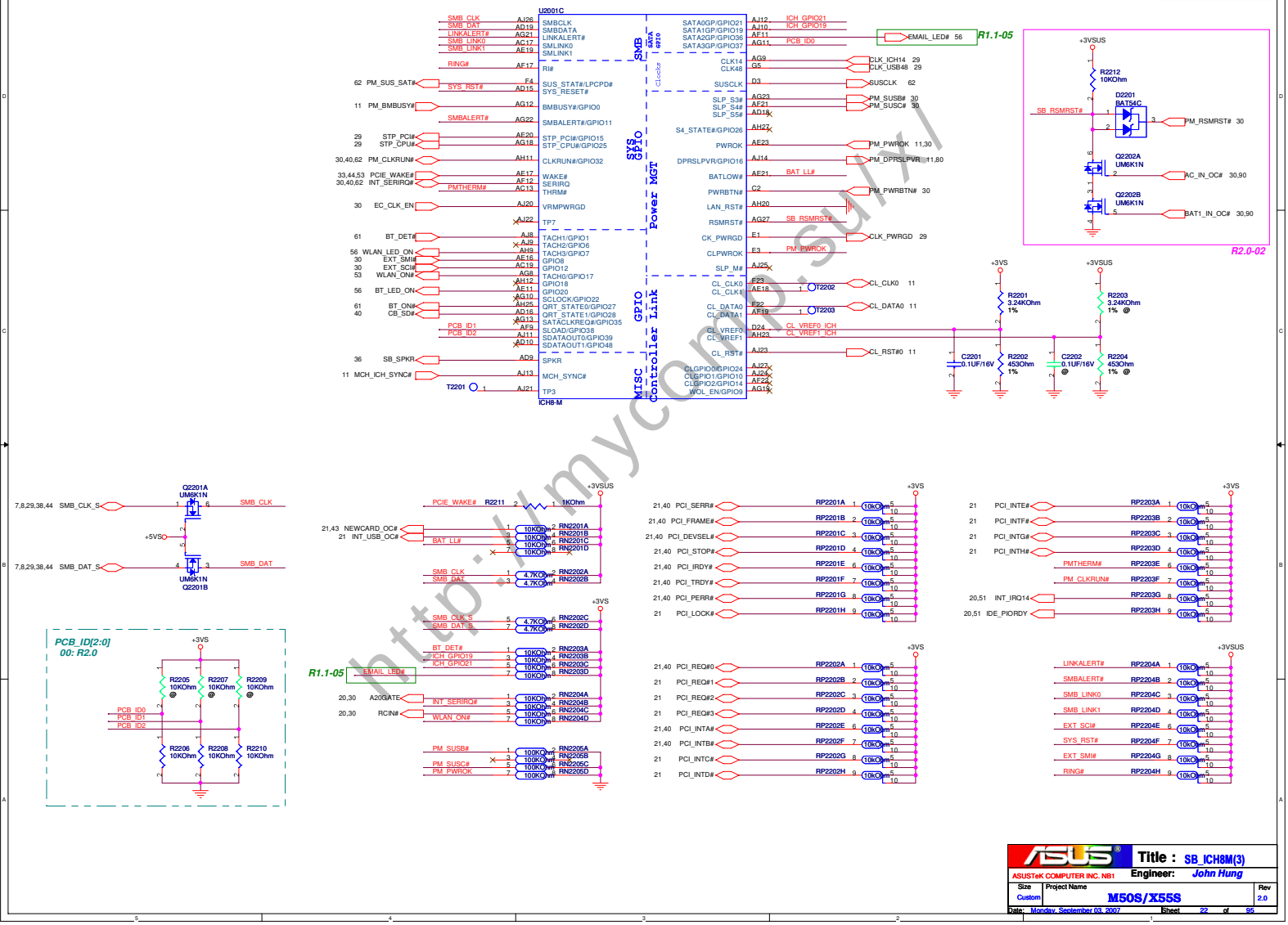
ASUSTeK COMPUTER INC. NB1

Title : SB_ICH8M(2)

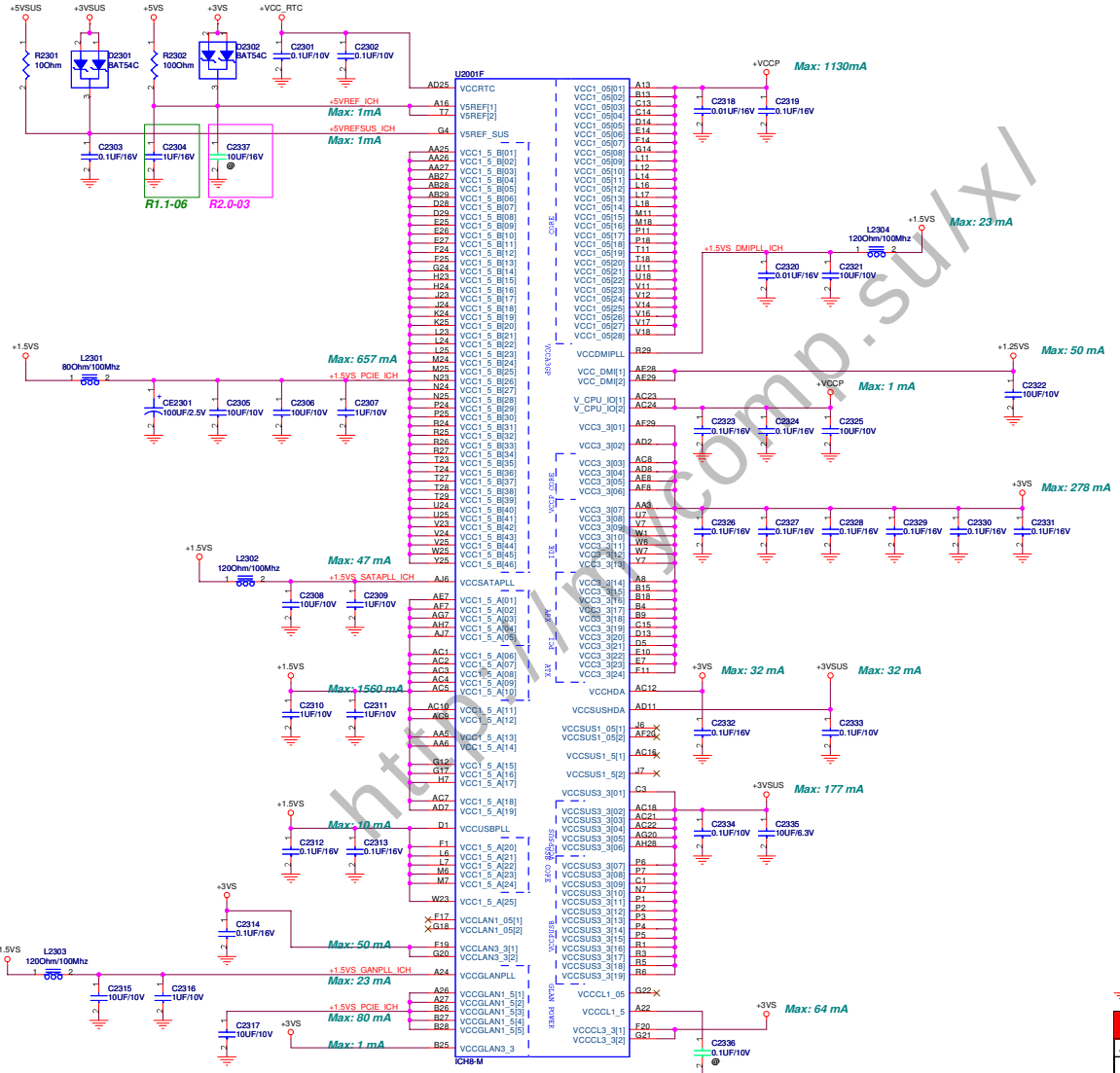
Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0

Date: Monday, September 03, 2007 Sheet 21 of 95



ASUSTeK COMPUTER INC. NB1	Title : SB_ICH8M(3)	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 22 of 95	



ASUSTeK COMPUTER INC. NB1

Title : SB_ICH8M(PWR)

Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0

Date: Monday, September 03, 2007 Sheet 23 of 95

ASUSTeK COMPUTER INC. NB1	Title : SB_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 24 of 95		

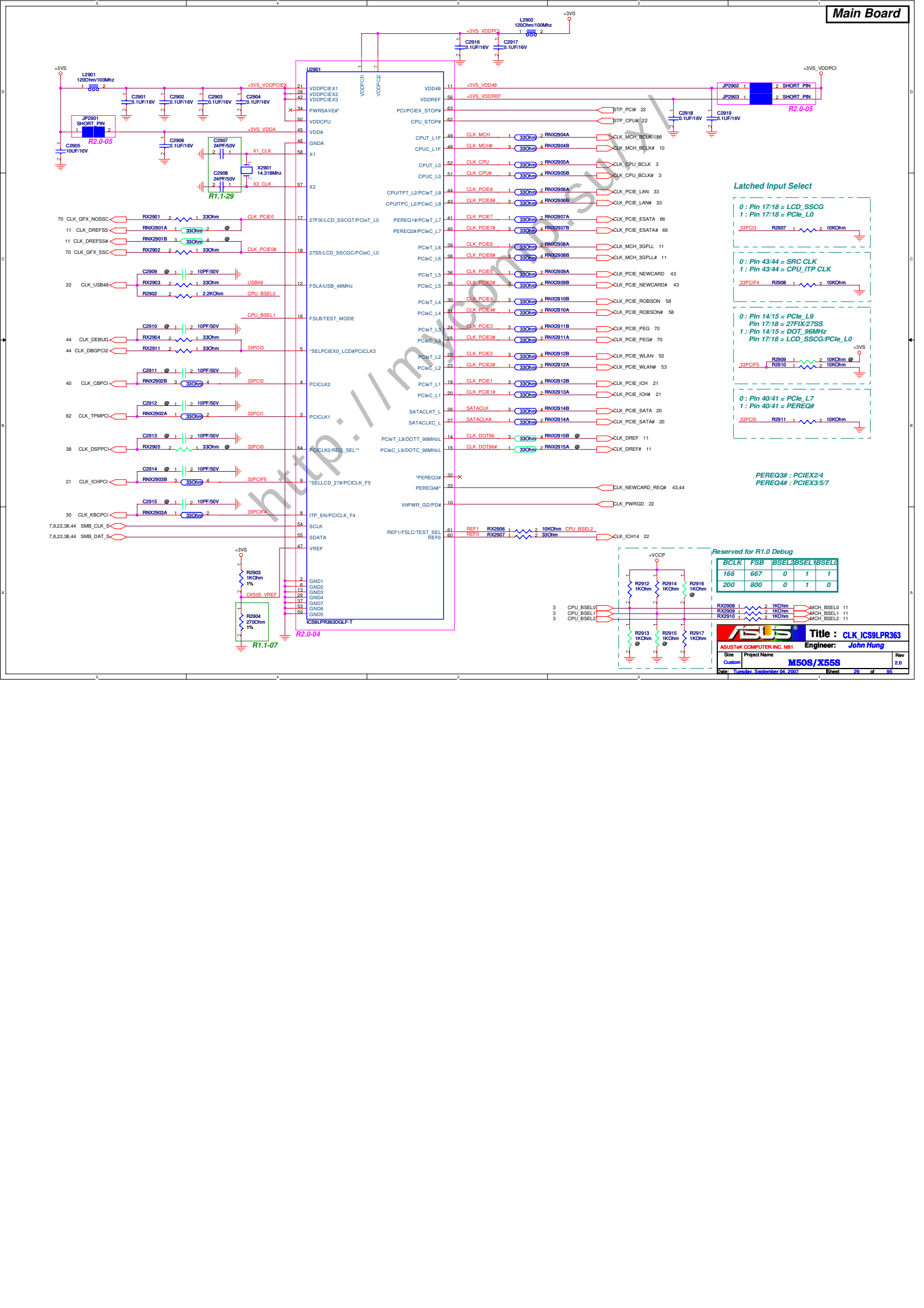
ASUSTeK COMPUTER INC. NB1	Title : SB_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 25 of 95	

ASUSTeK COMPUTER INC. NB1	Title : SB_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 28 of 95		

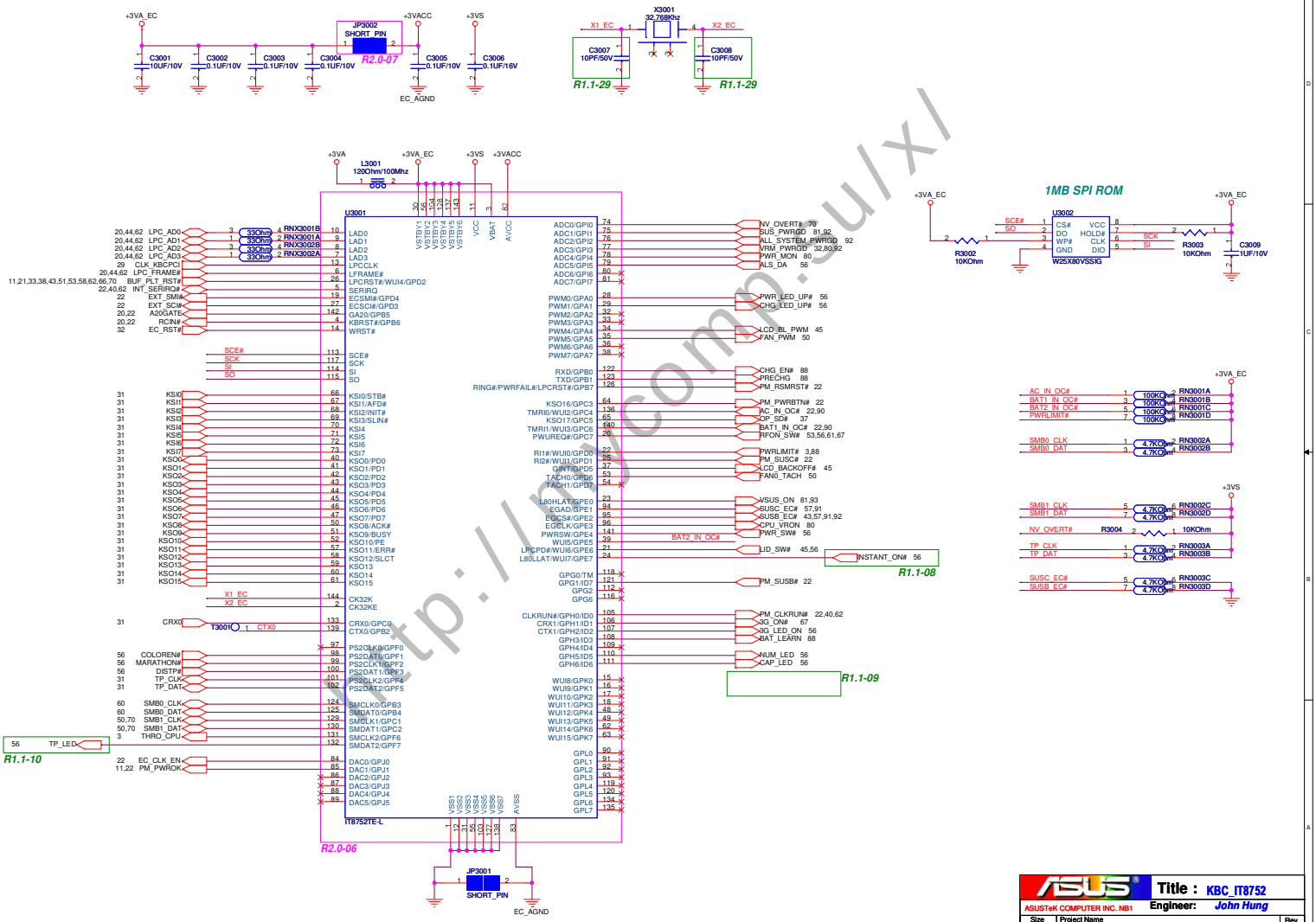
Main Board

ASUSTeK COMPUTER INC. NB1	Title : SB_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 27 of 95	

ASUSTeK COMPUTER INC. NB1	Title : SB_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 28 of 95		

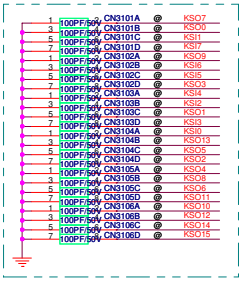


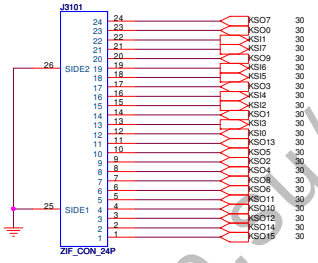
Main Board



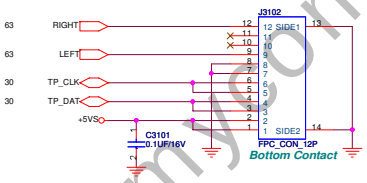
Keyboard

EMI

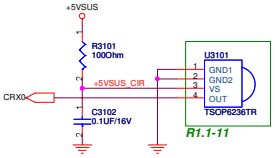


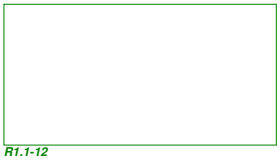


Touchpad

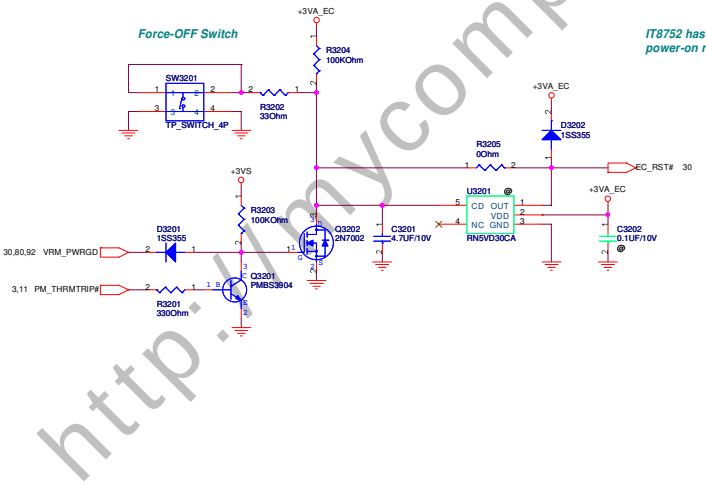


CIR

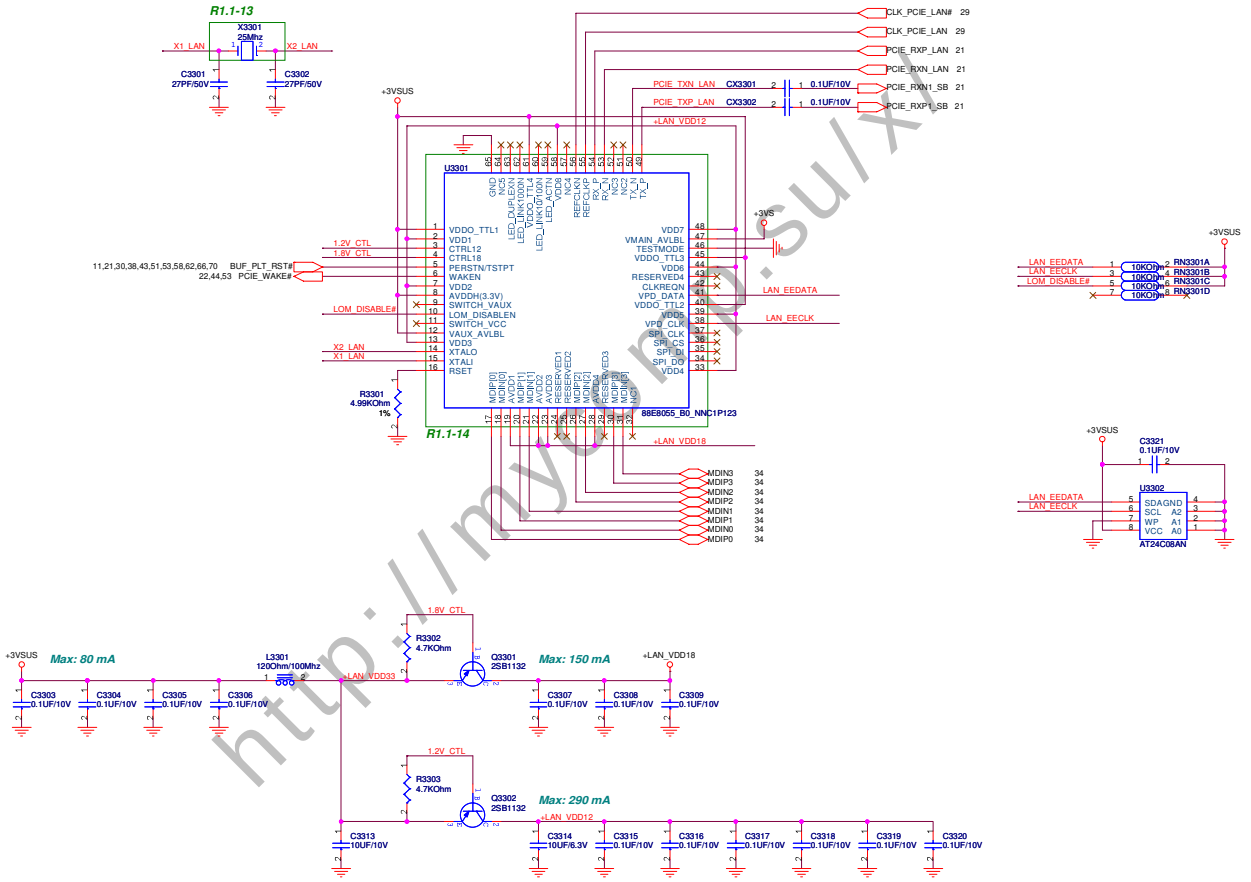




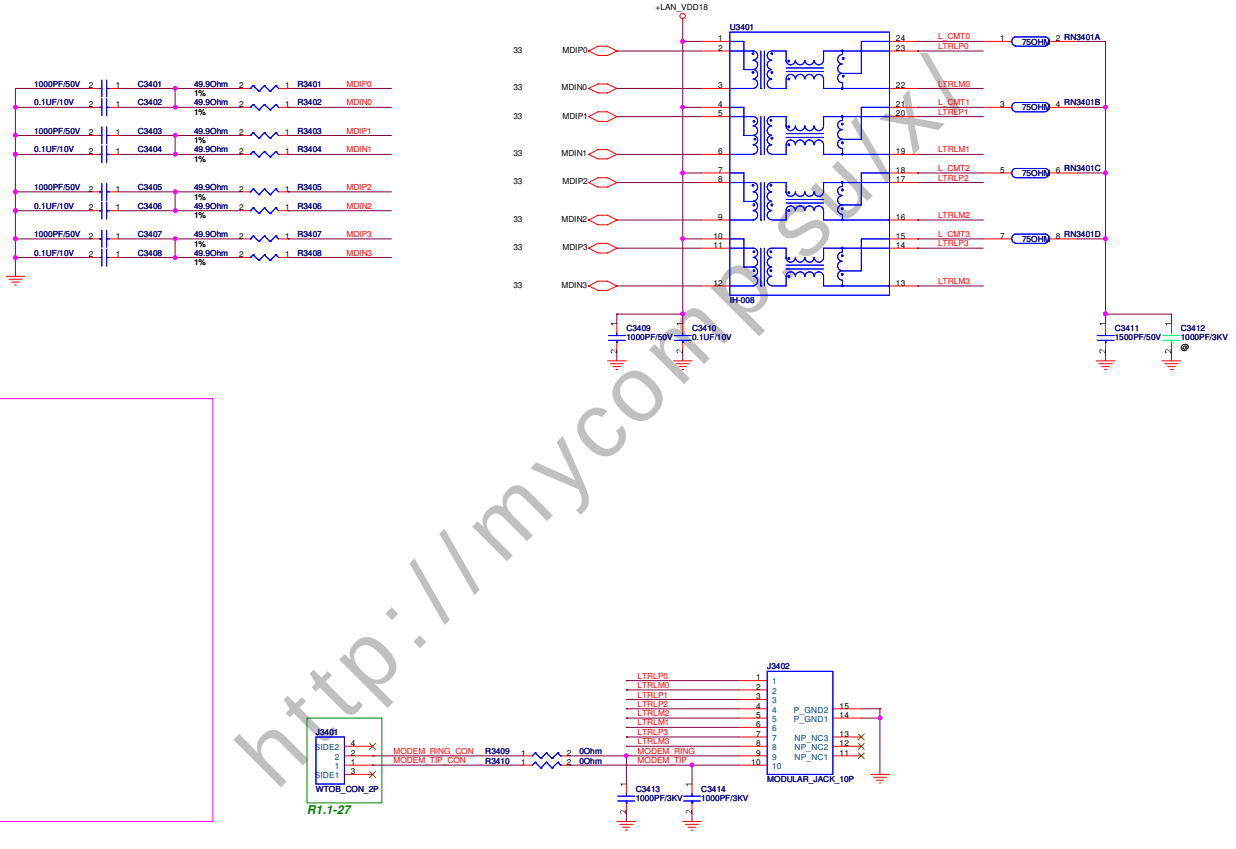
ASUSTeK COMPUTER INC. NB1	Title : KBC_KB, TP & CIR	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 31 of 95	



ASUSTeK COMPUTER INC. NB1	Title : RST_Reset Circuit	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 32 of 95	

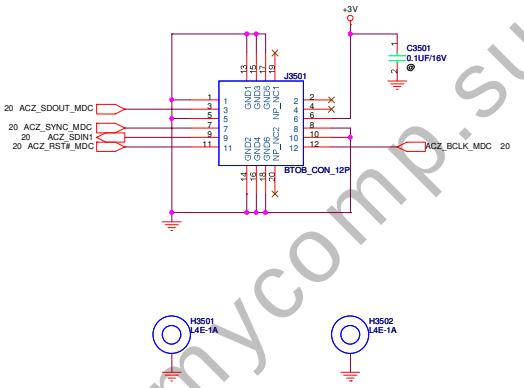


ASUSTeK COMPUTER INC. NB1	Title : LAN_88E8055	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 33 of 95	



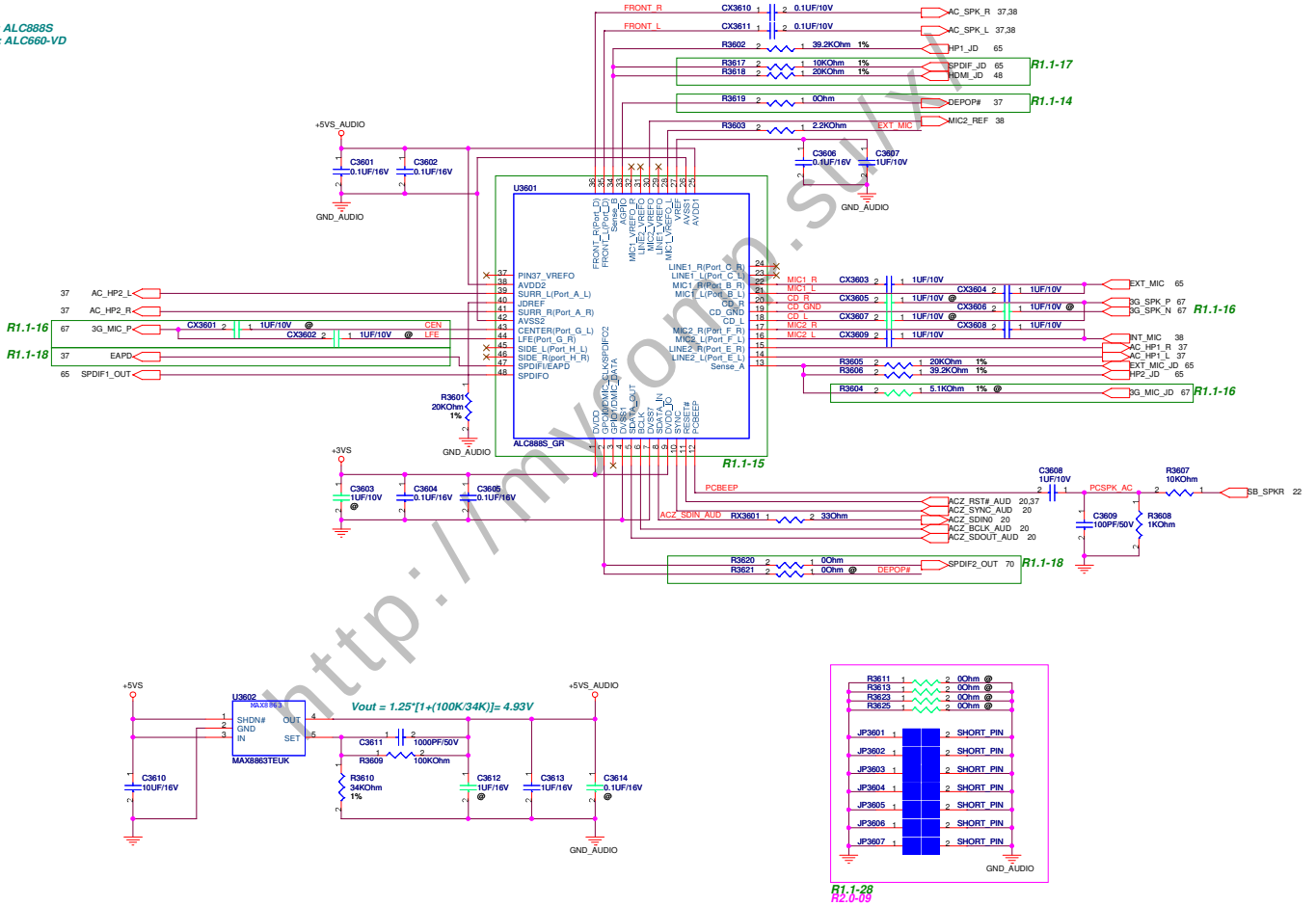
R1.1-28
R2.0-08

ASUSTeK COMPUTER INC. NB1	Title : LAN_RJ45 & RJ11		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 34 of 95		

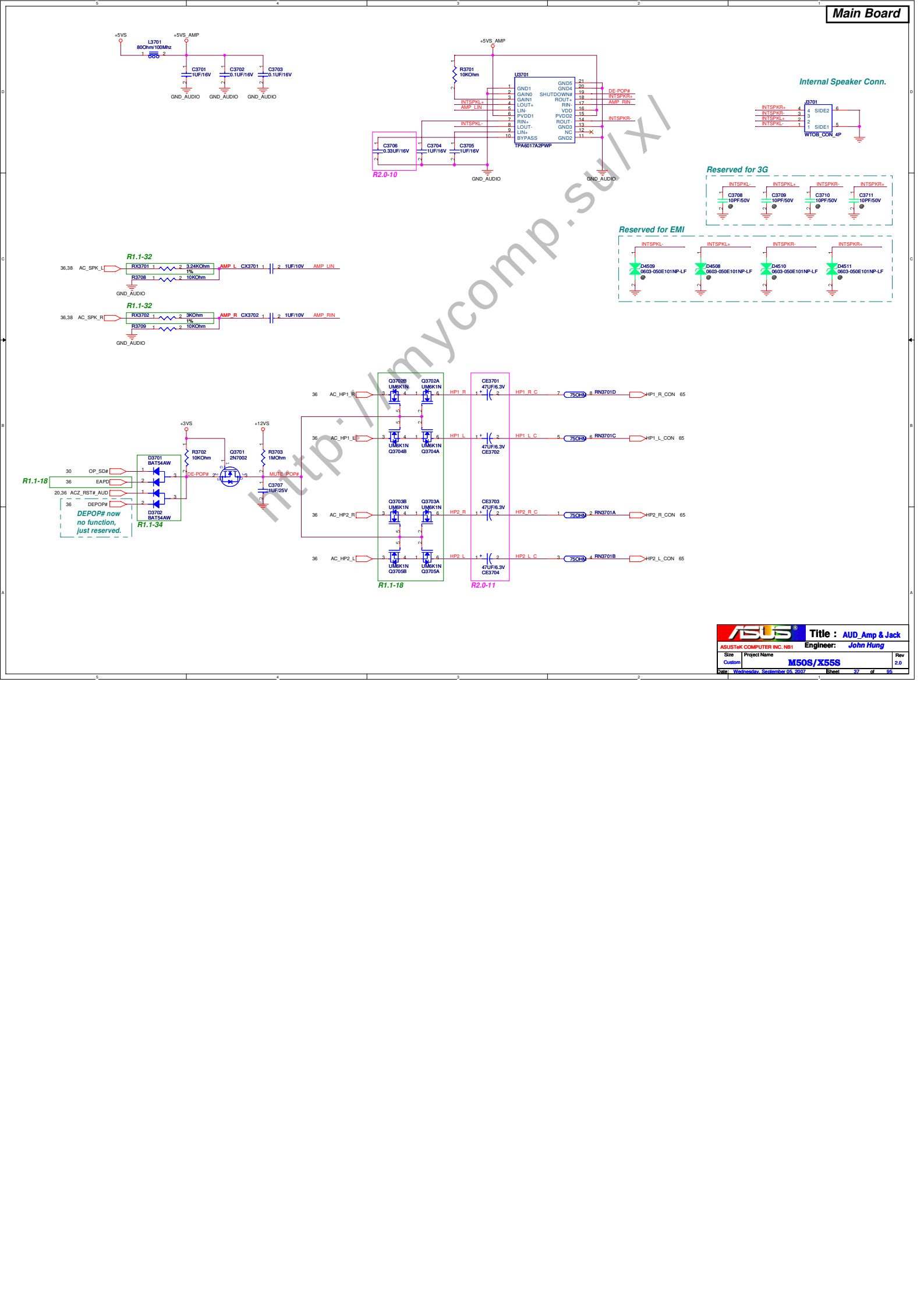


ASUSTeK COMPUTER INC. NB1	Title : LAN_MDC	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 35 of 95	

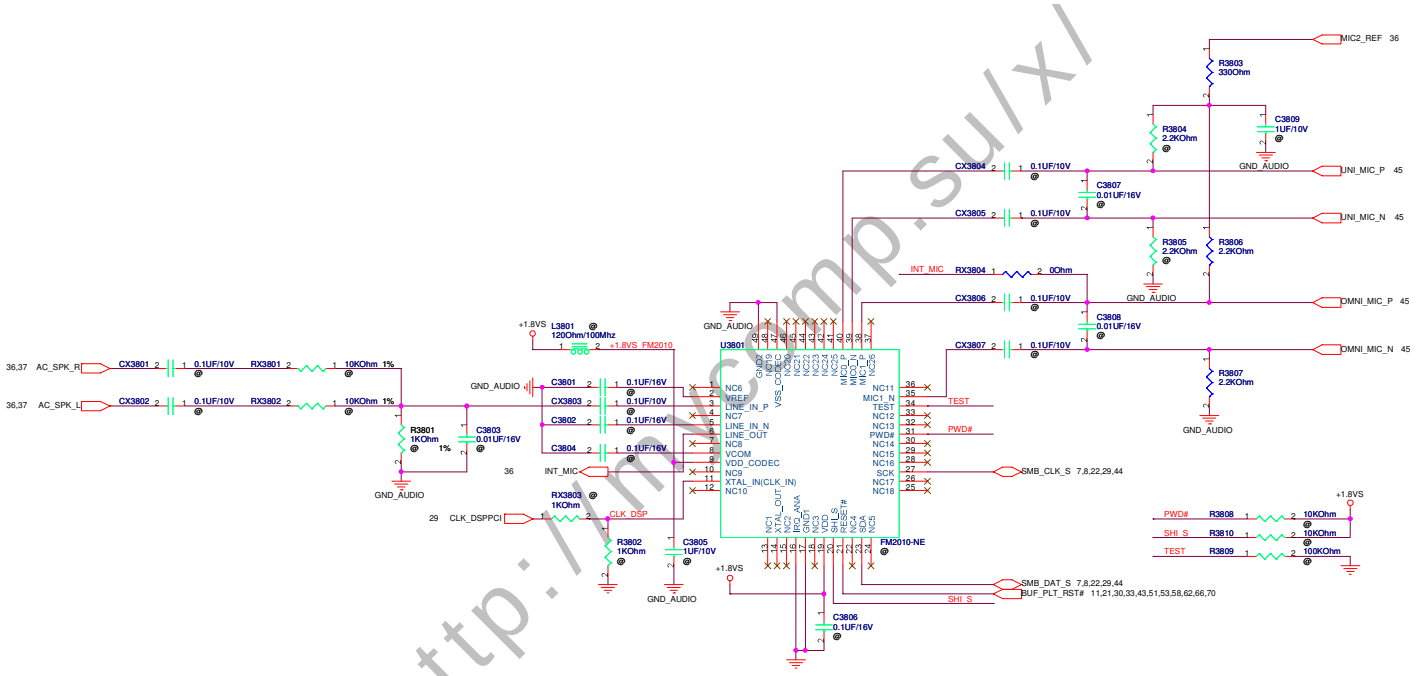
PM: ALC888S
GM: ALC660-VD



ASUSTeK COMPUTER INC. NB1	Title : AUD_ALC888S	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 38 of 95	

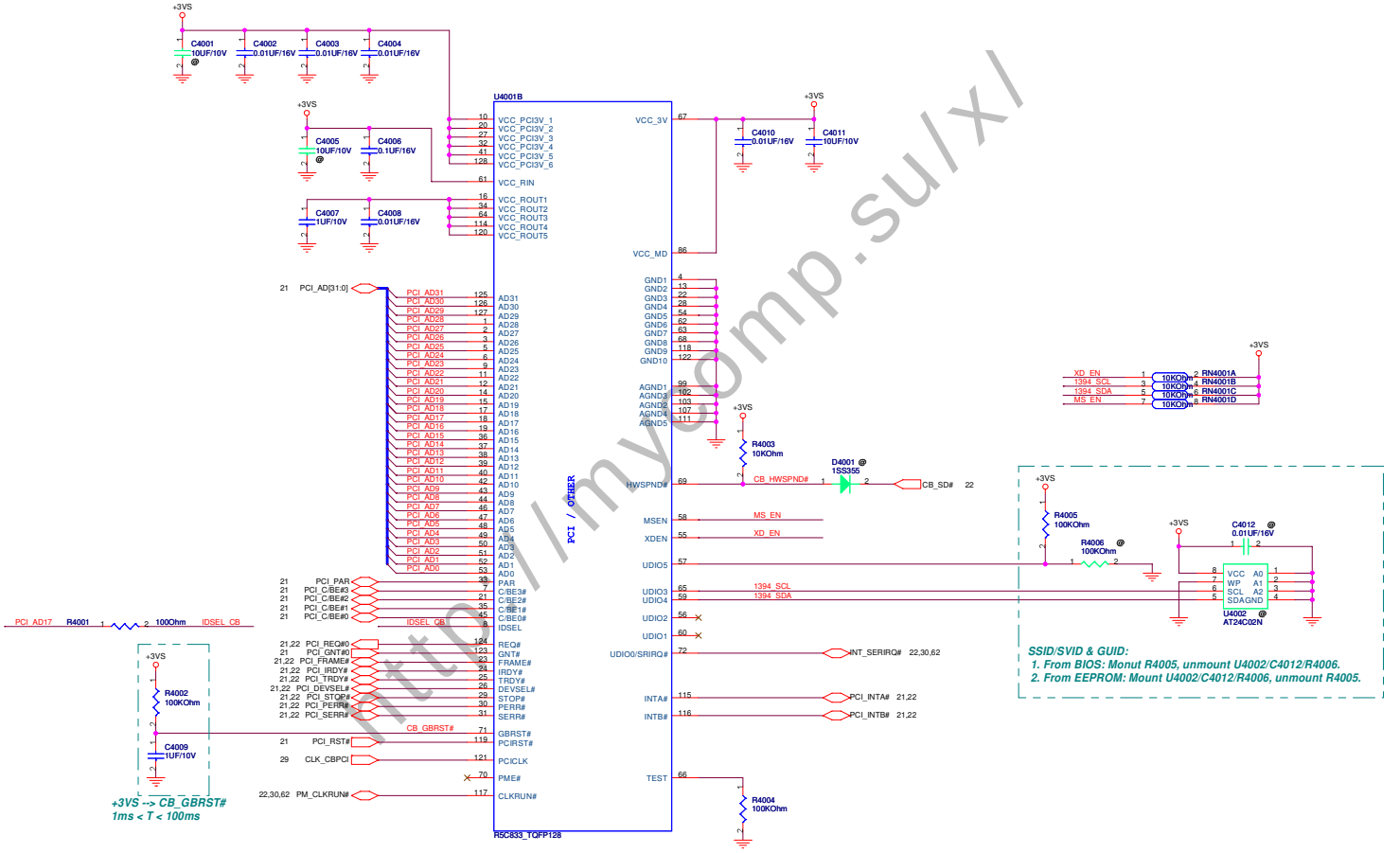


ASUSTeK COMPUTER INC. NB1	Title : AUD_Amp & Jack	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Wednesday, September 05, 2007	Sheet 37 of 95	

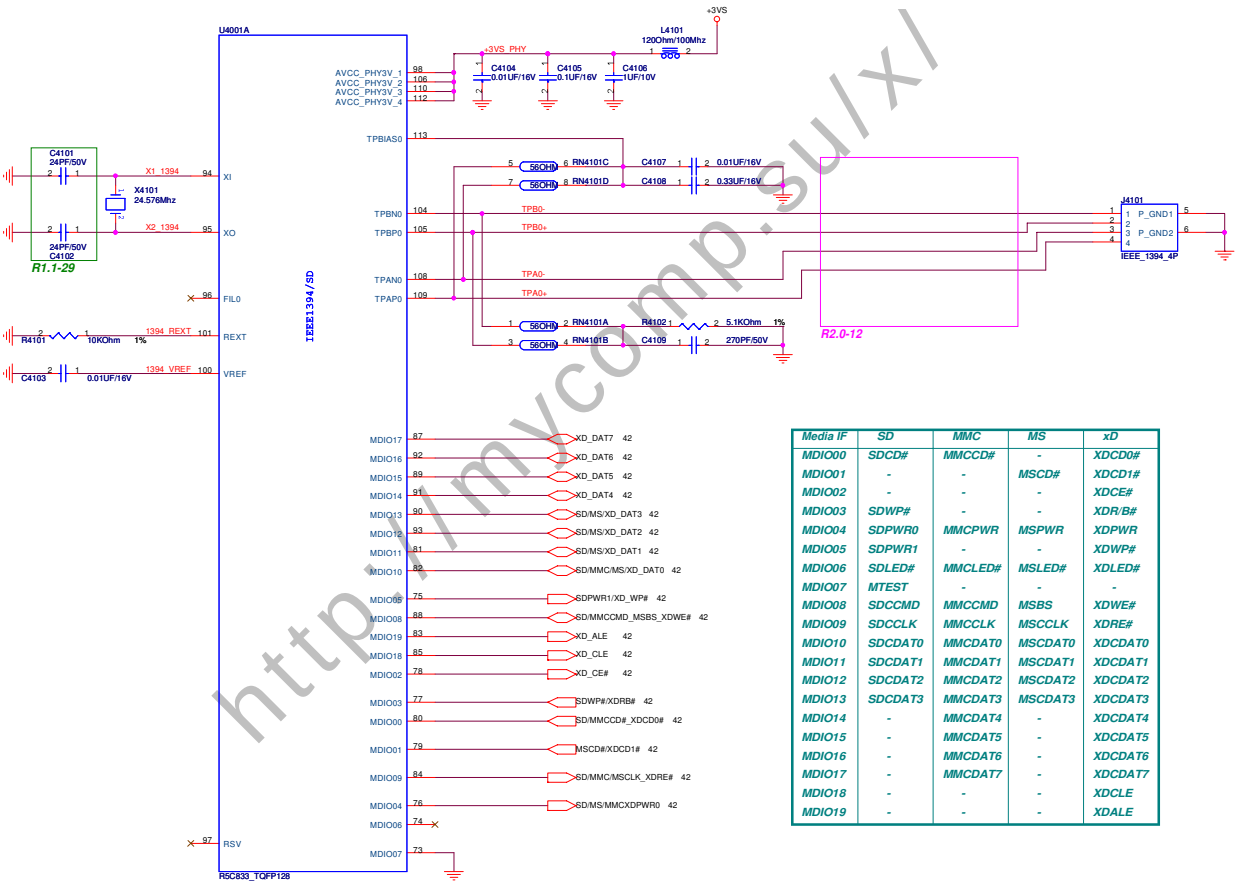


ASUSTeK COMPUTER INC. NB1	Title : AUD_FM2010		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Tuesday, September 04, 2007	Sheet 38 of 95		

ASUSTeK COMPUTER INC. NB1	Title : AUD_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 39 of 95		



ASUSTeK COMPUTER INC. NB1	Title : CB_R5C833		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 40 of 95		



Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XDPWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLED#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XDCLE
MDIO19	-	-	-	XDALE

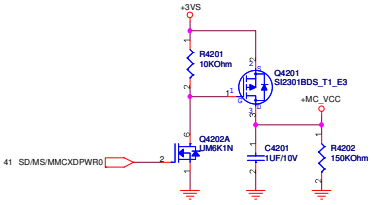
ASUSTeK COMPUTER INC. NB1

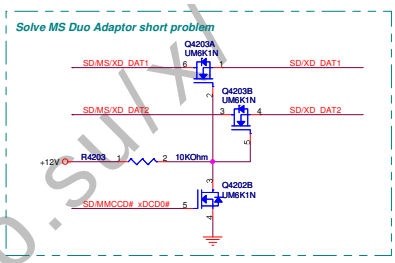
Title : CB_R5C833

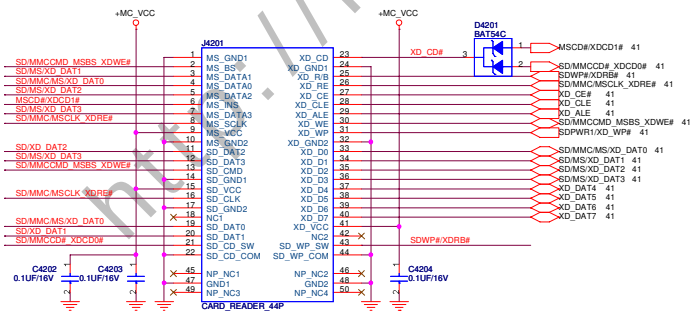
Engineer: John Hung

Size: Custom | Project Name: M50S/X55S | Rev: 2.0

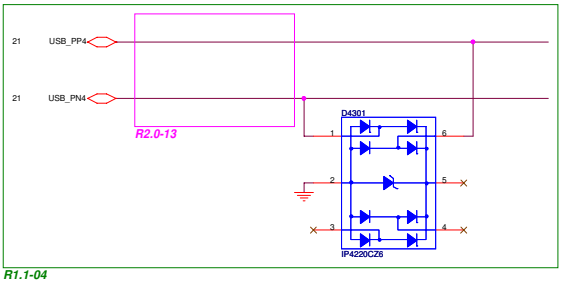
Date: Monday, September 03, 2007 | Sheet 41 of 95

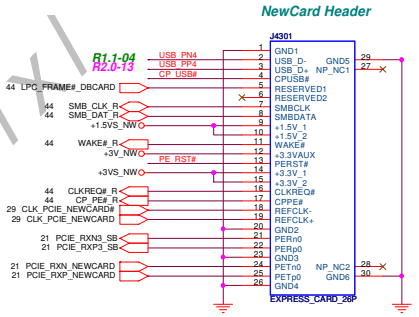


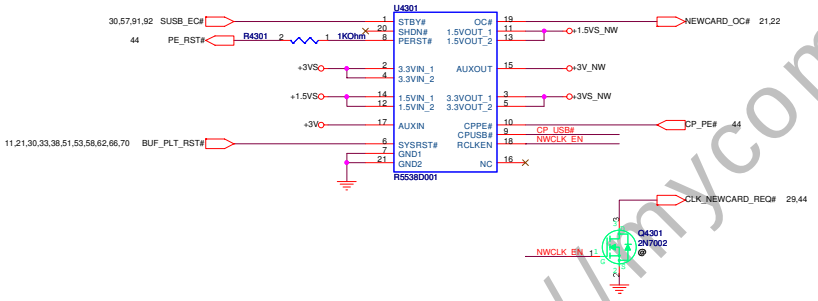


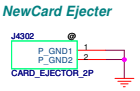


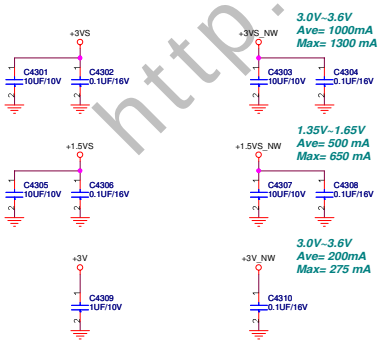
ASUSTeK COMPUTER INC. NB1	Title : CB_4in1 CardReader	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 42 of 95	





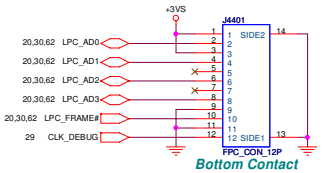






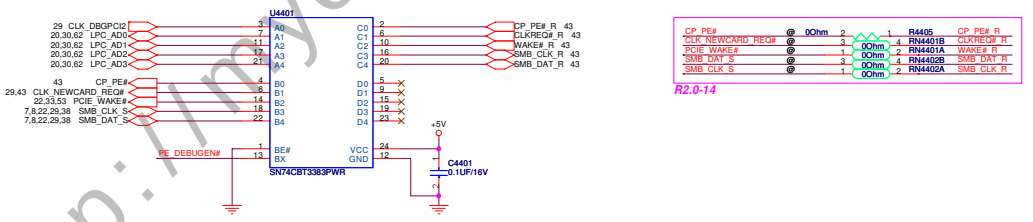
ASUSTeK COMPUTER INC. NB1	Title : CB_NewCard	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 43 of 95	

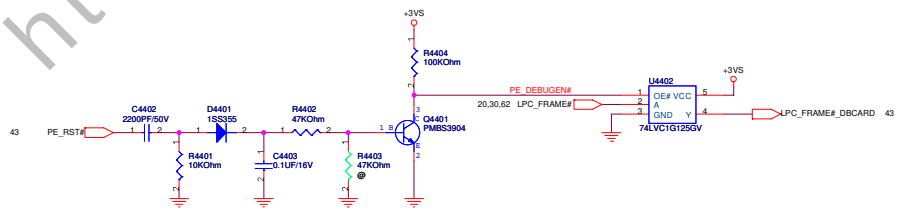
LPC Debug Port



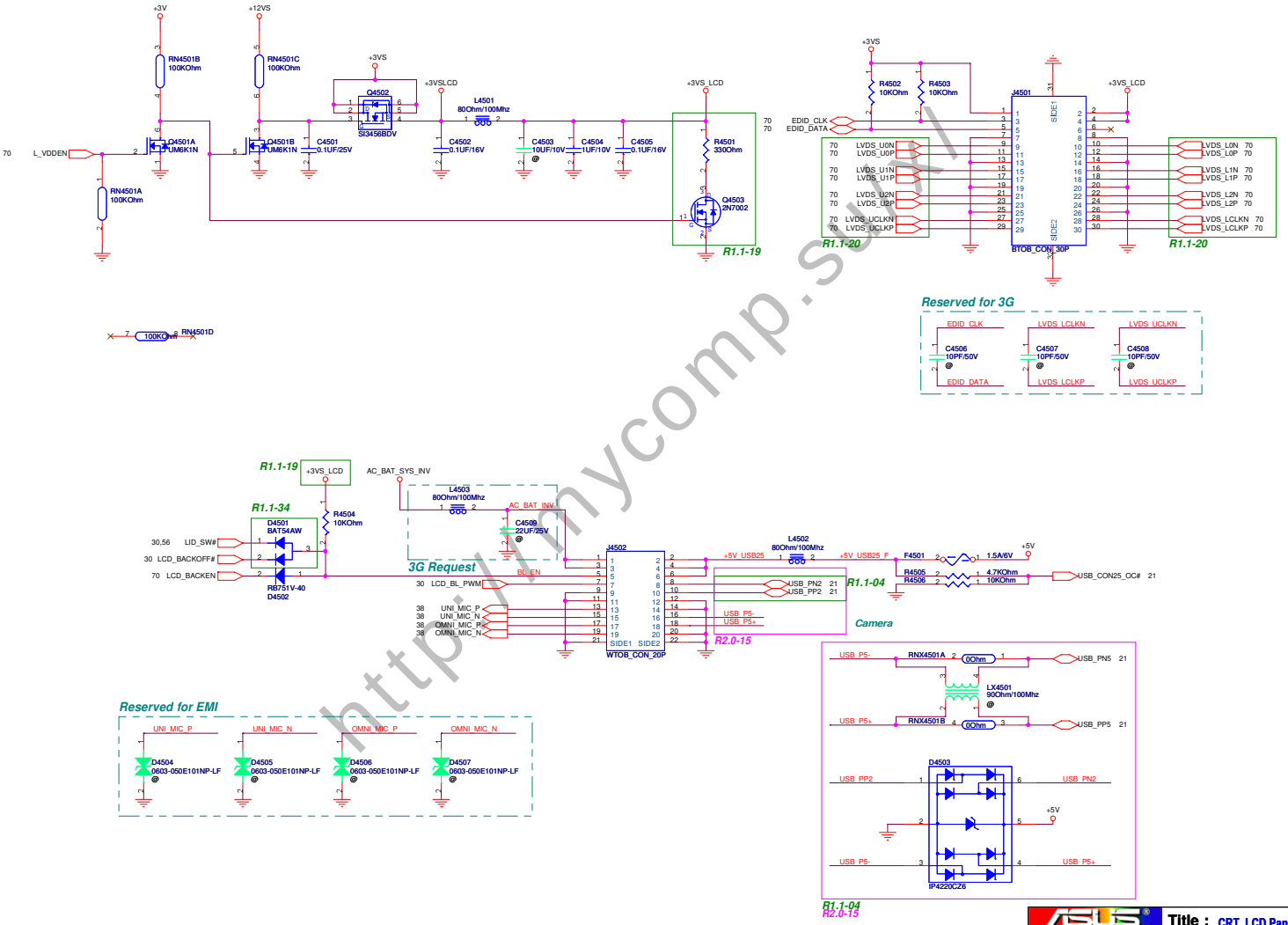
Bottom Contact

For NewCard Debug Card

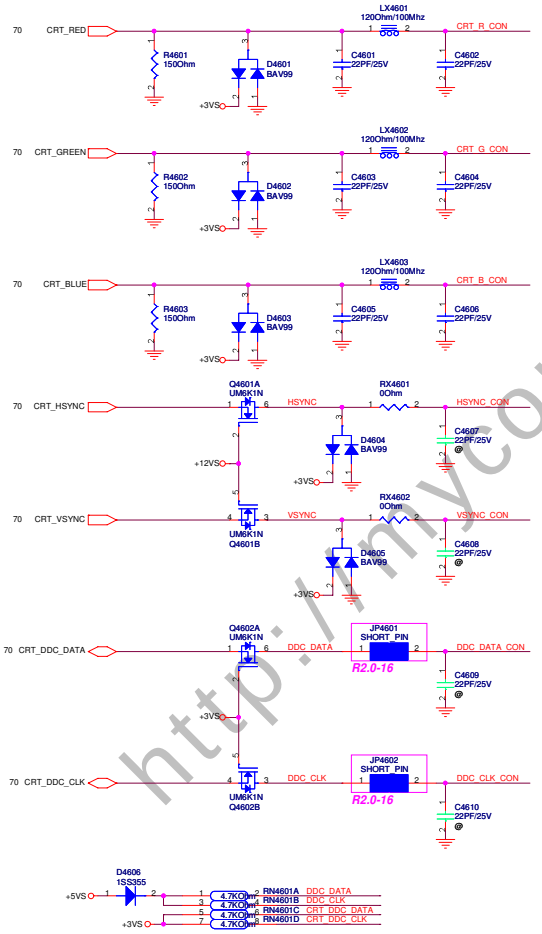


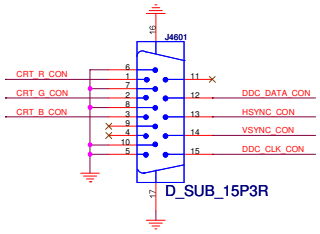


ASUSTeK COMPUTER INC. NB1	Title : BUG_LPC Debug		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 44 of 95		

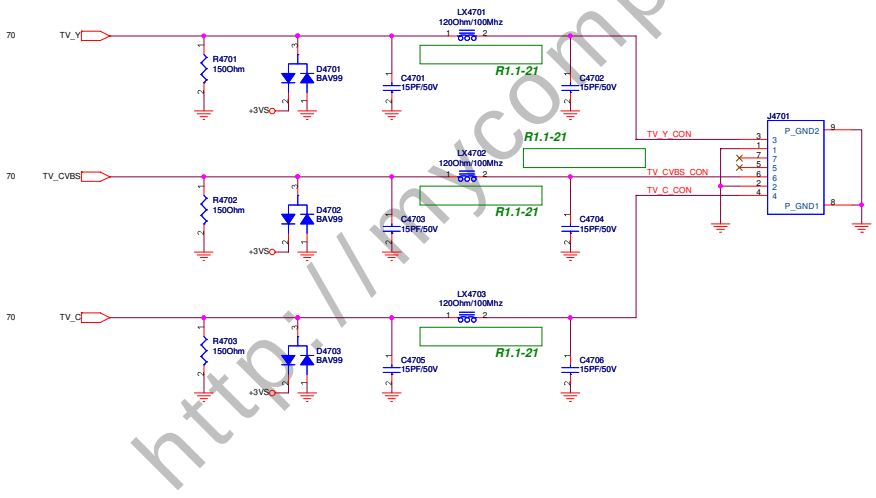


ASUSTeK COMPUTER INC. NB1	Title : CRT_LCD Panel		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 45 of 95		

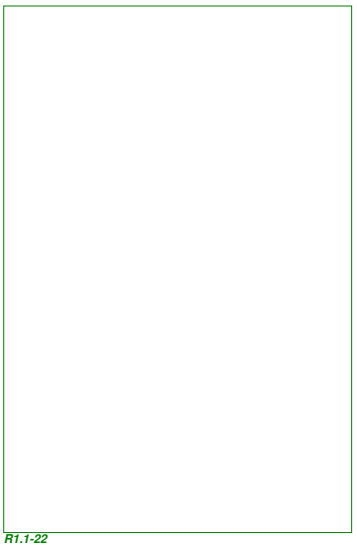


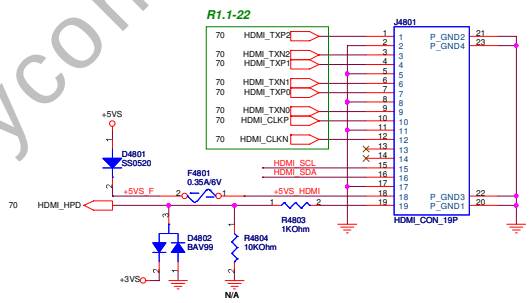


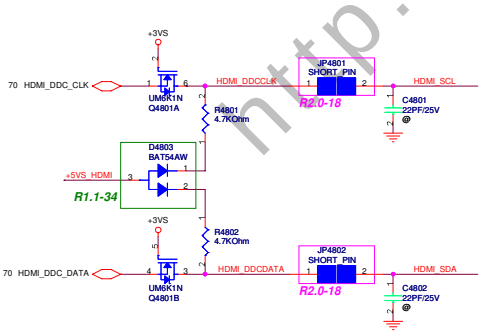
ASUSTeK COMPUTER INC. NB1	Title : CRT_D-Sub		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 46 of 95		

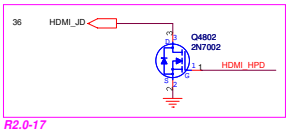


ASUSTeK COMPUTER INC. NB1	Title : TV_TV-Out	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 47 of 95	





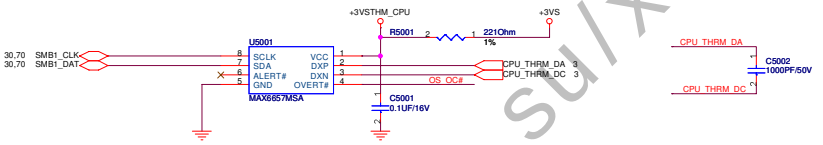




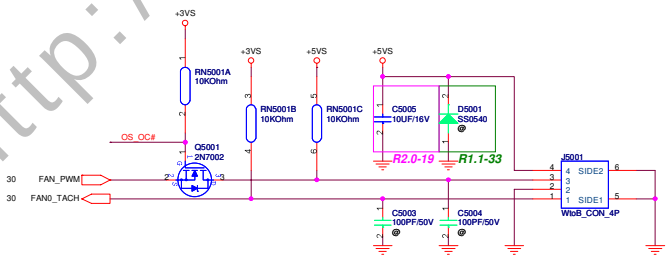
ASUSTeK COMPUTER INC. NB1	Title : CRT_HDMI	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 48 of 95	

ASUSTeK COMPUTER INC. NB1	Title : TV_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 49 of 95		

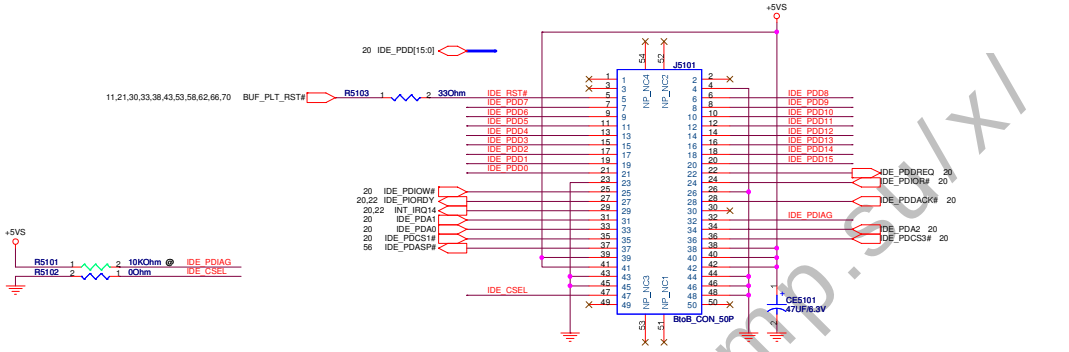
CPU Thermal Sensor

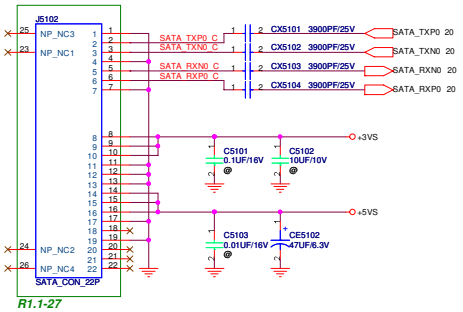


PWM Fan



ASUSTeK COMPUTER INC. NB1	Title : FAN_Fan & Sensor	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 50 of 95	

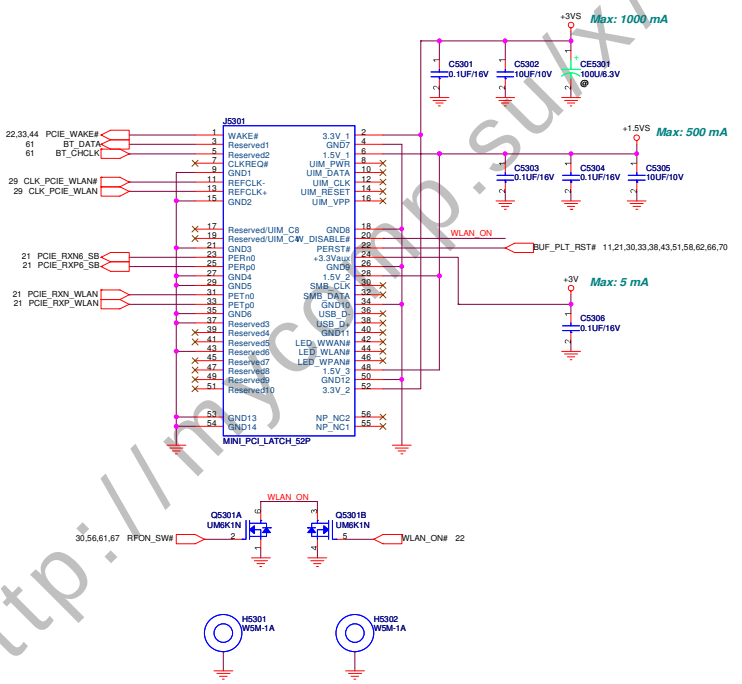




R1.1-27

ASUSTeK COMPUTER INC. NB1	Title : XDD_HDD & ODD		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 51 of 95		

ASUSTeK COMPUTER INC. NB1	Title : USB_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 52 of 95		

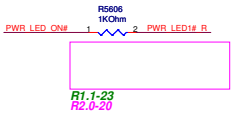


ASUSTeK COMPUTER INC. NB1	Title : PCI_WLAN	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Tuesday, September 04, 2007	Sheet 53 of 95	

ASUSTeK COMPUTER INC. NB1	Title : BAR_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 54 of 95		

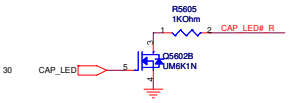
ASUSTeK COMPUTER INC. NB1	Title : SIO_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 55 of 95		

Power LED

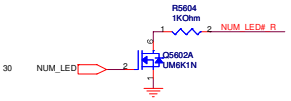


R1.1-23
R2.0-20

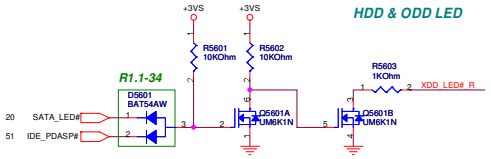
Cap Lock LED



Num Lock LED

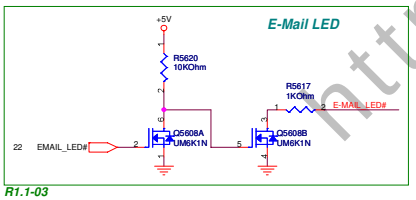


HDD & ODD LED



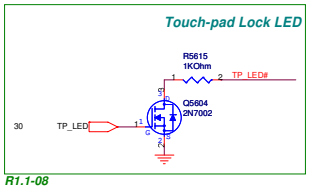
R1.1-34

E-Mail LED

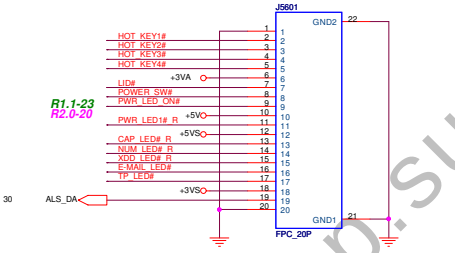


R1.1-03

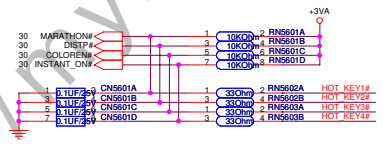
Touch-pad Lock LED

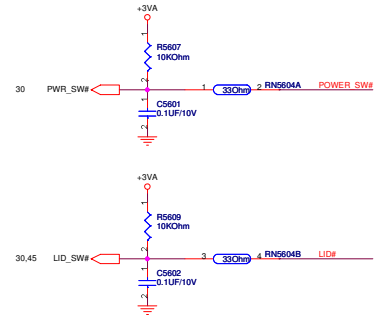


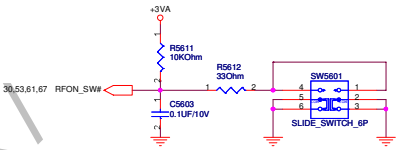
R1.1-08



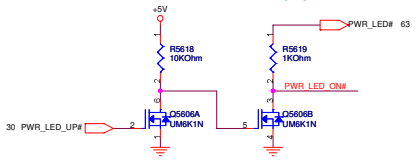
R1.1-23
R2.0-20



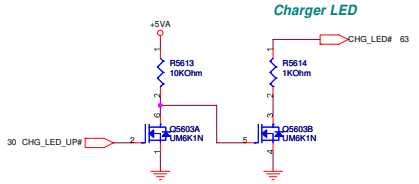




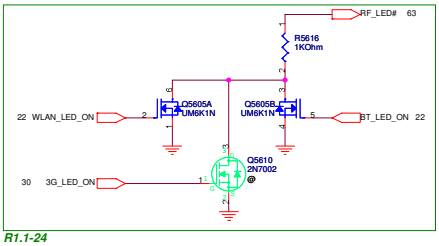
Power LED



Charger LED



WLAN LED



R1.1-24

ASUSTeK COMPUTER INC. NB1	Title : LED_Indicator	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
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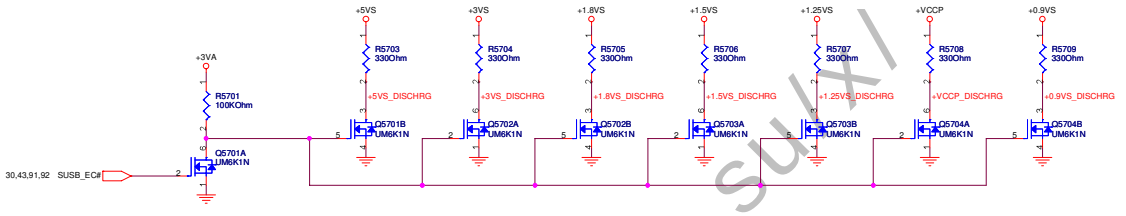
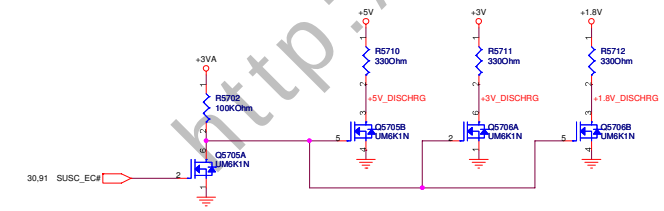
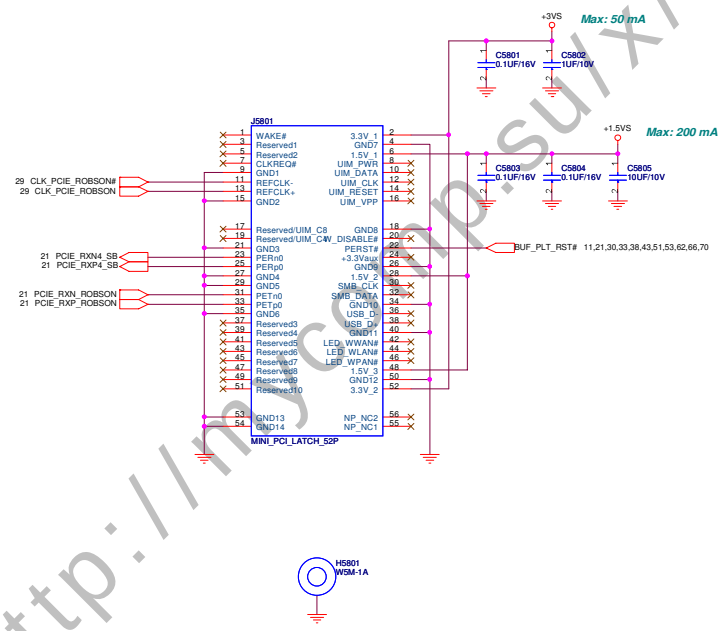




ASUSTeK COMPUTER INC. NB1	Title : DSG_Discharge	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 57 of 95	

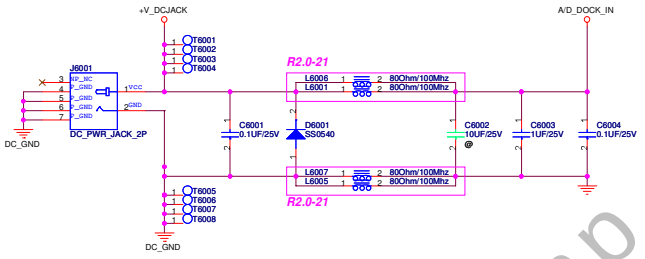


ASUSTeK COMPUTER INC. NB1	Title : ROB_Robson	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 58 of 95	

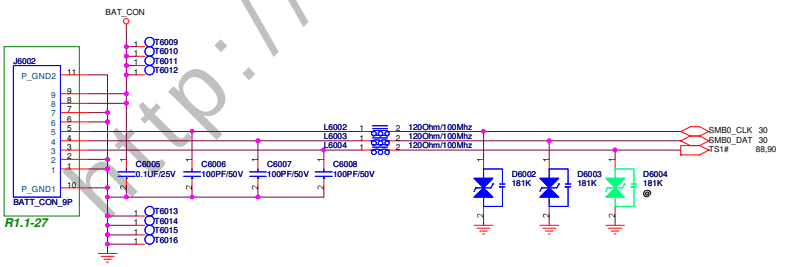
Main Board

ASUSTeK COMPUTER INC. NB1	Title : DJ_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 59 of 95	

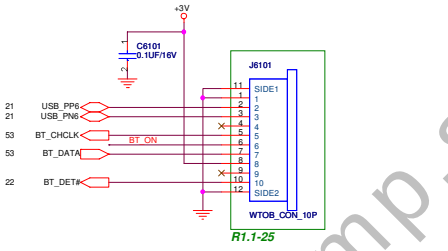
DC Jack



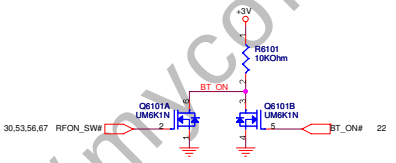
Battery Connector



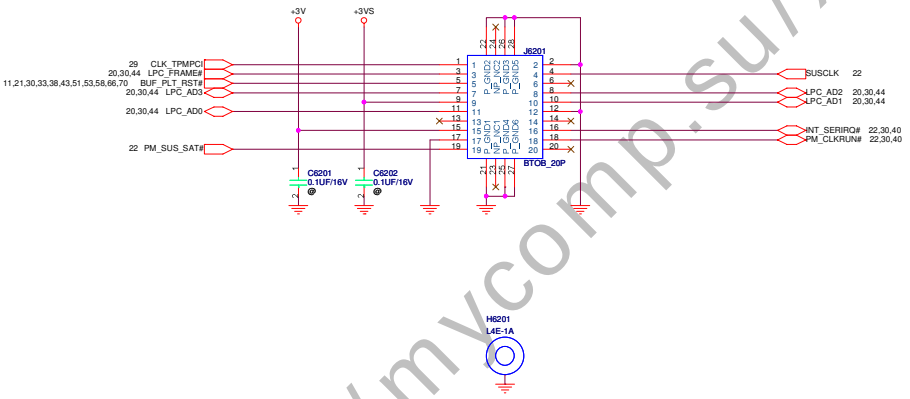
ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 60 of 95	



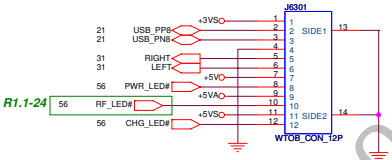
R1.1-25



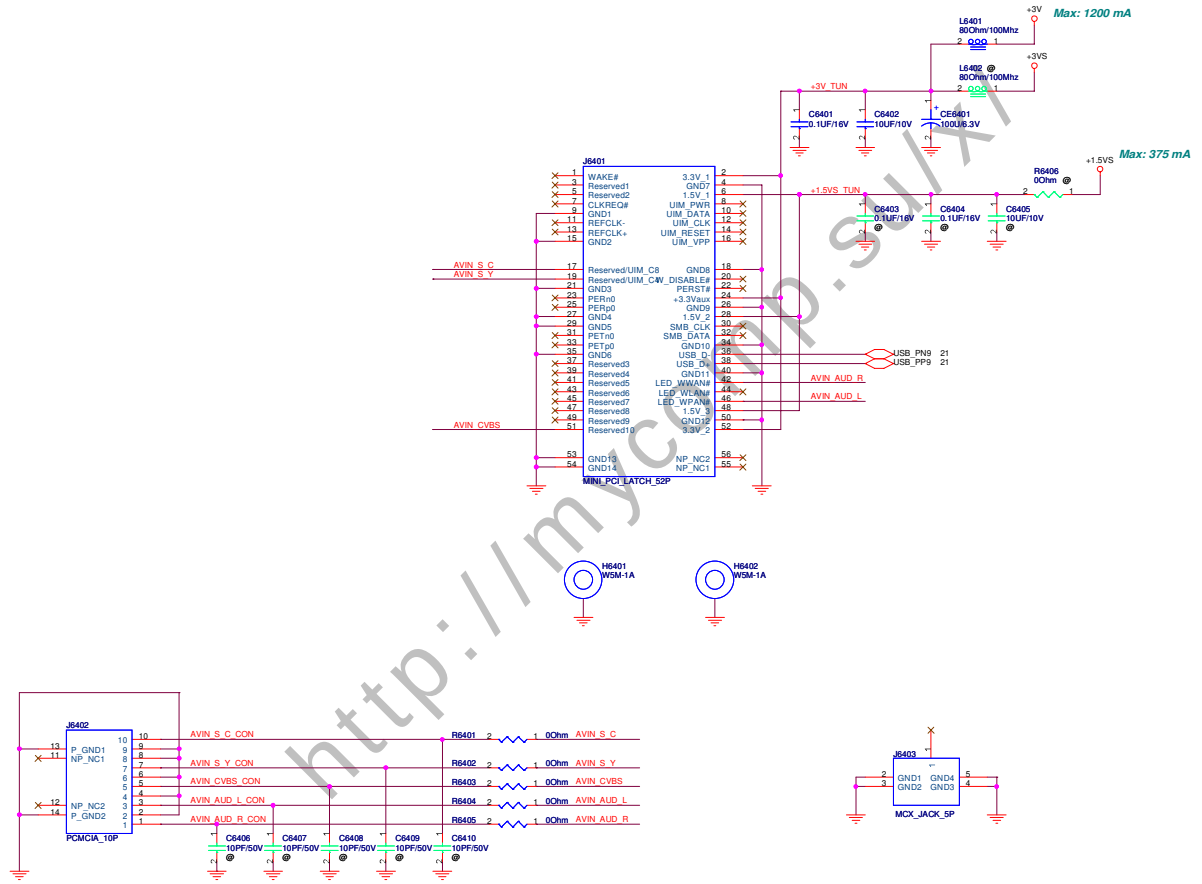
ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 61 of 95	



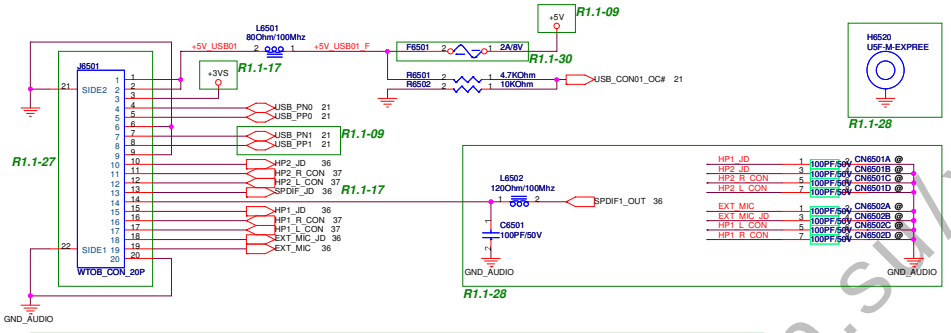
ASUSTeK COMPUTER INC. NB1	Title : TPM_TPM 1.2	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 62 of 95	

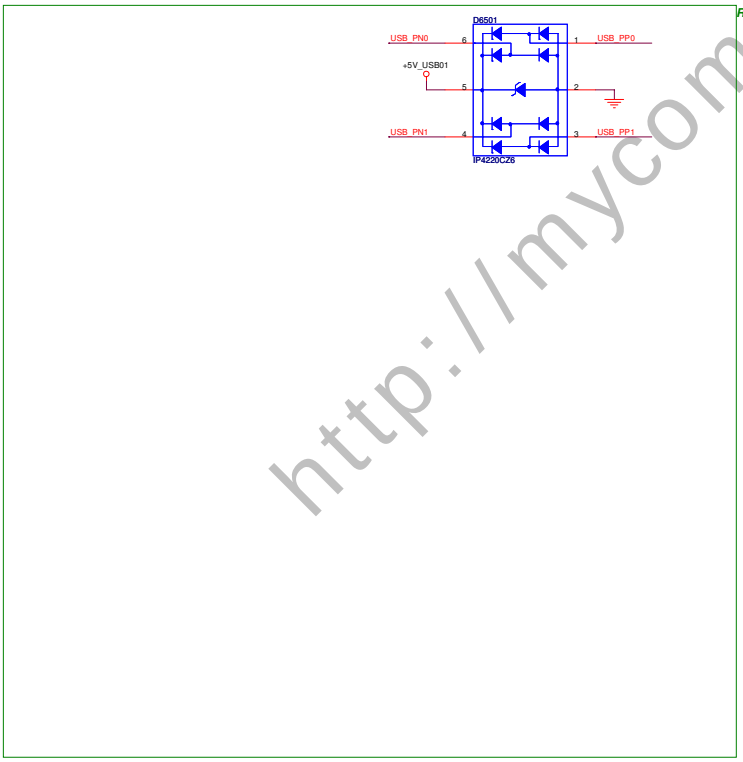


ASUSTeK COMPUTER INC. NB1	Title : FP_Fingerprint Conn.	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 63 of 95	

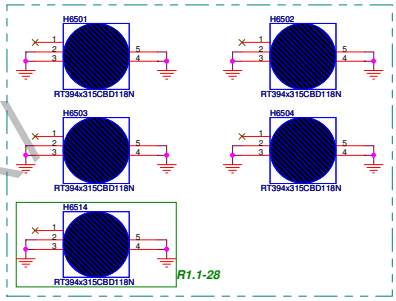


ASUSTeK COMPUTER INC. NB1	Title : TUN_TV Tuner	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Tuesday, September 04, 2007	Sheet 64 of 95	

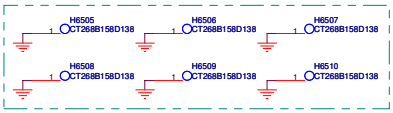




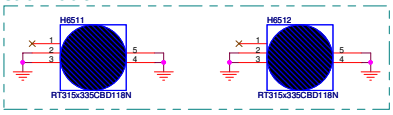
Screw Hole A



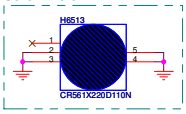
Screw Hole B



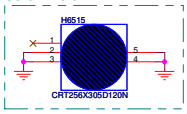
Screw Hole C



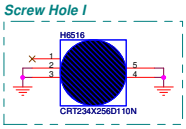
Screw Hole F



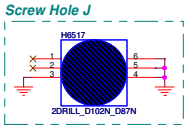
Screw Hole H



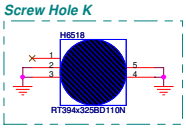
Screw Hole I



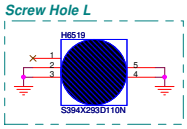
Screw Hole J



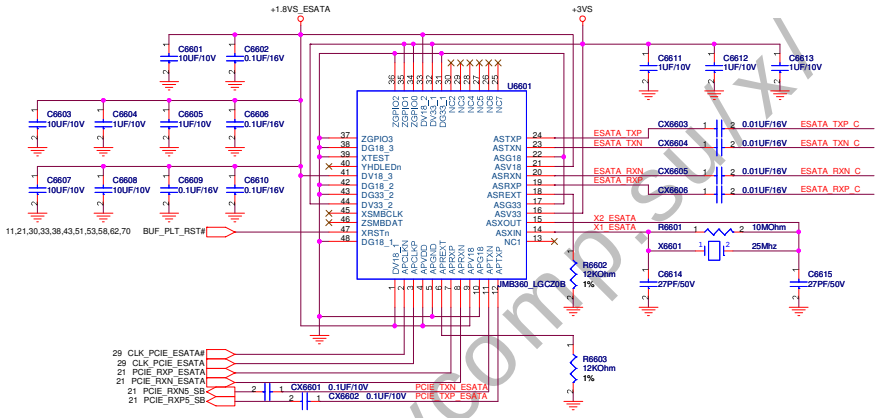
Screw Hole K



Screw Hole L



ASUSTeK COMPUTER INC. NB1	Title : ME_Conn & Screw Holes	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 65 of 95	

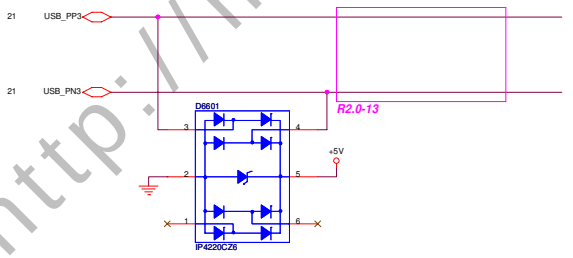


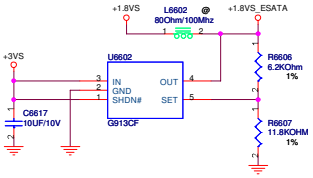
ZGPIO : Clock Type of PCI Express
0 = 25MHz Oscillator (D)
1 = 100MHz from PCI Express Finger

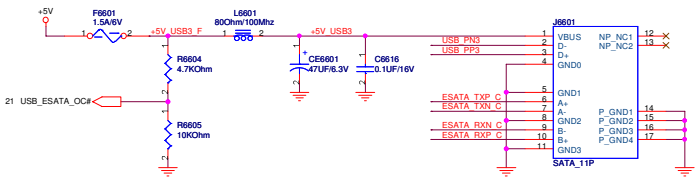
ZGPI1 : Clock Source of SATA II
0 = from Internal Clock Source (D)
1 = from ASXIN & ASXOUT

ZGPI2 : Interface to Debug Registers
0 = SMBus I/F (D)
1 = Reserved

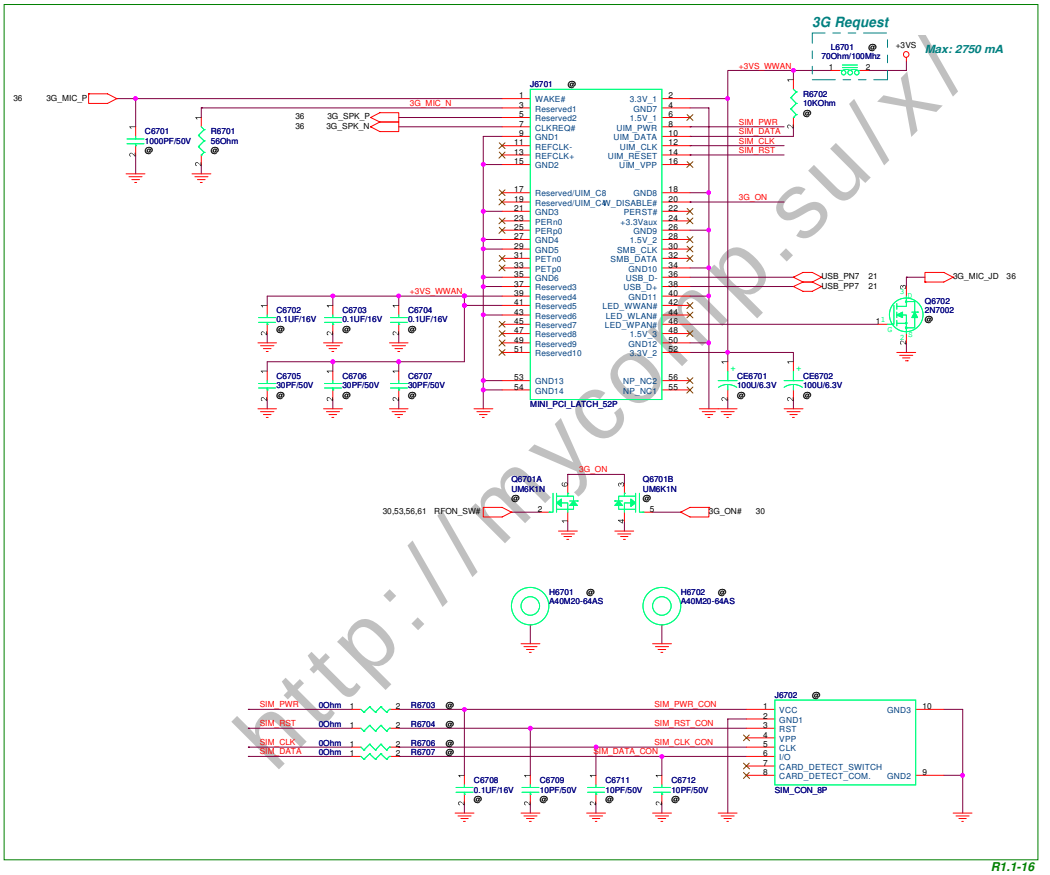
ZGPI2 : SMBus ID Address
0 = 8'h44 (D)
1 = 8'h4A







Title : ESA_JMB360		
ASUSTeK COMPUTER INC. NB1	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 66 of 95	



R1.1-16

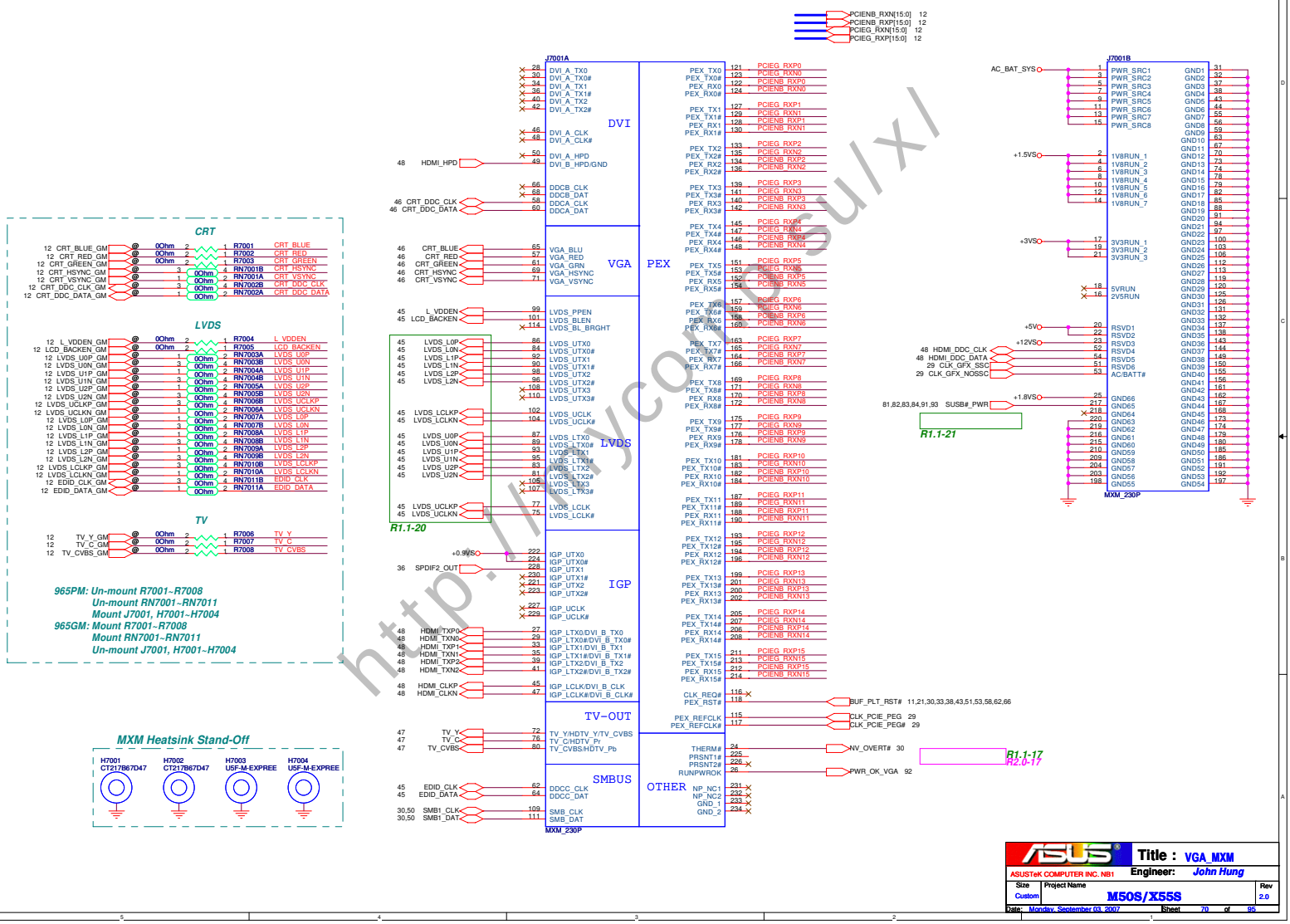
ASUSTeK COMPUTER INC. NB1	Title : WAN_WWAN	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 67 of 95	

R1.1-26

ASUSTeK COMPUTER INC. NB1	Title : OTH_****	
	Engineer: John Hung	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 68 of 95	

Main Board

ASUSTeK COMPUTER INC. NB1	Title : OTH_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 69 of 95		



ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 71 of 95		

ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 72 of 95		

ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 73 of 95		

Main Board

Title : VGA_****

ASUSTeK COMPUTER INC. NB1

Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0

Date: Monday, September 03, 2007 Sheet 74 of 95

ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 75 of 95		

ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 78 of 95		

Main Board

Title : VGA_****

ASUSTeK COMPUTER INC. NB1

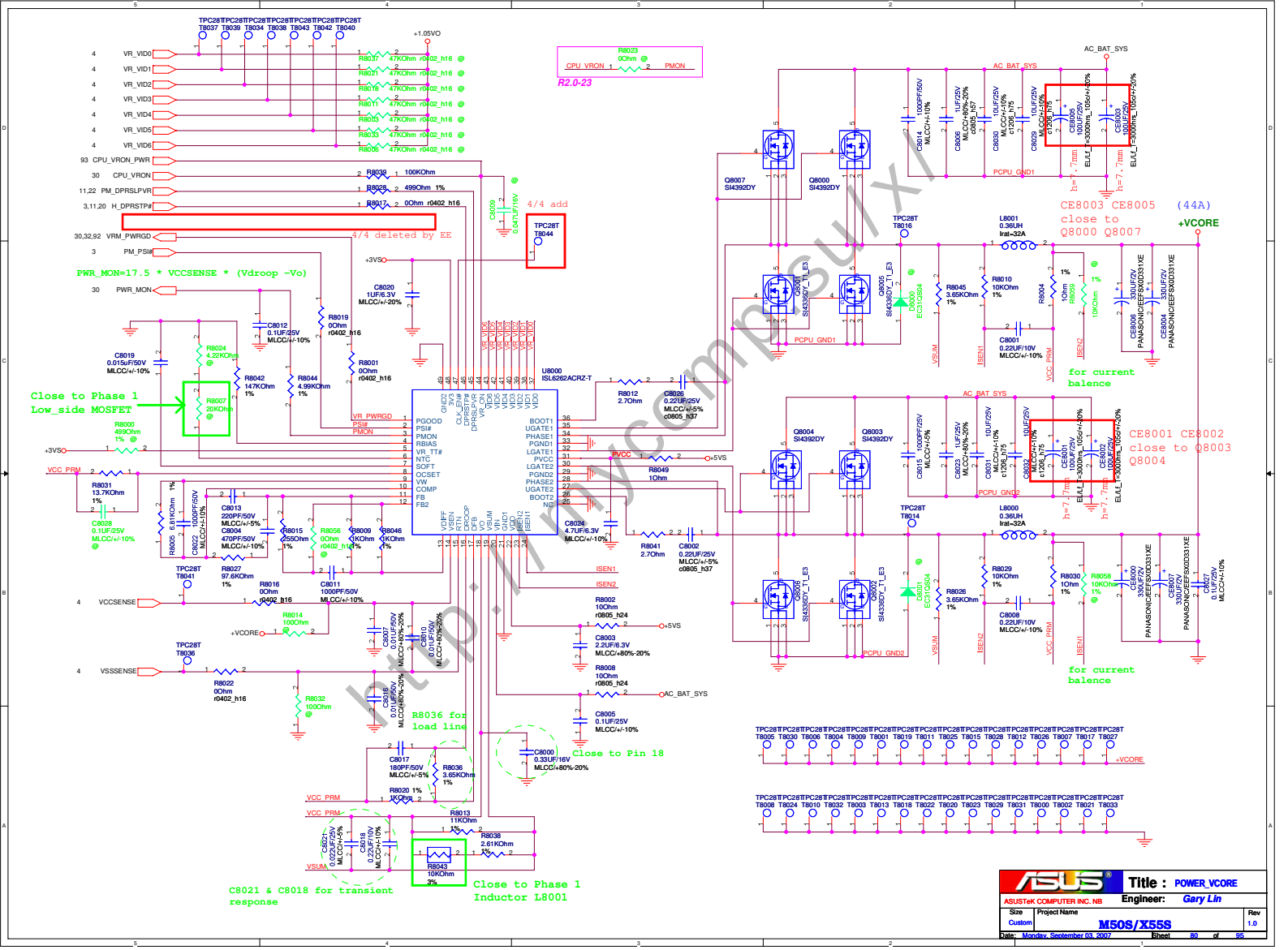
Engineer: John Hung

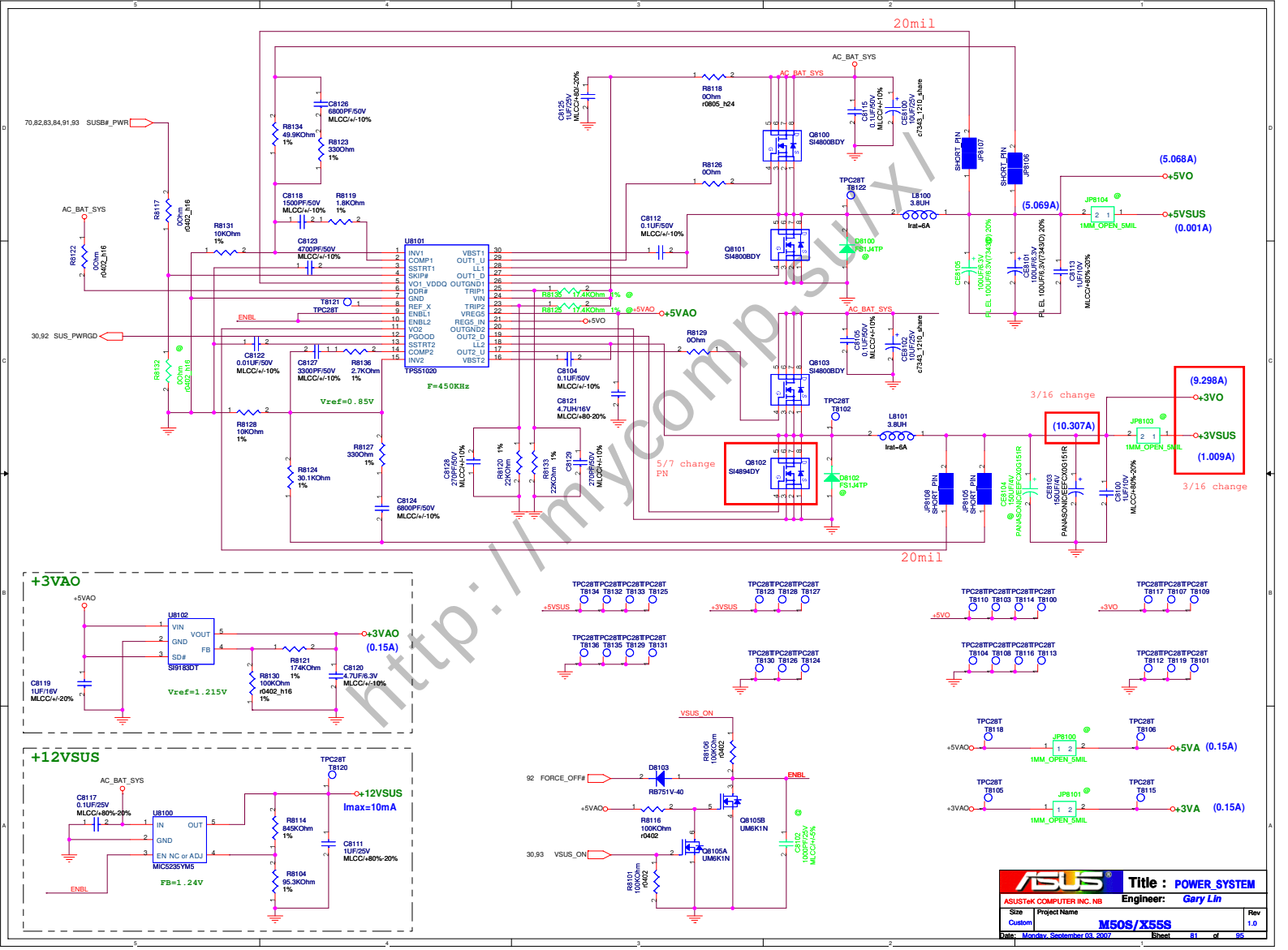
Size	Project Name	Rev
Custom	M50S/X55S	2.0

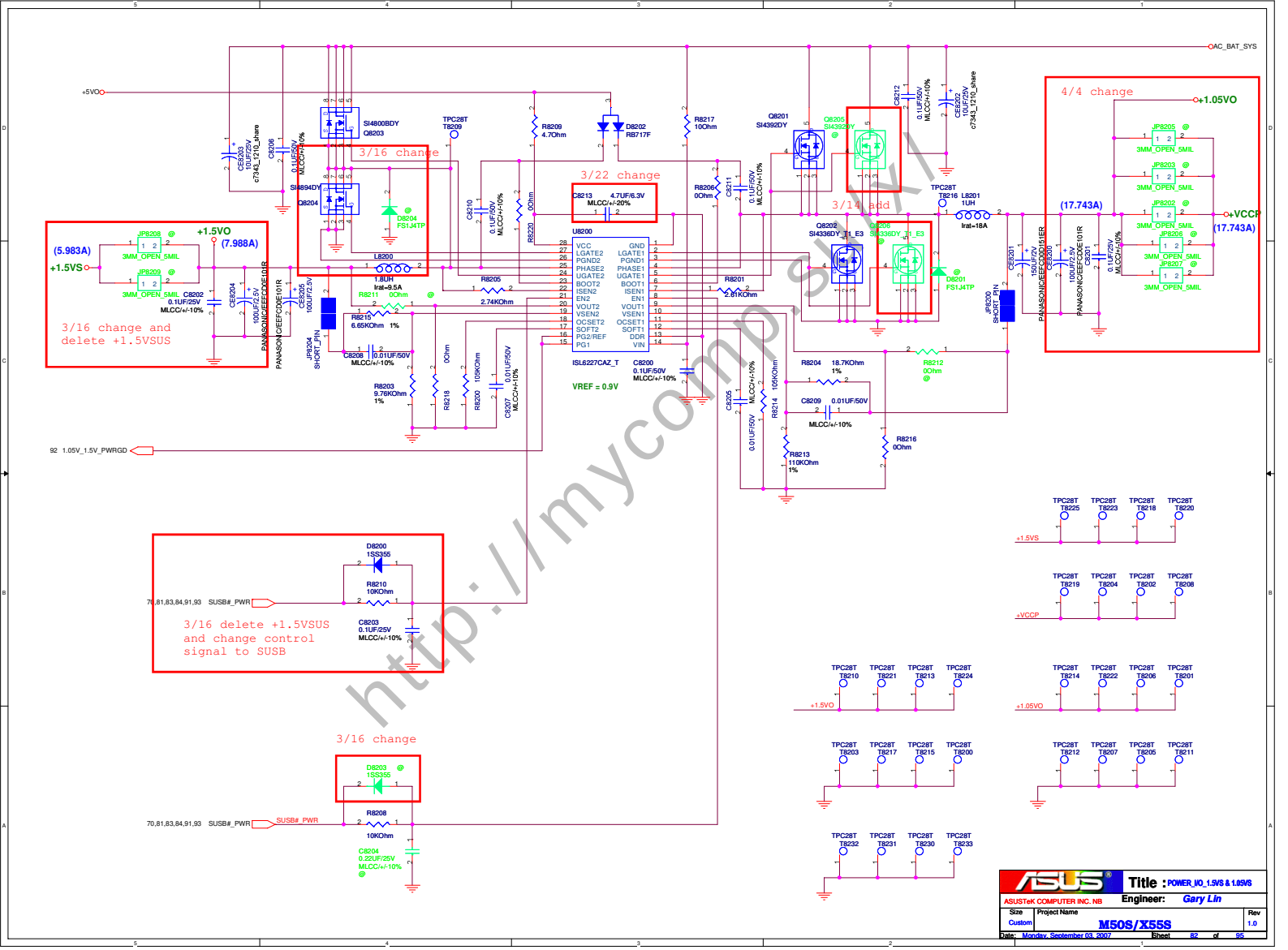
Date: Monday, September 03, 2007 Sheet 77 of 95

ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 78 of 95		

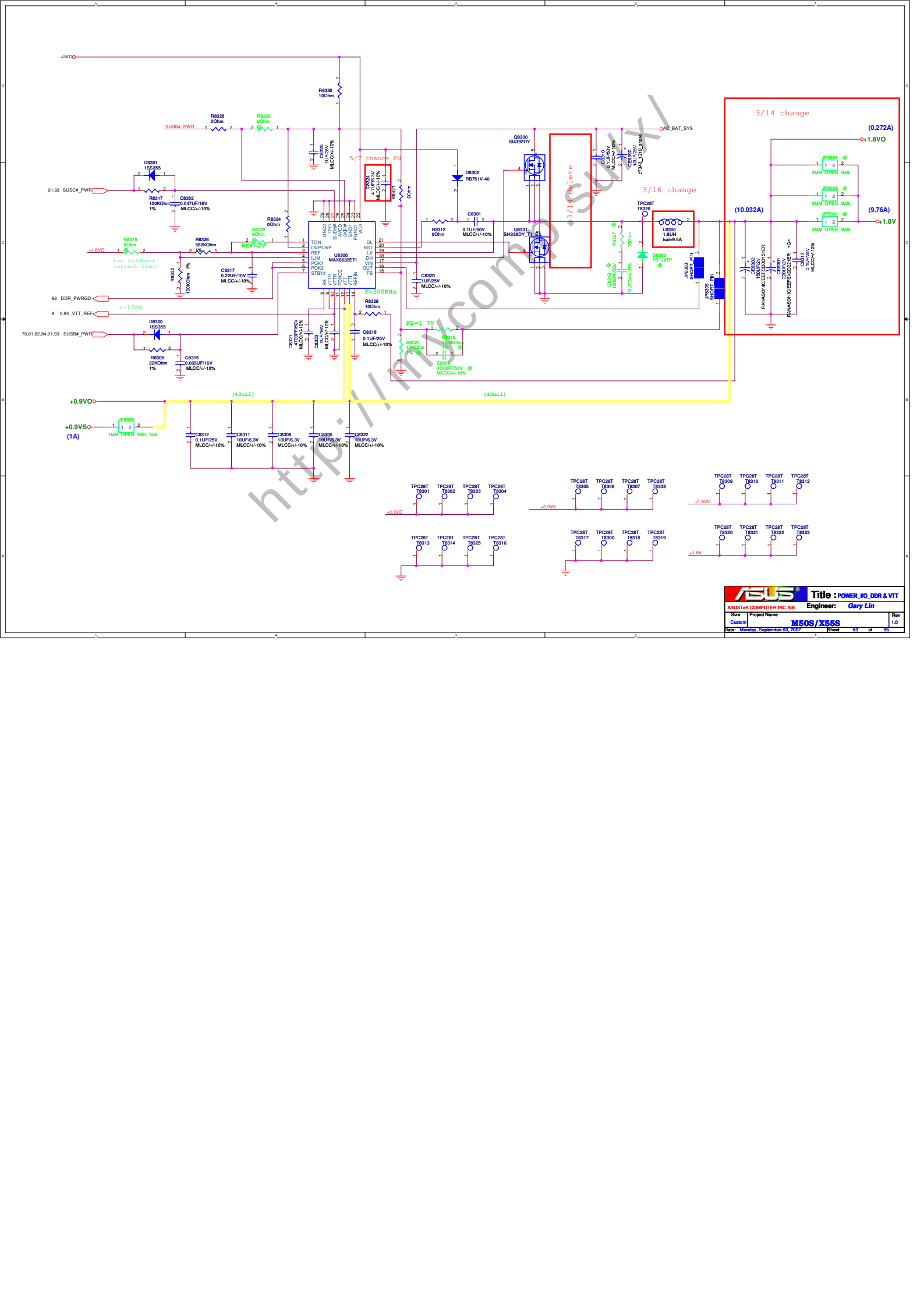
ASUSTeK COMPUTER INC. NB1	Title : VGA_****		
	Engineer: John Hung		
Size: Custom	Project Name: M50S/X55S		Rev: 2.0
Date: Monday, September 03, 2007	Sheet 79 of 95		


PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1
Low_side MOSFET
4/4 deleted by EE
4/4 add
R2.0-23
R8036 for
load line
Close to Pin 18
C8021 & C8018 for transient
response
Close to Phase 1
Inductor L8001
CE8003 CE8005 (44A)
close to
Q8000 Q8007
+VCORE
for current
balence
CE8001 CE8002
close to Q8003
Q8004
for current
balence
U8000
ISL6262ACRZ-T
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Gary Lin
M50S/X55S
Monday, September 03, 2007

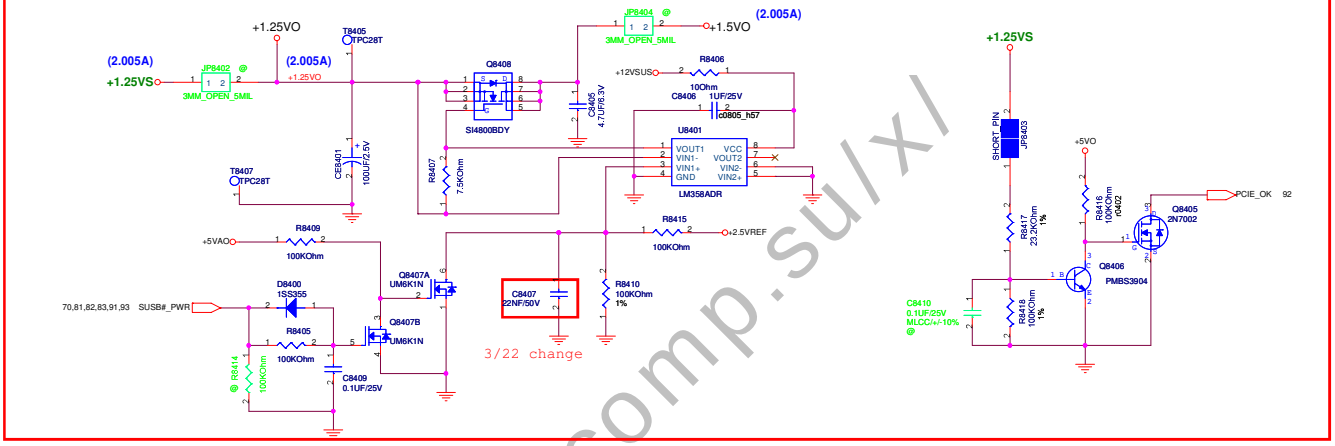




ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_1.5VS & 1.05VS	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 82 of 95	



+1.25VS 3/16 EE modify to daughter,so add this part



3/16 delete +2.5VSUS

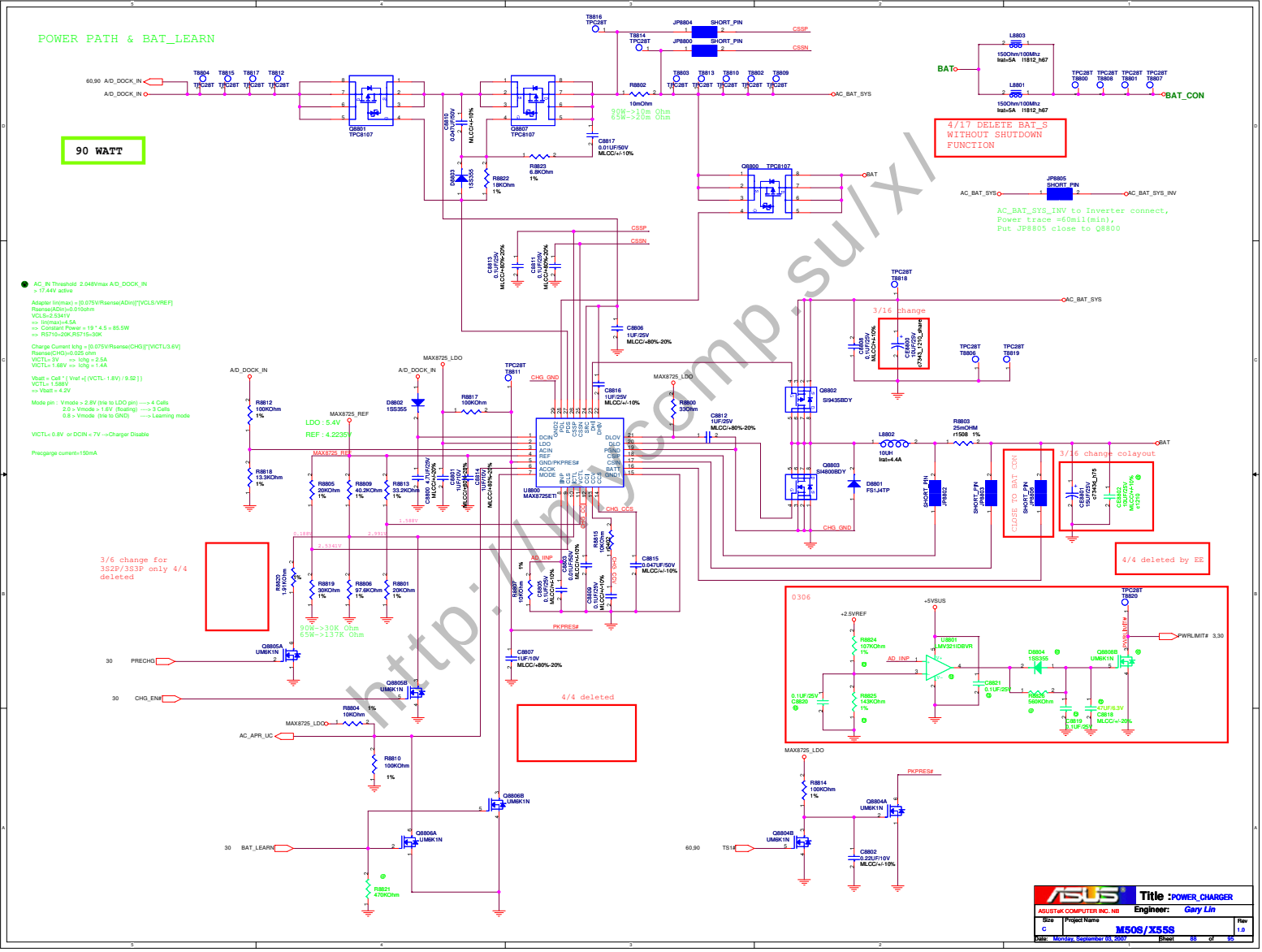
ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_+1.25VS	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 84 of 95	

3/14 EE modify to daughter,so delete this page

ASUSTeK COMPUTER INC. NB	Title : N/A	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 85 of 95	

ASUSTeK COMPUTER INC. NB	Title : N/A		
	Engineer: Gary Lin		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 86 of 95		

ASUSTeK COMPUTER INC. NB	Title : N/A	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 87 of 95	


POWER PATH & BAT_LEARN
90 WATT
4/17 DELETE BAT_S WITHOUT SHUTDOWN FUNCTION
AC_BAT_SYS_INV to Inverter connect, Power trace =60mil(min), Put JP8805 close to Q8800
3/16 change
3/16 change colayout
4/4 deleted by EE
4/4 deleted
3/6 change for 352P/333P only 4/4 deleted
90W->30K Ohm 65W->137K Ohm
90W->21m Ohm 65W->20m Ohm
LDO : 5.4V
REF : 4.2235V
AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF] Rsense(ADin)=0.010ohm VCLS=2.534V => Iin(max)=4.5A => Constant Power = 19 * 4.5 = 85.5W => R5710=20K,R5715=30K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V] Rsense(CHG)=0.025 ohm VICTL= 3V => Ichg = 2.5A VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL - 1.8V) / 9.52]] VCTL= 1.588V => Vbatt = 4.2V
Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells 2.0 > Vmode > 1.6V (floating) ----> 3 Cells 0.8 > Vmode (tie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V ->Charger Disable
Precgarge current=150mA
http://mycomp.su/xl
ASUSTeK COMPUTER INC. NB
Title : POWER_CHARGER
Engineer: Gary Lin
Size C
Project Name M50S/X55S
Rev 1.0
Date: Monday, September 03, 2007
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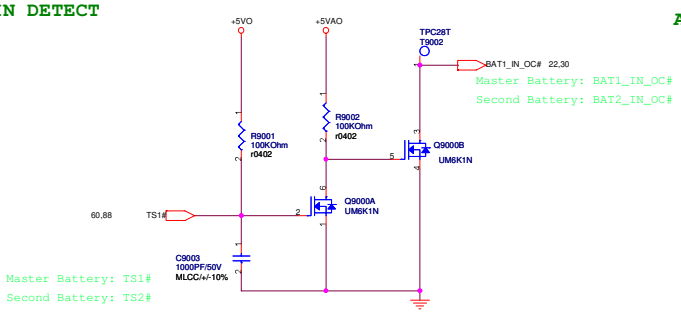
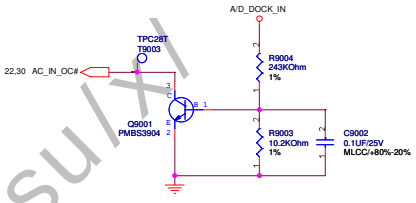
ASUSTeK COMPUTER INC. NB	Title : N/A		
	Engineer: Gary Lin		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 89 of 95		

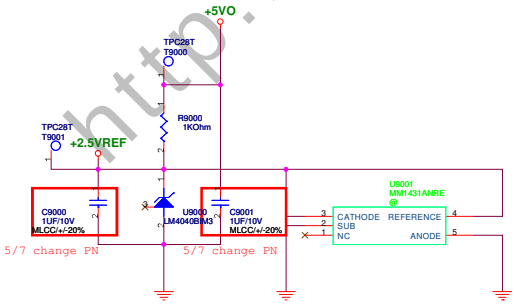
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



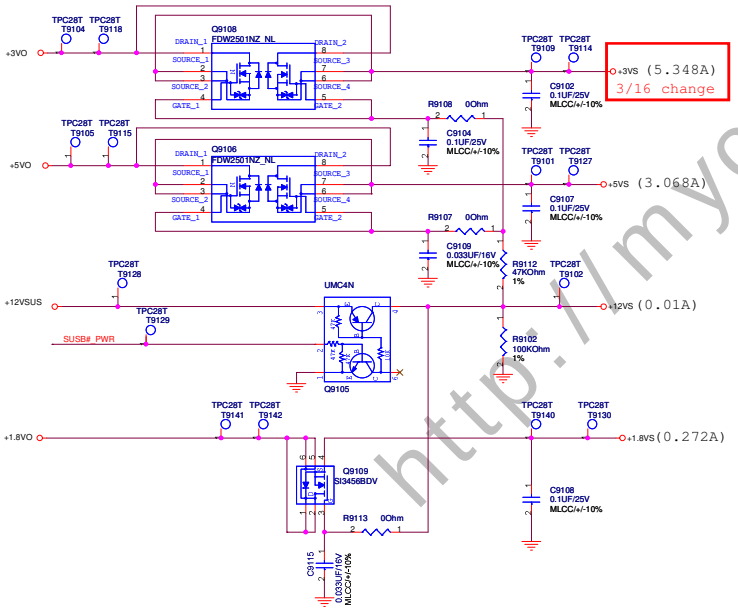
U9000 & U9001 colay

ASUSTeK COMPUTER INC. NB	Title : POWER_DETECT	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 90 of 95	

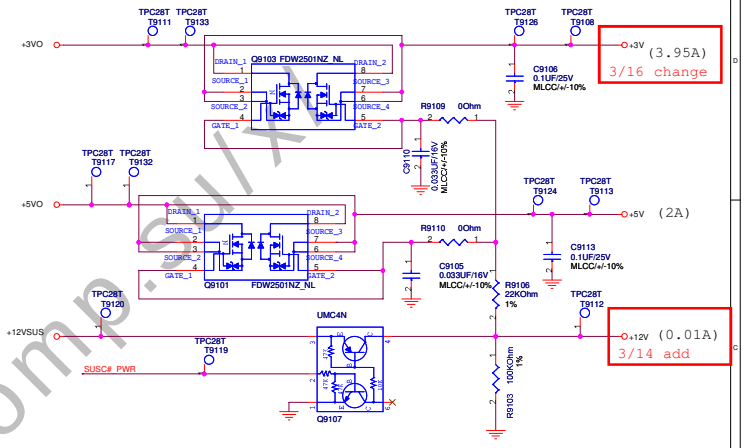
SUSB#_PWR POWER

3/16 delete +1.5VS from load switch

3/14 delete +VRAM

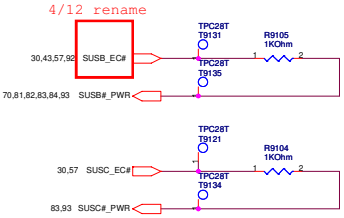


SUSC#_PWR POWER



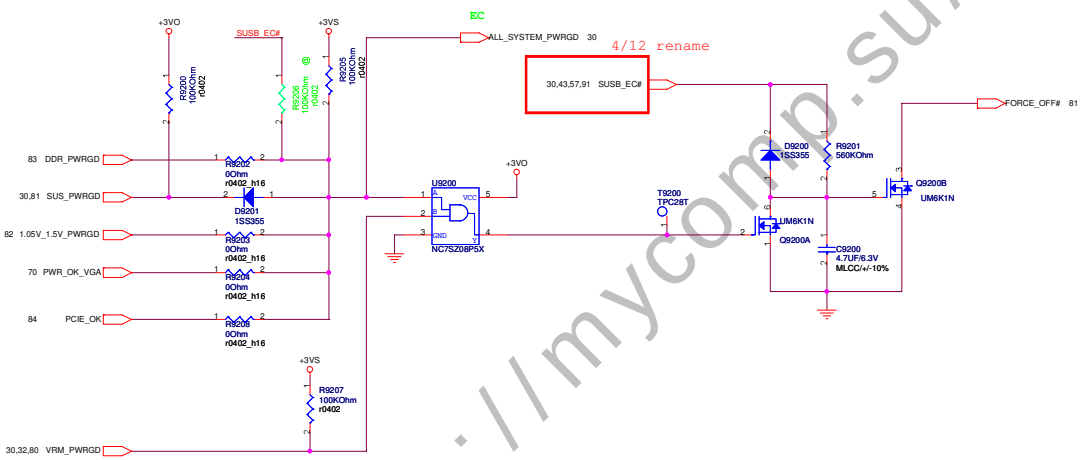
3/16 delete +1.5V

4/12 rename



ASUSTeK COMPUTER INC. NB	Title : POWER_LOAD SWITCH	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 91 of 95	

POWER GOOD DETECTER



ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Gary Lin	
Size: Custom	Project Name: M50S/X55S	Rev: 1.0
Date: Monday, September 03, 2007	Sheet 92 of 95	

AC_BAT_SYS_INV — AC_BAT_SYS_INV 45,88

AC_BAT_SYS — AC_BAT_SYS 70,80,81,82,83,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

+2.5VREF — +2.5VREF 84,88,90

+3VA — +3VA 20,30,56,57,81

+5VAO — +5VAO 81,84,90

+5VO — +5VO 81,82,83,84,90,91

+5VSUS — +5VSUS 23,31,81,88

+5V — +5V 15,44,45,56,57,63,65,66,70,91

+5VS — +5VS 22,23,31,36,37,46,48,50,51,56,57,63,80,91

+3VO — +3VO 81,91,92

+3VSUS — +3VSUS 22,23,33,81

+3V — +3V 35,43,45,53,57,61,62,64,91

+3VS — +3VS 7,8,11,15,21,22,23,29,30,32,33,36,37,40,41,42,43,44,45,46,47,48,50,51,53,56,57,58,62,63,64,65,66,67,70,80,91,92

+5VA — +5VA 56,63,81

+12VSUS — +12VSUS 81,84,91

+12V — +12V 42,91

+12VS — +12VS 37,45,46,70,91

+1.8VO — +1.8VO 83,91

+1.8V — +1.8V 7,8,9,11,14,15,57,83

+1.8VS — +1.8VS 38,57,66,70,91

+0.9VS — +0.9VS 9,57,70,83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,82

+VCCP — +VCCP 3,4,5,10,12,14,15,20,23,29,57,82

+1.5VO — +1.5VO 82,84

+1.5VS — +1.5VS 4,15,21,23,43,53,57,58,64,70,82

+VCORE — +VCORE 4,5,80

+1.25VS — +1.25VS 11,15,23,57,84

FOR POWER TEST

+3VA

JP9300 — 1 2 — SGL_JUMP @ — CPU_VRON_PWR 80

JP9301 — 1 2 — SUSB#_PWR — SUSB#_PWR 70,81,82,83,84,91 — SGL_JUMP @

JP9302 — 1 2 — SUSC#_PWR — SUSC#_PWR 83,91 — SGL_JUMP @

JP9303 — 1 2 — VSUS_ON — VSUS_ON 30,81 — SGL_JUMP @

ASUSTeK COMPUTER INC. NB

Title : POWER_SIGNAL

Engineer: Gary Lin

Size	Project Name	Rev
Custom	M50S/X55S	1.0

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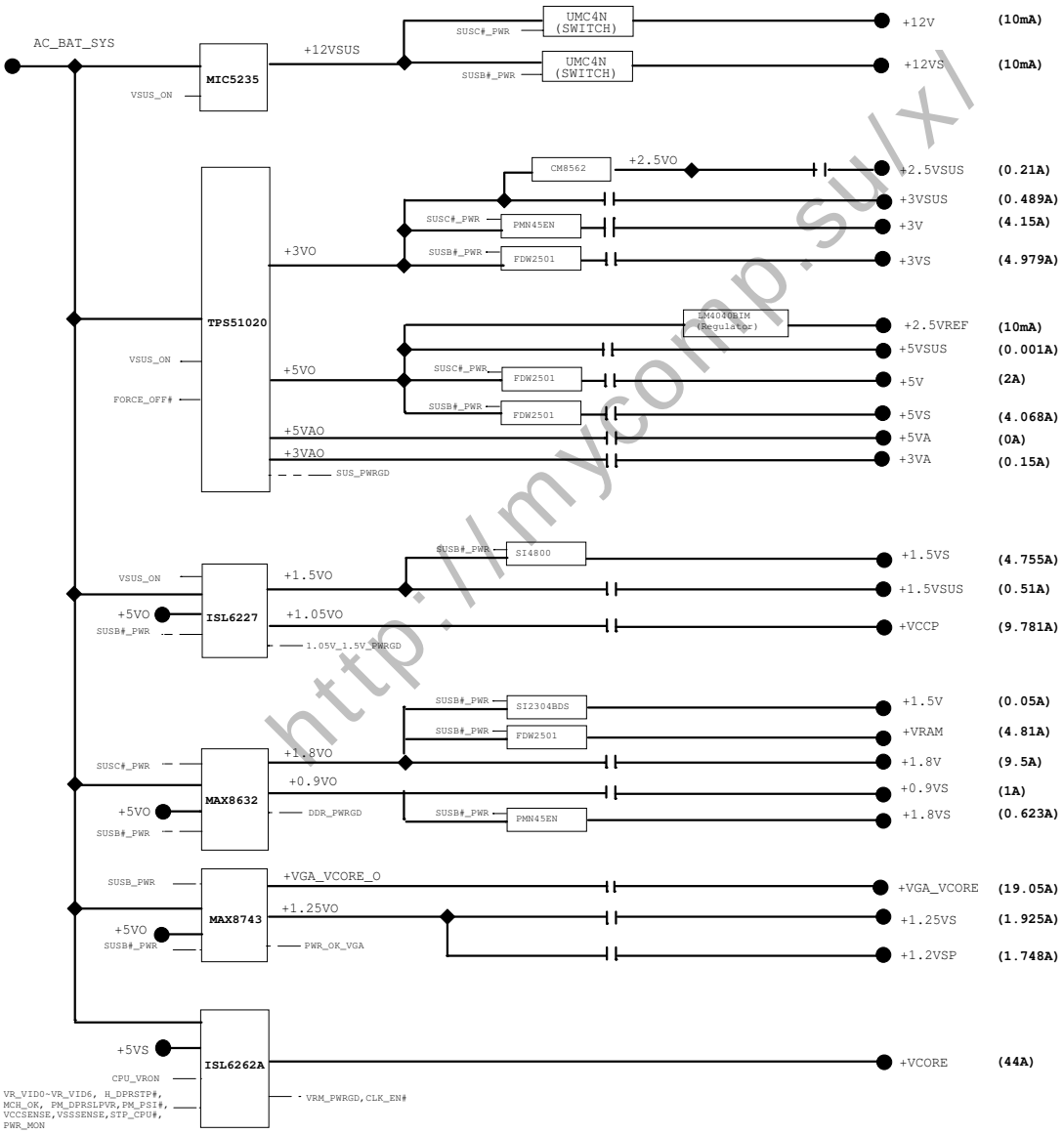
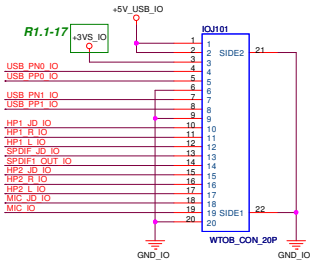
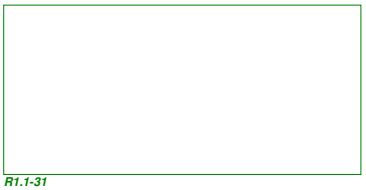
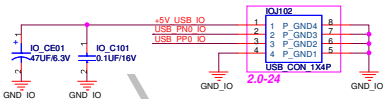


ASUSTeK COMPUTER INC. NB	Title : POWER_FLOWCHART		
	Engineer: Gary Lin		
Size: Custom	Project Name: M50S/X55S		Rev: 1.0
Date: Monday, September 03, 2007	Sheet 84 of 95		

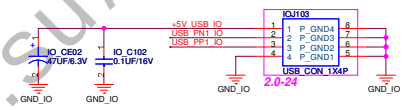


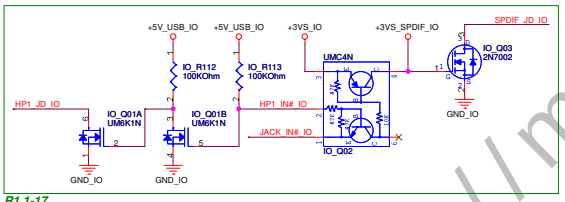


USB Port 0

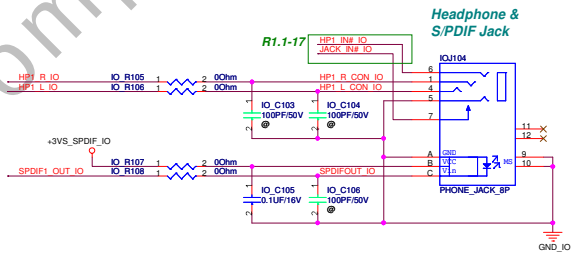


USB Port 1

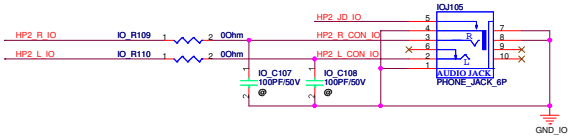




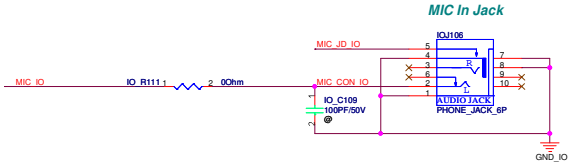
Headphone & S/PDIF Jack



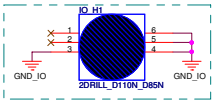
Headphone Jack



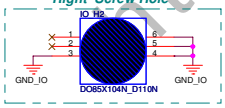
MIC In Jack



Left Screw Hole



Right Screw Hole



ASUSTeK COMPUTER INC. NB1	Title : USB & Audio Jack	
	Engineer: Wenchi_Shen	
Size: Custom	Project Name: M50S/X55S	Rev: 2.0
Date: Monday, September 03, 2007	Sheet 95 of 96	

Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		** Merge IO board into main board PCB. Page 95. 01.Remove VR_VID[6:0] testing series 0 0hm. Page 4. 02.Change 6pcs +VCORE capacitors to No-Stuff for cost down. Page 5. 03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9. 04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45. 05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56. 06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23. 07.Follow R1E to change R2904 to 270ohm. Page 29. 08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30. 09.PM REquest: Remove USB port charger function. Page 30,65. 10.PM change WWAN LED to touch-pad lock LED. Page 30,56. 11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31. 12.Remove testing 2nd CIR design. Page 31. 13.Change X3301 to 49S type for cost down. Page 33. 14.LAN chip version change. Page 33. 15.Audio codec chip change version. Page 36. 16.N1Sv/X55 will not supprot 3G function. Page 36,67. 17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95. 18.Modify audio de-pop circuit. Page 36,37. 19.Modify LVDS power sequence failed bug. Page 45. 20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70. 21.Remove HDTV support function. Page 47,70. 22.Remove HDMI EMI filter design. Page 48. 23.X55 need two pwer LEDs. Page 56. 24.PM change WLAN LED to RF LED. Page 56,63. 25.Bluetooth pin define error. Page 61. 26.Remove co-layout sequence logic control circuit. Page 68. 27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65. 28.EMI modification. Page 34,36,65. 29.Crystal accuracy fine-tune. Page 30.USB droop test fail. Page 65. 31.Remove IO board USB common choke design. Page 95. 32.Speaker fine-tune. Page 37. 33.Cost down for 4-wire PWM fan. Page 50. 34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.
R2.0 Pink Block		01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15. 02.Add CMOS crack protection circuit. Page 22. 03.Reserve C2337 (10UF/16V) for +5VREF_ICH. Page 23. 04.Change ICS9LPR363 version from D to E for SATA clock jitter improve. Page 29. 05.With EMI's confirmation, replace R2901, R2905, R2906 with short-pad JP2901, JP2902, JP2903. Page 29. 06.With EC's confirmation, change ITE8752 P/N to 06G042016011. Page 30. 07.With EMI's confirmation, replace R3001 with short-pad JP3002. Page 30. 08.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34. 09.With EMI's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624, R3626 to short-pad JP3601~JP3607. And change R3611, R3613, R3623, R3625 to No-Stuff. Page 36. 10.Post wave sounds abnormal when audio amplifier use GMT G1431. Change C3706 to 0.33UF to shorten audio amplifier start-up time. Page 37.

Rev	Date	Description
		11.For cost down, change CE3701~CE3704 to 47UF. And after EA test, these can pass Vista audio criteria. Page 37. 12.With EMI's confirmation, remove reserved 1394 common choke circuit. Page 41. 13.With EMI's confirmation, remove reserved NewCard USB common choke circuit. Page 43. 14.Add NewCard debug card co-layout circuit. Page 44. 15.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45. 16.With EMI's confirmation, replace RX4603, RX4604 with JP4601, JP4602. Page 46. 17.HDMI jack detection modification. Page 48,70. 18.With EMI's confirmation, replace RX4809, RX4810 with JP4801, JP4802. Page 48. 19.Change PWM FAN capacitors to 10UF. Page 50. 20.Modify X55S power LED design. Page 56. 21.Modify DC_IN bead for 120W design. Page 60. 22.With EMI's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 66. 23.Reserve R8023 for shortage issue of ISL6262A. Page 80. 24.QTR USB plug test failed, change USB connector. Page 95.

ASUSTeK COMPUTER INC. NB1

Title : Revision History

Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	1.0

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