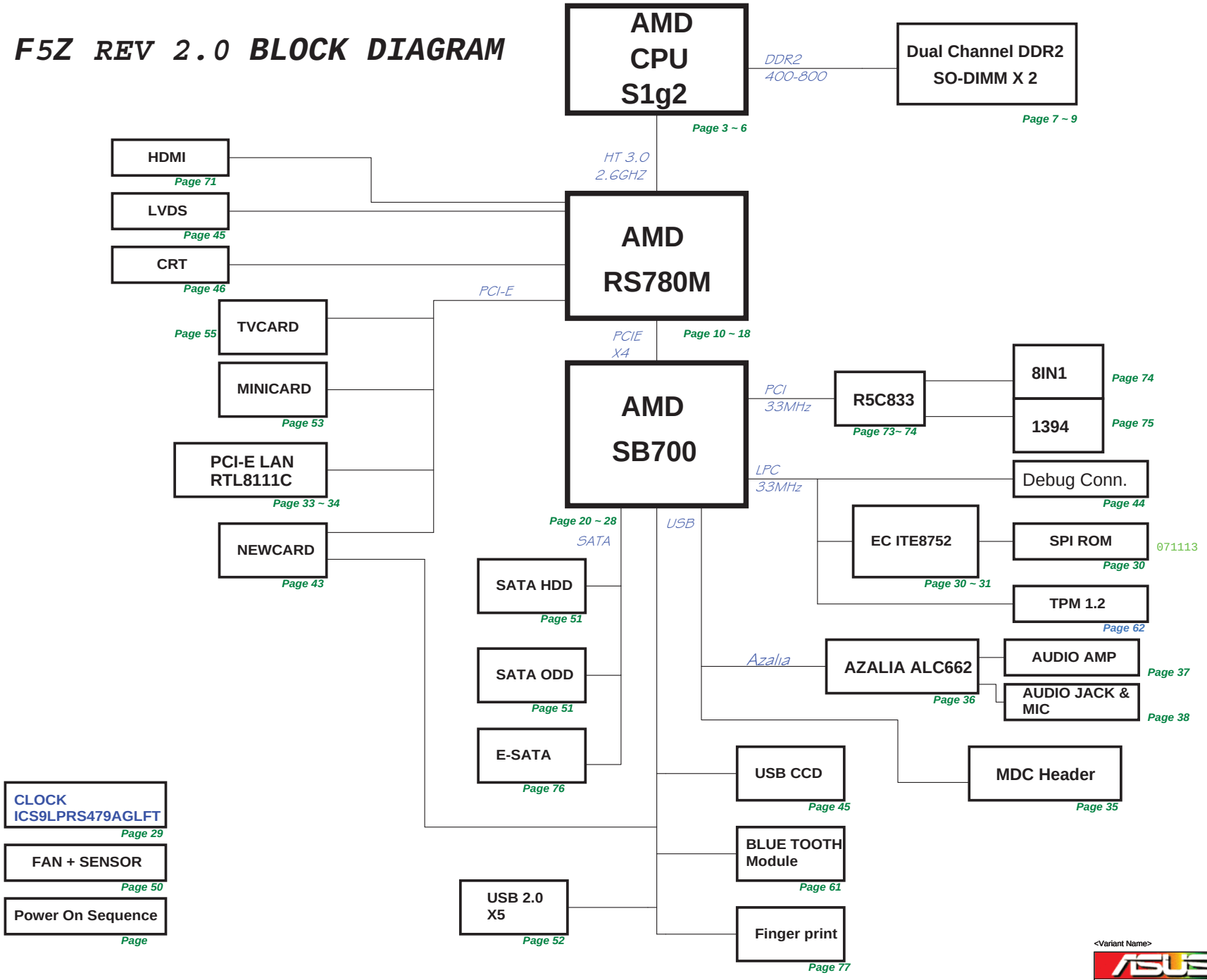
F5Z REV 2.0 BLOCK DIAGRAM



<Variant Name>

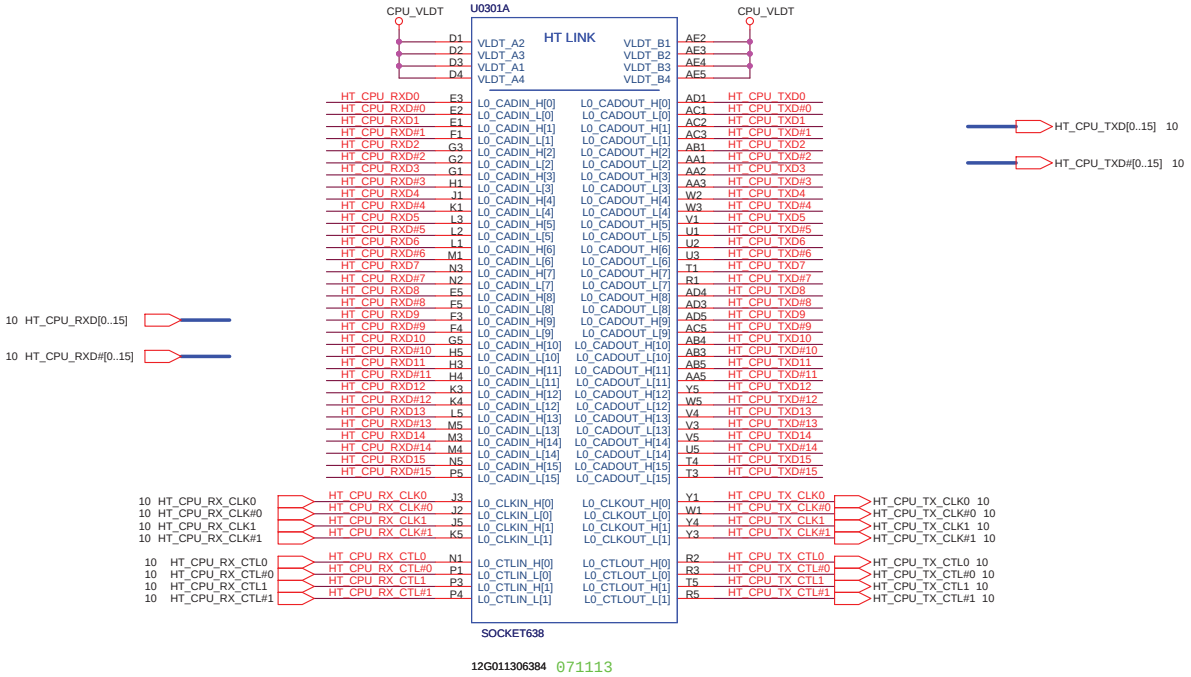
Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F5Z	2.0

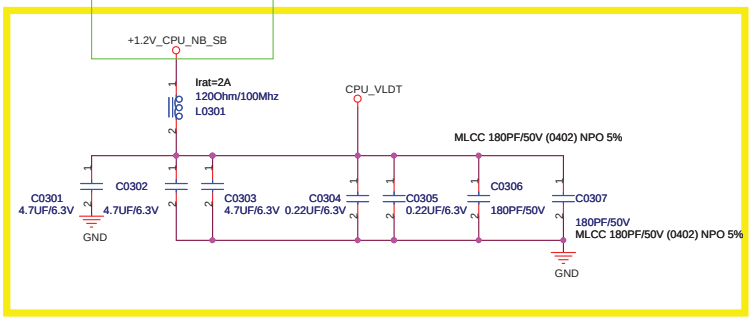
Date: Monday, May 19, 2008 Sheet 1 of 94



12G011306384 071113

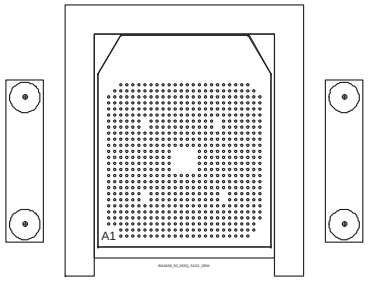
Do not cross plane.

071219 Recover



Place close to socket

* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



ASUSTeK.Computer.INC

Title : Griffin HT I/F

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 3 of 94

Processor Memory Interface

place close to RROCESSOR within 1.5 inch

place close to RROCESSOR within 1.5 inch

7 MEM_MA0_CLK7 — MEM_MA0_CLK_H7 — C0405 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L7 — 7 MEM_MA0_CLK#7

7 MEM_MA0_CLK1 — MEM_MA0_CLK_H1 — C0406 1.5PF/50V MLCC/+/-0.1PF — MEM_MA0_CLK_L1 — 7 MEM_MA0_CLK#1

071114

8 MEM_MB0_CLK7 — MEM_MB0_CLK_H7 — C0407 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L7 — 8 MEM_MB0_CLK#7

8 MEM_MB0_CLK1 — MEM_MB0_CLK_H1 — C0408 1.5PF/50V MLCC/+/-0.1PF — MEM_MB0_CLK_L1 — 8 MEM_MB0_CLK#1

PLACE THEM CLOSE TO CPU WITHIN 1".

+0.9V — U0301B — SOCKET638

MEM:CMD/CTRL/CLK

VTT2 D10, VTT8 C10, VTT3 B10, VTT1 AD10, VTT4 W10, VTT5 AC10, VTT6 AB10, VTT7 AA10, VTT9 A10

M_ZP AE10 — R0401 39.2OHM 1% — M_ZP

M_ZN AE10 — R0402 39.2OHM 1% — M_ZN

T0401 TPC28T — MEM_MA_RESET# H16 — RSVD8

VTT_SENSE Y10 — VTT_SENSE 1 — T0417 TPC28T — 071115

M_VREF W17 — CPU_M_VREF

RSVD6 B18 — MEM_MB_RESET# TPC28T 1 — T0410

MA0_ODT[0] T19 — 7,9 MEM_MA0_ODT0

MA0_ODT[1] V22 — 7,9 MEM_MA0_ODT1

MA1_ODT[0] U21 — TPC28T T0402 — MEM_MA1_ODT0

MA1_ODT[1] V19 — TPC28T T0403 — MEM_MA1_ODT1

MB0_ODT[0] W26 — MEM_MB0_ODT0 8,9

MB0_ODT[1] W23 — MEM_MB0_ODT1 8,9

MB1_ODT[0] Y26 — MEM_MB1_ODT0 1 — T0411 TPC28T

MA0_CS_L[0] T20 — 7,9 MEM_MA0_CS#0

MA0_CS_L[1] U19 — 7,9 MEM_MA0_CS#1

MA1_CS_L[0] U20 — T0404 TPC28T

MA1_CS_L[1] V20 — T0405 TPC28T

MB0_CS_L[0] V26 — MEM_MB0_CS#0 8,9

MB0_CS_L[1] W25 — MEM_MB0_CS#1 8,9

MB1_CS_L[0] U22 — TPC28T 1 — T0412

MA_CKE[0] J22 — 7,9 MEM_MA_CKE0

MA_CKE[1] J20 — 7,9 MEM_MA_CKE1

MB_CKE[0] J25 — MEM_MB_CKE0 8,9

MB_CKE[1] H26 — MEM_MB_CKE1 8,9

MA_CLK_H[5] N19 — T0406 TPC28T

MA_CLK_L[5] N20 — T0407 TPC28T

MA_CLK_H[1] E16 — MEM_MA0_CLK_H1

MA_CLK_L[1] F16 — MEM_MA0_CLK_L1

MA_CLK_H[7] Y16 — MEM_MA0_CLK_H7

MA_CLK_L[7] AA16 — MEM_MA0_CLK_L7

MA_CLK_H[4] P19 — T0408 TPC28T

MA_CLK_L[4] P20 — T0409 TPC28T

MB_CLK_H[5] P22 — TPC28T 1 — T0413

MB_CLK_L[5] R22 — TPC28T 1 — T0414

MB_CLK_H[1] A17 — MEM_MB0_CLK_H1

MB_CLK_L[1] A18 — MEM_MB0_CLK_L1

MB_CLK_H[7] AF18 — MEM_MB0_CLK_H7

MB_CLK_L[7] AF17 — MEM_MB0_CLK_L7

MB_CLK_H[4] R26 — TPC28T 1 — T0415

MB_CLK_L[4] R25 — TPC28T 1 — T0416

7,9 MEM_MA_ADD[0..15]

MA_ADD[0] N21, MA_ADD[1] M20, MA_ADD[2] N22, MA_ADD[3] M19, MA_ADD[4] M22, MA_ADD[5] L20, MA_ADD[6] M24, MA_ADD[7] L21, MA_ADD[8] L19, MA_ADD[9] K22, MA_ADD[10] R21, MA_ADD[11] L22, MA_ADD[12] K20, MA_ADD[13] V24, MA_ADD[14] K24, MA_ADD[15] K19

MB_ADD[0] P24, MB_ADD[1] N24, MB_ADD[2] P26, MB_ADD[3] N23, MB_ADD[4] N26, MB_ADD[5] L23, MB_ADD[6] N25, MB_ADD[7] L24, MB_ADD[8] M26, MB_ADD[9] K26, MB_ADD[10] T26, MB_ADD[11] L26, MB_ADD[12] L25, MB_ADD[13] W24, MB_ADD[14] J23, MB_ADD[15] J24

MEM_MB_ADD[0..15] 8,9

MA_BANK[0] R20 — 7,9 MEM_MA_BANK0

MA_BANK[1] R23 — 7,9 MEM_MA_BANK1

MA_BANK[2] J21 — 7,9 MEM_MA_BANK2

MB_BANK[0] R24 — MEM_MB_BANK0 8,9

MB_BANK[1] U26 — MEM_MB_BANK1 8,9

MB_BANK[2] J26 — MEM_MB_BANK2 8,9

MA_RAS_L R19 — 7,9 MEM_MA_RAS#

MA_CAS_L T22 — 7,9 MEM_MA_CAS#

MA_WE_L T24 — 7,9 MEM_MA_WE#

MB_RAS_L U25 — MEM_MB_RAS# 8,9

MB_CAS_L U24 — MEM_MB_CAS# 8,9

MB_WE_L U23 — MEM_MB_WE# 8,9

+1.8V — R0405 0Ohm @ — +3VSUS — C0401 — GND — 0.1UF/16V

LMV321IDBVR — U0401 — R0408 10Ohm — CPU_M_VREF

R0403 1KOhm 1% — R0404 1KOhm 1%

R0406 @ 0Ohm — R0409 10KOhm — C0403 0.1UF/16V — C0404 1000PF/16V

C0402 1000PF/16V — R0407 0Ohm

PLACE CLOSE TO CPU

sensing point for op-amp feedback routed near CPU

GND

071203 change U0401 P/N for NB footprint

7 MEM_MA_DQS[0..7]

7 MEM_MA_DQS#[0..7]

8 MEM_MB_DQS[0..7]

8 MEM_MB_DQS#[0..7]

U0301C — MEM:DATA — SOCKET638

8 MEM_MB_DATA[0..63]

MEM_MB_DATA0 C11, MEM_MB_DATA1 A11, MEM_MB_DATA2 A14, MEM_MB_DATA3 B14, MEM_MB_DATA4 G11, MEM_MB_DATA5 E11, MEM_MB_DATA6 D12, MEM_MB_DATA7 A13, MEM_MB_DATA8 A15, MEM_MB_DATA9 A16, MEM_MB_DATA10 A19, MEM_MB_DATA11 A20, MEM_MB_DATA12 C14, MEM_MB_DATA13 D14, MEM_MB_DATA14 C18, MEM_MB_DATA15 D18, MEM_MB_DATA16 D20, MEM_MB_DATA17 A21, MEM_MB_DATA18 D24, MEM_MB_DATA19 C25, MEM_MB_DATA20 B20, MEM_MB_DATA21 C20, MEM_MB_DATA22 B24, MEM_MB_DATA23 C24, MEM_MB_DATA24 E23, MEM_MB_DATA25 E24, MEM_MB_DATA26 G25, MEM_MB_DATA27 G26, MEM_MB_DATA28 C26, MEM_MB_DATA29 D26, MEM_MB_DATA30 G23, MEM_MB_DATA31 G24, MEM_MB_DATA32 AA24, MEM_MB_DATA33 AA23, MEM_MB_DATA34 AD24, MEM_MB_DATA35 AE24, MEM_MB_DATA36 AA26, MEM_MB_DATA37 AA25, MEM_MB_DATA38 AD26, MEM_MB_DATA39 AE25, MEM_MB_DATA40 AC22, MEM_MB_DATA41 AD22, MEM_MB_DATA42 AE20, MEM_MB_DATA43 AF20, MEM_MB_DATA44 AF24, MEM_MB_DATA45 AF23, MEM_MB_DATA46 AC20, MEM_MB_DATA47 AD20, MEM_MB_DATA48 AD18, MEM_MB_DATA49 AE18, MEM_MB_DATA50 AC14, MEM_MB_DATA51 AD14, MEM_MB_DATA52 AE19, MEM_MB_DATA53 AC18, MEM_MB_DATA54 AF16, MEM_MB_DATA55 AF15, MEM_MB_DATA56 AF13, MEM_MB_DATA57 AC12, MEM_MB_DATA58 AB11, MEM_MB_DATA59 Y11, MEM_MB_DATA60 AE14, MEM_MB_DATA61 AF14, MEM_MB_DATA62 AF11, MEM_MB_DATA63 AD11

MB_DATA[0..63]

MA_DATA[0] G12, MA_DATA[1] F12, MA_DATA[2] H14, MA_DATA[3] G14, MA_DATA[4] H11, MA_DATA[5] H12, MA_DATA[6] C13, MA_DATA[7] E13, MA_DATA[8] H15, MA_DATA[9] E15, MA_DATA[10] E17, MA_DATA[11] H17, MA_DATA[12] E14, MA_DATA[13] F14, MA_DATA[14] C17, MA_DATA[15] G17, MA_DATA[16] G18, MA_DATA[17] C19, MA_DATA[18] D22, MA_DATA[19] E20, MA_DATA[20] E18, MA_DATA[21] F18, MA_DATA[22] B22, MA_DATA[23] C23, MA_DATA[24] F20, MA_DATA[25] F22, MA_DATA[26] H24, MA_DATA[27] J19, MA_DATA[28] E21, MA_DATA[29] F22, MA_DATA[30] H20, MA_DATA[31] H22, MA_DATA[32] Y24, MA_DATA[33] AB24, MA_DATA[34] AB22, MA_DATA[35] AA21, MA_DATA[36] W22, MA_DATA[37] W21, MA_DATA[38] Y22, MA_DATA[39] AA22, MA_DATA[40] Y20, MA_DATA[41] AA20, MA_DATA[42] AA18, MA_DATA[43] AB18, MA_DATA[44] AB21, MA_DATA[45] AD21, MA_DATA[46] AD19, MA_DATA[47] Y18, MA_DATA[48] AD17, MA_DATA[49] W16, MA_DATA[50] W14, MA_DATA[51] Y14, MA_DATA[52] Y17, MA_DATA[53] AB17, MA_DATA[54] AB15, MA_DATA[55] AD15, MA_DATA[56] AB13, MA_DATA[57] AD13, MA_DATA[58] Y12, MA_DATA[59] W11, MA_DATA[60] AB14, MA_DATA[61] AA14, MA_DATA[62] AB12, MA_DATA[63] AA12

MA_DATA[0..63] 7

8 MEM_MB_DM[0..7]

MEM_MB_DM0 A12, MEM_MB_DM1 B16, MEM_MB_DM2 A22, MEM_MB_DM3 E25, MEM_MB_DM4 AB26, MEM_MB_DM5 AE22, MEM_MB_DM6 AC16, MEM_MB_DM7 AD12

MB_DM[0..7]

MA_DM[0] E12, MA_DM[1] C15, MA_DM[2] E19, MA_DM[3] F24, MA_DM[4] AC24, MA_DM[5] Y19, MA_DM[6] AB16, MA_DM[7] Y13

MA_DM[0..7] 7

MEM_MB_DQS0 C12, MEM_MB_DQS#0 B12, MEM_MB_DQS1 D16, MEM_MB_DQS#1 C16, MEM_MB_DQS2 A24, MEM_MB_DQS#2 A23, MEM_MB_DQS3 F26, MEM_MB_DQS#3 E26, MEM_MB_DQS4 AC25, MEM_MB_DQS#4 AC26, MEM_MB_DQS5 AF21, MEM_MB_DQS#5 AF22, MEM_MB_DQS6 AE16, MEM_MB_DQS#6 AD16, MEM_MB_DQS7 AF12, MEM_MB_DQS#7 AE12

MB_DQS_H[0] MB_DQS_L[0] MB_DQS_H[1] MB_DQS_L[1] MB_DQS_H[2] MB_DQS_L[2] MB_DQS_H[3] MB_DQS_L[3] MB_DQS_H[4] MB_DQS_L[4] MB_DQS_H[5] MB_DQS_L[5] MB_DQS_H[6] MB_DQS_L[6] MB_DQS_H[7] MB_DQS_L[7]

MA_DQS_H[0] MA_DQS_L[0] MA_DQS_H[1] MA_DQS_L[1] MA_DQS_H[2] MA_DQS_L[2] MA_DQS_H[3] MA_DQS_L[3] MA_DQS_H[4] MA_DQS_L[4] MA_DQS_H[5] MA_DQS_L[5] MA_DQS_H[6] MA_DQS_L[6] MA_DQS_H[7] MA_DQS_L[7]

MEM_MA_DQS0 G13, MEM_MA_DQS#0 H13, MEM_MA_DQS1 G16, MEM_MA_DQS#1 G15, MEM_MA_DQS2 C22, MEM_MA_DQS#2 C21, MEM_MA_DQS3 G22, MEM_MA_DQS#3 G21, MEM_MA_DQS4 AD23, MEM_MA_DQS#4 AC23, MEM_MA_DQS5 AB19, MEM_MA_DQS#5 AB20, MEM_MA_DQS6 Y15, MEM_MA_DQS#6 W15, MEM_MA_DQS7 W12, MEM_MA_DQS#7 W13

To SODIMM socket 1

To SODIMM socket 0

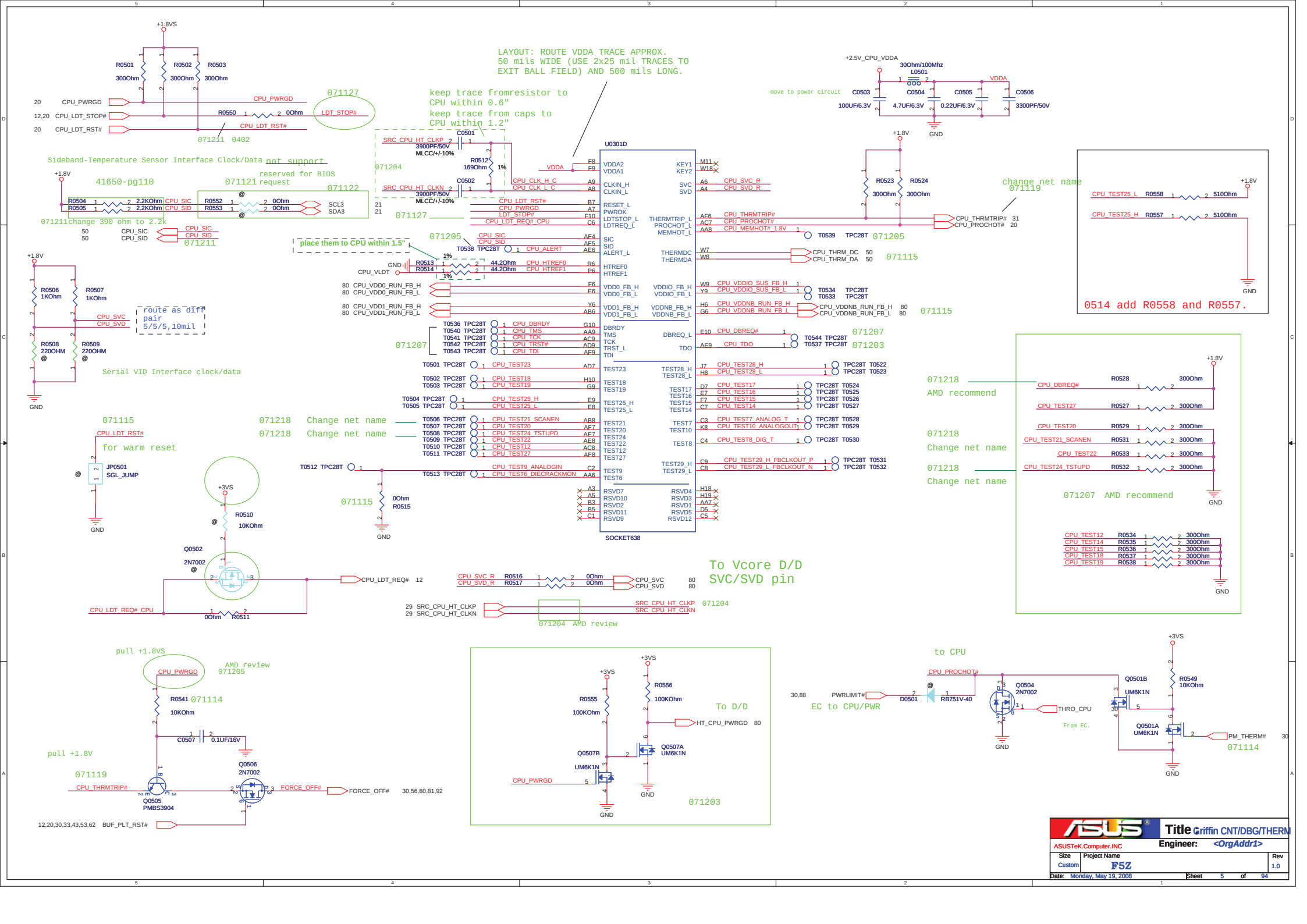
ASUSTeK.Computer.INC

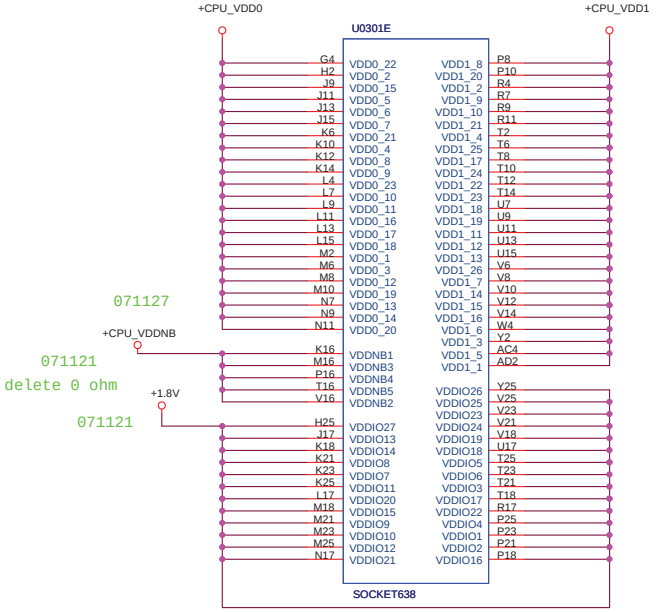
Title : Griffin DDR2 MEM I/F

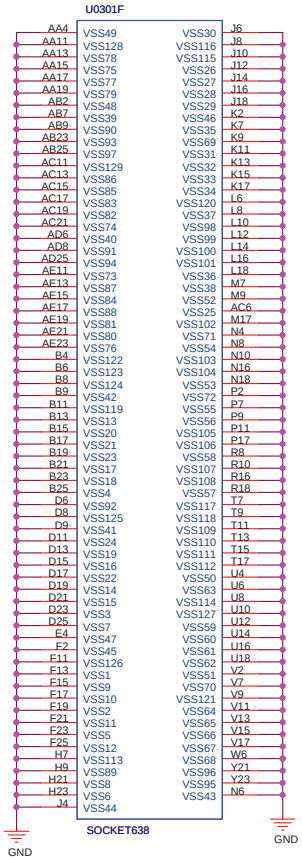
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	1.0

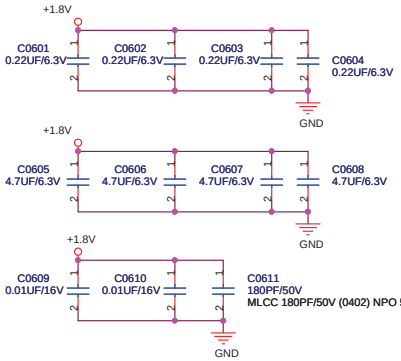
Date: Monday, May 19, 2008 Sheet 4 of 94


LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
U0301D
SOCKET638
+1.8VS
+3VS
+2.5V_CPU_VDDA
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
Sideband-Temperature Sensor Interface Clock/Data
not support
reserved for BIOS
request
change 390 ohm to 2.2k
Serial VID Interface clock/data
route as diff pair 5/5/5,10mil
place them to CPU within 1.5"
for warm reset
change net name
0514 add R0558 and R0557.
AMD recommend
To Vcore D/D SVC/SVD pin
EC to CPU/PWR
To D/D
to CPU
pull +1.8VS
pull +1.8V
AMD review
move to power circuit
ASUSTeK.Computer.INC
Title Griffin CNT/DBG/THERM
Engineer: <OrgAddr1>
Project Name F5Z
Size Custom
Rev 1.0
Date: Monday, May 19, 2008
Sheet 5 of 94

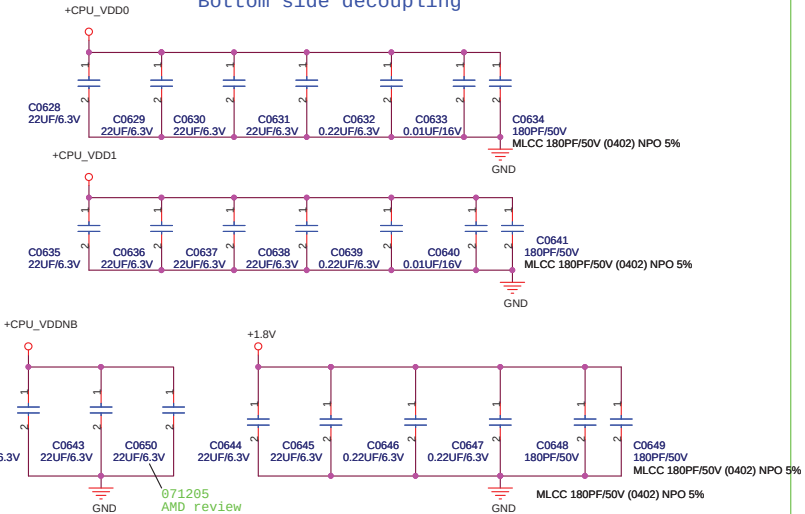




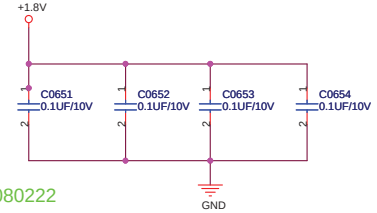
Decoupling between Processor and DIMMs, Place close to Porcessor as possible



Bottom side decoupling

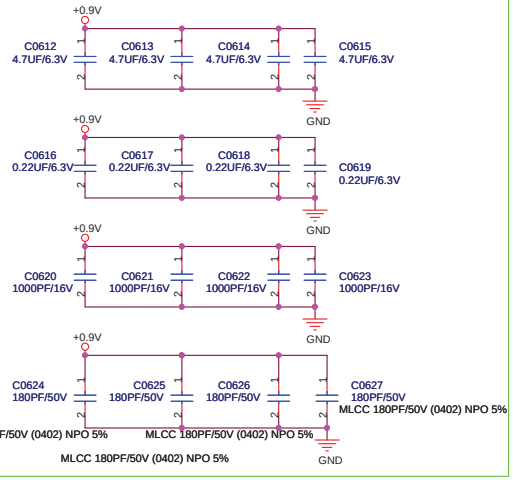


add MLCC 0.1UF/10V (0402) X7R 10% for EMI between +1.8v to GND moat.



080222

place close to socket



ASUSTeK.Computer.INC

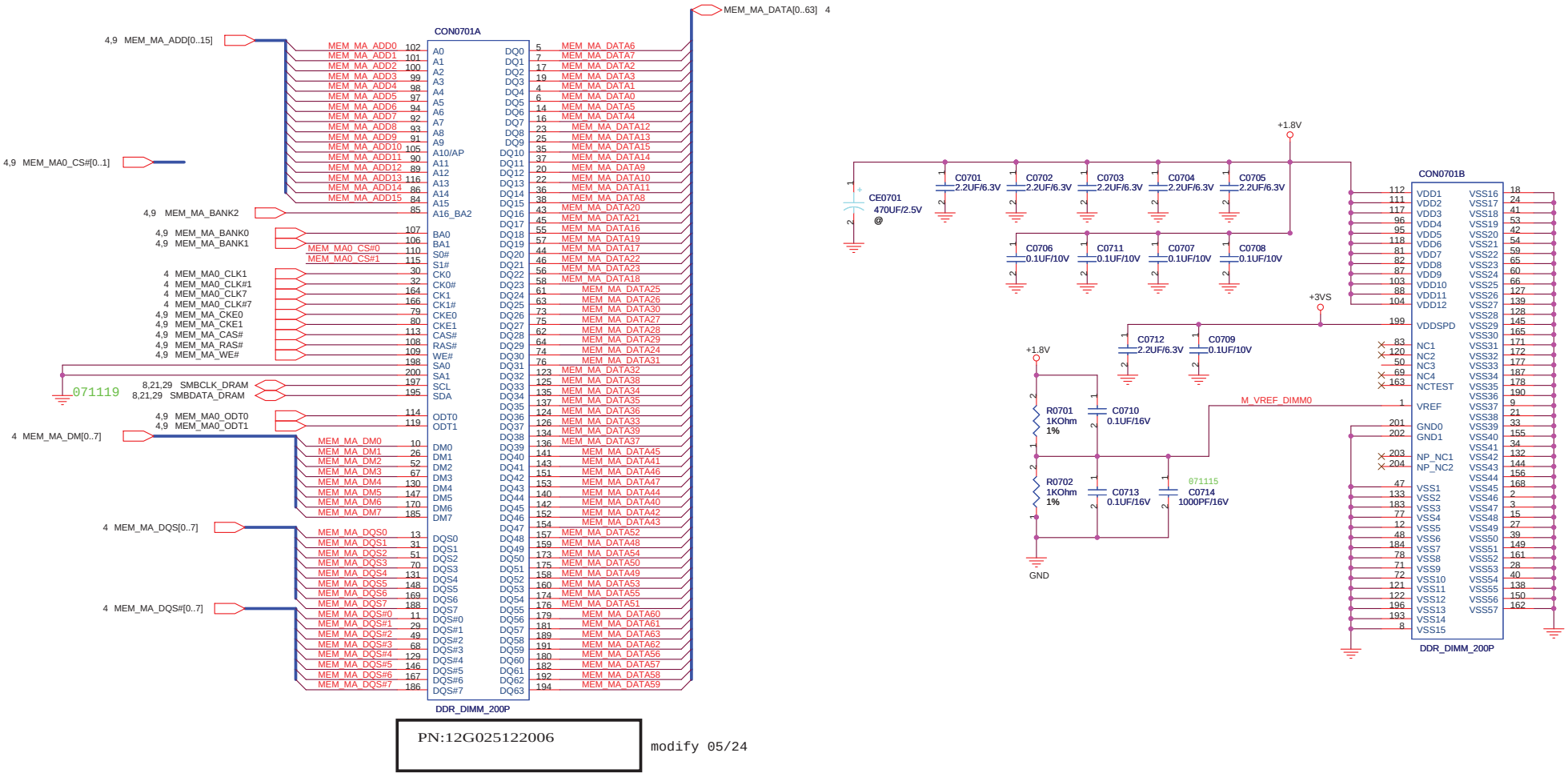
Title : Griffin Power

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 6 of 94

080220
SWAP



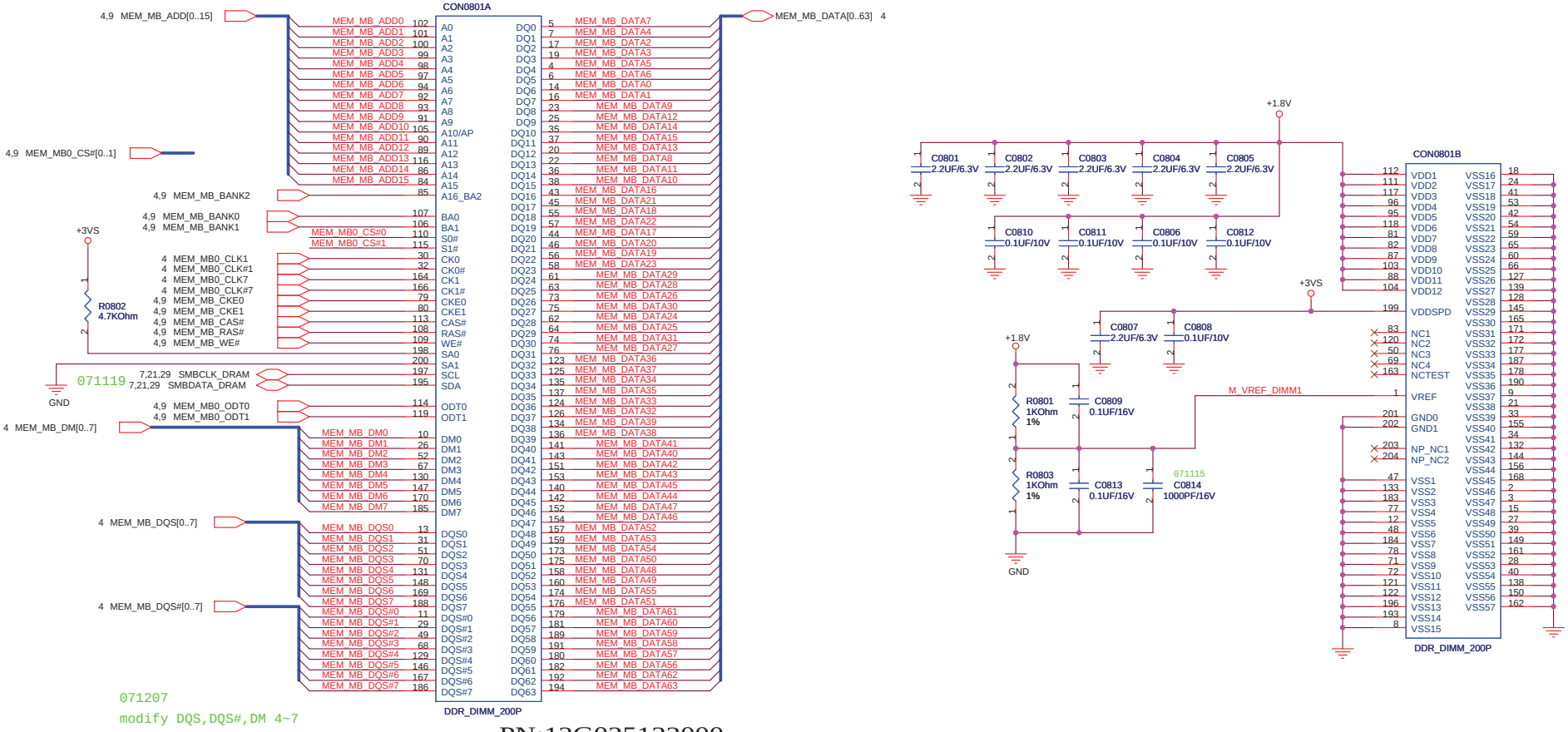
PN:12G025122006

modify 05/24

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM0	
	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 7 of 94	

080221
SWAP



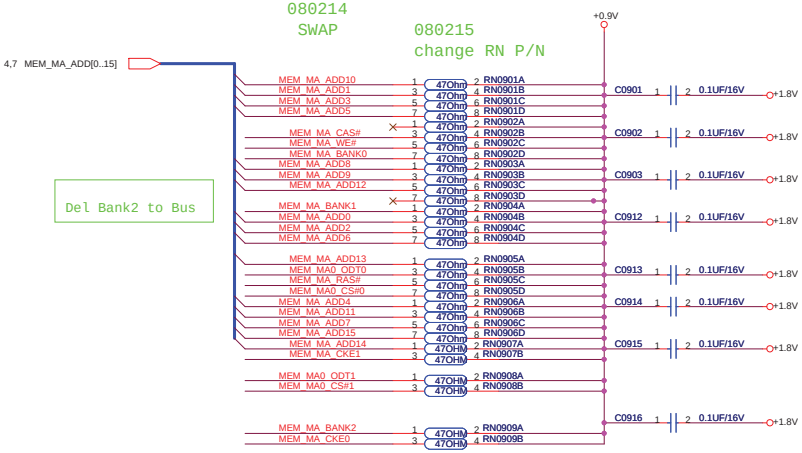
071207
modify DQS,DQS#,DM 4~7

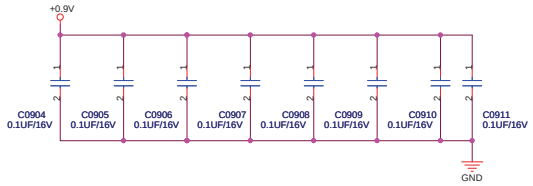
PN:12G025122000

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1		
	Engineer:		
Size: Custom	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 8 of 94		

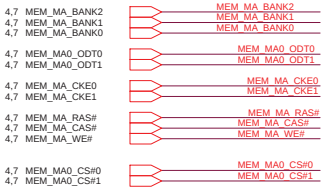
080214
SWAP

080215
change RN P/N





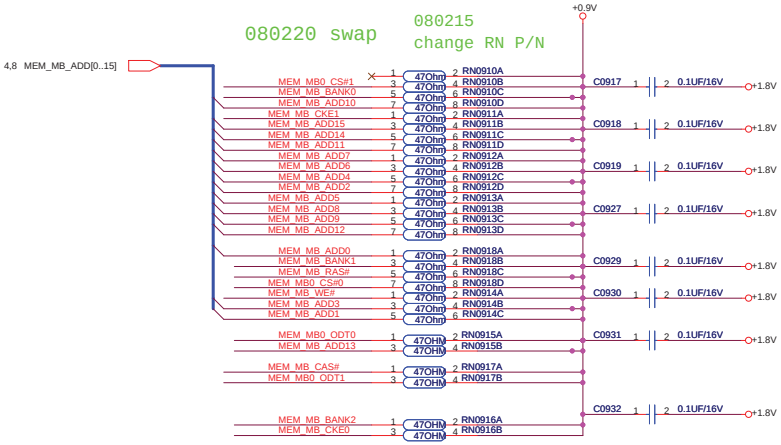
071207

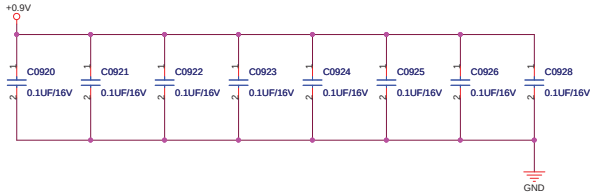


071121

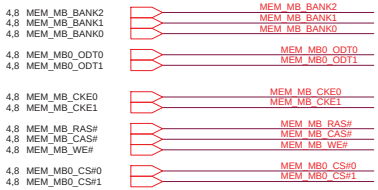
080220 swap

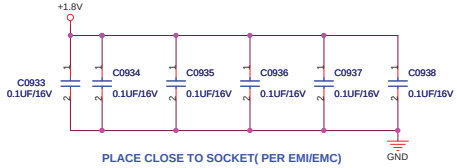
080215
change RN P/N





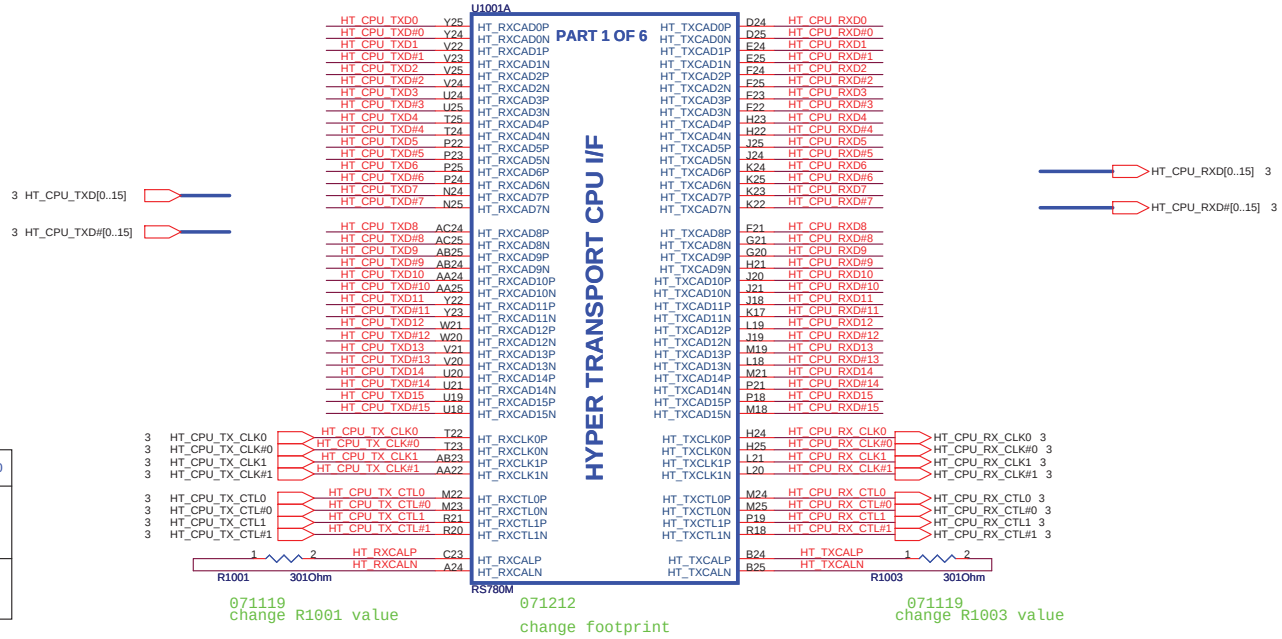
071211





PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC	Title : DDR2_TERMINATIONS	
	Engineer:	
Size: Custom	Project Name: P5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 9 of 94	



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

071119
change R1001 value

071212
change footprint

071119
change R1003 value

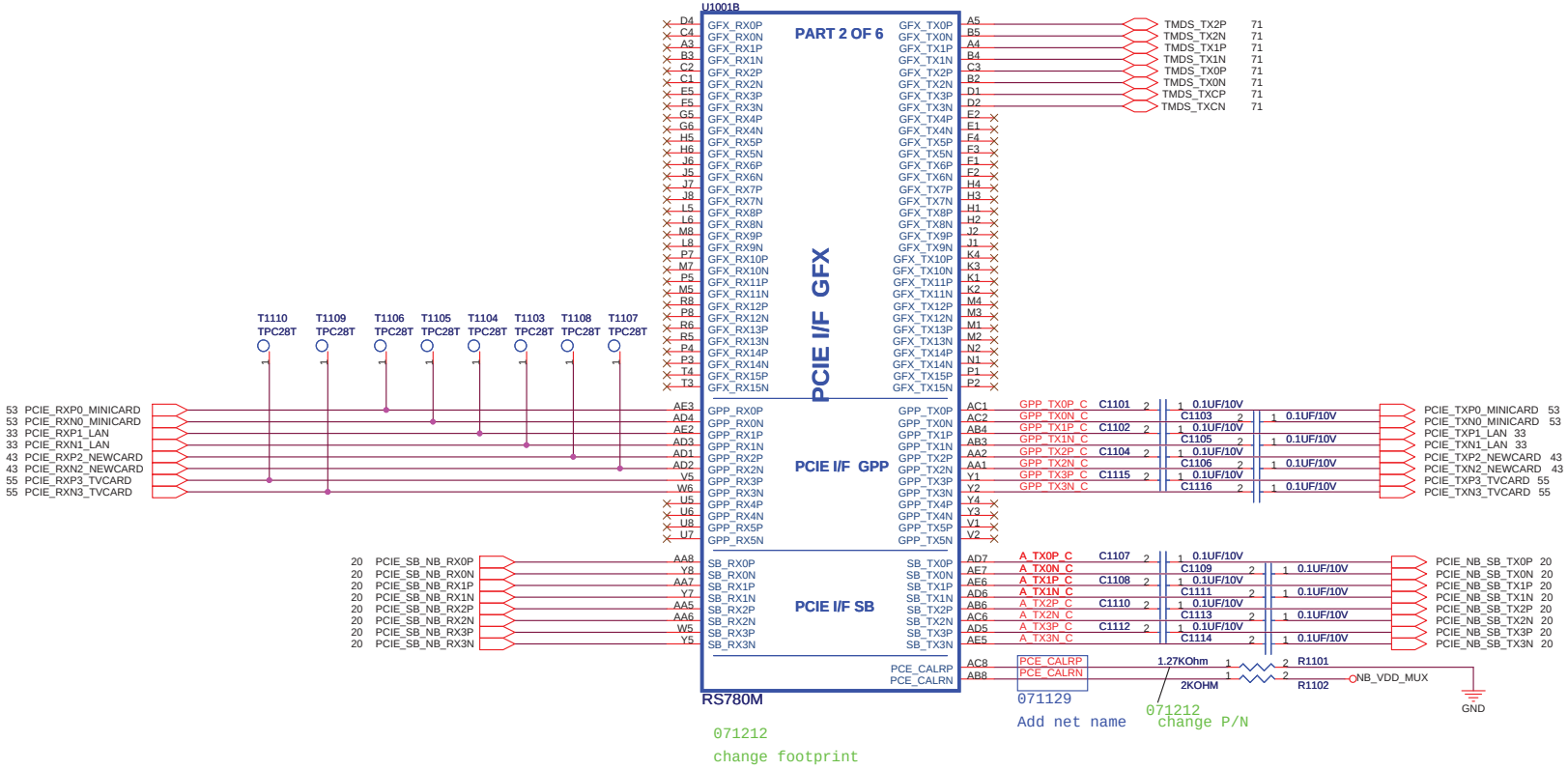
ASUSTeK.Computer.INC

Title : RS780M-HT LINK I/F

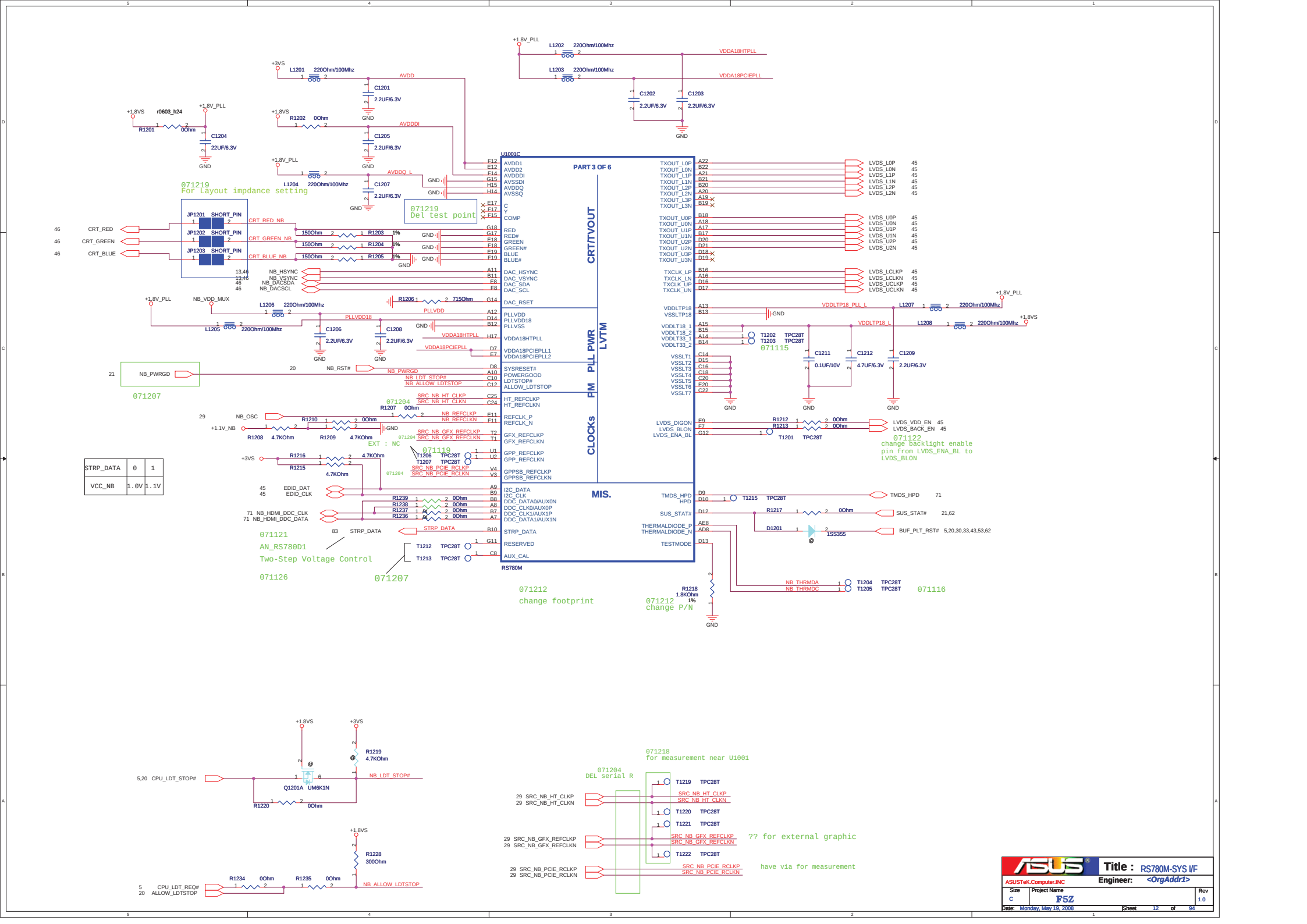
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	1.0

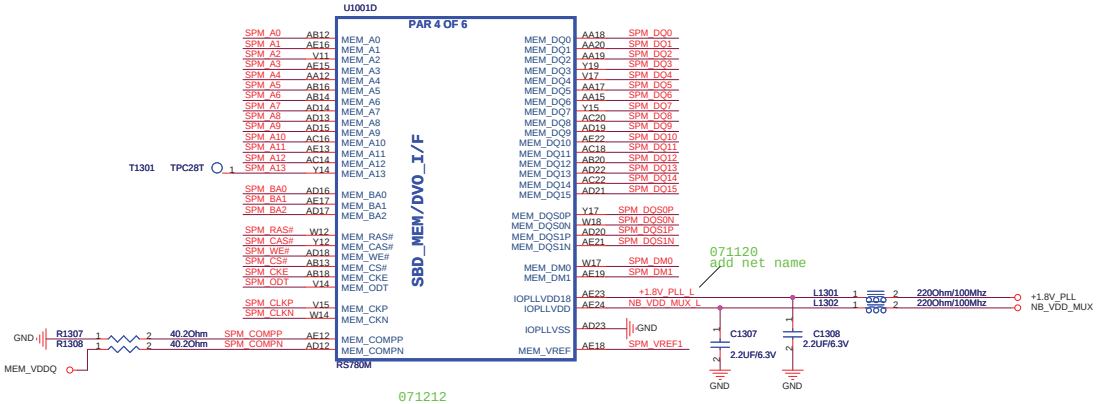
Date: Monday, May 19, 2008 Sheet 10 of 94



ASUSTeK.Computer.INC	Title : RS780M-PCIE LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 11 of 94	


U1001C
PART 3 OF 6
RS780M
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.
AVDD1
AVDD2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
COMP
RED
RED#
GREEN
GREEN#
BLUE
BLUE#
DAC_HSYNC
DAC_VSYNC
DAC_SDA
DAC_SCL
DAC_RSET
PLLVDD
PLLVDD18
PLLVSS
VDDA18HTPLL
VDDA18PCIEPLL
VDDA18PCIEPLL2
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P
REFCLK_N
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP
GPPSB_REFCLKN
I2C_DATA
I2C_CLK
DDC_DATA0/AUX0N
DDC_CLK0/AUX0P
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
STRP_DATA
RESERVED
AUX_CAL
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
VDDLTP18
VSSLTP18
VDDLT18_1
VDDLT18_2
VDDLT33_1
VDDLT33_2
VSSLT1
VSSLT2
VSSLT3
VSSLT4
VSSLT5
VSSLT6
VSSLT7
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
TMDS_HPD
SUS_STAT#
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
+1.8V_PLL
L1202 220Ohm/100Mhz
L1203 220Ohm/100Mhz
VDDA18HTPLL
VDDA18PCIEPLL
C1202 2.2UF/6.3V
C1203 2.2UF/6.3V
GND
+3VS
L1201 220Ohm/100Mhz
AVDD
C1201 2.2UF/6.3V
+1.8VS
r0603_h24
R1201 0Ohm
C1204 22UF/6.3V
R1202 0Ohm
AVDDDI
C1205 2.2UF/6.3V
L1204 220Ohm/100Mhz
AVDDQ_L
C1207 2.2UF/6.3V
071219
For Layout impdance setting
071219
Del test point
JP1201 SHORT_PIN
JP1202 SHORT_PIN
JP1203 SHORT_PIN
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_RED_NB
CRT_GREEN_NB
CRT_BLUE_NB
150Ohm
R1203 1%
R1204 1%
R1205 1%
NB_HSYNC
NB_VSYNC
NB_DACSDA
NB_DACSCL
NB_VDD_MUX
L1206 220Ohm/100Mhz
L1205 220Ohm/100Mhz
R1206 715Ohm
PLLVDD
PLLVDD18
C1206 2.2UF/6.3V
C1208 2.2UF/6.3V
VDDA18HTPLL
VDDA18PCIEPLL
NB_PWRGD
NB_RST#
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
071207
071204
SRC_NB_HT_CLKP
SRC_NB_HT_CLKN
R1207 0Ohm
NB_OSC
R1210 0Ohm
+1.1V_NB
R1208 4.7KOhm
R1209 4.7KOhm
SRC_NB_GFX_REFCLKP
SRC_NB_GFX_REFCLKN
EXT : NC
071119
T1206 TPC28T
T1207 TPC28T
SRC_NB_PCIE_RCLKP
SRC_NB_PCIE_RCLKN
R1216 4.7KOhm
R1215 4.7KOhm
EDID_DAT
EDID_CLK
R1239 0Ohm
R1238 0Ohm
R1237 0Ohm
R1236 0Ohm
NB_HDMI_DDC_CLK
NB_HDMI_DDC_DATA
STRP_DATA
T1212 TPC28T
T1213 TPC28T
071121
AN_RS780D1
Two-Step Voltage Control
071126
071207
071212
change footprint
071212
change P/N
R1218 1.8KOhm 1%
LVDS_L0P
LVDS_L0N
LVDS_L1P
LVDS_L1N
LVDS_L2P
LVDS_L2N
LVDS_U0P
LVDS_U0N
LVDS_U1P
LVDS_U1N
LVDS_U2P
LVDS_U2N
LVDS_LCLKP
LVDS_LCLKN
LVDS_UCLKP
LVDS_UCLKN
VDDLTP18_PLL_L
VDDLTP18_L
L1207 220Ohm/100Mhz
L1208 220Ohm/100Mhz
T1202 TPC28T
T1203 TPC28T
071115
C1211 0.1UF/10V
C1212 4.7UF/6.3V
C1209 2.2UF/6.3V
R1212 0Ohm
R1213 0Ohm
T1201 TPC28T
LVDS_VDD_EN
LVDS_BACK_EN
071122
change backlight enable
pin from LVDS_ENA_BL to
LVDS_BLON
T1215 TPC28T
TMDS_HPD
R1217 0Ohm
SUS_STAT#
D1201 1SS355
BUF_PLT_RST#
NB_THRMDA
NB_THRMDC
T1204 TPC28T
T1205 TPC28T
071116
STRP_DATA
0
1.0V
VCC_NB
1.1V
R1219 4.7KOhm
CPU_LDT_STOP#
Q1201A UM6K1N
R1220 0Ohm
NB_LDT_STOP#
R1228 300Ohm
R1234 0Ohm
R1235 0Ohm
CPU_LDT_REQ#
ALLOW_LDTSTOP
071218
for measurement near U1001
071204
DEL serial R
T1219 TPC28T
T1220 TPC28T
T1221 TPC28T
T1222 TPC28T
?? for external graphic
have via for measurement
ASUSTeK.Computer.INC
Title : RS780M-SYS I/F
Engineer: <OrgAddr1>
Size C
Project Name F5Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 12 of 94

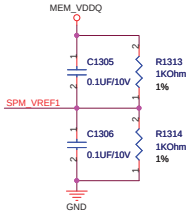
071113

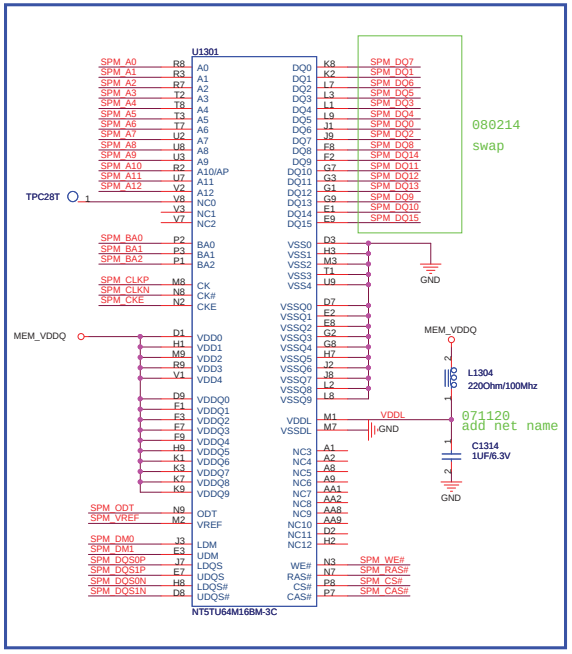


071120
add net name

071212
change footprint

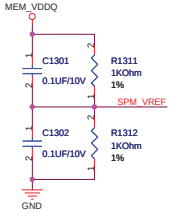
071119





080214
swap

071120
add net name



071212 Change to Naya Pin 92

071218

AMD Qualified

16Mx16 Hynix HY5PS561621AFP-25 asus P/N: 03G15123621 4

32Mx16 Qimonda HYB18T512161B2F-25 asus P/N :03G15133F211

64Mx16 Samsung K4N16164QQ-HC25 asus P/N -

F5Z Use

DFT_GPIO1: LOAD_EEPROM_STRAPS

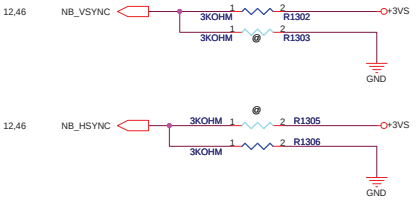
```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

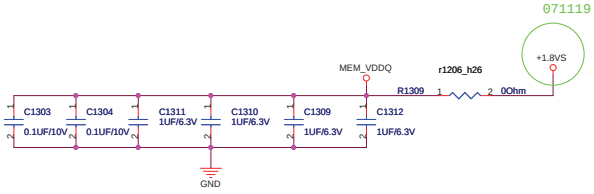
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

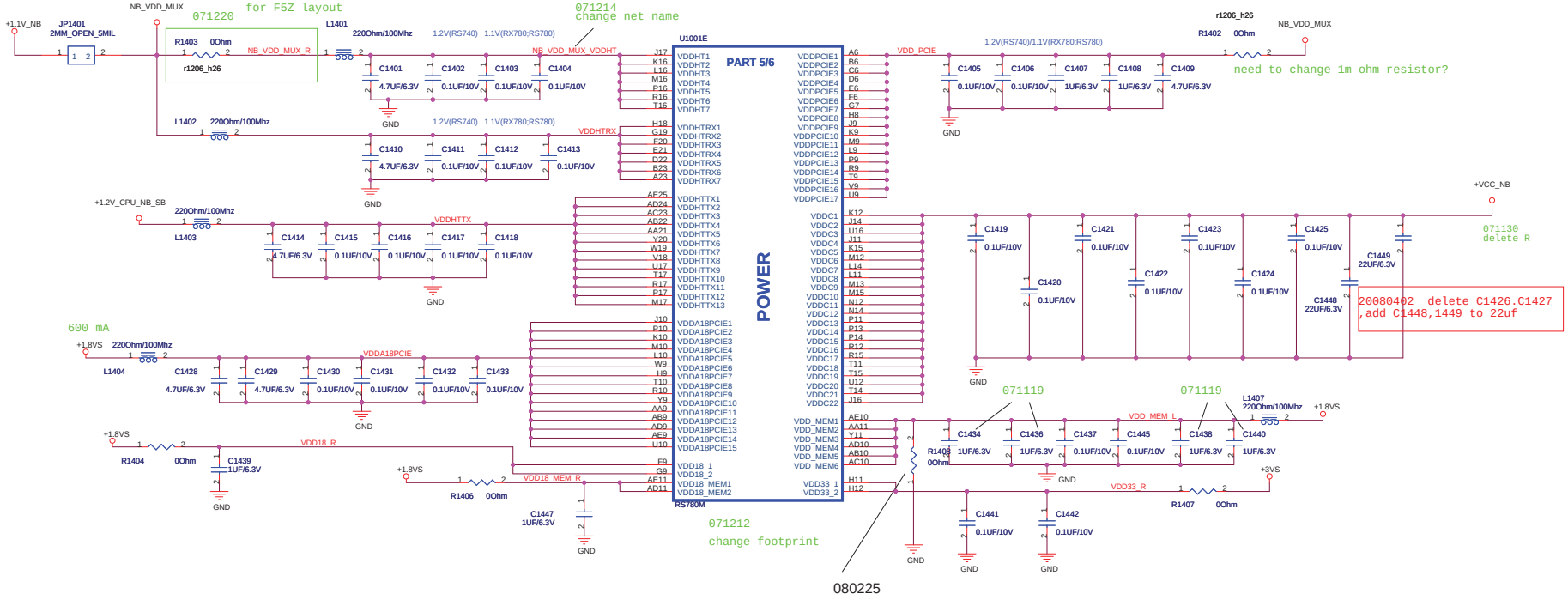
```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

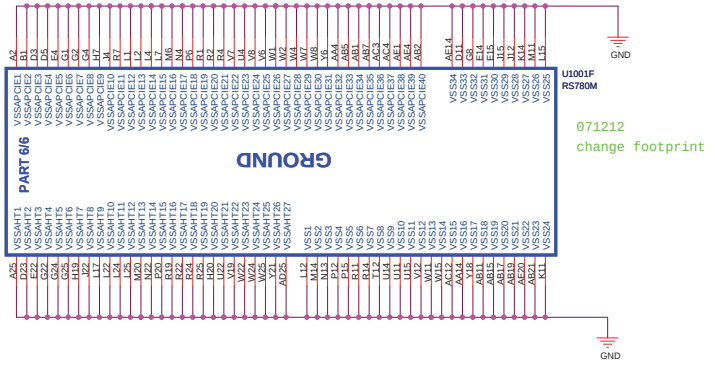


071119

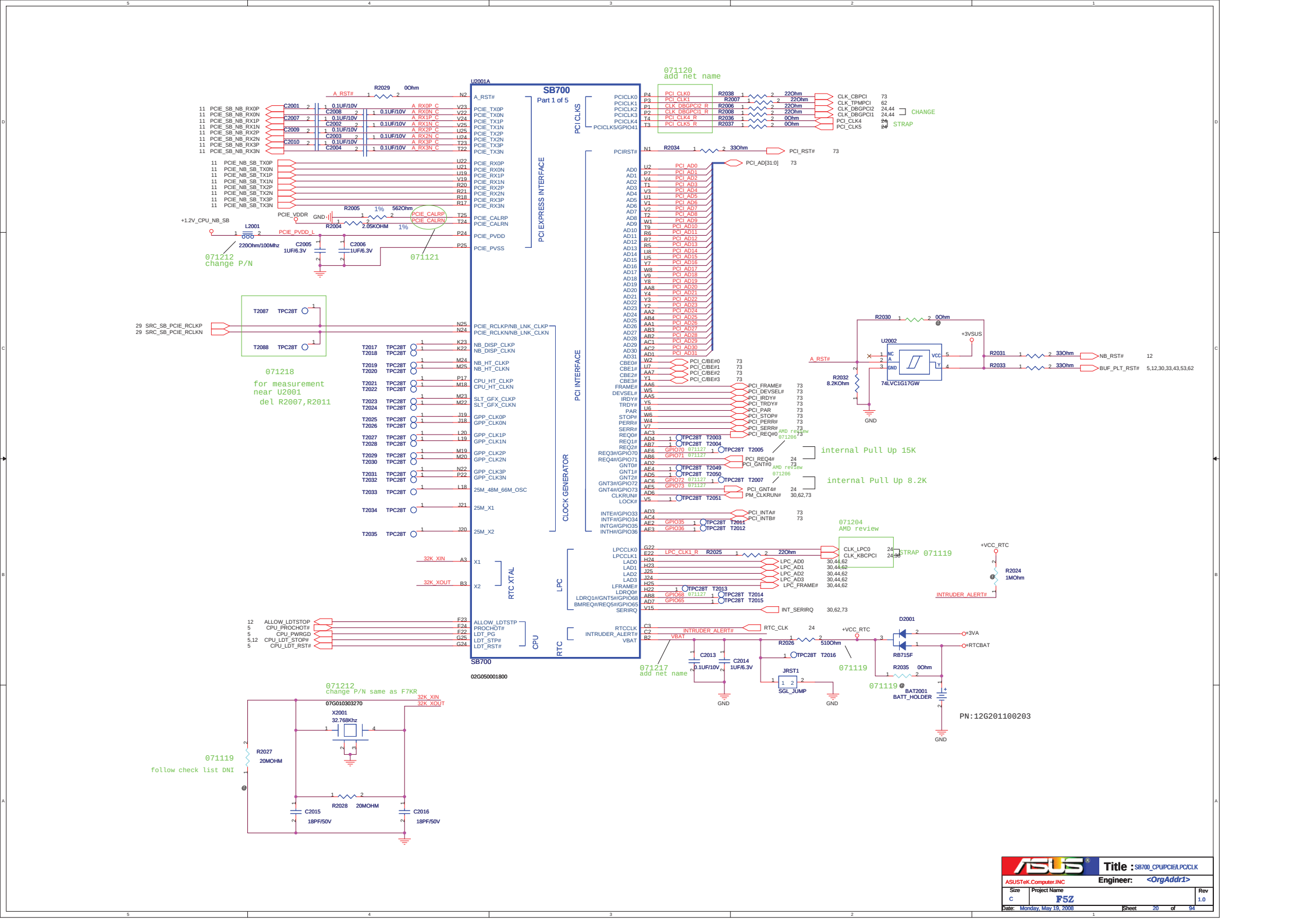


ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 13 of 94		

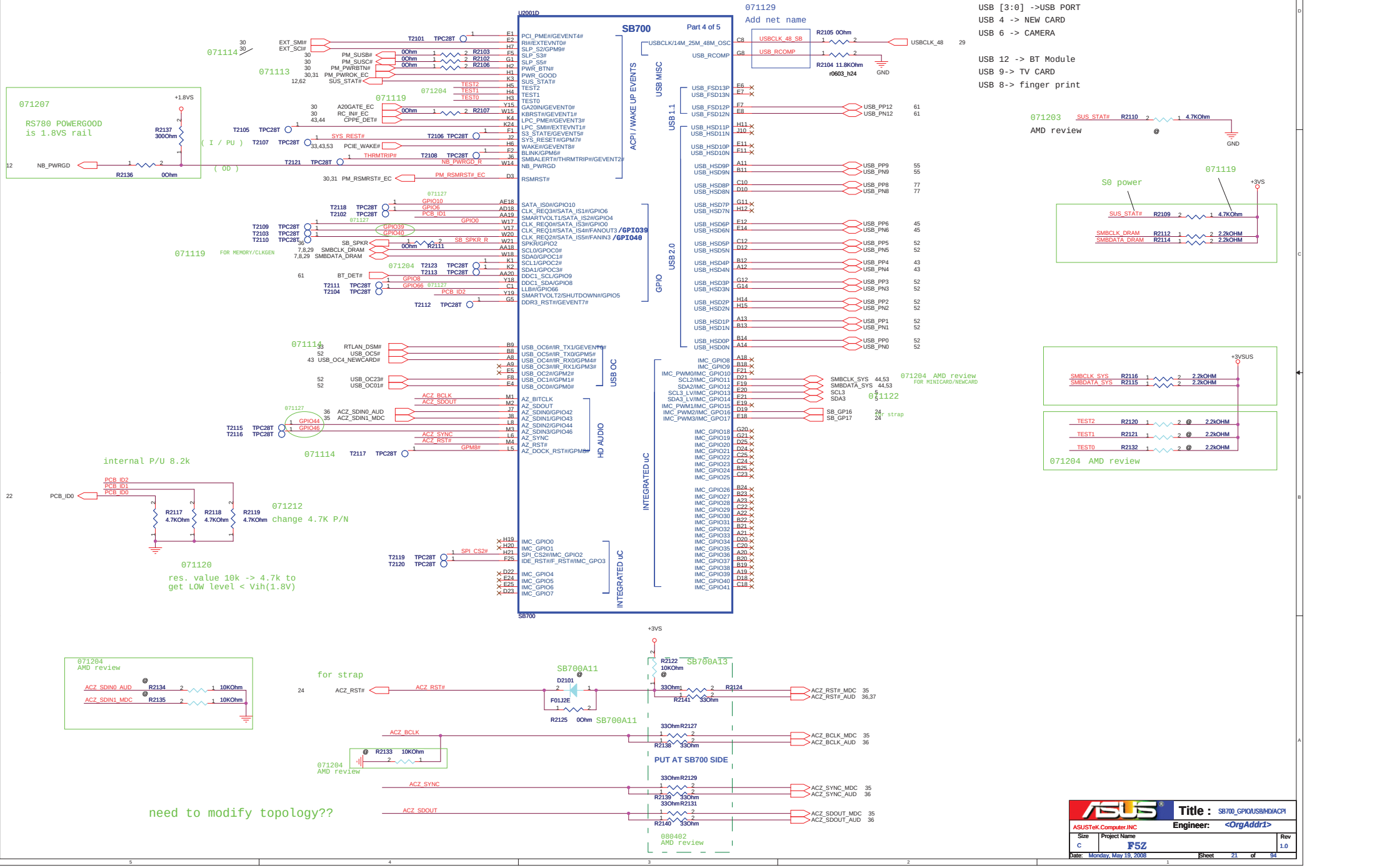


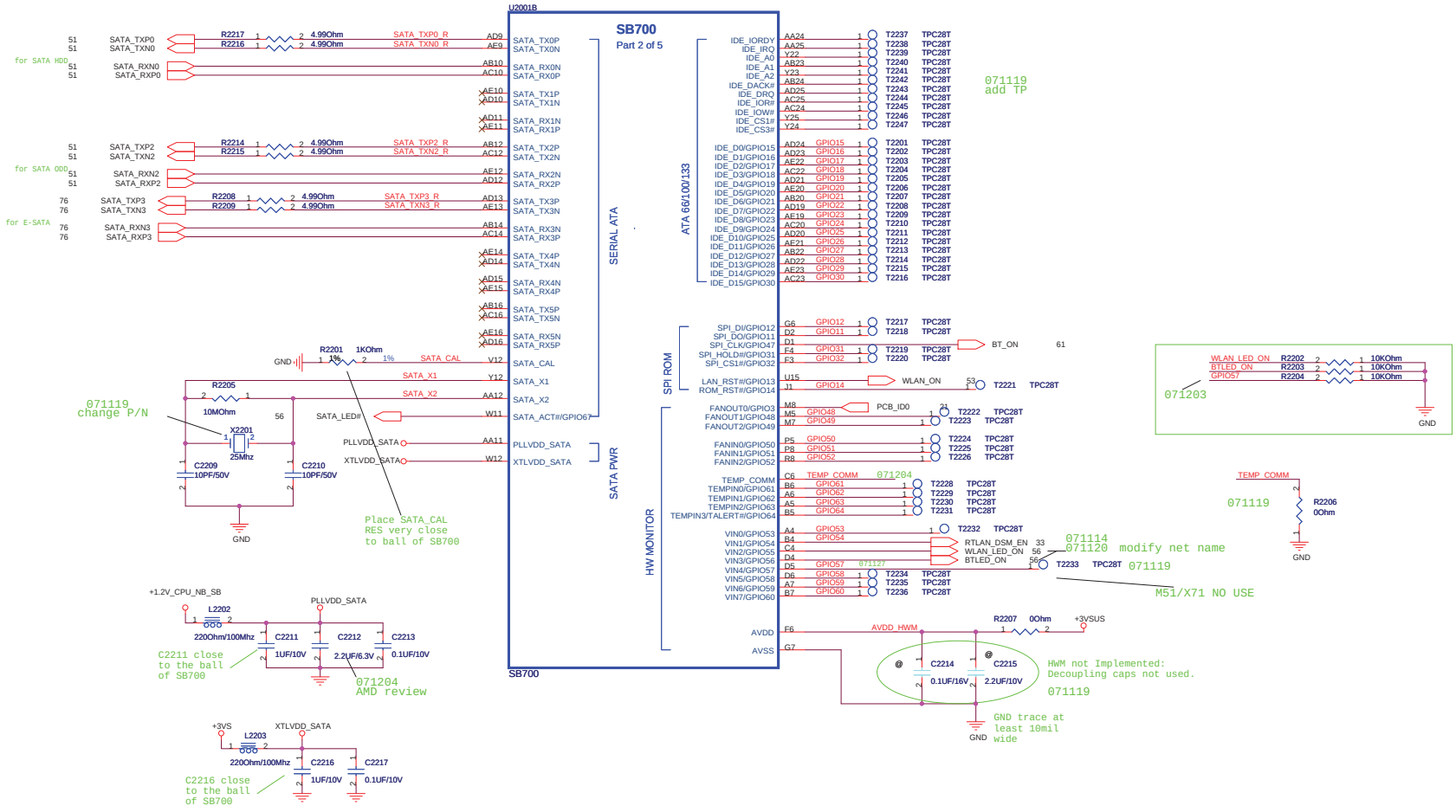


ASUSTeK.Computer.INC	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 14 of 94		

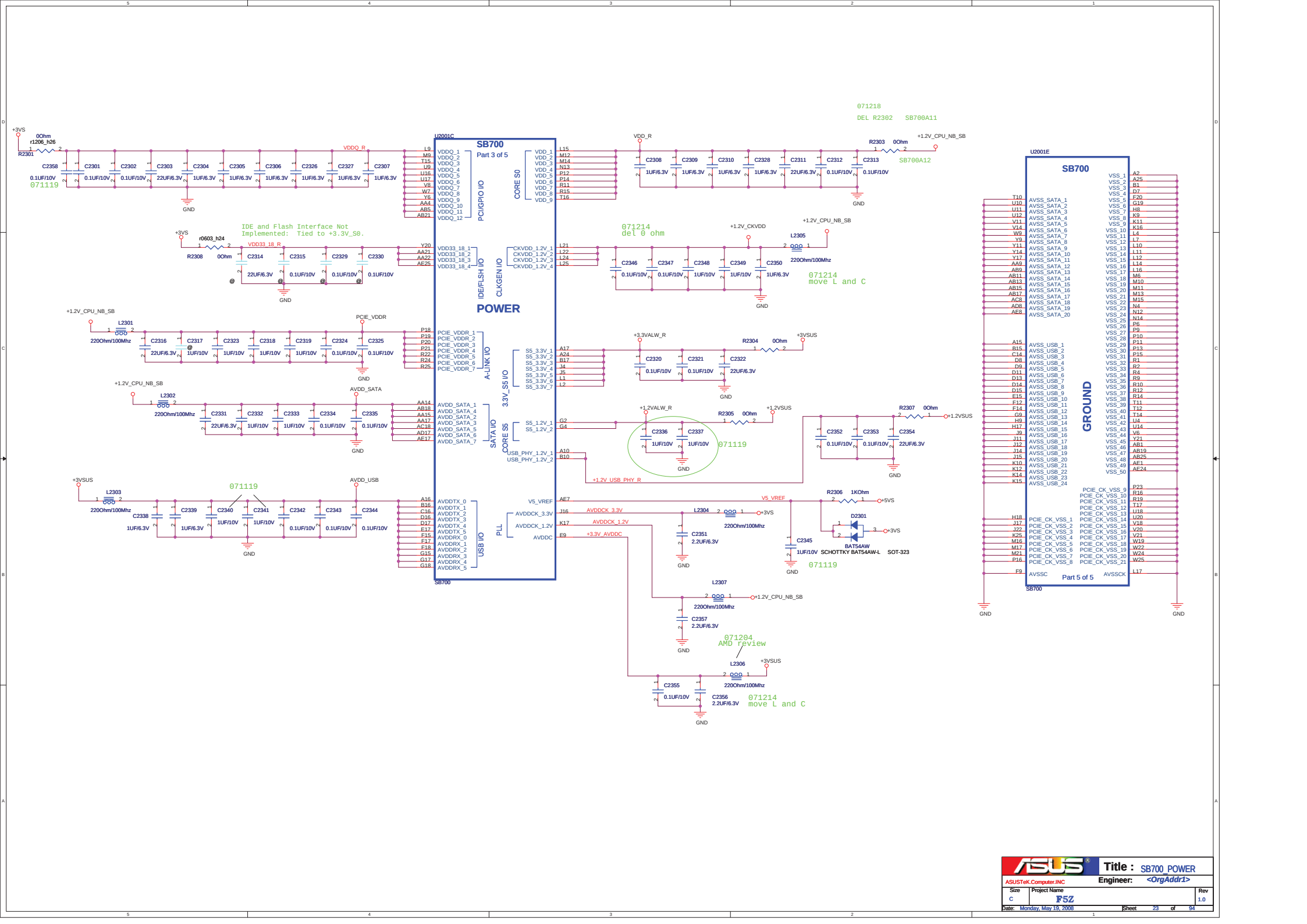


ASUSTeK.COMPUTER.INC	Title : SB700_CPU/PCIE/LPC/CLK		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 20 of 94		

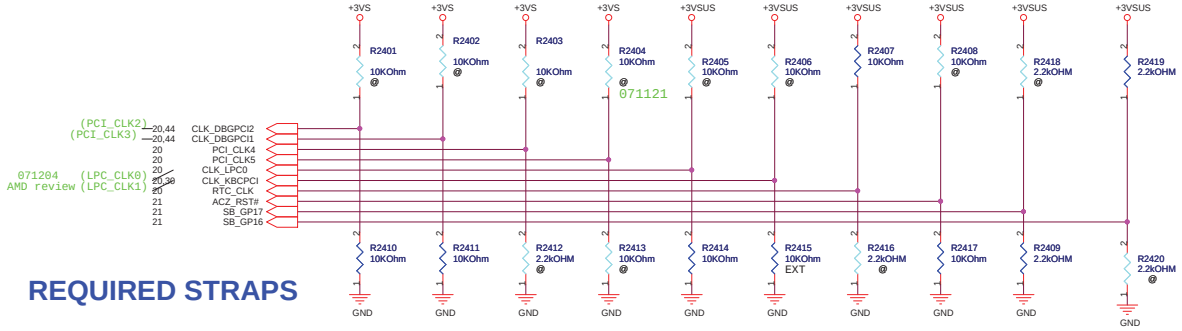

U2001D
SB700
Part 4 of 5
071129
Add net name
USB5->USB PORT
USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 6 -> CAMERA
USB 12 -> BT Module
USB 9-> TV CARD
USB 8-> finger print
071207
RS780 POWERGOOD
is 1.8VS rail
+1.8VS
R2137 300Ohm
R2136 0Ohm
NB_PWRGD
(I / PU)
(OD)
071114
071113
071204
071119
071127
FOR MEMORY/CLKGEN
internal P/U 8.2k
071212
change 4.7K P/N
071120
res. value 10k -> 4.7k to
get LOW level < Vih(1.8V)
071203
AMD review
S0 power
+3VS
+3VSUS
071204 AMD review
FOR MINICARD/NEWCARD
071122
for strap
SB700A11
SB700A13
PUT AT SB700 SIDE
080402
AMD review
need to modify topology??
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3 /GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3 /GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USBCLK_48_SB
R2105 0Ohm
R2104 11.8KOhm
r0603_h24
USBCLK_48
GND
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB_PP12
USB_PN12
USB_PP9
USB_PN9
USB_PP8
USB_PN8
USB_PP6
USB_PN6
USB_PP5
USB_PN5
USB_PP4
USB_PN4
USB_PP3
USB_PN3
USB_PP2
USB_PN2
USB_PP1
USB_PN1
USB_PP0
USB_PN0
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
SMBCLK_SYS
SMBDATA_SYS
SCL3
SDA3
SB_GP16
SB_GP17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
SUS_STAT#
SMBCLK_DRAM
SMBDATA_DRAM
TEST2
TEST1
TEST0
PCB_ID2
PCB_ID1
PCB_ID0
ACZ_BCLK
ACZ_SDOUT
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0_AUD
ACZ_SDIN1_MDC
ACZ_RST#_MDC
ACZ_RST#_AUD
ACZ_BCLK_MDC
ACZ_BCLK_AUD
ACZ_SYNC_MDC
ACZ_SYNC_AUD
ACZ_SDOUT_MDC
ACZ_SDOUT_AUD
Title : SB700_GPIO/USB/HD/ACPI
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F5Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 21 of 94



ASUSTeK.COMPUTER.INC	Title : SB700_PATA/SATA		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 22 of 94		


071218
DEL R2302 SB700A11
SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
IDE and Flash Interface Not Implemented: Tied to +3.3V_S0.
071214 del 0 ohm
071214 move L and C
071119
071204 AMD review
SB700A12
Title : SB700_POWER
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F5Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 23 of 94

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

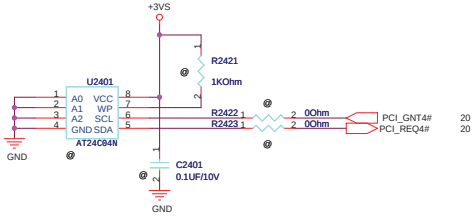


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

071206
AMD review



ASUSTeK.Computer.INC

Title : SB700_STRAP

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 24 of 94

071203
AMD review

071120

C2901 20PF/50V

X2901

14.318Mhz

R2901 10MOhm

C2902 20PF/50V

XTAL1_CLK
XTAL2_CLK

071203
AMD review

GND

+3.3VS_CLK

R2902 10KOhm

Modify to NC

071203

CLK_LAN_REQ# 1 T2901
CLK_NEWCARD_REQ# 1 T2902

PD#

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

071203 IDT

NB_OSC

R2907 200Ohm

R2926 100Ohm

GND

071129
Add net name

NB_OSC_GEN

VDDUSB_CLK

SEL_HTT66

XTAL1_CLK
XTAL2_CLK

21 USBCLK_48

R2908 33Ohm

USBCLK_48_R

071210

7,8,21 SMBCLK_DRAM
7,8,21 SMBDATA_DRAM

VDDA_CLK

U2901

1	REF2/SEL_27	VDDREF	56
2	REF1/SEL_SATA	VDDHTT	55
3	REF0/SEL_HTT66	HTT0T_LPRS/66M	54
4	GNDREF	HTT0C_LPRS/66M	53
5	X1	GNDHTT	52
6	X2	PD#	51
7	VDD48	CPUKG0T_LPRS	50
8	48MHz_0	CPUKG0C_LPRS	49
9	GND48	VDDCPU	48
10	SMBCLK	GNDCPU	47
11	SMBDAT	CLKREQ1#*	46
12	VDD1	VDDA	45
13	SRC4C_LPRS/27MHz_NS	GNDA	44
14	SRC4T_LPRS/27MHz_SS	GND2	43
15	GND1	VDD2	42
16	SRC3C_LPRS	CLKREQ3#*	41
17	SRC3T_LPRS	SB_SRC0T_LPRS	40
18	GNDSRC1	SB_SRC0C_LPRS	39
19	VDDSRC1	VDDSB_SRC	38
20	SRC2C_LPRS	GNDSB_SRC	37
21	SRC2T_LPRS	SB_SRC1T_LPRS	36
22	VDDSRC2	SB_SRC1C_LPRS	35
23	GNDSRC2	ATIG0T_LPRS	34
24	SRC1C_LPRS	ATIG0C_LPRS	33
25	SRC1T_LPRS	VDDATIG	32
26	SRC0C_LPRS	GNDATIG	31
27	SRC0T_LPRS	ATIG1T_LPRS	30
28	*CLKREQ0#	ATIG1C_LPRS	29

ICS9LPRS479AGLFT

53 CLK_PCIE_MINICARD#
53 CLK_PCIE_MINICARD

R2909 0Ohm CLK_PCIE_MINICARD#_GEN
R2910 0Ohm CLK_PCIE_MINICARD_GEN

Add net name 071129

55 CLK_PCIE_TVCARD#
55 CLK_PCIE_TVCARD

R2928 0Ohm CLK_PCIE_TVCARD#_GEN
R2927 0Ohm CLK_PCIE_TVCARD_GEN

+3.3VS_CLK

33 CLK_PCIE_LAN#
33 CLK_PCIE_LAN
43 CLK_PCIE_NEWCARD#
43 CLK_PCIE_NEWCARD

R2913 0Ohm CLK_PCIE_LAN#_GEN
R2914 0Ohm CLK_PCIE_LAN_GEN
R2911 0Ohm CLK_PCIE_NEWCARD#_GEN
R2912 0Ohm CLK_PCIE_NEWCARD_GEN

071212
SRC0/SRC1 swap

43,44 CLK_NEWCARD_REQ#

071212

GND

071203
net wrong connect

071207

+3.3VS_CLK

VDDREF_CLK

SRC_NB_HT_CLKP_GEN R2915 0Ohm SRC_NB_HT_CLKP 12
SRC_NB_HT_CLKN_GEN R2916 0Ohm SRC_NB_HT_CLKN 12

PD#

SRC_CPU_HT_CLKP_GEN R2917 0Ohm SRC_CPU_HT_CLKP 5
SRC_CPU_HT_CLKN_GEN R2918 0Ohm SRC_CPU_HT_CLKN 5

CLK_LAN_REQ# 33

071212

VDDA_CLK

PCIE_MINICARD_CLKREQ#

SRC_NB_PCIE_RCLKP_GEN R2919 0Ohm SRC_NB_PCIE_RCLKP 12
SRC_NB_PCIE_RCLKN_GEN R2920 0Ohm SRC_NB_PCIE_RCLKN 12

SRC_SB_PCIE_RCLKP_GEN R2921 0Ohm SRC_SB_PCIE_RCLKP 20
SRC_SB_PCIE_RCLKN_GEN R2922 0Ohm SRC_SB_PCIE_RCLKN 20
SRC_NB_GFX_REFCLKP_GEN R2923 0Ohm SRC_NB_GFX_REFCLKP 12
SRC_NB_GFX_REFCLKN_GEN R2924 0Ohm SRC_NB_GFX_REFCLKN 12

071129
Add net name

+3.3VS_CLK

R2906 4.7KOhm

SEL_HTT66

R2925 8.2KOhm

071120
change 4.7k->8.2k

GND

PCIE_MINICARD_CLKREQ#

R2905 0Ohm

071203
SRC3 control by BIOS

GND

Change from 489 to 479

500mA+50mA

+3VS L2904 600Ohm/100Mhz +3.3VS_CLK

C2909 0.1UF/16V
C2910 0.1UF/16V
C2911 0.1UF/16V
C2912 0.1UF/16V

071203
AMD review

C2913 22UF/6.3V
C2914 0.1UF/16V
C2915 0.1UF/16V
C2916 0.1UF/16V
C2917 0.1UF/16V

GND

50mA

+3VS L2901 600Ohm/100Mhz VDDUSB_CLK

C2903 2.2UF/10V
C2904 0.1UF/16V

071203
AMD review

071207
IDT recommend

+3VS L2902 600Ohm/100Mhz VDDREF_CLK

C2905 2.2UF/10V
C2906 0.1UF/16V

071207

50mA

+3VS L2903 600Ohm/100Mhz VDDA_CLK

C2907 22UF/6.3V
C2908 0.1UF/16V

071203
AMD review

<Variant Name>

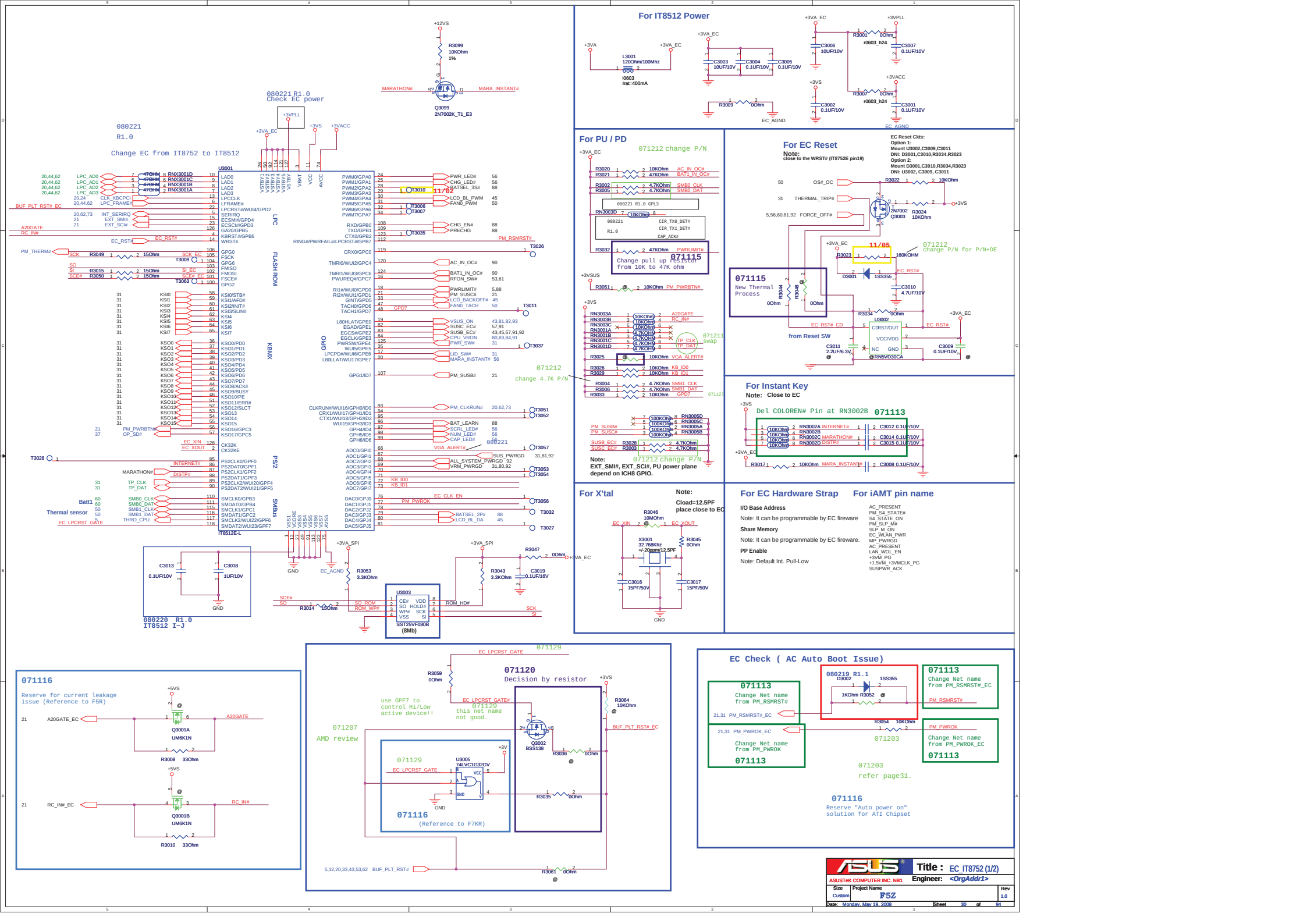
ASUSTeK COMPUTER INC

Title : ICS9LPRS489AGLFT

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 29 of 94

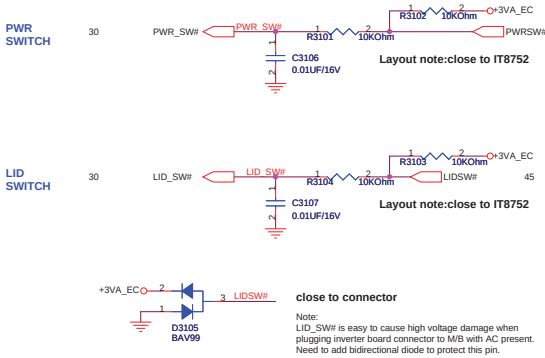

080221 R1.0
Check EC power
080221
R1.0
Change EC from IT8752 to IT8512
U3001
IT8512E-L
080220 R1.0
IT8512 I~J
For IT8512 Power
For PU / PD
071212 change P/N
11/02
Change pull up resistor from 10K to 47K ohm
071115
New Thermal Process
For EC Reset
Note:
close to the WRST# (IT8752E pin19)
EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011
11/05
071212
change P/N for P/N+DE
For Instant Key
Note: Close to EC
Del COLOREN# Pin at RN3002B
071113
For X'tal
Note:
Cload=12.5PF
place close to EC
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
071116
Reserve for current leakage issue (Reference to FSR)
Q3001A
UM6K1N
Q3001B
UM6K1N
071120
Decision by resistor
071129
use GPF7 to control Hi/Low active device!!
this net name not good.
071207
AMD review
071116
(Reference to F7KR)
EC Check (AC Auto Boot Issue)
080219 R1.1
071113
Change Net name from PM_RSMRST#
Change Net name from PM_PWROK
Change Net name from PM_RSMRST#_EC
Change Net name from PM_PWROK_EC
071203
refer page31.
071116
Reserve "Auto power on" solution for ATI Chipset
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size: Custom
Project Name: F52
Rev: 1.0
Date: Monday, May 19, 2008
Sheet 30 of 94

For Battery

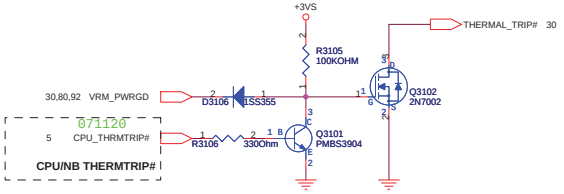
Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

In Page 60

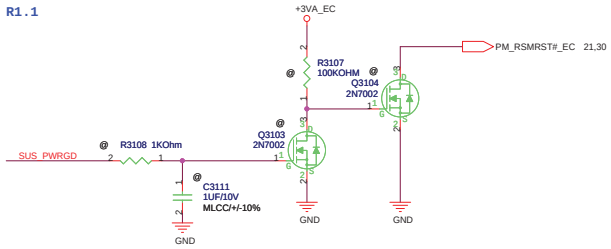
For Switch



For Thermal Control Method



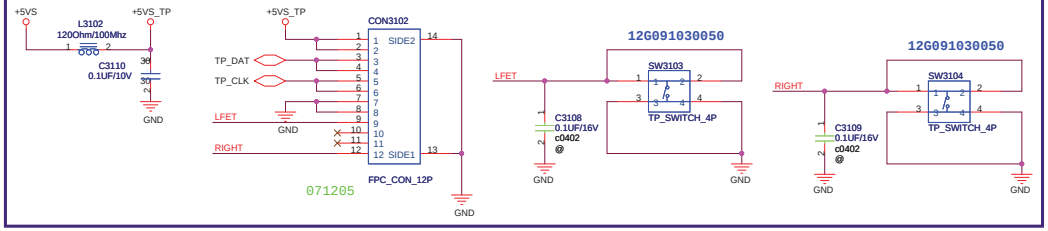
R1.1



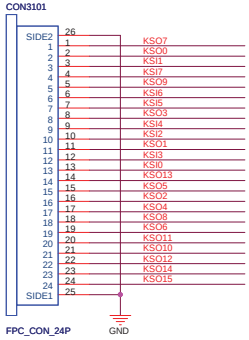
080219 Q3103 & Q3104 pin2 and pin3 Reverse

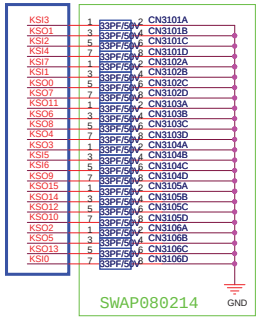
080219 Reserve for SB700 interface

Touch-Pad (F7se)



Keyboard Connector (F7se)





ASUSTeK COMPUTER INC. NB1	Title : EC_IT8511 (2/2)		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 31 of 94		

ALL Follow Design IP

071119 Add net name

close to IC 200 mil

071113

Add net name

close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%
close to L3301 with in 200 mil

60 mil

071212 change P/N

071130 Add L3304

071130 Add R3318

40mil

Add DSM function

Reserved DSM Function

Change to 2N7002

40 mil

071212 change P/N

40mil

CONNECT TO 3.3V ENABLE
;0V TO DISABLE SWIRTCHING REGULATOR

close to pin63 within 200 mil

close to pin64

071120 Reserved

Pin.33 is Clkreq# pin similar to Clkrun function in the PCI interface. If this function not implemented, make this pin floating or connect to the ground.

To Transformer

To SB

From SB

071121 close to LAN CHIP To SB

071129 Correct net name

From Clock Gen.

From SB

071217 Base on Design IP

25MHz Crystal

<Variant Name>

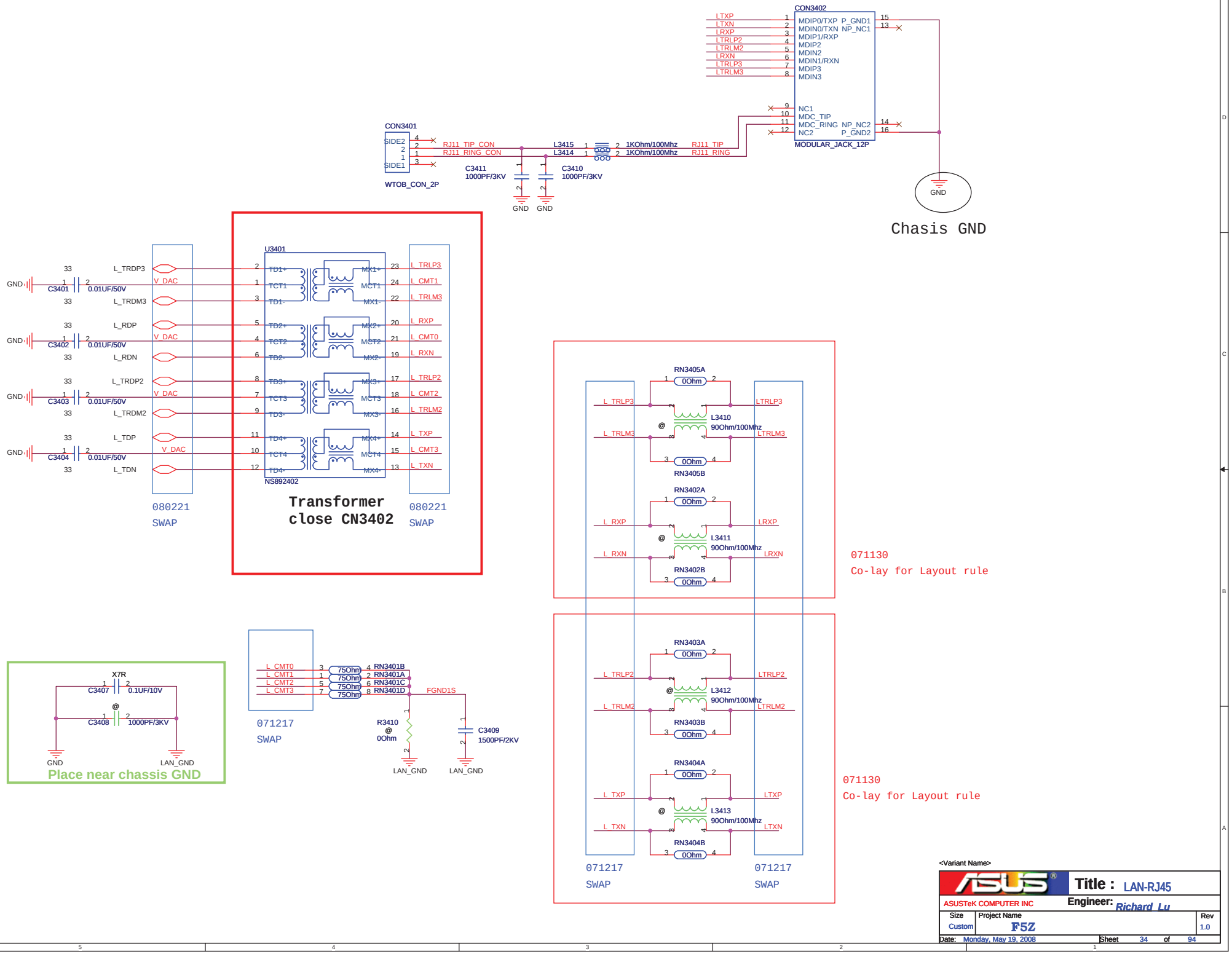
Title : LAN-RTL8111C

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 33 of 94



<Variant Name>

ASUSTeK COMPUTER INC

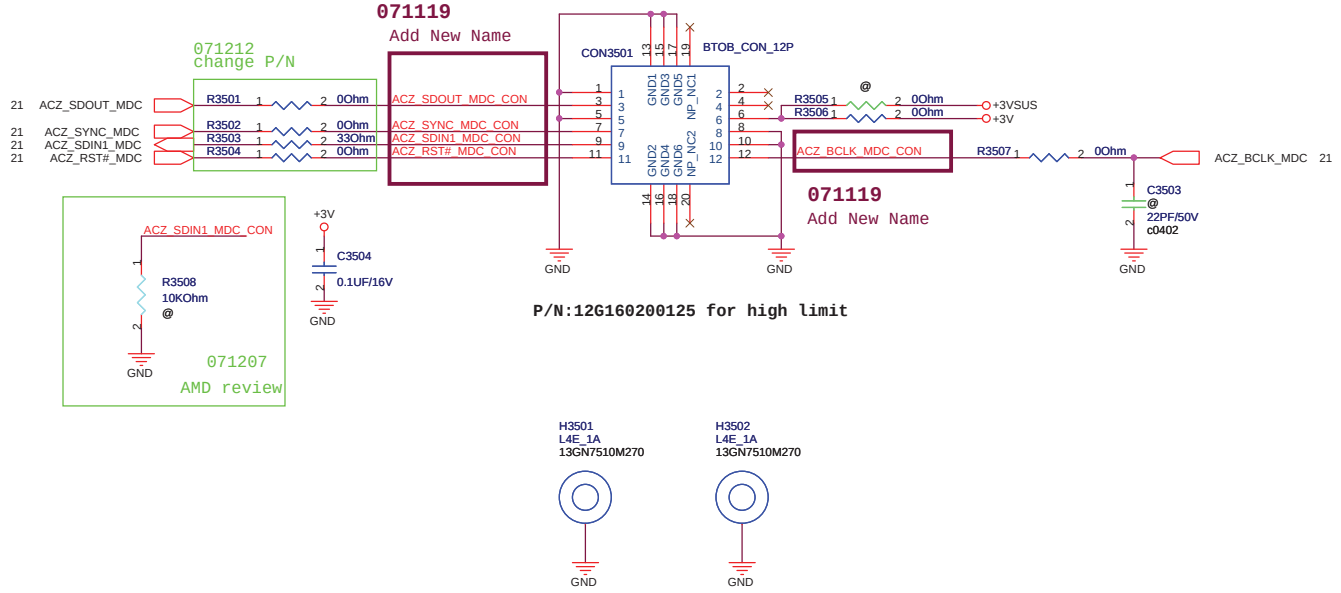
Title : LAN-RJ45

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 34 of 94

MDC



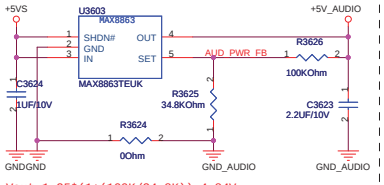
<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN-MDC	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 35 of 94	

ALC663		
	Mount	R3614,R3674,R3675,RX3612,RX3613,R3618,R3613,R3612,C3629,C3608
	NO Mount	R3672,R3673,R3631,R3632,R3608

AUDIO POWER

080519



Vout=1.25*(1+(100K/34.8K))=4.84V
Vdrop about 150mV@100mA
2nd source:GMT G923 470T1UF SOT23-5
(P/N:06G007342012)

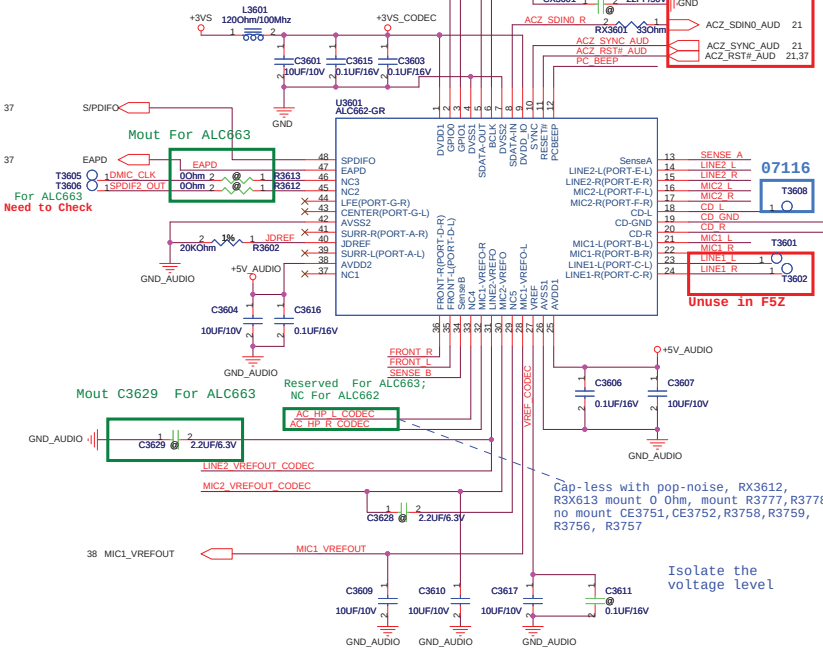
CODEC:ALC662 / ALC663

Mount R3614 For ALC663 ;
Mount R3617 For ALC662

Need to Check

Digital

FROM ICH



Mout For ALC663

Mout C3629 For ALC663

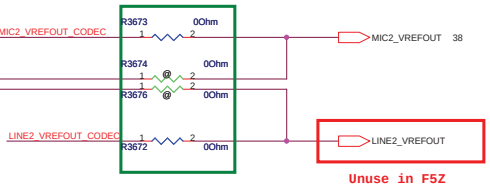
Reserved For ALC663;
NC For ALC662

Cap-less with pop-noise, RX3612,
R3X613 mount 0 Ohm, mount R3777,R3778
no mount CE3751,CE3752,R3758,R3759,
R3756, R3757

Isolate the
voltage level

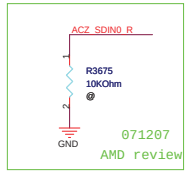
Mout R3674 and R3676 For ALC663 ;
Mount R3673 and R3672 For ALC662;

07116



Unuse in F5Z

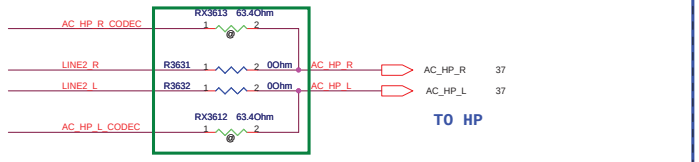
Unuse in F5Z

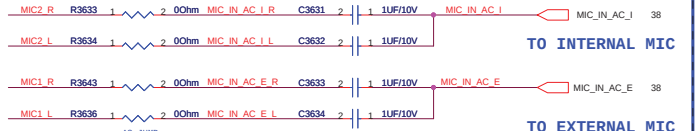


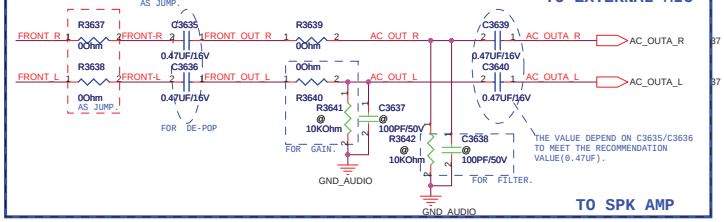
071207
AMD review

FOR NORMAL FUNCTION .

Mount RX3613 and RX3612 For ALC663;
Mount R3632 and R3631 For ALC632;



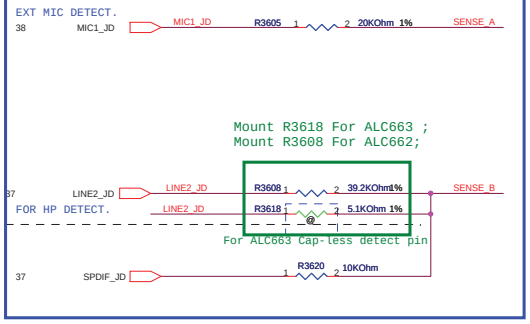




07116

Del Audio DJ Function

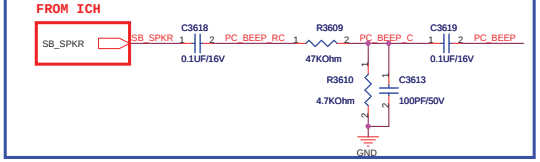
DETECTION

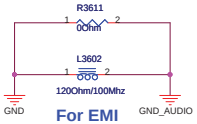


PC BEEP

Reserve for Cardbus
controllor that has
PCMCIA function.

IF NO PCMCIA,DNI IT.

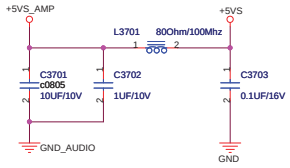




<Variant Name>

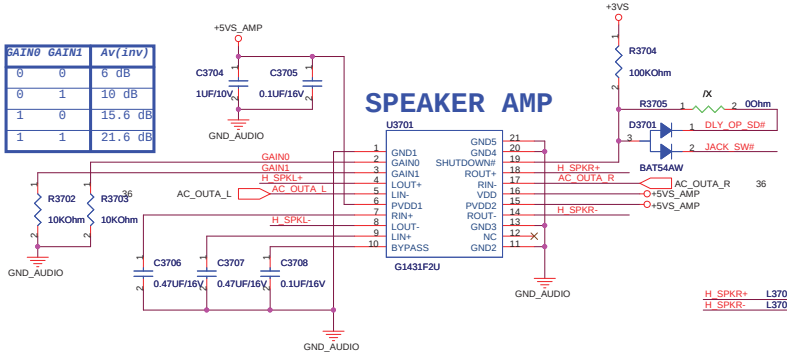
ASUSTeK COMPUTER INC.	Title : CODEC-ALC662	
	Engineer: Richard_Lu	
Size: C	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 36 of 94	

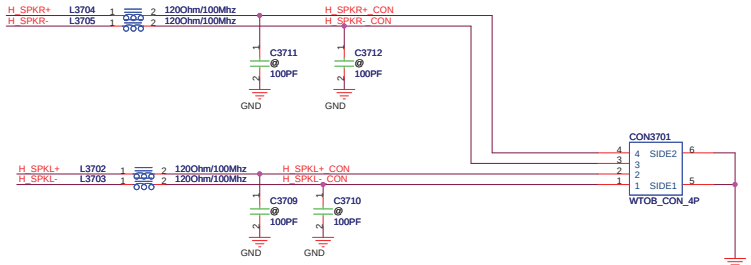
AMP POWER



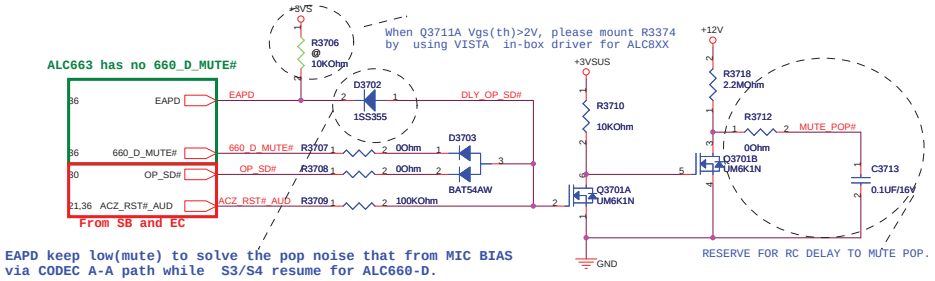
SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



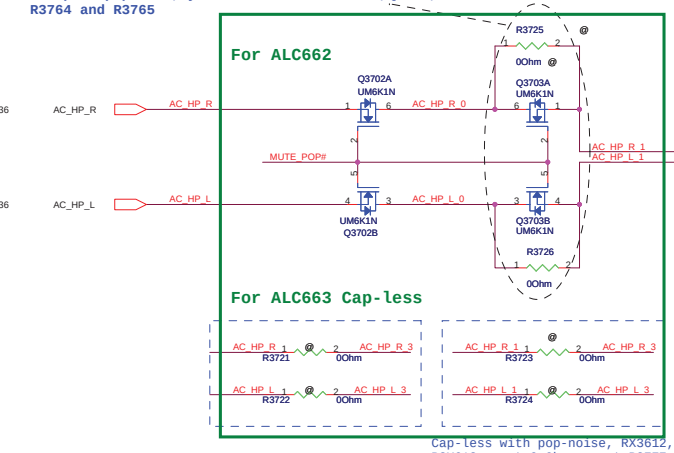


MUTE CONTROL



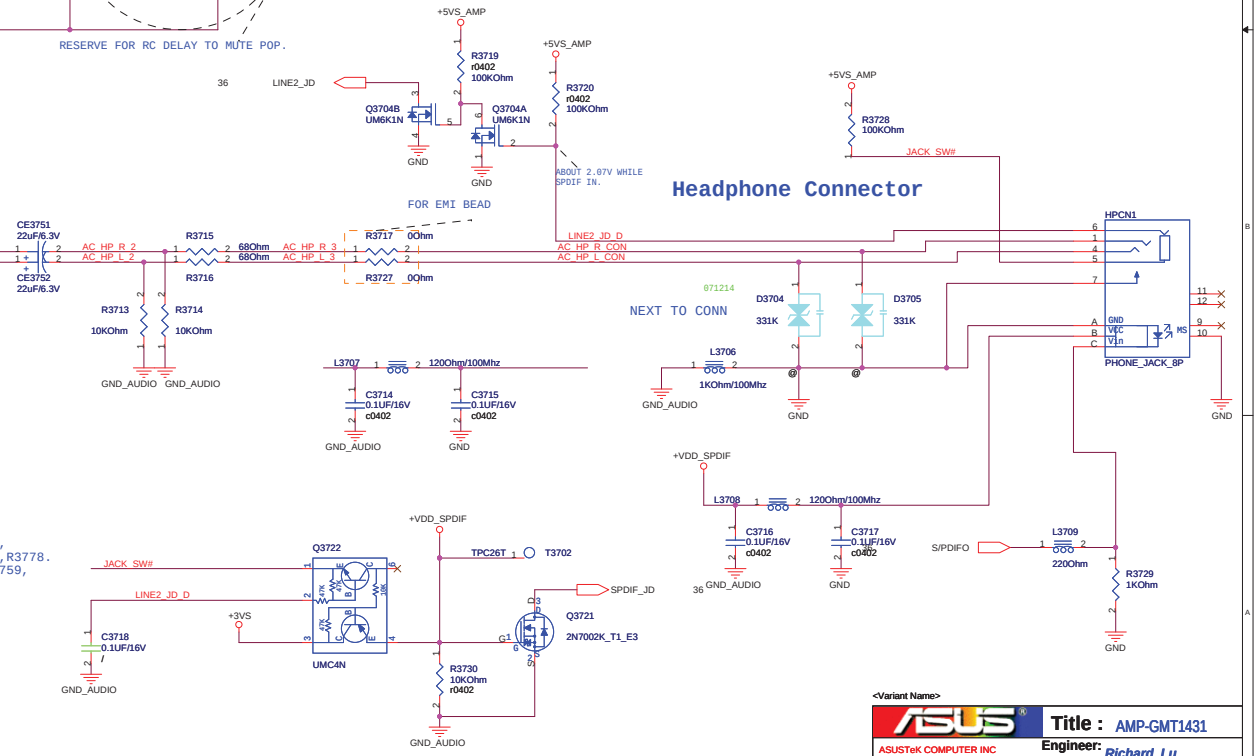
EAPD keep low(mute) to solve the pop noise that from MIC BIAS via CODEC A-A path while S3/S4 resume for ALC660-D.
Base on pop noise by each model.if your model do not care the A-A path pop-nose, you can not mount D3711,Q3755,but mount R3764 and R3765

TYPE	LINE_OUT	S/PDIF_OUT	NC
LINE2_JD_D	L	H	H
JACK_SW#	L	L	H



For ALC663 Cap-less,mount R3775,R3776,RX3612,RX3613

Cap-less with pop-noise, RX3612, R3X613 mount 0 Ohm, mount R3777,R3778. no mount CE3751,CE3752,R3758,R3759, R3756, R3757



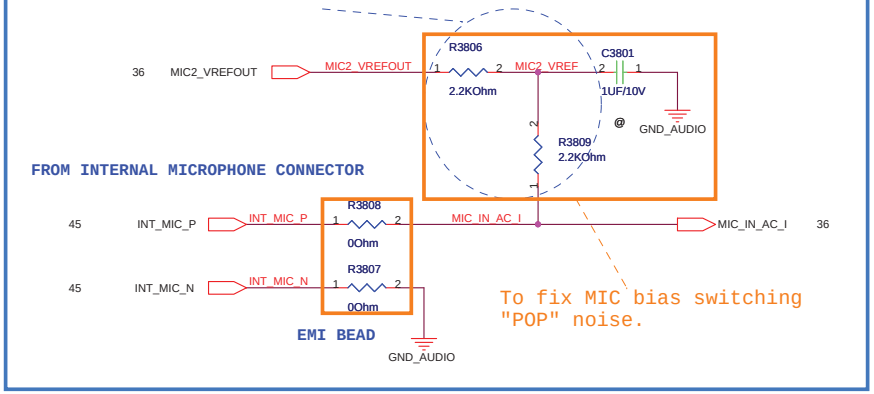
<Variant Name>

ASUSTeK COMPUTER INC	Title : AMP-GMT1431	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 37 of 94	

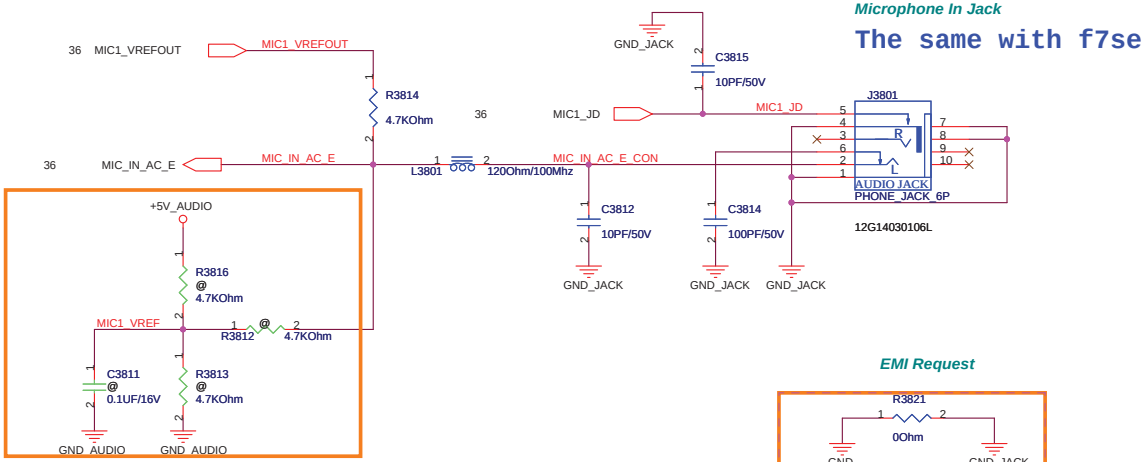
071116 Change form F5R to Design IP

INTERNAL MICROPHONE

If EAPD available(fix MIC bias switching "POP" noise):
Replace R3801,R3802 by one 4.7K ohm resistor.
DNI C3801.



EXTERNAL MICROPHONE



Reserved the external MIC bias(T filter).

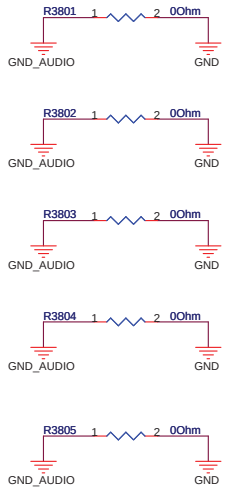
Microphone In Jack

The same with f7se

EMI Request

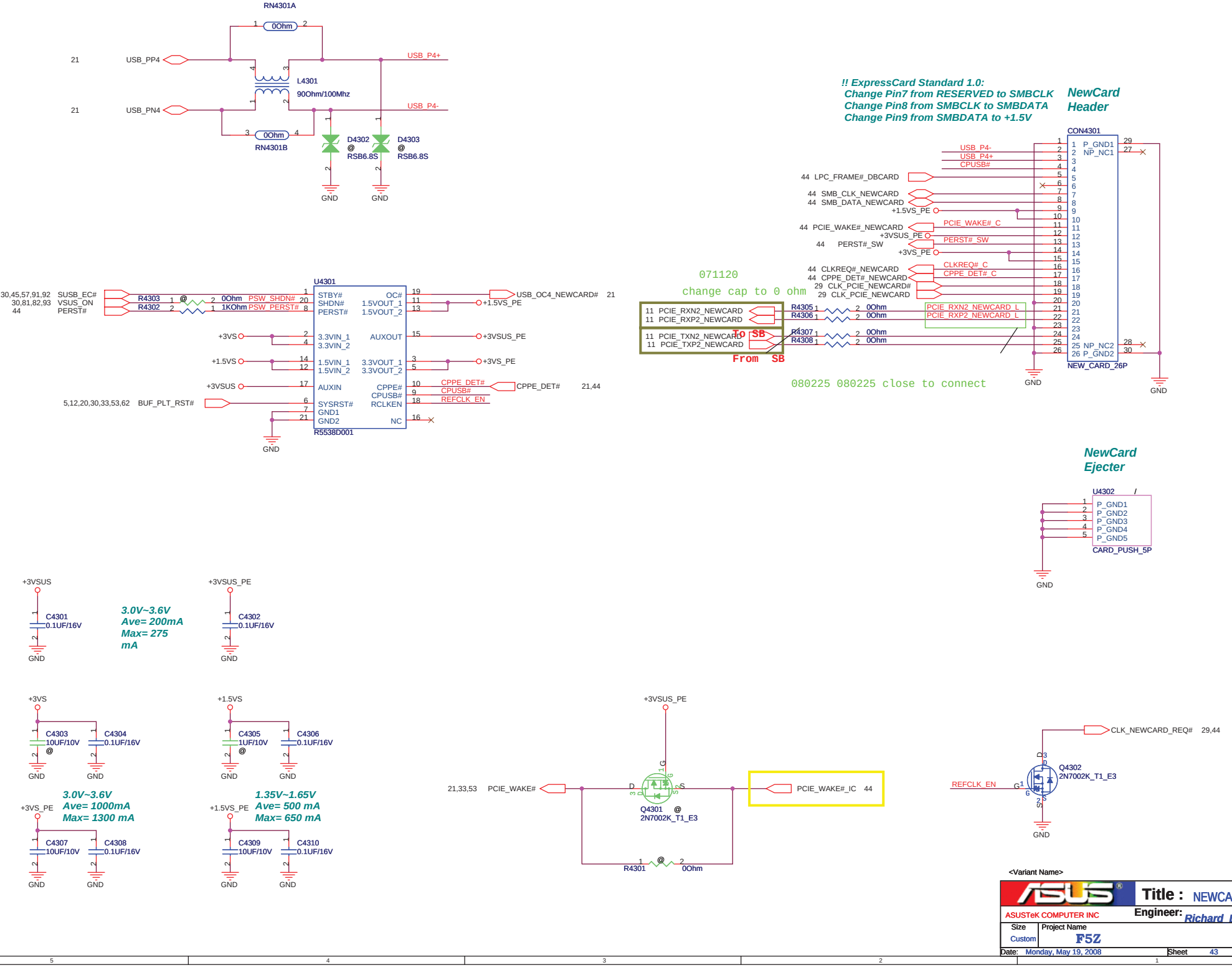
F5Z

071212
change 0 ohm P/N



<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC-IN Jack	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 38 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

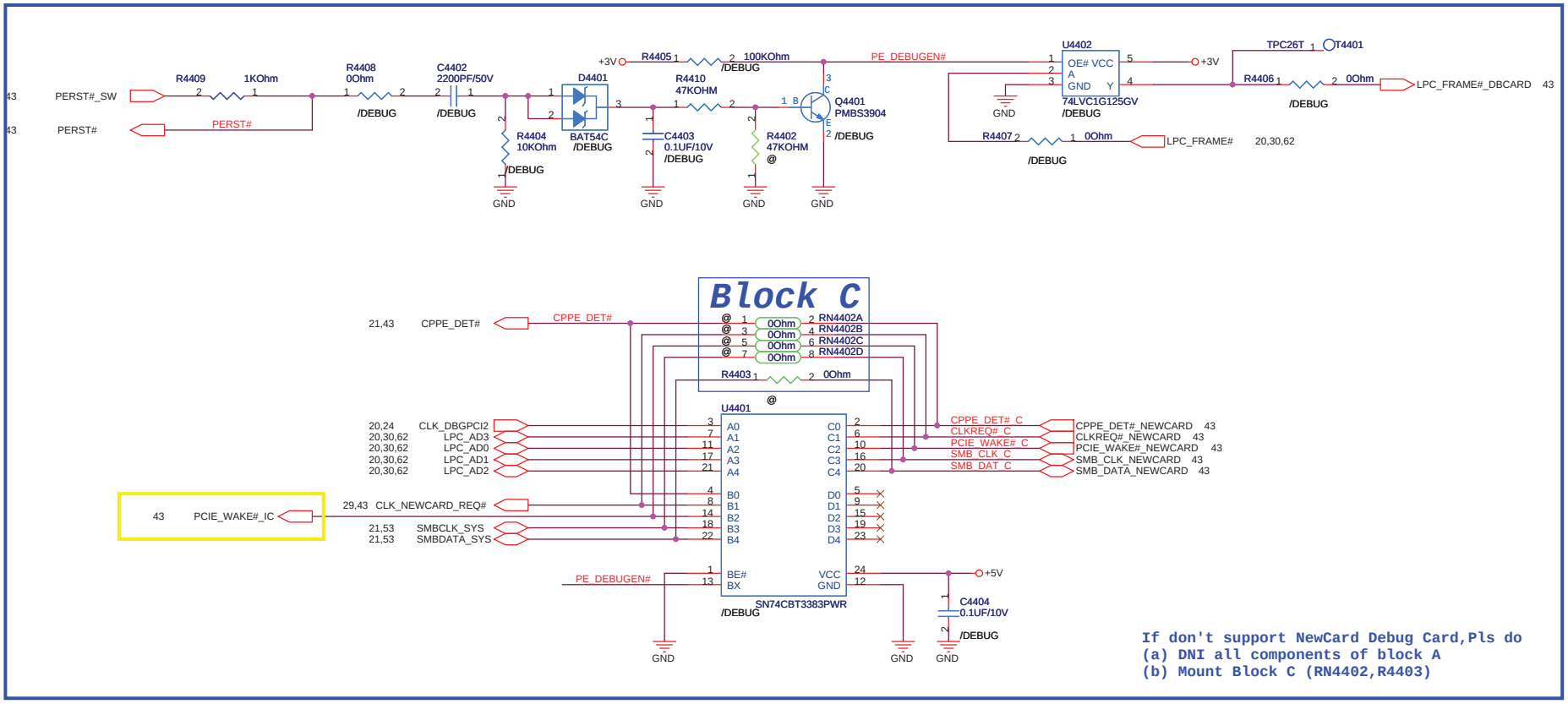
Title : NEWCARD

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	1.0

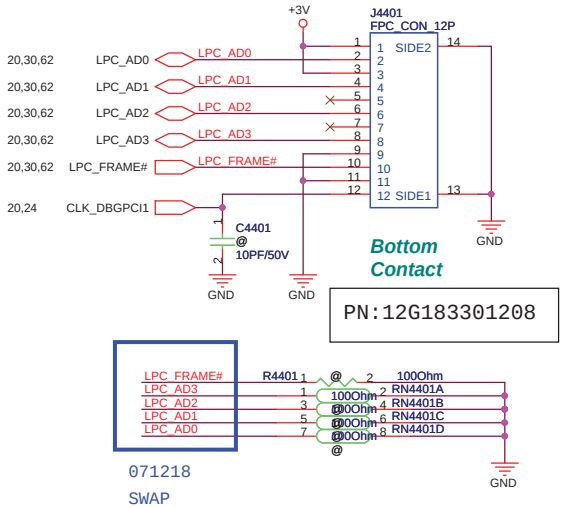
Date: Monday, May 19, 2008 Sheet 43 of 94

Block A



For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

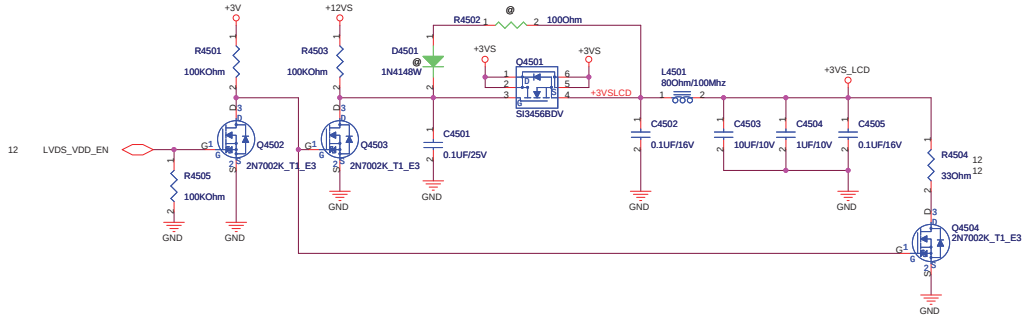


<Variant Name>

ASUSTeK COMPUTER INC	Title : DEBUG	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 44 of 94	

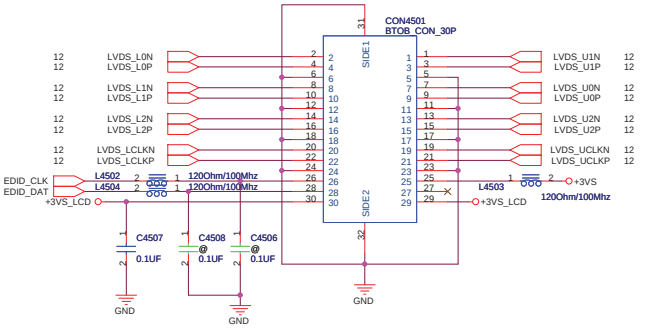
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

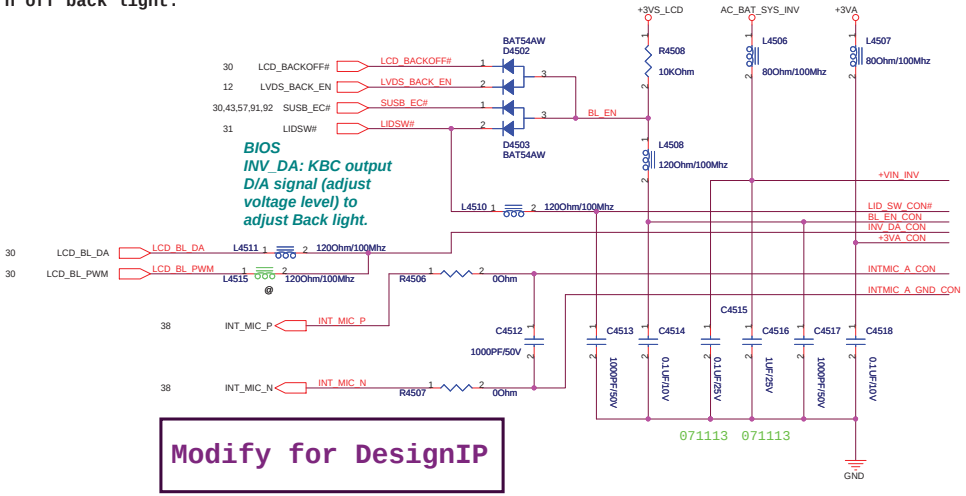
LCD LVDS Interface



INVERTER Interface

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

connect to JP8805
071203



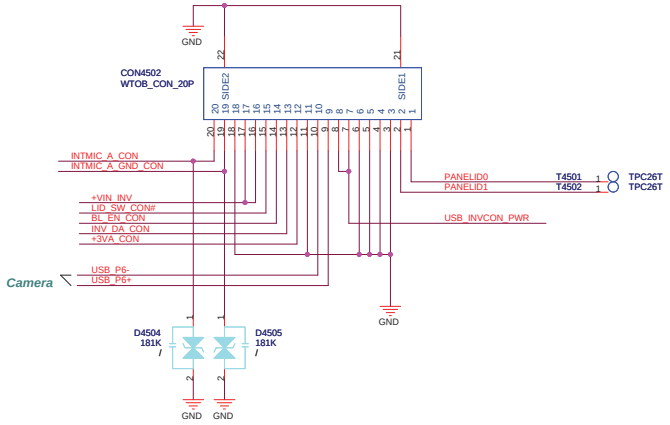
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

071113 071113

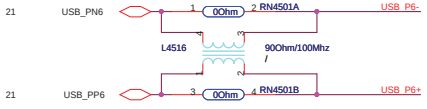
Modify for DesignIP

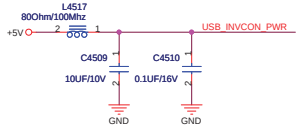
INVERTER
Interface/Speaker CONN.

Delete LID_SW SCH



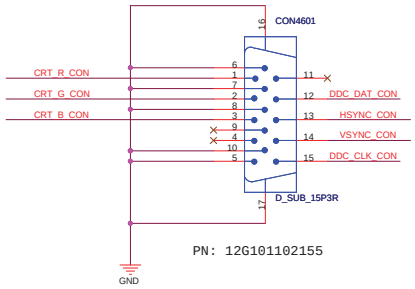
EMI REQUEST





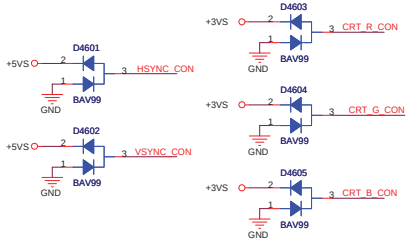
<Variant Name>

ASUSTeK COMPUTER INC.	Title : LVDS & INVERTER	
	Engineer: Richard_Lu	
Size: C	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 45 of 94	



PN: 12G101102155

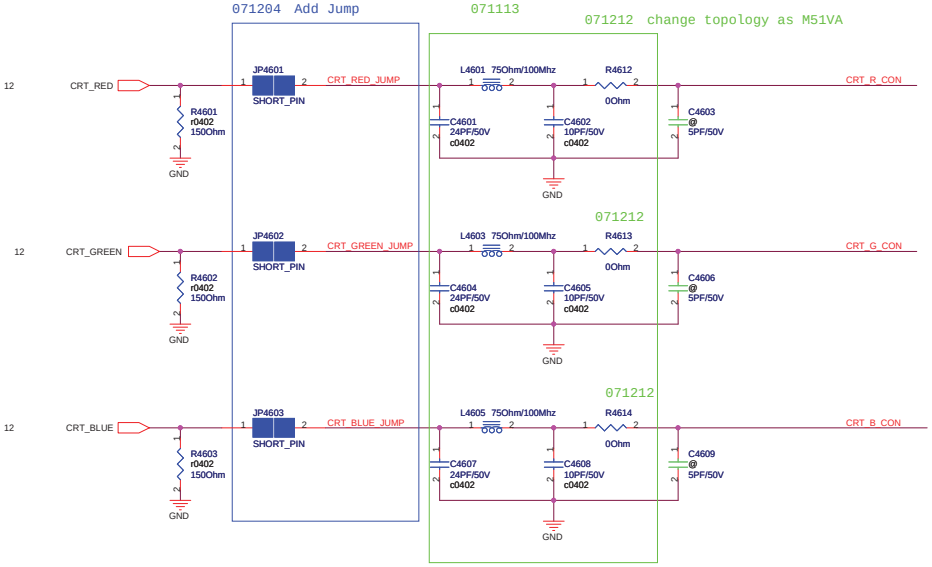
PLACE ESD Diodes near VGA port

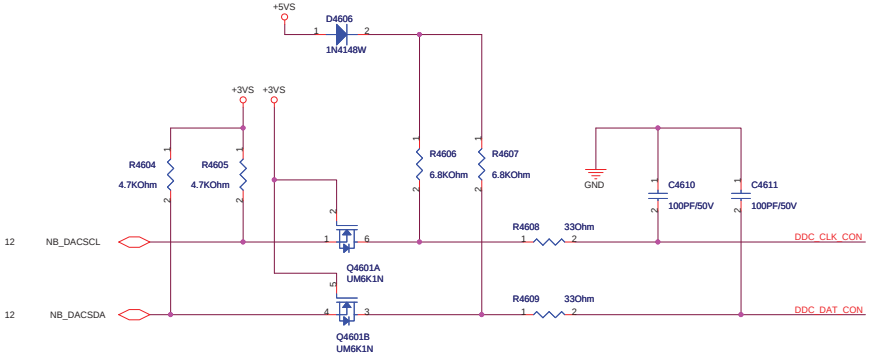


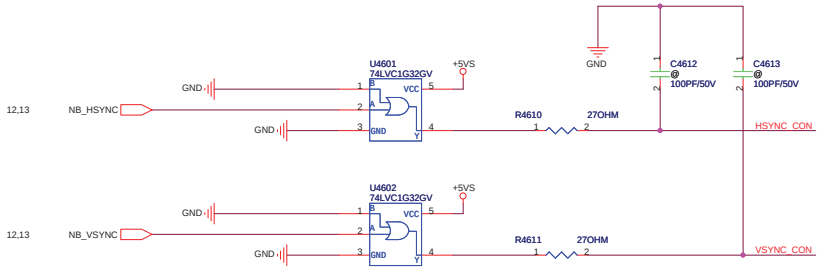
071204 Add Jump

071113

071212 change topology as M51VA



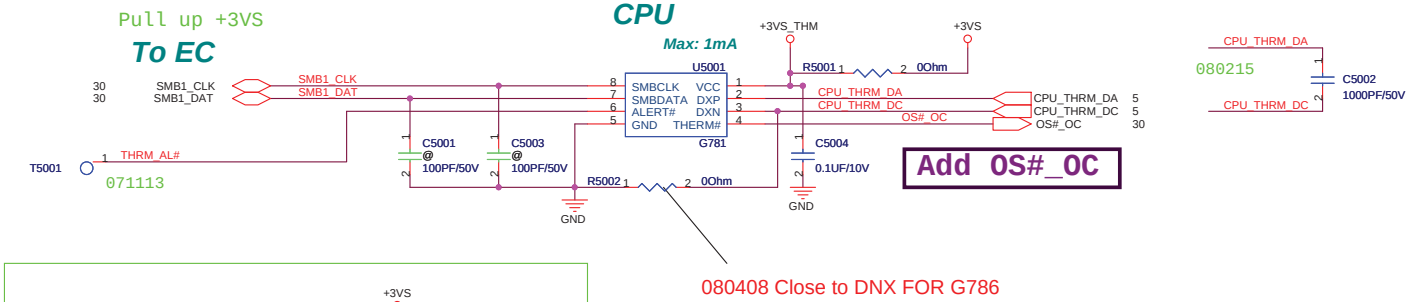




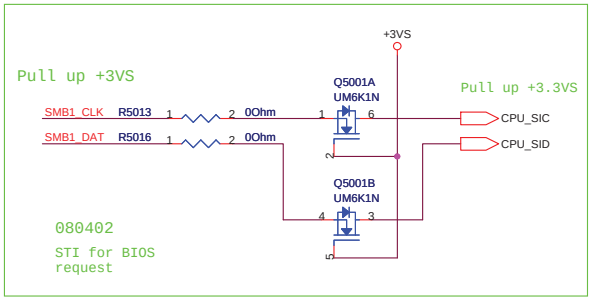
<Variant Name>

ASUSTeK COMPUTER INC	Title : CRT	
	Engineer: Richard_Lu	
Size: C	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 46 of 94	

Thermal Sensor



080408 Close to DNX FOR G786

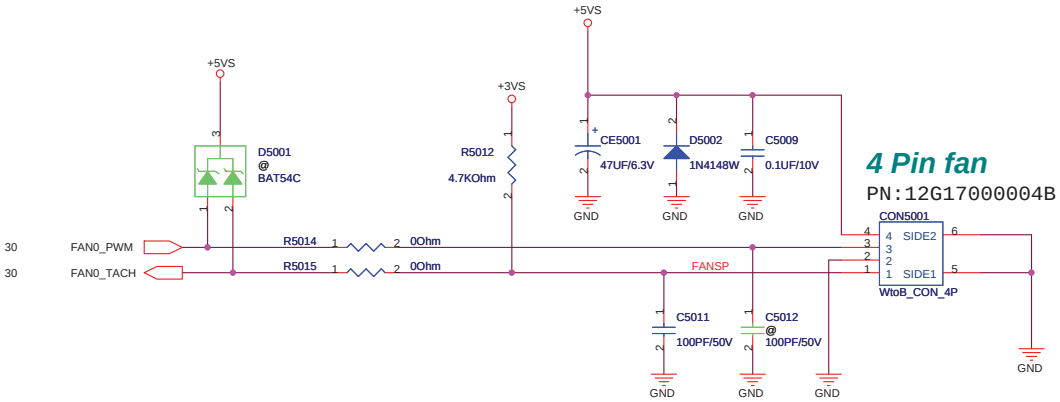


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control

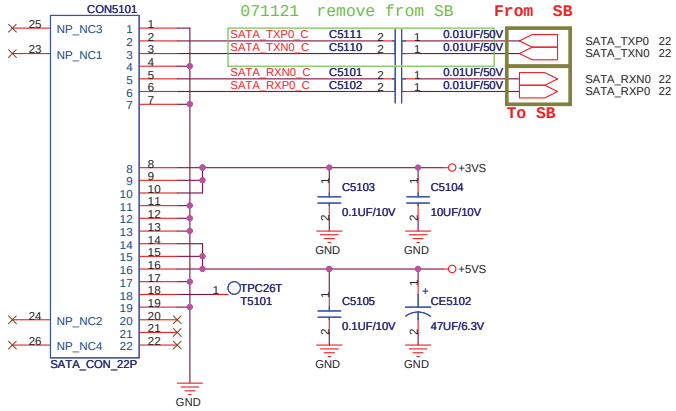


<Variant Name>

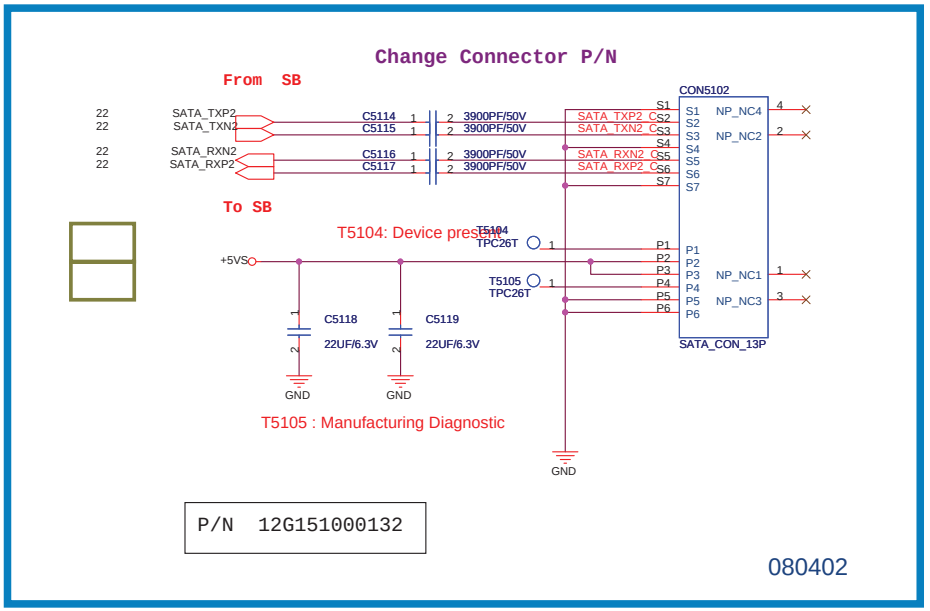
ASUSTeK COMPUTER INC	Title : THER SENSOR & FAN	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 50 of 94	

SATA HDD

071212
change 0.01UF P/N



ODD

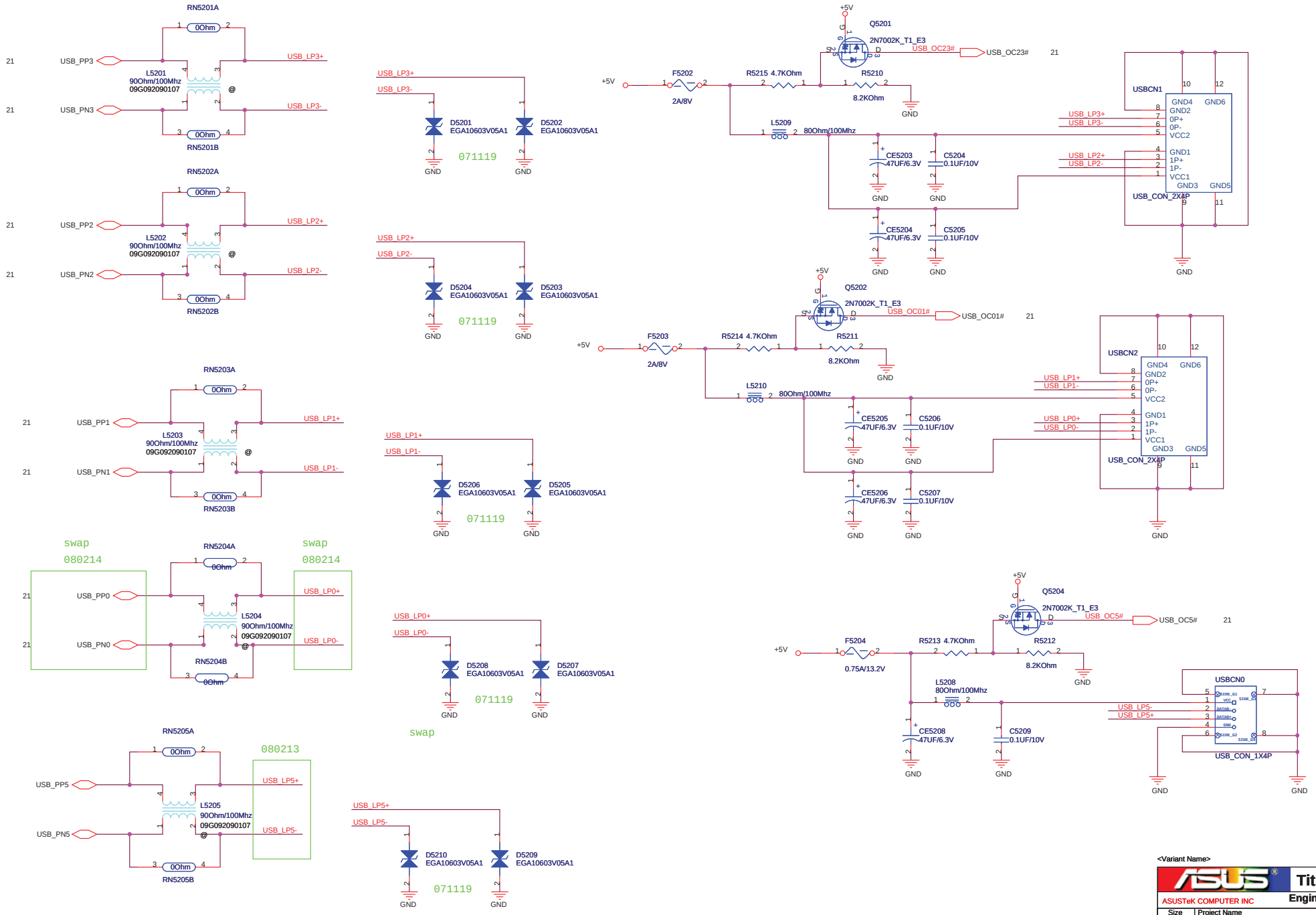


<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CD-ROM	
	Engineer: Richard Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 51 of 94	

071119 change common choke and R P/N

Change all MOS with ESD part



<Variant Name>

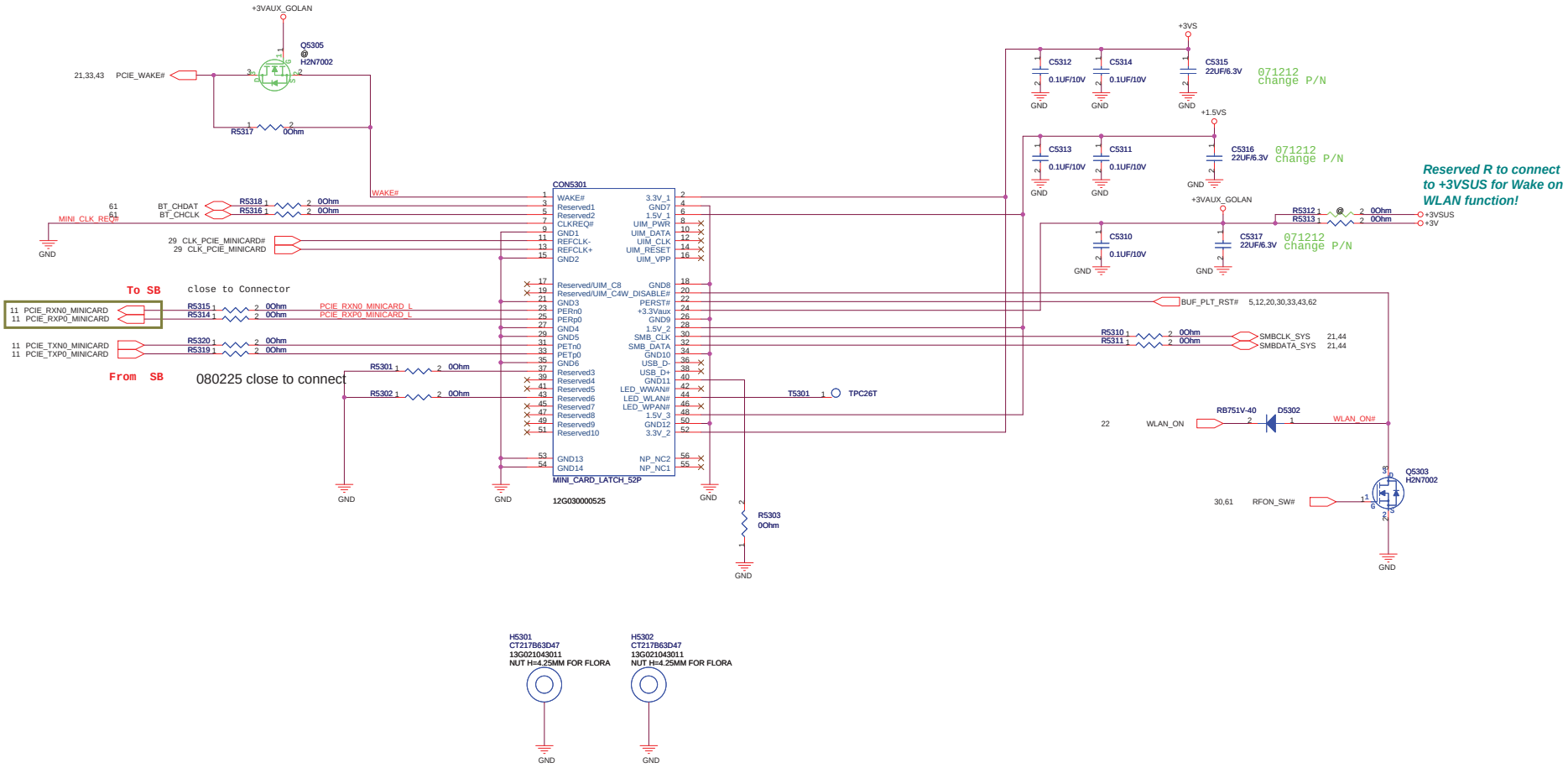
ASUSTeK COMPUTER INC

Title : USB CONN

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 52 of 94



<Variant Name>

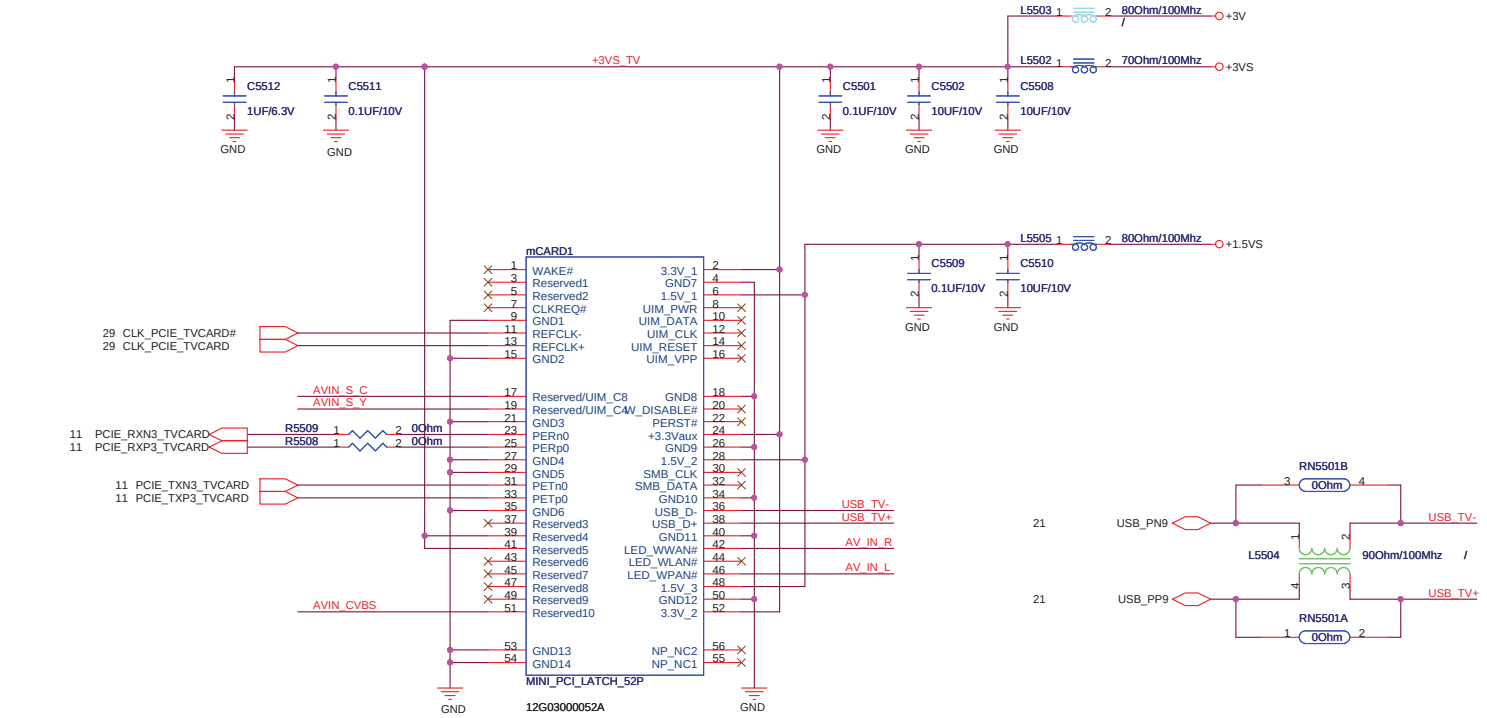
ASUSTeK COMPUTER INC.

Title : MINICARD

Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 53 of 94



H = 5.2mm

FOR TV TUNER

(UWB OPTION)

TV Conn.

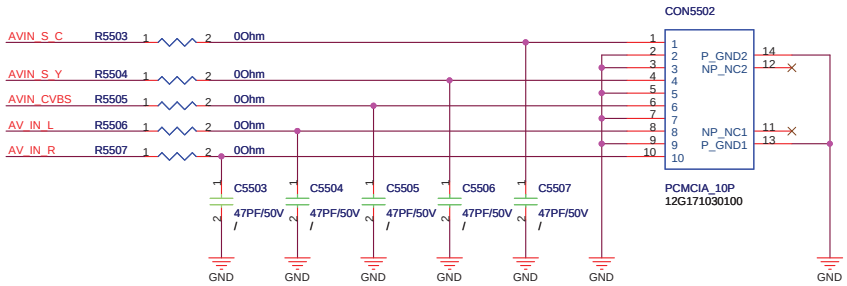
H5501
L4E-1A
13GN7510M270-1

H5502
L4E-1A
13GN7510M270-1

GND GND

H = 3.0mm

ME P/N : 14G152075000



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

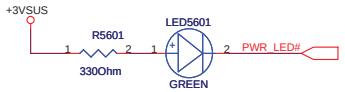
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	1.0

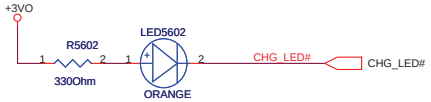
Date: Monday, May 19, 2008 Sheet 55 of 94

LED

For POWER LED

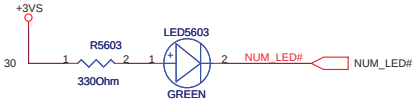


BATTERY LED



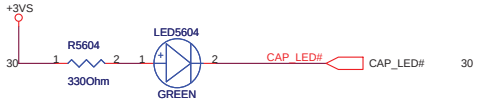
Num Lock

071122



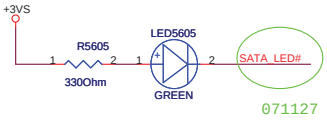
Cap Lock

071122



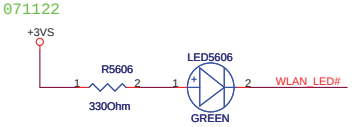
SATA/IDE LED

071122



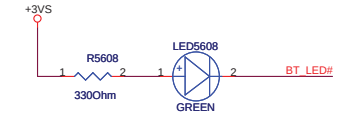
WireLess LED

071122



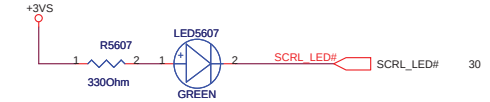
BT LED

071122



Scroll Lock

071122



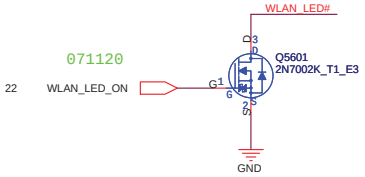
Change all LED for 5mA

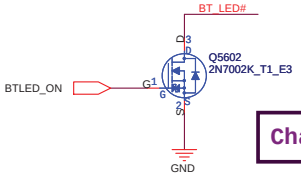
delete D5601

071127

From SB GPIO

071120





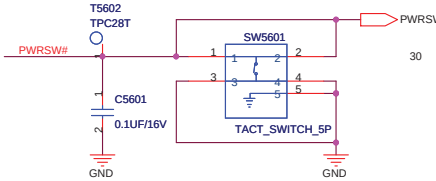
Change all MOS with ESD part

F5Z SWITCH CIRCUIT

Move SW from P32 to P56

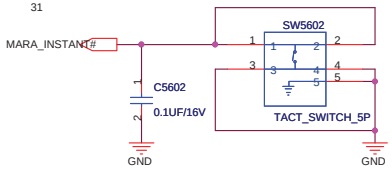
Add SHUT Down SCH

Power SW.

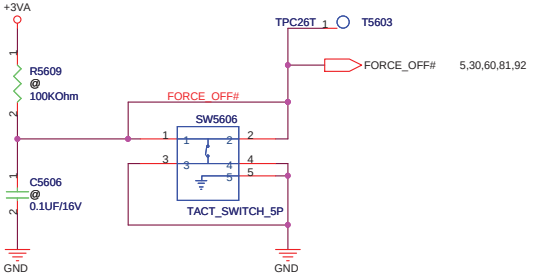


P/N: 12G091030050

Marathon SW.

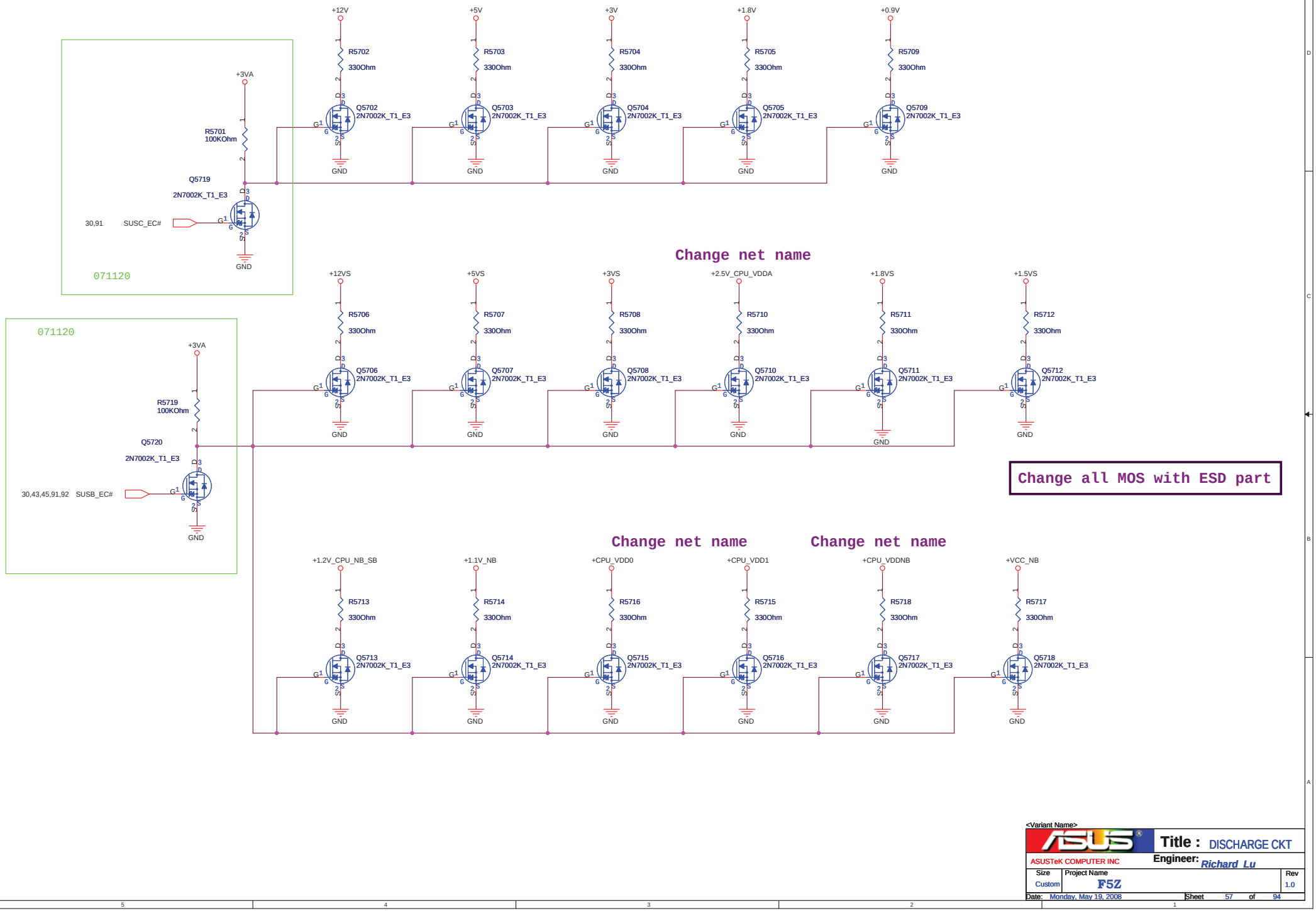


SHUT_DOWN#



<Variant Name>

ASUSTeK COMPUTER INC	Title : LED/PWR SWICH	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 56 of 94	



<Variant Name>

Title : DISCHARGE CKT

ASUSTeK COMPUTER INC

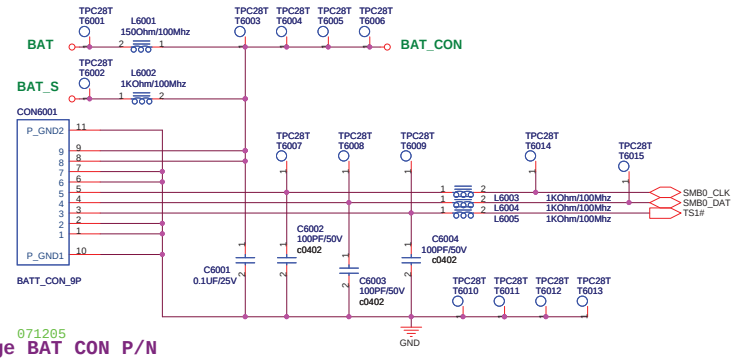
Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 57 of 94

071120 cahnge PL->L,PT->T,PC->C

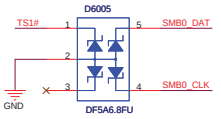
BATTERY



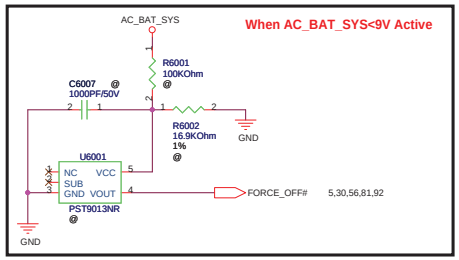
071205
Change BAT CON P/N

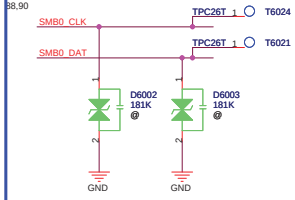
Reference To M51

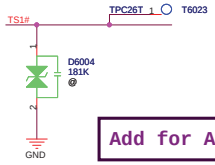
071203 change footprint



Without Battery & Pull out Adapter

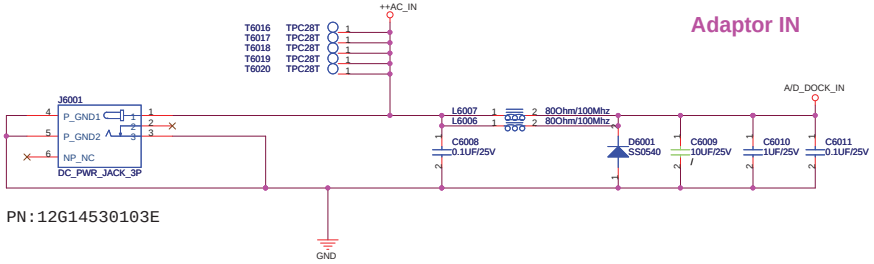






Add for AC Adapter protect

DC JACK-IN



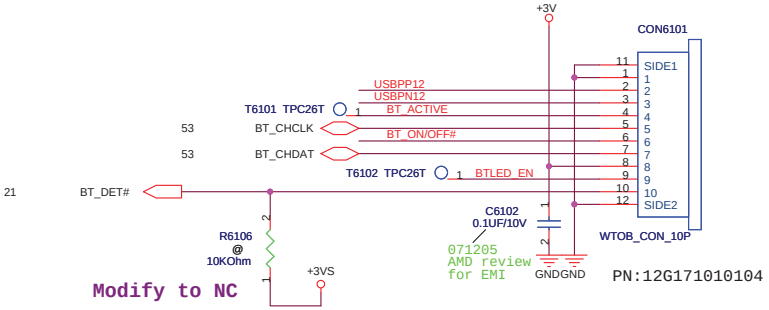
PN:12G14530103E

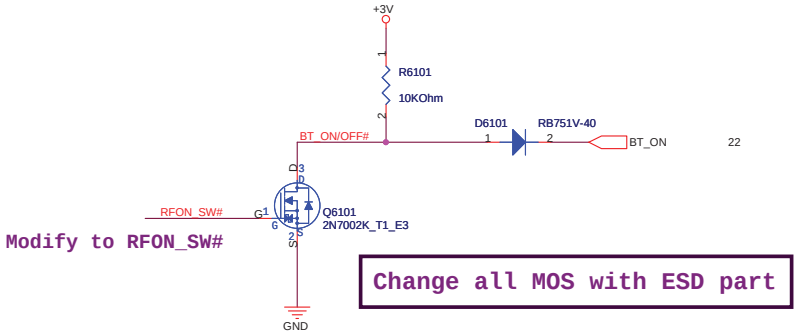
071218
Delete GND_DC , Bead
,and Test Point

<Variant Name>

ASUSTeK COMPUTER INC.	Title : DC_Jack & BAT Con	
	Engineer: Richard_Lu	
Size: C	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 60 of 94	

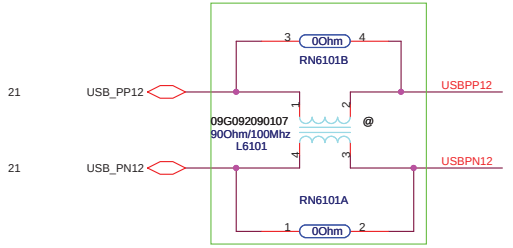
For Bluetooth





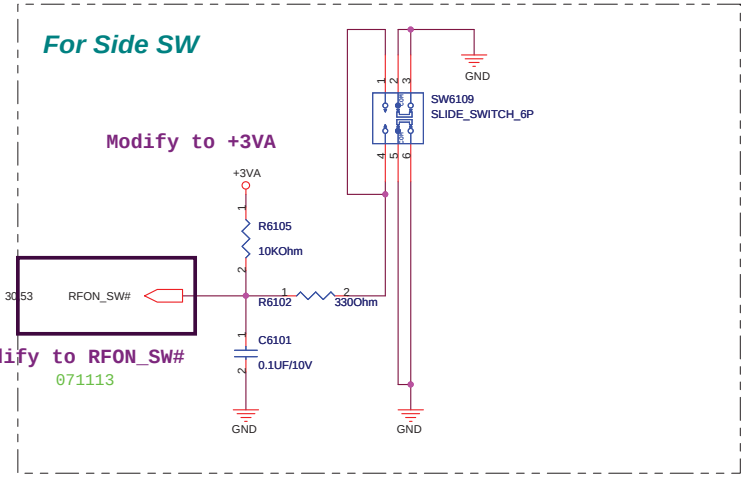
Change all MOS with ESD part

RN swap
071214



071120 change common choke and R P/N

For Side SW

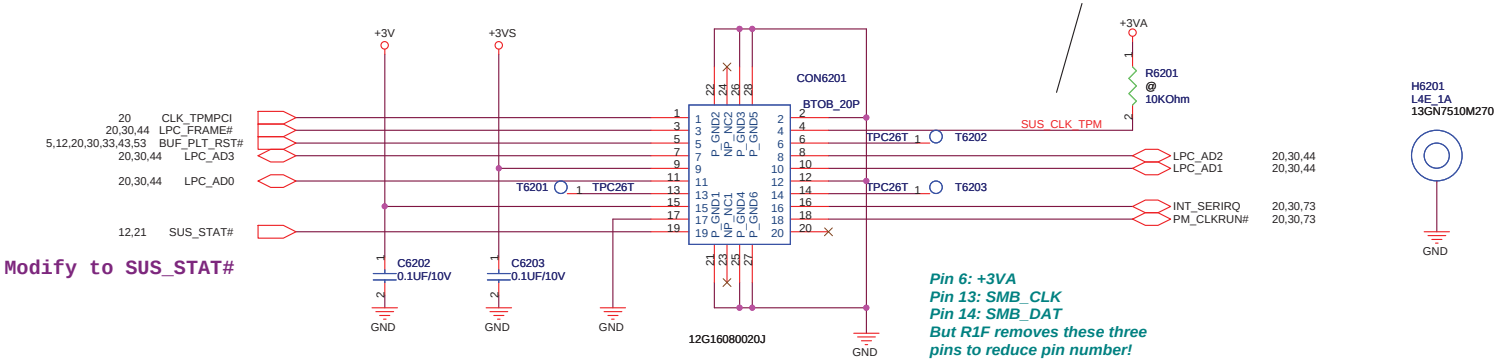


<Variant Name>

ASUSTeK COMPUTER INC	Title : BT & Slide SW	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 61 of 94	

For TPM Module

071120
TPM module has internal crystal



H6201
L4E_1A
13GN7510M270

GND

Modify to SUS_STAT#

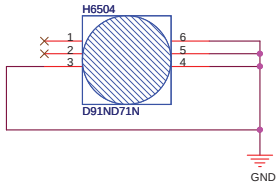
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

SN:12G16080020J

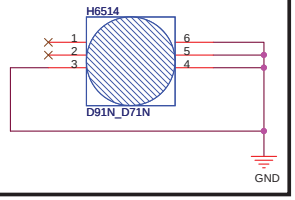
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 62 of 94	

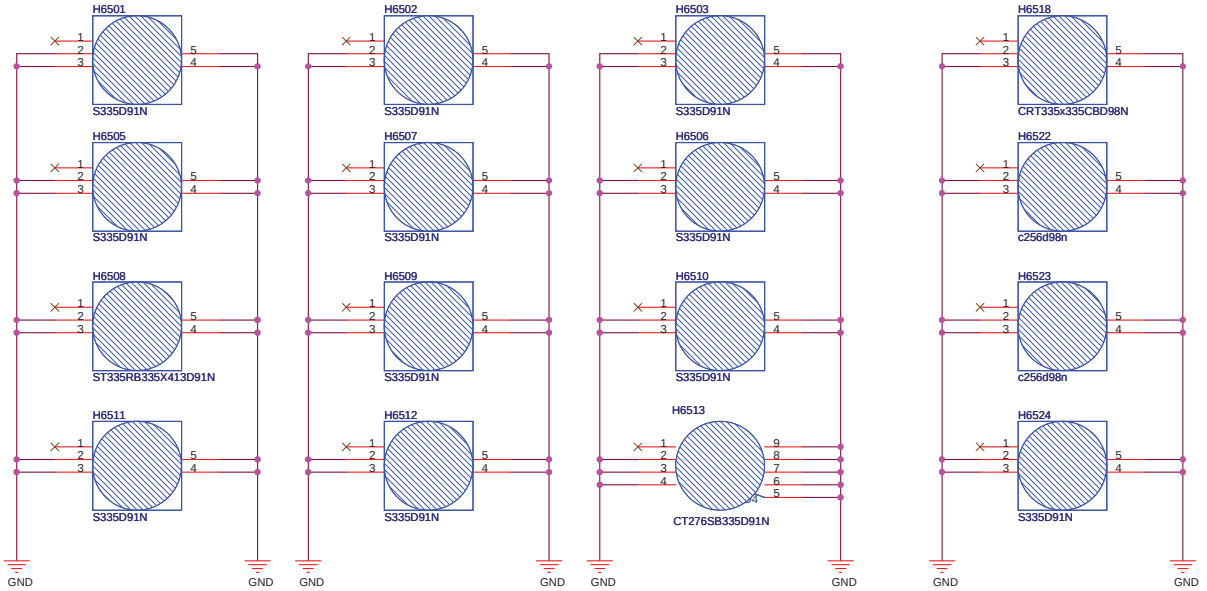
FOR LEFT UNDER



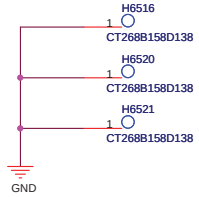
FOR RIGHT UP



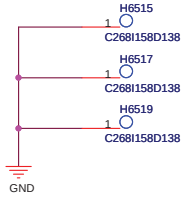
FOR SCREW HOLE

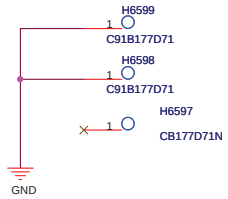


FOR CPU



FOR VGA





<Variant Name>

ASUSTeK COMPUTER INC

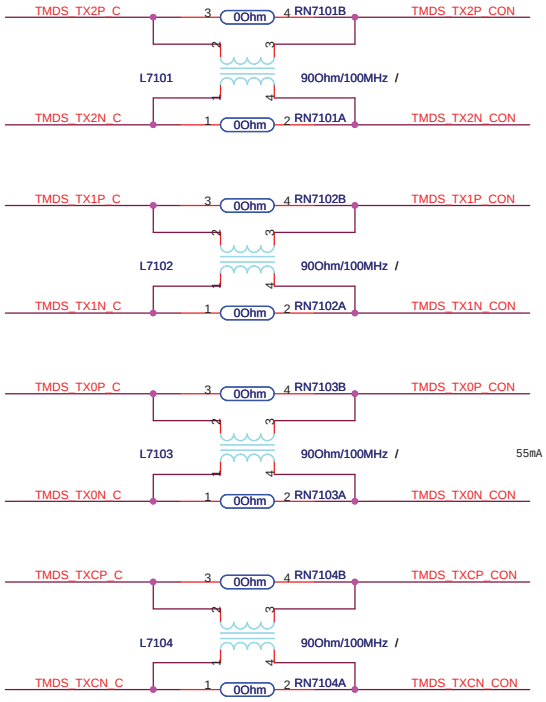
Title : Screw Hole

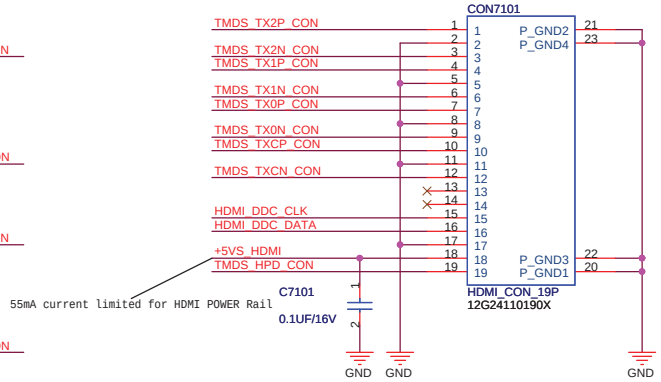
Engineer: <OrgAddr1>

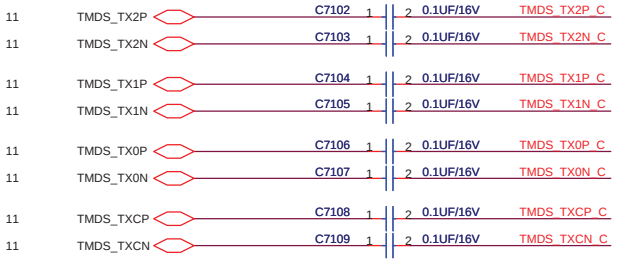
Size	Project Name	Rev
Custom	F5Z	1.0

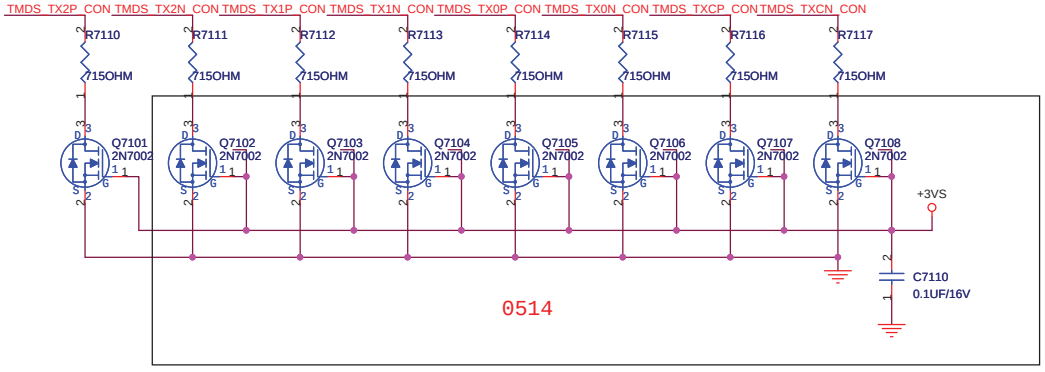
Date: Monday, May 19, 2008 Sheet 65 of 94

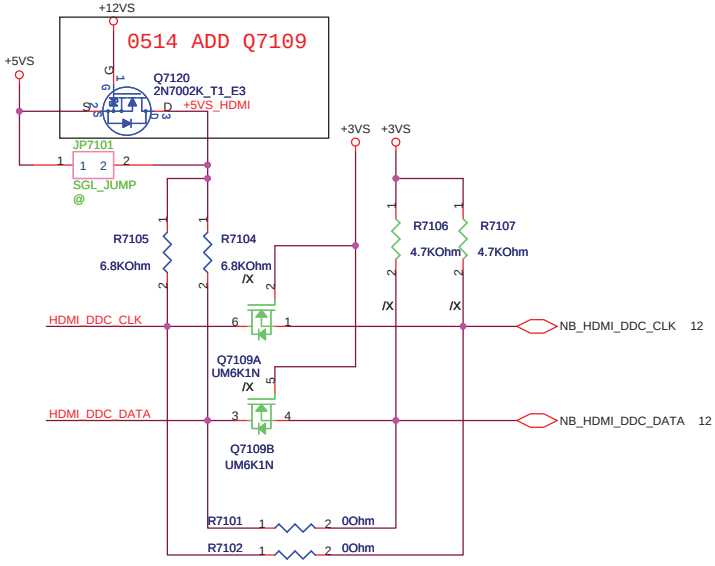
HDMI

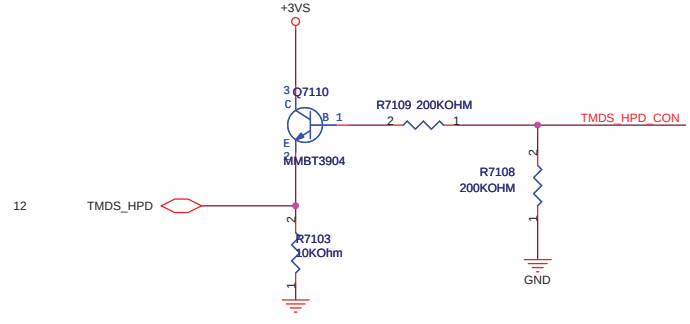












<variant_name>

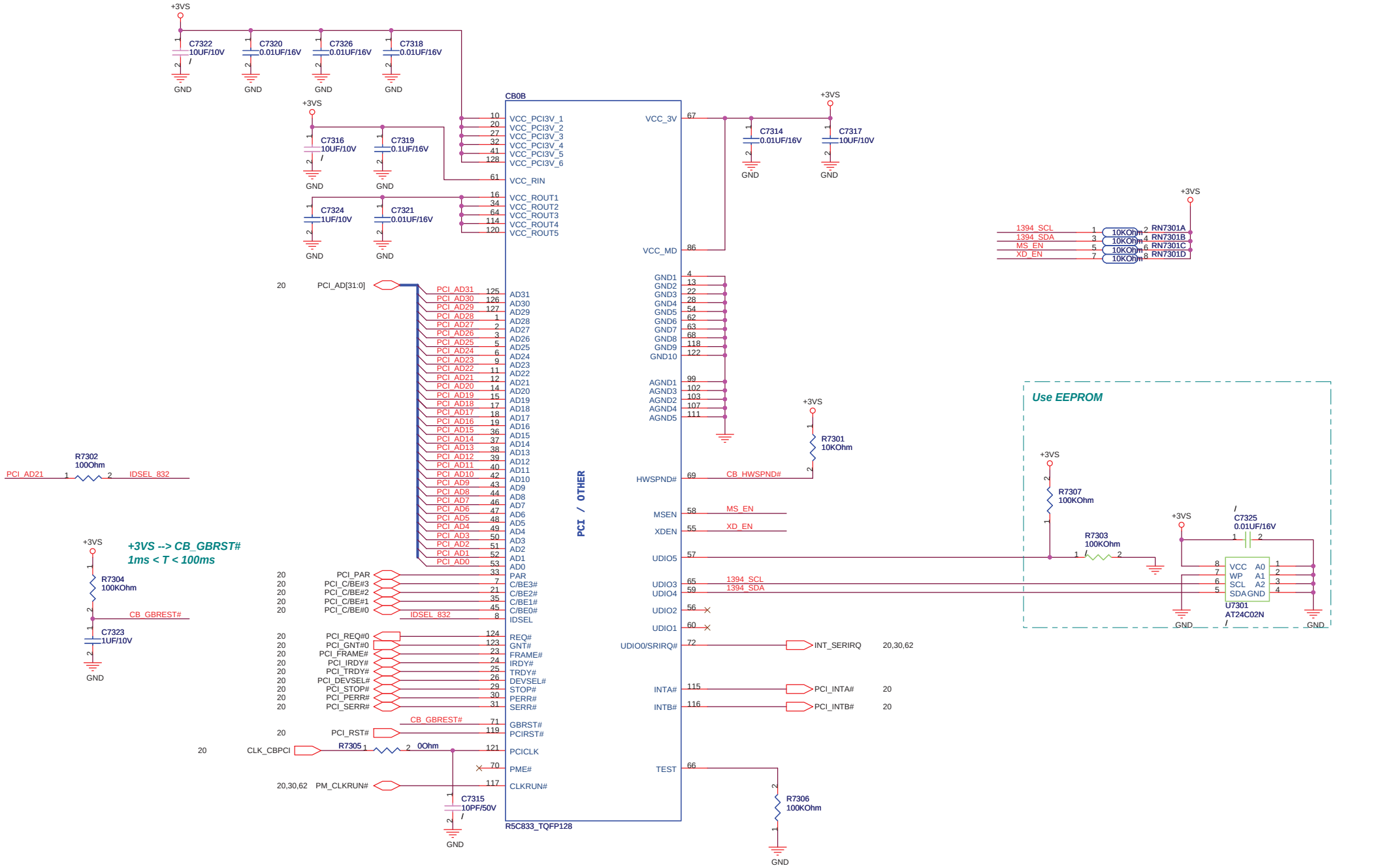
ASUSTeK COMPUTER INC

Title : HDMI CON

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 71 of 94



<Variant Name>

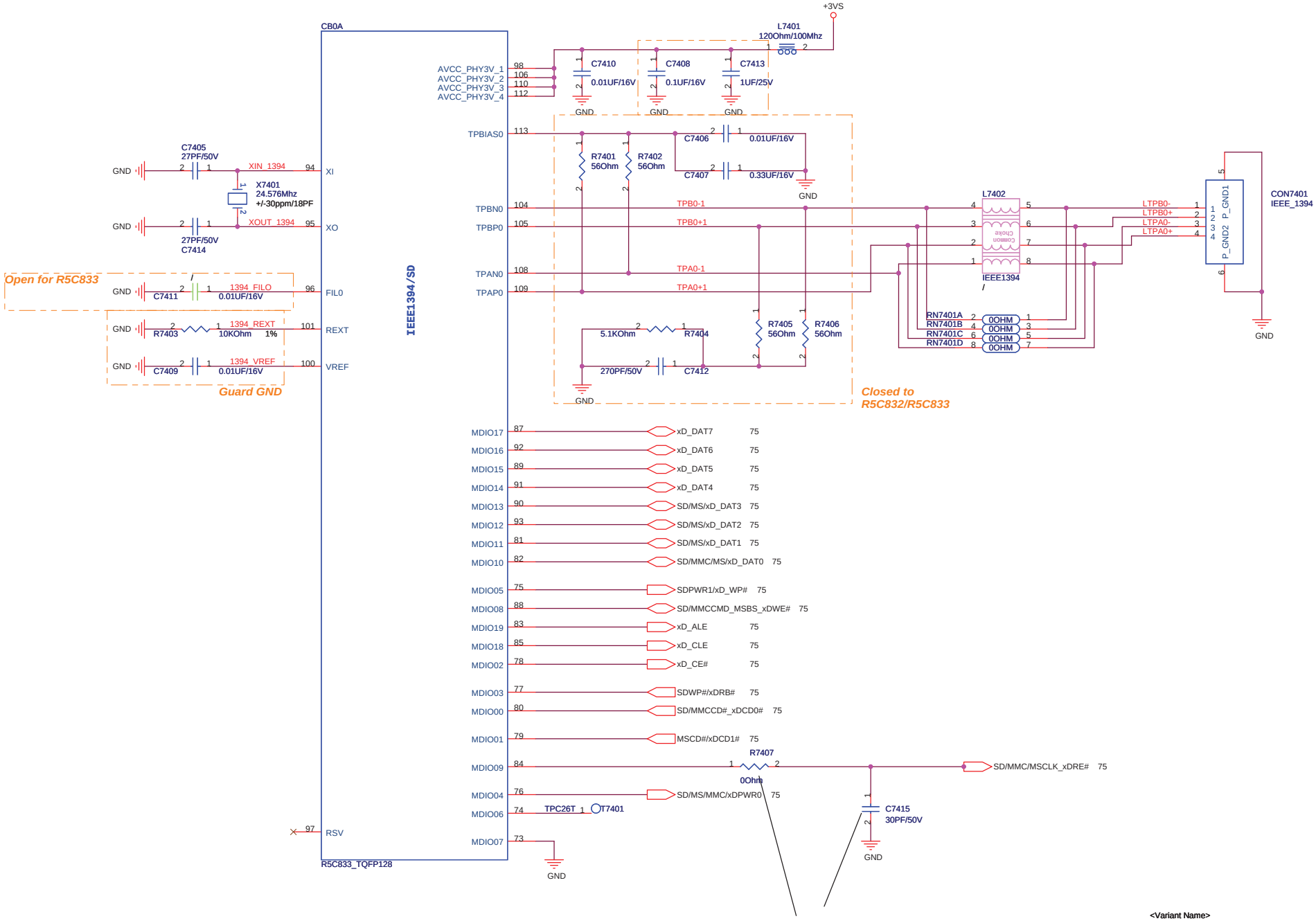
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 73 of 94



080408 Add r7407 and c7415 for EMI

<Variant Name>

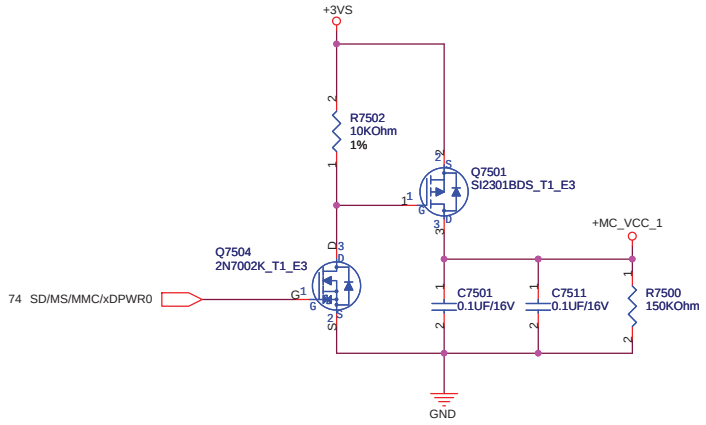
Title : *

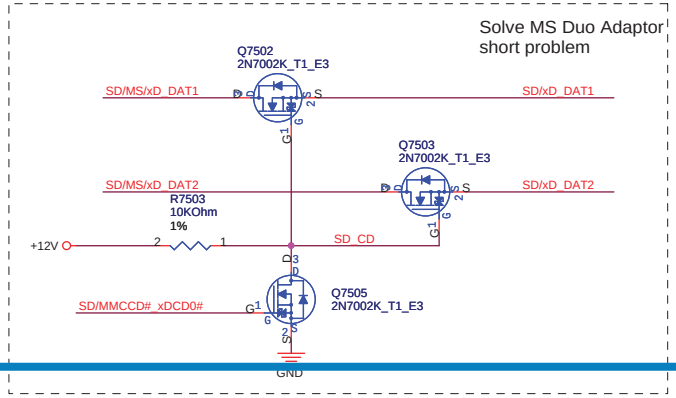
ASUSTeK COMPUTER INC

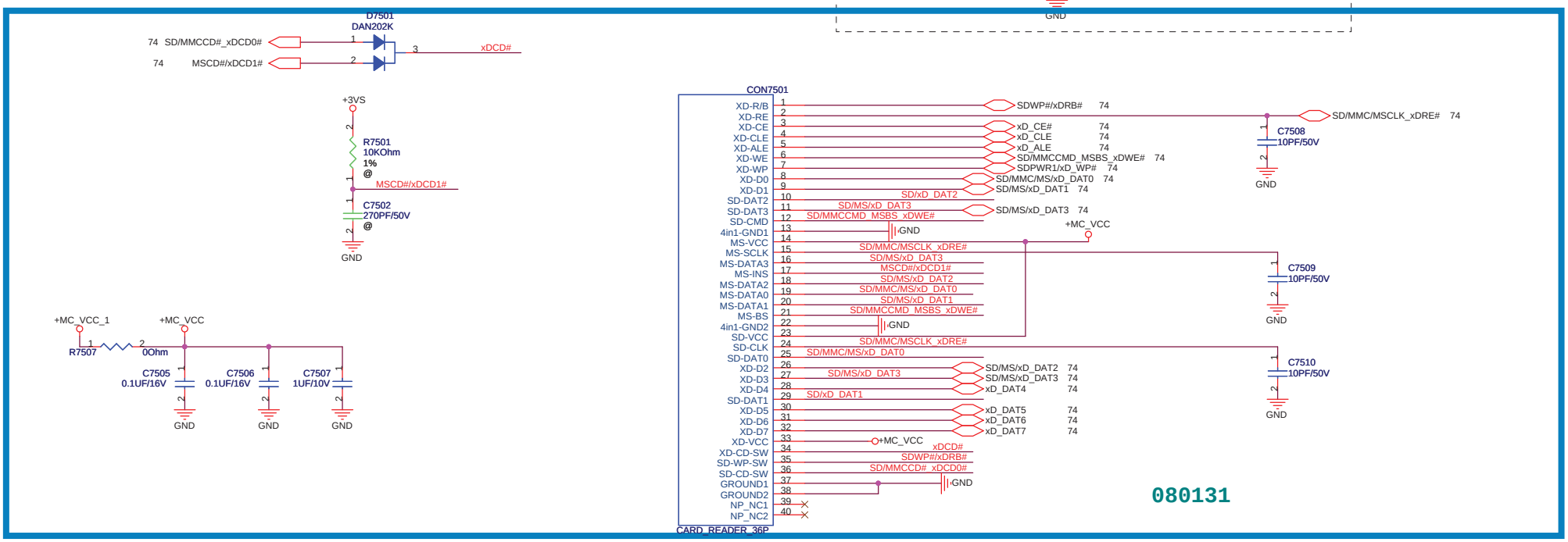
Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 74 of 94







<Variant Name>

ASUSTeK COMPUTER INC

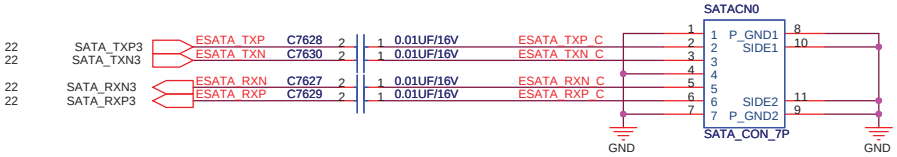
Title : *

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 75 of 94

eSATA Connector



<Variant Name>

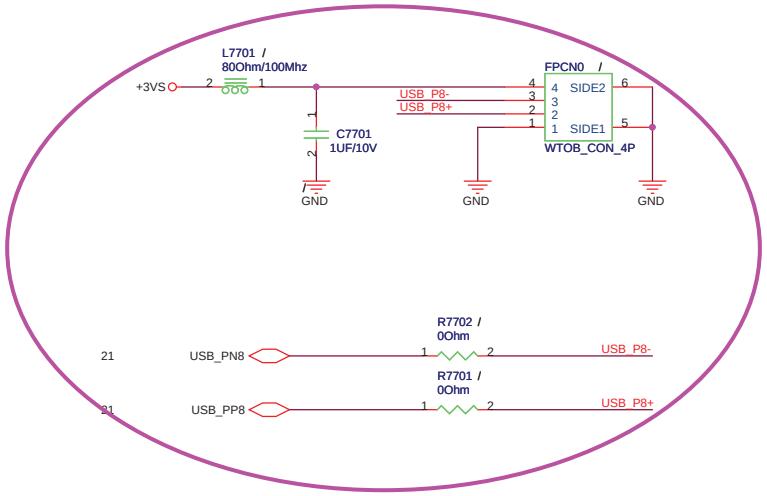
ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 76 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 77 of 94

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V Pre_metal	X	X

VFIXEN VID Codes

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8

Design Current : 4A
Maximum current : 4.4A
OCP point Typ : 4.6A
+CPU_VDDNB +CPU_VDDNB_O

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 21.6A
+CPU_VDD0

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 21.6A
+CPU_VDD1

U8000 ISL6265HRTZ-T

Parallel

Parallel

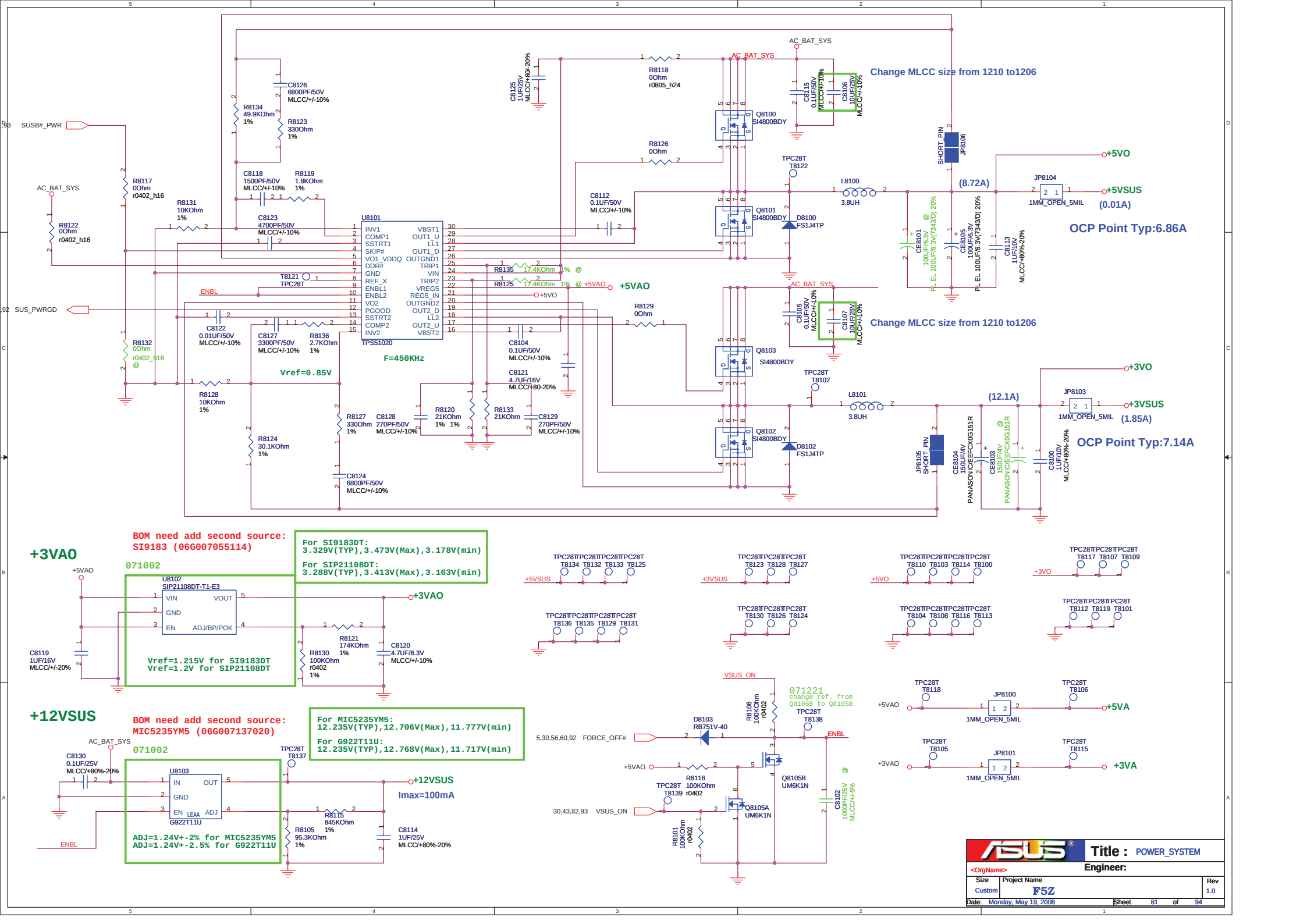
close to CPU socket

Change Footprint For Net_IN

+3VSUS

SVC	SVD	Output
R8076	R8077	1.4
R8076	R8074	1.2
R8075	R8077	1.0
R8075	R8074	0.8

Title :	POWER_VCORE
<OrgName>	Engineer:
Size: Custom	Project Name: F5Z
Rev:	1.0
Date: Monday, May 19, 2008	Sheet 80 of 94


SUSB#_PWR
SUS_PWRGD
AC_BAT_SYS
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
Change MLCC size from 1210 to1206
Change MLCC size from 1210 to1206
+5VAO
+5VO
+5VSUS
(0.01A)
(8.72A)
OCP Point Typ:6.86A
+3VO
+3VSUS
(1.85A)
(12.1A)
OCP Point Typ:7.14A
+3VA0
BOM need add second source:
SI9183 (06G007055114)
071002
For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)
For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)
U8102
SIP21108DT-T1-E3
Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)
071002
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
U8103
G922T11U
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U
+12VSUS
Imax=100mA
VSUS_ON
FORCE_OFF#
071221
change ref. from
Q8106B to Q8105B
Title : POWER_SYSTEM
Engineer:
<OrgName>
Size
Custom
Project Name
F5Z
Rev
1.0
Date: Monday, May 19, 2008
Sheet 81 of 94

* Rocset = Ioc * DRC / 10uA

+1.2VO: ROCSET = R8213 ; R8215 = R8213=10KOhm; OCP>7.5A

+1.8VO: ROCSET = R8212 ; R8212 =R8211 =4.7KOhm ; OCP>14A

* VREF = 0.6V+-1%

+1.2VO = VREF * (R8206 + R8214) / R8214 =1.2V+-2%

+1.8VO = VREF * (R8207 + R8210) / R8207=1.806V+-2.38% (1.764~1.849)

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

+1.2VO: Rfset =R8204; Fsw=366KHz

+1.8VO: Rfset =R8202; Fsw=300KHz

* Pin 29 connect to GND with 5 Via independent, isolate Pin17 and Pin18

08/02/26change

08/04/14change

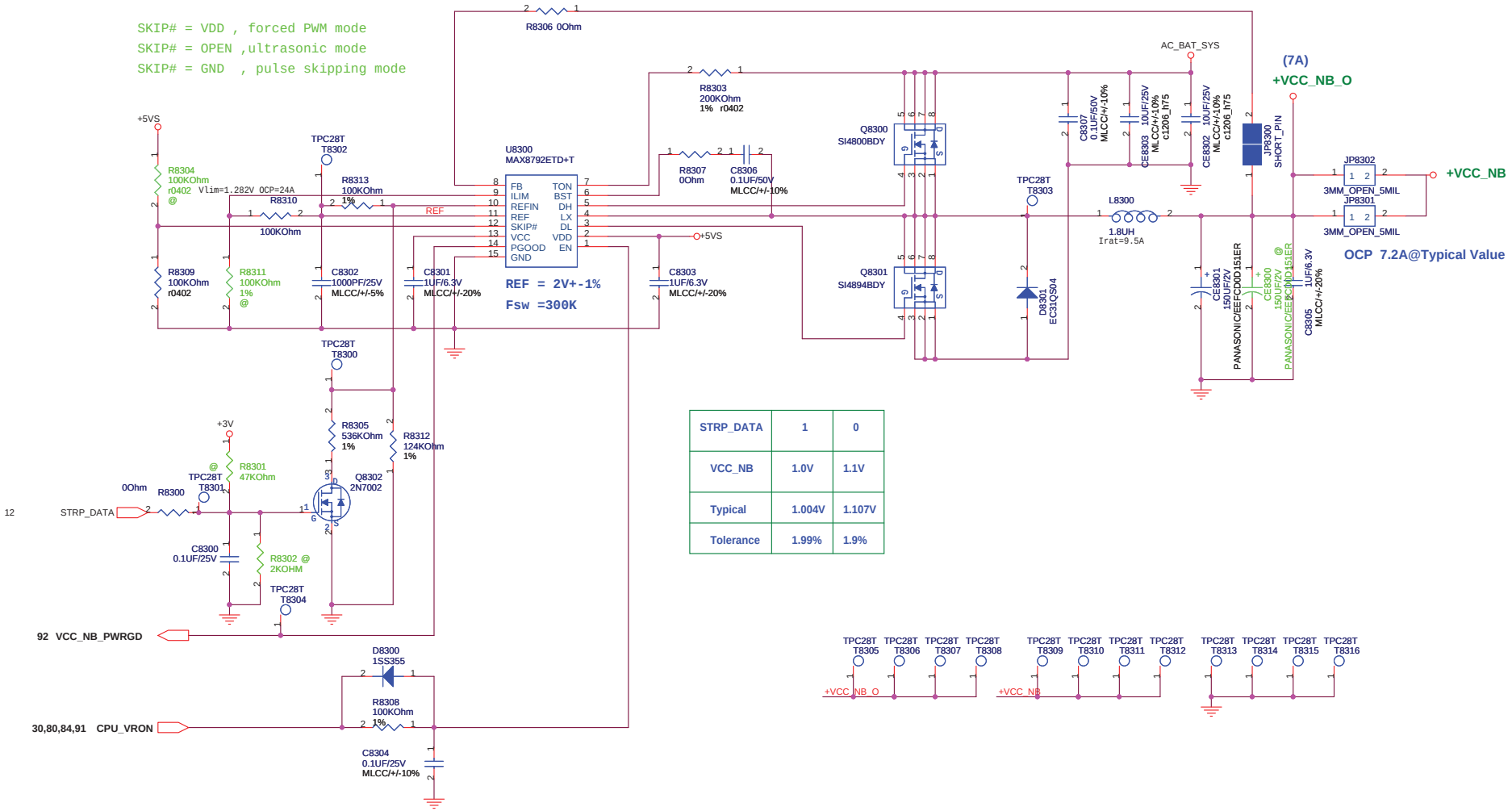
FSW2:366Khz

FSW1:300Khz

for jitter

08/02/26change

Title	POWER_I/O_1.2VO & 1.8VO&0.9VO
Engineer:	<OrgName>
Size	Custom
Project Name	F5Z
Rev	1.0
Date:	Monday, May 19, 2008
Sheet	82 of 94



STRP_DATA	1	0
VCC_NB	1.0V	1.1V
Typical	1.004V	1.107V
Tolerance	1.99%	1.9%

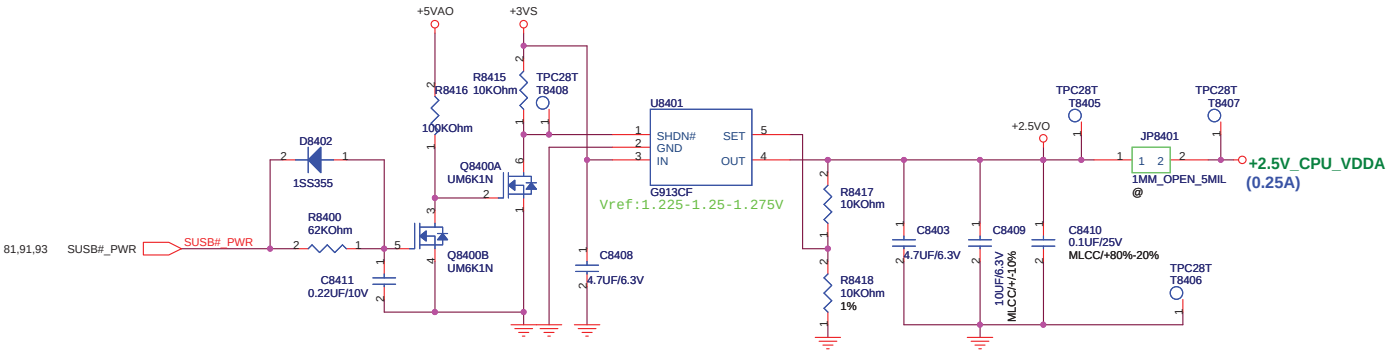
Title :POWER_I/O_VCC_NB

<OrgName> Engineer:

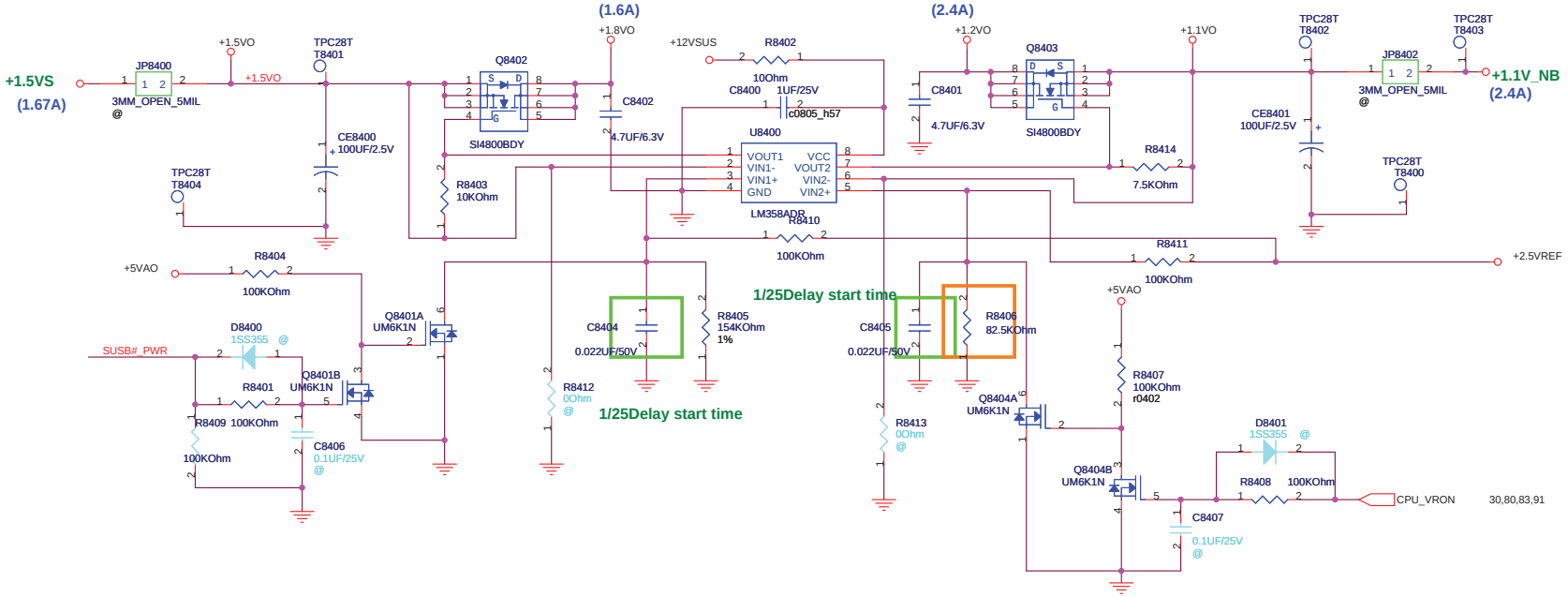
Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 83 of 94

+2.5V_CPU_VDDA

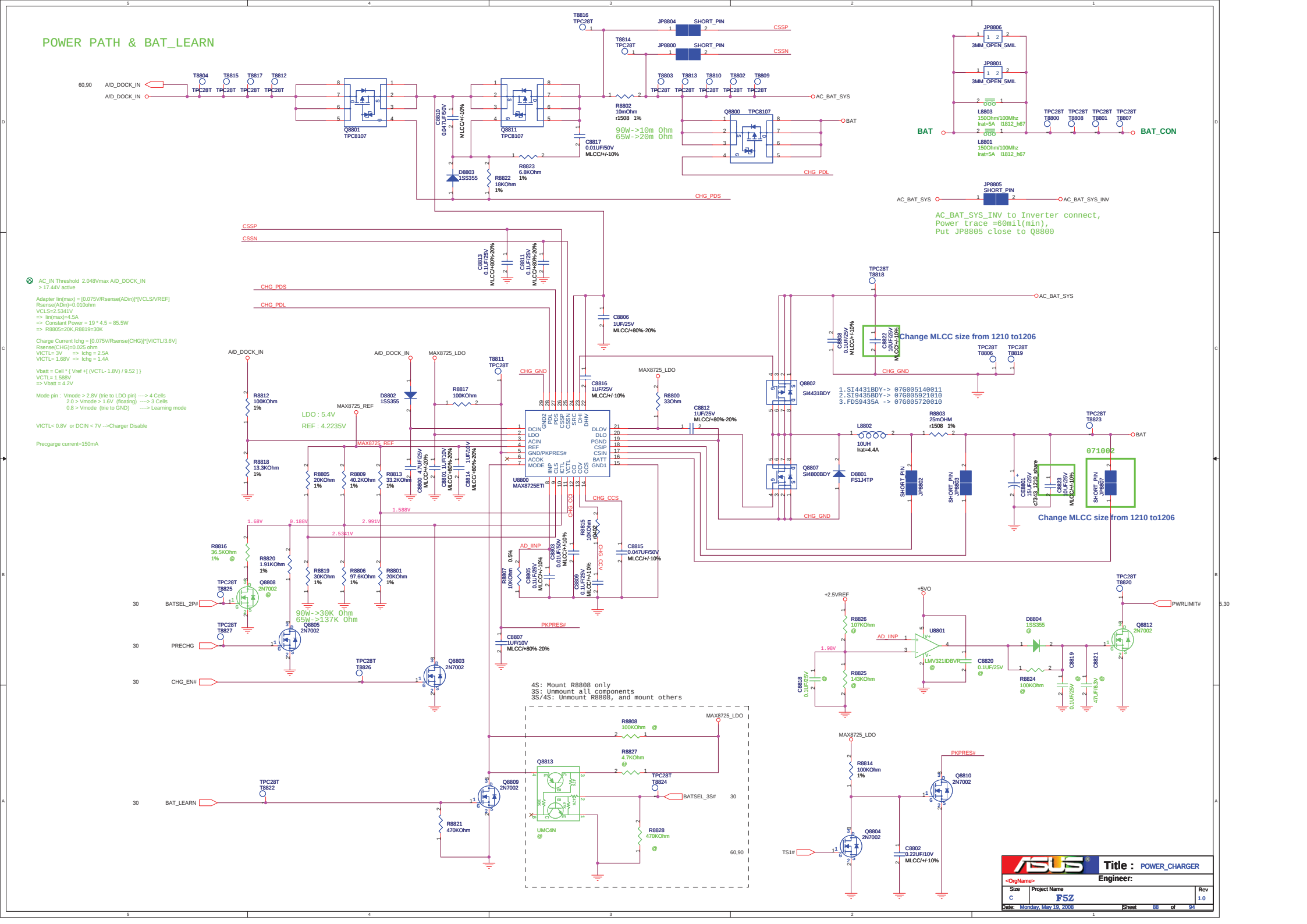


+1.5VS & +1.1V_NB

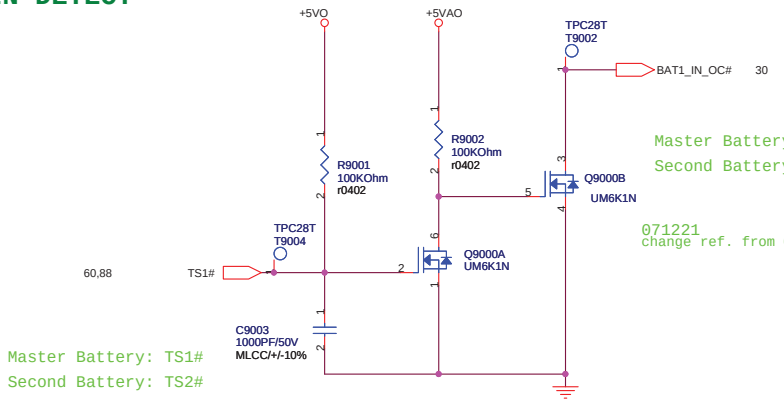


ASUS	Title : POWER_+2.5VS&+1.5VS & +1.1VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 84 of 94	

POWER PATH & BAT_LEARN



BATTERY IN DETECT

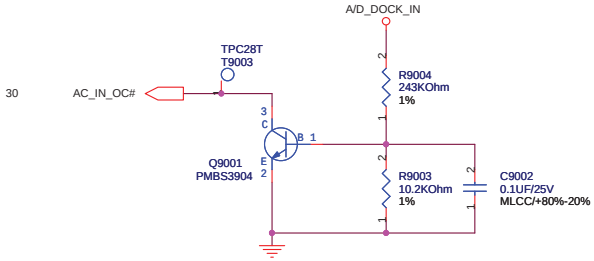


Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

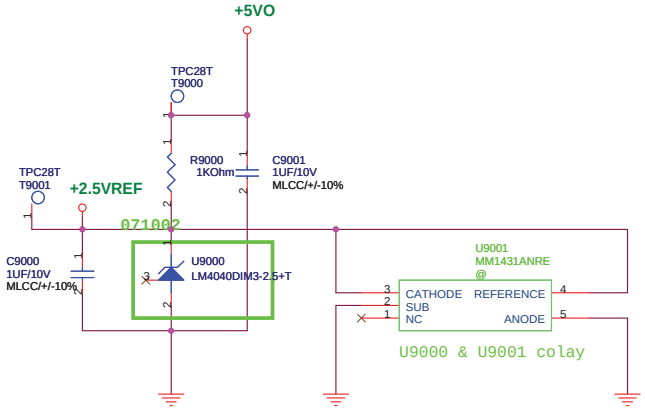
071221
change ref. from Q9002B to Q9000B

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF

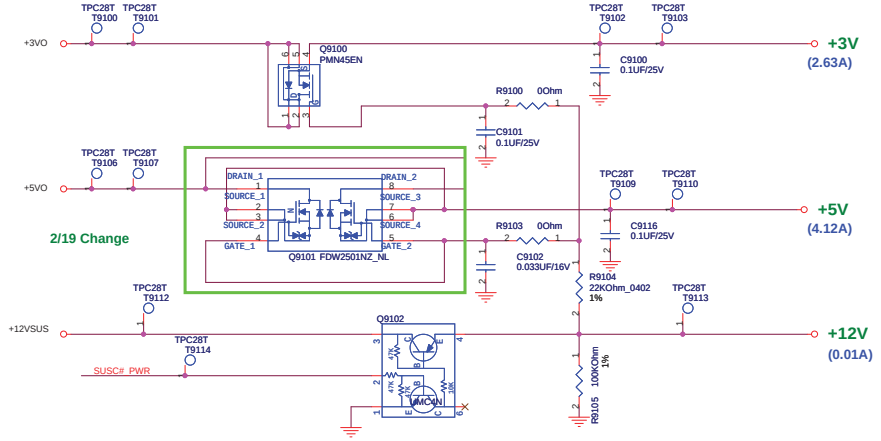


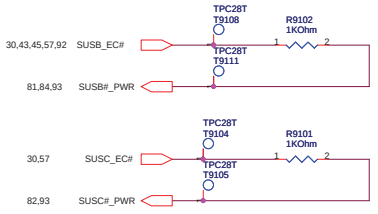
U9000 & U9001 colay

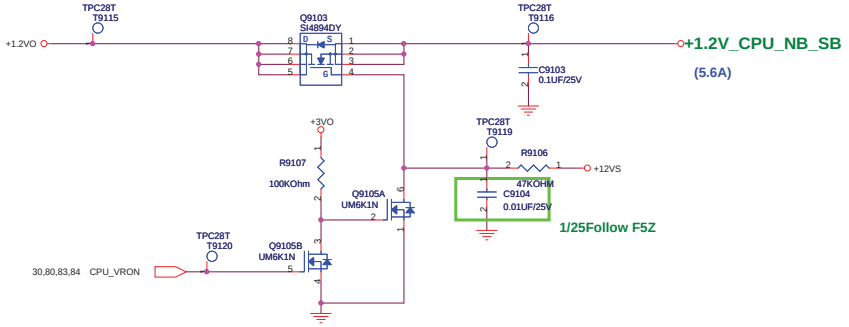
U9000 Main source change to 06G006002414(tolerence:1%).
Add second source 06G006002610 (tolerence:1%),
06G006002412 (tolerence:0.2%) and
06G006002020(tolerence:0.2%)

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 90 of 94	

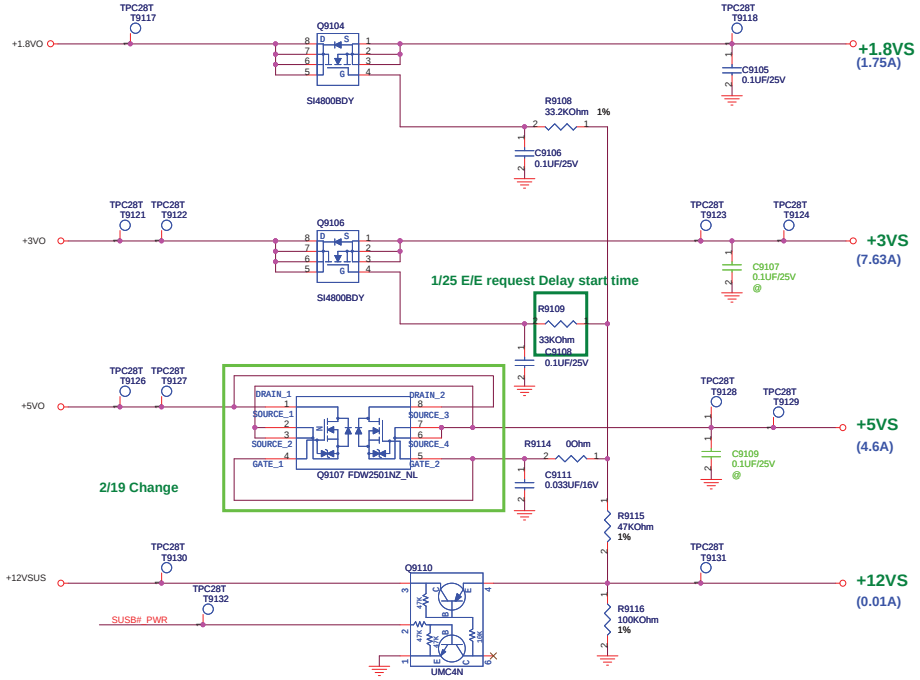
SUSC#_PWR POWER





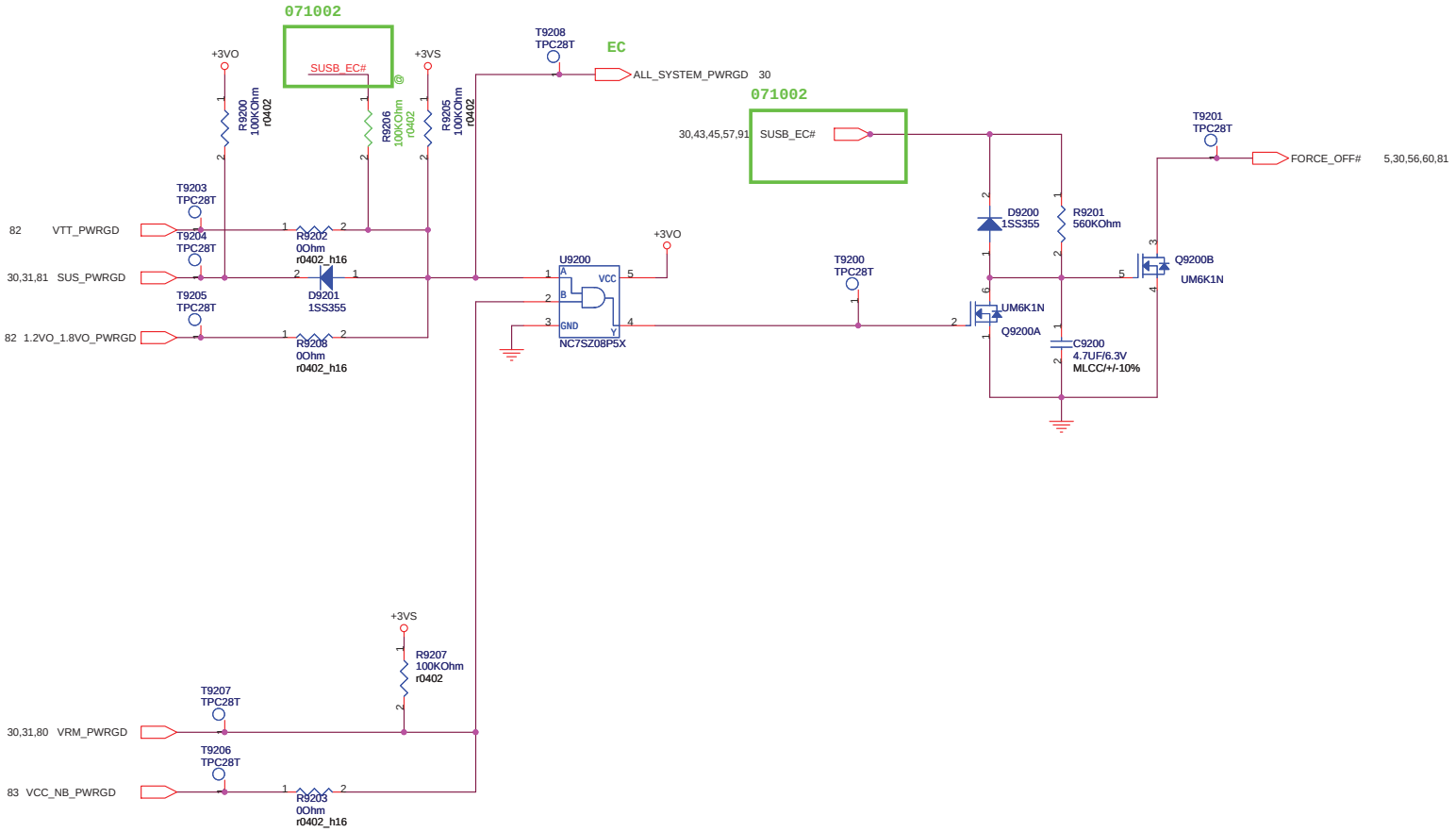


SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 91 of 94	

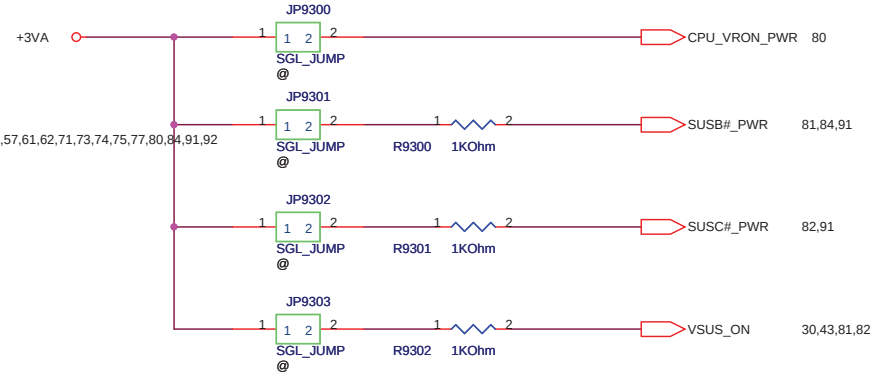
POWER GOOD DETECTER



Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 92 of 94	

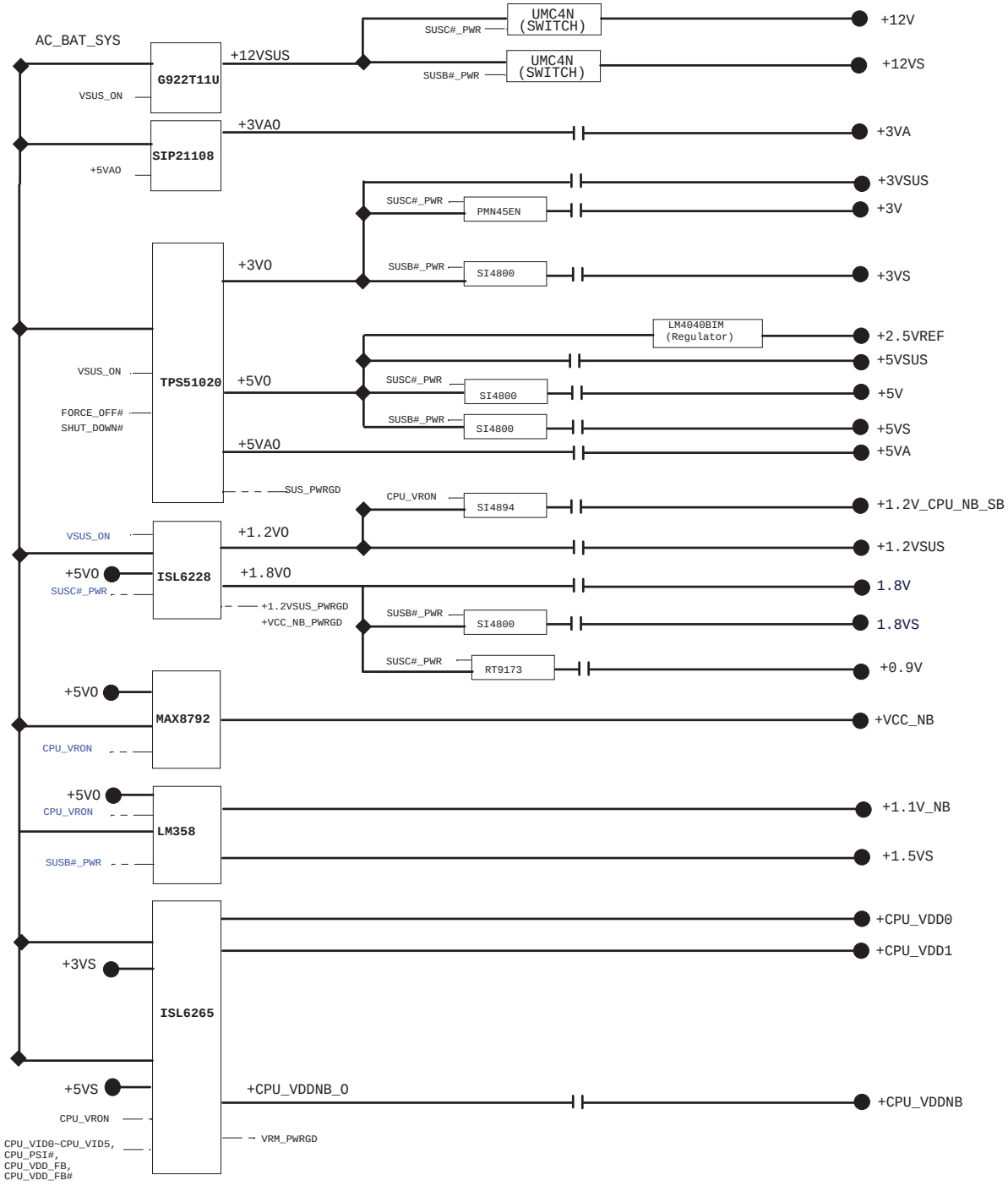
AC_BAT_SYS	AC_BAT_SYS	60,80,81,82,83,88
BAT	BAT	60,88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	82,84,88,90
+3VA	+3VA	20,30,45,56,57,61,62,81
+5VAO	+5VAO	81,84,90
+5VO	+5VO	81,82,88,90,91
+5VSUS	+5VSUS	81
+5V	+5V	44,45,52,57,91
+5VS	+5VS	23,30,31,36,37,46,50,51,57,71,80,83,91
+3VO	+3VO	56,81,91,92
+3VSUS	+3VSUS	4,20,21,22,23,24,30,33,35,37,43,53,56,80,81
+3V	+3V	30,35,44,45,53,55,57,61,62,83,91
+3VS	+3VS	5,7,8,12,13,14,21,22,23,24,29,30,31,33,36,37,43,45,46,50,51,53,55,56,57,61,62,71,73,74,75,77,80,84,91,92
+12VSUS	+12VSUS	81,84,91
+12V	+12V	37,57,75,91
+12VS	+12VS	30,45,57,71,91
+1.8VO	+1.8VO	82,84,91
+1.8V	+1.8V	4,5,6,7,8,9,57,82
+1.8VS	+1.8VS	5,12,13,14,21,57,91
+0.9V	+0.9V	4,6,9,57,82
+0.9VO	+0.9VO	82
+2.5V_CPU_VDDA	+2.5V_CPU_VDDA	5,57,84
+1.5VS	+1.5VS	43,53,55,57,84
+1.5VO	+1.5VO	84
+1.1VO	+1.1VO	84
+1.1V_NB	+1.1V_NB	12,14,57,84
+1.2VO	+1.2VO	82,84,91
+1.2VSUS	+1.2VSUS	23,82
+1.2V_CPU_NB_SB	+1.2V_CPU_NB_SB	3,14,20,22,23,57,91
+VCC_NB_O	+VCC_NB_O	83
+VCC_NB	+VCC_NB	14,57,83
+CPU_VDD0	+CPU_VDD0	6,57,80
+CPU_VDD1	+CPU_VDD1	6,57,80
+CPU_VDDNB_O	+CPU_VDDNB_O	80
+CPU_VDDNB	+CPU_VDDNB	6,57,80

FOR POWER TEST



<OrgName>	Title : POWER_SIGNAL		
	Engineer:		
Size: B	Project Name: F5Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 93 of 94		

F5Z



Title : POWER_FLOWCHART

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	F5Z	1.0

Date: Monday, May 19, 2008 Sheet 94 of 94