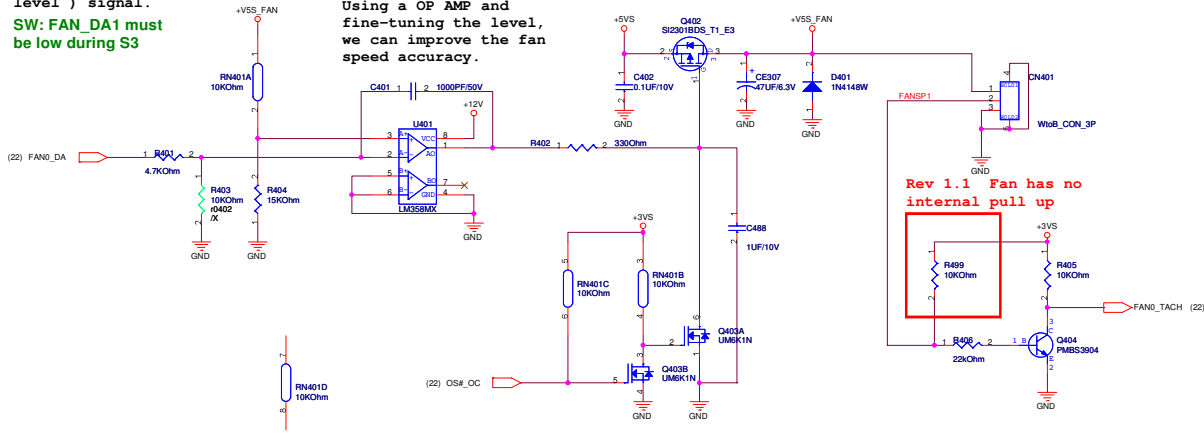


Fan Speed Control

KBC will issue a analog (a voltage level) signal.
SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

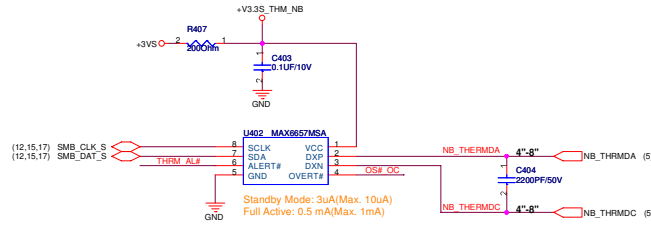


Route H_THERMDA and H_THERMDC on the same layer

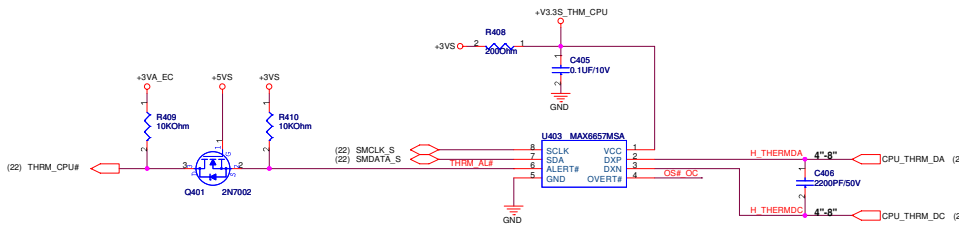
-----OTHER SIGNALS
12 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
12 mils
-----OTHER SIGNALS

Avoid BPSB,Power

Rev 1.1 Fan has no internal pull up



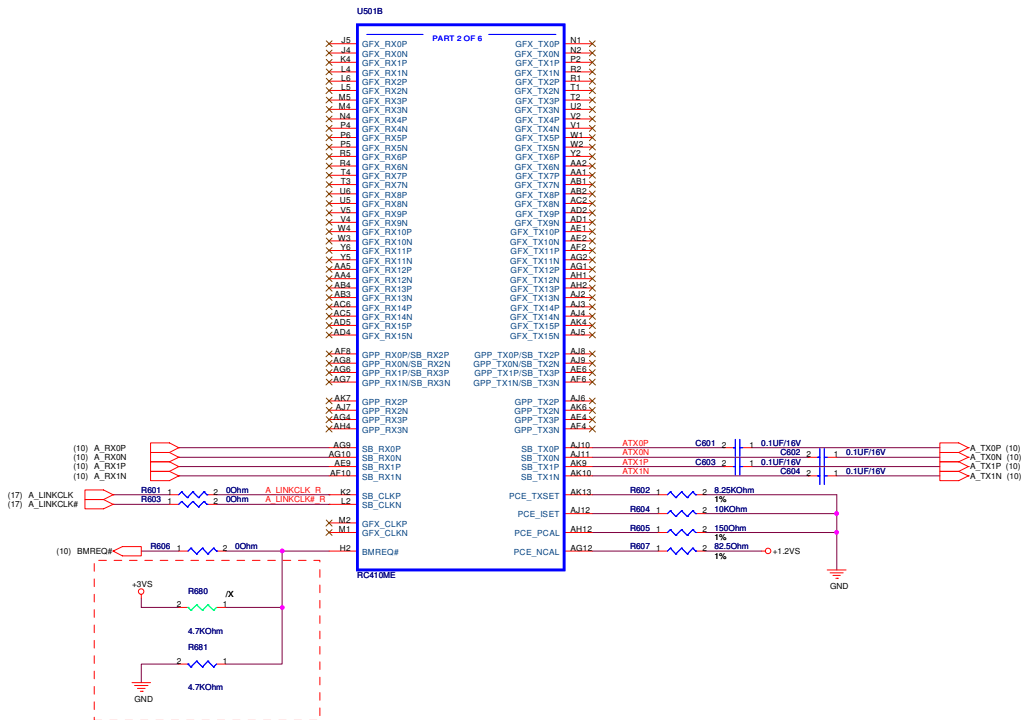
NB Detect



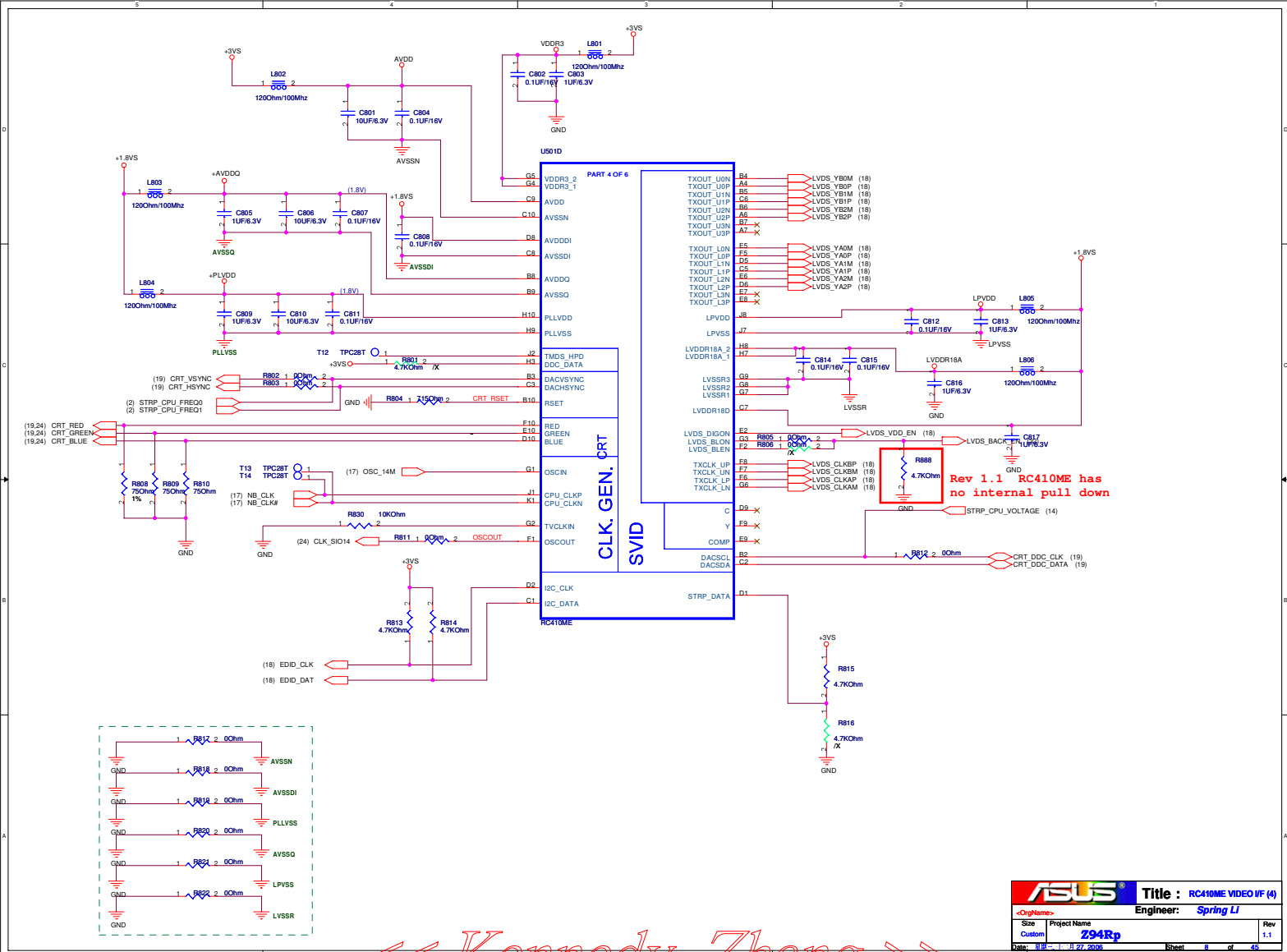
CPU Detect

« Kennedy_Zhang »

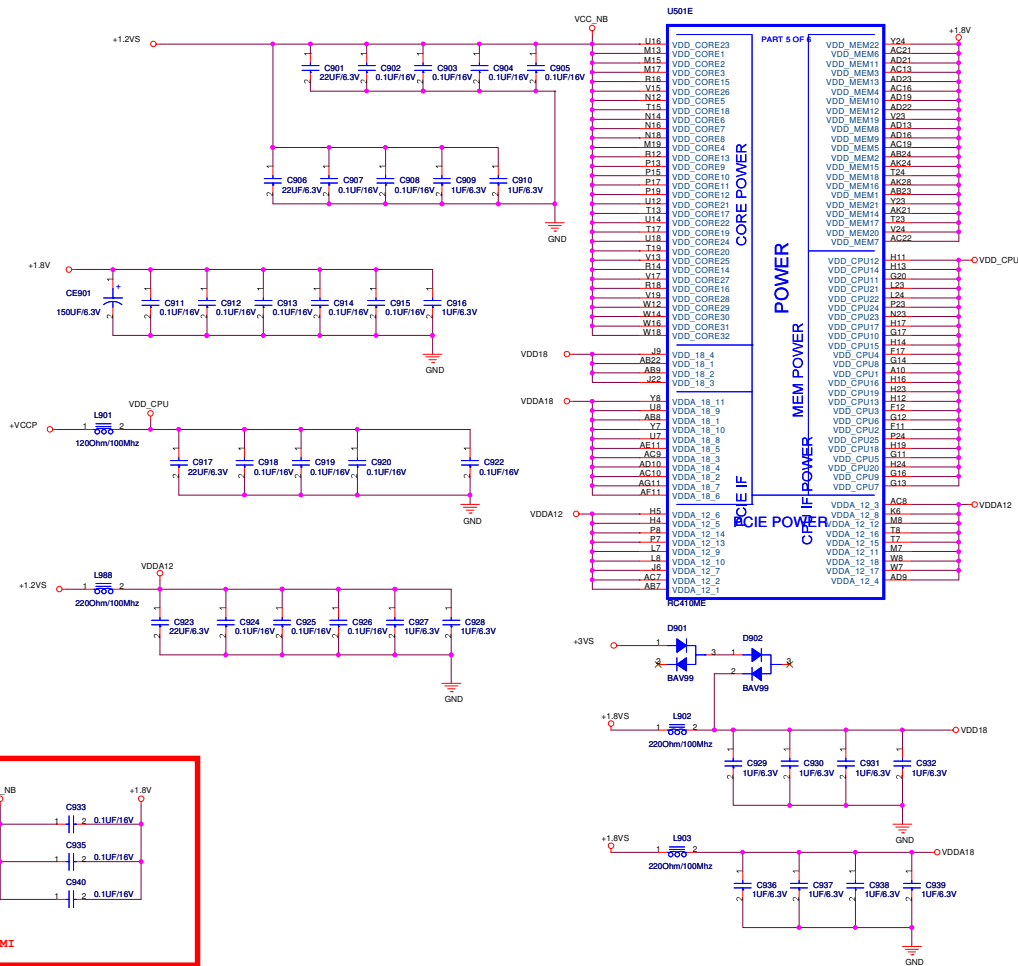
ASUS		Title : THERMAL SENSOR.FAN	
Size		Engineer: Spring LI	
Custom	Project Name	Z94Rp	
Date: 2008-05-23	Rev	1.1	
Sheet 4 of 45			



<< Kennedy_Zhang >>

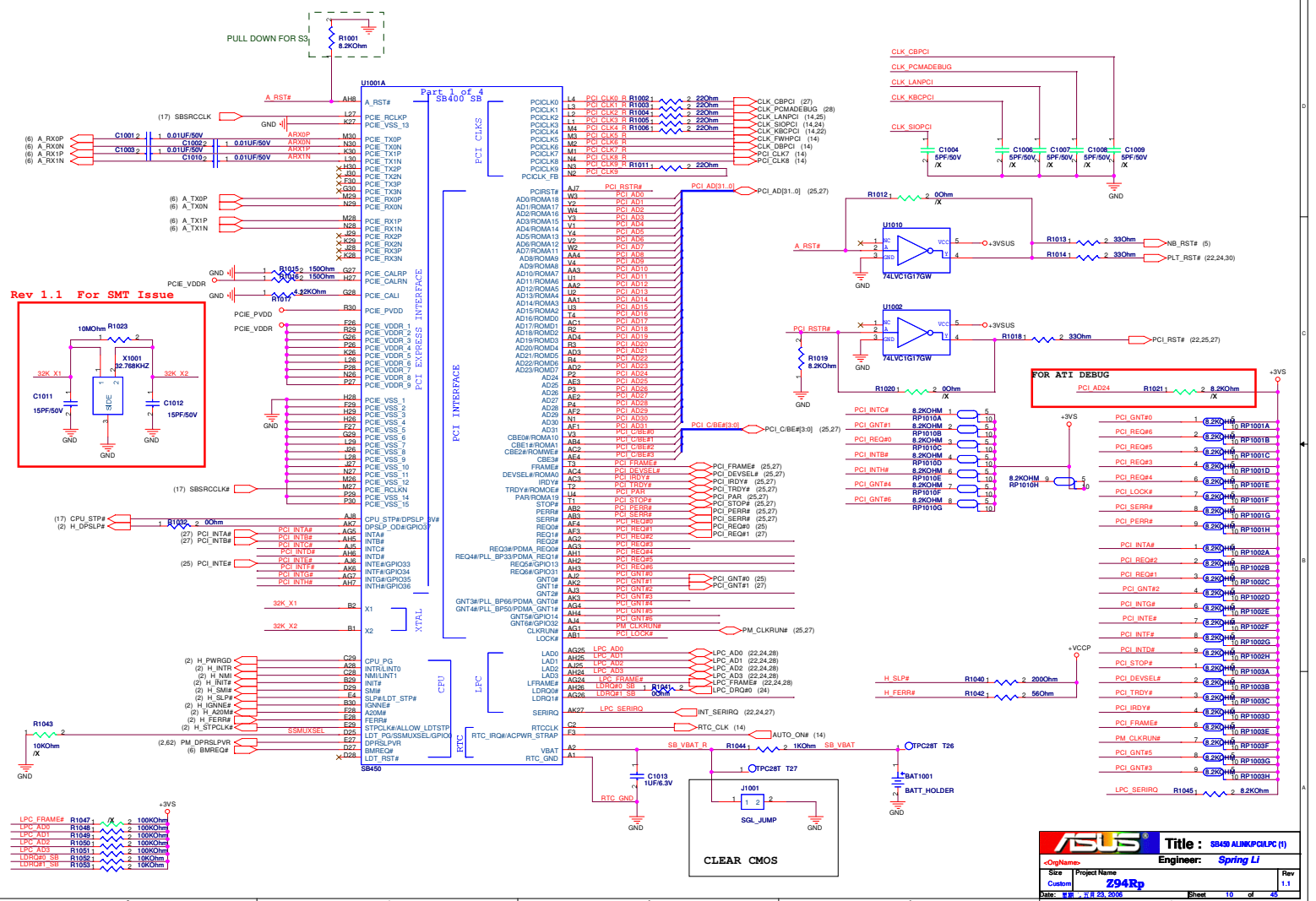


<< Kennedy_Zhang >>

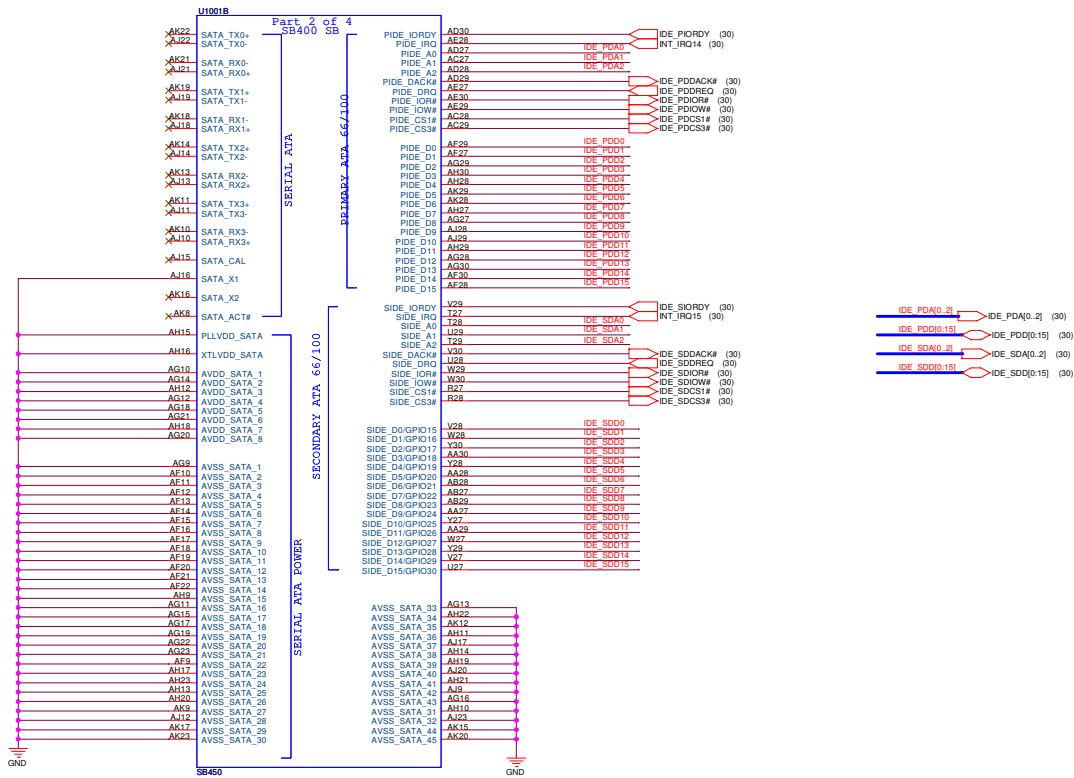


PART 5 OF 6		
W5	VSSA40	VSS70
W6	VSSA41	VSS71
W7	VSSA42	VSS72
W8	VSSA43	VSS73
W9	VSSA44	VSS74
W10	VSSA45	VSS75
W11	VSSA46	VSS76
W12	VSSA47	VSS77
W13	VSSA48	VSS78
W14	VSSA49	VSS79
W15	VSSA50	VSS80
W16	VSSA51	VSS81
W17	VSSA52	VSS82
W18	VSSA53	VSS83
W19	VSSA54	VSS84
W20	VSSA55	VSS85
W21	VSSA56	VSS86
W22	VSSA57	VSS87
W23	VSSA58	VSS88
W24	VSSA59	VSS89
W25	VSSA60	VSS90
W26	VSSA61	VSS91
W27	VSSA62	VSS92
W28	VSSA63	VSS93
W29	VSSA64	VSS94
W30	VSSA65	VSS95
W31	VSSA66	VSS96
W32	VSSA67	VSS97
W33	VSSA68	VSS98
W34	VSSA69	VSS99
W35	VSSA70	VSS100
W36	VSSA71	VSS101
W37	VSSA72	VSS102
W38	VSSA73	VSS103
W39	VSSA74	VSS104
W40	VSSA75	VSS105
W41	VSSA76	VSS106
W42	VSSA77	VSS107
W43	VSSA78	VSS108
W44	VSSA79	VSS109
W45	VSSA80	VSS110
W46	VSSA81	VSS111
W47	VSSA82	VSS112
W48	VSSA83	VSS113
W49	VSSA84	VSS114
W50	VSSA85	VSS115
W51	VSSA86	VSS116
W52	VSSA87	VSS117
W53	VSSA88	VSS118
W54	VSSA89	VSS119
W55	VSSA90	VSS120
W56	VSSA91	VSS121
W57	VSSA92	VSS122
W58	VSSA93	VSS123
W59	VSSA94	VSS124
W60	VSSA95	VSS125
W61	VSSA96	VSS126
W62	VSSA97	VSS127
W63	VSSA98	VSS128
W64	VSSA99	VSS129
W65	VSSA100	VSS130
W66	VSSA101	VSS131
W67	VSSA102	VSS132
W68	VSSA103	VSS133
W69	VSSA104	VSS134
W70	VSSA105	VSS135
W71	VSSA106	VSS136
W72	VSSA107	VSS137
W73	VSSA108	VSS138
W74	VSSA109	VSS139
W75	VSSA110	VSS140
W76	VSSA111	VSS141
W77	VSSA112	VSS142
W78	VSSA113	VSS143
W79	VSSA114	VSS144
W80	VSSA115	VSS145
W81	VSSA116	VSS146
W82	VSSA117	VSS147
W83	VSSA118	VSS148
W84	VSSA119	VSS149
W85	VSSA120	VSS150

<< Kennedy_Zhang >>

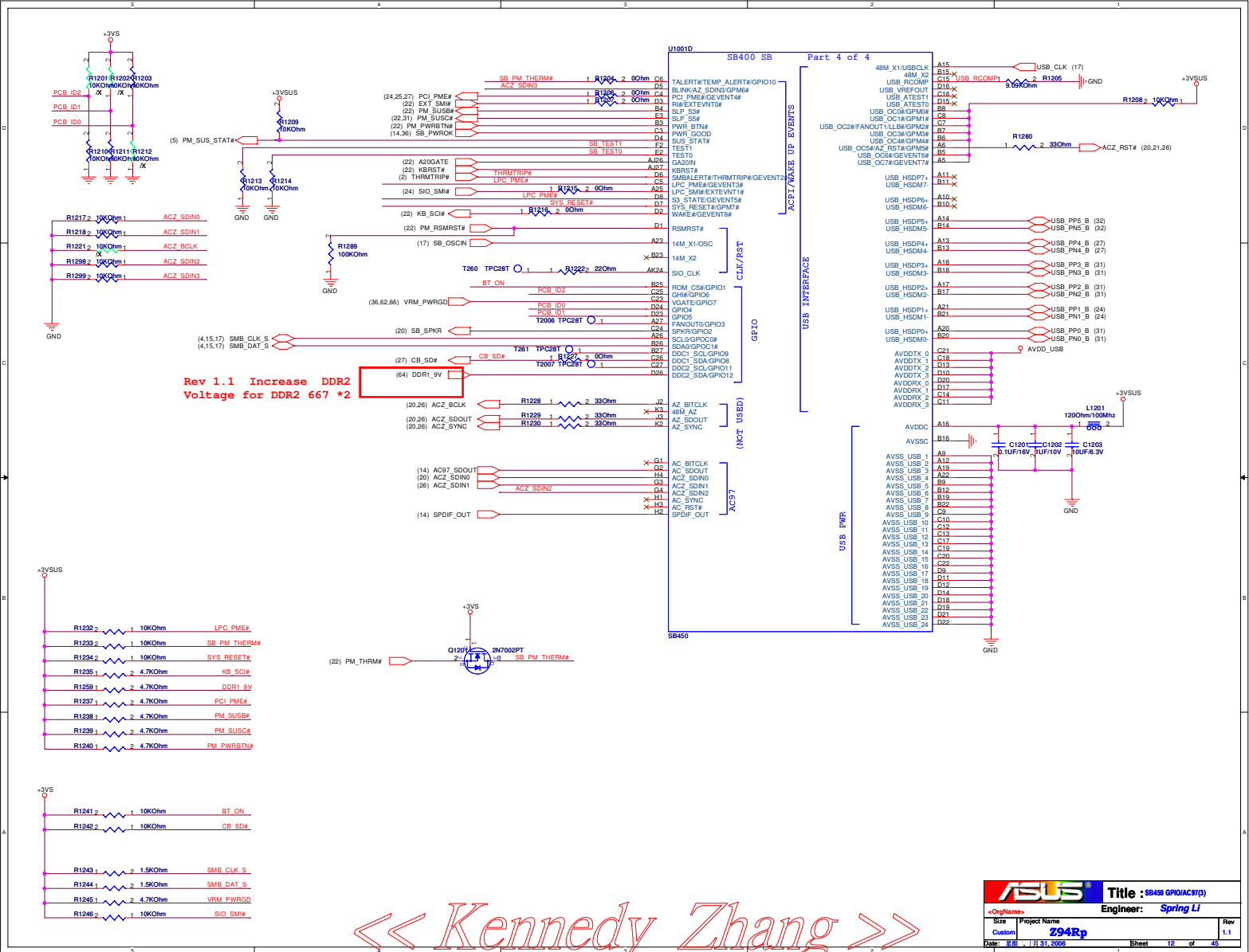


<< Kennedy_Zhang >>

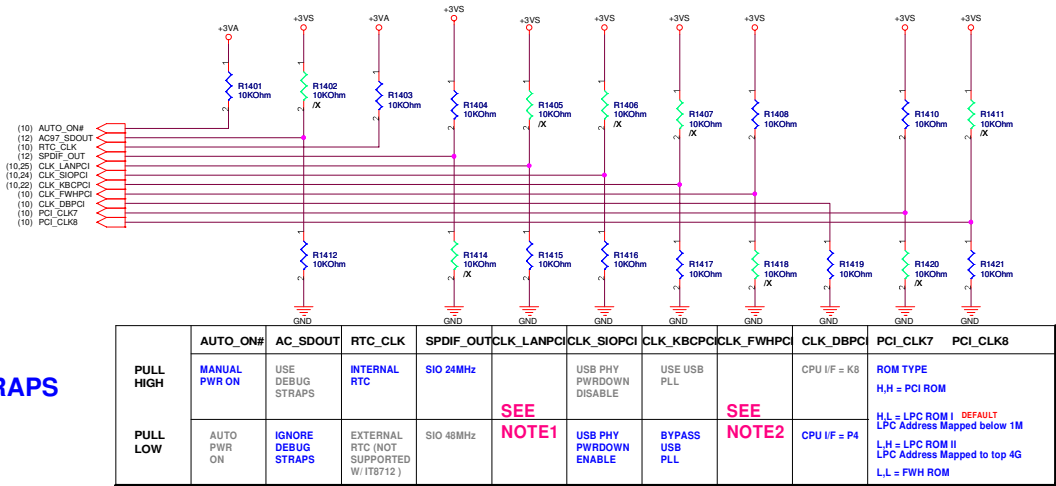


<< Kennedy_Zhang >>

ASUS		Title : S845 IDE 2
<OrgName>		Engineer: Spring LI
Size	Project Name	Rev
Custom	Z94Rp	1.1
Date: 8.8.2008	Sheet 11	of 45



REQUIRED STRAPS

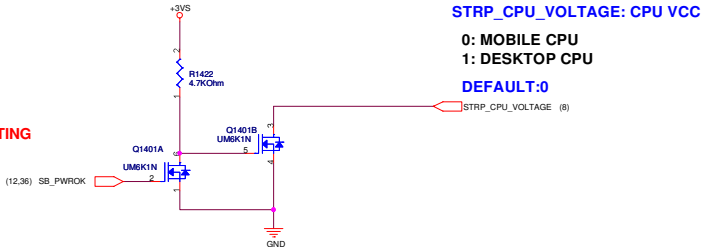


NOTE
1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

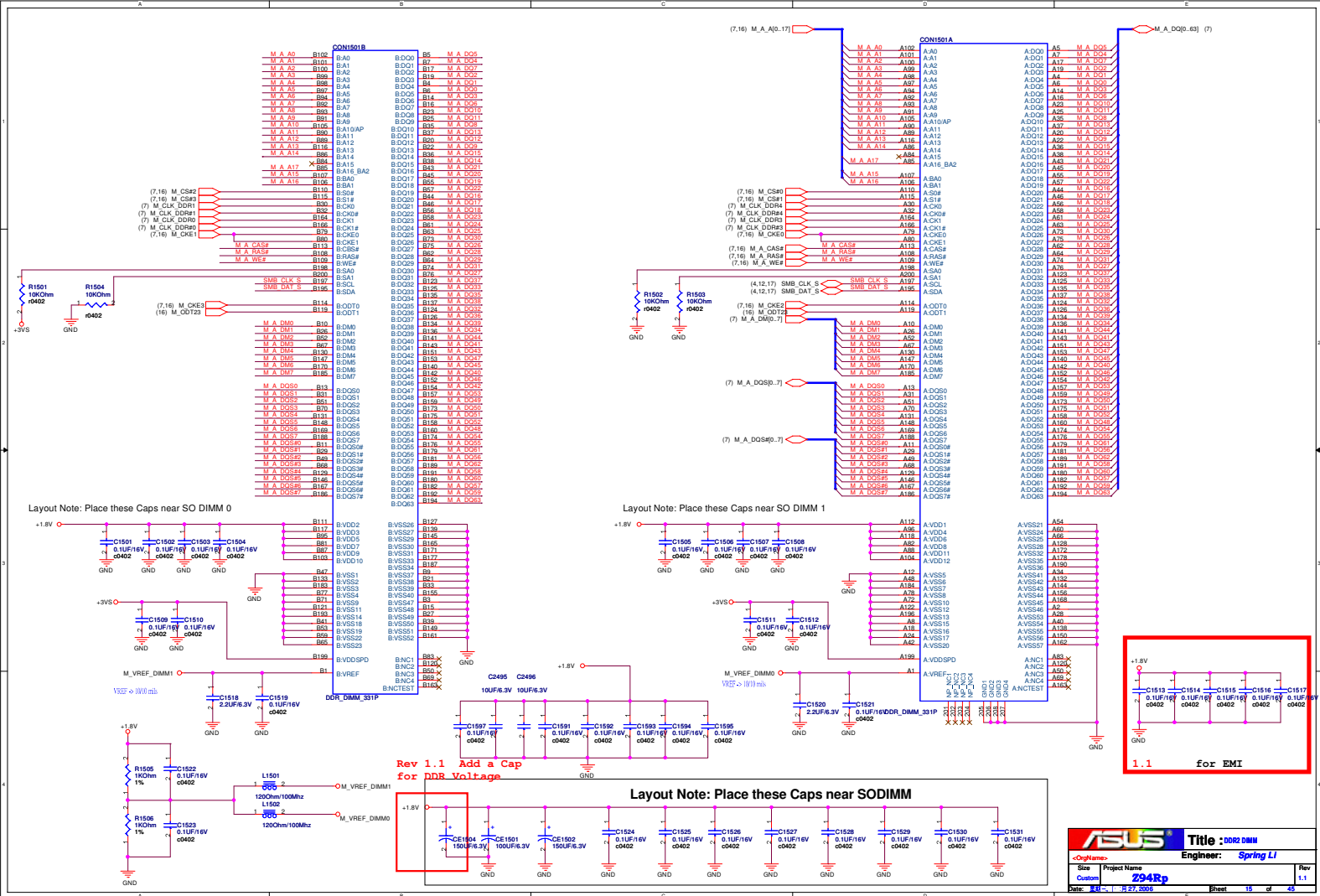
2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH



ASUS		Title : SB450 STRAPS(5)	
-OrigName-		Engineer: Spring Li	
Site	Project Name		Rev
Custm	Z94Rp		1.1
Date: 8/8	7/8/2006	Sheet 14	of 45

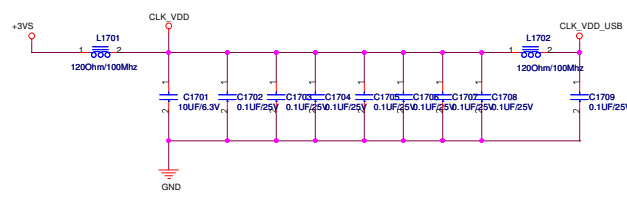
<< Kennedy_Zhang >>



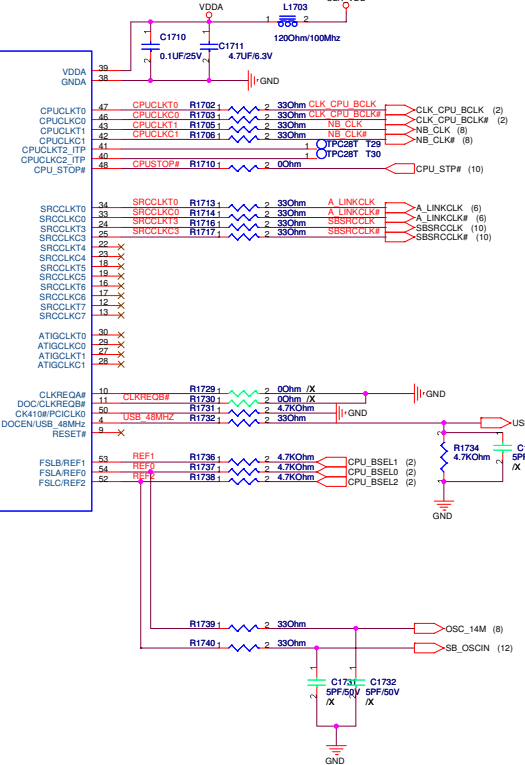
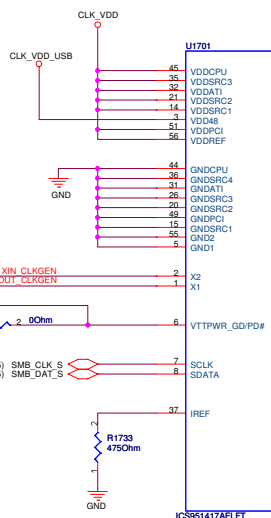
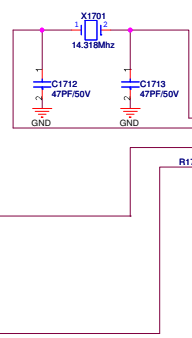
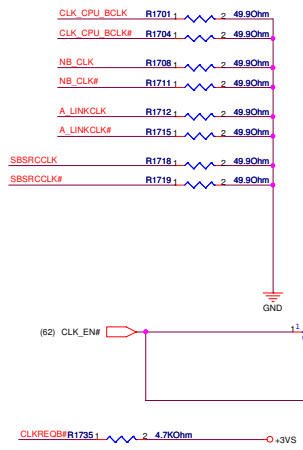
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



PLACE termination close to source IC



BCLK	FSB	BSEL0	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Title :CLOCK GENERATOR

<OrgName>
 Engineer: Spring Li

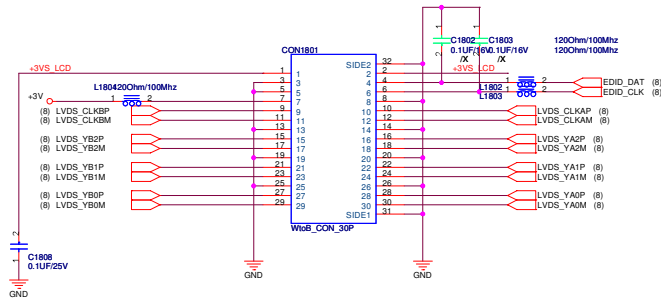
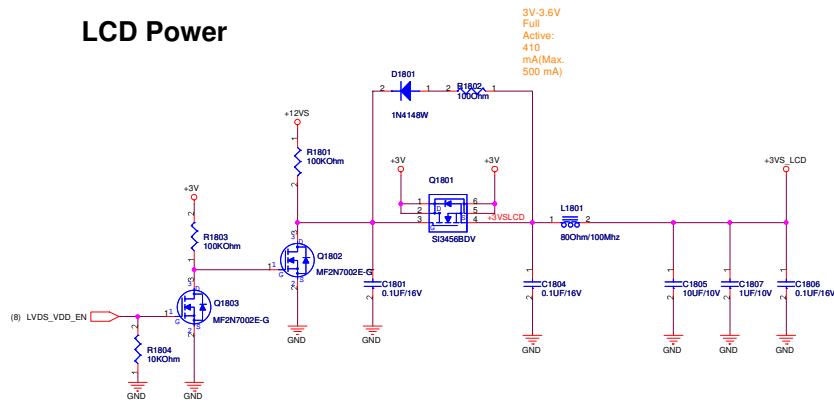
Size
 Project Name
 Rev

Custom
 Z94Rp
 1.1

Date: 2006.05.23
 Sheet 17 of 46

<< Kennedy_Zhang >>

LCD Power

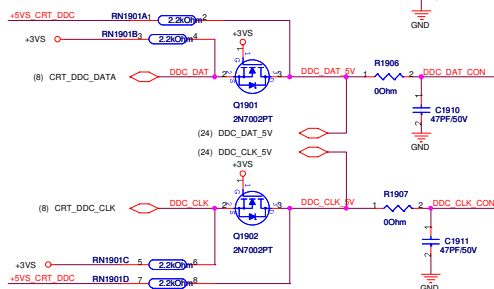
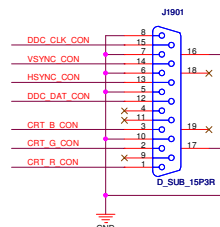
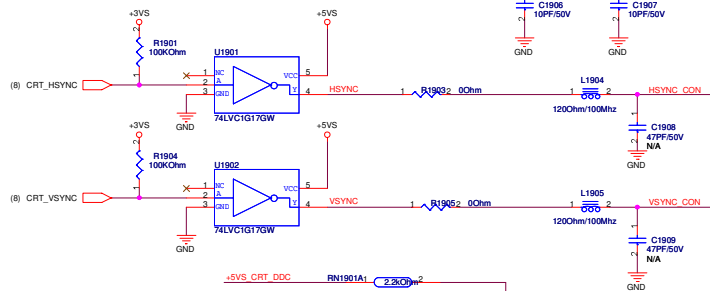
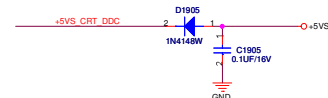
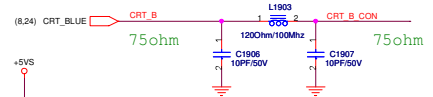
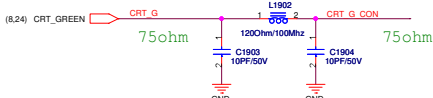
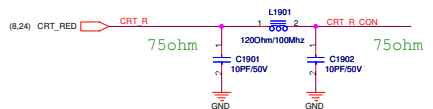
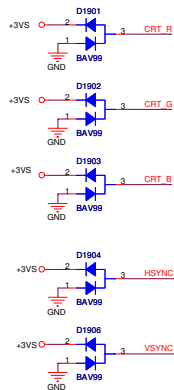


Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

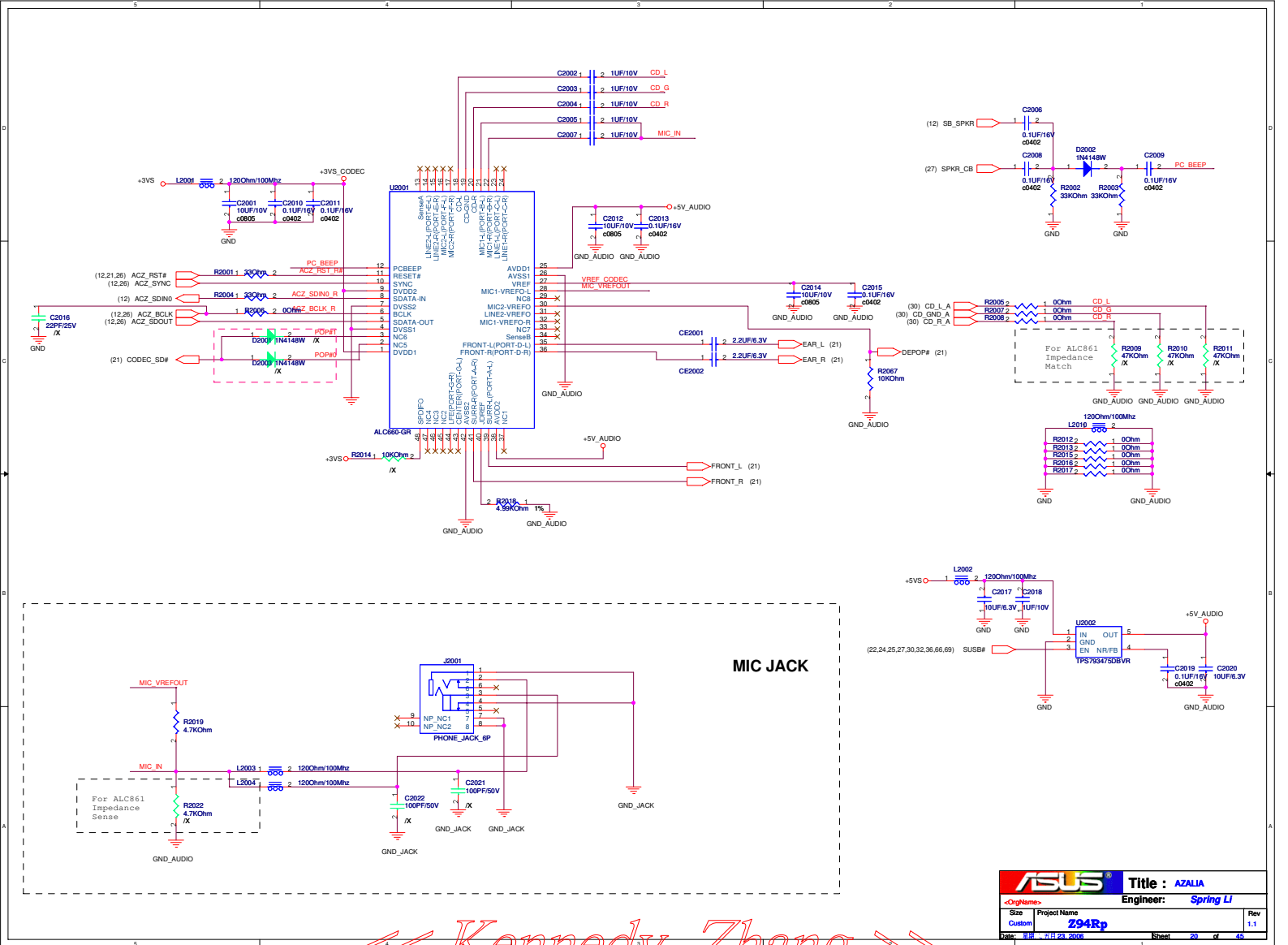
<< Kennedy_Zhang >>

ASUS		Title : LVDS & INVERTER (CAMERA)	
<OrigName>		Engineer: Spring Li	
Size	Project Name	Rev	
Custom	Z94Rp	1.1	
Date: 8/22/2020	Sheet: 18	of 48	



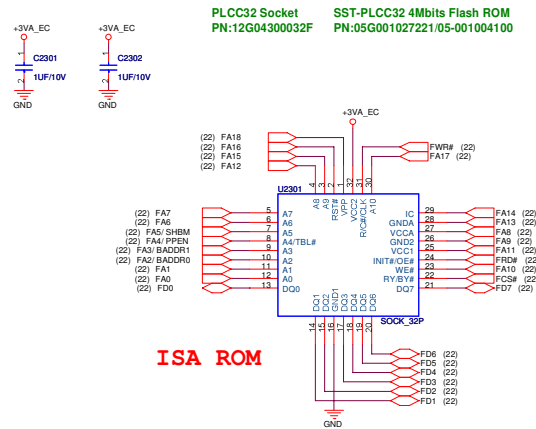
« Kennedy_Zhang »

ASUS		Title : CRT CONNECTOR	
<OrigName>		Engineer: Spring Li	
Size	Project Name		Rev
Custom	294Rp		1.1
Date: 8/22/2008		Sheet: 19	of 48



« Kennedy_Zhang »

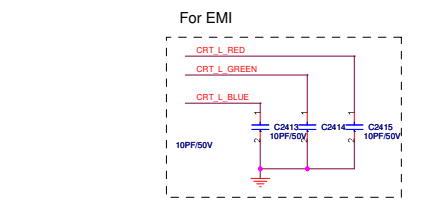
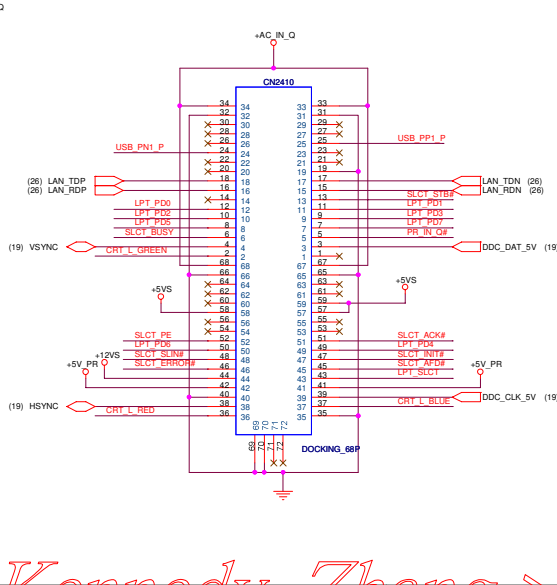
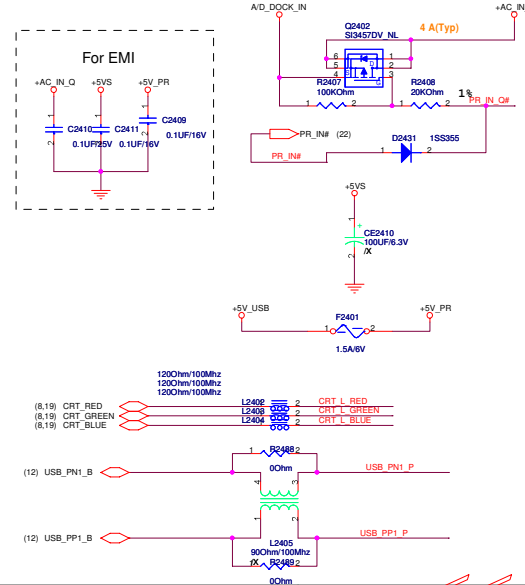
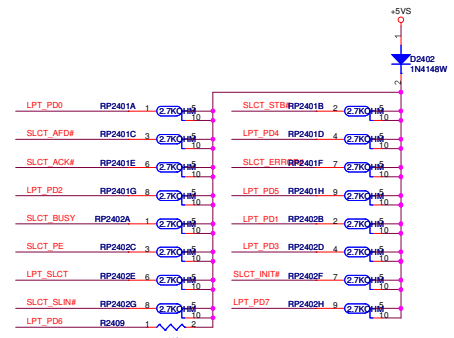
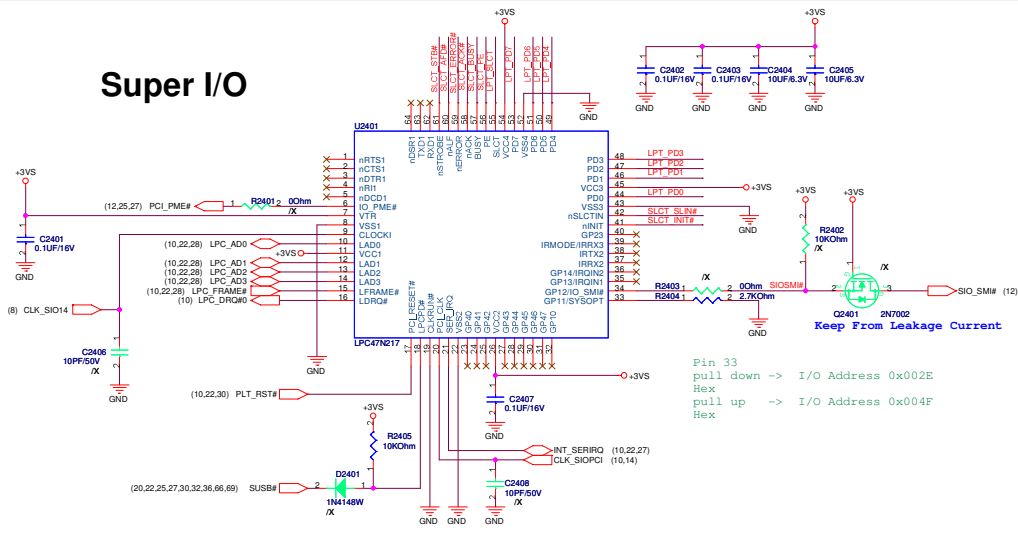




<< Kennedy_Zhang >>

ASUS		Title : ISA ROM & SPI ROM	
<OrigName>		Engineer: Spring LI	
Size	Project Name	Rev	
Custom	794Rp	1.1	
Date: 8/8/2008	Sheet 23 of 48		

Super I/O



ASUS		Title : Blank	
Project Name		Engineer: Spring LI	
Size	Custom	Rev	1.1
Date: 8/8/2008		Sheet: 24 of 45	

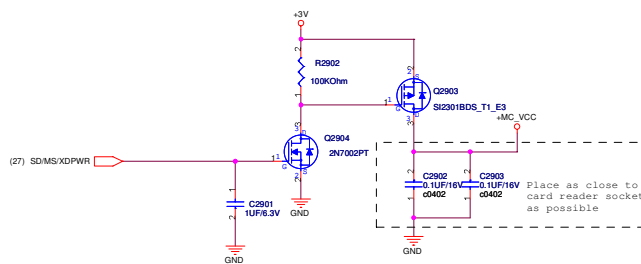
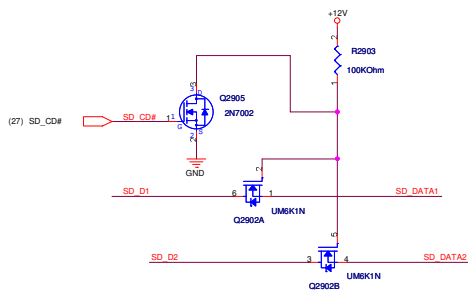
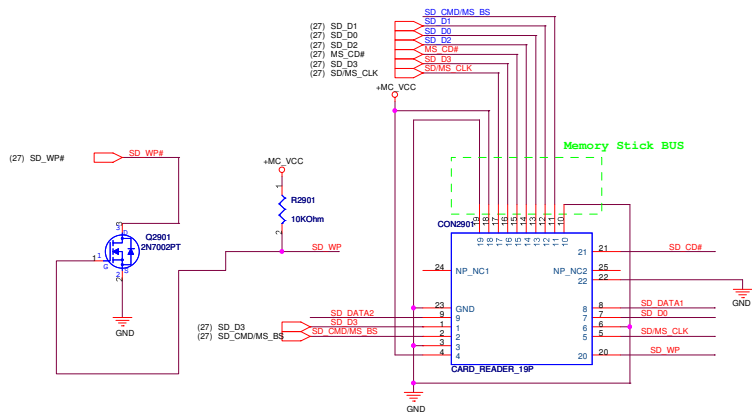
« Kennedy_Zhang »



Memory Card Detect

MS_CD#	SD_CD#	Not Support
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

MC_CD# : Memory Card Detect



Title : 4IN 1 CON

Engineer: Spring LI

Size

Project Name

Rev

Custom

Z94Rp

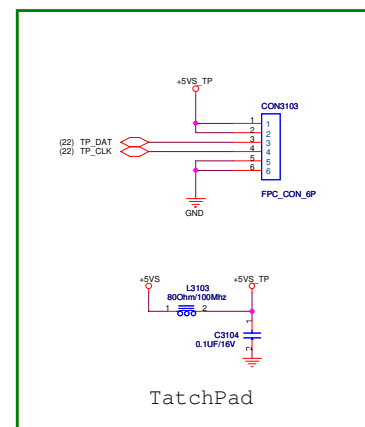
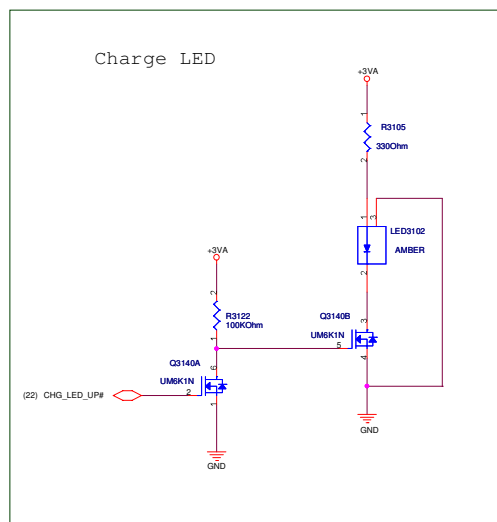
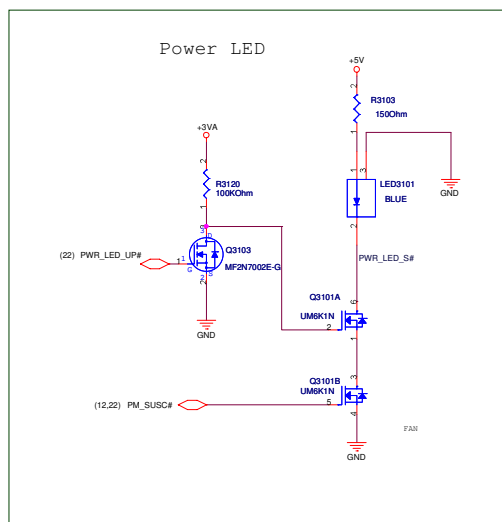
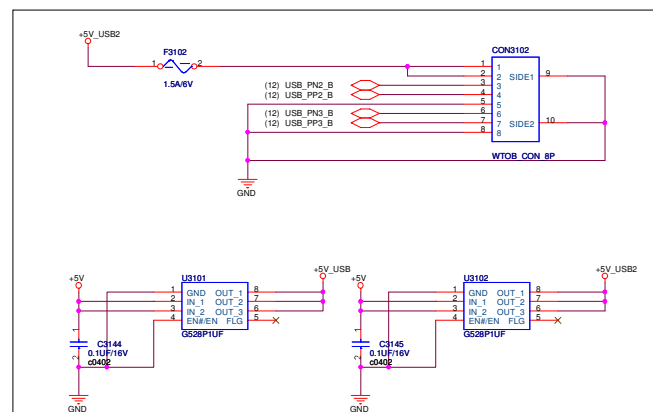
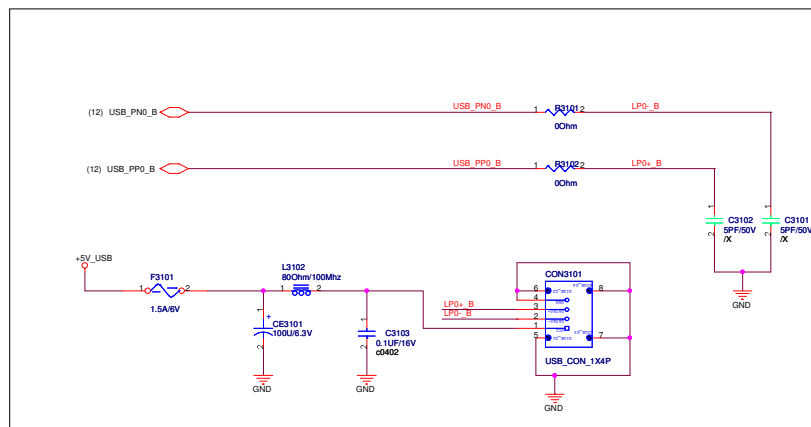
1.1

Date: 8/2/2008

Sheet 28 of 48

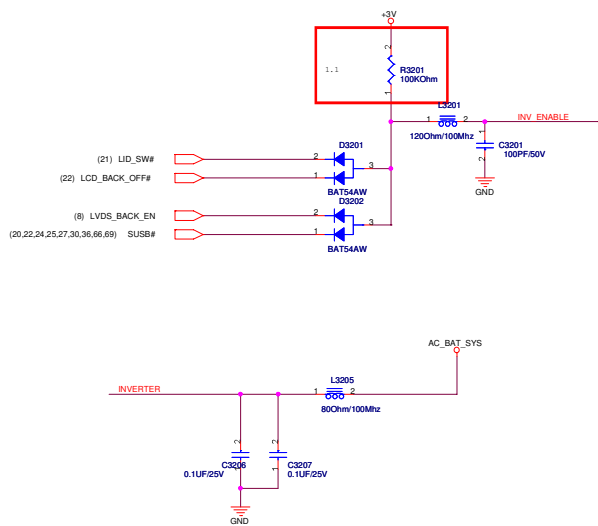
<< Kennedy_Zhang >>

USB

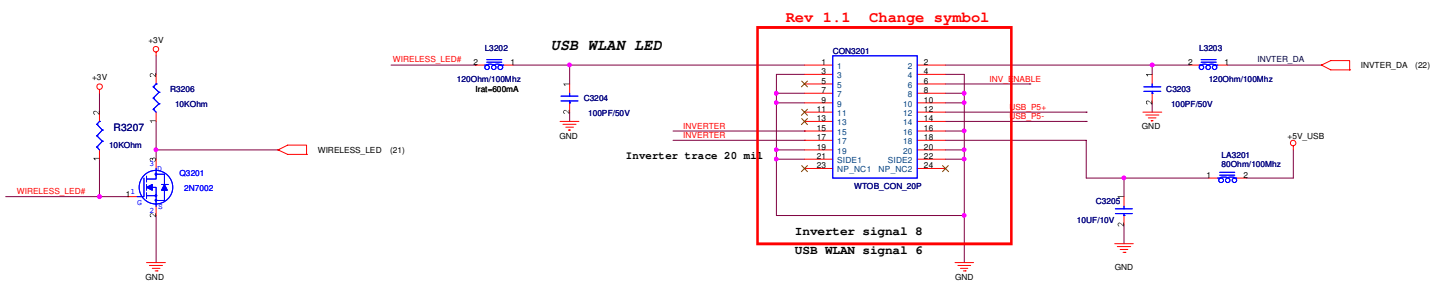
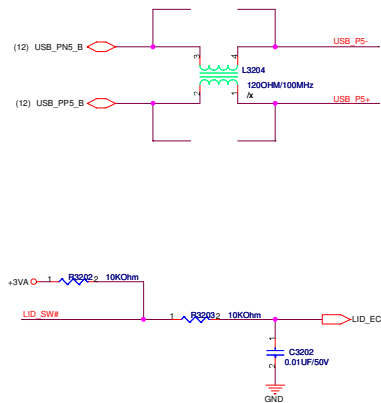


ASUS		Title : USB / LED / TP	
Engineer: Spring Li		Rev: 1.1	
Size: Custom	Project Name: Z94Rp	Date: 8/8/2018	
Sheet: 31		of 48	

<< Kennedy_Zhang >>

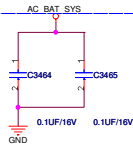
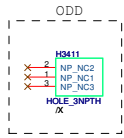
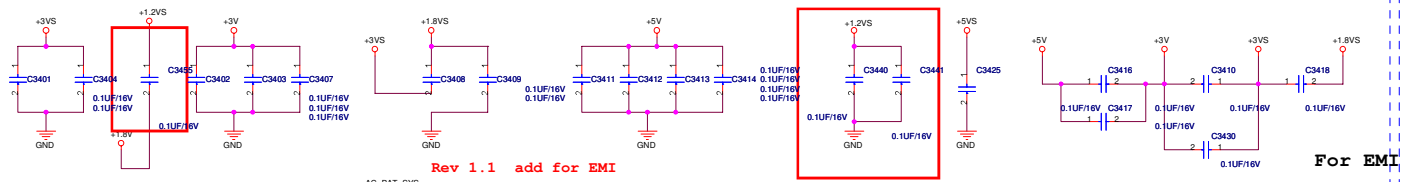


USB WIRESSLEE LAN

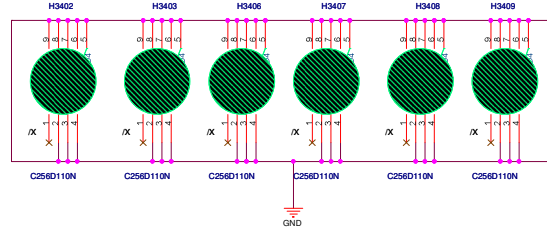


ASUS		Title : FUNCTION KEY & BT	
Engineer: Spring LI		Rev 1.1	
Size	Project Name	Date: 8/23/2018	
Custom	294Rp	Sheet 32 of 48	

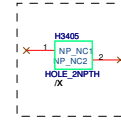
<< Kennedy_Zhang >>



Hole no GND --- A



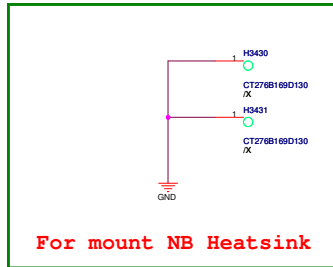
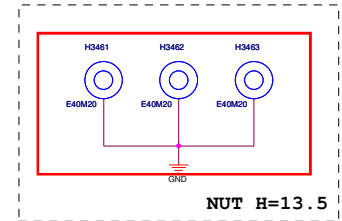
PAD Hole (2hole) --- E



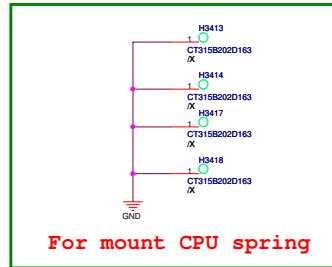
Oblong drill hole



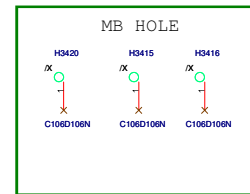
For HDD



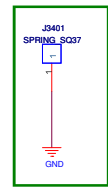
For mount NB Heatsink



For mount CPU spring



MB HOLE

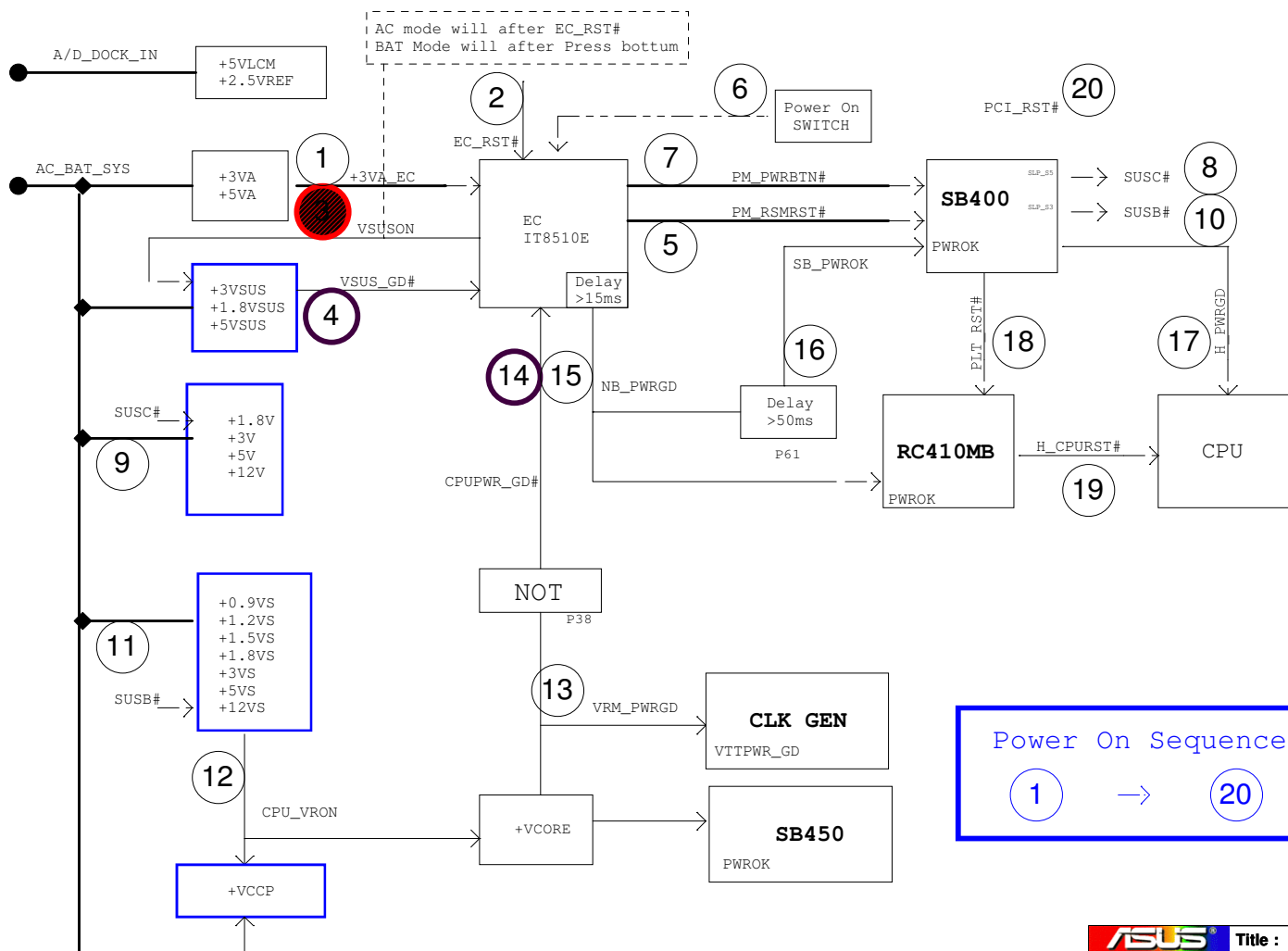


For EMI

PTH Hole

ASUS		Title : Hole	
Engineer: Spring LI		Rev	
Size	Project Name	Date: 2008.05.18.2008	
Custom	294Rp	Sheet 33 of 45	

<< Kennedy_Zhang >>



Power On Sequence

1 → 20

« Kennedy_Zhang »

ASUS		Title : Power Sequence	
Engineer: Spring Li		Rev: 1.1	
Size	Project Name	Date: 2024.04.20	
Custom	294Rp	Sheet: 34 of 45	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	
GPIO 31	I/O	S0	PCI_GNT#5
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0 -> 8 W/V 1 -> NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

**Title : SYSTEM RESOURCE**

Engineer: *Spring Li*

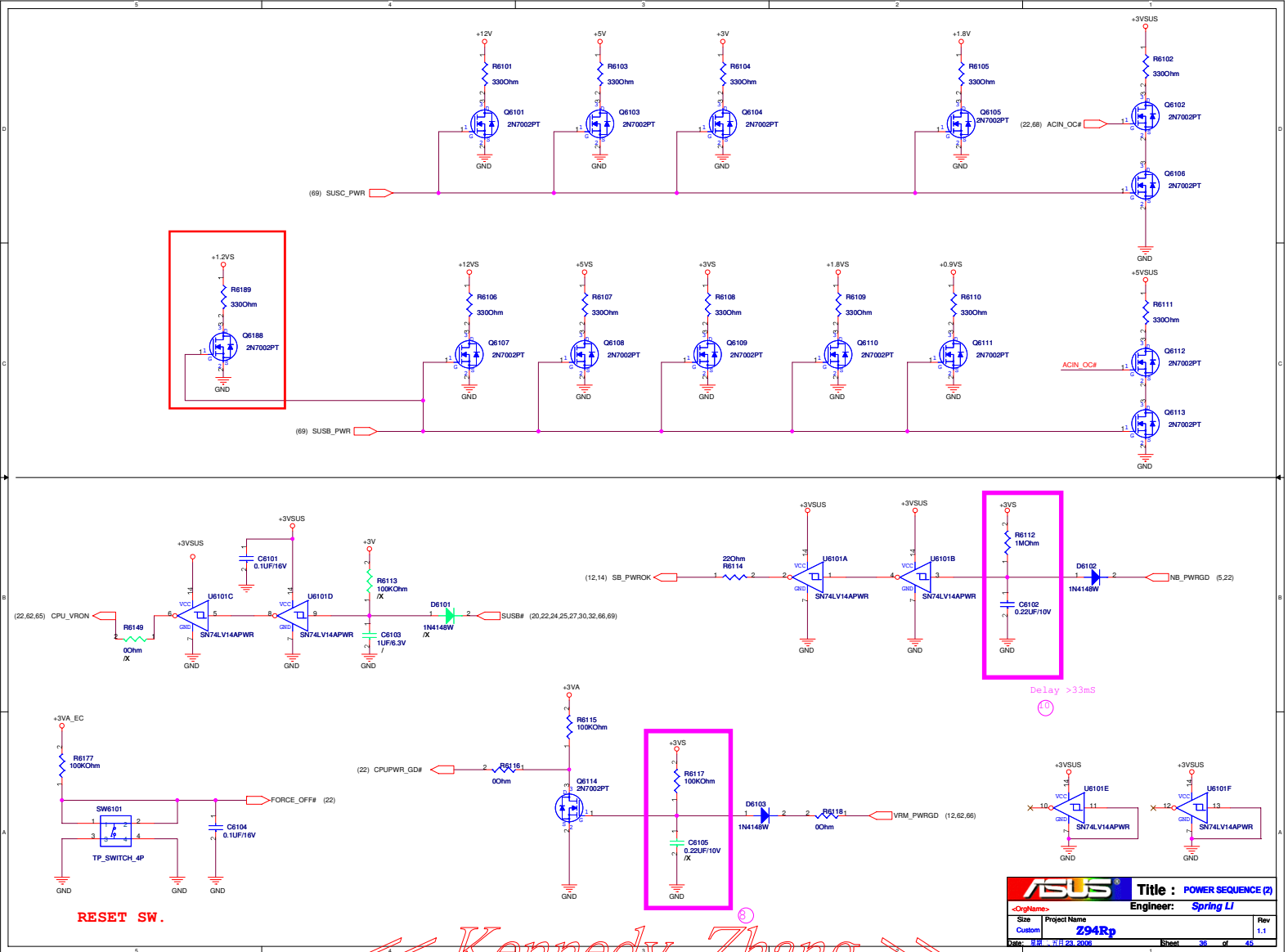
Size
Custom

Project Name
Z94Rp

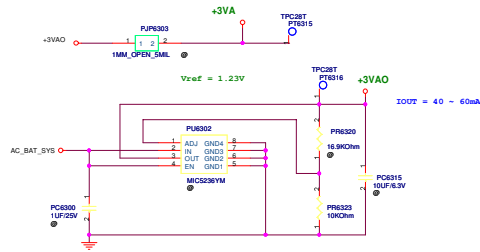
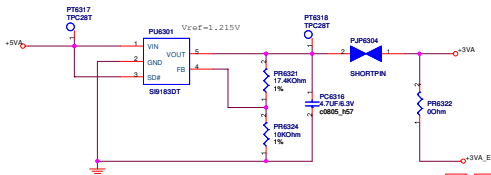
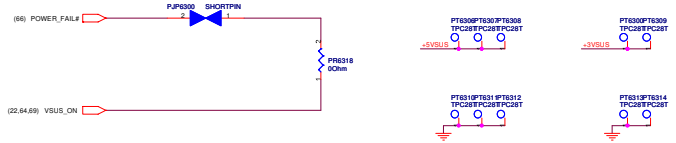
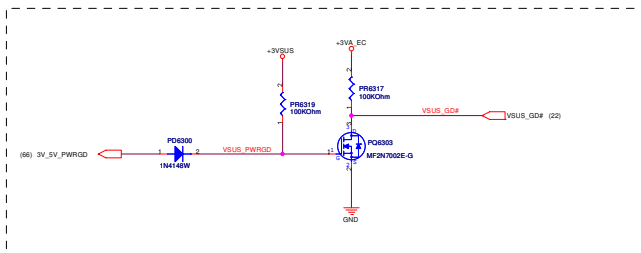
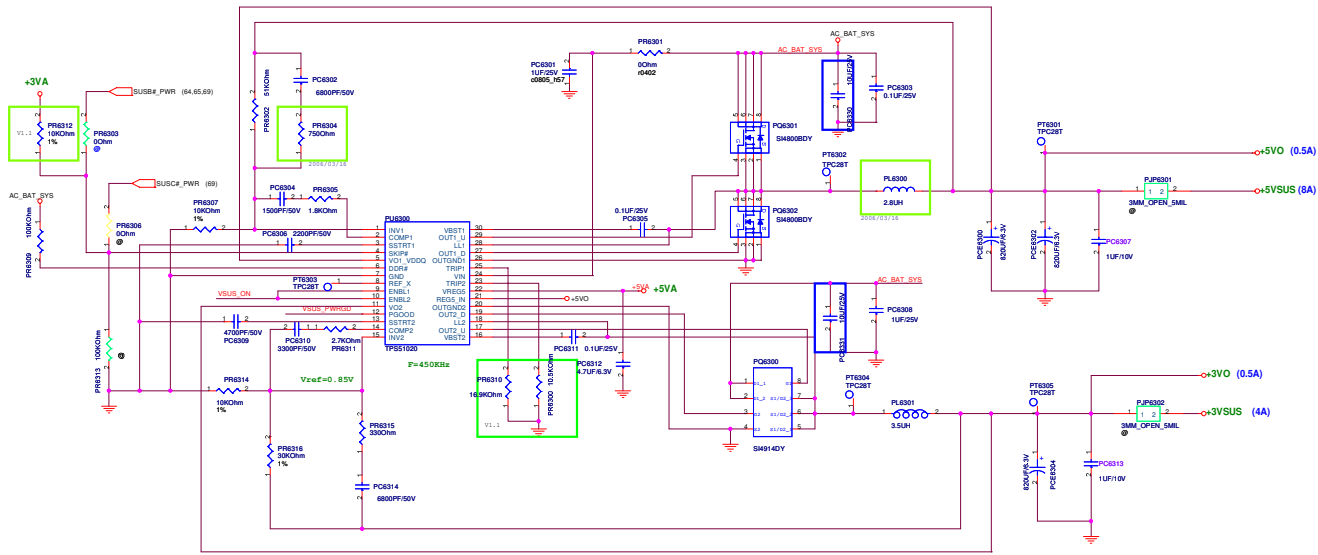
Rev
1.1

Date: *2024.04.20*Sheet: *35* of *45*

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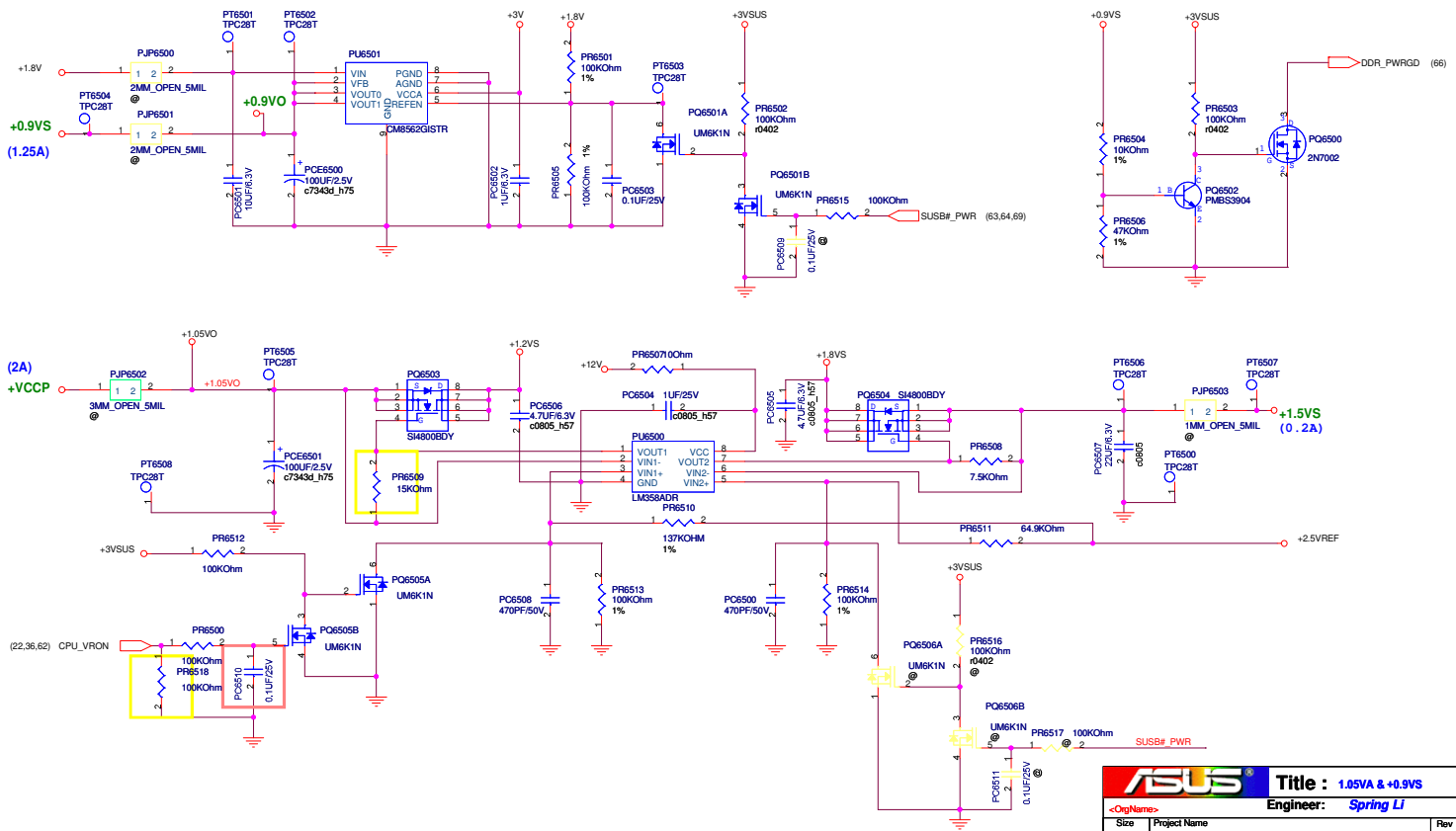


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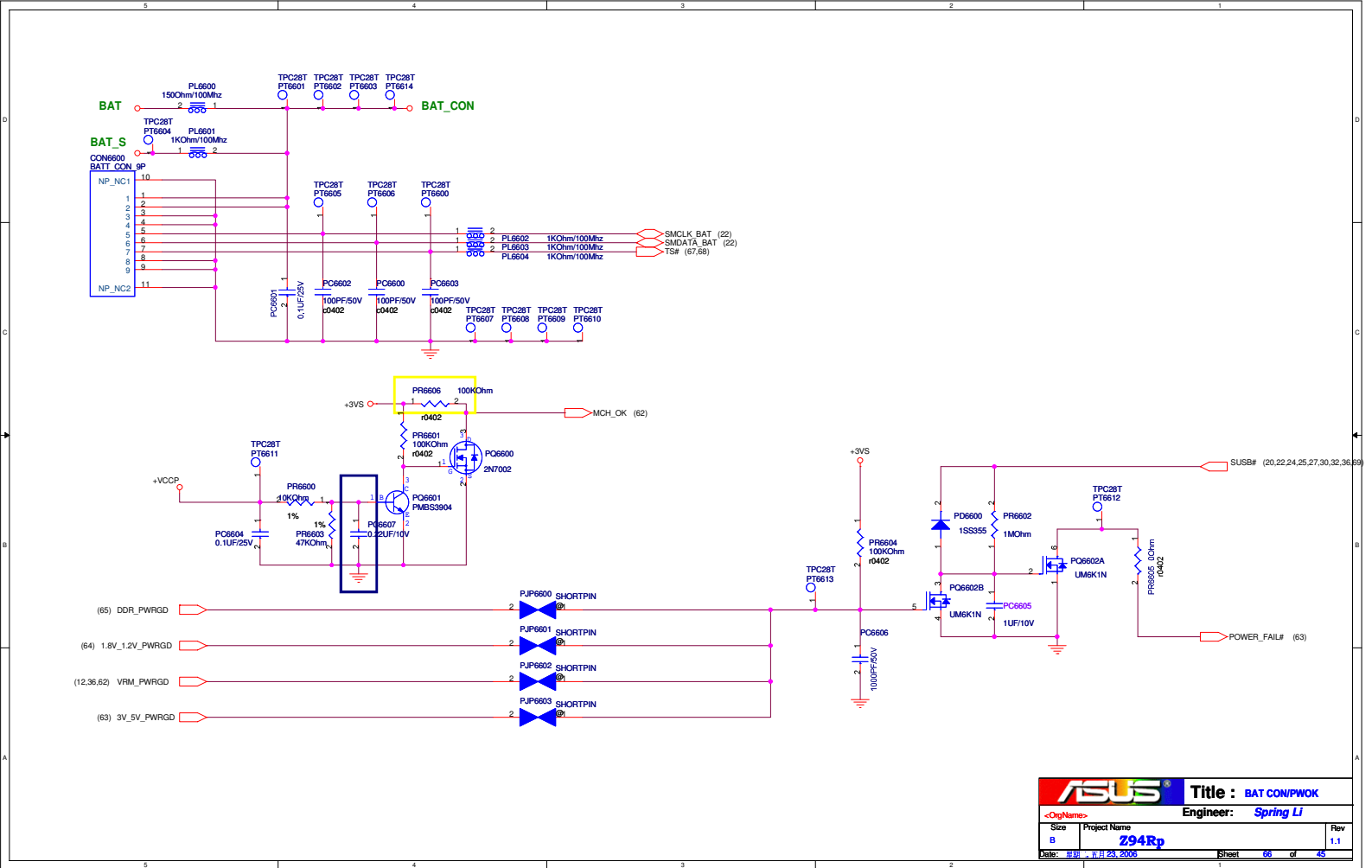


ASUS			Title : SYSTEM +5VA & +3VA	
Ver	Project Name	Engineer	Spring LJ	
C		294Rp	Rev	
Date: 11-15-2009			Sheet	61 of 61

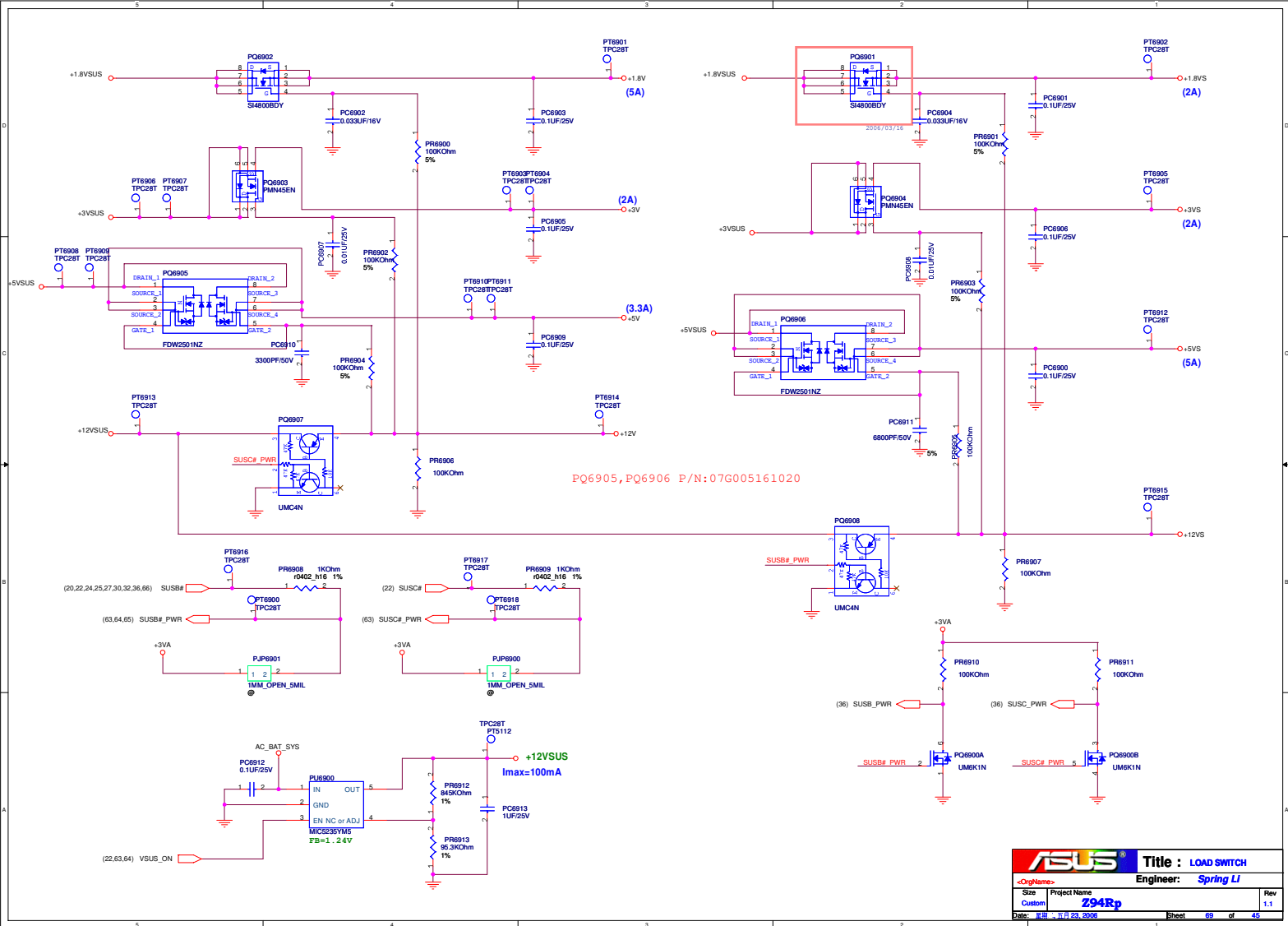
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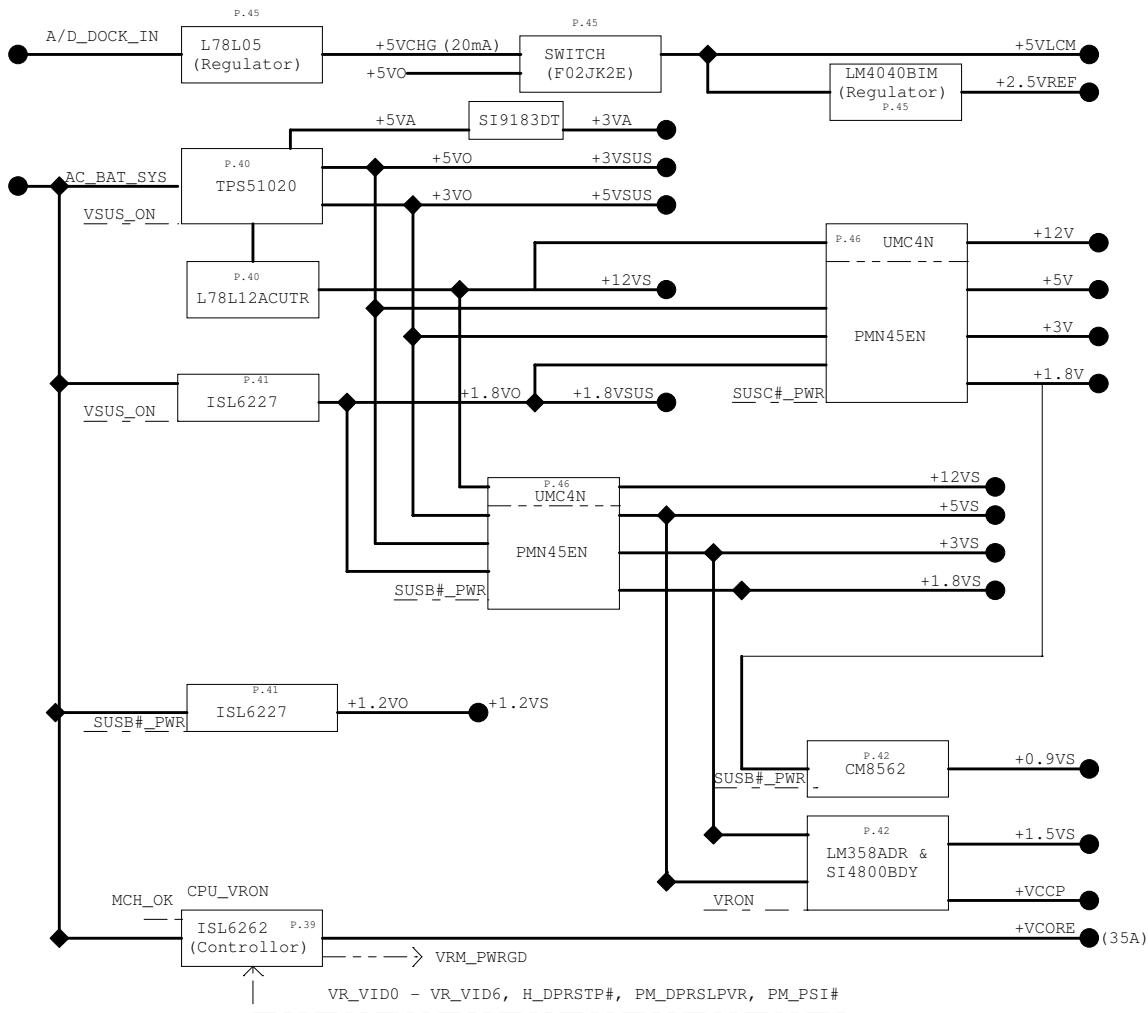
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ASUS		Title : POWER BLOCK DIAGRAM	
Engineer: Spring Li		Rev: 1.1	
Size: Custom	Project Name: Z94Rp	Date: 08/04/2016	
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