A8J/F SCHEMATIC R11

PAGE	Content
	SYSTEM PAGE REF.
4	YONAH CPU (1)
5	YONAH CPU (2)
6	CPU CAP/THERMAL SENSOR
7	CLOCK GEN.
8	Calistoga--CPU
9	Calistoga--PCIE
10	Calistoga--DDR2
11	Calistoga--POWER
12	Calistoga--GND
13	Calistoga--Strap
14	DDR2 SO-DIMM_0
15	DDR2 SO-DIMM_1
16	DDR2 ADDRESS TERMINATION
17	VGA CONN
18	LVDS & INVERTER CONN
19	CRT & TV_OUT
20	ICH7M--CPU,IDE,AUDIO
21	ICH7M--PCI,PCI-E,USB
22	ICH7M--GPIO
23	ICH7M--VCC,GND
24	HDD & CD-ROM CONN
25	USB PORTS
26	SUPER I/O LPC47N217
27	BIOS & FIR
28	KBC 38857
29	SM BUS & POWER PORT
30	PCI-E--GIGA_LAN RTL8111B
31	PCI-E--MINI CARD
32	PCI-E--NEW CARD
33	PCI--1394,CardReader R5C832
34	PCI--4 IN1 CON
35	PCI--Empty
36	AUDIO CODEC AD1986A
37	AUDIO AMP G1420
38	MDC,B/T,TPM & DISCHG,HOLE
39	DVI CONN
40	ACIN, BAT, FAN, I/O PORT
41	SW & LED & TP
42	POWER-ON SEQUENCE
43	HISTORY
44	I/O PORT

PAGE	Content
	POWER PAGE REF.
50	50_POWER_VCORE
51	51_POWER_SYSTEM
52	52_POWER_I/O_1.8V & 1.05VS
53	53_POWER_I/O_+1.5VS
54	54_POWER_I/O_VTT & +2.5VS
55	55_POWER_VGA_CORE(Empty)
56	56_POWER_VGA_RAM(Empty)
57	57_POWER_CHARGER
58	58_POWER_PIC
59	59_POWER_SELECTOR
60	60_POWER_PROTECT
61	61_POWER_LOAD SWITCH
62	62_POWER_FLOWCHART
63	63_POWER_SIGNAL

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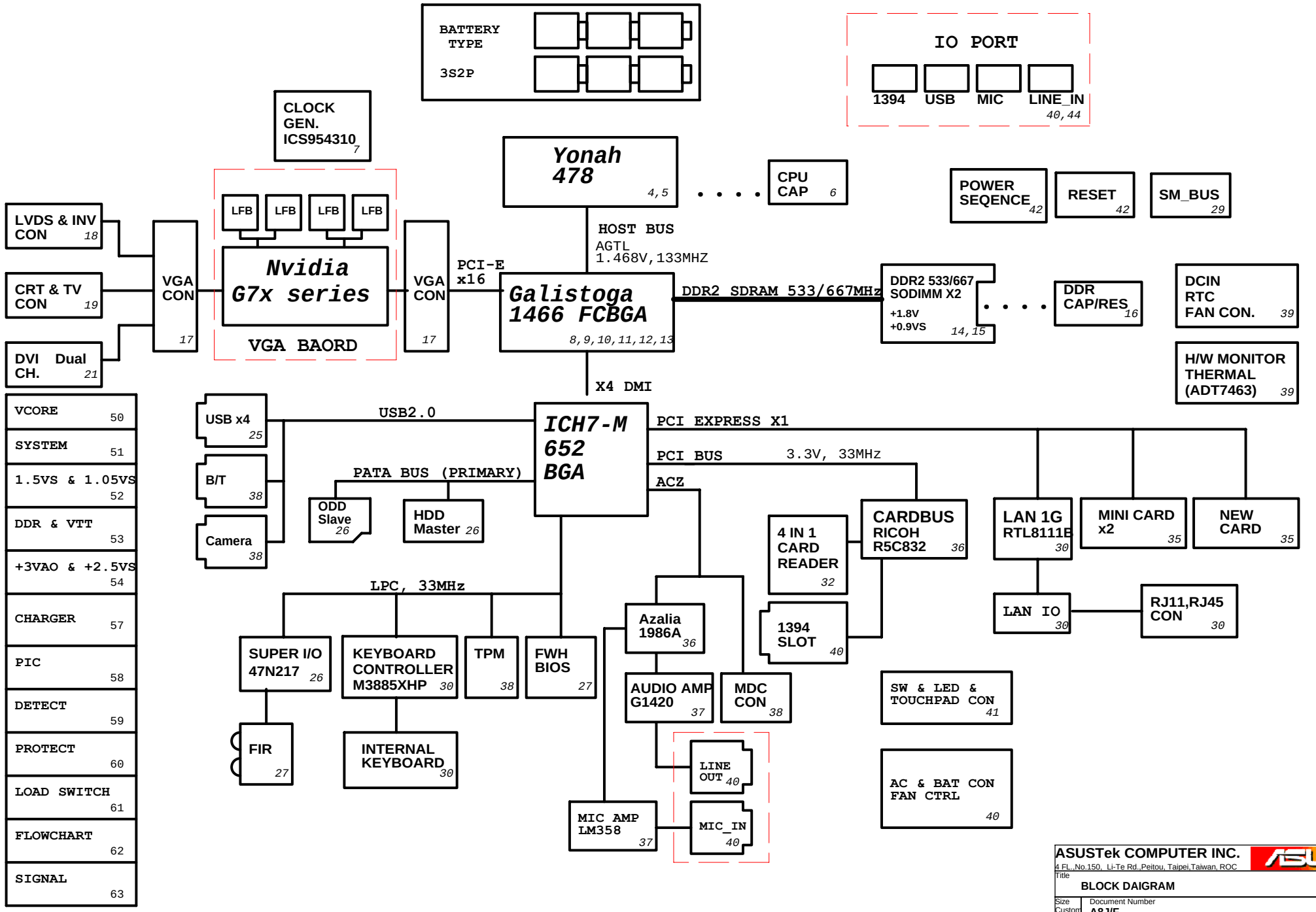
Title: PAGE REF.

Size: Custom | Document Number: A8J/F | Rev: 1.1

Date: Thursday, October 06, 2005 | Sheet 1 of 63

A8J/F Yonah/Galistoga BLOCK DIAGRAM



ASUSTek COMPUTER INC.	
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Title	BLOCK DAIGRAM
Size: Custom	Document Number: A8J/F
Rev	1.1
Date:	Thursday, October 06, 2005
Sheet	2 of 63

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Integrated LAN	AD24(NO USE)			
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
CLK GEN. = 1101001x (D2h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010010x (A4h)
VGA_Thermal IC = 1001100x (9Ah)

ICH7M_GPIO		Use As	Signal Name	Power
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BACK_OFF#	+3VS
GPIO 07	i	GPI	RF_SW_OFF#	+3VS
GPIO 08	i	GPI	EXTSMI#_3A	+3VSUS
GPIO 09	i	GPI	PD_DET#	+3VSUS
GPIO 10	i	GPI	CHG_FULL_OC	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KB_SCI#	+3VSUS
GPIO 13	i	GPI	SIO_SMI#	+3VSUS
GPIO 14	i	GPI	PD_UnDock#	+3VSUS
GPIO 15	i	GPO	802_LED_EN#	+3VSUS
GPIO 16	O	0 GPO	PM_DPRSLPVR	+3VS
GPIO 17	O	1 GPO	PCI_GNT#5	+3VS
GPIO 18	O	1 GPO	STP_PCI#	+3VS
GPIO 19	i	1 GPI	PD_RDY#	+3VS
GPIO 20	O	1 GPO	STP_CPU#	+3VS
GPIO 21	i	1 GPO	PD_SIO_RST#	+3VS
GPIO 22	i	1 Native	PCI_REQ#4	+3VS
GPIO 23	i	1 Native	LPC_DRQ#1	+3VS
GPIO 24	O	0 GPO	PD_EN#	+3VSUS
GPIO 25	O	1 GPO	CB_SD#	+3VSUS
GPIO 26	O	0 GPO	OP_SD#	+3VSUS
GPIO 27	O	0 GPO	WLAN_ON#	+3VSUS
GPIO 28	O	0 GPO	1Hz	+3VSUS
GPIO 29	i	0 Native	USB_OC#5	+3VSUS
GPIO 30	i	0 Native	USB_OC#6	+3VSUS
GPIO 31	i	0 Native	USB_OC#7	+3VSUS
GPIO 32	O	1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O	1 GPO	BT_ON/OFF#	+3VS
GPIO 34	O	0 GPO	FWH_WP#	+3VS
GPIO 35	O	0 GPO	SATACLKREQ#	+3VS
GPIO 36	i	0 GPO	BT_LED_EN#	+3VS
GPIO 37	i	0 GPI	PCB_ID0	+3VS
GPIO 38	i	0 GPI	PCB_ID1	+3VS
GPIO 39	i	0 GPI	PCB_ID2	+3VS
GPIO [40:47]		NA	NA	NA
GPIO 48		Native	PCI_GNT#4	+3VS
GPIO 49		Native	H_PWRGD	+VCORE

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI		+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI		+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI	NONE	+3VS
GPIO11	GPO	NONE	+3VS
GPIO12	GPO	NONE	+3VS
GPIO13	GPI	NONE	+3VS
GPIO14	GPI	NONE	+3VS
GPIO23	GPO	ATI_RST#	+3VS
GPIO40	GPI		+3VS
GPIO41	GPI		+3VS
GPIO40	GPI		+3VS
GPIO43	GPI		+3VS
GPIO44	GPI		+3VS
GPIO45	GPI		+3VS
GPIO46	GPI	VGA_DETEC#	+3VS
GPIO47	GPI		+3VS

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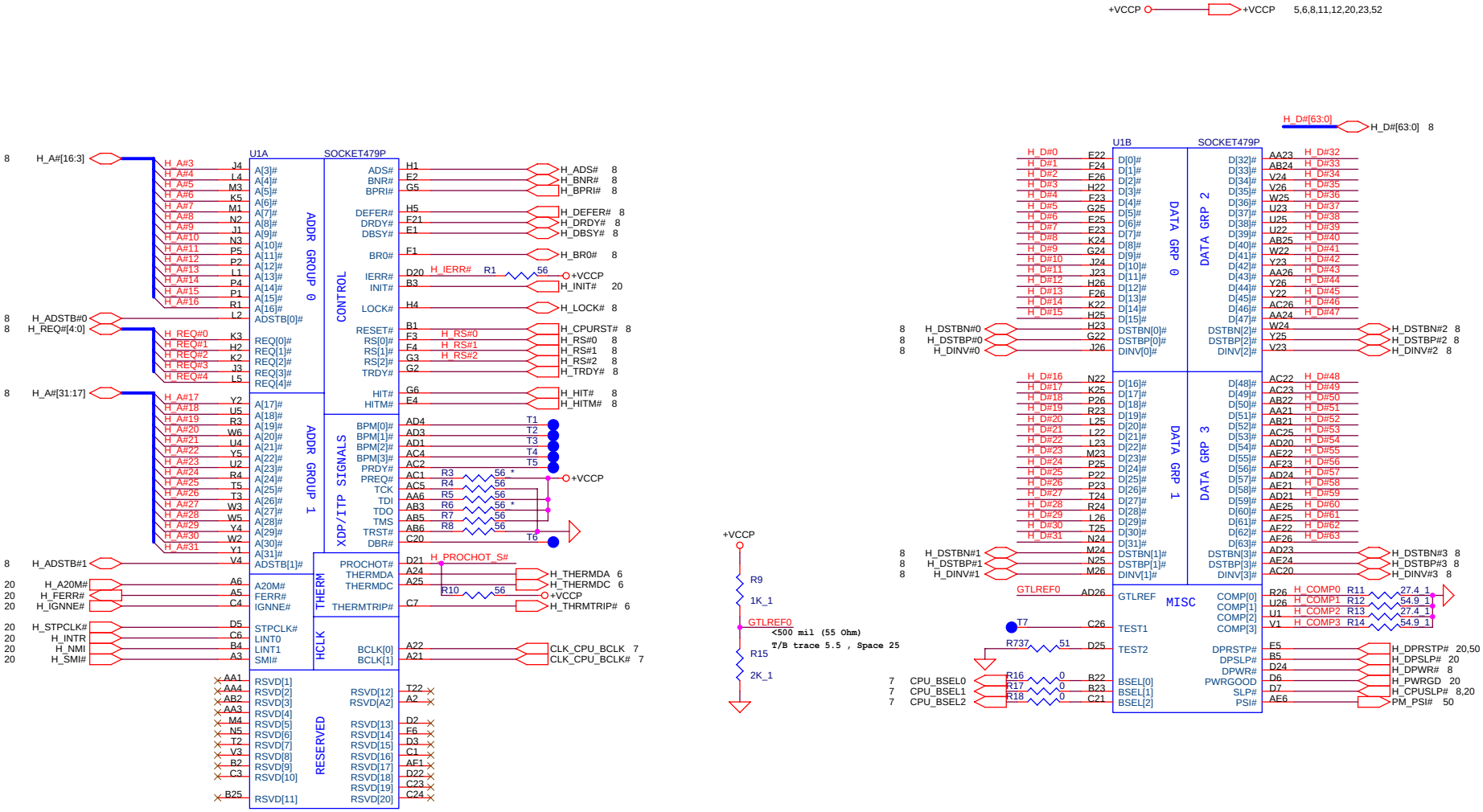
Title: SCHEMATICS REF.

Size: Custom | Document Number: A8J/F | Rev: 1.1

Date: Thursday, October 06, 2005 | Sheet 3 of 63



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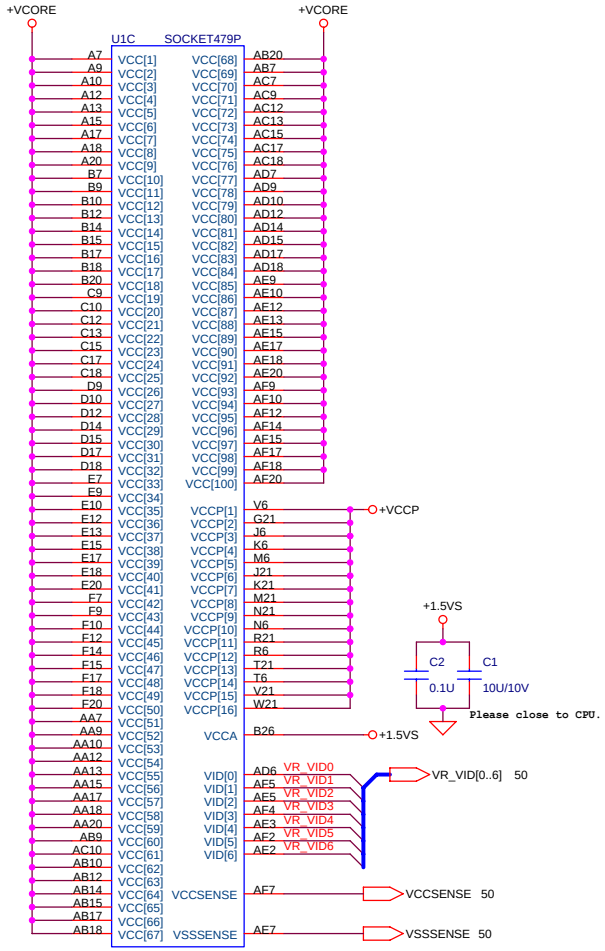
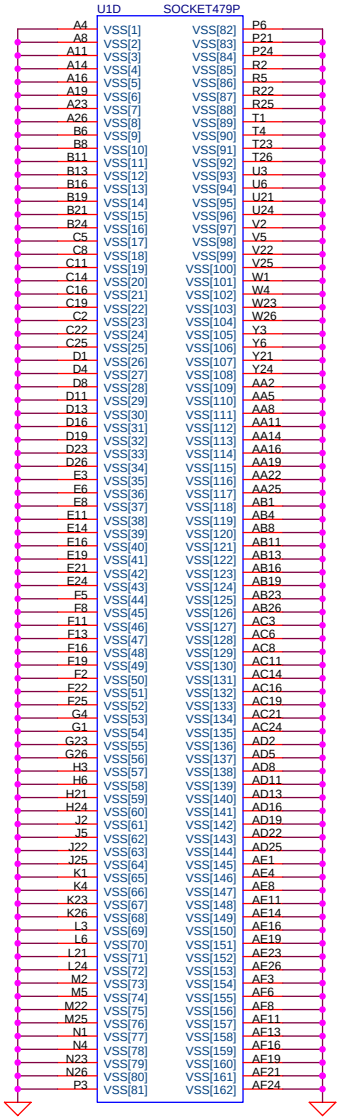
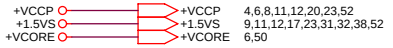
Title: **YONAH CPU1**

Size	Document Number	Rev
Custom	**A8J/F**	1.1

Date: Thursday, October 06, 2005 Sheet 4 of 63







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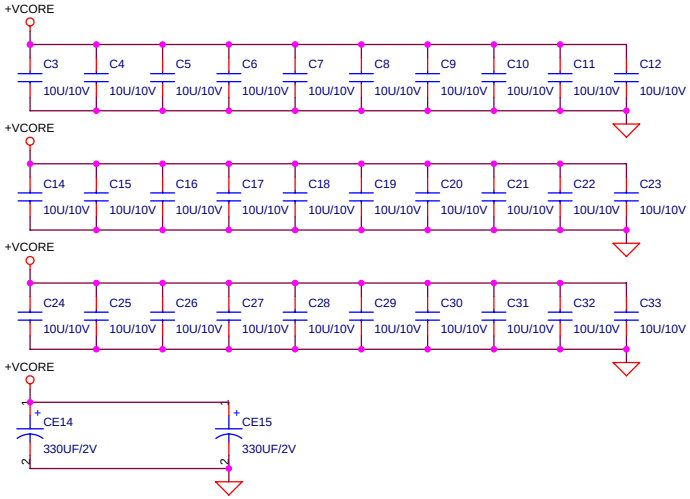
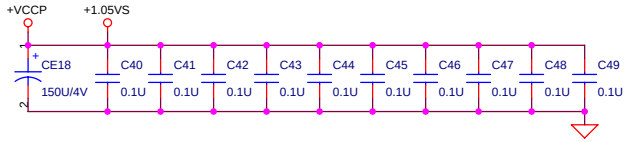
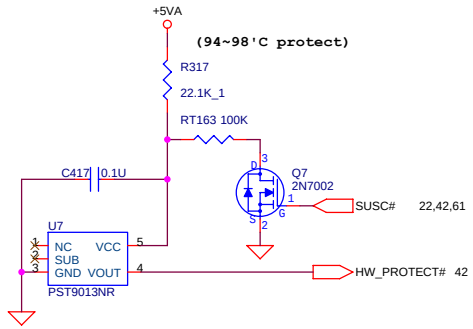
Title: **YONAH CPU2**

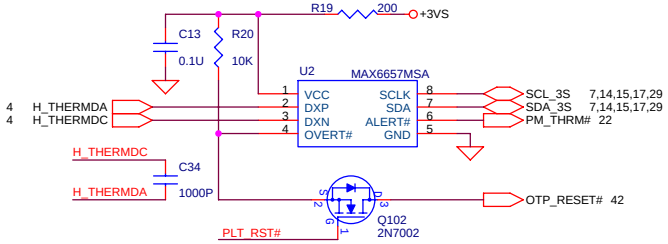
Size	Document Number	Rev
Custom	**A8J/F**	1.1

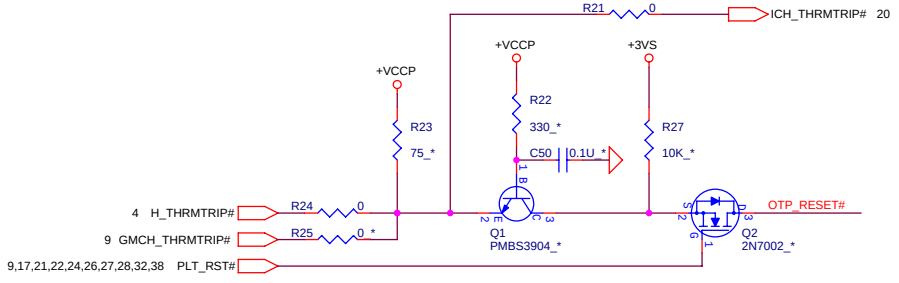
Date: Thursday, October 06, 2005 Sheet 5 of 63











+VCCP	+VCCP	4,5,8,11,12,20,23,52
+VCORE	+VCORE	5,50
+3VS	+3VS	7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,38,41,50,52,60,61
+5VA	+5VA	51,54,57

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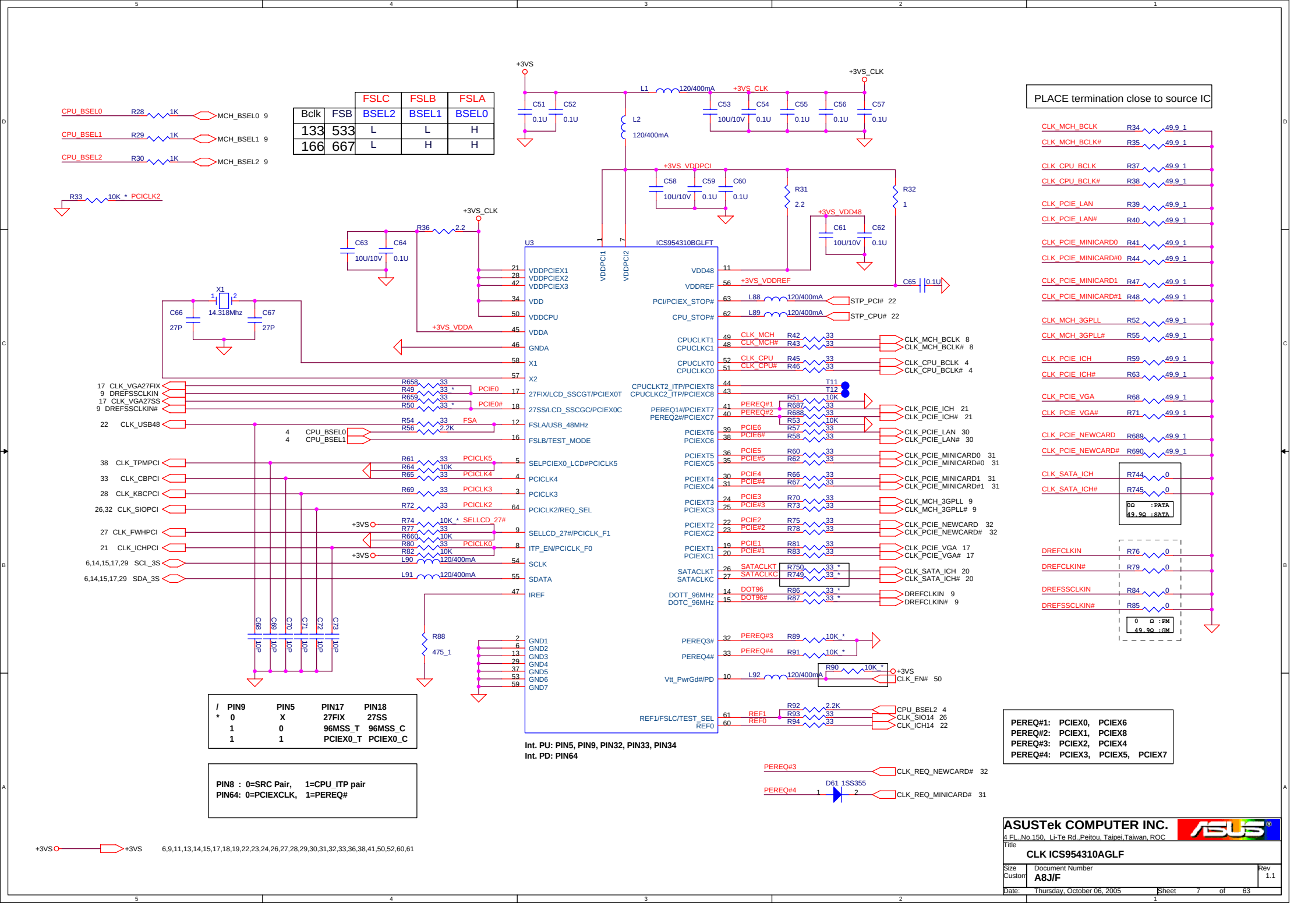
Title: **CPU CAP,THERMAL SENSOR**

Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 6 of 63


CPU_BSEL0 R28 1K MCH_BSEL0 9
CPU_BSEL1 R29 1K MCH_BSEL1 9
CPU_BSEL2 R30 1K MCH_BSEL2 9
R33 10K * PCICLK2
Bclk FSB FSLC BSEL2 FSLB BSEL1 FSLA BSEL0
133 533 L L H
166 667 L H H
PLACE termination close to source IC
U3 ICS954310BGLFT
+3VS +3VS_CLK +3VS_VDDPCI +3VS_VDD48 +3VS_VDDREF +3VS_VDDA
L1 120/400mA L2 120/400mA
C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65
R31 2.2 R32 1 R36 2.2
X1 14.318Mhz C66 27P C67 27P
VDDPCIEX1 VDDPCIEX2 VDDPCIEX3 VDD VDDCPU VDDA GNDA X1 X2
27FIX/LCD_SSCGT/PCIEX0T 27SS/LCD_SSCGC/PCIEX0C FSLA/USB_48MHz FSLB/TEST_MODE
SELPCIEX0_LCD#PCICLK5 PCICLK4 PCICLK3 PCICLK2/REQ_SEL SELLCD_27#/PCICLK_F1 ITP_EN/PCICLK_F0 SCLK SDATA IREF
GND1 GND2 GND3 GND4 GND5 GND6 GND7
VDD48 VDDREF PCI/PCIEX_STOP# CPU_STOP#
CPUCLKT1 CPUCLKC1 CPUCLKT0 CPUCLKC0 CPUCLKT2_ITP/PCIEXT8 CPUCLKC2_ITP/PCIEXC8
PEREQ1#/PCIEXT7 PEREQ2#/PCIEXC7 PCIEXT6 PCIEXC6 PCIEXT5 PCIEXC5 PCIEXT4 PCIEXC4 PCIEXT3 PCIEXC3 PCIEXT2 PCIEXC2 PCIEXT1 PCIEXC1
SATACLKT SATACLKC DOTT_96MHz DOTC_96MHz PEREQ3# PEREQ4# Vtt_PwrGd#/PD REF1/FSLC/TEST_SEL REF0
CLK_MCH_BCLK CLK_MCH_BCLK# CLK_CPU_BCLK CLK_CPU_BCLK# CLK_PCIE_LAN CLK_PCIE_LAN# CLK_PCIE_MINICARD0 CLK_PCIE_MINICARD#0 CLK_PCIE_MINICARD1 CLK_PCIE_MINICARD#1 CLK_MCH_3GPLL CLK_MCH_3GPLL# CLK_PCIE_ICH CLK_PCIE_ICH# CLK_PCIE_VGA CLK_PCIE_VGA# CLK_PCIE_NEWCARD CLK_PCIE_NEWCARD# CLK_SATA_ICH CLK_SATA_ICH# DREFCLKIN DREFCLKIN# DREFSSCLKIN DREFSSCLKIN#
STP_PCI# 22 STP_CPU# 22
CLK_USB48 22 CLK_TPMPCI 38 CLK_CBPCI 33 CLK_KBCPCI 28 CLK_SIOPCI 26,32 CLK_FWHPCI 27 CLK_ICHPCI 21 SCL_3S 6,14,15,17,29 SDA_3S 6,14,15,17,29
CLK_VGA27FIX 17 DREFSSCLKIN 9 CLK_VGA27SS 17 DREFSSCLKIN# 9
CPU_BSEL0 4 CPU_BSEL1 4
PCIE0 PCIE0# FSA
PCICLK5 PCICLK4 PCICLK3 PCICLK2 SELLCD_27# PCICLK0
R658 R49 R659 R50 R54 R56 R61 R64 R65 R69 R72 R74 R77 R660 R80 R82 L90 L91 R88 475_1
C68 C69 C70 C71 C72 C73 10P
PEREQ#1 PEREQ#2 PCIE6 PCIE6# PCIE5 PCIE5# PCIE4 PCIE4# PCIE3 PCIE3# PCIE2 PCIE2# PCIE1 PCIE1# SATACLKT SATACLKC DOT96 DOT96#
R687 R688 R53 R57 R58 R60 R62 R66 R67 R70 R73 R75 R78 R81 R83 R750 R749 R86 R87 R89 R91 R90 L92 R92 R93 R94
REF1 REF0
CLK_MCH CLK_MCH# CLK_CPU CLK_CPU#
R42 R43 R45 R46
CLK_MCH_BCLK 8 CLK_MCH_BCLK# 8 CLK_CPU_BCLK 4 CLK_CPU_BCLK# 4
CLK_PCIE_ICH 21 CLK_PCIE_ICH# 21 CLK_PCIE_LAN 30 CLK_PCIE_LAN# 30 CLK_PCIE_MINICARD0 31 CLK_PCIE_MINICARD#0 31 CLK_PCIE_MINICARD1 31 CLK_PCIE_MINICARD#1 31 CLK_MCH_3GPLL 9 CLK_MCH_3GPLL# 9 CLK_PCIE_NEWCARD 32 CLK_PCIE_NEWCARD# 32 CLK_PCIE_VGA 17 CLK_PCIE_VGA# 17 CLK_SATA_ICH 20 CLK_SATA_ICH# 20 DREFCLKIN 9 DREFCLKIN# 9
CLK_EN# 50
CPU_BSEL2 4 CLK_SIO14 26 CLK_ICH14 22
R744 R745 0Ω :PATA 49.9Ω :SATA
R76 R79 R84 R85 0Ω :PM 49.9Ω :GM
PEREQ#3 PEREQ#4 D61 1SS355 CLK_REQ_NEWCARD# 32 CLK_REQ_MINICARD# 31
PEREQ#1: PCIEX0, PCIEX6
PEREQ#2: PCIEX1, PCIEX8
PEREQ#3: PCIEX2, PCIEX4
PEREQ#4: PCIEX3, PCIEX5, PCIEX7
/ * PIN9 0 1 1 PIN5 X 0 1 PIN17 27FIX 96MSS_T PCIEX0_T PIN18 27SS 96MSS_C PCIEX0_C
PIN8 : 0=SRC Pair, 1=CPU_ITP pair
PIN64: 0=PCIEXCLK, 1=PEREQ#
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
Int. PD: PIN64
+3VS +3VS 6,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,38,41,50,52,60,61
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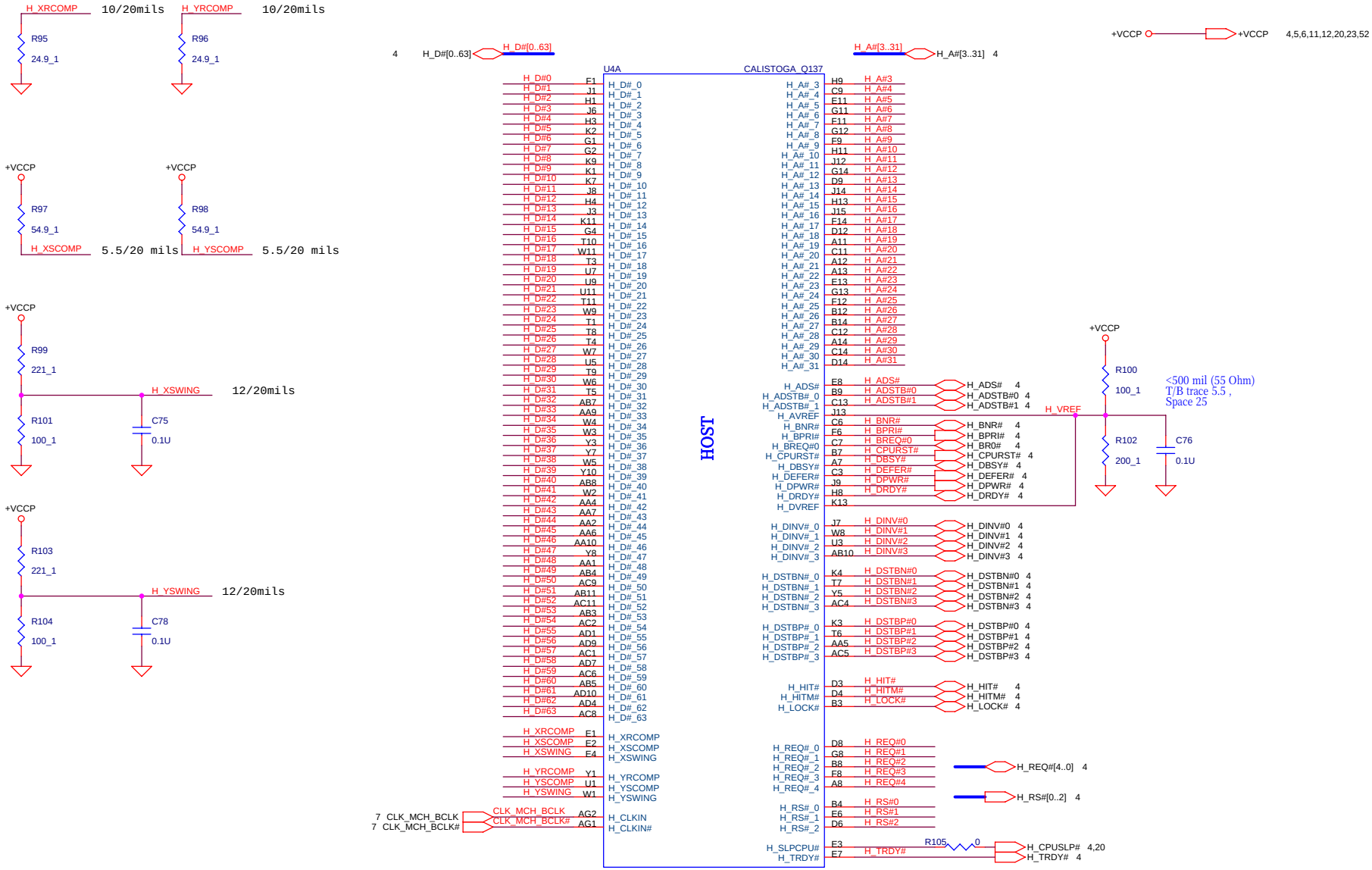
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
CLK ICS954310AGLF
Size Custom
Document Number A8J/F
Rev 1.1
Date: Thursday, October 06, 2005
Sheet 7 of 63



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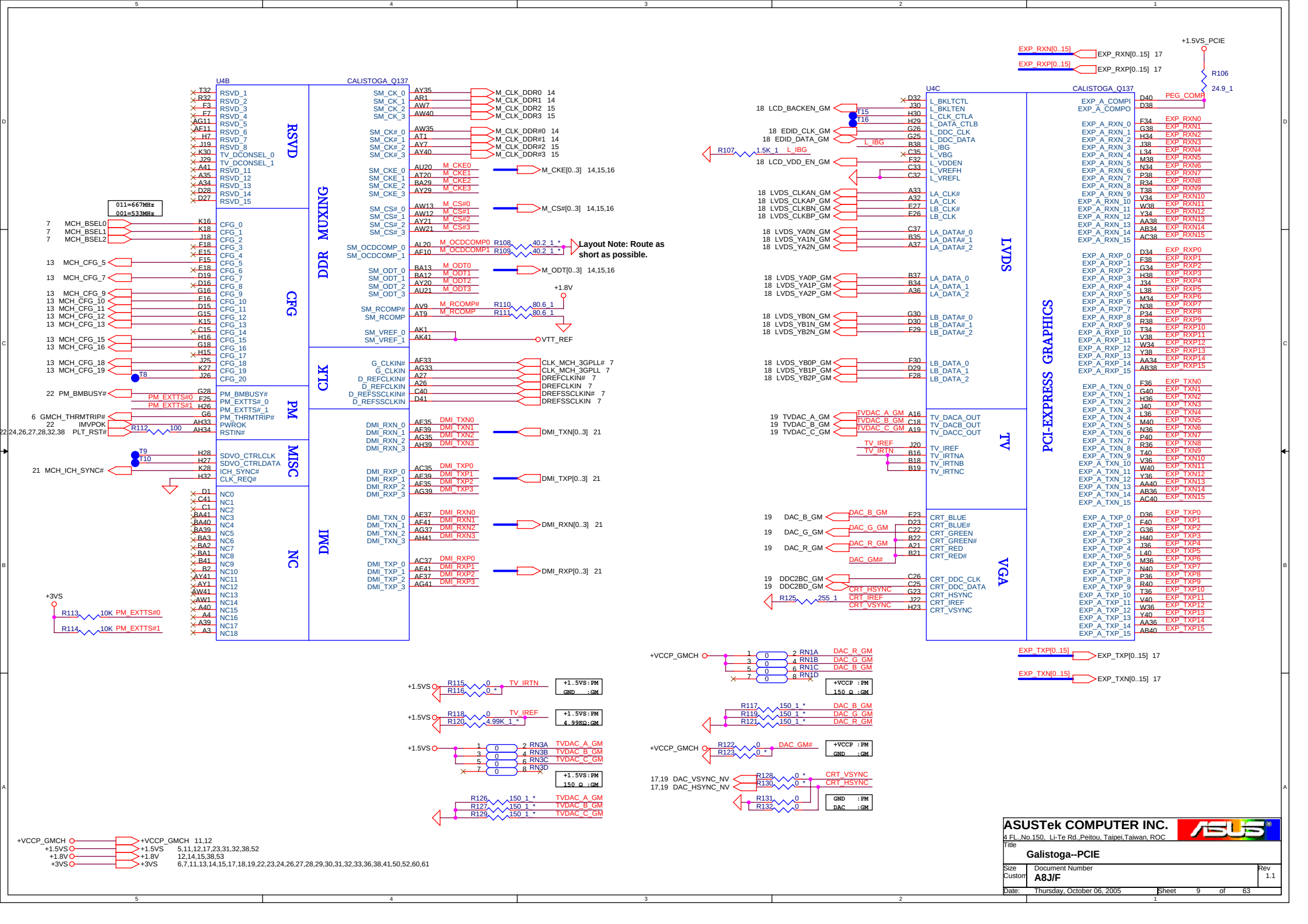
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: Galistoga--CPU		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 8 of 63	


U4B
CALISTOGA_Q137
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
U4C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
Layout Note: Route as short as possible.
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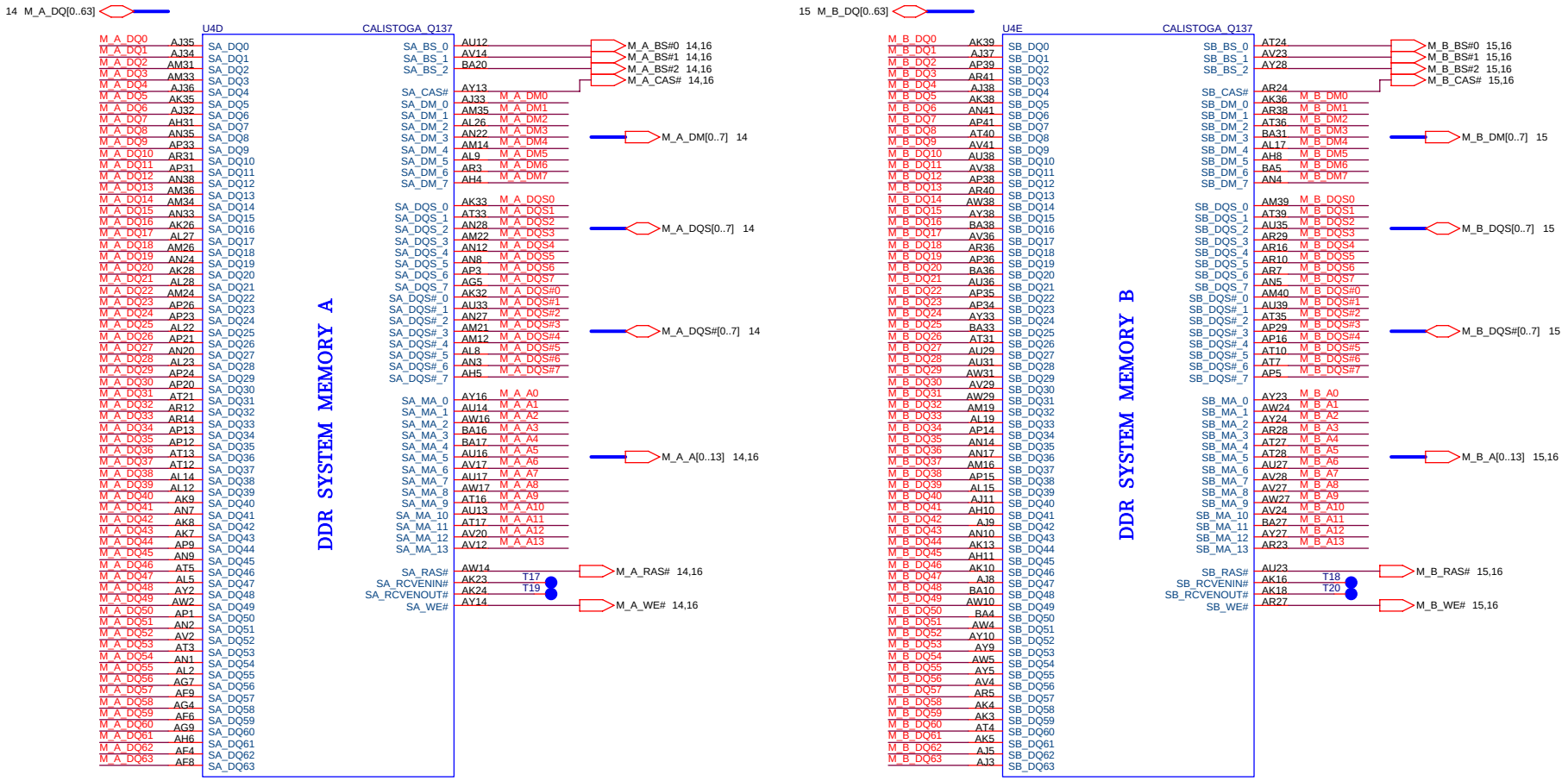
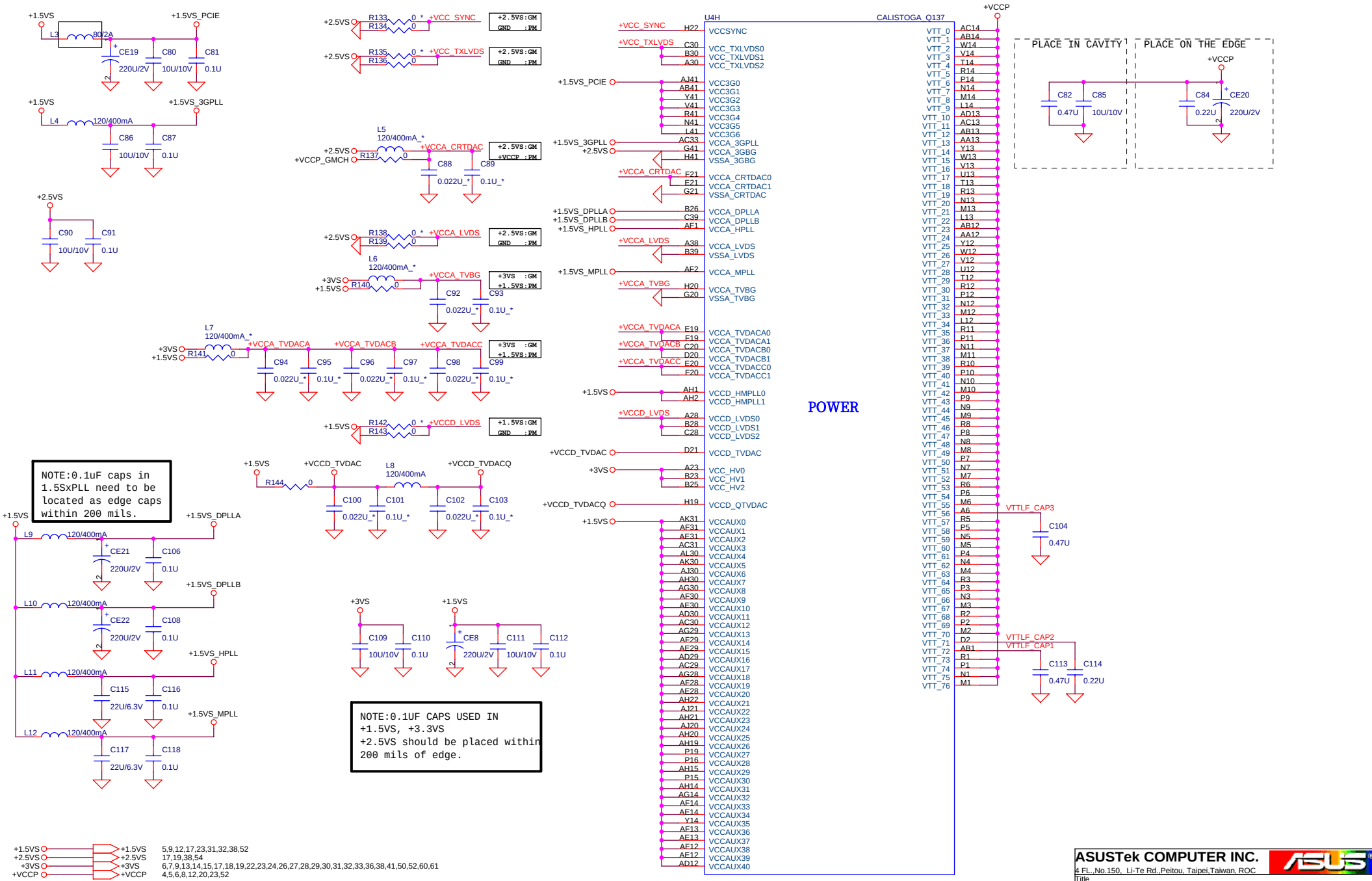
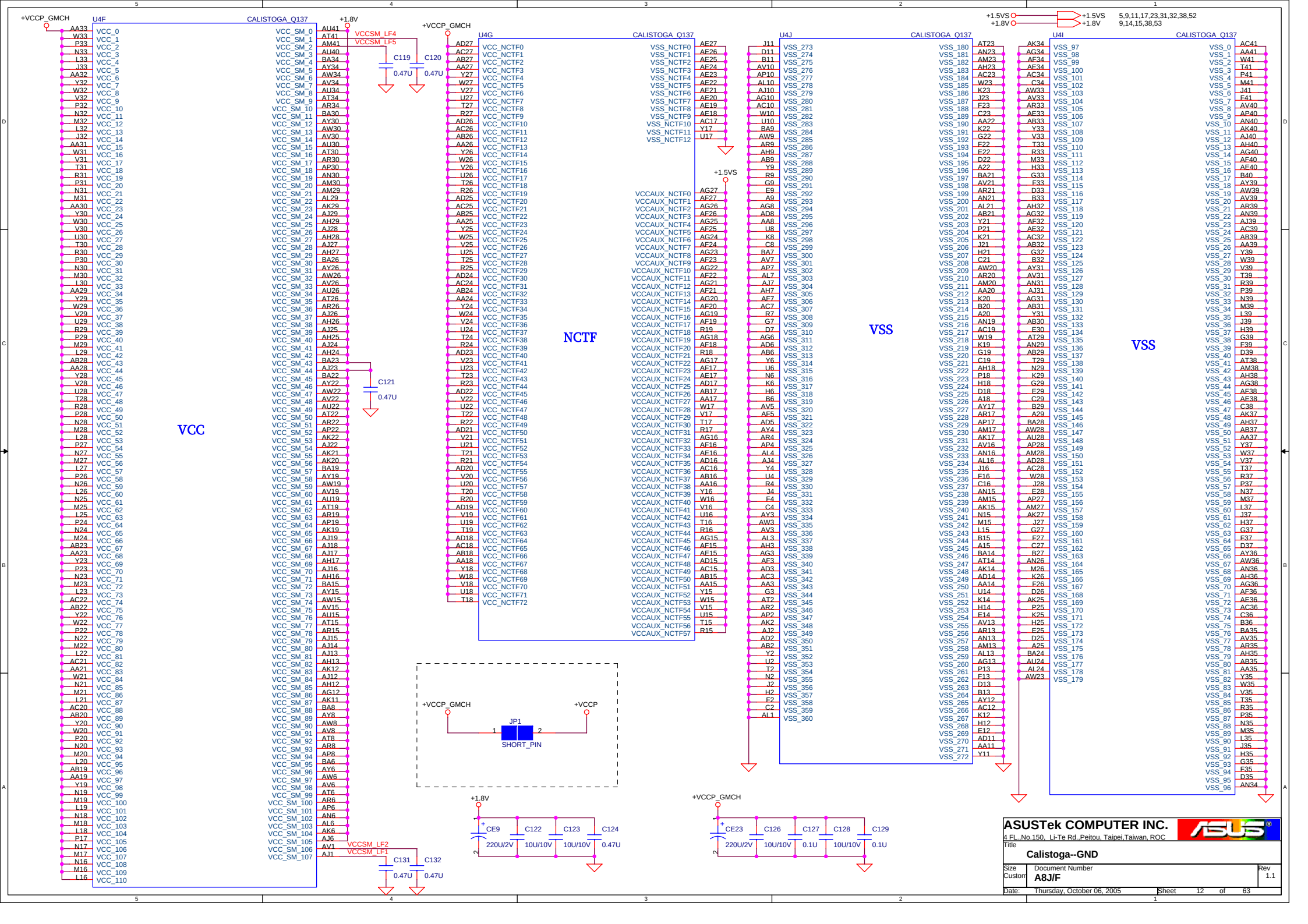
Title
Galistoga--PCIE
Size
Custom
Document Number
A8J/F
Rev
1.1
Date:
Thursday, October 06, 2005
Sheet
9
of
63

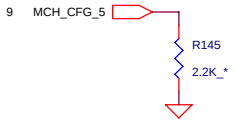


ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: Calistoga--DDR2		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 10 of 63	


+1.5VS
+1.5VS_PCIE
L3 80/2A
CE19 220U/2V
C80 10U/10V
C81 0.1U
+1.5VS
+1.5VS_3GPLL
L4 120/400mA
C86 10U/10V
C87 0.1U
+2.5VS
C90 10U/10V
C91 0.1U
+2.5VS
R133 0 *
R134 0
+VCC_SYNC
+2.5VS:GM
GND :PM
+2.5VS
R135 0 *
R136 0
+VCC_TXLVDS
+2.5VS:GM
GND :PM
L5 120/400mA_*
+2.5VS
+VCCP_GMCH
R137 0
+VCCA_CRTDAC
+2.5VS:GM
+VCCP :PM
C88 0.022U_*
C89 0.1U_*
+2.5VS
R138 0 *
R139 0
+VCCA_LVDS
+2.5VS:GM
GND :PM
L6 120/400mA_*
+3VS
+1.5VS
R140 0
+VCCA_TVBG
+3VS :GM
+1.5VS:PM
C92 0.022U_*
C93 0.1U_*
L7 120/400mA_*
+3VS
+1.5VS
R141 0
+VCCA_TVDACA
+VCCA_TVDACB
+VCCA_TVDACC
+3VS :GM
+1.5VS:PM
C94 0.022U_*
C95 0.1U_*
C96 0.022U_*
C97 0.1U_*
C98 0.022U_*
C99 0.1U_*
+1.5VS
R142 0 *
R143 0
+VCCD_LVDS
+1.5VS:GM
GND :PM
NOTE:0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.
+1.5VS
+VCCD_TVDAC
R144 0
L8 120/400mA
+VCCD_TVDACQ
C100 0.022U_*
C101 0.1U_*
C102 0.022U_*
C103 0.1U_*
+1.5VS
+1.5VS_DPLLA
L9 120/400mA
CE21 220U/2V
C106 0.1U
+1.5VS_DPLLB
L10 120/400mA
CE22 220U/2V
C108 0.1U
+1.5VS_HPLL
L11 120/400mA
C115 22U/6.3V
C116 0.1U
+1.5VS_MPLL
L12 120/400mA
C117 22U/6.3V
C118 0.1U
+3VS
C109 10U/10V
C110 0.1U
+1.5VS
CE8 220U/2V
C111 10U/10V
C112 0.1U
NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.
U4H
CALISTOGA_Q137
POWER
+VCC_SYNC H22 VCCSYNC
+VCC_TXLVDS C30 VCC_TXLVDS0
B30 VCC_TXLVDS1
A30 VCC_TXLVDS2
+1.5VS_PCIE AJ41 VCC3G0
AB41 VCC3G1
Y41 VCC3G2
V41 VCC3G3
R41 VCC3G4
N41 VCC3G5
L41 VCC3G6
+1.5VS_3GPLL AC33 VCCA_3GPLL
+2.5VS G41 VCCA_3GBG
H41 VSSA_3GBG
+VCCA_CRTDAC F21 VCCA_CRTDAC0
E21 VCCA_CRTDAC1
G21 VSSA_CRTDAC
+1.5VS_DPLLA B26 VCCA_DPLLA
+1.5VS_DPLLB C39 VCCA_DPLLB
+1.5VS_HPLL AF1 VCCA_HPLL
+VCCA_LVDS A38 VCCA_LVDS
B39 VSSA_LVDS
+1.5VS_MPLL AF2 VCCA_MPLL
+VCCA_TVBG H20 VCCA_TVBG
G20 VSSA_TVBG
+VCCA_TVDACA E19 VCCA_TVDACA0
F19 VCCA_TVDACA1
+VCCA_TVDACB C20 VCCA_TVDACB0
D20 VCCA_TVDACB1
+VCCA_TVDACC E20 VCCA_TVDACC0
F20 VCCA_TVDACC1
+1.5VS AH1 VCCD_HMPLL0
AH2 VCCD_HMPLL1
+VCCD_LVDS A28 VCCD_LVDS0
B28 VCCD_LVDS1
C28 VCCD_LVDS2
+VCCD_TVDAC D21 VCCD_TVDAC
+3VS A23 VCC_HV0
B23 VCC_HV1
B25 VCC_HV2
+VCCD_TVDACQ H19 VCCD_QTVDAC
+1.5VS AK31 VCCAUX0
AF31 VCCAUX1
AE31 VCCAUX2
AC31 VCCAUX3
AL30 VCCAUX4
AK30 VCCAUX5
AJ30 VCCAUX6
AH30 VCCAUX7
AG30 VCCAUX8
AF30 VCCAUX9
AE30 VCCAUX10
AD30 VCCAUX11
AC30 VCCAUX12
AG29 VCCAUX13
AF29 VCCAUX14
AE29 VCCAUX15
AD29 VCCAUX16
AC29 VCCAUX17
AG28 VCCAUX18
AF28 VCCAUX19
AE28 VCCAUX20
AH22 VCCAUX21
AJ21 VCCAUX22
AH21 VCCAUX23
AJ20 VCCAUX24
AH20 VCCAUX25
AH19 VCCAUX26
P19 VCCAUX27
P16 VCCAUX28
AH15 VCCAUX29
P15 VCCAUX30
AH14 VCCAUX31
AG14 VCCAUX32
AF14 VCCAUX33
AE14 VCCAUX34
Y14 VCCAUX35
AF13 VCCAUX36
AE13 VCCAUX37
AF12 VCCAUX38
AE12 VCCAUX39
AD12 VCCAUX40
+VCCP
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 Y14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1
VTTLF_CAP3
C104 0.47U
VTTLF_CAP2
VTTLF_CAP1
C113 0.47U
C114 0.22U
PLACE IN CAVITY
C82 0.47U
C85 10U/10V
PLACE ON THE EDGE
+VCCP
C84 0.22U
CE20 220U/2V
+1.5VS +1.5VS 5,9,12,17,23,31,32,38,52
+2.5VS +2.5VS 17,19,38,54
+3VS +3VS 6,7,9,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,38,41,50,52,60,61
+VCCP +VCCP 4,5,6,8,12,20,23,52
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
Calistoga--PWR
Size Custom
Document Number A8J/F
Rev 1.1
Date: Thursday, October 06, 2005
Sheet 11 of 63

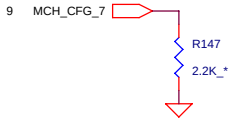

+VCCP_GMCH
U4F
CALISTOGA_Q137
VCC
+1.8V
VCCSM_LF4
VCCSM_LF5
C119
C120
0.47U
C121
VCCSM_LF2
VCCSM_LF1
C131
C132
U4G
NCTF
U4J
VSS
+1.5VS
+1.8V
U4I
JP1
SHORT_PIN
+VCCP
CE9
C122
C123
C124
220U/2V
10U/10V
CE23
C126
C127
C128
C129
0.1U
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Calistoga--GND
A8J/F
Thursday, October 06, 2005
Sheet 12 of 63

+3VS +3VS 6,7,9,11,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,38,41,50,52,60,61



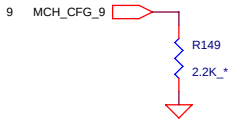
CFG5 : DMI STRAP

LOW = DMI X 2
HIGH = DMI X 4 (Default)



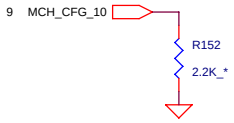
CFG7 : CPU STRAP

LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



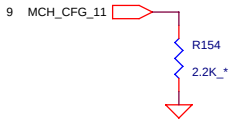
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



CFG10 : HOST PLL VCO SELECT

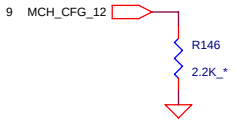
LOW = RESERVED
HIGH = MOBILITY (Default)



CFG11 : PSB 4x CLK ENABLE

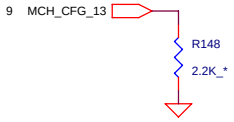
LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)

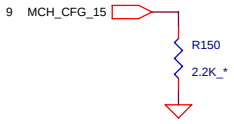
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.



CFG[13:12] : GMCH TEST MODE SELECT

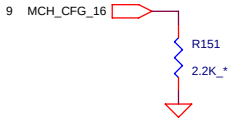
00 = Partial CLK gating disable
01 = XOR Mode Enable
10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)





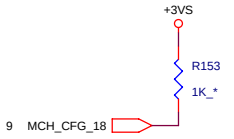
CFG15 : ICH RESET Disable

LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



CFG16 : FSB Dynamic ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)
HIGH = 1.5V

CFG19 : DMI LANE REVERSAL

LOW = NORMAL (Default)
HIGH = LANES REVERSED

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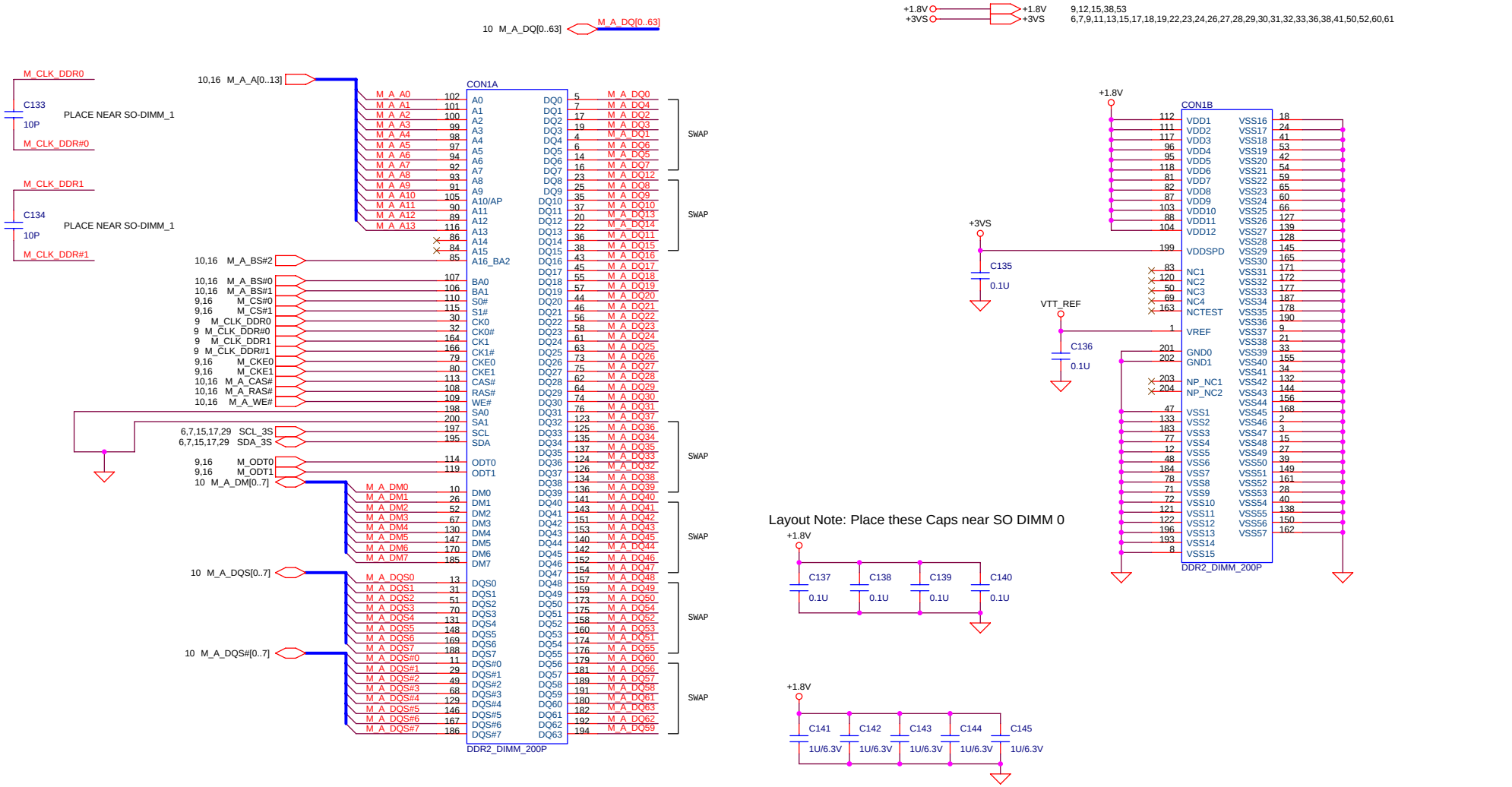
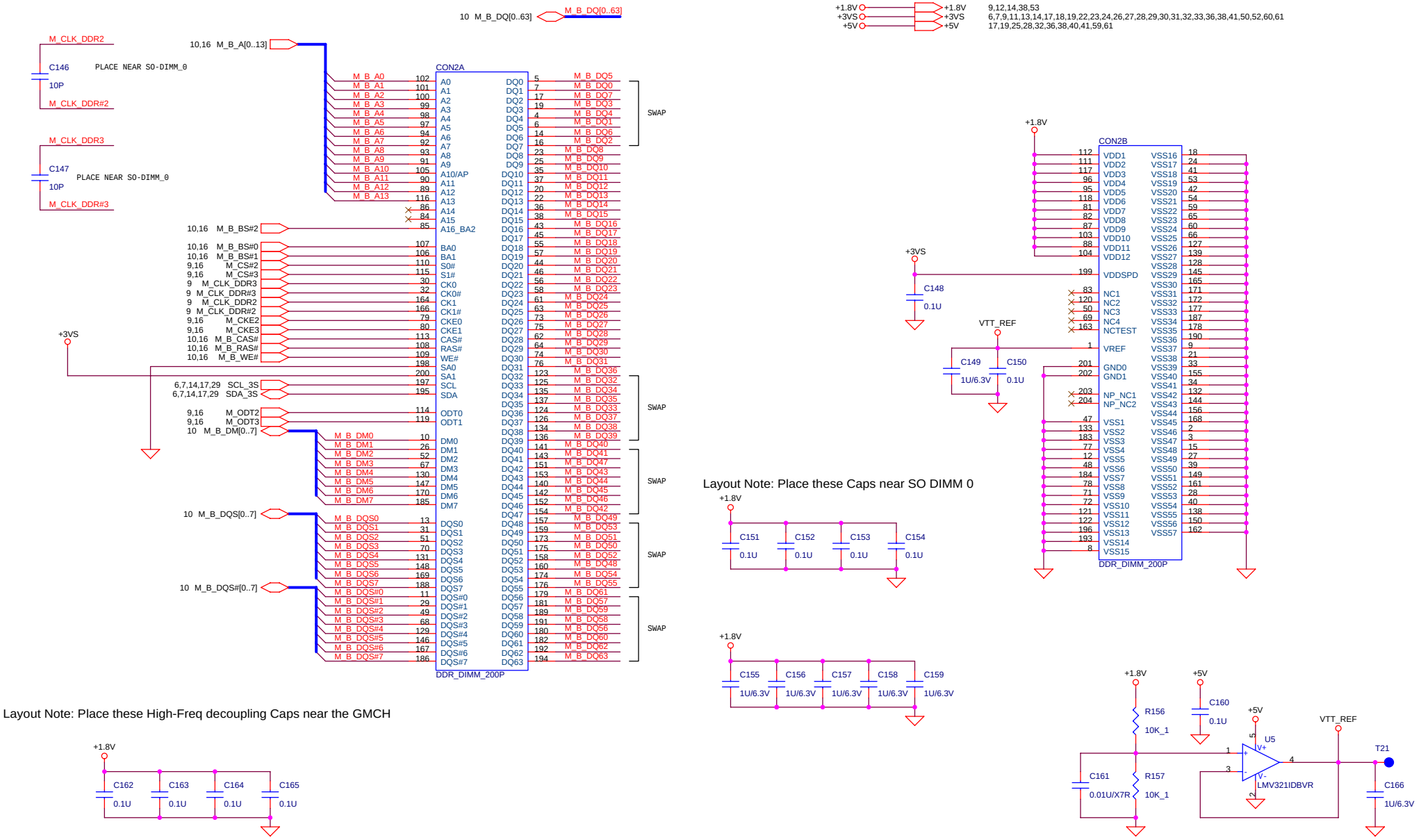
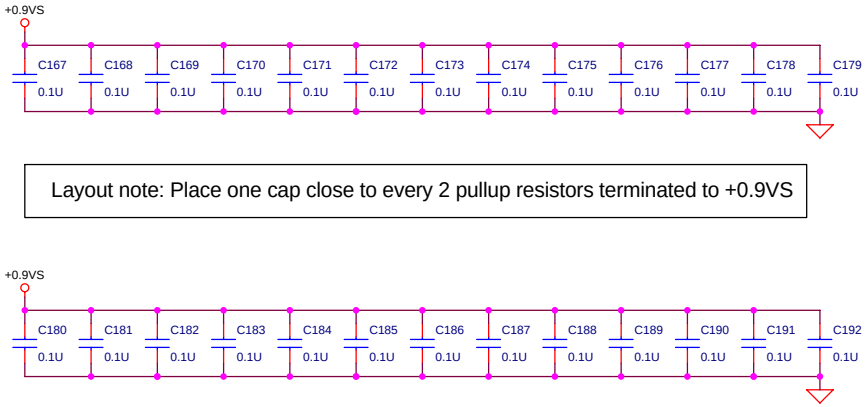
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: Galistoga--straps		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 13 of 63	



ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: **DDR2 SO-DIMM0**		
Size: Custom	Document Number: **A8J/F**	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 14 of 63	

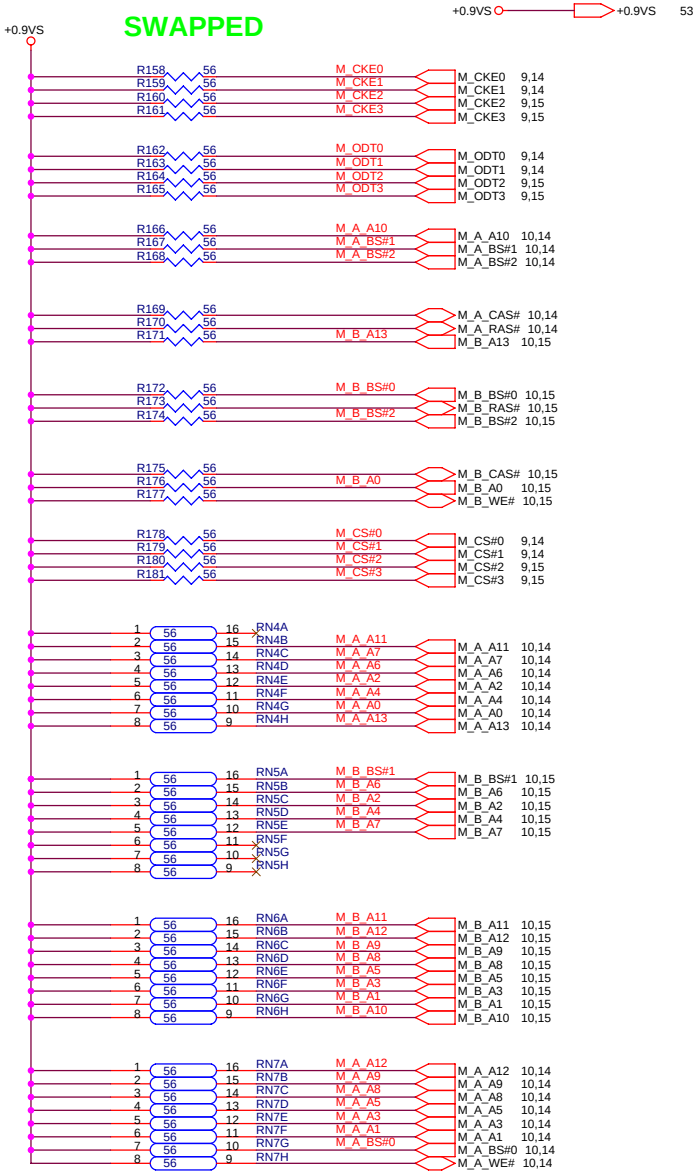


ASUSTek COMPUTER INC.	
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title	**DDR2 SO-DIMM1**
Size: Custom	Document Number: **A8J/F**
Rev	1.1
Date: Thursday, October 06, 2005	Sheet 15 of 63



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

SWAPPED

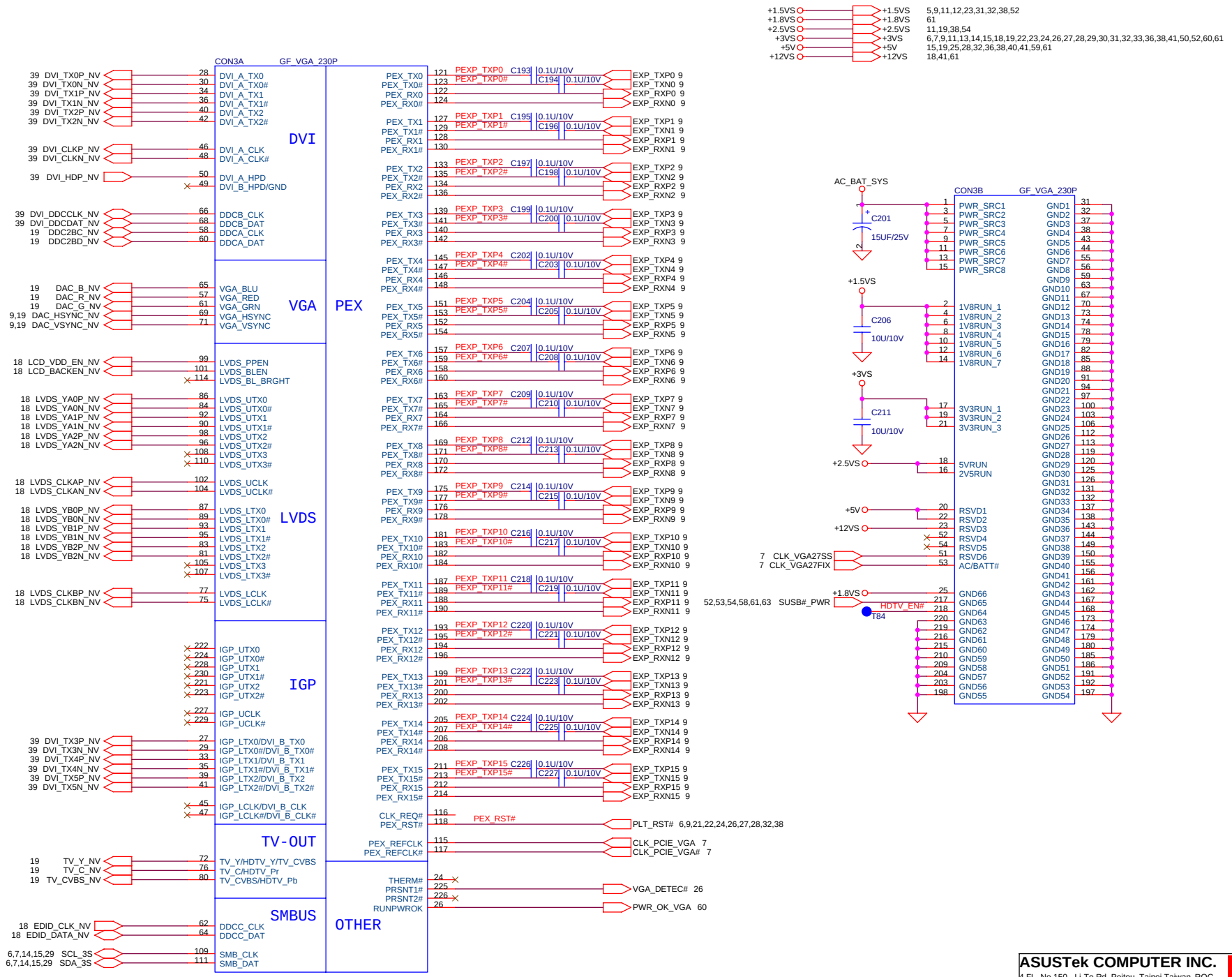


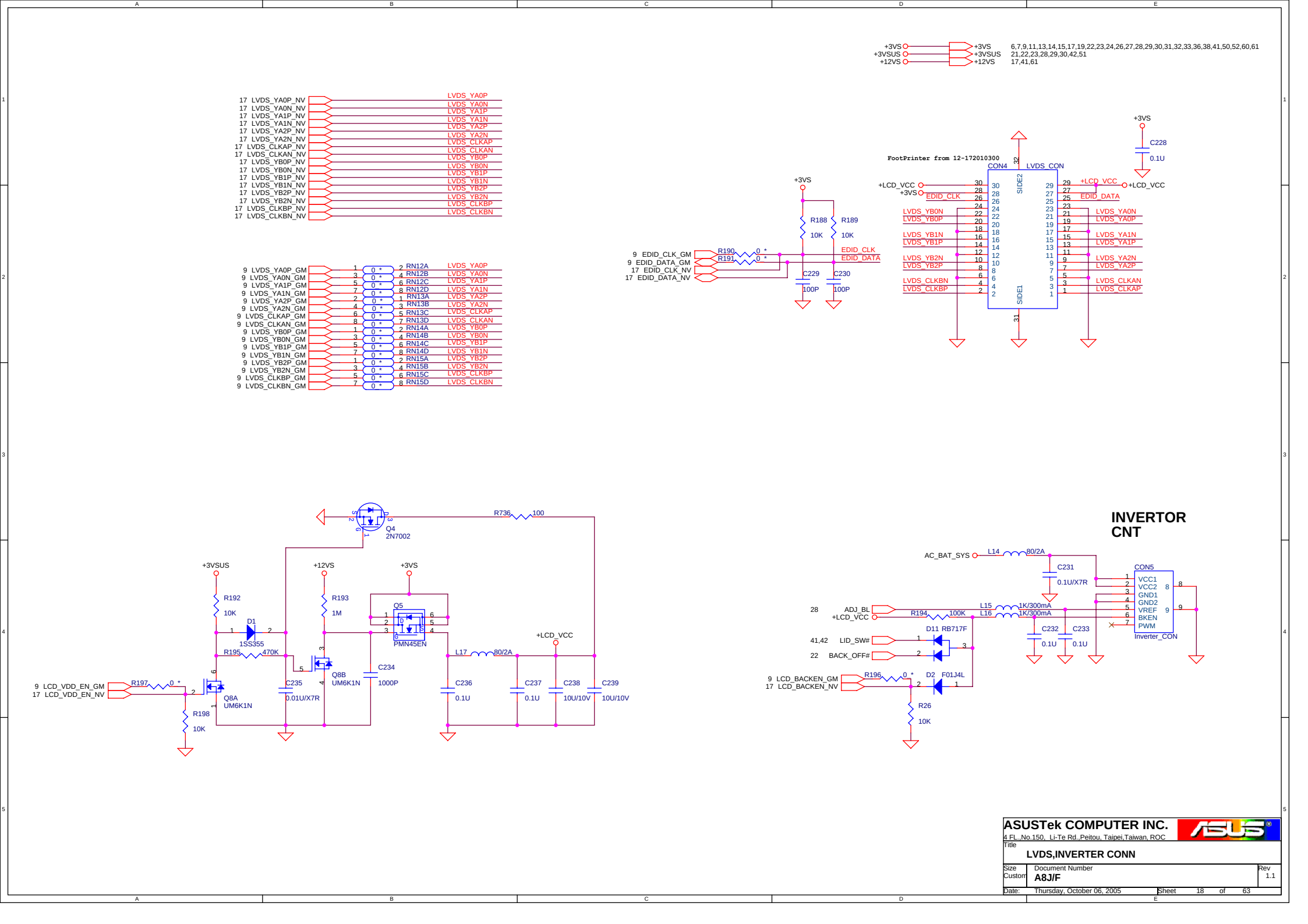
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: **DDR2 ADDRESS TERMINATION**

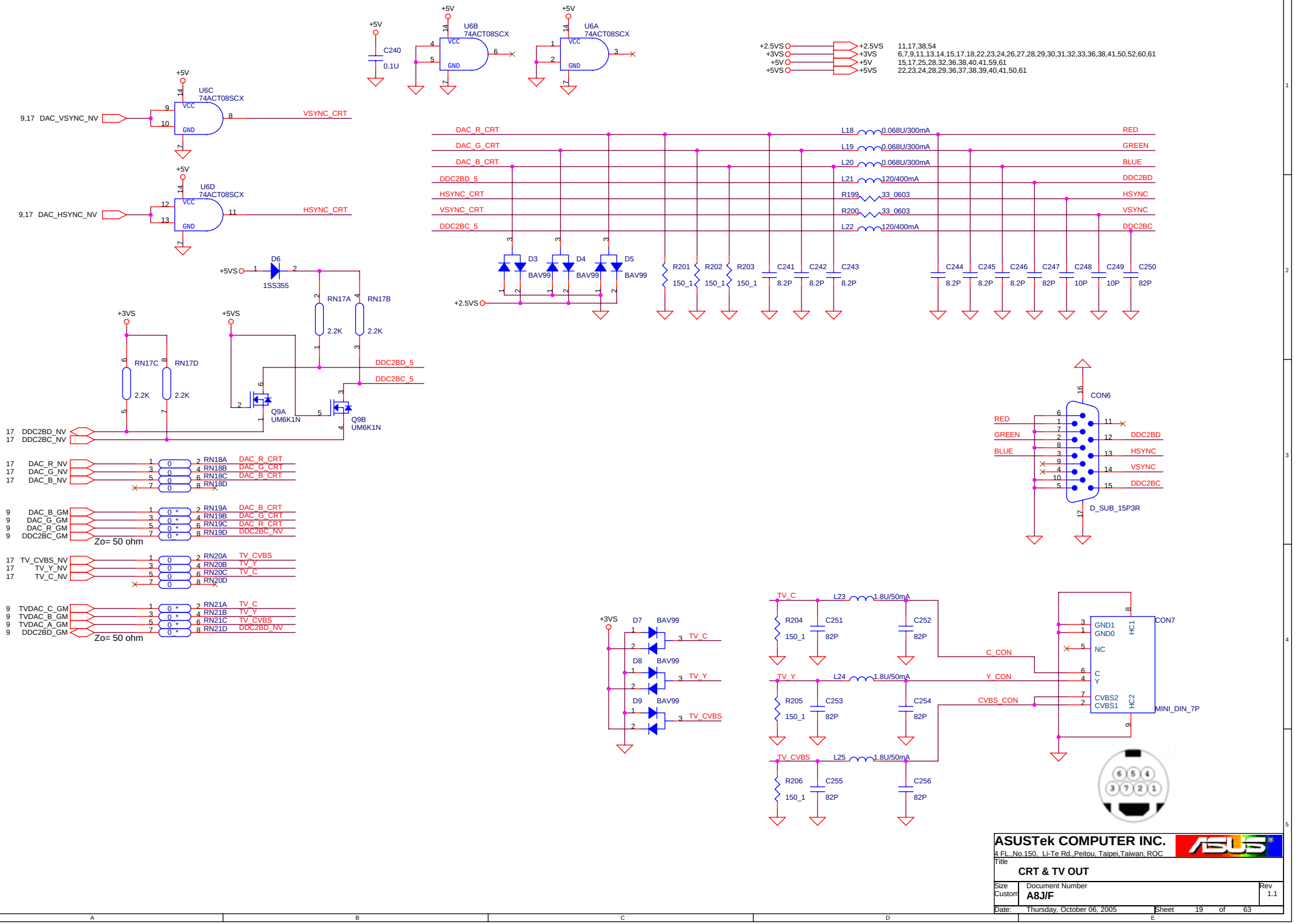
Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 16 of 63


+1.5VS +1.5VS 5,9,11,12,23,31,32,38,52
+1.8VS +1.8VS 61
+2.5VS +2.5VS 11,19,38,54
+3VS +3VS 6,7,9,11,13,14,15,18,19,22,23,24,26,27,28,29,30,31,32,33,36,38,41,50,52,60,61
+5V +5V 15,19,25,28,32,36,38,40,41,59,61
+12VS +12VS 18,41,61
CON3A GF_VGA_230P
DVI
VGA
LVDS
IGP
TV-OUT
SMBUS
PEX
OTHER
DVI_A_TX0 DVI_A_TX0# DVI_A_TX1 DVI_A_TX1# DVI_A_TX2 DVI_A_TX2#
DVI_A_CLK DVI_A_CLK#
DVI_A_HPD DVI_B_HPD/GND
DDCB_CLK DDCB_DAT DDCA_CLK DDCA_DAT
VGA_BLU VGA_RED VGA_GRN VGA_HSYNC VGA_VSYNC
LVDS_PPEN LVDS_BLEN LVDS_BL_BRGHT
LVDS_UTX0 LVDS_UTX0# LVDS_UTX1 LVDS_UTX1# LVDS_UTX2 LVDS_UTX2# LVDS_UTX3 LVDS_UTX3#
LVDS_UCLK LVDS_UCLK#
LVDS_LTX0 LVDS_LTX0# LVDS_LTX1 LVDS_LTX1# LVDS_LTX2 LVDS_LTX2# LVDS_LTX3 LVDS_LTX3#
LVDS_LCLK LVDS_LCLK#
IGP_UTX0 IGP_UTX0# IGP_UTX1 IGP_UTX1# IGP_UTX2 IGP_UTX2#
IGP_UCLK IGP_UCLK#
IGP_LTX0/DVI_B_TX0 IGP_LTX0#/DVI_B_TX0# IGP_LTX1/DVI_B_TX1 IGP_LTX1#/DVI_B_TX1# IGP_LTX2/DVI_B_TX2 IGP_LTX2#/DVI_B_TX2#
IGP_LCLK/DVI_B_CLK IGP_LCLK#/DVI_B_CLK#
TV_Y/HDTV_Y/TV_CVBS TV_C/HDTV_Pr TV_CVBS/HDTV_Pb
DDCC_CLK DDCC_DAT
SMB_CLK SMB_DAT
PEX_TX0 PEX_TX0# PEX_RX0 PEX_RX0#
PEX_TX1 PEX_TX1# PEX_RX1 PEX_RX1#
PEX_TX2 PEX_TX2# PEX_RX2 PEX_RX2#
PEX_TX3 PEX_TX3# PEX_RX3 PEX_RX3#
PEX_TX4 PEX_TX4# PEX_RX4 PEX_RX4#
PEX_TX5 PEX_TX5# PEX_RX5 PEX_RX5#
PEX_TX6 PEX_TX6# PEX_RX6 PEX_RX6#
PEX_TX7 PEX_TX7# PEX_RX7 PEX_RX7#
PEX_TX8 PEX_TX8# PEX_RX8 PEX_RX8#
PEX_TX9 PEX_TX9# PEX_RX9 PEX_RX9#
PEX_TX10 PEX_TX10# PEX_RX10 PEX_RX10#
PEX_TX11 PEX_TX11# PEX_RX11 PEX_RX11#
PEX_TX12 PEX_TX12# PEX_RX12 PEX_RX12#
PEX_TX13 PEX_TX13# PEX_RX13 PEX_RX13#
PEX_TX14 PEX_TX14# PEX_RX14 PEX_RX14#
PEX_TX15 PEX_TX15# PEX_RX15 PEX_RX15#
CLK_REQ# PEX_RST#
PEX_REFCLK PEX_REFCLK#
THERM# PRSNT1# PRSNT2# RUNPWROK
PEXP_TXP0 C193 PEXP_TXP0# C194 PEXP_TXP1 C195 PEXP_TXP1# C196 PEXP_TXP2 C197 PEXP_TXP2# C198 PEXP_TXP3 C199 PEXP_TXP3# C200 PEXP_TXP4 C202 PEXP_TXP4# C203 PEXP_TXP5 C204 PEXP_TXP5# C205 PEXP_TXP6 C207 PEXP_TXP6# C208 PEXP_TXP7 C209 PEXP_TXP7# C210 PEXP_TXP8 C212 PEXP_TXP8# C213 PEXP_TXP9 C214 PEXP_TXP9# C215 PEXP_TXP10 C216 PEXP_TXP10# C217 PEXP_TXP11 C218 PEXP_TXP11# C219 PEXP_TXP12 C220 PEXP_TXP12# C221 PEXP_TXP13 C222 PEXP_TXP13# C223 PEXP_TXP14 C224 PEXP_TXP14# C225 PEXP_TXP15 C226 PEXP_TXP15# C227 0.1U/10V
PEX_RST# PLT_RST# 6,9,21,22,24,26,27,28,32,38
CLK_PCIE_VGA 7 CLK_PCIE_VGA# 7
VGA_DETEC# 26 PWR_OK_VGA 60
AC_BAT_SYS C201 15UF/25V
CON3B GF_VGA_230P
PWR_SRC1 PWR_SRC2 PWR_SRC3 PWR_SRC4 PWR_SRC5 PWR_SRC6 PWR_SRC7 PWR_SRC8
1V8RUN_1 1V8RUN_2 1V8RUN_3 1V8RUN_4 1V8RUN_5 1V8RUN_6 1V8RUN_7
C206 10U/10V
3V3RUN_1 3V3RUN_2 3V3RUN_3
C211 10U/10V
5VRUN 2V5RUN
RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 AC/BATT#
CLK_VGA27SS CLK_VGA27FIX
SUSB#_PWR 52,53,54,58,61,63
HDTV_EN# T84
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25 GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
VGA CONN
Size Custom
Document Number A8J/F
Rev 1.1
Date: Thursday, October 06, 2005
Sheet 17 of 63



ASUSTek COMPUTER INC.			
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC			
Title: LVDS,INVERTER CONN			
Size: Custom	Document Number: A8J/F		Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 18 of 63		

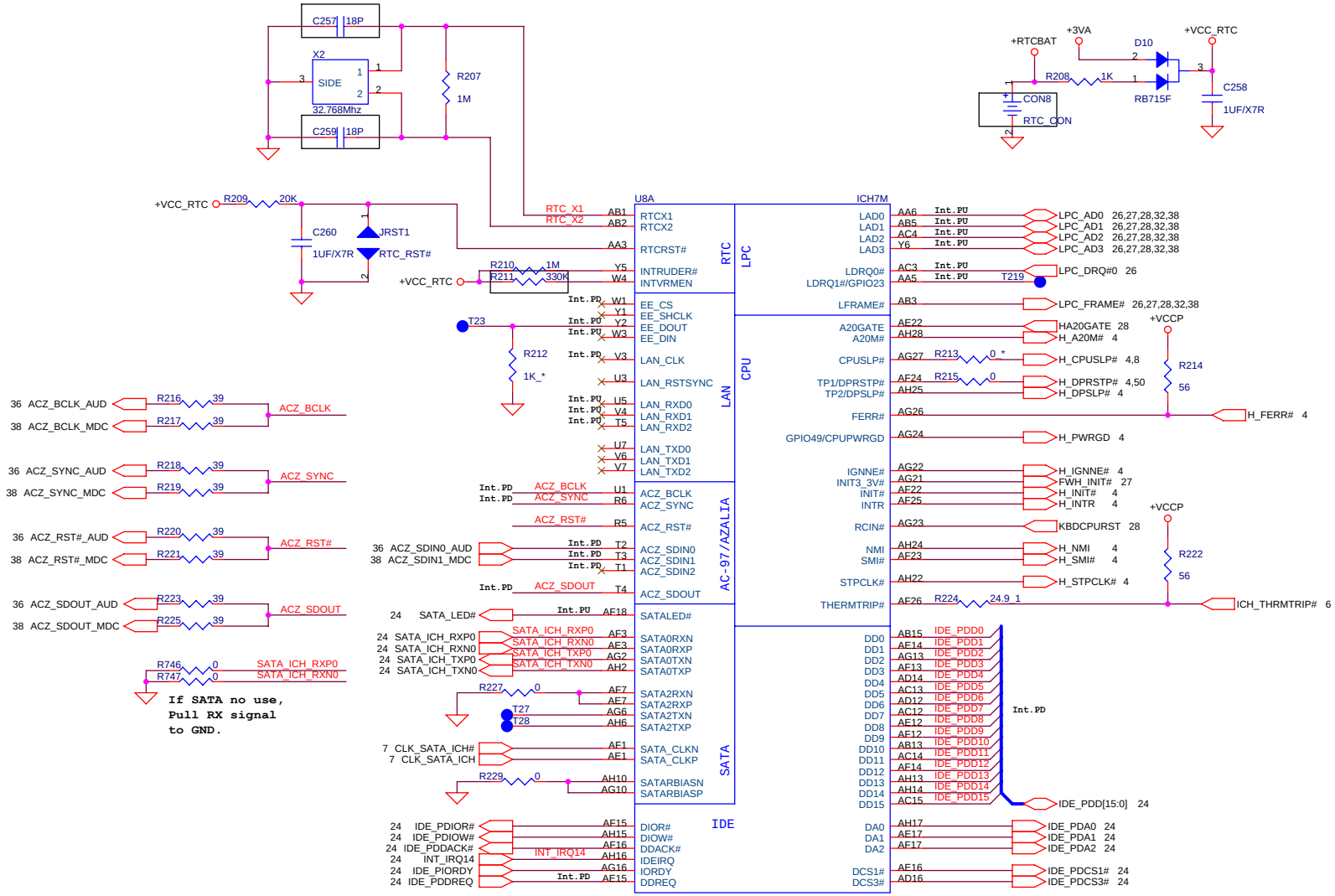


ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

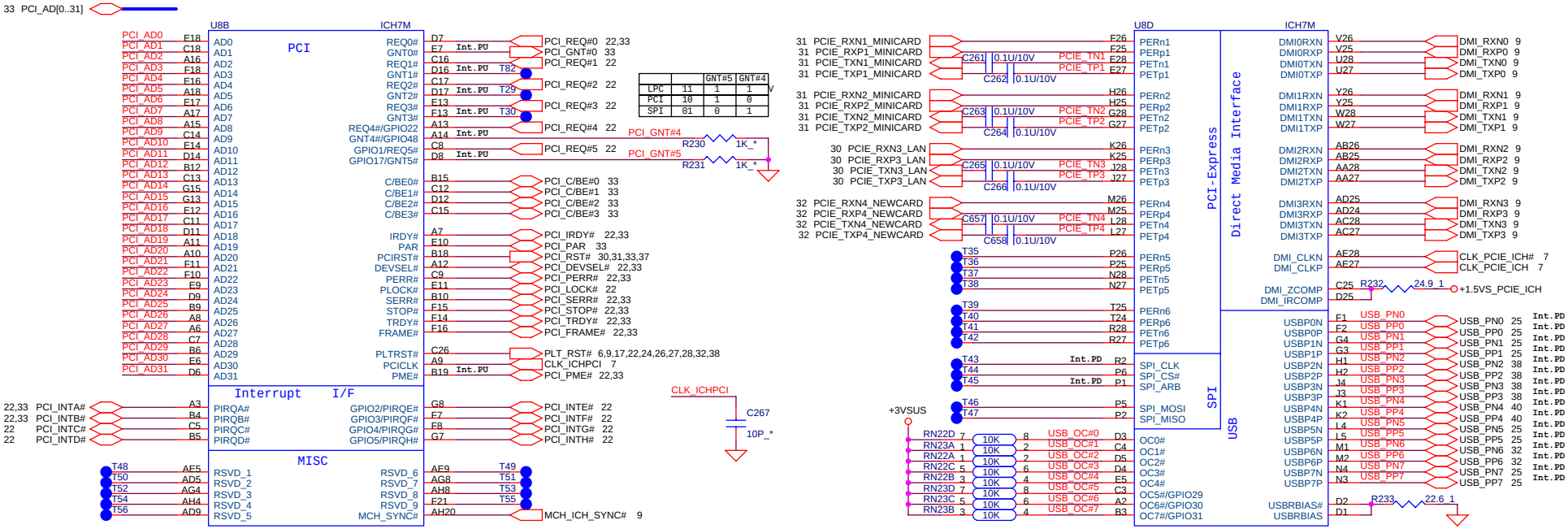
Title: **CRT & TV OUT**

Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 19 of 63



ASUSTek COMPUTER INC.			
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC			
Title: ICH7M--CPU,IDE,AUDIO			
Size: Custom	Document Number: A8J/F		Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 20 of 63		



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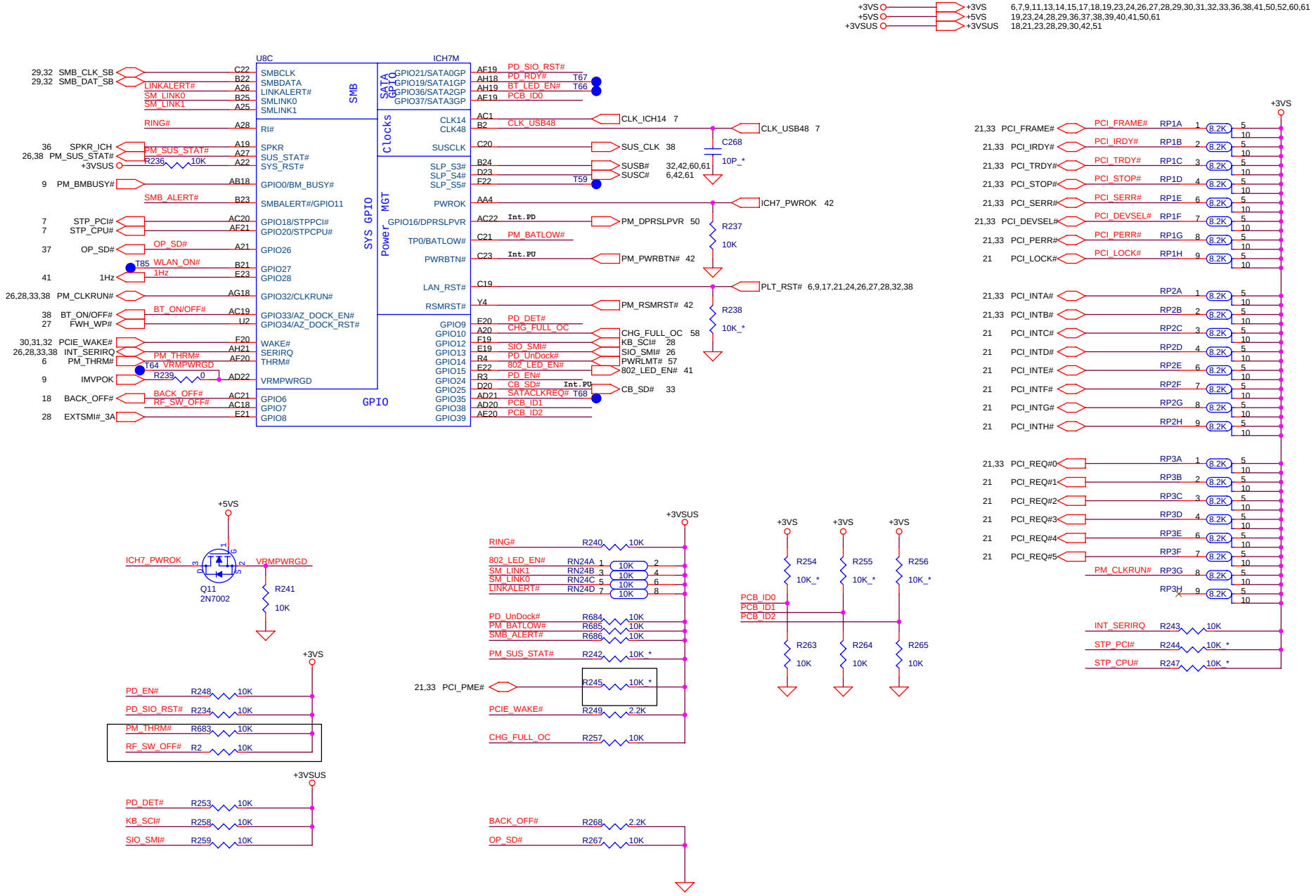
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

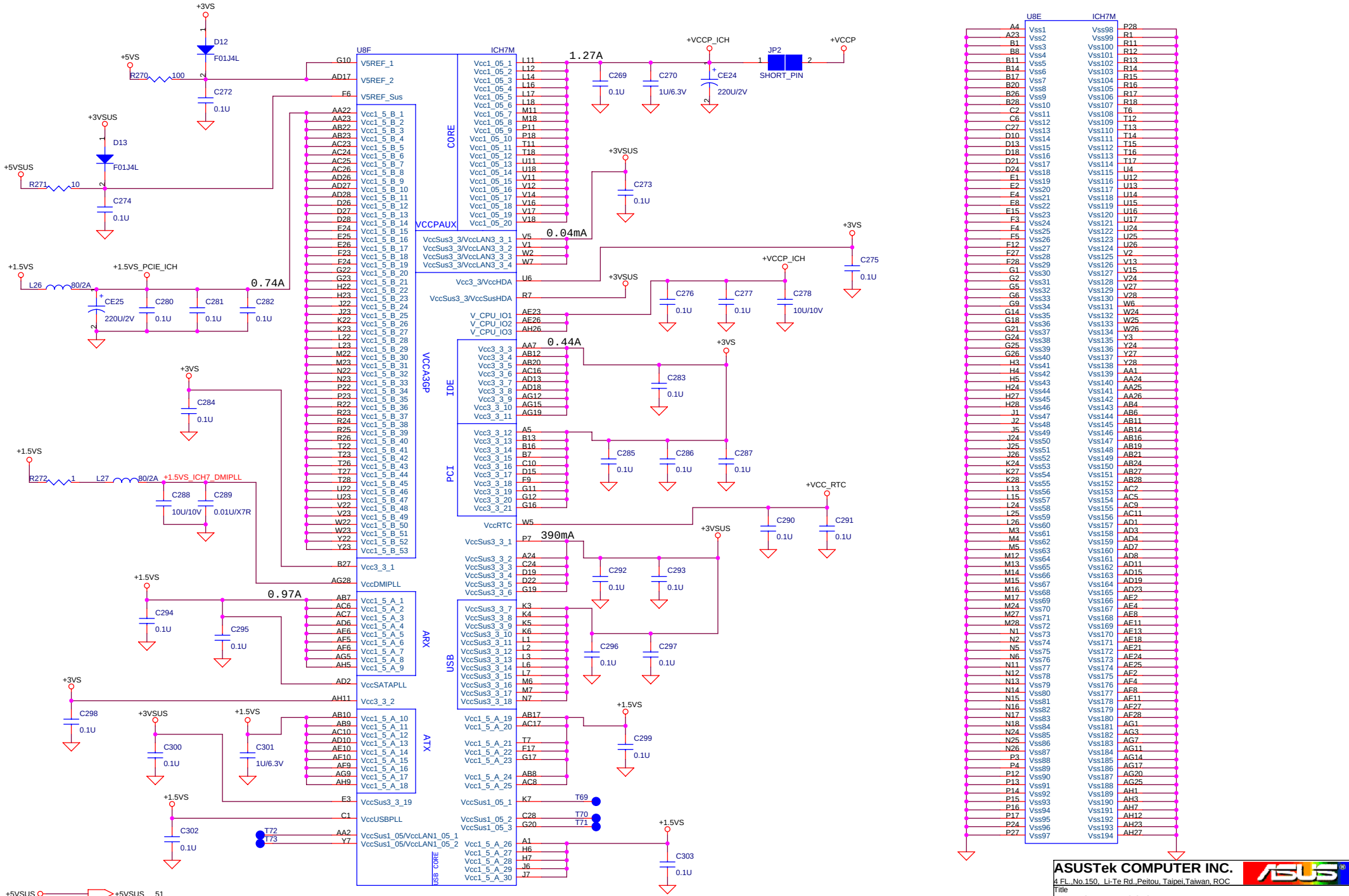
Title: **ICH7M--PCI,PCI-E,USB**

Size	Document Number	Rev
Custom	**A8J/F**	1.1

Date: Thursday, October 06, 2005 Sheet 21 of 63



Company	ASUSTek COMPUTER INC.	
Address	4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title	ICH7M--GPIO	
Size	Custom	
Document Number	A8J/F	Rev 1.1
Date:	Thursday, October 06, 2005	Sheet 22 of 63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ICH7M
CORE
VCCPAUX
VCCA3GP
IDE
PCI
USB
ARX
ATX
DSUS
V5REF_1
V5REF_2
V5REF_Sus
Vcc1_5_B_1
Vcc1_5_B_2
Vcc1_5_B_3
Vcc1_5_B_4
Vcc1_5_B_5
Vcc1_5_B_6
Vcc1_5_B_7
Vcc1_5_B_8
Vcc1_5_B_9
Vcc1_5_B_10
Vcc1_5_B_11
Vcc1_5_B_12
Vcc1_5_B_13
Vcc1_5_B_14
Vcc1_5_B_15
Vcc1_5_B_16
Vcc1_5_B_17
Vcc1_5_B_18
Vcc1_5_B_19
Vcc1_5_B_20
Vcc1_5_B_21
Vcc1_5_B_22
Vcc1_5_B_23
Vcc1_5_B_24
Vcc1_5_B_25
Vcc1_5_B_26
Vcc1_5_B_27
Vcc1_5_B_28
Vcc1_5_B_29
Vcc1_5_B_30
Vcc1_5_B_31
Vcc1_5_B_32
Vcc1_5_B_33
Vcc1_5_B_34
Vcc1_5_B_35
Vcc1_5_B_36
Vcc1_5_B_37
Vcc1_5_B_38
Vcc1_5_B_39
Vcc1_5_B_40
Vcc1_5_B_41
Vcc1_5_B_42
Vcc1_5_B_43
Vcc1_5_B_44
Vcc1_5_B_45
Vcc1_5_B_46
Vcc1_5_B_47
Vcc1_5_B_48
Vcc1_5_B_49
Vcc1_5_B_50
Vcc1_5_B_51
Vcc1_5_B_52
Vcc1_5_B_53
Vcc3_3_1
VccDMIPLL
Vcc1_5_A_1
Vcc1_5_A_2
Vcc1_5_A_3
Vcc1_5_A_4
Vcc1_5_A_5
Vcc1_5_A_6
Vcc1_5_A_7
Vcc1_5_A_8
Vcc1_5_A_9
VccSATAPLL
Vcc3_3_2
Vcc1_5_A_10
Vcc1_5_A_11
Vcc1_5_A_12
Vcc1_5_A_13
Vcc1_5_A_14
Vcc1_5_A_15
Vcc1_5_A_16
Vcc1_5_A_17
Vcc1_5_A_18
VccSus3_3_19
VccUSBPLL
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
Vcc1_5_A_19
Vcc1_5_A_20
Vcc1_5_A_21
Vcc1_5_A_22
Vcc1_5_A_23
Vcc1_5_A_24
Vcc1_5_A_25
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VccSus1_05_2
VccSus1_05_3
Vcc1_5_A_26
Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
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Vcc1_05_10
Vcc1_05_11
Vcc1_05_12
Vcc1_05_13
Vcc1_05_14
Vcc1_05_15
Vcc1_05_16
Vcc1_05_17
Vcc1_05_18
Vcc1_05_19
Vcc1_05_20
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
Vcc3_3_3
Vcc3_3_4
Vcc3_3_5
Vcc3_3_6
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VccSus3_3_16
VccSus3_3_17
VccSus3_3_18
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+3VSUS
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+1.5VS_ICH7_DMIPLL
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+VCCP
+VCC_RTC
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0.44A
390mA
0.74A
0.97A
D12
F01J4L
D13
R270
100
R271
10
R272
1
L26
L27
80/2A
C272
C273
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C269
C270
CE24
CE25
220U/2V
10U/10V
0.01U/X7R
1U/6.3V
0.1U
JP2
SHORT_PIN
T69
T70
T71
T72
T73
U8E
ICH7M
Vss1
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AB14
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AF28
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AG3
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AG17
AG20
AG25
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AH3
AH7
AH12
AH23
AH27
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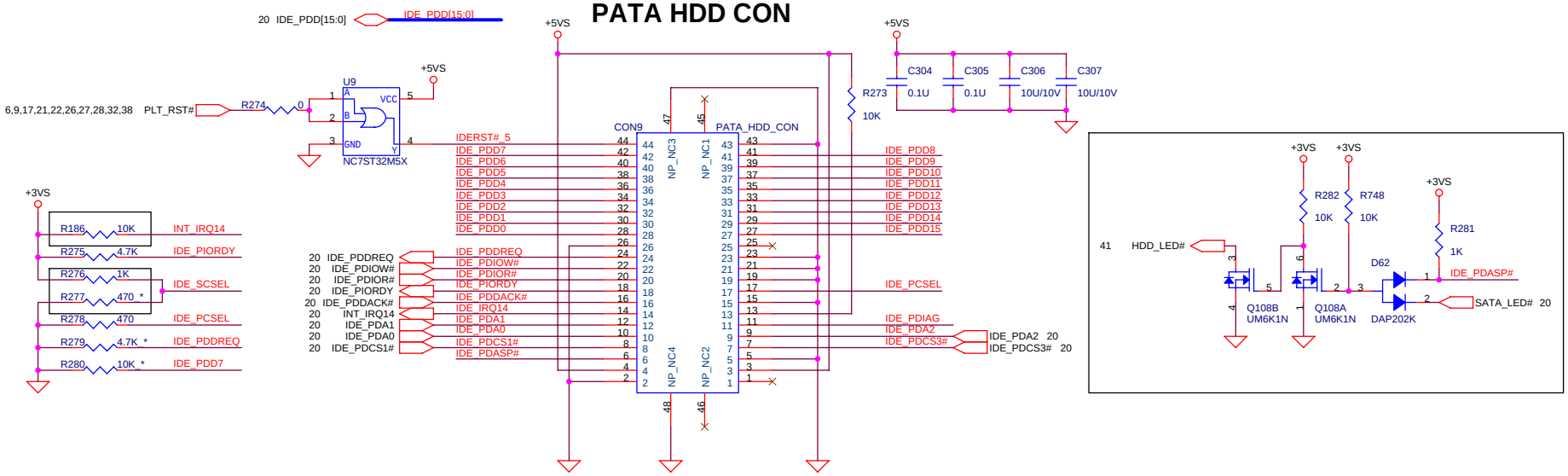
+VCCP 4,5,6,8,11,12,20,52
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
ICH7M--VCC,GND
Size
Custom
Document Number
A8J/F
Rev
1.1
Date:
Thursday, October 06, 2005
Sheet
23
of
63

PATA HDD CON



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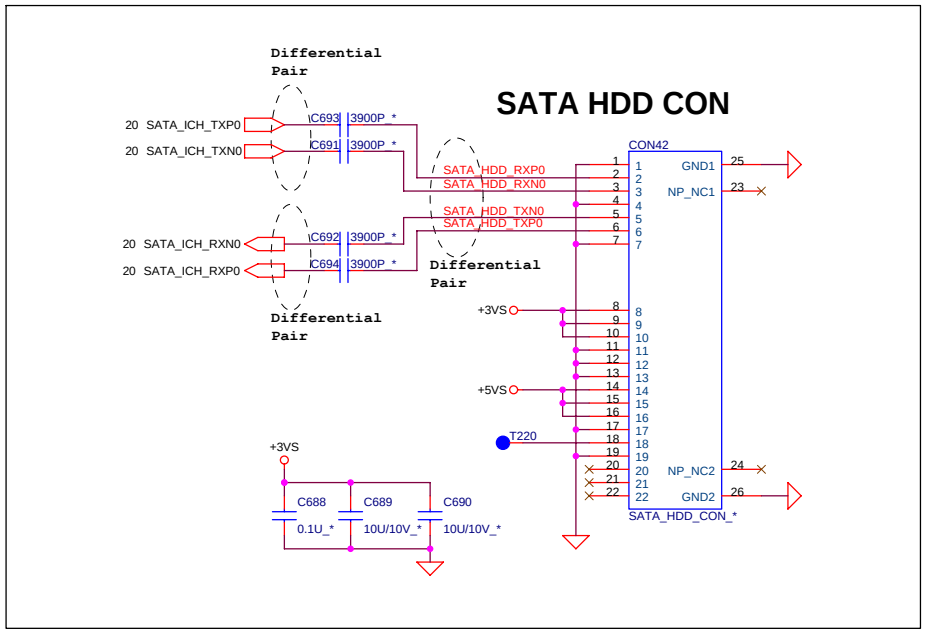
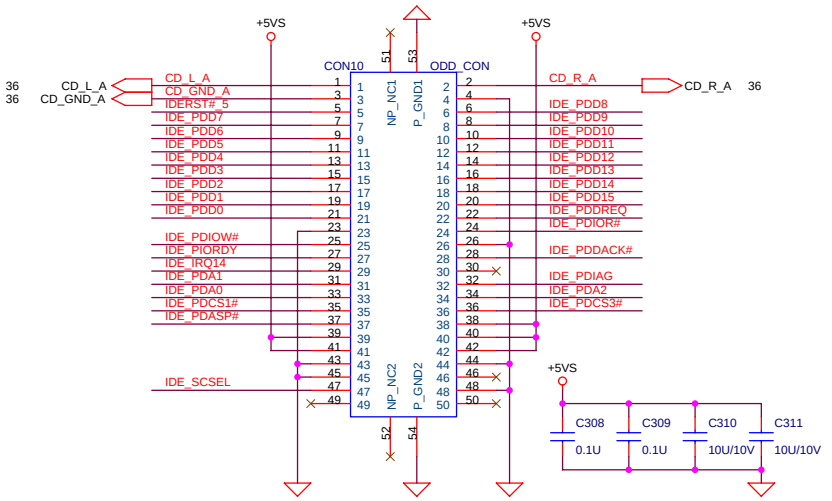


PATA CD-ROM CON



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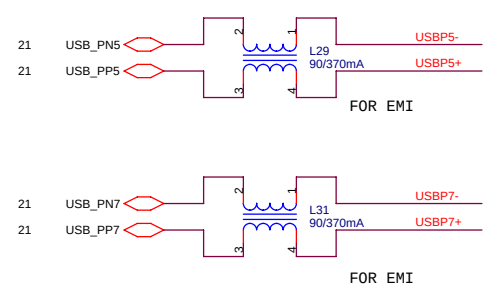
+5V +5V 15,17,19,25,28,32,36,38,40,41,59,61

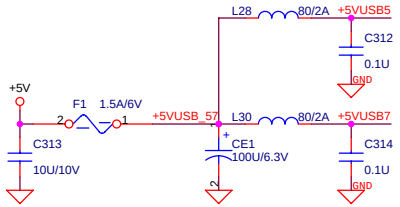
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

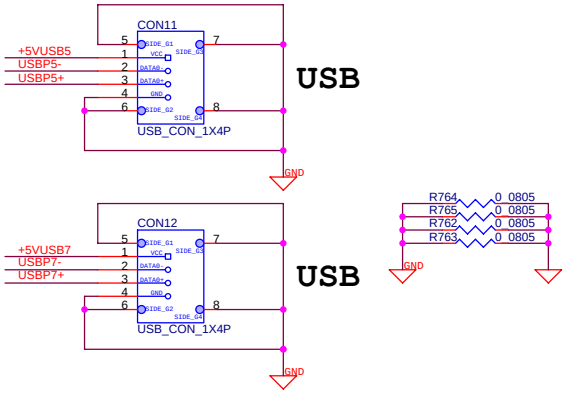
Title: **HDD & CD-ROM CONN**

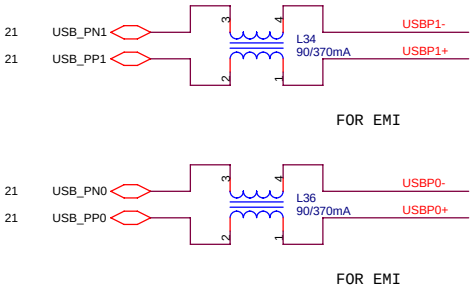
Size	Document Number	Rev
Custom	A8J/F	1.1

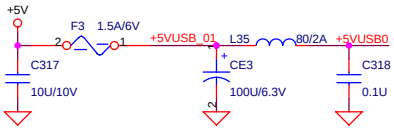
Date: Thursday, October 06, 2005 Sheet 24 of 63

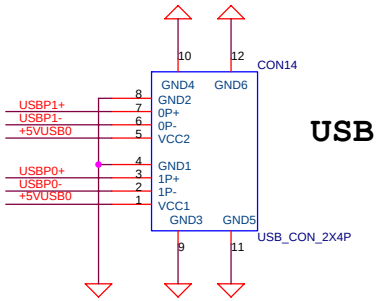






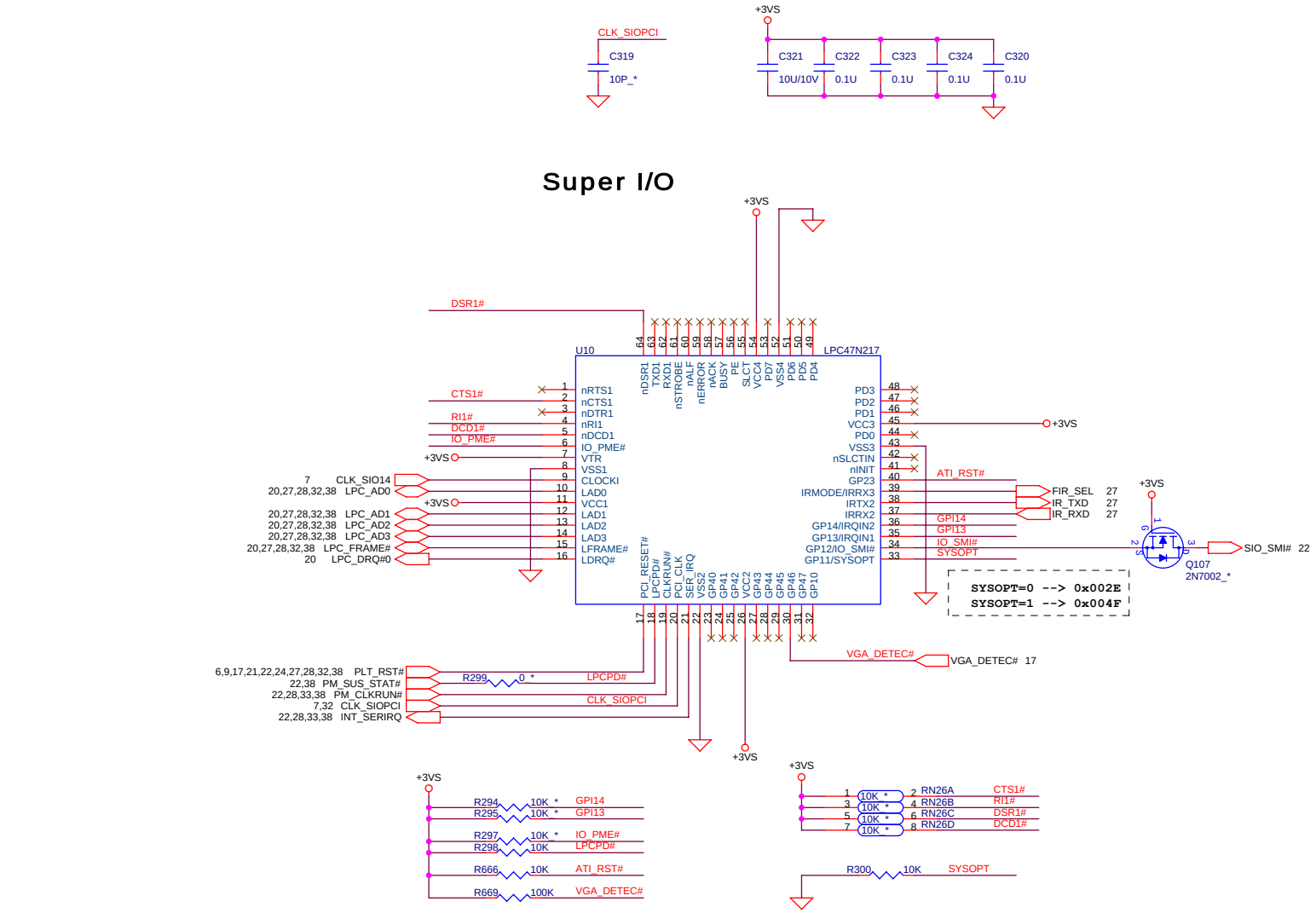






15,17,19,28,32,36,38,40,41,59,61

ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: USB PORTS		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 25 of 63	



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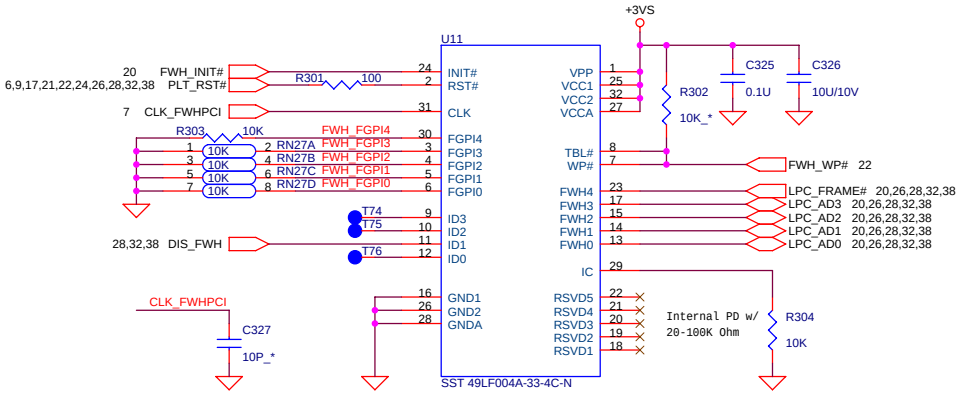
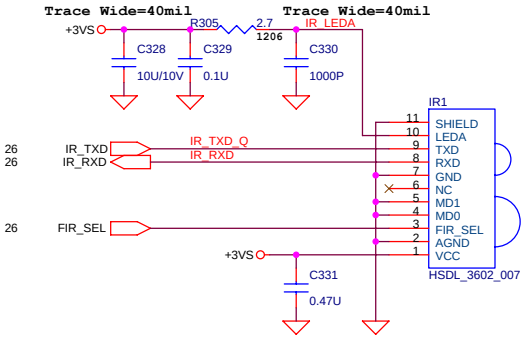
ASUSTek COMPUTER INC.			
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC			
Title: SUPER IO LPC47N217			
Size: Custom	Document Number: A8J/F		Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 26 of 63		



PLCC32 Socket Part Number :
12-043000321

Graphics from:
05-001005111



+3VS +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,28,29,30,31,32,33,36,38,41,50,52,60,61

ASUSTek COMPUTER INC.
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Title: **BIOS , IR**

Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 27 of 63

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

CON43 DEBUG_CON
SIDE2: LPC_AD0, LPC_AD1, LPC_AD2, DIS_FWH, LPC_AD3, LPC_FRAME#
SIDE1: CLK_KBCPCI
DIS_FWH 27,32,38

KSI0 RP4A, KSI1 RP4B, KSI2 RP4C, KSI3 RP4D, KSI4 RP4E, KSI5 RP4F, KSI6 RP4G, KSI7 RP4H — 10K

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

CON16 Internal_KB_CON
SIDE2: KSI1, KSO7, KSI7, KSO0, KSI6, KSO9, KSI5, KSO3, KSI4, KSO1, KSI2, KSI3, KSO5, KSO13, KSI0, KSO2, KSO4, KSO8, KSO6, KSO11, KSO10, KSO12, KSO14, KSO15, KBDDT0
SIDE1: KBDDT1

RN29A RN29B RN29C RN29D RP5A RP5B RP5C RP5D RP5E RP5F RP5G RP5H — 10K

CLK_KBCPCI — C337 10P_*

U13 M38857

22,26,33,38 INT_SERIRQ	63	P87/SERIRQ
7 CLK_KBCPCI	64	P86/LCLK
6,9,17,21,22,24,26,27,32,38 PLT_RST#	65	P85/LRESET#
20,26,27,32,38 LPC_FRAME#	66	P84/LFRAME#
20,26,27,32,38 LPC_AD3	67	P83/LAD3
20,26,27,32,38 LPC_AD2	68	P82/LAD2
20,26,27,32,38 LPC_AD1	69	P81/LAD1
20,26,27,32,38 LPC_AD0	70	P80/LAD0
	71	VCC
	72	VREF
	31	P27 SCR_LED#
	32	P26
	33	P25
	34	P24 SET_PCIRSTNS#
57 BAT_LEARN	35	P23 BAT_LEARN
	36	P22 R321 100K
42 KBCRSM	37	P21
	38	P20
	23	P42/INT0
	22	P43/INT1*
KBCPURST_3Q	21	P44/RXD
KBC_GA20	20	P45/TXD
KBSCI_3Q	19	P46/SCLK1
22,26,33,38 PM_CLKRUN#	18	P47/SRDY1#/CLKRUN#
BAT_LLOW#_OC	17	P50/INT5*
FAN1_TACH	16	P51/INT20
KBDDT0	15	P52/INT30/1-WIRE1
KBDDT1	14	P53/INT40/1-WIRE2
	13	P54/CNTR0*
	12	P55/CNTR1*
	11	P56/DA1/PWM01
	10	P57/DA2/PWM11
	74	P67/AN7
	75	P66/AN6
	76	P65/AN5
	77	P64/AN4
	78	P63/AN3
	79	P62/AN2
	80	P61/AN1
	1	P60/AN0
	4	P75/INT41
	5	P74/INT31
	6	P73/INT21
	7	P72
	8	P71
INTCLK_5S	9	P70
INTDATA_5S		
	2	P77/SCL
	3	P76/SDA
	39	P17/KSO15 KSO15
	40	P16/KOS14 KSO14
	41	P15/KSO13 KSO13
	42	P14/KSO12 KSO12
	43	P13/KSO11 KSO11
	44	P12/KSO10 KSO10
	45	P11/KSO9 KSO9
	46	P10/KSO8 KSO8
	47	P07/KSO7 KSO7
	48	P06/KSO6 KSO6
	49	P05/KSO5 KSO5
	50	P04/KSO4 KSO4
	51	P03/KSO3 KSO3
	52	P02/KSO2 KSO2
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	54	P00/KSO0 KSO0
	55	P37/KSI8 KSI7
	56	P36/KSI7 KSI6
	57	P35/KSI6 KSI5
	58	P34/KSI5 KSI4
	59	P33/KSI4 KSI3
	60	P32/KSI3 KSI2
	61	P31/PWM10/KSI2 KSI1
	62	P30/PWM00/KSI0 KSI0
	28	XIN X1_KBC
	29	XOUT X2_KBC
	27	P40/XCOUT KBC_EXTSMI
	26	P41/XCIN
	25	RESET# PCI_RSTNS#
	24	CNVSS
	30	VSS
	73	AVSS

80mA

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

C338 0.1U, C339 0.1U

RN28A RN28B RN28C RN28D — 10K

41 MSK_INSTKEY#
40 WATCHDOG
41 SWDJ_EN
58 BAT_LLOW#_OC
40 FAN1_TACH
42 LID_KBC#
59 BAT_IN_OC#
40 FAN1_DC
18 ADJ_BL
41 PANLOCK_#
41 MARATHON_#
59 ACIN_OC#
41 WIRELESS_#
41 INTERNET_#
41 BLUETOOTH_#

D14 1SS355

RN30A RN30B RN30C RN30D — 10K

PANLOCK_LED 41

R319 10K, R320 10K

R322 10K, R323 10K

D15 1SS355, D16 1SS355

KBC_GA20 — HA20GATE 20
KBCPURST_3Q — KBDCPURST 20
KBSCI_3Q — KB_SCI# 22

Q13 2N7002

X1_KBC — C340 10P — X3 8MHZ — C341 10P — X2_KBC
R324 1M

R326 4.7K, R327 4.7K

40,58 SMC_BAT — Q14A UM6K1N
40,58 SMD_BAT — Q14B UM6K1N

RN33A RN33B RN33C RN33D — 10K

BAT_LLOW#_OC
FAN1_TACH
BAT_LEARN — R734 100K

R331 4.7K, R332 4.7K

41 INTCLK_5S
41 INTDATA_5S

R325 10K — EXTSMI#_3A 22

KBC_EXTSMI — R333 10K — Q15 2N7002

PLT_RST#
SET_PCIRSTNS# — R330 47K
U14 74LVC1G32GV — PCI_RSTNS# — PCI_RSTNS# 30

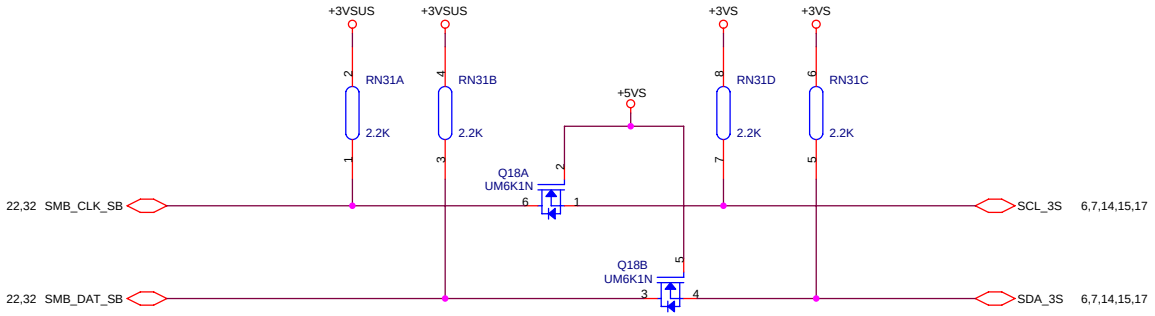
C342 0.1U

+3V	+3V	30,31,32,34,37,38,42,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,29,30,31,32,33,36,38,41,50,52,60,61
+3VSUS	+3VSUS	18,21,22,23,29,30,42,51
+5V	+5V	15,17,19,25,32,36,38,40,41,59,61
+5VS	+5VS	19,22,23,24,29,36,37,38,39,40,41,50,61
+5VLCM	+5VLCM	57,58,59,60

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: KBC 38857
Size: Custom
Document Number: A8J/F
Rev: 1.1
Date: Thursday, October 06, 2005
Sheet 28 of 63

ICH7-M



Termal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM

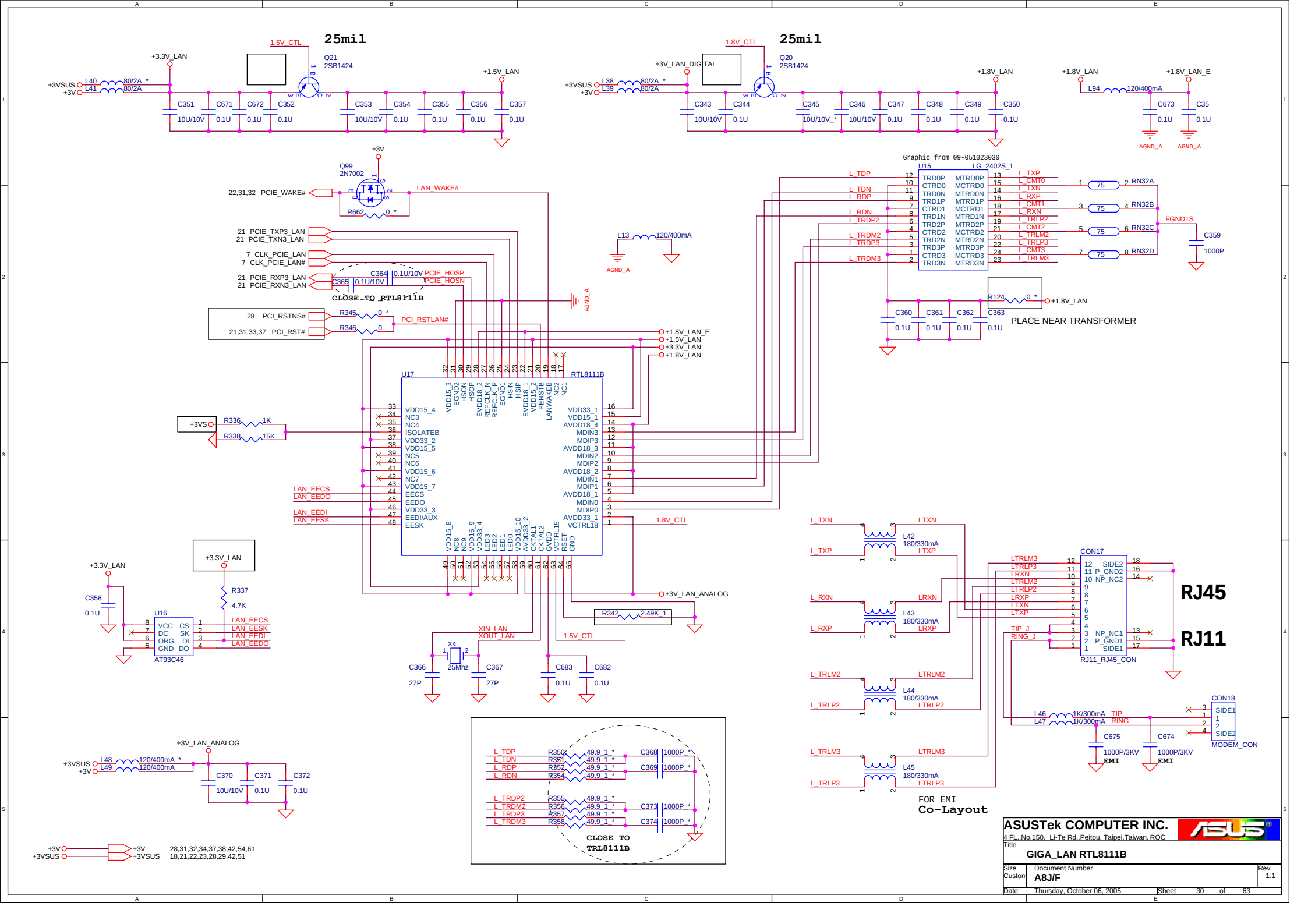
+3VA	+3VA	20,38,41,42,54,63
+5VA	+5VA	6,51,54,57
+3VSUS	+3VSUS	18,21,22,23,28,30,42,51
+5VSUS	+5VSUS	23,51
+0.9VS	+0.9VS	16,53
+VCCP	+VCCP	4,5,6,8,11,12,20,23,52
+1.5VS	+1.5VS	5,9,11,12,17,23,31,32,38,52
+2.5VS	+2.5VS	11,17,19,38,54
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,30,31,32,33,36,38,41,50,52,60,61
+5VS	+5VS	19,22,23,24,28,36,37,38,39,40,41,50,61
+12VS	+12VS	17,18,41,61
+1.8V	+1.8V	9,12,14,15,38,53
+3V	+3V	28,30,31,32,34,37,38,42,54,61
+5V	+5V	15,17,19,25,28,32,36,38,40,41,59,61
+12V	+12V	34,37,61
+VCORE	+VCORE	5,6,50
+5VLCM	+5VLCM	28,57,58,59,60

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: SM BUS & POWER PORT

Size: Custom | Document Number: A8J/F | Rev: 1.1

Date: Thursday, October 06, 2005 | Sheet 29 of 63

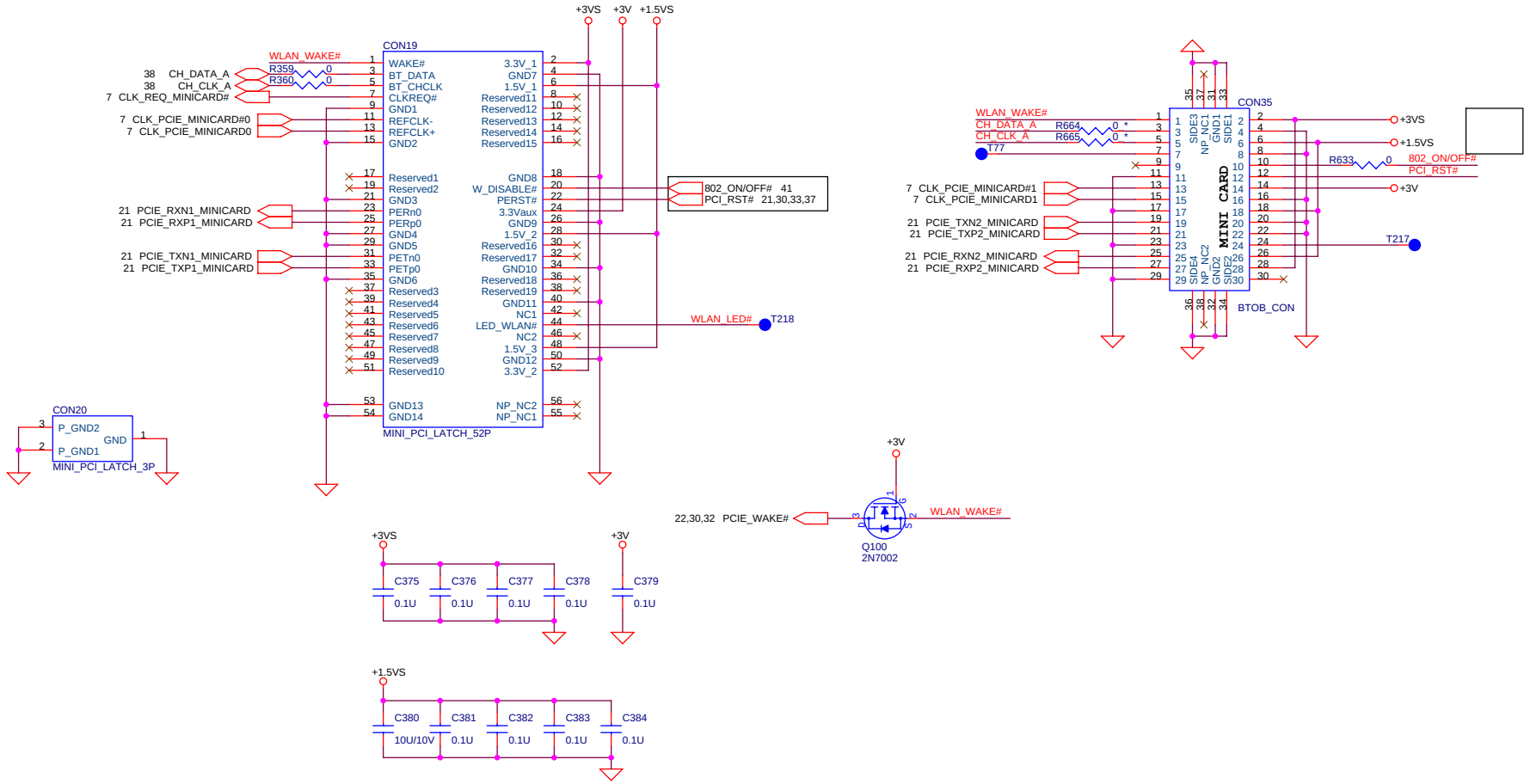


ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: GIGA_LAN RTL8111B

Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 30 of 63



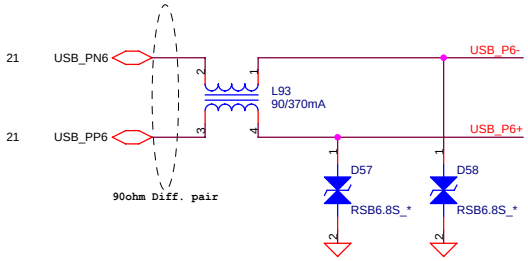
+1.5VS	+1.5VS	5,9,11,12,17,23,32,38,52
+3V	+3V	28,30,32,34,37,38,42,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,32,33,36,38,41,50,52,60,61

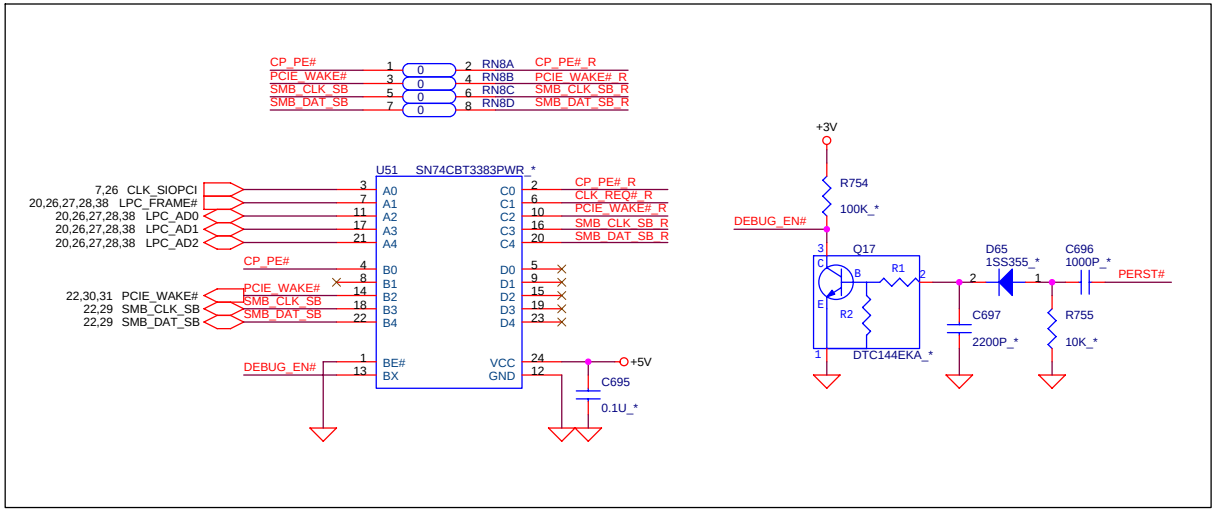
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

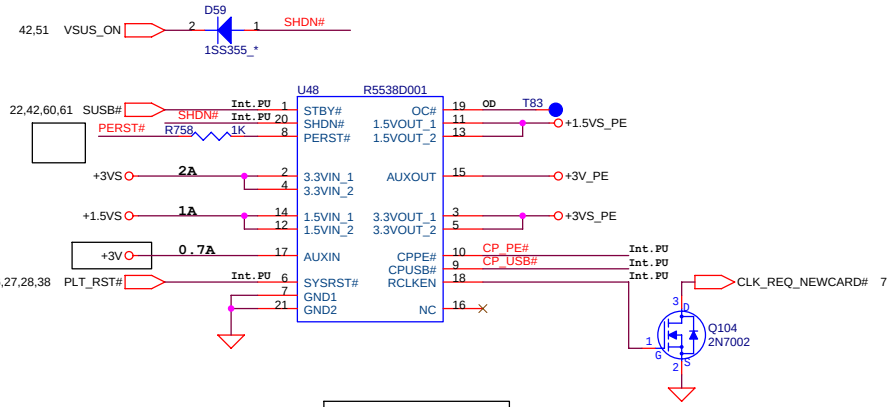
Title: **MINI CARD**

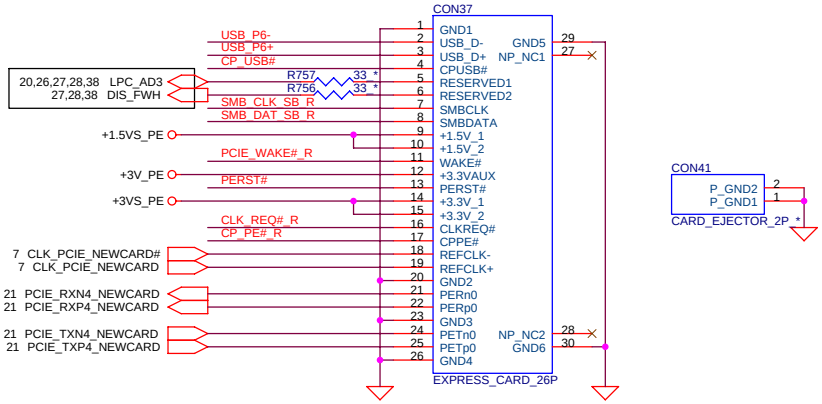
Size	Document Number	Rev
Custom	A8J/F	1.1

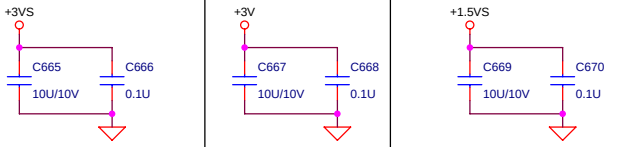
Date: Thursday, October 06, 2005 Sheet 31 of 63

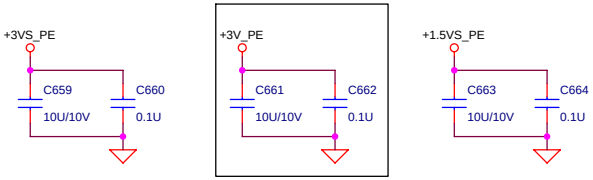












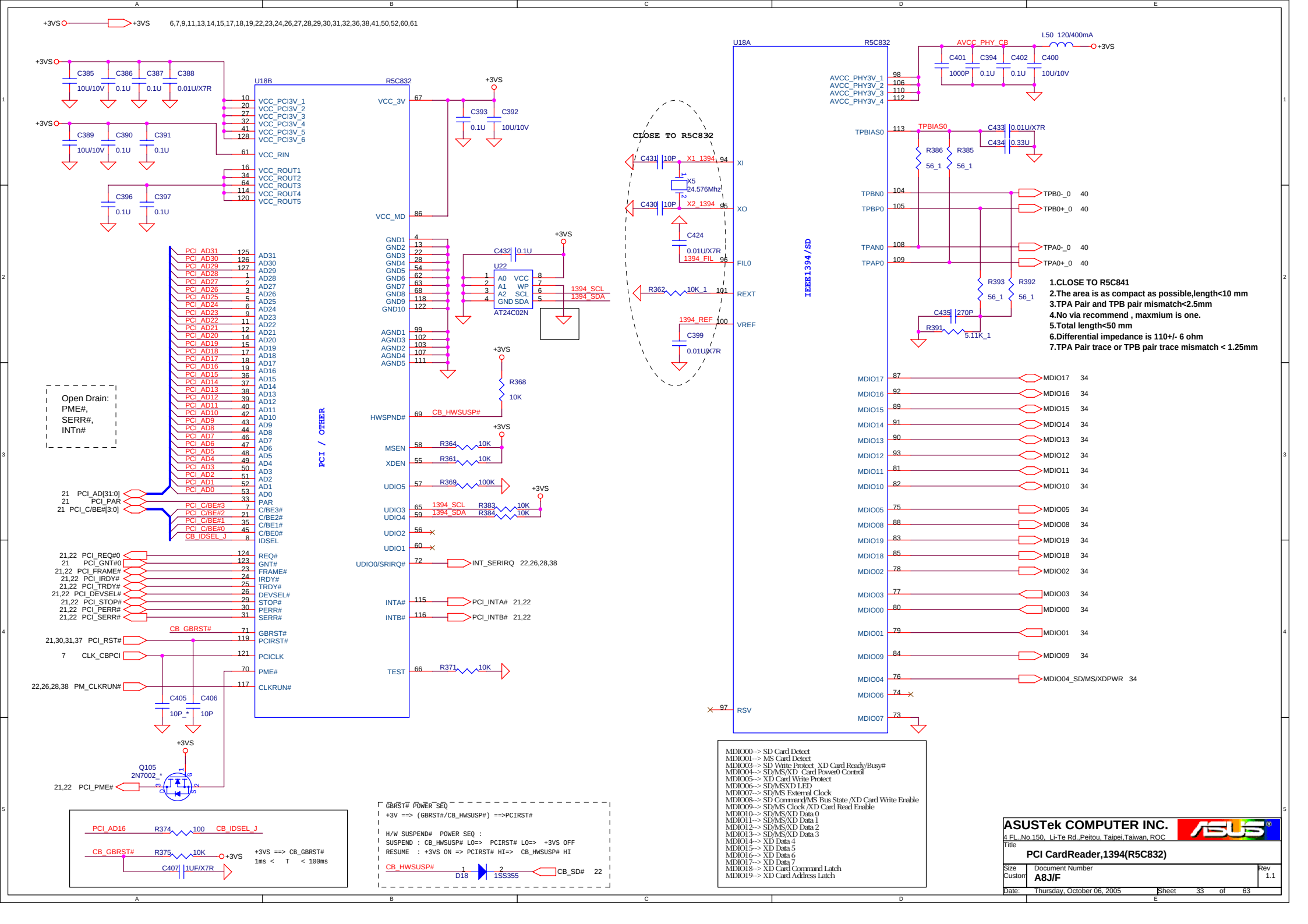
+1.5VS	+1.5VS	5,9,11,12,17,23,31,38,52
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,33,36,38,41,50,52,60,61
+3V	+3V	28,30,31,34,37,38,42,54,61

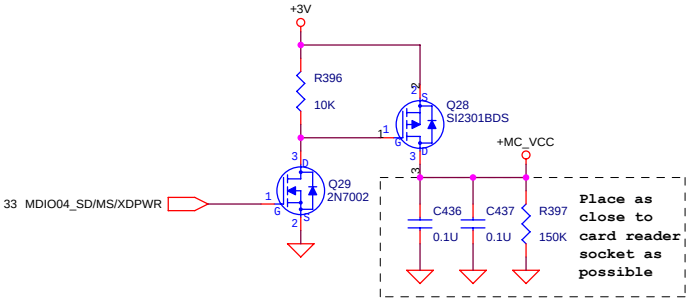
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

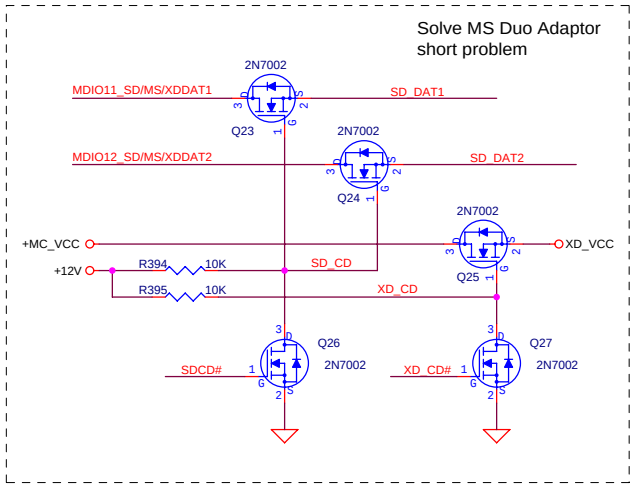
Title: **NEW CARD**

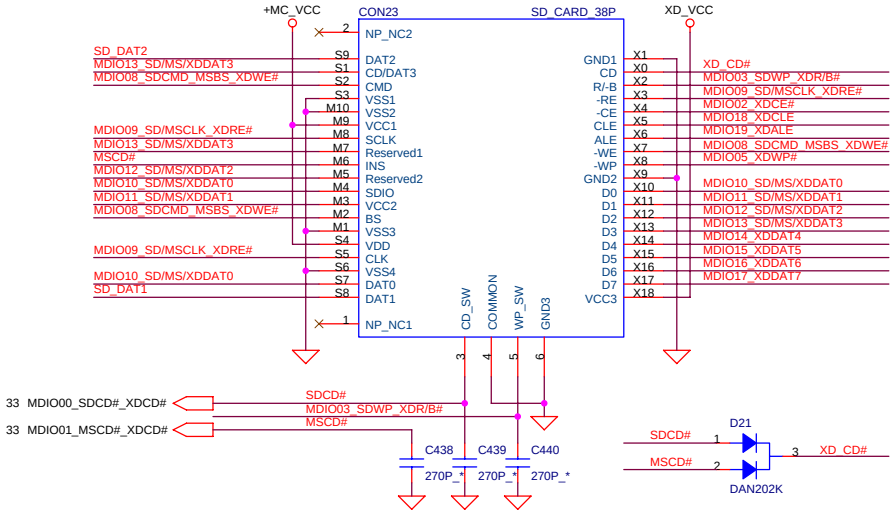
Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 32 of 63


+3VS +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,36,38,41,50,52,60,61
U18B
R5C832
U18A
R5C832
PCI / OTHER
IEEE1394/SD
CLOSE TO R5C832
C385 C386 C387 C388 10U/10V 0.1U 0.1U 0.01U/X7R
C389 C390 C391 10U/10V 0.1U 0.1U
C396 C397 0.1U 0.1U
C393 C392 0.1U 10U/10V
C432 0.1U
U22 AT24C02N
1394_SCL 1394_SDA
C431 10P X1_1394 X5 24.576Mhz C430 10P X2_1394
C424 0.01U/X7R
1394_FIL
R362 10K_1
1394_REF C399 0.01U/X7R
L50 120/400mA
AVCC_PHY_CB
C401 1000P C394 0.1U C402 0.1U C400 10U/10V
TPBIAS0 C433 0.01U/X7R C434 0.33U
R386 56_1 R385 56_1
R393 56_1 R392 56_1
C435 270P R391 5.11K_1
1.CLOSE TO R5C841
2.The area is as compact as possible,length<10 mm
3.TPA Pair and TPB pair mismatch<2.5mm
4.No via recommend , maxmium is one.
5.Total length<50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm
Open Drain: PME#, SERR#, INTn#
R368 10K
R364 10K
R361 10K
R369 100K
R383 10K
R384 10K
R371 10K
C405 10P_* C406 10P
Q105 2N7002_*
R374 100 CB_IDSEL_J
R375 10K
C407 1UF/X7R
+3VS ==> CB_GBRST#
1ms < T < 100ms
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
CB_HWSUSP# D18 1SS355 CB_SD# 22
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title
PCI CardReader,1394(R5C832)
Size Custom
Document Number A8J/F
Rev 1.1
Date: Thursday, October 06, 2005
Sheet 33 of 63







+3V
+12V
+3V
+12V
28,30,31,32,37,38,42,54,61
37,61

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: **4 IN 1 CONN**

Size: Custom | Document Number: **A8J/F** | Rev: 1.1

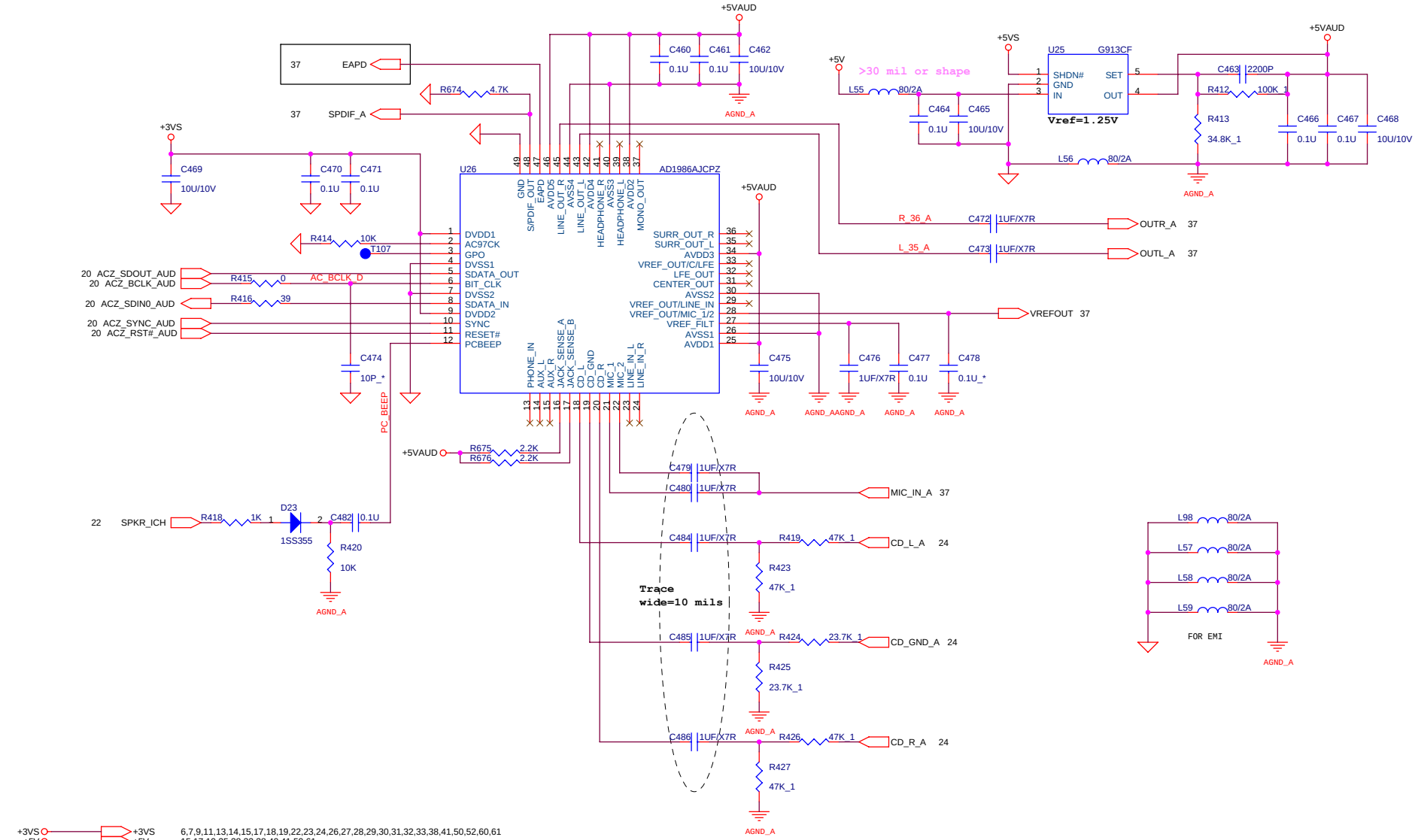
Date: Thursday, October 06, 2005 | Sheet 34 of 63

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: **Empty**

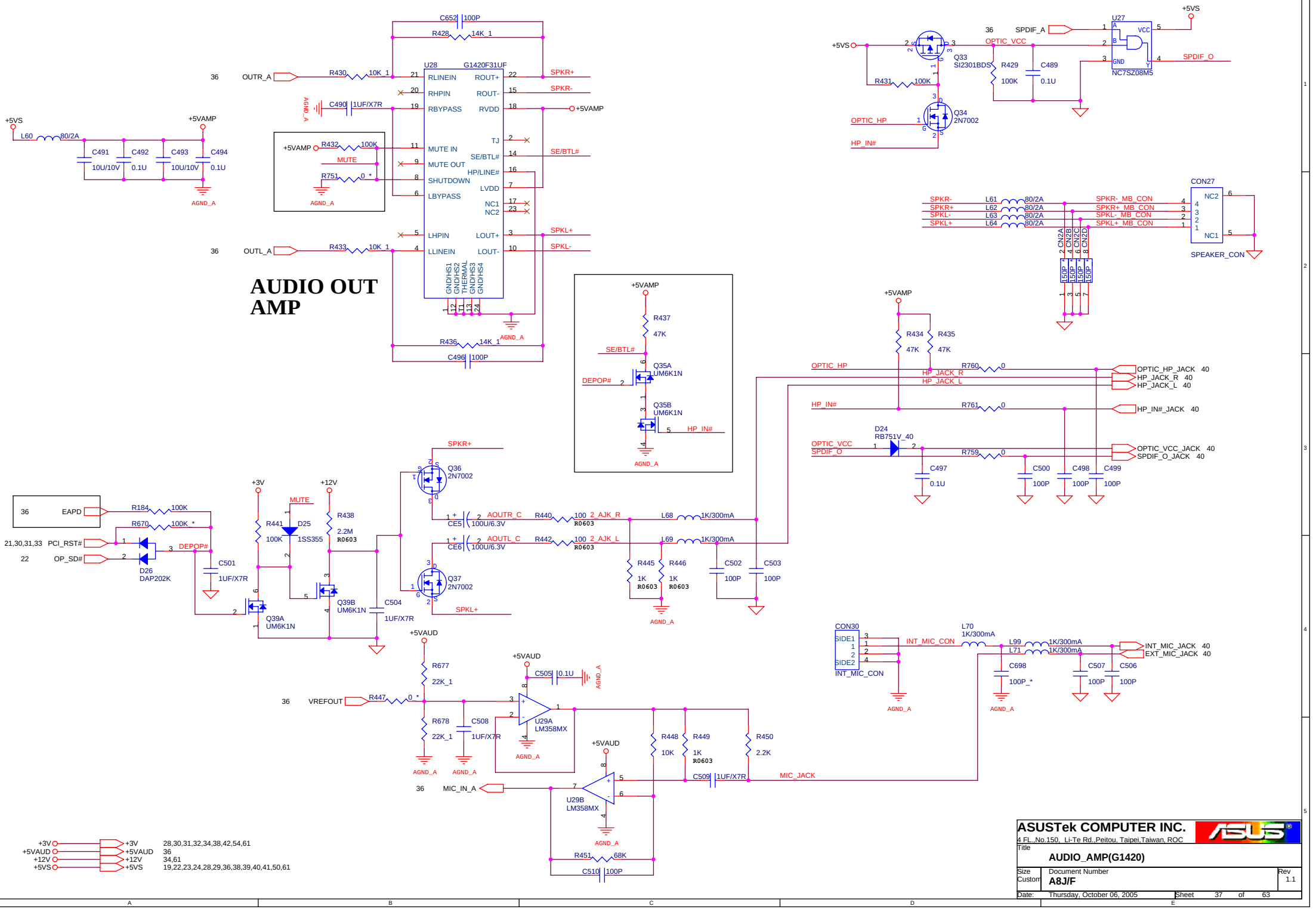
Size: Custom | Document Number: **A8J/F** | Rev: 1.1

Date: Thursday, October 06, 2005 | Sheet 35 of 63



ASUSTek COMPUTER INC.	
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC	
Title	ADI1986A
Size: Custom	Document Number: A8J/F
Rev	1.1
Date: Thursday, October 06, 2005	Sheet 36 of 63

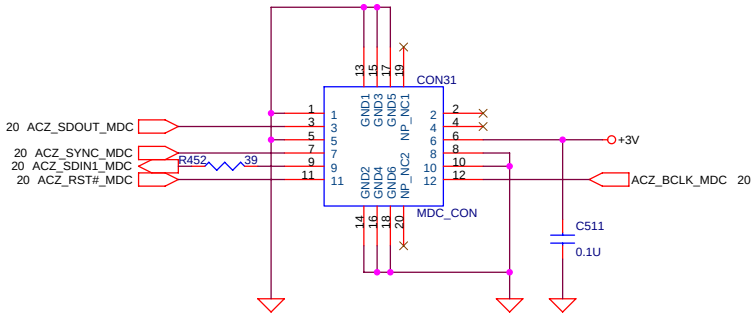
AUDIO OUT AMP



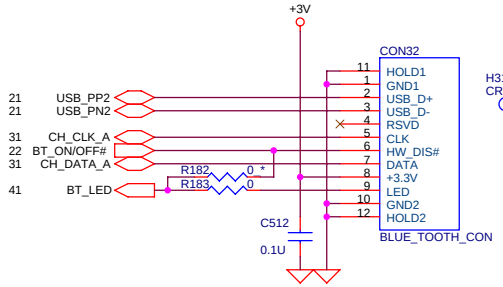
+3V	+3V	28,30,31,32,34,38,42,54,61
+5VAUD	+5VAUD	36
+12V	+12V	34,61
+5VS	+5VS	19,22,23,24,28,29,36,38,39,40,41,50,61

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

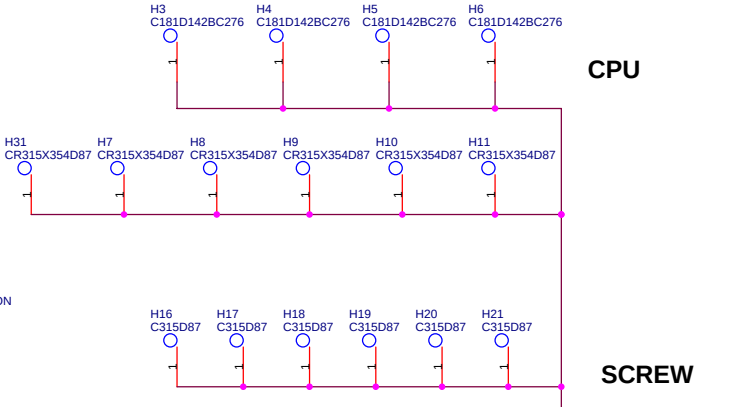
Title	AUDIO_AMP(G1420)	
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 37 of 63	

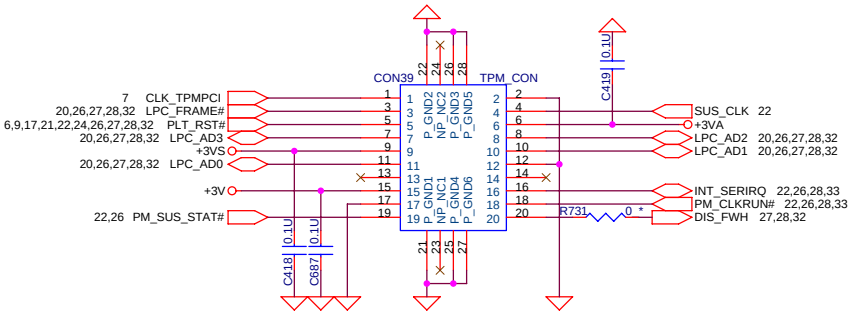


Azalia MDC MODEM CON

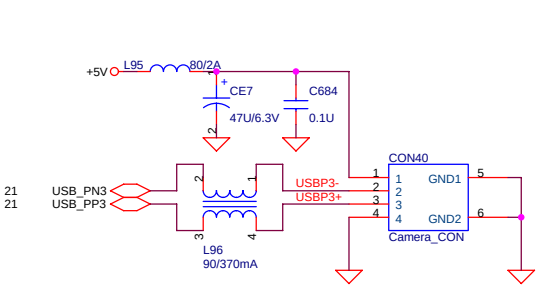


Bluetooth Module CON

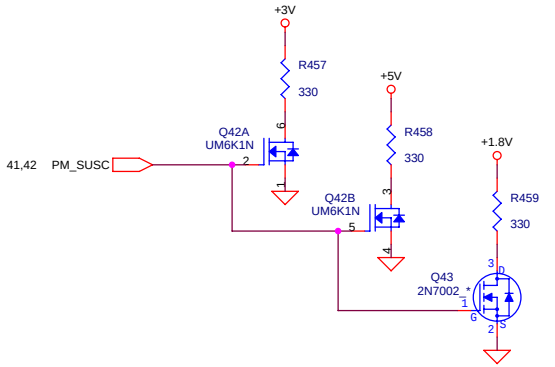


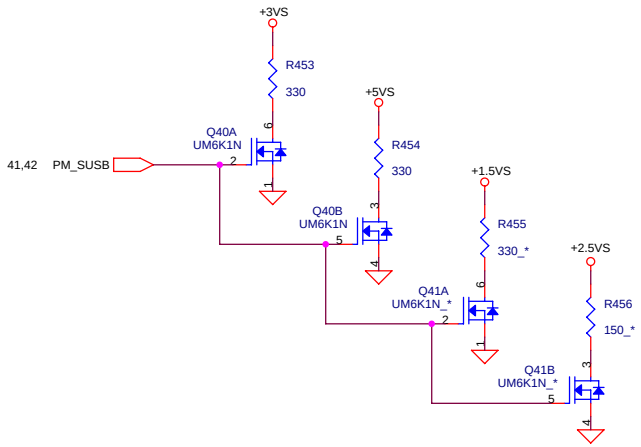


TPM Module CON



Camera Module CON





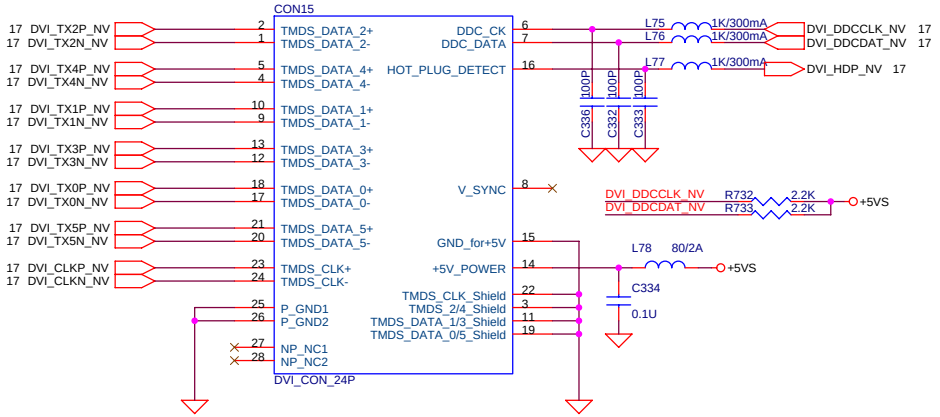
+1.5VS	+1.5VS	5,9,11,12,17,23,31,32,52
+1.8V	+1.8V	9,12,14,15,53
+2.5VS	+2.5VS	11,17,19,54
+3V	+3V	28,30,31,32,34,37,42,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,41,50,52,60,61
+5V	+5V	15,17,19,25,28,32,36,40,41,59,61
+5VS	+5VS	19,22,23,24,28,29,36,37,39,40,41,50,61

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: MDC,B/T,TPM,Camera & DISCHG,HOLE

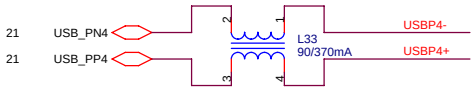
Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 38 of 63



+5VS +5VS 19,22,23,24,28,29,36,37,38,40,41,50,61

ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: DVI CONN		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 39 of 63	



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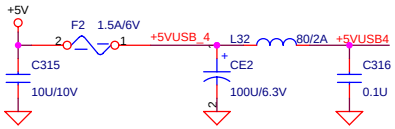
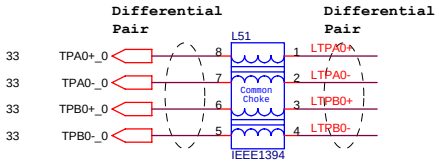
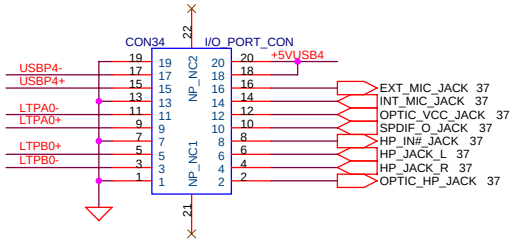
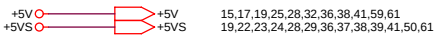
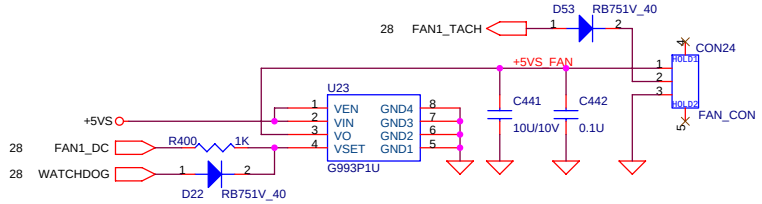




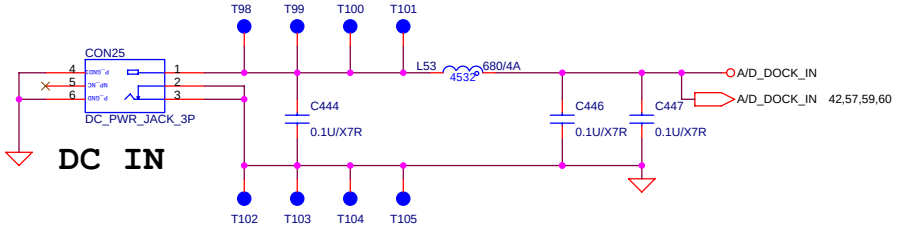


I/O PORT



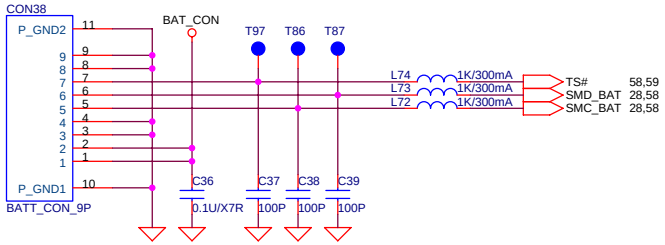


FAN CONTROL



DC IN

ACIN_CONN



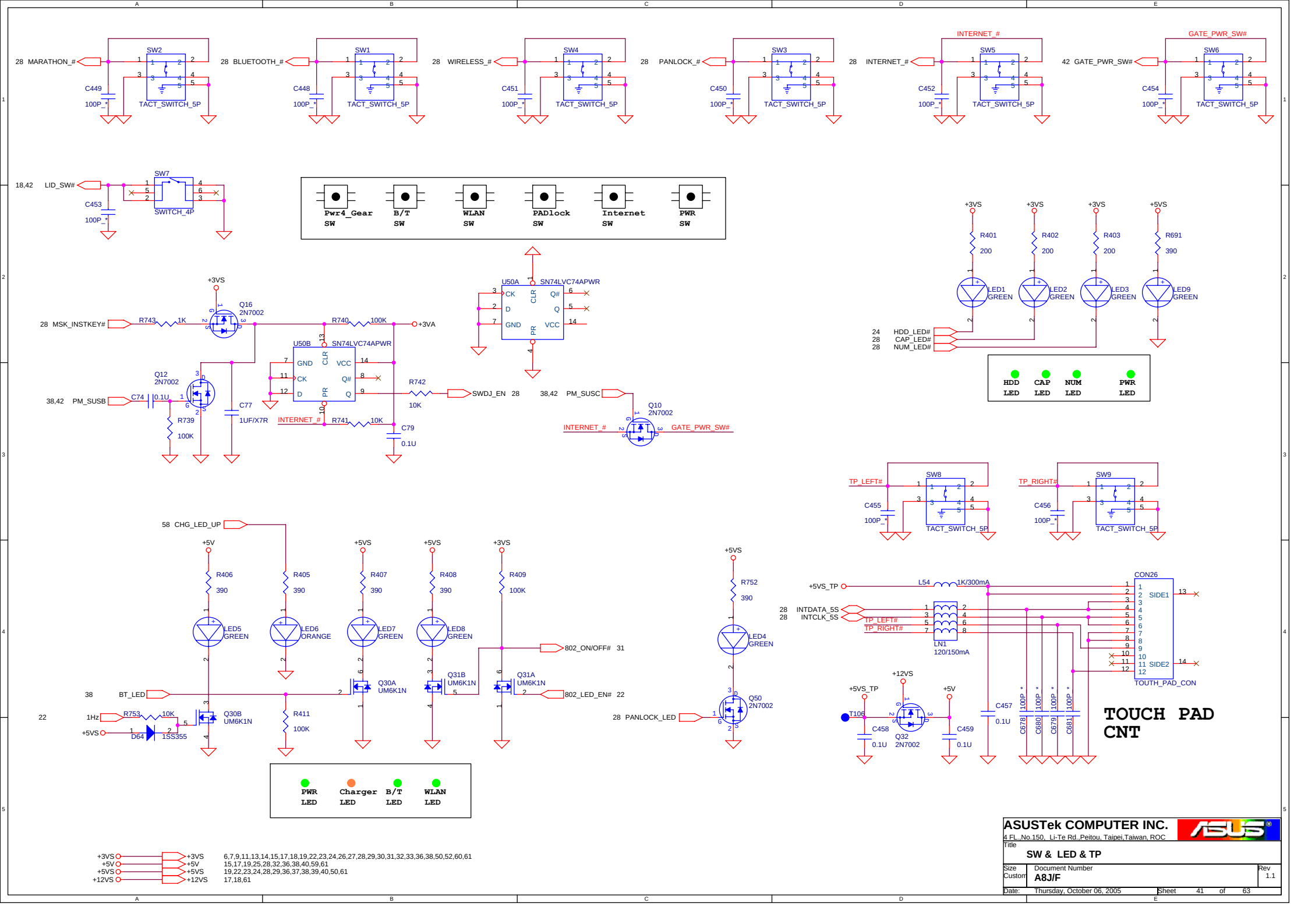
BAT_CONN

ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: FAN_CTRL & ACIN & BAT & I/O PORT

Size: Custom | Document Number: A8J/F | Rev: 1.1

Date: Thursday, October 06, 2005 | Sheet 40 of 63

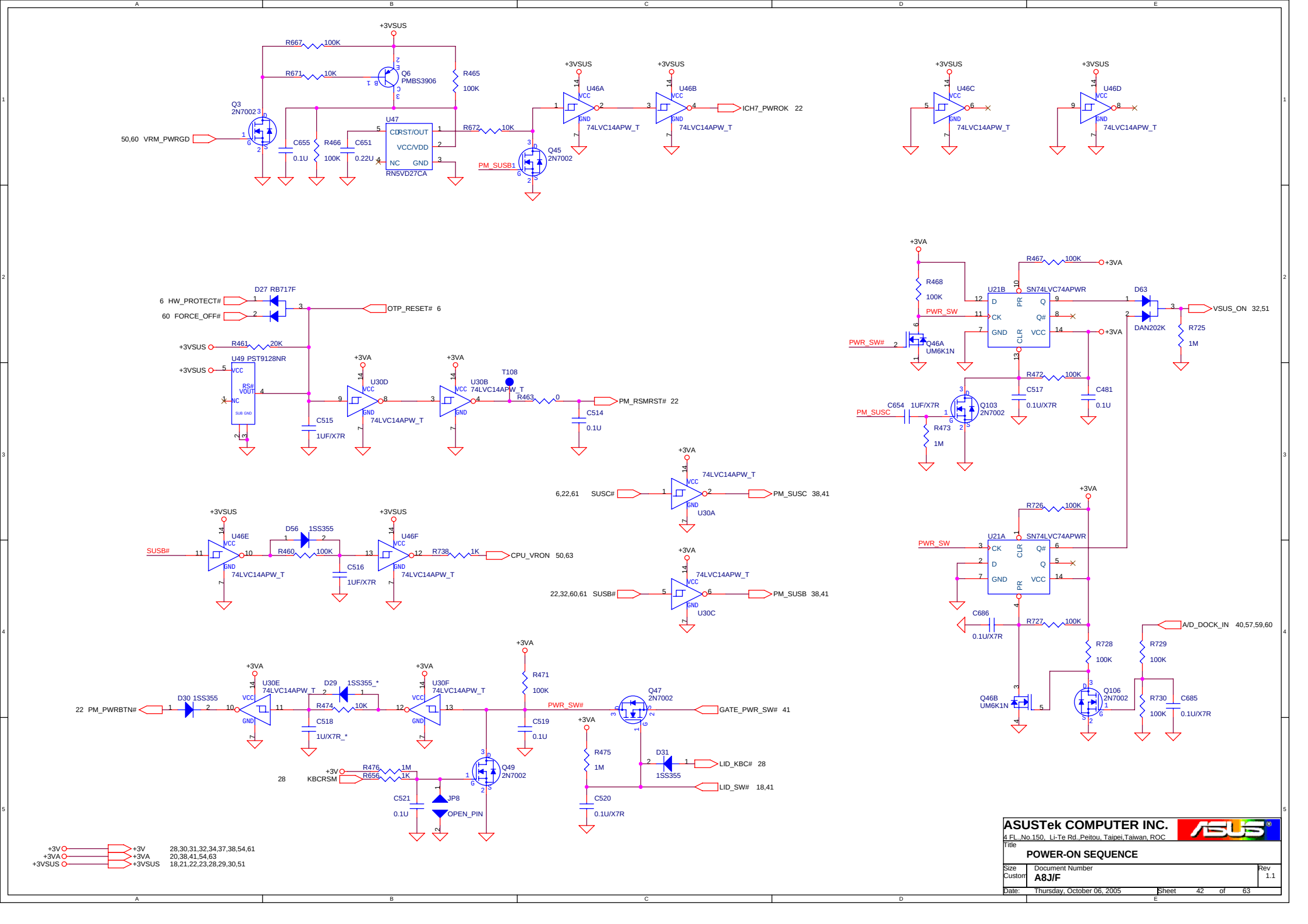


ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: SW & LED & TP

Size	Document Number	Rev
Custom	A8J/F	1.1

Date: Thursday, October 06, 2005 Sheet 41 of 63



ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title	POWER-ON SEQUENCE	
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 42 of 63	

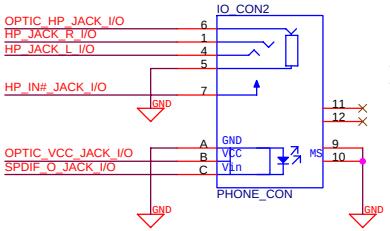
Revision History

Power:

System:

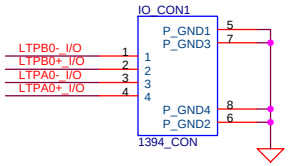
ASUSTek COMPUTER INC.
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

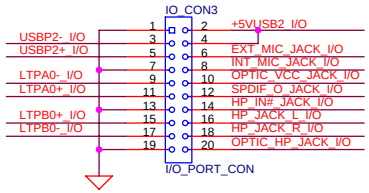
Title: HISTORY		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 43 of 63	

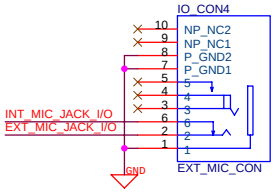


LINE_OUT SPDIF

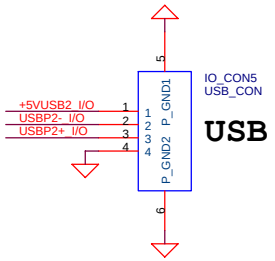
1394A



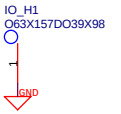


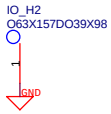


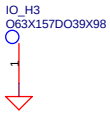
MIC

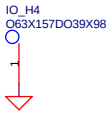


USB

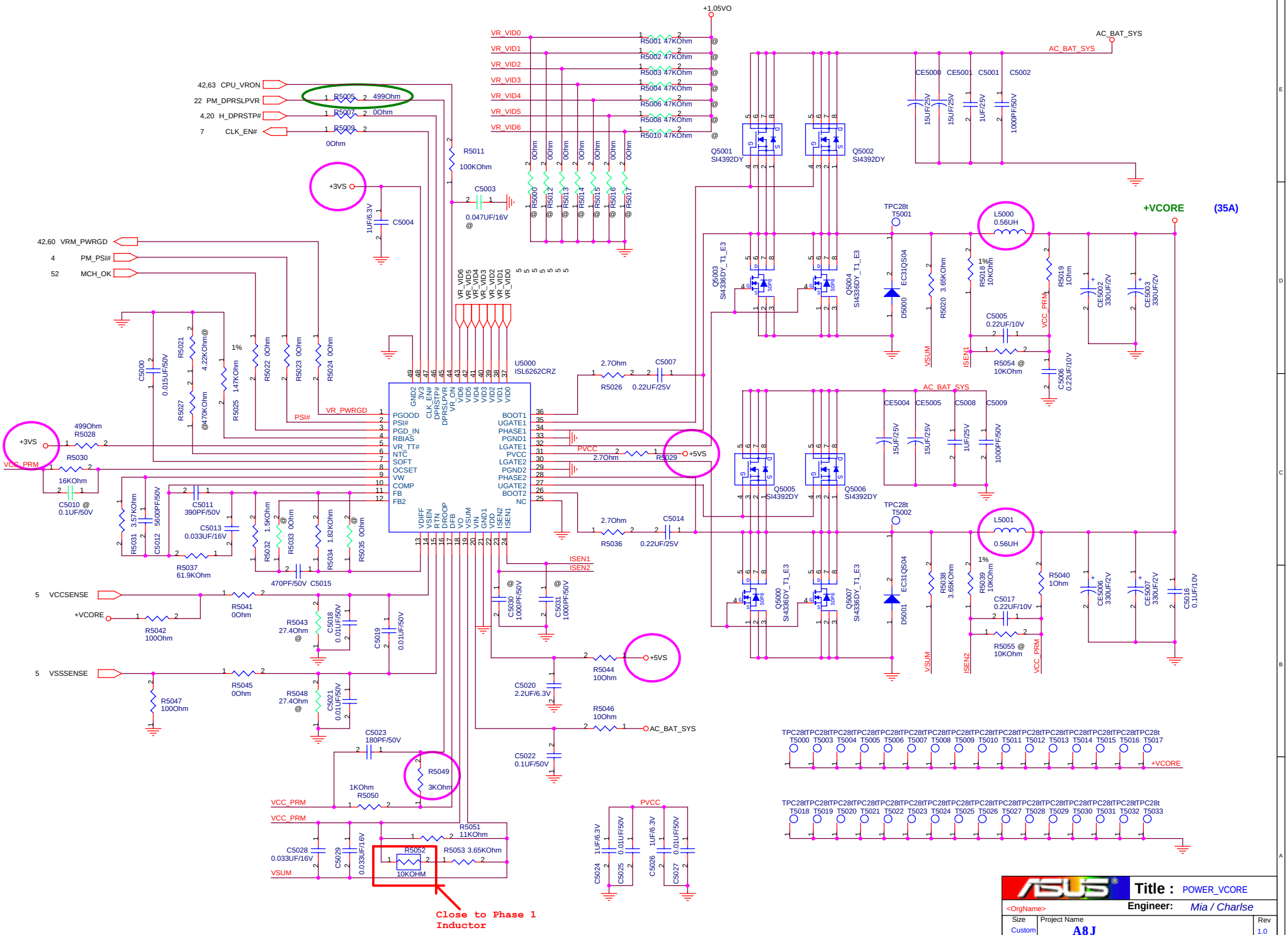




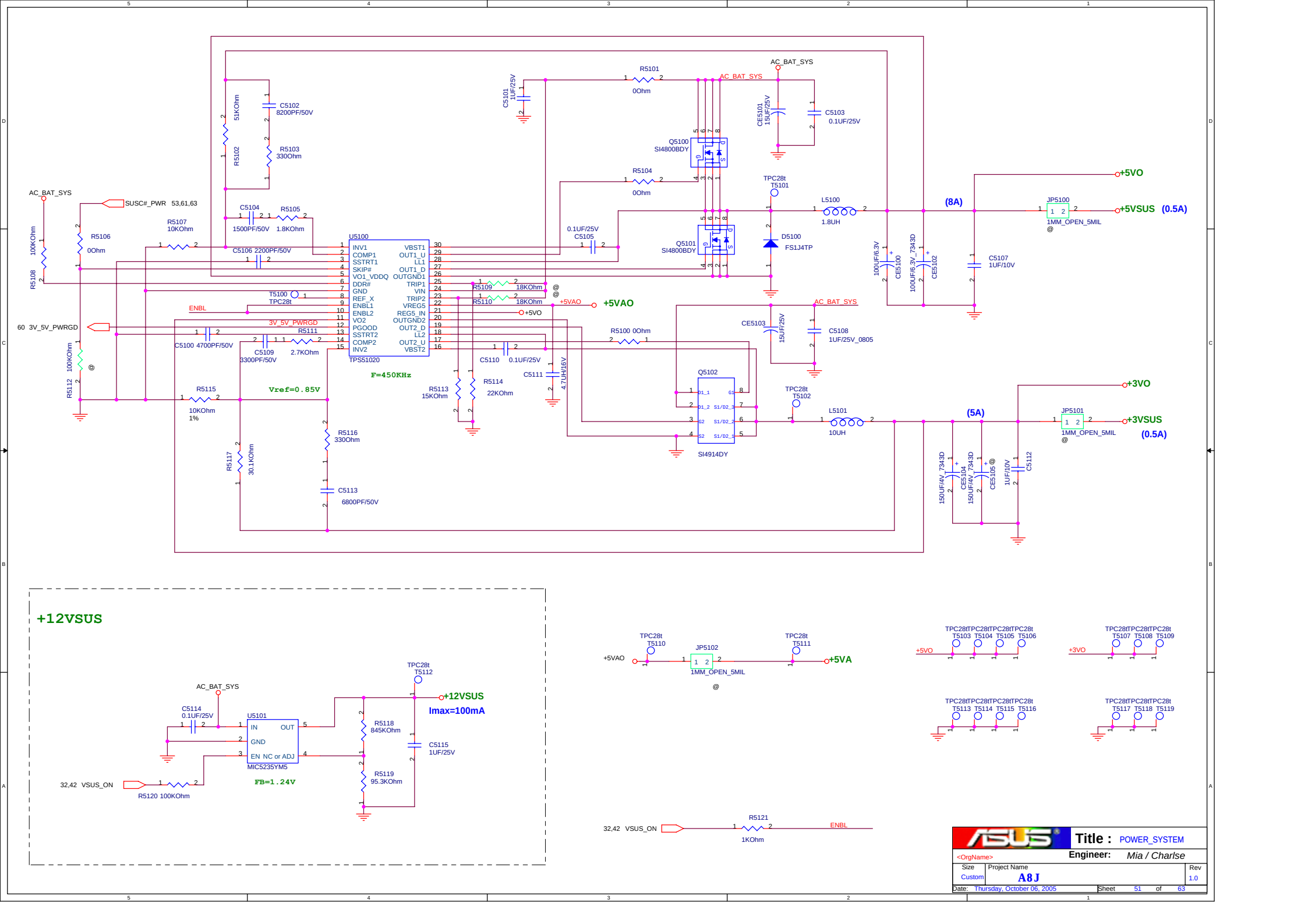




ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: I/O PORT		
Size: Custom	Document Number: A8J/F	Rev: 1.1
Date: Thursday, October 06, 2005	Sheet 44 of 63	



Title : POWER_VCORE			
<OrgName>	Engineer: Mia / Charlse		
Size: Custom	Project Name: A8J		Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 50 of 63		



ASUS

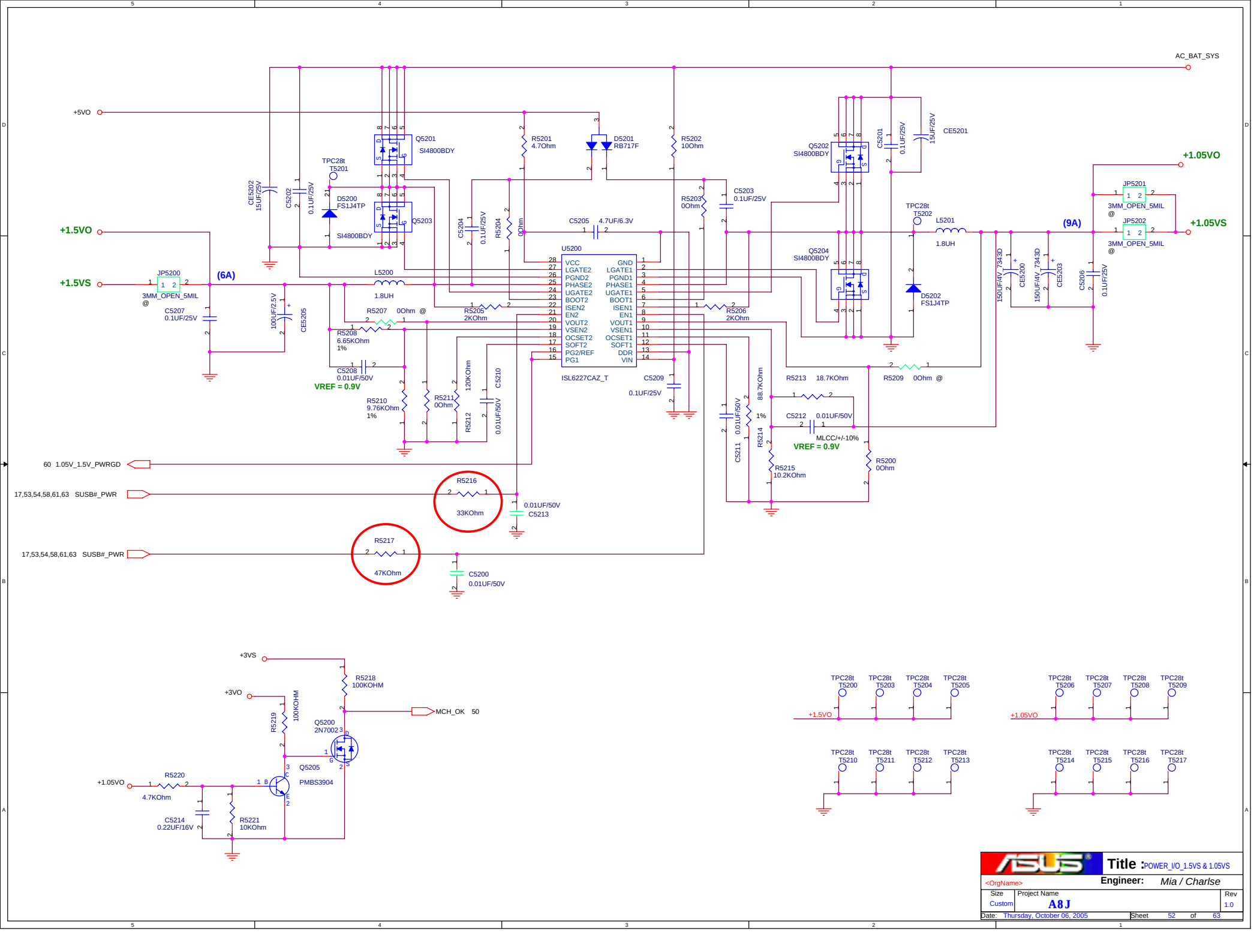
Title : POWER_SYSTEM

<OrgName>

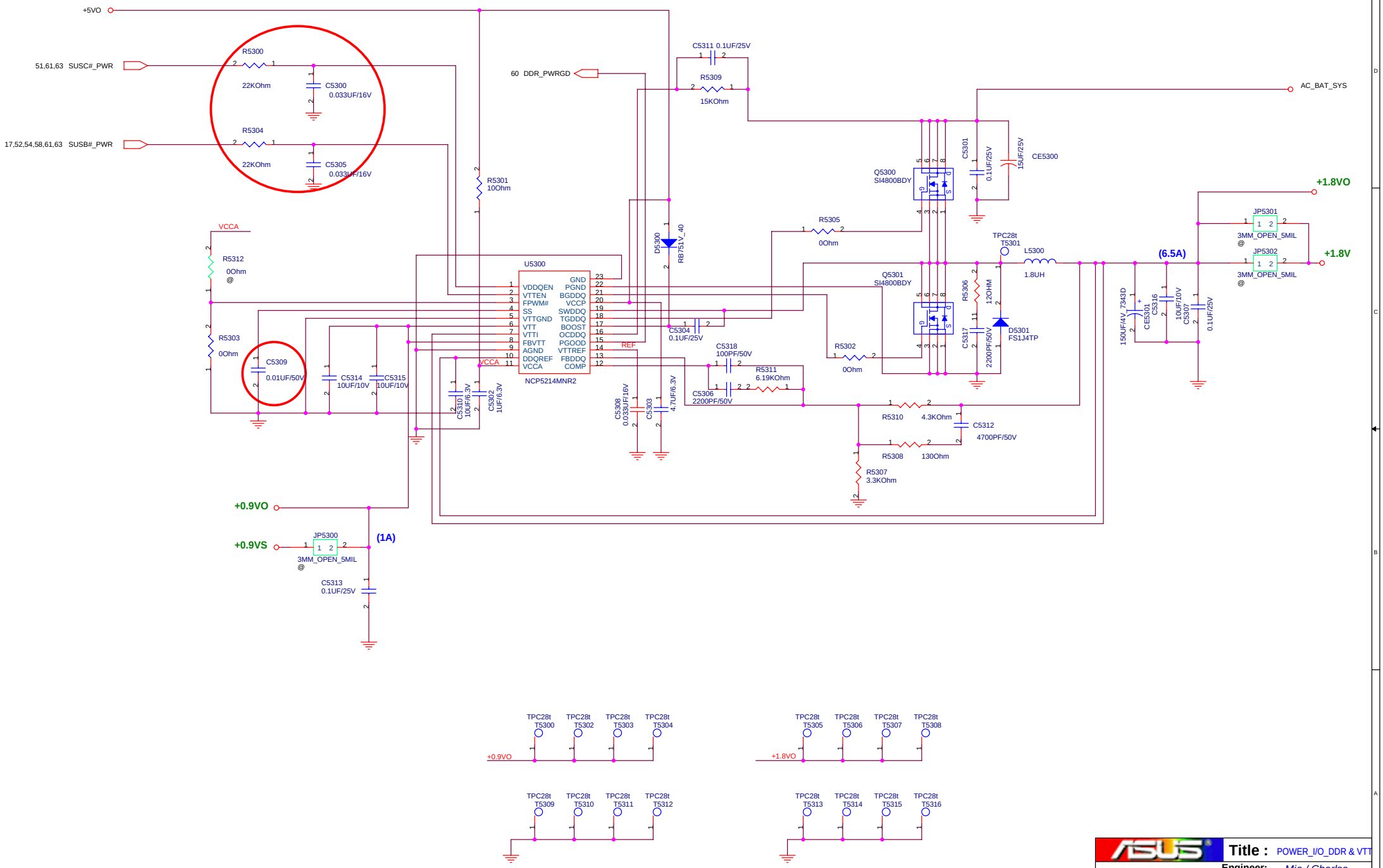
Engineer: *Mia / Charlse*

Size	Project Name	Rev
Custom	A8J	1.0

Date: Thursday, October 06, 2005 Sheet 51 of 63

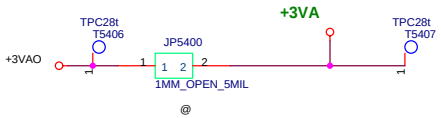


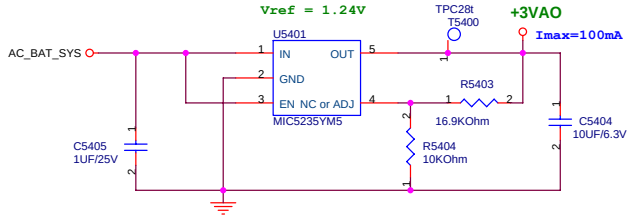
Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 52 of 63	



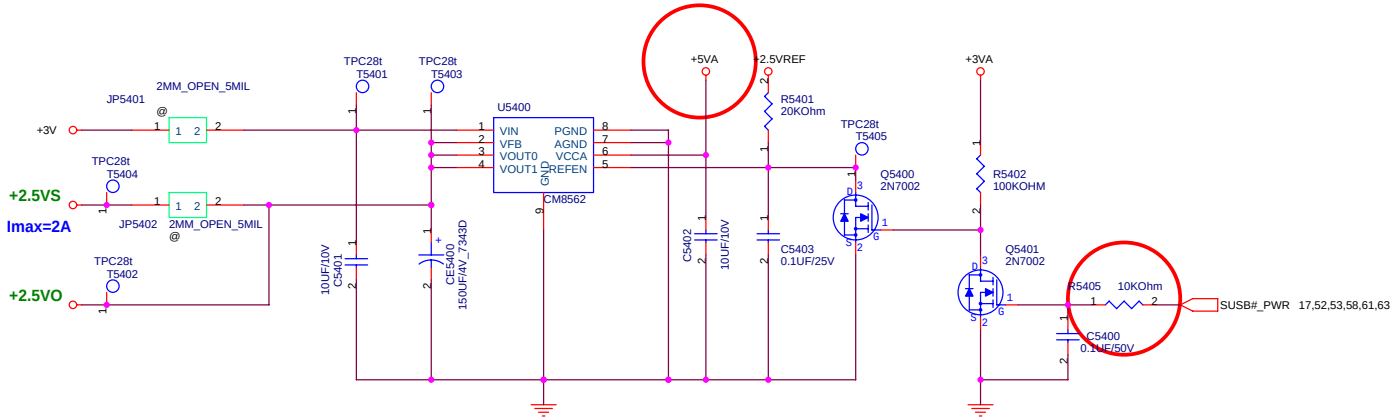
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 53 of 63	

+3VAO





+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 54 of 63	

Title :	POWER_VGA_CORE
<OrgName>	Engineer: Mia / Charlse
Size: Custom	Project Name: A8J
Rev: 2.1	
Date: Thursday, October 06, 2005	Sheet 55 of 63

Title :	POWER_VGA_RAM
<OrgName>	Engineer: Mia / Charlse
Size: Custom	Project Name: A8J
Rev: 1.0	
Date: Thursday, October 06, 2005	Sheet 56 of 63

TOTAL POWER=65W
-->3.42A

BATSEL_2P# = "H" (1P)			
BAT cpapcity	R5712	VICTL(V)	ICHG(A)
2000mAH	41.2K	1.8976	1.39
2200mAH	52.3K	2.0989	1.537
2400mAH	66.5K	2.2918	1.679
2600mAH	86.6K	2.4871	1.822

Vref = 4.096V
VLDO = 5.4V

Vbatt = Cell * { 4V +[0.4 X (VCTL/REFIN)] }
VCTL= LDO
=> Vbatt = 4.2V X CELLS

VICTL= 3V

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG)=0.025 ohm
VICTL= 3.4632V => Ichg = 2.53A

RES\NB	Vrefin=3V A8F(65W)	Vrefin=3.5V A8J(90W)
R5721	47K	47K
R5723	15K	18K
R5737	15K	4.7K
R5738	33K	33K
R5716	18K	10K
R5718	15K	23.7K

CHG_EN#	AC_APR_UC	SWITCH
H	H	OFF
H	L	ON
L	H	ON
L	L	ON

CELL pin : (trie to REFIN pin) ----> 4 Cells
(floating) ----> 3 Cells

Check 3720 package enough?

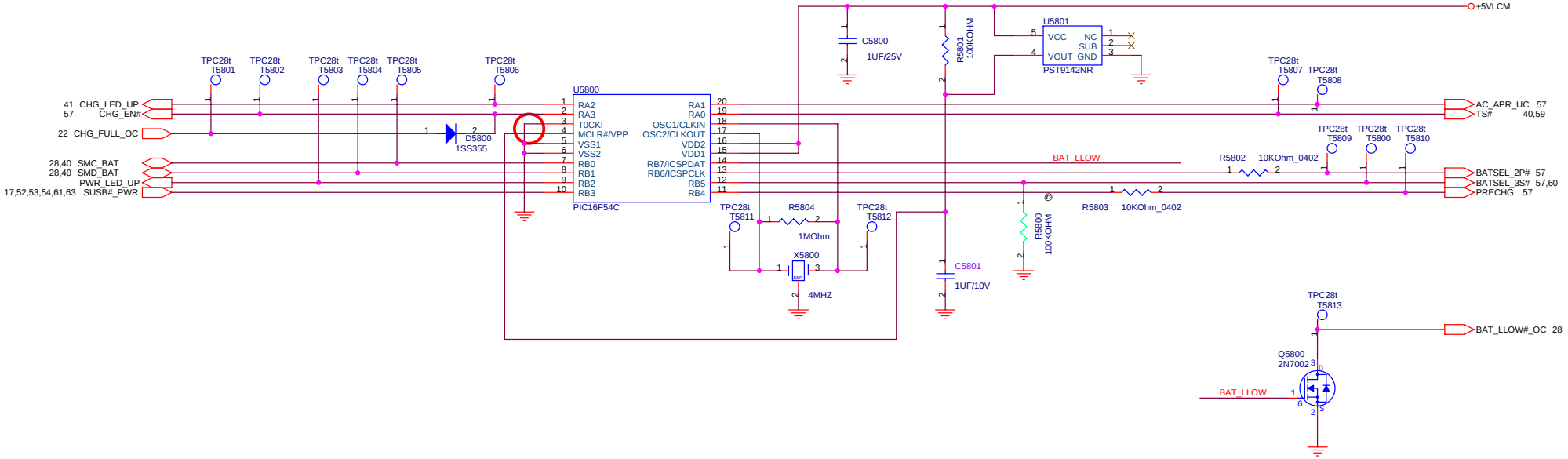
PRE_CHARGE CIRCUIT

Pre-charge voltage 10V@3S
Pre-charge voltage 13.04V@4S

DETECT CIRCUIT (BATT <8.025V@3S)
DETECT CIRCUIT (BATT <10.98V@4S)

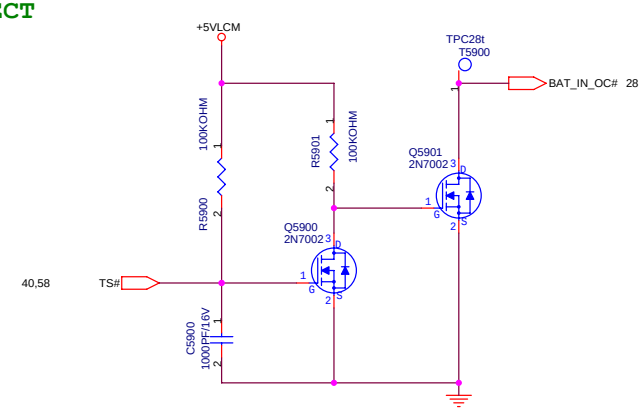
Title :	POWER_CHARGER		
<OrgName>	Engineer:	Mia / Charlse	
Size: C	Project Name: A8J		Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 57 of 63		

PIC16F54C

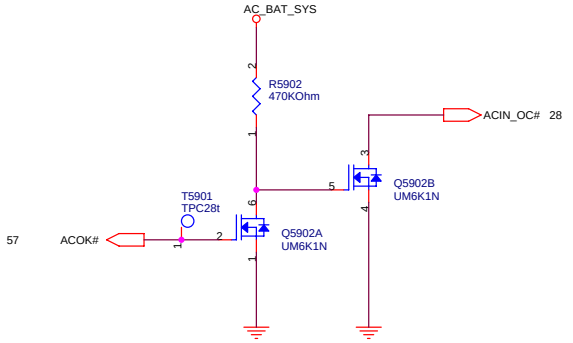


ASUS	Title : POWER_PIC	
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 58 of 63	

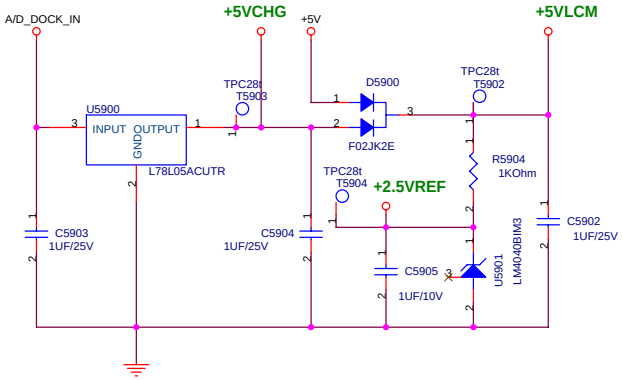
BATTERY IN DETECT



ADAPTER IN DETECT

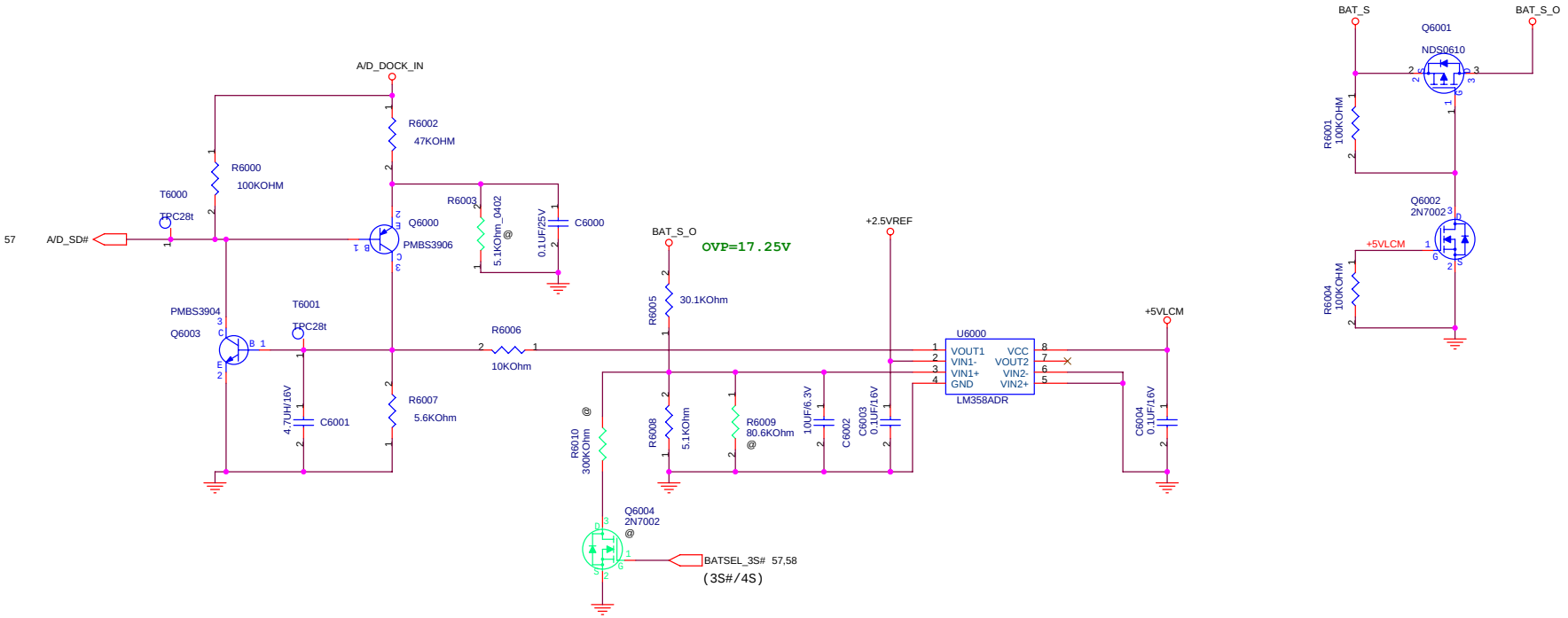


+5VLCM, +5VCHG & +2.5VREF

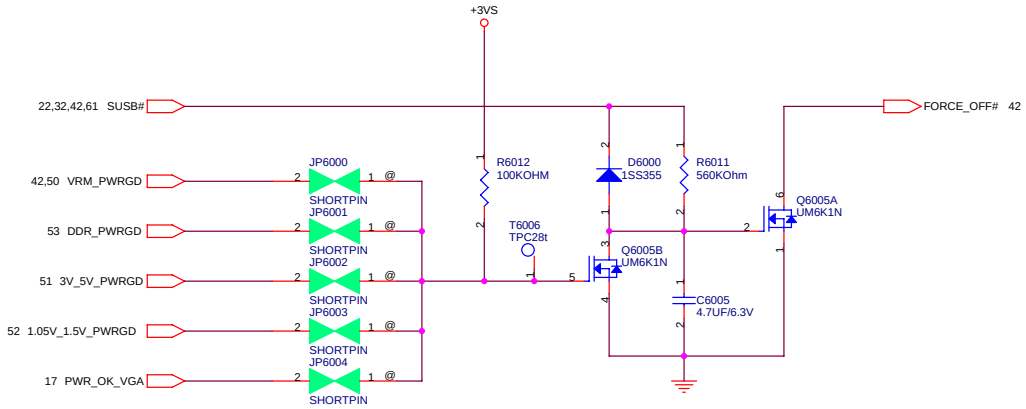


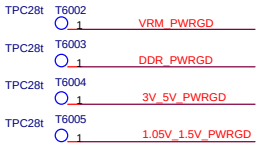
ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 59 of 63	

BATTERY A/D_SD# (OVP)



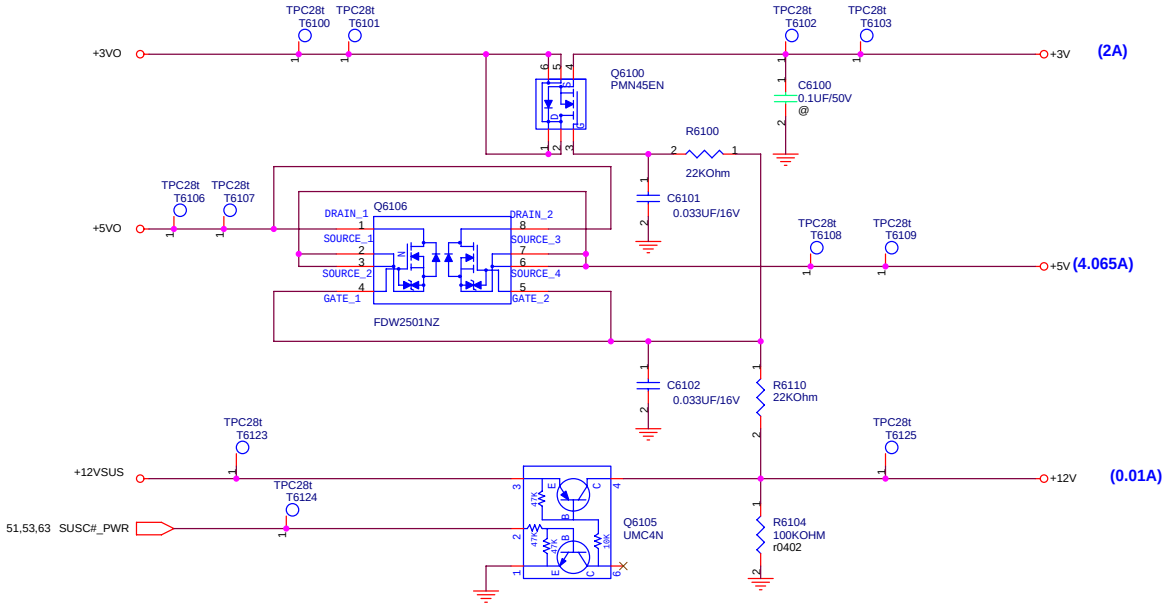
POWER GOOD DETECTER

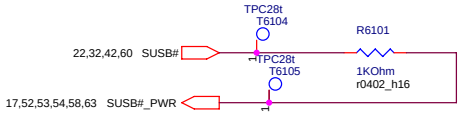




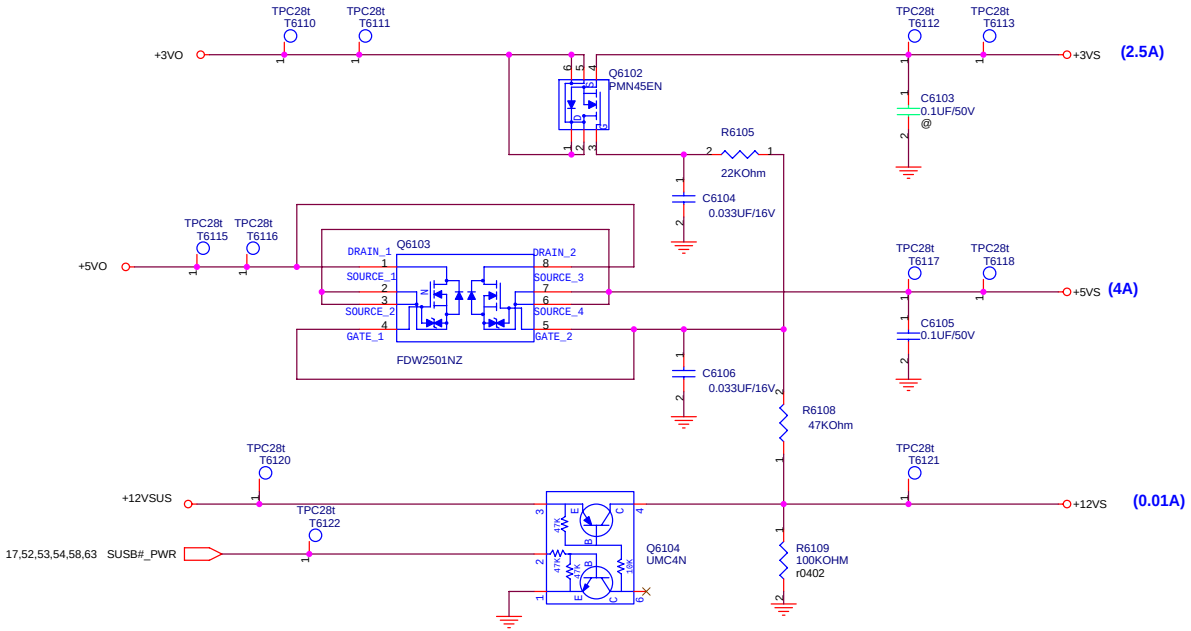
Title : POWER_PROTECT		
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 60 of 63	

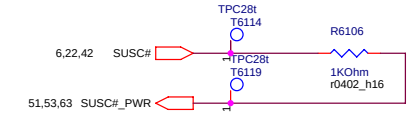
SUSC#_PWR POWER

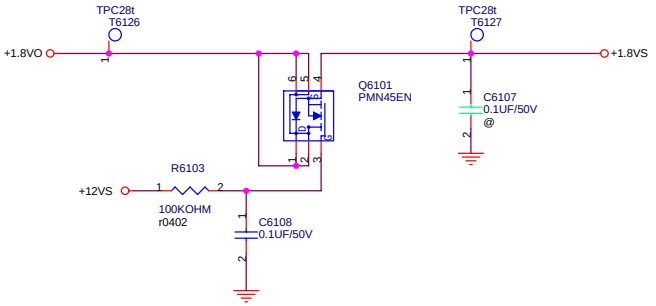




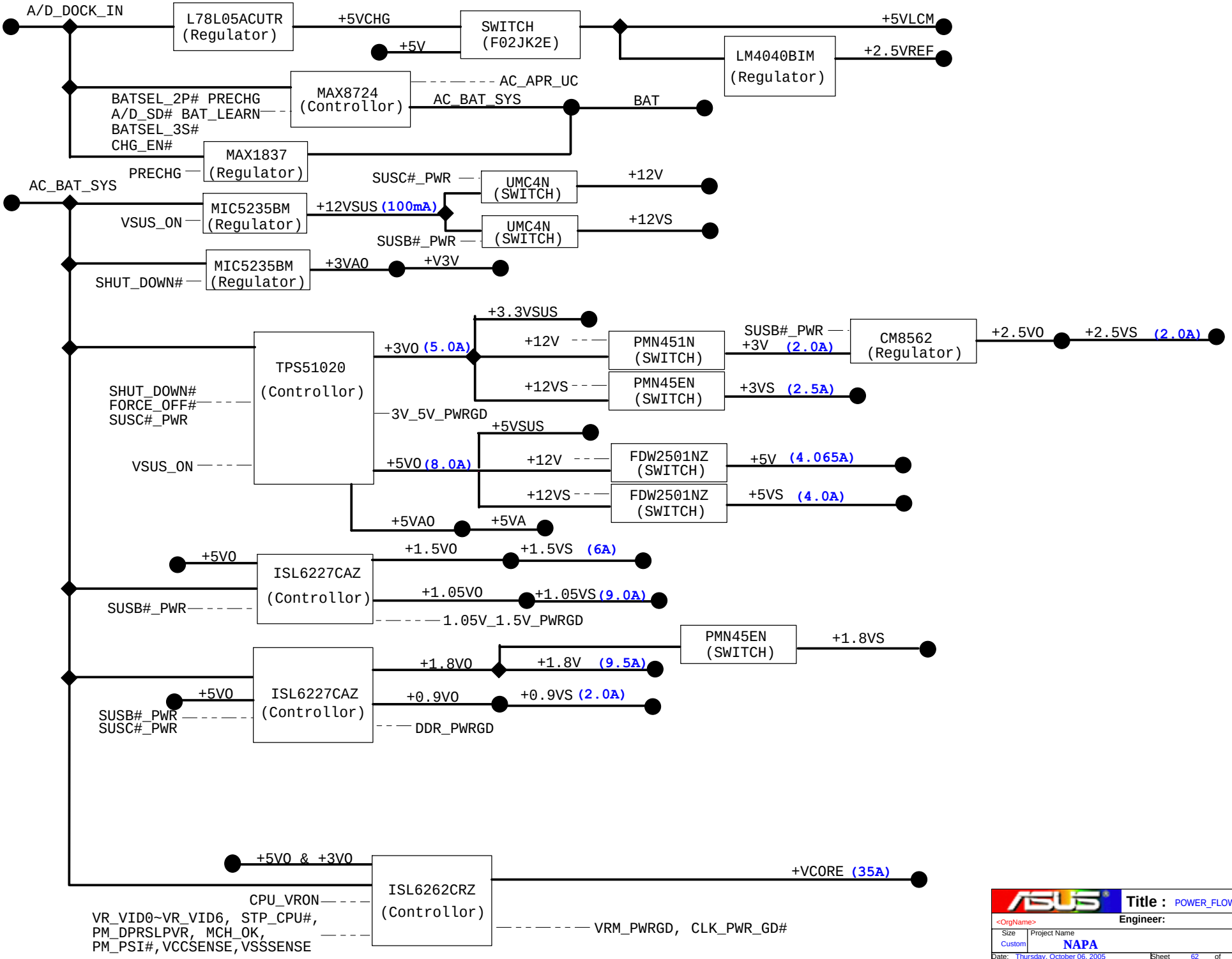
SUSB#_PWR POWER





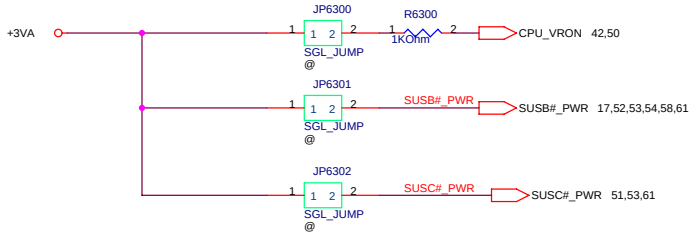


Title : POWER_LOAD SWITCH		
<OrgName>	Engineer: Mia / Charlse	
Size: Custom	Project Name: A8J	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 61 of 63	



ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 62 of 63	

FOR POWER TEST



Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: NAPA	Rev: 1.0
Date: Thursday, October 06, 2005	Sheet 63 of 63	