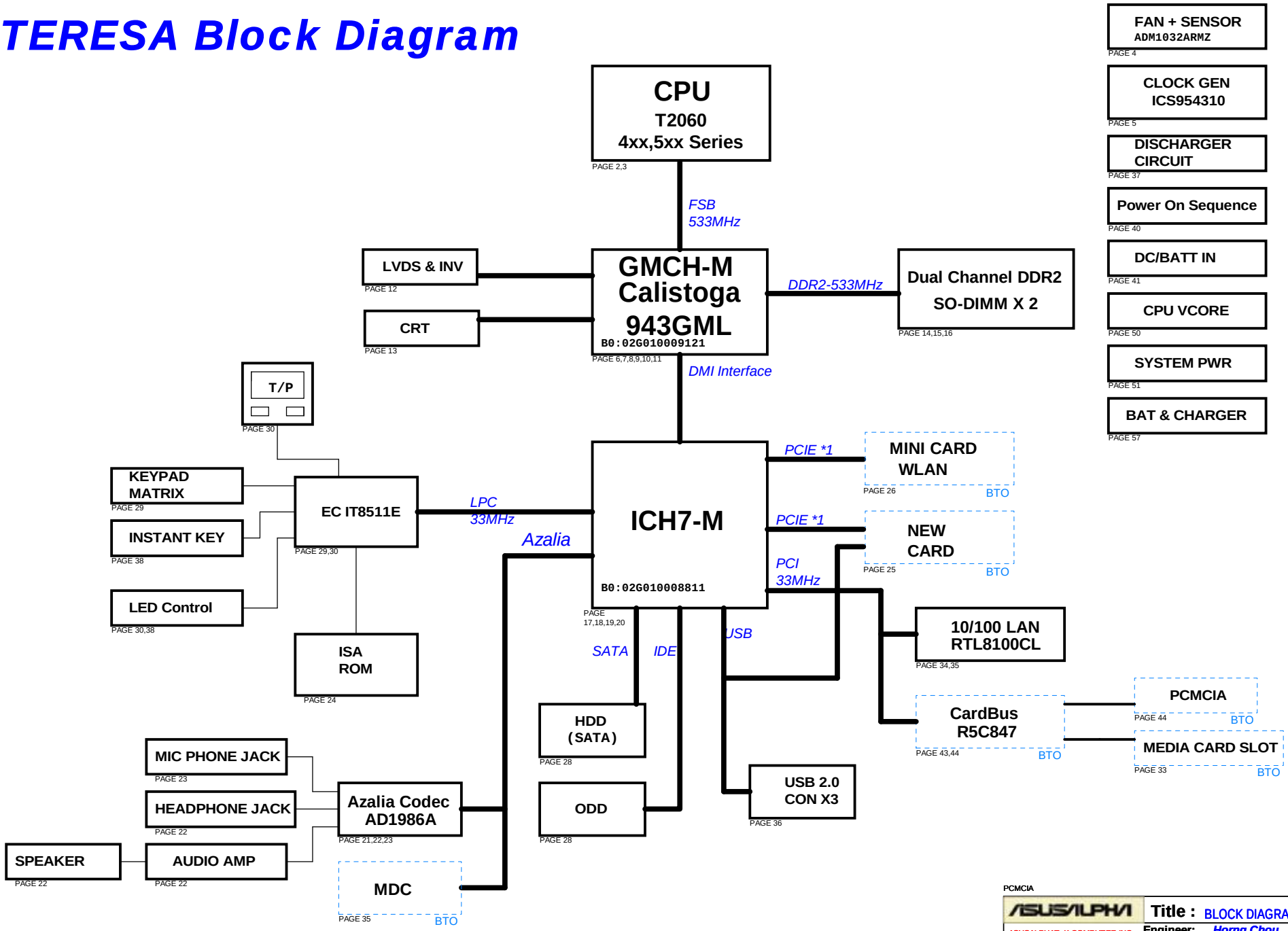
TERESA Block Diagram



PCMCIA

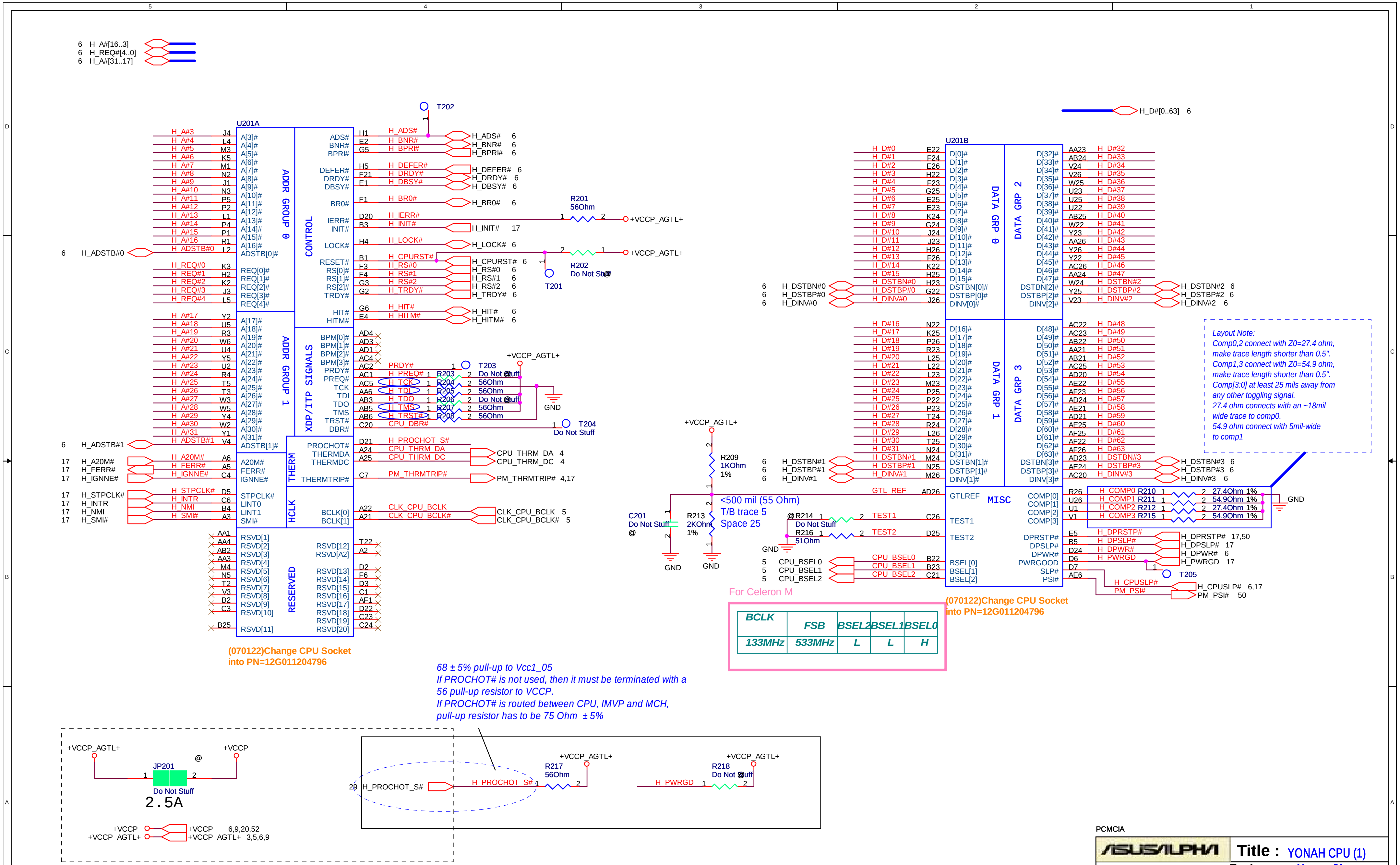
ASUSALPHA

Title : BLOCK DIAGRAM

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 1 of 57



Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

BCLK	FSB	BSEL2	BSEL1	BSEL0
133MHz	533MHz	L	L	H

(070122)Change CPU Socket into PN=12G011204796

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

PCMCIA

ASUSALPHATeK COMPUTER INC.

Title : YONAH CPU (1)

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 2 of 57

Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCC	1.0V	1.2V	1.3V
	C3	C2	C0
ICC	14.7A	16.5A	29Ah

Celeron M FSB:533MHz			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
	MIN	TYP	MAX
ICCP			2.5A

Modity Table for Celeron M

+VCORE +VCORE

U201C

VCC[1] A7, VCC[2] A9, VCC[3] A10, VCC[4] A12, VCC[5] A13, VCC[6] A15, VCC[7] A17, VCC[8] A18, VCC[9] A20, VCC[10] B7, VCC[11] B9, VCC[12] B10, VCC[13] B12, VCC[14] B14, VCC[15] B15, VCC[16] B17, VCC[17] B18, VCC[18] B20, VCC[19] C9, VCC[20] C10, VCC[21] C12, VCC[22] C13, VCC[23] C15, VCC[24] C17, VCC[25] C18, VCC[26] D9, VCC[27] D10, VCC[28] D12, VCC[29] D14, VCC[30] D15, VCC[31] D17, VCC[32] D18, VCC[33] E7, VCC[34] E9, VCC[35] E10, VCC[36] E12, VCC[37] E13, VCC[38] E15, VCC[39] E17, VCC[40] E18, VCC[41] E20, VCC[42] F7, VCC[43] F9, VCC[44] F10, VCC[45] F12, VCC[46] F14, VCC[47] F15, VCC[48] F17, VCC[49] F18, VCC[50] F20, VCC[51] AA7, VCC[52] AA9, VCC[53] AA10, VCC[54] AA12, VCC[55] AA13, VCC[56] AA15, VCC[57] AA17, VCC[58] AA18, VCC[59] AA20, VCC[60] AB9, VCC[61] AC10, VCC[62] AB10, VCC[63] AB12, VCC[64] AB14, VCC[65] AB15, VCC[66] AB17, VCC[67] AB18

VCC[68] AB20, VCC[69] AB7, VCC[70] AC7, VCC[71] AC9, VCC[72] AC12, VCC[73] AC13, VCC[74] AC15, VCC[75] AC17, VCC[76] AC18, VCC[77] AD7, VCC[78] AD9, VCC[79] AD10, VCC[80] AD12, VCC[81] AD14, VCC[82] AD15, VCC[83] AD17, VCC[84] AD18, VCC[85] AE9, VCC[86] AE10, VCC[87] AE12, VCC[88] AE13, VCC[89] AE15, VCC[90] AE17, VCC[91] AE18, VCC[92] AE20, VCC[93] AF9, VCC[94] AF10, VCC[95] AF12, VCC[96] AF14, VCC[97] AF15, VCC[98] AF17, VCC[99] AF18, VCC[100] AF20

VCCP[1] V6, VCCP[2] G21, VCCP[3] J6, VCCP[4] K6, VCCP[5] M6, VCCP[6] J21, VCCP[7] K21, VCCP[8] M21, VCCP[9] N21, VCCP[10] N6, VCCP[11] R21, VCCP[12] R6, VCCP[13] T21, VCCP[14] T6, VCCP[15] V21, VCCP[16] W21

VCCA B26

VID[0] AD6, VID[1] AF5, VID[2] AE5, VID[3] AF4, VID[4] AE3, VID[5] AF2, VID[6] AE2

VCCSENSE AF7, VSSSENSE AE7

+VCCA JP301 +1.5VO

JP301: 1 2 — Do Not Stuff — @

+VCCP_AGTL+ RN303D 7 0Ohm 8

+VCCA 120mA / 20mil Close to Pin B26

C301 10UF/10V C318 0.01UF/25V

GND checklist suggests 10uF POSCAP

H_VID0	1	0Ohm	2	RN302A
H_VID1	3	0Ohm	4	RN302B
H_VID2	5	0Ohm	6	RN302C
H_VID3	7	0Ohm	8	RN302D
H_VID4	1	0Ohm	2	RN303A
H_VID5	3	0Ohm	4	RN303B
H_VID6	5	0Ohm	6	RN303C

VR_VID0 50, VR_VID1 50, VR_VID2 50, VR_VID3 50, VR_VID4 50, VR_VID5 50, VR_VID6 50

R301 1 2 100Ohm +VCORE

VCCSENSE 50, VSSSENSE 50

R302 100Ohm GND

(070122)Change CPU Socket into PN=12G011204796

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

U201D

VSS[1] A4, VSS[2] A8, VSS[3] A11, VSS[4] A14, VSS[5] A16, VSS[6] A19, VSS[7] A23, VSS[8] A26, VSS[9] B6, VSS[10] B8, VSS[11] B11, VSS[12] B13, VSS[13] B16, VSS[14] B19, VSS[15] B21, VSS[16] B24, VSS[17] C5, VSS[18] C8, VSS[19] C11, VSS[20] C14, VSS[21] C16, VSS[22] C19, VSS[23] C2, VSS[24] C22, VSS[25] C25, VSS[26] D1, VSS[27] D4, VSS[28] D8, VSS[29] D11, VSS[30] D13, VSS[31] D16, VSS[32] D19, VSS[33] D23, VSS[34] D26, VSS[35] E3, VSS[36] E6, VSS[37] E8, VSS[38] E11, VSS[39] E14, VSS[40] E16, VSS[41] E19, VSS[42] E21, VSS[43] E24, VSS[44] F5, VSS[45] F8, VSS[46] F11, VSS[47] F13, VSS[48] F16, VSS[49] F19, VSS[50] F2, VSS[51] F22, VSS[52] F25, VSS[53] G4, VSS[54] G1, VSS[55] G23, VSS[56] G26, VSS[57] H3, VSS[58] H6, VSS[59] H21, VSS[60] H24, VSS[61] J2, VSS[62] J5, VSS[63] J22, VSS[64] J25, VSS[65] K1, VSS[66] K4, VSS[67] K23, VSS[68] K26, VSS[69] L3, VSS[70] L6, VSS[71] L21, VSS[72] L24, VSS[73] M2, VSS[74] M5, VSS[75] M22, VSS[76] M25, VSS[77] N1, VSS[78] N4, VSS[79] N23, VSS[80] N26, VSS[81] P3

VSS[82] P6, VSS[83] P21, VSS[84] P24, VSS[85] R2, VSS[86] R5, VSS[87] R22, VSS[88] R25, VSS[89] T1, VSS[90] T4, VSS[91] T23, VSS[92] T26, VSS[93] U3, VSS[94] U6, VSS[95] U21, VSS[96] U24, VSS[97] V2, VSS[98] V5, VSS[99] V22, VSS[100] V25, VSS[101] W1, VSS[102] W4, VSS[103] W23, VSS[104] W26, VSS[105] Y3, VSS[106] Y6, VSS[107] Y21, VSS[108] Y24, VSS[109] AA2, VSS[110] AA5, VSS[111] AA8, VSS[112] AA11, VSS[113] AA14, VSS[114] AA16, VSS[115] AA19, VSS[116] AA22, VSS[117] AA25, VSS[118] AB1, VSS[119] AB4, VSS[120] AB8, VSS[121] AB11, VSS[122] AB13, VSS[123] AB16, VSS[124] AB19, VSS[125] AB23, VSS[126] AB26, VSS[127] AC3, VSS[128] AC6, VSS[129] AC8, VSS[130] AC11, VSS[131] AC14, VSS[132] AC16, VSS[133] AC19, VSS[134] AC21, VSS[135] AC24, VSS[136] AD2, VSS[137] AD5, VSS[138] AD8, VSS[139] AD11, VSS[140] AD13, VSS[141] AD16, VSS[142] AD19, VSS[143] AD22, VSS[144] AD25, VSS[145] AE1, VSS[146] AE4, VSS[147] AE8, VSS[148] AE11, VSS[149] AE14, VSS[150] AE16, VSS[151] AE19, VSS[152] AE23, VSS[153] AE26, VSS[154] AF3, VSS[155] AF6, VSS[156] AF8, VSS[157] AF11, VSS[158] AF13, VSS[159] AF16, VSS[160] AF19, VSS[161] AF21, VSS[162] AF24

GND GND

(070122)Change CPU Socket into PN=12G011204796

+VCCP_AGTL+ +VCCP_AGTL+ 2,5,6,9

+VCORE +VCORE 50

+1.5VS +1.5VS 7,9,10,20,25,26,37,52

+VCORE

CE301 Do Not Stuff @ — 1215---PWR comp Place the cap on North of Secondary side

GND

Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

(070131)Change 22UF into 10UF

Place these upper side inside socket cavity on L1

C302 C303 C304 C305 C306 C307 — 10UF/10V — GND

Place these lower side inside socket cavity on L1

C309 C311 C308 C310 C312 C313 — 10UF/10V — GND

Place these upper side inside socket cavity on L6

C314 C315 C316 C317 — 10UF/10V — GND

Place these lower side inside socket cavity on L6

C319 C320 C321 C322 — 10UF/10V — GND

(061228)Change into 10UF/10V PN:11G236322636360
C302,C303,C309,C311
C314,C315,C316,C317
C319,C320,C321,C322

+VCCP_AGTL+

+1.05V Decoupling Capacitor
Place near CPU

C323 C324 C325 C326 C327 C328 — c0402 — 0.1UF/10V

CE302 100UF/2.5

GND

(070205)Change P/N: 11G232310436320

PCMCIA

ASUSALPHA

Title : Yonah CPU (2)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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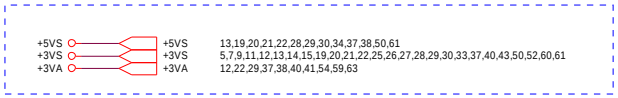
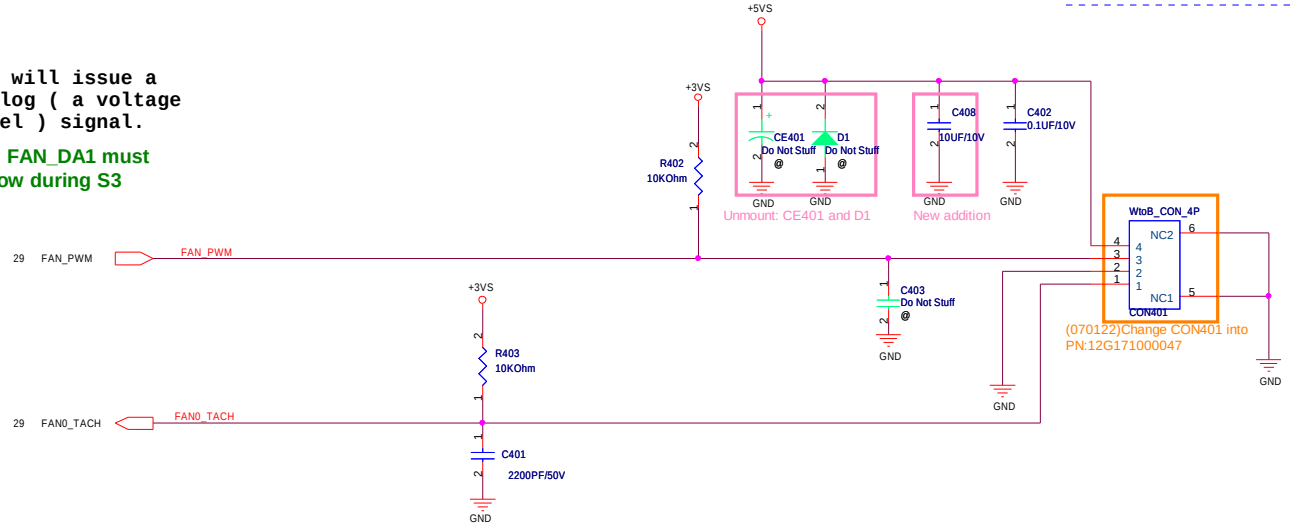
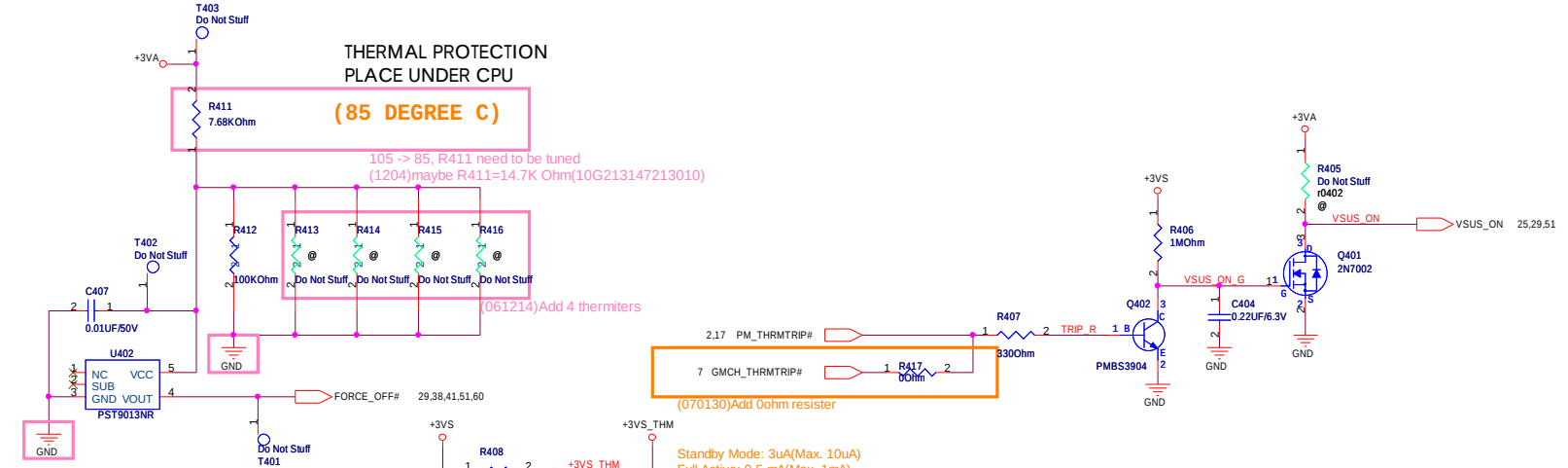
Fan Speed Control



KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3





Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

ASUSALPHA

Title : THER-SENSOR,FAN

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 4 of 57

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,6,9

+3VS — +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

(070130)Change C516 from 27PF to 33PF

Delete CLK_TPMPCI(connect to pin37

(070205) R533 Remove

Remove 0ohm

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519,Remove R550 R534

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

ICS954310CGLFT

Internal Pull-Up Resistor

Internal Pull-Down Resistor

PCMCIA

ASUSALPHATeK COMPUTER INC.

Title : CLOCK GEN

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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2 H_D#[0..63]

H_A#[31..3] 2

+VCCP +VCCP 2,9,20,52

+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,9

U601A

HOST

H_D#0	F1	H_D#_0	
H_D#1	J1	H_D#_1	
H_D#2	H1	H_D#_2	
H_D#3	J6	H_D#_3	
H_D#4	H3	H_D#_4	
H_D#5	K2	H_D#_5	
H_D#6	G1	H_D#_6	
H_D#7	G2	H_D#_7	
H_D#8	K9	H_D#_8	
H_D#9	K1	H_D#_9	
H_D#10	K7	H_D#_10	
H_D#11	J8	H_D#_11	
H_D#12	H4	H_D#_12	
H_D#13	J3	H_D#_13	
H_D#14	K11	H_D#_14	
H_D#15	G4	H_D#_15	
H_D#16	T10	H_D#_16	
H_D#17	W11	H_D#_17	
H_D#18	T3	H_D#_18	
H_D#19	U7	H_D#_19	
H_D#20	U9	H_D#_20	
H_D#21	U11	H_D#_21	
H_D#22	T11	H_D#_22	
H_D#23	W9	H_D#_23	
H_D#24	T1	H_D#_24	
H_D#25	T8	H_D#_25	
H_D#26	T4	H_D#_26	
H_D#27	W7	H_D#_27	
H_D#28	U5	H_D#_28	
H_D#29	T9	H_D#_29	
H_D#30	W6	H_D#_30	
H_D#31	T5	H_D#_31	
H_D#32	AB7	H_D#_32	
H_D#33	AA9	H_D#_33	
H_D#34	W4	H_D#_34	
H_D#35	W3	H_D#_35	
H_D#36	Y3	H_D#_36	
H_D#37	Y7	H_D#_37	
H_D#38	W5	H_D#_38	
H_D#39	Y10	H_D#_39	
H_D#40	AB8	H_D#_40	
H_D#41	W2	H_D#_41	
H_D#42	AA4	H_D#_42	
H_D#43	AA7	H_D#_43	
H_D#44	AA2	H_D#_44	
H_D#45	AA6	H_D#_45	
H_D#46	AA10	H_D#_46	
H_D#47	Y8	H_D#_47	
H_D#48	AA1	H_D#_48	
H_D#49	AB4	H_D#_49	
H_D#50	AC9	H_D#_50	
H_D#51	AB11	H_D#_51	
H_D#52	AC11	H_D#_52	
H_D#53	AB3	H_D#_53	
H_D#54	AC2	H_D#_54	
H_D#55	AD1	H_D#_55	
H_D#56	AD9	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AD7	H_D#_58	
H_D#59	AC6	H_D#_59	
H_D#60	AB5	H_D#_60	
H_D#61	AD10	H_D#_61	
H_D#62	AD4	H_D#_62	
H_D#63	AC8	H_D#_63	

H_XRCOMP	E1	H_XRCOMP	
H_XSCOMP	E2	H_XSCOMP	
H_XSWING	E4	H_XSWING	
H_YRCOMP	Y1	H_YRCOMP	
H_YSCOMP	U1	H_YSCOMP	
H_YSWING	W1	H_YSWING	
5 CLK_MCH_BCLK	AG2	H_CLKIN	
5 CLK_MCH_BCLK#	AG1	H_CLKIN#	

H_A#_3	H9	H_A#3	
H_A#_4	C9	H_A#4	
H_A#_5	E11	H_A#5	
H_A#_6	G11	H_A#6	
H_A#_7	F11	H_A#7	
H_A#_8	G12	H_A#8	
H_A#_9	F9	H_A#9	
H_A#_10	H11	H_A#10	
H_A#_11	J12	H_A#11	
H_A#_12	G14	H_A#12	
H_A#_13	D9	H_A#13	
H_A#_14	J14	H_A#14	
H_A#_15	H13	H_A#15	
H_A#_16	J15	H_A#16	
H_A#_17	F14	H_A#17	
H_A#_18	D12	H_A#18	
H_A#_19	A11	H_A#19	
H_A#_20	C11	H_A#20	
H_A#_21	A12	H_A#21	
H_A#_22	A13	H_A#22	
H_A#_23	E13	H_A#23	
H_A#_24	G13	H_A#24	
H_A#_25	F12	H_A#25	
H_A#_26	B12	H_A#26	
H_A#_27	B14	H_A#27	
H_A#_28	C12	H_A#28	
H_A#_29	A14	H_A#29	
H_A#_30	C14	H_A#30	
H_A#_31	D14	H_A#31	

H_ADS#	E8	H_ADS#	H_ADS# 2
H_ADSTB#_0	B9	H_ADSTB#0	H_ADSTB#0 2
H_ADSTB#_1	C13	H_ADSTB#1	H_ADSTB#1 2
H_AVREF	J13	H_VREF	
H_BNR#	C6	H_BNR#	H_BNR# 2
H_BPRI#	F6	H_BPRI#	H_BPRI# 2
H_BREQ#0	C7	H_BR0#	H_BR0# 2
H_CPURST#	B7	H_CPURST#	H_CPURST# 2
H_DBSY#	A7	H_DBSY#	H_DBSY# 2
H_DEFER#	C3	H_DEFER#	H_DEFER# 2
H_DPWR#	J9	H_DPWR#	H_DPWR# 2
H_DRDY#	H8	H_DRDY#	H_DRDY# 2
H_DVREF	K13		

H_DINV#_0	J7	H_DINV#0	H_DINV#0 2
H_DINV#_1	W8	H_DINV#1	H_DINV#1 2
H_DINV#_2	U3	H_DINV#2	H_DINV#2 2
H_DINV#_3	AB10	H_DINV#3	H_DINV#3 2
H_DSTBN#_0	K4	H_DSTBN#0	H_DSTBN#0 2
H_DSTBN#_1	T7	H_DSTBN#1	H_DSTBN#1 2
H_DSTBN#_2	Y5	H_DSTBN#2	H_DSTBN#2 2
H_DSTBN#_3	AC4	H_DSTBN#3	H_DSTBN#3 2
H_DSTBP#_0	K3	H_DSTBP#0	H_DSTBP#0 2
H_DSTBP#_1	T6	H_DSTBP#1	H_DSTBP#1 2
H_DSTBP#_2	AA5	H_DSTBP#2	H_DSTBP#2 2
H_DSTBP#_3	AC5	H_DSTBP#3	H_DSTBP#3 2
H_HIT#	D3	H_HIT#	H_HIT# 2
H_HITM#	D4	H_HITM#	H_HITM# 2
H_LOCK#	B3	H_LOCK#	H_LOCK# 2

H_REQ#[4..0] 2

H_REQ#_0	D8	H_REQ#0	
H_REQ#_1	G8	H_REQ#1	
H_REQ#_2	B8	H_REQ#2	
H_REQ#_3	F8	H_REQ#3	
H_REQ#_4	A8	H_REQ#4	

H_RS#[0..2] 2

H_RS#_0	B4	H_RS#0	
H_RS#_1	E6	H_RS#1	
H_RS#_2	D6	H_RS#2	
H_SLPCPU#	E3	N_CPUSLP#	2 R611 0Ohm 1 H_CPUSLP# 2,17
H_TRDY#	E7	H_TRDY#	H_TRDY# 2

CALISTOGA_Q137

+VCCP_AGTL+

R601 100Ohm 1%

R606 200Ohm 1%

C601 0.1UF/10V

GND GND

<500 mil (55 Ohm) T/B trace 5.5 , Space 25

Layout Note: 0.1uF should be placed 100mils or less from GMCH pin.

+VCCP +VCCP

R602 54.9Ohm 1%

R603 54.9Ohm 1%

5.5/20 mils

H_XSCOMP H_YSCOMP

H_XRCOMP H_YRCOMP

R604 24.9Ohm 1%

R605 24.9Ohm 1%

10/20mils

GND GND

+VCCP

R607 221Ohm 1%

H_XSWING

C602 0.1UF/10V

R608 100Ohm 1%

GND GND

10/20mils

+VCCP

R609 221Ohm 1%

H_YSWING

C603 0.1UF/10V

R610 100Ohm 1%

GND GND

Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing

PCMCIA

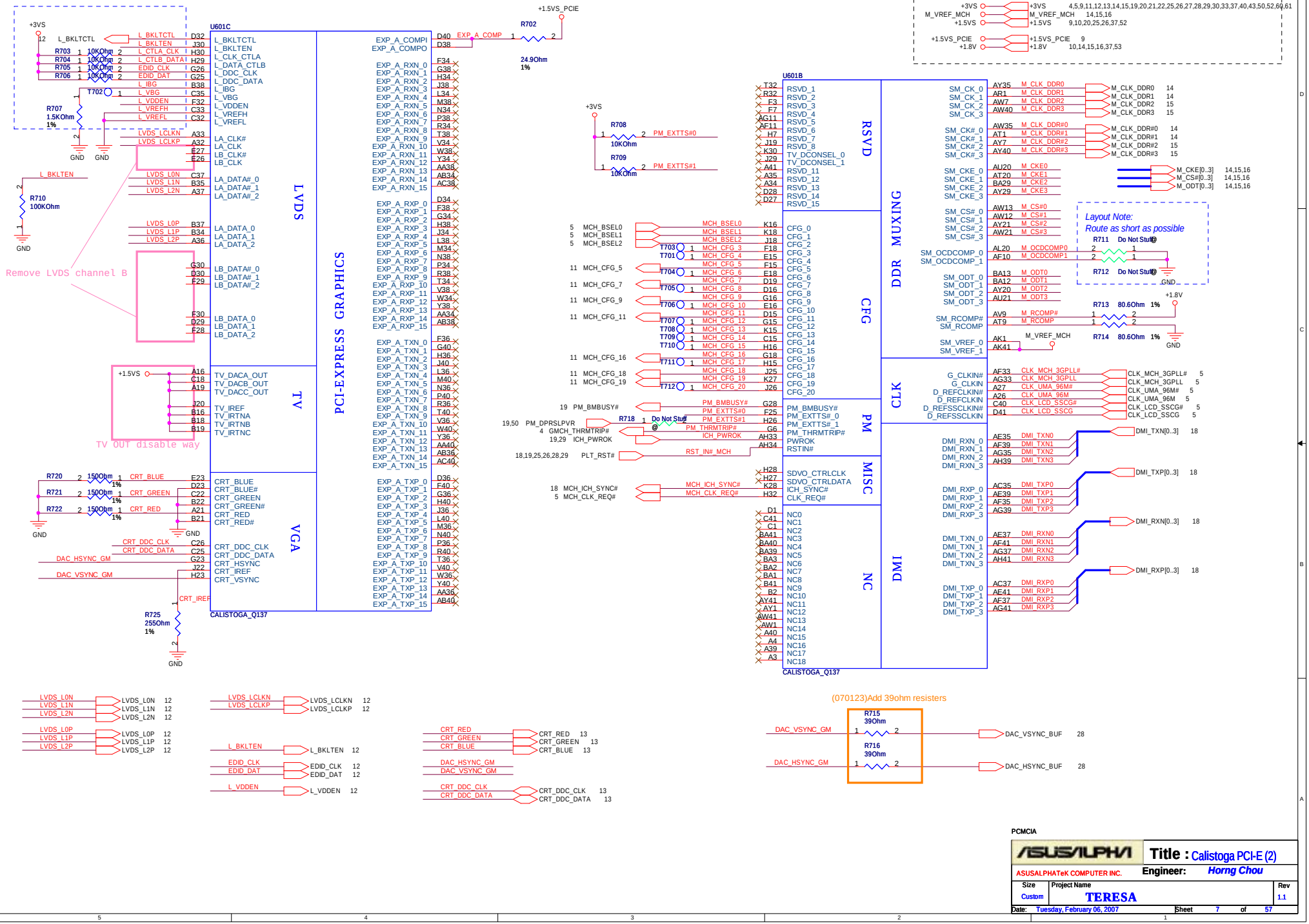
ASUSALPHA

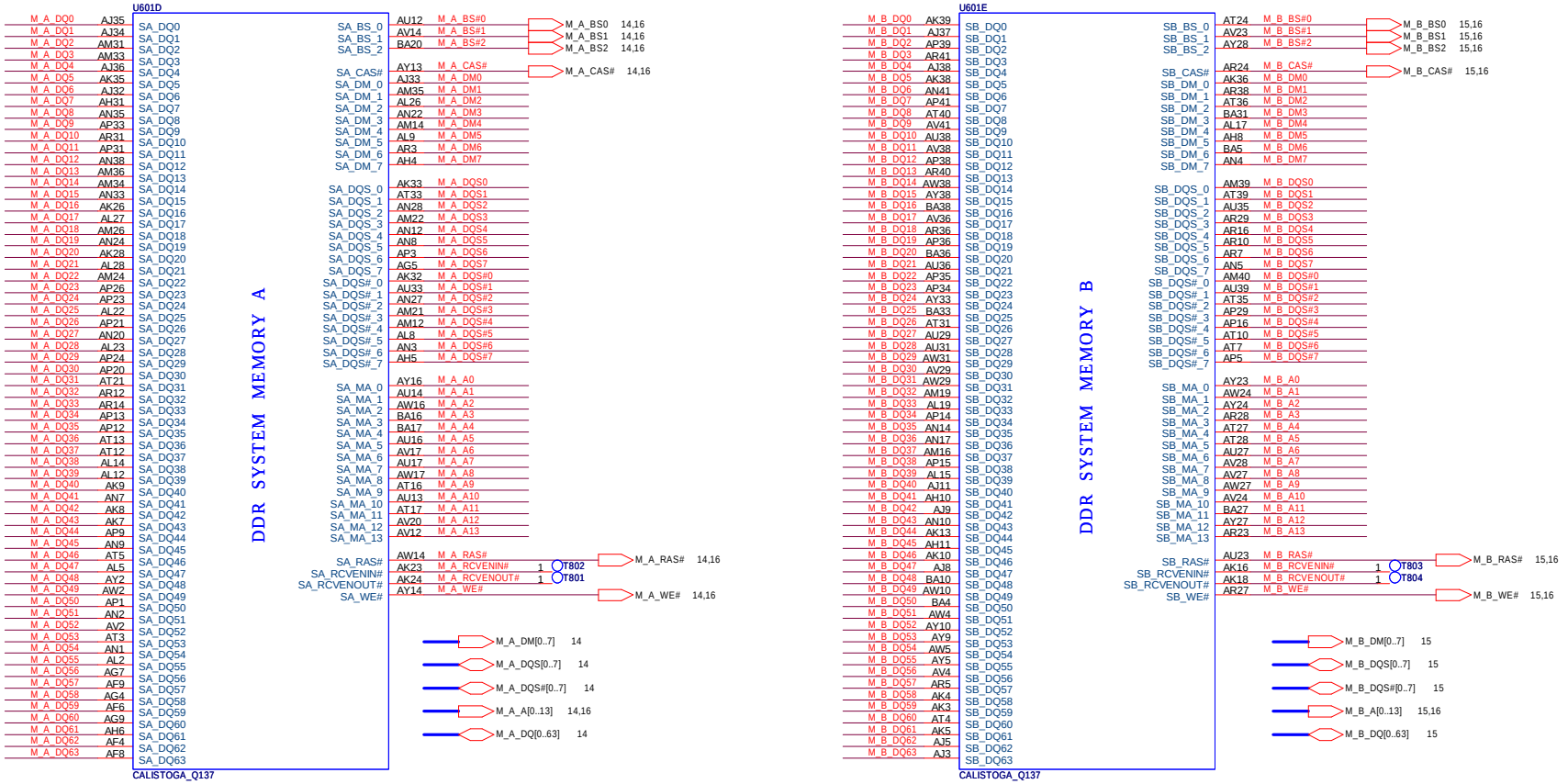
Title : Calistoga GMCH (1)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 6 of 57


U601C
CALISTOGA_Q137
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
Remove LVDS channel B
TV OUT disable way
U601B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
Layout Note:
Route as short as possible
(070123)Add 39ohm resisters
PCMCIA
ASUSALPHATeK COMPUTER INC.
Title : Calistoga PCI-E (2)
Engineer: Horng Chou
TERESA
Size: Custom
Rev: 1.1
Date: Tuesday, February 06, 2007
Sheet 7 of 57



PCMCIA

ASUSALPHATeK COMPUTER INC.

Title : Calistoga DDR2 (3)

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 8 of 57

Layout Note:
Place filter components
close to GMCH

Layout Note:
Caps should be on Top layer

VCC3G

1500 mA

VCCA_3GPLL

VCCAUX
1900 mA

(070131)
220UF=>150UF

VCCA_DPLLA
50 mA

VCCA_DPLLB
50 mA

VCCA_HPLL
45 mA

VCCA_MPLL
45 mA

(070131)C923, C927:unmount

Layout Note:
0.1uF caps in 1.5VS_xPLL
need to be located as edge
caps within 200 mils.

GMCH VCORE

+1.05VS
3500 mA

JP902 Do Not Stuff @
JP901 Do Not Stuff @

VCCD_LVDS 20 mA
Pin A28 B28 C28

VCCD_TVDAC
Pin D21

24 mA

VCCD_QTVDAC
H19 C28

Layout Note:
These Caps should be within
250 mils of edge of GMCH

TV OUT disable way

POWER

U601H
CALISTOGA_Q137

Layout Note:
These 0.1uF caps should
be placed within 200 mils
of edge

VCC_SYNC
Pin H22

VCCA_LVDS
Pin A38 10 mA

VCCA_3GBG
Pin G41 2 mA

VCCTX_LVDS 60 mA
Pin A30 B30 C30

R905 10Ohm
D902 BAT54C

70 mA

VCCA_CRTDAC
Pin E21 F21

Layout Note:
These Caps should
be within 250 mils of
edge of GMCH

VCC_HV 40 mA
Pin A23 B23 B25

+VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH 10
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+2.5VS 37,54
+1.5VS 7,10,20,25,26,37,52

800 mA

Layout Note:
Place on the edge

Layout Note:
Place in cavity

(070118)
change into 11G08D210791

Remove TV OUT Power

NOTE:0.1UF CAPS USED IN +1.5VS,
+3.3VS
+2.5VS should be placed within
200 mils of edge.

PCMCIA

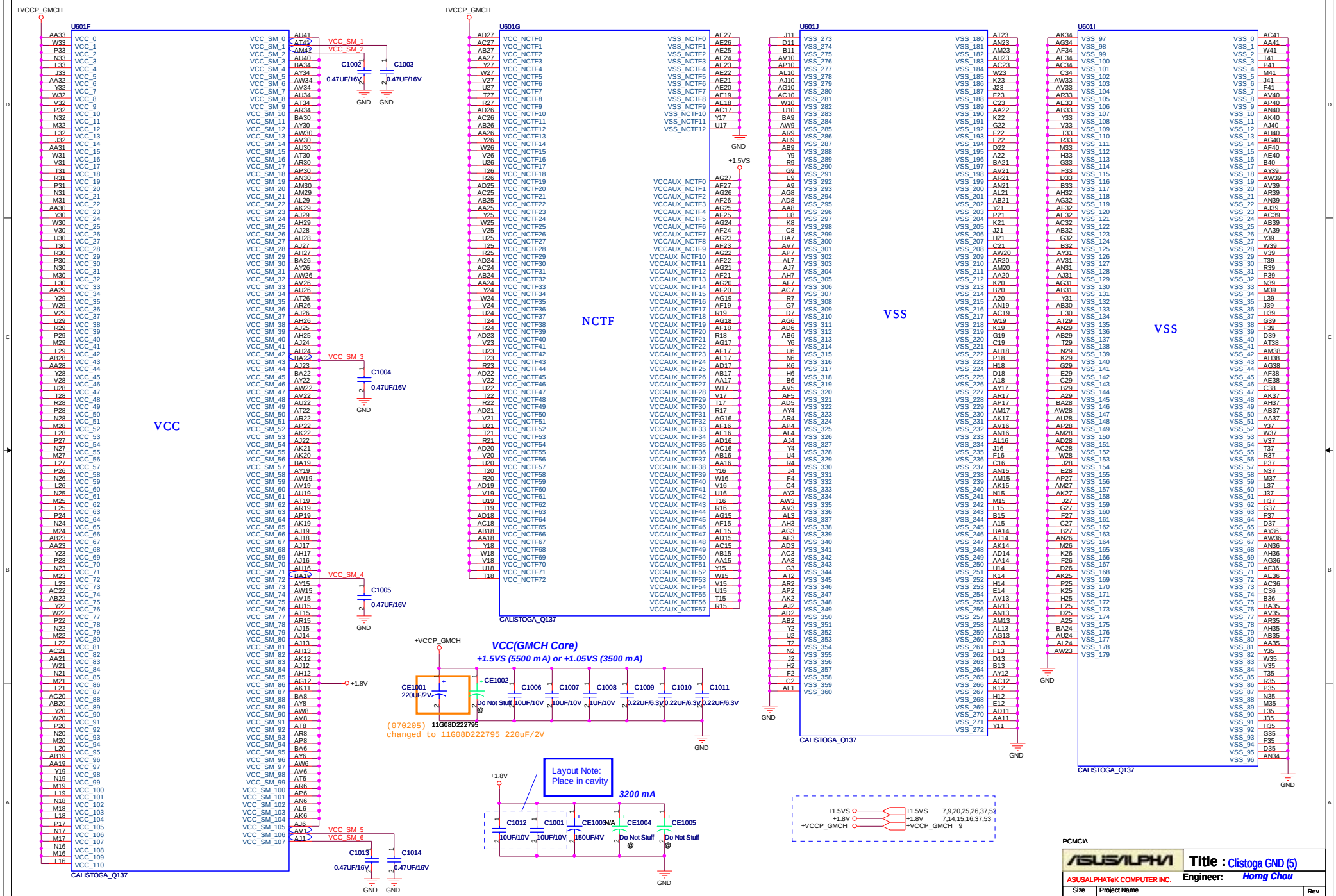
ASUSALPHATeK COMPUTER INC.

Title : Calistoga Power (4)

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 9 of 57



PCMCIA

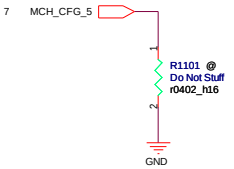
ASUSALPHATeK COMPUTER INC.

Title : Clistoga GND (5)

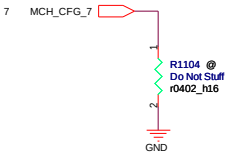
Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

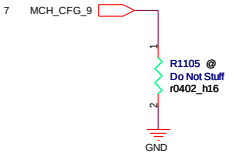
Date: Tuesday, February 06, 2007 Sheet 10 of 57



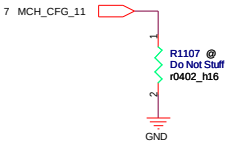
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



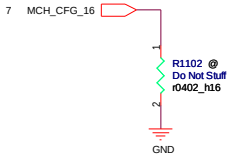
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



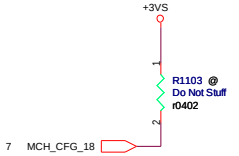
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



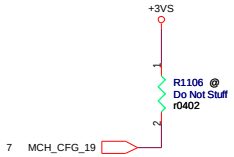
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

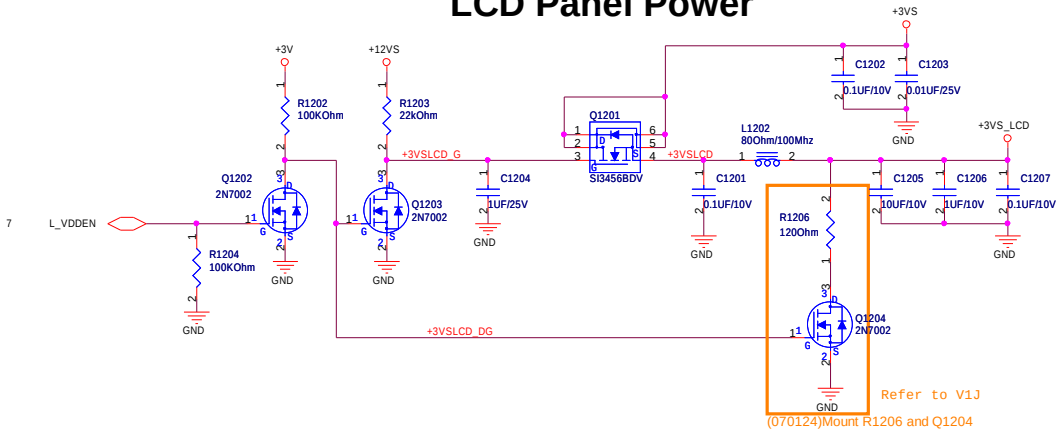
(061215)Remove +2.5VS power supply

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

PCMCIA
ASUSALPHA
Title : Calistoga Strapping
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size: Custom | Project Name: TERESA | Rev: 1.1
Date: Tuesday, February 06, 2007 | Sheet 11 of 57

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



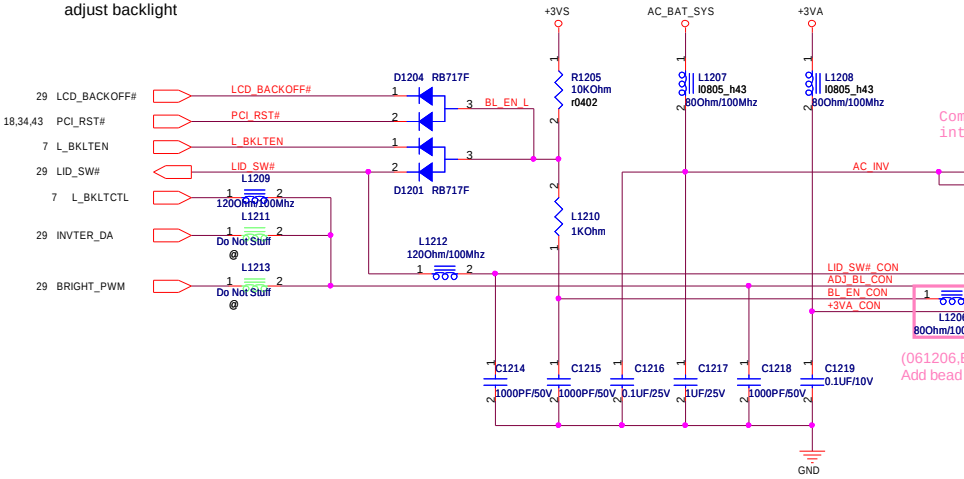
Remove CMOS Camera(USB4)

LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel



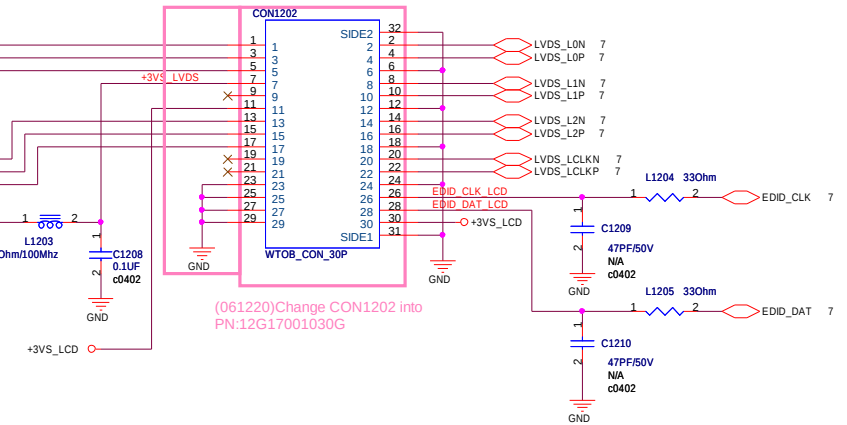
Combine Inverter interface into LVDS interface

(061206,EMI)
Add bead

LCD LVDS & INVERTER Interface

Delete LVDS channel B

Rearrange pin location(061201)



(061220)Change CON1202 into PN:12G17001030G

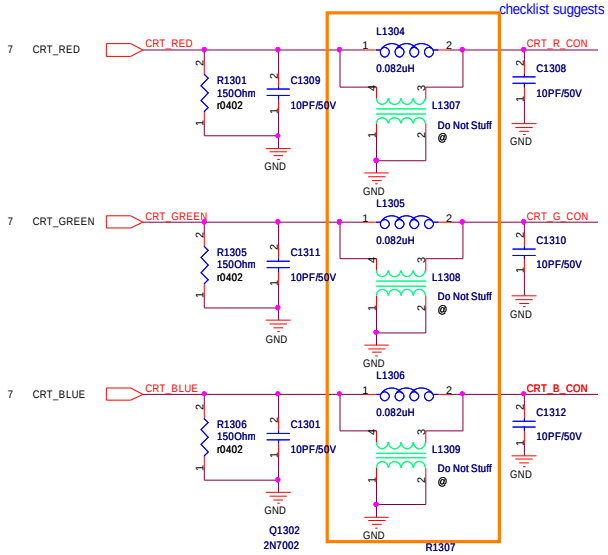
PCMCIA

ASUSALPHA	Title : LVDS & INVERTER	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 12 of 57	

CRT OUT

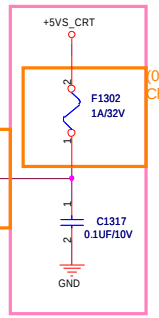
(061206,EMI)
Add L1307, L1308, L1309
(070205) tune performance
changed to 09G023821009 0.082uH

checklist suggests 47ohm/100MHz



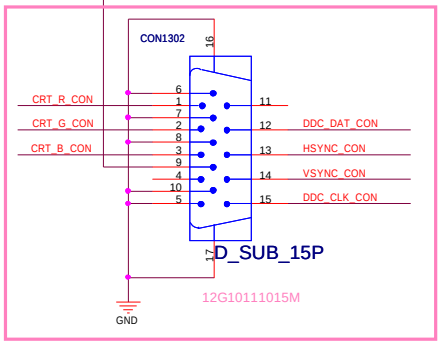
New addition for Teresa

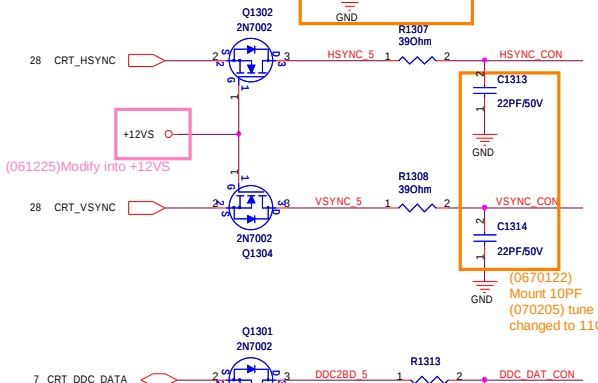
(070201)
Remove 0om resister



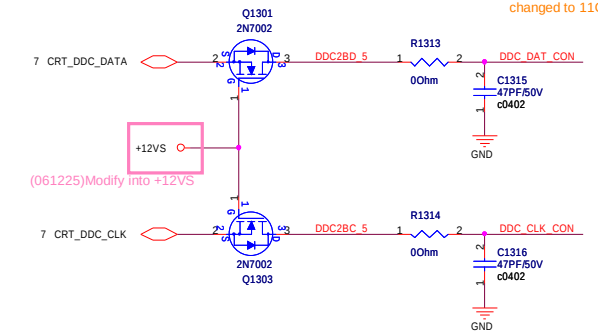
(070130)
Change fuse into 1A

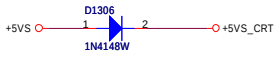
Change D-SUB into PN:12G10111015M

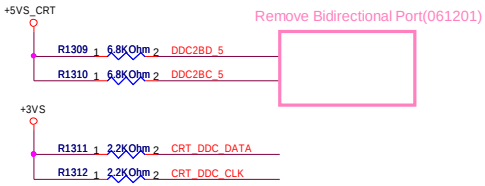




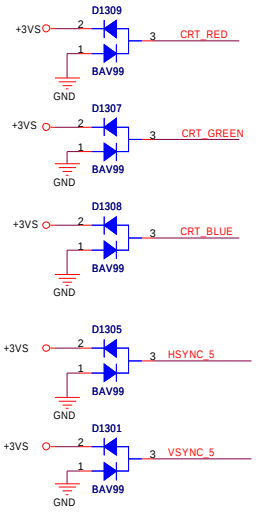
(0670122)
Mount 10PF
(070205) tune performance
changed to 11G232022004360 22pF







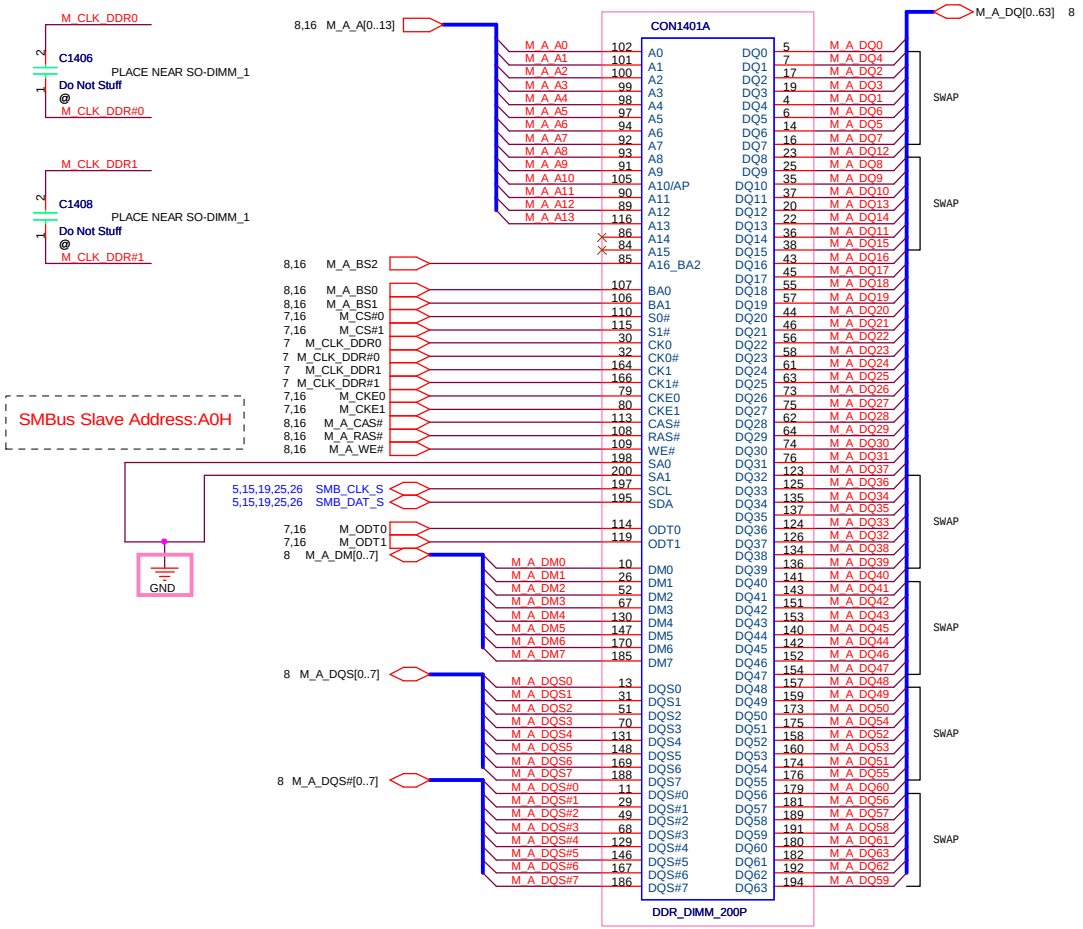
Remove Bidirectional Port(061201)



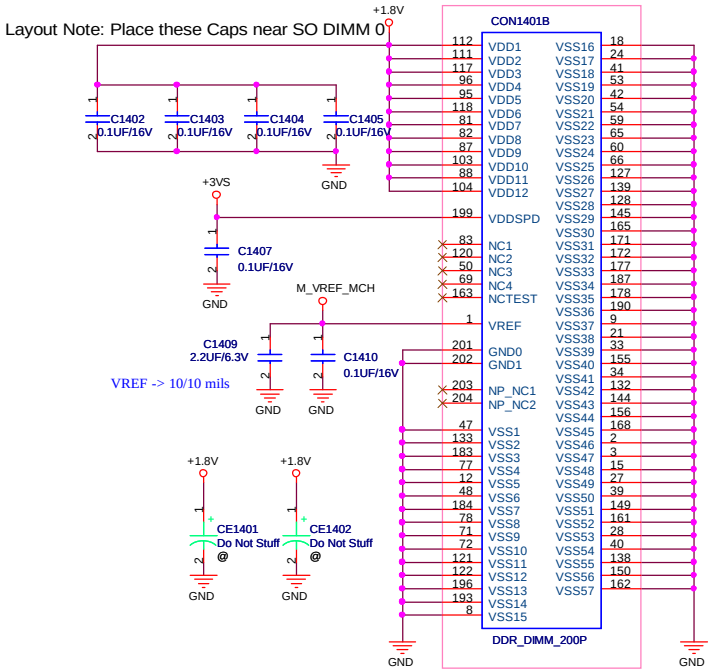
PCMCIA

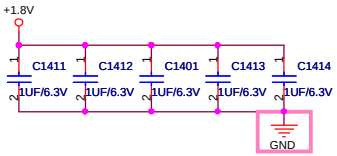
ASUSALPHA	Title : CRT & TV OUT	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 13 of 57	

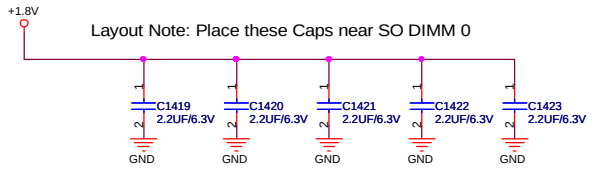
(061221)Change CON1401 into PN:12G02502200R



(061221)Change CON1401 into PN:12G02502200R







SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

PCMCIA

ASUSALPHA	Title : DDR2 SO-DIMM0	
ASUSALPHAteK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 14 of 57	

SMBus Slave Address:A4H

M_CLK_DDR2
C1507 PLACE NEAR SO-DIMM_0
Do Not Stuff
@
M_CLK_DDR#2

M_CLK_DDR3
C1509 PLACE NEAR SO-DIMM_0
Do Not Stuff
@
M_CLK_DDR#3

8,16 M_B_A[0..13]
8 M_B_DQ[0..63]
M_B_DQ[0..63]

(061227)Update PCB footprint
PN:12G025032008

CON1501A

M_B_A0	102	A0	DQ0	5	M_B_DQ5
M_B_A1	101	A1	DQ1	7	M_B_DQ0
M_B_A2	100	A2	DQ2	17	M_B_DQ7
M_B_A3	99	A3	DQ3	19	M_B_DQ3
M_B_A4	98	A4	DQ4	4	M_B_DQ4
M_B_A5	97	A5	DQ5	6	M_B_DQ1
M_B_A6	94	A6	DQ6	14	M_B_DQ6
M_B_A7	92	A7	DQ7	16	M_B_DQ2
M_B_A8	93	A8	DQ8	23	M_B_DQ8
M_B_A9	91	A9	DQ9	25	M_B_DQ9
M_B_A10	105	A10/AP	DQ10	35	M_B_DQ10
M_B_A11	90	A11	DQ11	37	M_B_DQ11
M_B_A12	89	A12	DQ12	20	M_B_DQ12
M_B_A13	116	A13	DQ13	22	M_B_DQ13
	86	A14	DQ14	36	M_B_DQ14
	84	A15	DQ15	38	M_B_DQ15
	85	A16_BA2	DQ16	43	M_B_DQ16
			DQ17	45	M_B_DQ17
	107	BA0	DQ18	55	M_B_DQ18
	106	BA1	DQ19	57	M_B_DQ19
	110	S0#	DQ20	44	M_B_DQ20
	115	S1#	DQ21	46	M_B_DQ21
	30	CK0	DQ22	56	M_B_DQ22
	32	CK0#	DQ23	58	M_B_DQ23
	164	CK1	DQ24	61	M_B_DQ24
	166	CK1#	DQ25	63	M_B_DQ25
	79	CKE0	DQ26	73	M_B_DQ26
	80	CKE1	DQ27	75	M_B_DQ27
	113	CAS#	DQ28	62	M_B_DQ28
	108	RAS#	DQ29	64	M_B_DQ29
	109	WE#	DQ30	74	M_B_DQ30
	198	SA0	DQ31	76	M_B_DQ31
	200	SA1	DQ32	123	M_B_DQ36
	197	SCL	DQ33	125	M_B_DQ32
	195	SDA	DQ34	135	M_B_DQ34
			DQ35	137	M_B_DQ35
	114	ODT0	DQ36	124	M_B_DQ33
	119	ODT1	DQ37	126	M_B_DQ37
M_B_DM0	10	DM0	DQ38	134	M_B_DQ38
M_B_DM1	26	DM1	DQ39	136	M_B_DQ39
M_B_DM2	52	DM2	DQ40	141	M_B_DQ49
M_B_DM3	67	DM3	DQ41	143	M_B_DQ53
M_B_DM4	130	DM4	DQ42	151	M_B_DQ54
M_B_DM6	147	DM5	DQ43	153	M_B_DQ55
M_B_DM7	170	DM6	DQ44	140	M_B_DQ48
M_B_DM5	185	DM7	DQ45	142	M_B_DQ52
			DQ46	152	M_B_DQ51
			DQ47	154	M_B_DQ50
M_B_DQS0	13	DQS0	DQ48	157	M_B_DQ62
M_B_DQS1	31	DQS1	DQ49	159	M_B_DQ57
M_B_DQS2	51	DQS2	DQ50	173	M_B_DQ59
M_B_DQS3	70	DQS3	DQ51	175	M_B_DQ58
M_B_DQS4	131	DQS4	DQ52	158	M_B_DQ56
M_B_DQS6	148	DQS5	DQ53	160	M_B_DQ60
M_B_DQS7	169	DQS6	DQ54	174	M_B_DQ61
M_B_DQS5	188	DQS7	DQ55	176	M_B_DQ63
M_B_DQS#0	11	DQS#0	DQ56	179	M_B_DQ42
M_B_DQS#1	29	DQS#1	DQ57	181	M_B_DQ47
M_B_DQS#2	49	DQS#2	DQ58	189	M_B_DQ40
M_B_DQS#3	68	DQS#3	DQ59	191	M_B_DQ45
M_B_DQS#4	129	DQS#4	DQ60	180	M_B_DQ43
M_B_DQS#6	146	DQS#5	DQ61	182	M_B_DQ46
M_B_DQS#7	167	DQS#6	DQ62	192	M_B_DQ41
M_B_DQS#5	186	DQS#7	DQ63	194	M_B_DQ44

DDR_DIMM_200P

SWAP
SWAP
SWAP

8,16 M_B_BS2
8,16 M_B_BS0
8,16 M_B_BS1
7,16 M_CS#2
7,16 M_CS#3
7 M_CLK_DDR3
7 M_CLK_DDR#3
7 M_CLK_DDR2
7 M_CLK_DDR#2
7,16 M_CKE2
7,16 M_CKE3
8,16 M_B_CAS#
8,16 M_B_RAS#
8,16 M_B_WE#

+3VS
R1501
1 2
10KOhm
+3VS_SET
GND

5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S

7,16 M_ODT2
7,16 M_ODT3
8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

Address reference +1.8V, add four
0.1uF decoupling CAP.

+1.8V
C1502 0.1UF/16V c0402
C1503 0.1UF/16V c0402
C1504 0.1UF/16V c0402
C1505 0.1UF/16V c0402
GND

+3VS
C1506 0.1UF/16V
GND

M_VREF_MCH
VREF -> 10/10 mils
C1508 1UF/6.3V
C1501 0.1UF/16V
GND

(061227)Update PCB footprint
PN:12G025032008

CON1501B

112	VDD1	VSS16	18		
111	VDD2	VSS17	24		
117	VDD3	VSS18	41		
96	VDD4	VSS19	53		
95	VDD5	VSS20	42		
118	VDD6	VSS21	54		
81	VDD7	VSS22	59		
82	VDD8	VSS23	65		
87	VDD9	VSS24	60		
103	VDD10	VSS25	66		
88	VDD11	VSS26	127		
104	VDD12	VSS27	139		
		VSS28	128		
199	VDDSPD	VSS29	145		
		VSS30	165		
83	NC1	VSS31	171		
120	NC2	VSS32	172		
50	NC3	VSS33	177		
69	NC4	VSS34	187		
163	NCTEST	VSS35	178		
		VSS36	190		
1	VREF	VSS37	9		
		VSS38	21		
201	GND0	VSS39	33		
202	GND1	VSS40	155		
		VSS41	34		
203	NP_NC1	VSS42	132		
204	NP_NC2	VSS43	144		
		VSS44	156		
47	VSS1	VSS45	168		
133	VSS2	VSS46	2		
183	VSS3	VSS47	3		
77	VSS4	VSS48	15		
12	VSS5	VSS49	27		
48	VSS6	VSS50	39		
184	VSS7	VSS51	149		
78	VSS8	VSS52	161		
71	VSS9	VSS53	28		
72	VSS10	VSS54	40		
121	VSS11	VSS55	138		
122	VSS12	VSS56	150		
196	VSS13	VSS57	162		
193	VSS14				
8	VSS15				

DDR_DIMM_200P

GND GND

Layout Note: Place these Caps near SO DIMM 0

Layout Note: Place these Caps near SO DIMM 0

+1.8V
C1510 0.1UF/16V
C1511 0.1UF/16V
C1512 0.1UF/16V
C1513 0.1UF/16V
GND

Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V
C1514 0.1UF/16V c0402
C1515 0.1UF/16V c0402
C1516 0.1UF/16V c0402
C1517 0.1UF/16V c0402
GND GND GND GND

Layout Note: Place these CAPs near the GMCH

+1.8V
C1518 2.2UF/6.3V
C1519 2.2UF/6.3V
C1520 2.2UF/6.3V
C1521 2.2UF/6.3V
C1522 2.2UF/6.3V
GND GND GND GND GND

PCMCIA

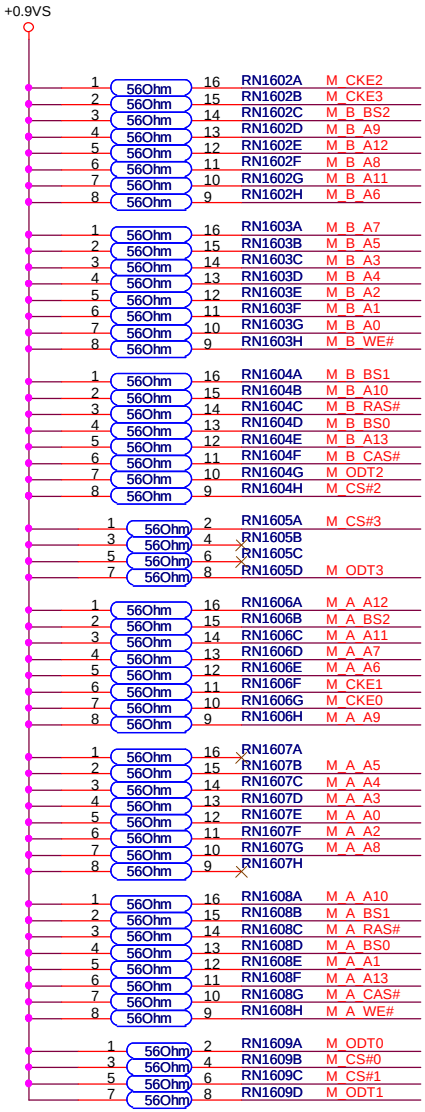
ASUSALPHA

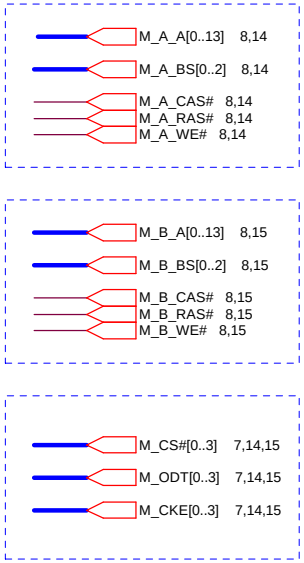
Title : DDR2 SO-DIMM1

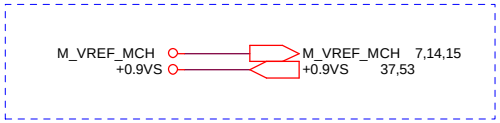
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

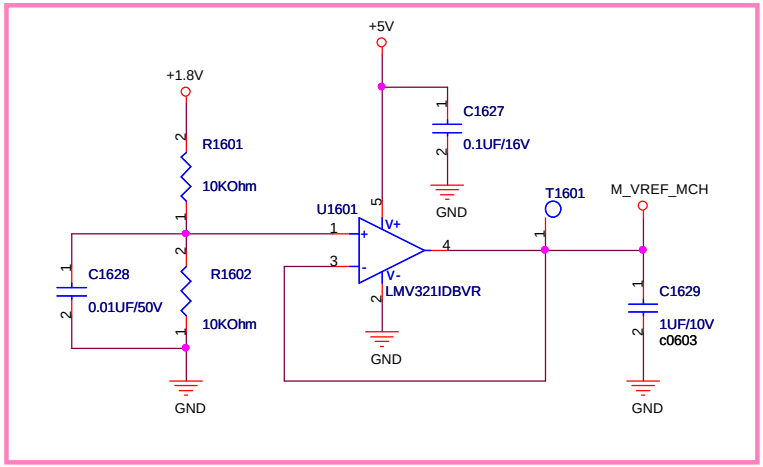
Date: Tuesday, February 06, 2007 Sheet 15 of 57

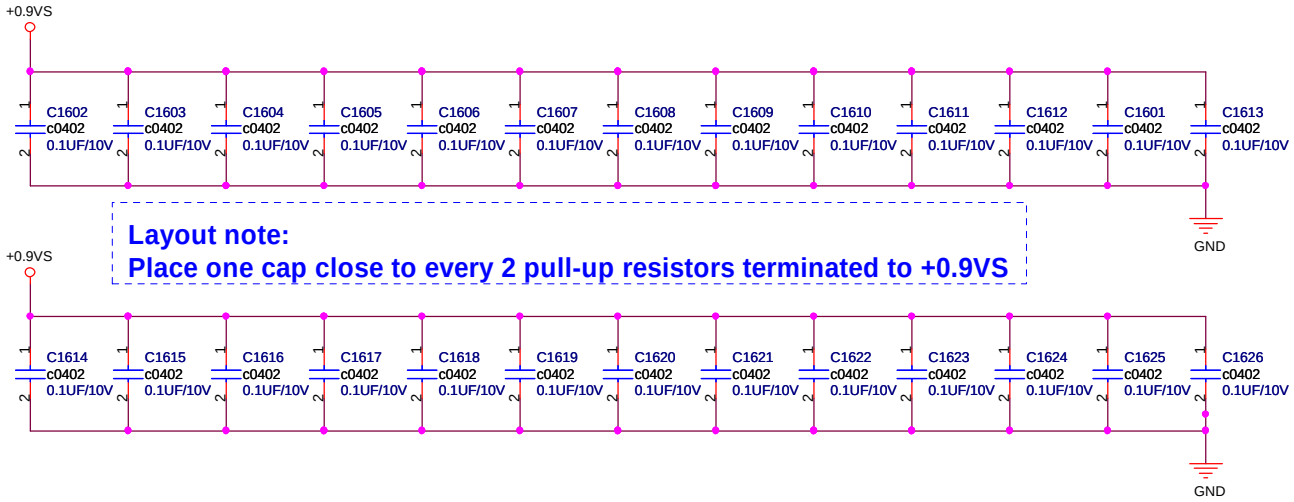






Add Voltage Follower

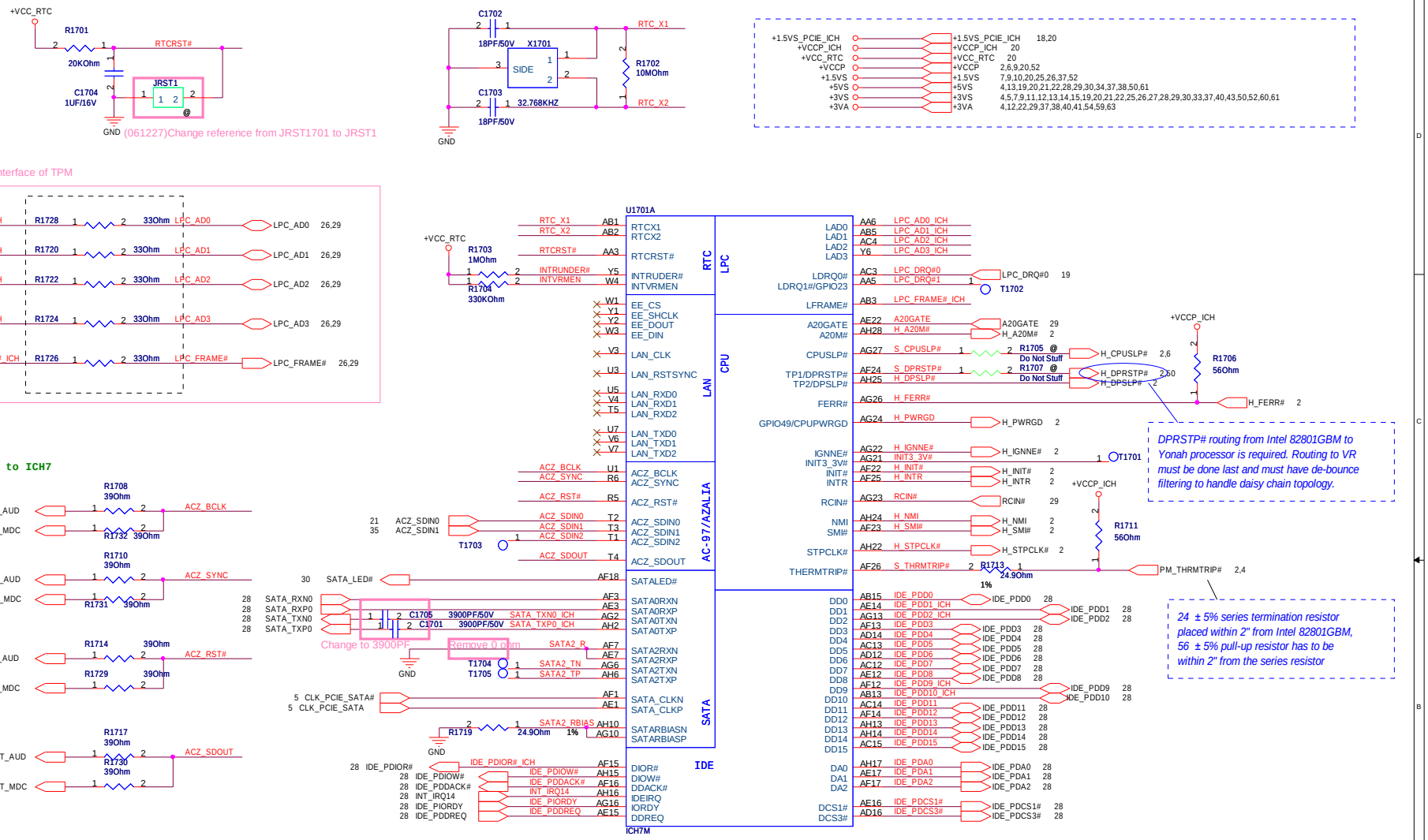




Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

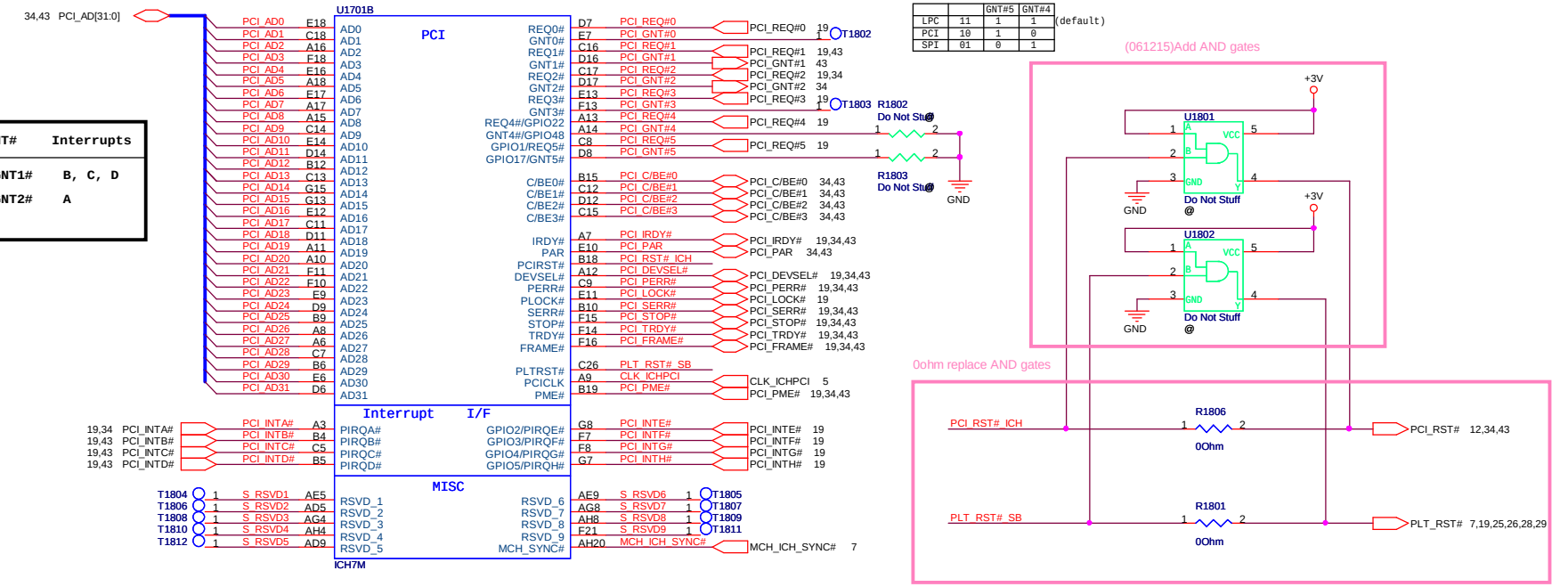
PCMCIA

ASUSALPHA	Title : DDR2 TERM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 16 of 57	


+VCC_RTC
R1701
20KOhm
C1704
1UF/16V
JRST1
RTCRST#
GND
(061227)Change reference from JRST1701 to JRST1
C1702
18PF/50V
X1701
SIDE
32.768KHZ
C1703
18PF/50V
RTC_X1
RTC_X2
R1702
10MOhm
GND
+1.5VS_PCIE_ICH 18,20
+VCCP_ICH 20
+VCC_RTC 20
+VCCP 2,6,9,20,52
+1.5VS 7,9,10,20,25,26,37,52
+5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61
+3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,40,43,50,52,60,61
+3VA 4,12,22,29,37,38,40,41,54,59,63
Delete LPC interface of TPM
LPC_AD0_ICH R1728 33Ohm LPC_AD0 LPC_AD0 26,29
LPC_AD1_ICH R1720 33Ohm LPC_AD1 LPC_AD1 26,29
LPC_AD2_ICH R1722 33Ohm LPC_AD2 LPC_AD2 26,29
LPC_AD3_ICH R1724 33Ohm LPC_AD3 LPC_AD3 26,29
LPC_FRAME#_ICH R1726 33Ohm LPC_FRAME# LPC_FRAME# 26,29
U1701A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
ICH7M
R1703 1MOhm
R1704 330KOhm
INTRUDER# Y5
INTVRMEN W4
EE_CS W1
EE_SHCLK Y1
EE_DOUT Y2
EE_DIN W3
LAN_CLK V3
LAN_RSTSYNC U3
LAN_RXD0 U5
LAN_RXD1 V4
LAN_RXD2 T5
LAN_TXD0 U7
LAN_TXD1 V6
LAN_TXD2 V7
ACZ_BCLK U1
ACZ_SYNC R6
ACZ_RST# R5
ACZ_SDIN0 T2
ACZ_SDIN1 T3
ACZ_SDIN2 T1
ACZ_SDOUT T4
T1703
SATALED# AF18
SATA0RXN AF3
SATA0RXP AE3
SATA0TXN AG2
SATA0TXP AH2
SATA2RXN AE7
SATA2RXP AE7
SATA2TXN AG6
SATA2TXP AH6
SATA_CLKN AF1
SATA_CLKP AE1
SATARBIASN AH10
SATARBIASP AG10
R1719 24.9Ohm 1%
DIOR# AF15
DIOW# AH15
DDACK# AF16
IDEIRQ AH16
IORDY AG16
DDREQ AE15
LAD0 AA6 LPC_AD0_ICH
LAD1 AB5 LPC_AD1_ICH
LAD2 AC4 LPC_AD2_ICH
LAD3 Y6 LPC_AD3_ICH
LDRQ0# AC3 LPC_DRQ#0
LDRQ1#/GPIO23 AA5 LPC_DRQ#1
T1702
LFRAME# AB3 LPC_FRAME# ICH
A20GATE AE22 A20GATE
A20M# AH28 H_A20M#
CPUSLP# AG27 S_CPUSLP# R1705 @ Do Not Stuff H_CPUSLP#
TP1/DPRSTP# AF24 S_DPRSTP# R1707 @ Do Not Stuff H_DPRSTP#
TP2/DPSLP# AH25 H_DPSLP#
FERR# AG26 H_FERR#
GPIO49/CPUPWRGD AG24 H_PWRGD
IGNNE# AG22 H_IGNNE#
INIT3_3V# AG21 INIT3_3V#
INIT# AF22 H_INIT#
INTR AF25 H_INTR
RCIN# AG23 RCIN#
NMI AH24 H_NMI
SMI# AF23 H_SMI#
STPCLK# AH22 H_STPCLK#
THERMTRIP# AF26 S_THRMTRIP# R1713 24.9Ohm 1%
PM_THRMTRIP# 2,4
+VCCP_ICH
R1706 56Ohm
R1711 56Ohm
H_FERR# 2
T1701
DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.
24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor
DD0 AB15 IDE_PDD0
DD1 AE14 IDE_PDD1_ICH
DD2 AG13 IDE_PDD2_ICH
DD3 AF13 IDE_PDD3
DD4 AD14 IDE_PDD4
DD5 AC13 IDE_PDD5
DD6 AD12 IDE_PDD6
DD7 AC12 IDE_PDD7
DD8 AE12 IDE_PDD8
DD9 AF12 IDE_PDD9_ICH
DD10 AB13 IDE_PDD10_ICH
DD11 AC14 IDE_PDD11
DD12 AF14 IDE_PDD12
DD13 AH13 IDE_PDD13
DD14 AH14 IDE_PDD14
DD15 AC15 IDE_PDD15
DA0 AH17 IDE_PDA0
DA1 AE17 IDE_PDA1
DA2 AF17 IDE_PDA2
DCS1# AE16 IDE_PDCS1#
DCS3# AD16 IDE_PDCS3#
close to ICH7
R1708 39Ohm ACZ_BCLK_AUD ACZ_BCLK
R1732 39Ohm ACZ_BCLK_MDC
R1710 39Ohm ACZ_SYNC_AUD ACZ_SYNC
R1731 39Ohm ACZ_SYNC_MDC
R1714 39Ohm ACZ_RST_AUD ACZ_RST#
R1729 39Ohm ACZ_RST_MDC
R1717 39Ohm ACZ_SDOUT_AUD ACZ_SDOUT
R1730 39Ohm ACZ_SDOUT_MDC
SATA_LED#
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
C1705 3900PF/50V SATA_TXN0_ICH
C1701 3900PF/50V SATA_TXP0_ICH
Change to 3900PF
Remove 0 ohm
SATA2_R
SATA2_TN
SATA2_TP
T1704
T1705
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATA2_RBIAS
IDE_PDIOR# ICH
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PIORDY
IDE_PDDREQ
Check with EMI: remove 0 ohm
=>IDE_PDIOR#_ICH
IDE_PDD1_ICH
IDE_PDD2_ICH
IDE_PDD9_ICH
IDE_PDD10_ICH
ACZ_SDOUT | PWROK rising | TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC | PD
ACZ_SYNC | PWROK rising | sets bit 0 of RPC.PC | PD
EE_CS | | should not be pulled high | PD
EE_DOUT | | should not be pulled low | PU
GNT2# | | should not be pulled low | PU
GNT3# | PWROK rising | low: "top-block swap" mode | PU
GNT5#/GPIO17# GNT4#/GPIO48 | PWROK rising | GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC | PU
GPIO16/DPRSLPVR | | should not be pulled high | PD
GPIO25 | RSMRST# rising | should not be pulled low | PU
INTVRMEN | ALWAYS | high: Enable integrated VccSus1_05 VRM |
LINKALERT# | | REQUIRE an extenal pull-up R | Need PU
REQ[4:1]# | PWROK rising | |
SATALED# | | should not be pulled low | Conditional PU
SPKR | PWROK rising | high: "No reboot" mode | PD
TP3 | PWROK rising | should not be pulled low unless using XOR Chain testing | PU
PCMCIA
Title : ICH7-M (1/4)
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
Sheet 17 of 57

PCI Device

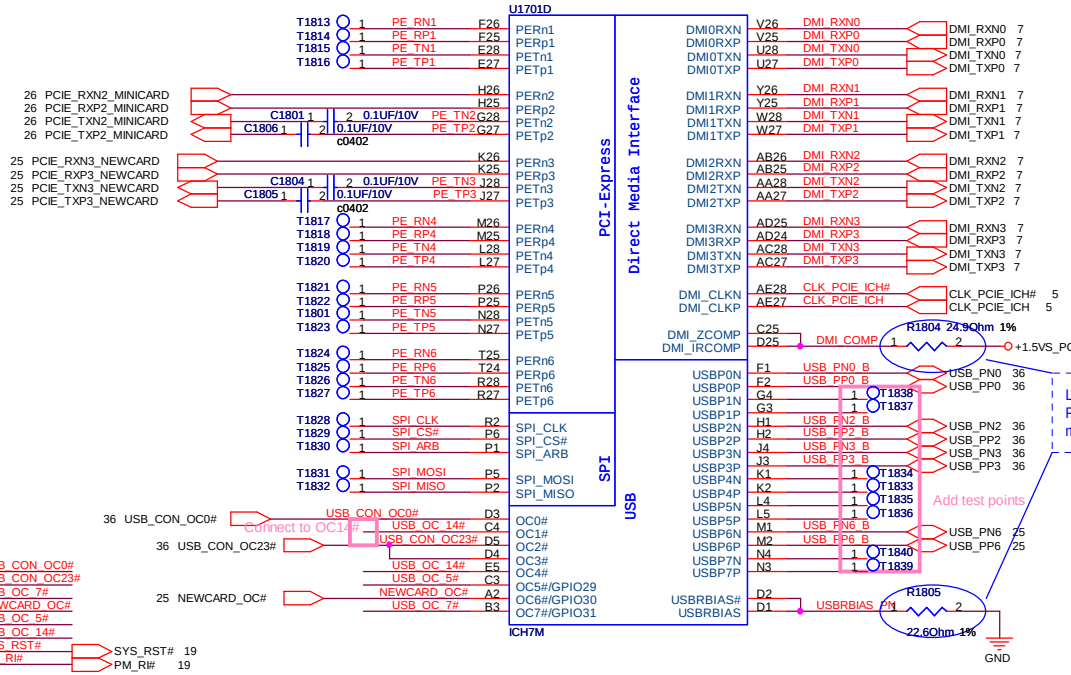
Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A



		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

(061215)Add AND gates

0ohm replace AND gates



(061204)CRT H/VSYNC buffer circuit move to page-28

Modify USB Device table

USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	Unused

Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

PCMCIA

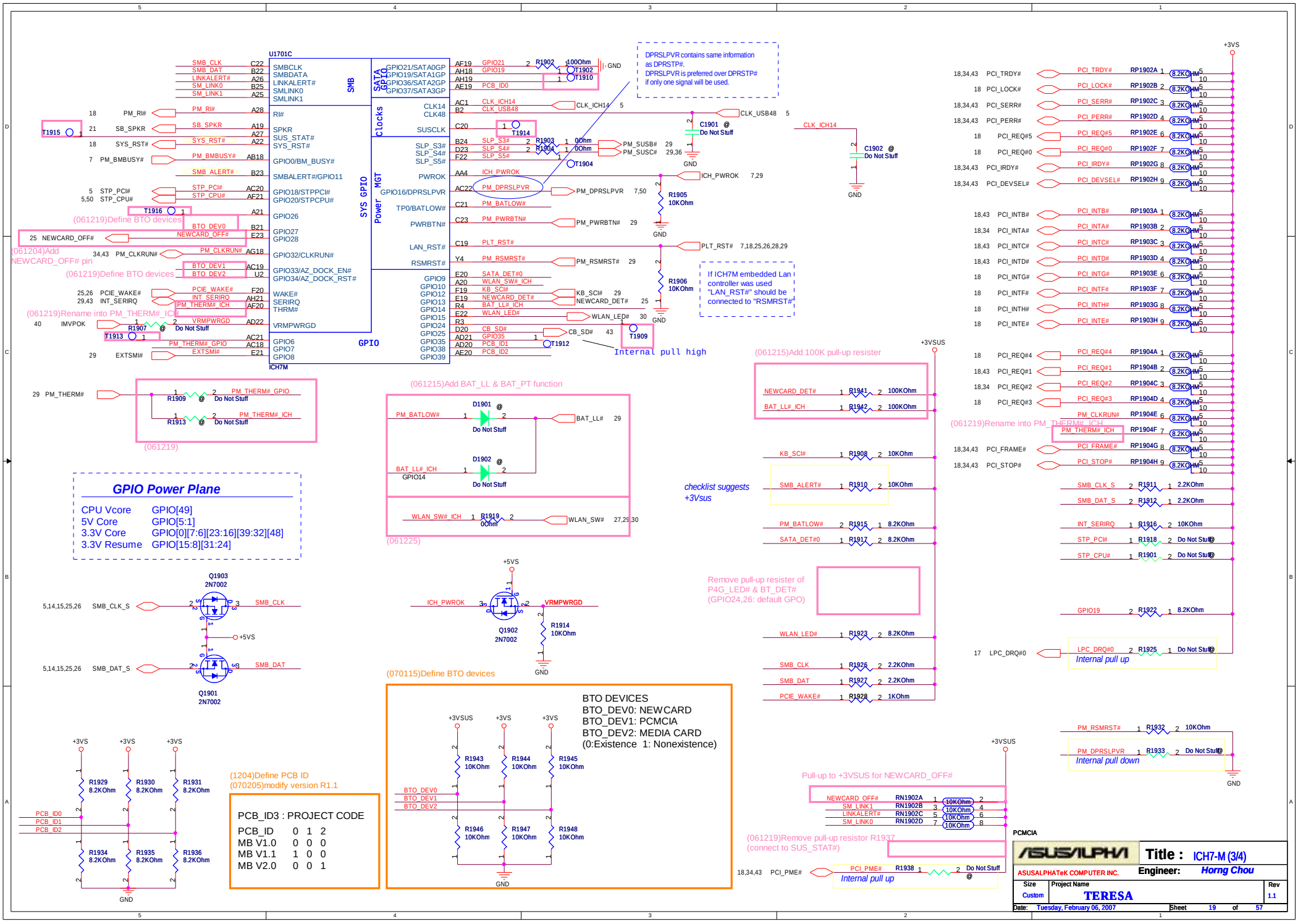
ASUSALPHA

Title : ICH7-M (2/4)

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

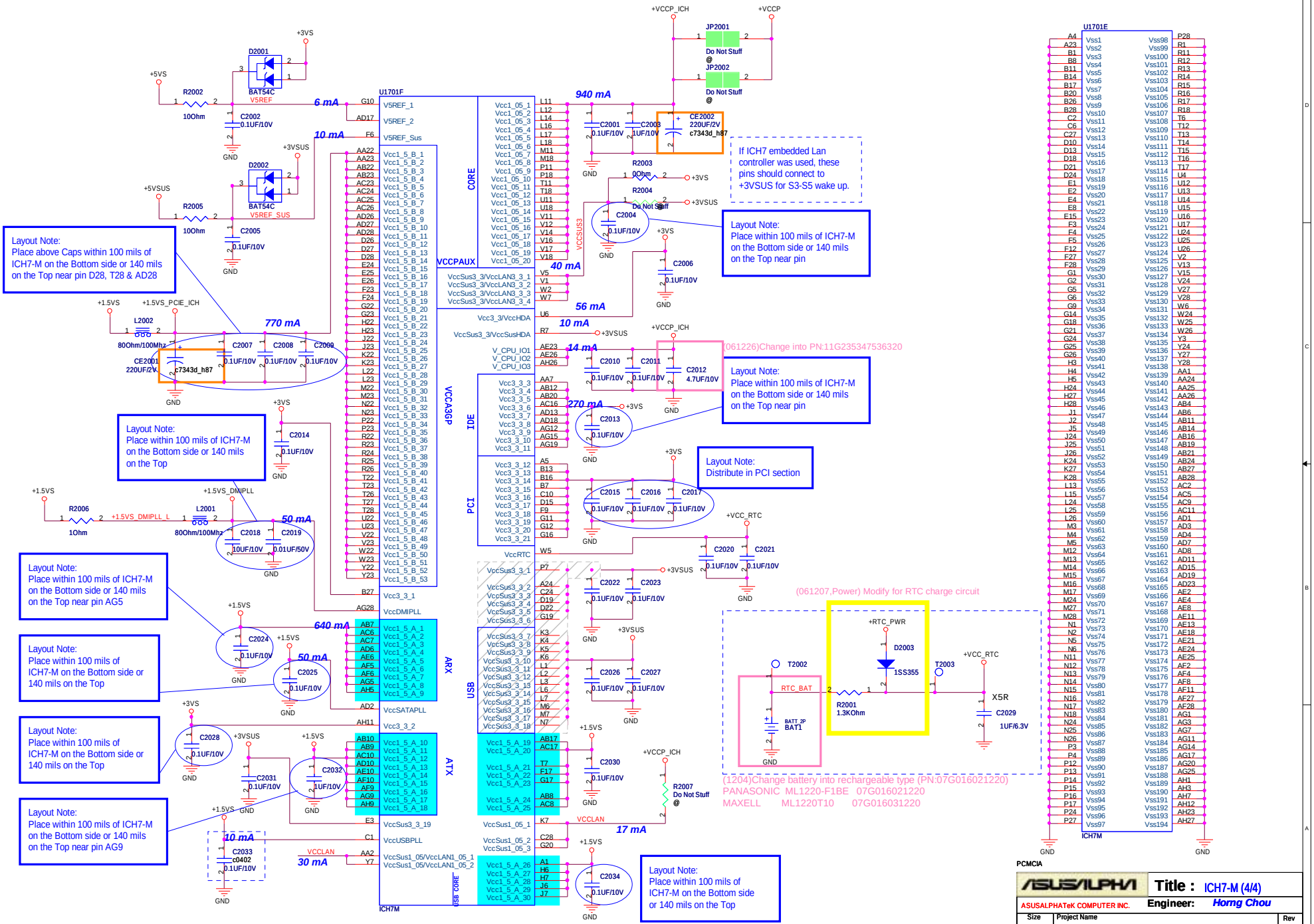
Size	Project Name	Rev
Custom	TERESA	1.1

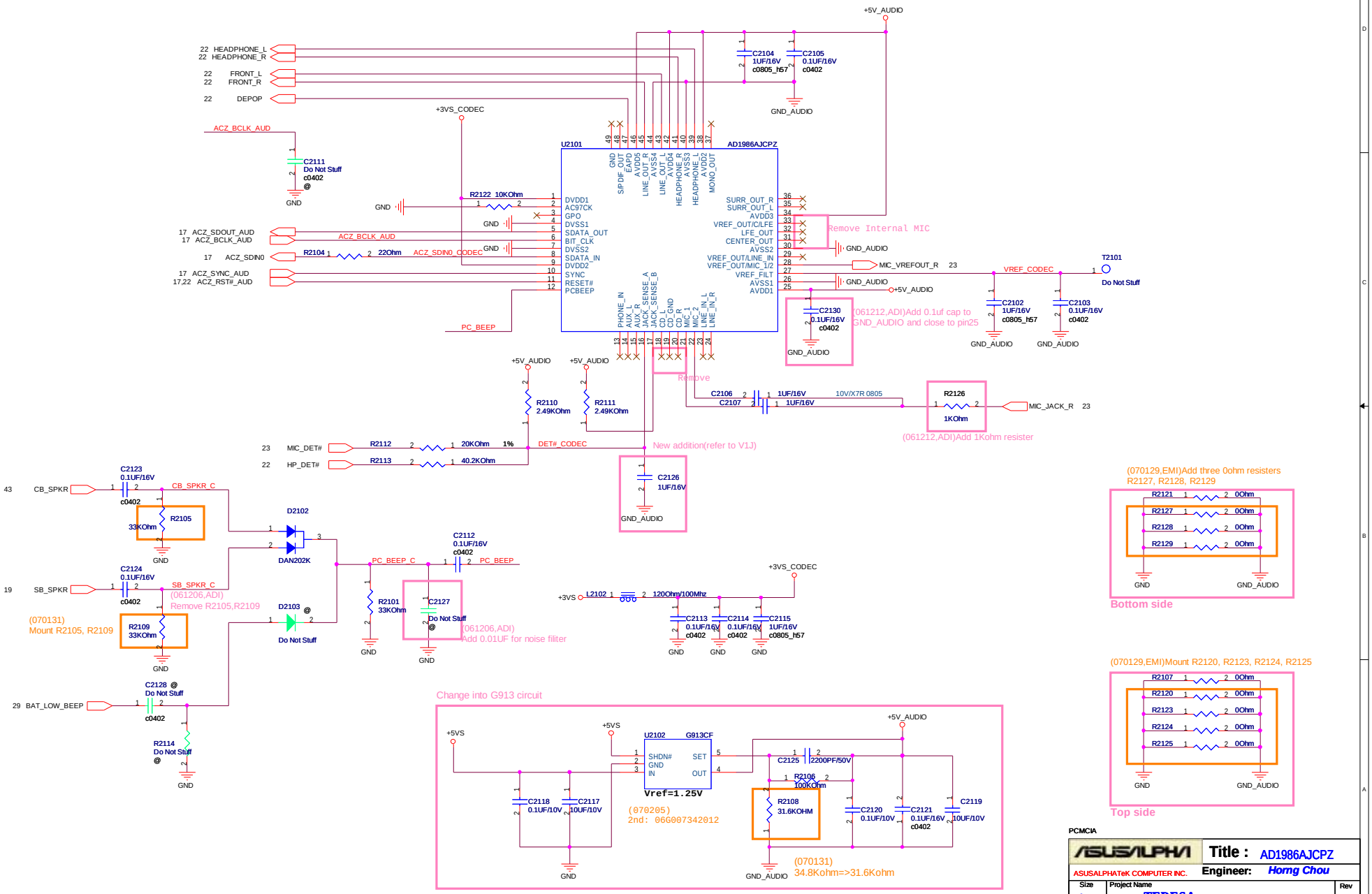
Date: Tuesday, February 06, 2007 Sheet 18 of 57



GPIO Power Plane

CPU Vcore	GPIO[49]
5V Core	GPIO[5:1]
3.3V Core	GPIO[0][7:6][23:16][39:32][48]
3.3V Resume	GPIO[15:8][31:24]


U1701F
ICH7M
U1701E
ICH7M
Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Distribute in PCI section
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
(061226)Change into PN:11G235347536320
(061207,Power) Modify for RTC charge circuit
(1204)Change battery into rechargeable type (PN:07G016021220)
PANASONIC ML1220-F1BE 07G016021220
MAXELL ML1220T10 07G016031220
PCMCIA
Title : ICH7-M (4/4)
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
Sheet 20 of 57



PCMCIA

ASUSALPHA

Title : AD1986AJCPZ

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 21 of 57

(070126) Change R2201, R2202, R2203, R2204 into 27k ohm

R2202 27KOhm
C2202 68PF/50V
R2203 27KOhm
C2203 68PF/50V

21 FRONT_R
C2206 0.47UF/16V
R2206 10KOhm
R2209 10KOhm
C2208 1UF/10V
C2209 1UF/10V X7R

U2201
RLINEIN ROUT+ → INTSPKR+
RHPIN ROUT- → INTSPKR-
RBYPASS RVDD
TJ
MUTE IN SE/BTL# → SE/BTL#
MUTE OUT HP/LINE#
SHUTDOWN LVDD
LBYPASS
NC1 NC2
GND/HS1 GND/HS2 THERMAL GND/HS3 GND/HS4
G1420F31UF

R2210 10KOhm

VDD_AMP
C2211 1UF/10V
C2213 0.1UF/16V
C2214 1UF/16V c0805_h57
C2215 1UF/16V c0805_h57
L2203 80Ohm/100Mhz
+5VS

GND_AUDIO

21 FRONT_L
C2216 1UF/10V
R2212 10KOhm
C2217 0.47UF/16V
R2214 10KOhm
LHPIN LOUT+ → INTSPKL+
LLINEIN LOUT- → INTSPKL-

C2218 68PF/50V
R2204 27KOhm
C2219 68PF/50V
R2201 27KOhm

Remove Woofer circuit

(070110)modify JACK_IN circuit
JACK_IN
R2217 100KOhm
+3VS

21 HP_DET#
SE/BTL#
Q2201 2N7002
Q2202 2N7002
Q2207 2N7002
GND

R2234 Do Not Stuff INTSPKR+
R2235 0Ohm HEADPHONE_R 21

(061212,ADI) Placing Q2203, Q2205 on the other side of CE2202, CE2201

Q2203 2N7002
Q2205 2N7002
CE2202 330UF/6.3V
CE2201 330UF/6.3V
EAR_R AOUTR_C R2221 33Ohm AJK_R
EAR_L AOUTL_C R2224 33Ohm AJK_L
L2204 1KOhm/100Mhz
L2205 1KOhm/100Mhz
R2225 1KOhm
R2226 1KOhm
GND_AUDIO

HP_JACK_R
HP_JACK_L

HP JACK
PHONE_JACK_6P
NP_NC2 NP_NC1 P_GND2 P_GND1
CON2202
GND_JACK

+3VA +12VS
R2219 10MOhm
R2220 100KOhm
R2222 100KOhm r0402
R2223 100KOhm
+3VS
Q2204 2N7002
Q2208 2N7002
Q2206 2N7002
C2222 0.47UF/16V c0603

17,21 ACZ_RST#_AUD
29 OP_SD#
D2201 BAT54WAPT
21 DEPOP

C2220 100PF/50V
C2221 100PF/50V
JACK_IN
L2201 1KOhm/100Mhz
C2223 100PF/50V

100PF/50V use 11G2330101043 11---change

(070117)Change Phone Jack into PN:12G14000106M

Change for Layout

(061213,ADI)GND_JACK connect to GND_AUDIO directly

R2236 0Ohm HEADPHONE_L 21
R2237 Do Not Stuff INTSPKL+

(070130,EMI)Add 4 Varistors(D2202~D2205)
D2202 D2203 D2204 D2205

(070117) change into 12G17100004F
CON2203 SIDE2 SIDE1
WtoB_CON_4P

To Internal Speaker Connector
INTSPKL+ R2228 120Ohm/100Mhz
INTSPKL- R2229 120Ohm/100Mhz
INTSPKR+ R2231 120Ohm/100Mhz
INTSPKR- R2232 120Ohm/100Mhz

C2224 c0402 1000PF/50V
C2225 c0402 1000PF/50V
C2226 c0402 1000PF/50V
C2227 c0402 1000PF/50V

(061206,EMI) Add one 0ohm resister
R2240 0Ohm
R2233 0Ohm

(070129,EMI)Change 0ohm resisters into beads
L2238 120Ohm/100Mhz
L2239 120Ohm/100Mhz

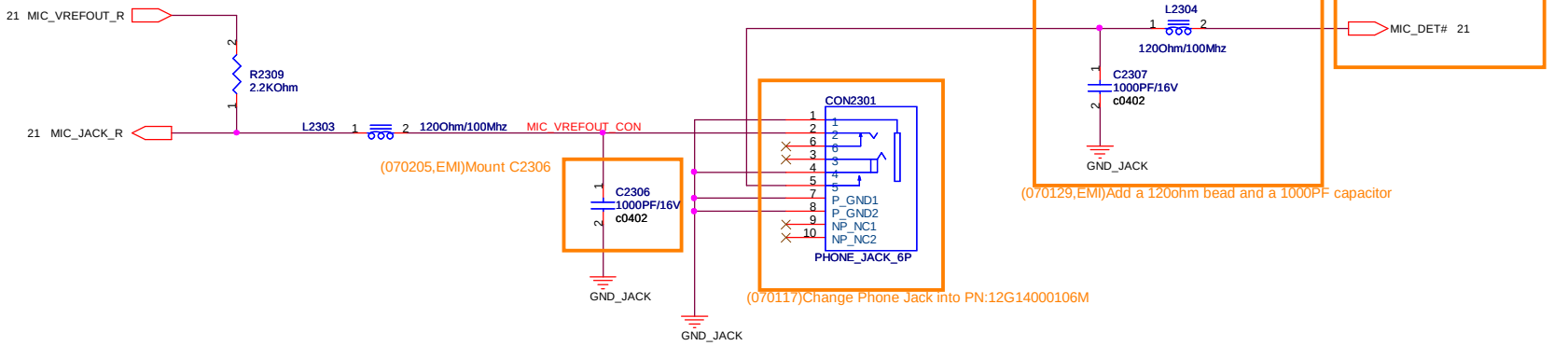
PCMCIA

ASUSALPHA	Title : AUDIO AMP	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 22 of 57	

Remove Internal MIC pre-Amplifier

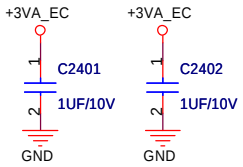
(070110)modify MIC_DET# circuit

MICROPHONE IN

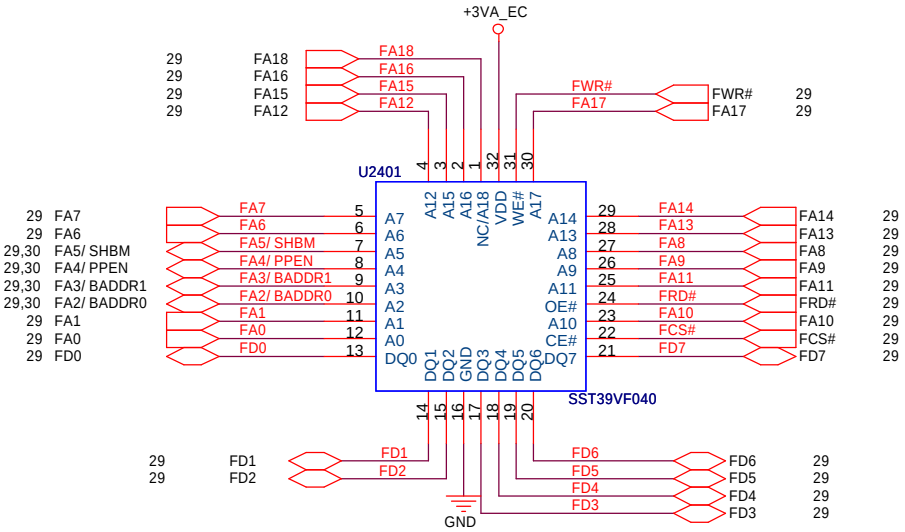


PCMCIA

ASUSALPHA	Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 23 of 57	



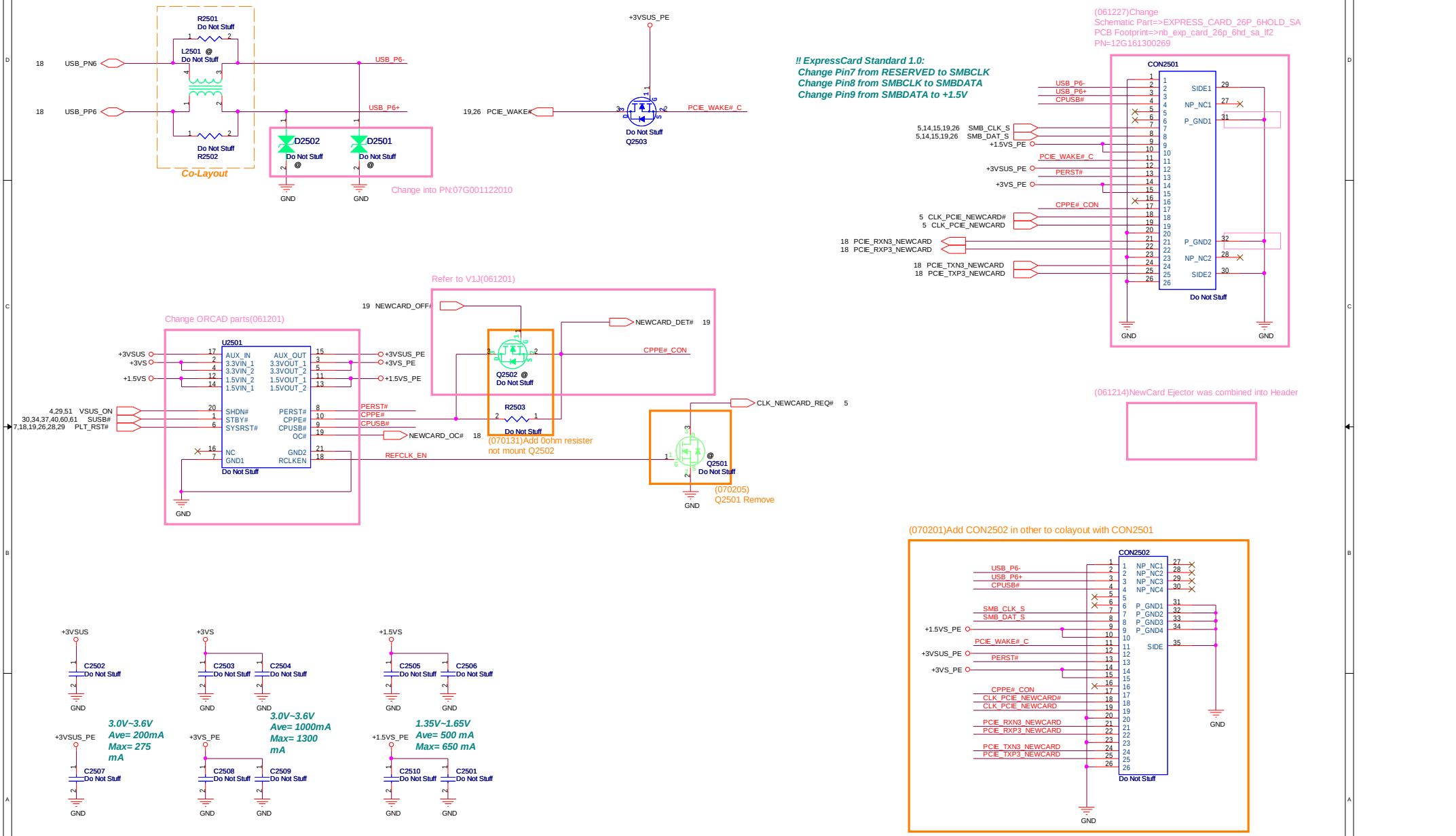
ISA ROM



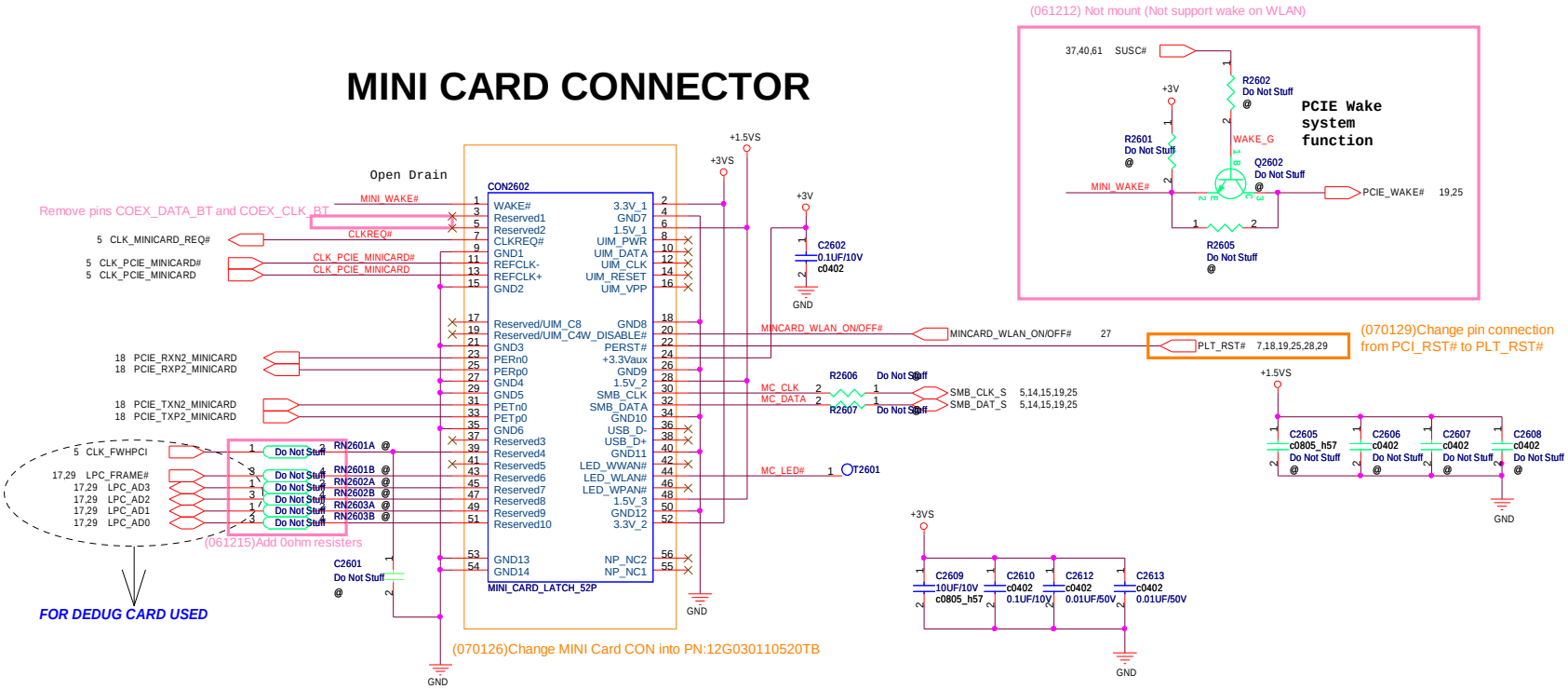
(070205)05G001014110
2nd: 05G001027221

PCMCIA

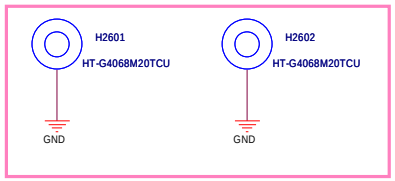
ASUSALPHATeK COMPUTER INC.	Title : ISA ROM	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 24 of 57	


NewCard Header
(061227)Change
Schematic Part=>EXPRESS_CARD_26P_6HOLD_SA
PCB Footprint=>nb_exp_card_26p_6hd_sa_lf2
PN=12G161300269
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V
R2501
Do Not Stuff
L2501 @
Do Not Stuff
R2502
Do Not Stuff
Co-Layout
USB_PN6
USB_PP6
USB_P6-
USB_P6+
D2502
D2501
Do Not Stuff
GND
Change into PN:07G001122010
+3VSUS_PE
PCIE_WAKE#
PCIE_WAKE#_C
Q2503
Do Not Stuff
CON2501
Do Not Stuff
SMB_CLK_S
SMB_DAT_S
+1.5VS_PE
+3VSUS_PE
+3VS_PE
PERST#
CPPE#_CON
CLK_PCIE_NEWCARD#
CLK_PCIE_NEWCARD
PCIE_RXN3_NEWCARD
PCIE_RXP3_NEWCARD
PCIE_TXN3_NEWCARD
PCIE_TXP3_NEWCARD
(061214)NewCard Ejector was combined into Header
Refer to V1J(061201)
Change ORCAD parts(061201)
U2501
Do Not Stuff
NEWCARD_OFF#
NEWCARD_DET#
Q2502 @
Do Not Stuff
R2503
Do Not Stuff
CLK_NEWCARD_REQ#
NEWCARD_OC#
REFCLK_EN
(070131)Add 0ohm resister
not mount Q2502
Q2501
Do Not Stuff
(070205)
Q2501 Remove
(070201)Add CON2502 in other to colayout with CON2501
CON2502
C2502
C2503
C2504
C2505
C2506
C2507
C2508
C2509
C2510
C2501
3.0V~3.6V
Ave= 200mA
Max= 275
mA
3.0V~3.6V
Ave= 1000mA
Max= 1300
mA
1.35V~1.65V
Ave= 500 mA
Max= 650 mA
PCMCIA
Title : NEWCARD
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size
Custom
Project Name
TERESA
Rev
1.1
Date: Tuesday, February 06, 2007
Sheet 25 of 57

MINI CARD CONNECTOR



Instead of Mini-PCIE latch connecter.For cost down.



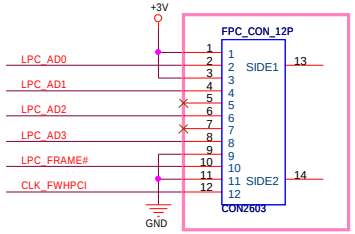
(070201)Change MINI Card NUT into PN:13G021056061TB

WLAN SPEC:

		WLL3140	WLL4080
Transmit Mode Current	11.a		550mA
	11.b	525mA	560mA
	11.g	560mA	550mA
	11.n		
Receive Mode Current	11.a		280mA
	11.b	430mA	270mA
	11.g	460mA	280mA
	11.n		
Sleep Mode Current		220mA	20mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V
	TYP	3.3V	3.3V
	MAX	3.6V	3.6V

Debug Card CON

(061206)Change Debug CON into PN:12G18340120E



PCMCIA

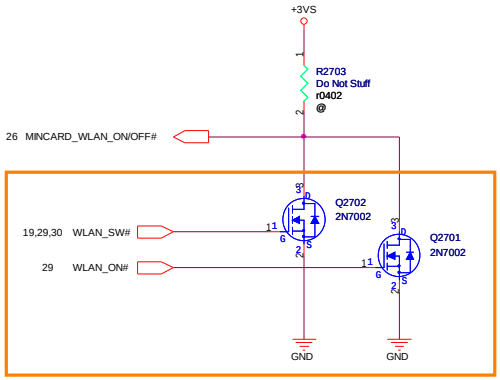
ASUSALPHA	Title : MINI PCIEX/DEBUG CON
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou
Size: Custom	Project Name: TERESA
Rev: 1.1	
Date: Tuesday, February 06, 2007	Sheet 26 of 57

For Bluetooth

Deltete Bluetooth CON

For Side SW

WLAN ON/OFF Control



(070202)Modify WLAN on/off circuit

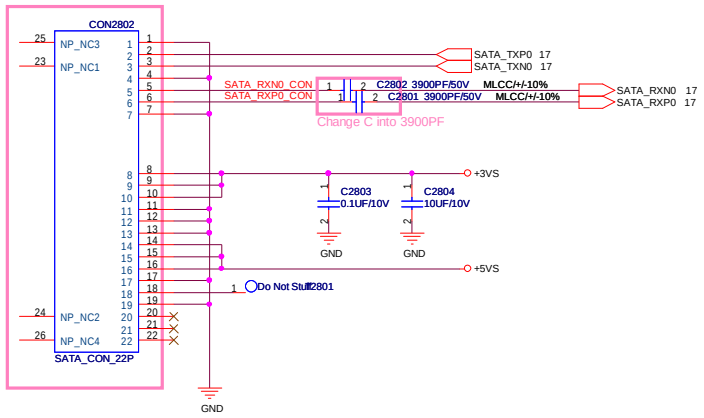
Deltete BT ON/OFF Control

Deltete FR Switch

PCMCIA

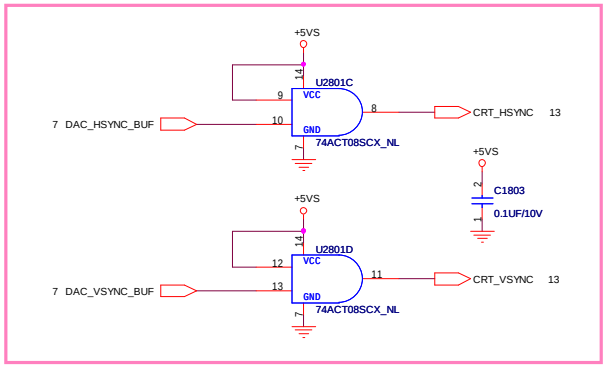
ASUSALPHA	Title : WLAN CONTROL	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 27 of 57	

(061208)Change SATA CON into PN:12G15101022A

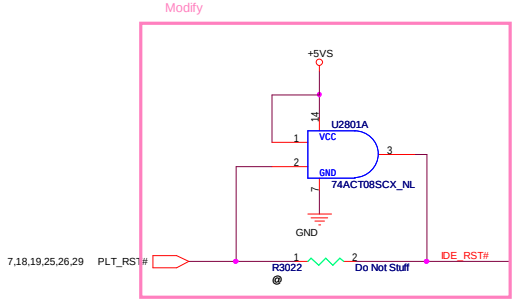


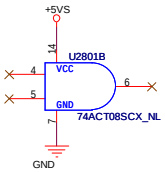
SATA HDD

Change AND gate into 5V Vcc

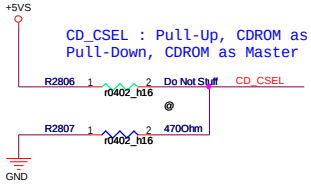


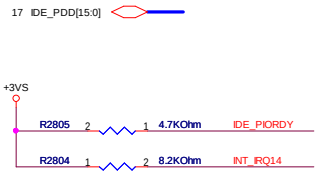
Modify

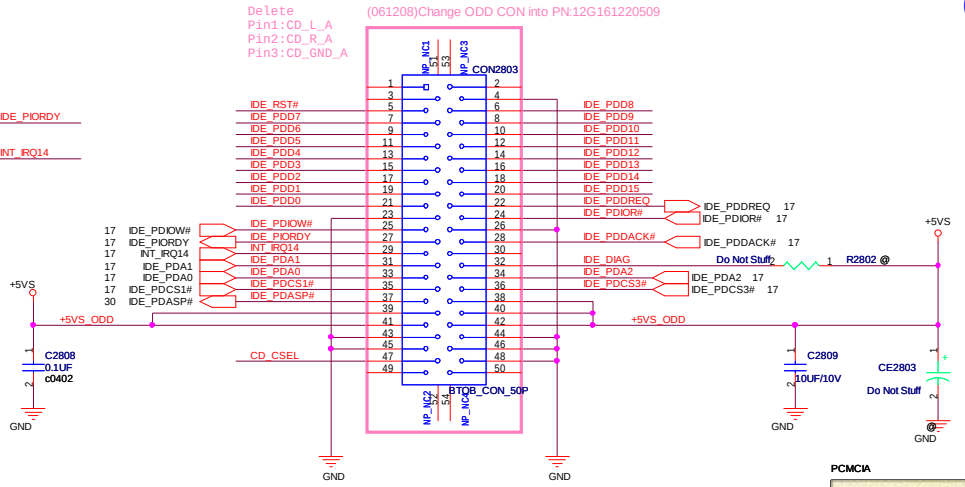




CD-ROM

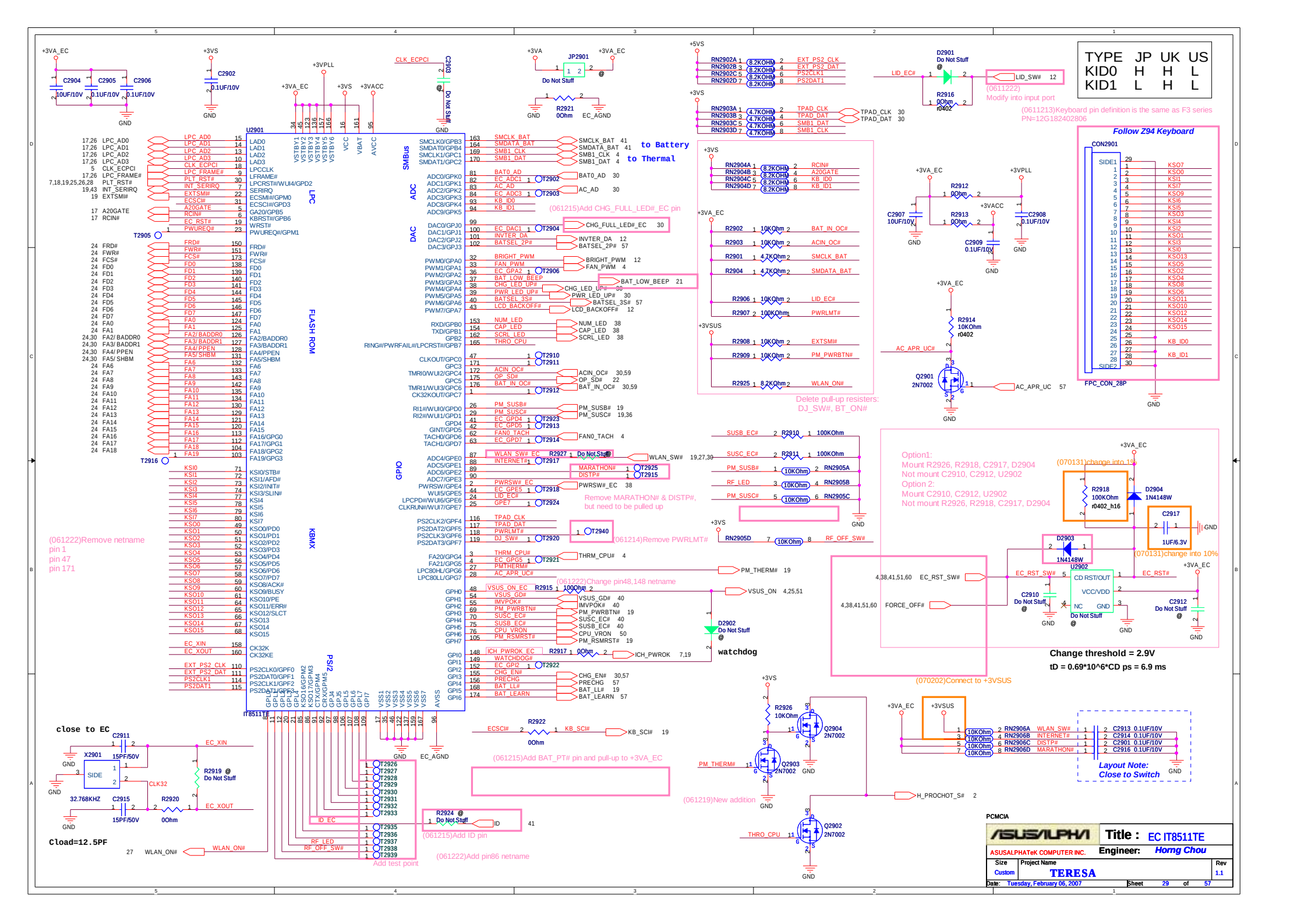






PCMCIA

ASUSALPHA	Title :	PATA-SATA & ODD
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 28 of 57	


TYPE JP UK US
KID0 H H L
KID1 L H L
U2901
IT8511TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
Follow Z94 Keyboard
CON2901
FPC_CON_28P
to Battery
to Thermal
(061215)Add CHG_FULL_LED#_EC pin
Delete pull-up resisters:
DJ_SW#, BT_ON#
Remove MARATHON# & DISTP#,
but need to be pulled up
(061214)Remove PWRLMT#
(061222)Change pin48,148 netname
watchdog
(061222)Remove netname
pin 1
pin 47
pin 171
close to EC
Cload=12.5PF
(061215)Add BAT_PT# pin and pull-up to +3VA_EC
(061219)New addition
(061215)Add ID pin
(061222)Add pin86 netname
Add test point
(061213)Keyboard pin definition is the same as F3 series
PN=12G182402806
(0611222)
Modify into input port
Option1:
Mount R2926, R2918, C2917, D2904
Not mount C2910, C2912, U2902
Option 2:
Mount C2910, C2912, U2902
Not mount R2926, R2918, C2917, D2904
(070131)change into 1%
(070131)change into 10%
(070202)Connect to +3VSUS
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
Layout Note:
Close to Switch
PCMCIA
Title : EC IT8511TE
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
Sheet 29 of 57

EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

+3VA_EC
R3002 @ Do Not Stuff r0402
FA2/ BADDR0
FA2/ BADDR0 24,29
R3006 10KOhm r0402
GND

+3VA_EC
R3003 10KOhm r0402
FA3/ BADDR1
FA3/ BADDR1 24,29
R3007 @ Do Not Stuff r0402
GND

BADDR[1:0]

No pull up:	The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:	The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:	The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

EC ADC

Battery

BAT
16.8V
R3004 @ Do Not Stuff r0402_h16
BAT0_R_AD
R3005 @ Do Not Stuff
R3008 @ Do Not Stuff
D3002 @ Do Not Stuff
D3003 @ Do Not Stuff
C3002 @ Do Not Stuff c0402
BAT0_AD 29
GND

Share Memory

+3VA_EC
R3010 10KOhm r0402
FA5/ SHBM
FA5/ SHBM 24,29
R3013 @ Do Not Stuff r0402
GND

SHBM

No pull up:	Disable shared memory with host BIOS
Ext 10K up:	Enable shared memory with host BIOS

+3VA_EC
R3001 @ Do Not Stuff r0402
FA4/ PPEN
FA4/ PPEN 24,29
R3014 10KOhm r0402
GND

PPEN

No pull up:	Normal
Ext 10K up:	KBS interface pins are switched to parallel port interface for in-system programming.

Adaptor

A/D_DOCK_IN
19V
3V
R3009 @ Do Not Stuff
AC_R_AD
R3011 @ Do Not Stuff
R3012 @ Do Not Stuff
D3001 @ Do Not Stuff
D3004 @ Do Not Stuff
C3003 @ Do Not Stuff c0402
2.99V
AC_AD 29
GND
(070205,EMI)Mount

LED Board Interface

Connect to LED Board FFC

(070131,EMI)New addition for EMI
(070205)mount
D3009 0603-050E101NP-LF
(061219)New addition for EMI

+5VSUS
+5V
C3008 0.01UF/25V
C3007 0.1UF/10V
HDD_LED#
802_LED#_R
CHG_LED#_R
PWR_LED#_R
SUSPEND_LED#
L3024 L3025 L3026 L3027 L3028 L3029 L3030 L3031 L3032 2120Ohm/100Mhz
CON3001
SIDE1 SIDE2
FPC_CON_12P
Change LED CON into PN:12G18340120E

+5VS
L3002 80Ohm/100Mhz
+5VS_TP
C3006 0.1UF/10V
19,27,29 WLAN_SW#
WLAN_SW#
CHG_FULL_LED#

Touchpad Board Interface

Connect to Touchpad Board FFC

+5VS_TP
TPAD_DAT
TPAD_CLK
C3009 0.1UF/10V
C3011 100PF/50V
C3012 100PF/50V
CON3002
SIDE1 SIDE2
FPC_CON_6P
(061215)Change TP CON into PN:12G18340060D
(070129,EMI)add two 100PF capacitors

HDD LED

+3VS +5VS
R3019 10KOhm
R3020 Do Not Stuff @
17 SATA_LED#
28 IDE_PDASP#
D3005
Do Not Stuff @
D3008
1N4148W
HDD_LED#
(061212)Modify HDD LED circuit

(061201)Modify Charge & Power circuit

CHARGE LED

+5VSUS
CHG_LED#_R
ORANGE
R3015 10KOhm
T3001
Q3003 2N7002
Q3001 2N7002
29 CHG_LED_UP#
GND

Solution 1

+3VSUS
D3007 @ Do Not Stuff
R3021 @ Do Not Stuff
29,57 CHG_EN#
U3001
C3010 Do Not Stuff @
Q3011 Do Not Stuff @
Q3006 Do Not Stuff @
29,59 ACIN_OC#
29,59 BAT_IN_OC#
CHG_FULL_LED#
GREEN
Q3005 2N7002
GND

Solution 2

R3023 10KOhm +5VSUS
29 CHG_FULL_LED#_EC
2N7002 Q3007
GND

POWER LED

25,34,37,40,60,61 SUSB#
+5V
D3006 1N4148W
R3017 10KOhm
PWR_LED#_R
GREEN
Q3008 2N7002
Q3002 2N7002
29 PWR_LED_UP#
GND
SUSPEND_LED#
ORANGE
Q3010 2N7002
GND

(061212)Modify charge full circuit : solution1 & solution2

WLAN LED

+5VS
R3016 10KOhm
802_LED#_R
Q3009 2N7002
Q3004 2N7002
Remove 0ohm
Remove RF_LED pin
19 WLAN_LED#
GND

PCMCIA

ASUSALPHA

Title : EC IT8511/LED&TP CON.

ASUSALPHATeK COMPUTER INC. **Engineer: Horng Chou**

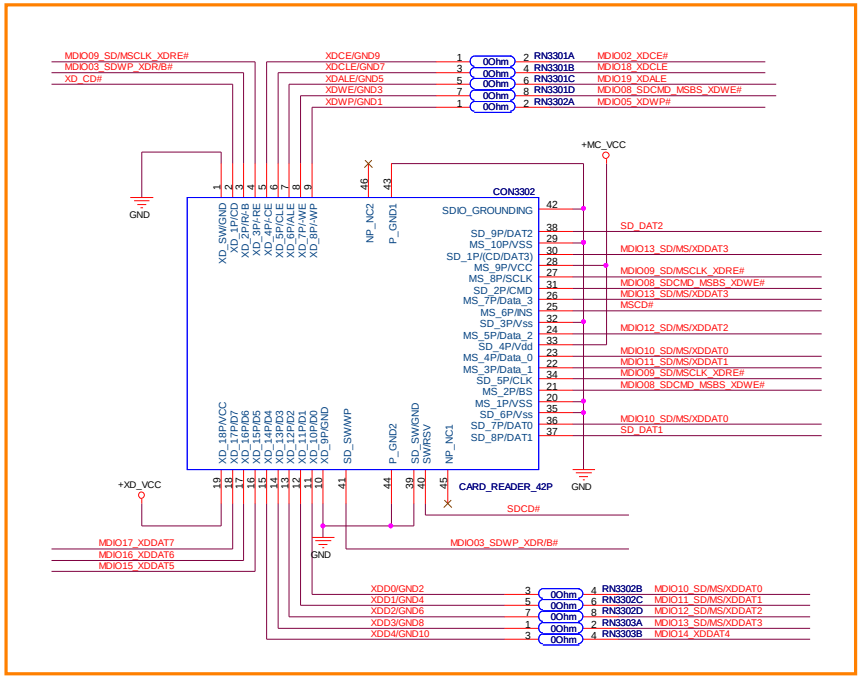
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 30 of 57

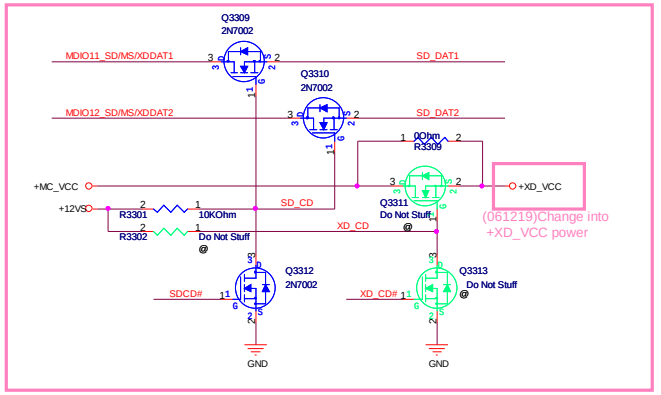
MEDIA CARD SLOT

(070124)Add Media Card CON for colayout

(070130)Add RN3301, RN3302, RN3303



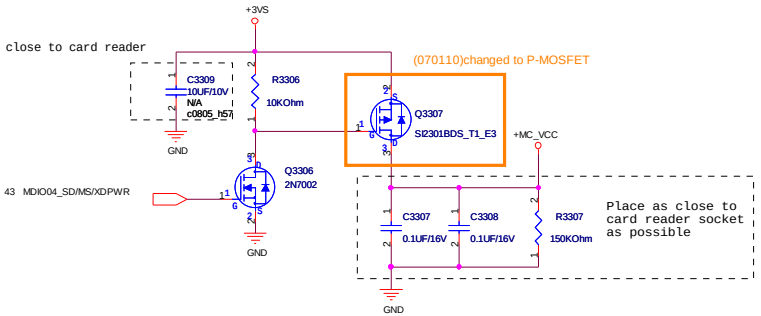
Solve-MS Duo Adaptor short problem / XD short problem



Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

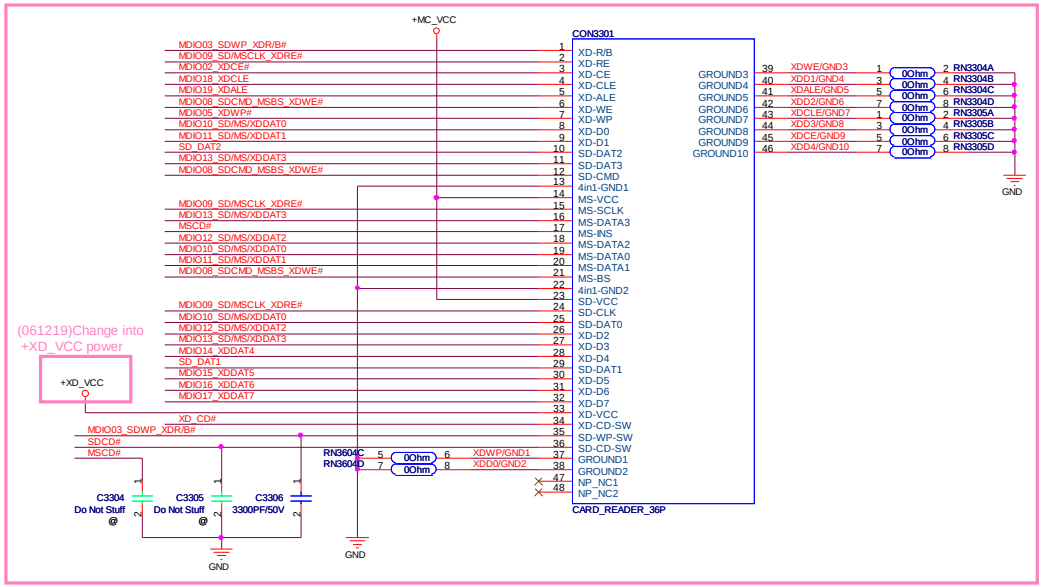
Change circuit from AAT4610A to SI2301



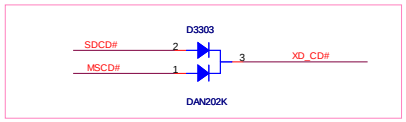
(061208)Change CON3301 into PN:12G340003601
(061225)Change schematic part & PCB Footprint

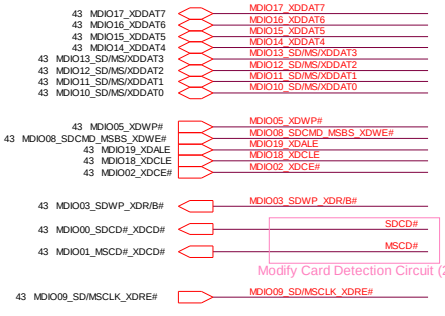
MEDIA CARD SLOT

(070130)Add RN3303, RN3304, RN3305

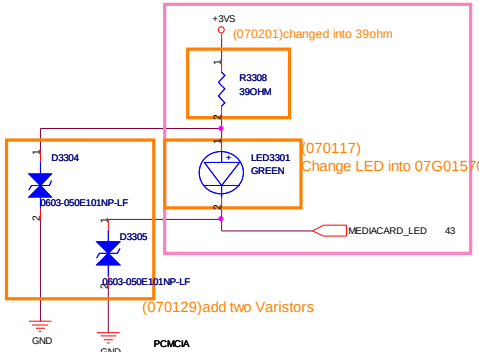


Modify Card Detection Circuit (1/2)





(161219)Change reference into R3308&LED3301



PCMCIA

ASUSALPHATeK COMPUTER INC.

Title : MEDIA CARD SLOT

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 33 of 57

Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3

(061207,REALTEK)Connect 0ohm to GND

R3412 Do Not Stuff @

PCI_AD[0..31] 18,43

18,43 PCI_C/BE#0

PCI_C/BE#1 18,43
PCI_PAR 18,43
PCI_SERR# 18,19,43
PCI_PERR# 18,19,43
PCI_STOP# 18,19,43
PCI_DEVSEL# 18,19,43
PCI_TRDY# 18,19,43

CLKRUN — R3402 @ Do Not Stuff — PM_CLKRUN# 19,43

U3401 RTL8100CL

PCI_IRDY# 18,19,43
PCI_FRAME# 18,19,43
PCI_C/BE#2 18,43
PCI_C/BE#3 18,43

R3407 33Ohm — LAN_IDSEL — PCI_AD23

R3408 need close to LAN chip

R3408 5.6KOhm 1% — LAN_RSET

XTAL1 XTAL2

L_TDP L_TDN L_RDP L_RDN CTRL25

C3405 0.1UF/10V c0402

18,19 PCI_INTA#
12,18,43 PCI_RST#
5 CLK_LAN_PCI

C3408 @ Do Not Stuff c0402

R3410 1KOhm 1% — +5VS

R3409 Do Not Stuff @

R3411 15KOhm 1%

25,30,37,40,60,61 SUSB#

PCI_PME# 18,19,43
PCI_REQ#2 18,19
PCI_GNT#2 18

(061207,REALTEK)Add voltage divider

Layout Note:
L_TDP, L_TDN termination resistors
should be near chip

C3402 0.01UF/25V — LAN_T_T — R3403 49.9Ohm 1% r0402_h16 — L_TDP 35
R3404 49.9Ohm 1% r0402_h16 — L_TDN 35

C3403 0.01UF/25V — LAN_T_R — R3405 49.9Ohm 1% r0402_h16 — L_RDP 35
R3401 49.9Ohm 1% r0402_h16 — L_RDN 35

Layout Note:
L_RDP, L_RDN termination resistors
should be near transformer

R3406 3.6KOhm r0402_h16

U3402 AT93C46 — EECS EESK EEDI/AUX EEDO

C3404 0.1UF/10V c0402

(061207)Change to PN:07G010Q12500

X3401 25Mhz — XTAL1 XTAL2

C3406 30PF/50V — C3407 30PF/50V

(070131)change into 30PF

Change trace wide into 30mil

Q3401 MW772M3L 07G003231011 — CTRL25

30 mil

C3417 10UF/10V c0805_h57
C3418 c0402 0.1UF/10V
C3419 c0402 0.1UF/10V
C3420 c0402 0.1UF/10V
C3421 c0402 0.1UF/10V

(061207,REALTEK)Recommend change to 22UF

L3401 120Ohm/100Mhz

20 mil

C3414 c0402 0.1UF/10V
C3415 c0402 0.1UF/10V
C3416 c0402 0.1UF/10V

30 mil

C3409 c0402 0.1UF/10V
C3410 10UF/10V c0805_h57
@ C3401 c0402 Do Not Stuff
@ C3411 c0402 Do Not Stuff
@ C3412 c0402 Do Not Stuff
@ C3413 c0402 Do Not Stuff

(061207,REALTEK)Remove capacitors

PCMCIA

ASUSALPHA
ASUSALPHATeK COMPUTER INC.

Title : LAN_RTL8100CL
Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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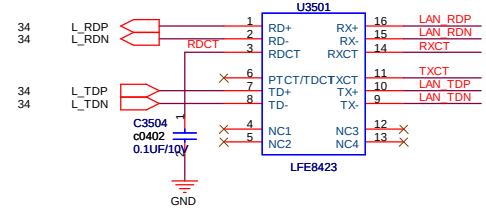
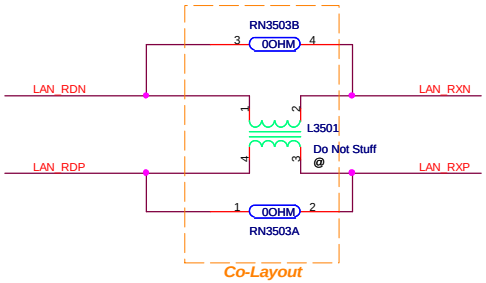
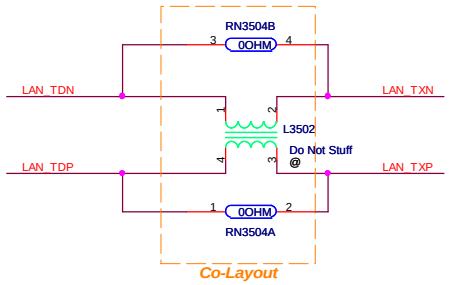
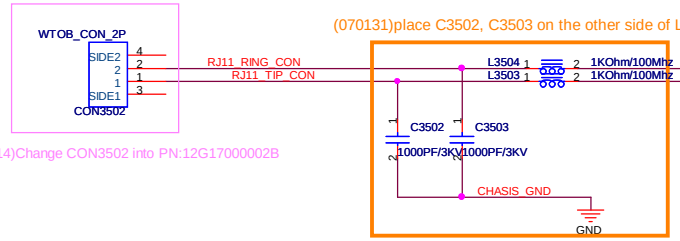
LAN PORT

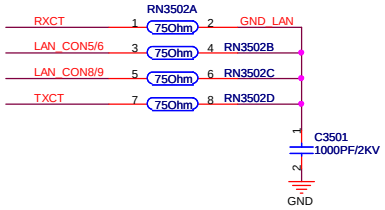
TRANSFORMER 10/100MB



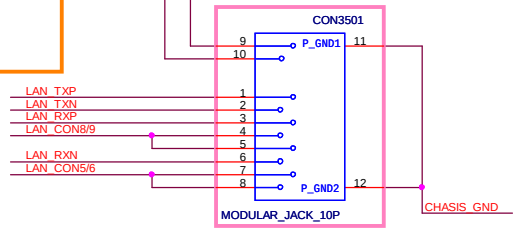






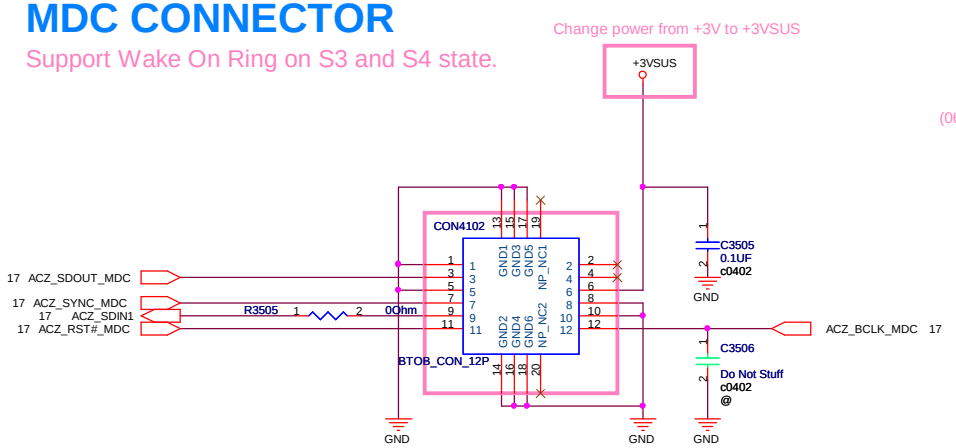


RJ11&RJ45



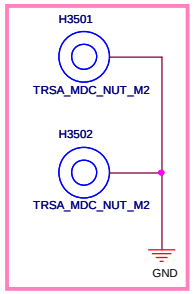
MDC CONNECTOR

Support Wake On Ring on S3 and S4 state.



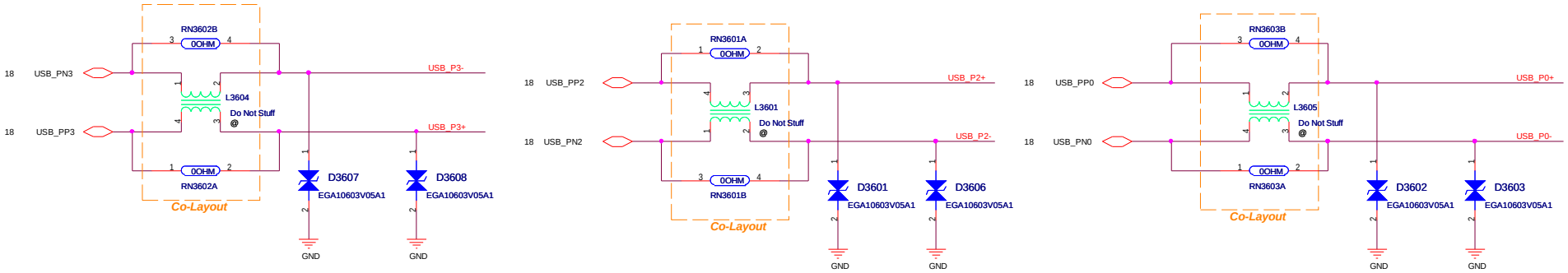
B:MDC NUT

(061219)Change MDC NUT into PN:13G021054000



PCMCIA

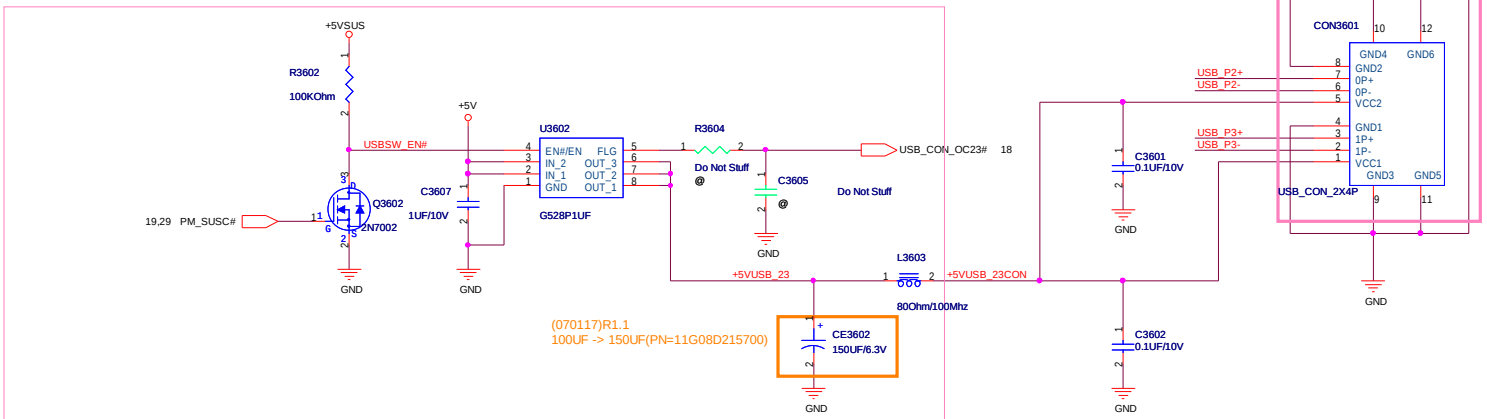
ASUSALPHA	Title : RJ45/RJ11/MDC	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 35 of 57	



Delete N-MOSFET PMN45EN

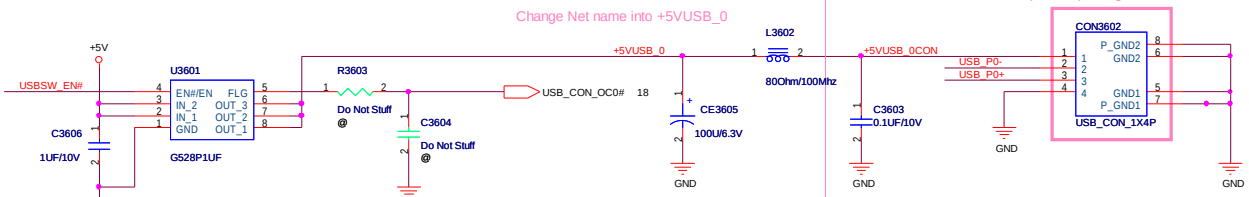
(061211)Change USB CON into PN:12G13111108F

Add USB Switch



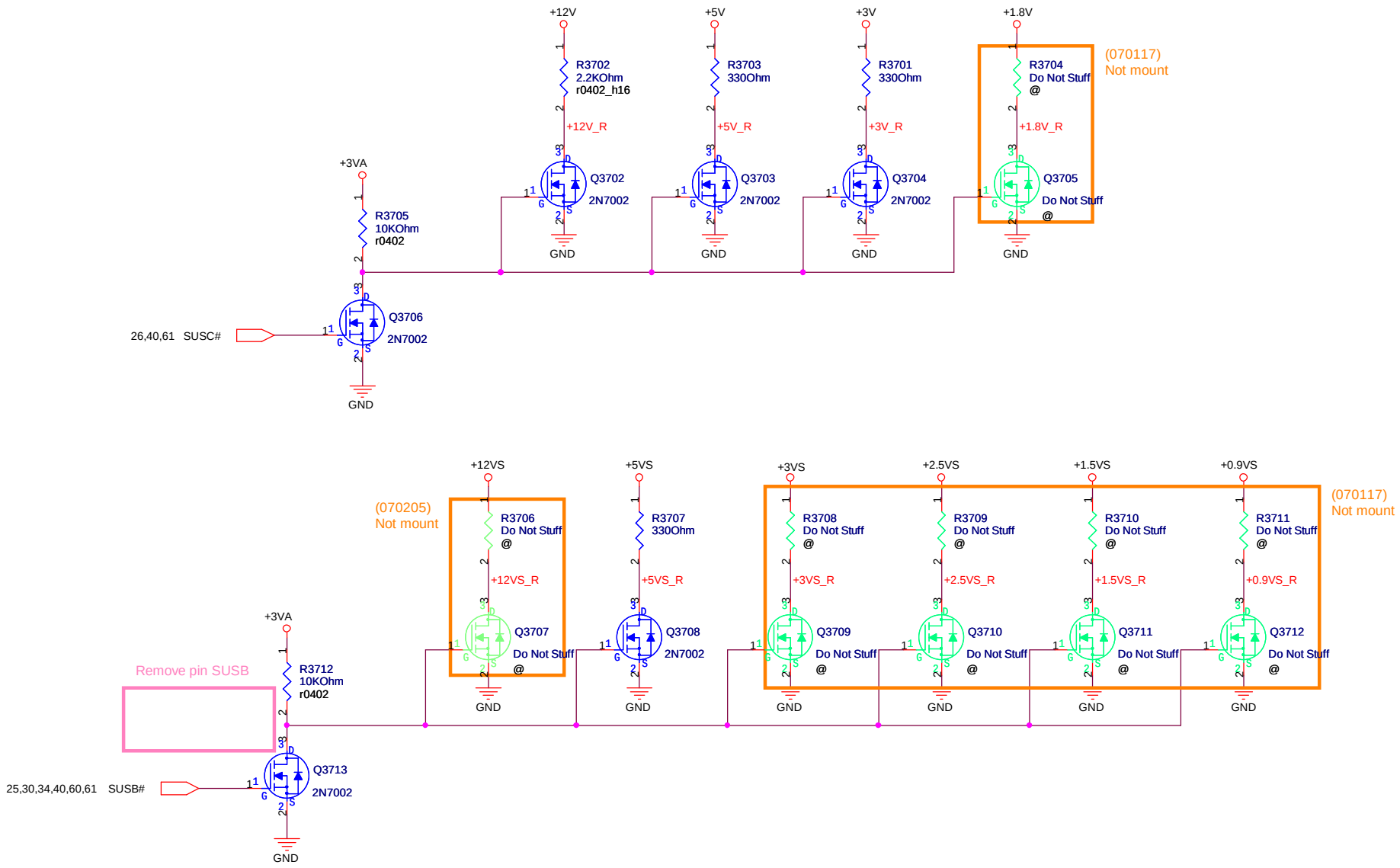
Change Net name into +5VUSB_0

(061206)Change USB CON into PN:12G131030043



PCMCIA

ASUSALPHA	Title : USB CONN x3	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 36 of 57	



PCMCIA

ASUSALPHA	Title : Discharge Circuit	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 37 of 57	

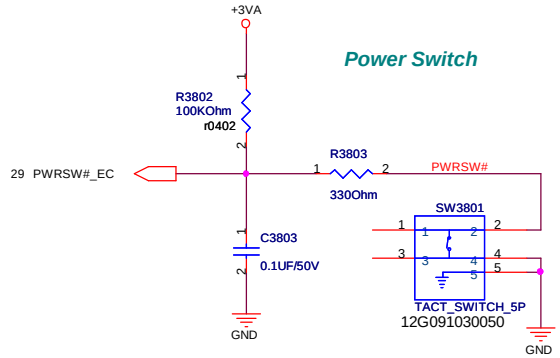
Main Board SW & LED

Power LED move to daughter board

Delete RF/Touchpad and Power4 Gear SWITCH

Delete RF LED and Power4 Gear LED

Power Switch

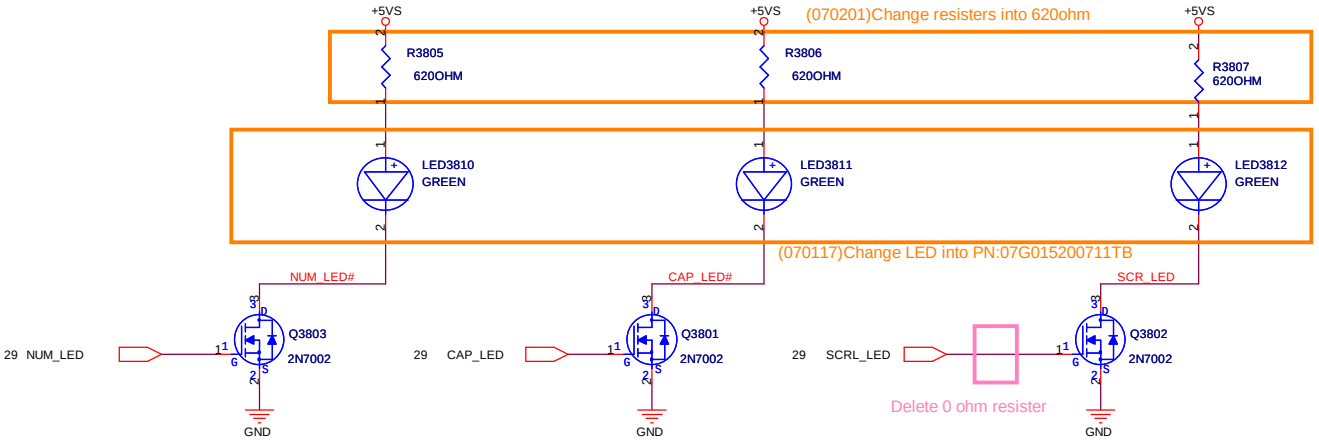


NUMBER LOCK LED

CAPS LOCK LED

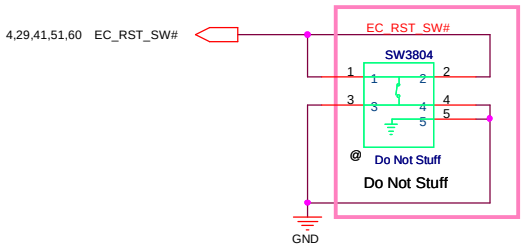
SCROLL LOCK LED

(070201)Change resisters into 620ohm



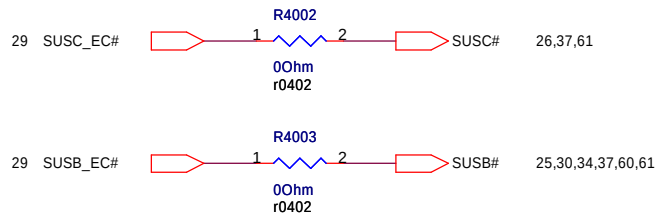
Reset Switch

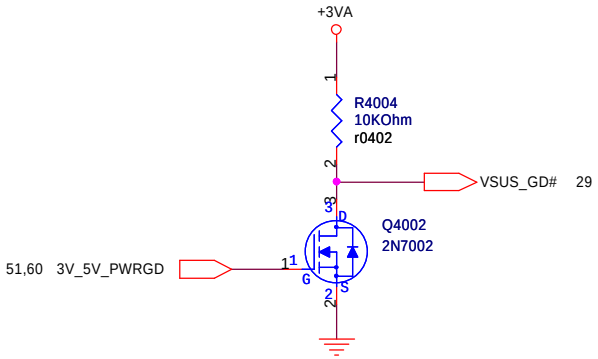
SW does not mount

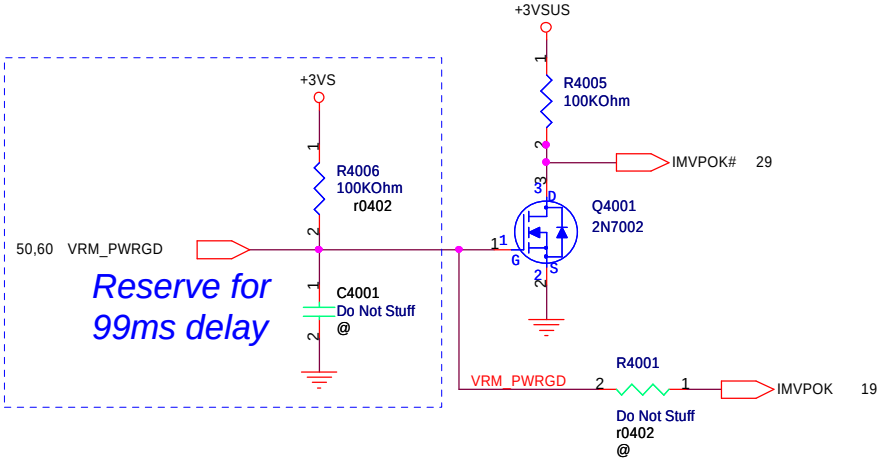


PCMCIA

ASUSALPHATeK COMPUTER INC.	Title : SW/LED	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 38 of 57	



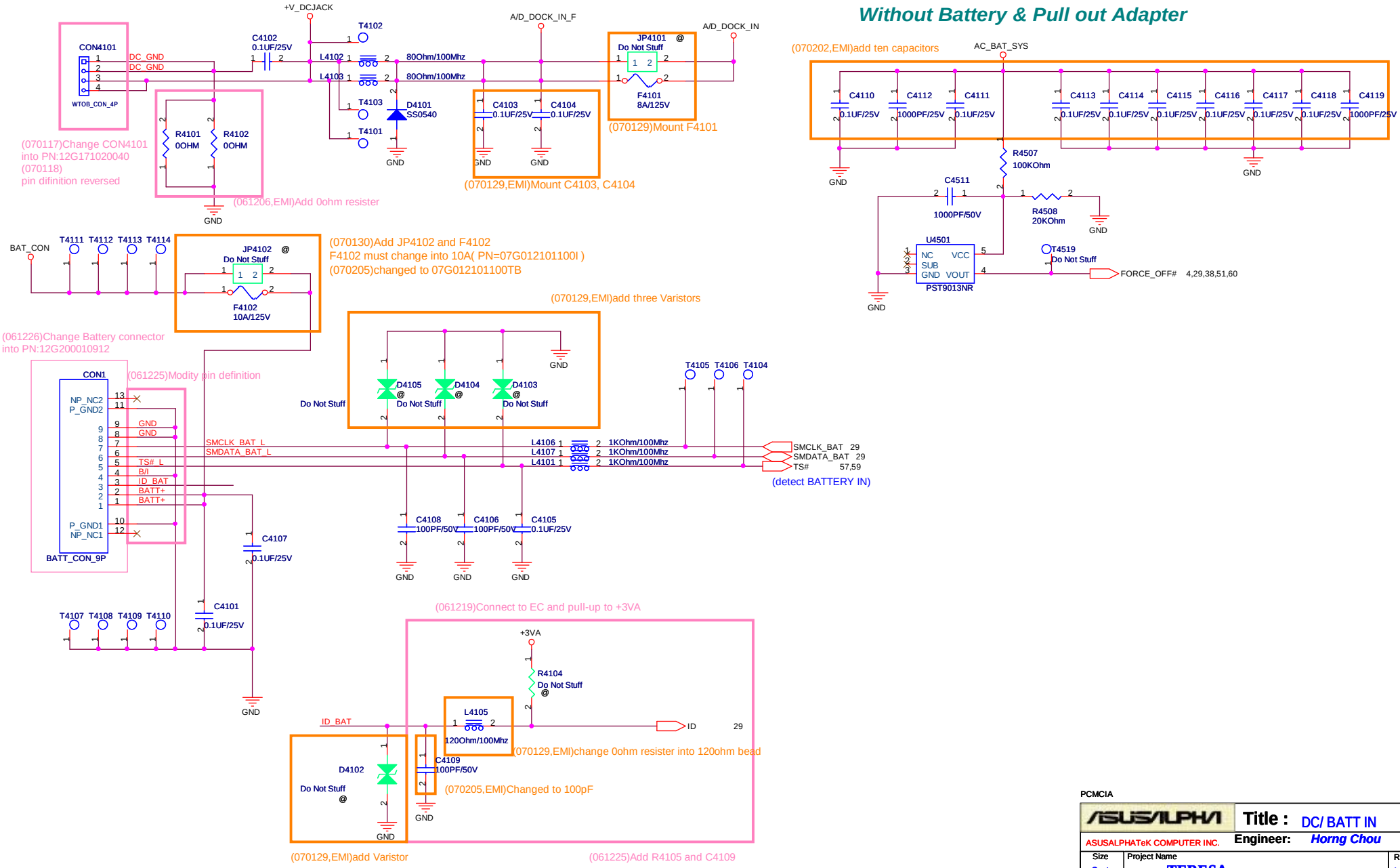




PCMCIA

ASUSALPHA	Title : POWER-ON SEQ.	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 40 of 57	

DC Power Jack



PCMCIA

ASUSALPHA

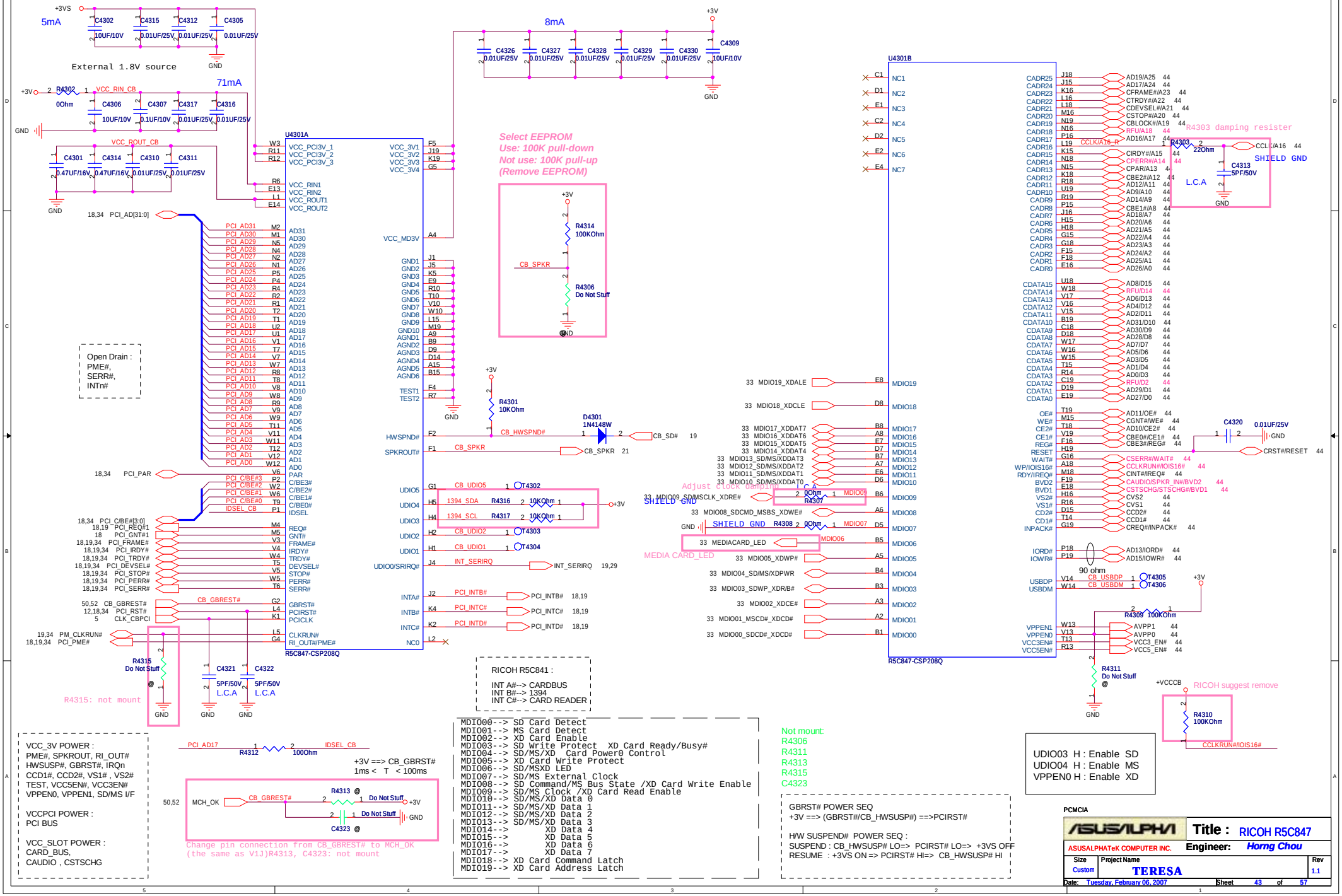
Title : DC/ BATT IN

ASUSALPHATeK COMPUTER INC.

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 41 of 57


5mA
8mA
71mA
External 1.8V source
U4301A
R5C847-CSP208Q
U4301B
Select EEPROM
Use: 100K pull-down
Not use: 100K pull-up
(Remove EEPROM)
R4314 100KOhm
R4306 Do Not Stuff
R4303 damping resister
R4303 22Ohm
C4313 5PF/50V
L.C.A
SHIELD GND
Open Drain :
PME#,
SERR#,
INTn#
R4301 10KOhm
D4301 1N4148W
Adjust clock damping
R4307 0Ohm
R4308 0Ohm
MEDIA CARD_LED
90 ohm
R4309 100KOhm
R4311 Do Not Stuff
R4310 100KOhm
RICOH suggest remove
R4315 Do Not Stuff
R4315: not mount
C4321 5PF/50V L.C.A
C4322 5PF/50V L.C.A
R4312 100Ohm
+3V ==> CB_GBRST#
1ms < T < 100ms
R4313 @ Do Not Stuff
C4323 @ Do Not Stuff
Change pin connection from CB_GBREST# to MCH_OK
(the same as V1J)R4313, C4323: not mount
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
Not mount:
R4306
R4311
R4313
R4315
C4323
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCMCIA
ASUSALPHATeK COMPUTER INC.
Title : RICOH R5C847
Engineer: Horng Chou
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
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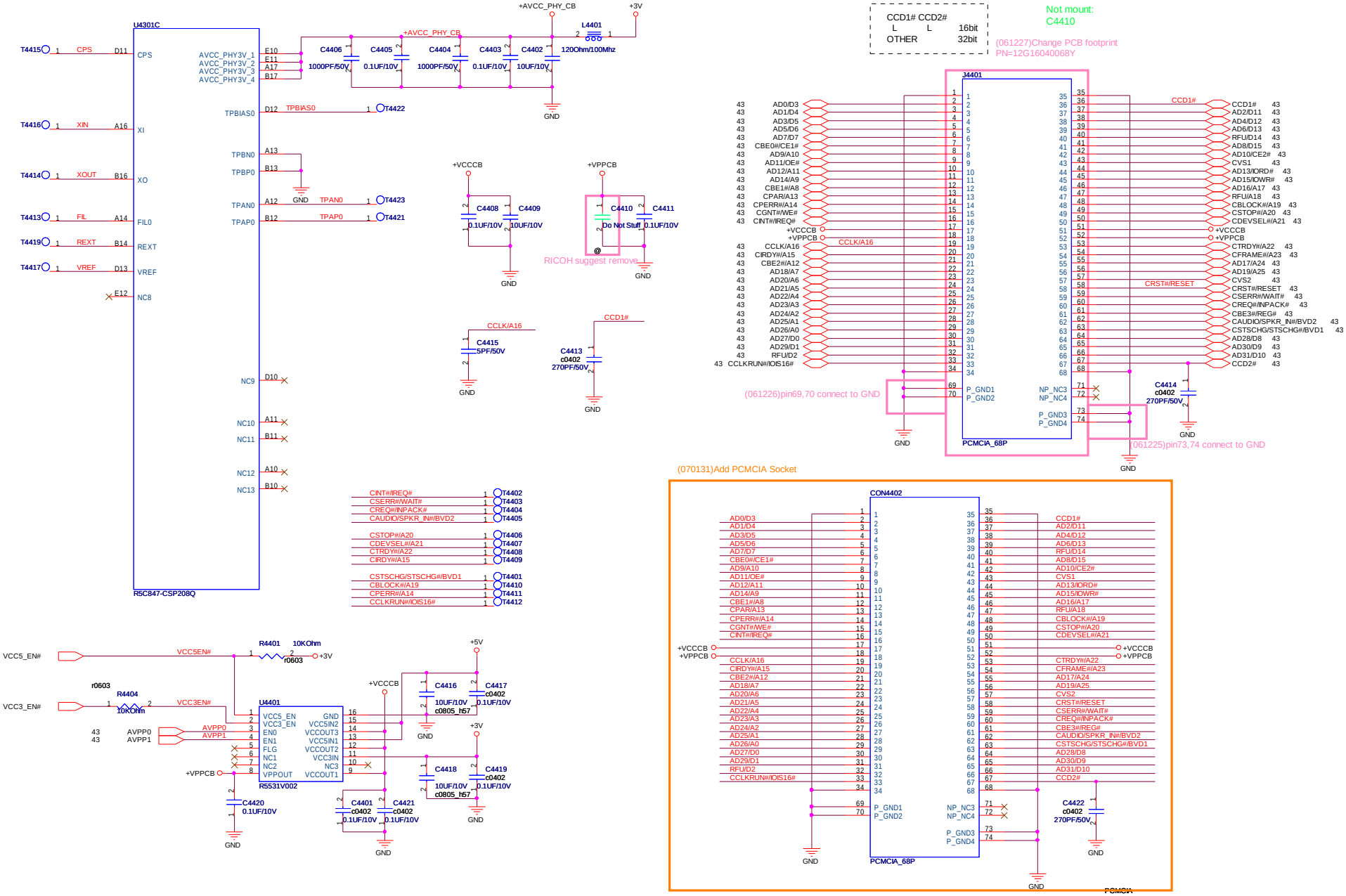
PCMCIA SOCKET



CCD1# CCD2#
L L 16bit
OTHER 32bit

Not mount:
C4410

(061227)Change PCB footprint
PN=12G16040068Y

(061226)pin69,70 connect to GND

(061225)pin73,74 connect to GND

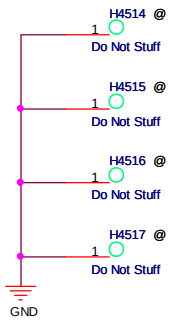
(070131)Add PCMCIA Socket

PCMCIA

ASUSALPHA	Title : CARDBUS SOCKET	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 44 of 57	

A:CPU BKT

PN:s01756



B:MDC NUT

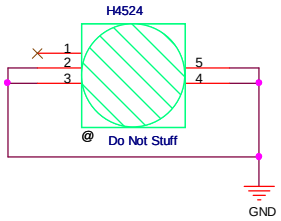
MDC NUT put on page35 (H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on page26(H2601, H2602)

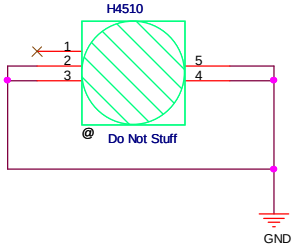
C:TOP TO BTM

PN:S01912



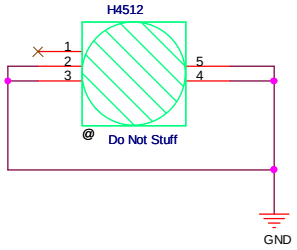
D:FIX MB

PN:s01769



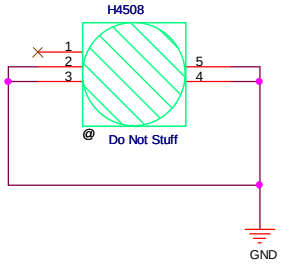
E:TOP TO BTM

PN:S01911



G:FIX MB

PN:s01783



H:SYS BOSS

PN:S01914

I:MB TO IO BKT

PN:S01913

J:SYS BOSS

PN:S01915

K:MB TO IO BKT

PN:S01705

L:TOP TO BTM

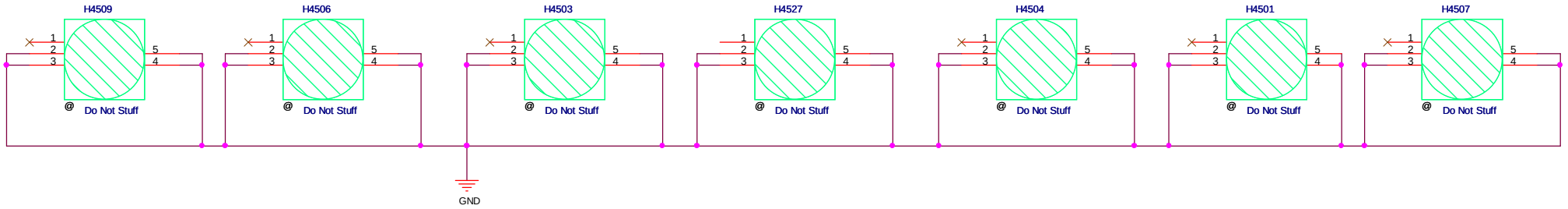
PN:S01916

M:SYS BOSS

PN:s01917

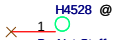
N:TOP TO BTM

PN:S01851



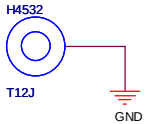
O:ALIGNMENT HOLE

PN:temp_5262_gh15



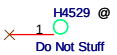
T:NB SINK NUT

PN:13GNJ510M170-1



P:ALIGNMENT HOLE

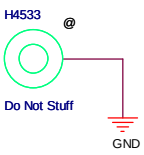
PN:s01724



EMI NUT

for LVDS cable

PN:13G021029050



U:TOP TO BTM

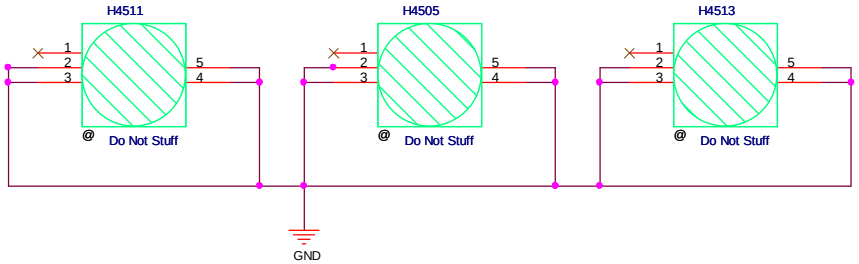
PN:S01854

V:TOP TO BTM

PN:S01857

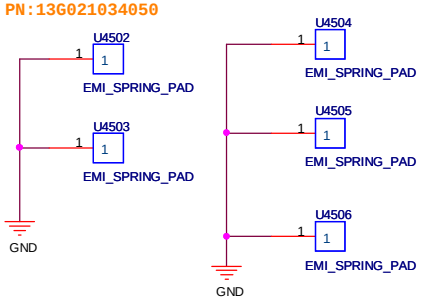
W:TOP TO BTM

PN:S01918



EMI SPRING

PN:13G021034050



PCMCIA

ASUSALPHA	Title : SCREW HOLE	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 45 of 57	

R1.0 to R1.1

Page	Action
3	Change C304, C305, C306, C307, C308, C310, C312, C313 into 10UF for cost down.
4	Add R418 and Q404 to avoid error action.
7	Add R715 and R716 in other to improve signal quality.
12	Mount R1206 and Q1204 in other to reduce discharge time.
13	Change C1313, C1314 into 22PF in other to improve undershoot.
13	Change the rated current of the fuse(F1302) into 1A for customer's demand.
21	Mount R2105 and R2109, or there is no dialing tone.
21	Modify R2108 into 31.6Kohm in other to tune +5V_AUDIO.
21	Add three 0ohm resisters R2127, R2128, R2129 for EMI.
22	Change R2201~R2204 into 27Kohm for speaker volume.
22	Change 0ohm resisters(R2238, R2239) into beads.
22	Remove a N-MOS and a resistor on JACK_IN side due to change a new HP JACK.
22	Add 4 Varistors(D2202~D2205) for EMI.
23	Remove a N-MOS due to change a new MIC JACK.
23	Add a 120ohm bead L2304 and a 1000PF capacitor C2307 for EMI.
25	Add 0ohm resister R2503 and change Q2502 into unmount.
25	Add CON2502 in other to colayout with CON2501.
26	Connect not PCI_RST# but PLT_RST# to the RESET# signal of PCIE MiniCard for customer's demand.
27	Connect pin20 of MiniCard to the signal of OR conditions of WLAN_SW# and WLAN_ON# for customer's demand.
29	Change tolerance of R2918 into 1% and C2917 into 10% for the timing of EC_RST#.
29	Change WLAN_SW# into pull-up +3VSUS
30	Add 100PF capacitors C3011 and C3012 for EMI.
33	Add CON3302, RN3301, RN3302, RN3303, RN3304, RN3305 in other to colayout with CON3301.
33	Add Varistors D3304 and D3305 for EMI.
33	Change R3308 into 39ohm for the brightness of LED3301.
34	Change C3406, C3407 into 30PF in other to fit 25MHz frequency.
35	Place C3502, C3503 on the other side of L3503, L3504 for layout.
36	Change CE3602 from 100UF to 150UF in other to fit droop SPEC.
37	Change R3704, Q3705, R3708, Q3709, R3709, Q3710, R3710, Q3711, R3711, Q3711 into unmount because they don't affect the discharge circuit.
38	Change resisters R3805, R3806, R3807 into 620ohm in other to tune brightness.
41	Change the fuse F4101 into mount for customer's demand.
41	Add the colayout of JP4102 and F4102 for customer's demand.
41	Change 0ohm resister R4105 into 120ohm bead L4105 for EMI.
41	Add four Varistors D4102, D4103, D4104, D4105 and ten capacitors C4110~C4119 for EMI.
41	Chane C4103, C4104 into mount for EMI.
70	Chane R7002 into 80.6ohm for brightness.

R1.1 to R1.2

Page	Action

R1.2 to R2.0

Page	Action	Reason

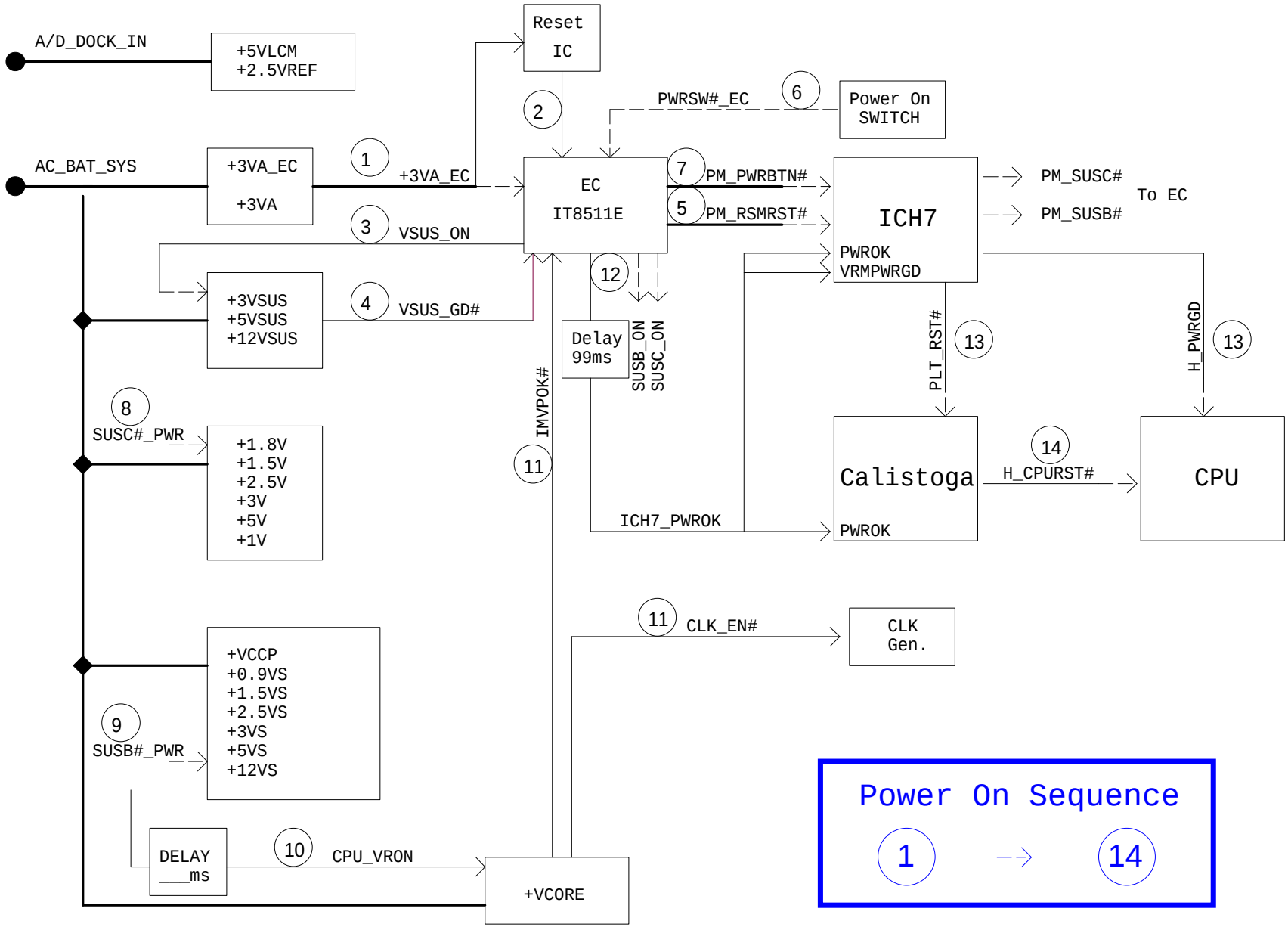
PCMCIA

ASUSALPHA | Title : HISTORY

ASUSALPHATeK COMPUTER INC. | Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 | Sheet 46 of 57



PCMCIA

ASUSALPHA	Title :	FLOWCHART
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 47 of 57	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	O	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	BAT_LOW_BEEP(Reserved)	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCHDOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	/	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	/	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I			/	
1	CK32KOUT/GPC7	/	O			/	
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	BAT0_AD	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	AC_AD	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID0	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	/	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	/	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	/	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	/	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AC18	GPIO07	PM_THERM#_GPIO (Reserved)	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_SW#_ICH	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	NEWCARD_DET#	I
R4	GPIO14	BAT_LL#_ICH (Reserved)	I
E22	GPIO15	WLAN_LED#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STPPCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STPCPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	REQ4#/GPIO22	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	CB_SD#	O
A21	GPIO26	/	
B21	GPIO27	BTO_DEV0	I
E23	GPIO28	NEWCARD_OFF#	O
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AC19	GPIO33/AZ_DOCK_EN#	BTO_DEV1	I
U2	GPIO34/AZ_DOCK_RST#	BTO_DEV2	I
AD21	GPIO35	/	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12F
Pink: different from T12F

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

PCMCIA

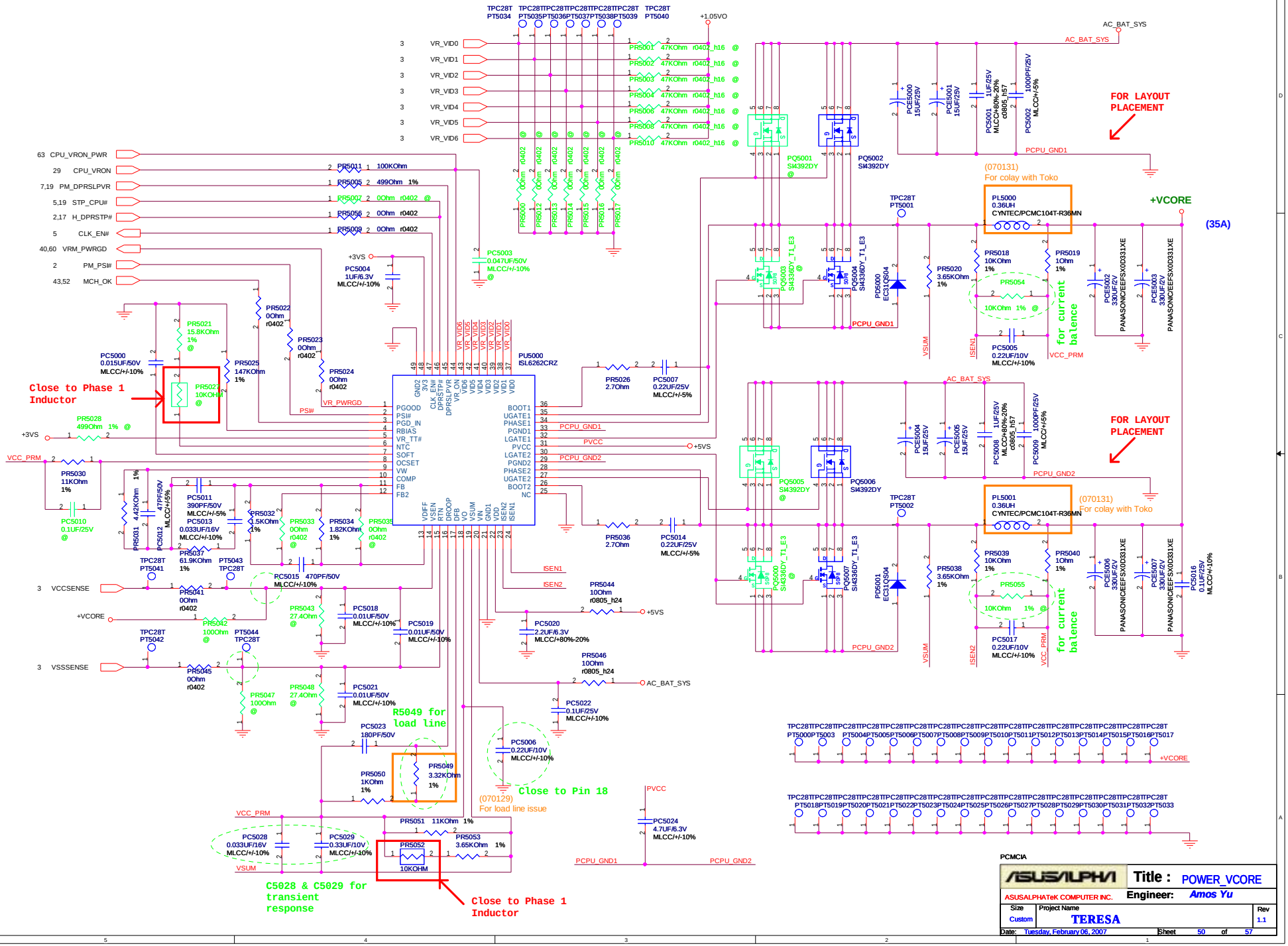
ASUSALPHA

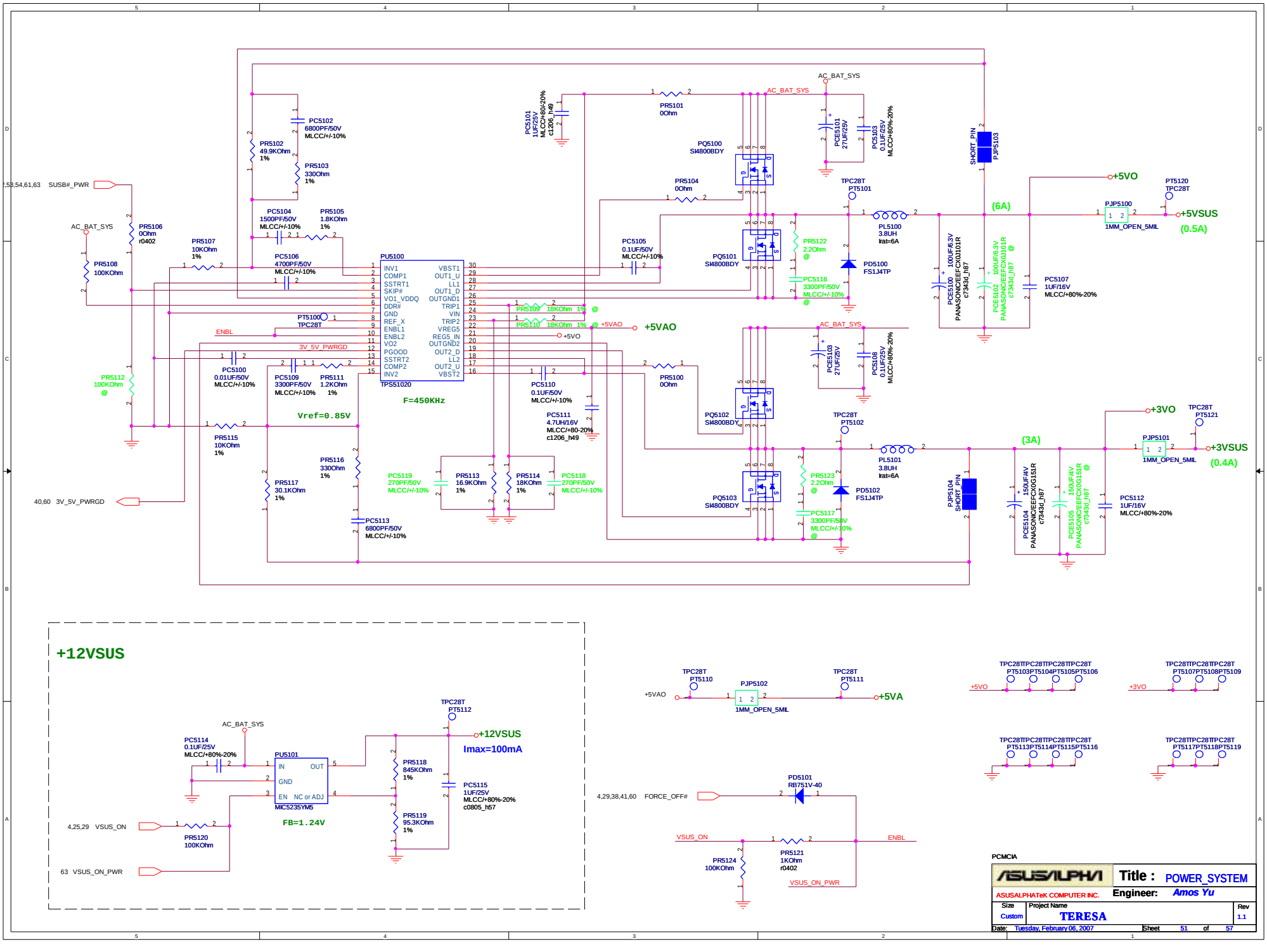
Title : GPIO Setting

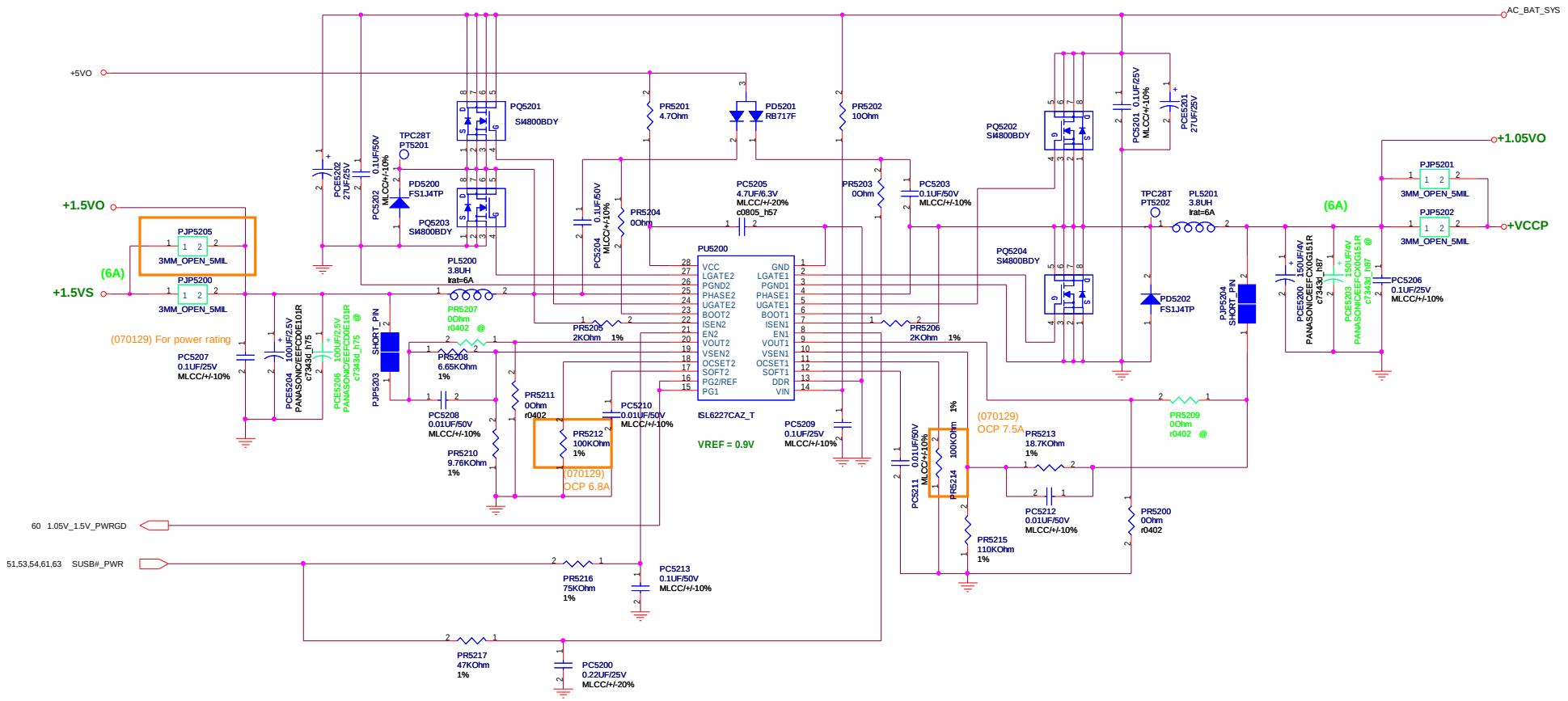
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 48 of 57


+VCORE
(35A)
FOR LAYOUT PLACEMENT
for current balence
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
(070129)
For load line issue
C5028 & C5029 for transient response
Close to Phase 1 Inductor
(070131)
For colay with Toko
PU5000 ISL6262CRZ
PCMCIA
Title : POWER_VCORE
ASUSALPHATeK COMPUTER INC.
Engineer: Amos Yu
Size: Custom
Project Name: TERESA
Rev: 1.1
Date: Tuesday, February 06, 2007
Sheet 50 of 57


+12VSUS
Imax=100mA
FB=1.24V
PU5101
MIC5235YM5
PC5114
0.1UF/25V
MLCC/+80%-20%
PR5118
845KOhm
1%
PR5119
95.3KOhm
1%
PC5115
1UF/25V
MLCC/+80%-20%
c0805_h57
PR5120
100KOhm
4,25,29 VSUS_ON
63 VSUS_ON_PWR
TPC28T
PT5112
AC_BAT_SYS
PD5101
RB751V-40
4,29,38,41,60 FORCE_OFF#
VSUS_ON
ENBL
PR5124
100KOhm
PR5121
1KOhm
r0402
VSUS_ON_PWR
+5VAO
PJP5102
1MM_OPEN_5MIL
+5VA
PT5110
PT5111
PU5100
TPS51020
F=450KHz
Vref=0.85V
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
PR5100
0Ohm
PR5101
0Ohm
PR5102
49.9KOhm
1%
PR5103
330Ohm
1%
PR5104
0Ohm
PR5105
1.8KOhm
1%
PR5106
0Ohm
r0402
PR5107
10KOhm
1%
PR5108
100KOhm
PR5109
3300PF/50V
MLCC/+/-10%
PR5110
0.1UF/50V
MLCC/+/-10%
PR5111
1.2KOhm
1%
PR5112
100KOhm
@
PR5113
16.9KOhm
1%
PR5114
18KOhm
1%
PR5115
10KOhm
1%
PR5116
330Ohm
1%
PR5117
30.1KOhm
1%
PR5122
2.2Ohm
@
PR5123
2.2Ohm
@
PR5126
18KOhm 1%
PR5127
18KOhm 1%
PC5100
0.01UF/50V
MLCC/+/-10%
PC5101
1UF/25V
MLCC/+80%-20%
c1206_h49
PC5102
6800PF/50V
MLCC/+/-10%
PC5103
0.1UF/25V
MLCC/+80%-20%
PC5104
1500PF/50V
MLCC/+/-10%
PC5105
0.1UF/50V
MLCC/+/-10%
PC5106
4700PF/50V
MLCC/+/-10%
PC5107
1UF/16V
MLCC/+80%-20%
PC5108
0.1UF/25V
MLCC/+80%-20%
PC5109
3300PF/50V
MLCC/+/-10%
PC5110
0.1UF/50V
MLCC/+/-10%
PC5111
4.7UH/16V
MLCC/+80-20%
c1206_h49
PC5112
1UF/16V
MLCC/+80%-20%
PC5113
6800PF/50V
MLCC/+/-10%
PC5116
3300PF/50V
MLCC/+/-10%
@
PC5117
3300PF/50V
MLCC/+/-10%
@
PC5118
270PF/50V
MLCC/+/-10%
PC5119
270PF/50V
MLCC/+/-10%
PCE5100
100UF/6.3V
PANASONIC/EEFCX0J101R
c7343d_h87
PCE5101
27UF/25V
PCE5102
100UF/6.3V
PANASONIC/EEFCX0J101R
c7343d_h87
@
PCE5103
27UF/25V
PCE5104
150UF/4V
PANASONIC/EEFCX0G151R
c7343d_h87
PCE5105
150UF/4V
PANASONIC/EEFCX0G151R
c7343d_h87
@
PD5100
FS1J4TP
PD5102
FS1J4TP
PJP5100
1MM_OPEN_5MIL
PJP5101
1MM_OPEN_5MIL
PJP5104
SHORT PIN
PJP5103
SHORT PIN
PL5100
3.8UH
Irat=6A
PL5101
3.8UH
Irat=6A
PQ5100
SI4800BDY
PQ5101
SI4800BDY
PQ5102
SI4800BDY
PQ5103
SI4800BDY
PT5100
TPC28T
PT5101
TPC28T
PT5102
TPC28T
PT5120
TPC28T
PT5121
TPC28T
+5VO
(6A)
+5VSUS
(0.5A)
+3VO
(3A)
+3VSUS
(0.4A)
+5VAO
+5VO
ENBL
3V_5V_PWRGD
40,60 3V_5V_PWRGD
2,53,54,61,63 SUSB#_PWR
TPC28TPT5103PT5104PT5105PT5106
TPC28TPT5107PT5108PT5109
TPC28TPT5113PT5114PT5115PT5116
TPC28TPT5117PT5118PT5119
PCMCIA
ASUSALPHATeK COMPUTER INC.
Title : POWER_SYSTEM
Engineer: Amos Yu
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
Sheet 51 of 57



PCMCIA

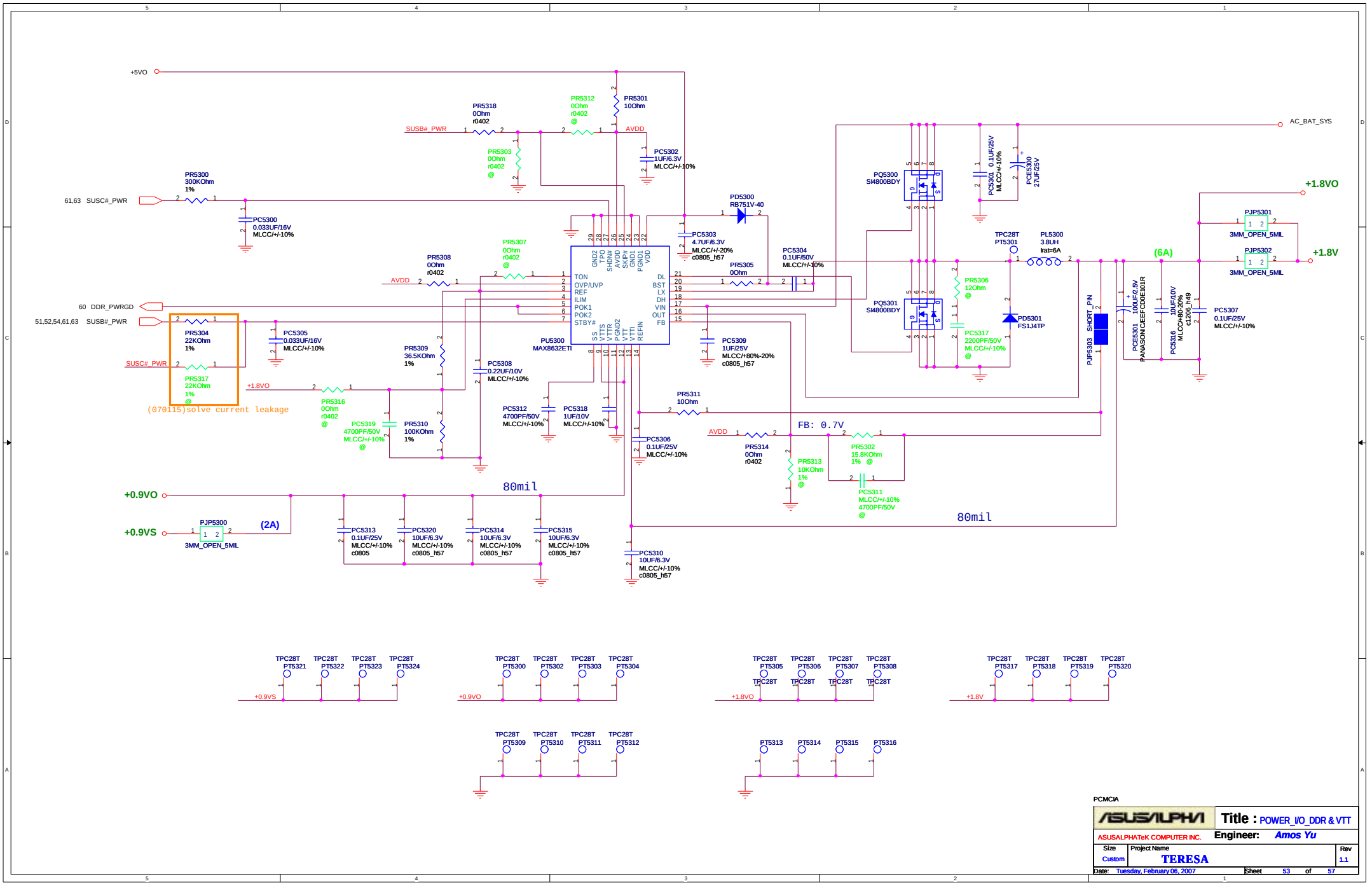
ASUSALPHA

Title : POWER_I/O_1.5VS & 1.05VS

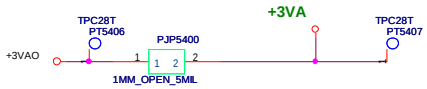
ASUSALPHATeK COMPUTER INC. Engineer: Amos Yu

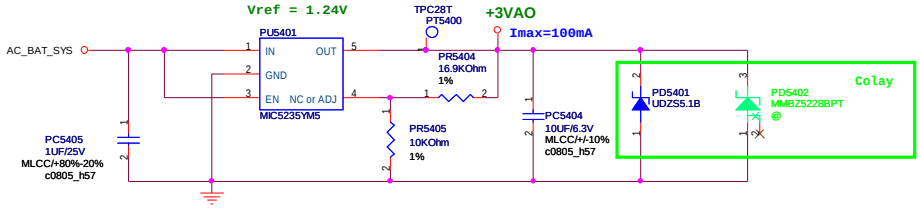
Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 52 of 57

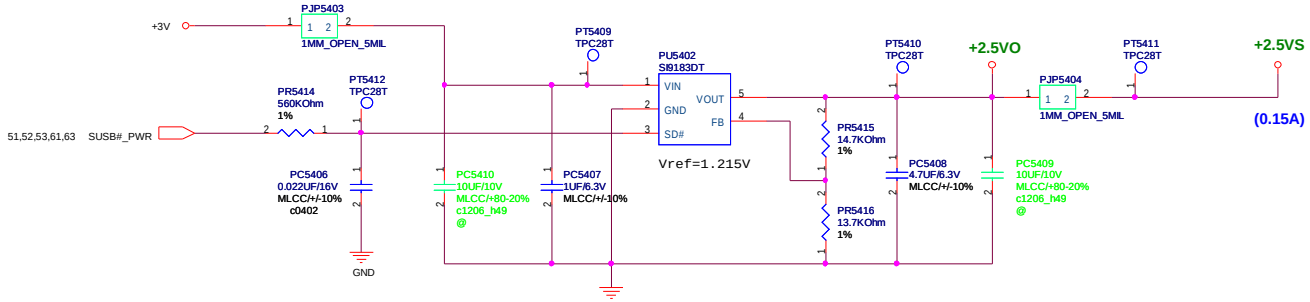

+5VO
PR5318 0Ohm r0402
PR5312 0Ohm r0402 @
PR5301 10Ohm
SUSB#_PWR
AVDD
PR5303 0Ohm r0402 @
PC5302 1UF/6.3V MLCC/+/-10%
AC_BAT_SYS
PR5300 300KOhm 1%
61,63 SUSC#_PWR
PC5300 0.033UF/16V MLCC/+/-10%
PD5300 RB751V-40
PC5303 4.7UF/6.3V MLCC/+/-20% c0805_h57
PQ5300 SI4800BDY
PC5301 0.1UF/25V MLCC/+/-10%
PCE5300 27UF/25V
+1.8VO
PJP5301
3MM_OPEN_5MIL
PJP5302
3MM_OPEN_5MIL
+1.8V
TPC28T PT5301
PL5300 3.8UH Irat=6A
(6A)
PR5307 0Ohm r0402 @
PR5308 0Ohm r0402
PC5304 0.1UF/50V MLCC/+/-10%
PR5305 0Ohm
PR5306 12Ohm @
PQ5301 SI4800BDY
PC5317 2200PF/50V MLCC/+/-10% @
PD5301 FS1J4TP
PJP5303 SHORT_PIN
PCE5301 100UF/2.5V PANASONICEEFCD0E101R
PC5316 10UF/10V MLCC/+80-20% c1206_h49
PC5307 0.1UF/25V MLCC/+/-10%
60 DDR_PWRGD
51,52,54,61,63 SUSB#_PWR
PR5304 22KOhm 1%
PC5305 0.033UF/16V MLCC/+/-10%
SUSC# PWR
PR5317 22KOhm 1% @
(070115)solve current leakage
+1.8VO
PR5316 0Ohm r0402 @
PC5319 4700PF/50V MLCC/+/-10% @
PR5309 36.5KOhm 1%
PR5310 100KOhm 1%
PC5308 0.22UF/10V MLCC/+/-10%
PU5300 MAX8632ETI
PC5309 1UF/25V MLCC/+80%-20% c0805_h57
PC5312 4700PF/50V MLCC/+/-10%
PC5318 1UF/10V MLCC/+/-10%
PR5311 10Ohm
PC5306 0.1UF/25V MLCC/+/-10%
AVDD
PR5314 0Ohm r0402
FB: 0.7V
PR5313 10KOhm 1% @
PR5302 15.8KOhm 1% @
PC5311 MLCC/+/-10% 4700PF/50V @
80mil
80mil
+0.9VO
+0.9VS
PJP5300
(2A)
3MM_OPEN_5MIL
PC5313 0.1UF/25V MLCC/+/-10% c0805
PC5320 10UF/6.3V MLCC/+/-10% c0805_h57
PC5314 10UF/6.3V MLCC/+/-10% c0805_h57
PC5315 10UF/6.3V MLCC/+/-10% c0805_h57
PC5310 10UF/6.3V MLCC/+/-10% c0805_h57
TPC28T PT5321
TPC28T PT5322
TPC28T PT5323
TPC28T PT5324
+0.9VS
TPC28T PT5300
TPC28T PT5302
TPC28T PT5303
TPC28T PT5304
+0.9VO
TPC28T PT5305
TPC28T PT5306
TPC28T PT5307
TPC28T PT5308
+1.8VO
TPC28T PT5317
TPC28T PT5318
TPC28T PT5319
TPC28T PT5320
+1.8V
TPC28T PT5309
TPC28T PT5310
TPC28T PT5311
TPC28T PT5312
PT5313
PT5314
PT5315
PT5316
PCMCIA
Title : POWER_I/O_DDR & VTT
ASUSALPHATeK COMPUTER INC.
Engineer: Amos Yu
Size Custom
Project Name TERESA
Rev 1.1
Date: Tuesday, February 06, 2007
Sheet 53 of 57

+3VA0

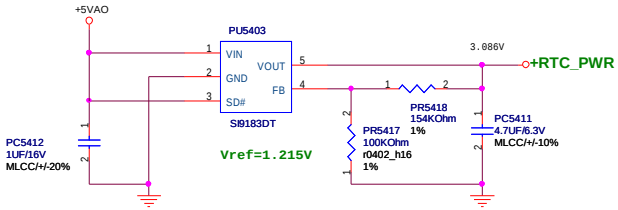




+2.5VS



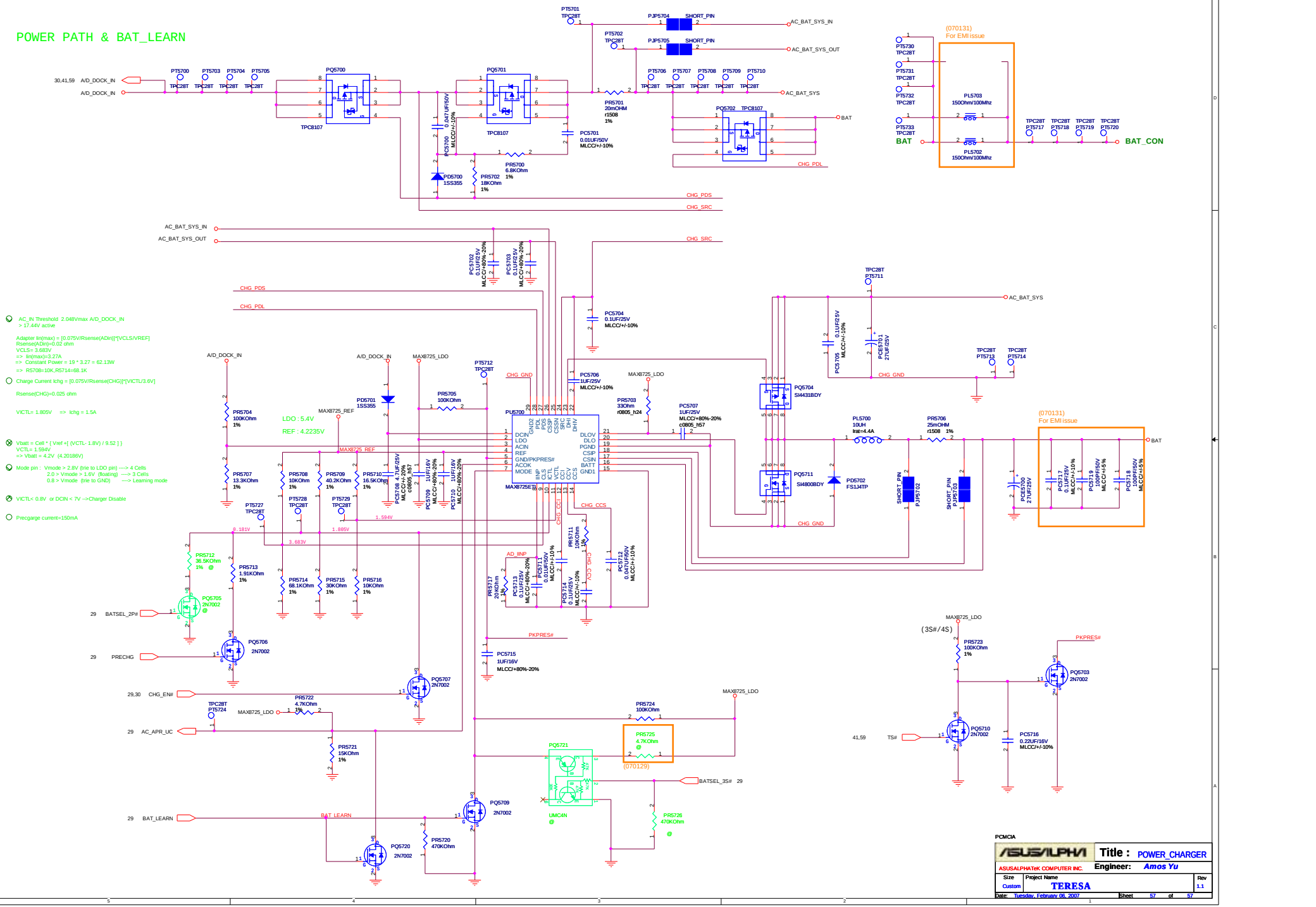
+RTC_PWR



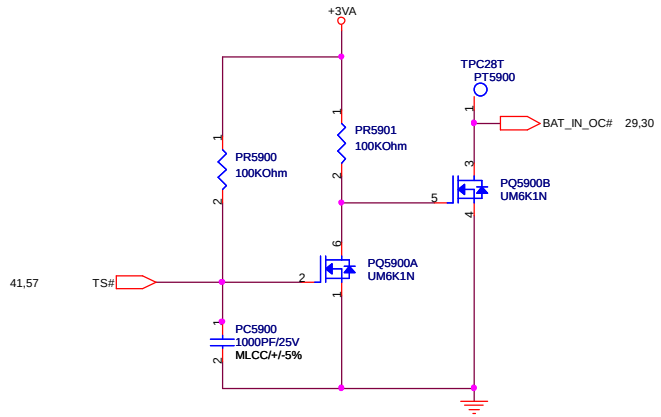
PCMCIA

ASUSALPHA	Title : POWER_I/O_+3VA & +2.5V	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 54 of 57	

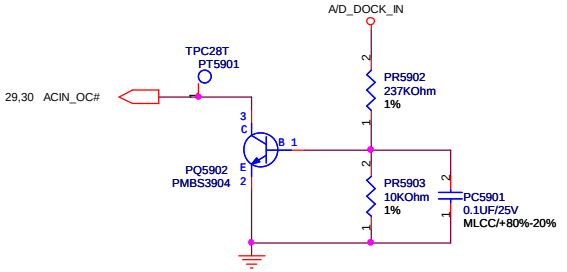
POWER PATH & BAT_LEARN



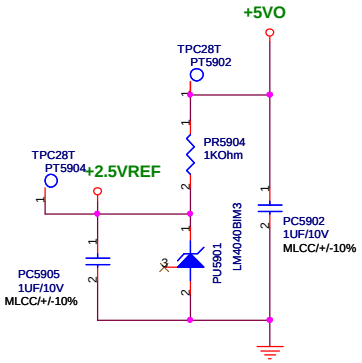
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



PCMCIA

ASUSALPHA

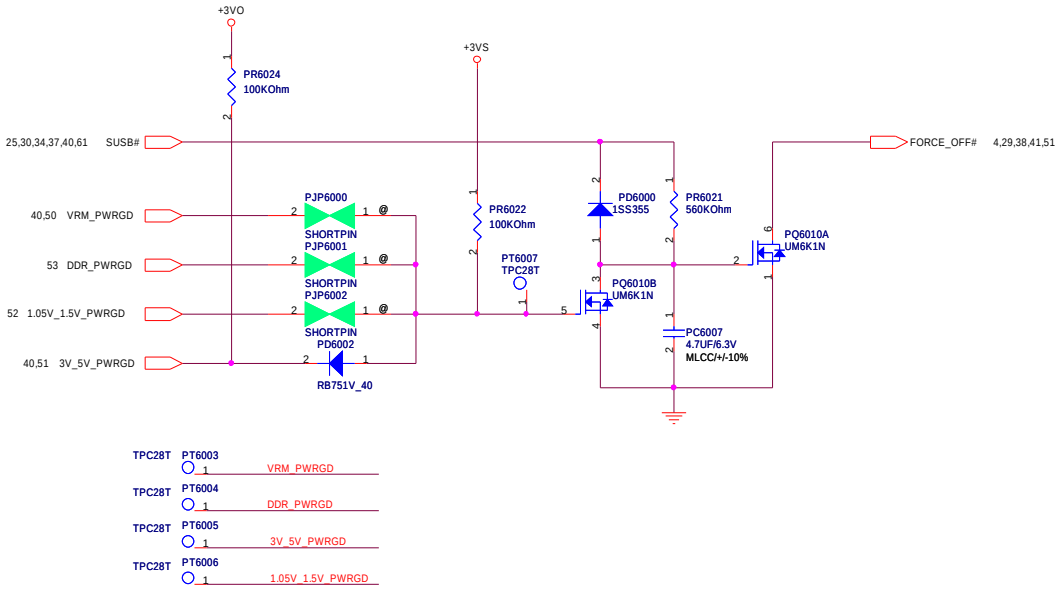
Title : POWER_DETECT

ASUSALPHATeK COMPUTER INC. Engineer: Amos Yu

Size	Project Name	Rev
Custom	TERESA	1.1

Date: Tuesday, February 06, 2007 Sheet 59 of 57

POWER GOOD DETECTER



TPC28T PT6003 — VRM_PWRGD

TPC28T PT6004 — DDR_PWRGD

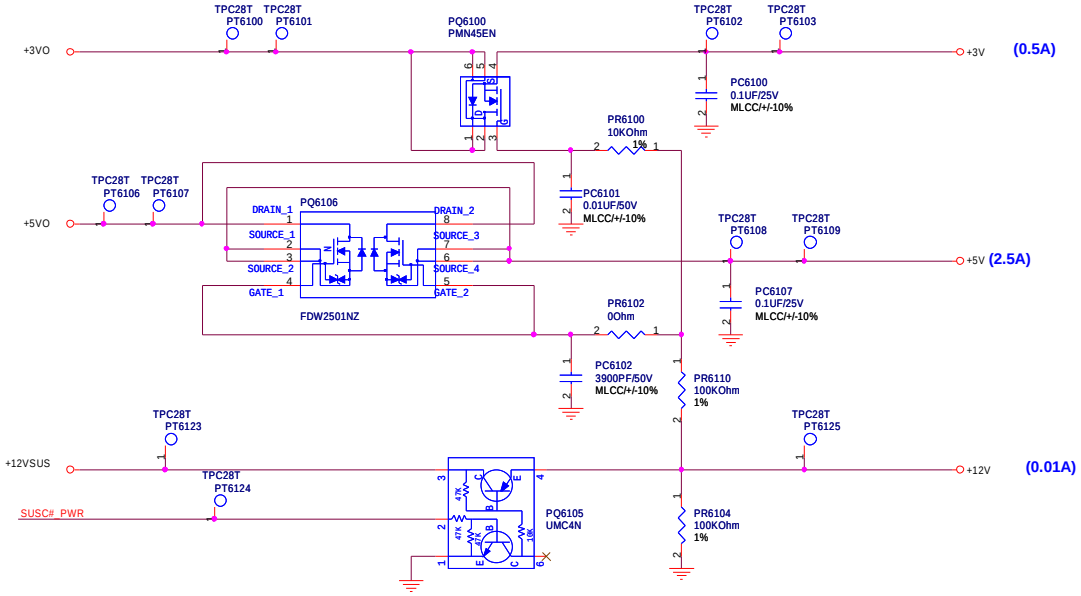
TPC28T PT6005 — 3V_5V_PWRGD

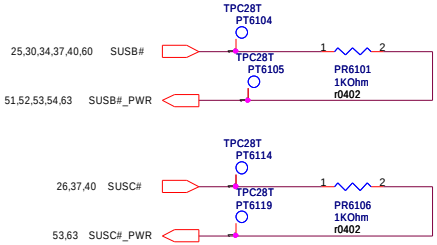
TPC28T PT6006 — 1.05V_1.5V_PWRGD

PCMCIA

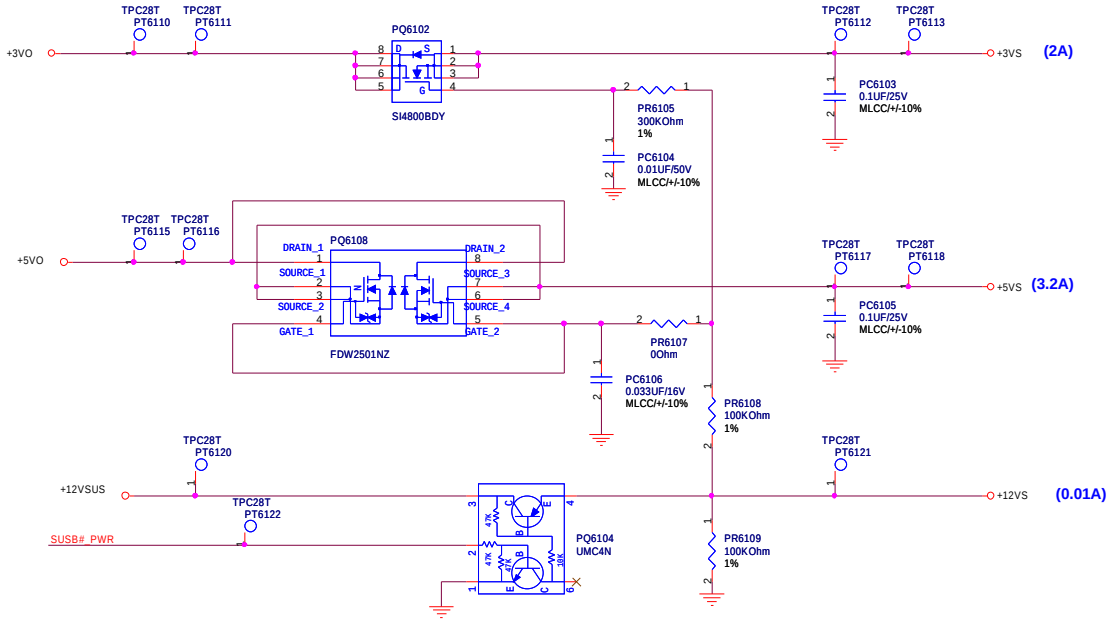
ASUSALPHA	Title : POWER_PROTECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
Date: Tuesday, February 06, 2007	Sheet 60 of 57	

SUSC#_PWR POWER





SUSB#_PWR POWER



PCMCIA

ASUSALPHA

Title : POWER_LOAD SWITCH

ASUSALPHATeK COMPUTER INC. Engineer: Amos Yu

Size	Project Name	Rev
Custom	TERESA	1.1

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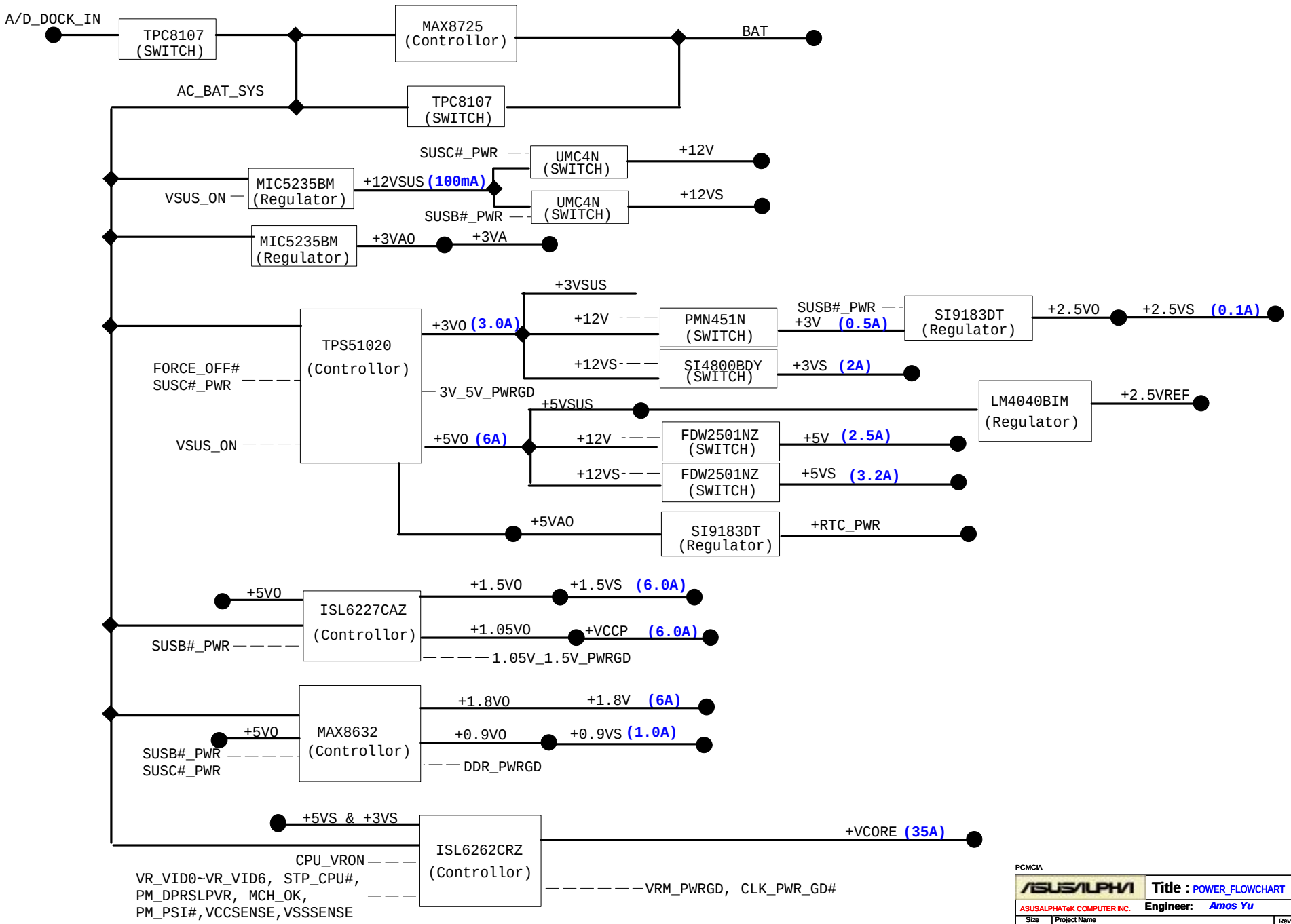

PCMCIA

ASUSALPHA

Title : POWER_FLOWCHART

ASUSALPHATeK COMPUTER INC.

Engineer: Amos Yu

Size	Project Name	Rev
Custom	TERESA	1.1

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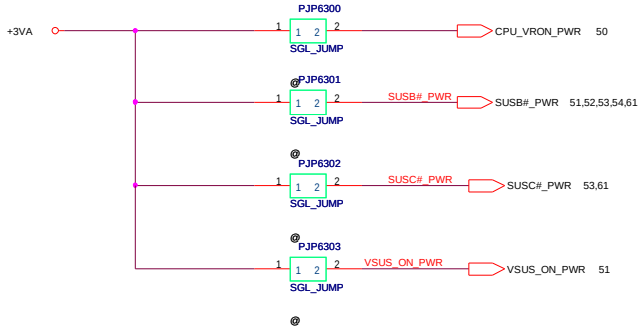
FOR POWER TEST



PCMCIA

ASUSALPHA	Title : POWER_SIGNAL	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos Yu	
Size: Custom	Project Name: TERESA	Rev: 1.1
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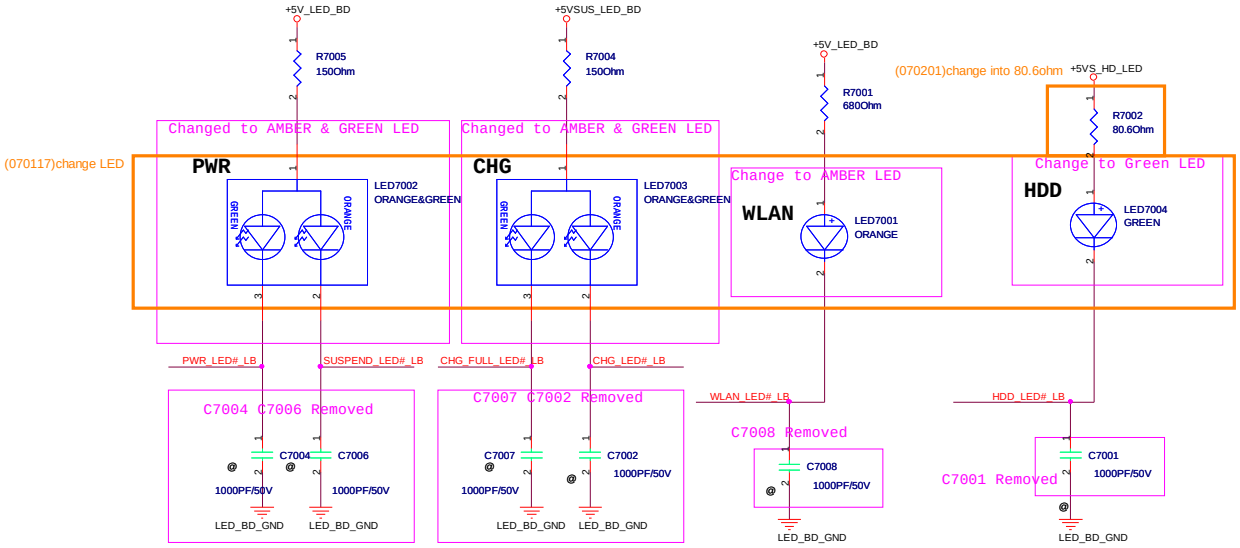
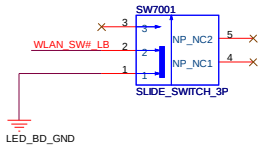
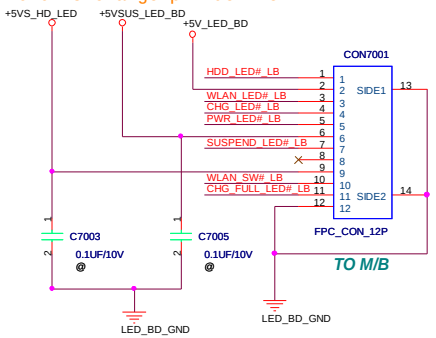
LEFT & RIGHT Button remove to TP BOARD



New added SW for Teresa

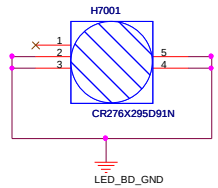


070115 Change pin define

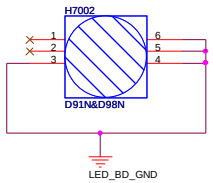


CON to T/P remove to TP BOARD

IR receive module removed



DETAIL: Q



DETAIL: S

PCMCIA

ASUSALPHA	Title : LED Board	
ASUSALPHATeK COMPUTER INC.	Engineer: Potter_Huang	
Size: Custom	Project Name: TERESA	Rev: 1.1
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TERESA SCHEMATIC V1.0

PCMCIA

ASUSALPHA

Title : Content & History

ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA	1.1

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