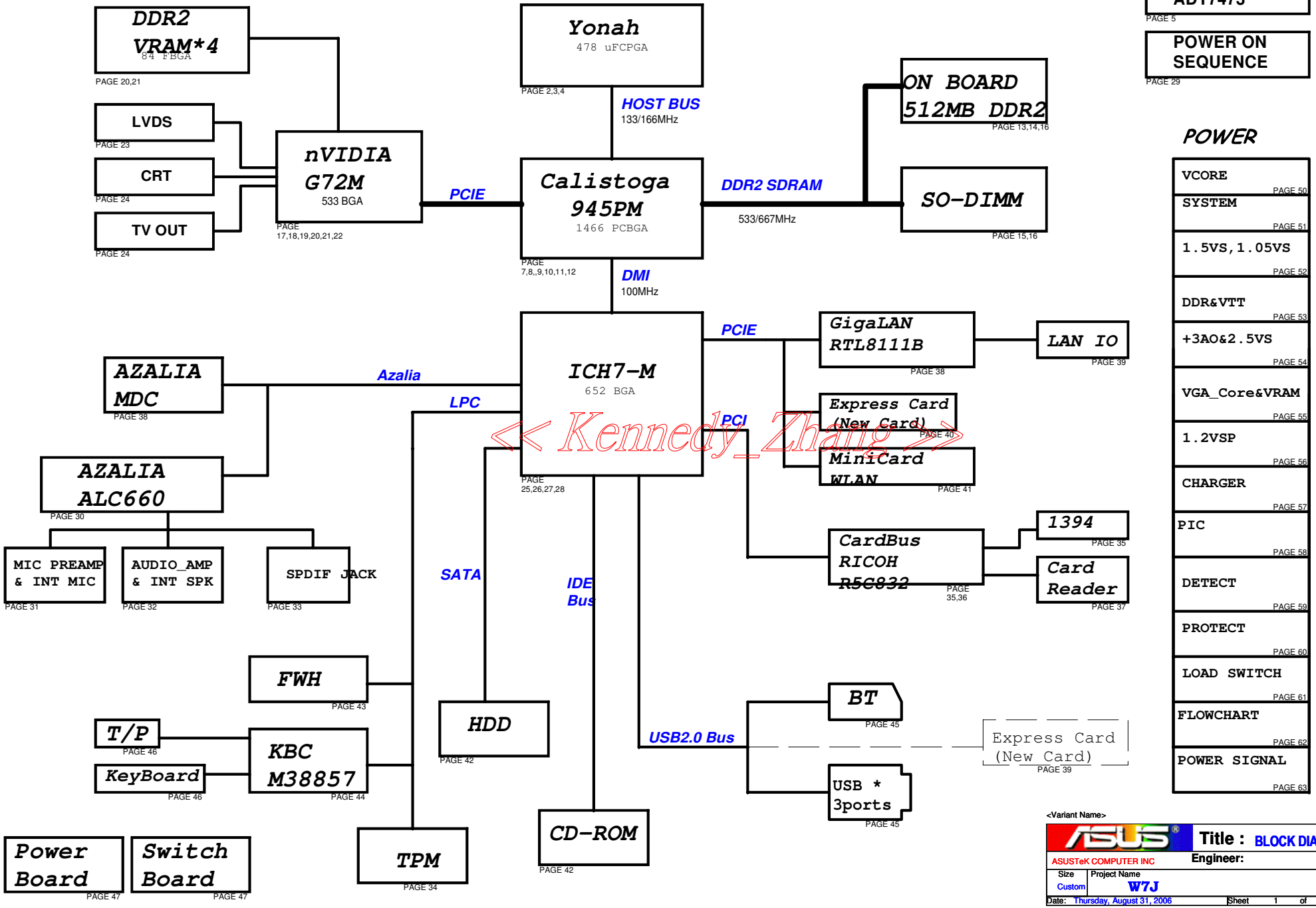
T76J: YONAH/CALISTOGA-PM/G72M BLOCK DIAGRAM



<Variant Name>

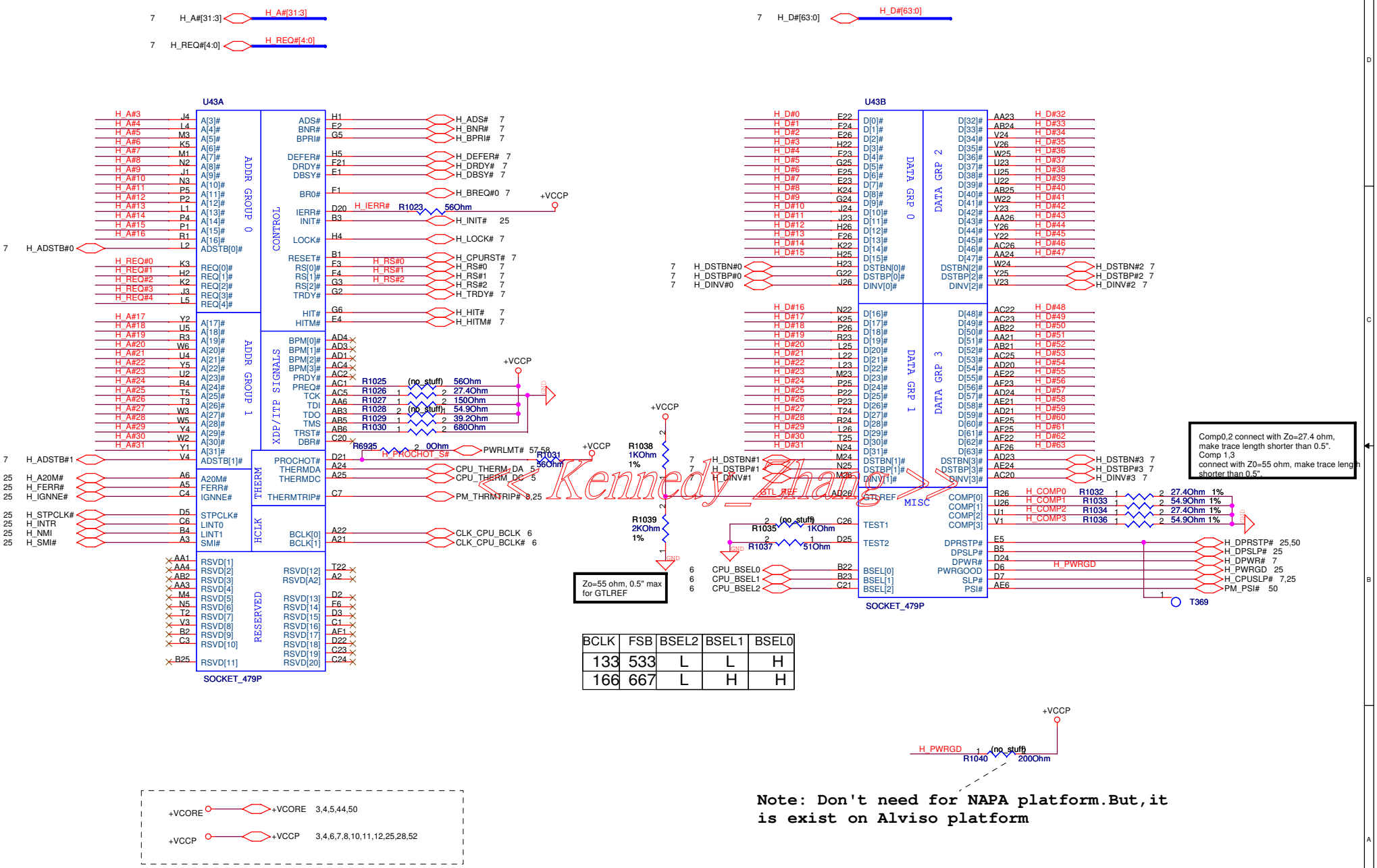
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 1 of 64



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Note: Don't need for NAPA platform.But,it is exist on Alviso platform

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

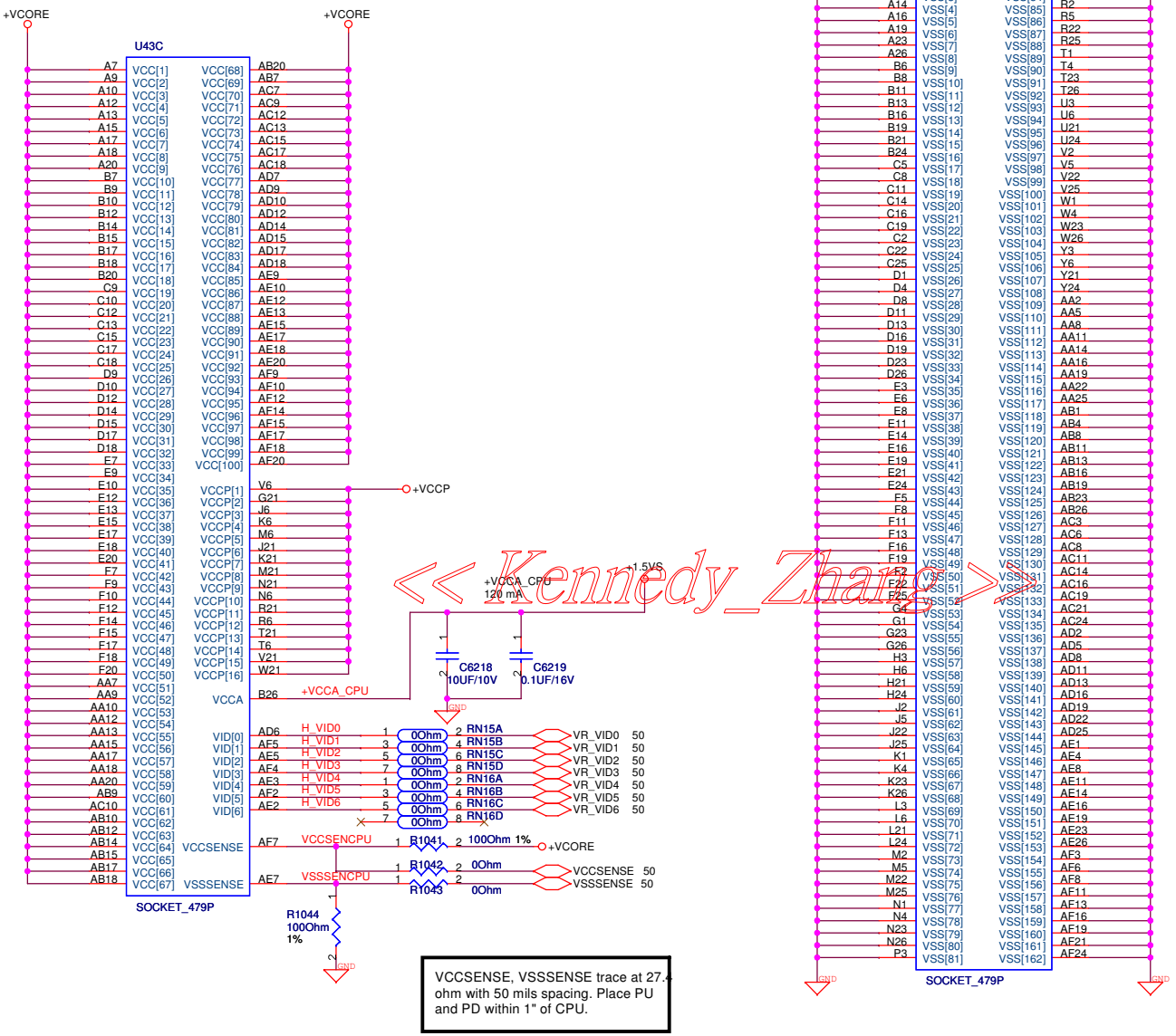
Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 2 of 64

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



<< Kennedy_Zhang >>

VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

<Variant Name>

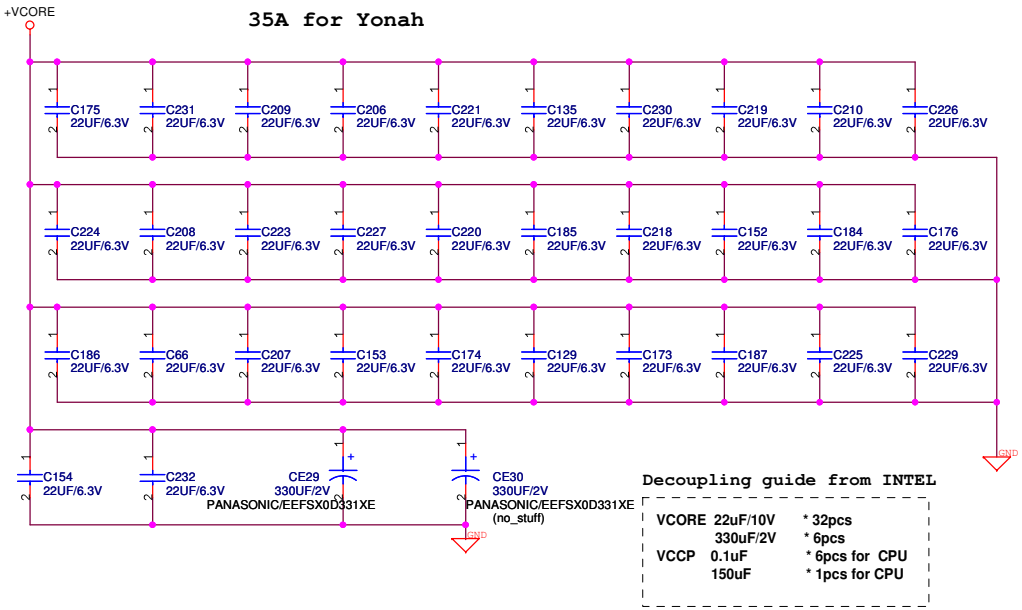
ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

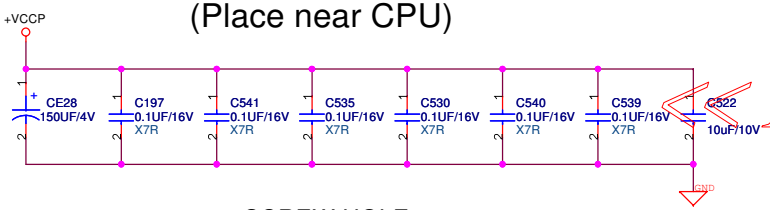
Date: Thursday, August 31, 2006 Sheet 3 of 64



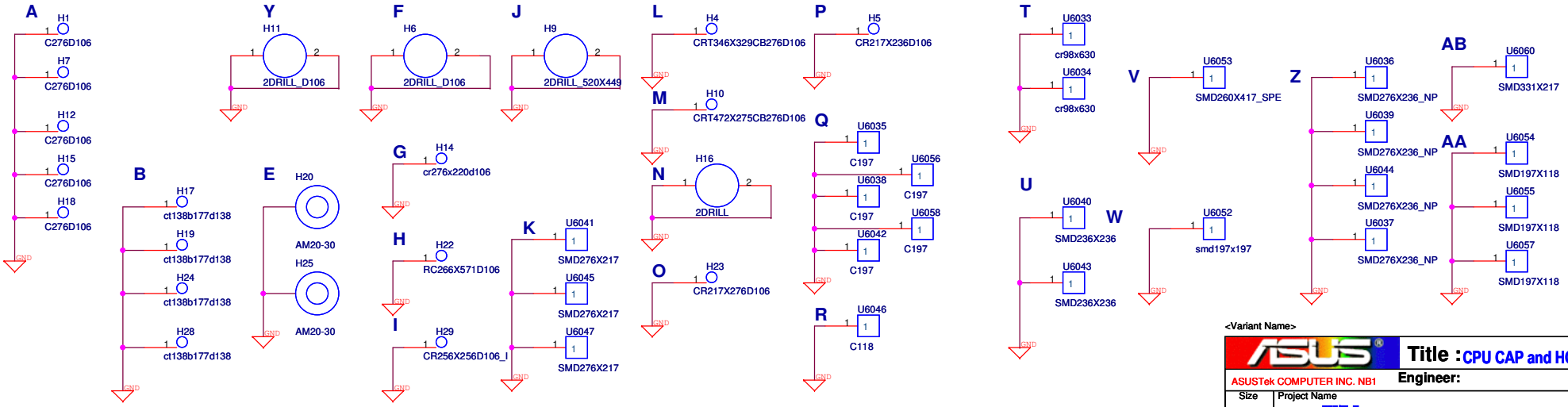
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



SCREW HOLE



<Variant Name>

ASUSTek COMPUTER INC. NB1

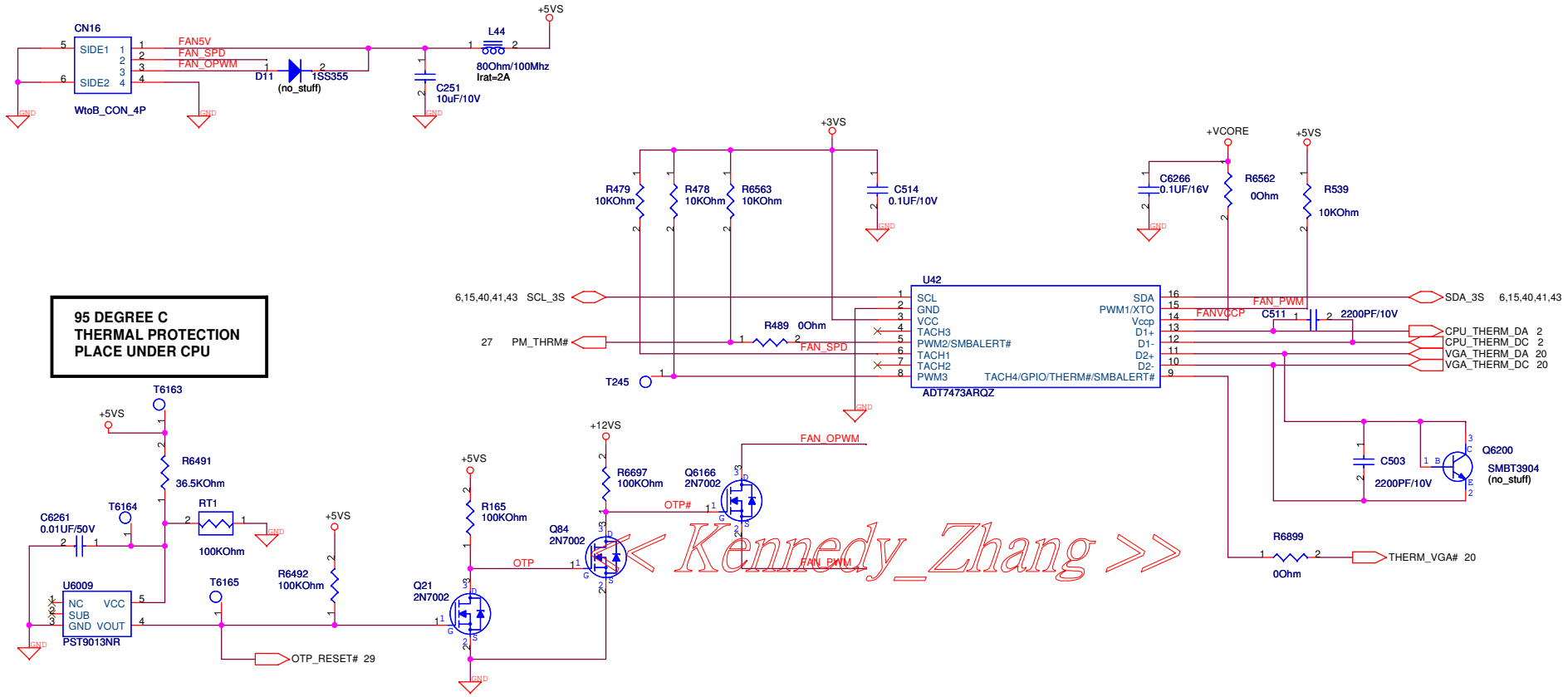
Title : CPU CAP and HOLES

Engineer:

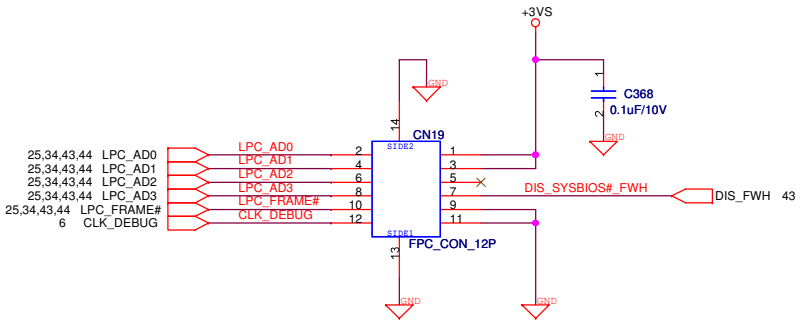
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 4 of 64

FAN & THERMAL CONTROLLER



LPC DEBUG PORT



<Variant Name>

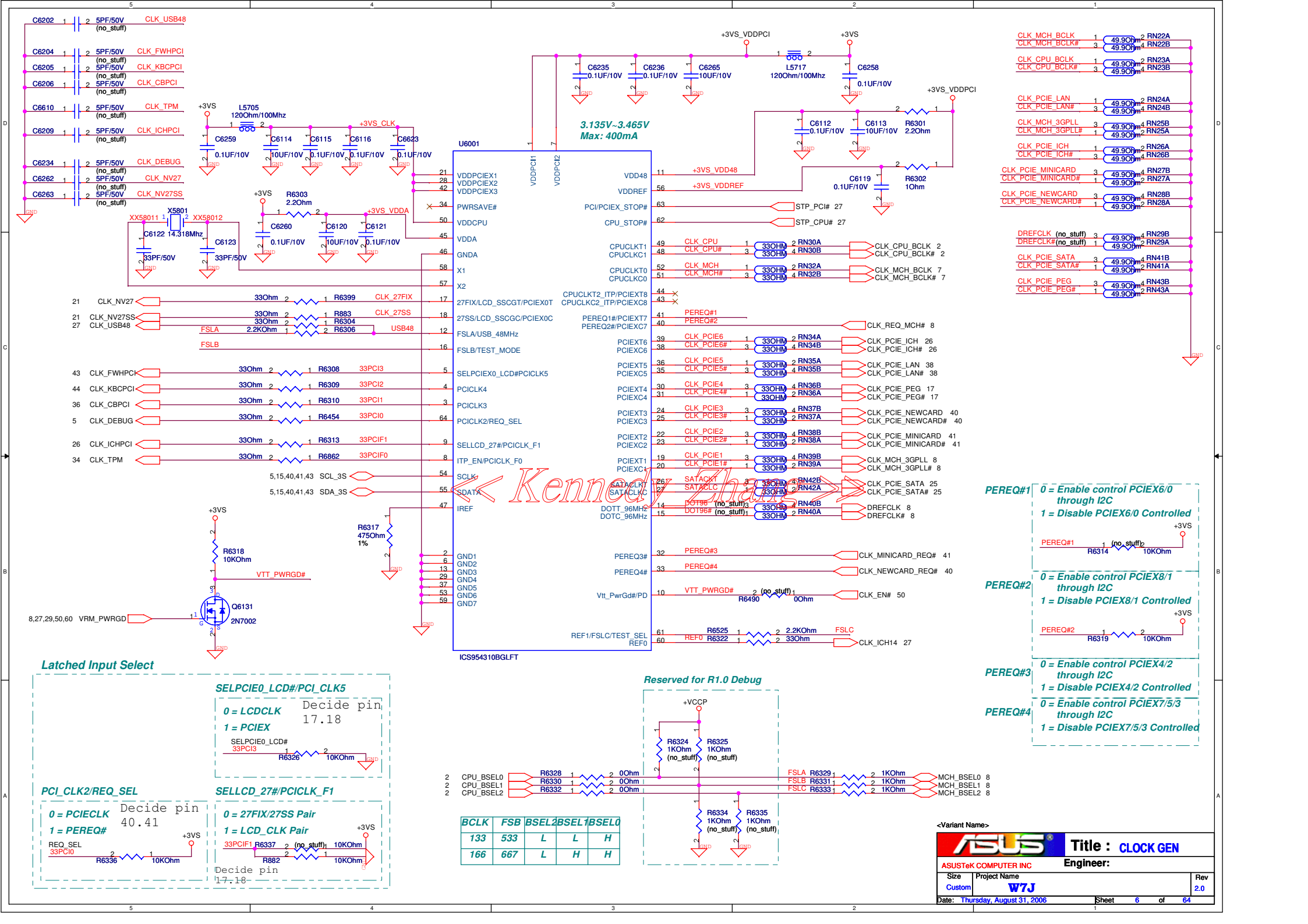
ASUSTeK COMPUTER INC

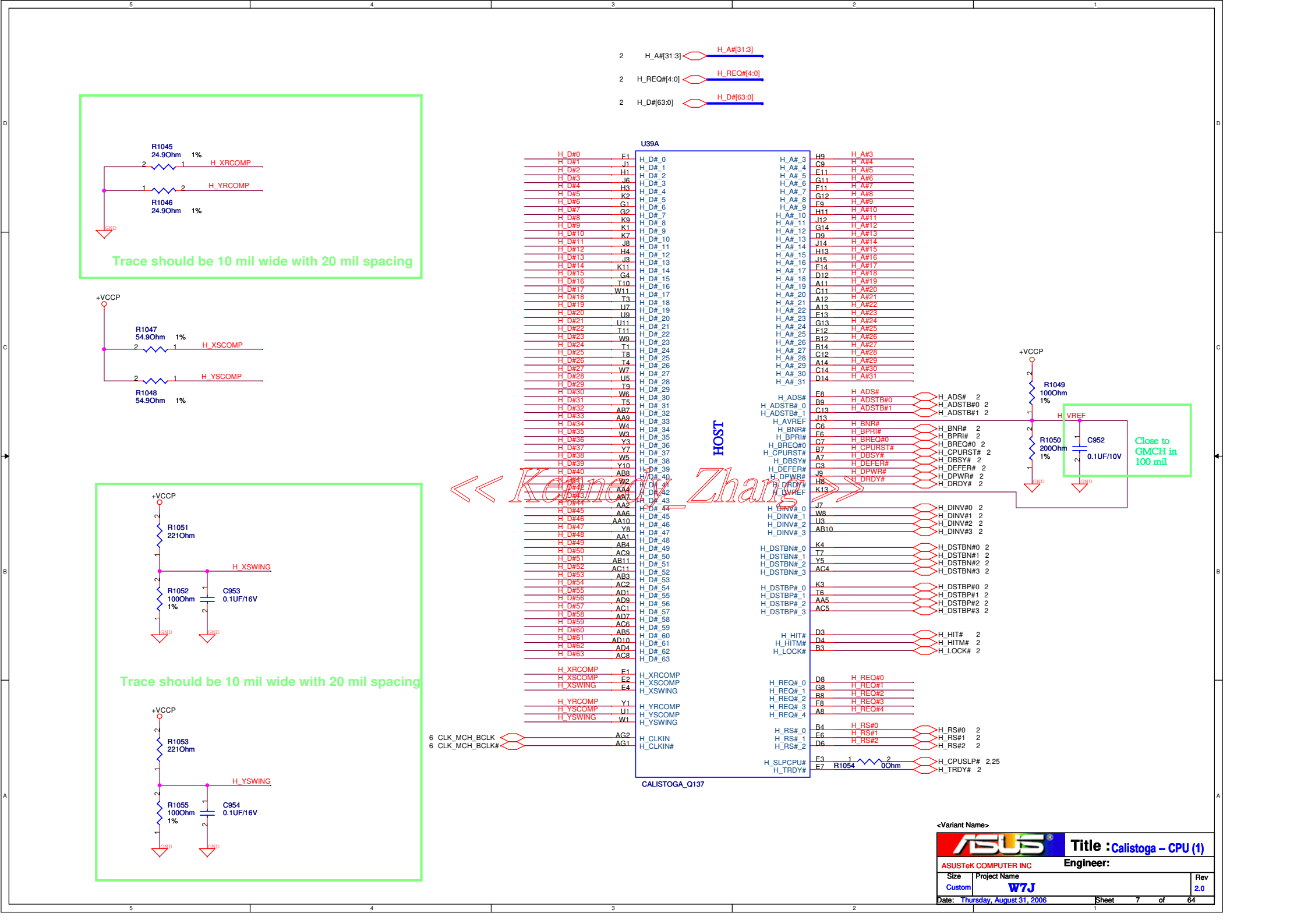
Title : FAN & debug port

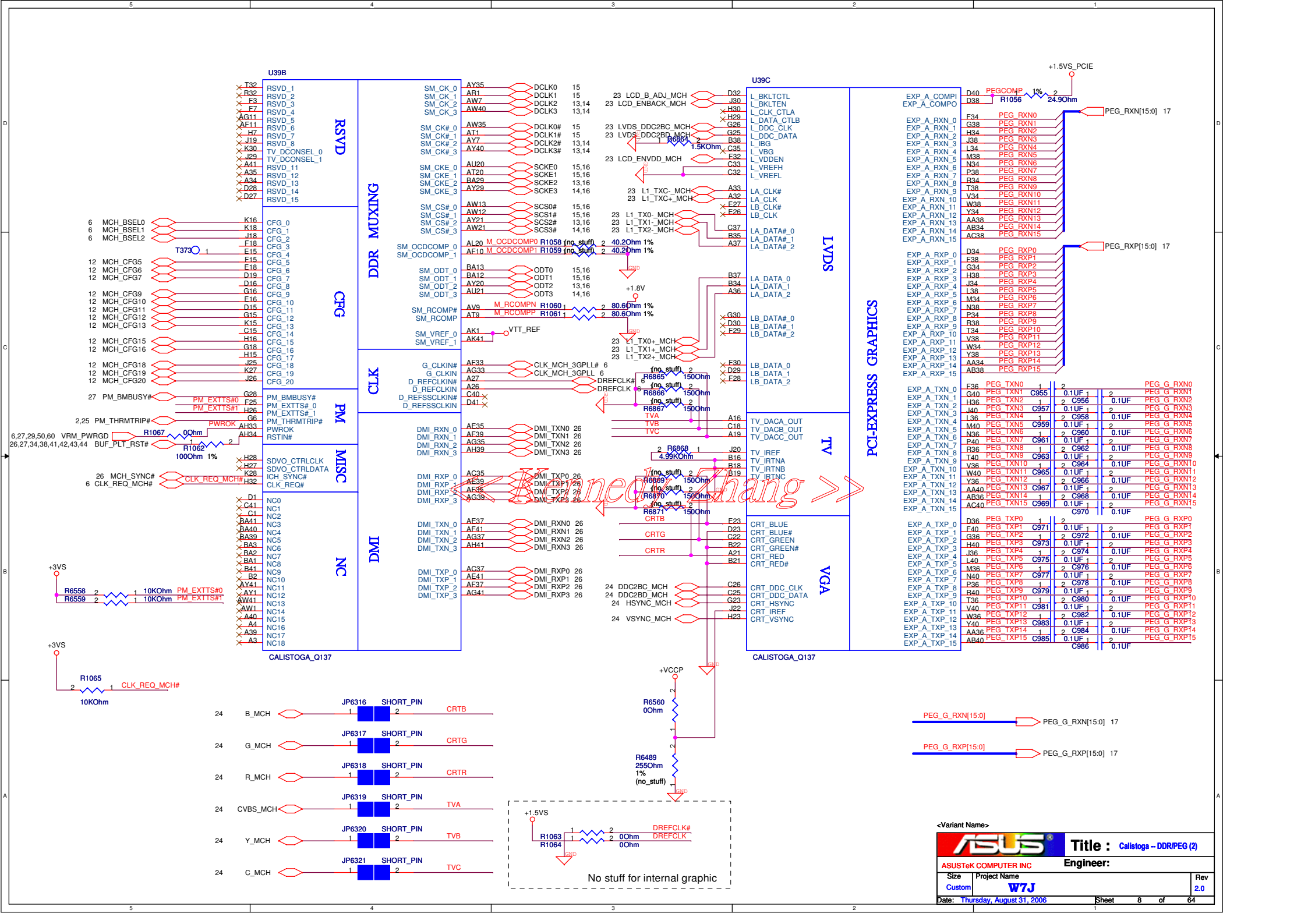
Engineer:

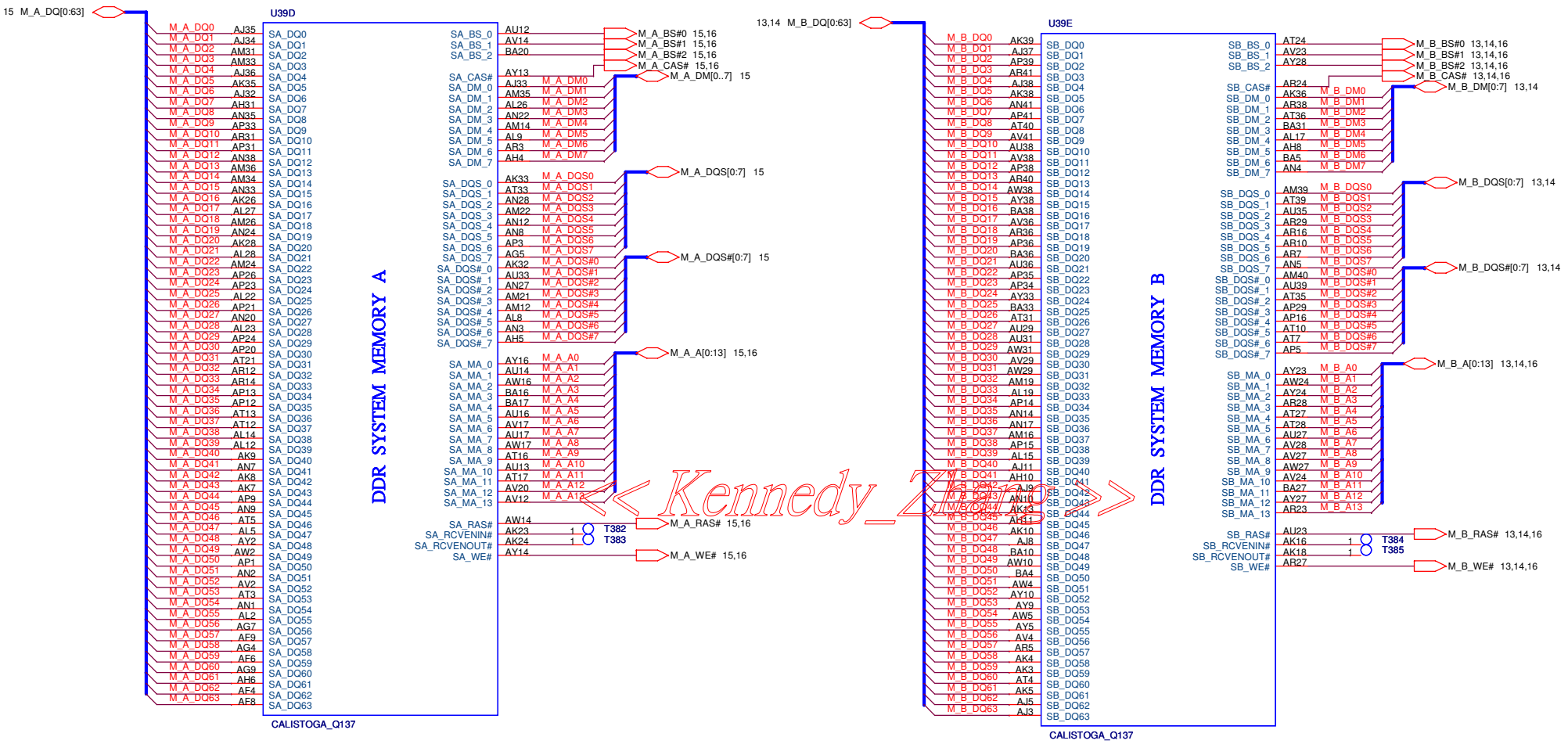
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 5 of 64


U6001
ICS954310BGLFT
3.135V~3.465V
Max: 400mA
Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
PCI_CLK2/REQ_SEL
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27#/PCICLK_F1
0 = 27FIX/27SS Pair
1 = LCD_CLK Pair
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#1
0 = Enable control PCIEX6/0 through I2C
1 = Disable PCIEX6/0 Controlled
PEREQ#2
0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer:
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 6 of 64


R1045
24.9Ohm 1%
H_XRCOMP
H_YRCOMP
R1046
24.9Ohm 1%
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1047
54.9Ohm 1%
H_XSCOMP
H_YSCOMP
R1048
54.9Ohm 1%
+VCCP
R1051
221Ohm
H_XSWING
R1052
100Ohm
1%
C953
0.1UF/16V
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1053
221Ohm
H_YSWING
R1055
100Ohm
1%
C954
0.1UF/16V
2 H_A#[31:3]
H_A#[31:3]
2 H_REQ#[4:0]
H_REQ#[4:0]
2 H_D#[63:0]
H_D#[63:0]
U39A
HOST
CALISTOGA_Q137
6 CLK_MCH_BCLK
6 CLK_MCH_BCLK#
H_CLKIN
H_CLKIN#
H_XRCOMP
H_XSCOMP
H_XSWING
H_YRCOMP
H_YSCOMP
H_YSWING
H_ADS#
H_ADSTB#0
H_ADSTB#1
H_AVREF
H_BNR#
H_BPRI#
H_BREQ#0
H_CPURST#
H_DBSY#
H_DEFER#
H_DPWR#
H_DRDY#
H_DVREF
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_HIT#
H_HITM#
H_LOCK#
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_RS#0
H_RS#1
H_RS#2
H_SLPCPU#
H_TRDY#
R1054
0Ohm
H_CPUSLP# 2,25
H_TRDY# 2
+VCCP
R1049
100Ohm
1%
H_VREF
R1050
200Ohm
1%
C952
0.1UF/10V
Close to GMCH in 100 mil
GND
<< Kennedy Zhang >>
<Variant Name>
Title : Calistoga – CPU (1)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 7 of 64


U39B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
CALISTOGA_Q137
U39C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
No stuff for internal graphic
<Variant Name>
Title : Calistoga -- DDR/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 8 of 64



<Variant Name>

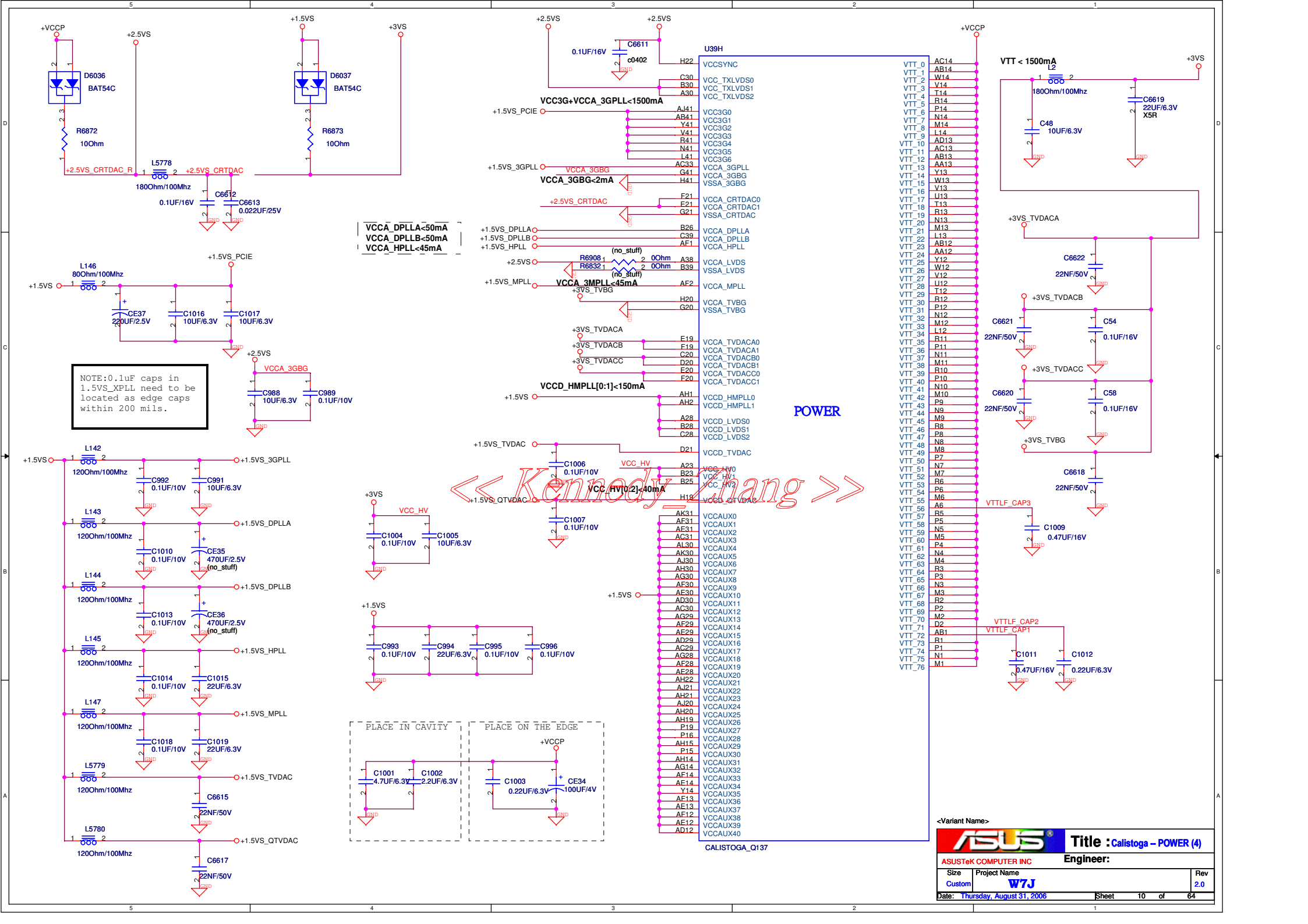
ASUSTeK COMPUTER INC

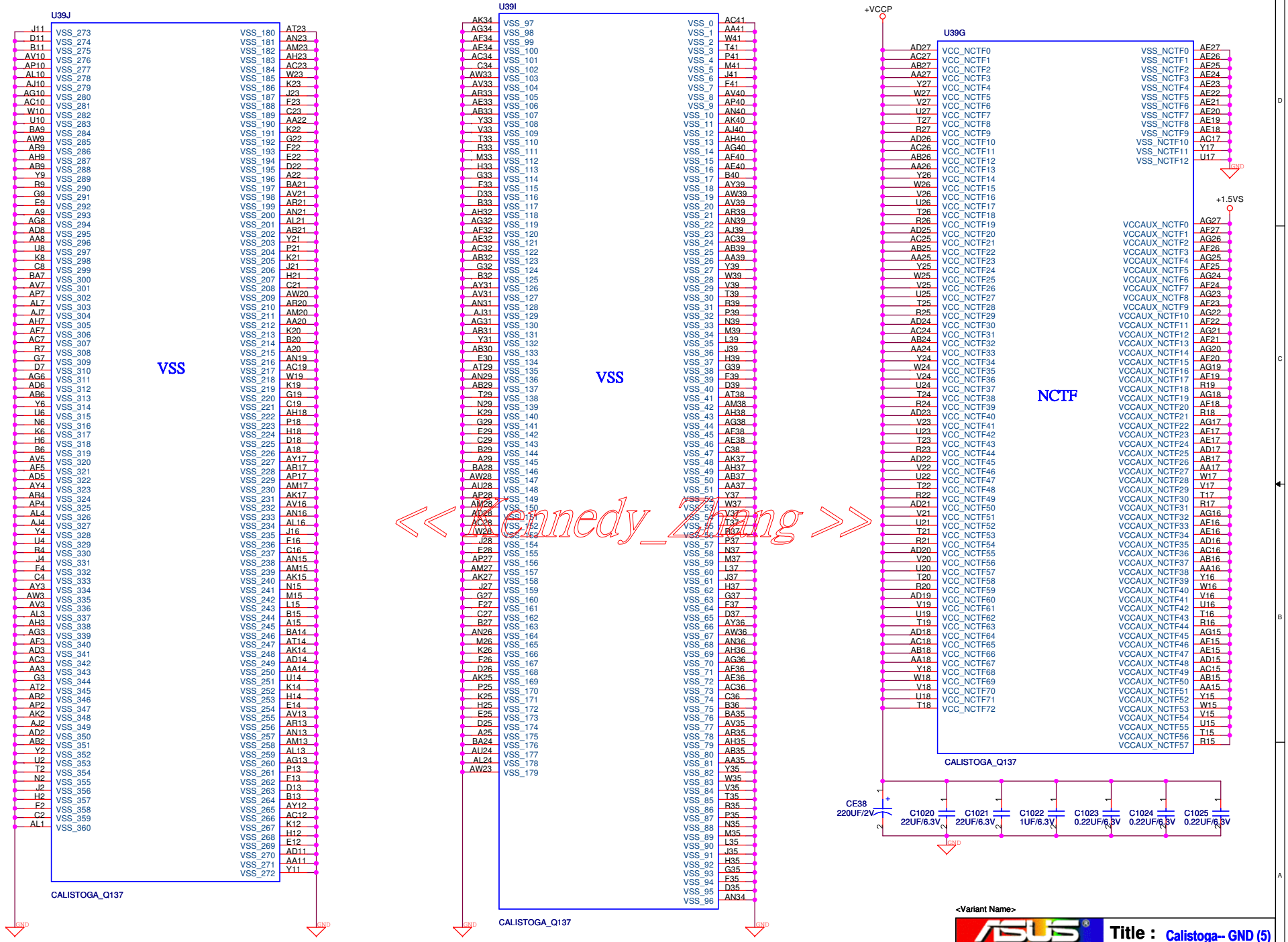
Title : Calistoga – DDR bus (3)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 9 of 64





<Variant Name>

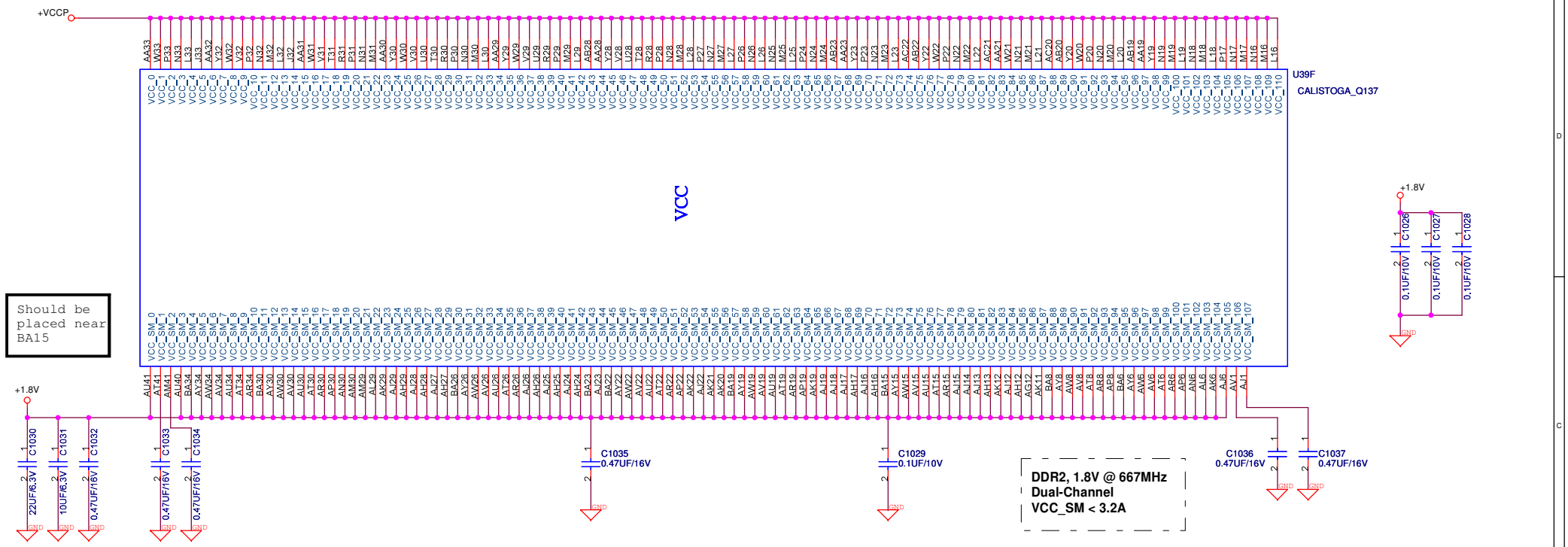
ASUSTeK COMPUTER INC

Title : Calistoga-- GND (5)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 11 of 64



8 MCH_CFG5 — R1069 2.2KOhm (no_stuff) — GND

CFG5 : DMI STRAP
LOW = DMI X 2
HIGH = DMI X 4 (Default)

8 MCH_CFG9 — R1077 2.2KOhm — GND

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

8 MCH_CFG15 — R1078 2.2KOhm (no_stuff) — GND

CFG15 :ICH RESET DISABLE
LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION

8 MCH_CFG12 — R1076 2.2KOhm (no_stuff) — GND
8 MCH_CFG13 — R1072 2.2KOhm (no_stuff) — GND

8 MCH_CFG6 — R6479 2.2KOhm (no_stuff) — GND

CFG6 : DDR STRAP
LOW = Moby Dick
HIGH = Calistoga (Default)

8 MCH_CFG10 — R1070 2.2KOhm (no_stuff) — GND

CFG10: HOST PLL VCO SELECT
LOW = RESERVED
HIGH = MOBILITY

8 MCH_CFG16 — R1071 2.2KOhm (no_stuff) — GND

CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

+3VS — R1079 1KOhm (no_stuff) — 8 MCH_CFG19

8 MCH_CFG7 — R1075 2.2KOhm (no_stuff) — GND

CFG7 : CPU STRAP
LOW = RSVD
HIGH = Mobile CPU (Default)

8 MCH_CFG11 — R1073 2.2KOhm (no_stuff) — GND

CFG11 : PSB 4X CLK ENABLE
LOW = Reserved
HIGH = Calistoga (Default)

CFG18 : GMCH Core Voltage Level
LOW = 1.05V (Default)
HIGH = 1.5V

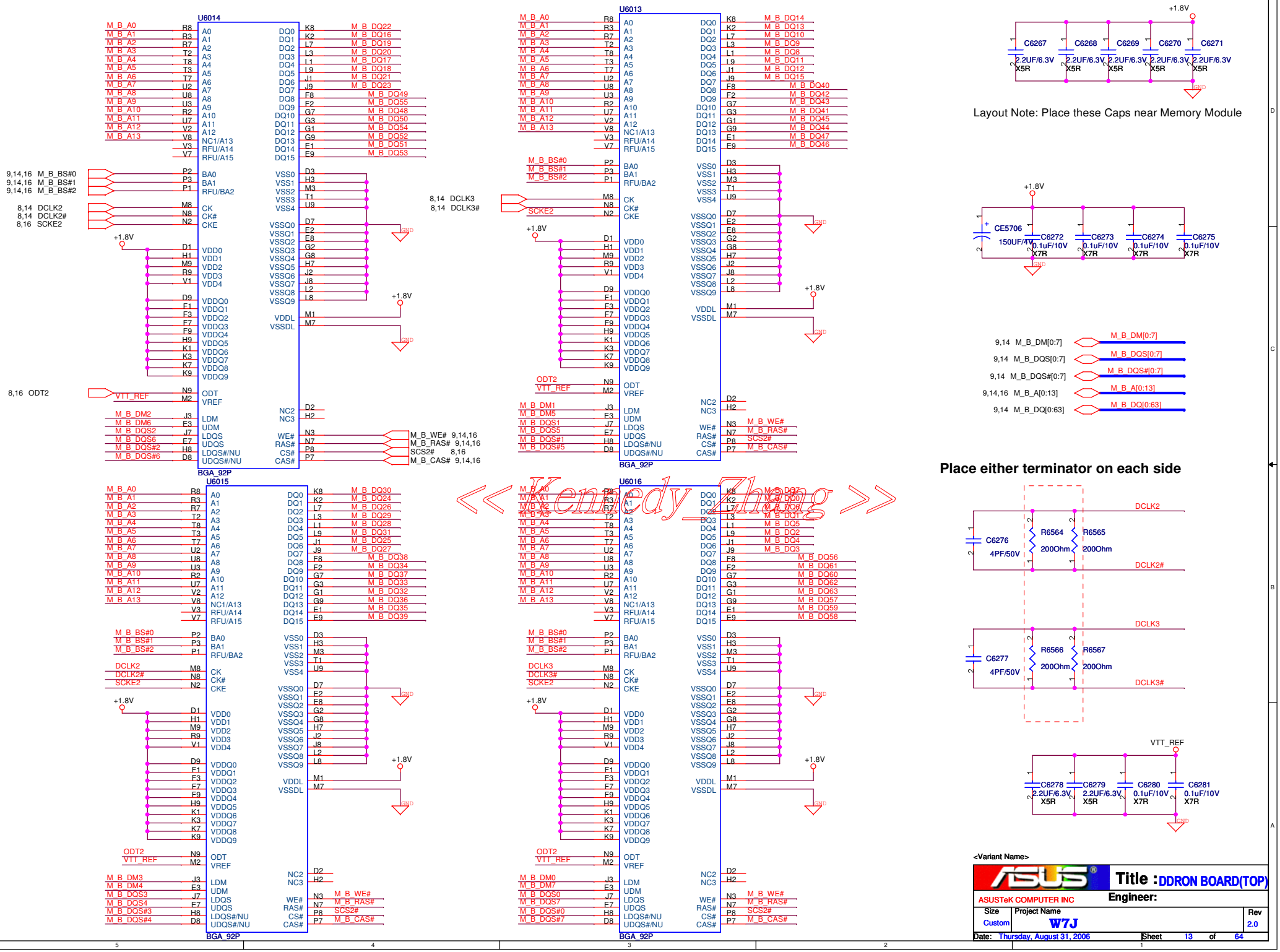
+3VS — R1074 1KOhm (no_stuff) — 8 MCH_CFG18

CFG20 : PCIE Backward Interpoerability mode
LOW = only SDVO or PCIE*1 isoperational (default)
HIGH = SDVO and PCIE*1 are operating simulaneously via the PEG port

+3VS — R6480 1KOhm (no_stuff) — 8 MCH_CFG20

<Variant Name>

ASUSTeK COMPUTER INC	Title : Calistoga-- GND (6)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 12 of 64	


U6014
U6013
U6015
U6016
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_DM2
M_B_DM6
M_B_DQS2
M_B_DQS6
M_B_DQS#2
M_B_DQS#6
M_B_DM3
M_B_DM4
M_B_DQS3
M_B_DQS4
M_B_DQS#3
M_B_DQS#4
M_B_DM1
M_B_DM5
M_B_DQS1
M_B_DQS5
M_B_DQS#1
M_B_DQS#5
M_B_DM0
M_B_DM7
M_B_DQS0
M_B_DQS7
M_B_DQS#0
M_B_DQS#7
M_B_DQ22
M_B_DQ16
M_B_DQ19
M_B_DQ20
M_B_DQ17
M_B_DQ18
M_B_DQ21
M_B_DQ23
M_B_DQ49
M_B_DQ55
M_B_DQ48
M_B_DQ50
M_B_DQ54
M_B_DQ52
M_B_DQ51
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M_B_DQ14
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M_B_DQ40
M_B_DQ42
M_B_DQ43
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M_B_DQ46
M_B_DQ30
M_B_DQ24
M_B_DQ26
M_B_DQ29
M_B_DQ28
M_B_DQ31
M_B_DQ25
M_B_DQ27
M_B_DQ38
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M_B_DQ37
M_B_DQ33
M_B_DQ32
M_B_DQ36
M_B_DQ35
M_B_DQ39
M_B_DQ7
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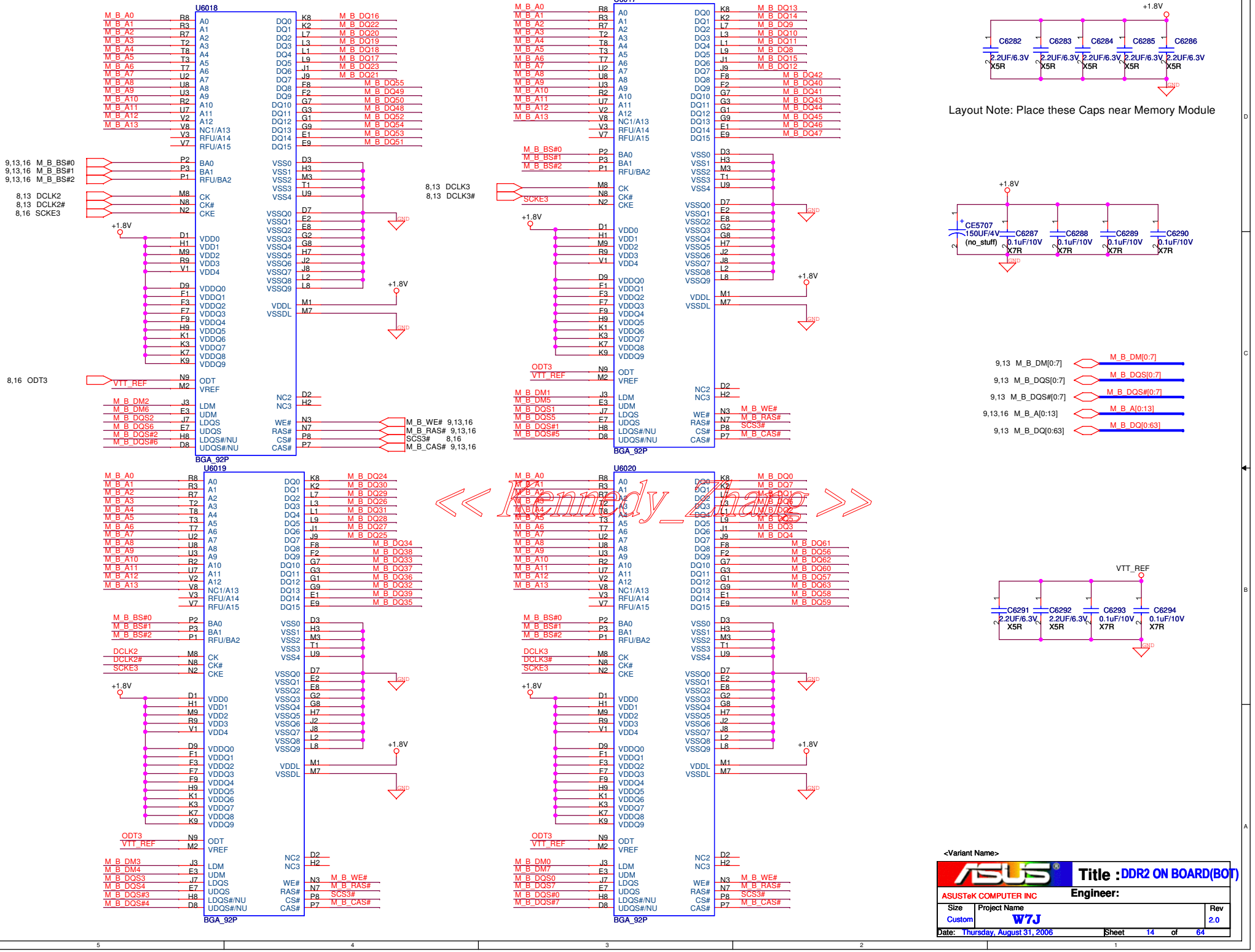
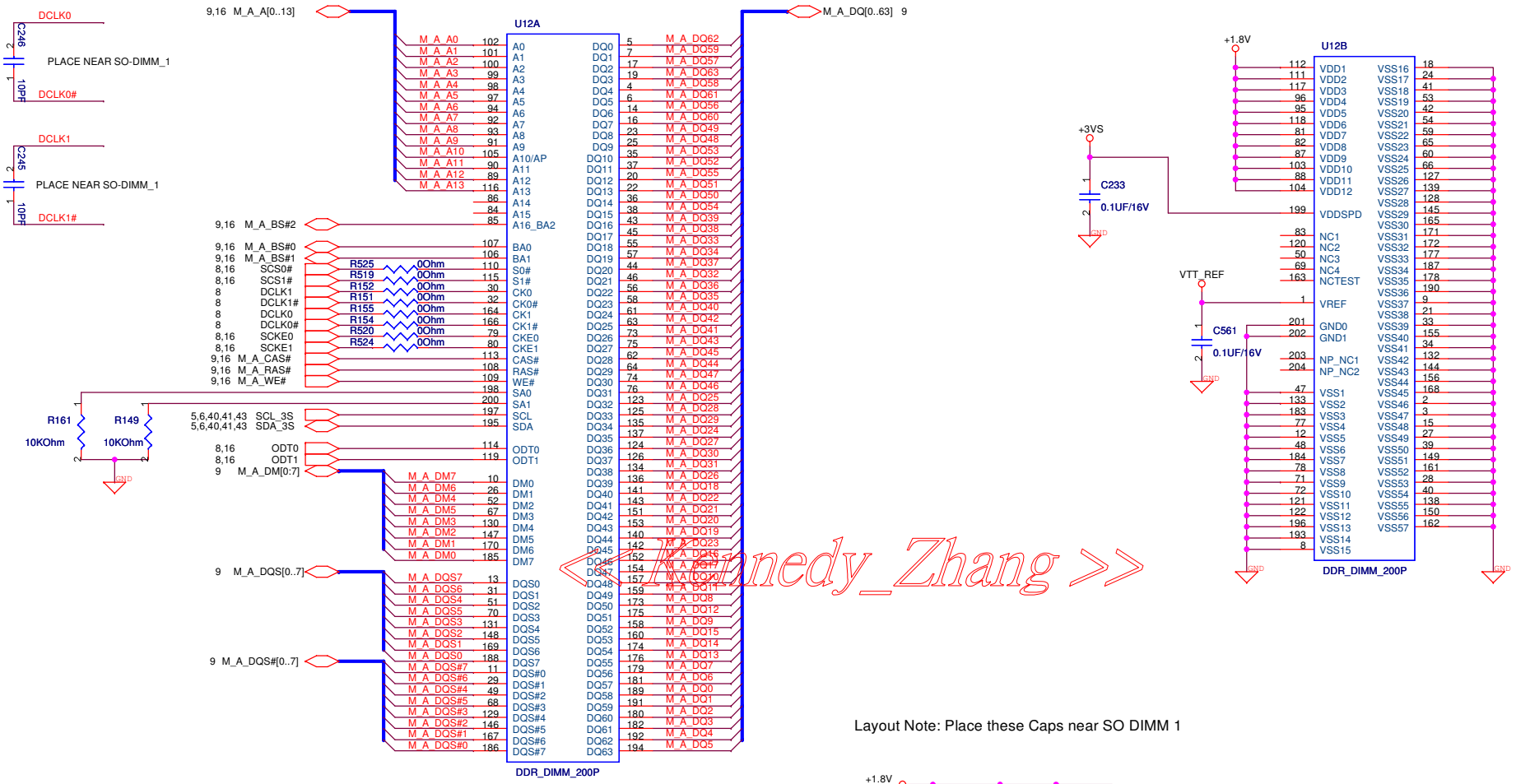
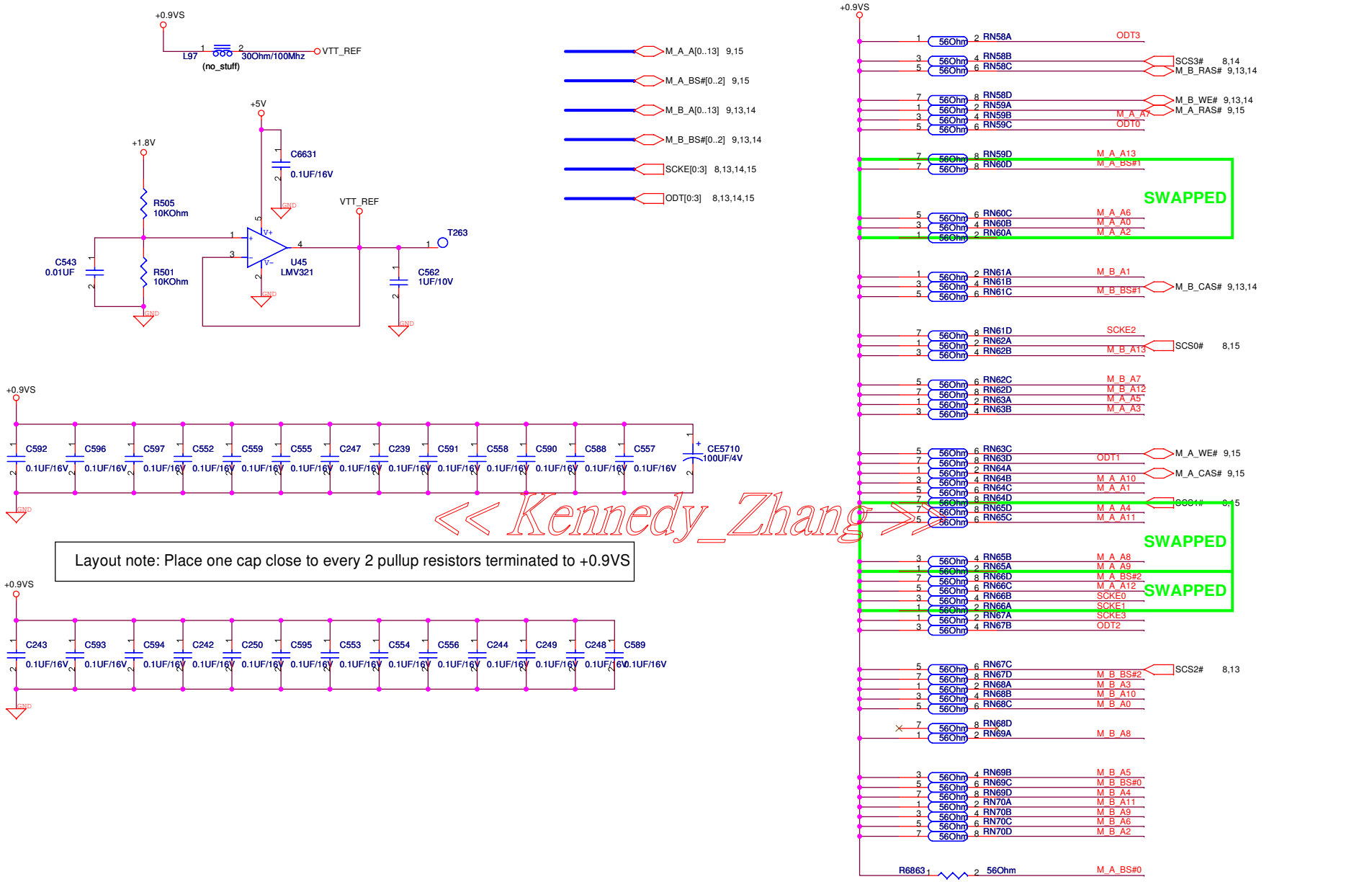
M_B_DQ5
M_B_DQ2
M_B_DQ4
M_B_DQ3
M_B_DQ56
M_B_DQ61
M_B_DQ60
M_B_DQ62
M_B_DQ63
M_B_DQ57
M_B_DQ59
M_B_DQ58
M_B_WE#
M_B_RAS#
M_B_CAS#
SCS2#
SCKE2
DCLK2
DCLK2#
DCLK3
DCLK3#
ODT2
VTT_REF
+1.8V
GND
9,14,16 M_B_BS#0
9,14,16 M_B_BS#1
9,14,16 M_B_BS#2
8,14 DCLK2
8,14 DCLK2#
8,16 SCKE2
8,14 DCLK3
8,14 DCLK3#
8,16 ODT2
M_B_WE# 9,14,16
M_B_RAS# 9,14,16
SCS2# 8,16
M_B_CAS# 9,14,16
C6267
C6268
C6269
C6270
C6271
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5706
150UF/4V
C6272
C6273
C6274
C6275
0.1uF/10V
X7R
9,14 M_B_DM[0:7]
9,14 M_B_DQS[0:7]
9,14 M_B_DQS#[0:7]
9,14,16 M_B_A[0:13]
9,14 M_B_DQ[0:63]
Place either terminator on each side
C6276
4PF/50V
R6564
R6565
200Ohm
C6277
R6566
R6567
C6278
C6279
C6280
C6281
<Variant Name>
Title : DDRON BOARD(TOP)
Engineer:
ASUSTeK COMPUTER INC
Size
Custom
Project Name
W7J
Rev
2.0
Date: Thursday, August 31, 2006
Sheet 13 of 64


U6018
U6017
U6019
U6020
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
SCKE3
DCLK3
DCLK3#
ODT3
VTT_REF
M_B_DM2
M_B_DM6
M_B_DQS2
M_B_DQS6
M_B_DQS#2
M_B_DQS#6
M_B_DM3
M_B_DM4
M_B_DQS3
M_B_DQS4
M_B_DQS#3
M_B_DQS#4
M_B_DM1
M_B_DM5
M_B_DQS1
M_B_DQS5
M_B_DQS#1
M_B_DQS#5
M_B_DM0
M_B_DM7
M_B_DQS0
M_B_DQS7
M_B_DQS#0
M_B_DQS#7
M_B_WE#
M_B_RAS#
SCS3#
M_B_CAS#
+1.8V
GND
Layout Note: Place these Caps near Memory Module
C6282
C6283
C6284
C6285
C6286
2.2UF/6.3V X5R
CE5707 150UF/4V (no_stuff)
C6287
C6288
C6289
C6290
0.1uF/10V X7R
C6291
C6292
C6293
C6294
M_B_DM[0:7]
M_B_DQS[0:7]
M_B_DQS#[0:7]
M_B_A[0:13]
M_B_DQ[0:63]
VTT_REF
<Variant Name>
Title : DDR2 ON BOARD(BOT)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
2.0
Date: Thursday, August 31, 2006
Sheet 14 of 64





Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

<Variant Name>

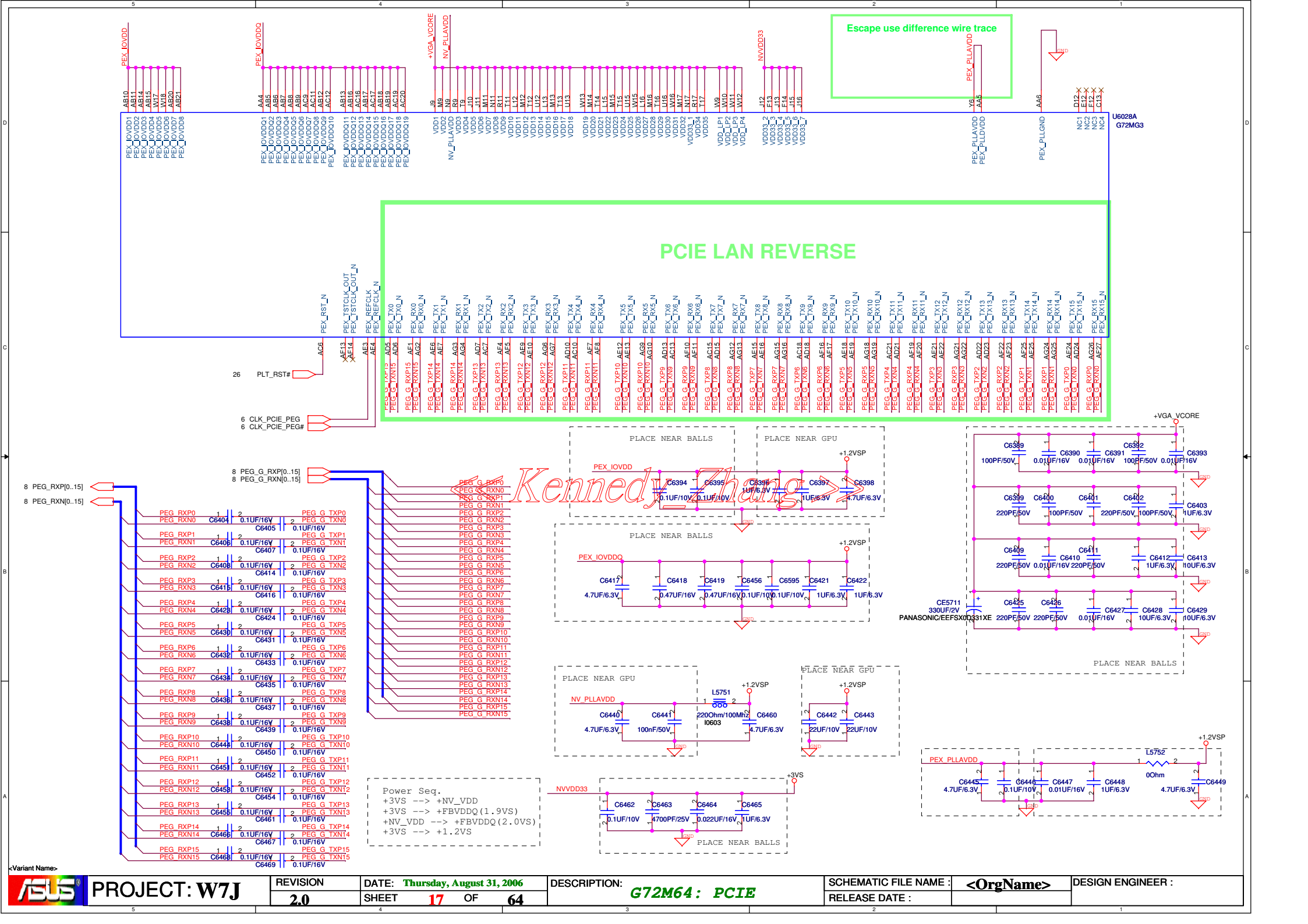
ASUSTeK COMPUTER INC

Title : DDR2 ADDR TERM

Engineer:

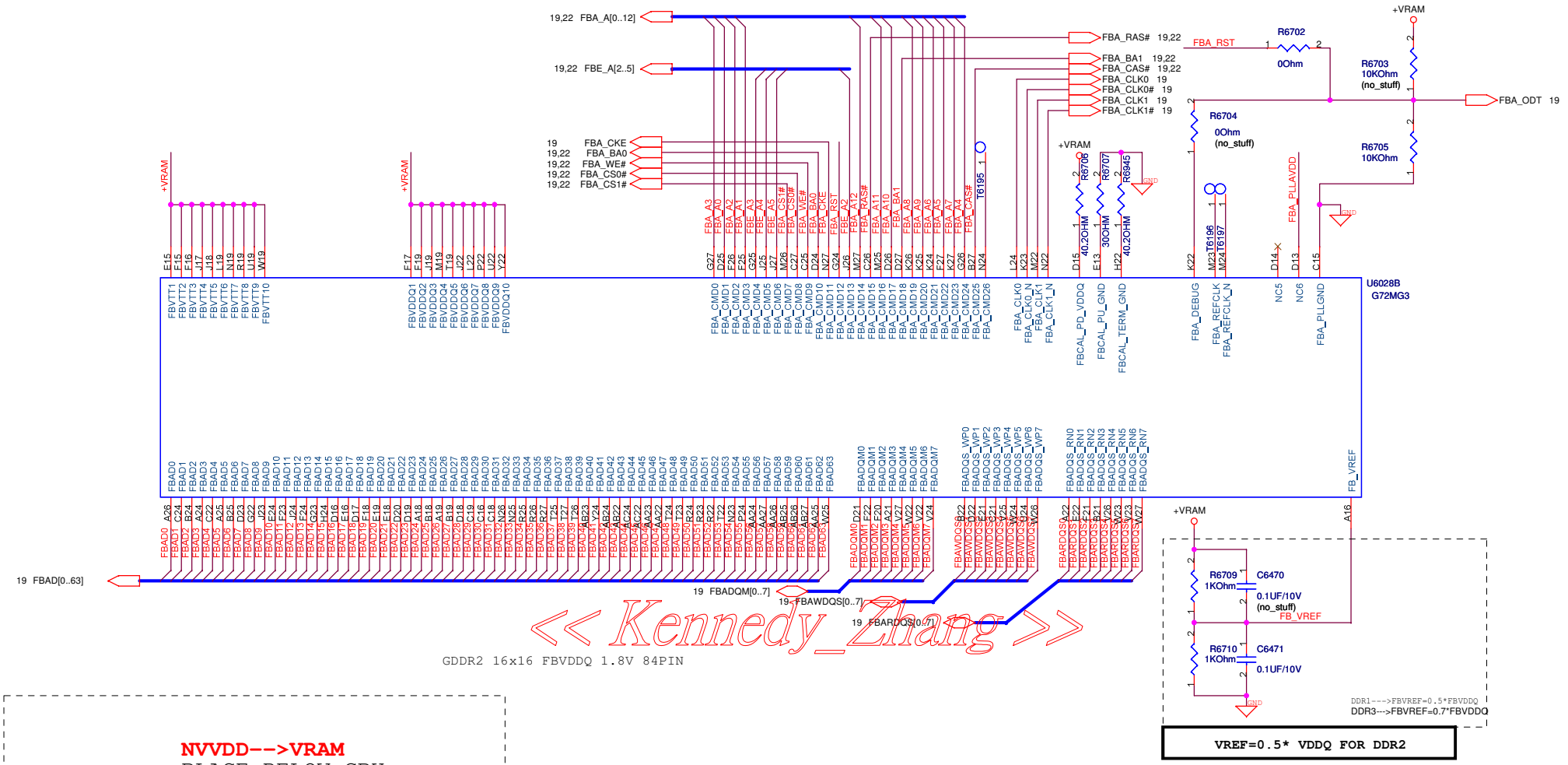
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 16 of 64



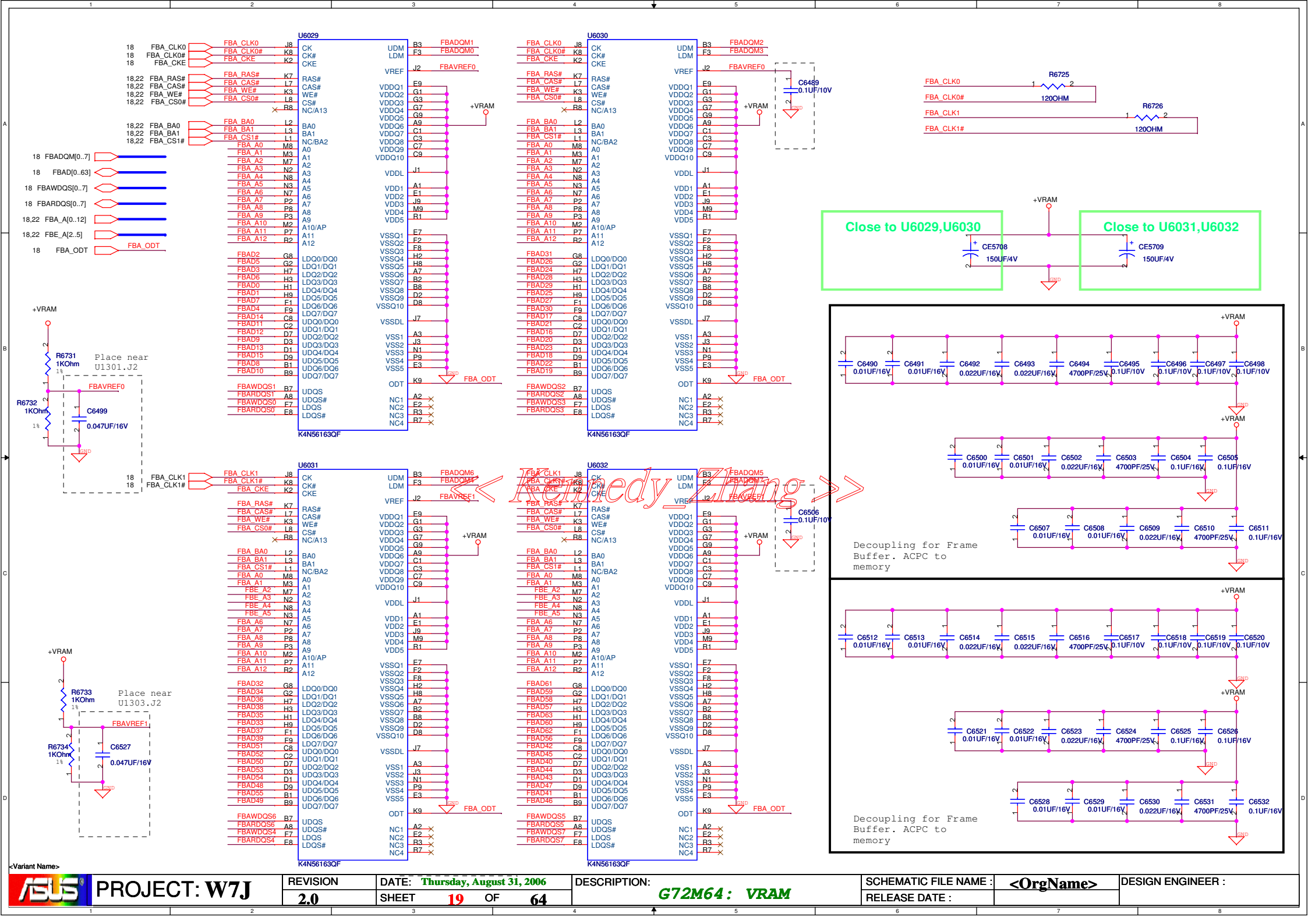
<Variant Name>

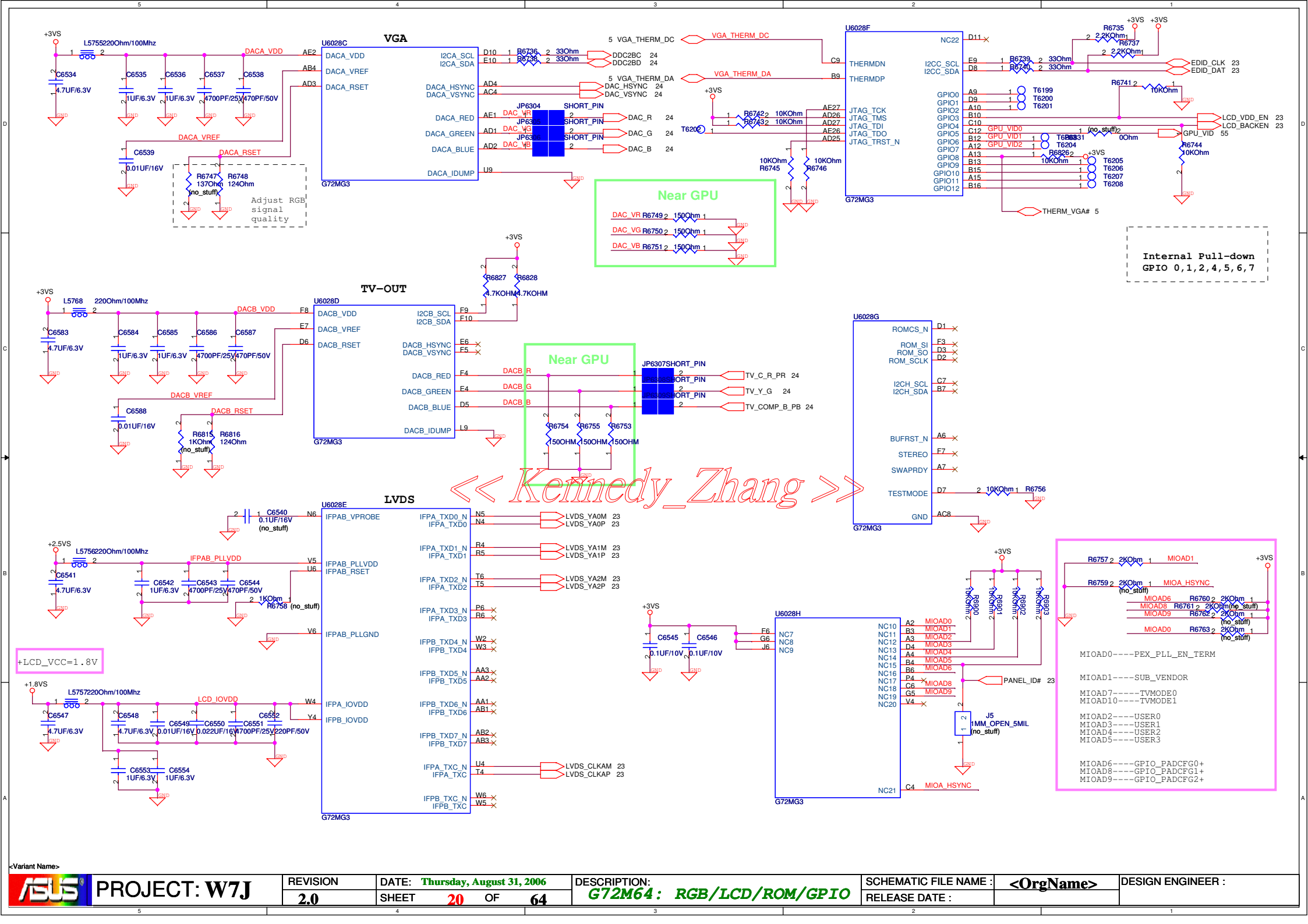
PROJECT: W7J	REVISION	DATE: Thursday, August 31, 2006	DESCRIPTION: G72M64 : PCIE	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
	2.0	SHEET 17 OF 64		RELEASE DATE :	



<Variant Name>

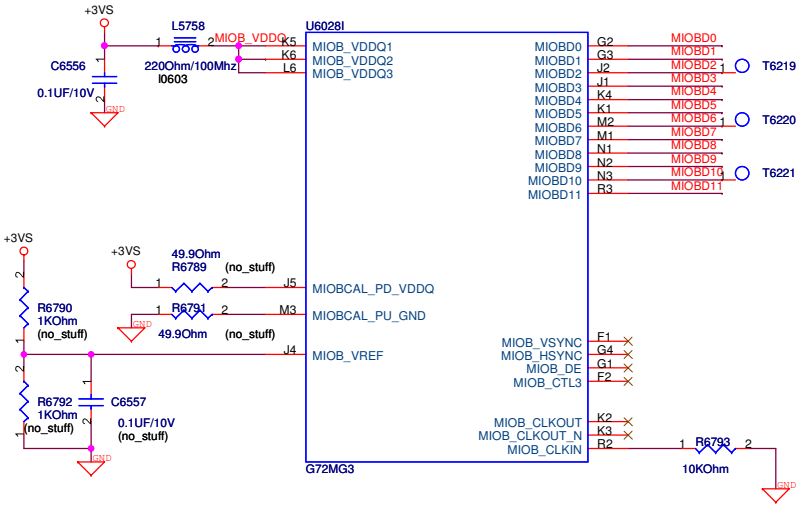
PROJECT: W7J	REVISION 2.0	DATE: Thursday, August 31, 2006	DESCRIPTION: G72M64 : FB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 18 OF 64		RELEASE DATE :	

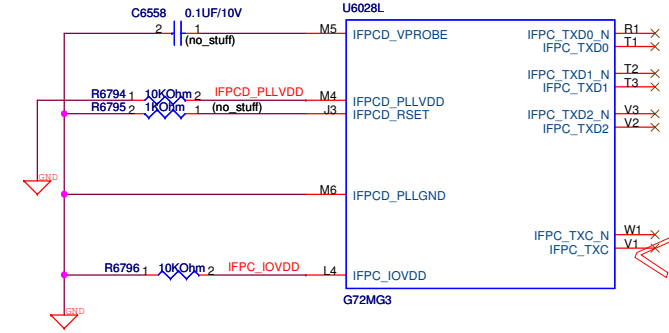

U6029
U6030
U6031
U6032
K4N56163QF
FBA_CLK0
FBA_CLK0#
FBA_CKE
FBA_RAS#
FBA_CAS#
FBA_WE#
FBA_CS0#
FBA_BA0
FBA_BA1
FBA_CS1#
FBA_A0
FBA_A1
FBA_A2
FBA_A3
FBA_A4
FBA_A5
FBA_A6
FBA_A7
FBA_A8
FBA_A9
FBA_A10
FBA_A11
FBA_A12
FBA_CLK1
FBA_CLK1#
FBA_CKE
FBA_ODT
+VRAM
FBAVREF0
FBAVREF1
R6731 1KOhm
R6732 1KOhm
R6733 1KOhm
R6734 1KOhm
C6499 0.047UF/16V
C6527 0.047UF/16V
Place near U1301.J2
Place near U1303.J2
R6725 120OHM
R6726 120OHM
C6489 0.1UF/10V
CE5708 150UF/4V
CE5709 150UF/4V
Close to U6029,U6030
Close to U6031,U6032
C6490 0.01UF/16V
C6491 0.01UF/16V
C6492 0.022UF/16V
C6493 0.022UF/16V
C6494 4700PF/25V
C6495 0.1UF/10V
C6496 0.1UF/10V
C6497 0.1UF/10V
C6498 0.1UF/10V
C6500 0.01UF/16V
C6501 0.01UF/16V
C6502 0.022UF/16V
C6503 4700PF/25V
C6504 0.1UF/16V
C6505 0.1UF/16V
C6506 0.1UF/10V
C6507 0.01UF/16V
C6508 0.01UF/16V
C6509 0.022UF/16V
C6510 4700PF/25V
C6511 0.1UF/16V
C6512 0.01UF/16V
C6513 0.01UF/16V
C6514 0.022UF/16V
C6515 0.022UF/16V
C6516 4700PF/25V
C6517 0.1UF/10V
C6518 0.1UF/10V
C6519 0.1UF/10V
C6520 0.1UF/10V
C6521 0.01UF/16V
C6522 0.01UF/16V
C6523 0.022UF/16V
C6524 4700PF/25V
C6525 0.1UF/16V
C6526 0.1UF/16V
C6528 0.01UF/16V
C6529 0.01UF/16V
C6530 0.022UF/16V
C6531 4700PF/25V
C6532 0.1UF/16V
Decoupling for Frame Buffer. ACPC to memory
Decoupling for Frame Buffer. ACPC to memory
<Variant Name>
PROJECT: W7J
REVISION 2.0
DATE: Thursday, August 31, 2006
SHEET 19 OF 64
DESCRIPTION: G72M64 : VRAM
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER :

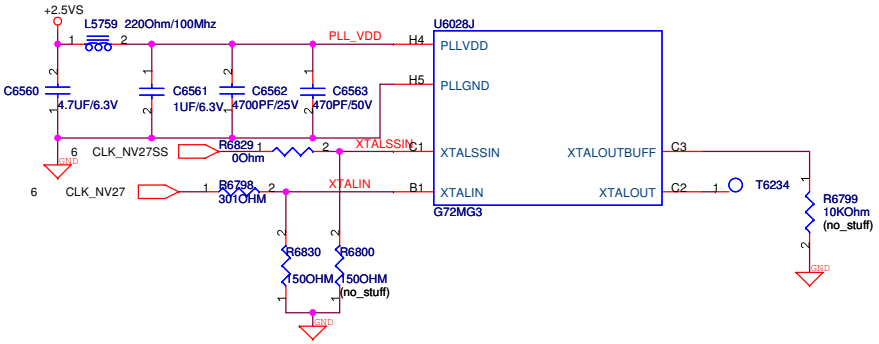


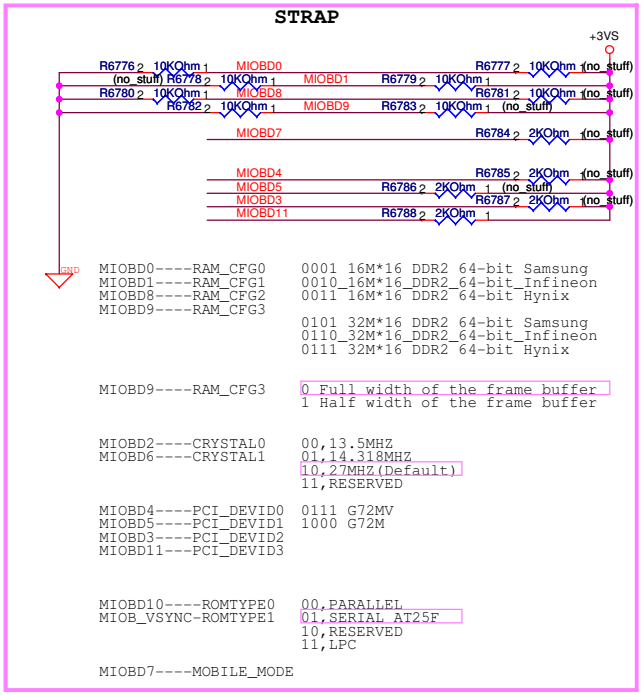
<Variant Name>

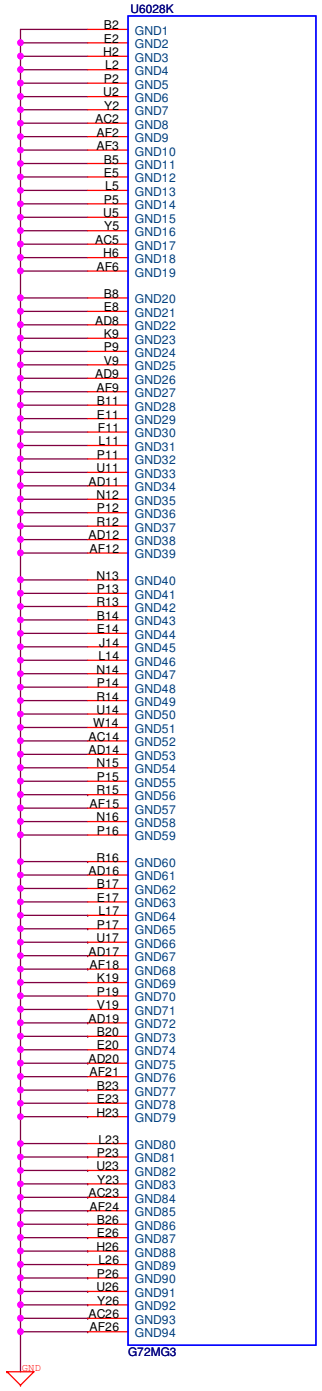
PROJECT: W7J	REVISION	DATE: Thursday, August 31, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	2.0	SHEET 20 OF 64	G72M64 : RGB/LCD/ROM/GPIO	RELEASE DATE :	<OrgName>







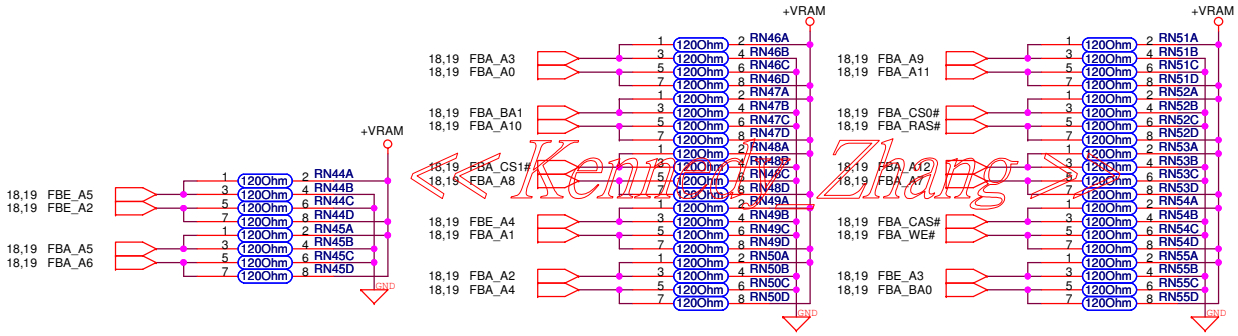




<Variant Name>

PROJECT: W7J	REVISION 2.0	DATE: Thursday, August 31, 2006	DESCRIPTION: G72M64 : MIOB/CRYSTAL/TMDS	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 21 OF 64		RELEASE DATE :	

FBA CMD/ADDR Termination



<Variant Name>

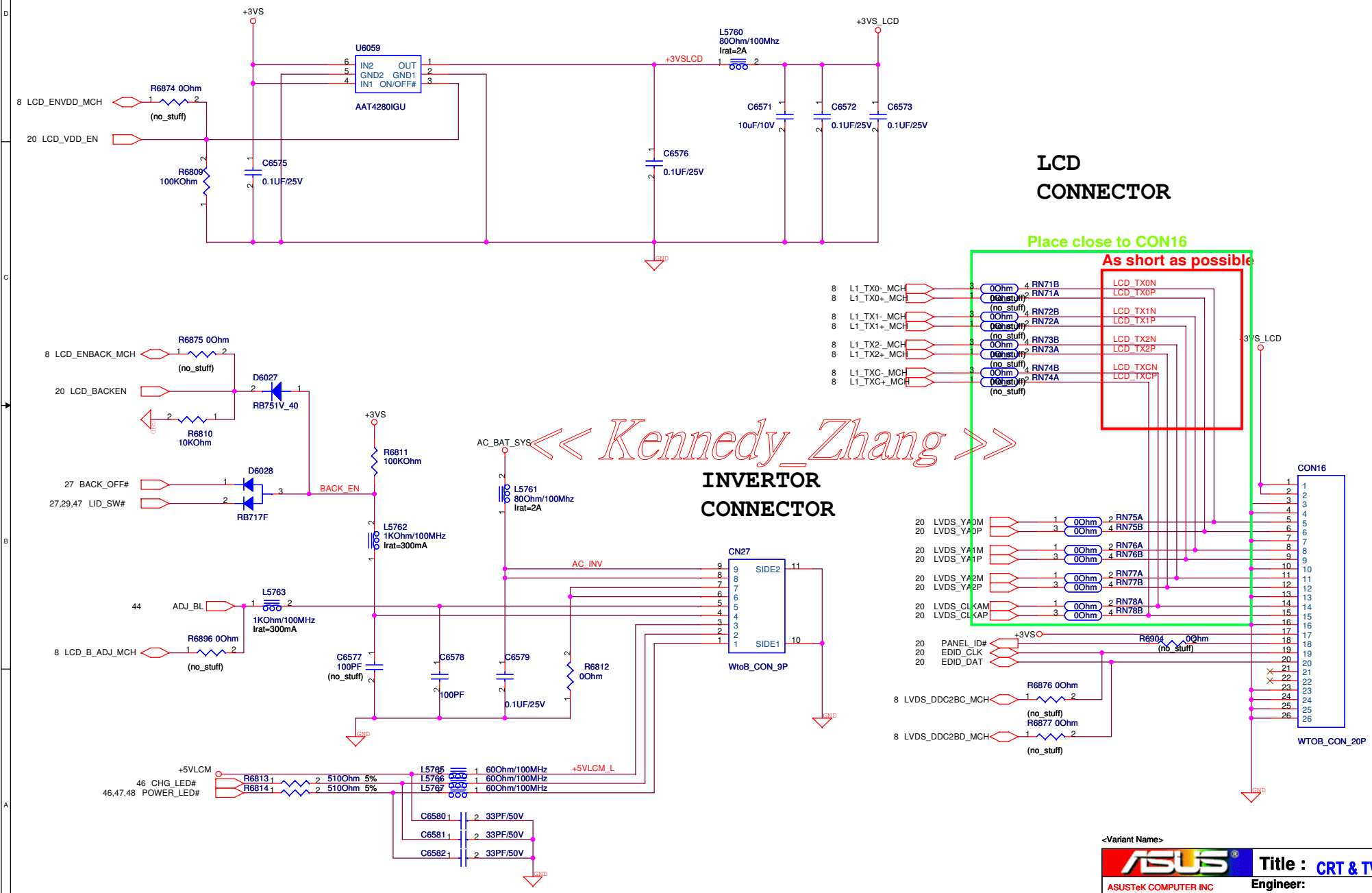
ASUSTeK COMPUTER INC

Title : G72M-Terminator

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 22 of 64



<Variant Name>

ASUSTeK COMPUTER INC

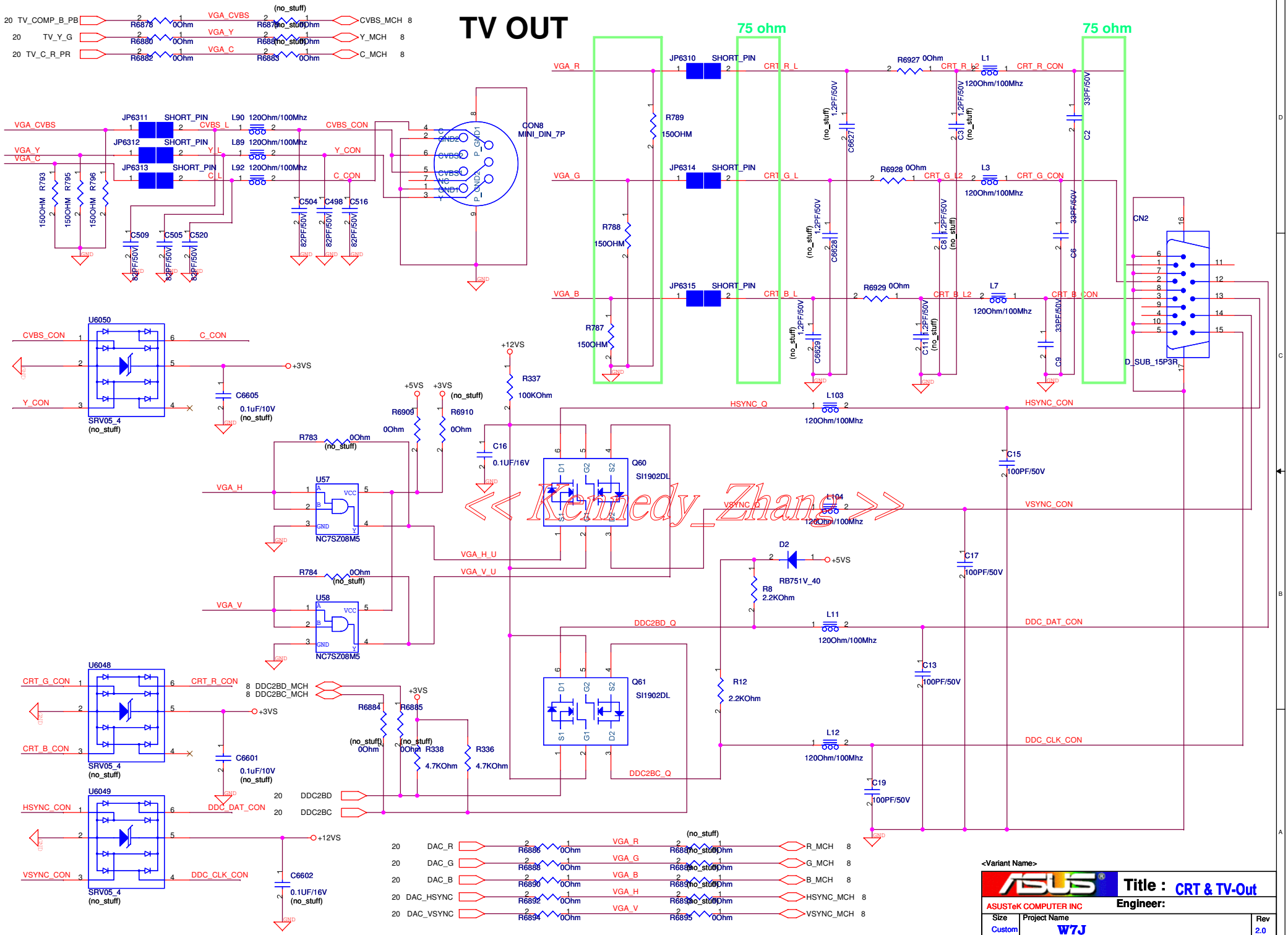
Title : CRT & TV-Out

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

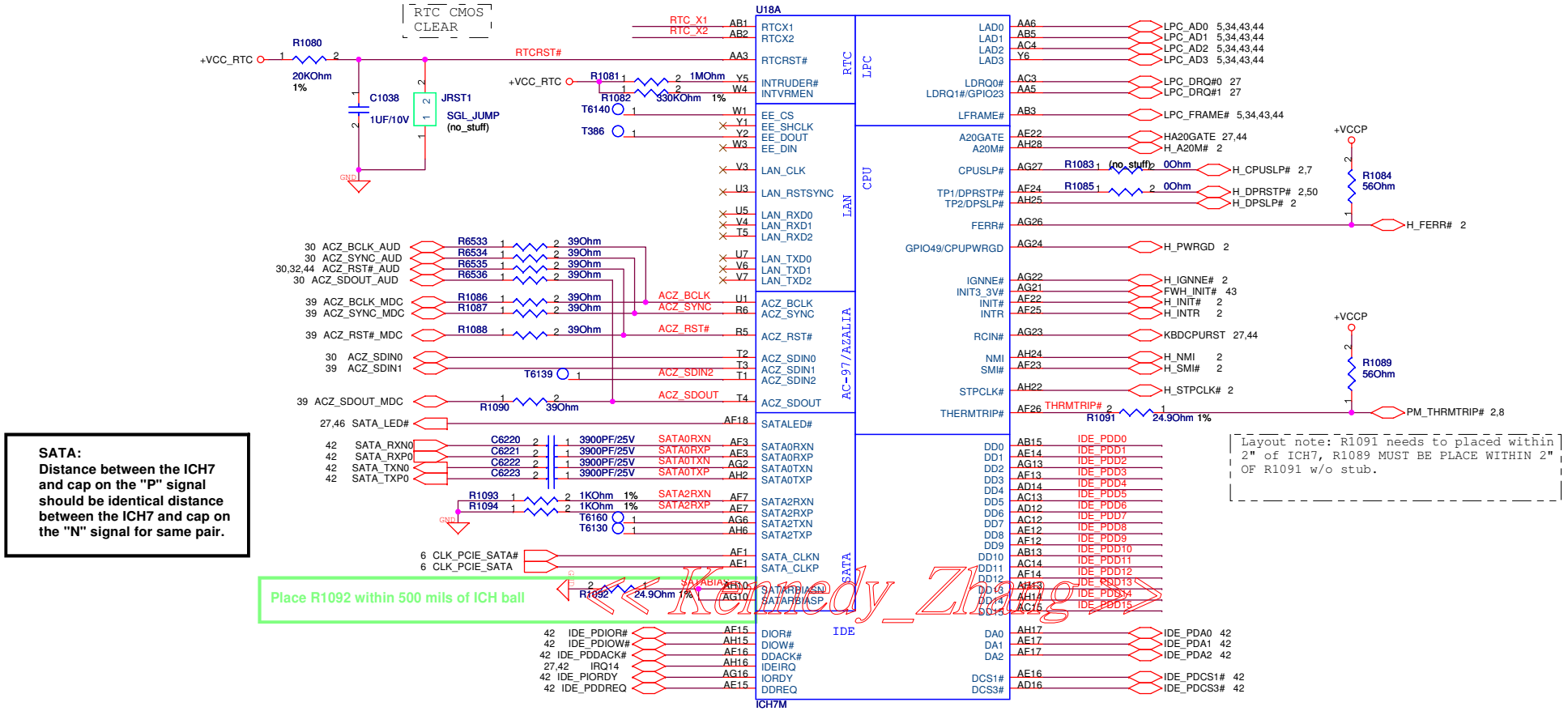
Date: Thursday, August 31, 2006 Sheet 23 of 64

TV OUT



<Variant Name>

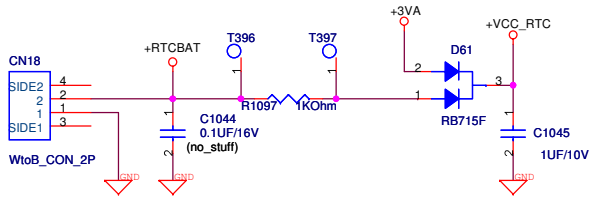
ASUSTeK COMPUTER INC	Title : CRT & TV-Out	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 24 of 64	

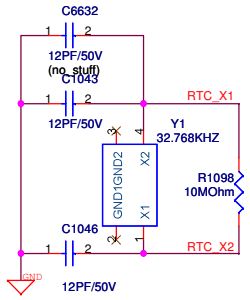


SATA:
Distance between the ICH7 and cap on the "P" signal should be identical distance between the ICH7 and cap on the "N" signal for same pair.

SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.

RTC BAT





RTC Battery
P/N=07-016322032

<Variant Name>

Title : ICH7-M (1)

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 25 of 64

36 PCI_AD[0..31] — PCI_AD[0..31]

ICH7 Boot BIOS select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

GNT#3 without PD, if NOT top-block swap(inter high)

U18B — ICH7M

PCI: AD0–AD31 (E18, C18, A16, E16, F18, E16, E17, A17, A15, C14, E14, D14, B12, C13, G15, G13, E12, C11, D11, A11, A10, F11, E10, E9, D9, B9, A8, A6, C7, B6, E6, D6)

REQ#0 D7 — PCI_REQ#0 27,36
GNT0# E7 — PCI_GNT#0 36
REQ#1 C16 — PCI_REQ#1 27 — T6133
GNT1# D16 — T6170
REQ2# C17 — PCI_REQ#2 27 — R6403 1KOhm (no_stuff)
GNT2# D17
REQ3# E13 — PCI_REQ#3 27
GNT3# F13
REQ4#/GPIO22 A13 — PCI_REQ#4 27 — T6135
GNT4#/GPIO48 A14
GPIO1/REQ5# C8 — PCI_REQ#5 27 — T6136
GPIO17/GNT5# D8

C/BE0# B15 — PCI_C/BE#0 36
C/BE1# C12 — PCI_C/BE#1 36
C/BE2# D12 — PCI_C/BE#2 36
C/BE3# C15 — PCI_C/BE#3 36

IRDY# A7 — PCI_IRDY# 27,36
PAR E10 — PCI_PAR 36
PCIRST# B18 — PCI_RST#_ICH
DEVSEL# A12 — PCI_DEVSEL# 27,36
PERR# C9 — PCI_PERR# 27,36
PLOCK# E11 — PCI_LOCK# 27
SERR# B10 — PCI_SERR# 27,36
STOP# F15 — PCI_STOP# 27,36
TRDY# F14 — PCI_TRDY# 27,36
FRAME# F16 — PCI_FRAME# 27,36

PLTRST# C26 — PLT_RST#_SB
PCICLK A9 — CLK_ICHPCI 6
PME# B19

+3VSUS — R6568 10KOhm

Interrupt I/F

27 PCI_INTA# — PIRQA# A3 — GPIO2/PIRQE# G8 — PCI_INTE# 27,36
27 PCI_INTB# — PIRQB# B4 — GPIO3/PIRQF# F7 — PCI_INTF# 27,36
27 PCI_INTC# — PIRQC# C5 — GPIO4/PIRQG# F8 — PCI_INTG# 27
27 PCI_INTD# — PIRQD# B5 — GPIO5/PIRQH# G7 — PCI_INTH# 27

MISC

T400 T403 T406 T409 T411 — RSVD_1 AE5, RSVD_2 AD5, RSVD_3 AG4, RSVD_4 AH4, RSVD_5 AD9
RSVD_6 AE9 — T401
RSVD_7 AG8 — T404
RSVD_8 AH8 — T407
RSVD_9 F21 — T410
MCH_SYNC# AH20 — MCH_SYNC# 8

pull up to +3VS by internal pull-up resistor

U18D — ICH7M

PCI-Express / Direct Media Interface

40 PCIE_RXN1 — PERn1 F26 — 0.1UF/10V — C1047 — PETN1 — DMI0RXN V26 — DMI_RXN0 8
40 PCIE_RXP1 — PERp1 F25 — 0.1UF/10V — C1048 — PETP1 — DMI0RXP V25 — DMI_RXP0 8
40 PCIE_TXN1 — PETn1 E28 — DMI0TXN U28 — DMI_TXN0 8
40 PCIE_TXP1 — PETp1 E27 — DMI0TXP U27 — DMI_TXP0 8

38 PCIE_RXN2 — PERn2 H26 — 0.1UF/10V — C1049 — PETN2 — DMI1RXN Y26 — DMI_RXN1 8
38 PCIE_RXP2 — PERp2 H25 — 0.1UF/10V — C1050 — PETP2 — DMI1RXP Y25 — DMI_RXP1 8
38 PCIE_TXN2 — PETn2 G28 — DMI1TXN W28 — DMI_TXN1 8
38 PCIE_TXP2 — PETp2 G27 — DMI1TXP W27 — DMI_TXP1 8

41 PCIE_RXN3 — PERn3 K26 — 0.1UF/10V — C1051 — PETN3 — DMI2RXN AB26 — DMI_RXN2 8
41 PCIE_RXP3 — PERp3 K25 — 0.1UF/10V — C1052 — PETP3 — DMI2RXP AB25 — DMI_RXP2 8
41 PCIE_TXN3 — PETn3 J28 — DMI2TXN AA28 — DMI_TXN2 8
41 PCIE_TXP3 — PETp3 J27 — DMI2TXP AA27 — DMI_TXP2 8

PERn4 M26 — DMI3RXN AD25 — DMI_RXN3 8
PERp4 M25 — DMI3RXP AD24 — DMI_RXP3 8
PETn4 L28 — DMI3TXN AC28 — DMI_TXN3 8
PETp4 L27 — DMI3TXP AC27 — DMI_TXP3 8

PERn5 P26 — DMI_CLKN AE28 — CLK_PCIE_ICH# 6
PERp5 P25 — DMI_CLKP AE27 — CLK_PCIE_ICH 6
PETn5 N28
PETp5 N27

DMI_ZCOMP C25 — DMICOMP
DMI_IRCOMP D25 — R1099 24.9Ohm 1% — +1.5VS
Place within 500 mils of ICH

PERn6 T25
PERp6 T24
PETn6 R28
PETp6 R27

USB

USBP0N F1 — USB_PN0 40
USBP0P F2 — USB_PP0 40
USBP1N G4 — USB_PN1 45
USBP1P G3 — USB_PP1 45
USBP2N H1 — USB_PN2 47
USBP2P H2 — USB_PP2 47
USBP3N J4 — USB_PN3 45
USBP3P J3 — USB_PP3 45
USBP4N K1 — USB_PN4 45
USBP4P K2 — USB_PP4 45
USBP5N L4 — USB_PN5 45
USBP5P L5 — USB_PP5 45
USBP6N M1
USBP6P M2
USBP7N N4 — T405
USBP7P N3 — T408

USBRBIAS# D2 — USBRBIAS
USBRBIAS D1 — R1100 22.6Ohm 1% — GND
Place within 500 mils of ICH

SPI_CLK R2
SPI_CS# P6
SPI_ARB P1
SPI_MOSI P5
SPI_MISO P2

+3V — RN18A 10KOhm (no_stuff) — RN18B 10KOhm (no_stuff)
RN18C 10KOhm (no_stuff) — RN18D 10KOhm (no_stuff)

27,40 USB_OC#0 — OC0# D3
OC1# C4
27 USB_OC#2 — OC2# D5
27,45 USB_OC#13 — OC3# D4
27,45 USB_OC#4 — OC4# E5
27 USB_OC#5 — OC5#/GPIO29 C3
27 USB_OC#6 — OC6#/GPIO30 A2
27 USB_OC#7 — OC7#/GPIO31 B3

<< Kennedy_Zhang >>

8,27,34,38,41,42,43,44 BUF_PLT_RST# — U68D 74HC08 — PLT_RST#_SB — +3V — C1056 0.01UF (no_stuff)

+3V — R1102 10KOhm — C1054 0.1UF/16V

17 PLT_RST# — R6408 0Ohm (no_stuff) — U68C 74HC08 — PLT_RST#_SB — R1104 0Ohm (no_stuff) — SW_RST# 27
R1106 0Ohm

+3V — C1053 0.1UF/16V — U68A 74HC08 — 36,40,42 PCI_RST# — PCI_RST#_ICH

+3V — C1055 0.1UF/16V — U69 74LVC1G32GV — PCI_RST# — 44 SET_PCIRSTNS# — R1108 10KOhm — R1109 47KOhm — C1057 0.01UF — PCI_RSTNS# 36,44

Can be issue SCI or SMI List: GPIO0~GPIO15

Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28

Only GPI Pin: GPIO0~8,11~15,26,29,30,31,40(5V),41
Only GPO Pin: GPIO16~17,19,21,23,48
Can be GPIO: GPIO24,25,27,28,33,34

Resume Power Input Pin List:
BATLOW#,AC_SDIN[0:1],LAN_RST#,
OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#

<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 26 of 64

The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

U18C

ICH7M

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SATA GPIO: GPIO21/SATA0GP, GPIO19/SATA1GP, GPIO36/SATA2GP, GPIO37/SATA3GP

Clocks: CLK14, CLK48, SUSCLK

SYS GPIO: RI#, SPKR, SUS_STAT#, SYS_RST#, GPIO0/BM_BUSY#, SMBALERT#/GPIO11, GPIO18/STPPCI#, GPIO20/STPCPU#, GPIO26, GPIO27, GPIO28, GPIO32/CLKRUN#, GPIO33/AZ_DOCK_EN#, GPIO34/AZ_DOCK_RST#, WAKE#, SERIRQ, THRM#, VRMPWRGD

Power MGT: SLP_S3#, SLP_S4#, SLP_S5#, PWROK, GPIO16/DPRSLPVR, TP0/BATLOW#, PWRBTN#, LAN_RST#, RSMRST#

GPIO: GPIO6, GPIO7, GPIO8, GPIO9, GPIO10, GPIO12, GPIO13, GPIO14, GPIO15, GPIO24, GPIO25, GPIO35, GPIO38, GPIO39

GPIO 16 should NOT pull high(inter low)

GPIO 25 should NOT pull low(inter high)

533Mhz 1
667Mhz 0

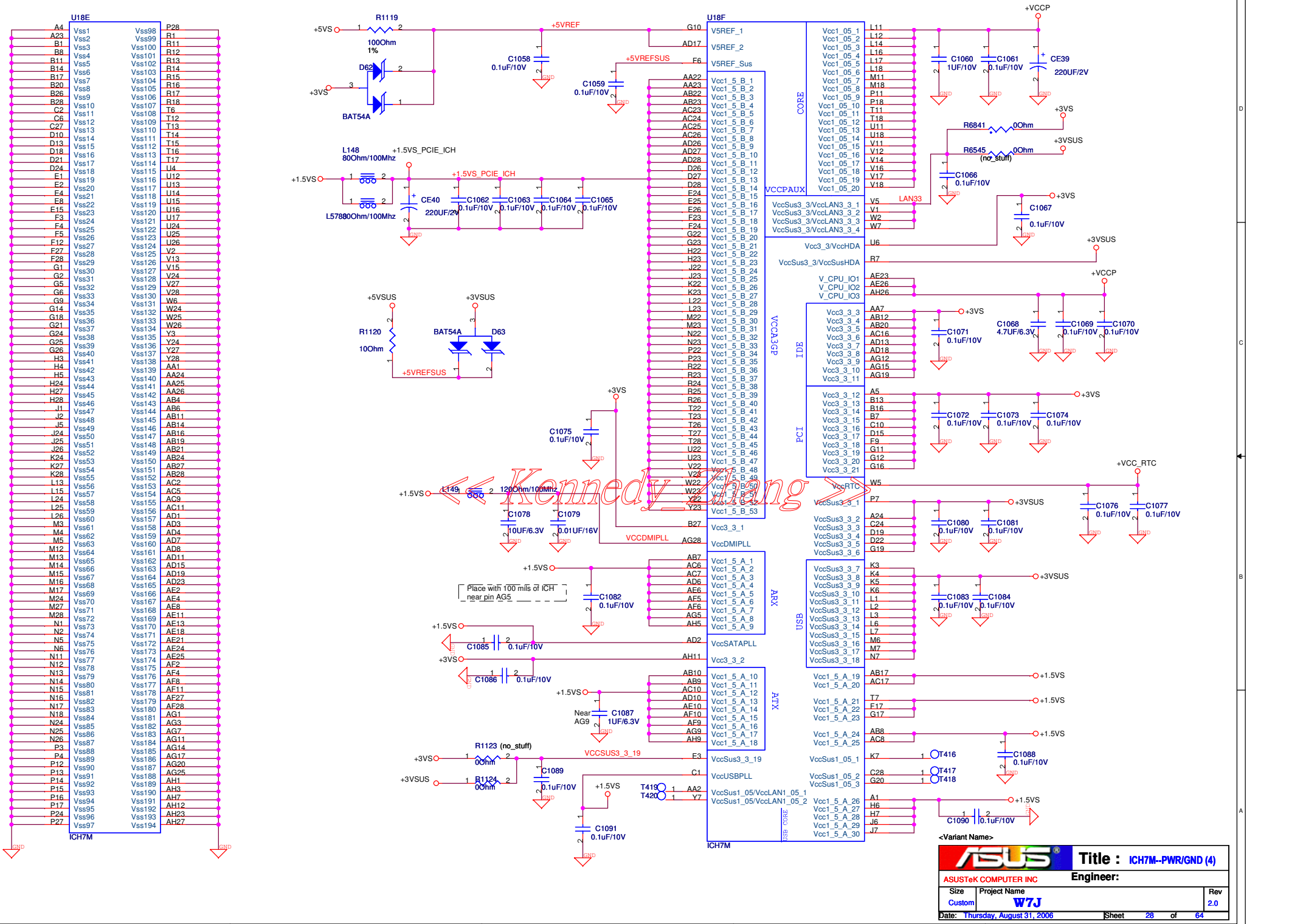
512M 1 0 1
256M 0 0 1

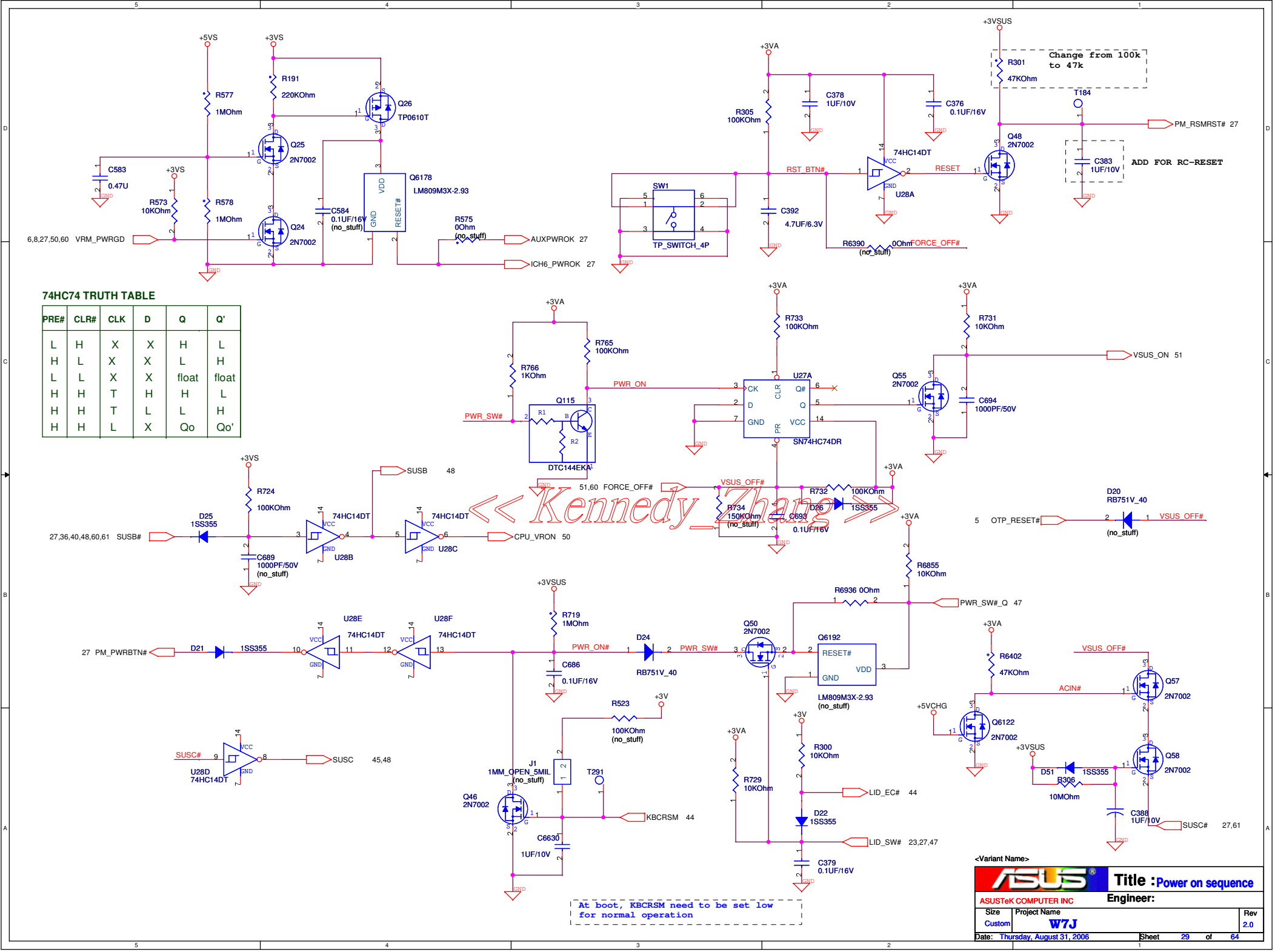
<< Kennedy Zhang >>

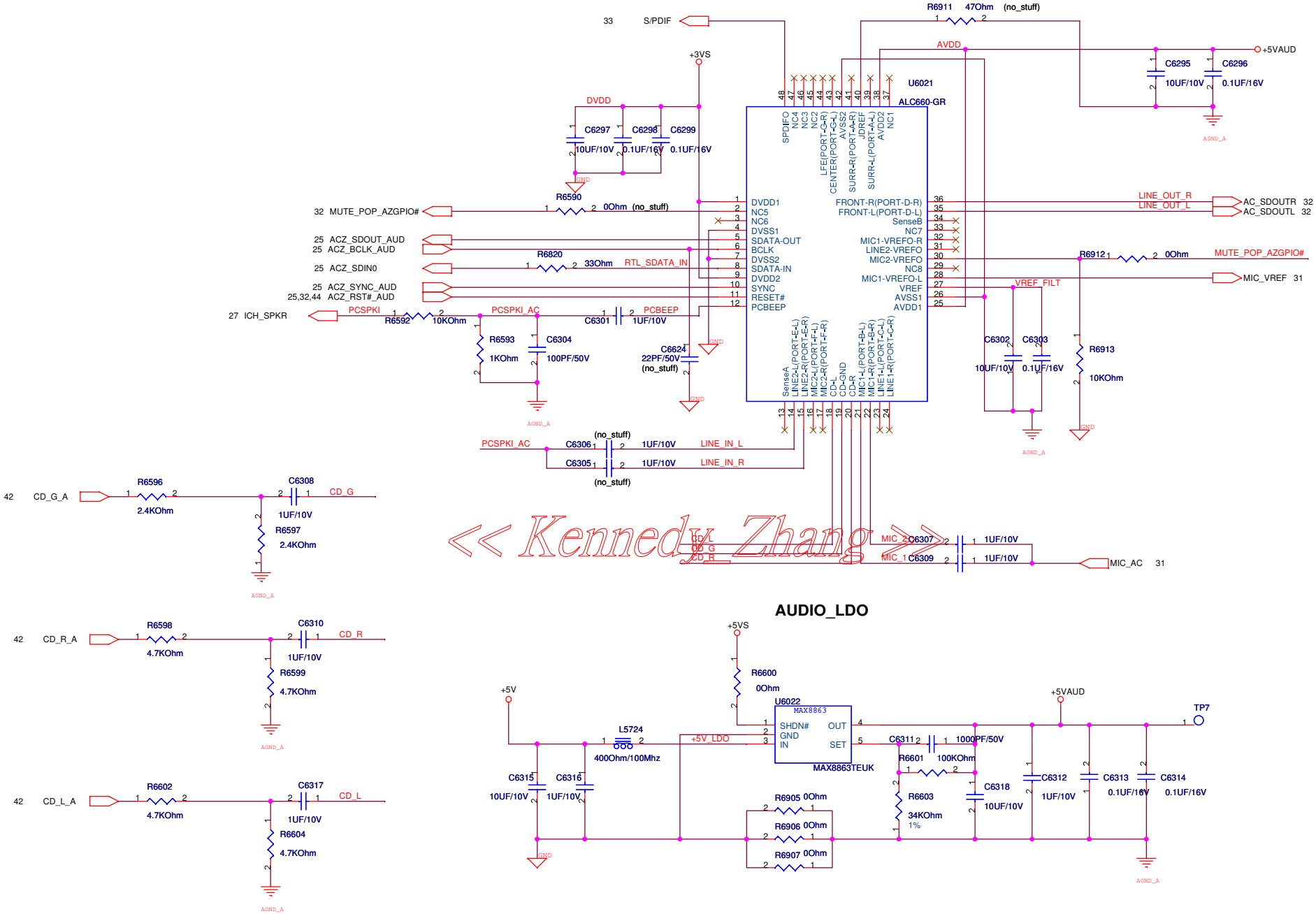
Q6197 2N7002

<Variant Name>

ASUSTeK COMPUTER INC	Title : ICH7M-(3)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 27 of 64	


U18E
ICH7M
U18F
ICH7M
R1119
100Ohm
1%
D62
BAT54A
+5VS
+3VS
+5VREF
C1058
0.1uF/10V
C1059
0.1uF/10V
+5VREFSUS
L148
80Ohm/100Mhz
L57880Ohm/100Mhz
+1.5VS
+1.5VS_PCIE_ICH
CE40
220UF/2V
C1062
C1063
C1064
C1065
0.1uF/10V
R1120
10Ohm
BAT54A
D63
+5VSUS
+3VSUS
+5VREFSUS
C1075
0.1uF/10V
L149
120Ohm/100Mhz
C1078
10UF/6.3V
C1079
0.01UF/16V
VCCDMIPLL
Place with 100 mils of ICH
near pin AG5
C1082
0.1uF/10V
C1085
0.1uF/10V
C1086
0.1uF/10V
Near
AG9
C1087
1UF/6.3V
R1123 (no_stuff)
0Ohm
R1124
0Ohm
VCCSUS3_3_19
C1089
0.1uF/10V
C1091
0.1uF/10V
T419
T420
CORE
VCCPAUX
LAN33
IDE
VCCA3GP
PCI
USB
ARX
ATX
USB CORE
C1060
1UF/10V
C1061
0.1uF/10V
CE39
220UF/2V
R6841
0Ohm
R6545
0Ohm
(no_stuff)
C1066
0.1uF/10V
C1067
0.1uF/10V
C1068
4.7UF/6.3V
C1069
0.1uF/10V
C1070
0.1uF/10V
C1071
0.1uF/10V
C1072
0.1uF/10V
C1073
0.1uF/10V
C1074
0.1uF/10V
C1076
0.1uF/10V
C1077
0.1uF/10V
C1080
0.1uF/10V
C1081
0.1uF/10V
C1083
0.1uF/10V
C1084
0.1uF/10V
C1088
0.1uF/10V
C1090
0.1uF/10V
T416
T417
T418
+VCCP
+VCC_RTC
+1.5VS
+3VS
+3VSUS
<Variant Name>
Title : ICH7M--PWR/GND (4)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: W7J
Rev: 2.0
Date: Thursday, August 31, 2006
Sheet 28 of 64

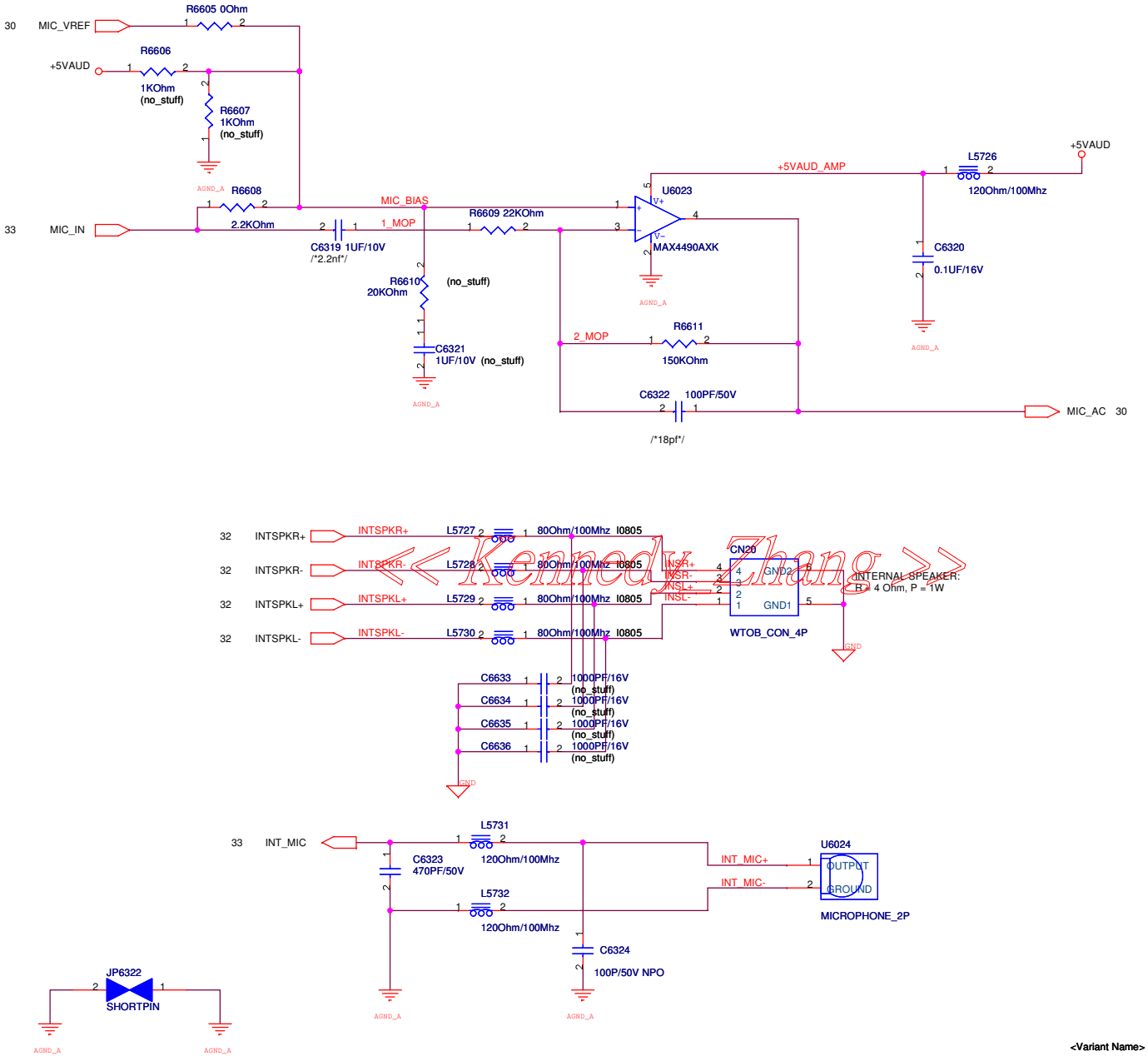

+5VS
+3VS
R577
1MOhm
R191
220KOhm
Q26
TP0610T
Q25
2N7002
C583
0.47U
R573
10KOhm
R578
1MOhm
Q24
2N7002
C584
0.1UF/16V
(no_stuff)
Q6178
LM809M3X-2.93
R575
0Ohm
(no_stuff)
6,8,27,50,60 VRM_PWRGD
AUXPWROK 27
ICH6_PWROK 27
+3VA
R305
100KOhm
C378
1UF/10V
C376
0.1UF/16V
74HC14DT
U28A
RST_BTN#
RESET
SW1
TP_SWITCH_4P
C392
4.7UF/6.3V
R6390
0Ohm
(no_stuff)
FORCE_OFF#
+3VSUS
R301
47KOhm
Change from 100k
to 47k
T184
PM_RSMRST# 27
Q48
2N7002
C383
1UF/10V
ADD FOR RC-RESET
74HC74 TRUTH TABLE
PRE# CLR# CLK D Q Q'
L H X X H L
H L X X L H
L L X X float float
H H T H H L
H H T L L H
H H L X Qo Qo'
R765
100KOhm
R766
1KOhm
PWR_ON
PWR_SW#
Q115
DTC144EKA
U27A
SN74HC74DR
R733
100KOhm
R731
10KOhm
VSUS_ON 51
Q55
2N7002
C694
1000PF/50V
+3VS
R724
100KOhm
SUSB 48
D25
1SS355
27,36,40,48,60,61 SUSB#
74HC14DT
U28B
U28C
C689
1000PF/50V
(no_stuff)
51,60 FORCE_OFF#
VSUS_OFF
R732
100KOhm
R734
150KOhm
(no_stuff)
D26
1SS355
C693
0.1UF/16V
CPU_VRON 50
D20
RB751V_40
5 OTP_RESET#
VSUS_OFF#
(no_stuff)
R6855
10KOhm
R6936 0Ohm
PWR_SW#_Q 47
U28E
U28F
74HC14DT
27 PM_PWRBTN#
D21
1SS355
R719
1MOhm
PWR_ON#
D24
RB751V_40
PWR_SW#
C686
0.1UF/16V
Q50
2N7002
Q6192
RESET#
VDD
GND
LM809M3X-2.93
(no_stuff)
R523
100KOhm
(no_stuff)
+3V
SUSC# 9
U28D
74HC14DT
8 SUSC 45,48
J1
1MM_OPEN_5MIL
(no_stuff)
T291
Q46
2N7002
KBCRSM 44
C6630
1UF/10V
R300
10KOhm
R729
10KOhm
LID_EC# 44
D22
1SS355
LID_SW# 23,27,47
C379
0.1UF/16V
R6402
47KOhm
ACIN#
Q57
2N7002
+5VCHG
Q6122
2N7002
Q58
2N7002
D51
1SS355
R306
10MOhm
C388
1UF/10V
SUSC# 27,61
At boot, KBCRSM need to be set low
for normal operation
<Variant Name>
Title : Power on sequence
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 29 of 64



<Variant Name>

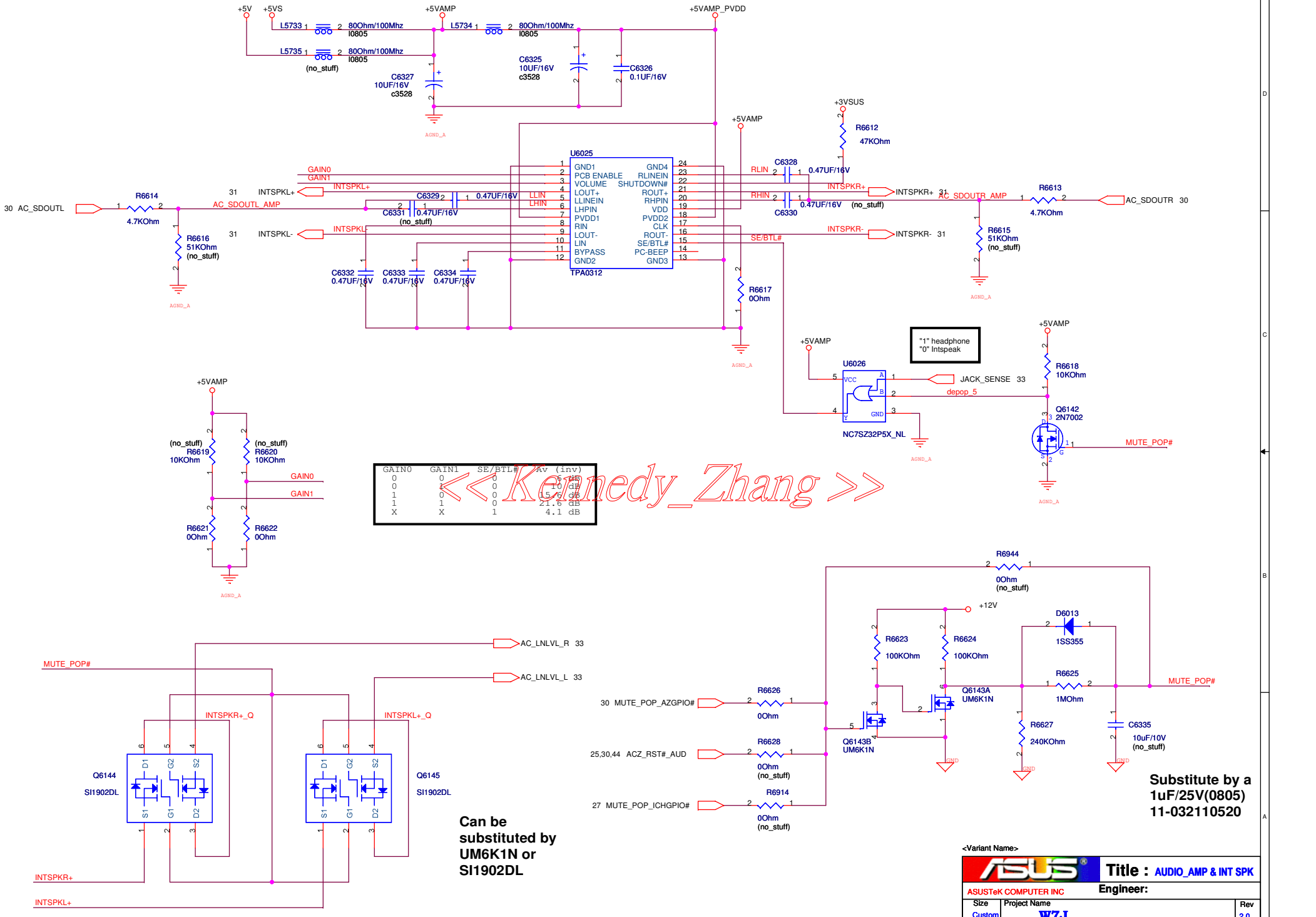
ASUSTeK COMPUTER INC	Title : AZALIA_ALC660	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 30 of 64	

MIC PreAmp & Mic Jack



<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC PREAMP & INT MIC	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 31 of 64	



<Variant Name>

ASUSTeK COMPUTER INC

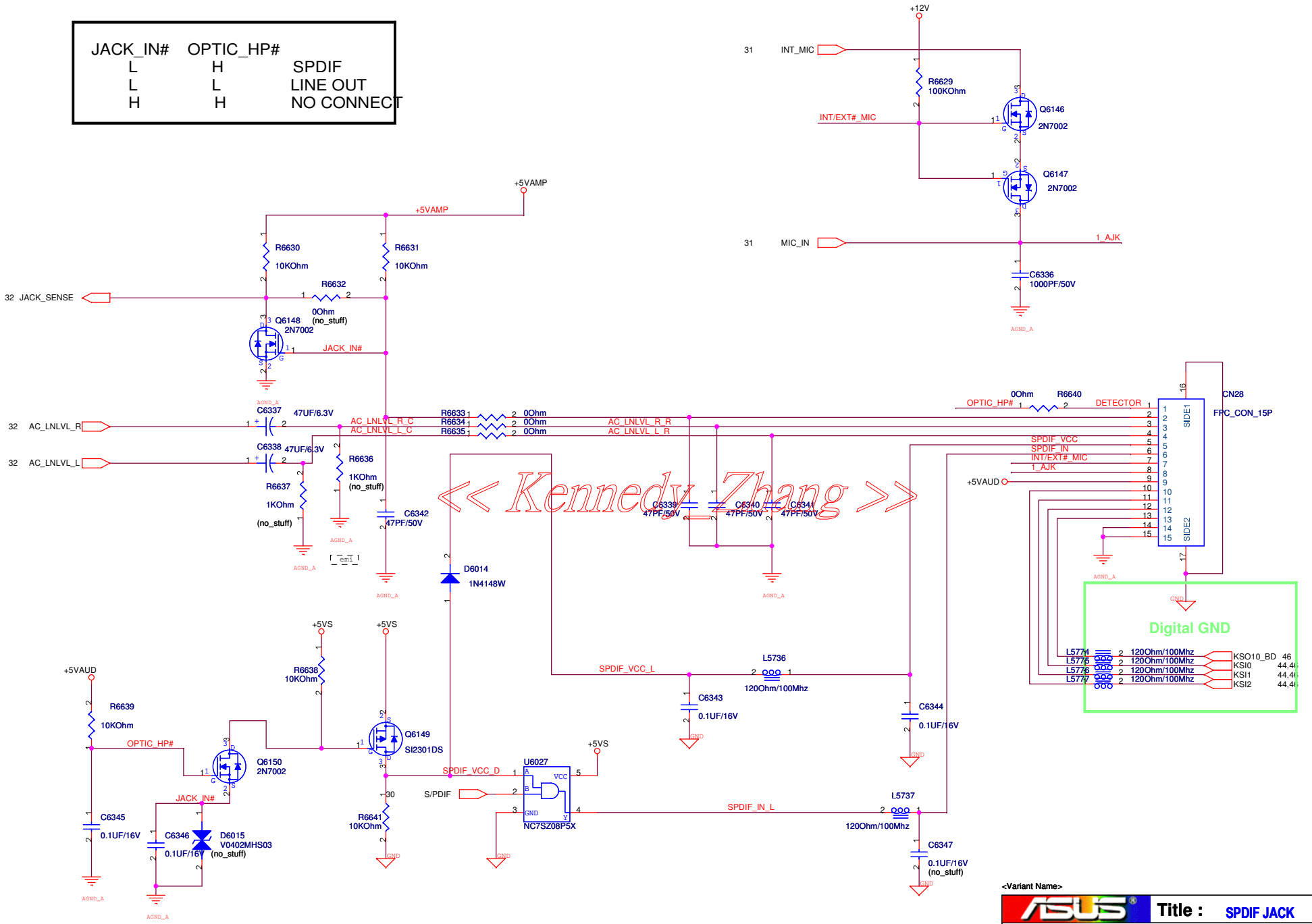
Title : AUDIO_AMP & INT SPK

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 32 of 64

JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

ASUSTeK COMPUTER INC

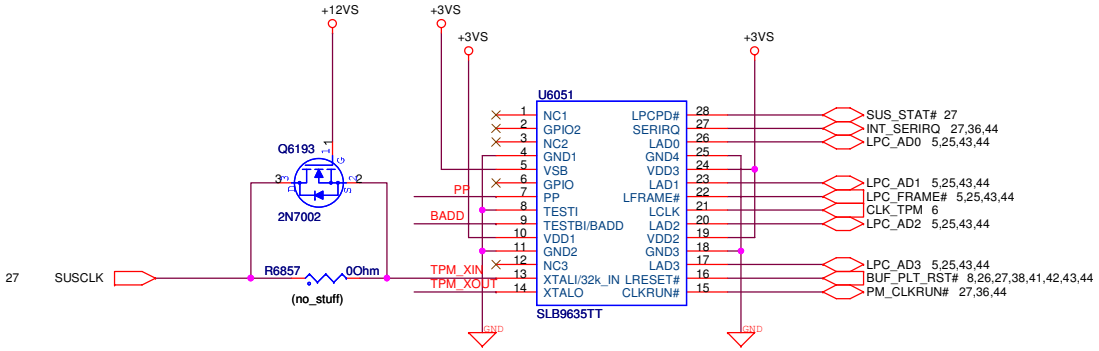
Title : SPDIF JACK

Engineer:

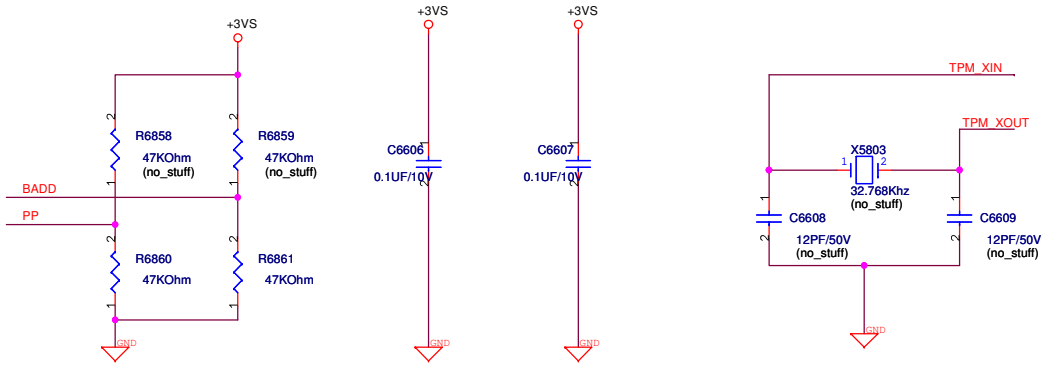
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 33 of 64

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.

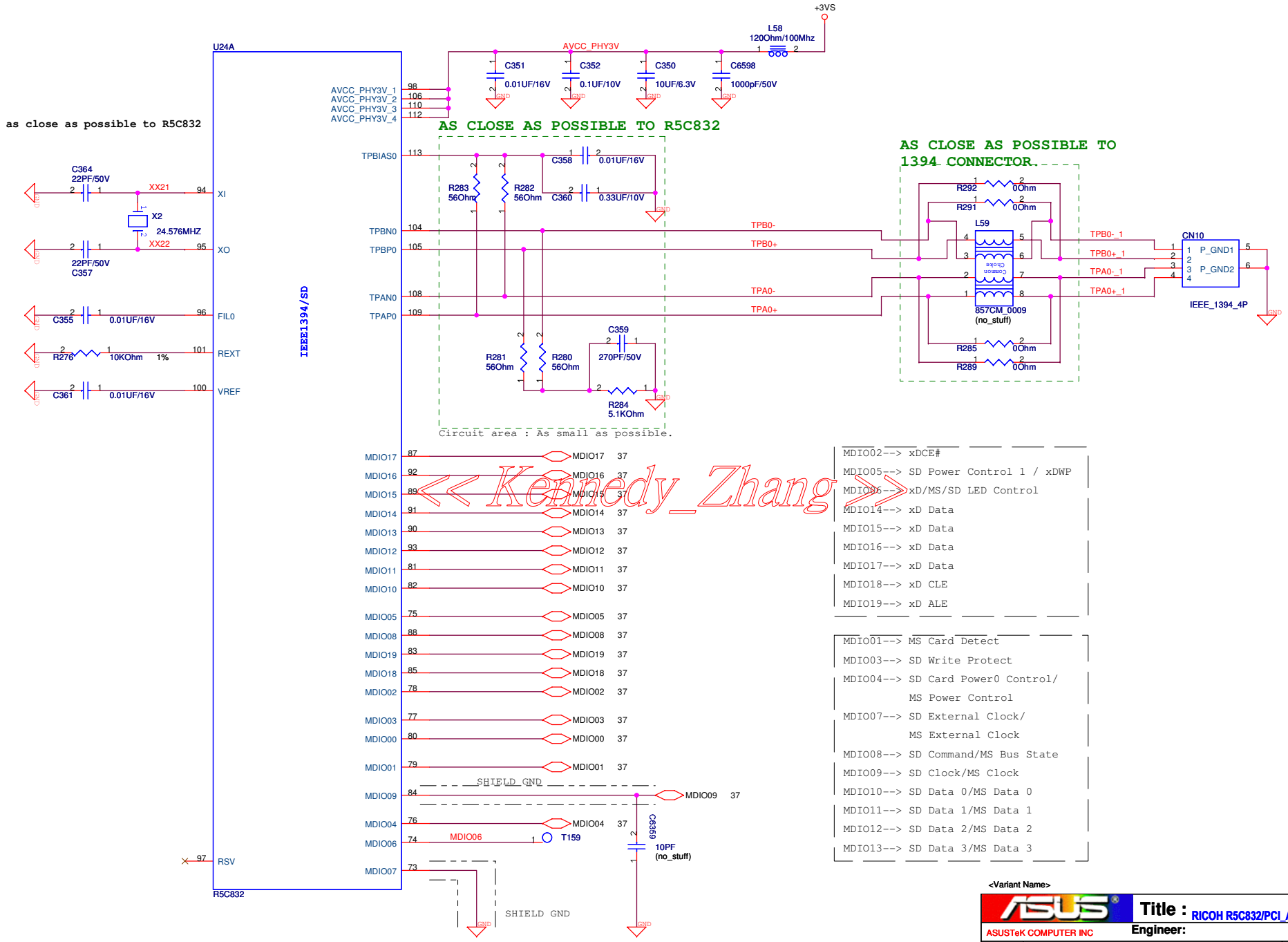


<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM 1.2	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 34 of 64	



<Variant Name>

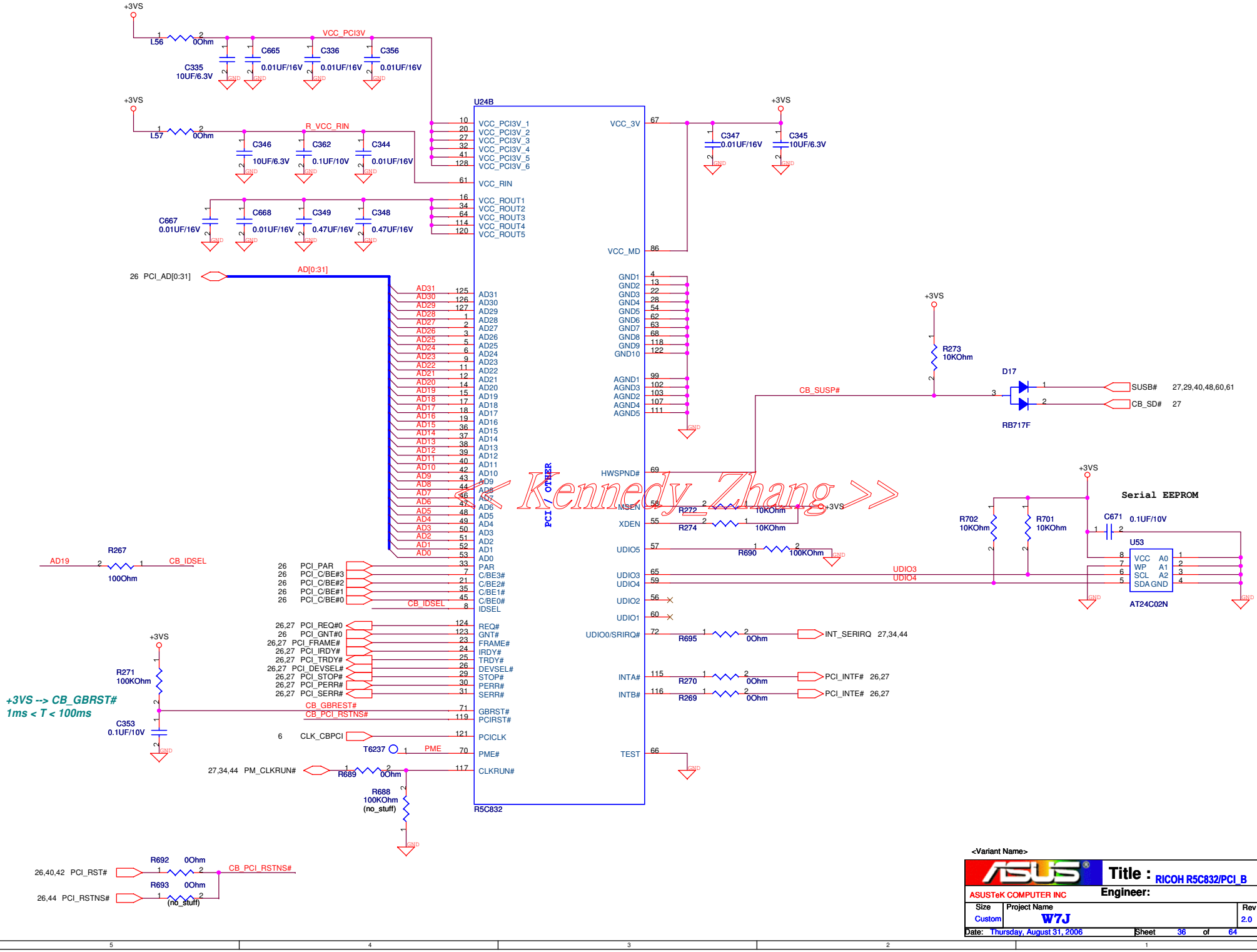
ASUSTeK COMPUTER INC

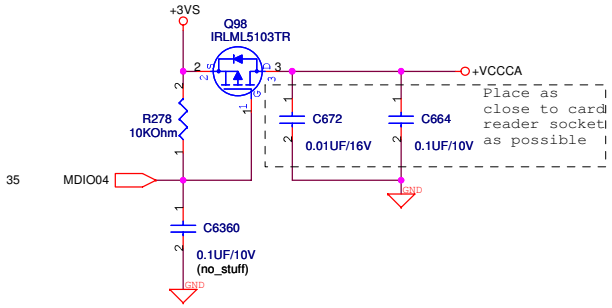
Title : RICOH R5C832/PCI_A

Engineer:

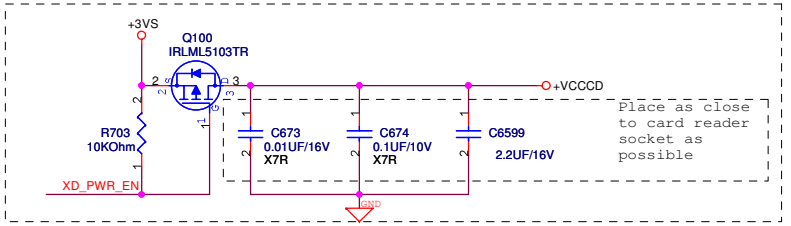
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 35 of 64

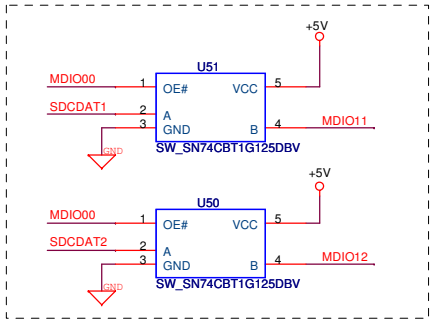




To correct the problem when MS Duo adaptor is in use.

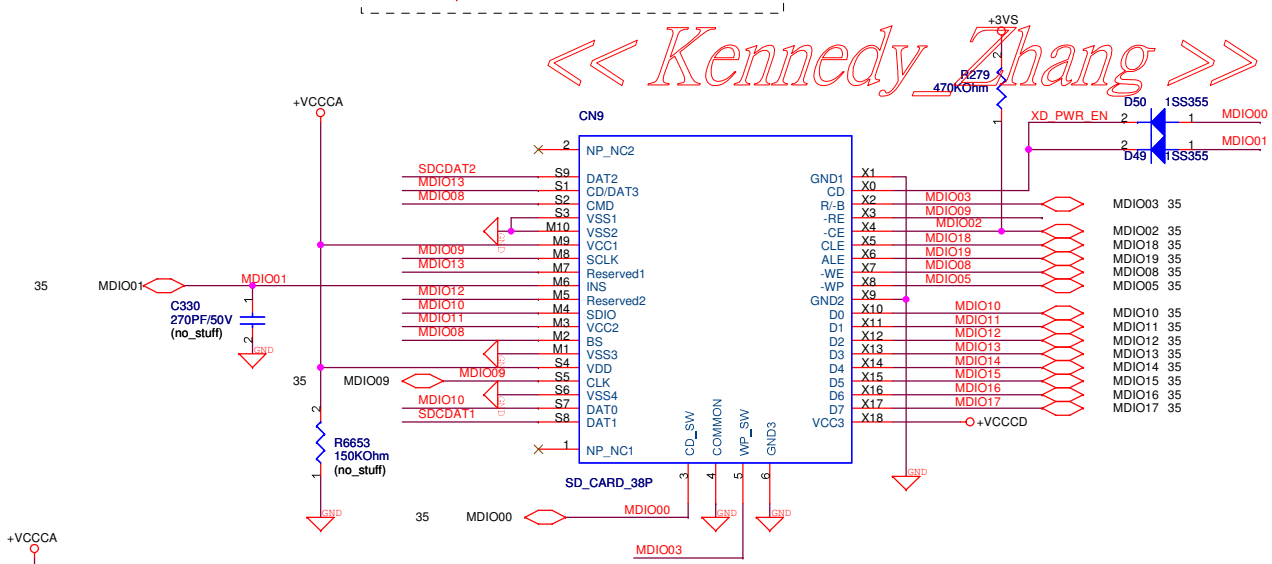


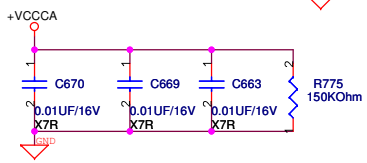
SD/MMC/MS/MS-PRO Card Reader Socket



MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

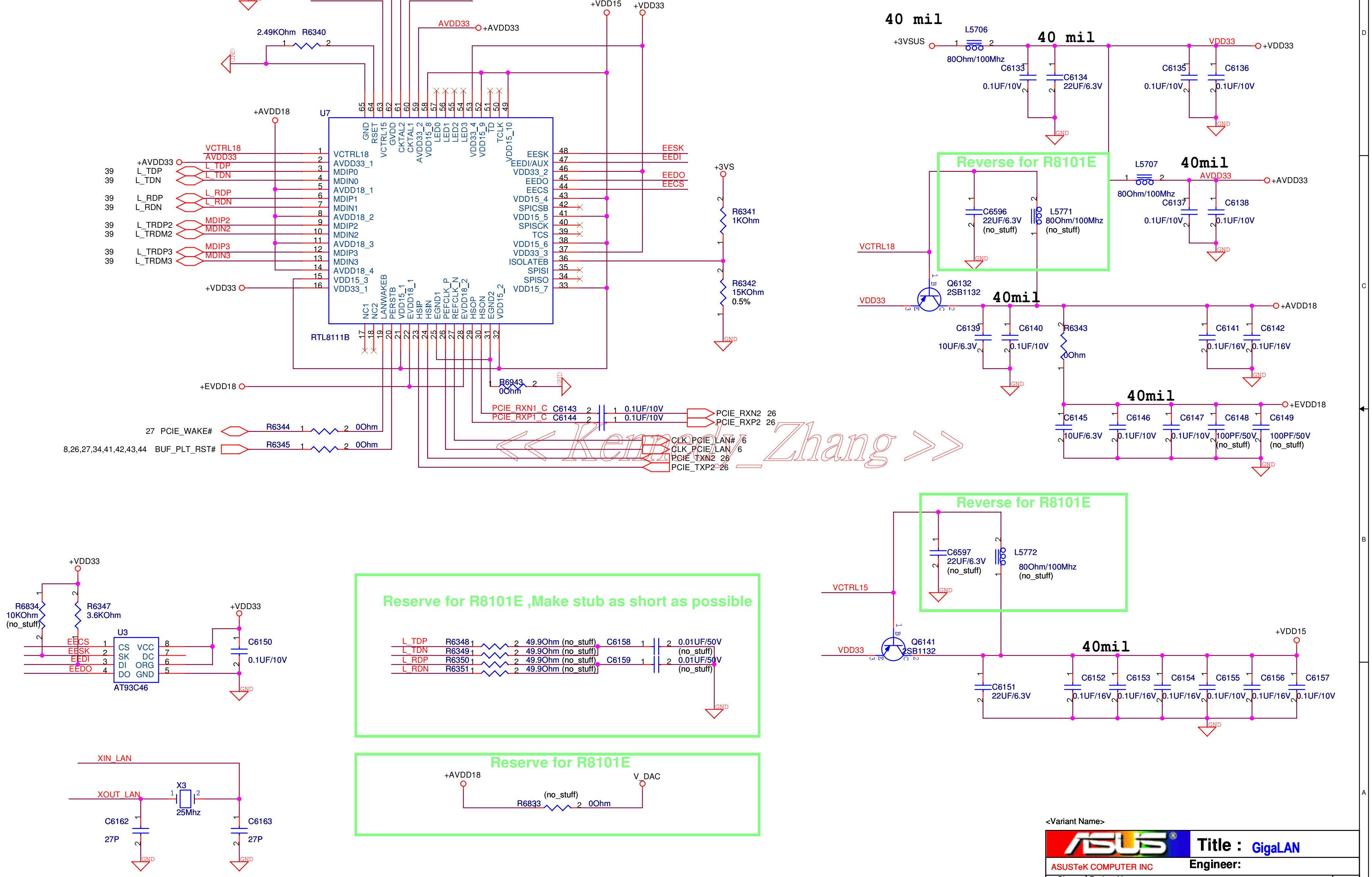




<Variant Name>

ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 37 of 64	

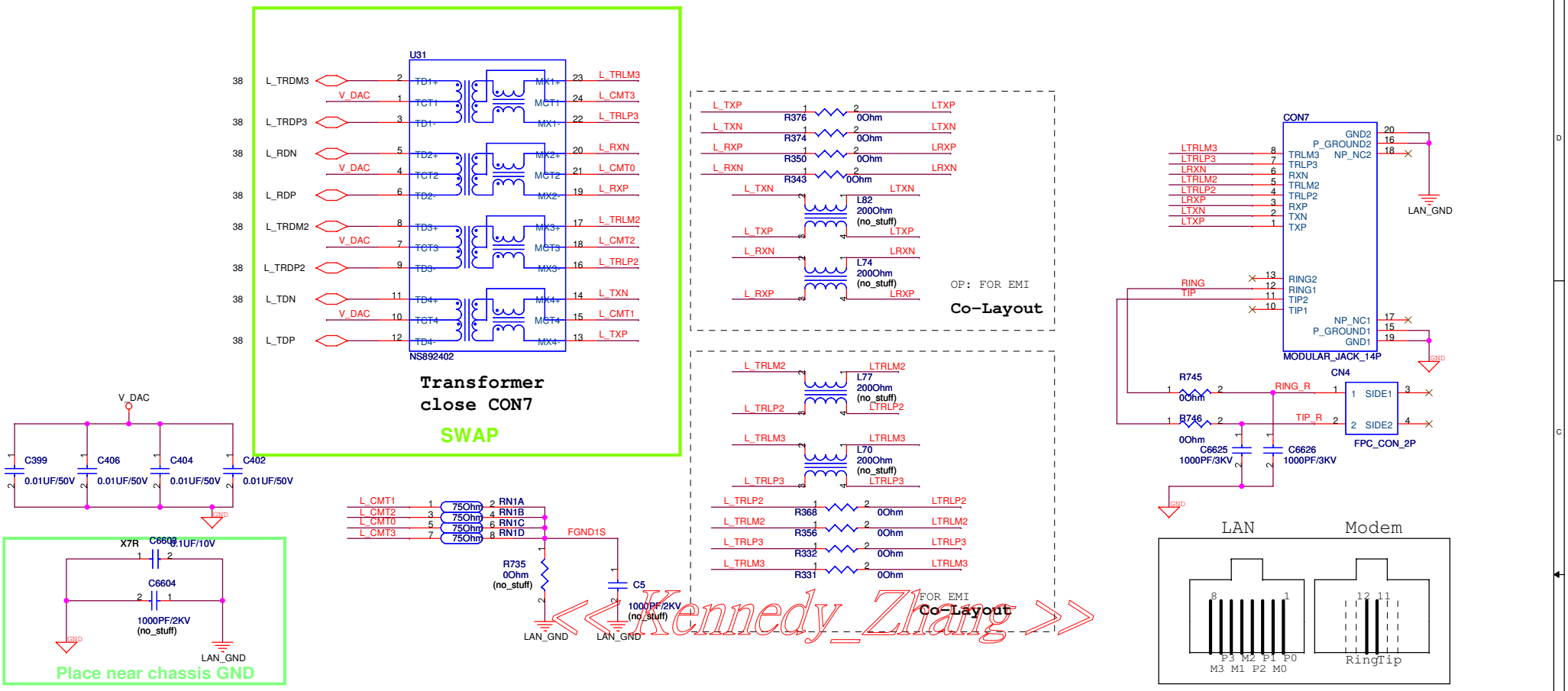
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



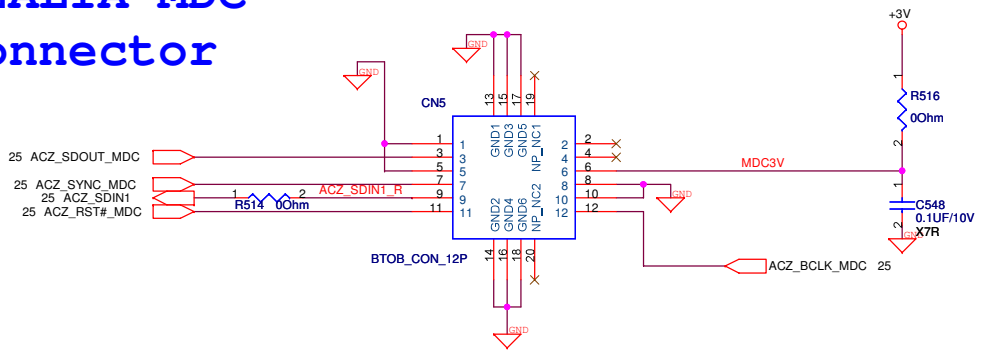
+GVDD15
C6600 1UF/10V
C6132 0.1UF/10V
VCTRL15
XIN_LAN
XOUT_LAN
AVDD33
+AVDD33
+VDD15
+VDD33
2.49KOhm R6340
U7
RTL8111B
+AVDD18
VCTRL18
L_TDP
L_TDN
L_RDP
L_RDN
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
MDIP2
MDIN2
MDIP3
MDIN3
VCTRL18
AVDD33_1
MDIP0
MDIN0
AVDD18_1
MDIP1
MDIN1
AVDD18_2
MDIP2
MDIN2
AVDD18_3
MDIP3
MDIN3
AVDD18_4
VDD15_3
VDD33_1
EESK
EEDI/AUX
VDD33_2
EEDO
EECS
VDD15_4
SPICSB
VDD15_5
SPISCK
TCS
VDD15_6
VDD33_3
ISOLATEB
SPISI
SPISO
VDD15_7
GND
RSET
VCTRL15
GVDD
CKTAL2
CKTAL1
AVDD33_2
VDD15_8
LED0
LED1
LED2
LED3
VDD33_4
VDD15_9
TD
TCLK
VDD15_10
NC1
NC2
LANWAKEB
PERSTB
VDD15_1
EVDD18_1
HSIP
HSIN
EGND1
REFCLK_P
REFCLK_N
EVDD18_2
HSOP
HSON
EGND2
VDD15_2
EESK
EEDI
EEDO
EECS
+3VS
R6341 1KOhm
R6342 15KOhm 0.5%
+EVDD18
R6943 0Ohm
PCIE_RXN1_C C6143 0.1UF/10V
PCIE_RXP1_C C6144 0.1UF/10V
PCIE_RXN2 26
PCIE_RXP2 26
27 PCIE_WAKE#
R6344 0Ohm
8,26,27,34,41,42,43,44 BUF_PLT_RST#
R6345 0Ohm
CLK_PCIE_LAN# 6
CLK_PCIE_LAN 6
PCIE_TXN2 26
PCIE_TXP2 26
40 mil
+3VSUS
L5706
80Ohm/100Mhz
40 mil
C6133 0.1UF/10V
C6134 22UF/6.3V
VDD33
C6135 0.1UF/10V
C6136 0.1UF/10V
Reverse for R8101E
C6596 22UF/6.3V (no_stuff)
L5771 80Ohm/100Mhz (no_stuff)
L5707
80Ohm/100Mhz
40mil
AVDD33
C6137 0.1UF/10V
C6138 0.1UF/10V
VCTRL18
Q6132 2SB1132
VDD33
40mil
+AVDD18
C6139 10UF/6.3V
C6140 0.1UF/10V
R6343 0Ohm
C6141 0.1UF/16V
C6142 0.1UF/16V
40mil
+EVDD18
C6145 10UF/6.3V
C6146 0.1UF/10V
C6147 0.1UF/10V
C6148 100PF/50V (no_stuff)
C6149 100PF/50V (no_stuff)
Reverse for R8101E
C6597 22UF/6.3V (no_stuff)
L5772 80Ohm/100Mhz (no_stuff)
VCTRL15
VDD33
Q6141 2SB1132
40mil
+VDD15
C6151 22UF/6.3V
C6152 0.1UF/16V
C6153 0.1UF/16V
C6154 0.1UF/16V
C6155 0.1UF/10V
C6156 0.1UF/16V
C6157 0.1UF/10V
+VDD33
R6834 10KOhm (no_stuff)
R6347 3.6KOhm
U3
CS SK DI DO
VCC DC ORG GND
AT93C46
C6150 0.1UF/10V
Reserve for R8101E ,Make stub as short as possible
L_TDP R6348 49.9Ohm (no_stuff) C6158 0.01UF/50V (no_stuff)
L_TDN R6349 49.9Ohm (no_stuff)
L_RDP R6350 49.9Ohm (no_stuff) C6159 0.01UF/50V (no_stuff)
L_RDN R6351 49.9Ohm (no_stuff)
XIN_LAN
XOUT_LAN
X3 25Mhz
C6162 27P
C6163 27P
Reserve for R8101E
+AVDD18
V_DAC
R6833 (no_stuff) 0Ohm
<< Kennedy_Zhang >>

<Variant Name>

ASUS	Title : GigaLAN		
ASUSTeK COMPUTER INC	Engineer:		
Size: Custom	Project Name: W7J		Rev: 2.0
Date: Thursday, August 31, 2006		Sheet 38 of 64	

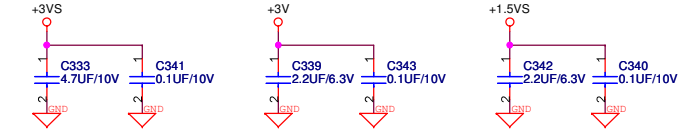


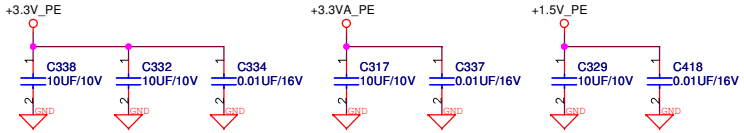
AZALIA MDC Connector

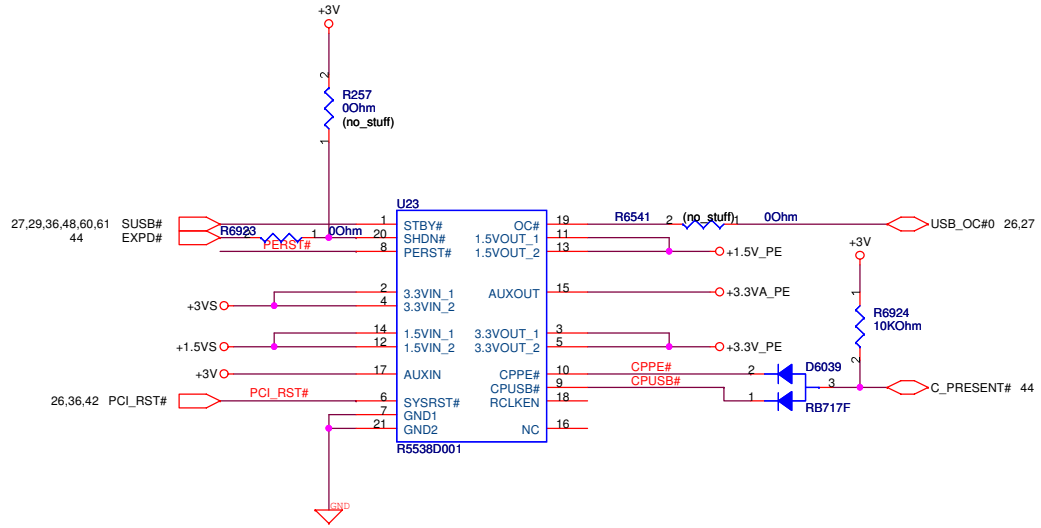


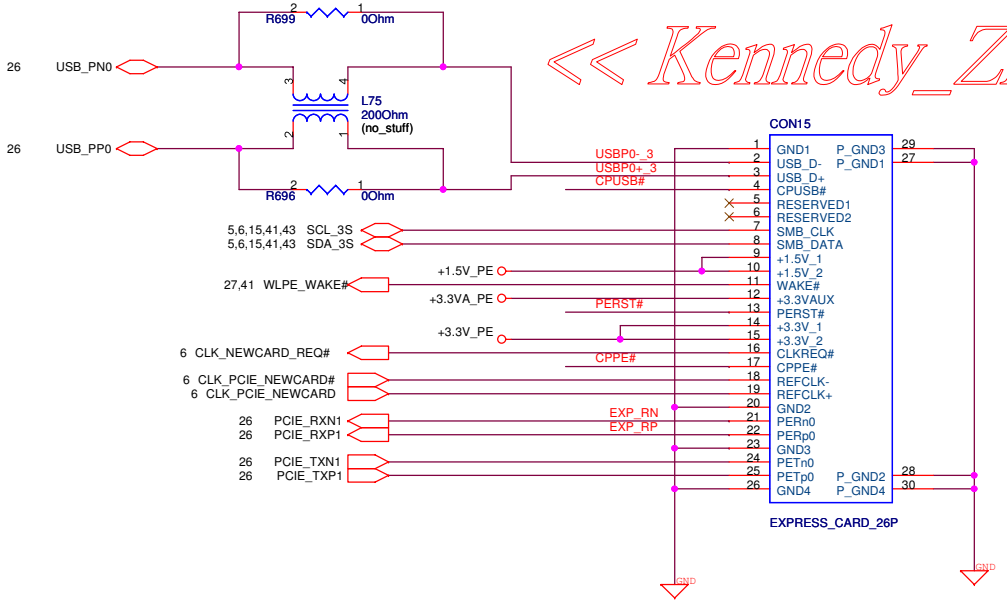
<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 39 of 64	









<Variant Name>

ASUSTeK COMPUTER INC

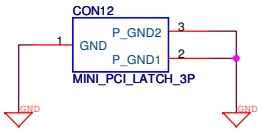
Title : Express Card

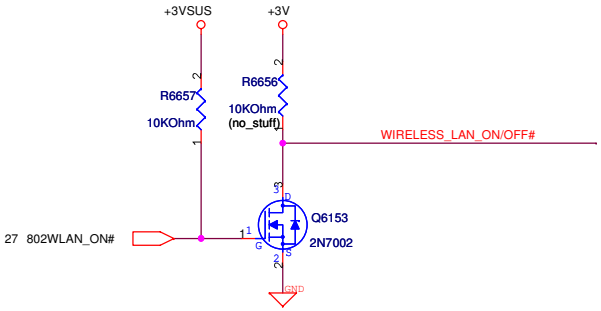
Engineer:

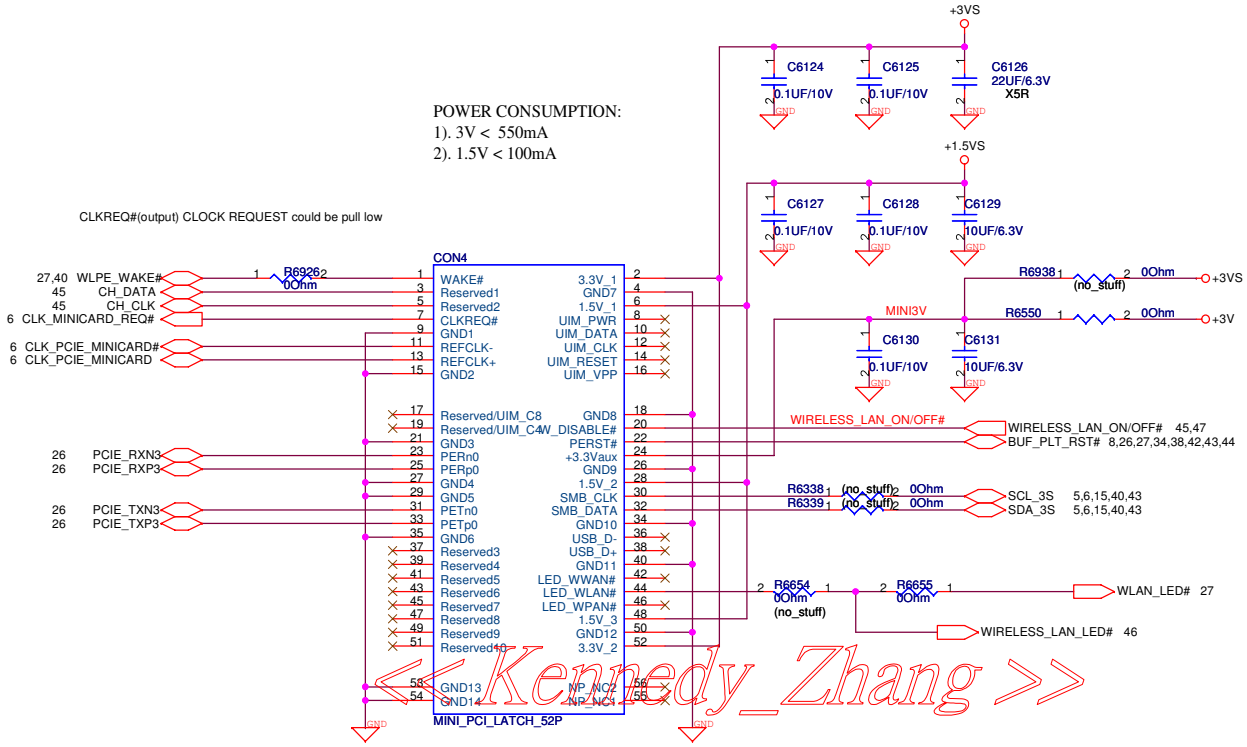
Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 40 of 64

Mini Card Latch

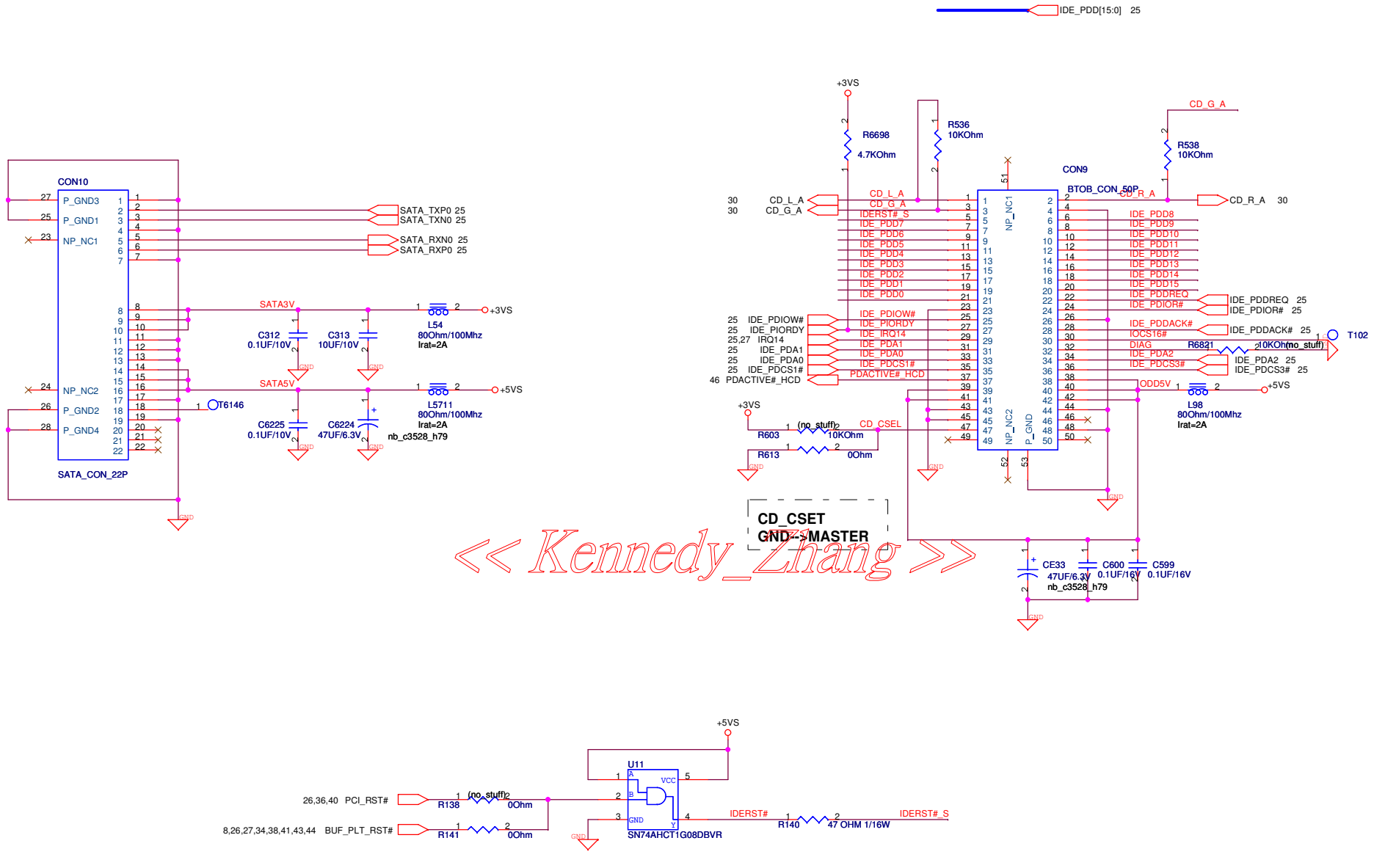


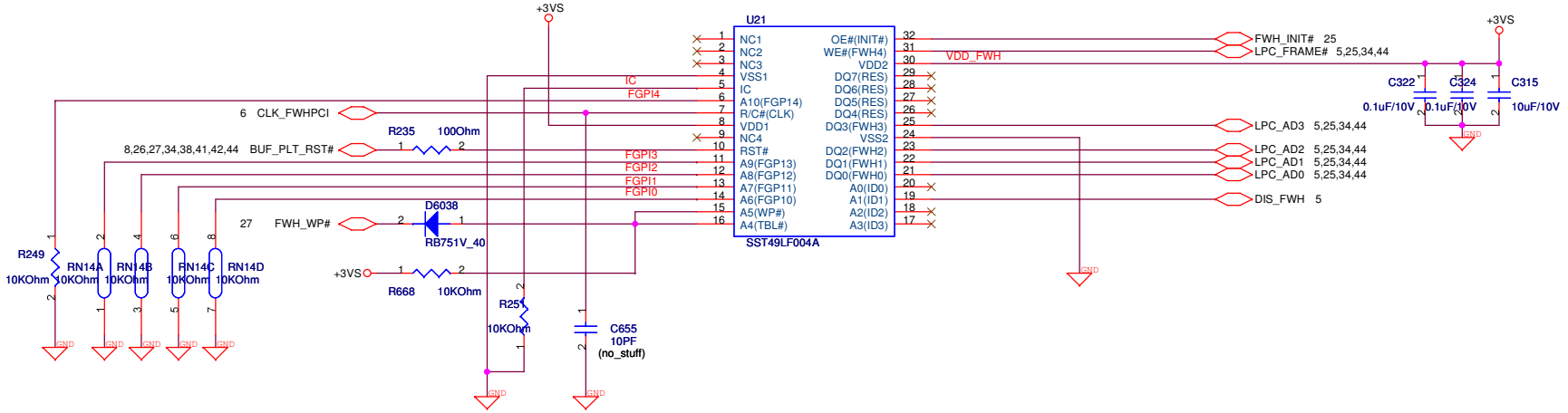




<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD (802.11)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 41 of 64	

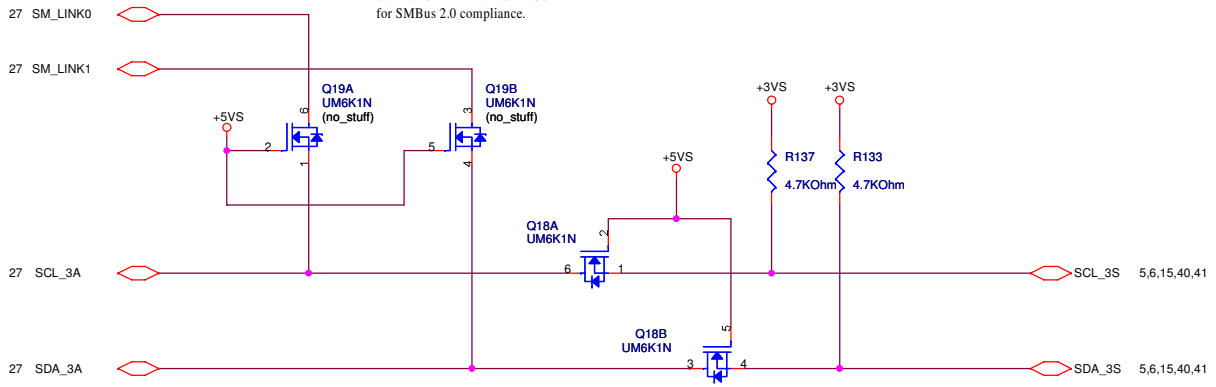




<< Kennedy_Zhang >>

ICH7-M

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



ICH7-M

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
EXPRESS CARD
MINI-CARD

<Variant Name>

ASUSTeK COMPUTER INC	Title : FWH , SM BUS	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 43 of 64	

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

KID1	KID0	Matrix
0	0	US
1	1	UK
0	1	JP

<variant_name>

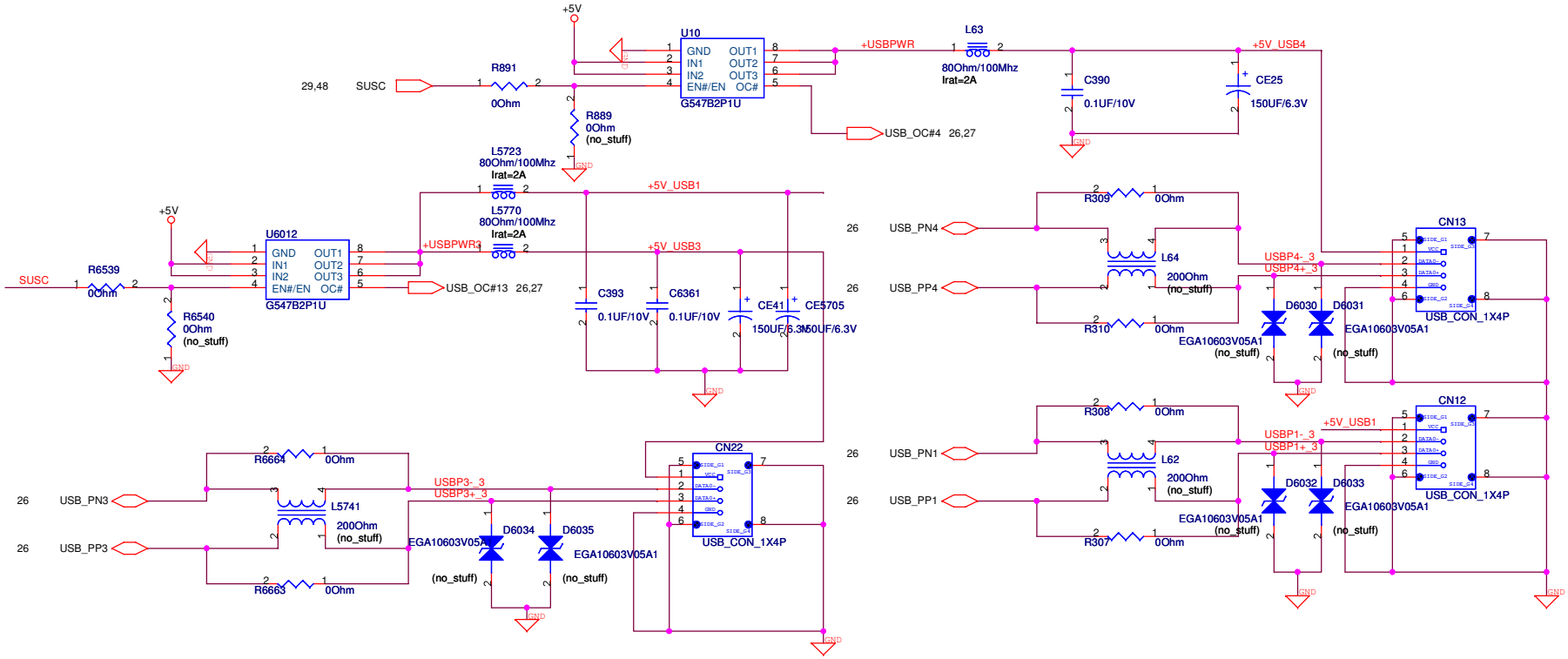
ASUSTeK COMPUTER INC

Title : KBC M38857

Engineer:

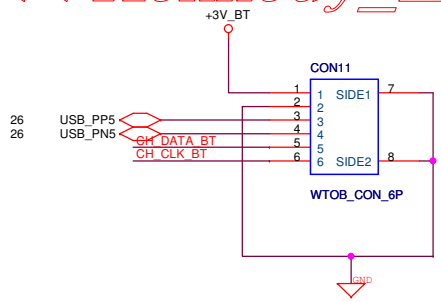
Size	Project Name	Rev
Custom	W7J	2.0

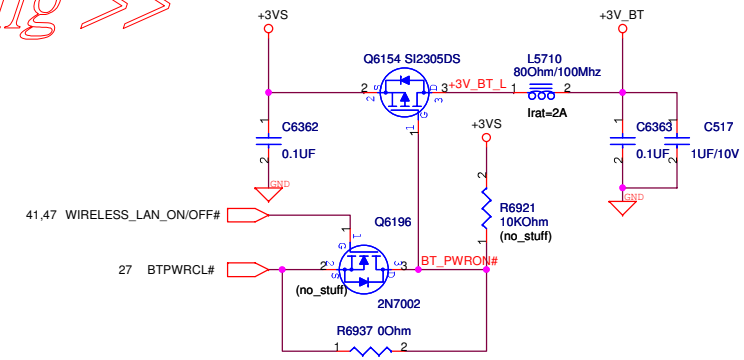
Date: Thursday, August 31, 2006 Sheet 44 of 64

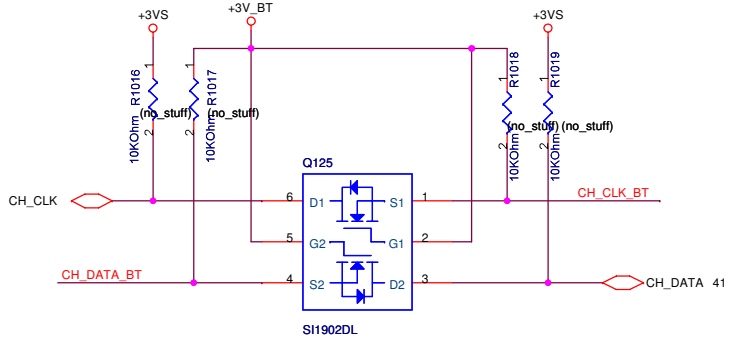


Bluetooth Module
Connector

<< Kennedy_Zhang >>







<Variant Name>

ASUSTeK COMPUTER INC

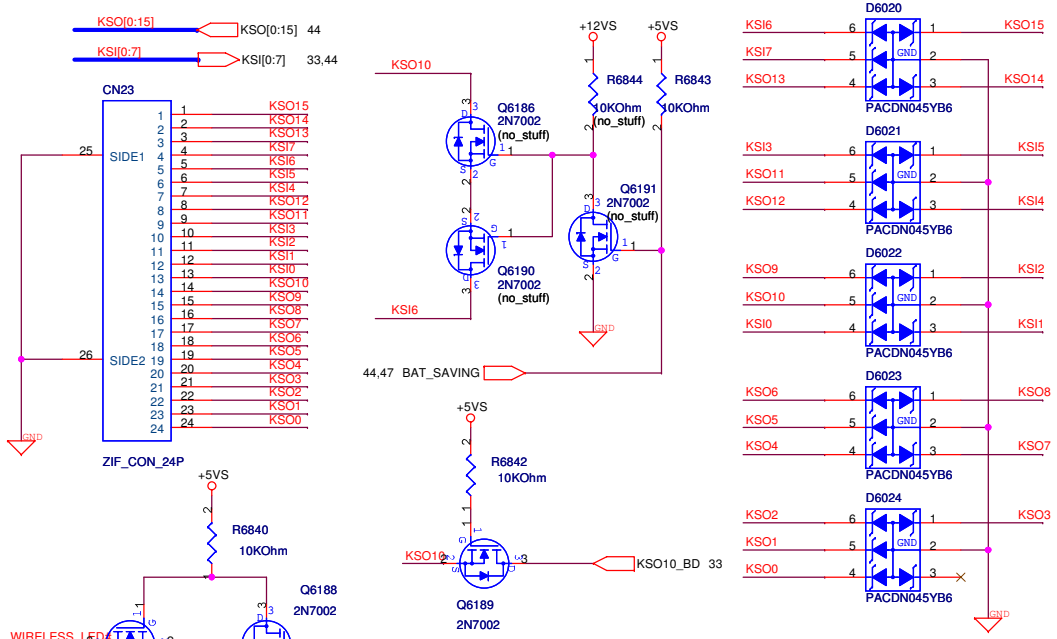
Title : USB * 3ports & BT

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

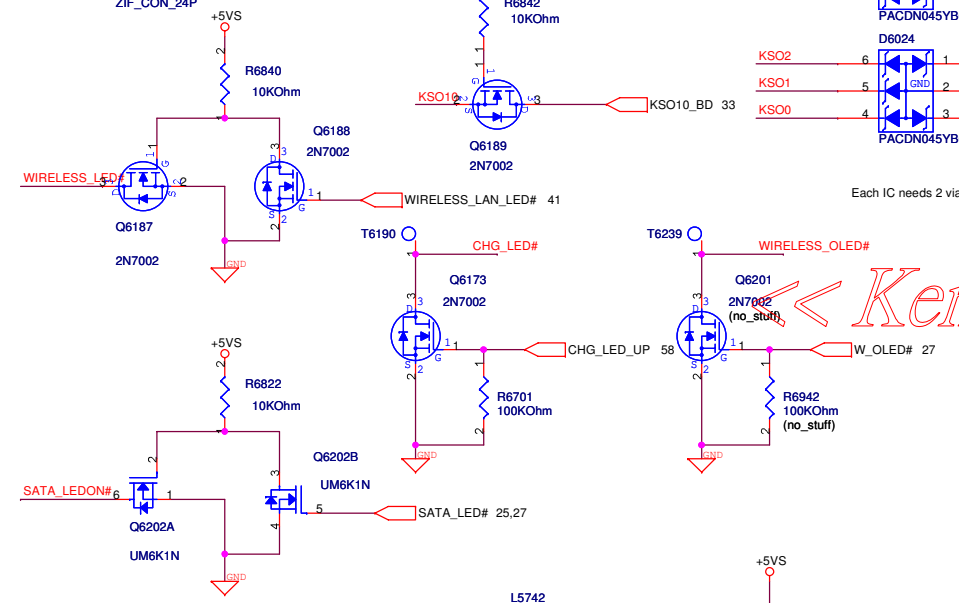
Date: Thursday, August 31, 2006 Sheet 45 of 64

Internal Keyboard Connector

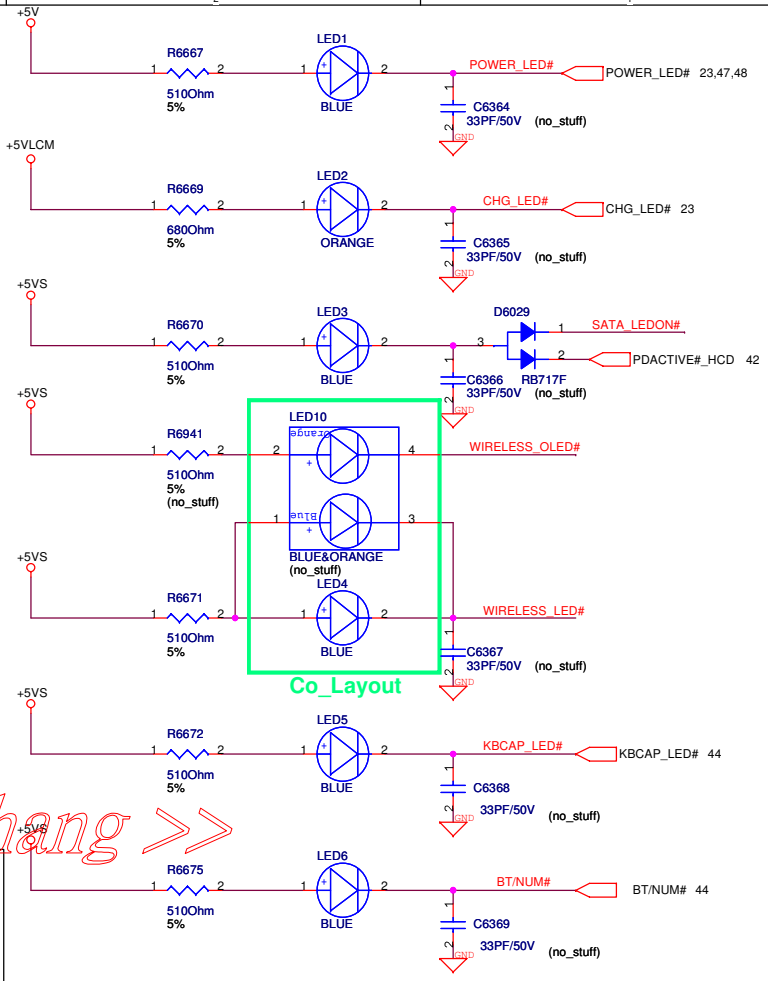


EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.

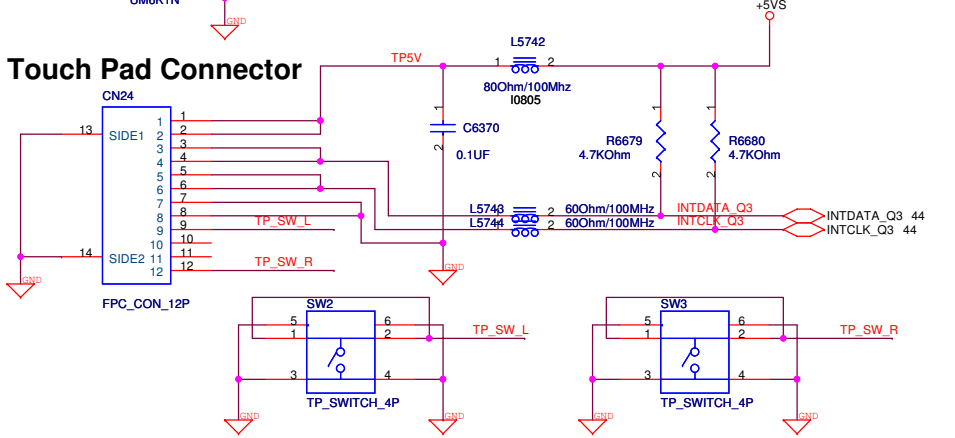
Each IC needs 2 vias to ground.



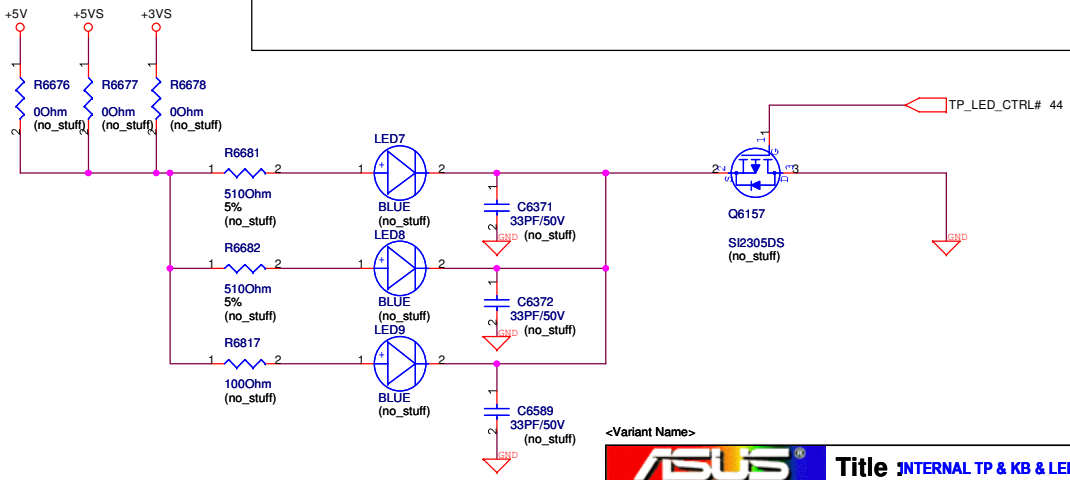
LEDs



Touch Pad Connector



Touch Pad LED

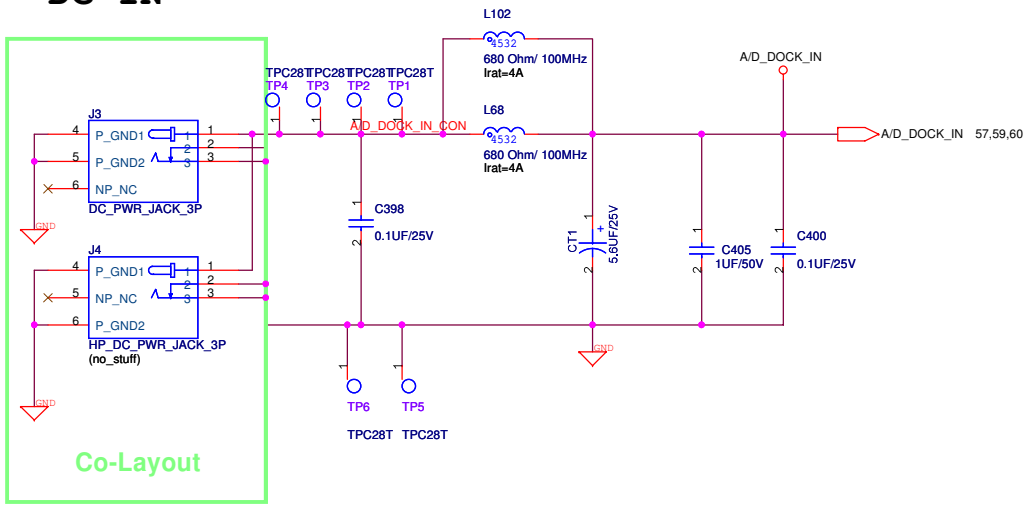


<Variant Name>

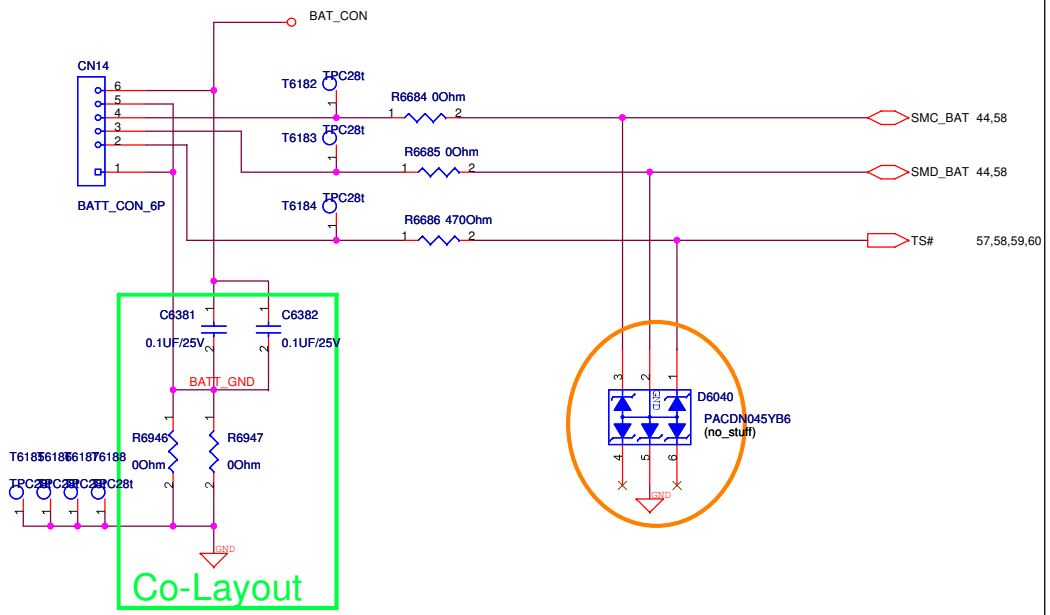
ASUSTeK COMPUTER INC	Title : INTERNAL TP & KB & LEDs	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 46 of 64	

EXT BOARD

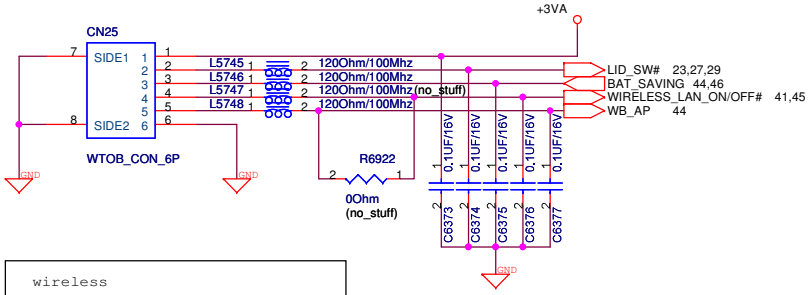
DC-IN



Battery Connector



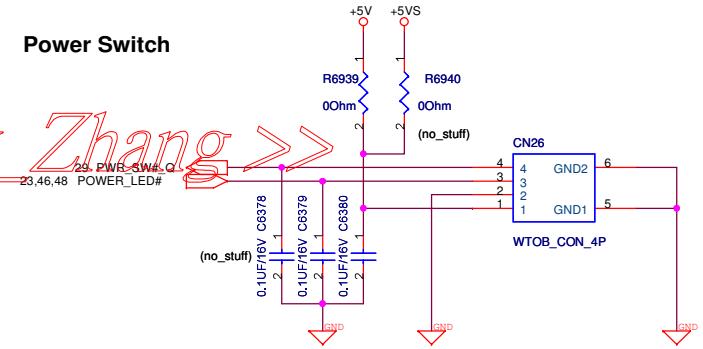
LID_SW_BD CN



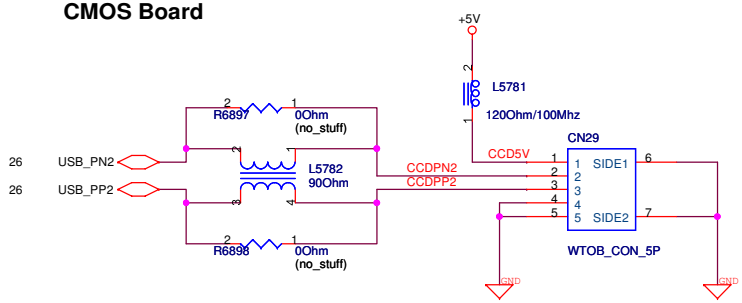

```
wireless
------------------------------
right on ---> active high
left off ---> active low


WB_AP
------------------------------
right off ---> active high
left  on  ---> active low
```

Power Switch



CMOS Board



<Variant Name>

ASUSTeK COMPUTER INC

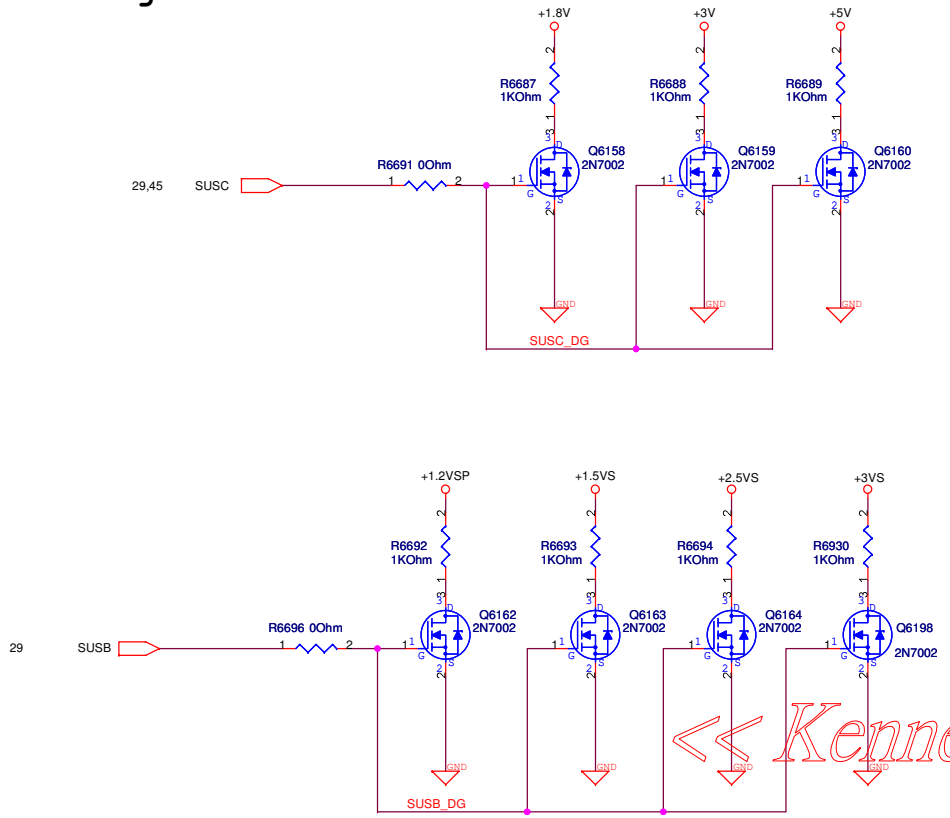
Title : DCIN,BATT CON,EXT BOARD

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 47 of 64

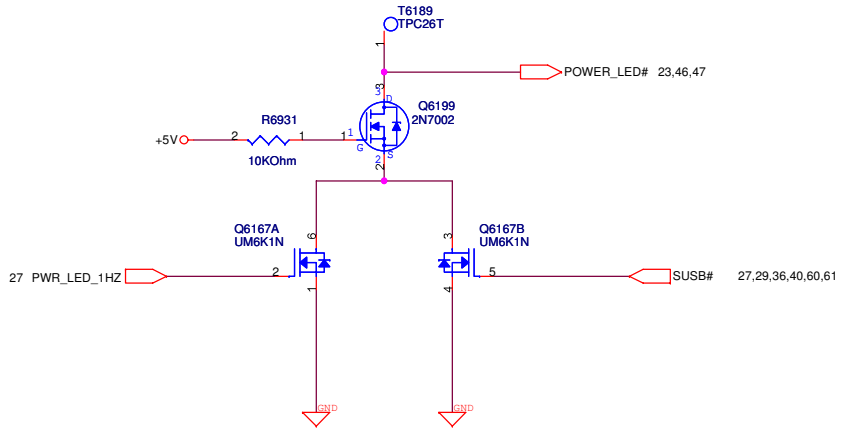
Discharge



Poewr List

+3VA	+3VA	25,29,47,54,63
+3VSUS	+3VSUS	26,27,28,29,32,38,41,51
+5VA	+5VA	51,54,60
+5VSUS	+5VSUS	28,51,60
+3V	+3V	26,29,39,40,41,44,54,61
+5V	+5V	16,30,32,37,44,45,46,47,59,61
+12V	+12V	27,32,33,61
+3VS	+3VS	5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,50,52,60,61
+5VS	+5VS	5,24,28,29,30,32,33,42,43,44,46,47,50,61
+12VS	+12VS	5,24,34,46,61
+VCORE	+VCORE	3,4,5,44,50
+VCCP	+VCCP	2,3,4,6,7,8,10,11,12,25,28,52
+1.2VSP	+1.2VSP	17,18,56
+2.5VS	+2.5VS	10,20,21,54
+1.8VS	+1.8VS	20,61
+0.9VS	+0.9VS	16,53
+1.5VS	+1.5VS	3,8,10,11,26,28,40,41,52
+VCC_RTC	+VCC_RTC	25,28
+1.8V	+1.8V	8,12,13,14,15,16,53
VTT_REF	VTT_REF	8,13,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	47,57,59,60
+VGA_VCORE	+VGA_VCORE	17,55

Power LED On



<Variant Name>

Discharge,Power Rail & Power LED On

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

Date: Thursday, August 31, 2006 Sheet 48 of 64

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARD READER	AD19	0	E
1394	AD19	0	F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor	0101110x (2E)
PIC	1001001x (92)
Express Card	TBD
Mini Card	TBD

ICH7-M GPIO	W7J
GPIO 0	PM_BMBUSY#
GPIO 1	PCI_REQ#5
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 6	BACK_OFF#
GPIO 7	MUTE_POP_ICHGPIO#
GPIO 8	EXTSMI#
GPIO 9	W_OLED#
GPIO 10	(PWRLMT#)
GPIO 11	SMBALERT#
GPIO 12	KBC_SCI#
GPIO 13	PWR_LED_1HZ
GPIO 14	WLAN_ON#
GPIO 15	802_LED_EN#
GPIO 16	DPRSLPVR
GPIO 17	GNT5#
GPIO 18	STP_PCI#
GPIO 19	Memoryclk
GPIO 20	STP_CPU#
GPIO 21	
GPIO 22	PCI_REQ#4
GPIO 23	LPC_DRQ#1
GPIO 24	SW_RST#
GPIO 25	CB_SD#
GPIO 26	MEM ID0
GPIO 27	MEM ID1
GPIO 28	MEM ID2
GPIO 29	USB_OC#5
GPIO 30	USB_OC#6
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 33	BT_ON#
GPIO 34	FWH_WP#
GPIO 35	SATACLKREQ#
GPIO 36	BT_LED_EN#
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 48	GNT4#
GPIO 49	CPUPWRGD

KBC GPIO	W7J
P23	
P22	BAT_LEARN
P21	
P20	KBCRSM
P42	WATCHDOG
P43	
P44	xKBRC
P45	GA20
P46	KBDSCI
P47	CLKRUN#
P50	BAT_LLOW#
P51	TP_LED_CTRL#
P52	
P53	EXPD#
P54	LID_EC#
P55	BAT_IN#
P56	CPU_FAN_PWM
P57	ADJ_BL
P67	WB_AP
P66	M_MODE#
P65	
P64	ACIN#
P63	EOC#_LED
P62	C_PRESENT#
P61	ACZ_RST#_AUD
P60	
P75	KBDCLK_5S
P74	MOUSECLK_5S
P73	INTCLK_Q3
P72	KBDDATA_5S
P71	MOUSEDATA_5S
P70	INTDATA_Q3
P77	SMC_KBC
P76	SMD_KBC
P27	SCROLL_LED#
P26	NUM_LED#
P25	CAP_LED#
P24	SET_RSTNS#
P40	EXT_SMI#
P41	

<Variant Name>

ASUSTeK COMPUTER INC

Title : System Resource

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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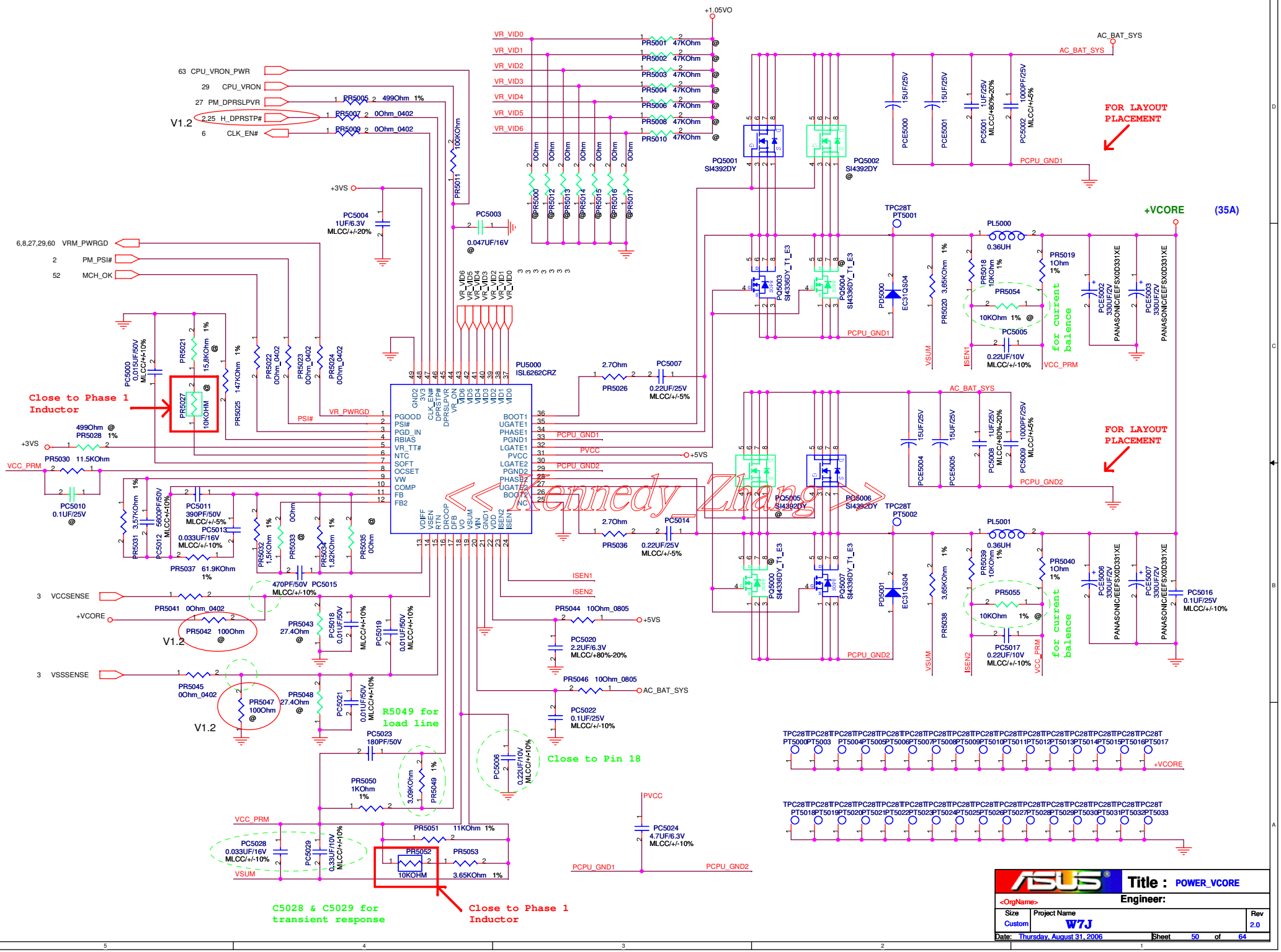
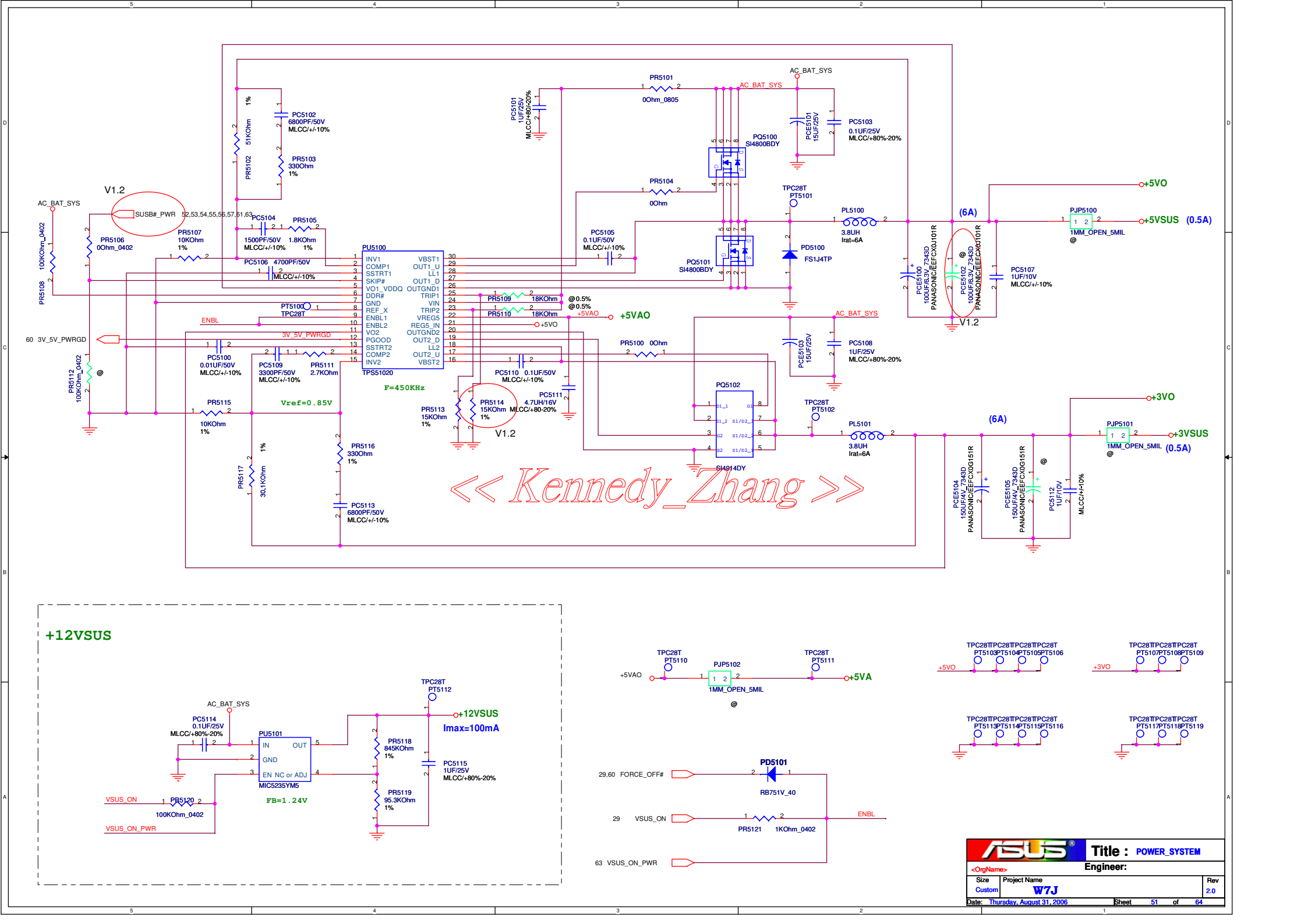
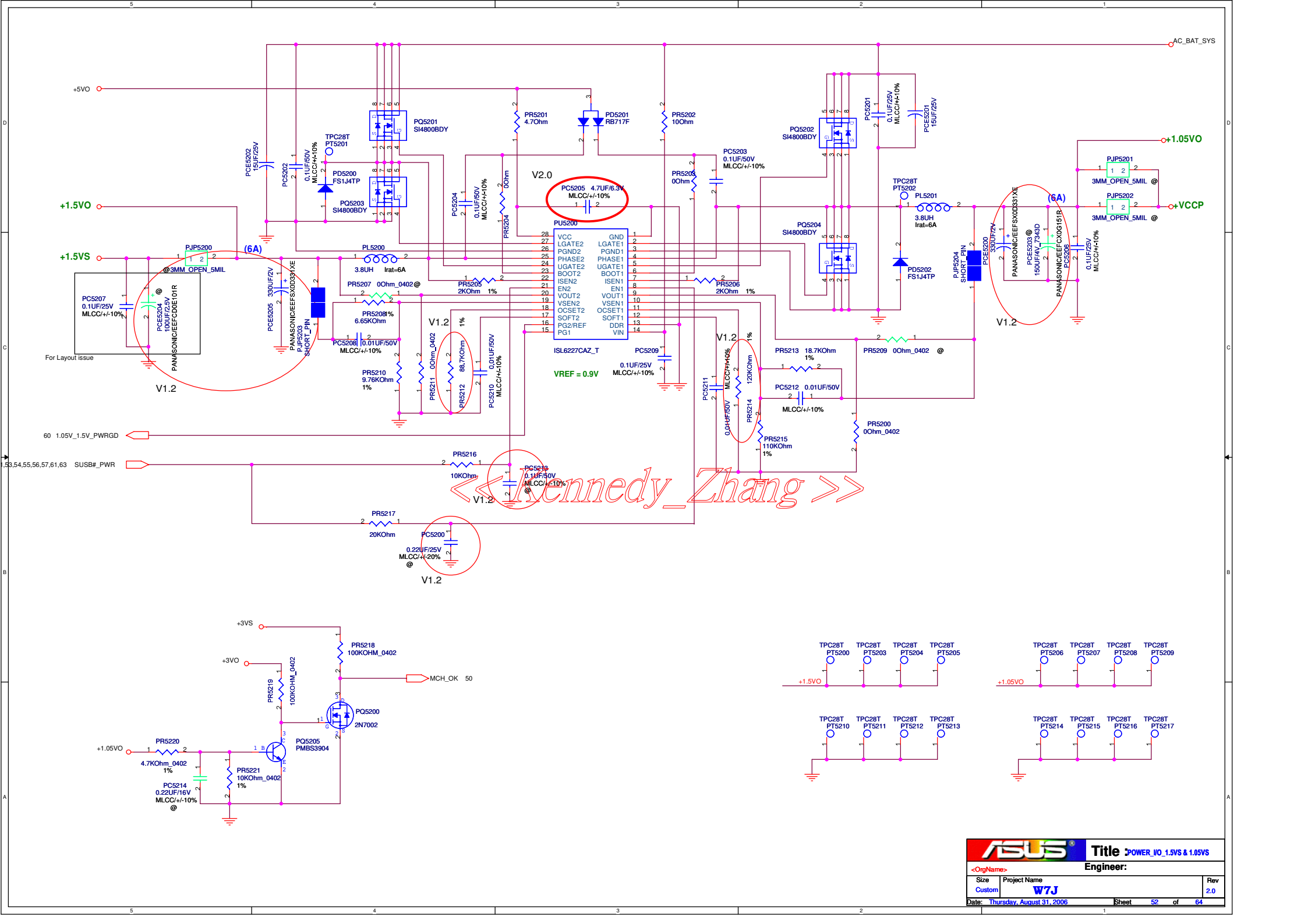
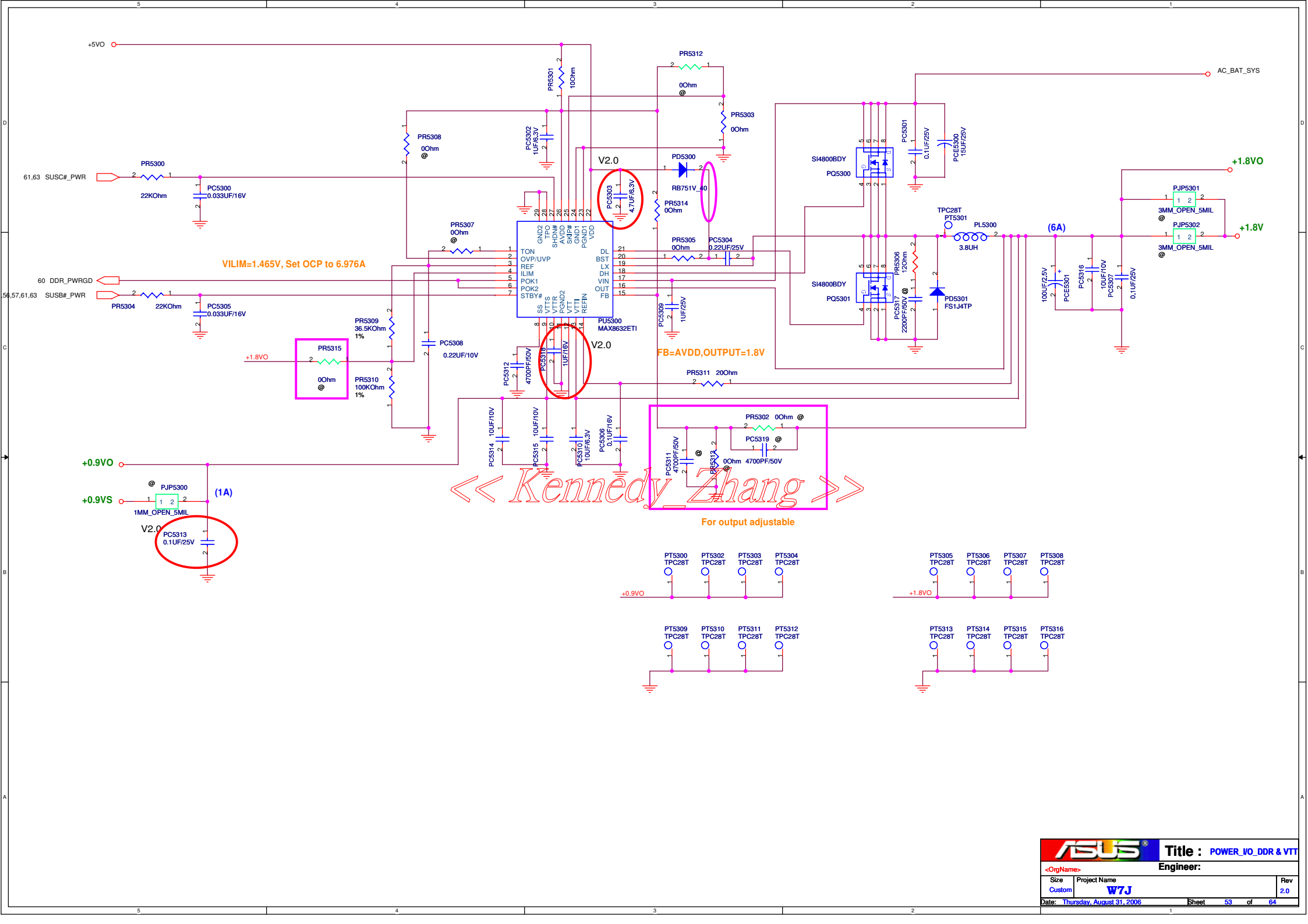

+1.05VO
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
PR5001 47KOhm
PR5002 47KOhm
PR5003 47KOhm
PR5004 47KOhm
PR5006 47KOhm
PR5008 47KOhm
PR5010 47KOhm
AC_BAT_SYS
FOR LAYOUT PLACEMENT
PCPU_GND1
PQ5001 SI4392DY
PQ5002 SI4392DY
PCE5000 15UF/25V
PCE5001 15UF/25V
PC5001 1UF/25V MLCC/+80%-20%
PC5002 1000PF/25V MLCC/+/-5%
+VCORE (35A)
TPC28T PT5001
PL5000 0.36UH
PR5019 1Ohm 1%
PR5018 10KOhm 1%
PR5054 10KOhm 1% @
PC5005 0.22UF/10V MLCC/+/-10%
for current balence
PCE5002 330UF/2V PANASONIC/EEFSXOD331XE
PCE5003 330UF/2V PANASONIC/EEFSXOD331XE
PD5000 EC31QS04
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PR5020 3.65KOhm 1%
VSUM
ISEN1
VCC_PRM
PU5000 ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
GND2
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
GND1
VDD
ISEN2
ISEN
PR5026 2.7Ohm
PC5007 0.22UF/25V MLCC/+/-5%
PR5036 2.7Ohm
PC5014 0.22UF/25V MLCC/+/-5%
PQ5005 SI4392DY
PQ5006 SI4392DY
PT5002
PL5001 0.36UH
PR5040 1Ohm 1%
PR5039 10KOhm 1%
PR5055 10KOhm 1% @
PC5017 0.22UF/10V MLCC/+/-10%
PC5016 0.1UF/25V MLCC/+/-10%
PD5001 EC31QS04
PQ5007 SI4336DY_T1_E3
PQ5008 SI4336DY_T1_E3
PR5038 3.65KOhm 1%
PCE5004 15UF/25V
PCE5005 15UF/25V
PC5008 1UF/25V MLCC/+80%-20%
PC5009 1000PF/25V MLCC/+/-5%
PCE5006 330UF/2V PANASONIC/EEFSXOD331XE
PCE5007 330UF/2V PANASONIC/EEFSXOD331XE
63 CPU_VRON_PWR
29 CPU_VRON
27 PM_DPRSLPVR
2,25 H_DPRSTP#
6 CLK_EN#
V1.2
PR5005 499Ohm 1%
PR5007 0Ohm_0402
PR5009 0Ohm_0402
PR5011 100KOhm
+3VS
PC5004 1UF/6.3V MLCC/+/-20%
PC5003 0.047UF/16V @
PR5000 0Ohm
PR5012 0Ohm
PR5013 0Ohm
PR5014 0Ohm
PR5015 0Ohm
PR5016 0Ohm
PR5017 0Ohm
6,8,27,29,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
PC5000 0.015UF/50V MLCC/+/-10%
PR5021 15.8KOhm 1%
PR5027 10KOHM 1%
PR5022 0Ohm_0402
PR5023 0Ohm_0402
PR5024 0Ohm_0402
PR5025 147KOhm 1%
PSI#
VR_PWRGD
Close to Phase 1 Inductor
499Ohm @ PR5028 1%
PR5030 11.5KOhm
PC5010 0.1UF/25V @
PR5031 3.57KOhm 1%
PC5012 560PF/50V MLCC/+/-10%
PC5011 390PF/50V MLCC/+/-5%
PC5013 0.033UF/16V MLCC/+/-10%
PR5037 61.9KOhm 1%
PR5032 1.5KOhm 1%
PR5033 0Ohm @
PR5034 1.82KOhm 1%
PR5035 0Ohm @
470PF/50V PC5015 MLCC/+/-10%
3 VCCSENSE
+VCORE
PR5041 0Ohm_0402
PR5042 100Ohm @
PR5043 27.4Ohm @
PC5018 0.01UF/50V MLCC/+/-10%
PC5019 0.01UF/50V MLCC/+/-10%
3 VSSSENSE
PR5045 0Ohm_0402
PR5047 100Ohm @
PR5048 27.4Ohm @
PC5021 0.01UF/50V MLCC/+/-10%
R5049 for load line
PC5023 180PF/50V
PR5050 1KOhm 1%
PR5049 3.09KOhm 1%
PC5006 0.22UF/10V MLCC/+/-10%
Close to Pin 18
ISEN1
ISEN2
PR5044 10Ohm_0805
PC5020 2.2UF/6.3V MLCC/+80%-20%
PR5046 10Ohm_0805
PC5022 0.1UF/25V MLCC/+/-10%
PVCC
PC5024 4.7UF/6.3V MLCC/+/-10%
PCPU_GND1
PCPU_GND2
VCC_PRM
PC5028 0.033UF/16V MLCC/+/-10%
PC5029 0.33UF/10V MLCC/+/-10%
VSUM
PR5051 11KOhm 1%
PR5052 10KOHM
PR5053 3.65KOhm 1%
C5028 & C5029 for transient response
Close to Phase 1 Inductor
TPC28T PT5000 PT5003 PT5004 PT5005 PT5006 PT5007 PT5008 PT5009 PT5010 PT5011 PT5012 PT5013 PT5014 PT5015 PT5016 PT5017
+VCORE
TPC28T PT5018 PT5019 PT5020 PT5021 PT5022 PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 PT5033
Kennedy Zhang
Title : POWER_VCORE
Engineer:
<OrgName>
Size Custom
Project Name W7J
Rev 2.0
Date: Thursday, August 31, 2006
Sheet 50 of 64



ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 51 of 64	



ASUS	Title : POWER_I/O_1.5VS & 1.05VS	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 52 of 64	



ASUS

Title : POWER_I/O_DDR & VTT

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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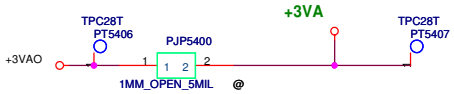
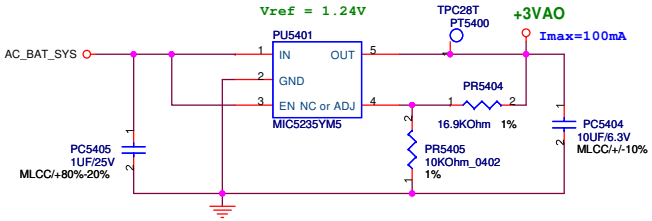
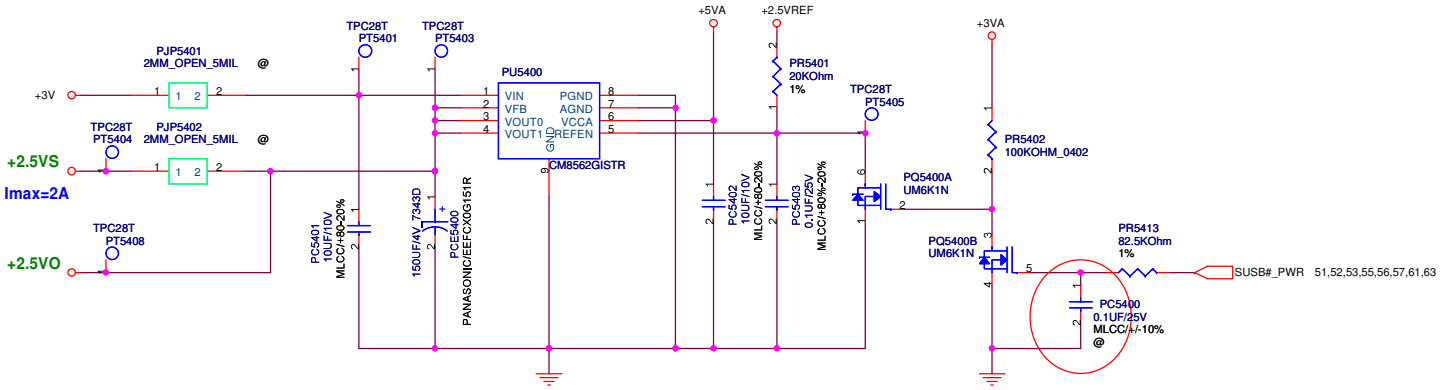
+3VAO

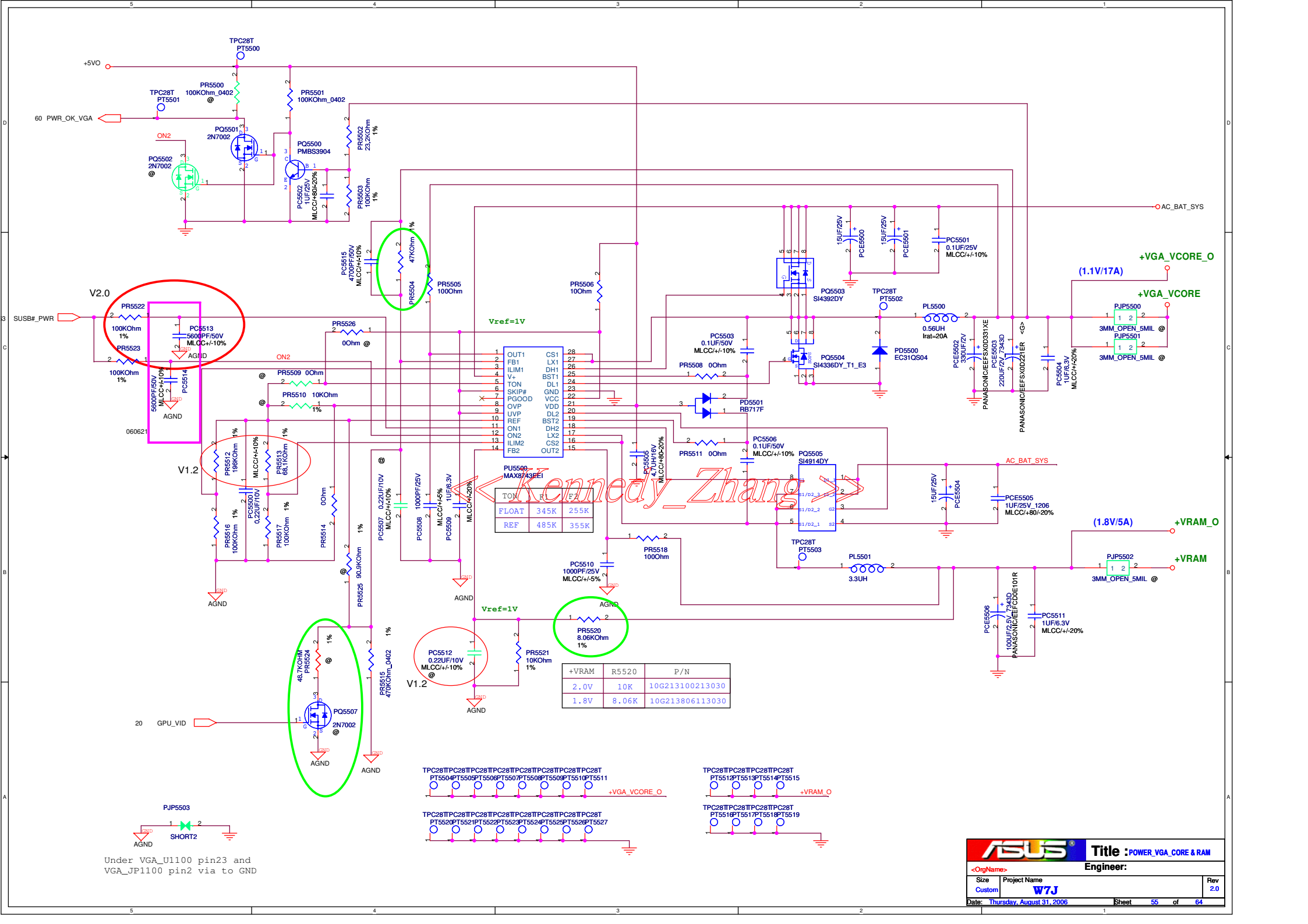




+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 54 of 64	



TOM	R1	R2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

ASUS

Title : POWER_VGA_CORE & RAM

Engineer:

<OrgName>

Size	Project Name	Rev
Custom	W7J	2.0

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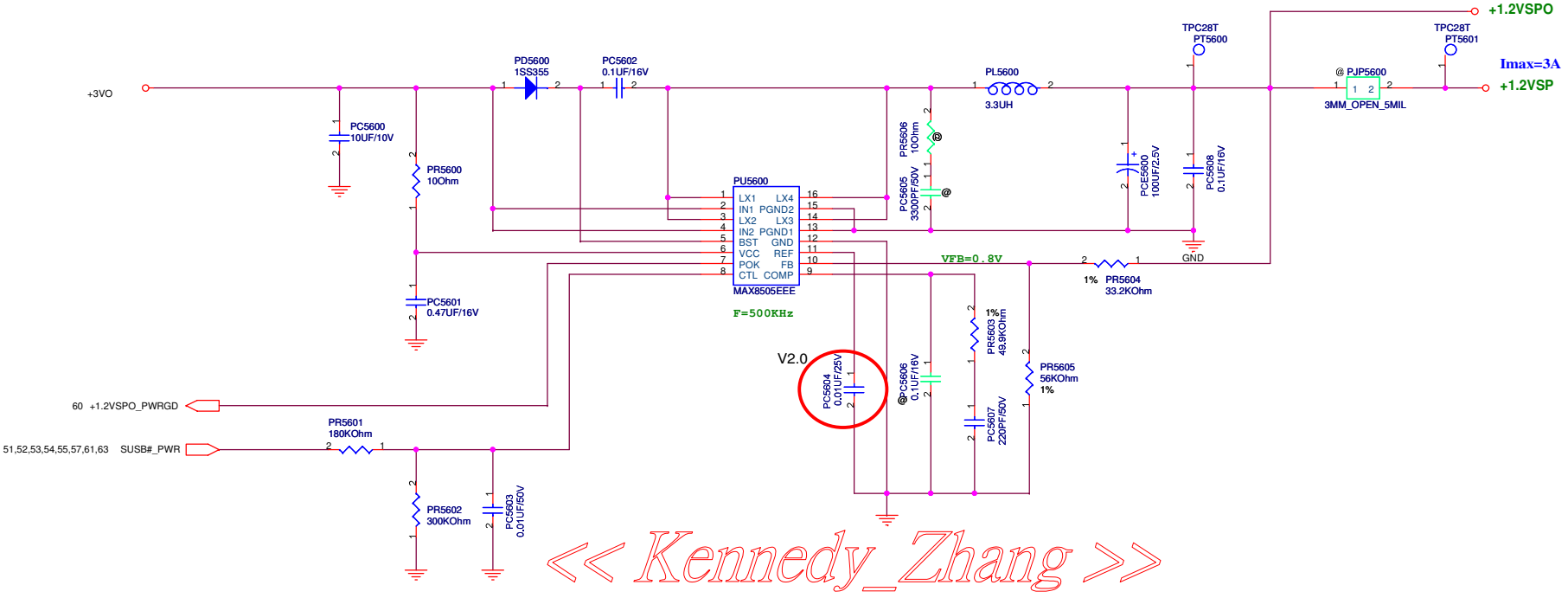
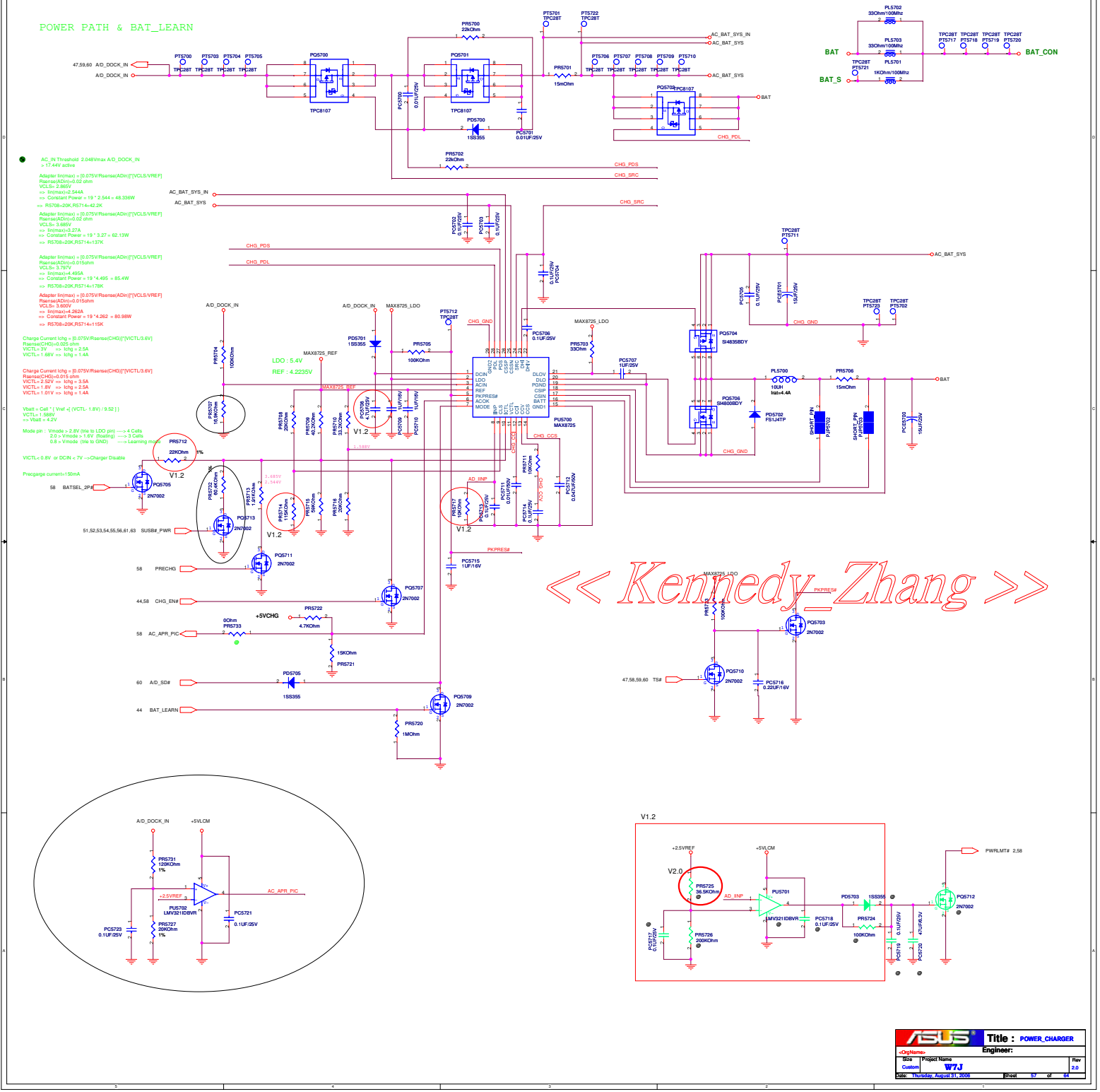
+1.2VSP



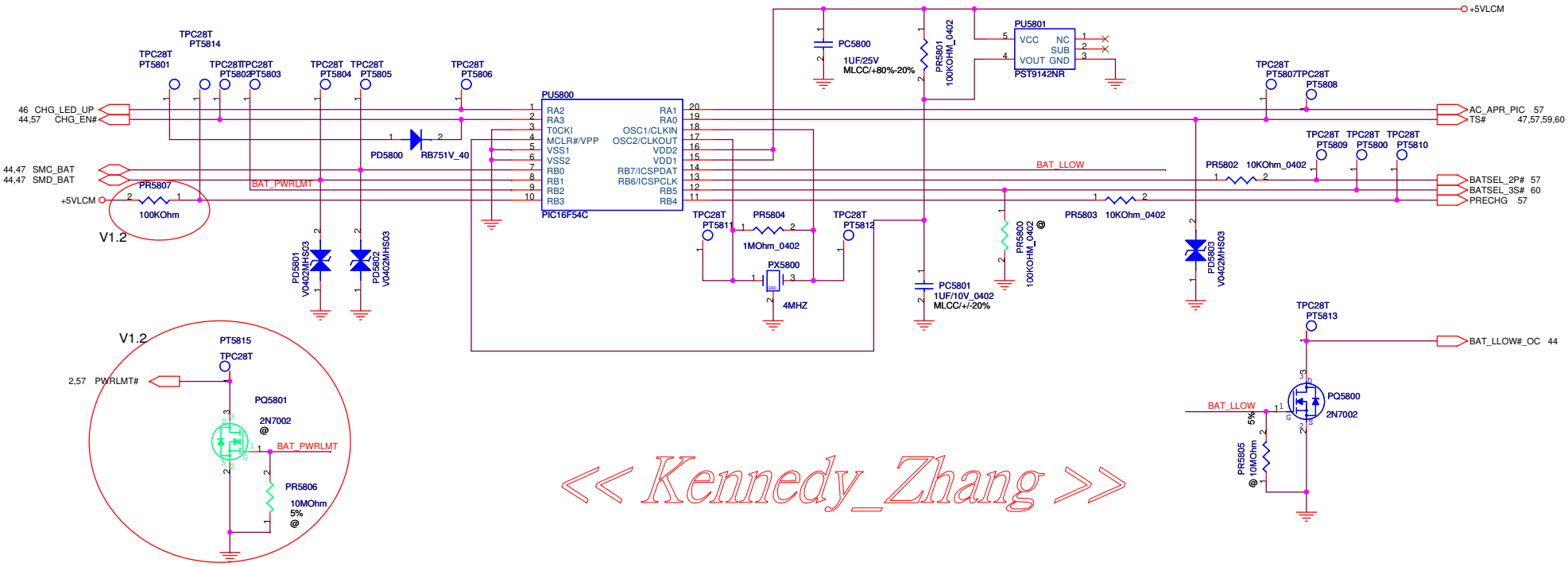
Title : POWER_VGA_+1.2VSP		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 56 of 64	

POWER PATH & BAT_LEARN



Title :	POWER_CHARGER
Engineer:	
<OrgName>	
Size: Custom	Project Name: W7J
Rev:	2.0
Date:	Thursday, August 31, 2006
Sheet	57 of 64

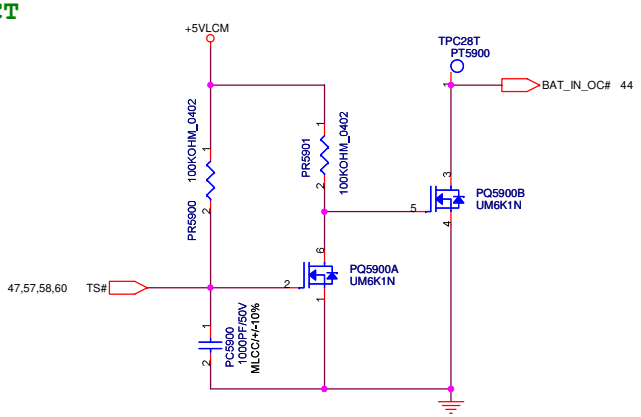
PIC16F54C



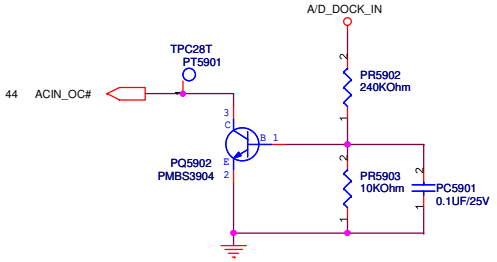
<< Kennedy_Zhang >>

ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 58 of 64	

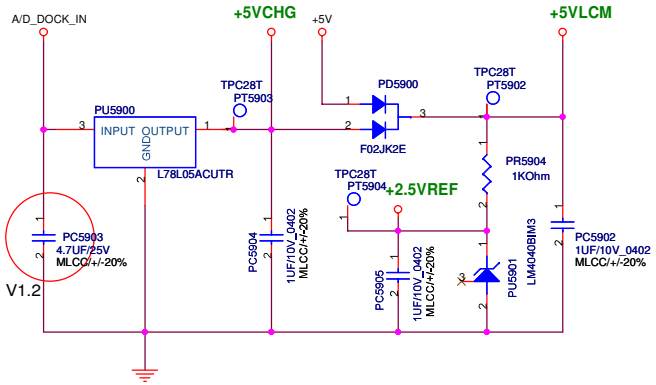
BATTERY IN DETECT



ADAPTER IN DETECT

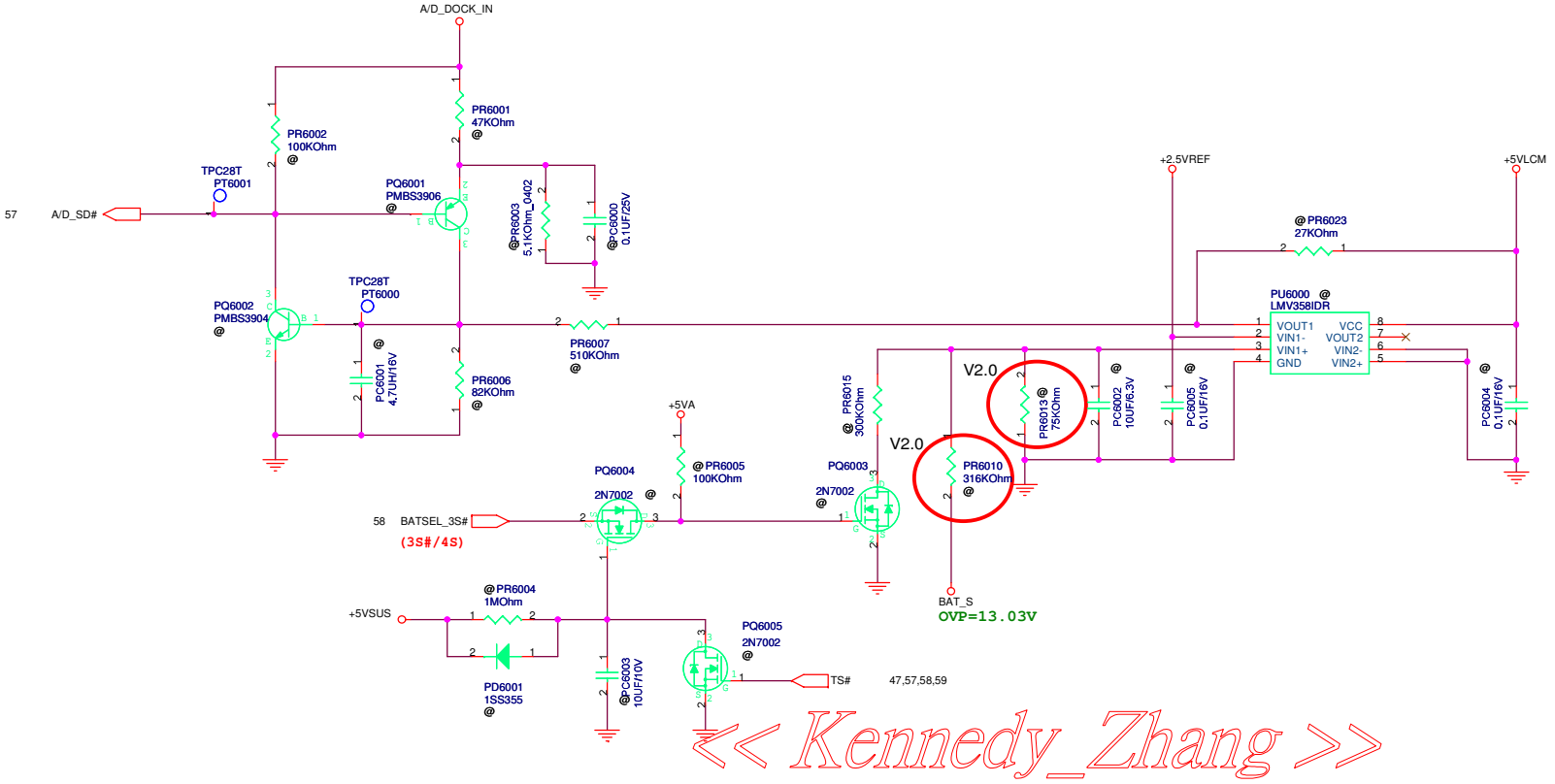


+5VLCM, +5VCHG & +2.5VREF

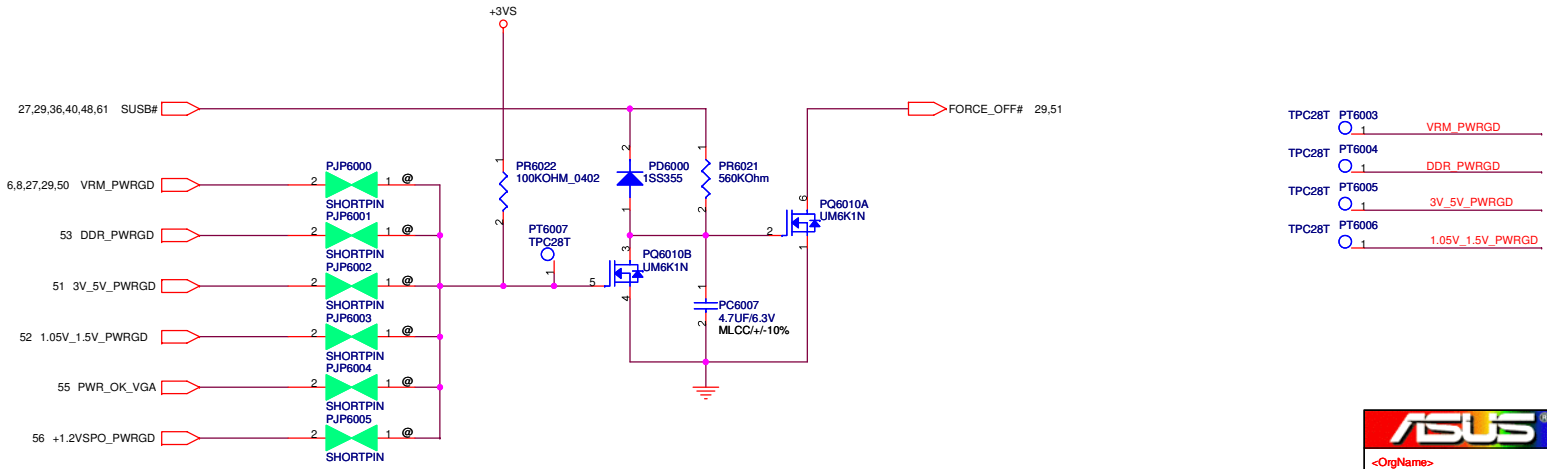


Title : POWER_DETECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 59 of 64	

BATTERY A/D_SD# (OVP)

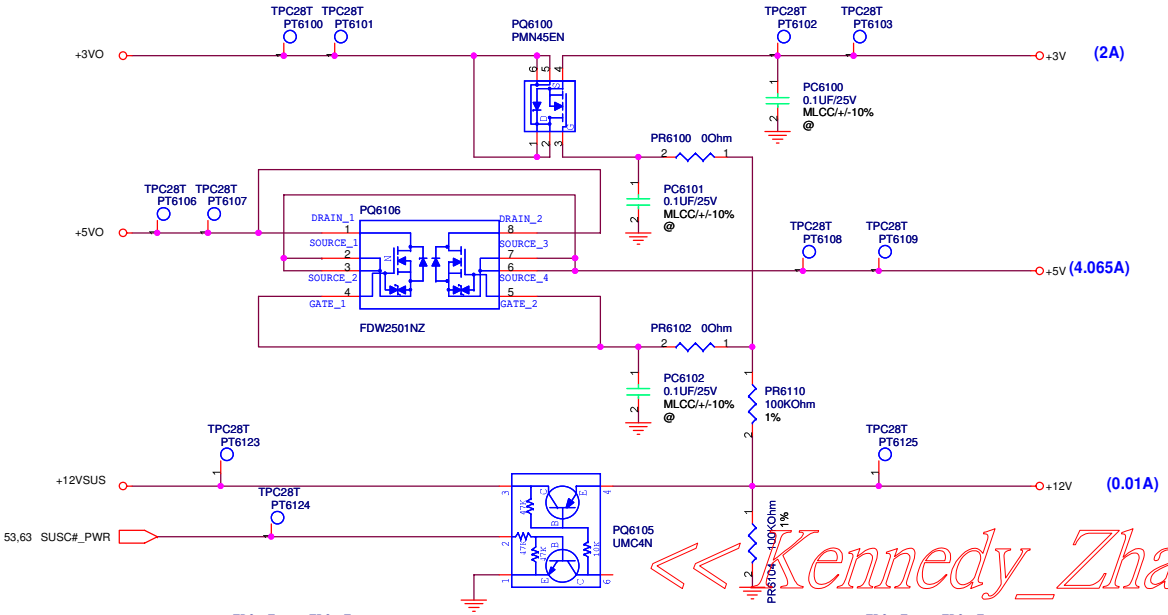


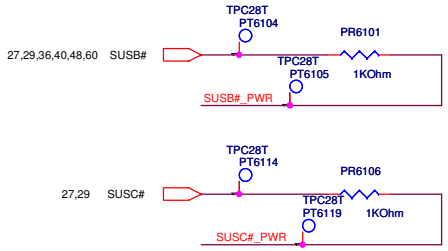
POWER GOOD DETECTER

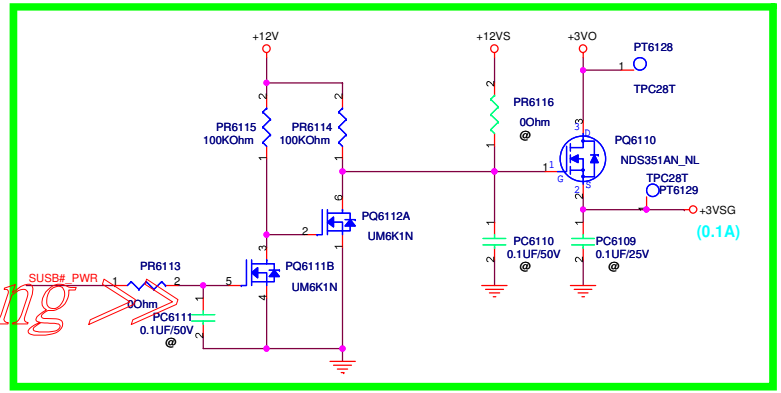


ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 60 of 64	

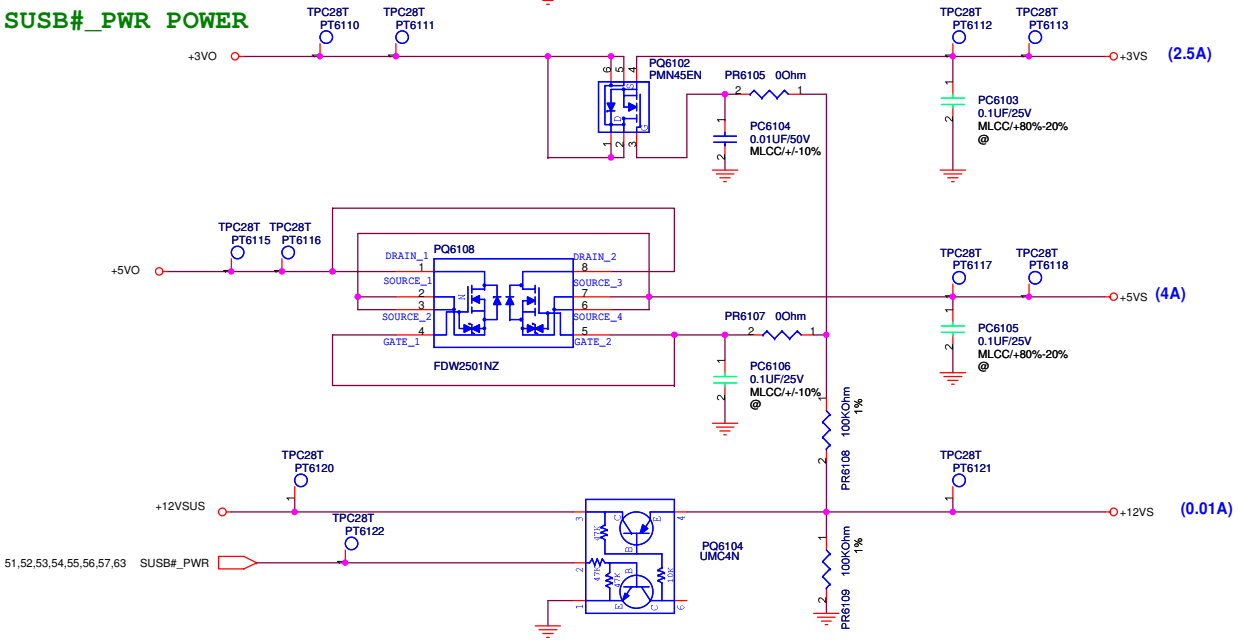
SUSC#_PWR POWER

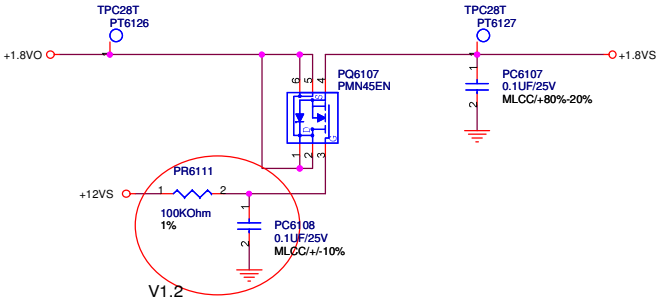






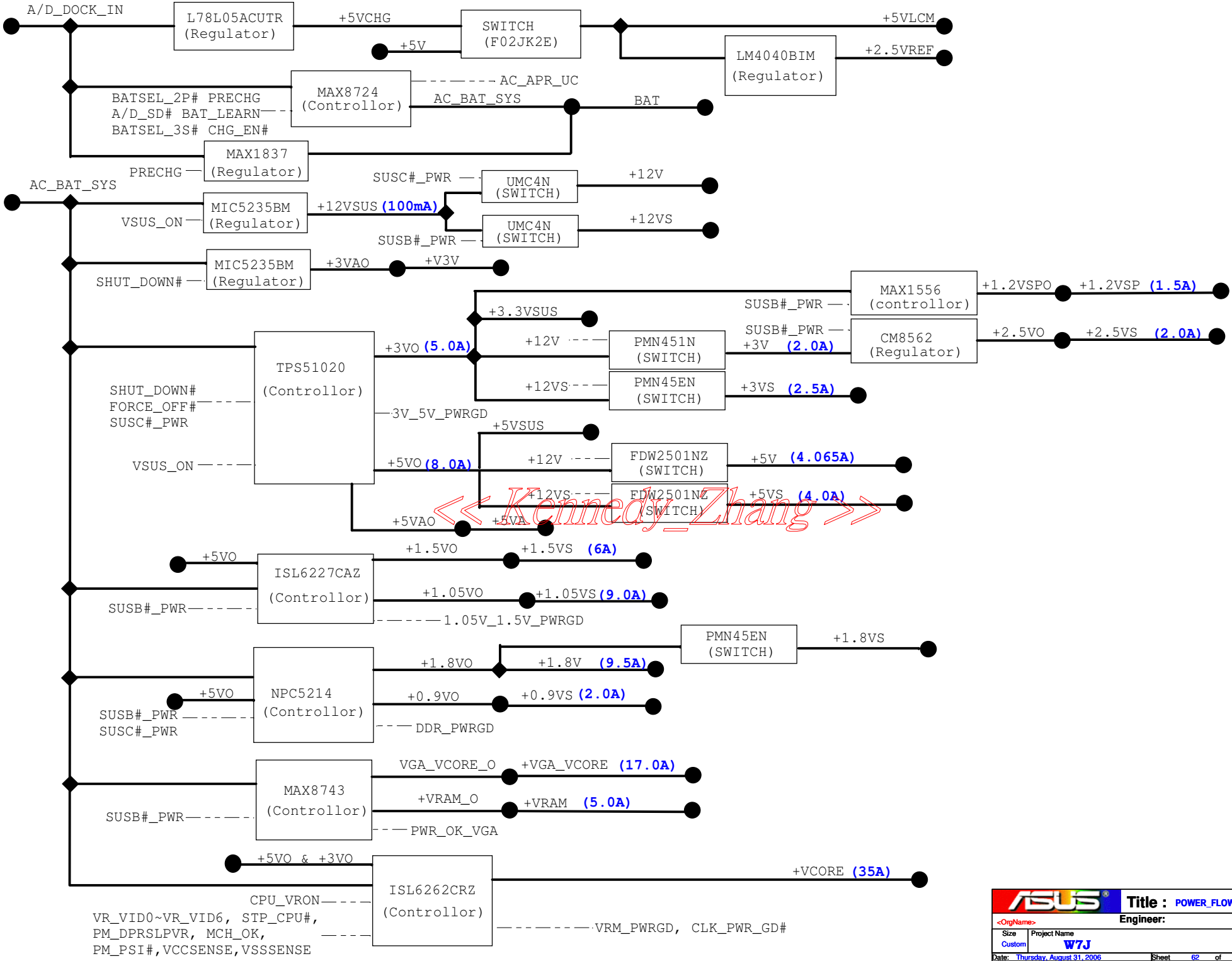
SUSB#_PWR POWER





V1.2

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 61 of 64	



AC_BAT_SYS → AC_BAT_SYS 23,50,51,52,53,54,55,57

+3VA → +3VA 25,29,47,54

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3VSUS → +3VSUS 26,27,28,29,32,38,41,51

+5VSUS → +5VSUS 28,51,60

+3V → +3V 26,29,39,40,41,44,48,54,61

+3VS → +3VS 5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,48,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 27,32,33,61

+12VS → +12VS 5,24,34,46,61

+5V → +5V 16,30,32,37,44,45,46,47,48,59,61

+5VS → +5VS 5,24,28,29,30,32,33,42,43,44,46,47,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 10,20,21,48,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,12,13,14,15,16,48,53

+1.8VS → +1.8VS 20,61

+VCCP → +VCCP 2,3,4,6,7,8,10,11,12,25,28,52

+0.9VS → +0.9VS 16,53

BAT → BAT 57

+5VCHG → +5VCHG 29,57,59

+5VLCM → +5VLCM 23,44,46,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,4,5,44,50

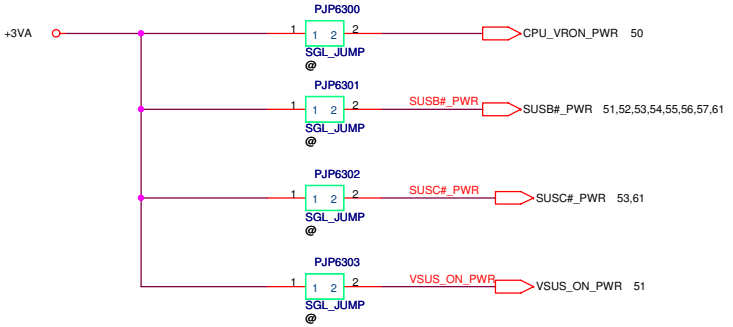
+VGA_VCORE → +VGA_VCORE 17,55

+VRAM → +VRAM 18,19,22,55

+1.2VSP → +1.2VSP 17,18,48,56

BAT_CON → BAT_CON 47,57

FOR POWER TEST



<< Kennedy_Zhang >>

Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 2.0
Date: Thursday, August 31, 2006	Sheet 63 of 64	

Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/29	1. Change Project name from W6J/H to W7J/F 2. Add NET: PWRLMT# to CPU pin: PROCHOT# (Page 2) 3. Add NET: DREFCLKSS,DREFCLKSS# to CLK GEN: pin17,pin18 (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# to GMCH: C40,D41 (Page 8) 5. Pull high GMCH VCCA_LVDC to +2.5VS (Page 10) 6. Add Jumper at G72M pin: B4 (Page 20) 7. Change R6811 from 200Kohm to 100Kohm (Page 23) 8. Change U57,U58 from 74LVC1G32GV to NC7SZ08M5 (Page 24) 9. Change D2 from EC31QS04 to RB751V_40 (Page 24) 10. Add Double-pi filter in VGA port (Page 24) 11. Swap ICH PCIE lans (Page 26) 12. Change GPIO7 NET from WB_AP to MUTE_POP_ICHGPIO# (Page 27) 13. Add NET: PWR_LED_1HZ to ICH: GPIO13 (Page 27) 14. Add Q6197 in net: PCIE_WAKE# (Page 27) 15. Add Q6192 in net: PWR_SW#_Q (Page 29) 16. Change R719 from 100Kohm to 1Mohm (Page 29) 17. Change R306 from 1Mohm to 10Mohm (Page 29) 18. Change C388 from 0.33uF to 1uF (Page 29) 19. Change Pull-high LID_EC# from +3VSUS to +3V (Page 29) 20. Change Audio CODEC from ADI1986 to ALC660 (Page 30) 21. Change R6614 from 0ohm to 4.7Kohm (Page 32) 22. Change R6616 from 10Kohm to 51KOhm (Page 32) 23. Change R6613 from 0ohm to 4.7Kohm (Page 32) 24. Change R6615 from 10Kohm to 51KOhm (Page 32) 25. Add NET: MUTE_POP_ICHGPIO# to MUTE_POP# circuit (Page 32) 26. Add Q6193 in net: SUSCLK (Page 34) 27. Change SLB9635TT pin16 from PLT_RST# to BUF_PLT_RST# (Page 34) 28. Delete NET PME# (Page 36) 29. Change Pull-high MDIO04 from +3V to +3VS (Page 37) 30. Change Pull-high XD_PWR_EN from +3V to +3VS (Page 37) 31. Change PCIE lans from port 1 to port 2 (Page 38) 32. Add C6625,C6626 in phone connector (Page 39) 33. Change PCIE lans from port 3 to port 1 (Page 40) 34. Add NET: EXPD# to R5538 pin20 (Page 40) 35. Add NET: C_PRESENT# to R5538 pin9,pin10 (Page 40) 36. Change PCIE lans from port 2 to port 3 (Page 41) 37. Change Pull-high 802WLAN_ON# from +3V to +3VSUS (Page 41) 38. Change FWH packaging from PLCC to TSOP (Page 43) 39. Add NET: EXPD# to M38857 P53 (Page 44) 40. Add NET: WB_AP to M38857 P67 (Page 44) 41. Add NET: C_PRESENT# to M38857 P62 (Page 44) 42. Add NET: ACZ_RST#_AUD to M38857 P61 (Page 44) 43. Change U10,U6012 pin4 from SUSC# to SUSC (Page 45) 44. Add Q6196 in net: BTPWRCL# (Page 45) 45. Add R6922 between net: WIRELESS_LAN_ON/OFF# and WB_AP (Page 47) 46. Add Q6198 in +3VS discharge (Page 48) 47. Change Power LED ON circuit (Page 48)

Rev	Date	Description
R1.2	2005/12/20	1. Change R6491 from 23.2KOhm to 51KOhm (Page 5) 2. Add Q6200 at U42 :D2+,D2- (Page 5) 3. Add NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 4. Add RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 5. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 6. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 7. Change R1001 from 1Kohm to C6631:0.1uF (Page 16) 8. Modify LCD enable circuit by U6059 (Page 23) 9. Change L89,L90,L92 to Bead 120Ohm/100MHz (Page 24) 10. Change Q60,Q61 from SI1906DL to SI1902DL (Page 24) 11. Add C6632 in Y1 (Page 25) 12. Connect H_DPRSTP# to PU5000 (Page 25) 13. Change U69 from SN74LVC1G32G to 74LVC1G32GV (Page 26) 14. Disonnect STP_CPU# to PU5000 (Page 27) 15. Add GPIO9:W_OLED# (Page 27) 16. Change R523 from 10KOhm to 100KOhm (Page 29) 17. Change R303 from 10KOhm to C6630:1uF (Page 29) 18. Add R6936 in Net:PWR_SW#_Q (Page 29) 19. Add R6633,R6634,R6635,R6636 in CN20(Page 31) 20. Add R6938 in +3.3Vaux (Page 41) 21. Change CE41,CE5705,CE25 from 100uF to 150uF (Page 45) 22. Add R6937 in BTPWRCL# (Page 45) 23. Change Q6180,Q6181 by Q6202 (Page 46) 24. Add Q6201,LED10 in WIRELESS_OLED# (Page 46) 25. Change R6686 from 0Ohm to 470Ohm (Page 47) 26. Add R6940 in Power Board +5Vs (Page 47)
R2.0	2006/2/23	1. Change R6491 from 51KOhm to 36.5KOhm (Page 5) 2. Del NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 3. Del RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 5. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 6. Add R6945 at U6028: H22 (Page 18) 7. Add R6944 in MUTE_POP# (Page 32) 8. Change L5708 to R6943 (Page 38) 9. Del R6915,R6916,R6917 in CON15 (Page 40) 10. Change R613 from 10K ohm to 0 ohm(Page 42) 11. Change CON11 from 8 pin to 6 pin (Page 45) 12. Add R6946,R6947 at BATT_GND (Page 47) 13. Add D6040 at CN14 (Page 47)

<Variant Name>

ASUSTek Computer INC. NB1

Title : History

Engineer:

Size	Project Name	Rev
Custom	W7J	2.0

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