T19R

Rev2.0

Yonah/RC410ME/IXP450 BLOCK DIAGRAM

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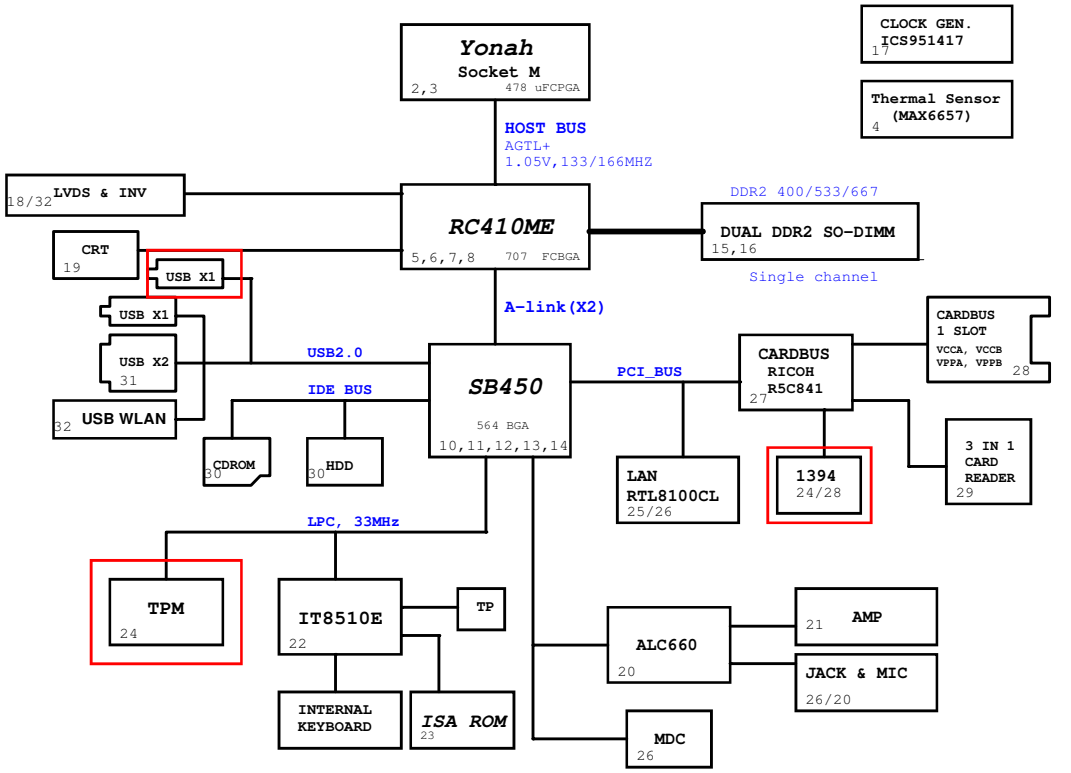
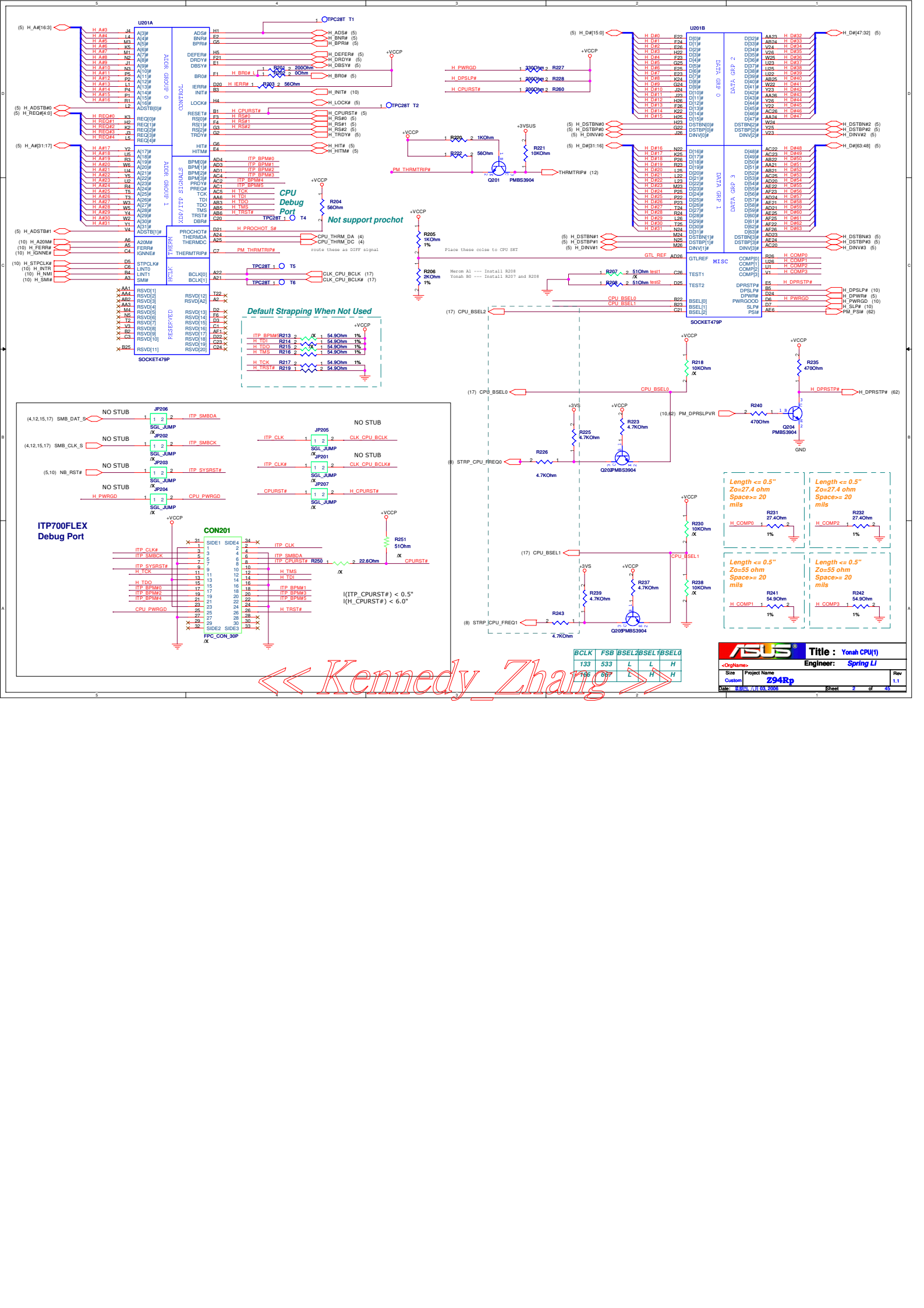
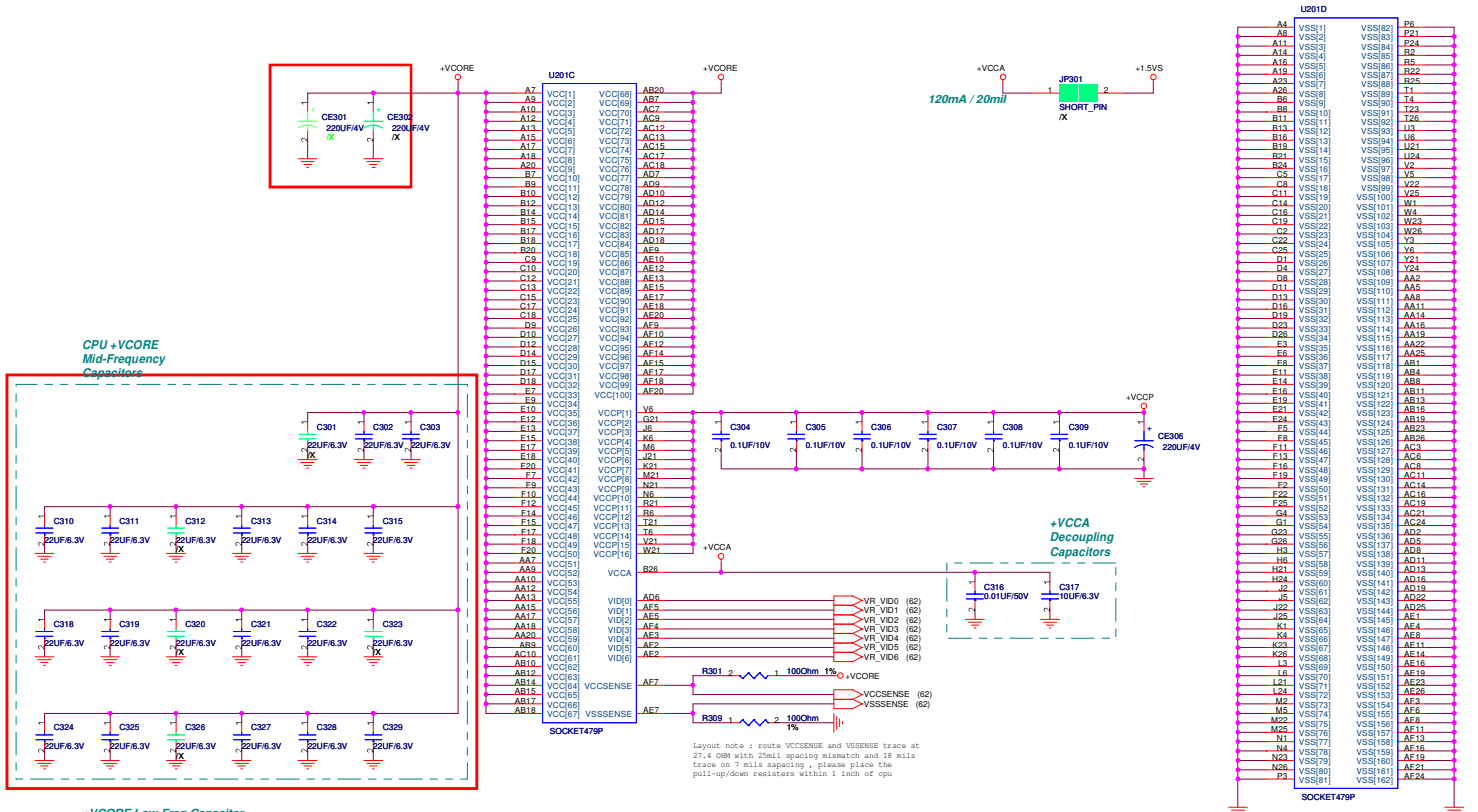
**	



ASUS-HD Server | Title : BLOCK DIAGRAM | Engineer: shelleys | Size: Custom | Project Name: T19R | Rev: 1.0 | Date: 星期四, 七月 20, 2006 | Sheet 1 of 45

<< Kennedy_Zhang >>


U201A
U201B
SOCKET479P
CPU Debug Port
Not support prochot
Default Strapping When Not Used
ITP700FLEX Debug Port
CON201
FPC_CON_30P
Meroma A1 === Install R208
Yonah B0 === Install R207 and R208
Place these colse to CPU SKT
route these as DIFF signal
I(ITP_CPURST#) < 0.5"
I(H_CPURST#) < 6.0"
Length <= 0.5" Zo=27.4 ohm Space>= 20 mils
Length <= 0.5" Zo=55 ohm Space>= 20 mils
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : Yonah CPU(1)
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 2 of 45
Kennedy_Zhang



+VCORE Low-Freq Capacitor
*Intel: 330UF *6*
*ATI: 330UF *6*
*R1F: 330UF *4*
*A7J: 330UF *5*
+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*ATI: 10UF *26*
*R1F: 22UF *16*
*A7J: 22UF*29 use 19*
*A6RF: 22UF*21 use 21*
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*R1F: 220UF *1, 0.1UF *4*
*A7J: 220UF *1, 0,1UF *6*
*A6RF: 220UF *1, 0,1UF *6*

ASUS

Title : Yonah CPU(2)

<OrgName>

Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

Date: 星期四, 八月 03, 2006 Sheet 3 of 45

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Fan Speed Control

KBC will issue a analog (a voltage level) signal.

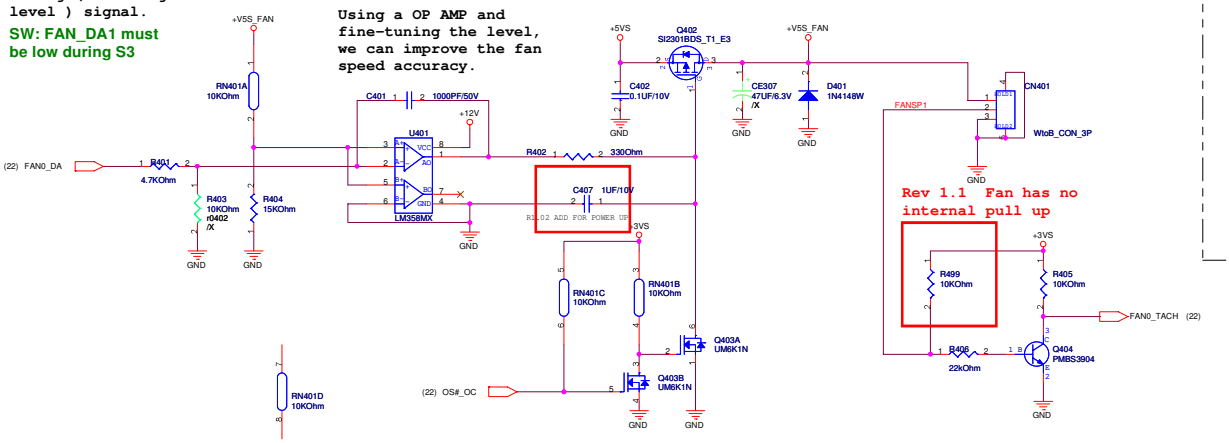
SW: FAN_DA1 must be low during S3

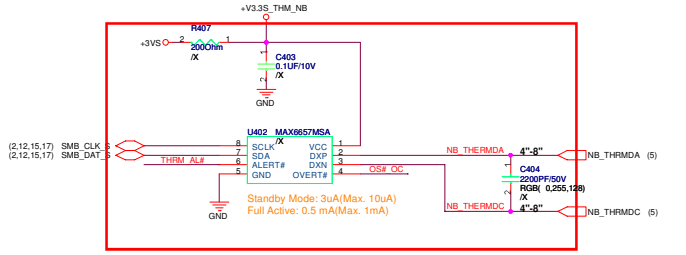
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

Route H_THERMDA and H_THERMDC on the same layer

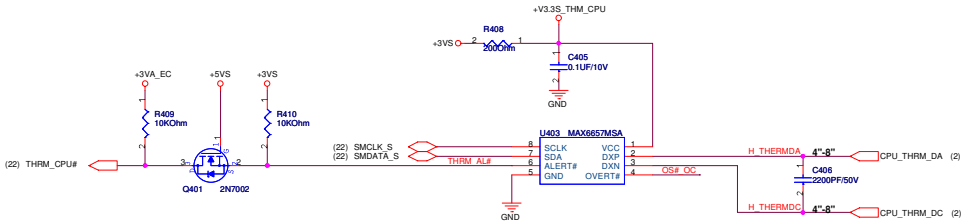
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



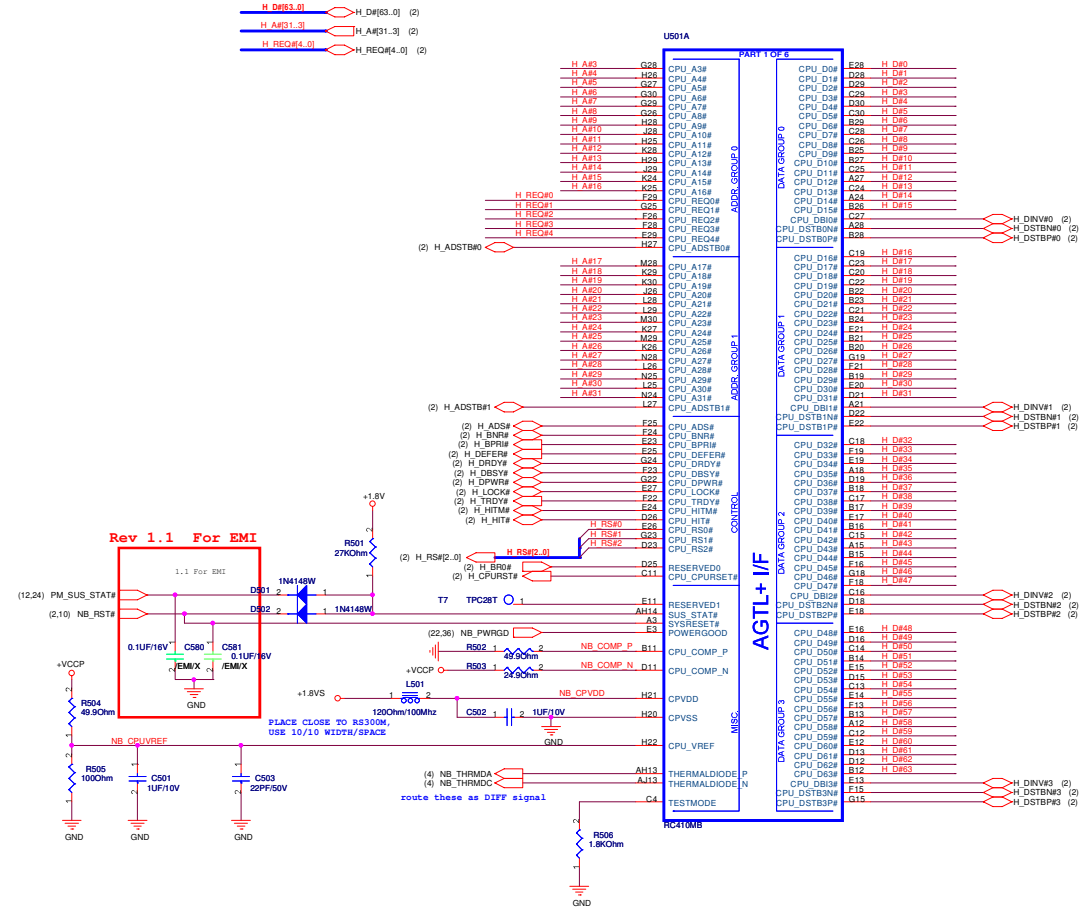


NB Detect



CPU Detect

Title : THERMAL SERSOR,FAN			
Engineer: Spring Li			
<OrgName>			
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 4	of 45	



Title : RC410ME AGTL I/F(1)			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 목요일, 八月 03, 2006	Sheet 5 of 45		

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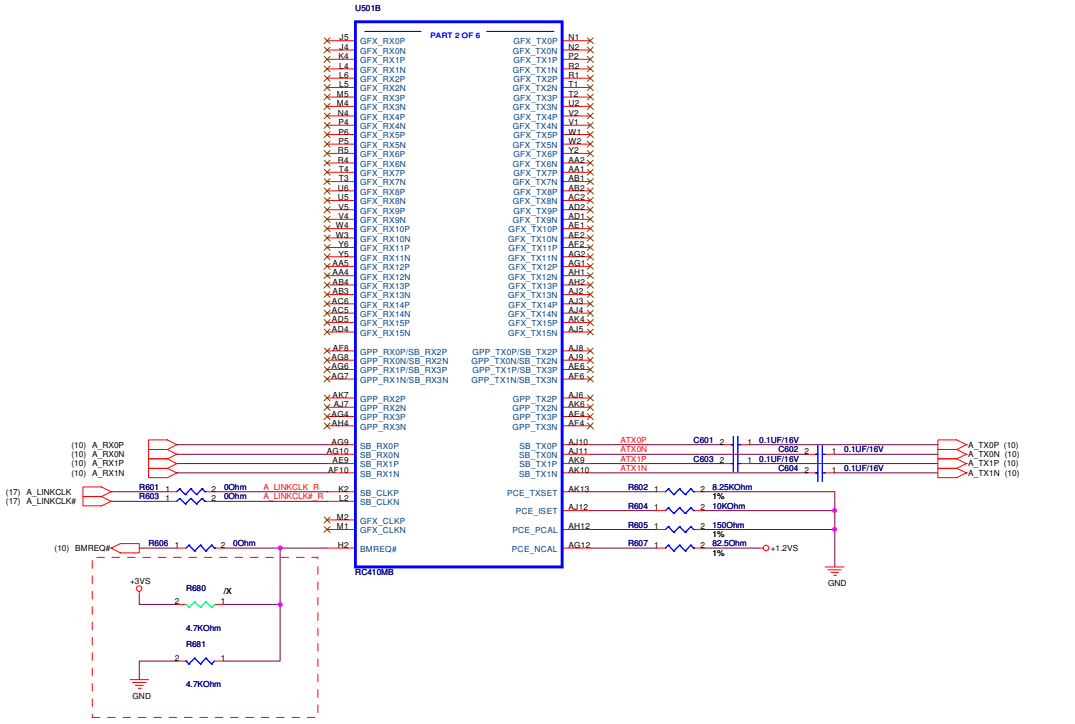
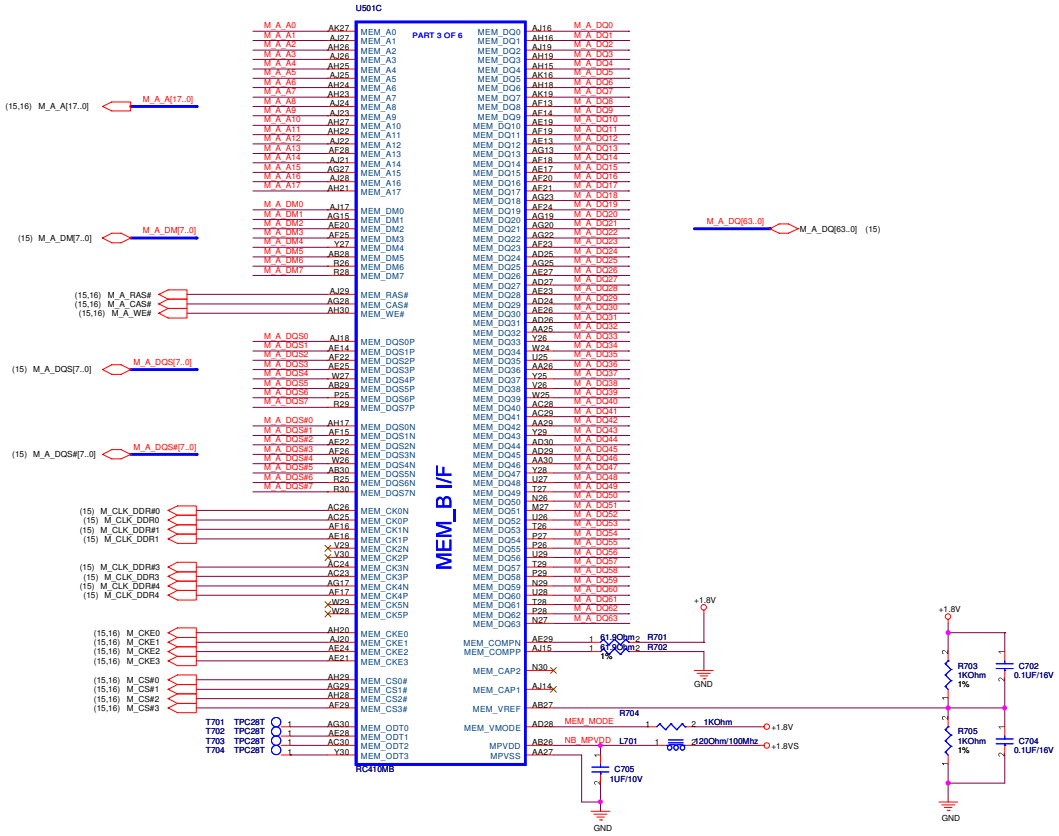


Title : RC410ME PCIE & A-Link(2)			
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 6 of 45		



<OrgName>	Title : RC410ME DDR2 I/F (3)		
	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 7	of 45	

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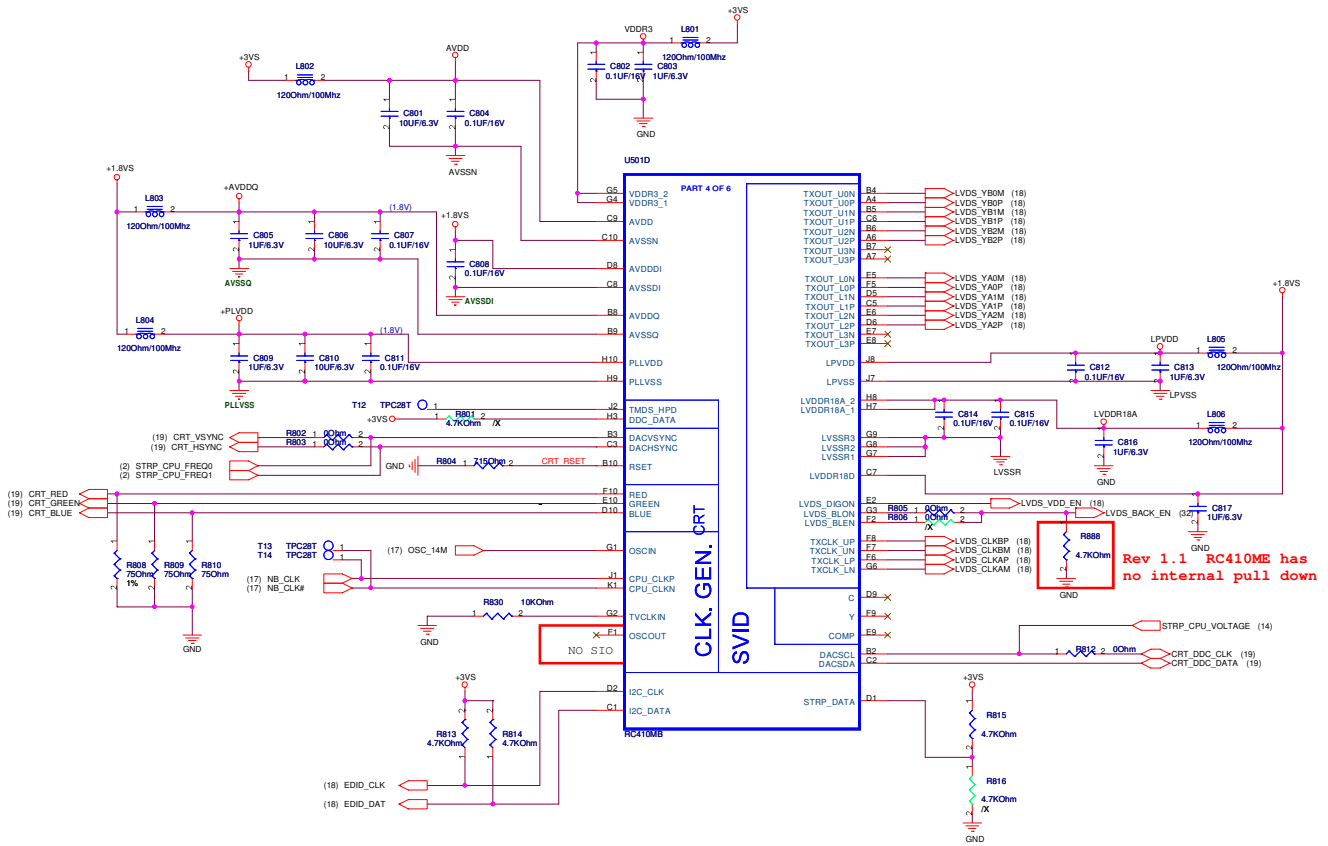
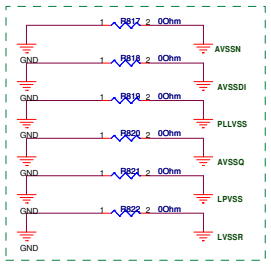
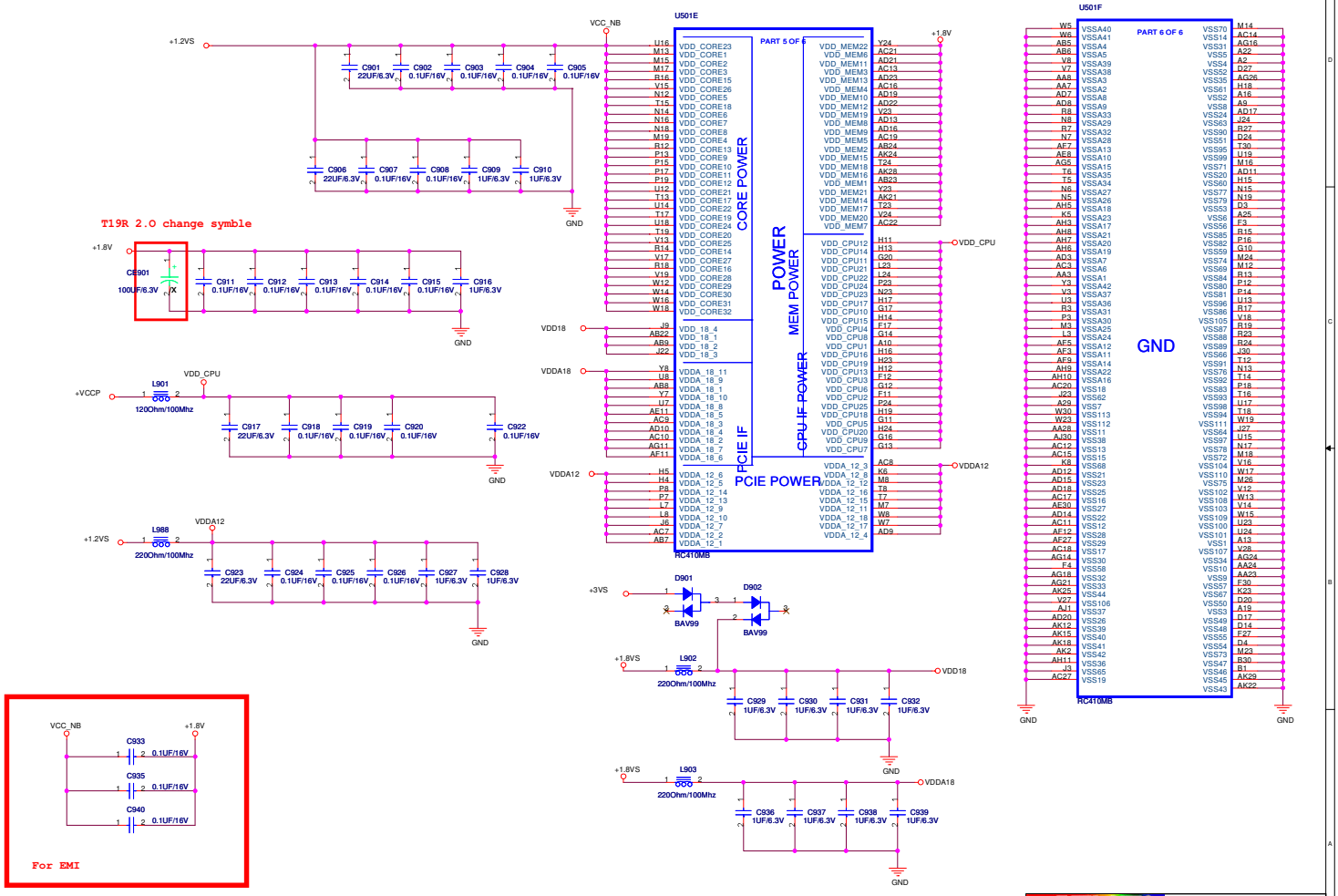


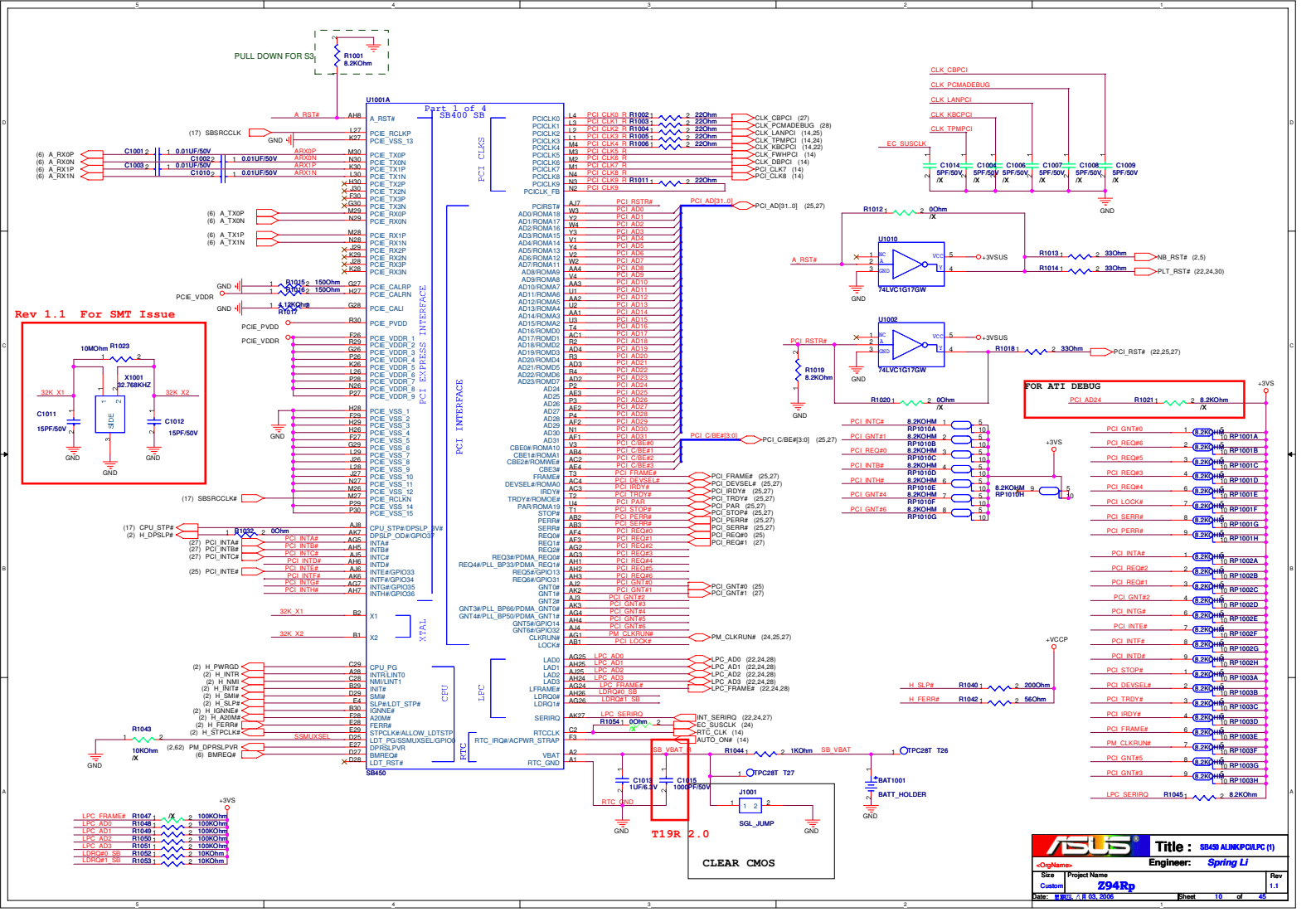


Title : RC410ME VIDEO I/F (4)			
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 8 of 45		

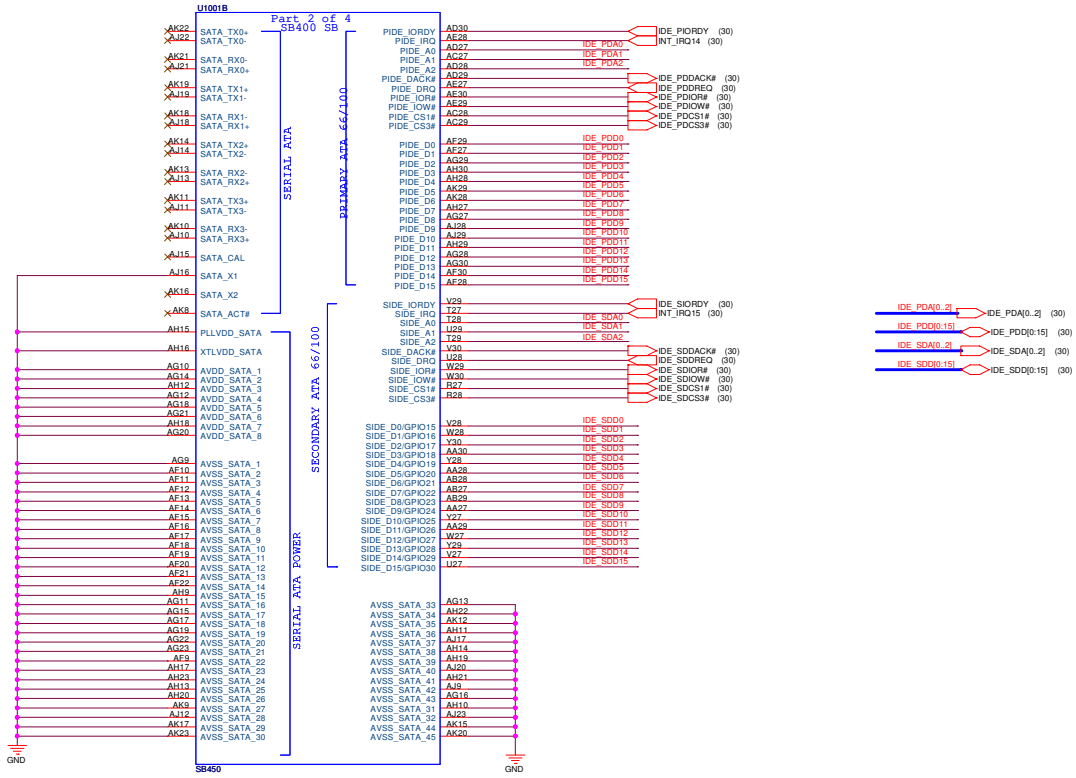


Title :	RC410ME POWER (5)		
<OrgName>		Engineer:	Spring LI
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二, 七月 10, 2006		Sheet 9 of 45	

<< Kennedy_Zhang >>

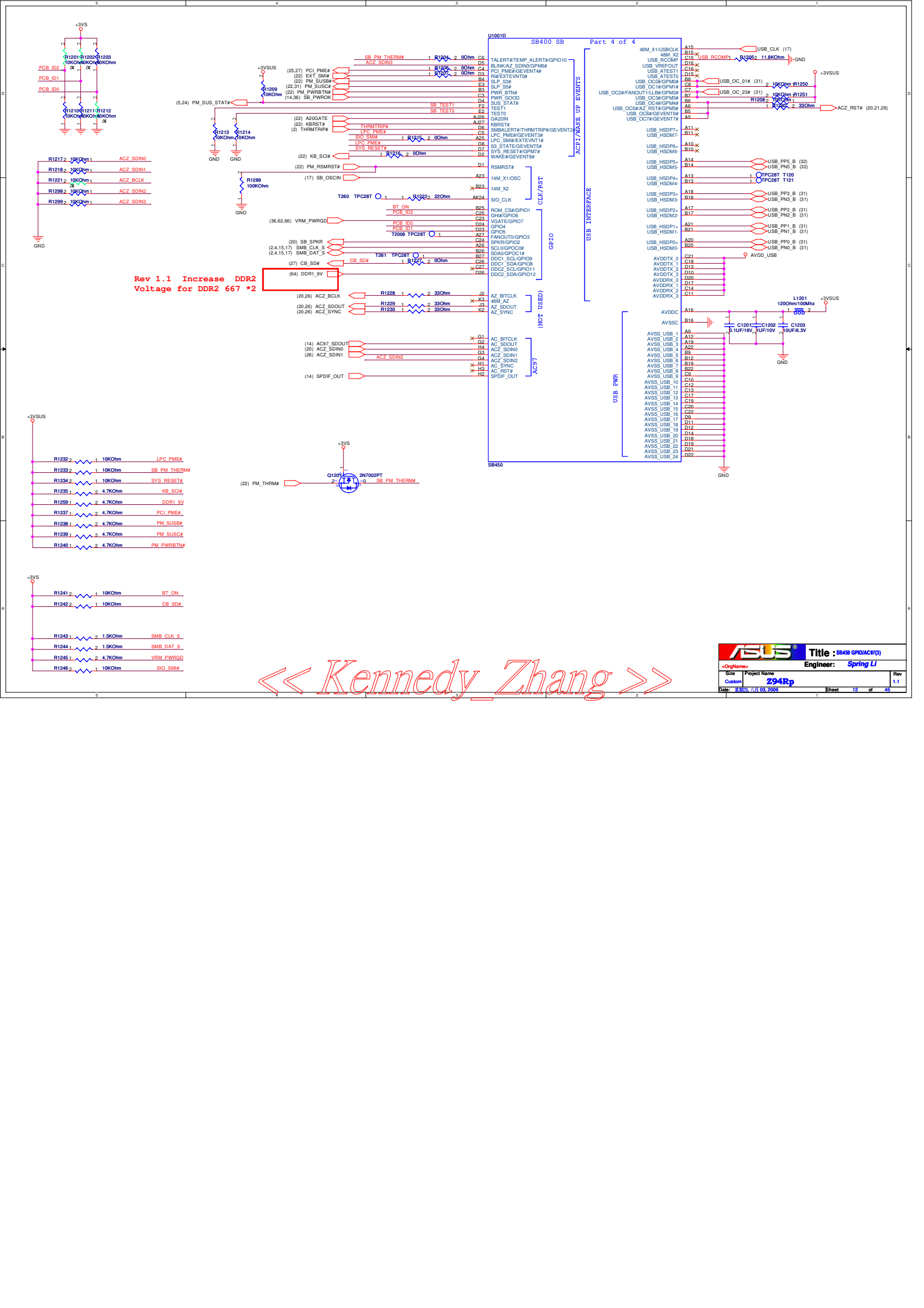


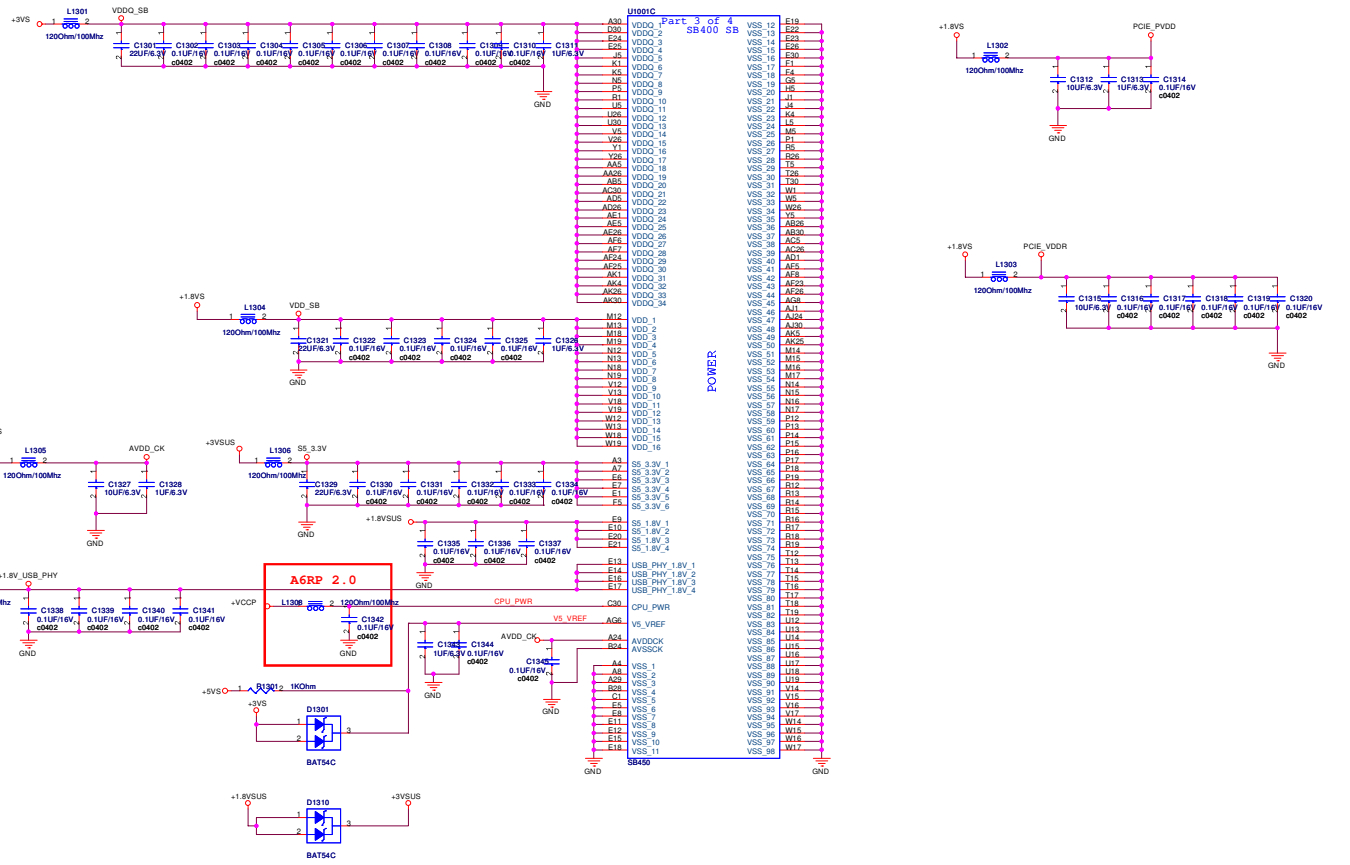
<< Kennedy_Zhang >>



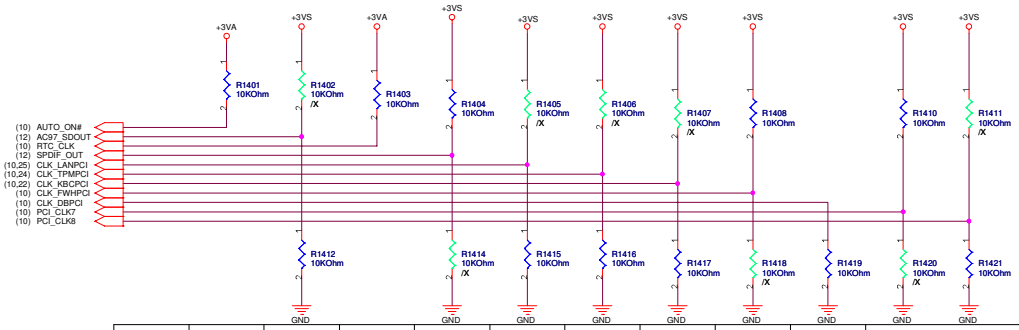
Title : SB450 IDE (2)		
<OrgName>	Engineer: Spring LI	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 11 of 45	

<< Kennedy_Zhang >>


U1001D
SB400 SB
Part 4 of 4
SB450
Rev 1.1 Increase DDR2 Voltage for DDR2 667 *2
ACPI/WAKE UP EVENTS
USB INTERFACE
CLK/RST
GPIO
(NOT USED)
AC97
USB_PWR
Title : SB450 GPIO/AC97(3)
Engineer: Spring Li
Z94Rp
Rev 1.1
Sheet 12 of 45
<< Kennedy_Zhang >>



ASUS	Title : SB450 PWR/DECOUPING		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: 294Rp		Rev: 1.1
Date: 星期二, 六月 24, 2008	Sheet 13 of 45		



REQUIRED STRAPS

	AUTO_ON#	AC_SDOUT	RTC_CLK	SPDIF_OUT	CLK_LANPCI	CLK_SIOPCI	CLK_KBCPCI	CLK_FWHPCI	CLK_DBPCI	PCI_CLK7 PCI_CLK8
PULL HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	SIO 24MHz	SEE NOTE1	USB PHY PWRDOWN DISABLE	USE USB PLL	SEE NOTE2	CPU I/F = K8	ROM TYPE H,H = PCI ROM H,L = LPC ROM I DEFAULT LPC Address Mapped below 1M L,H = LPC ROM II LPC Address Mapped to top 4G L,L = FWH ROM
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz		USB PHY PWRDOWN ENABLE	BYPASS USB PLL		CPU I/F = P4	

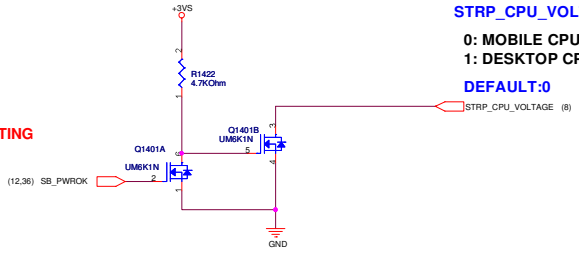
NOTE

1. USB CLK STRAPPING CHANGE

	A21,A22,A23	A31 AND NEWER
10K PULL UP	OSC/CLOCK BUFFER	CRYSTAL PAD
10K PULL DOWN	CRYSTAL PAD	OSC/CLOCK BUFFER

2. 14MHz CLOCK TYPE STRAPPING

	A11~A31	A32 AND ABOVE
	14MHz CLOCK PAD IS CRYSTAL PAD	PCIE COMMON MODE SETTING
10K PULL UP	CLOCK INPUT BUFFER	PCIE CM_SET LOW
10K PULL DOWN	CRYSTAL PAD	PCIE CM_SET HIGH



STRP_CPU_VOLTAGE: CPU VCC

0: MOBILE CPU
1: DESKTOP CPU

DEFAULT:0

ASUS	Title : SB450 STRAPS(5)	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 14 of 45	

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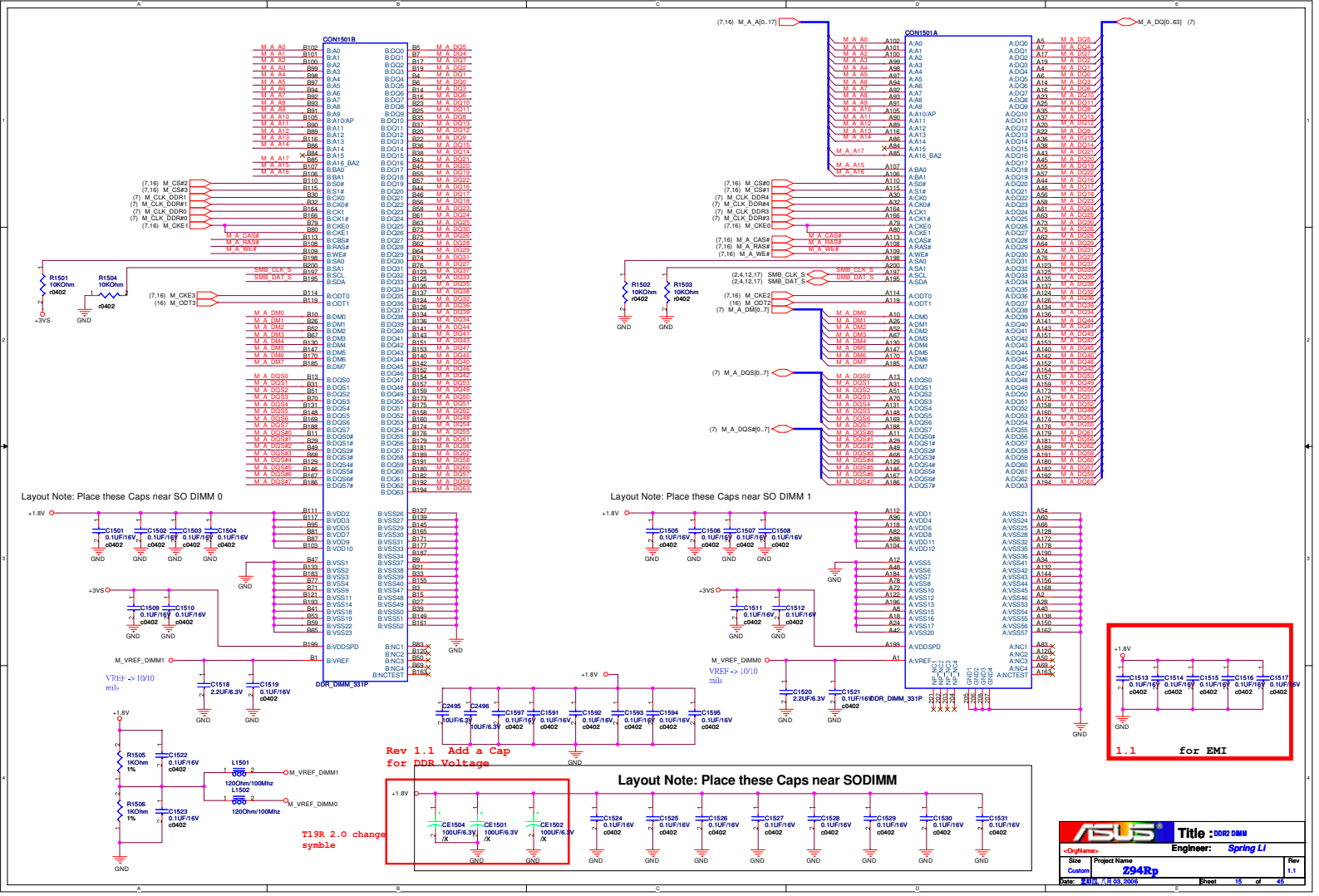
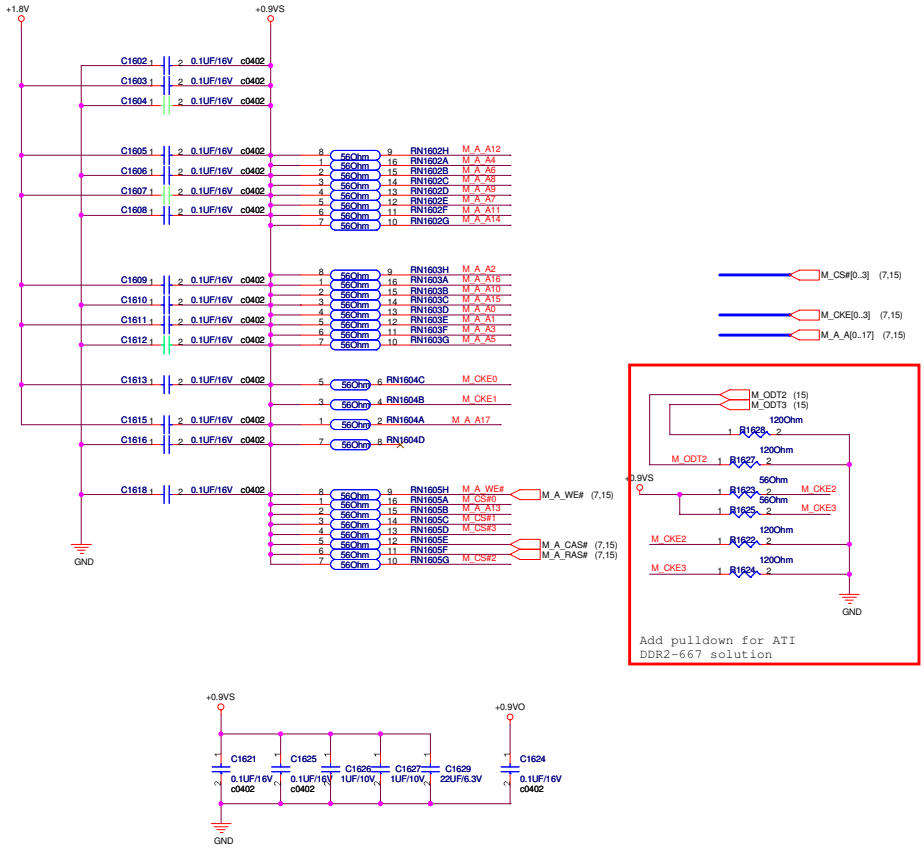


<< Kennedy_Zhang >>



Title : DDR2 Termination			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 16 of 45		

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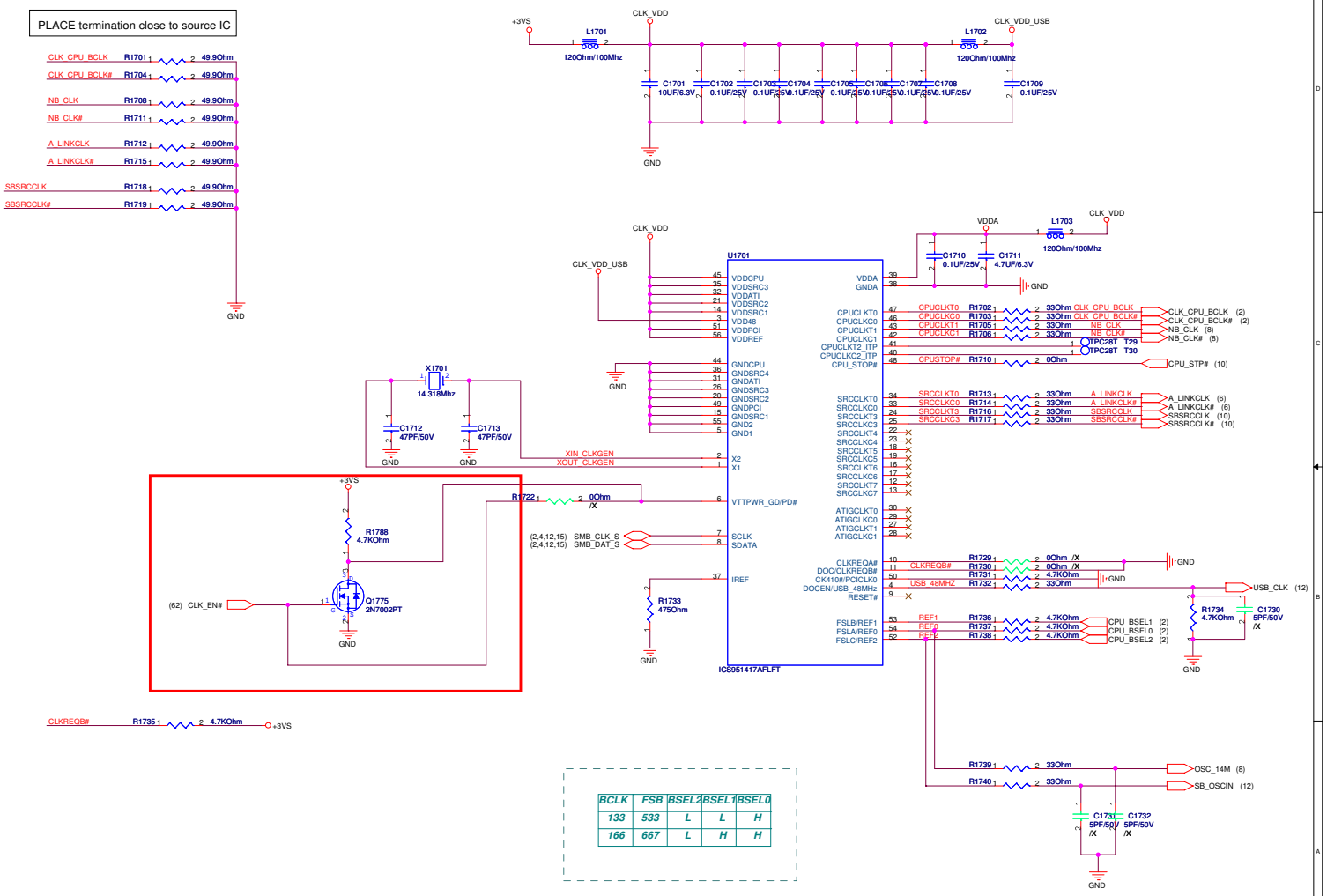

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Title : CLOCK GENERATOR

<OrgName> Engineer: Spring Li

Size	Project Name	Rev
Custom	Z94Rp	1.1

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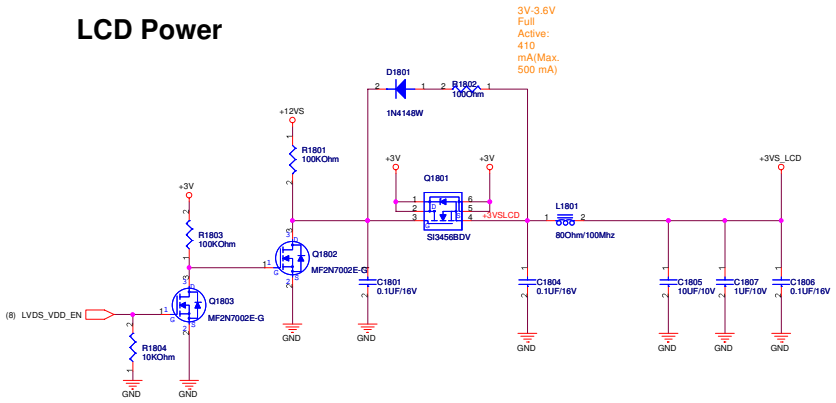
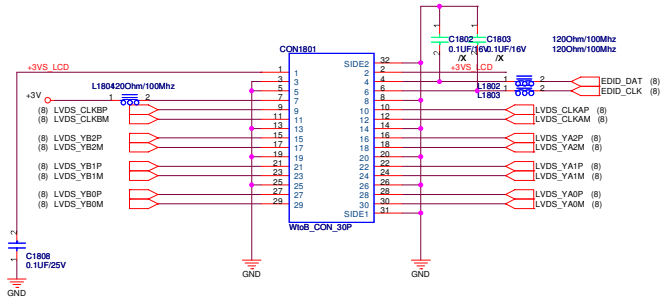
LCD Power

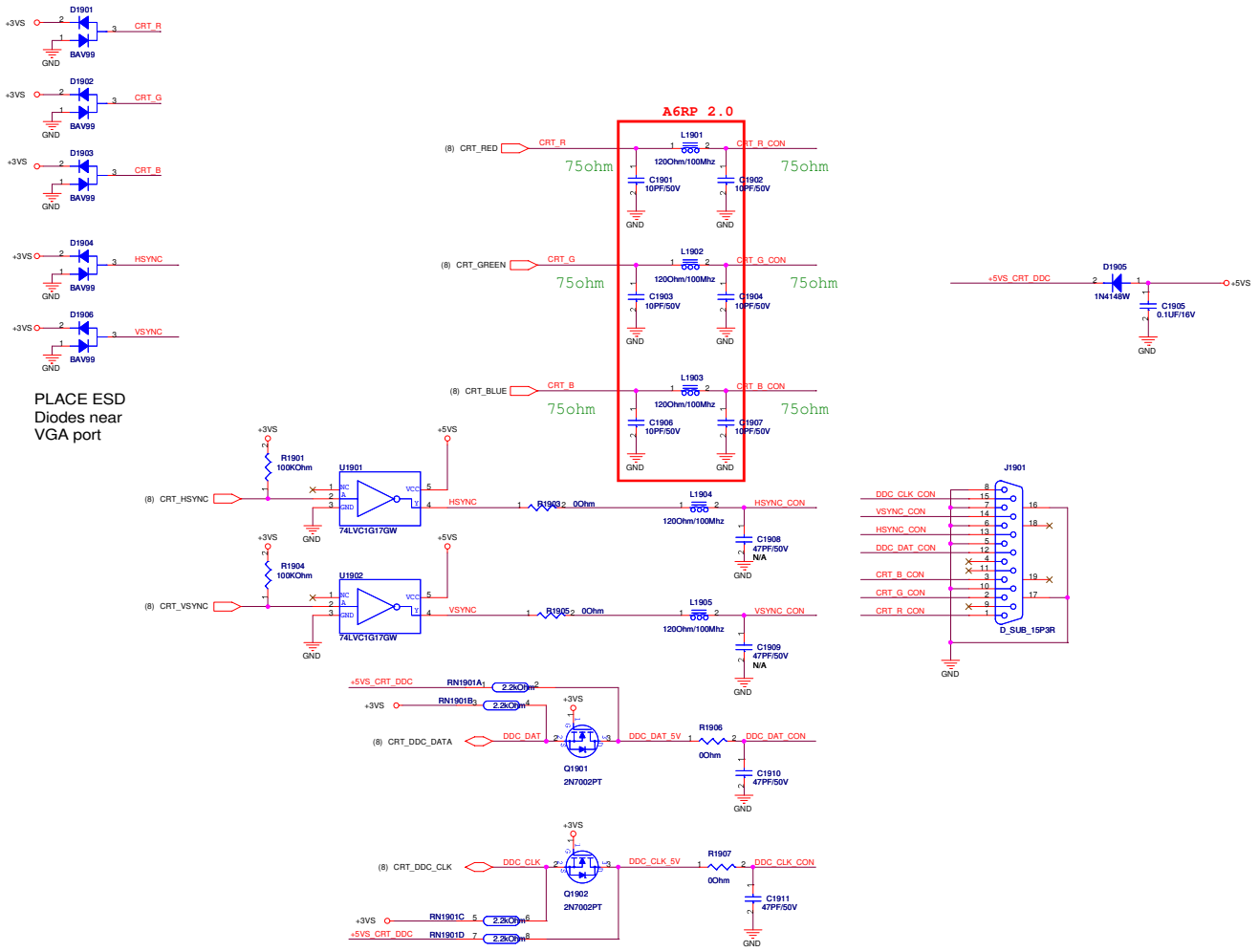




Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

ASUS	Title :	LVDS & INVERTER (CAMERA)
<OrgName>	Engineer:	Spring LI
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 18 of 45	



Title : CRT CONNECTOR

<OrgName> Engineer: Spring LI

Size: Custom | Project Name: Z94Rp | Rev: 1.1

Date: 星期四, 八月 03, 2006 | Sheet 19 of 45

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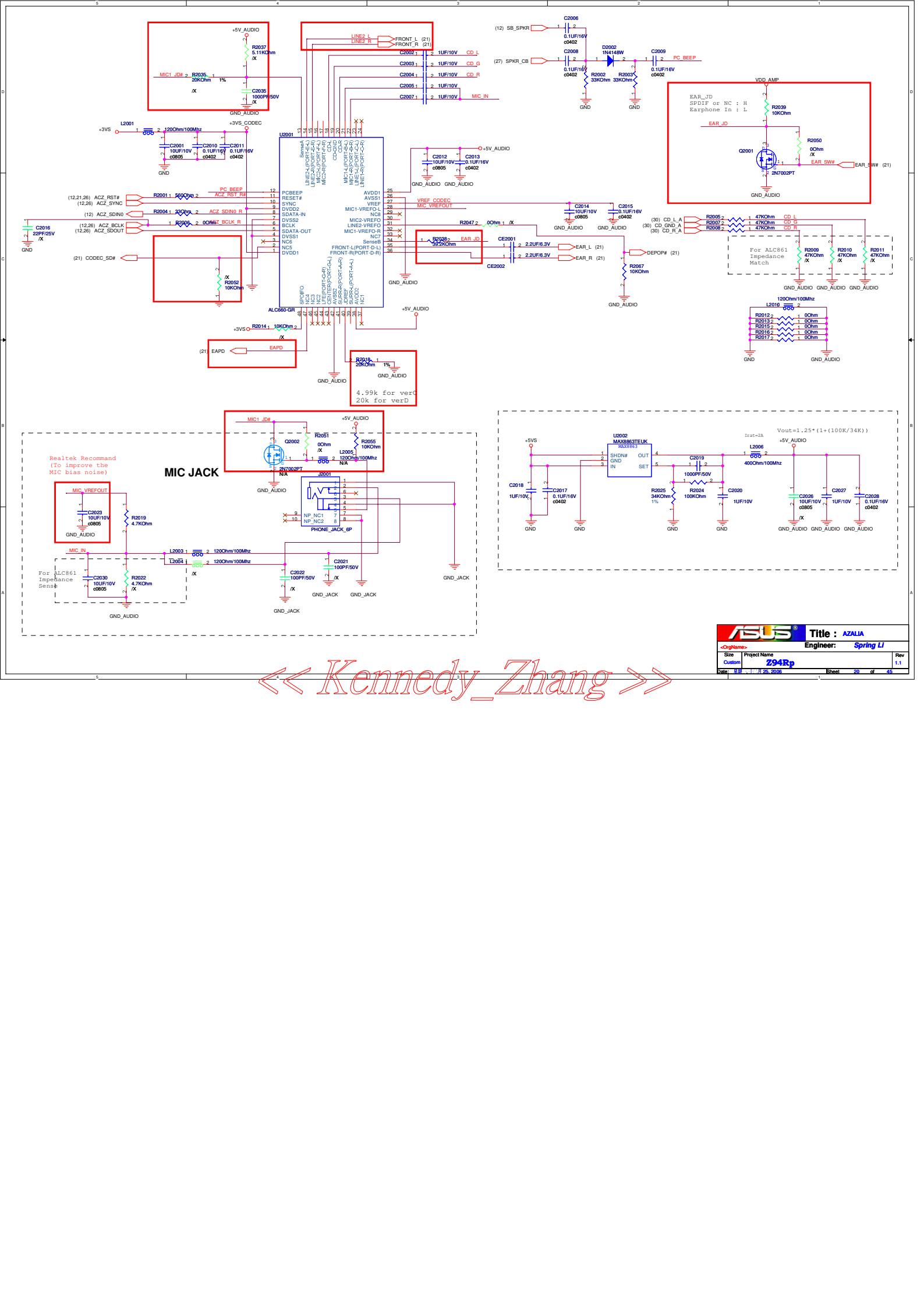
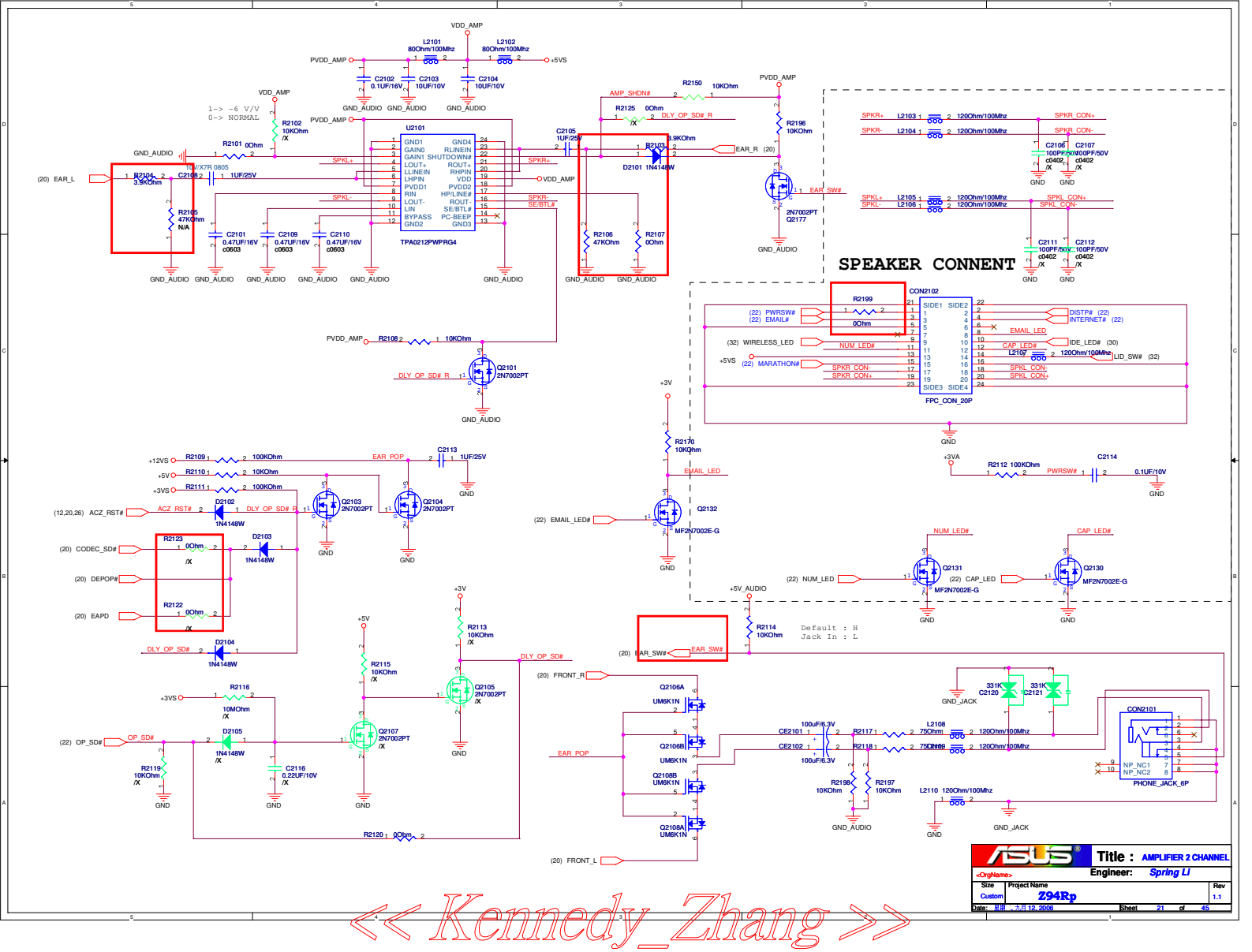
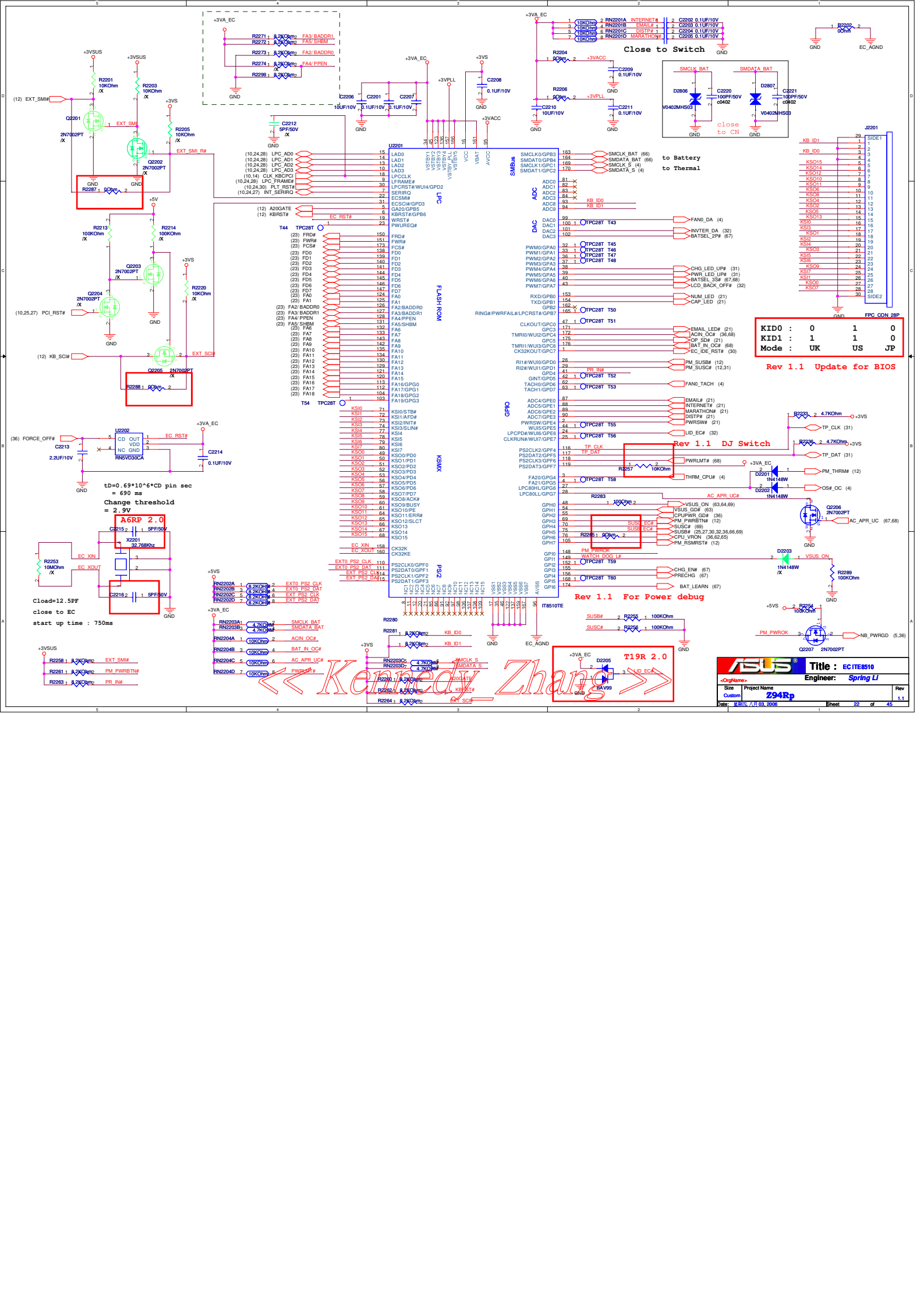
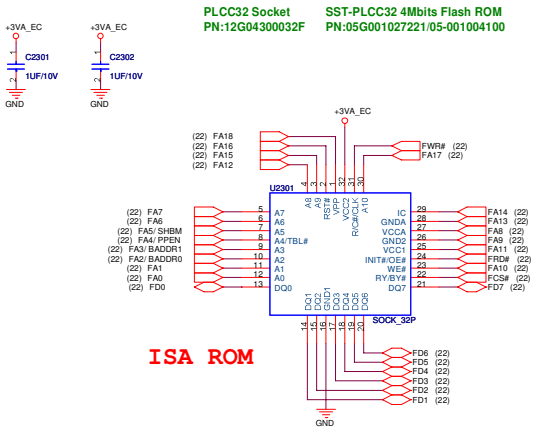
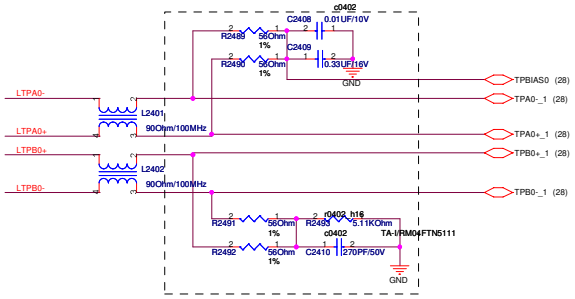


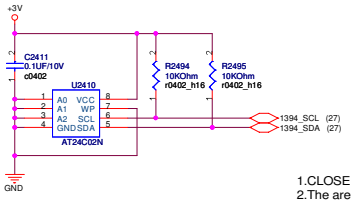

SPEAKER CONNENT
U2101
TPA0212PWPRG4
CON2102
FPC_CON_20P
CON2101
PHONE_JACK_6P
Q2101 2N7002PT
Q2103 2N7002PT
Q2104 2N7002PT
Q2105 2N7002PT
Q2107 2N7002PT
Q2132 MF2N7002E-G
Q2131 MF2N7002E-G
Q2130 MF2N7002E-G
Q2106A UM6K1N
Q2106B UM6K1N
Q2108B UM6K1N
Q2108A UM6K1N
D2101 1N4148W
D2102 1N4148W
D2103 1N4148W
D2104 1N4148W
D2105 1N4148W
Q2177 2N7002PT
Default : H
Jack In : L
Title : AMPLIFIER 2 CHANNEL
Engineer: Spring Li
Project Name 294Rp
Rev 1.1
Sheet 21 of 45
<< Kennedy_Zhang >>

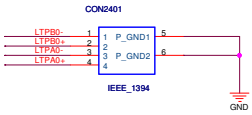

Close to Switch
to Battery
to Thermal
Rev 1.1 Update for BIOS
KID0 : 0 1 0
KID1 : 1 1 0
Mode : UK US JP
Rev 1.1 DJ Switch
Rev 1.1 For Power debug
A6RP 2.0
T19R 2.0
tD=0.69*10^6*CD pin sec
= 690 ms
Change threshold
= 2.9V
Cload=12.5PF
close to EC
start up time : 750ms
Title : EC ITE8510
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 22 of 45
<< Kennedy Zhang >>



Title : ISA ROM & SPI ROM			
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 23 of 45		

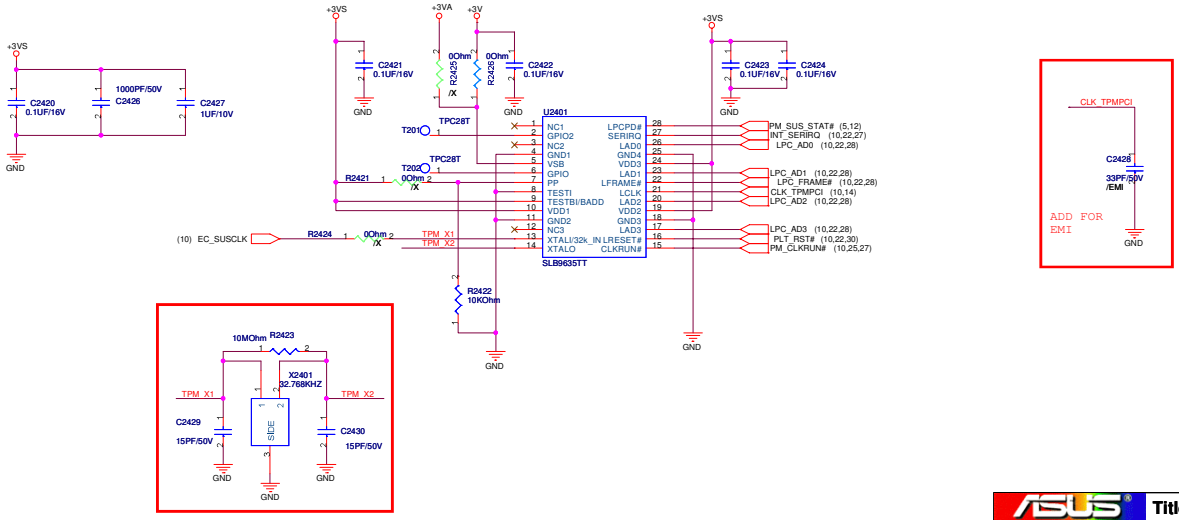






1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

TPM 1.2 function for OEM Customer



ASUS	Title : Blank		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 24 of 45		

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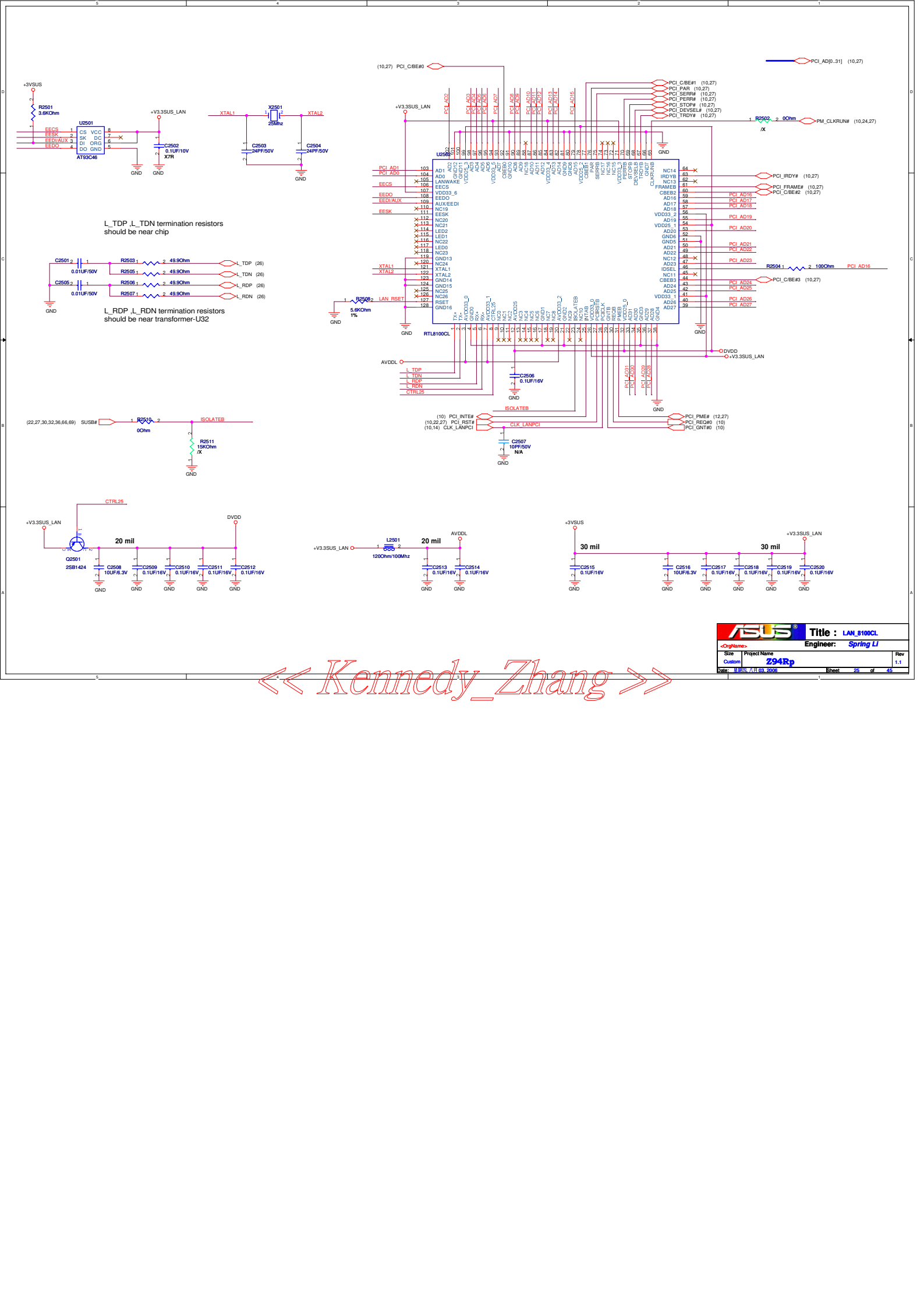

ASUS	Title : LAN_8100CL	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 25 of 45	

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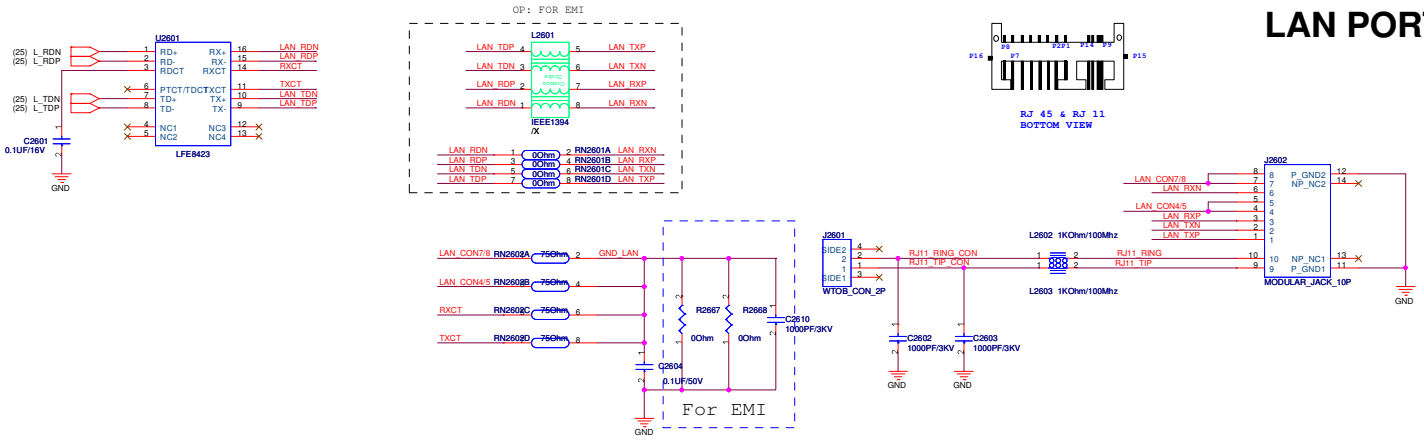
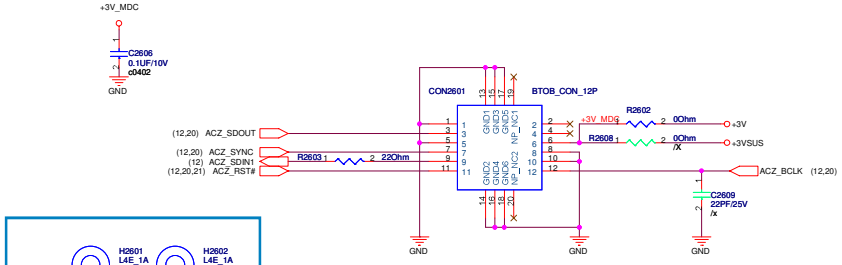
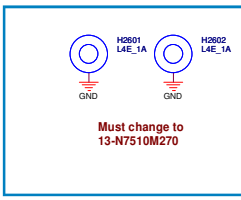
LAN PORT



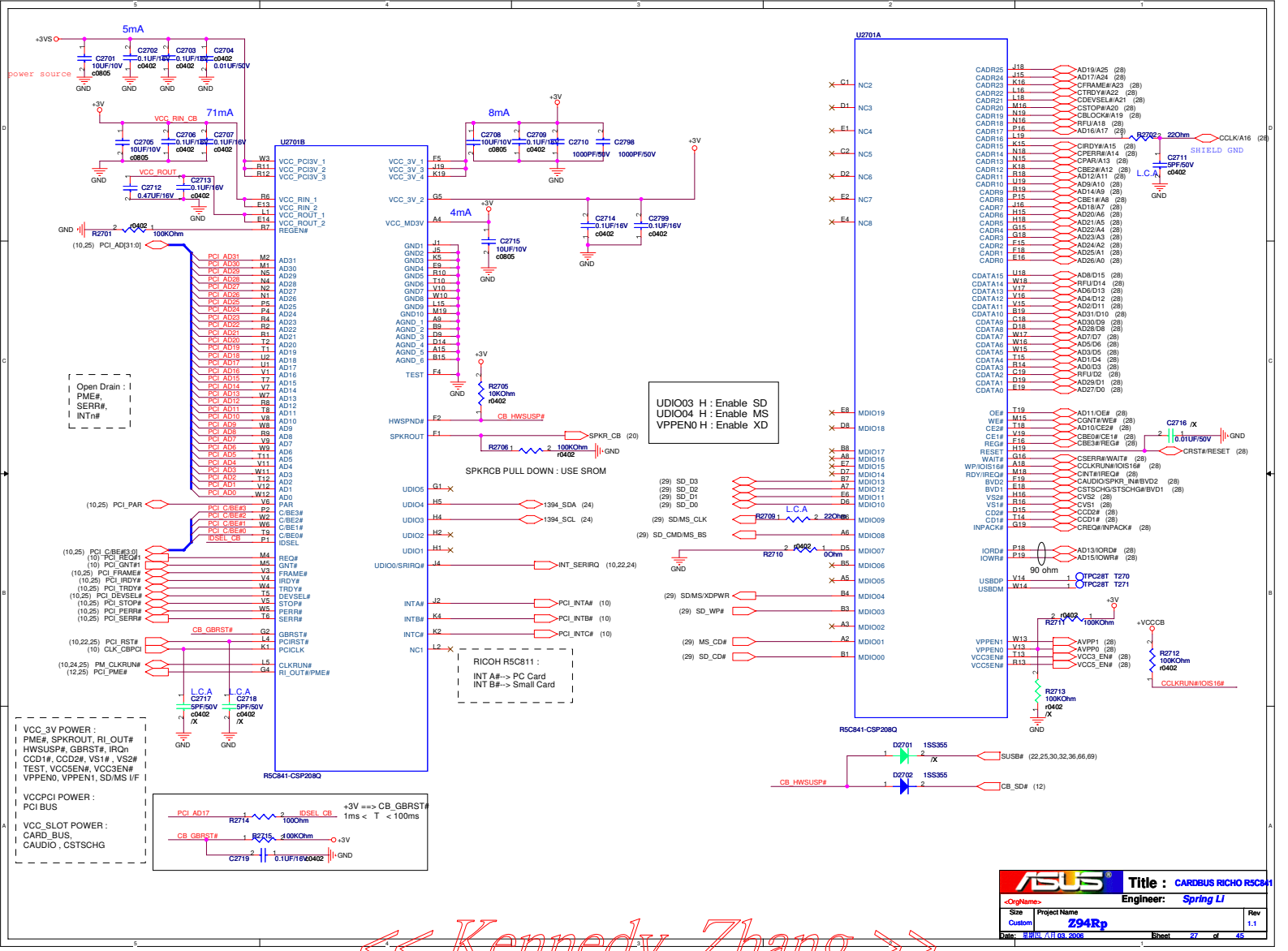
MDC

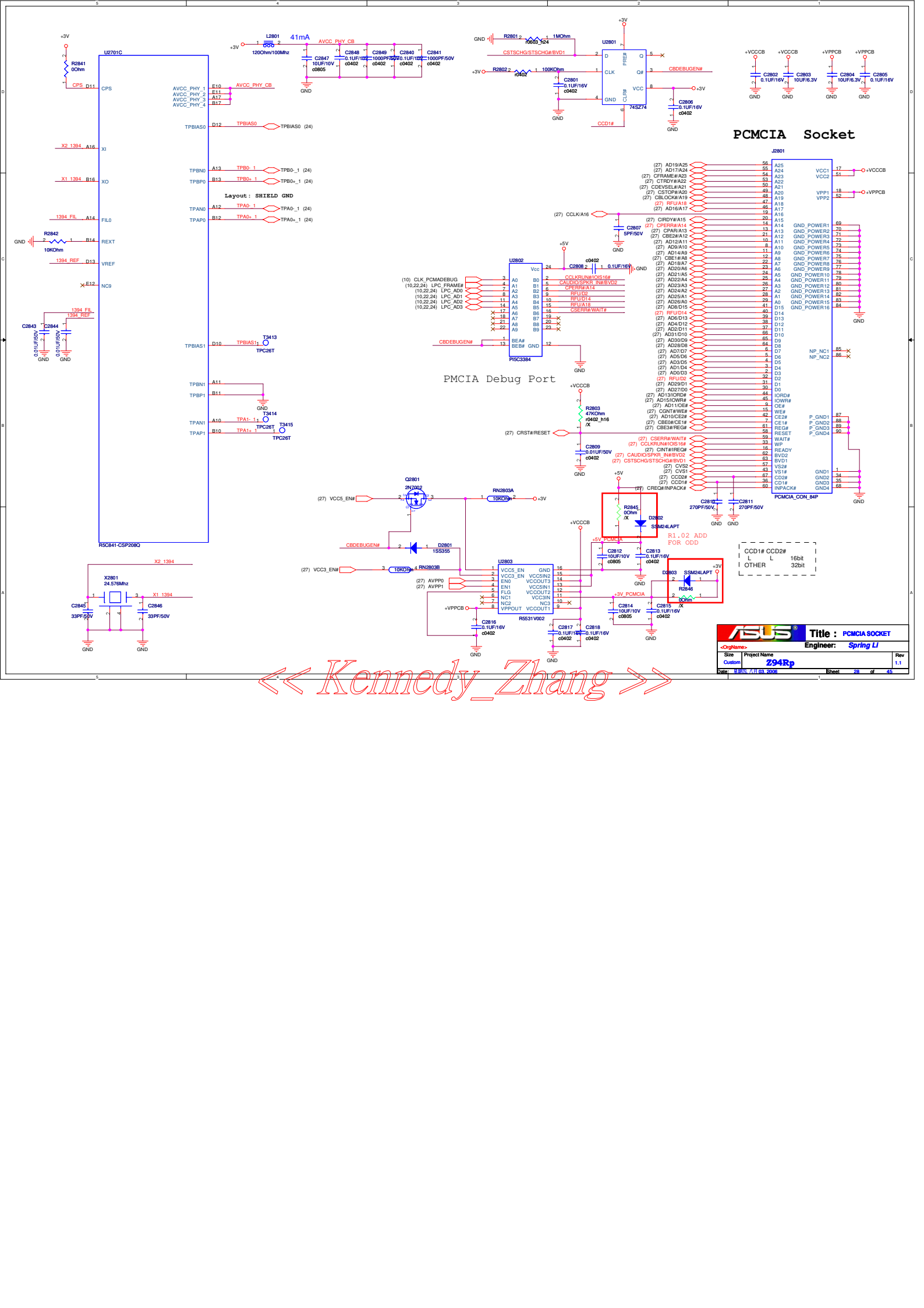




Title : RJ11+45 & MDC			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 26 of 45		

<< Kennedy_Zhang >>

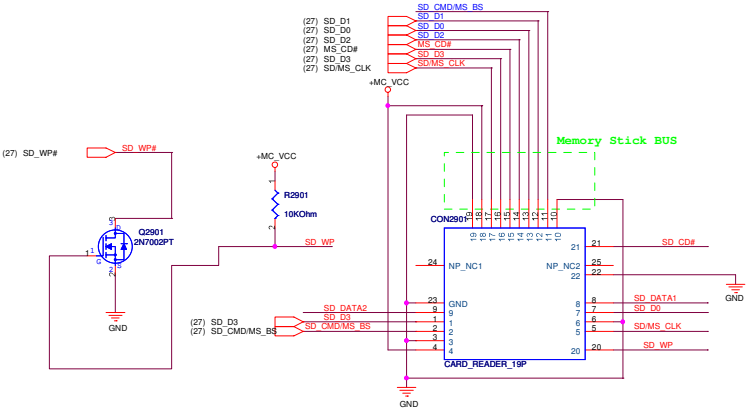


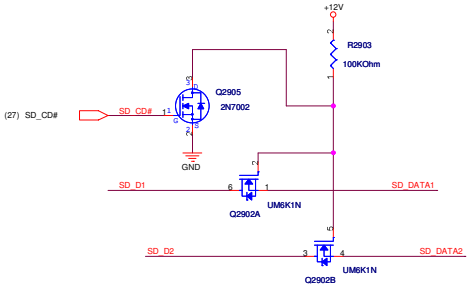

PCMCIA Socket
PMCIA Debug Port
Layout: SHIELD GND
R1.02 ADD FOR ODD
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : PCMCIA SOCKET
Engineer: Spring Li
Project Name Z94Rp
Rev 1.1
Sheet 28 of 45
<< Kennedy_Zhang >>

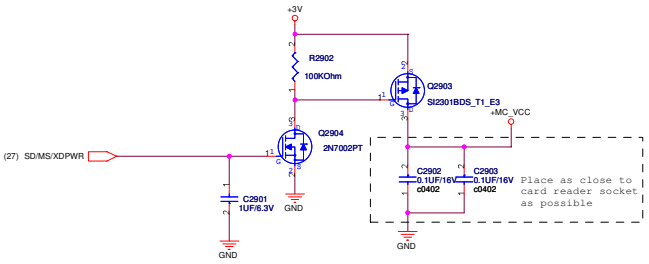
Memory Card Detect

MS_CD#	SD_CD#	
0	0	Not Support
1	0	Small Card
1	1	Memory Stick

MC_CD# : Memory Card Detect

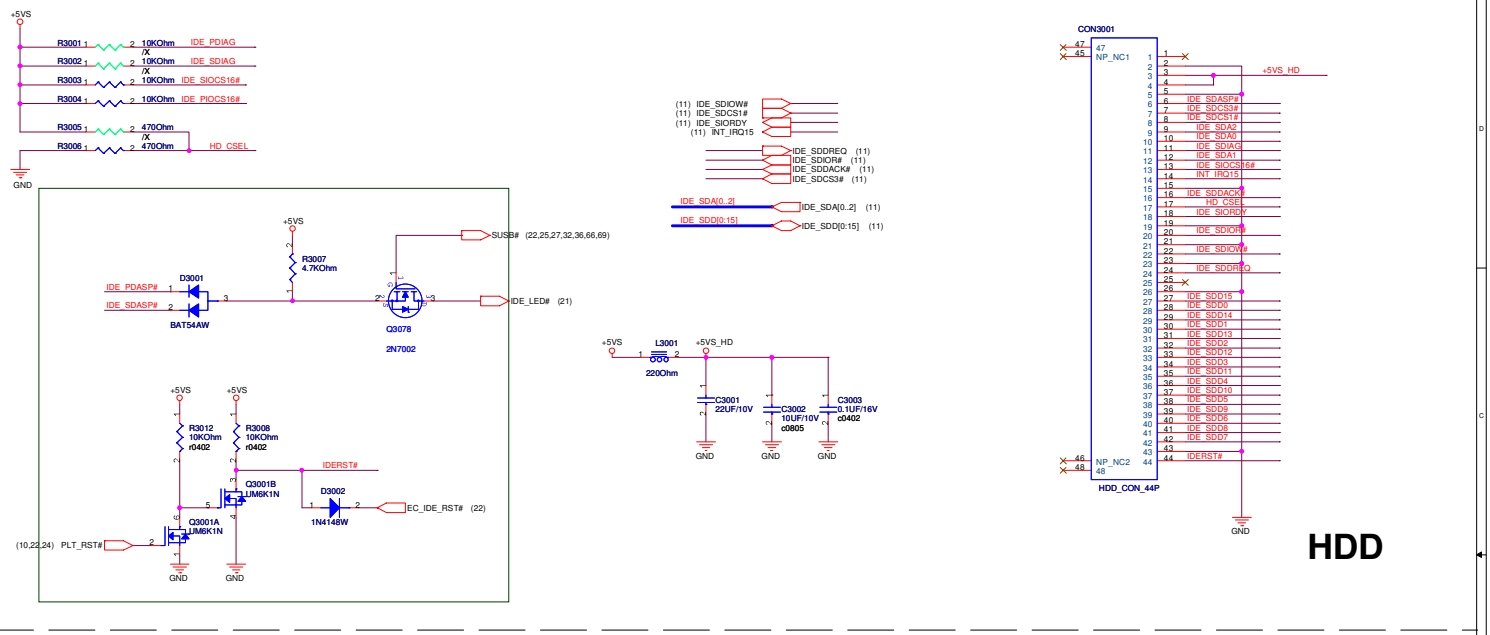




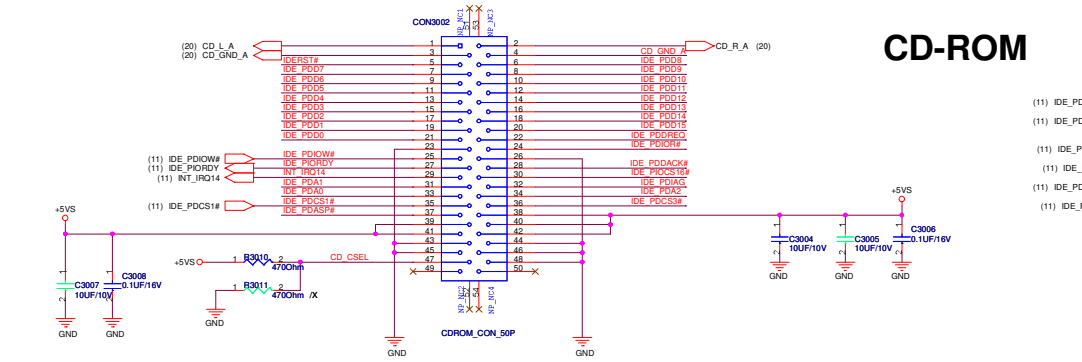


ASUS	Title : 4 IN 1 CON		
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期 二 月 25, 2006	Sheet 29 of 45		

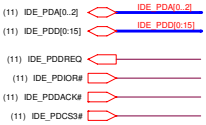
<< Kennedy_Zhang >>



HDD



CD-ROM

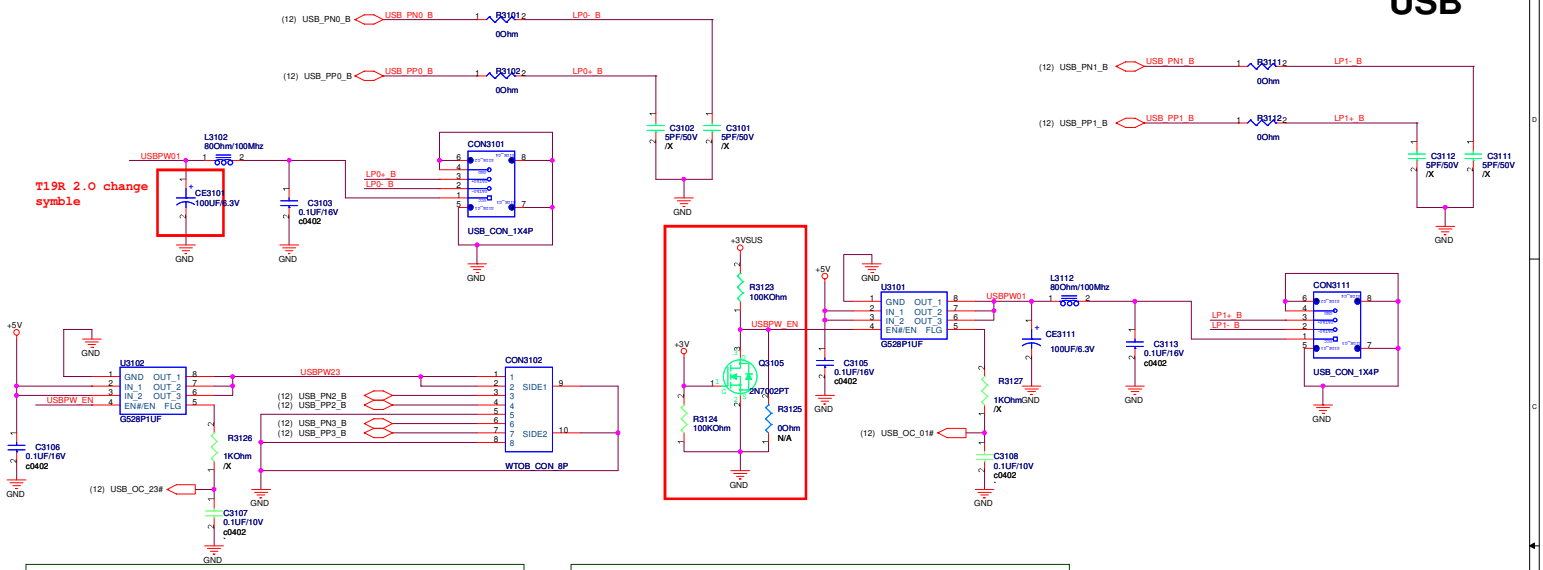


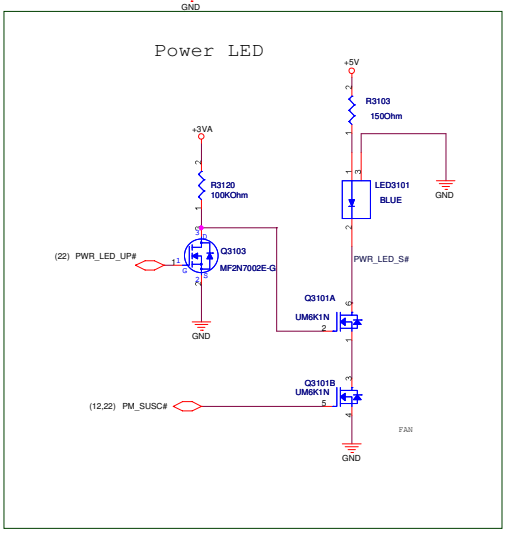
ODD_CSEL : Pull-Up, CDROM as Slave,
Pull-Down, CDROM as Master

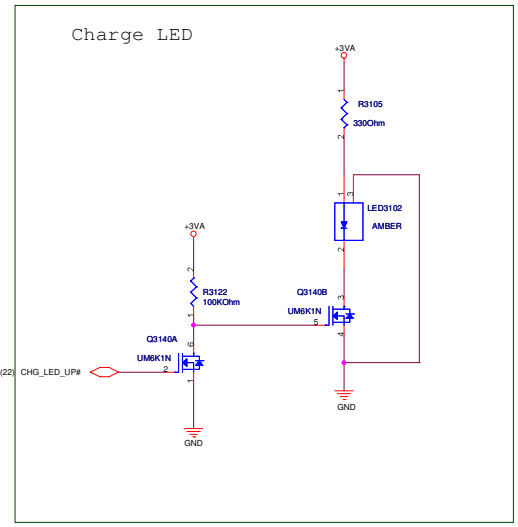
ASUS	Title : HDD & CD-ROM		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 월 19 일 03, 2006	Sheet 30 of 45		

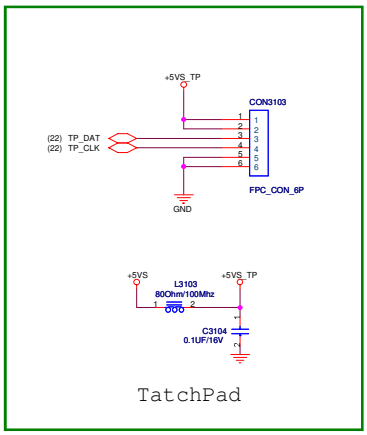
<< Kennedy_Zhang >>

USB



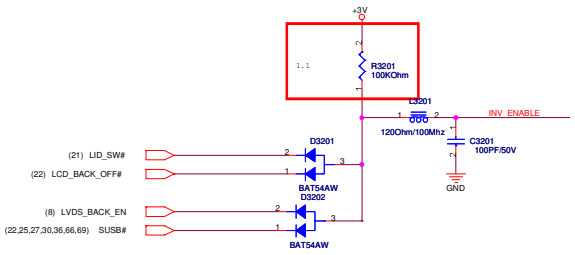




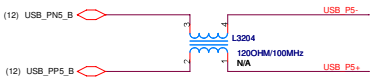


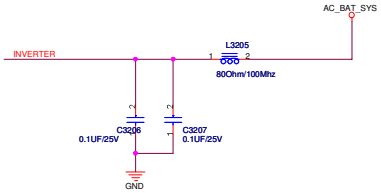
Title : USB / LED / TP			
<OrgName>	Engineer: Spring Li		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 31 of 45		

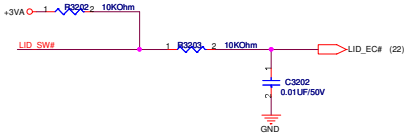
<< Kennedy_Zhang >>



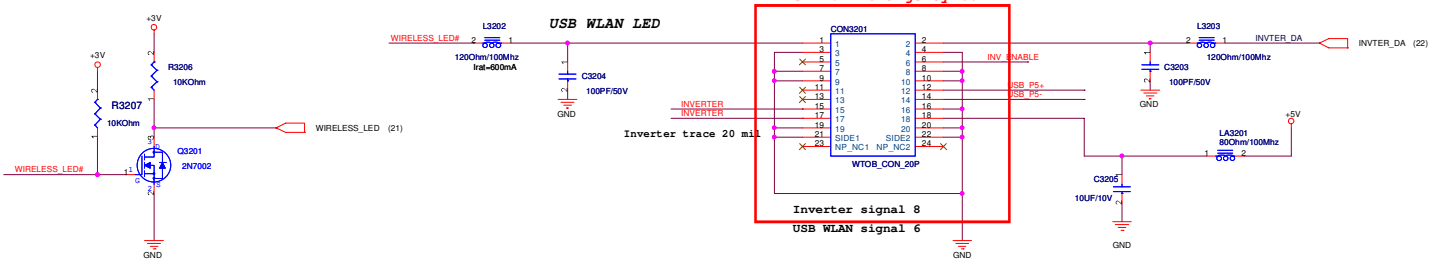
USB WIRESSLEE LAN





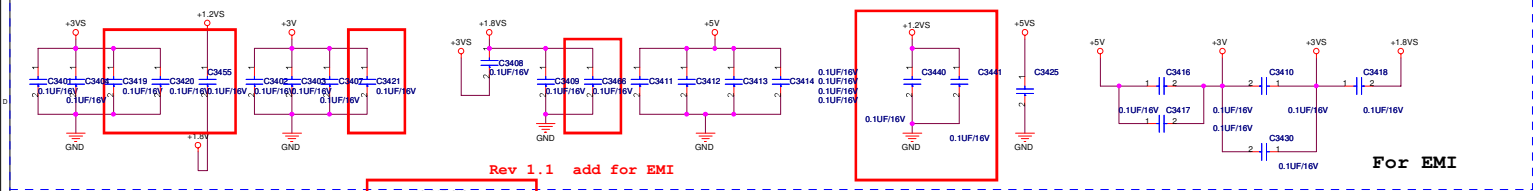


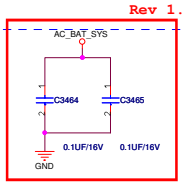
Rev 1.1 Change symbol

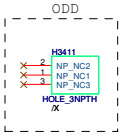


ASUS	Title : FUNCTION KEY & BT	
<OrgName>	Engineer: Spring Li	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 32 of 45	

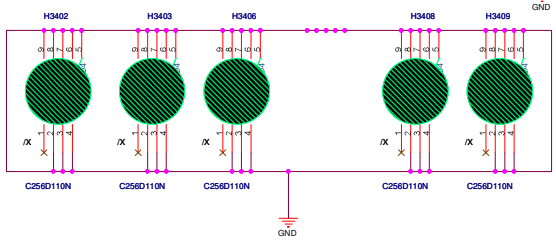
<< Kennedy_Zhang >>

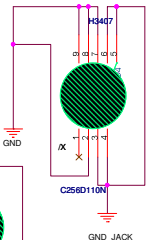




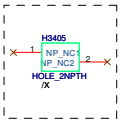


Hole no GND --- A

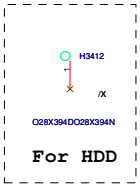




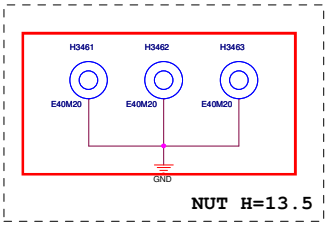
PAD Hole (2hole)--- E



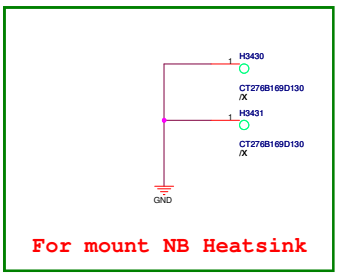
Oblong drill hole



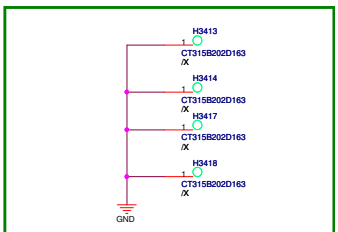
For HDD



NUT H=13.5

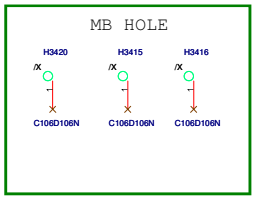


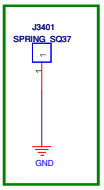
For mount NB Heatsink



For mount CPU spring

PTH Hole

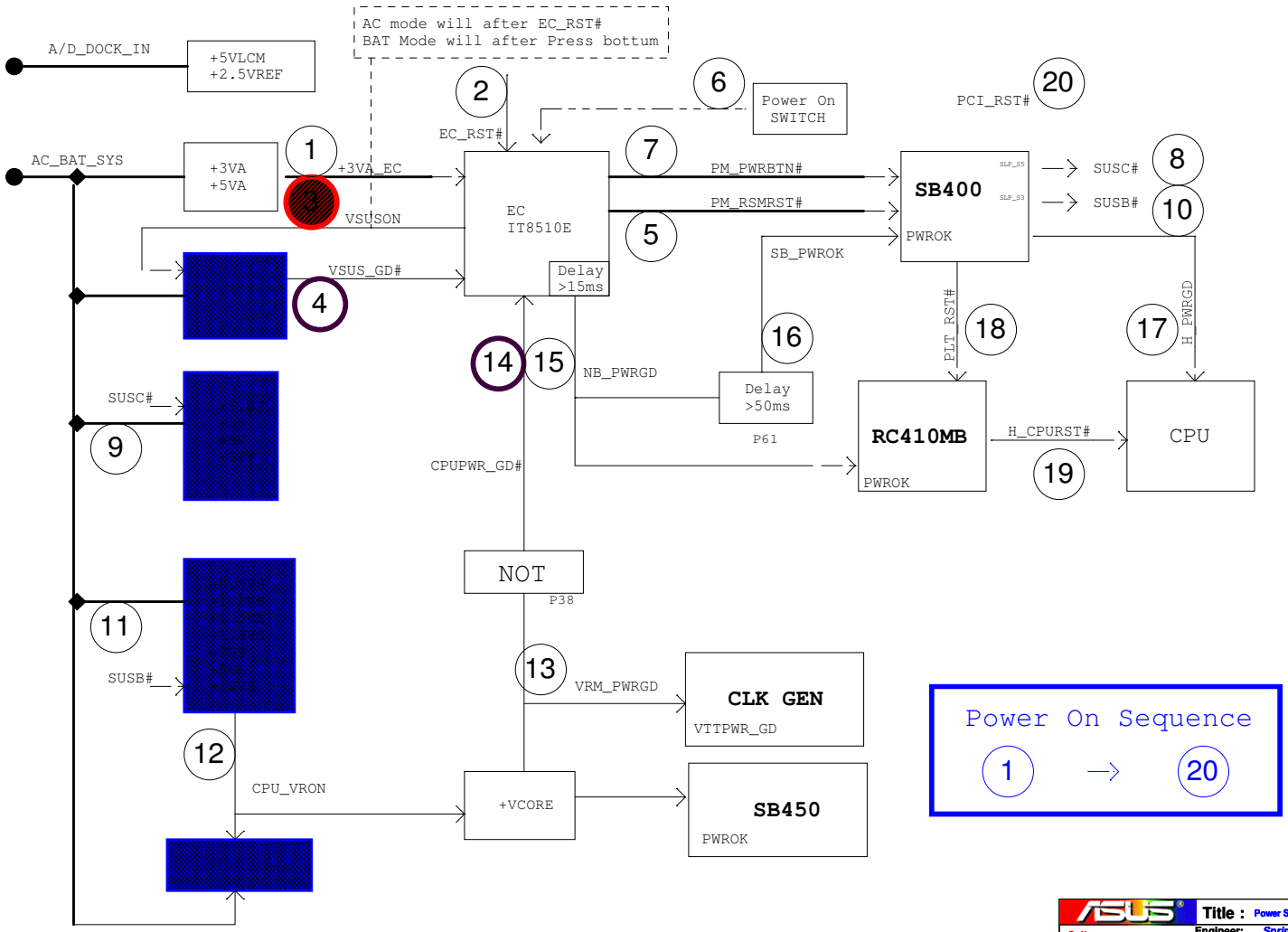




For EMI

ASUS	Title : Hole		
<OrgName>	Engineer: Spring LI		
Size: Custom	Project Name: Z94Rp		Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 33 of 45		

<< Kennedy_Zhang >>



Title : Power Sequence
<OrgName>
Engineer: Spring LI
Size: Custom
Project Name: Z94Rp
Rev: 1.1
Date: 星期四, 七月 13, 2006
Sheet 34 of 45

<< Kennedy_Zhang >>

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 LAN	AD16	0	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	A

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

SB400 GPIO TABLE

GPIO	TYPE	POWER DOMAIN	FUNCTION
GPIO 0	I/OD	S0	
GPIO 1	I/O	S0	
GPIO 2	I/O	S0	SB_SPKR
GPIO 3	I/O	S0	
GPIO 4	I/O	S0	PCB_ID0
GPIO 5	I/O	S0	PCB_ID1
GPIO 6	I/OD	S0	PCB_ID2
GPIO 7	I/O	S0	VRM_PWRGD
GPIO 8	I/O	S0	CB_SD#
GPIO 9	I/O	S0	BACK_OFF#
GPIO 10	I/O	S5	SB_PM_THERM#
GPIO 11	I/O	S0	
GPIO 12	I/O	S0	
GPIO 13	I/O	S0	
GPIO 14	I/O	S0	PCI_GNT#5
GPIO 31	I/O	S0	
GPIO 32	I/O	S0	PCI_GNT#6
GPIO 33	I/O	S0	PCI_INTE#
GPIO 34	I/O	S0	PCI_INTF#
GPIO 35	I/O	S0	PCI_INTG#
GPIO 36	I/O	S0	PCI_INTH#
GPM 0	I	S5	
GPM 1	I	S5	
GPM 2	I/O	S5	
GPM 3	I	S5	
GPM 4	I	S5	
GPM 5	I	S5	
GPM 6	I/OD	S5	PWRLED_1HZ
GPM 7	I	S5	SYS_RESET#
GEVENT 0	I	S5	
GEVENT 1	I	S0	
GEVENT 2	I	S5	THRMTRIP#
GEVENT 3	I	S5	LPC_PME#
GEVENT 4	I	S5	PCI_PME#
GEVENT 5	I	S5	H_PROCHOT#
GEVENT 6	I	S5	
GEVENT 7	I	S5	
GEVENT 8			KB_SCI
EXTEVENT#0			EXT_SMI#
EXTEVENT#1			SIO_SMI#

KBC GPIO	W1V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	LID_EC#	
P20(Pin 38)	KBCRSM	
P42(Pin 23)		
P43(Pin 22)	OP_SD#	
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI#	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID0	
P52(Pin 15)	KID1	
P53(Pin 14)		
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)		
P57(Pin 10)	INV_DA	
P67(Pin 74)		
P66(Pin 75)		
P65(Pin 76)	GAIN_AMP_K#	0->>6 V/V 1->>NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)		
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

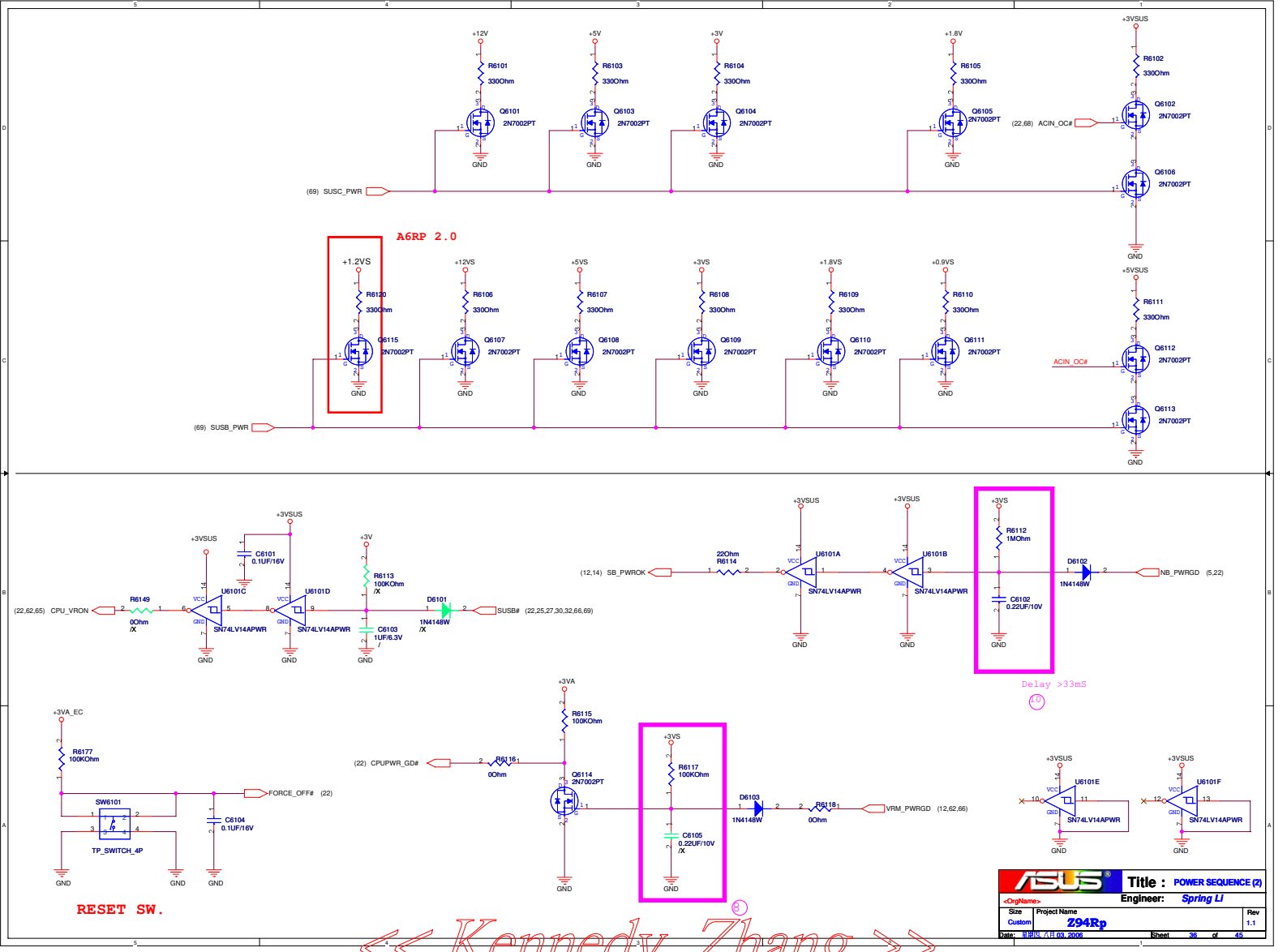
ASUS Title : SYSTEM RESOURCE

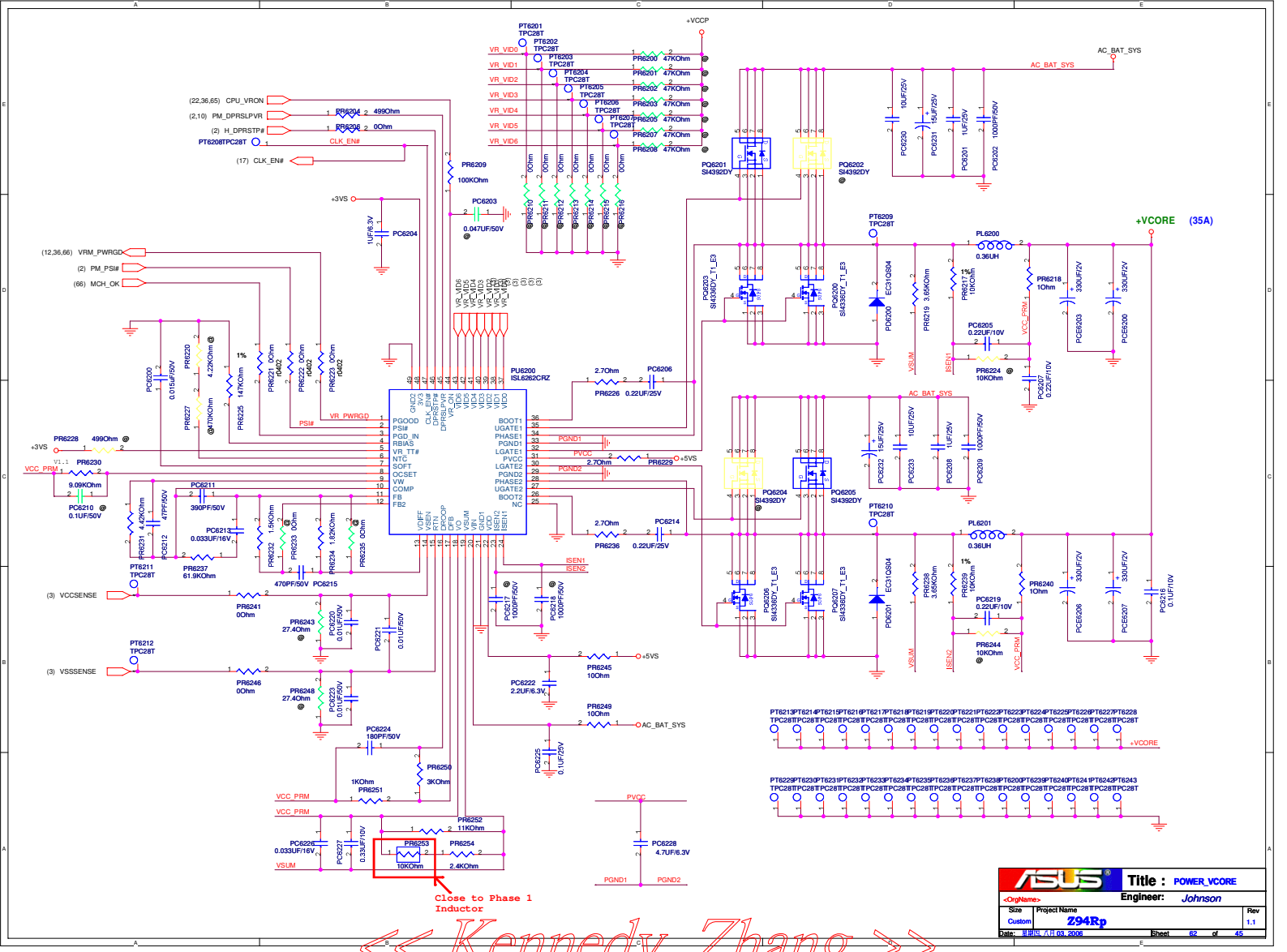
<OrgName> Engineer: Spring LI

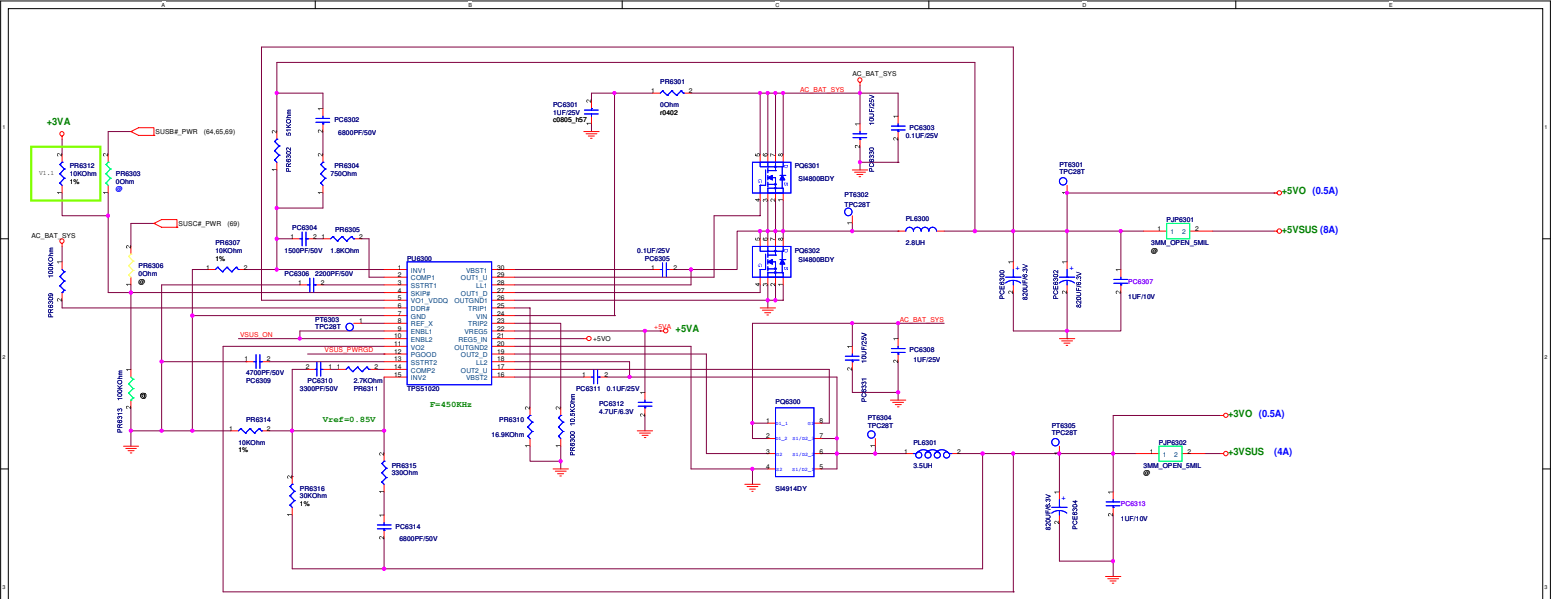
Size	Project Name	Rev
Custom	Z94Rp	1.1

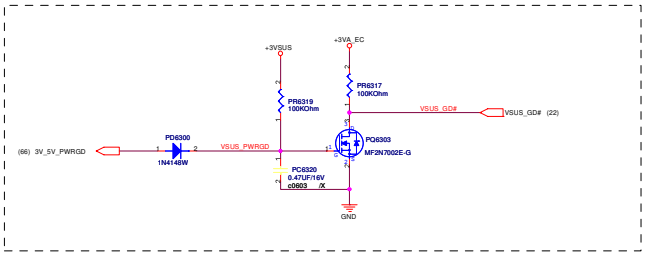
Date: 星期二, 六月 24, 2008 Sheet 35 of 45

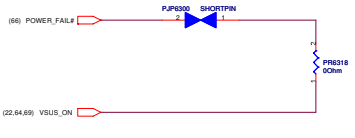
<< Kennedy_Zhang >>

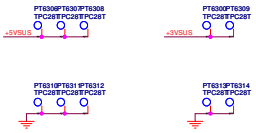


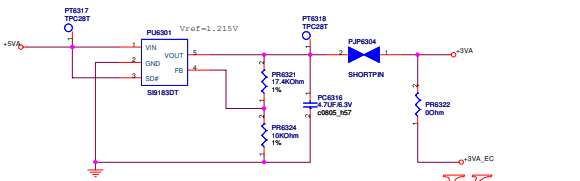

+VCCP
AC_BAT_SYS
+VCORE (35A)
PU6200 ISL6262CRZ
PQ6201 SI4392DY
PQ6202 SI4392DY
PQ6203 SI4362DY_T1_E3
PQ6200 SI4336DY_T1_E3
PQ6204 SI4392DY
PQ6205 SI4392DY
PQ6206 SI4336DY_T1_E3
PQ6207 SI4336DY_T1_E3
PD6200 EC31QS04
PD6201 EC31QS04
PL6200 0.36UH
PL6201 0.36UH
PT6201 TPC28T
PT6202 TPC28T
PT6203 TPC28T
PT6204 TPC28T
PT6205 TPC28T
PT6206 TPC28T
PT6207 TPC28T
PT6208TPC28T
PT6209 TPC28T
PT6210 TPC28T
PT6211 TPC28T
PT6212 TPC28T
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
(22,36,65) CPU_VRON
(2,10) PM_DPRSLPVR
(2) H_DPRSTP#
CLK_EN#
(17) CLK_EN#
(12,36,66) VRM_PWRGD
(2) PM_PSI#
(66) MCH_OK
VR_PWRGD
PSI#
+3VS
VCC_PRM
(3) VCCSENSE
(3) VSSSENSE
VSUM
ISEN1
ISEN2
PGND1
PGND2
PVCC
VCC_PRM1
Close to Phase 1 Inductor
Title : POWER_VCORE
Engineer: Johnson
Project Name Z94Rp
Rev 1.1
Sheet 62 of 45
<< Kennedy_Zhang >>

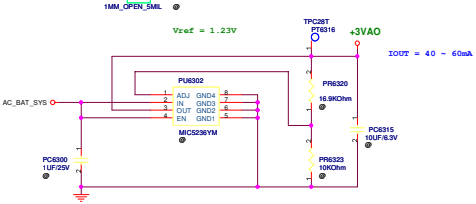












ASUS	Title : SYSTEM_+5VA & +3VA		
<OrgName>	Engineer: Johnson		
Size: C	Project Name: Z94Rp		Rev: 1.1
Date: 四月 八日 03, 2006	Sheet 63 of 45		

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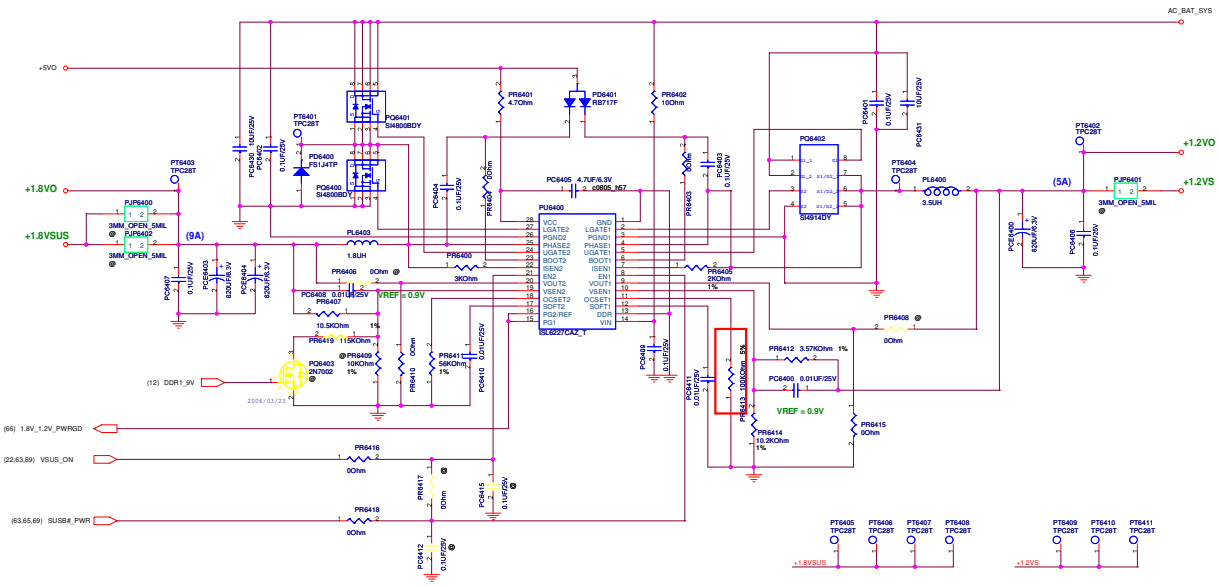

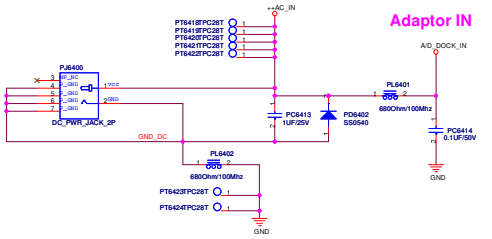

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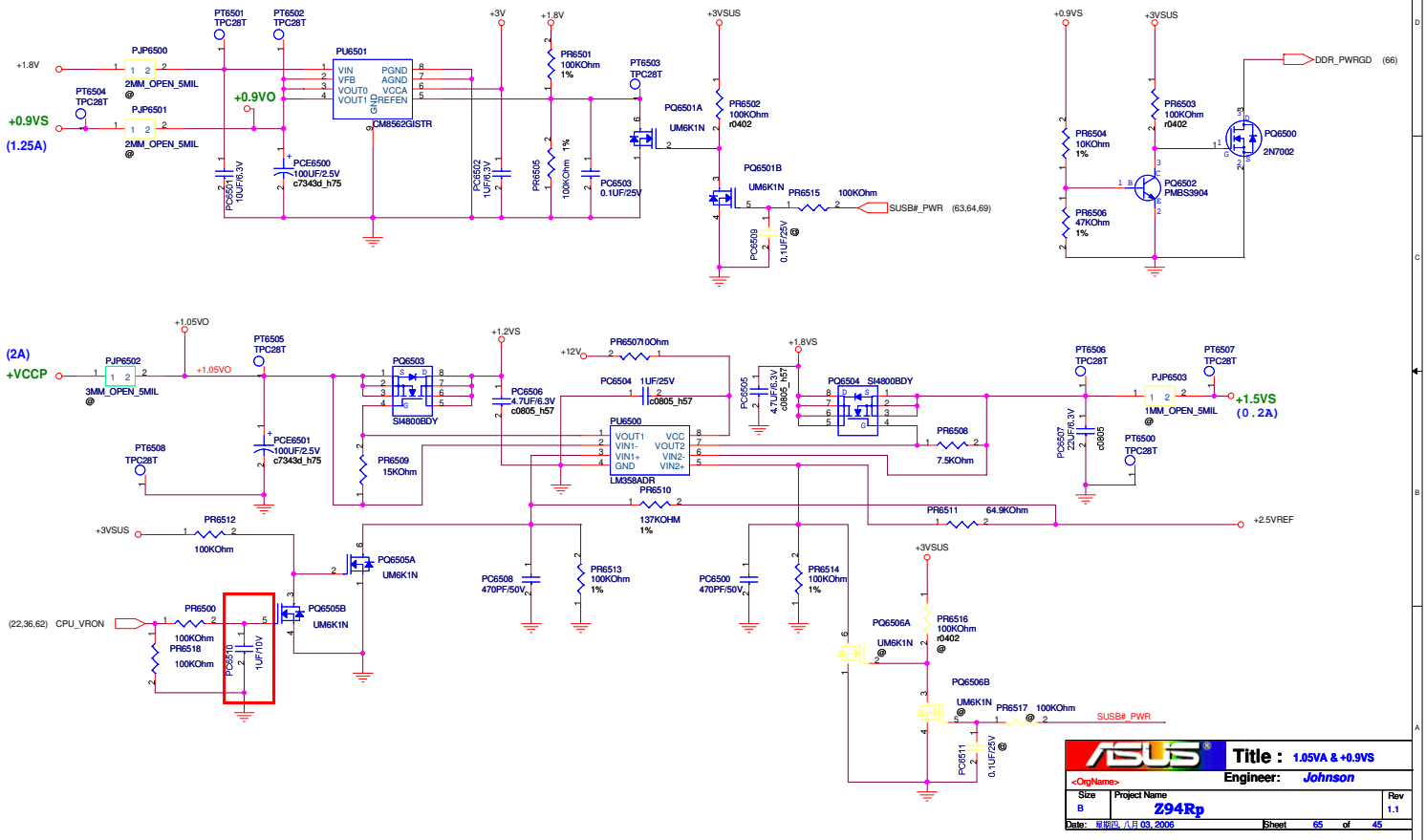
Title : 1.8V&1.2VS			
<OrgName>	Engineer: Johnson		
Size: C	Project Name: Z94Rp		Rev: 1.1
Date: 星期二, 八月 03, 2006	Sheet 64 of 65		



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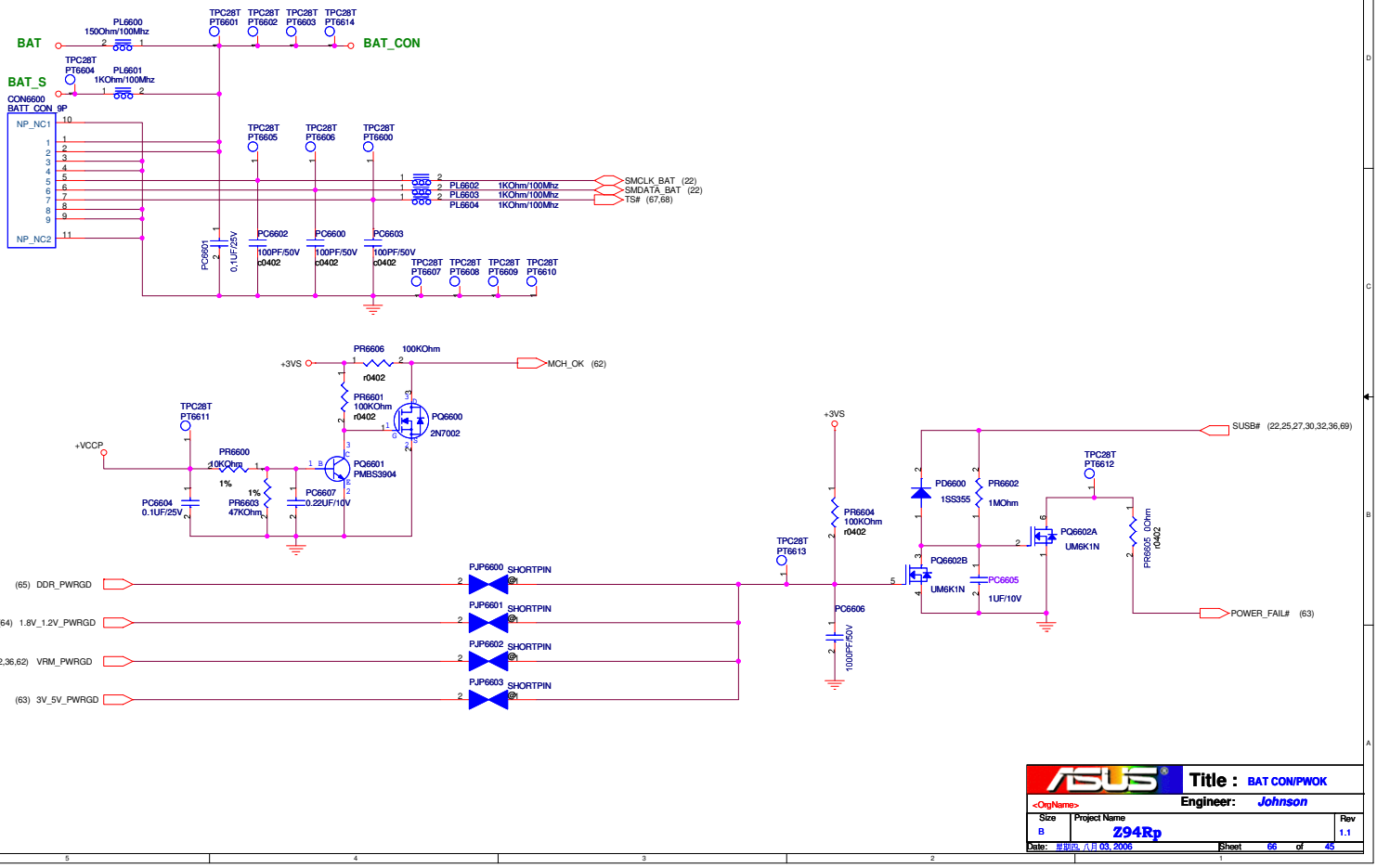

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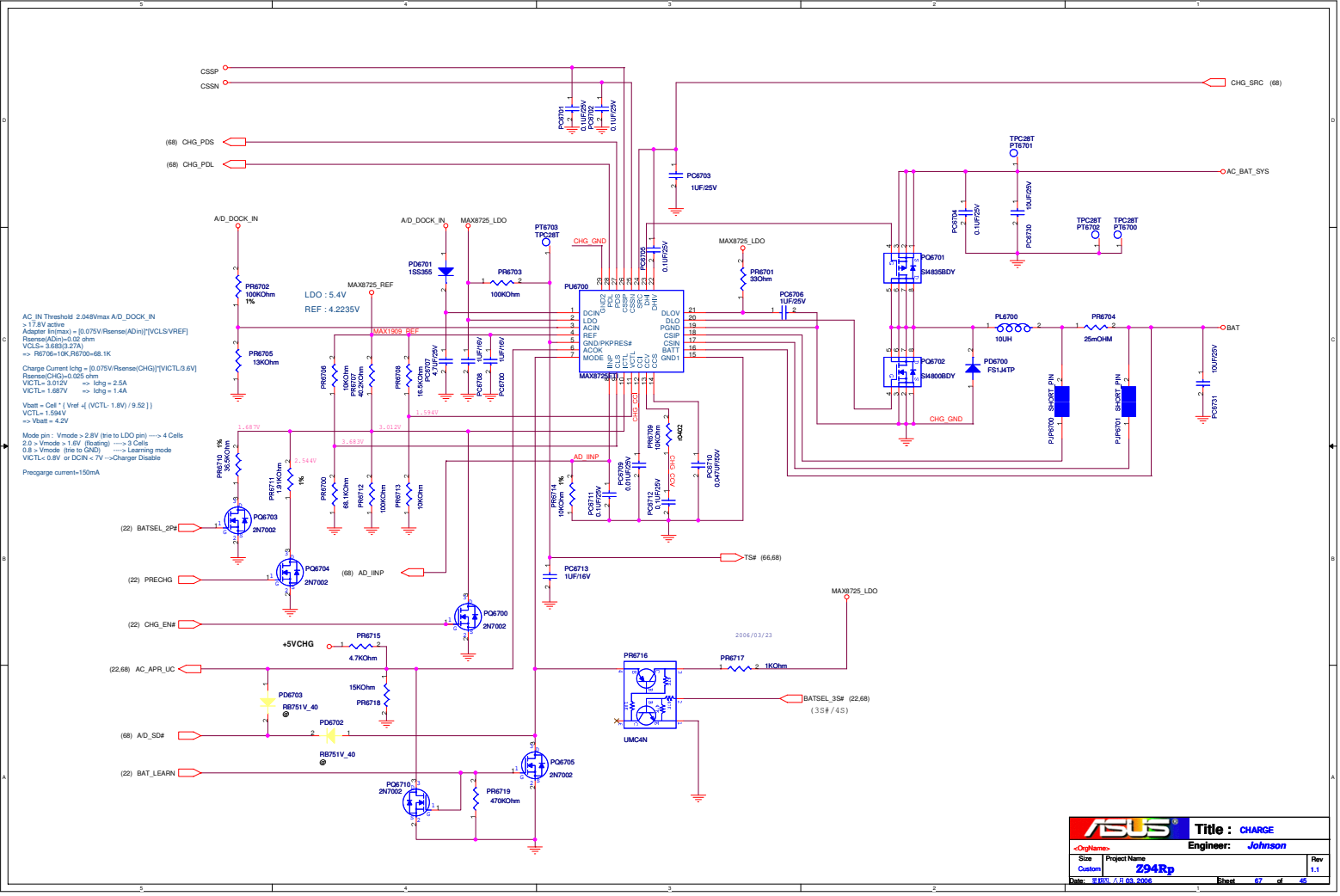

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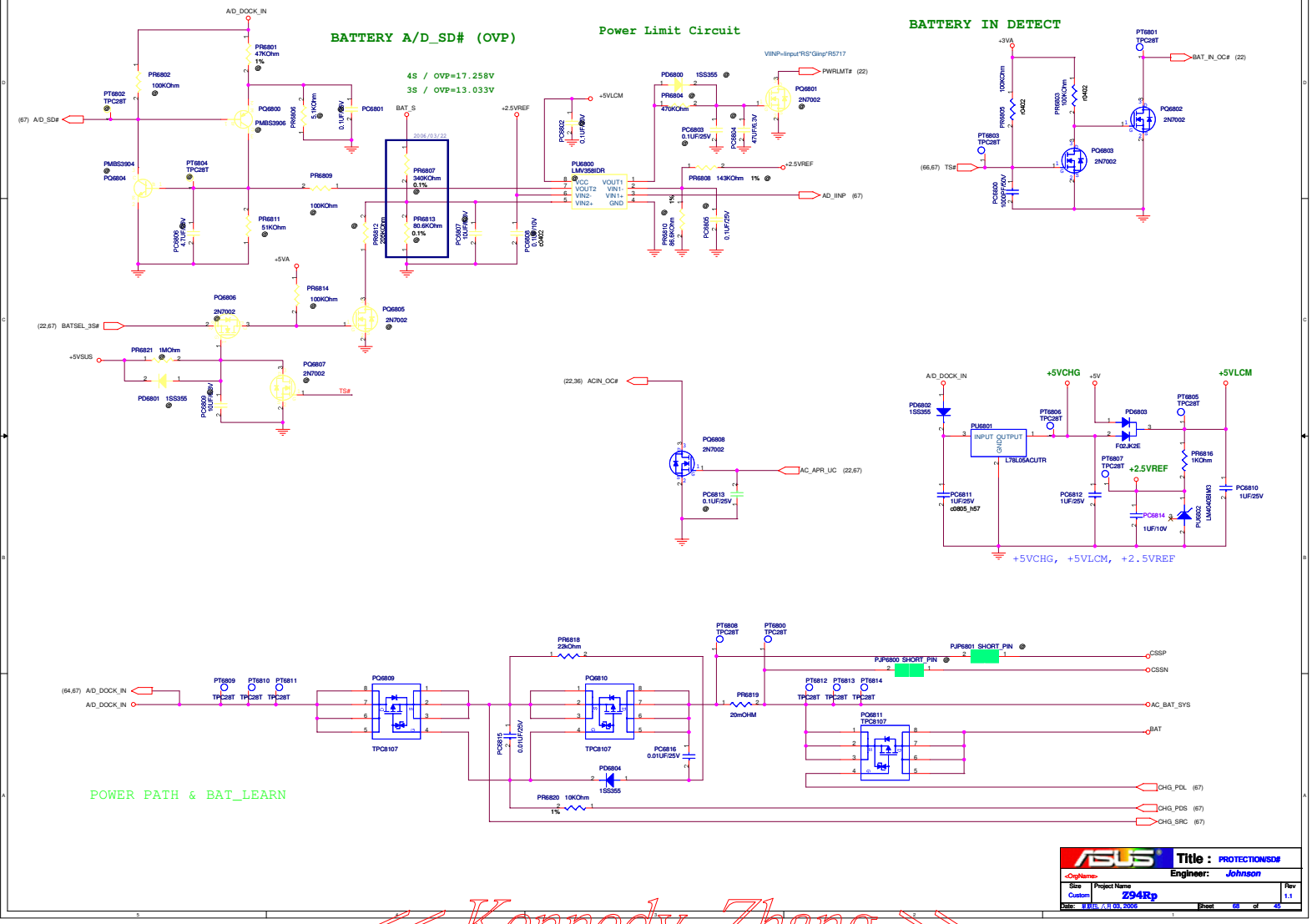

Title :	PROTECTION/SD#		
<OrgName>	Engineer:	Johnson	
Size	Project Name		Rev
Custom	Z94Rp		1.1
Date: 星期六, 03. 2006	Sheet	68	of 45

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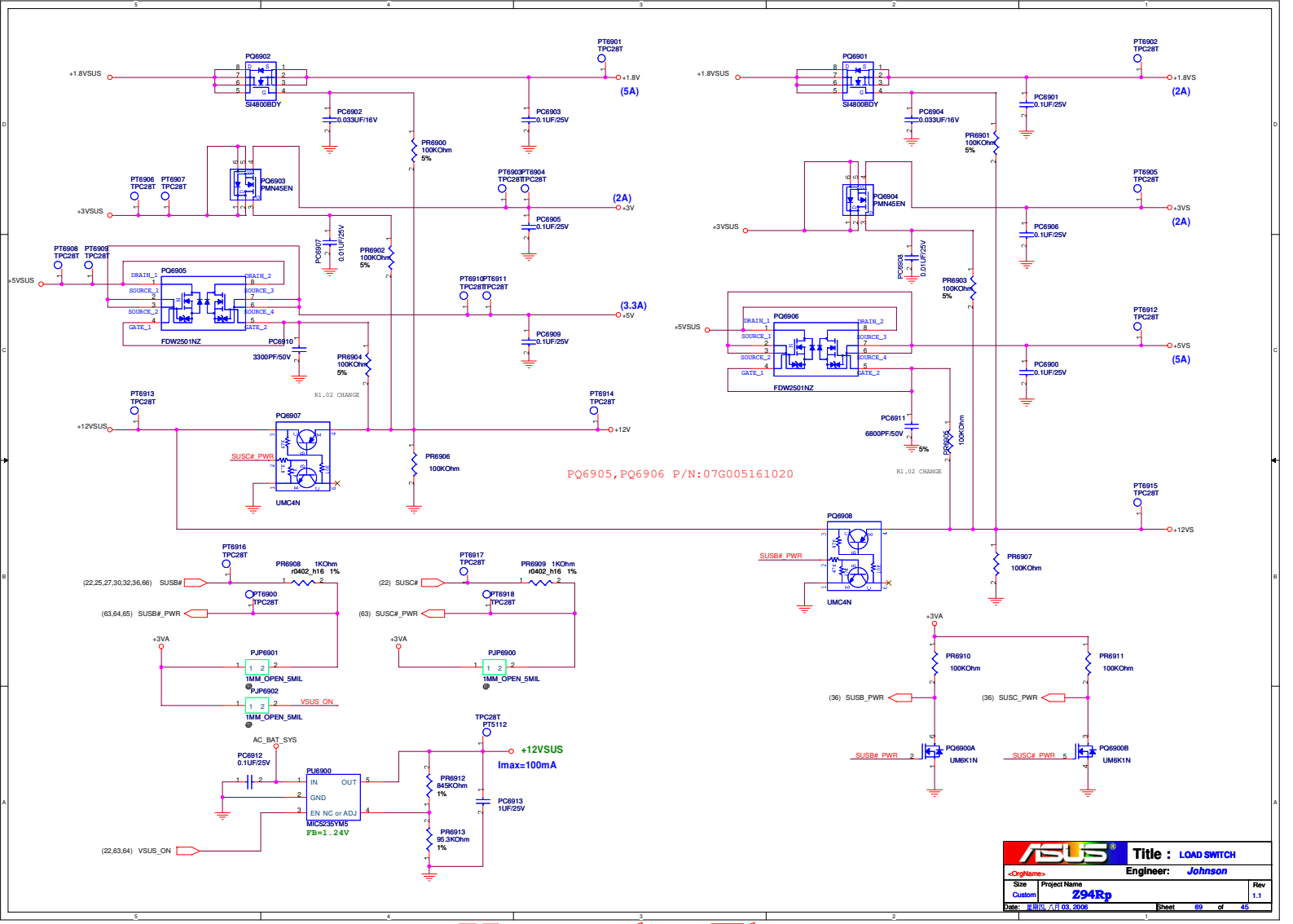

ASUS	Title : LOAD SWITCH	
<OrgName>	Engineer: Johnson	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期四, 八月 03, 2006	Sheet 69 of 45	

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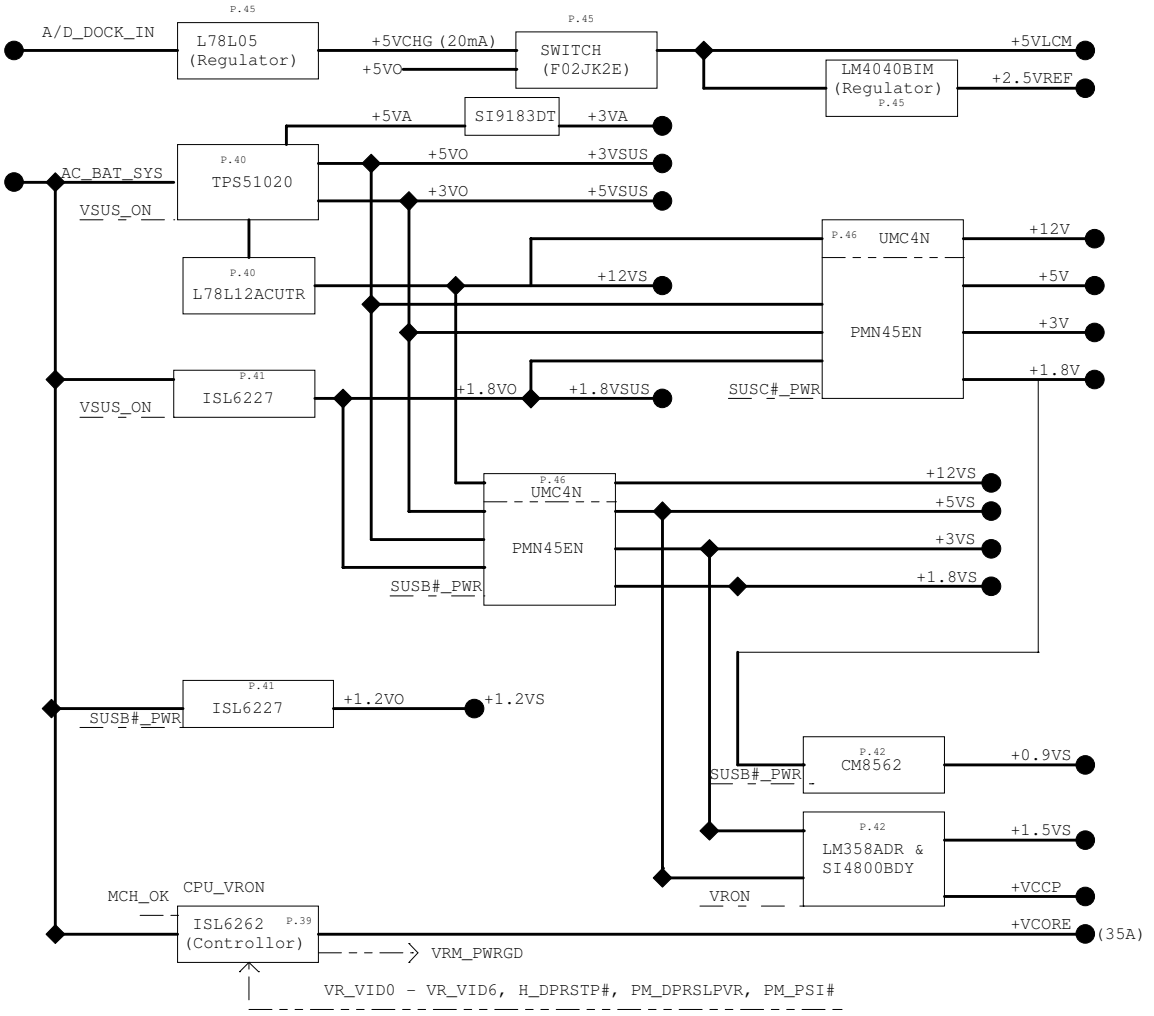

<OrgName>	Title : POWER BLOCK DIAGRAM	
	Engineer: Johnson	
Size: Custom	Project Name: Z94Rp	Rev: 1.1
Date: 星期二, 六月 24, 2008	Sheet 70 of 45	

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