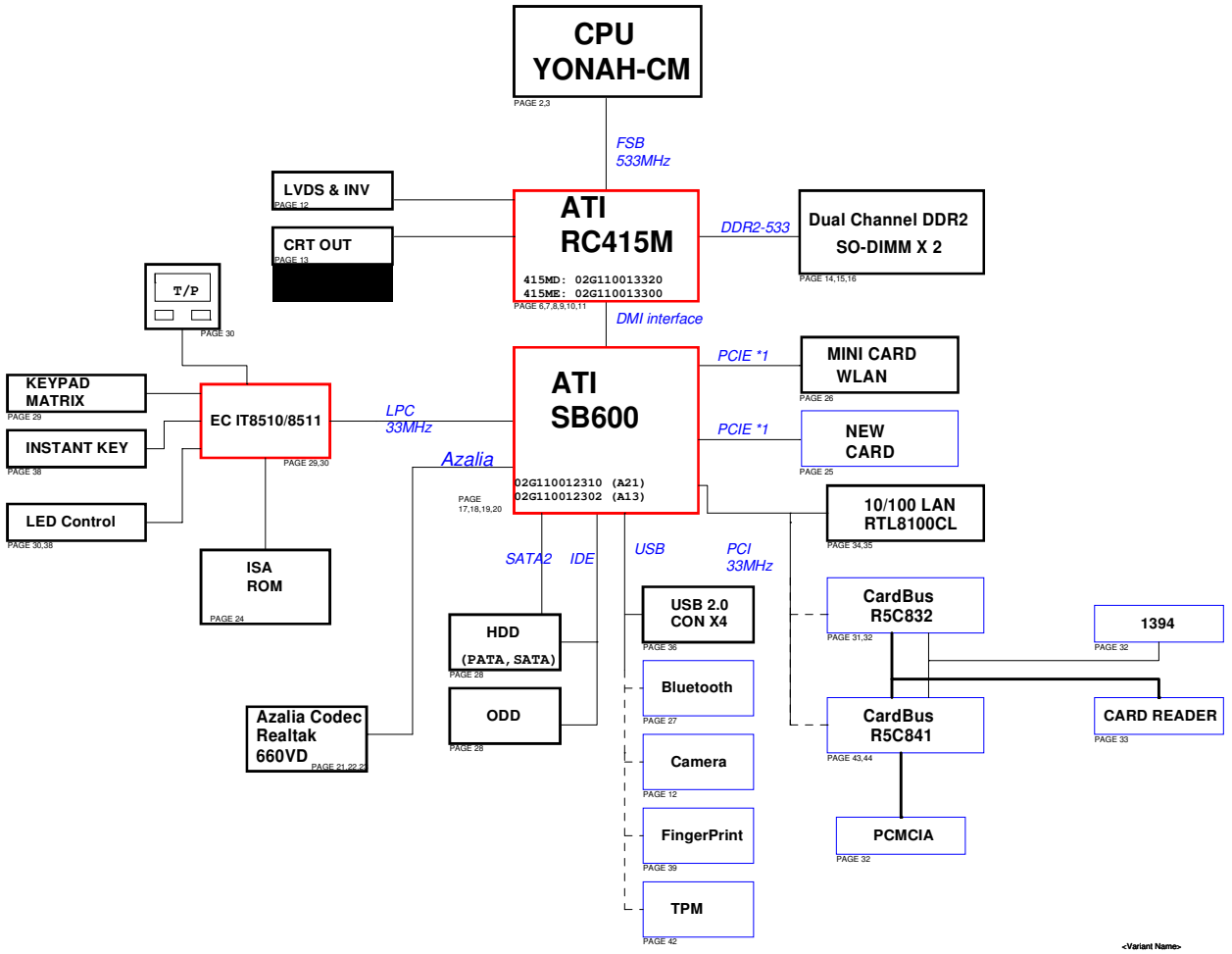
T12R Serier Block Diagram



<Variant Name>

Title : BLOCK DIAGRAM

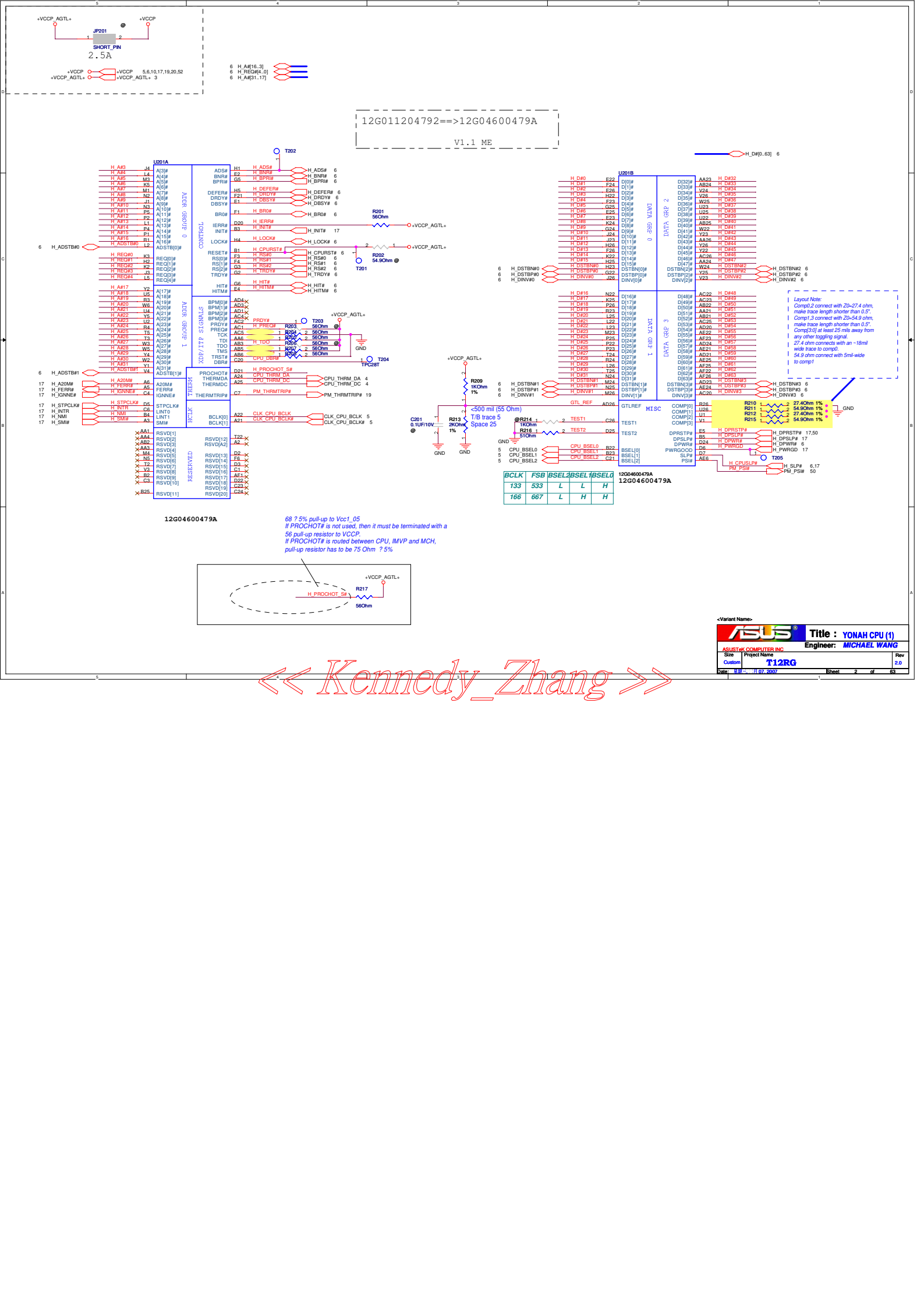
ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

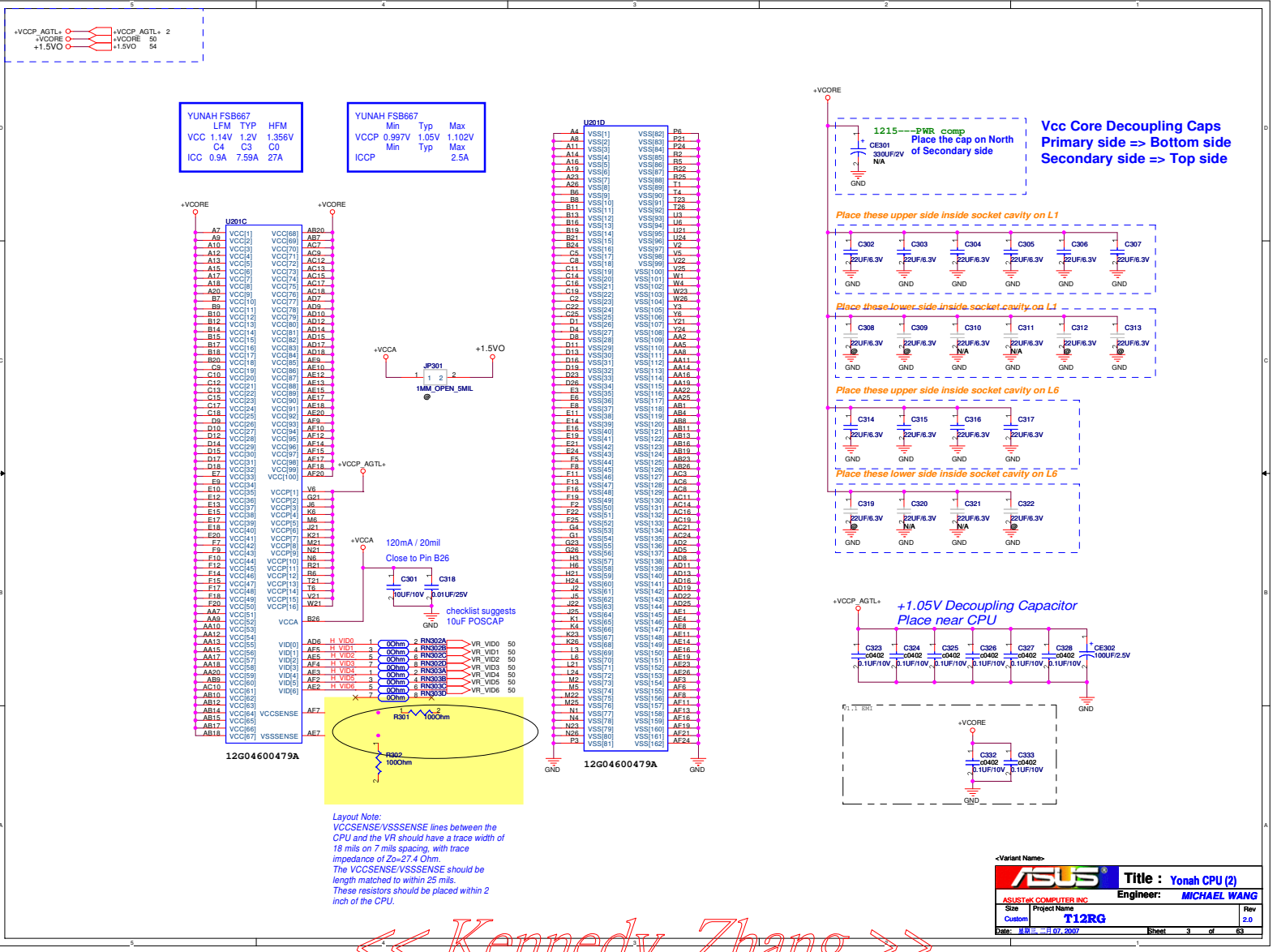
Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 1 of 63

<< Kennedy_Zhang >>



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



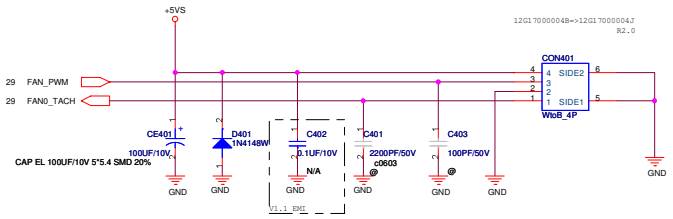
<< Kennedy_Zhang >>

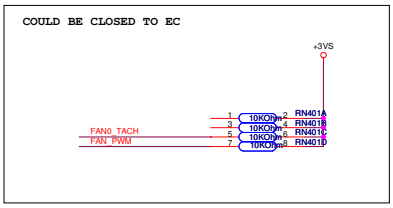
+5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS 5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

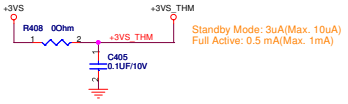
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



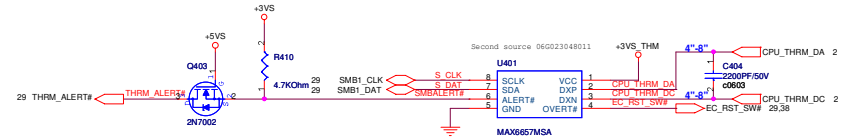




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



<Variant Name>

ASUSTeK COMPUTER INC

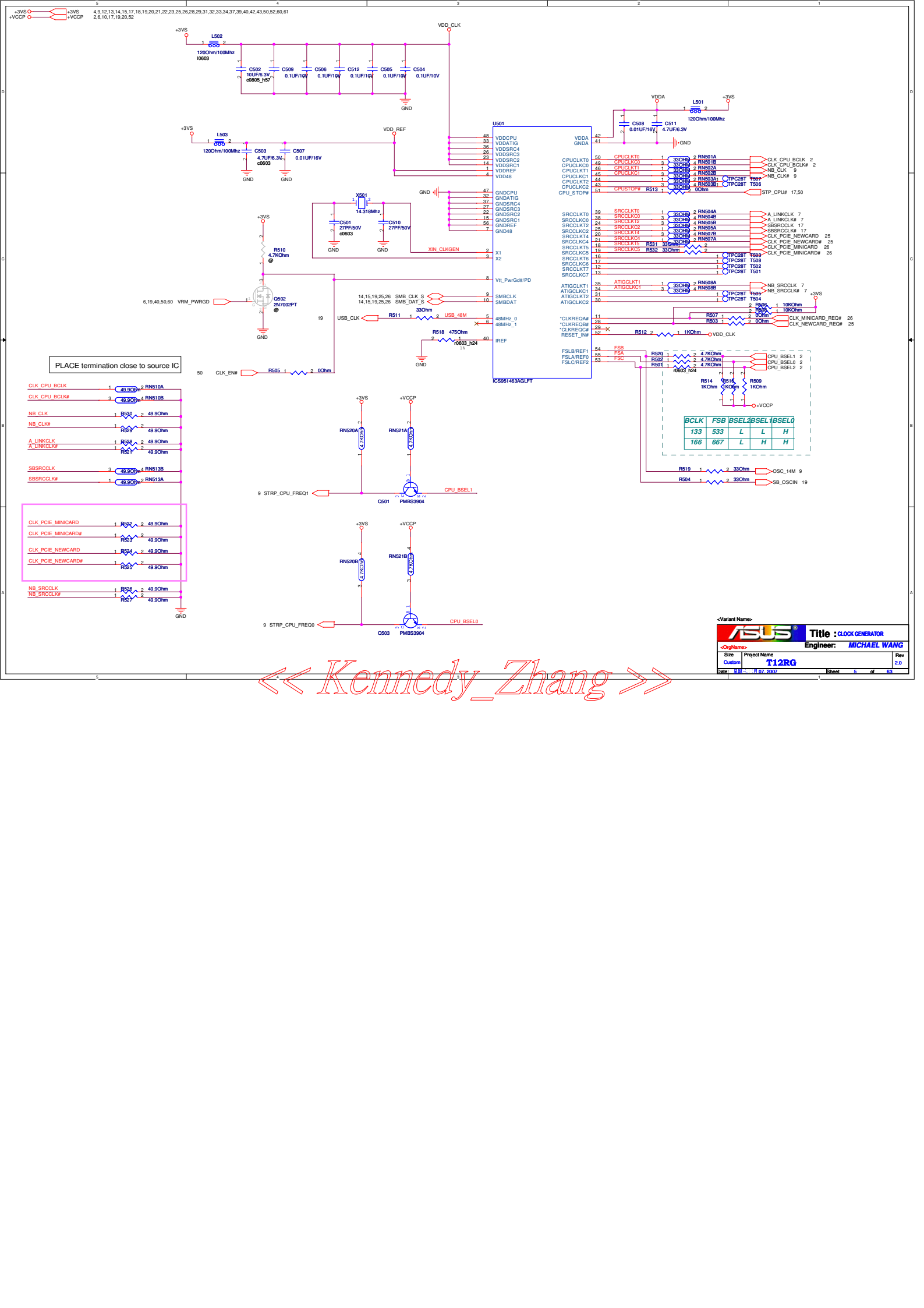
Title : THER-SENSOR,FAN

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期三, 一月 07, 2007 Sheet 4 of 63

<< Kennedy_Zhang >>



<Variant Name>

ASUS

Title : CLOCK GENERATOR

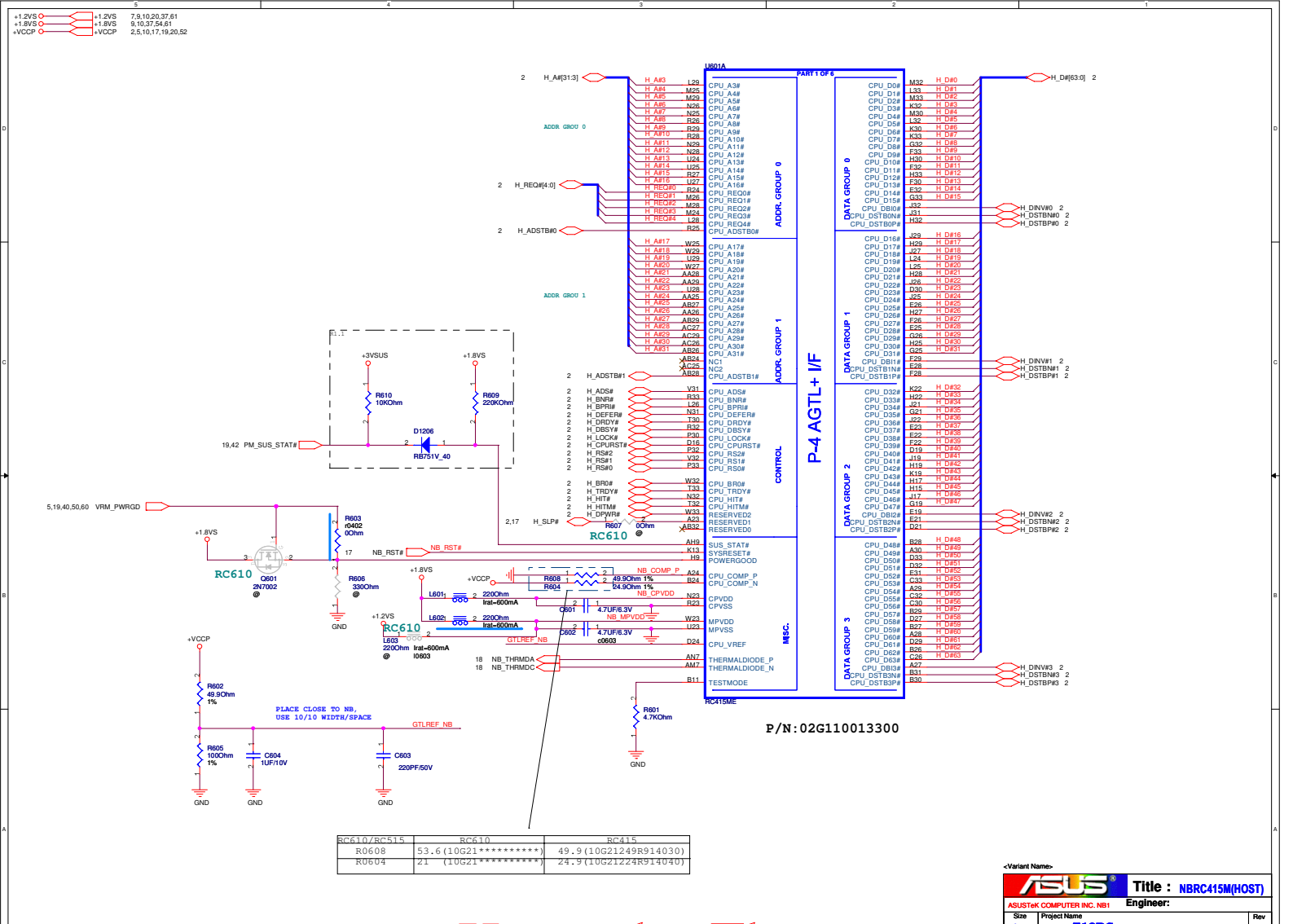
<OrgName>

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 5 of 63

<< Kennedy_Zhang >>



RC610/RC515	RC610	RC415
R0608	53.6(10G21**********)	49.9(10G21249R914030)
R0604	21 (10G21**********)	24.9(10G21224R914040)

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NBRC415M(HOST)

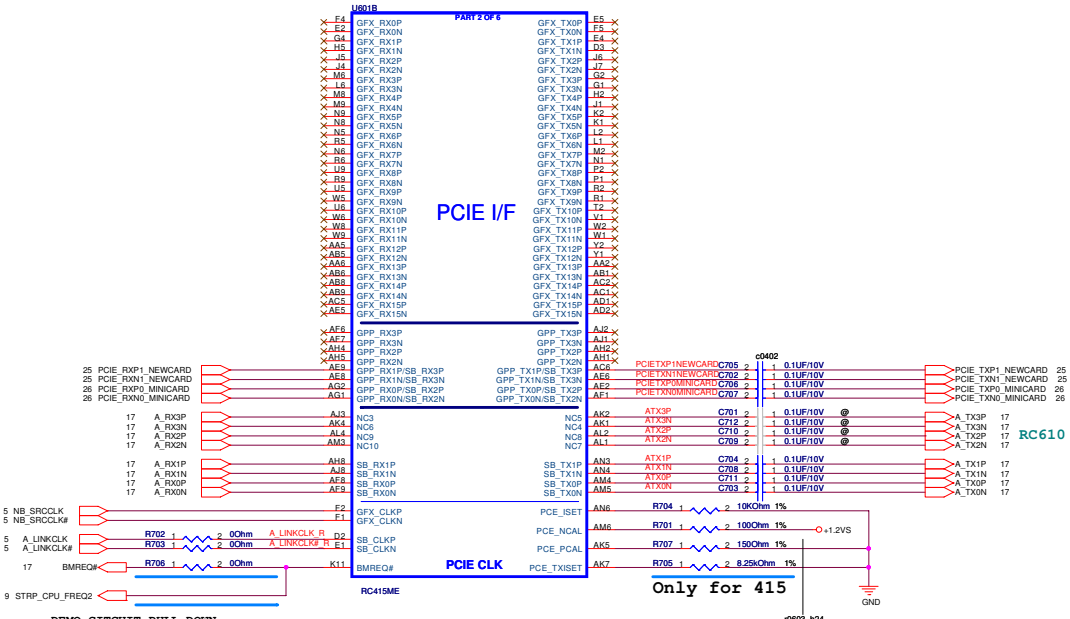
Engineer:

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 三月 07, 2007 Sheet 6 of 63

<< Kennedy_Zhang >>

+1.2VS +1.2VS 6,9,10,20,37,61



r0603 h24

RC610/RC515	RC610	RC415
R0704	1.47K(10G21*********)	10K(10G2131002130 30)
R0701	2K (10G21*********)	100(10G2131000130 10)
R0707	562 (10G21*********)	150(10G2131500130 30)

<Variant Name>

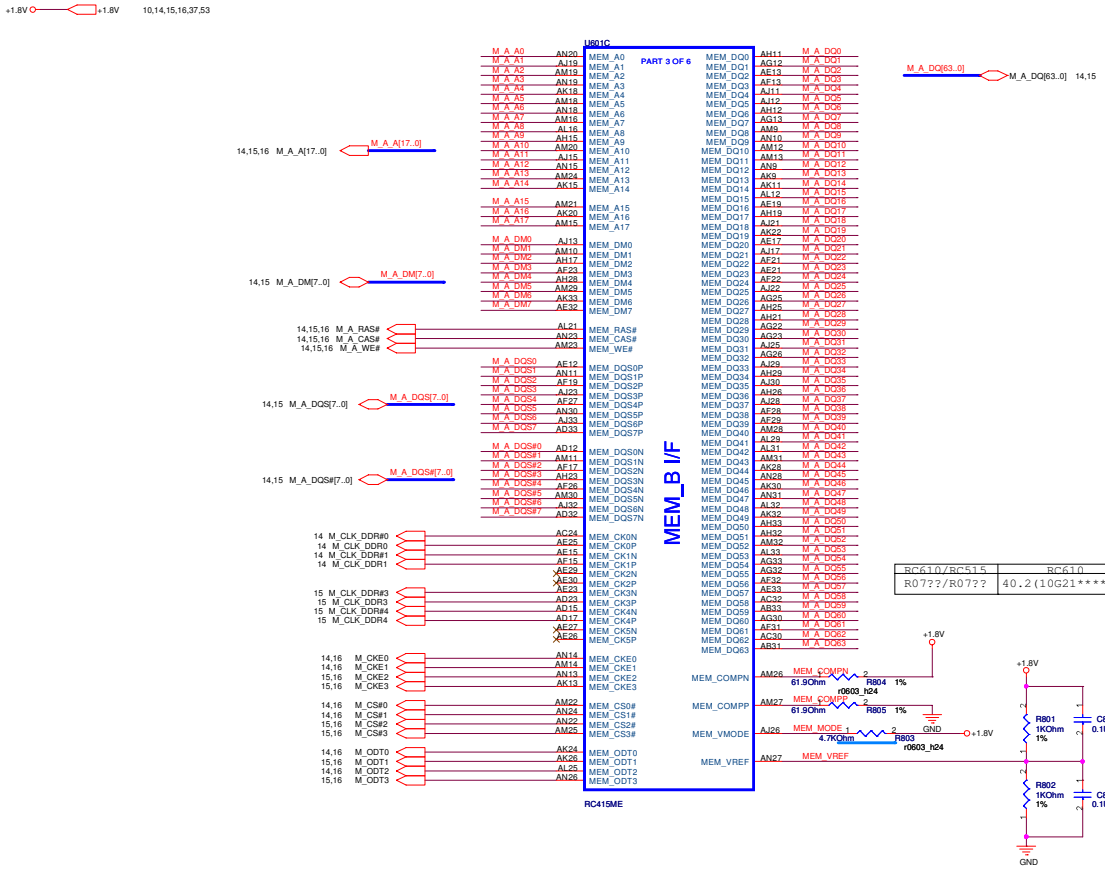
ASUSTeK COMPUTER INC. NB1

Title : NB-945PM(DMI & CFG)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

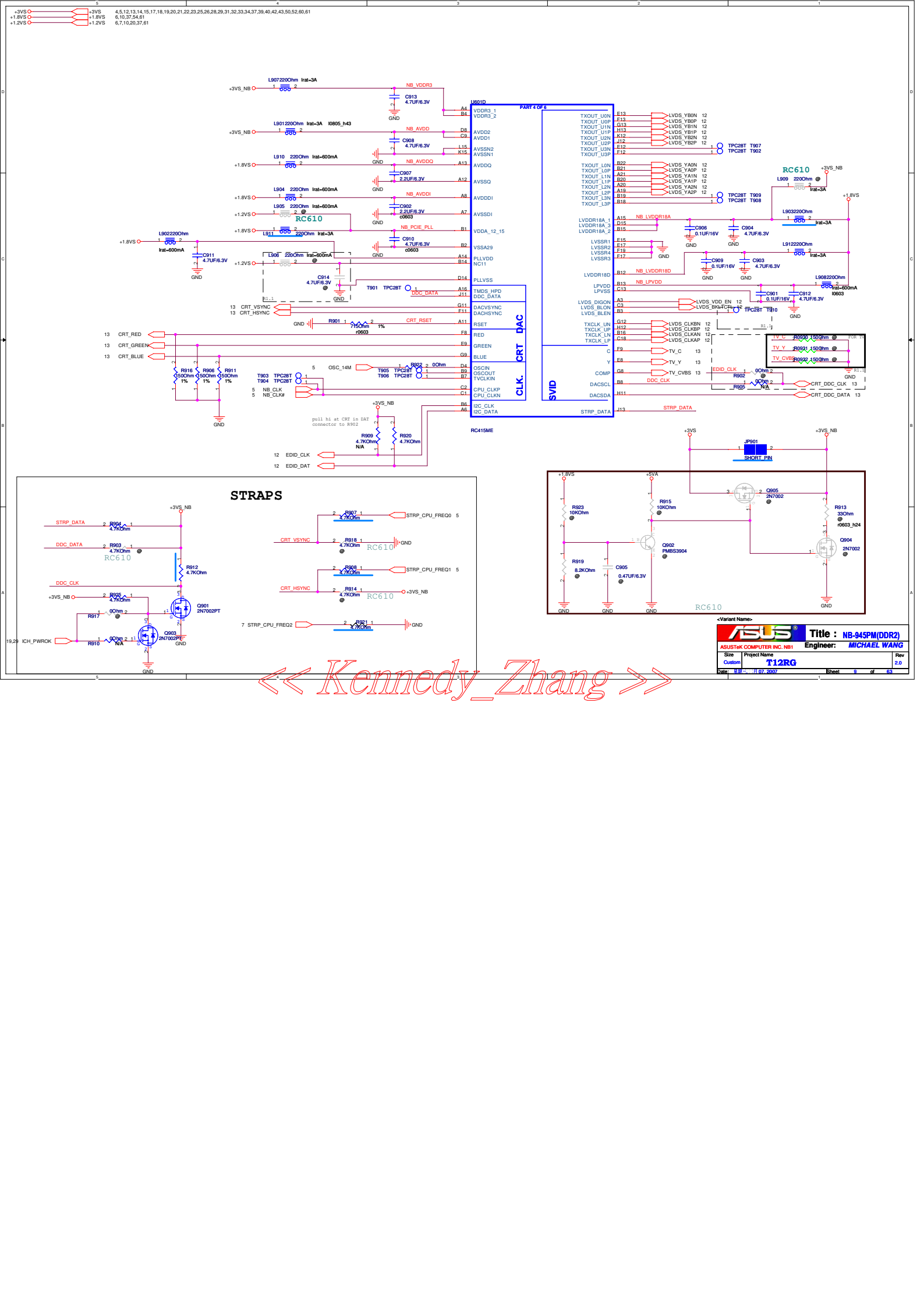
Date: 星期二, 一月 07, 2007 Sheet 7 of 63

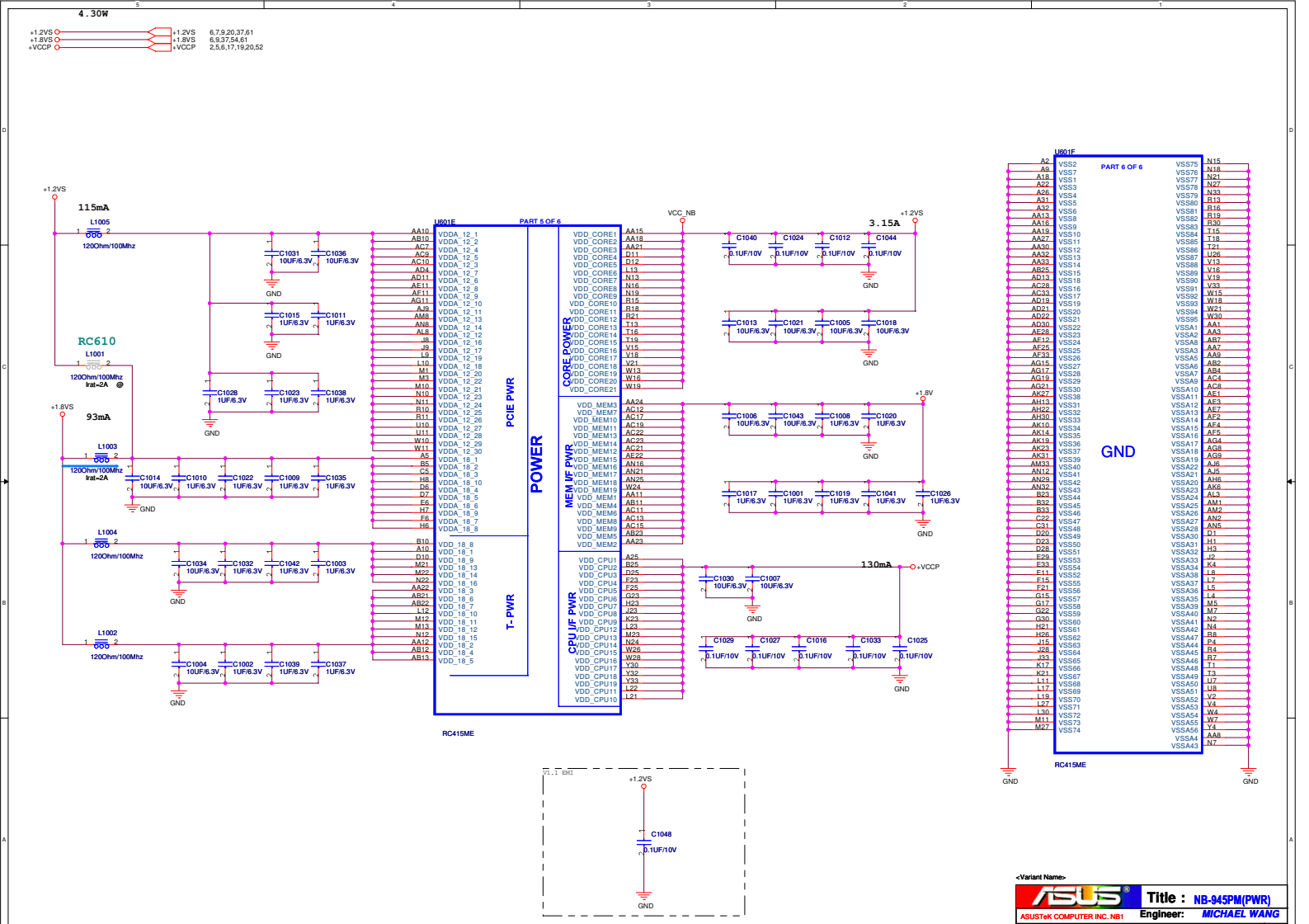


RC610/RC515	RC610	RC415
R07??/R07??	40.2(10G21*********)	61.9(10G2131002130 30)

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_945PM(PCI-E)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 8 of 63	


+3VS
+1.8VS
+1.2VS
4,5,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
6,10,37,54,61
6,7,10,20,37,61
U501D
PART 4 OF 6
RC415ME
SVID
CRT DAC
CLK.
STRAPS
RC610
Title : NB-945PM(DDR2)
ASUSTeK COMPUTER INC. NB1
Engineer: MICHAEL WANG
Project Name
T12RG
Rev
2.0
Sheet 9 of 63
<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(PWR)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 10 of 63	

<Variant Name>

Title : HISTORY

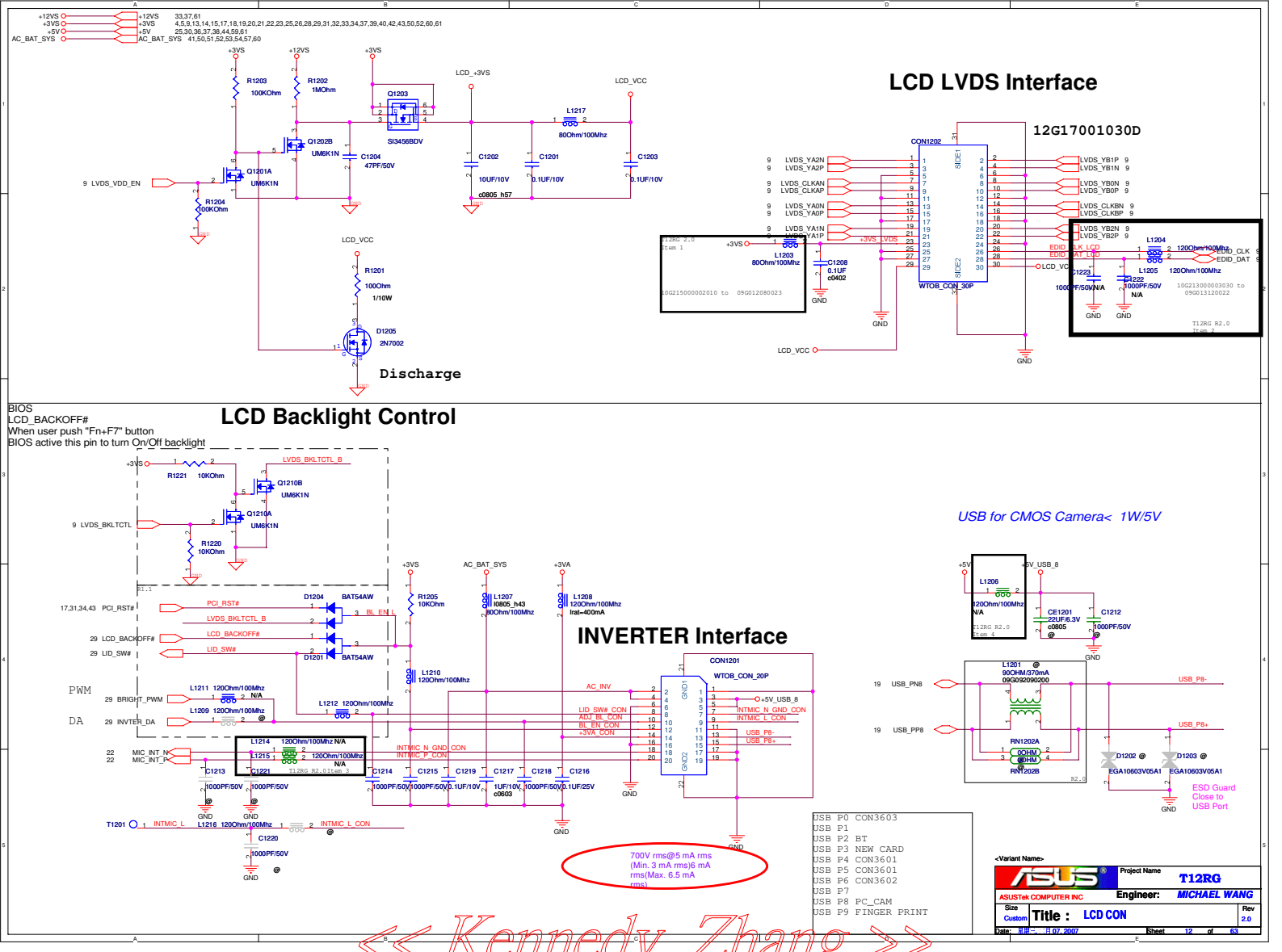
ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 11 of 63

<< Kennedy_Zhang >>



BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

LCD Backlight Control

INVERTER Interface

USB for CMOS Camera< 1W/5V

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT

<Variant Name>

ASUSTek COMPUTER INC	Project Name	T12RG
	Engineer:	MICHAEL WANG
Size: Custom	Title : LCD CON	Rev: 2.0
Date: 星期二, 七月 07, 2007	Sheet 12 of 63	

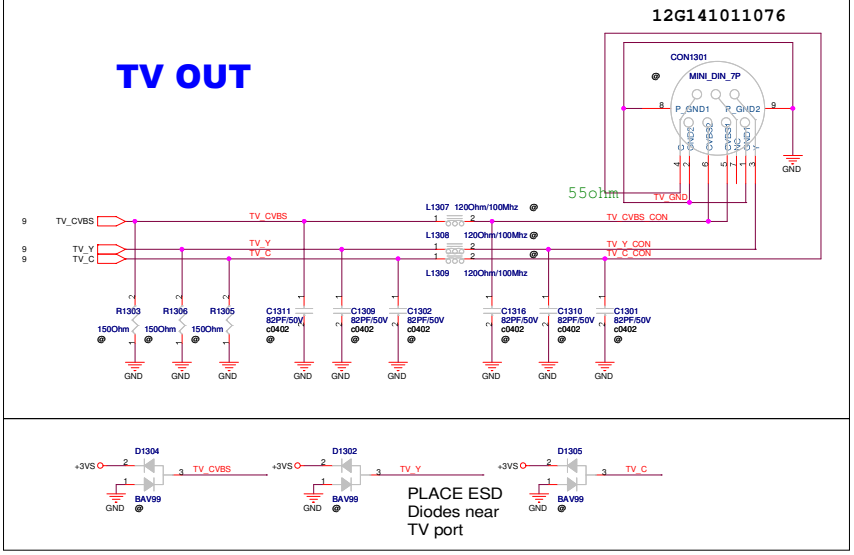
<< Kennedy_Zhang >>

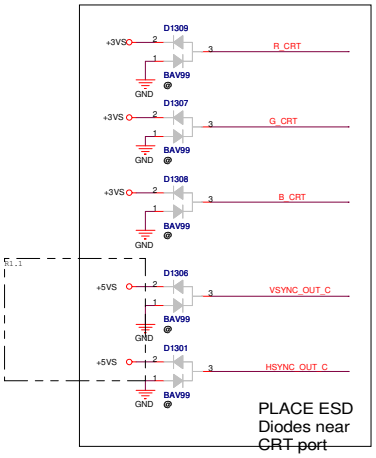
+5VS
+3VS
+5VS
+3VS
4,20,22,23,28,29,30,37,38,50,61
4,5,9,12,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

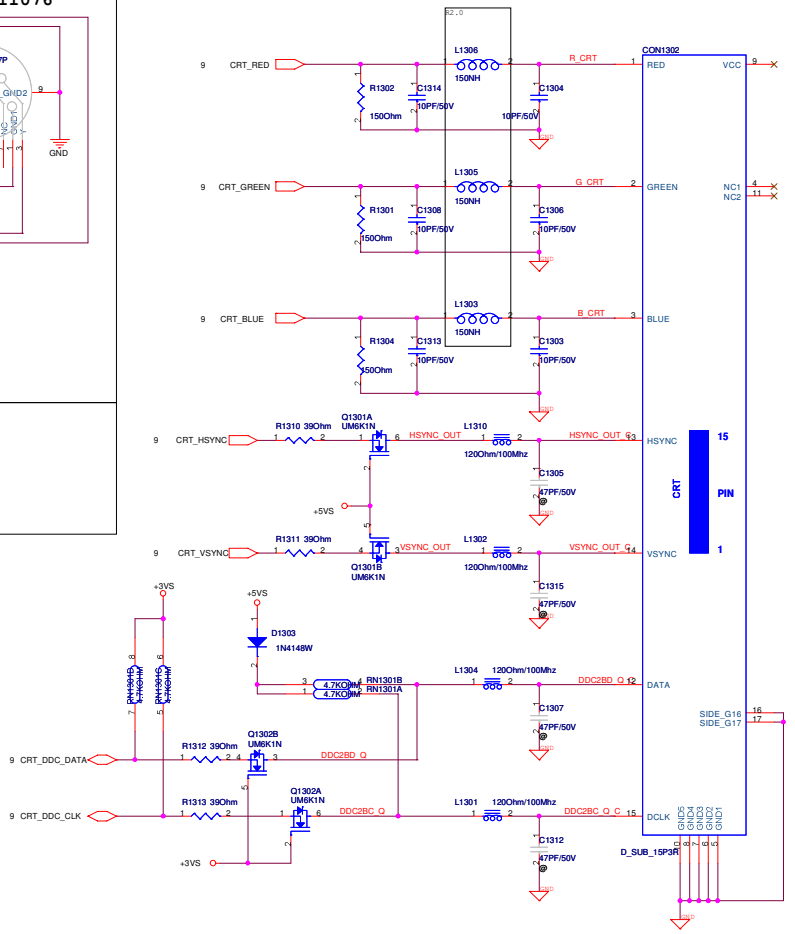
12G101102152
=>12G10110215A

12G141011076

TV OUT







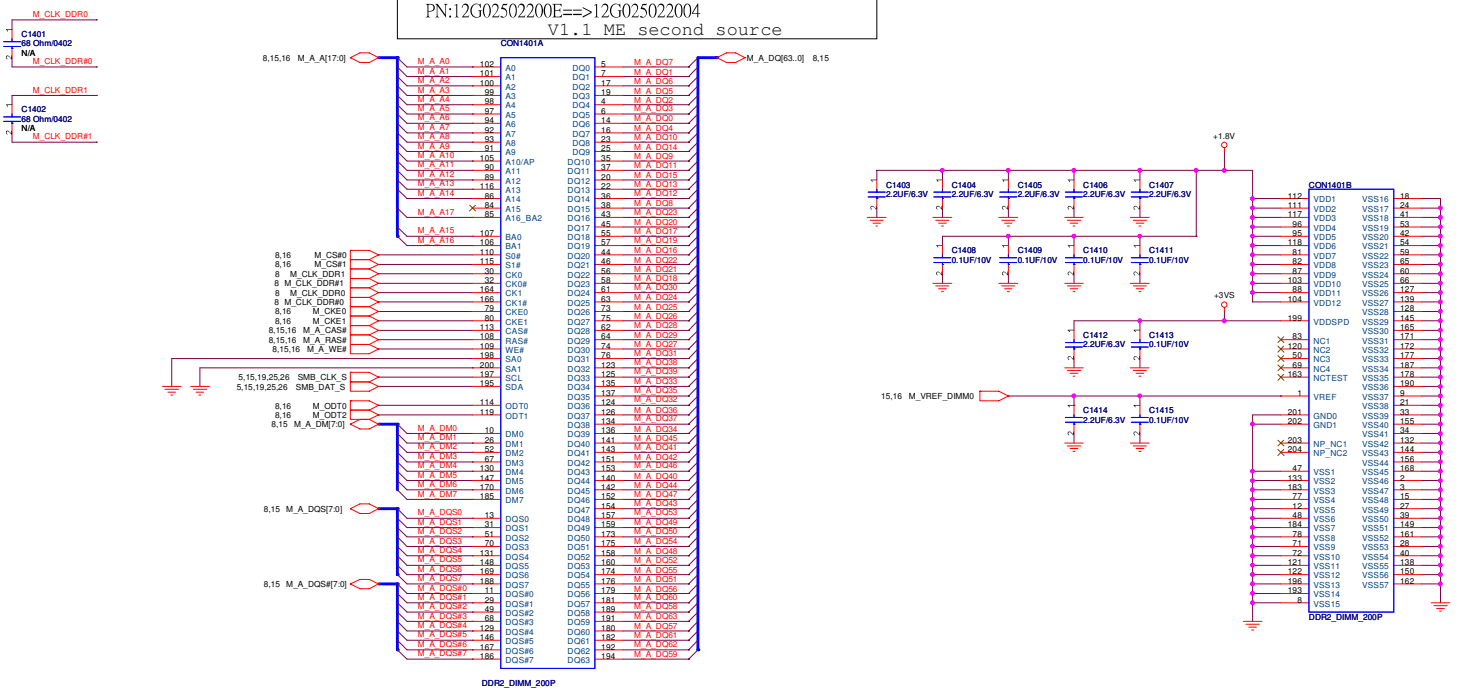
<Variant Name>

ASUSTeK COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 13 of 63	

<< Kennedy_Zhang >>

FRON

PN:12G02502200E==>12G025022004
V1.1 ME second source



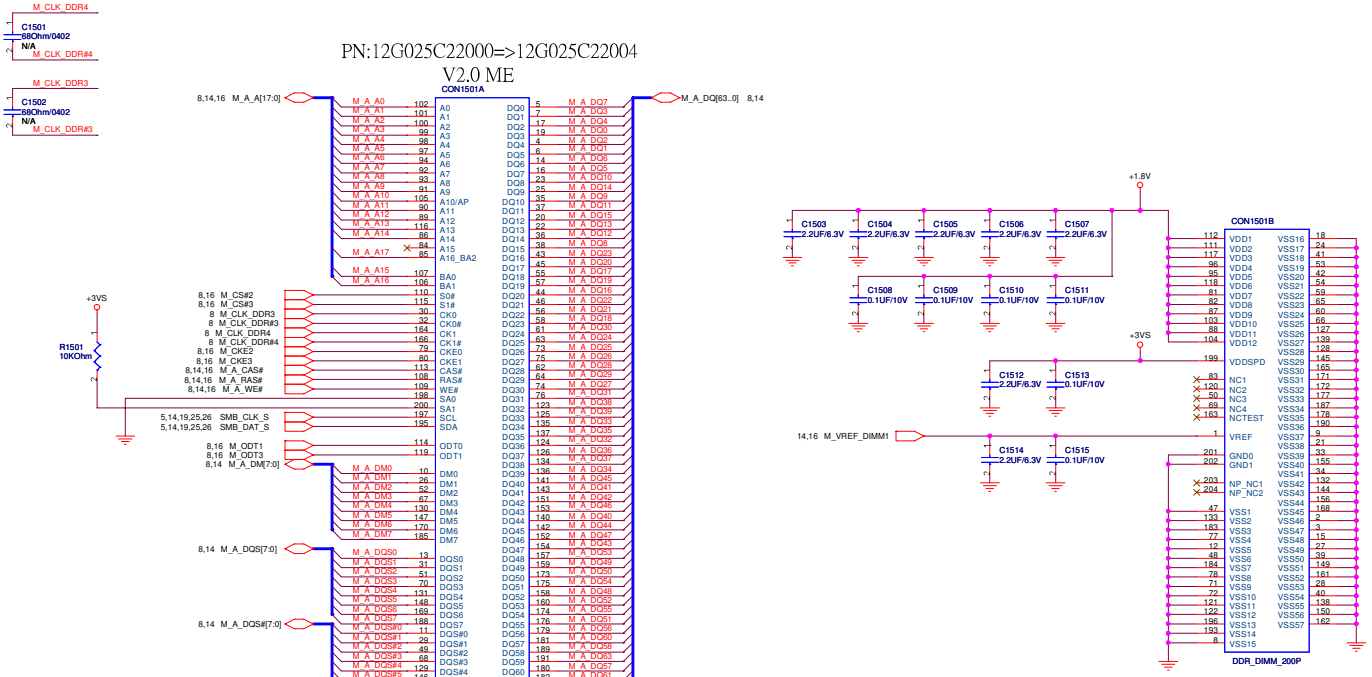
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 14 of 63	

<< Kennedy_Zhang >>

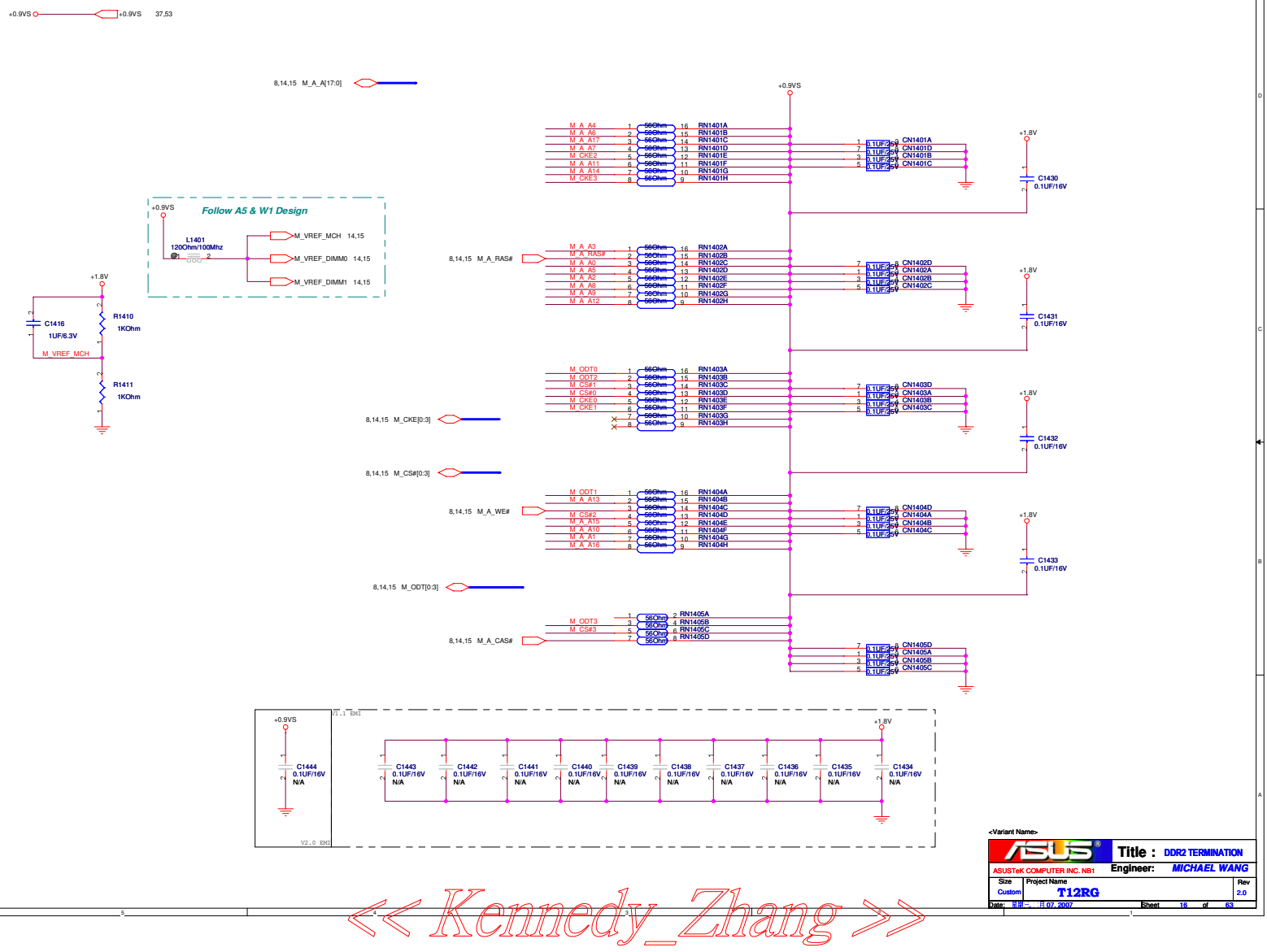
PN:12G025C22000=>12G025C22004

V2.0 ME



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 三月 07, 2007	Sheet 15 of 63	



<Variant Name>

ASUSTeK COMPUTER INC. NB1

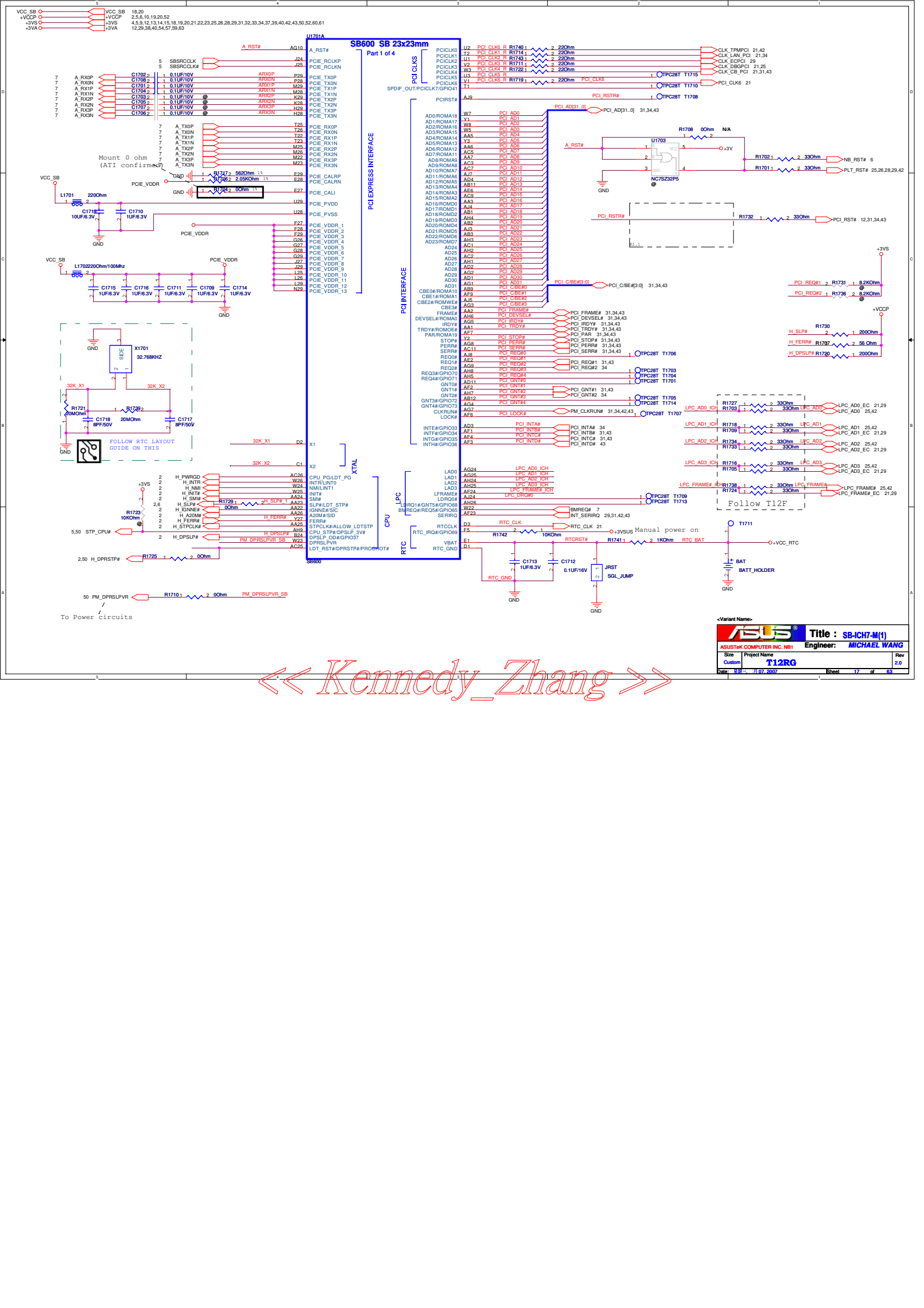
Title : DDR2 TERMINATION

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 16 of 63

<< Kennedy_Zhang >>



<Variant Name>

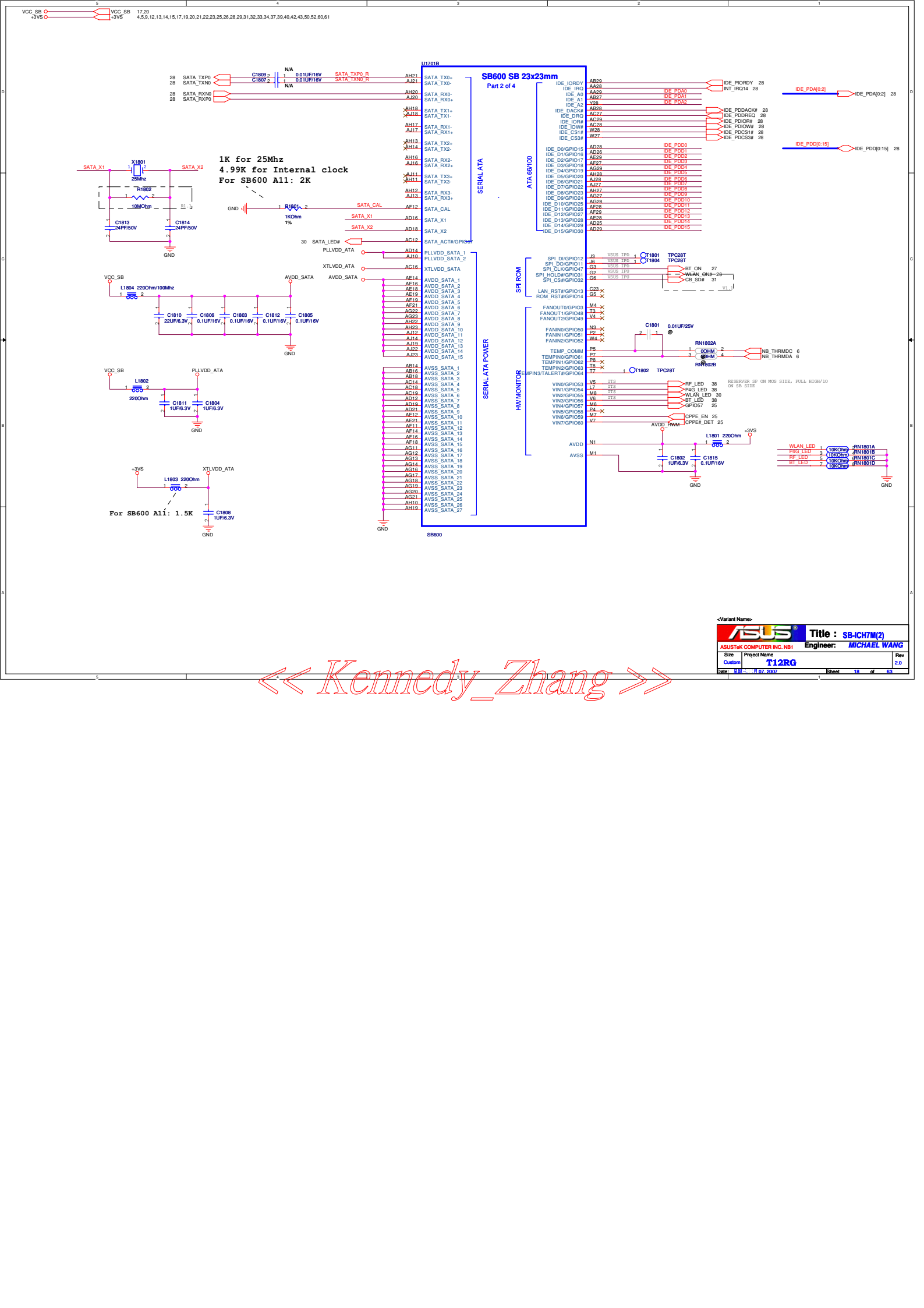
ASUSTeK COMPUTER INC. NB1

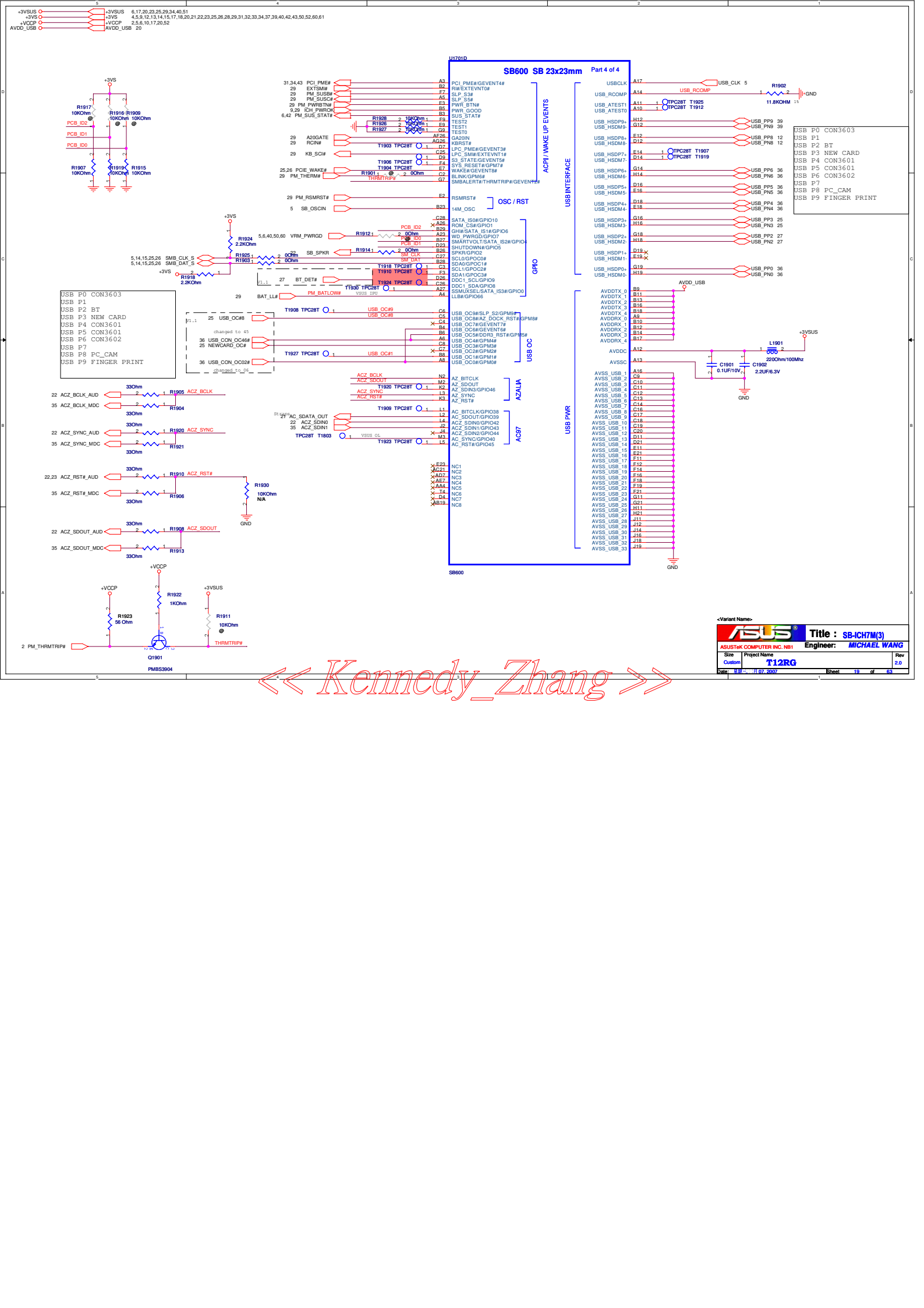
Title : SB-ICH7-M(1)

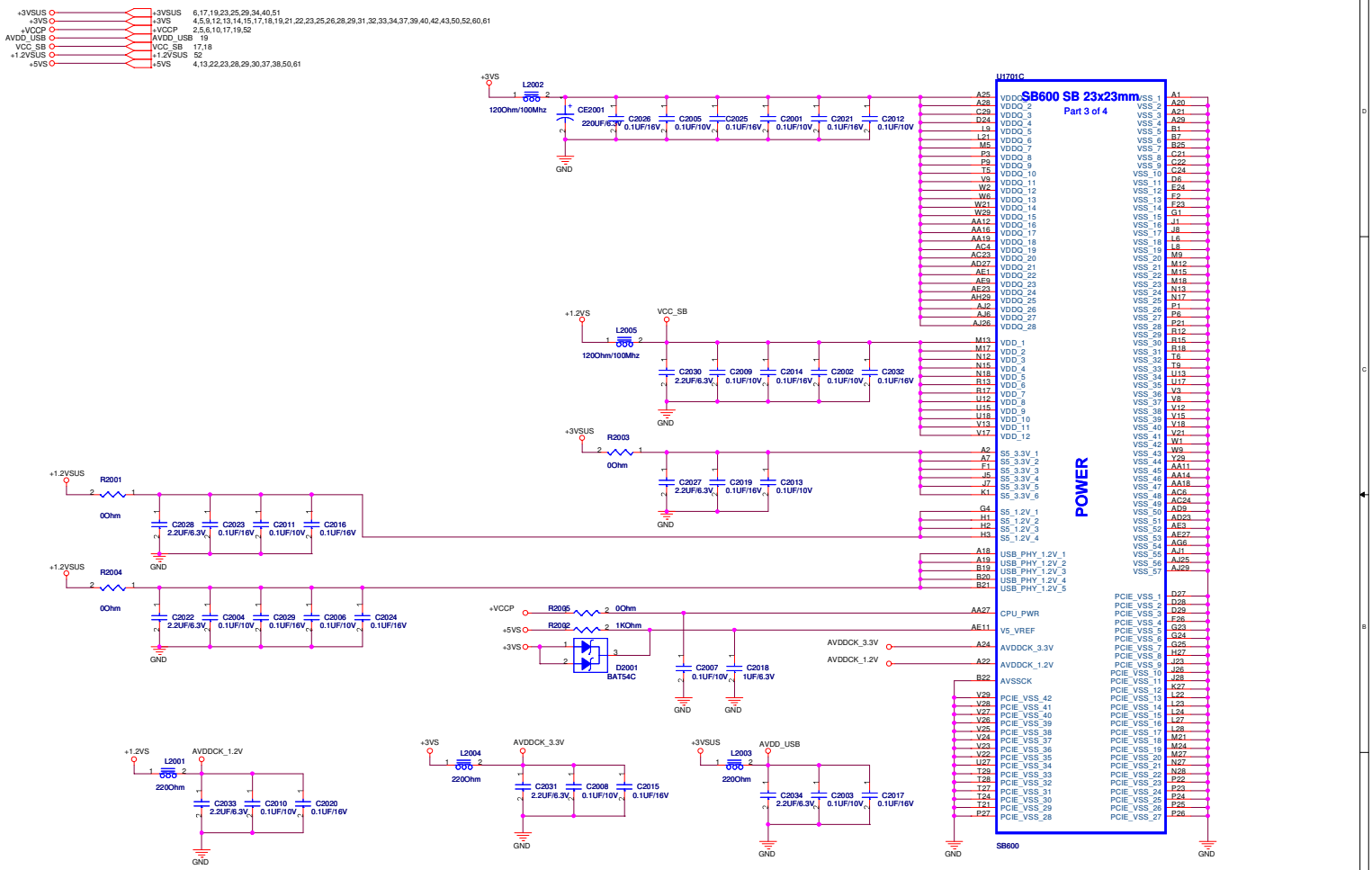
Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 17 of 63


VCC_SB
+3VS
17,20
4,5,9,12,13,14,15,17,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
U1701B
SB600 SB 23x23mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SB600
SATA_TXP0
SATA_TXN0
SATA_RXN0
SATA_RXP0
SATA_TXP0_R
SATA_TXN0_R
C1809
C1807
0.01UF/16V
N/A
SATA_TX0+
SATA_TX0-
SATA_RX0-
SATA_RX0+
SATA_TX1+
SATA_TX1-
SATA_RX1-
SATA_RX1+
SATA_TX2+
SATA_TX2-
SATA_RX2-
SATA_RX2+
SATA_TX3+
SATA_TX3-
SATA_RX3-
SATA_RX3+
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67
SATA_LED#
PLLVDD_ATA
XTLVDD_ATA
AVDD_SATA
X1801
25Mhz
R1802
10MOhm
C1813
24PF/50V
C1814
24PF/50V
1K for 25Mhz
4.99K for Internal clock
For SB600 A11: 2K
R1801
1KOhm
1%
GND
L1804 220Ohm/100Mhz
C1810
22UF/6.3V
C1806
0.1UF/16V
C1803
0.1UF/16V
C1812
0.1UF/16V
C1805
0.1UF/16V
L1802
220Ohm
C1811
1UF/6.3V
C1804
1UF/6.3V
L1803 220Ohm
C1808
1UF/6.3V
For SB600 A11: 1.5K
XTLVDD_ATA
+3VS
IDE_IORDY
IDE_IRQ
IDE_A0
IDE_A1
IDE_A2
IDE_DACK#
IDE_DRQ
IDE_IOR#
IDE_IOW#
IDE_CS1#
IDE_CS3#
IDE_D0/GPIO15
IDE_D1/GPIO16
IDE_D2/GPIO17
IDE_D3/GPIO18
IDE_D4/GPIO19
IDE_D5/GPIO20
IDE_D6/GPIO21
IDE_D7/GPIO22
IDE_D8/GPIO23
IDE_D9/GPIO24
IDE_D10/GPIO25
IDE_D11/GPIO26
IDE_D12/GPIO27
IDE_D13/GPIO28
IDE_D14/GPIO29
IDE_D15/GPIO30
IDE_PIORDY
INT_IRQ14
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDDACK#
IDE_PDDREQ
IDE_PDIOR#
IDE_PDIOW#
IDE_PDCS1#
IDE_PDCS3#
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDA[0:2]
IDE_PDD[0:15]
SPI_DI/GPIO12
SPI_DO/GPIO11
SPI_CLK/GPIO47
SPI_HOLD#/GPIO31
SPI_CS#/GPIO32
LAN_RST#/GPIO13
ROM_RST#/GPIO14
T1801
T1804
TPC28T
BT_ON
WLAN_ON#
CB_SD#
FANOUT0/GPIO3
FANOUT1/GPIO48
FANOUT2/GPIO49
FANIN0/GPIO50
FANIN1/GPIO51
FANIN2/GPIO52
TEMP_COMM
TEMPIN0/GPIO61
TEMPIN1/GPIO62
TEMPIN2/GPIO63
TEMPIN3/TALERT#/GPIO64
C1801
0.01UF/25V
RN1802A
RN1802B
NB_THRMDC
NB_THRMDA
T1802
VIN0/GPIO53
VIN1/GPIO54
VIN2/GPIO55
VIN3/GPIO56
VIN4/GPIO57
VIN5/GPIO58
VIN6/GPIO59
VIN7/GPIO60
RF_LED
P4G_LED
WLAN_LED
BT_LED
GPIO57
CPPE_EN
CPPE#_DET
RESERVER SP ON MOS SIDE, PULL HIGH/1O ON SB SIDE
AVDD_RWM
AVDD
AVSS
C1802
1UF/6.3V
C1815
0.1UF/16V
L1801 220Ohm
WLAN_LED
P4G_LED
RF_LED
BT_LED
10KOhm
RN1801A
RN1801B
RN1801C
RN1801D
AVDD_SATA_1
AVDD_SATA_2
AVDD_SATA_3
AVDD_SATA_4
AVDD_SATA_5
AVDD_SATA_6
AVDD_SATA_7
AVDD_SATA_8
AVDD_SATA_9
AVDD_SATA_10
AVDD_SATA_11
AVDD_SATA_12
AVDD_SATA_13
AVDD_SATA_14
AVDD_SATA_15
AVSS_SATA_1
AVSS_SATA_2
AVSS_SATA_3
AVSS_SATA_4
AVSS_SATA_5
AVSS_SATA_6
AVSS_SATA_7
AVSS_SATA_8
AVSS_SATA_9
AVSS_SATA_10
AVSS_SATA_11
AVSS_SATA_12
AVSS_SATA_13
AVSS_SATA_14
AVSS_SATA_15
AVSS_SATA_16
AVSS_SATA_17
AVSS_SATA_18
AVSS_SATA_19
AVSS_SATA_20
AVSS_SATA_21
AVSS_SATA_22
AVSS_SATA_23
AVSS_SATA_24
AVSS_SATA_25
AVSS_SATA_26
AVSS_SATA_27
<Variant Name>
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: MICHAEL WANG
Size: Custom
Project Name: T12RG
Rev: 2.0
Date: 星期一, 一月 07, 2007
Sheet 18 of 63
<< Kennedy_Zhang >>

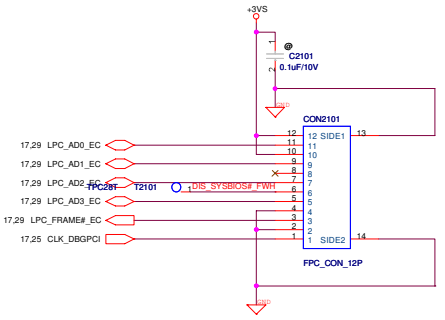


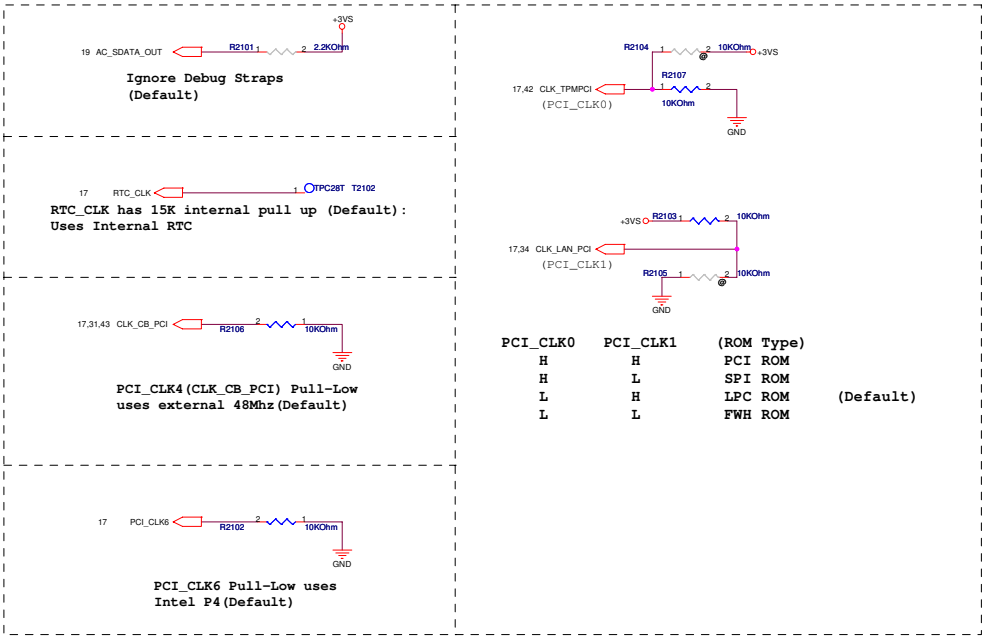


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(PWR)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 三月 07, 2007	Sheet 20 of 63	

<< Kennedy_Zhang >>





<Variant Name>

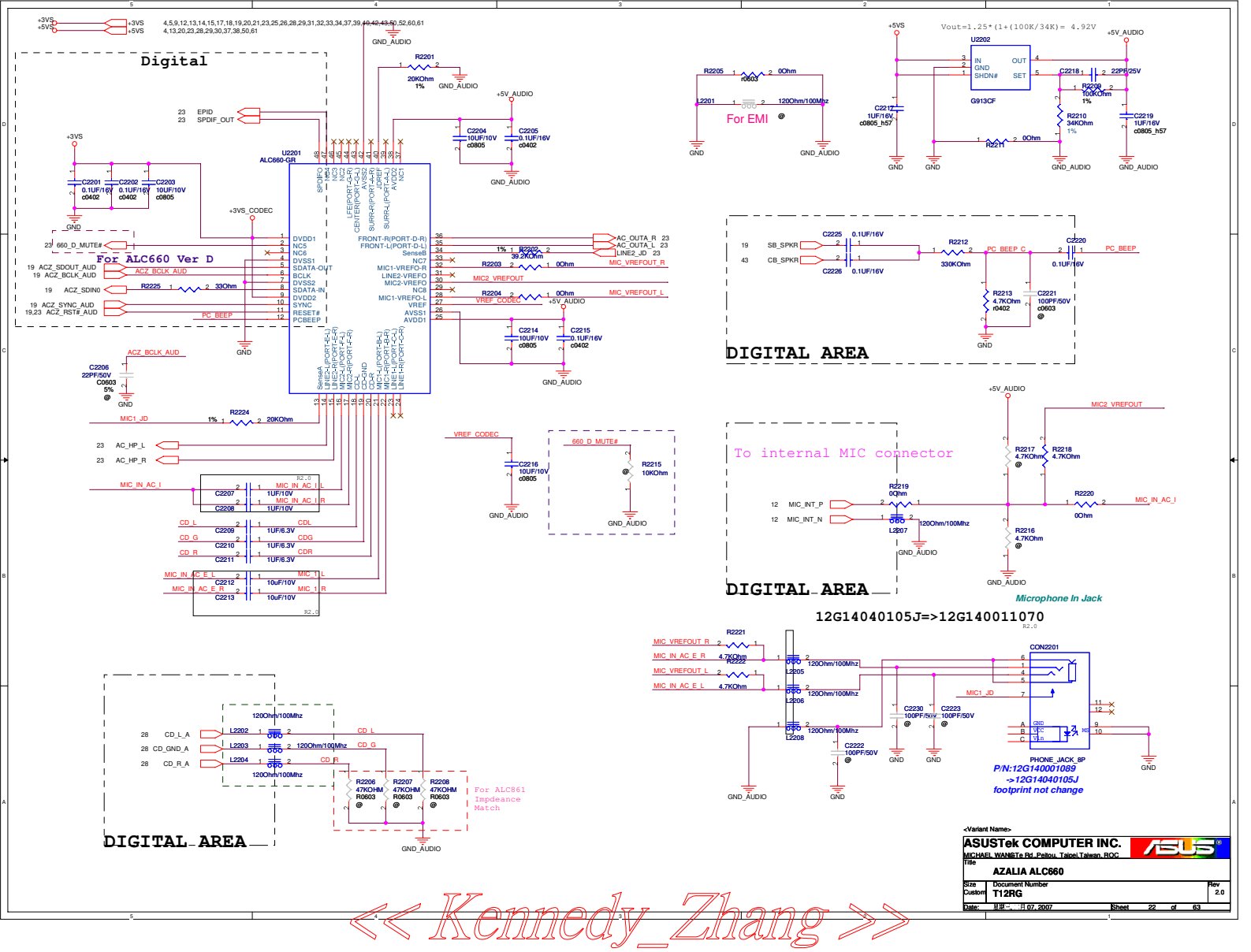
Title : BLOCK DIAGRAM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 21 of 63

<< Kennedy_Zhang >>



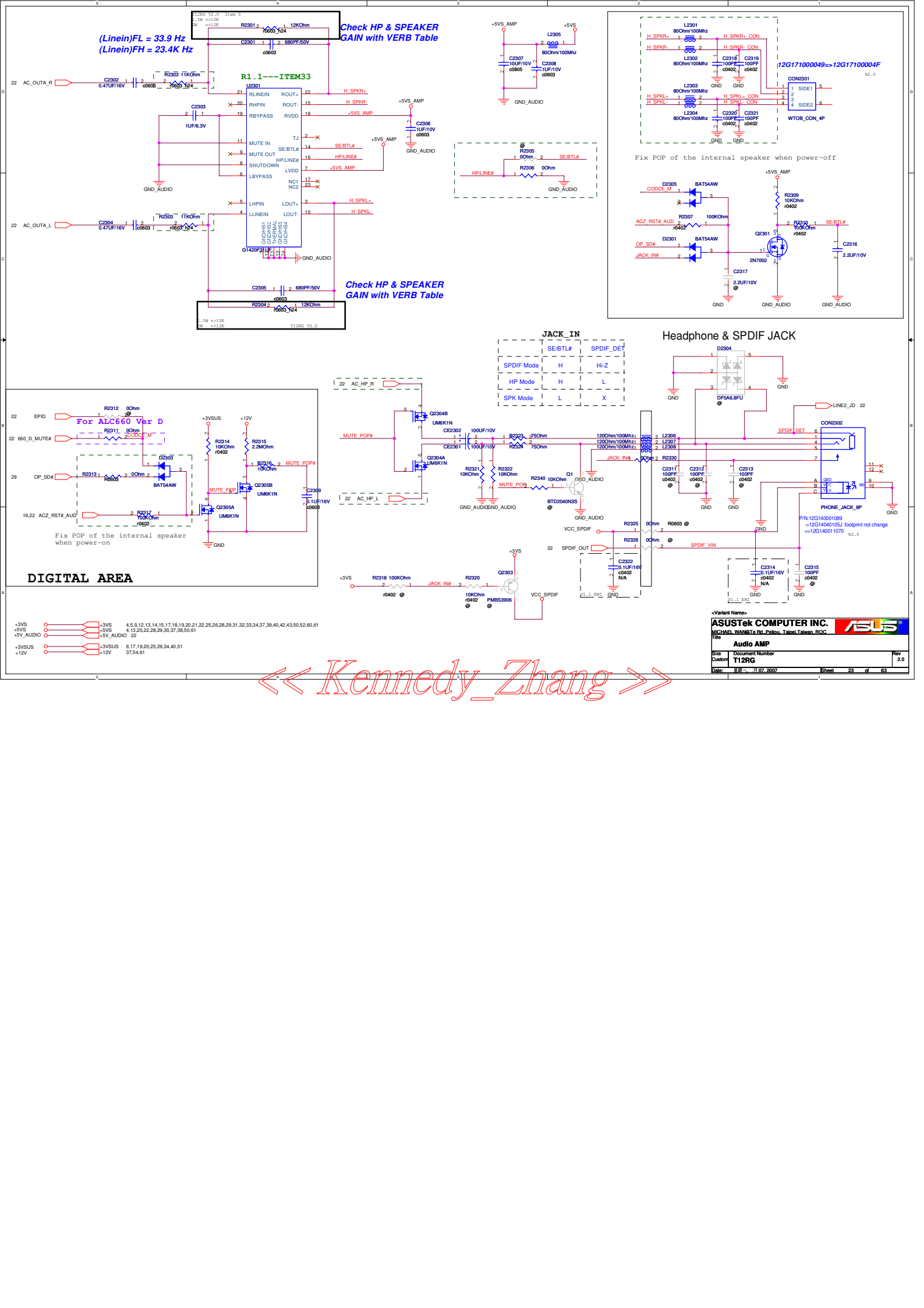
<Variant Name>
ASUSTek COMPUTER INC.
MICHAEL WANGTe Rd. Peitou, Taipei,Taiwan, ROC

Title: AZALIA ALC660

Size	Document Number	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 22 of 63

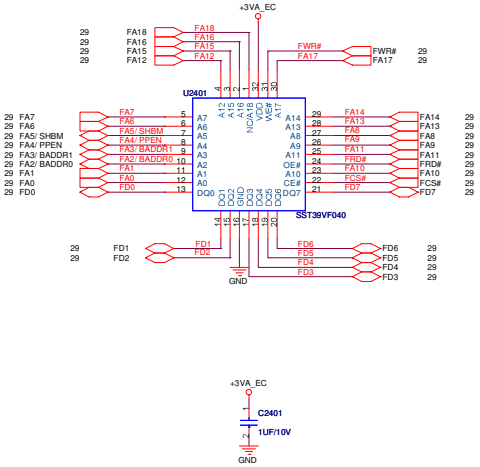
<< Kennedy_Zhang >>


(Linein)FL = 33.9 Hz
(Linein)FH = 23.4K Hz
Check HP & SPEAKER GAIN with VERB Table
R1.1---ITEM33
U2301
G1420F31UF
Check HP & SPEAKER GAIN with VERB Table
12G171000049=>12G17100004F
CON2301
WTOB_CON_4P
Fix POP of the internal speaker when power-off
JACK_IN
SE/BTL#
SPDIF_DET
SPDIF Mode
HP Mode
SPK Mode
Headphone & SPDIF JACK
CON2302
PHONE_JACK_8P
P/N:12G140001089
->12G14040105J :footprint not change
=>12G140011070
For ALC660 Ver D
Fix POP of the internal speaker when power-on
DIGITAL AREA
+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS 4,13,20,22,28,29,30,37,38,50,61
+5V_AUDIO 22
+3VSUS 6,17,19,20,25,29,34,40,51
+12V 37,54,61
<Variant Name>
ASUSTek COMPUTER INC.
MICHAEL WANGTe Rd. Peitou, Taipei,Taiwan, ROC
Audio AMP
Size Custom
Document Number T12RG
Rev 2.0
Date: 星期二, 一月 07, 2007
Sheet 23 of 63
<< Kennedy_Zhang >>

+3VA_EC +3VA_EC 26,29

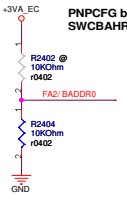
ISA ROM

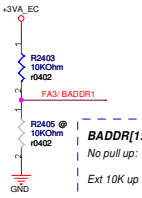
0.01A



EC Hardware Strap

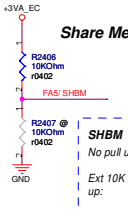
Strap value sampled after VSTBY power up reset





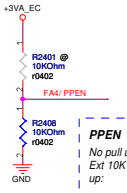
BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

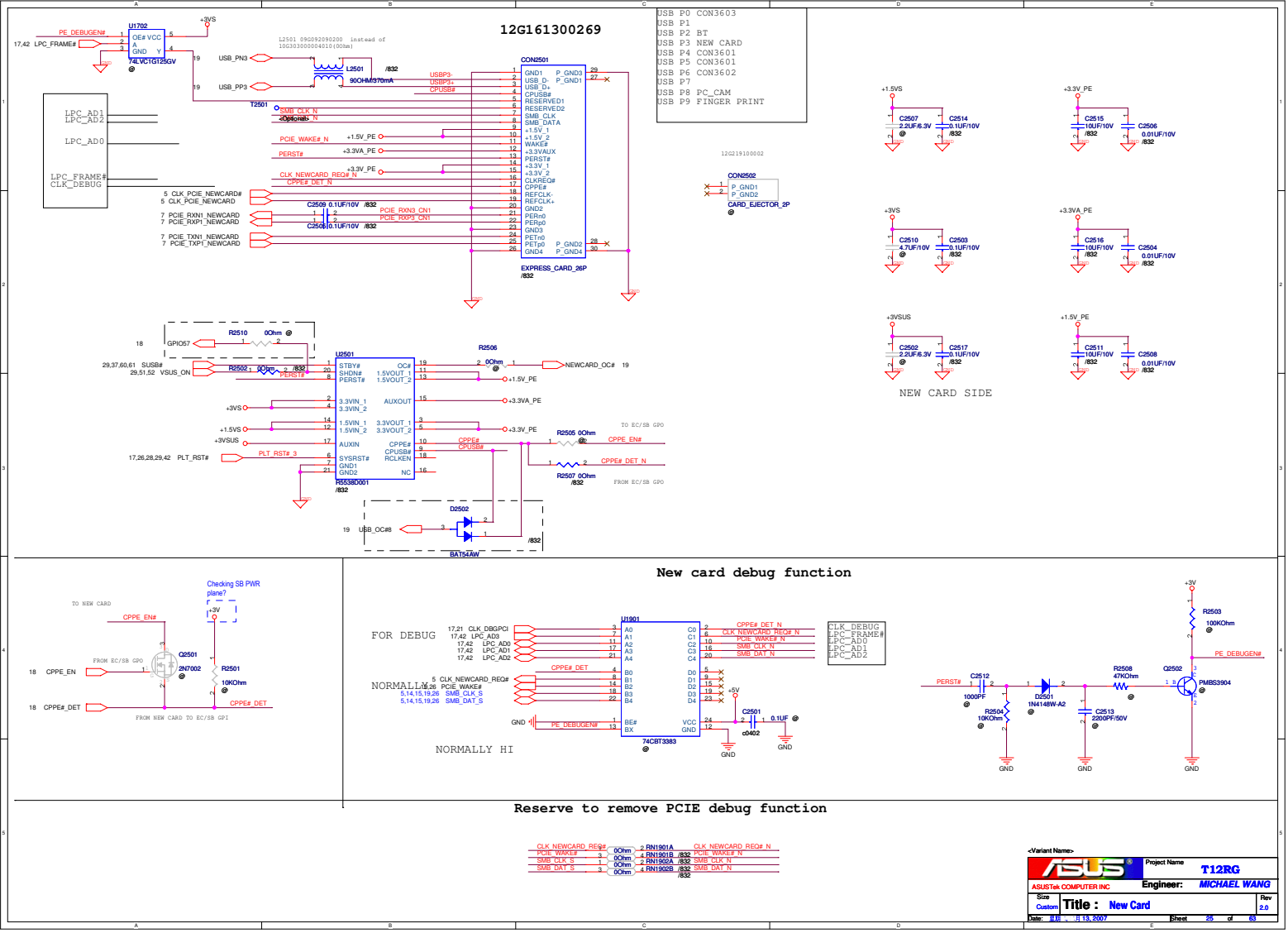


PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 十一月 07, 2007	Sheet 24 of 63	



New card debug function

Reserve to remove PCIE debug function

<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : New Card	Rev: 2.0
Date: 月 13, 2007	Sheet 25 of 63	

<< Kennedy_Zhang >>

+3V	+3V	17,25,27,31,35,37,42,43,44,61
+3VS	+3VS	4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.5VS	+1.5VS	25,37,54
+3VA_EC	+3VA_EC	24,29

12G030000526

CLKREQ#(output) CLOCK REQUEST could be pull low

CON2602

MINI_CARD_LATCH_52P

19,25	PCIE_WAKE#	1	WAKE#	3.3V_1	2
27	CH_DATA	3	Reserved1	GND7	4
27	CH_CLK	5	Reserved2	1.5V_1	6
5	CLK_MINICARD_REQ#	7	CLKREQ#	UIM_PWR	8
		9	GND1	UIM_DATA	10
5	CLK_PCIE_MINICARD#	11	REFCLK-	UIM_CLK	12
5	CLK_PCIE_MINICARD	13	REFCLK+	UIM_RESET	14
		15	GND2	UIM_VPP	16
		17	Reserved/UIM_C8	GND8	18
		19	Reserved/UIM_C4	W_DISABLE#	20
		21	GND3	PERST#	22
7	PCIE_RXN0_MINICARD	23	PERn0	+3.3Vaux	24
7	PCIE_RXP0_MINICARD	25	PERp0	GND9	26
		27	GND4	1.5V_2	28
		29	GND5	SMB_CLK	30
7	PCIE_TXN0_MINICARD	31	PETn0	SMB_DATA	32
7	PCIE_TXP0_MINICARD	33	PETp0	GND10	34
		35	GND6	USB_D-	36
		37	Reserved3	USB_D+	38
		39	Reserved4	GND11	40
		41	Reserved5	LED_WWAN#	42
		43	Reserved6	LED_WLAN#	44
		45	Reserved7	LED_WPAN#	46
		47	Reserved8	1.5V_3	48
		49	Reserved9	GND12	50
		51	Reserved10	3.3V_2	52
		53	GND13	NP_NC2	56
		54	GND14	NP_NC1	55

+3VS

C2602 0.1UF/10V GND

C2605 0.1UF/10V GND

C2606 10UF/6.3V GND

3.003V~3.597V
Max= 750 mA

+1.5VS

C2608 0.1UF/10V GND

C2601 0.1UF/10V GND

C2603 10UF/6.3V GND

1.425V~1.575V
Max= 375 mA

+3V

C2607 0.1UF/10V GND

C2604 1UF/6.3V GND

3.003V~3.597V
Max= 250 mA

WIRELESS_LAN_ON/OFF#

PLT_RST# 17,25,28,29,42

R2603 1 2 0Ohm @ SMB_CLK_S 5,14,15,19,25

R2601 1 2 0Ohm @ SMB_DAT_S 5,14,15,19,25

WL_LED# 1 T260TPC28t

CON2601

MINI_PCI_LATCH_5P

MINI_PCI-E LATCH_5P

GND

12G162210052

+3VA_EC

PULL HIGH ON SB SIDE AND IT INTERNAL PULL HIGH

INTERNAL PU

R2602 47KOhm @

WIRELESS_LAN_ON/OFF#

18 WLAN_ON#

Q2601 2N7002

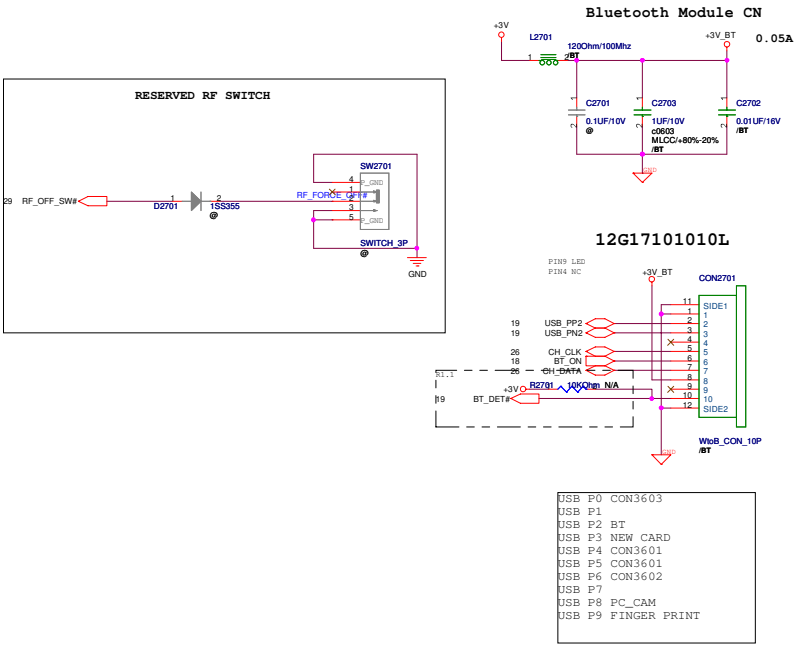
<Variant Name>

Project Name	T12RG		
ASUSTek COMPUTER INC	Engineer:	MICHAEL WANG	
Size: Custom	Title : MINI PCI		Rev: 2.0
Date: 星期二, 十月 07, 2007	Sheet 26 of 63		

<< Kennedy_Zhang >>

+3V +3V 17,25,26,31,35,37,42,43,44,61

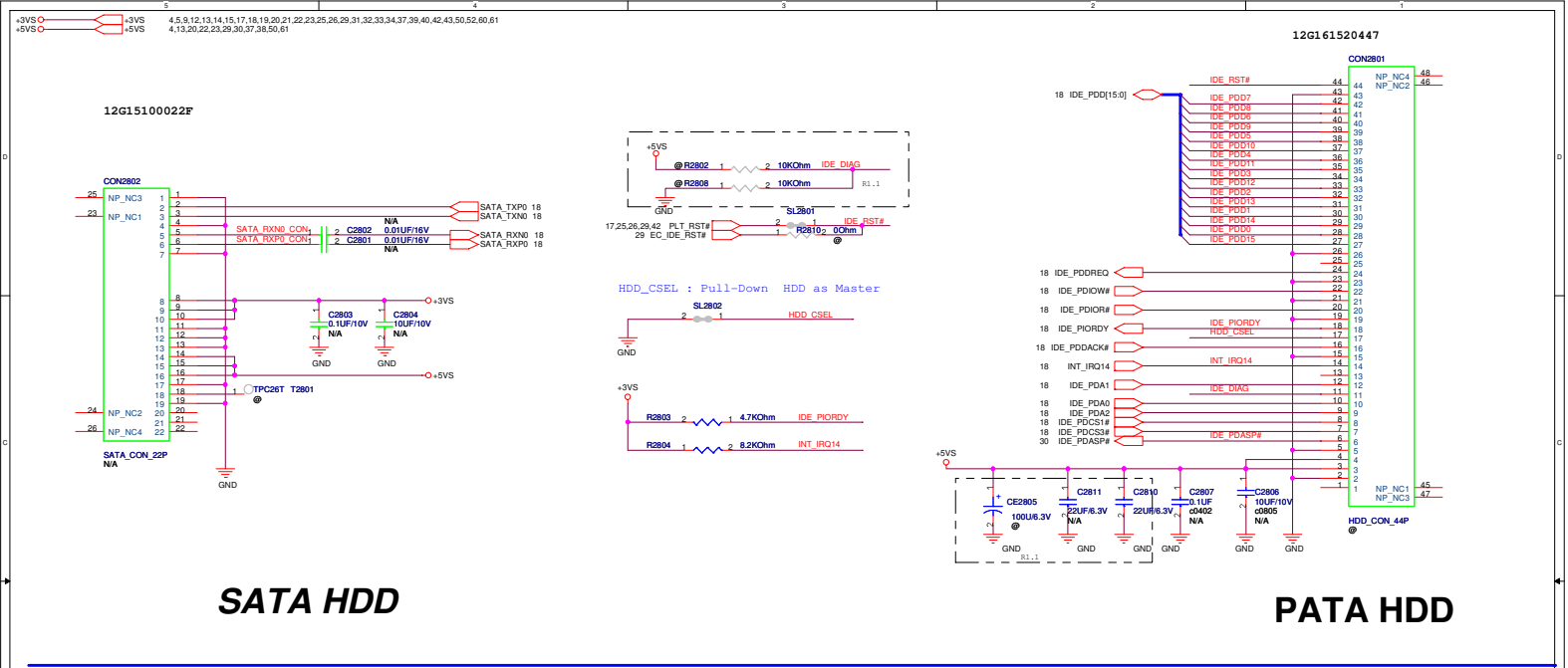
For Bluetooth



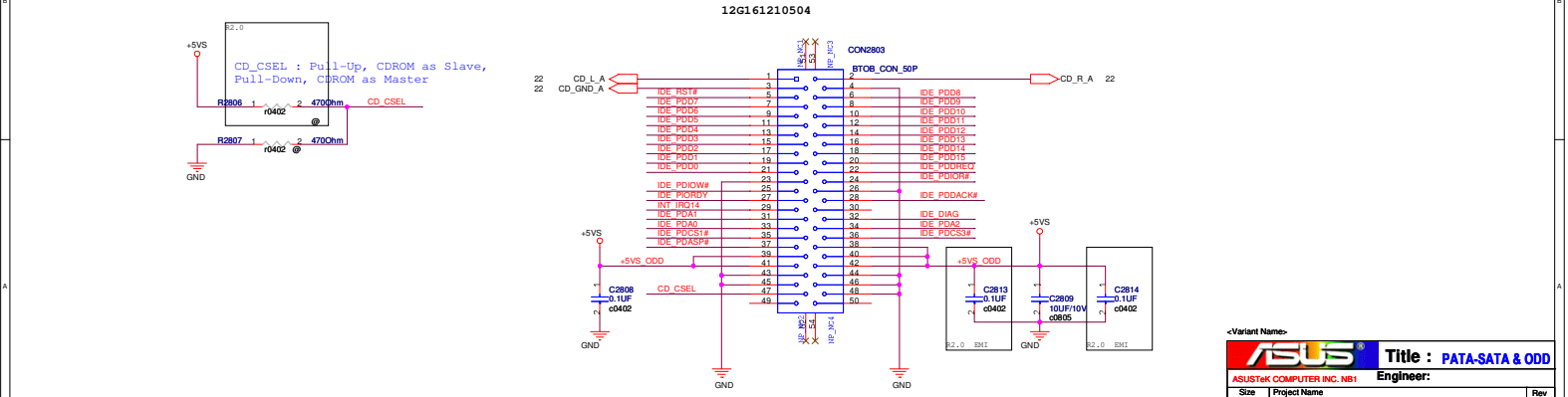

```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT
```

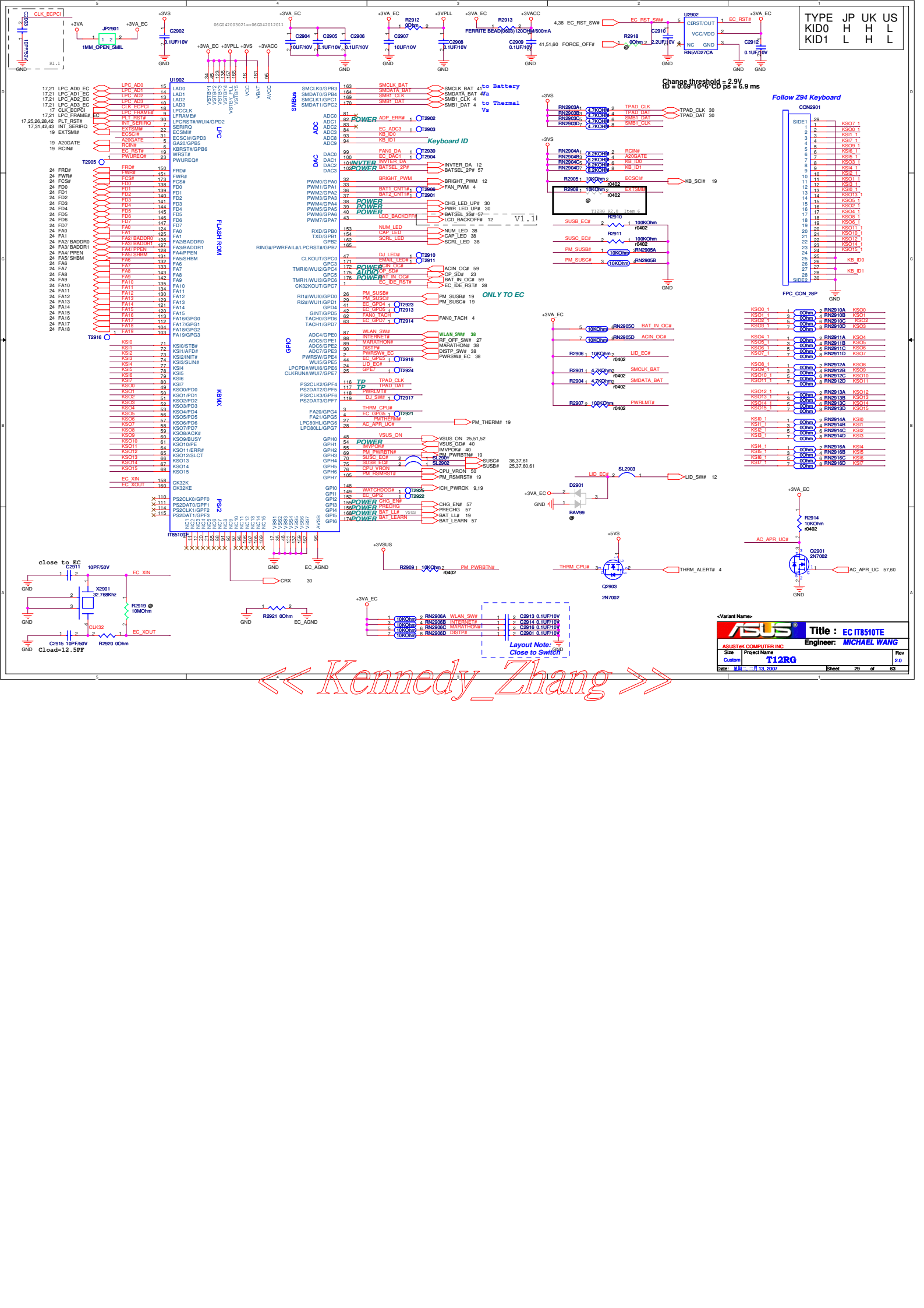
<Variant Name>

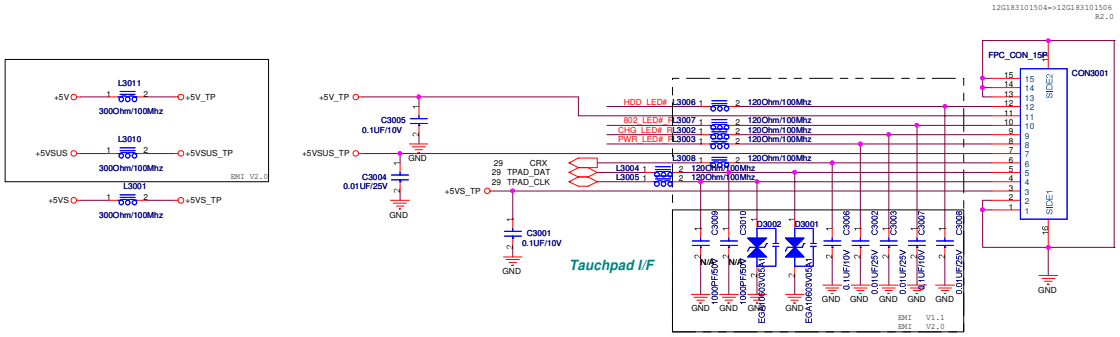
ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 27 of 63	



CD-ROM

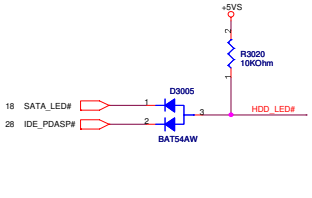



TYPE JP UK US
KID0 H H L
KID1 L H L
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
Follow Z94 Keyboard
ONLY TO EC
Layout Note:
Close to Switch
close to EC
Cload=12.5PF
U1902
IT8510TE
CON2901
FPC_CON_28P
Title : EC IT8510TE
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom
Project Name: T12RG
Rev: 2.0
Date: 13, 2007
Sheet 29 of 63
<Variant Name>
<< Kennedy_Zhang >>

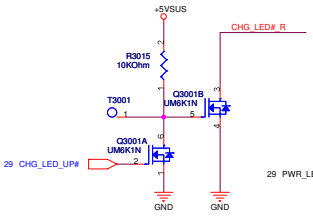


Touchpad

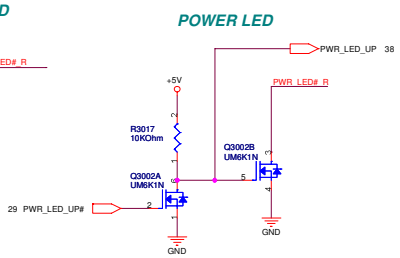
HDD LED



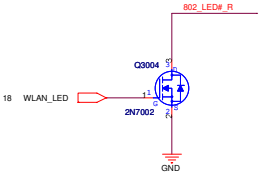
CHARGE LED



POWER LED



WLAN LED



<Variant Name>

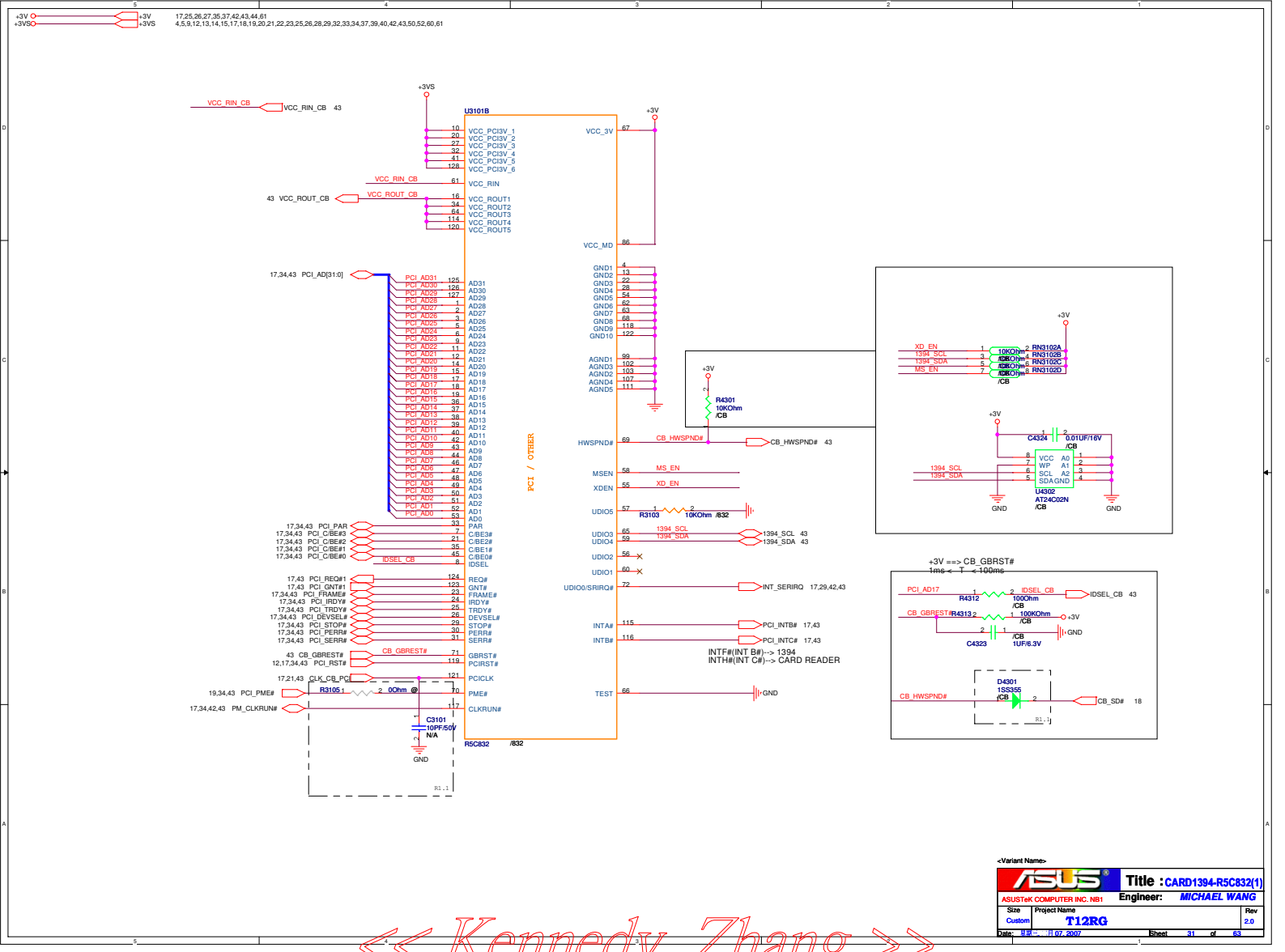
ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: MICHAEL WANG

Size	Project Name	Rev
A3	T12RG	2.0

Date: 星期一, 月 07, 2007 Sheet 30 of 63



<Variant Name>

Title : CARD1394-R5C832(1)

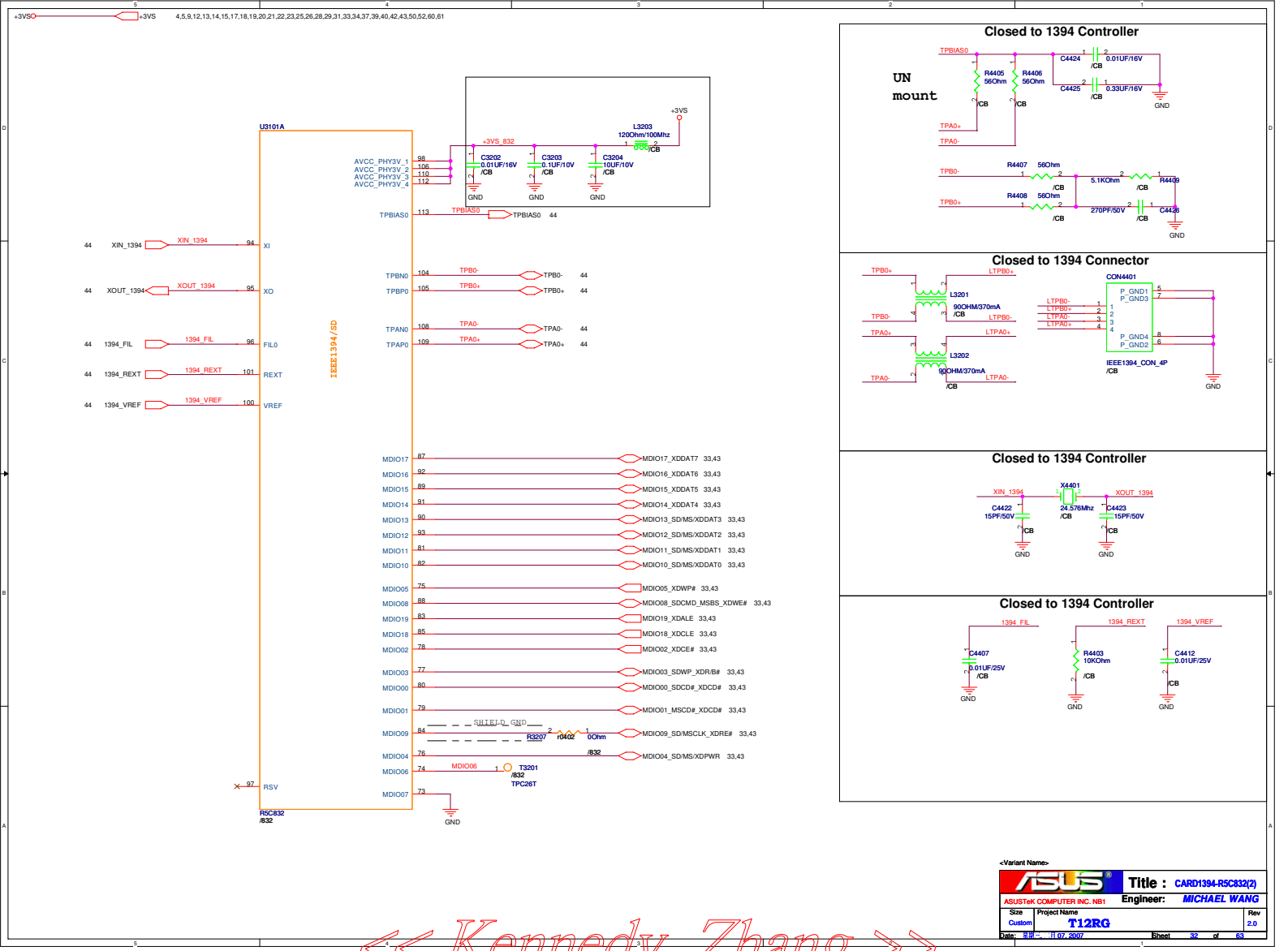
ASUSTeK COMPUTER INC. NB1

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 31 of 63

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

SD/MMC/MS/MS-PRO Card Reader Socket

32,43 MDIO17_XDDAT7 — MDIO17_XDDAT7
32,43 MDIO16_XDDAT6 — MDIO16_XDDAT6
32,43 MDIO15_XDDAT5 — MDIO15_XDDAT5
32,43 MDIO14_XDDAT4 — MDIO14_XDDAT4
32,43 MDIO13_SD/MS/XDDAT3 — MDIO13_SD/MS/XDDAT3
32,43 MDIO12_SD/MS/XDDAT2 — MDIO12_SD/MS/XDDAT2
32,43 MDIO11_SD/MS/XDDAT1 — MDIO11_SD/MS/XDDAT1
32,43 MDIO10_SD/MS/XDDAT0 — MDIO10_SD/MS/XDDAT0

32,43 MDIO05_XDWP# — MDIO05_XDWP#
32,43 MDIO08_SDCMD_MSBS_XDWE# — MDIO08_SDCMD_MSBS_XDWE#
32,43 MDIO19_XDALE — MDIO19_XDALE
32,43 MDIO18_XDCLE — MDIO18_XDCLE
32,43 MDIO02_XDCE# — MDIO02_XDCE#

32,43 MDIO03_SDWP_XDR/B# — MDIO03_SDWP_XDR/B#
32,43 MDIO00_SDCD#_XDCD# — MDIO00_SDCD#_XDCD#
32,43 MDIO01_MSCD#_XDCD# — MDIO01_MSCD#_XDCD#
32,43 MDIO09_SD/MSCLK_XDRE# — MDIO09_SD/MSCLK_XDRE#

12G340004402

+VCCCA
C3304 270P @
CON3301 CARD_READER_44P /CB

1	MS_GND1	XD_CD	23
2	MS_BS	XD_GND1	24
3	MS_DATA1	XD_R/B	25
4	MS_DATA0	XD_RE	26
5	MS_DATA2	XD_CE	27
6	MS_INS	XD_CLE	28
7	MS_DATA3	XD_ALE	29
8	MS_SCLK	XD_WE	30
9	MS_VCC	XD_WP	31
10	MS_GND2	XD_GND2	32
11	SD_DAT2	XD_D0	33
12	SD_DAT3	XD_D1	34
13	SD_CMD	XD_D2	35
14	SD_GND1	XD_D3	36
15	SD_VCC	XD_D4	37
16	SD_CLK	XD_D5	38
17	SD_GND2	XD_D6	39
18	NC1	XD_D7	40
19	SD_DAT0	XD_VCC	41
20	SD_DAT1	NC2	42
21	SD_CD_SW	SD_WP_SW	43
22	SD_CD_COM	SD_WP_COM	44
45	NP_NC1	NP_NC2	46
47	GND1	GND2	48

MDIO08_SDCMD_MSBS_XDWE#
MDIO11_SD/MS/XDDAT1
MDIO10_SD/MS/XDDAT0
MDIO12_SD/MS/XDDAT2
MSCD#
MDIO13_SD/MS/XDDAT3
MDIO09_SD/MSCLK_XDRE#
SD_DAT2
MDIO13_SD/MS/XDDAT3
MDIO08_SDCMD_MSBS_XDWE#
MDIO09_SD/MSCLK_XDRE#
MDIO10_SD/MS/XDDAT0
SD_DAT1
SDCD#
XD_CD#
MDIO03_SDWP_XDR/B#
MDIO09_SD/MSCLK_XDRE#
MDIO02_XDCE#
MDIO18_XDCLE
MDIO19_XDALE
MDIO08_SDCMD_MSBS_XDWE#
MDIO05_XDWP#
MDIO10_SD/MS/XDDAT0
MDIO11_SD/MS/XDDAT1
MDIO12_SD/MS/XDDAT2
MDIO13_SD/MS/XDDAT3
MDIO14_XDDAT4
MDIO15_XDDAT5
MDIO16_XDDAT6
MDIO17_XDDAT7
MDIO03_SDWP_XDR/B#
C3306 3300PF/50V N/A
C3305 270P @

+12VS — +12VS — 12,37,61
+3VS — +3VS — 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61

+3VS
Q3306 IRLML5103PBF /CB
R3305 100KOhm /CB
+VCCCA
C3308 0.1UF/10V /CB
Place as close to card reader socket as possible
32,43 MDIO04_SD/MS/XDPWR

+VCCCA
C3307 0.01UF/10V @
C3309 0.01UF/10V /CB
C3310 0.01UF/10V /CB
R3306 150K /CB
C3311 2.2UF/6.3V /CB
Place as close to card reader socket as possible

To coorect the problem when MS Duo adaptor is in use.

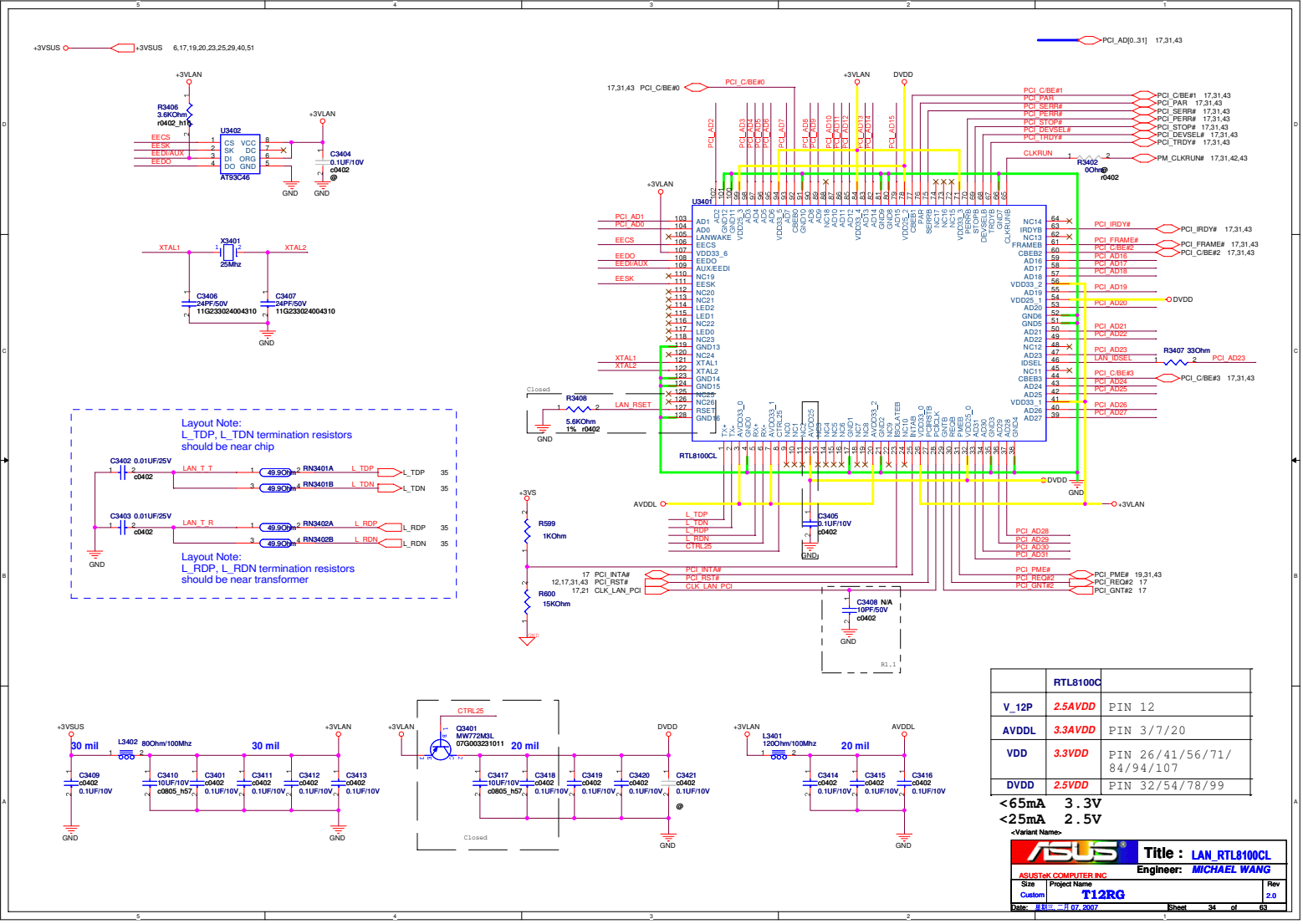
+12VS
SDCD#
R3301 10KOhm /CB
Q3301A UM6K1N /CB
GND
MDIO11_SD/MS/XDDAT1
Q3301B UM6K1N /CB
SD_DAT1
MDIO12_SD/MS/XDDAT2
Q3302A UM6K1N /CB
SD_DAT2

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

+3VS
R3302 10KOhm /CB
XD_CD#
SDCD#
D3301 DAP202K /CB
R3208 0Ohm r0402 @
Q3302B UM6K1N /CB
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D3302 DAP202K /CB
+3VS
R3304 10KOhm /CB
MSCD#
For Memory Stick Duo Adaptor shielding ground issue

<Variant Name>

ASUSTek COMPUTER INC
Project Name: T12RG
Engineer: MICHAEL WANG
Size: Custom
Title : CardReader
Rev: 2.0
Date: 星期三, 一月 07, 2007
Sheet 33 of 63



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

<65mA 3.3V
<25mA 2.5V
<Variant Name>

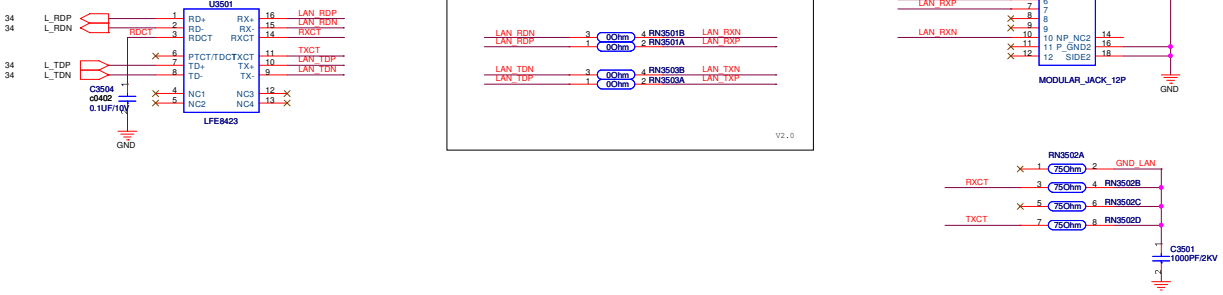
ASUSTeK COMPUTER INC	Title : LAN_RTL8100CL	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期二, 十月 07, 2007	Sheet 34 of 63	

<< Kennedy_Zhang >>

+3V +3V 17,25,26,27,31,37,42,43,44,61

LAN PORT

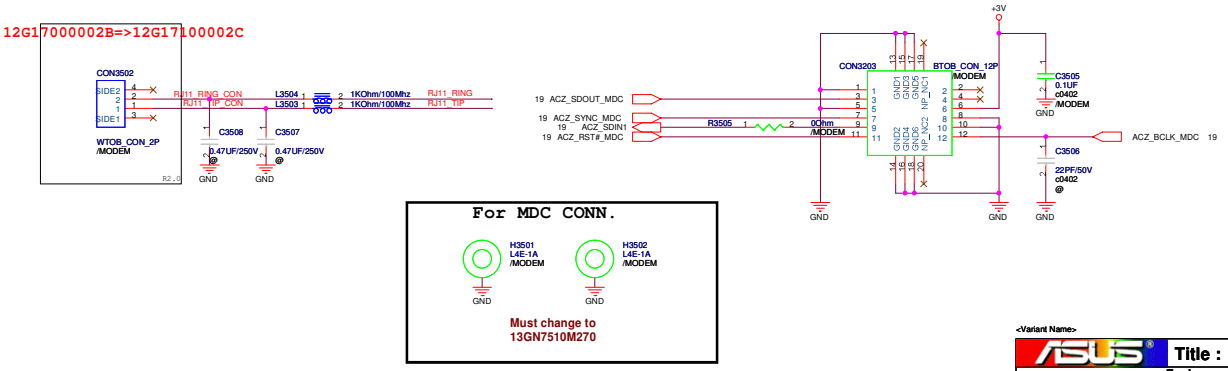
12G142111120



MDC CONNECTOR

12G161200124

12G17000002B=>12G17100002C



For MDC CONN.

H3501 L4E-1A /MODEM

H3502 L4E-1A /MODEM

GND

Must change to 13GN7510M270

<Variant Name>

Title : RJ11/45 & MDC

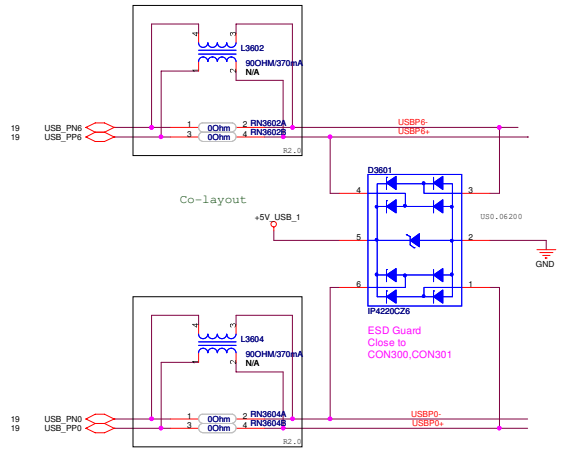
Engineer: MICHAEL WANG

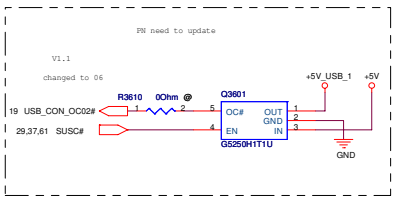
ASUSTeK COMPUTER INC

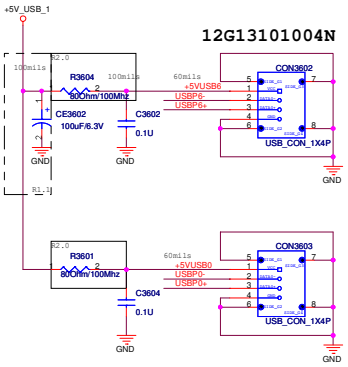
Size	Project Name	Rev
Custom	T12RG	2.0

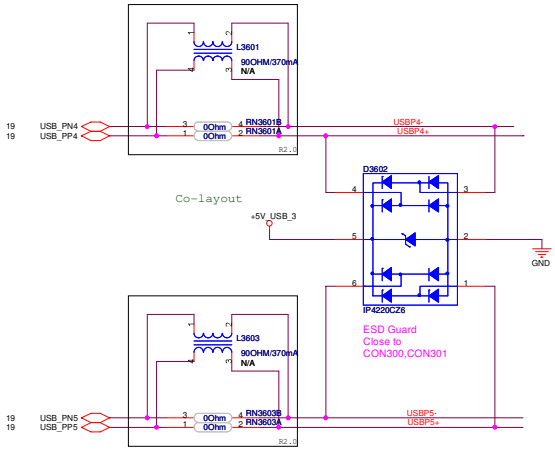
Date: 星期三, 二月 07, 2007 Sheet 35 of 63

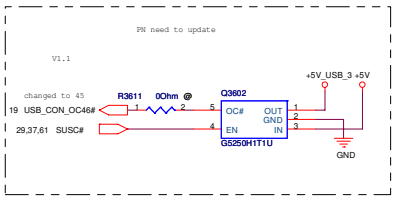
<< Kennedy_Zhang >>

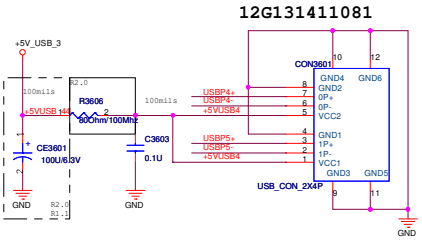






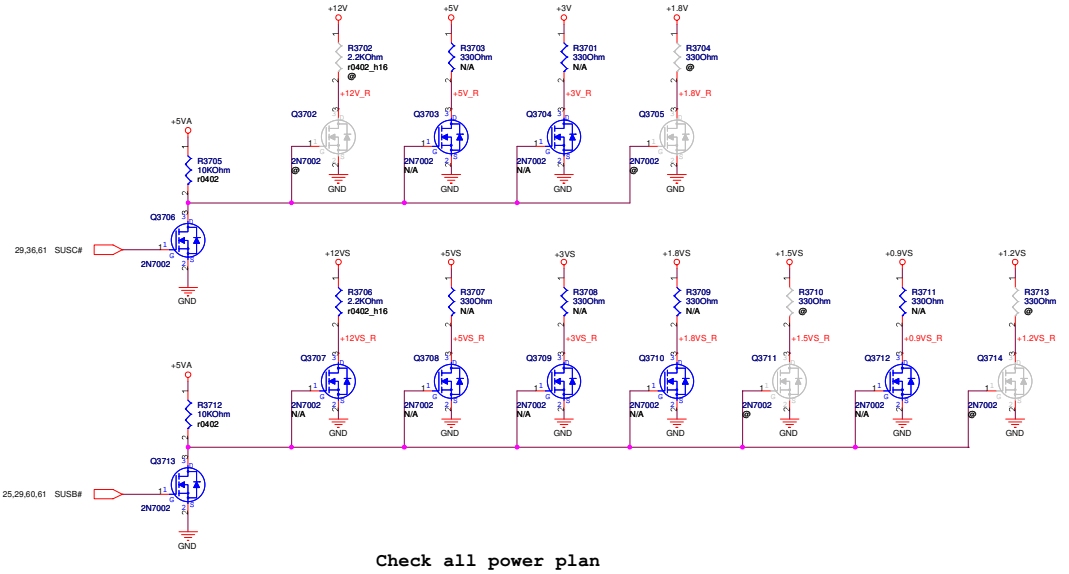






<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 2.0
Date: 星期一, 一月 07, 2007	Sheet 36 of 63	

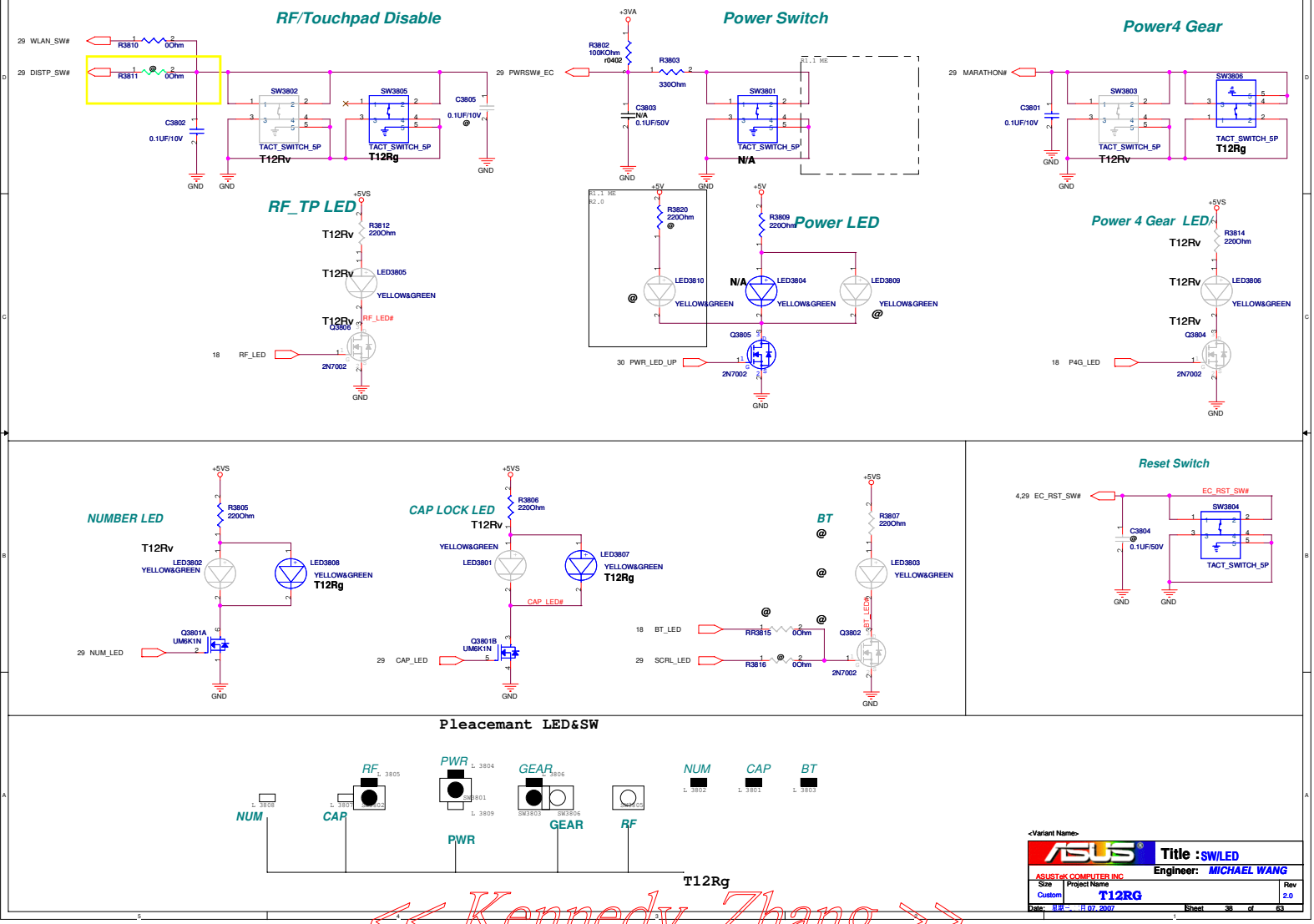


Check all power plan

<Variant Name>

ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期三, 一月 07, 2007	Sheet 37 of 63	

Main Board SW & LED



<Variant Name>

Title : SW/LED

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

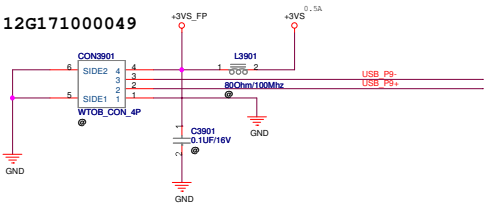
Size	Project Name	Rev
Custom	T12RG	2.0

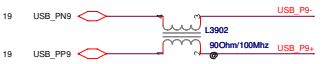
Date: 星期二, 四 07, 2007 Sheet 38 of 63

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT





<Variant Name>

Title : FINGER PRINT

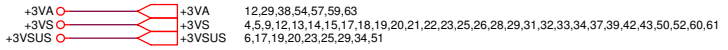
ASUSTeK COMPUTER INC

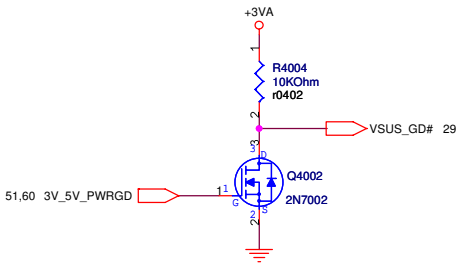
Engineer: MICHAEL WANG

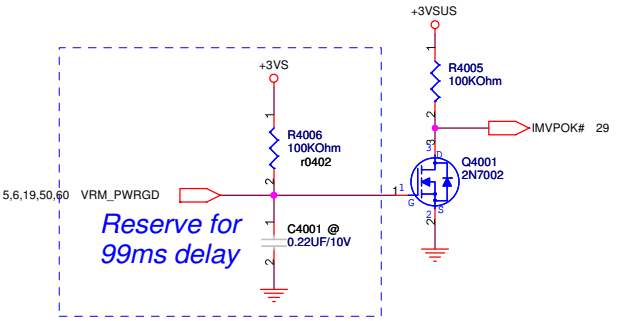
Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 39 of 63

<< Kennedy_Zhang >>







<Variant Name>

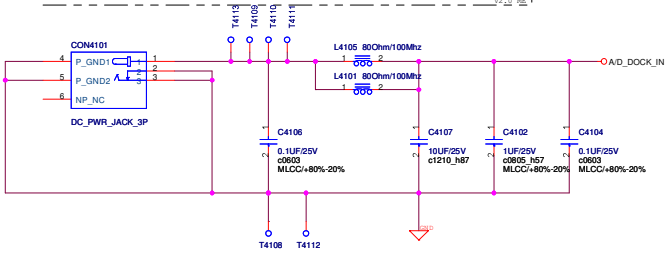
ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: MICHAEL WANG	
Size: A4	Project Name: T12RG	Rev: 2.0
Date: 星期三, 二月 07, 2007	Sheet 40 of 63	

A/D_DOCK_IN
BAT_CON
AC_BAT_SYS

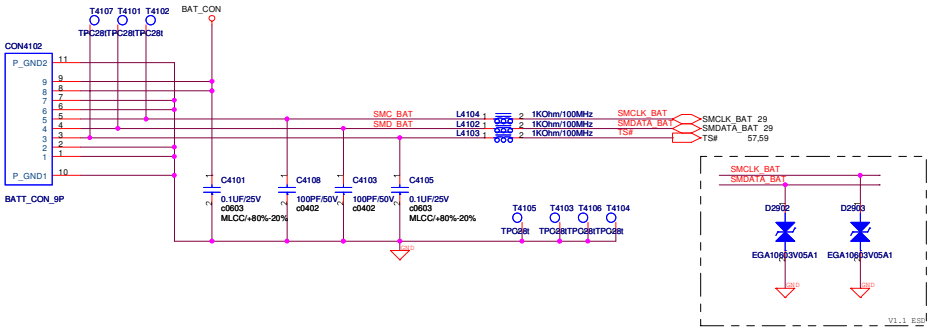
A/D_DOCK_IN 57,59
BAT_CON 57
AC_BAT_SYS 12,50,51,52,53,54,57,60

12G145002034=>12G14530103E=>12G14530103V

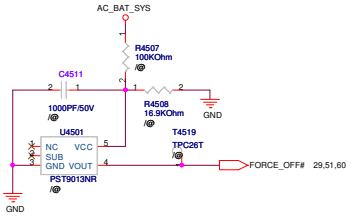
V2.0 ME



12G20001090G



Without Battery & Pull out Adapter
RESERVED



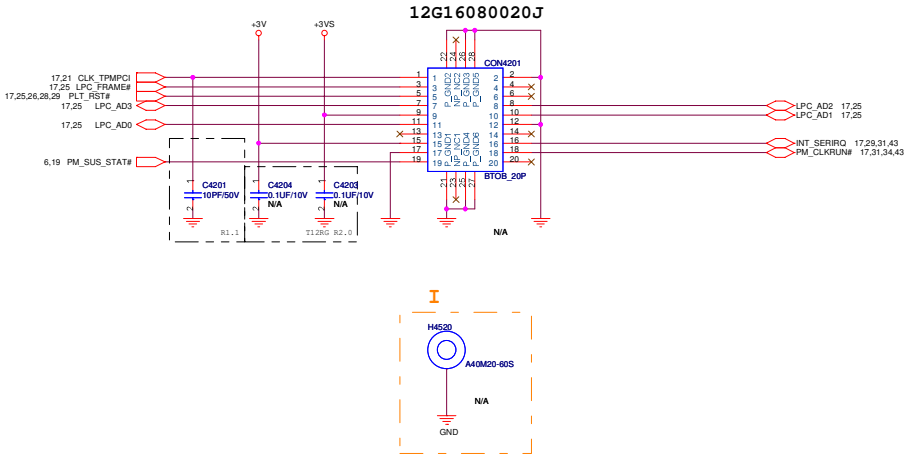
<Variant Name>

ASUSTek COMPUTER INC	Project Name: T12RG	Engineer: MICHAEL WANG
Size: Custom	Title : DC IN	Rev: 2.0
Date: 星期二, 十月 07, 2007	Sheet 41 of 63	

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

+3V +3V 17,25,26,27,31,35,37,43,44,61

TPM Module CON
RESERVED

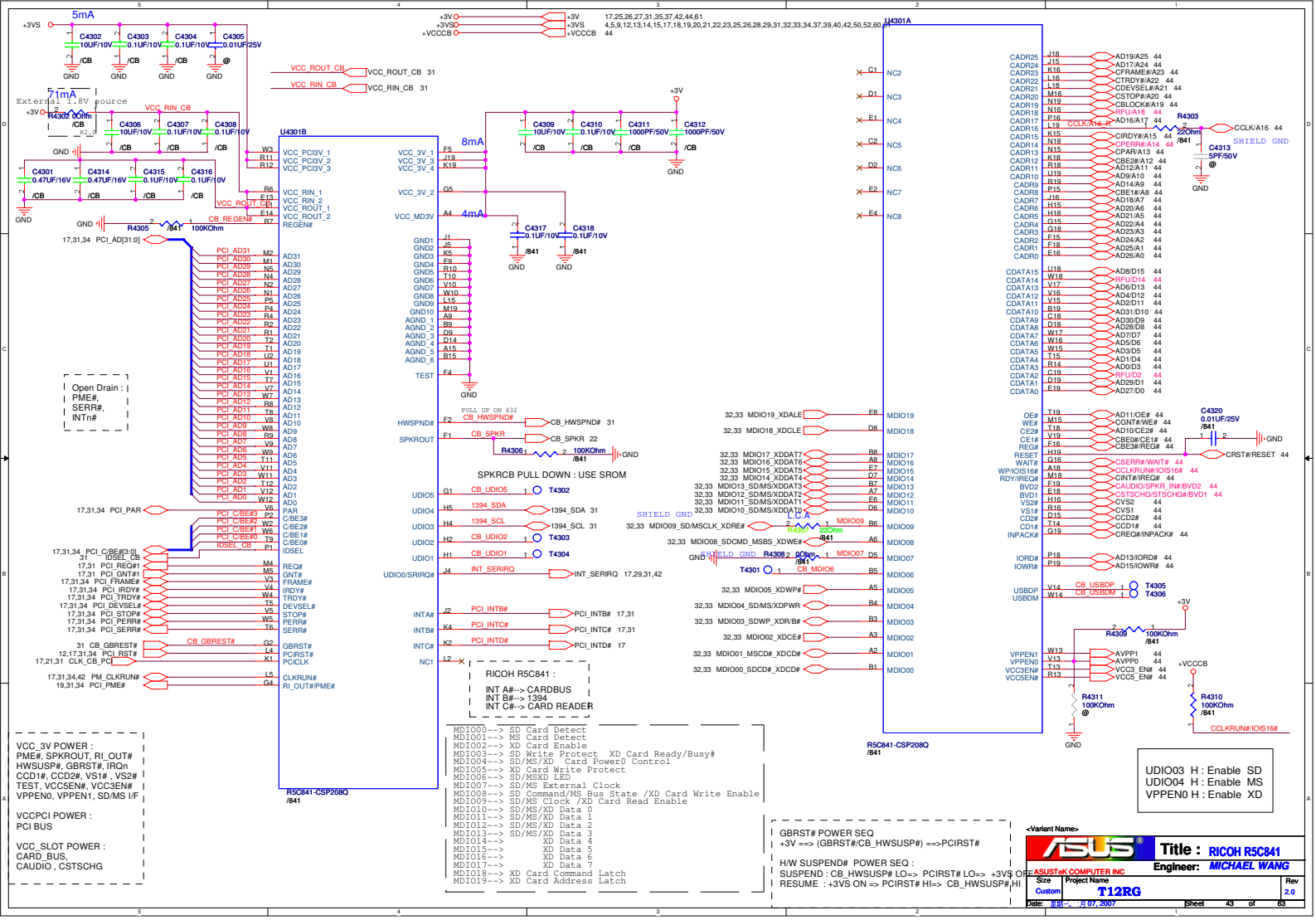


For TPM CONN.

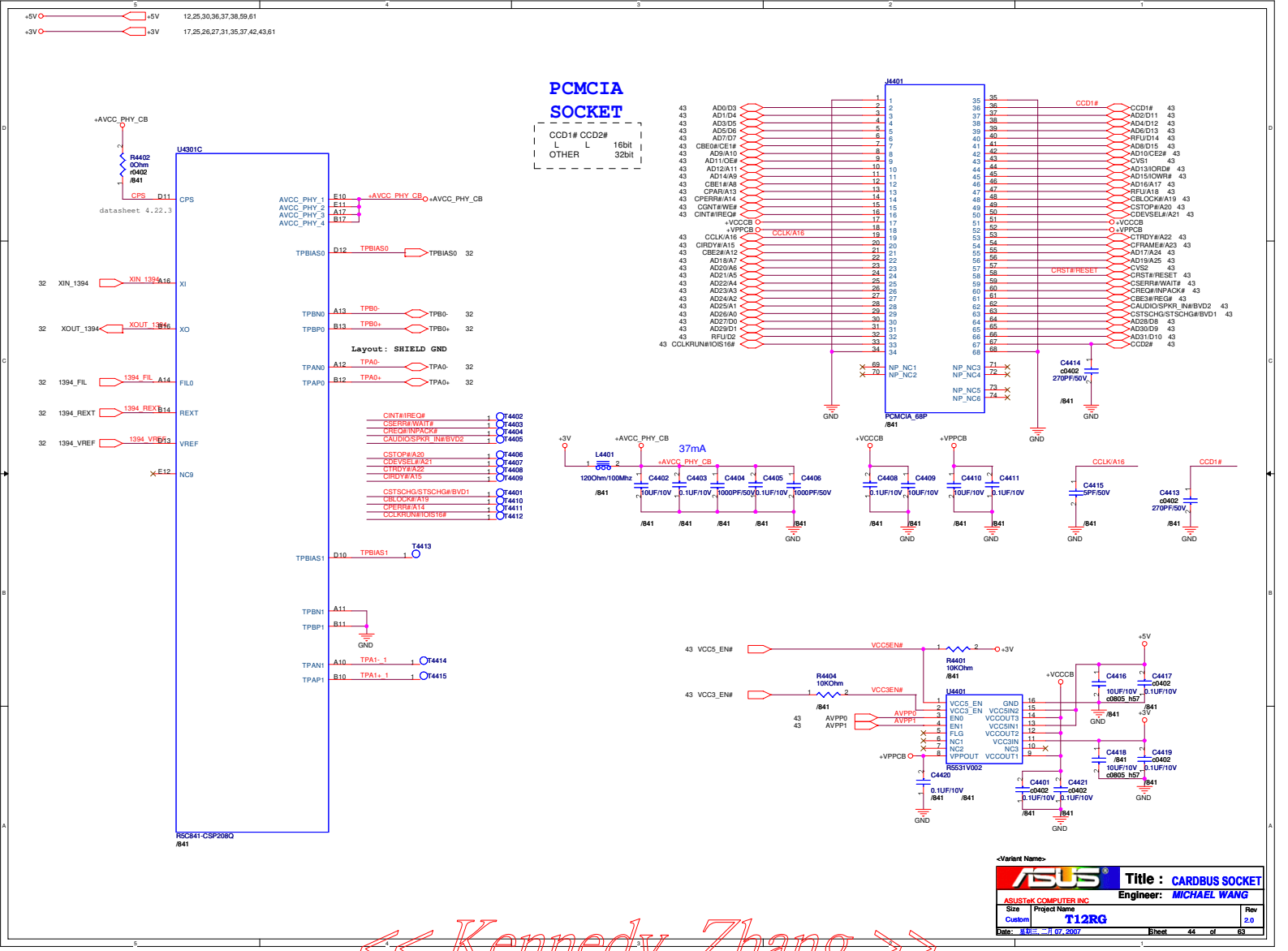
<Variant Name>

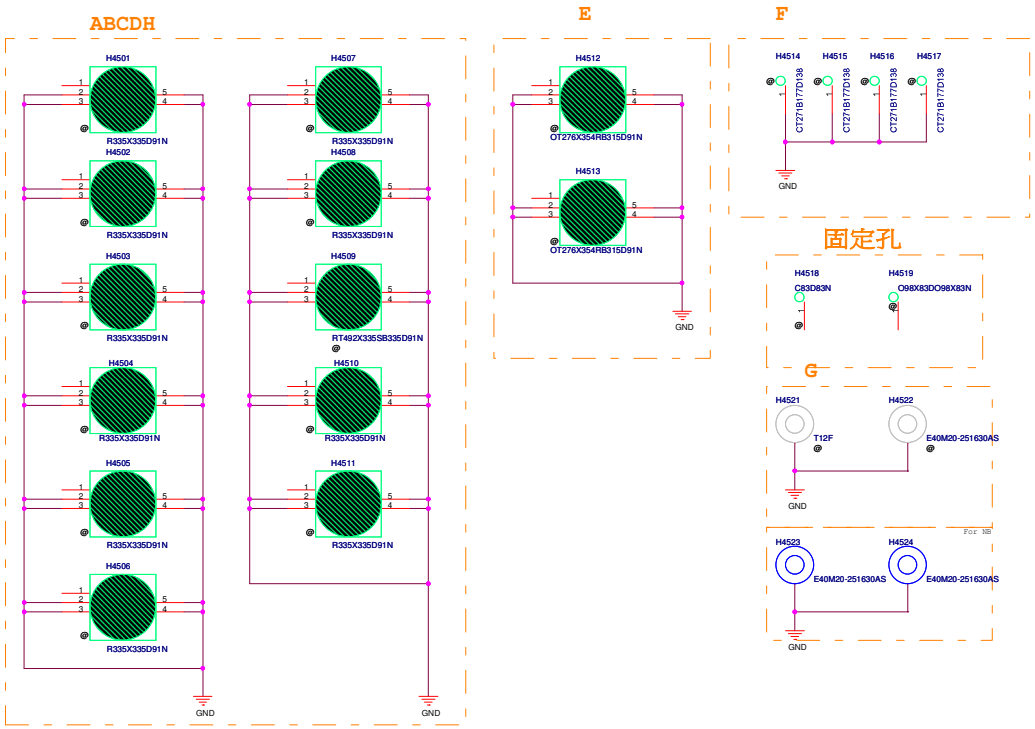
ASUSTek COMPUTER INC	Project Name: T12RG	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 42 of 63	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>





<Variant Name>

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12RG	Rev: 2.0
Date: 星期三, 一月 07, 2007	Sheet 45 of 63	

<Variant Name>

Title : HISTORY

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期一, 一月 07, 2007 Sheet 46 of 63

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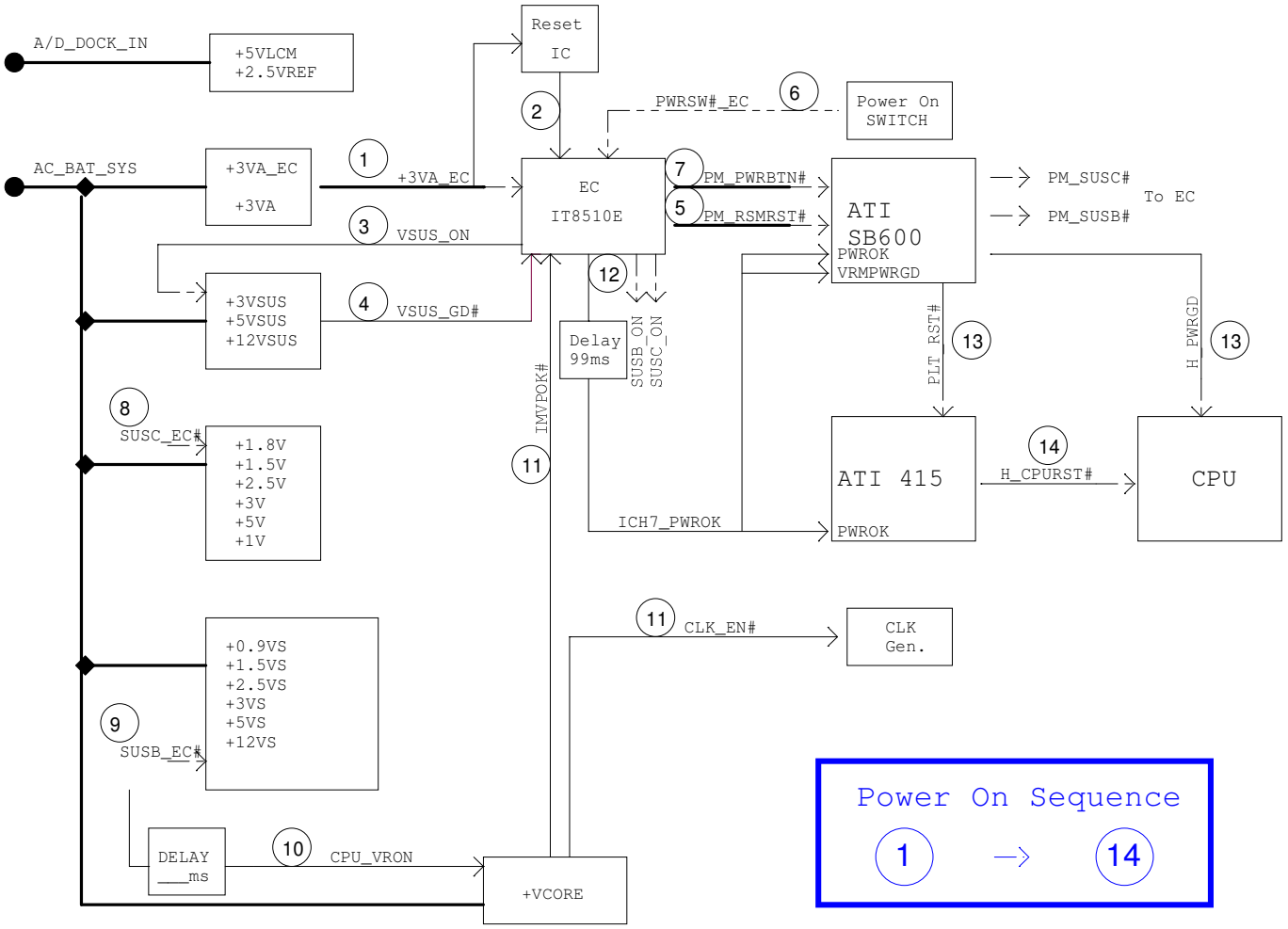

<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: 星期二, 一月 07, 2007 Sheet 47 of 63

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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

ASUSTeK COMPUTER INC

Title : GPIO Setting

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12RG	2.0

Date: [illegible] 07, 2007 Sheet 48 of 63

<< Kennedy_Zhang >>

T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9.All PCI clock added 6.8 pF to decrease skew.
10.PWM connected to EC and back-light connected to NB
11.D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12.page 19, added BT_DET# to detect BT.
13.Page 19, adjust USB OC ping to correspond USB port
14.Page 25, modification NEW CARD debug circuit to correspond new debug card
15.page 28, we used correctly capacity for customer request.
16.page 36, we used LDO with over current protect IC
17.page 41, DC in connector add 2nd source.
ME modify
1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加鎖絲繞付記號

6.DDR2 added 2nd source
P/N :12G025022004
DDR2 DIMM 200P,1.8V,H:4mm,STD
FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.總版圖修改

T12R V2.0 Modify History

1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 10U with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006-3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

T12Rg V1.0 modify from T12R V2.0

1. To modify BOM include LED(color&placement), SW(placement), HDD(PATA TO SATA), PCCAM(unmount), internal MIC(unmount) and R5C841(added 1394 cardreader and PCMCIA).

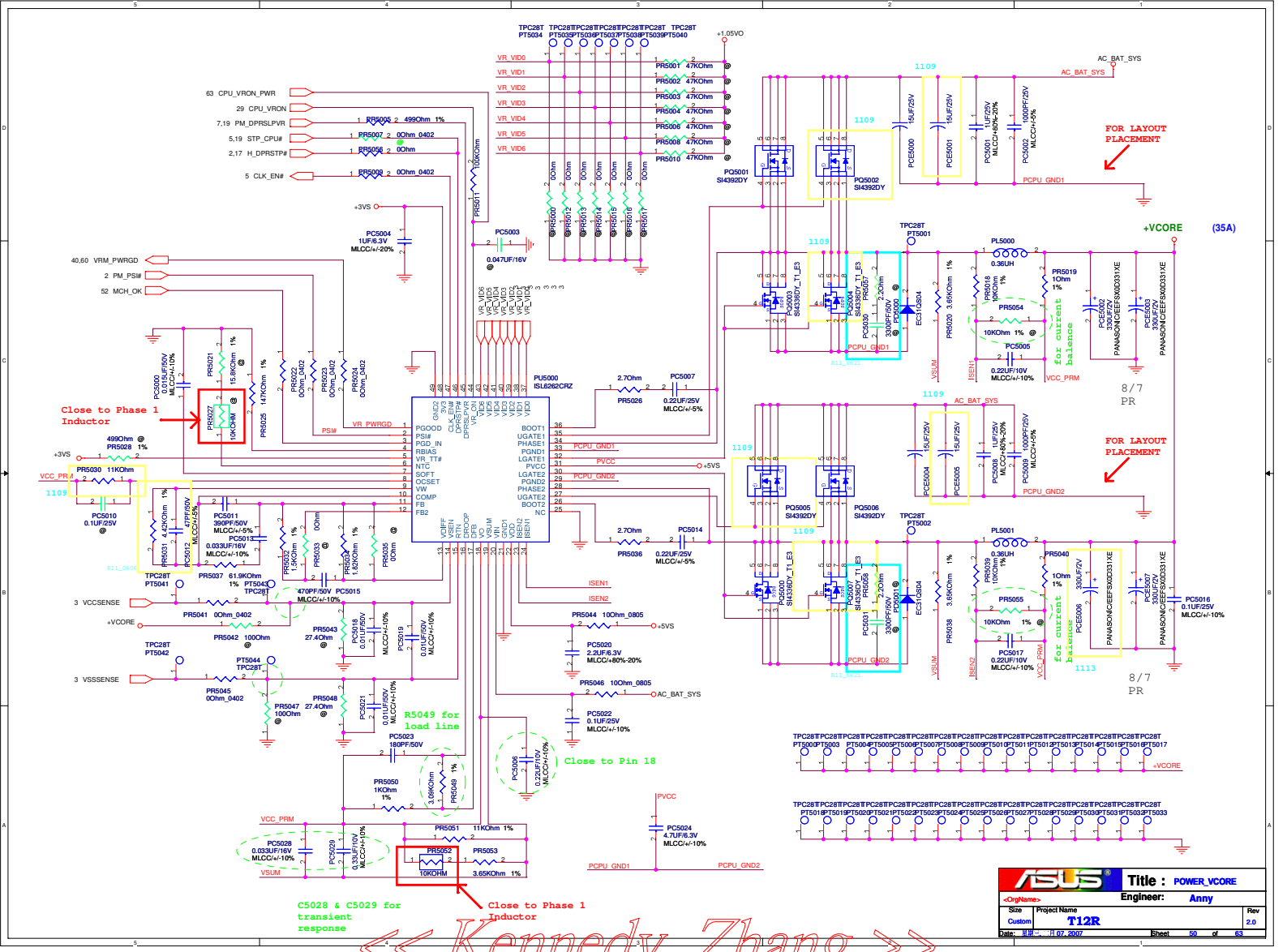
T12Rg V2.0

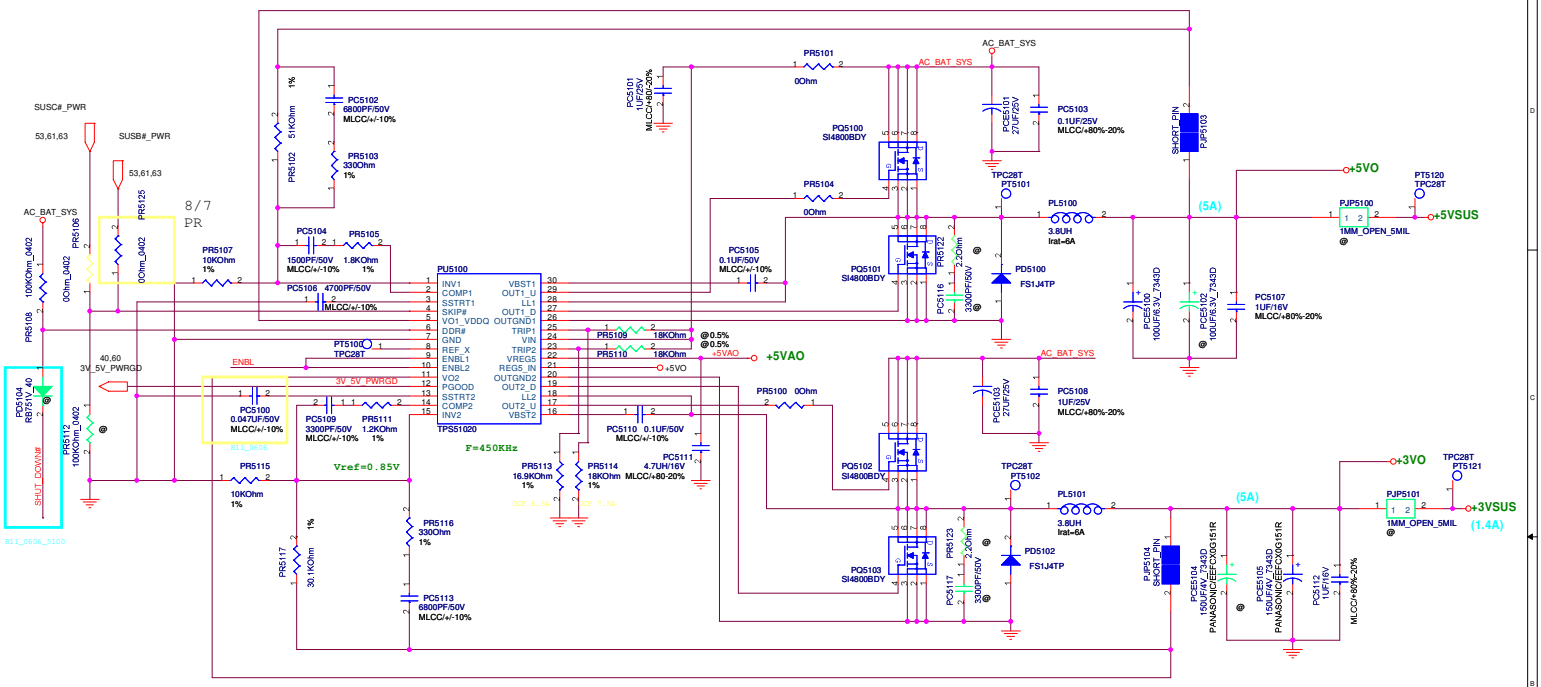
1. Page 12, L1203 0 Ohm to bead, EMI request.
2. Page 12, L1204 and L1205 0 Ohm to bead and mount C1222 C1223, EMI request.
3. Page 12, mount L1214 L1215 Ohm for added internal speaker.
4. Page 12, mount L1206, EMI request.
5. Page 6, R2301 and R2304 10K to 12K for 2W speaker..
6. Page 6, modify BOM, unmount R2908.

	X51 PCB X51	T12RG PCB T12R	T12RG PCB T12R	T12Rv 2.0 PCB T12R	T12Rv 2.1 PCB X51
NB	415ME	415ME	415ME	415MD	415ME
SB	SB600 A21	SB600 A21	SB600 A21	SB600 A13	SB600 A21
AUDIO	660VD	660VD	660VD	660VD	
SPDIF	N/A	N/A	N/A	N/A	
R5C832	N/A	N/A	N/A	N/A	
R5C841	OK	OK	OK	N/A	
1394	N/A	OK	OK	N/A	
CARD READER	OK	OK	OK	N/A	
PCMCIA	OK	OK	OK	N/A	
NEW CARD	N/A	N/A	N/A	N/A	
TPM	N/A	OK	OK	N/A	
BT	OK	N/A	N/A	N/A	
PC_CAM	N/A	N/A	N/A	OK	
INT. MIC.	N/A	OK	OK	OK	
MODEN	OK	N/A	OK	N/A	
TV	N/A	N/A	N/A	N/A	
SPEAKER	1.5W	2W	2W	1.5W	

ASUSTeK Computer Inc.
Title : HISTORY
Engineer:
Size: B | Project Name: T12RG | Rev: 1.0
Date: | Sheet of

<< Kennedy_Zhang >>


+VCORE (35A)
FOR LAYOUT PLACEMENT
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
for current balance
PU5000 ISL6262CRZ
Title : POWER_VCORE
Engineer: Anny
T12R
<< Kennedy_Zhang >>



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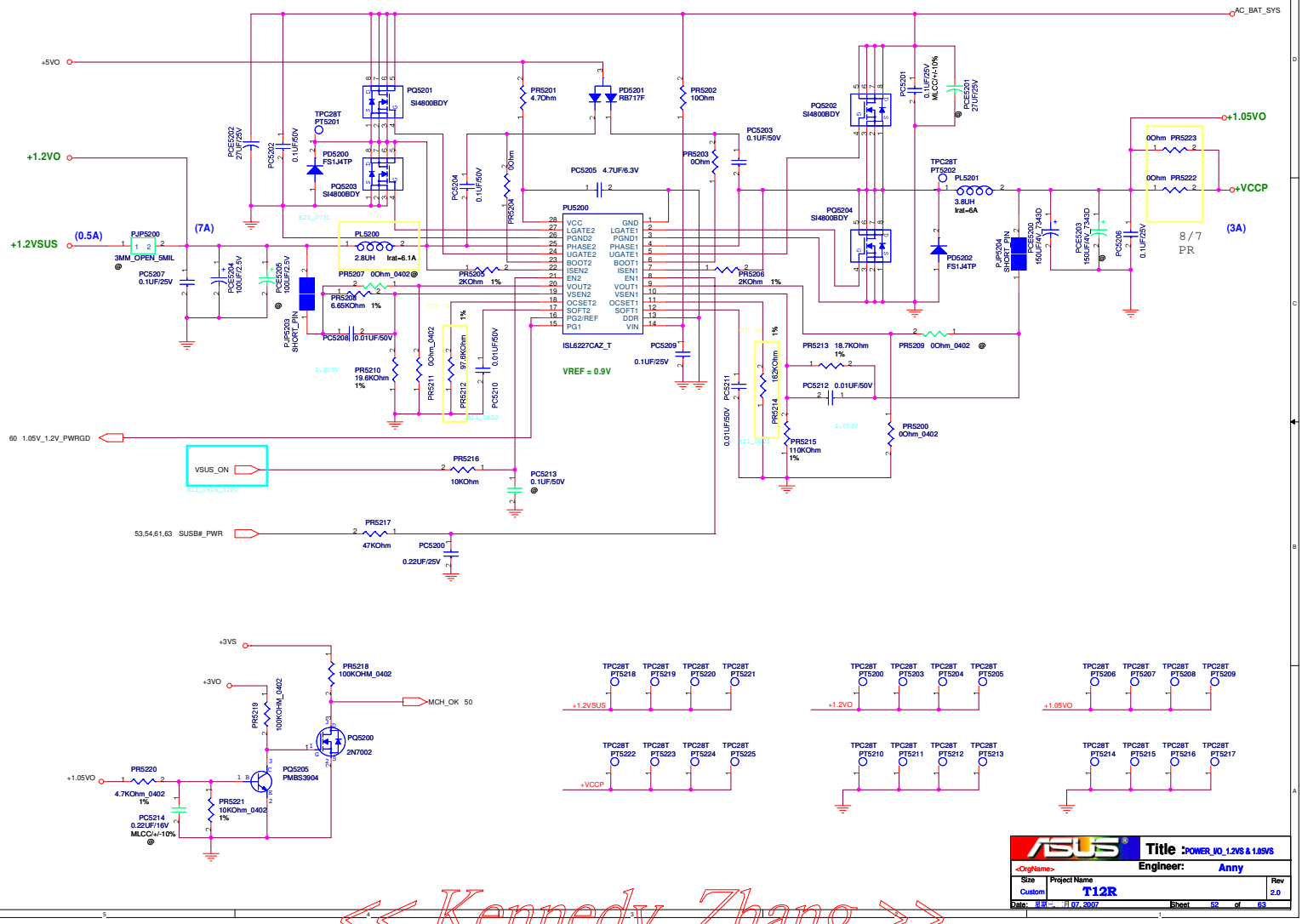
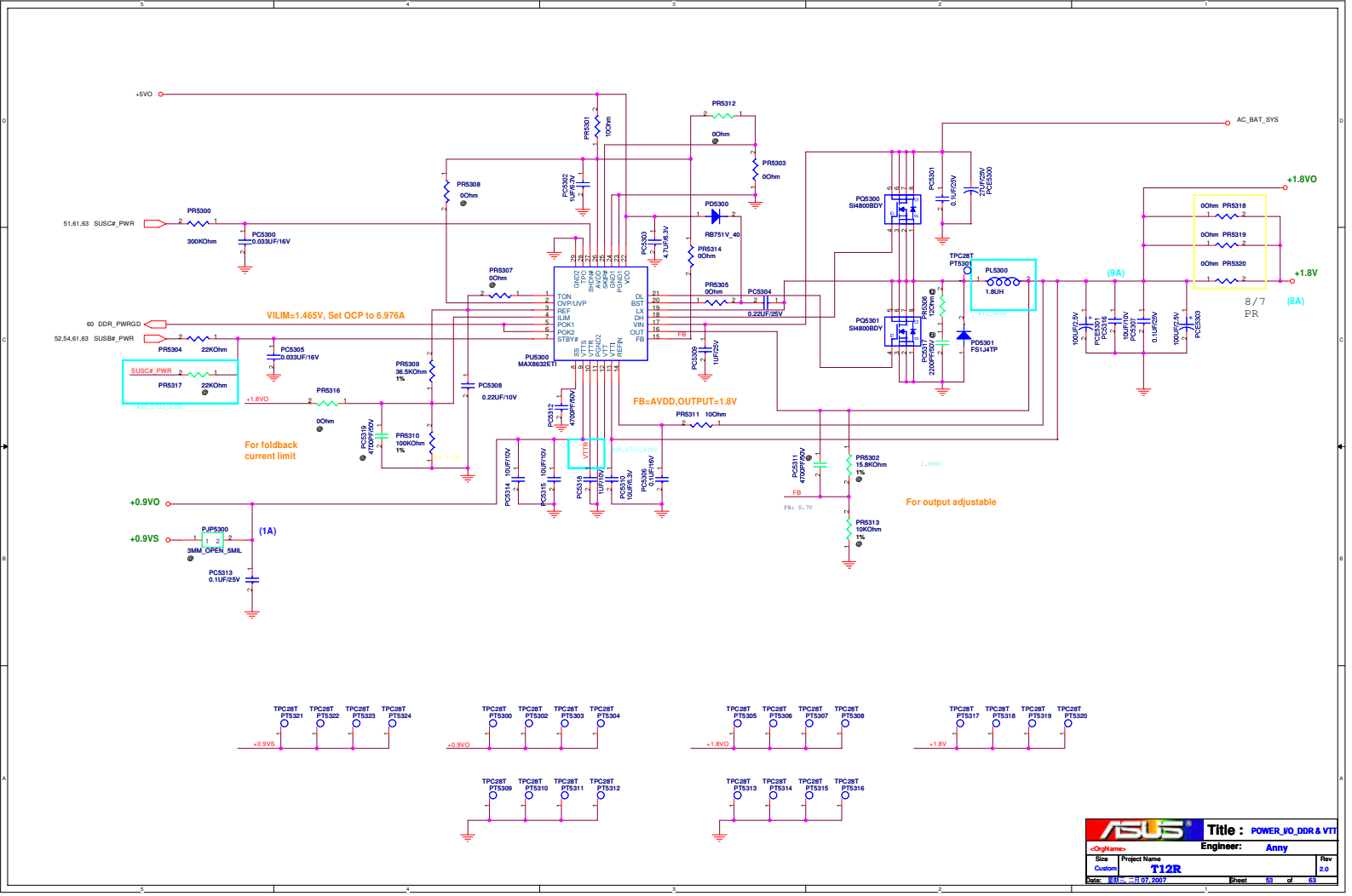
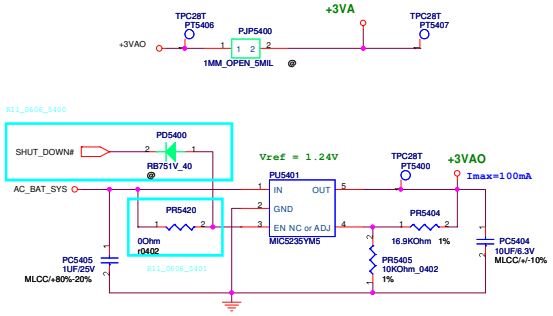


<< Kennedy_Zhang >>

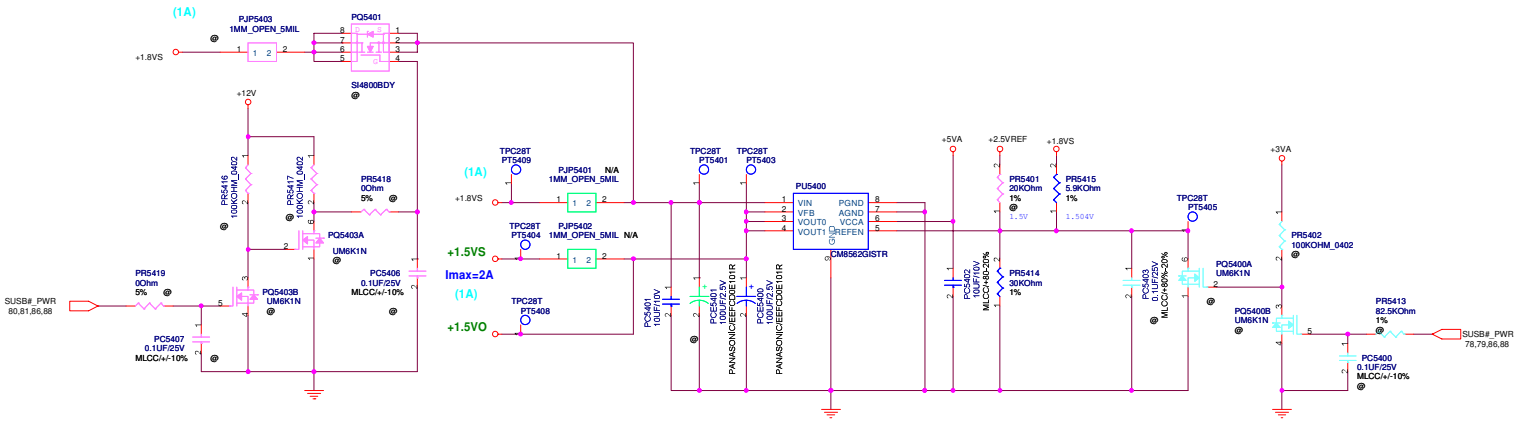


<< Kennedy_Zhang >>

+3VAO



+2.5VS



ASUS

Title : POWER_I/O_+3VA & +2.5V

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12R	2.0

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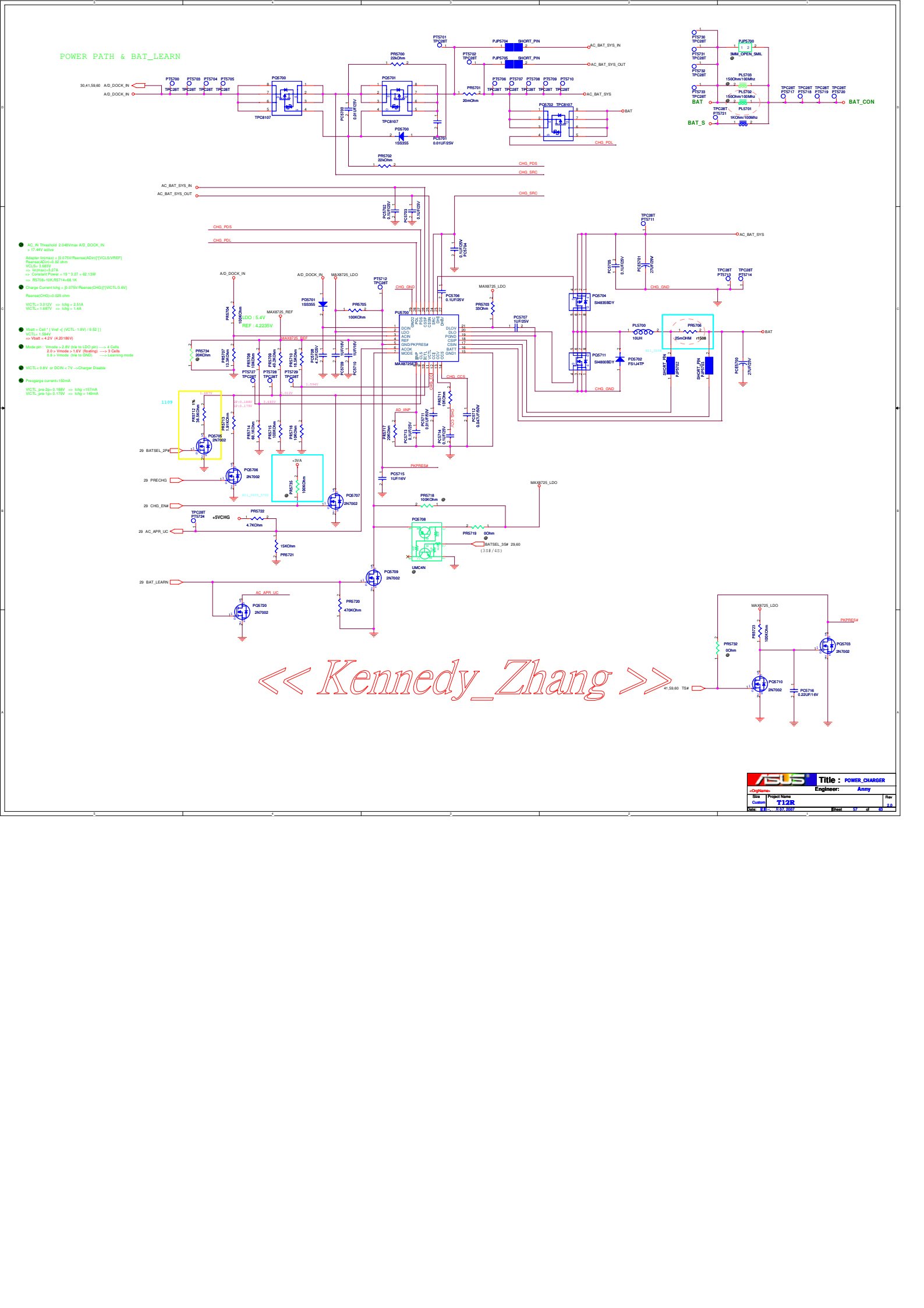

- AC_IN Threshold 2.048Vmax A/D_DOCK_IN
  > 17.44V active

  Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
  Rsense(ADin)=0.02 ohm
  VCLS= 3.683V
  => Iin(max)=3.27A
  => Constant Power = 19 * 3.27 = 62.13W
  => R5708=10K,R5714=68.1K
- Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

  Rsense(CHG)=0.025 ohm

  VICTL= 3.012V => Ichg = 2.51A
  VICTL= 1.687V => Ichg = 1.4A
- Vbatt = Cell * [Vref +[(VCTL- 1.6V) / 9.52]]
  VCTL= 1.584V
  => Vbatt = 4.2V (4.20186V)
- Mode pin : Vmode > 2.8V (Hiz to LDO pin) ----> 4 Cells
  2.0 > Vmode > 1.6V (floating) ----> 3 Cells
  0.8 > Vmode (Hiz to GND) ----> Learning mode
- VICTL< 0.8V or DCIN < 7V ->Charger Disable
- Precgarge current=150mA

  VICTL_pre-2p= 0.188V => Ichg =157mA
  VICTL_pre-1p= 0.179V => Ichg = 149mA

ASUS	Title : POWER_CHARGER		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
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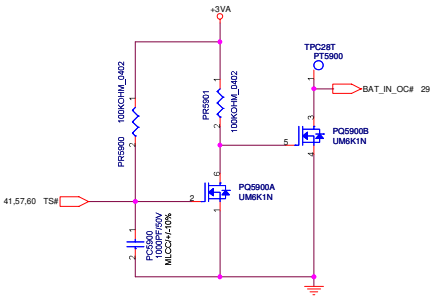
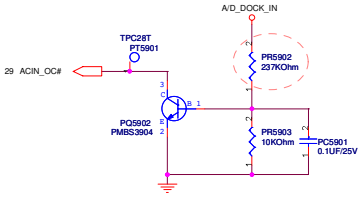
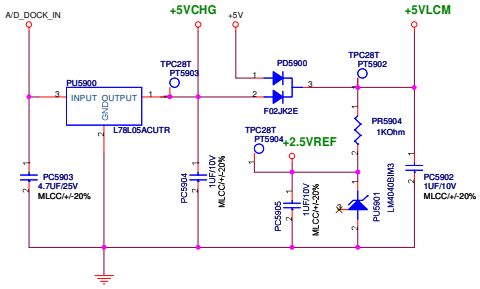
BATTERY IN DETECT



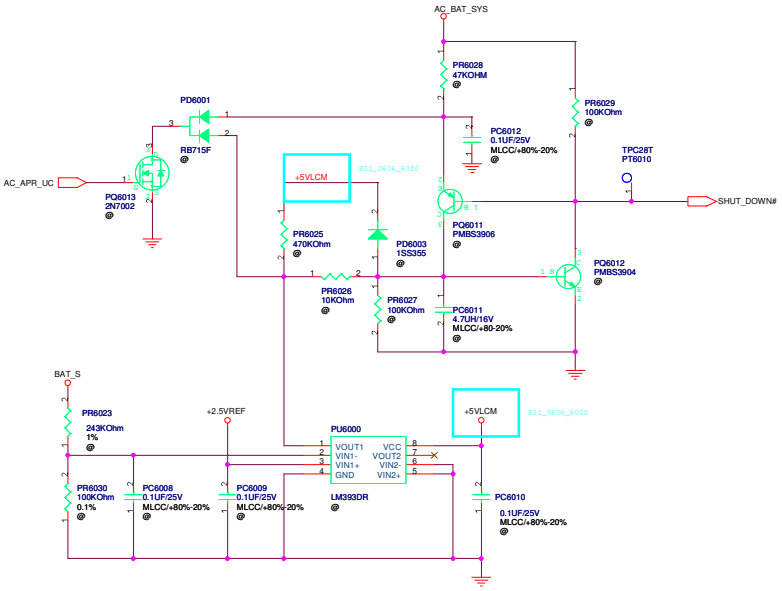
ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF

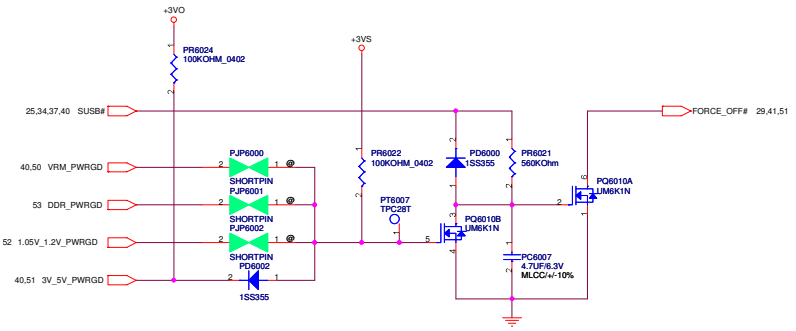


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: 星期一, 四 07, 2007	Sheet 59 of 63	



	8.575V	11.625V
R6023	243KOhm 10G2132433130 30 1%	365KOhm 10G2133653130 10 1%
R6024	100KOhm 10G2131003230 10 0.1%	100KOhm 10G2131003230 10 0.1%

POWER GOOD DETECTER



TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.2V_PWRGD

Title : POWER_PROTECT

<OrgName> Engineer: Anny

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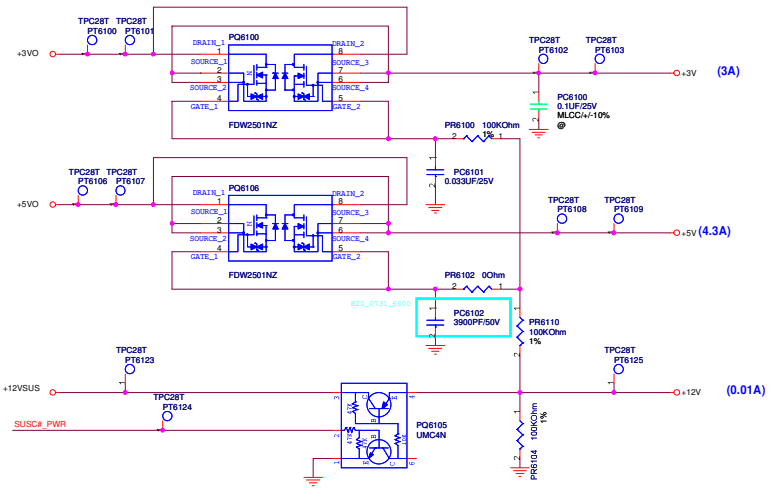
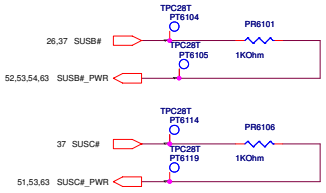
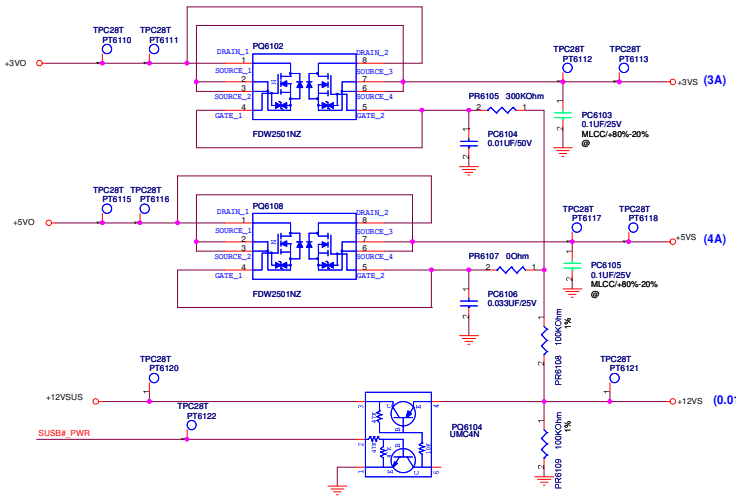
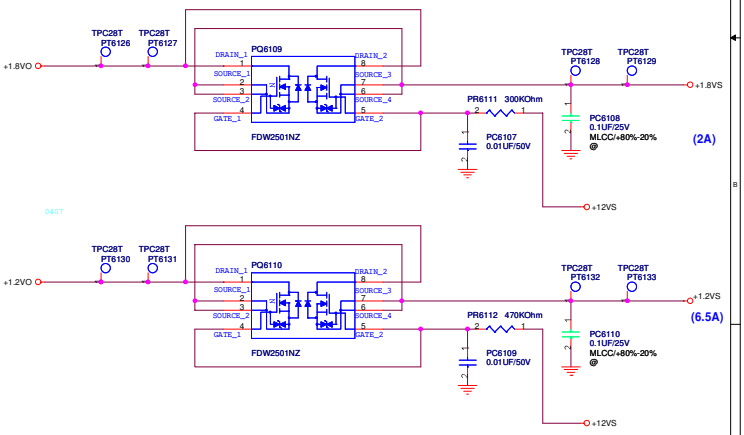
SUSC#_PWR POWER





SUSB#_PWR POWER





Title : POWER_LOAD SWITCH			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: T12R		Rev: 2.0
Date: 星期二, 一月 07, 2007	Sheet 61 of 63		

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AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57

+3VA → +3VA 4,12,20,22,29,37,38,40,54,59

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,61

+3VO → +3VO 51,52,60,61

+3VSUS → +3VSUS 18,19,20,25,29,34,40,51

+5VSUS → +5VSUS 20,30,51,60

+3V → +3V 12,18,26,27,31,37,42,43,44,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 36,37,54,61

+12VS → +12VS 12,22,27,33,37,61

+5V → +5V 9,12,30,36,37,44,59,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,37,38,50,61

+1.2VO → +1.2VO 52

+1.2VSUS → +1.2VSUS 52

+1.2VS → +1.2VS 61

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,37,53

+VCCP → +VCCP 2,6,9,20,52

+VCCP_AGTL+ → +VCCP_AGTL+ 2,3,5,6,9

+VCCP_GMCH → +VCCP_GMCH 9,10

+VCCP_ICH → +VCCP_ICH 17,20

+0.9VS → +0.9VS 16,37,53

BAT → BAT 30,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 57,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST

+3VA → PJP6300 (SGL_JUMP, @) → CPU_VRON_PWR 50

+3VA → PJP6301 (SGL_JUMP, @) → SUSB#_PWR → SUSB#_PWR 52,53,54,61

+3VA → PJP6302 (SGL_JUMP, @) → SUSC#_PWR → SUSC#_PWR 51,53,61

+3VA → PJP6303 (SGL_JUMP, @) → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
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R2.0

Item	Before	After	Reason	Owner	Date
R20_1109_50		Add PCE5001 PCE5005, PQ5002, PQ5004, PQ5005 and PQ5007	VCORE:CPU upgrade to merom reflash		2006.11.09
R20_1109_50	9.31K	11K	VCORE: PR5030 modify to 11K to Increase OCP.		2006.11.09
R20_1109_57	PR5712 and PQ5705 were unmounted	PR5712:36.5K and PQ5705 was mounted.	Charger: Modify PR5712 and PQ5705 for 3S1P select.		2006.11.09

ASUS Title : POWER_PIC

<OrgName> Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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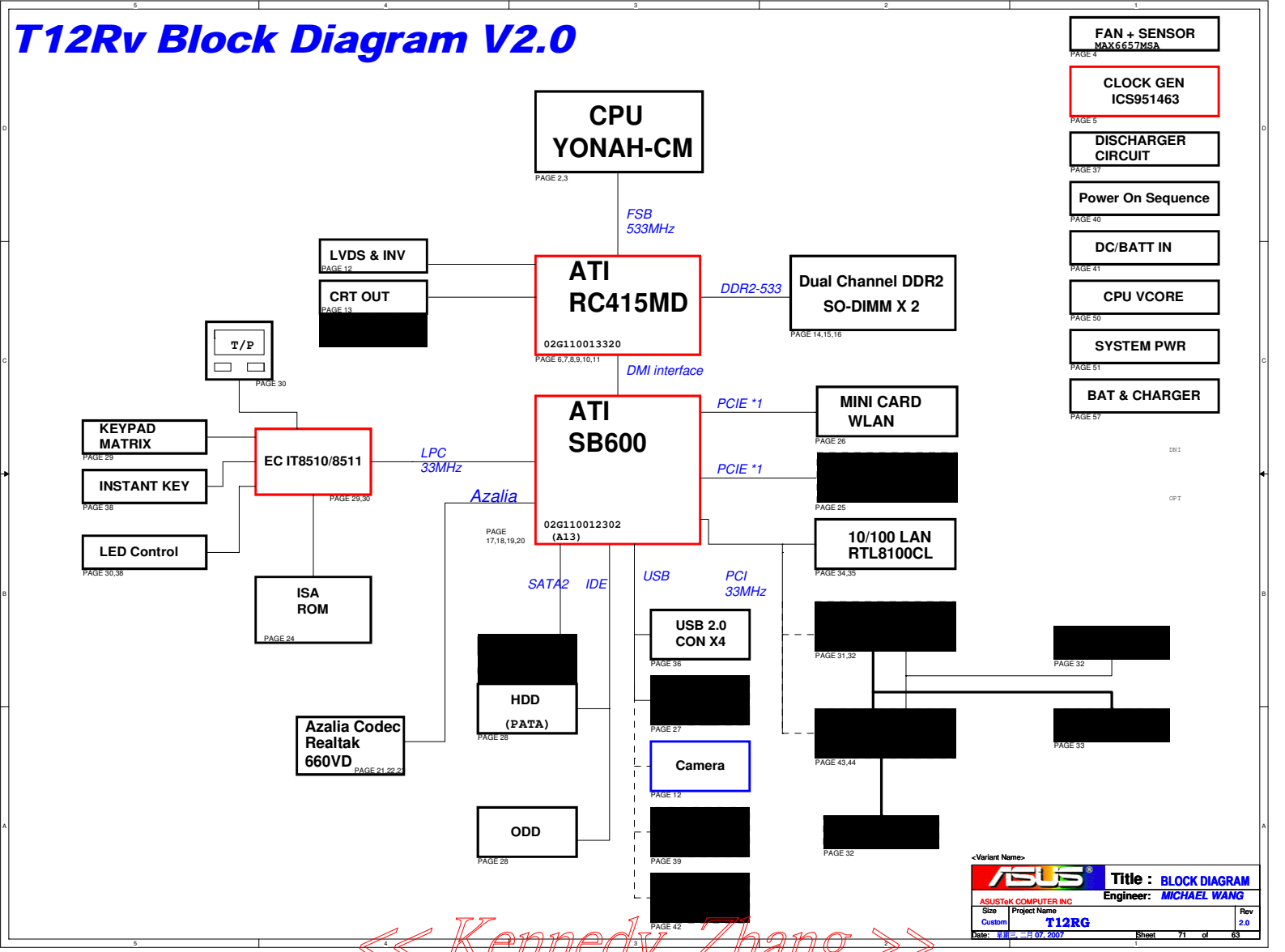
T12Rv Block Diagram V2.0



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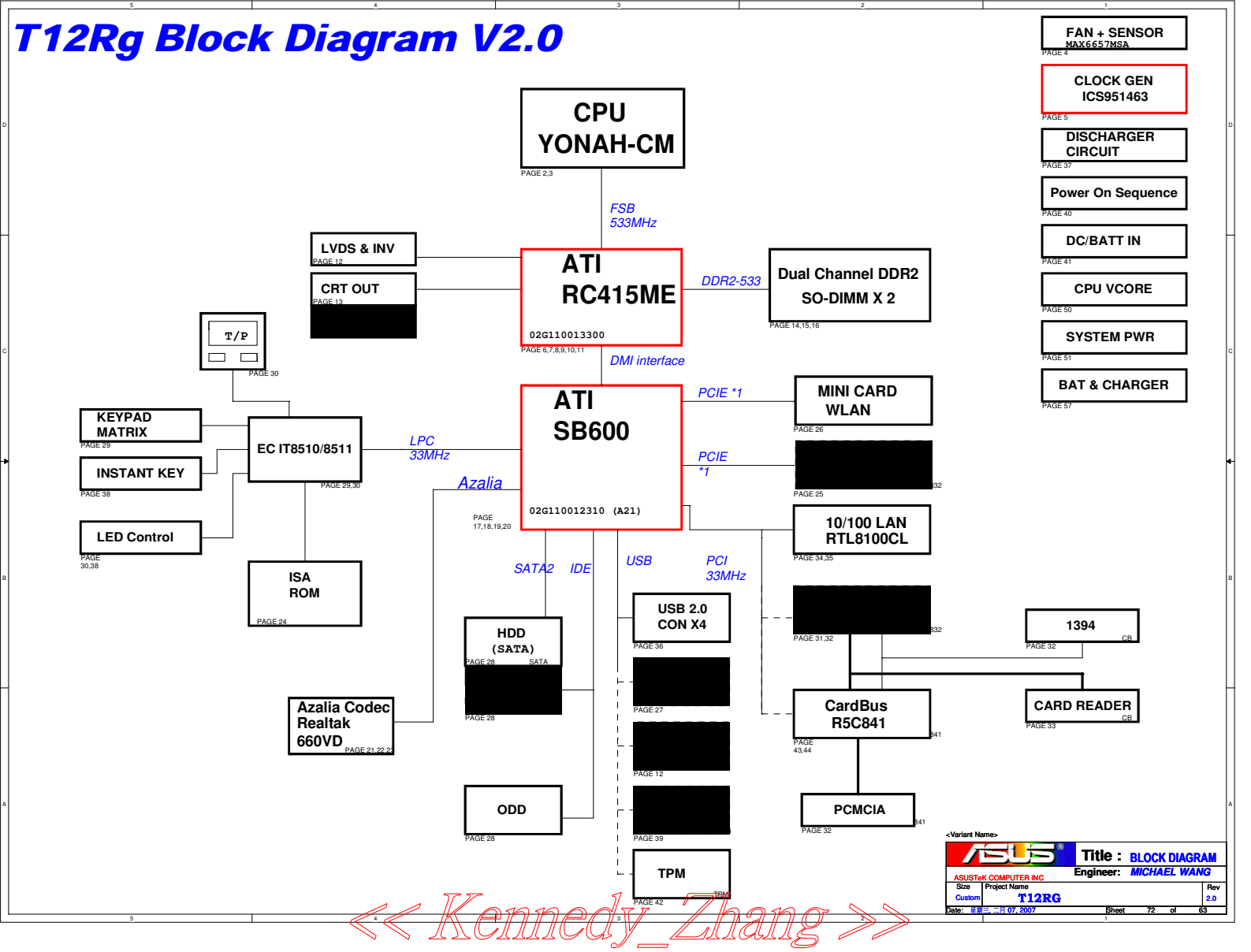
T12Rg Block Diagram V2.0



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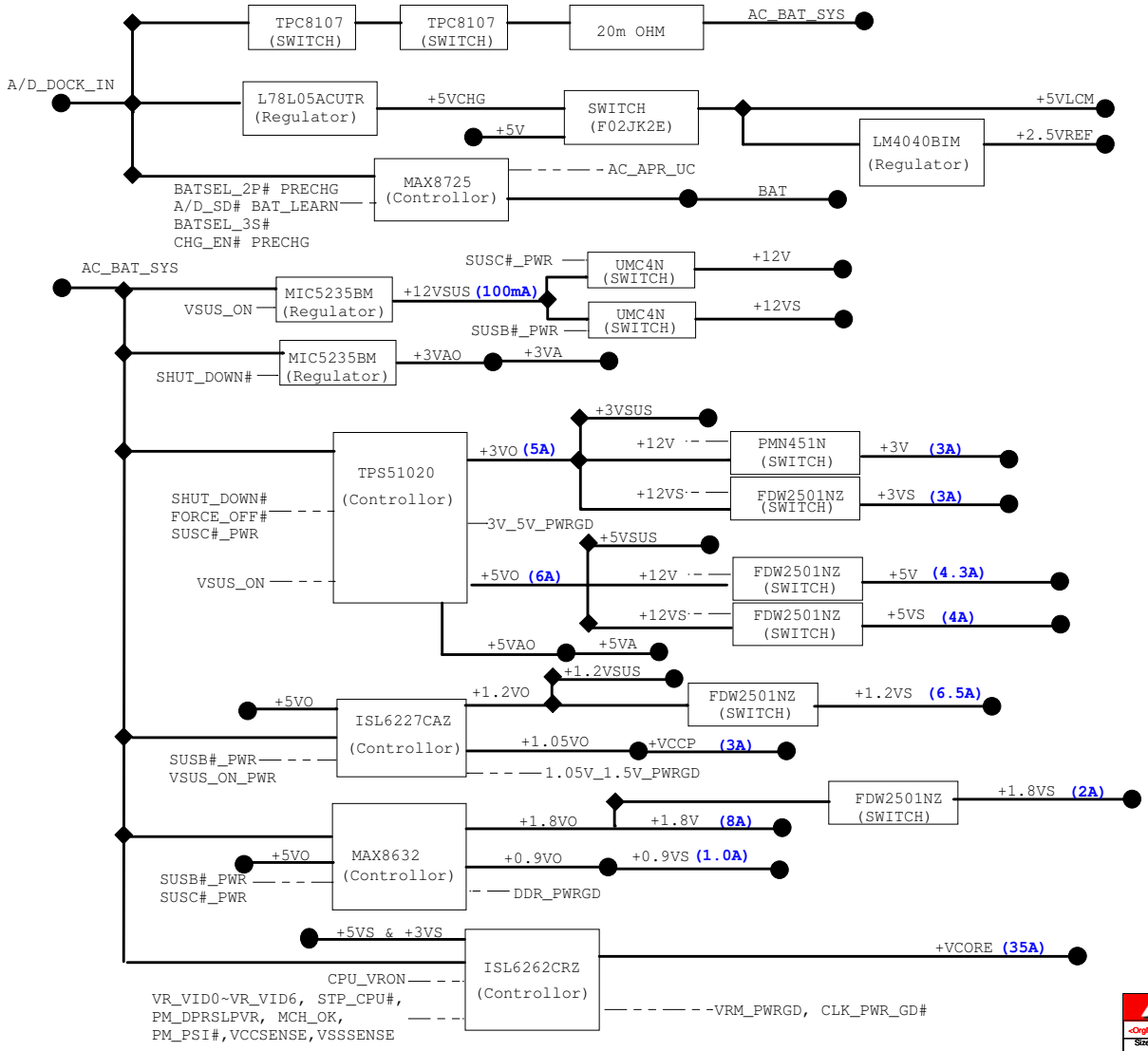

Title : POWER_FLOWCHART

<OrgName>

Engineer: Anny

Size	Project Name	Rev
Custom	T12R	2.0

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