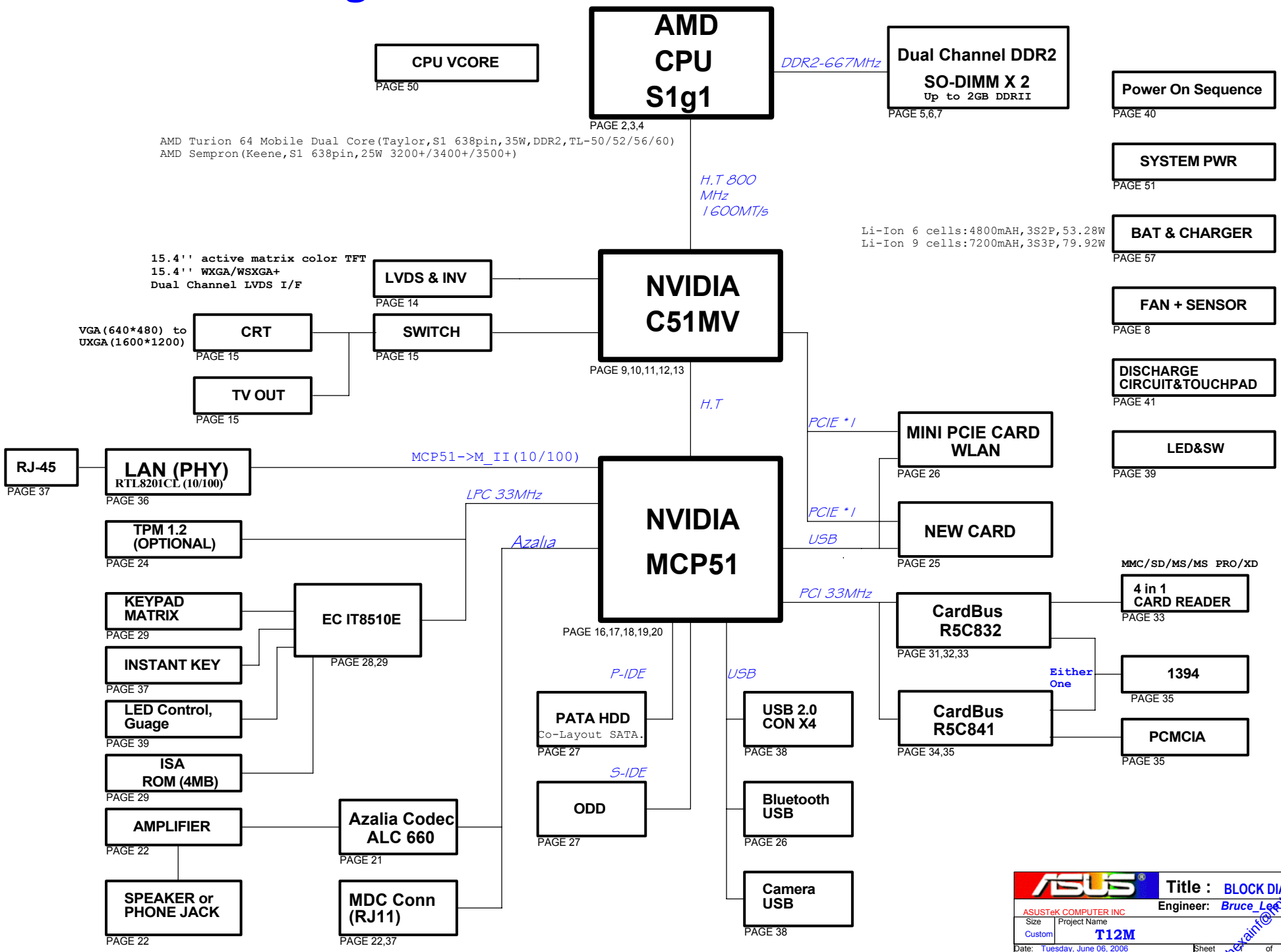
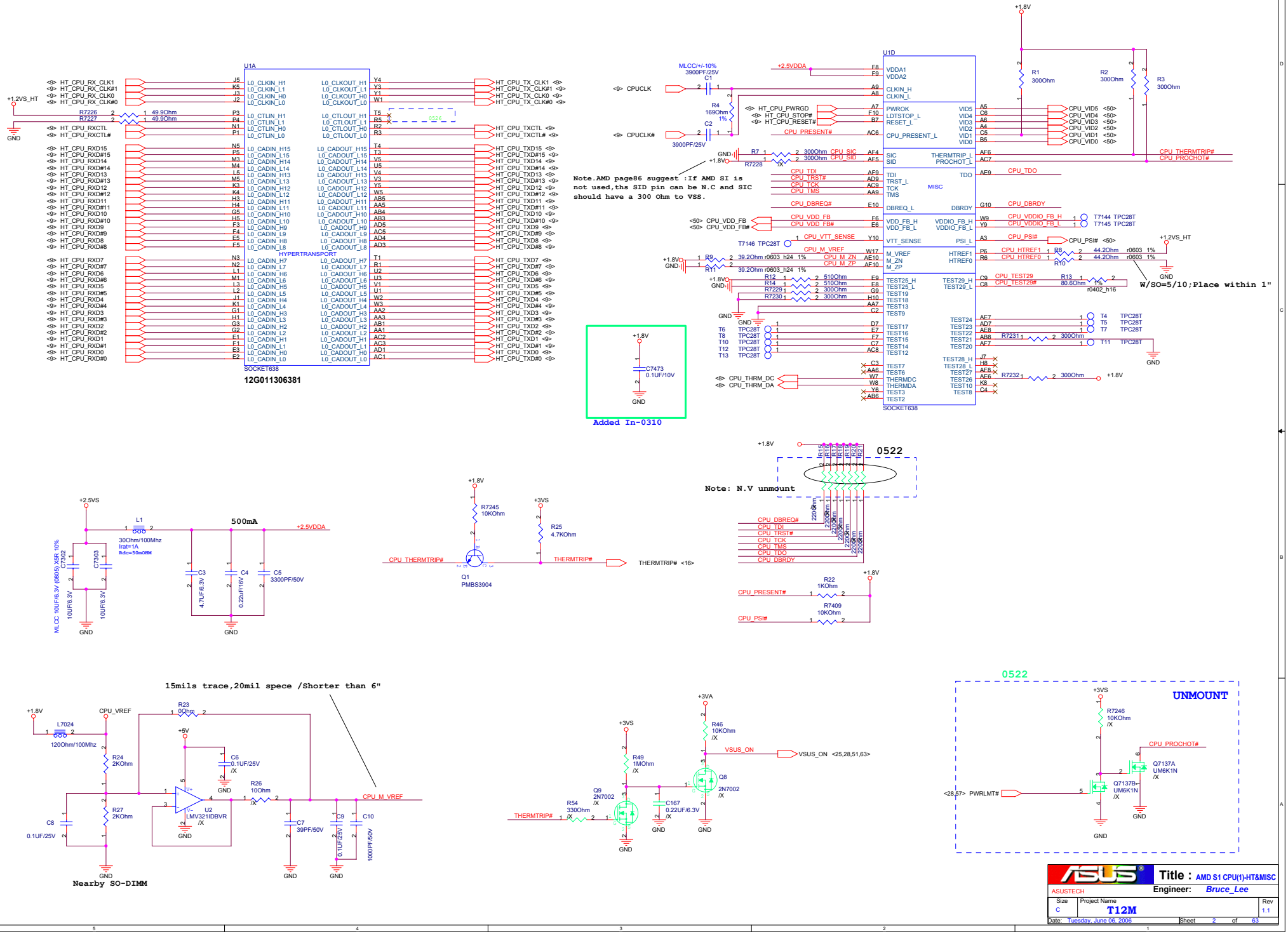
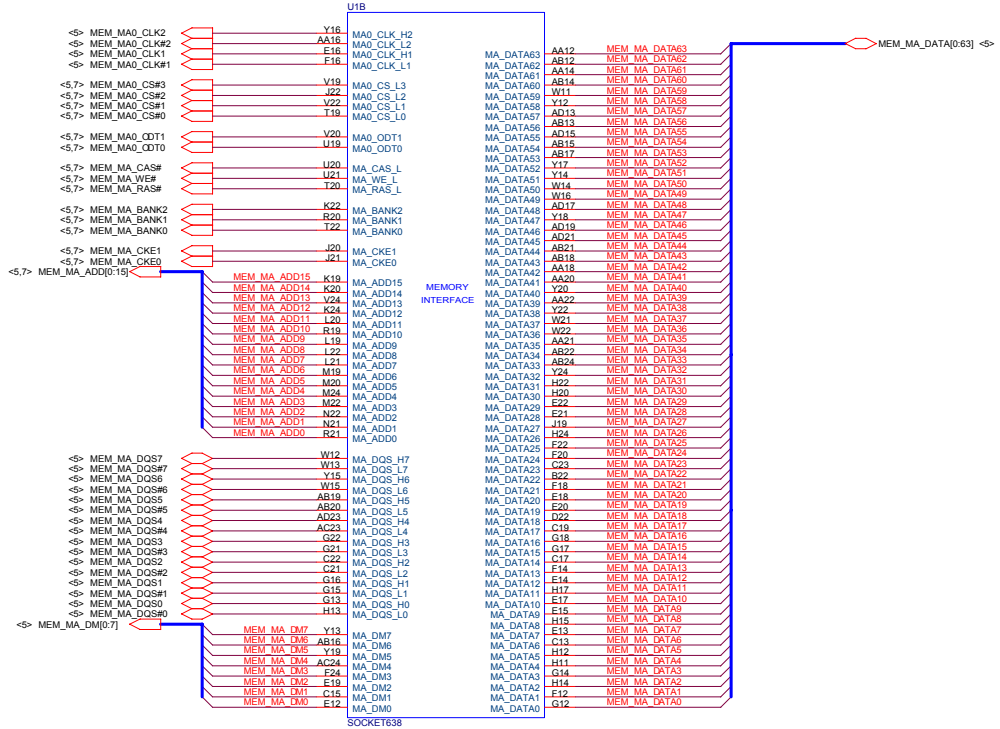
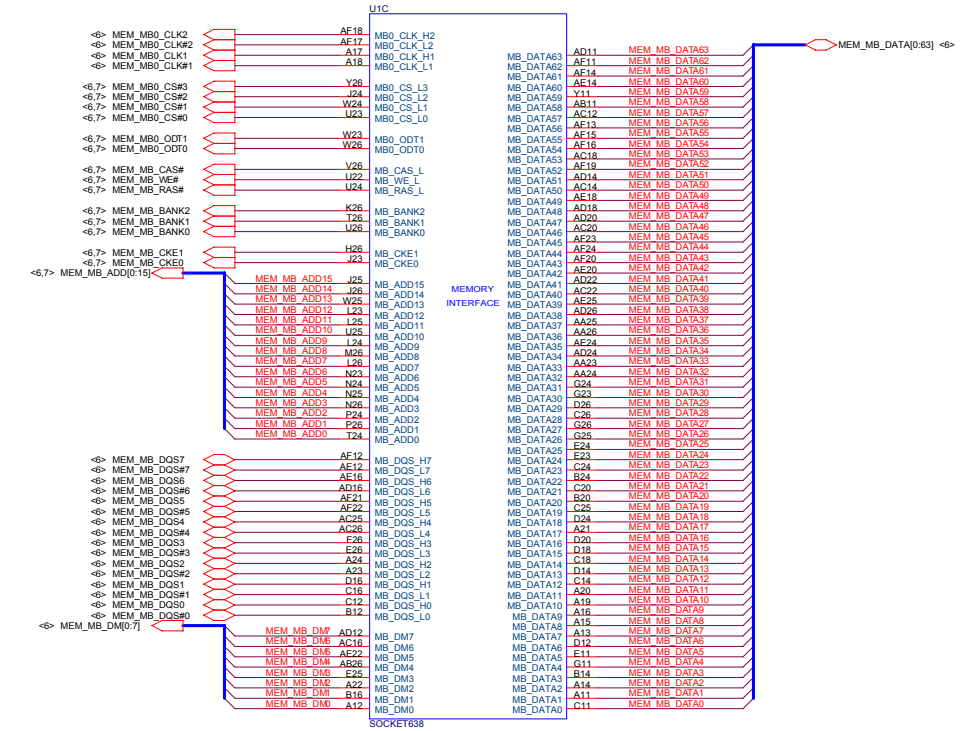
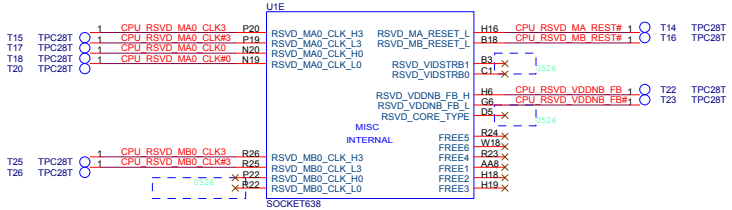
T12M Block Diagram

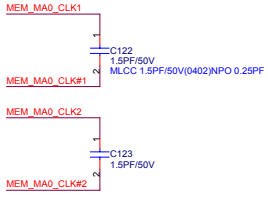


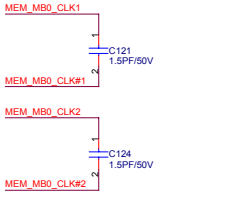

U1A
SOCKET638
12G011306381
HYPERTRANSPORT
U1D
SOCKET638
Note.AMD page86 suggest :If AMD SI is not used,ths SID pin can be N.C and SIC should have a 300 Ohm to VSS.
W/SO=5/10;Place within 1"
Added In-0310
0522
Note: N.V unmount
15mils trace,20mil spece /Shorter than 6"
Nearby SO-DIMM
UNMOUNT
Title : AMD S1 CPU(1)-HT&MISC
ASUSTECH
Engineer: Bruce_Lee
Project Name T12M
Rev 1.1
Date: Tuesday, June 06, 2006
Sheet 2 of 63











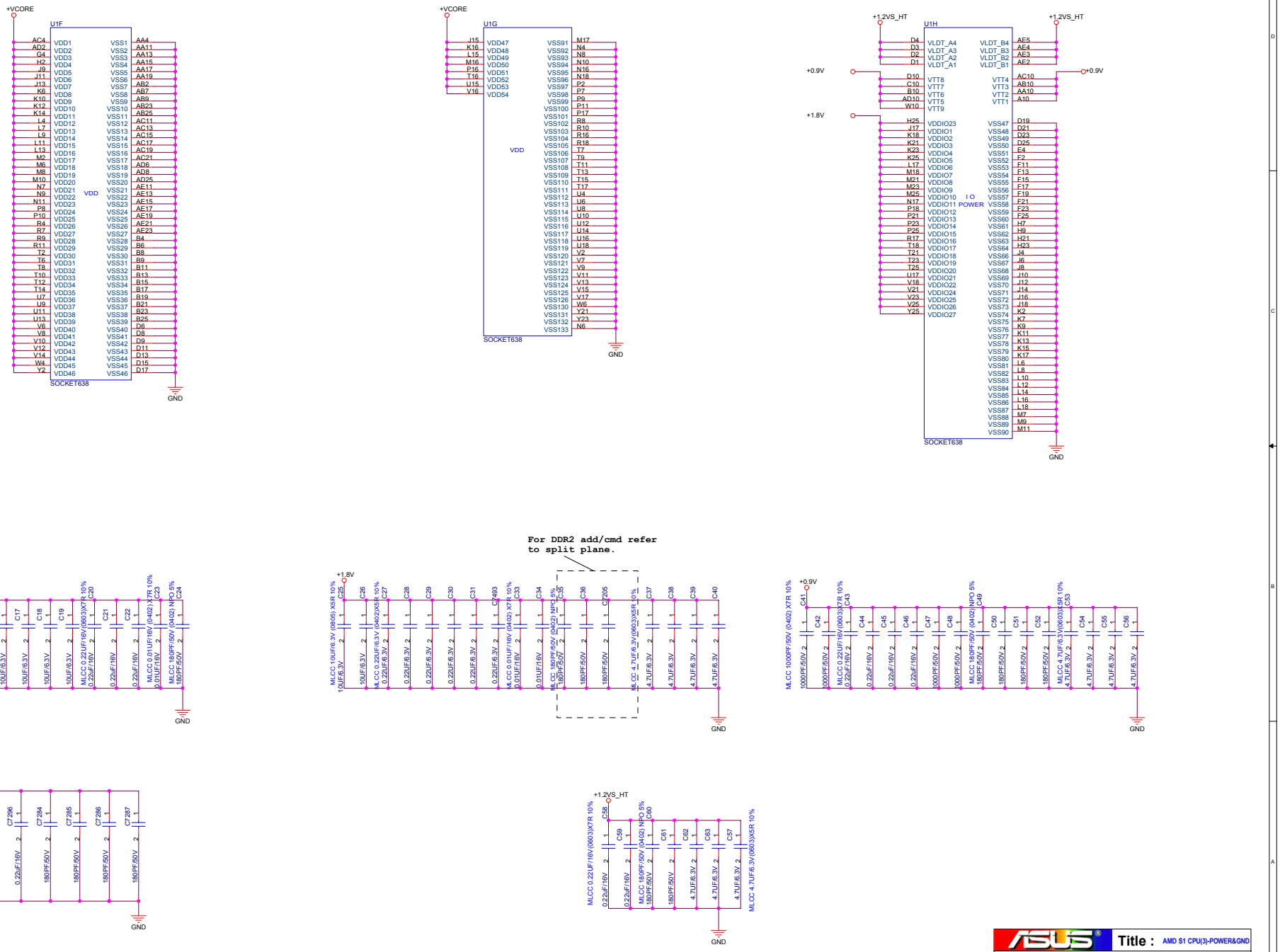
ASUSTECH

Title : AMD Socket AM2(2)-DDRII

Engineer: Peace_Lee

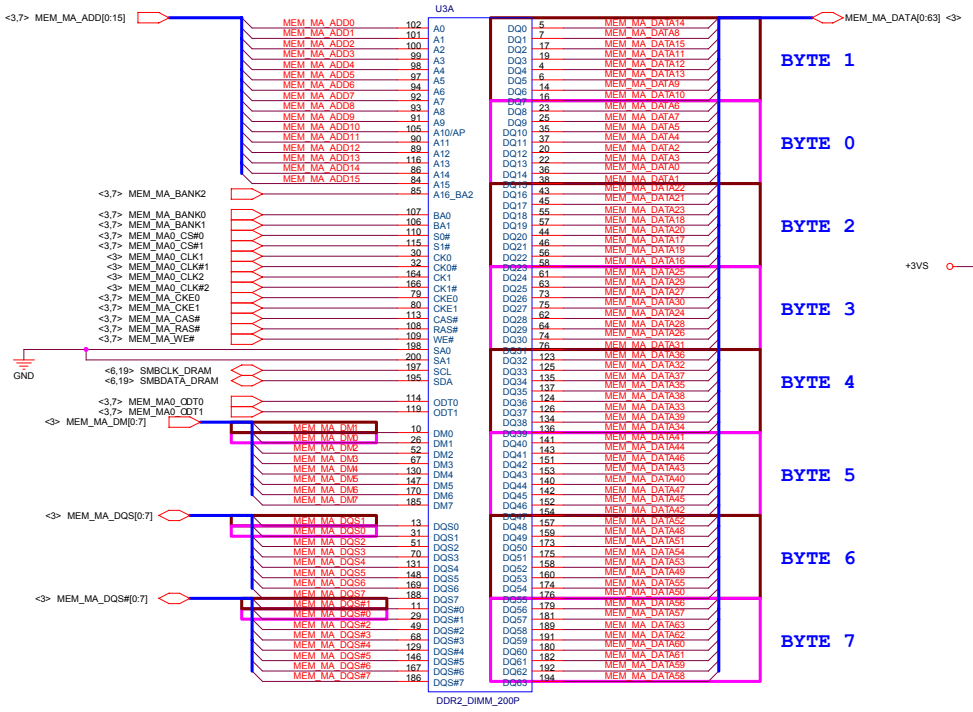
Size	Project Name	Rev
C	T12M	1.1

Date: Tuesday, June 06, 2006 Sheet 3 of 63

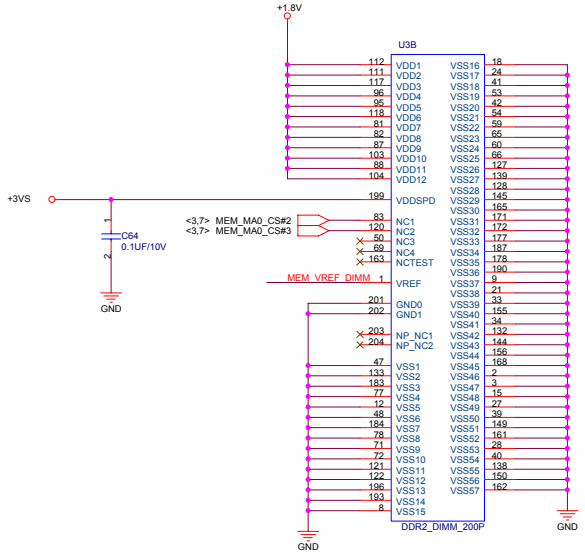


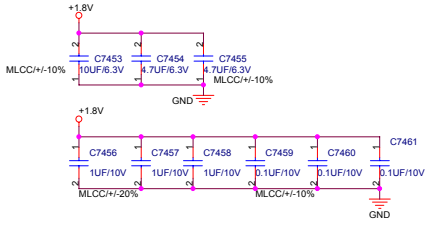
ASUSTECH	Title : AMD S1 CPU(3)-POWER&GND		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 4 of 63		

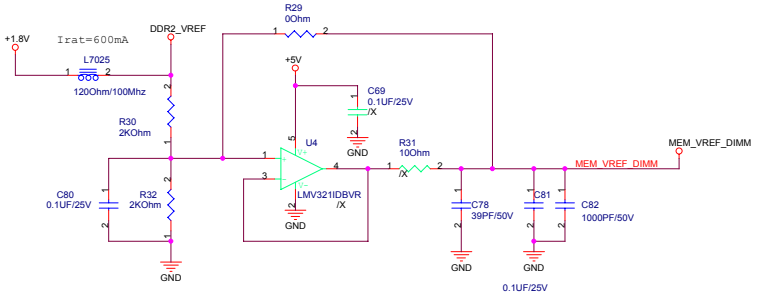
Reserve Type H=4mm



12G02502200F



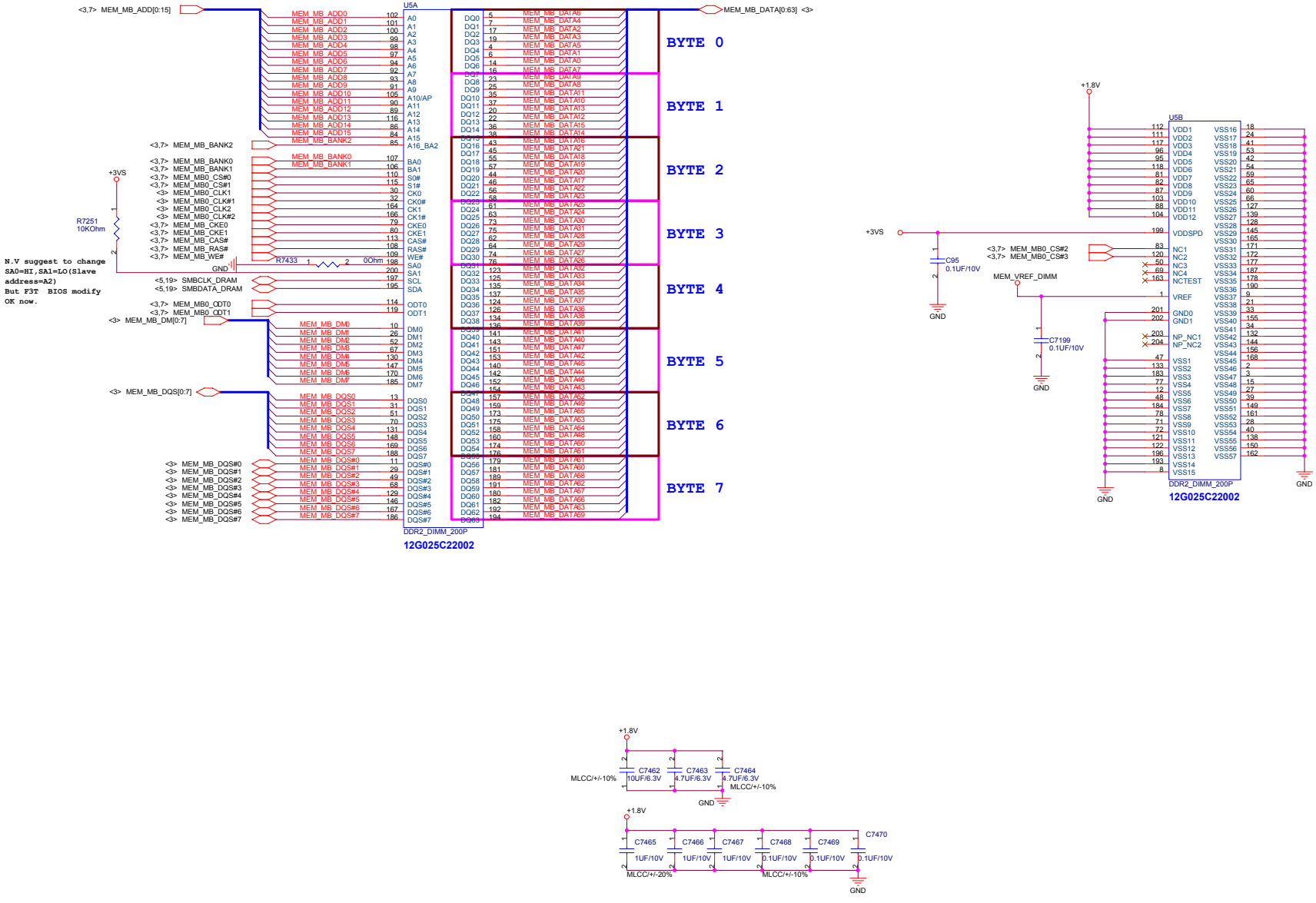




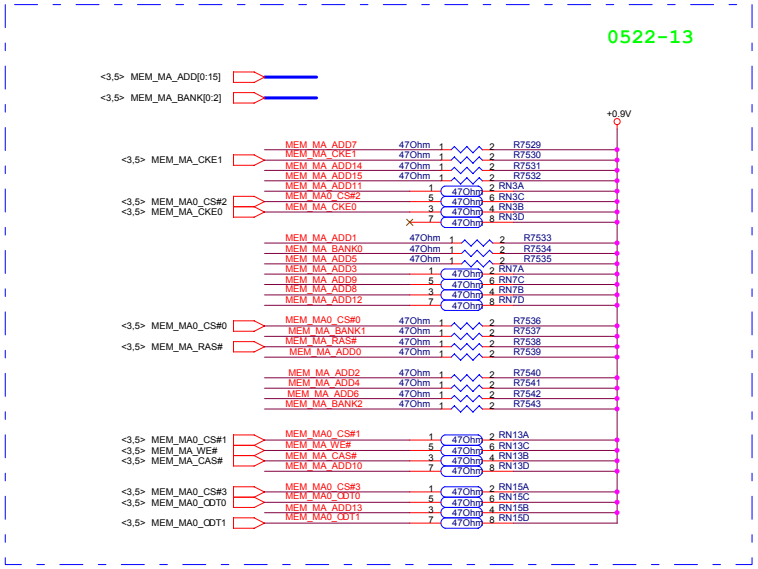
Nearby SO-DIMM

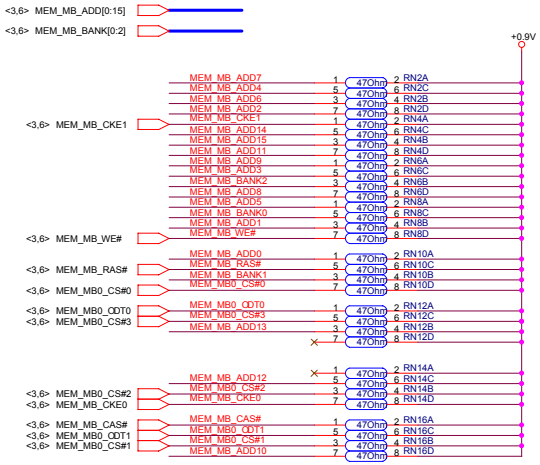
ASUSTECH	Title : DDR2 SO_DIMM-0	
	Engineer: Bruce_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 5 of 63	

Reserve Type H=9.2mm

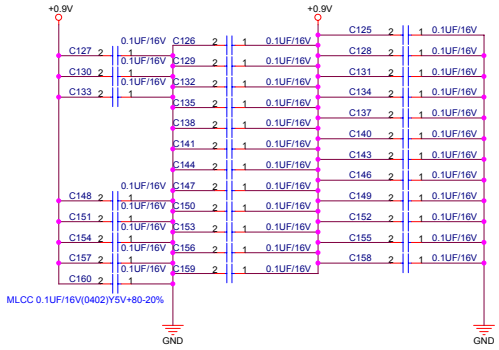


ASUSTECH	Title : DDR2_SO_DIMM-1		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 6 of 63		



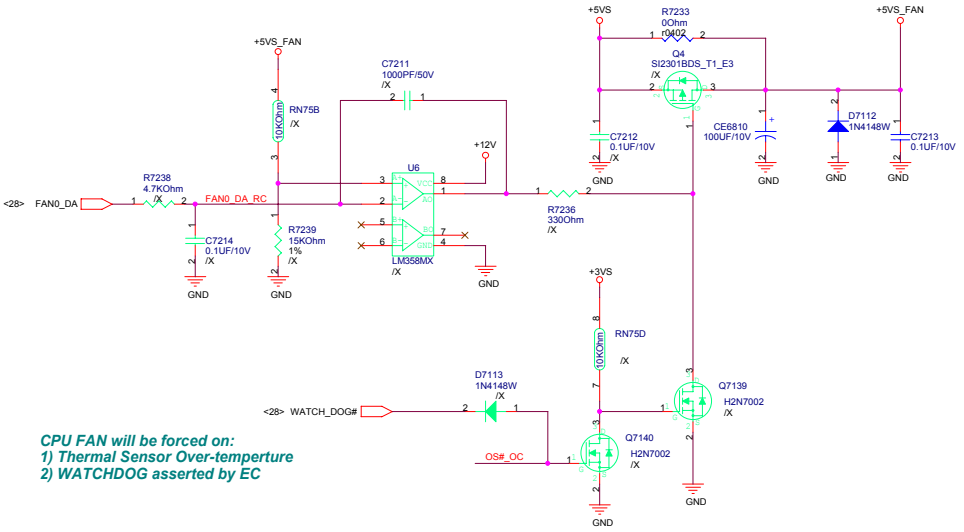


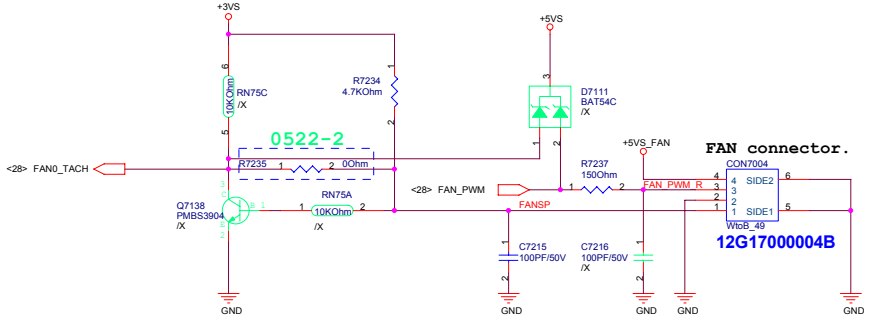
Layout Note: Place one cap close to every 2 pullup resitors terminated to +0.9V



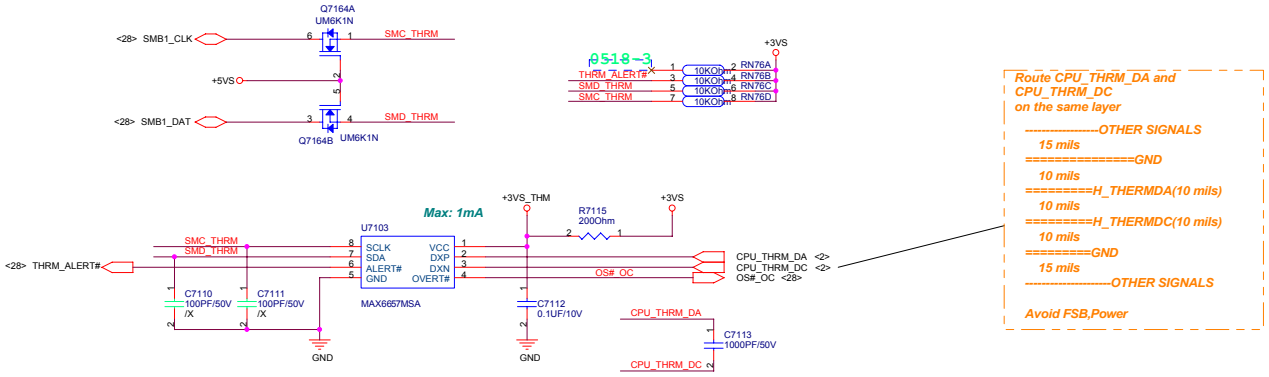
ASUSTECH	Title: DDR2_SODIMM1_TERMINATIONS	
	Engineer: Brian_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 7 of 63	

DC FAN control

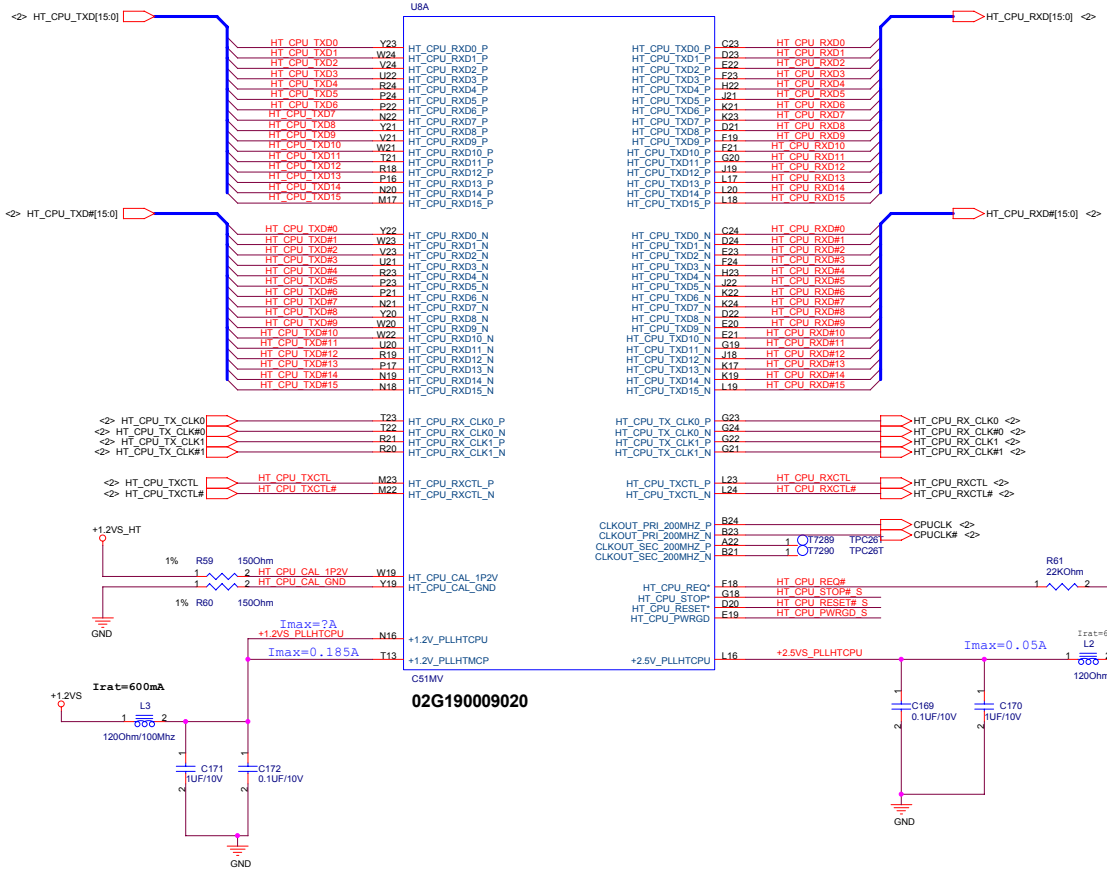




Thermal Sensor

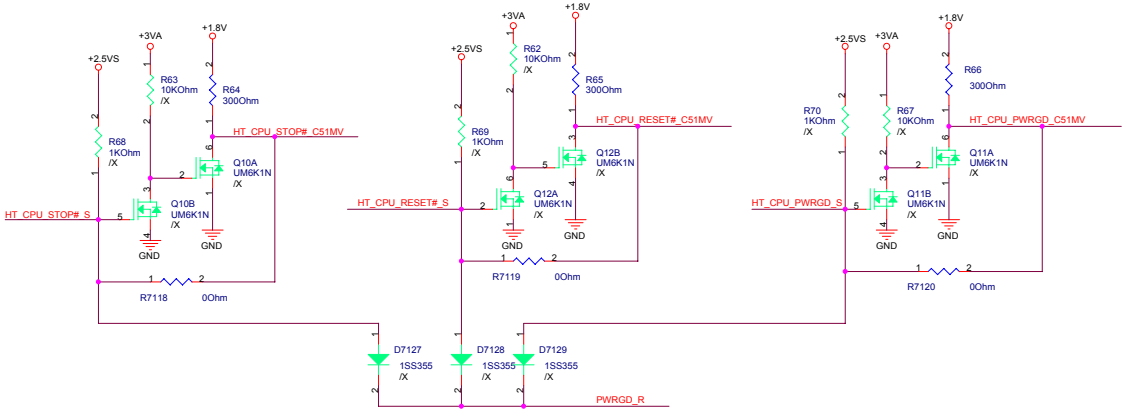


ASUSTECH	Title : THERMAL&FAN CONTROL	
	Engineer: Bruce_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 8 of 63	

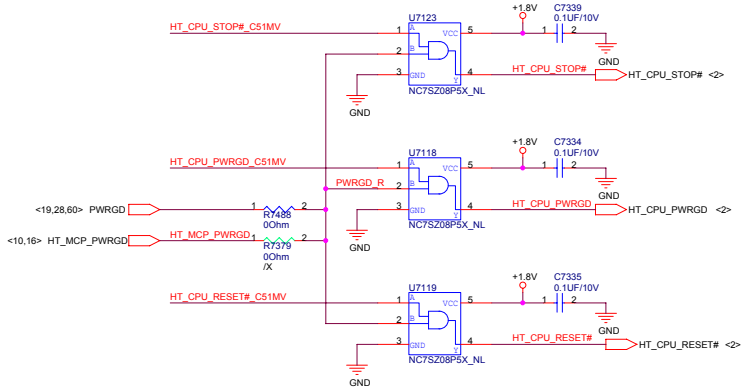


CPU de-glitch circuit

Voltage-level shifter/open-drain buffer
See Notes1.(N.V design guide page19.)

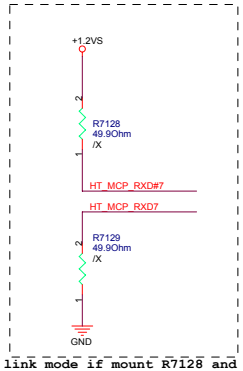


nVidia C51 Chipset side-band signal glitch issue solution.



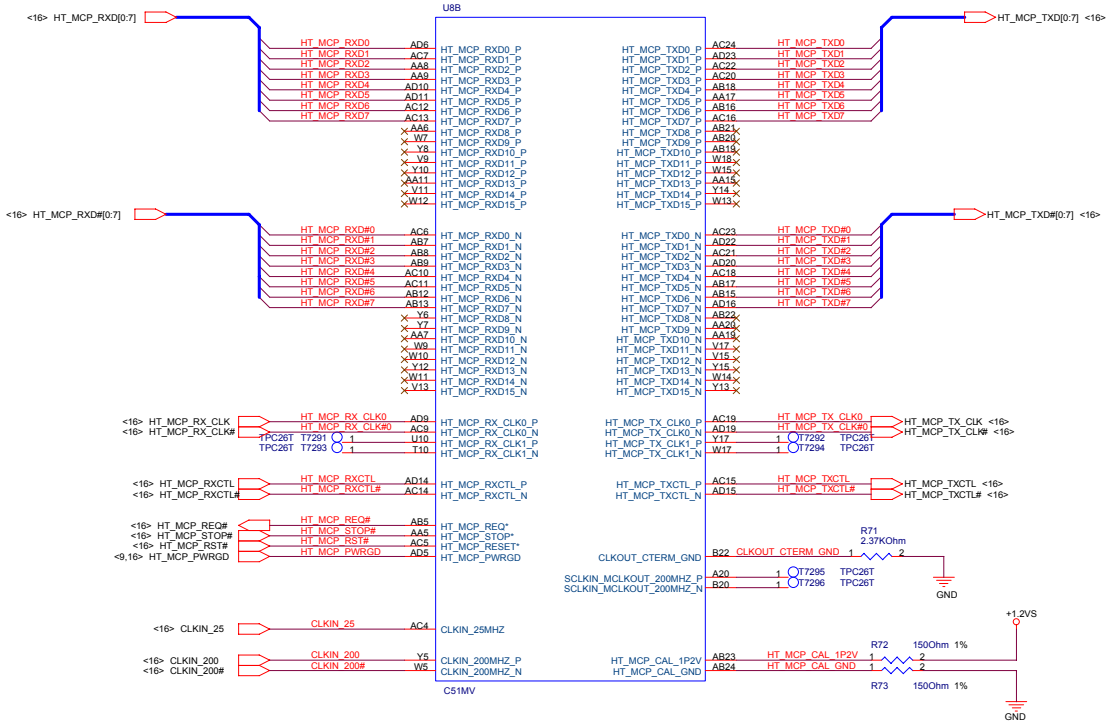
ASUSTECH	Title : C51MV HT TO CPU		
	Engineer: Bruce_Lee		
Size: Custom	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 9 of 63		

R close to IC within 1500 mils.
Place these resistors without stubs.

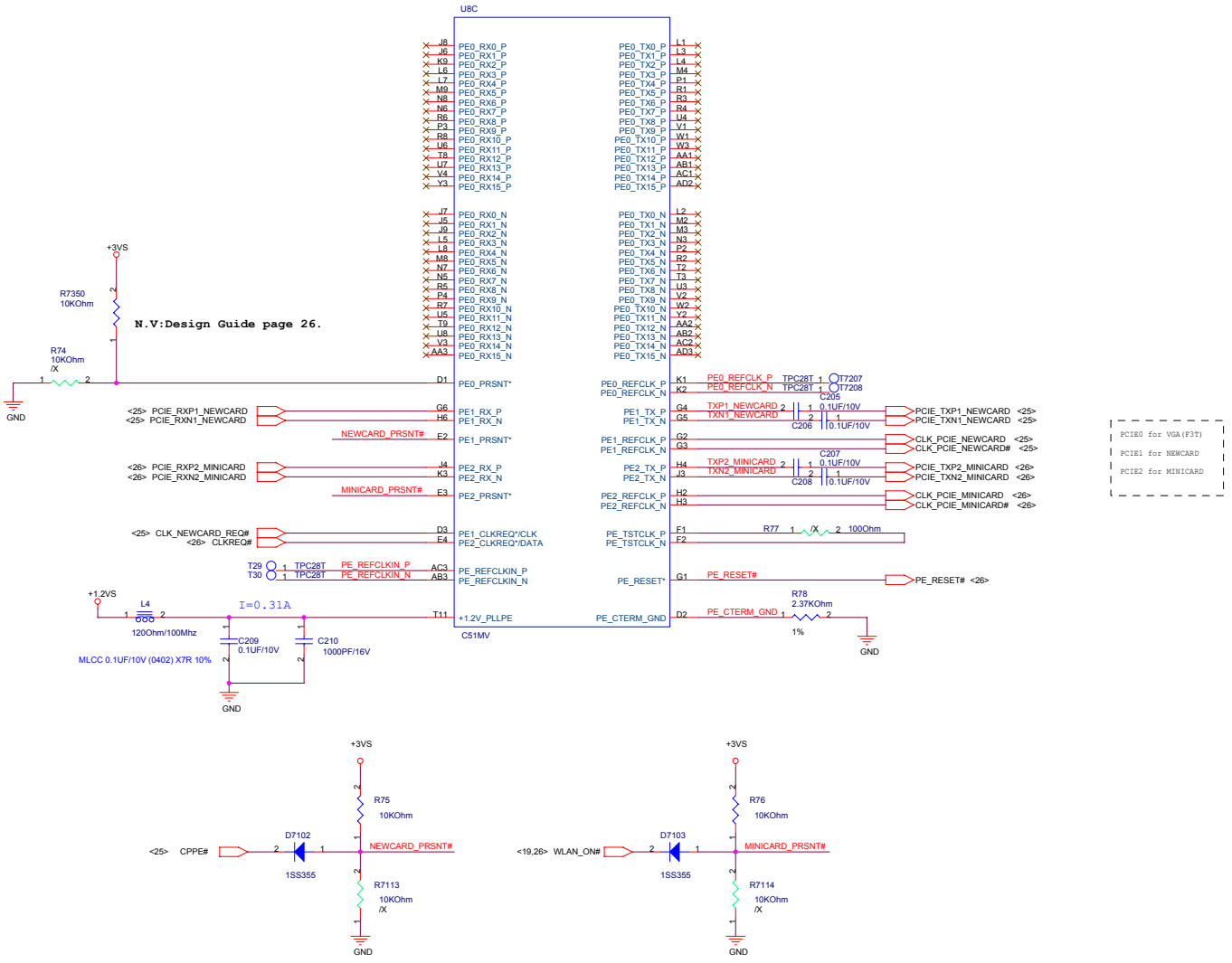


4*4 H.T link mode if mount R7128 and R7129.

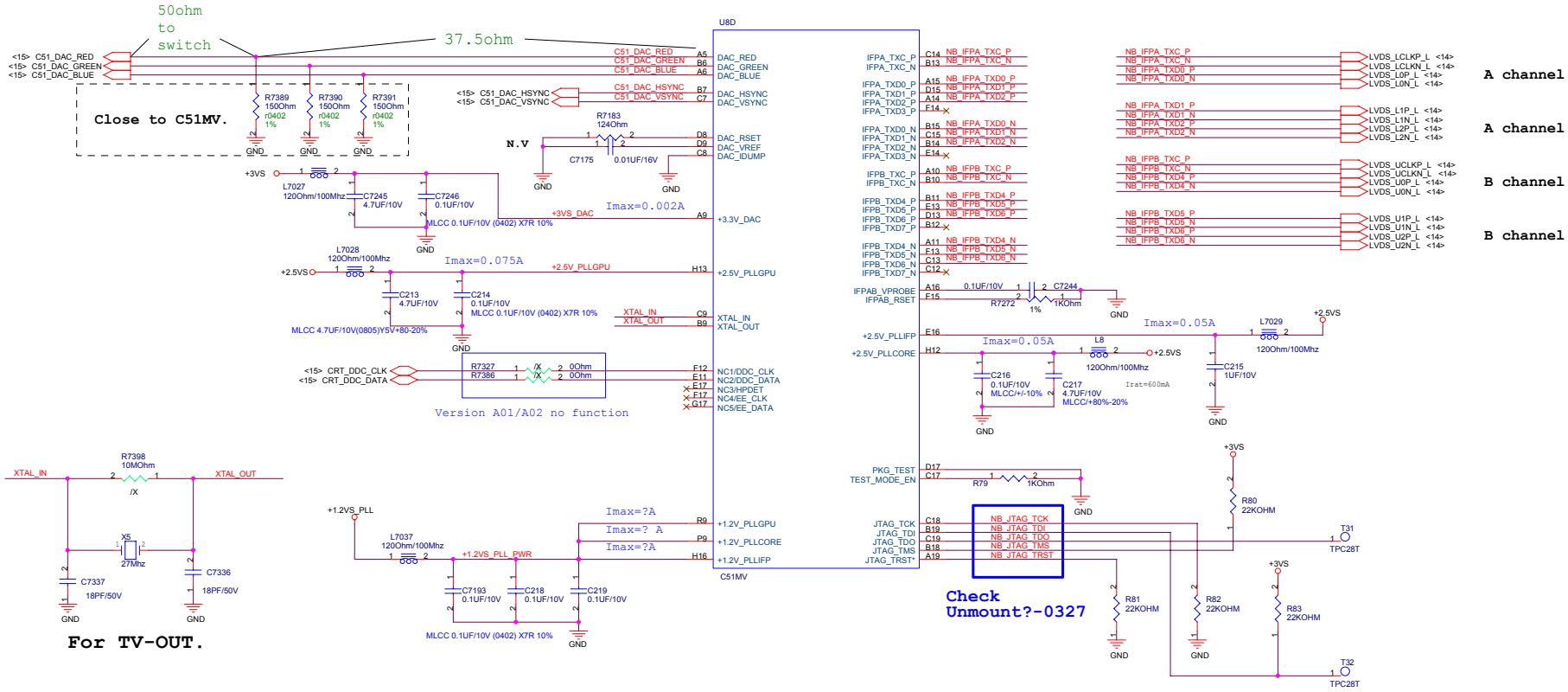
Nvidia suggests to change 8*8. Resisters setting can reference design guide chapter12 (Page 176).



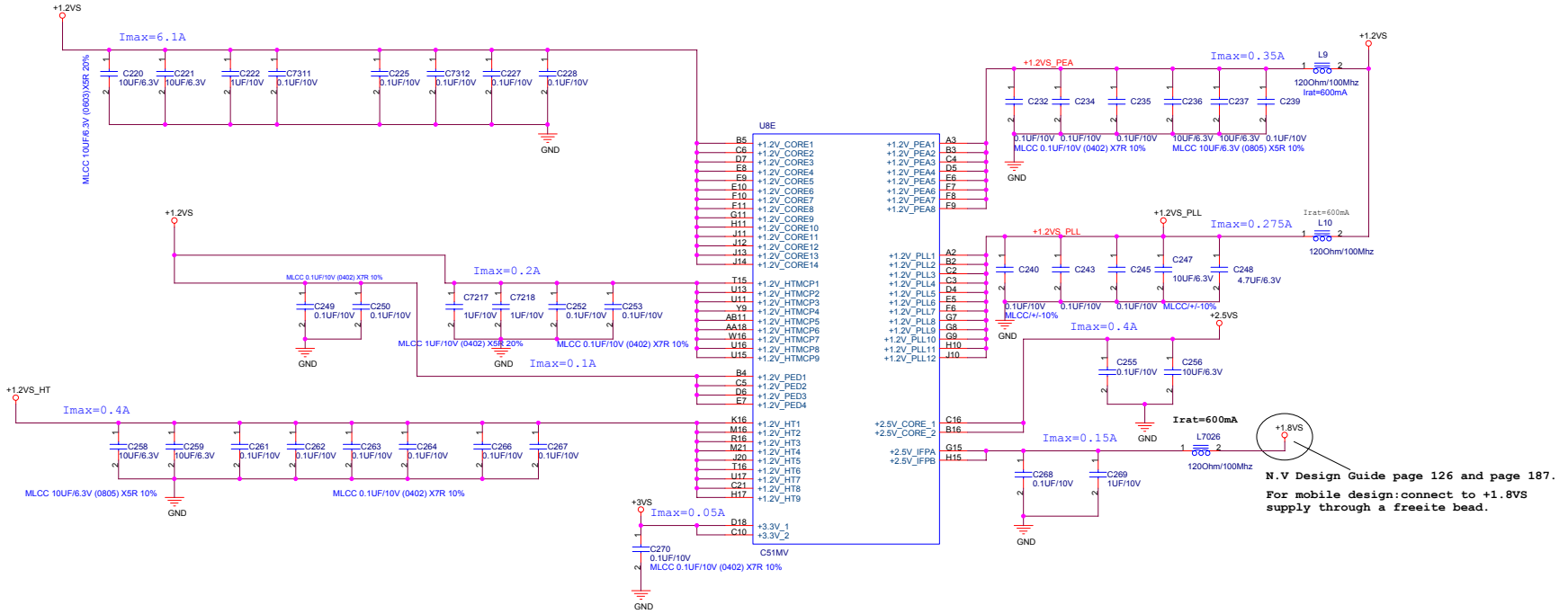
ASUSTECH	Title : C51MV HT TO MCP	
	Engineer: Bruce_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 10 of 63	

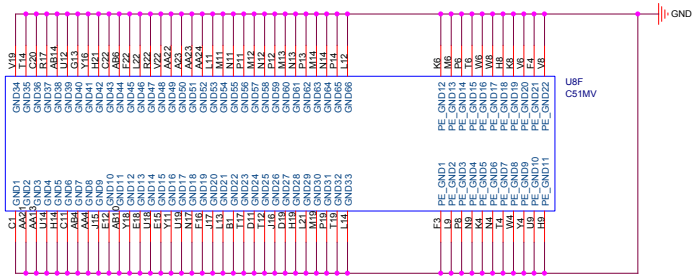


ASUSTECH	Title : C51MV PCIEx16	
	Engineer: Peace_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 11 of 63	



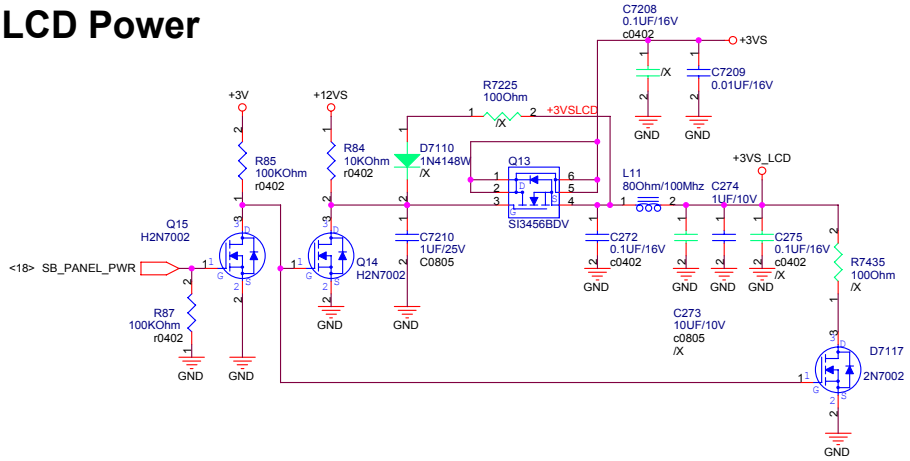
ASUSTECH	Title : C51MV VGA&LVDS		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 12 of 63		



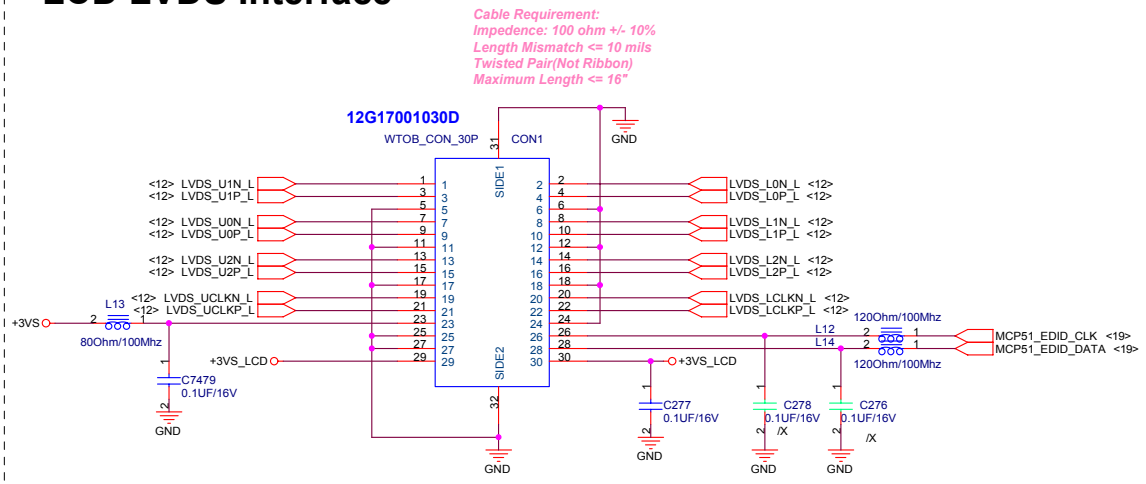


ASUSTECH	Title : C51MV_POWER&GND	
	Engineer: Peace_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 13 of 63	

LCD Power



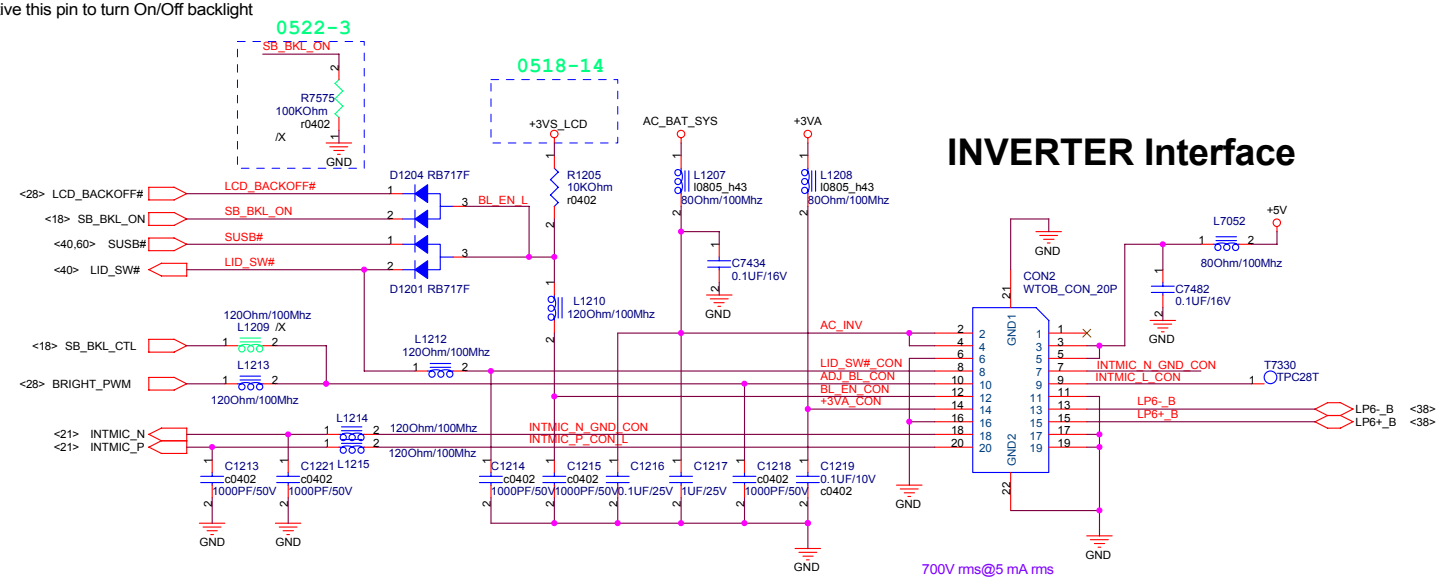
LCD LVDS Interface



Inverter & Backlight Controll

LCD Backlight Control *15.4" WXGA ,1280*800*

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

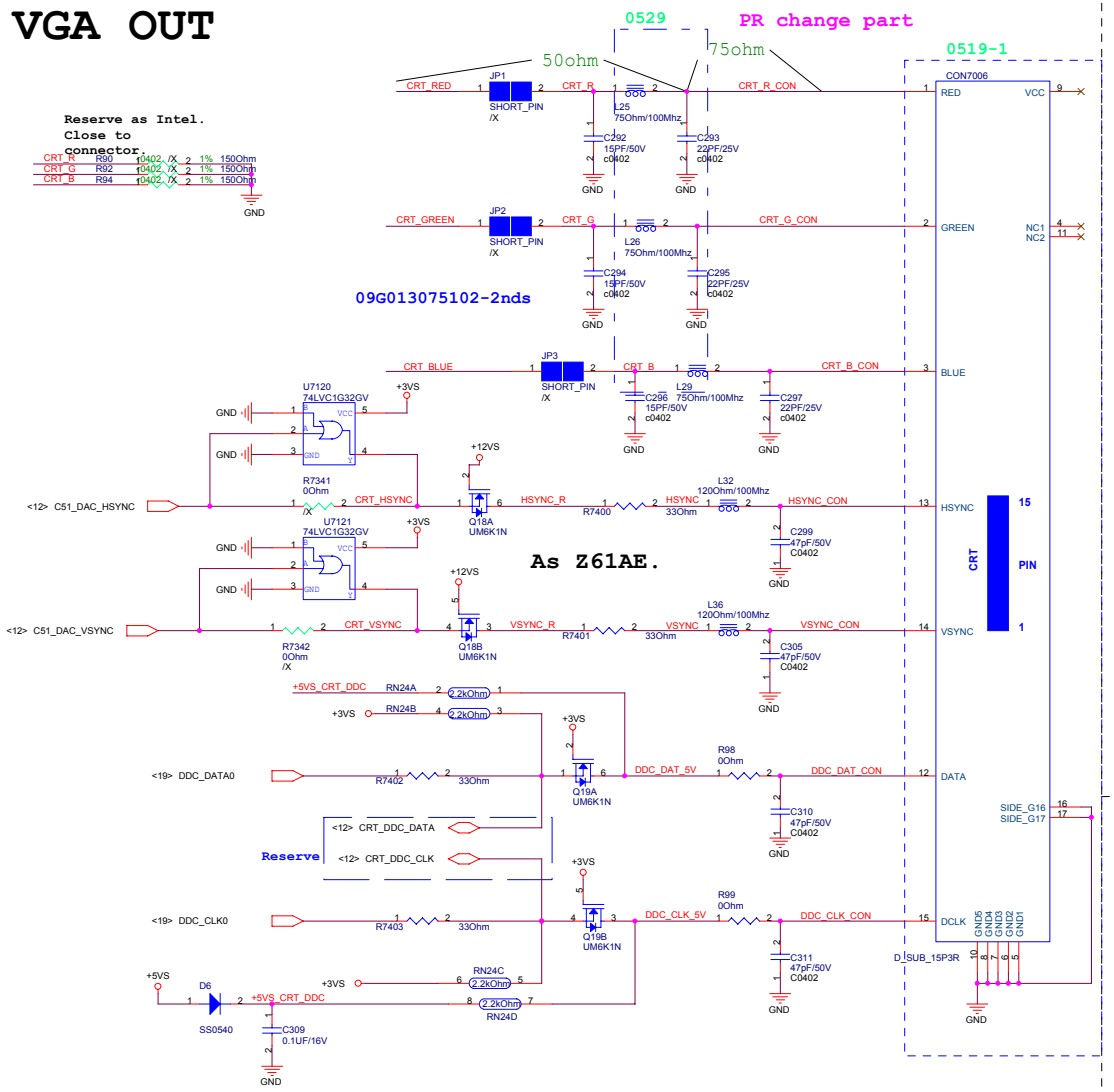


INVERTER Interface

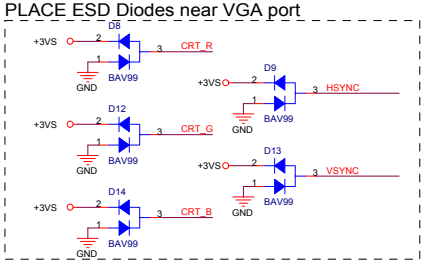
700V rms@5 mA rms
(Min. 3 mA rms)6 mA
rms(Max. 6.5 mA
rms)

ASUSTECH	Title : LVDS & INVERTER CONNECTOR	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 14 of 63	

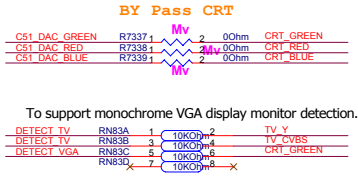
VGA OUT



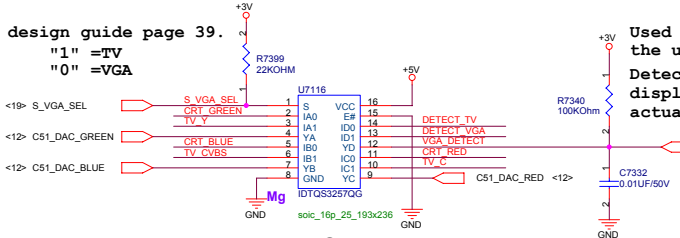
PLACE ESD Diodes near VGA port



TV-OUT and VGA OUT Switch.

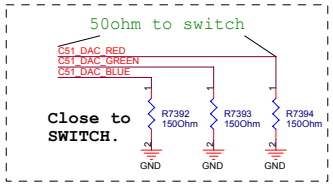


Nvidia design guide page 39.
"1" =TV
"0" =VGA



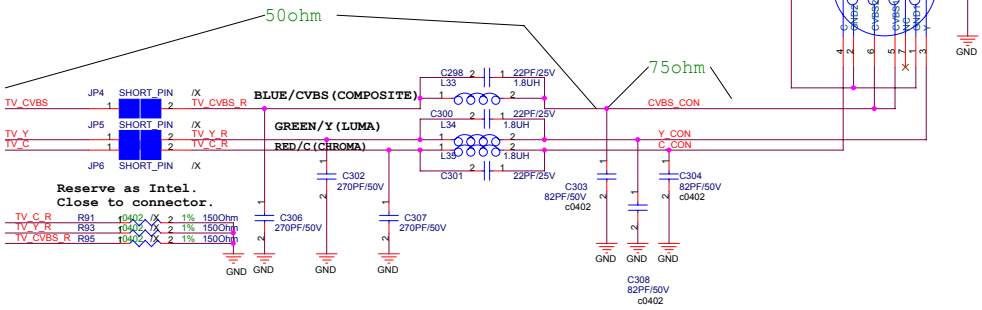
Used to detect load on the undriven output.
Detect whether a display(VGA or TV) is actually present.

Reference A8N-VM project.

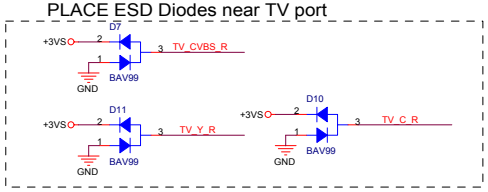


TV OUT

12G141011076

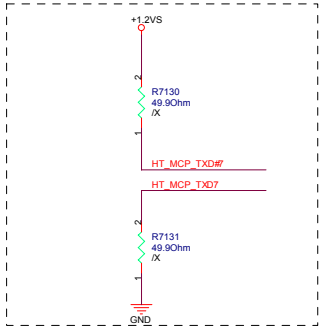


PLACE ESD Diodes near TV port



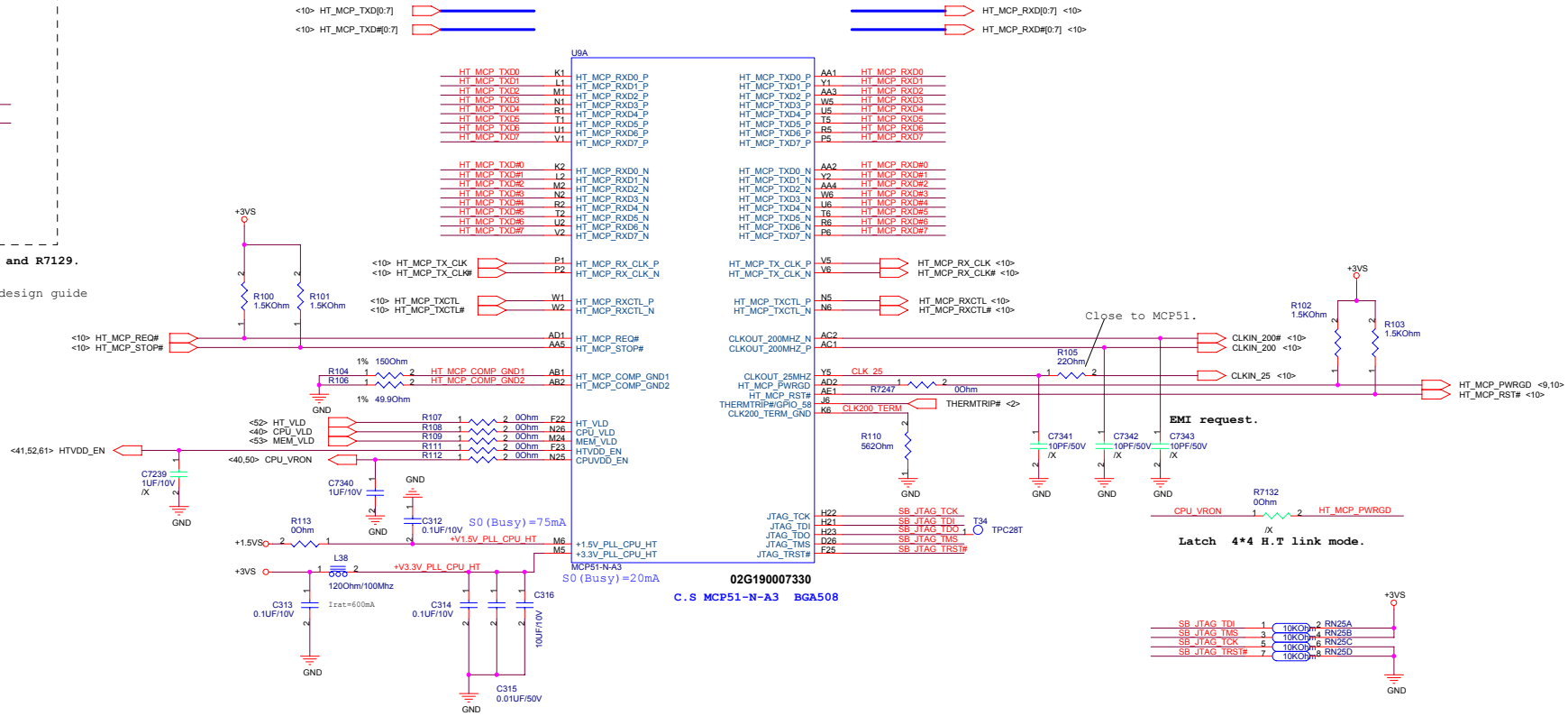
ASUSTeK	Title : TV&CRT CONNECTOR		
	Engineer: Bruce_Lee		
Size: Custom	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 15 of 63		

R close to IC within 1500 mils.
Place these resistors without stubs.

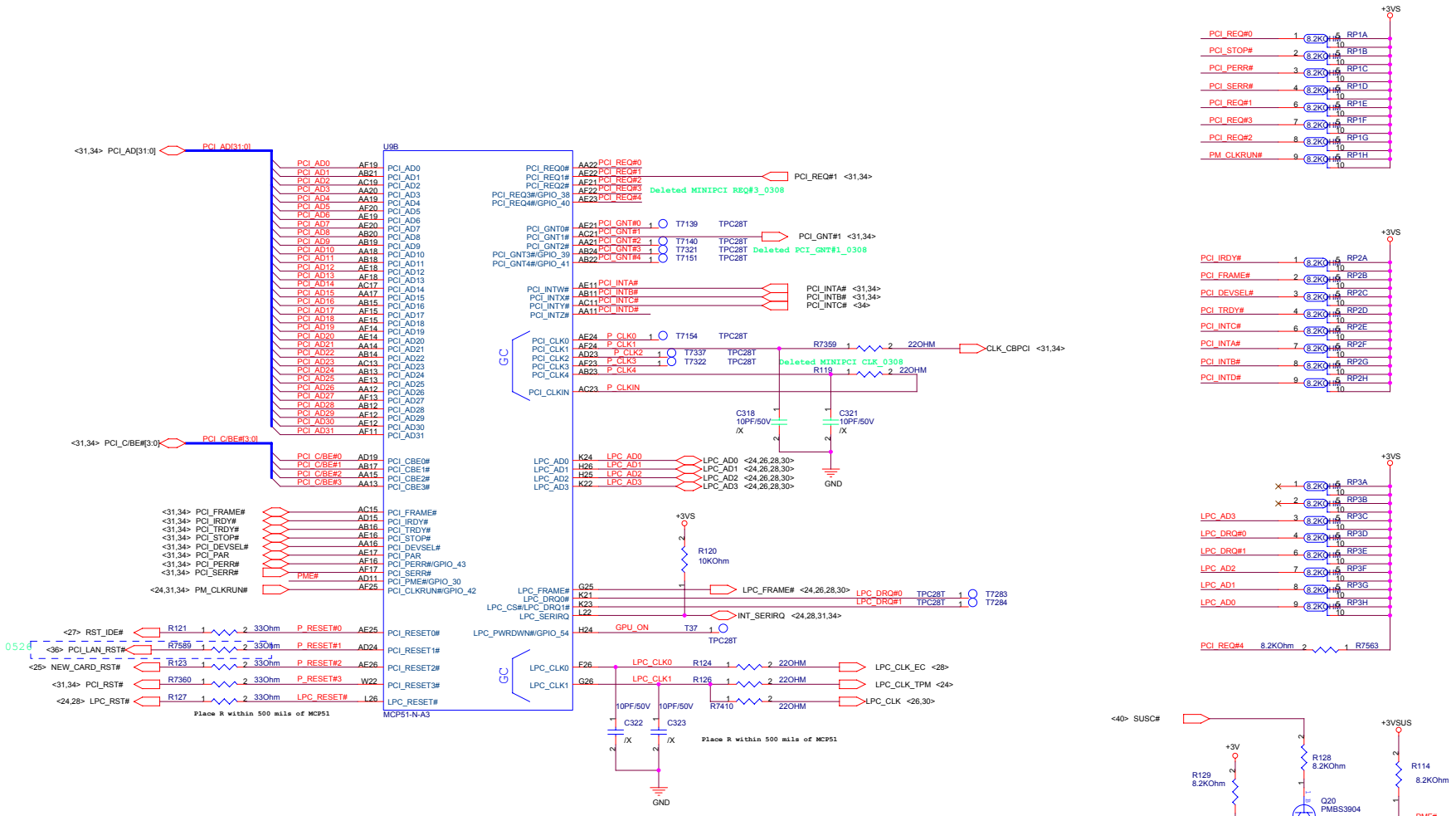


4*4 H.T link mode if mount R7128 and R7129.

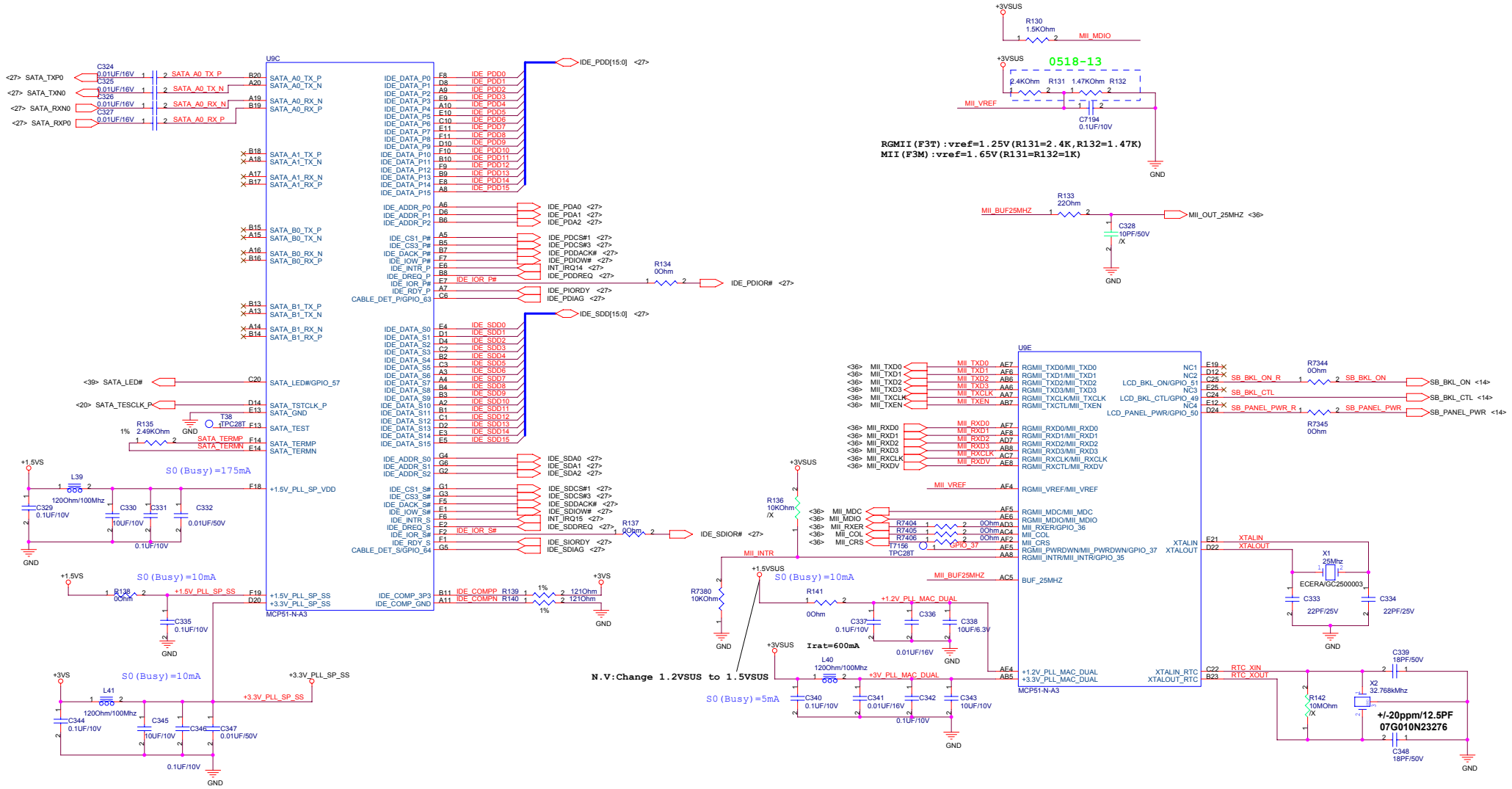
Nvidia suggests to change 8*8.
Resisters setting can reference design guide chapter12 (Page 176).



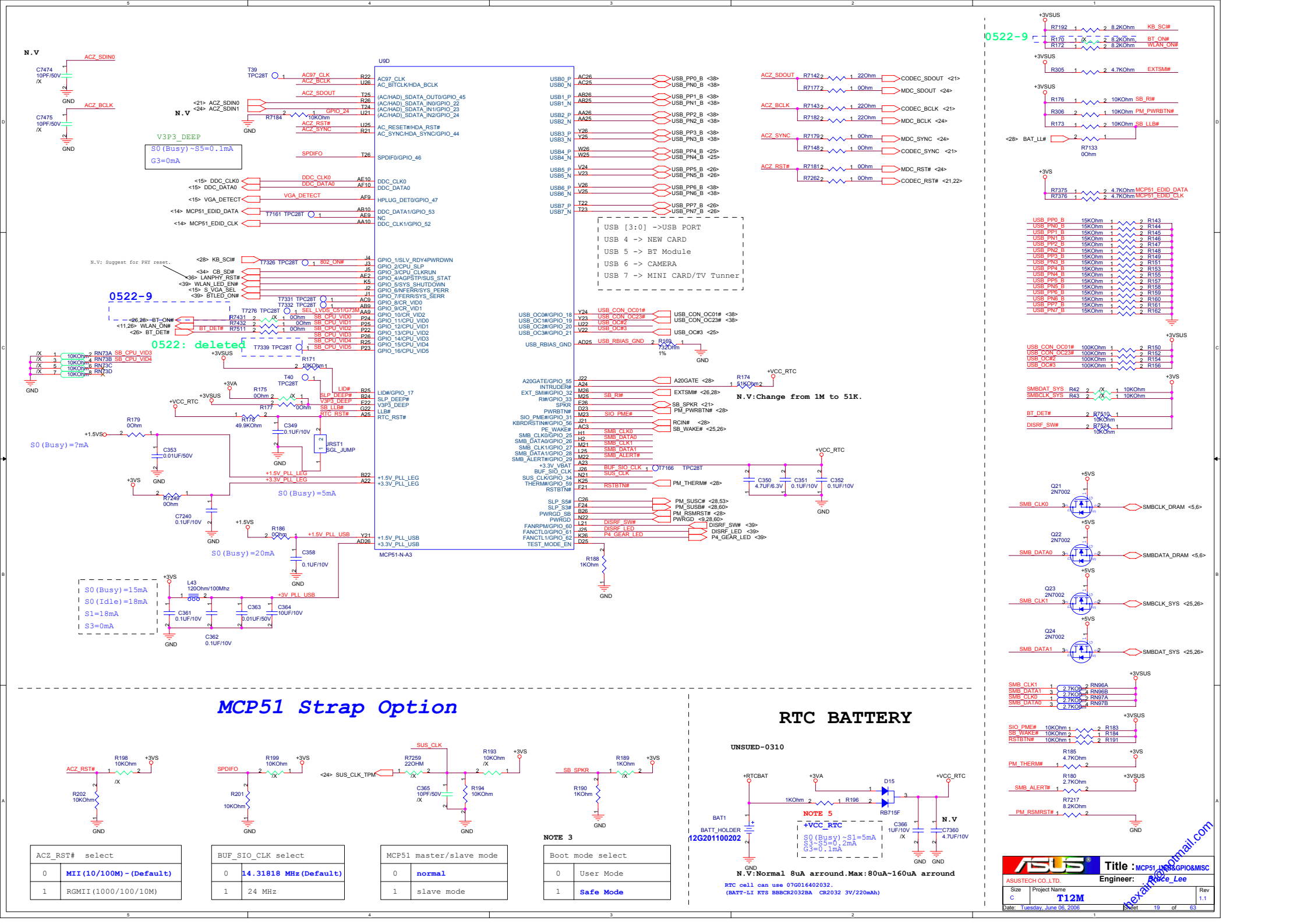
ASUSTEK CO.,LTD.	Title : MCP51_HT TO C51MV		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 16 of 63		

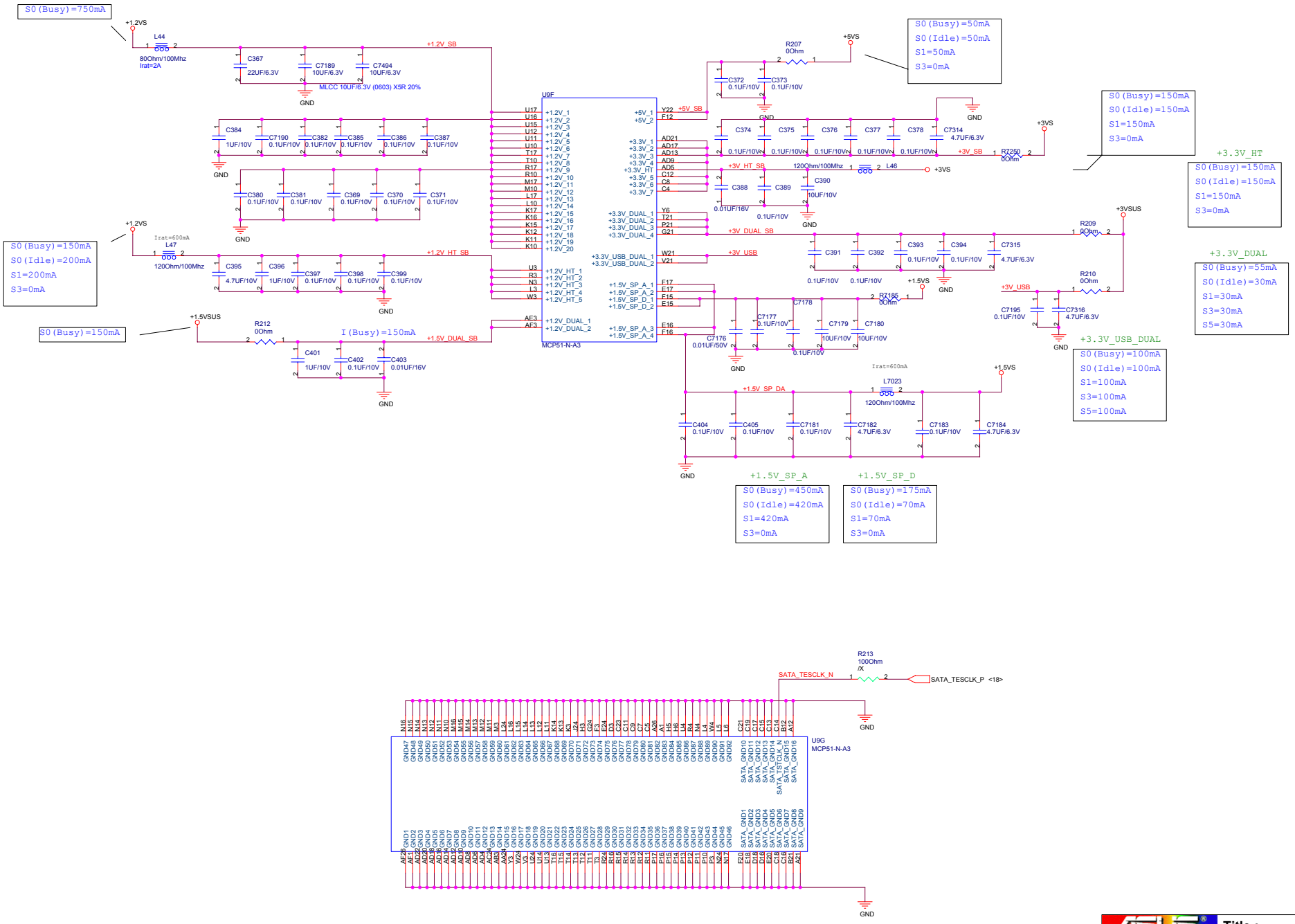


ASUSTECH CO.,LTD.
Title : MCP51 PCI I/F
Engineer: Peace_Lee
Size C
Project Name T12M
Rev 1.1
Date: Tuesday, June 06, 2006
Sheet 17 of 63
hexaimee@hotmail.com



ASUSTECH CO.,LTD.	Title : MCP51_SATA&IDE&LAN		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 18 of 63		

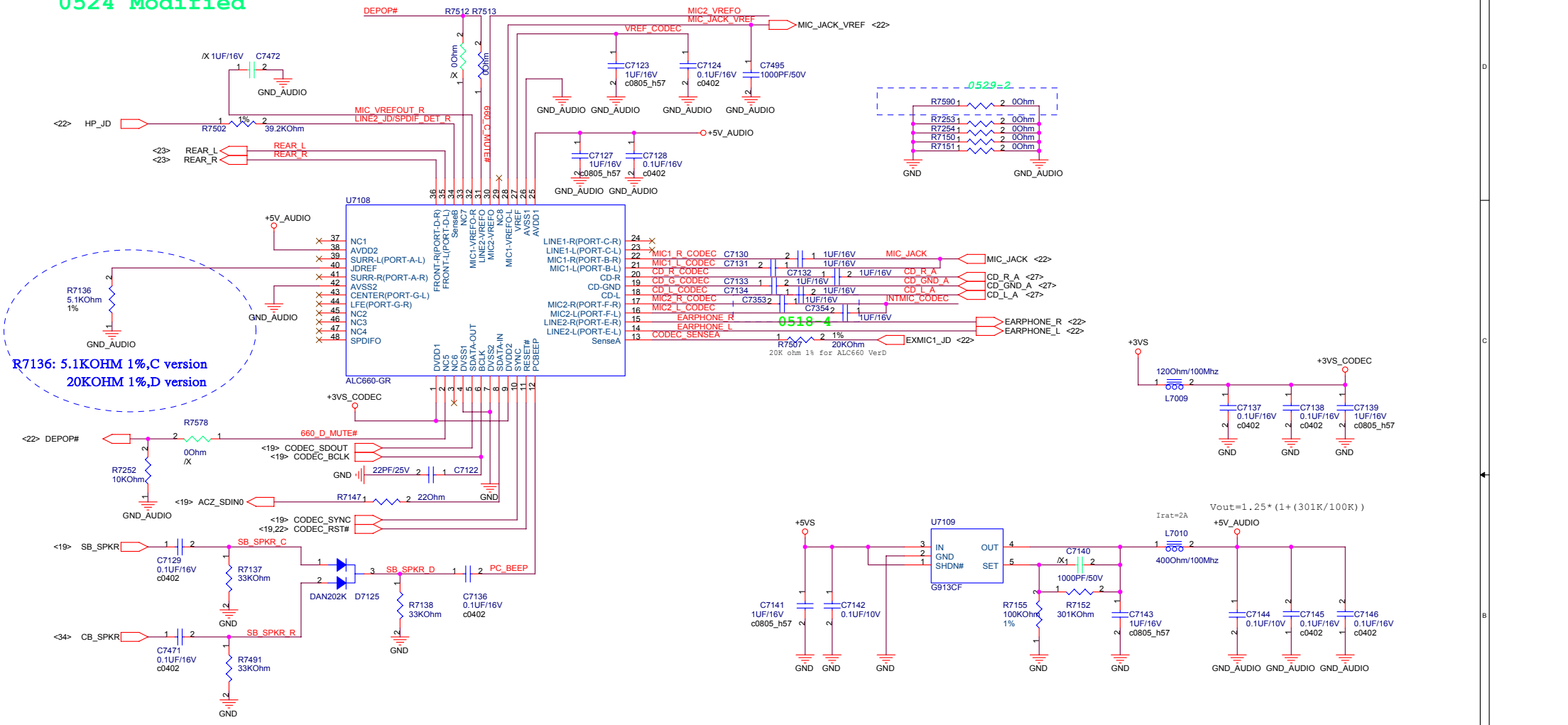

N.V
U9D
MCP51-N-A3
V3P3_DEEP
S0(Busy)~S5=0.1mA
G3=0mA
0522-9
0522: deleted
N.V:Change from 1M to 51K.
USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 5 -> BT Module
USB 6 -> CAMERA
USB 7 -> MINI CARD/TV Tunner
S0(Busy)=?mA
S0(Busy)=5mA
S0(Busy)=20mA
S0(Busy)=15mA
S0(Idle)=18mA
S1=18mA
S3=0mA
MCP51 Strap Option
RTC BATTERY
UNSUED-0310
NOTE 3
N.V:Normal 8uA arround.Max:80uA~160uA arround
RTC cell can use 07G016402032.
(BATT-LI KTS BBBCR2032BA CR2032 3V/220mAh)
ACZ_RST# select
0 MII(10/100M)-(Default)
1 RGMII(1000/100/10M)
BUF_SIO_CLK select
0 14.31818 MHz(Default)
1 24 MHz
MCP51 master/slave mode
0 normal
1 slave mode
Boot mode select
0 User Mode
1 Safe Mode
ASUSTECH CO.,LTD.
Title : MCP51 USB&GPIO&MISC
Engineer: Peace_Lee
Size C
Project Name T12M
Rev 1.1
Date: Tuesday, June 06, 2006
Sheet 19 of 63



ASUSTECH CO.,LTD.	Title : MCP51_POWER&GND		
	Engineer: Bruce_Lee		
Size: C	Project Name: T12M		Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 20 of 63		

AUDIO CODEC

0524 Modified

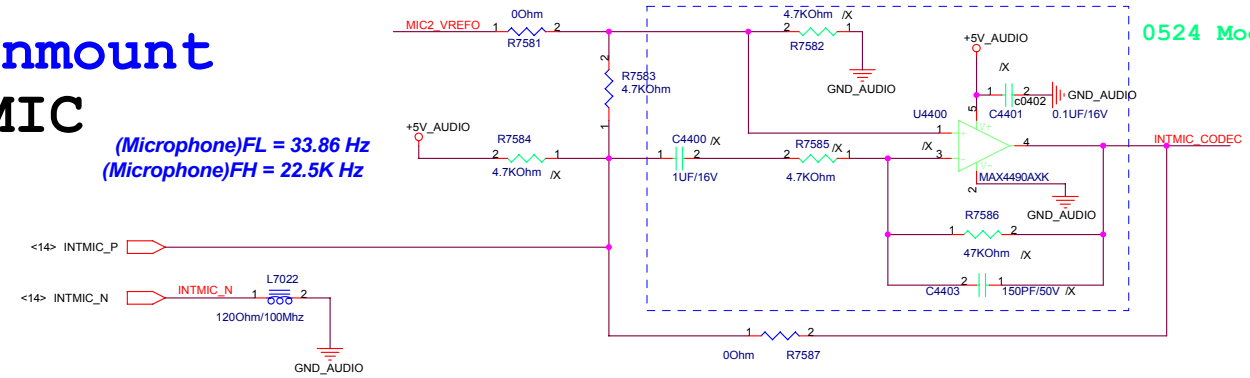


Pre-AMP Unmount

Internal MIC

(Microphone)FL = 33.86 Hz

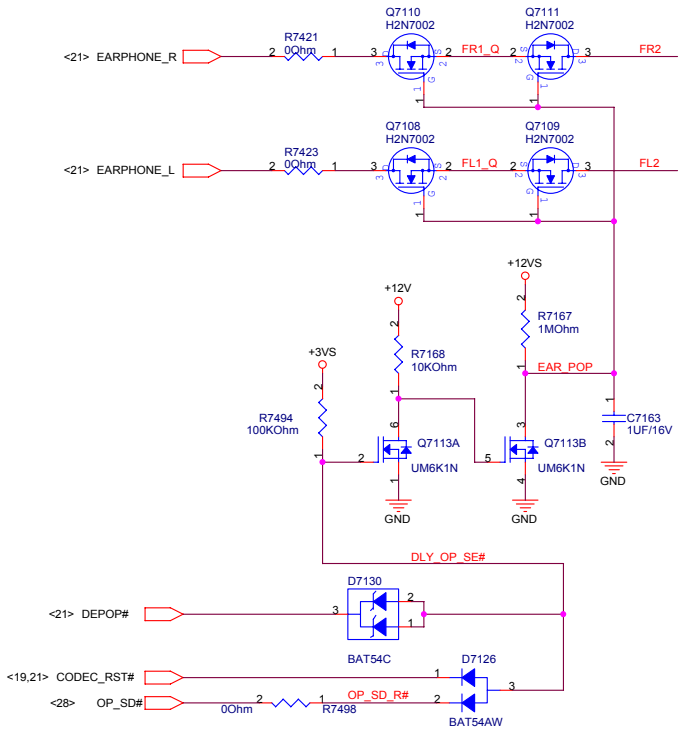
(Microphone)FH = 22.5K Hz



0524 Modified

ASUSTeK COMPUTER INC.	Title : AUDIO CODEC-ALC660	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 21 of 63	

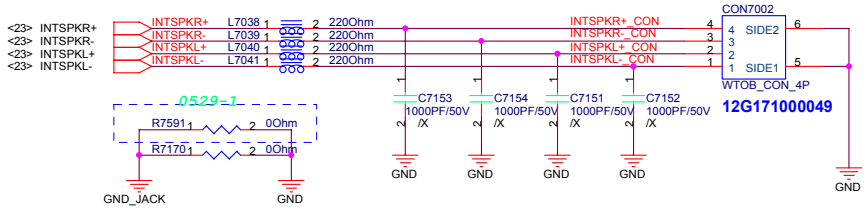
DEPOP CIRCUIT



Fix POP of the internal speaker
when power-on

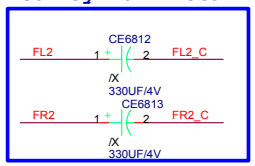
SPEAKER

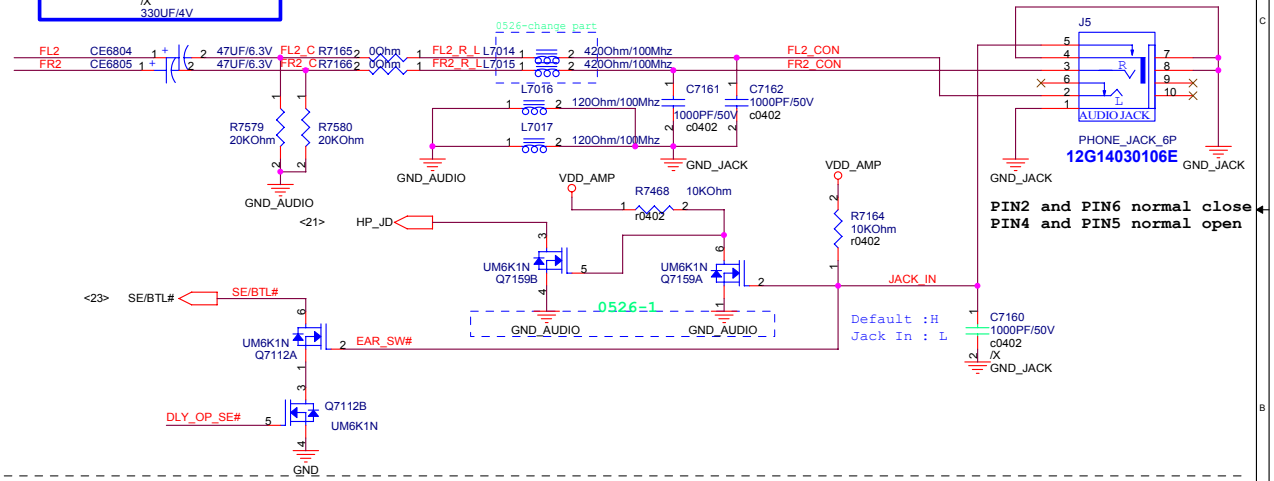
To Internal Speaker Connector



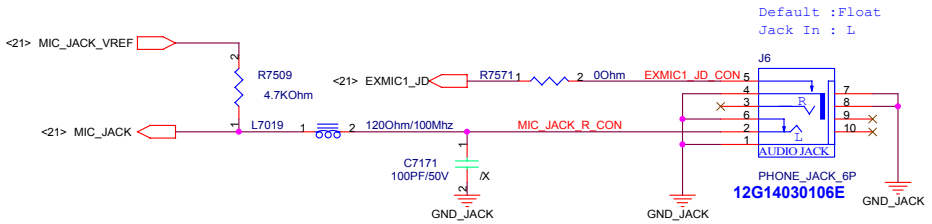
HeadPhone

Co-lay for vista



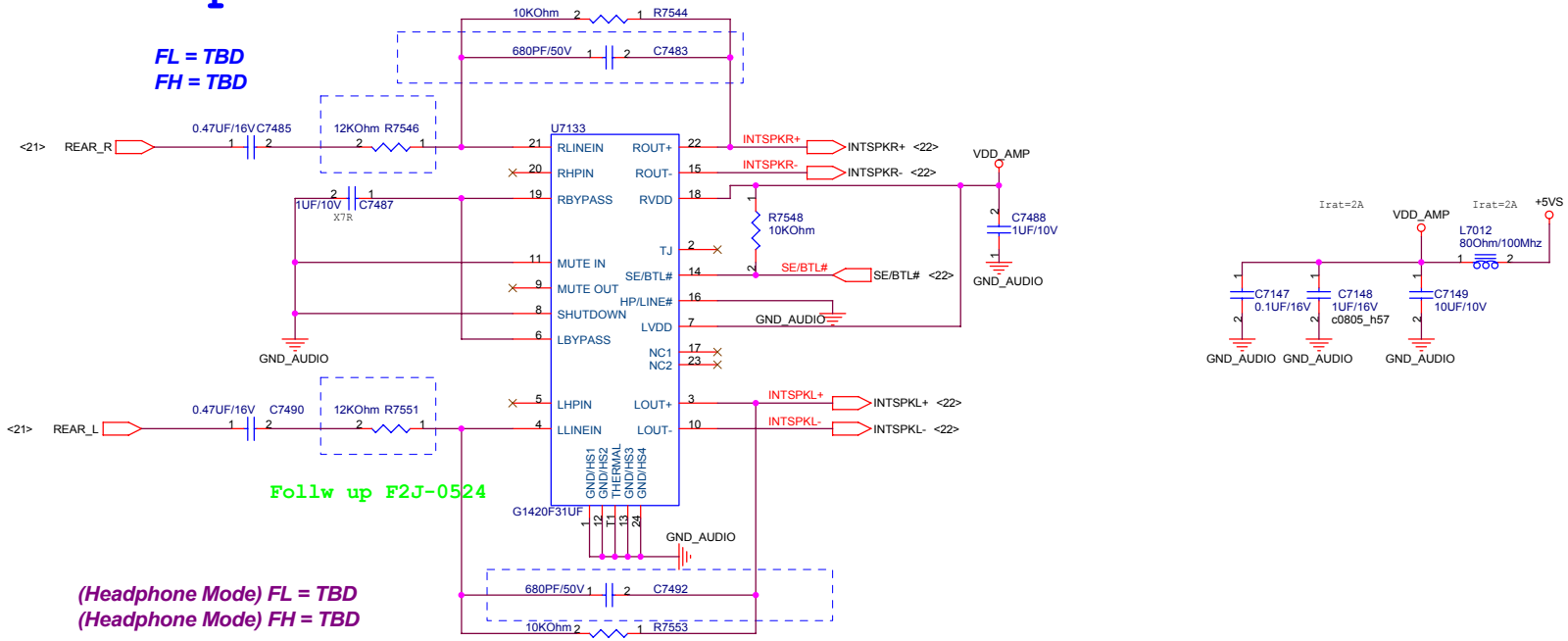


External Microphone



ASUSTeK COMPUTER INC.	Title : AUDIO SPK & JACK	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 22 of 63	

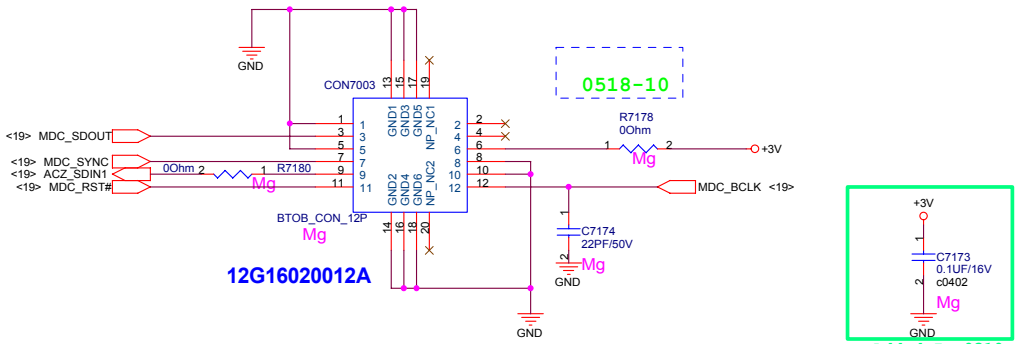
Audio Amplifier

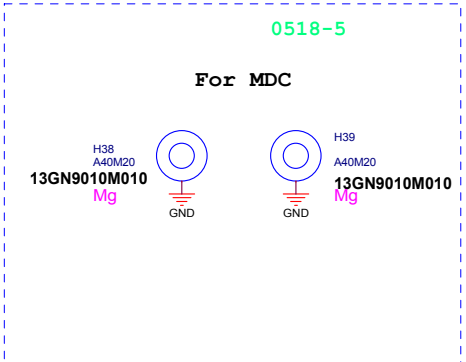


TV-Tuner

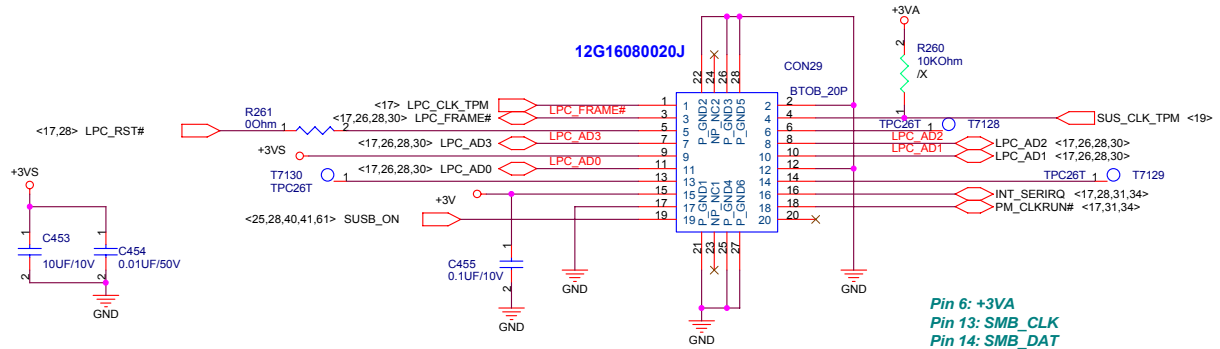
ASUSTeK COMPUTER INC	Title : Audio Amplifier/TV-Tuner	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 23 of 63	

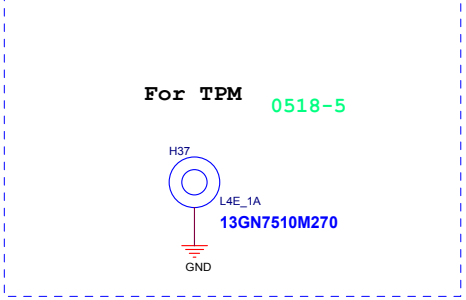
MDC CONN.



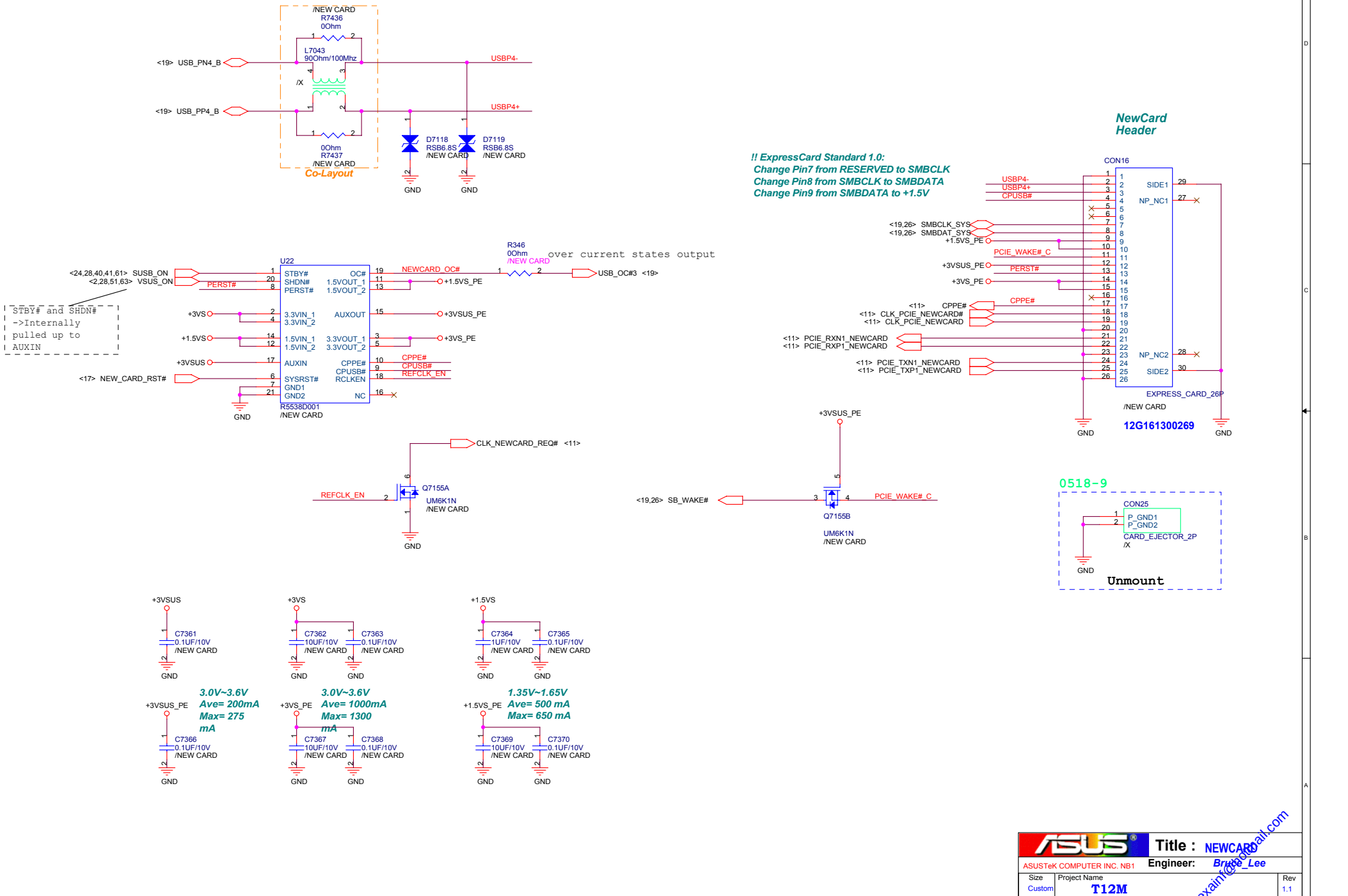


TPM CONN.



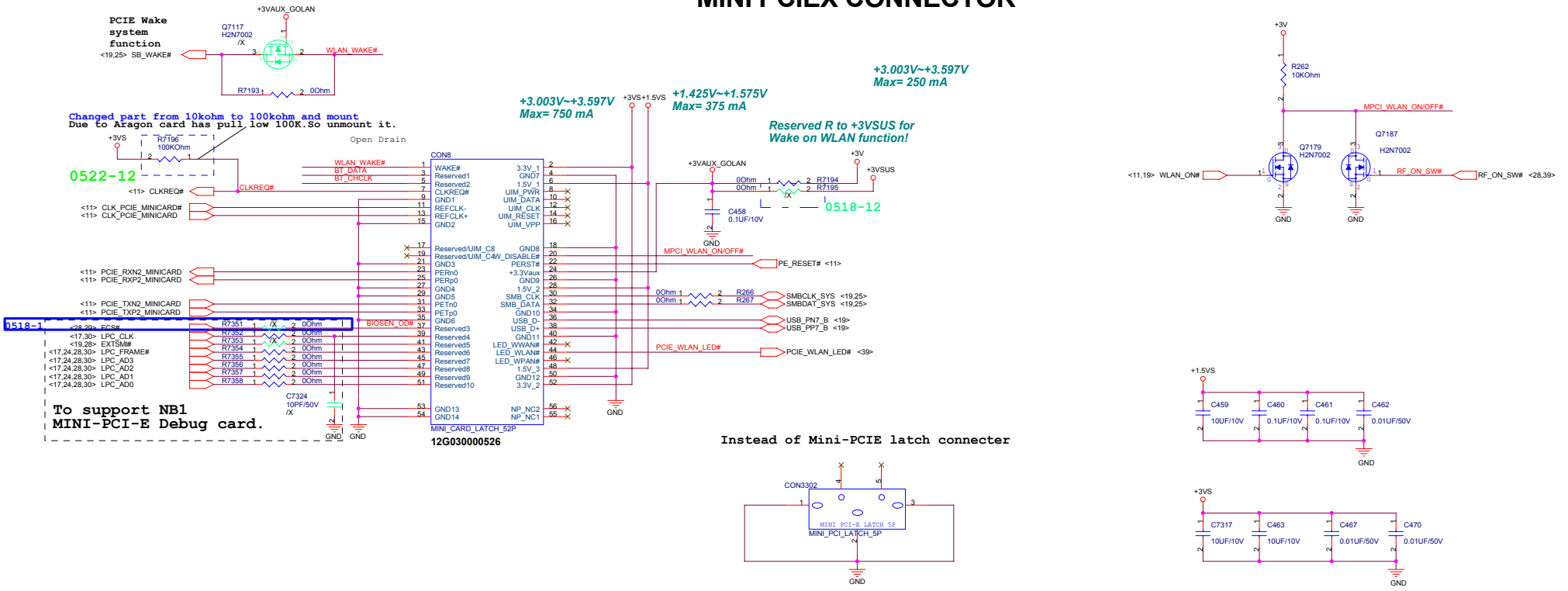


ASUSTeK COMPUTER INC	Title : TPM&MDC CONNECTOR	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 24 of 63	



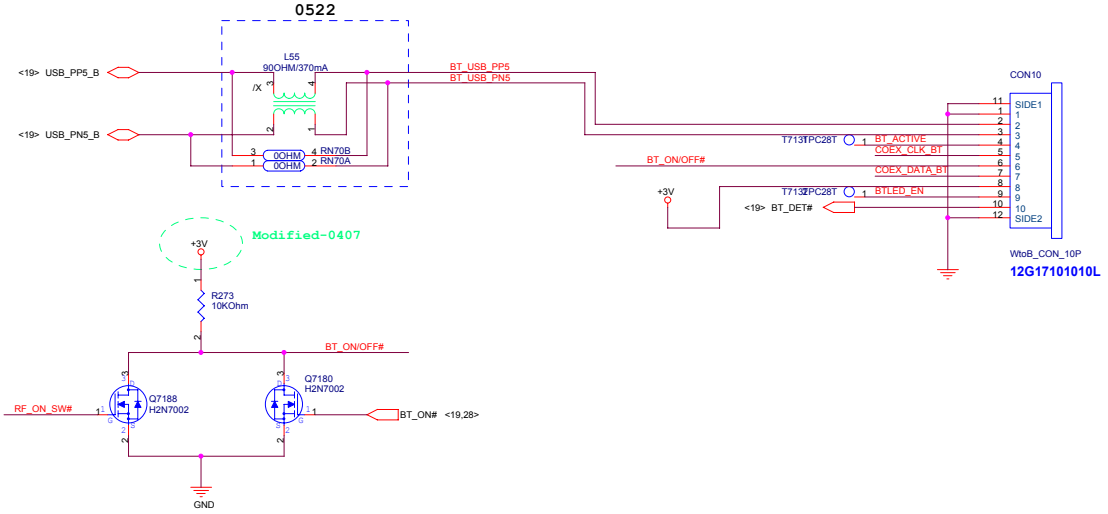
ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 25 of 63	

MINI PCIEX CONNECTOR

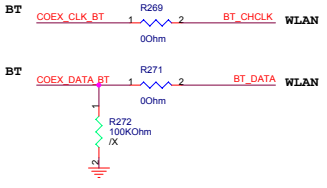


Instead of Mini-PCIE latch connecter

BLUETOOTH CONNECTOR

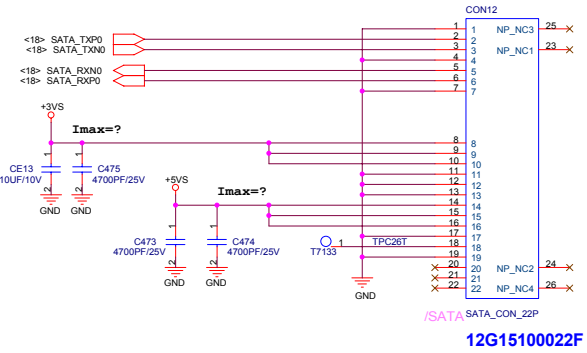


Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT



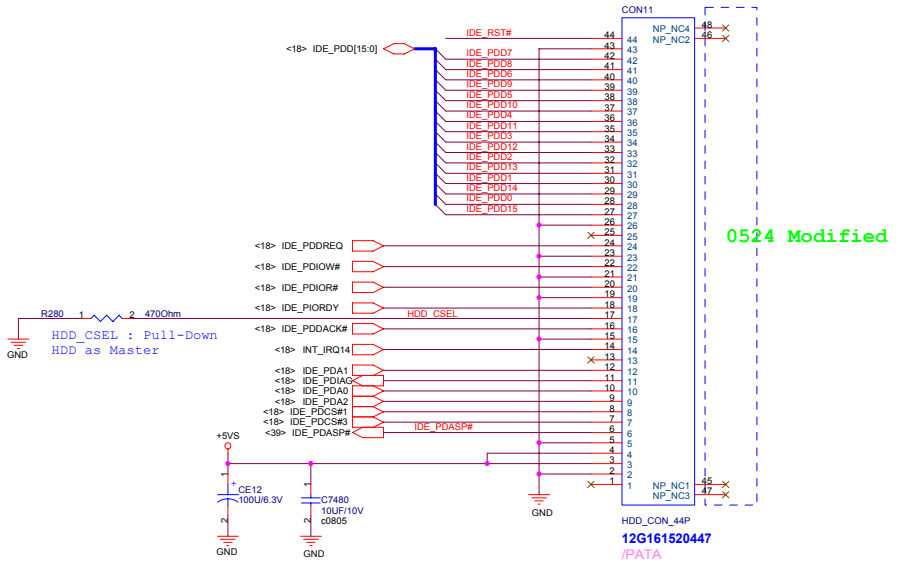
ASUSTeK COMPUTER INC	Title : MINI PCIEX & BT CONN.	
	Engineer: Bruce_Lee	
Size: C	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 26 of 63	

SATA_HDD



12G15100022F

PATA-HDD(Default)

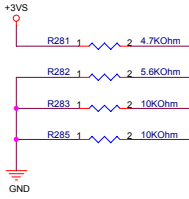


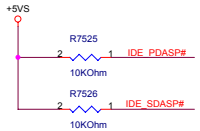
0524 Modified

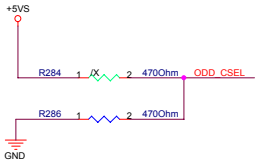
12G161520447

/PATA

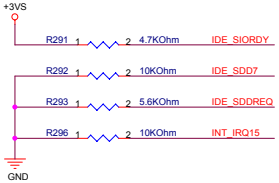
CD-ROM



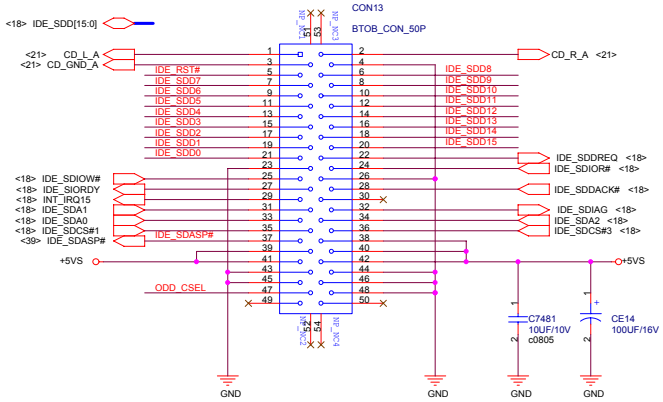


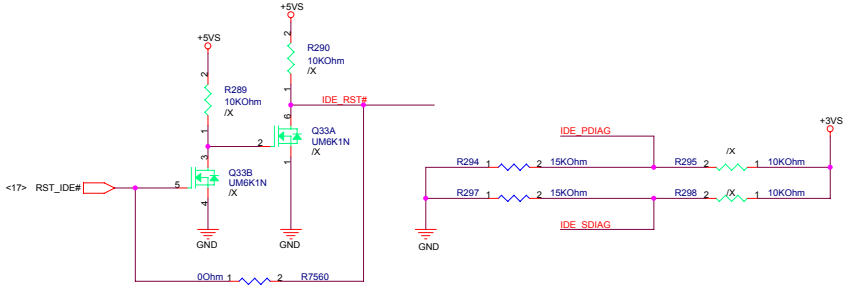


ODD_CSEL
Pull-Up: CDROM as Slave
Pull-Down: CDROM as Master



12G161210504





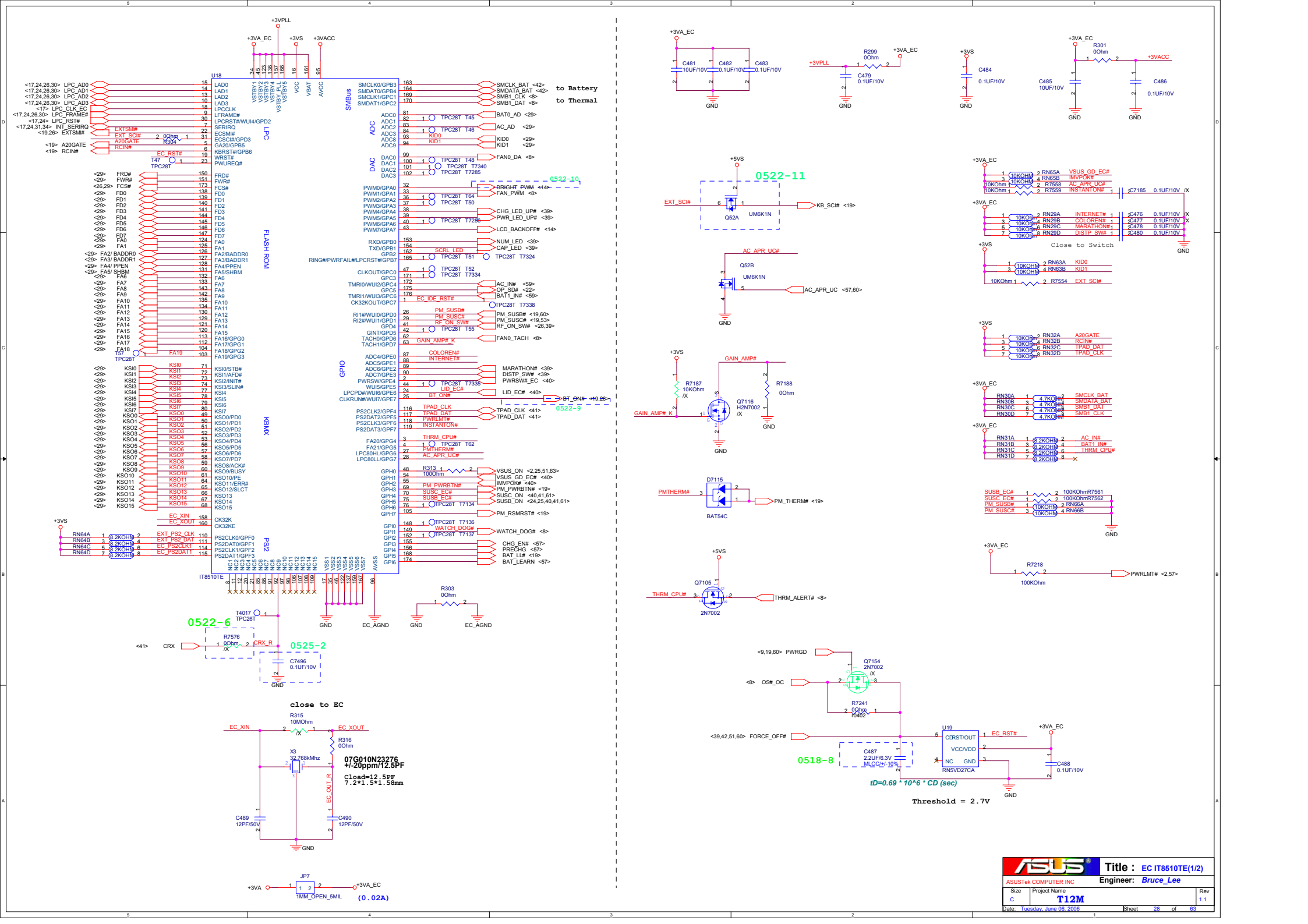
ASUSTEK CO.,LTD.

Title : HDD&ODD CONNECTOR

Engineer: Peace_Lee

Size	Project Name	Rev
C	T12M	1.1

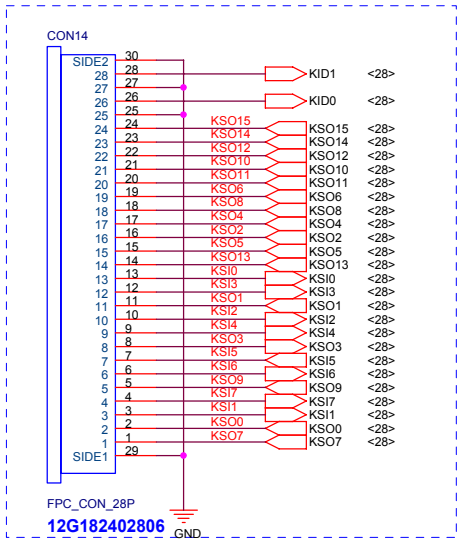
Date: Tuesday, June 06, 2006 Sheet 27 of 63


U18
IT8510TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
close to EC
07G010N23276
+/-20ppm/12.5PF
Cload=12.5PF
7.2*1.5*1.58mm
0522-6
0525-2
0522-10
0522-9
0522-11
0518-8
Close to Switch
tD=0.69 * 10^6 * CD (sec)
Threshold = 2.7V
(0.02A)
Title : EC IT8510TE(1/2)
ASUSTek COMPUTER INC
Engineer: Bruce_Lee
Project Name T12M
Rev 1.1
Sheet 28 of 63
Date: Tuesday, June 06, 2006

KBC connector

For Keyboard
Metrix Define same Z94

0518-7

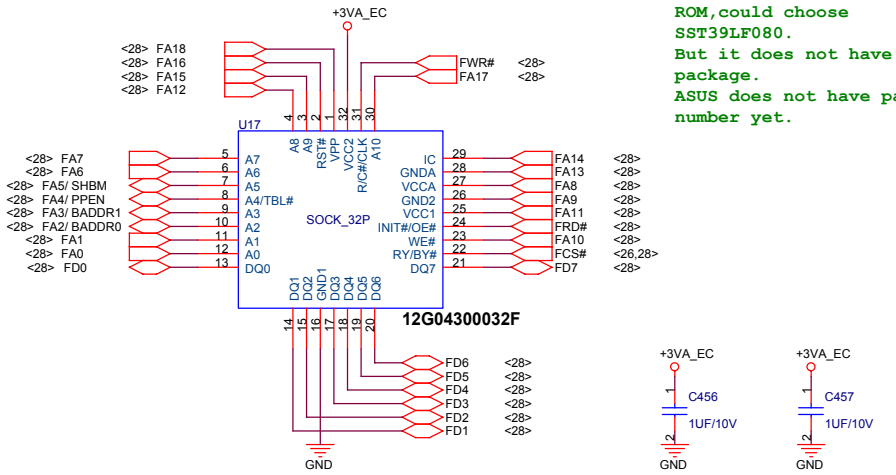


ISA ROM

(4Mbits)

SST-PLCC32 4Mbits Flash ROM
PN:05G001014110
(FLASH SST SST39VF040-70-4C-NHE
4M-70 PLCC-32)

If need to use 8Mbits ISA ROM,could choose SST39LF080.
But it does not have PLCC32 package.
ASUS does not have part number yet.



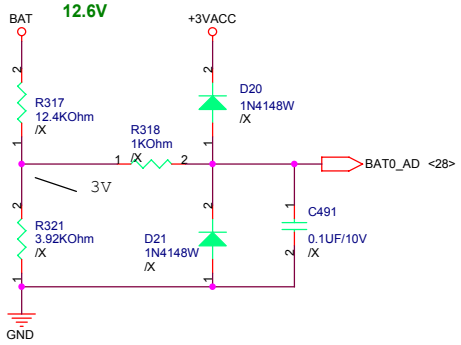
Flash ROM PN:05G001014110

EC ADC

Battery

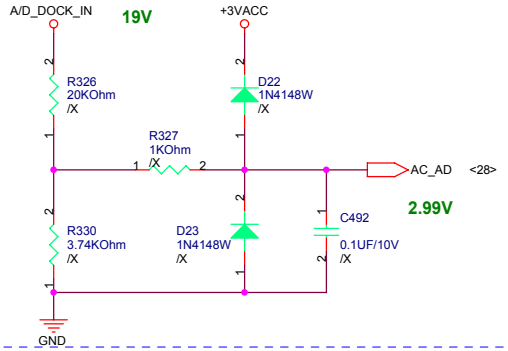
0522-1

12.6V



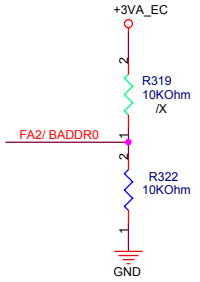
Adaptor

19V

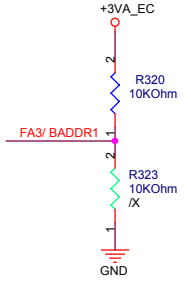


EC Hardware Strap

strap value sampled after VSTBY power up reset

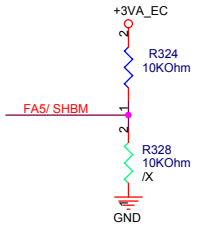


PNPCFG base address set by SWCBAHR/SWCBALR

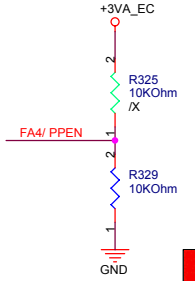


BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Share Memory



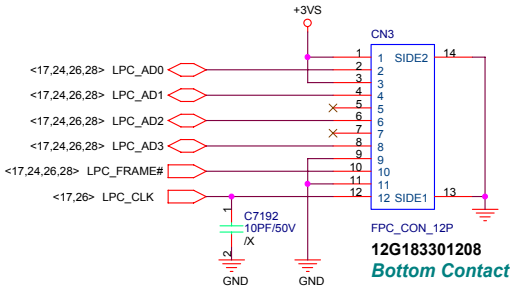
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS



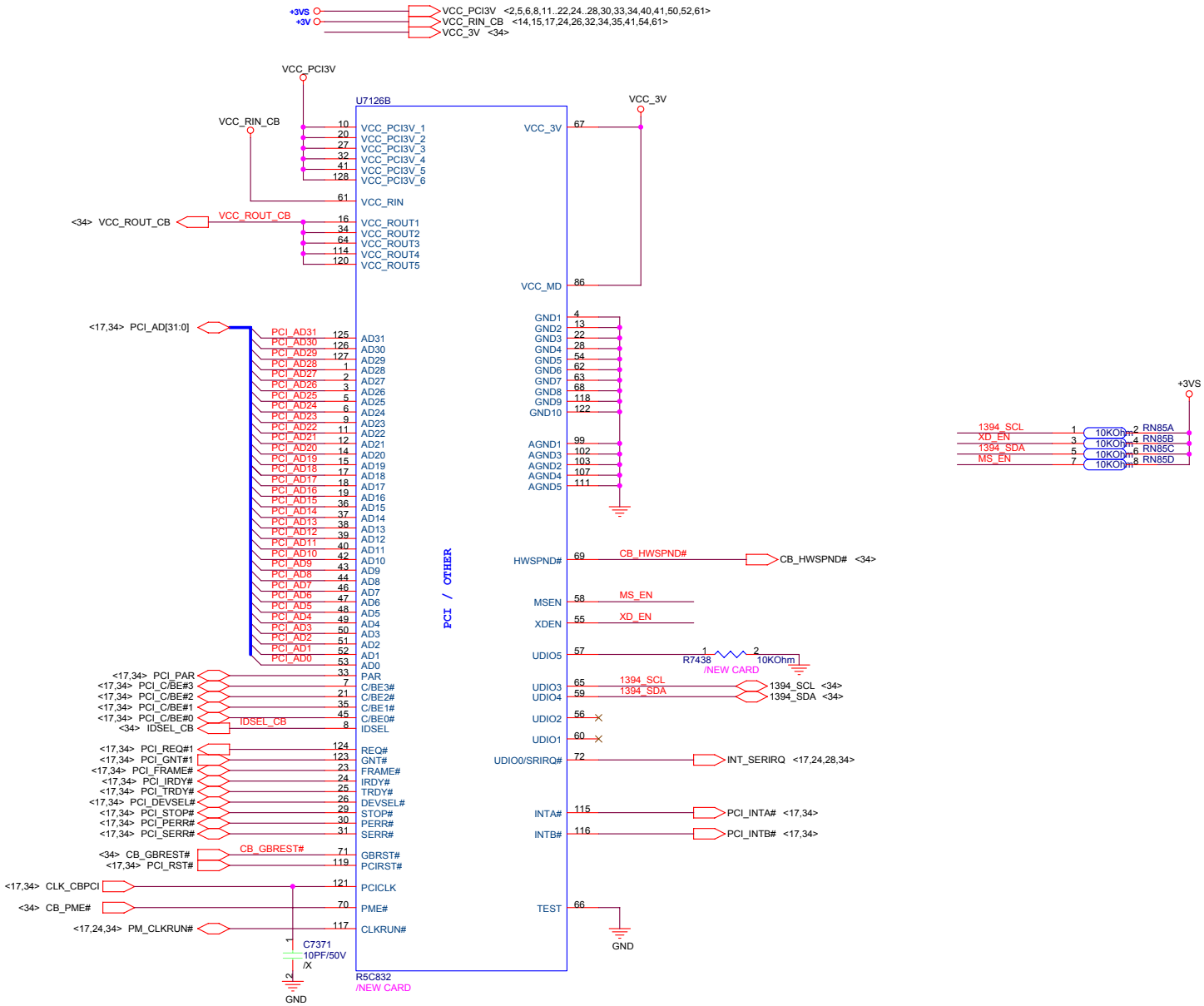
PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

ASUSTek COMPUTER INC	Title : EC IT8510TE(2/2)-ISA ROM&KBC	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 29 of 63	

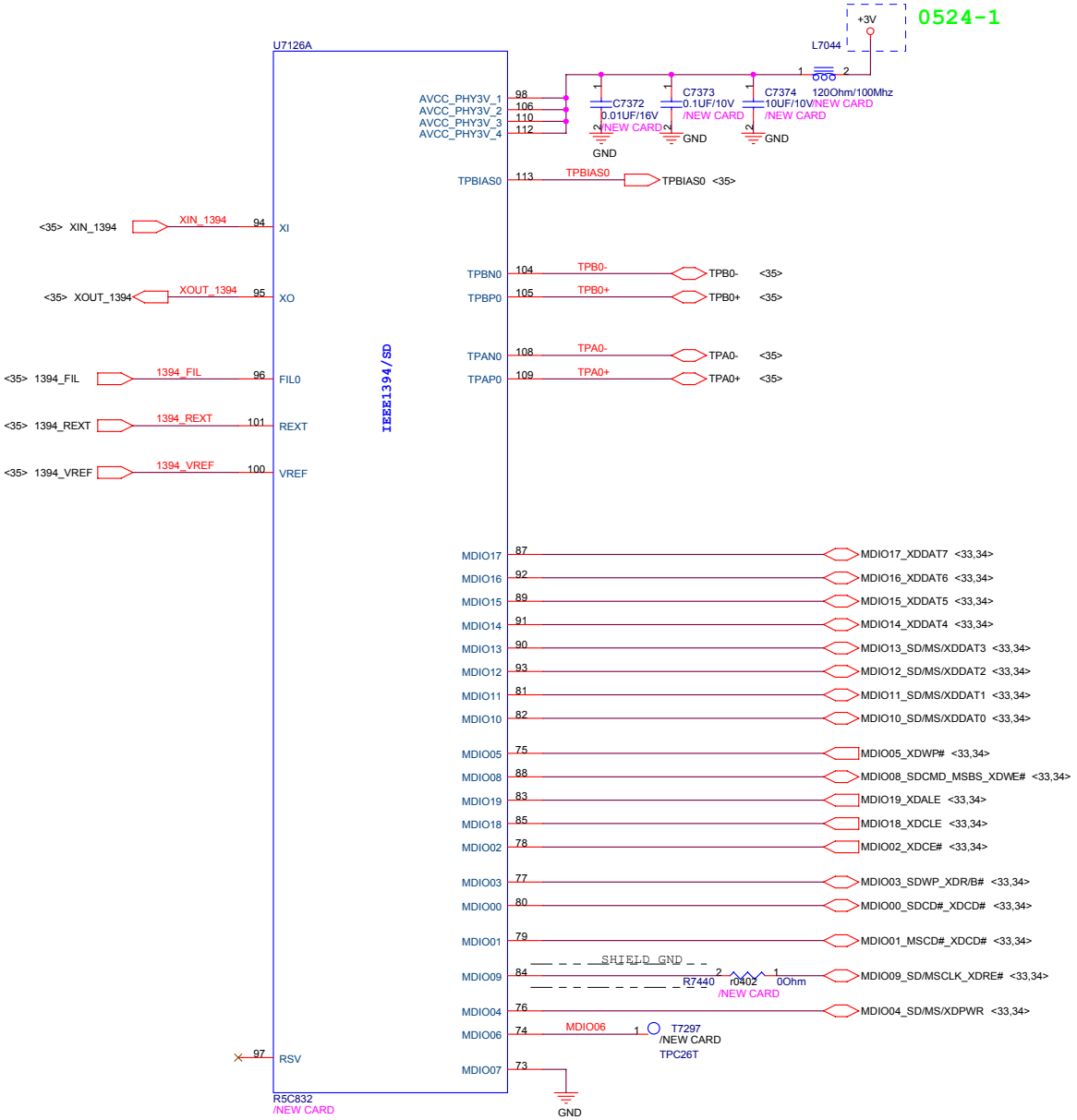
LPC DEGUG CONNCTOR



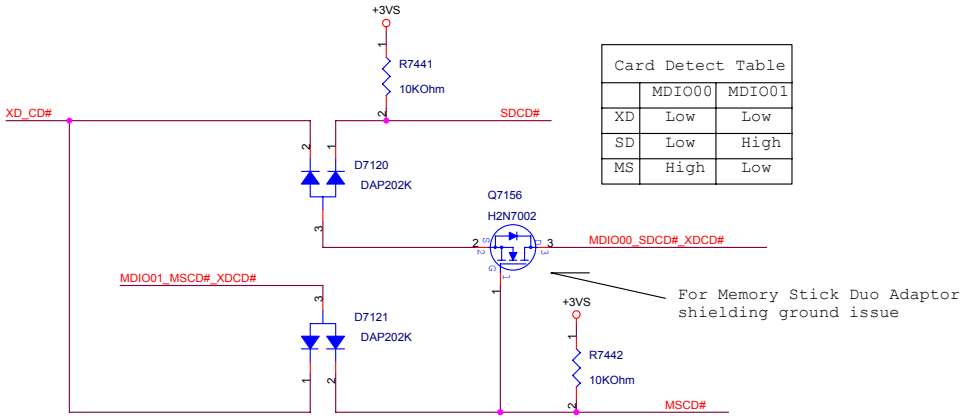
ASUSTeK COMPUTER INC	Title : LPC DEGUG CONNECTOR	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 30 of 63	



ASUSTeK COMPUTER INC. NB1	Title : CARD1394&R5C832(1)	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 31 of 63	

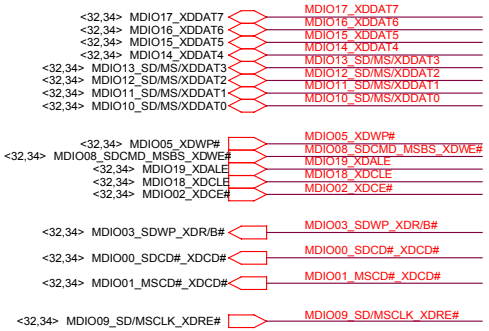


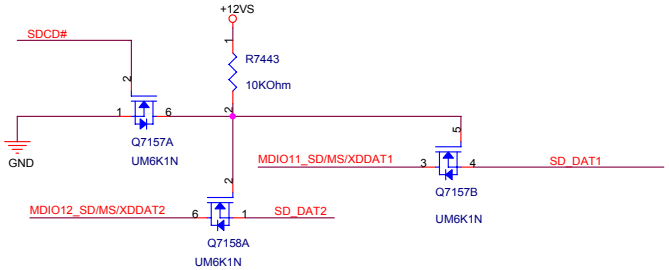
ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 32 of 63	

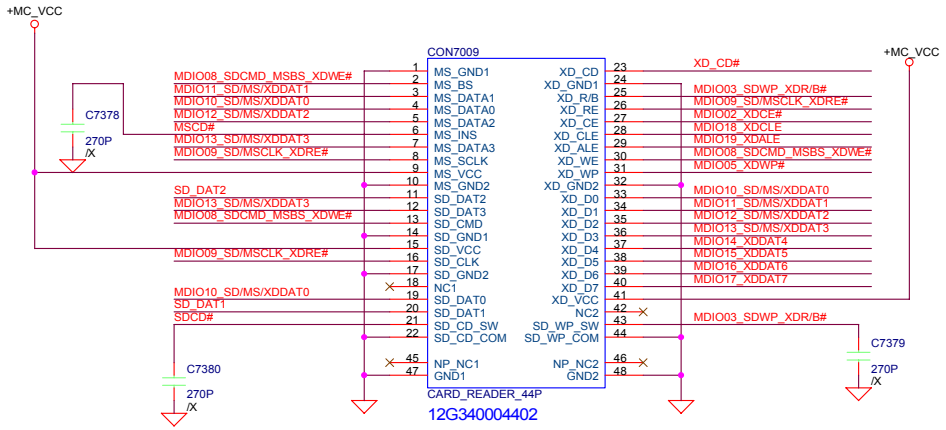


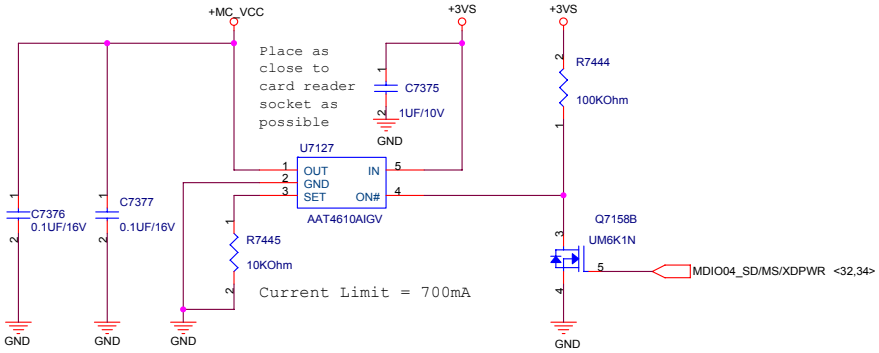
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU









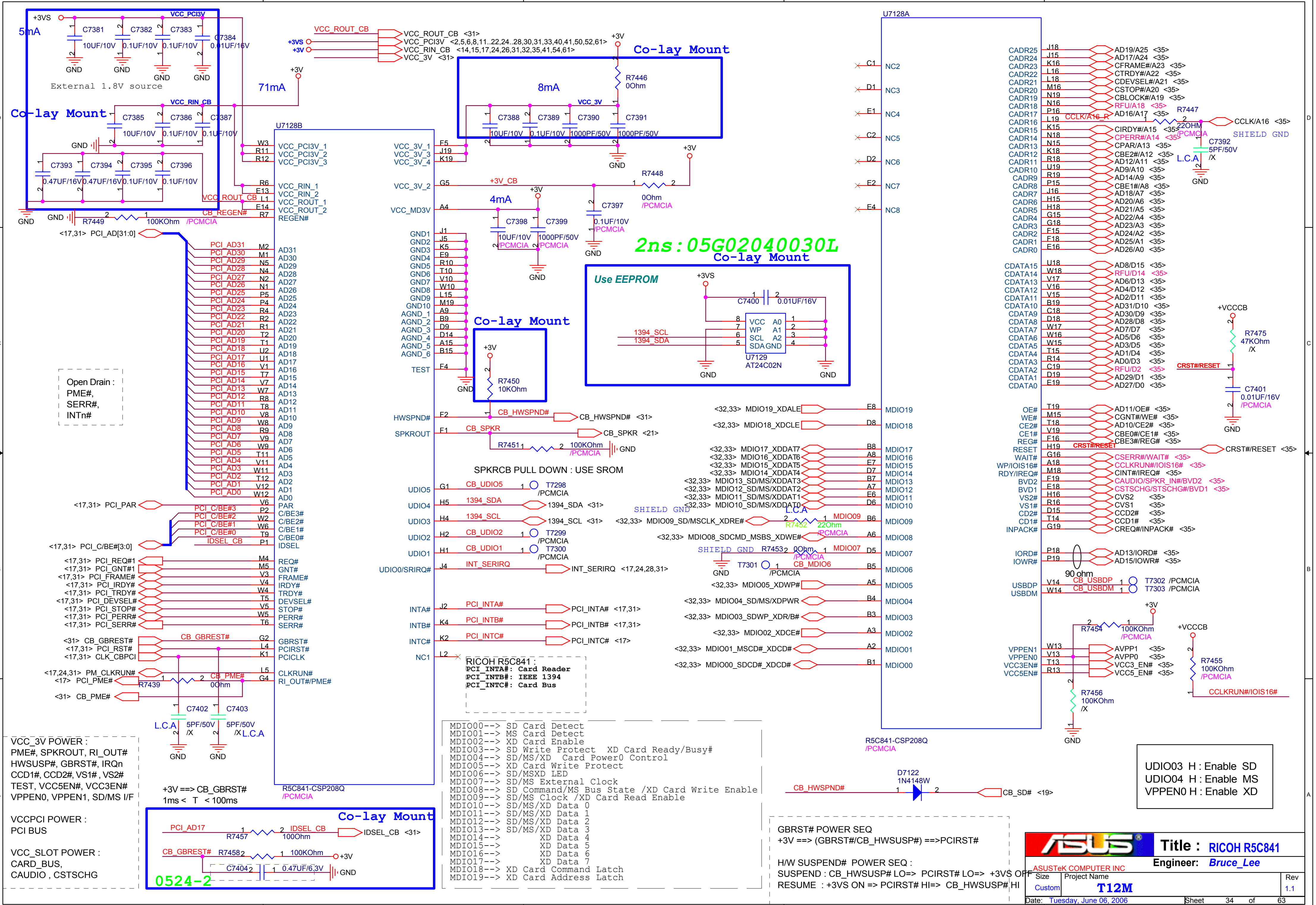
ASUSTeK COMPUTER INC

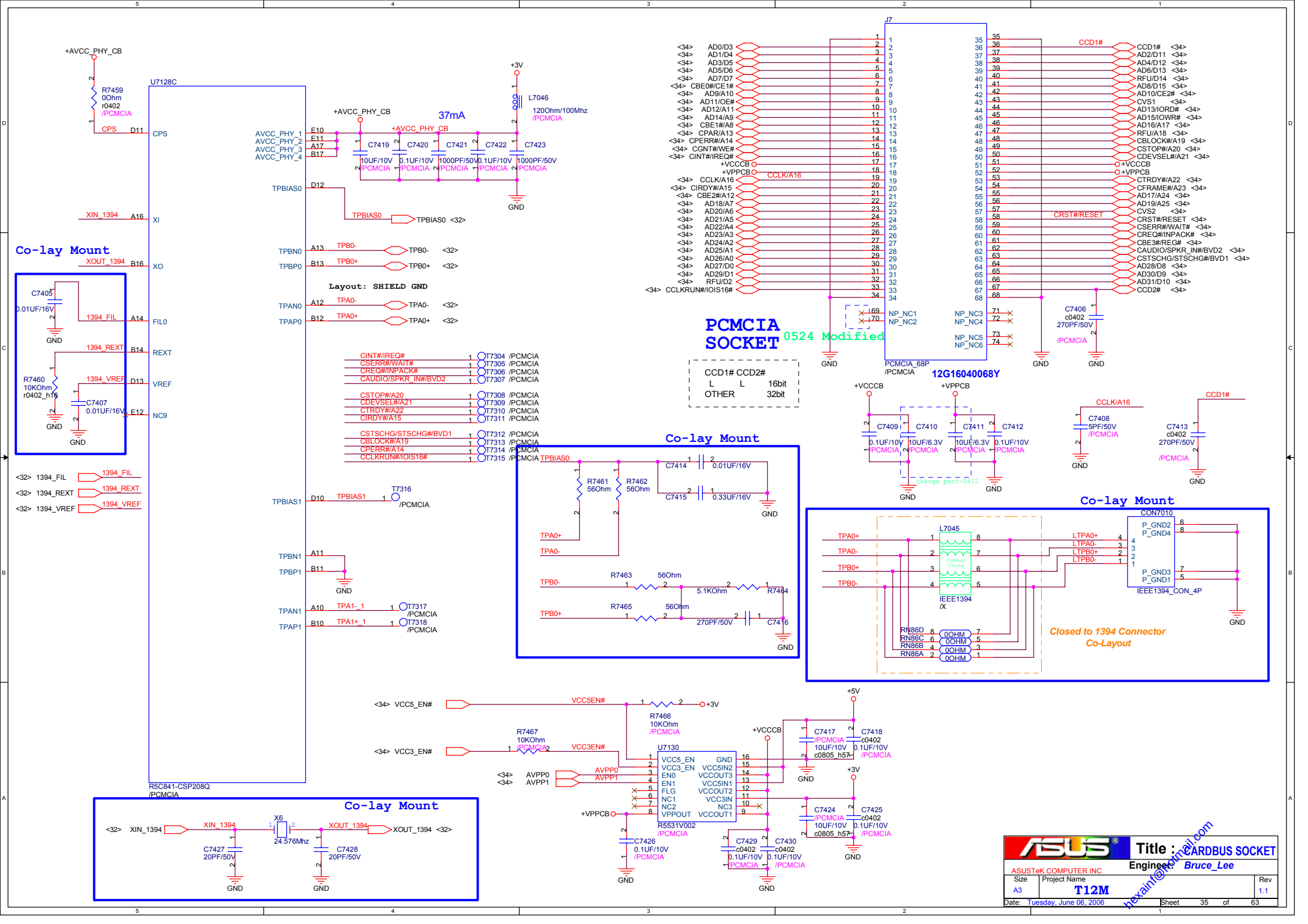
Title : 4 in 1 CARD READER

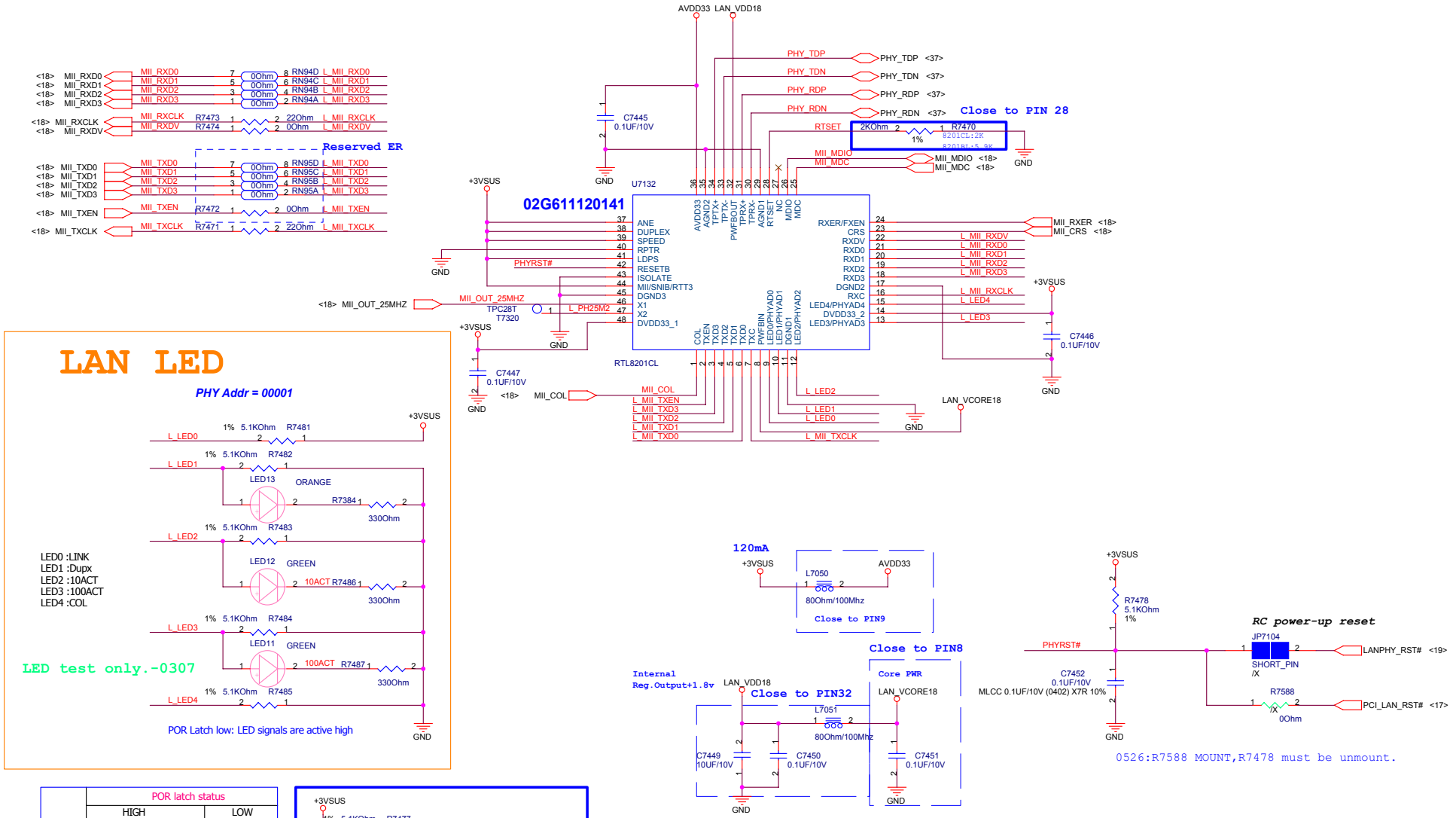
Engineer: Bruce_Lee

Size	Project Name	Rev
Custom	T12M	1.1

Date: Tuesday, June 06, 2006 Sheet 33 of 63

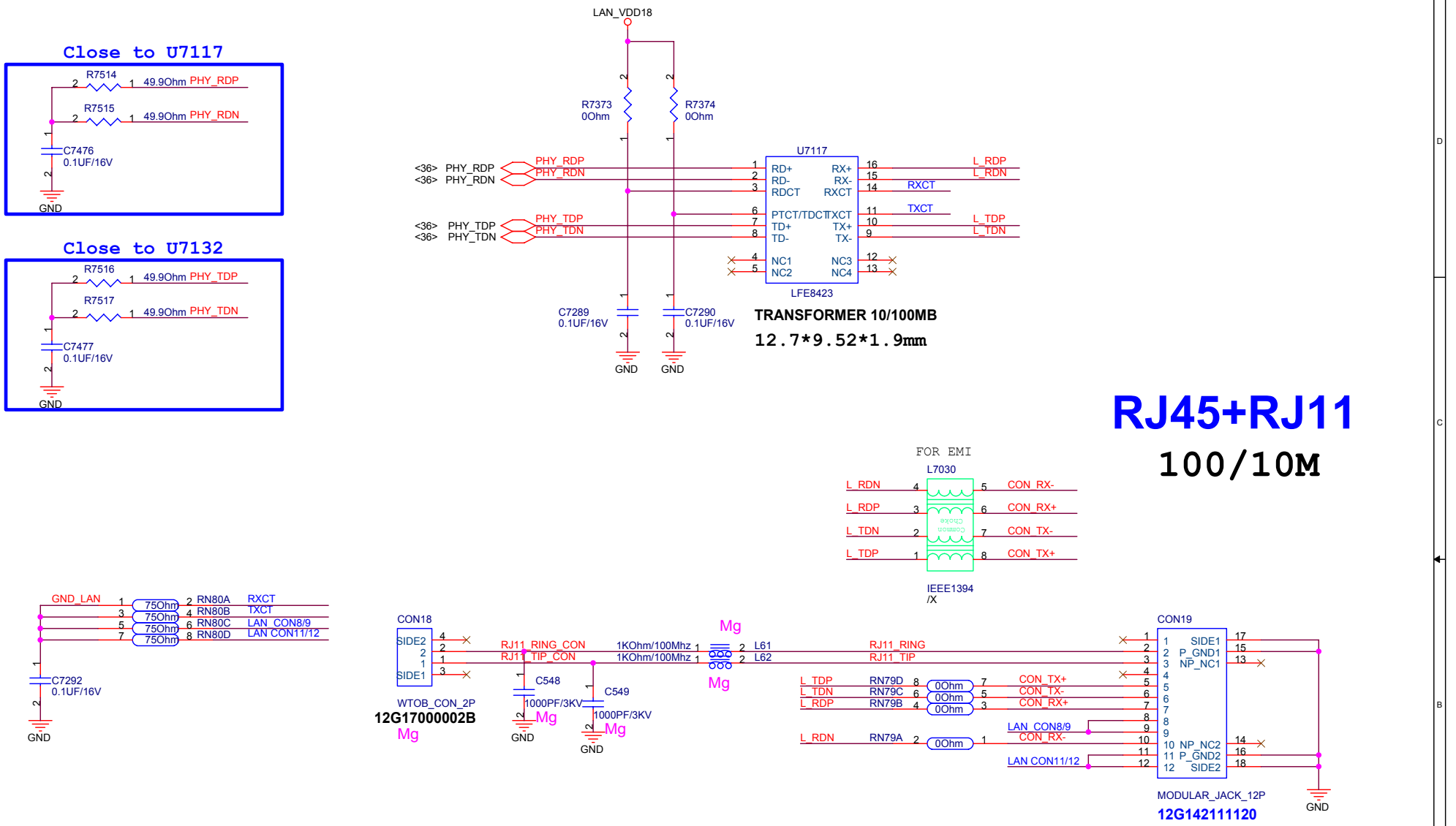

Co-lay Mount
External 1.8V source
5mA
71mA
8mA
4mA
U7128B
U7128A
2ns:05G02040030L
Use EEPROM
U7129
AT24C02N
Open Drain :
PME#,
SERR#,
INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
PCI_INTA#: Card Reader
PCI_INTB#: IEEE 1394
PCI_INTC#: Card Bus
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
0524-2
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
R5C841-CSP208Q
/PCMCIA
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Bruce_Lee
Size Custom
Project Name T12M
Rev 1.1
Date: Tuesday, June 06, 2006
Sheet 34 of 63


PCMCIA SOCKET 0524 Modified
12G16040068Y
PCMCIA_68P /PCMCIA
U7128C
R5C841-CSP208Q /PCMCIA
Co-lay Mount
Layout: SHIELD GND
CCD1# CCD2#
L L 16bit
OTHER 32bit
Closed to 1394 Connector Co-Layout
U7130
R5531V002 /PCMCIA
IEEE1394 /X
IEEE1394_CON_4P
37mA
Title : CARDBUS SOCKET
Engineer: Bruce_Lee
ASUSTeK COMPUTER INC
Size A3
Project Name T12M
Rev 1.1
Date: Tuesday, June 06, 2006
Sheet 35 of 63



	POR latch status	
	HIGH	LOW
ANE	Auto Negotiation Enable	Force mode
DUPLEX	Enable Full Duplex	Disable
SPEED	Operates at 100Mbps	10Mbps
RPTR	Repeater mode	Normal mode
LPDS	LPDS mode	Normal mode
MII/SNIB	MII mode	SNI mode

Title :	LAN PHY_RTL821CL(10/100)
ASUSTeK COMPUTER INC	Engineer: Bruce_Lee
Size: Custom	Project Name: T12M
Rev: 1.1	
Date: Tuesday, June 06, 2006	Sheet 36 of 63



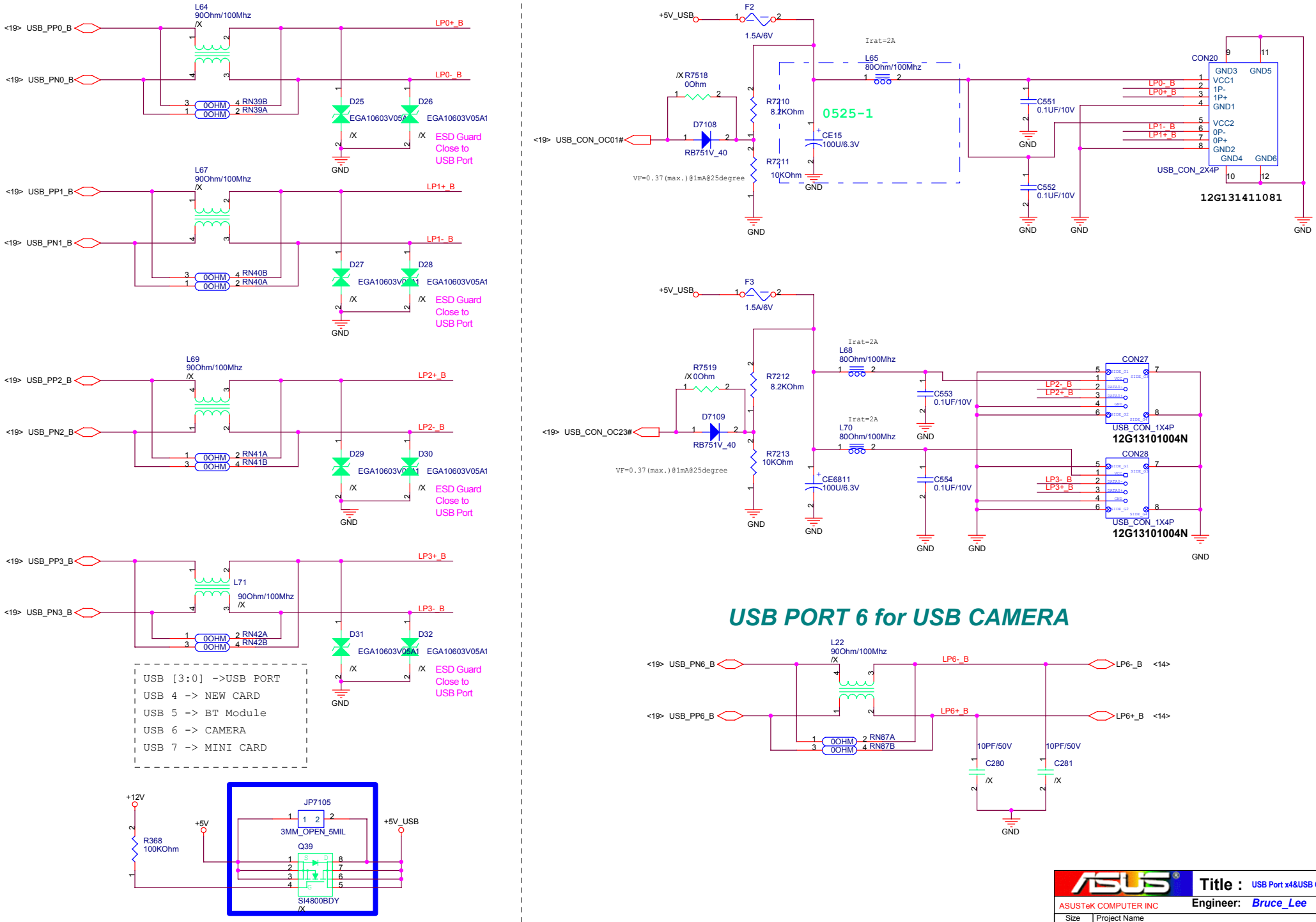
ASUSTeK COMPUTER INC

Title: RJ11&RJ45 CONNECTOR

Engineer: Bruce_Lee

Size	Project Name	Rev
Custom	T12M	1.1

Date: Tuesday, June 06, 2006 Sheet 37 of 63



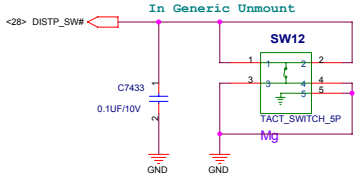
ASUSTeK COMPUTER INC	Title : USB Port x4&USB CAMERA	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 38 of 63	

SW Button

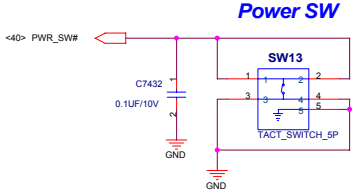
Mv:ParkarBell
Mg: Generic

Disable TP

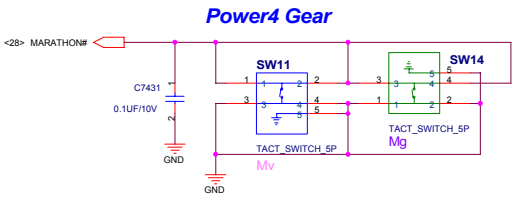
In Generic Unmount



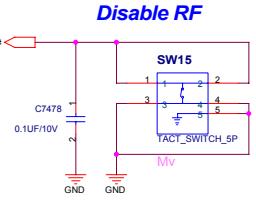
Power SW



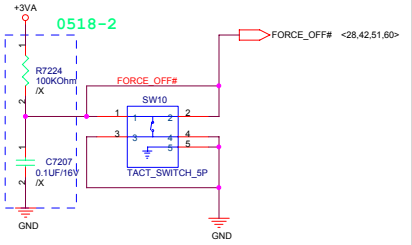
Power4 Gear



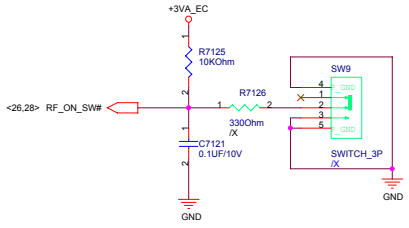
Disable RF



SHUT_DOWN#

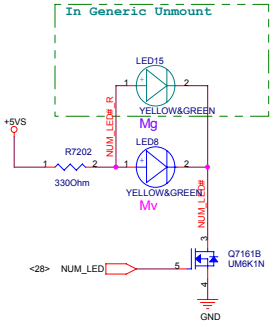


RF ON/OFF SWITCH For Side SW (Left side is turn ON.)

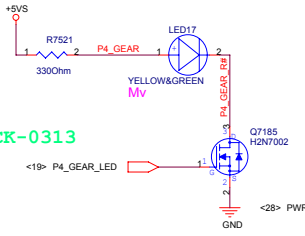


Main Board LED

Num Lock

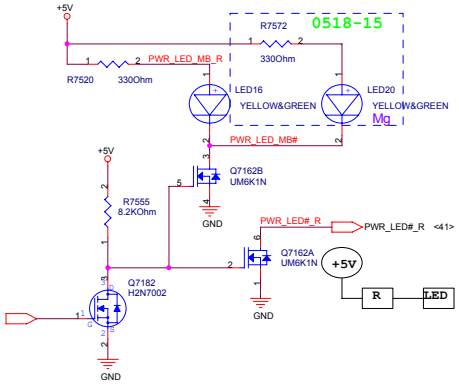


Power4 Gear

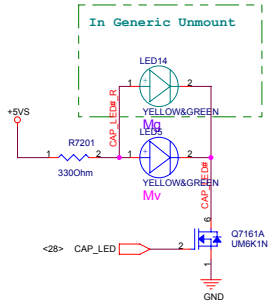


CHECK-0313

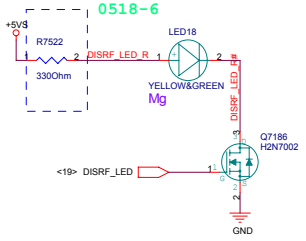
POWER LED



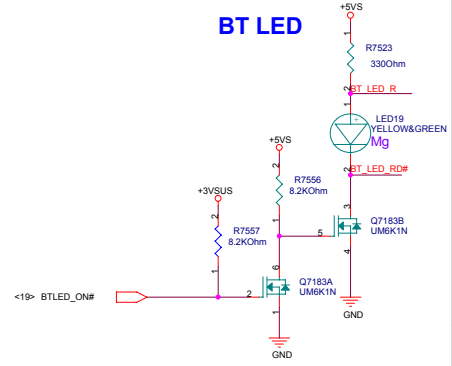
Cap. Lock



DISRF_ LED

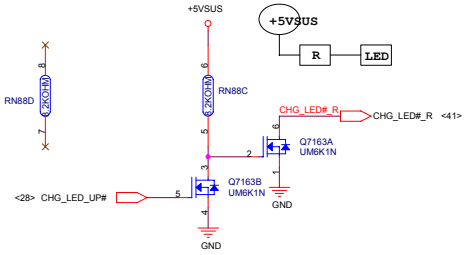


BT LED

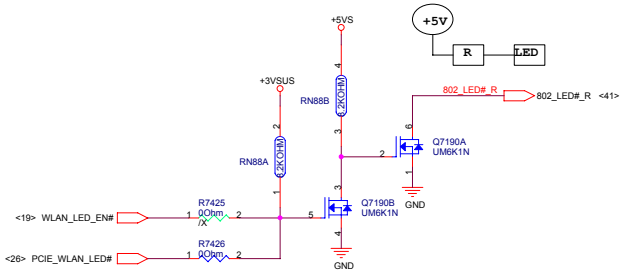


Touch PAD LED

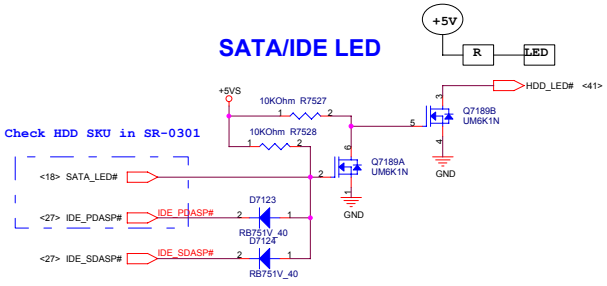
CHARGING LED



WireLess LED



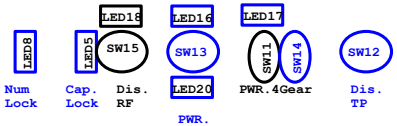
SATA/IDE LED



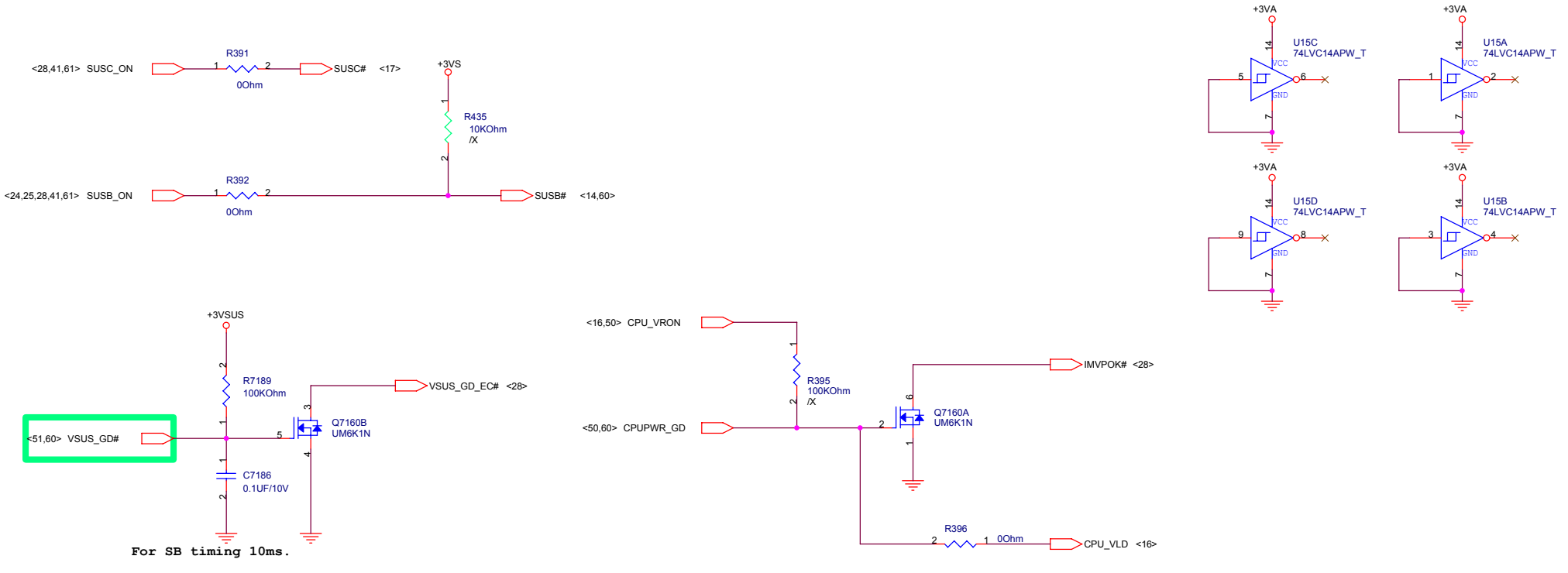
all sw and LED be mounted except sw14 in SR stage-0414

T12M LED & SW Location(TOP VIEW)

Black:Mv
Blue:Mg

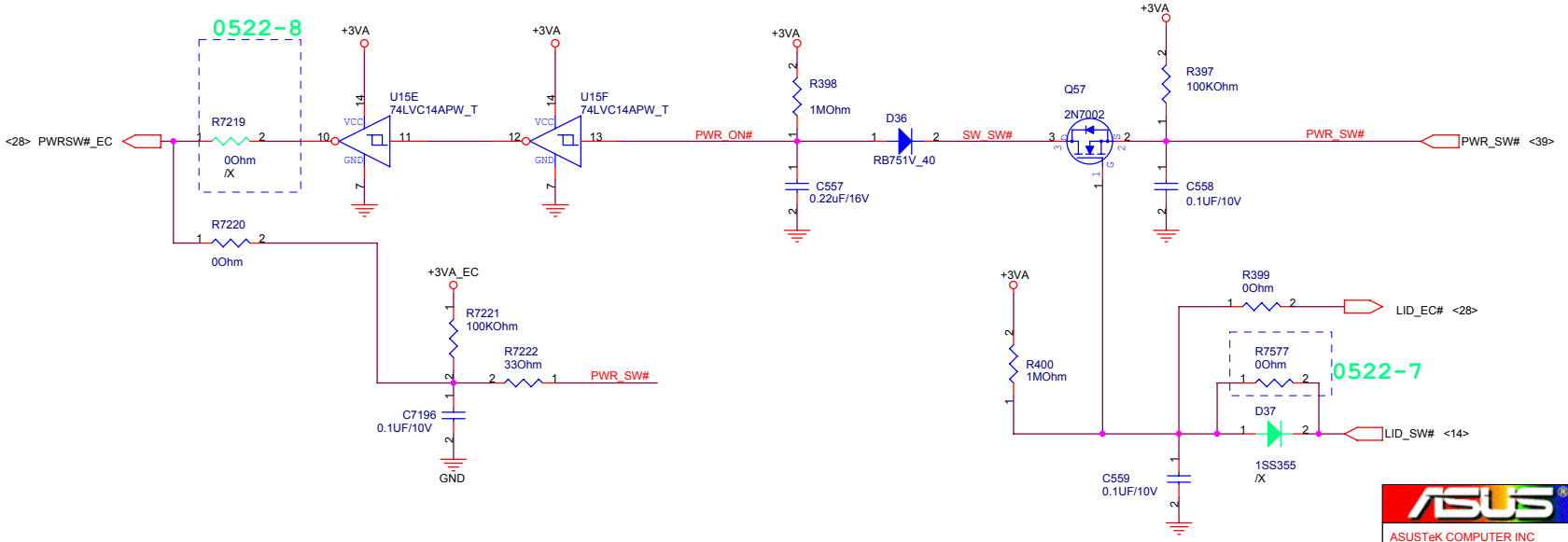


ASUSTeK COMPUTER INC
Title : LED & SW
Engineer: Bruce_Ke
Size: Custom
Project Name: T12M
Rev: 1.1
Date: Tuesday, June 06, 2006
Sheet 39 of 63



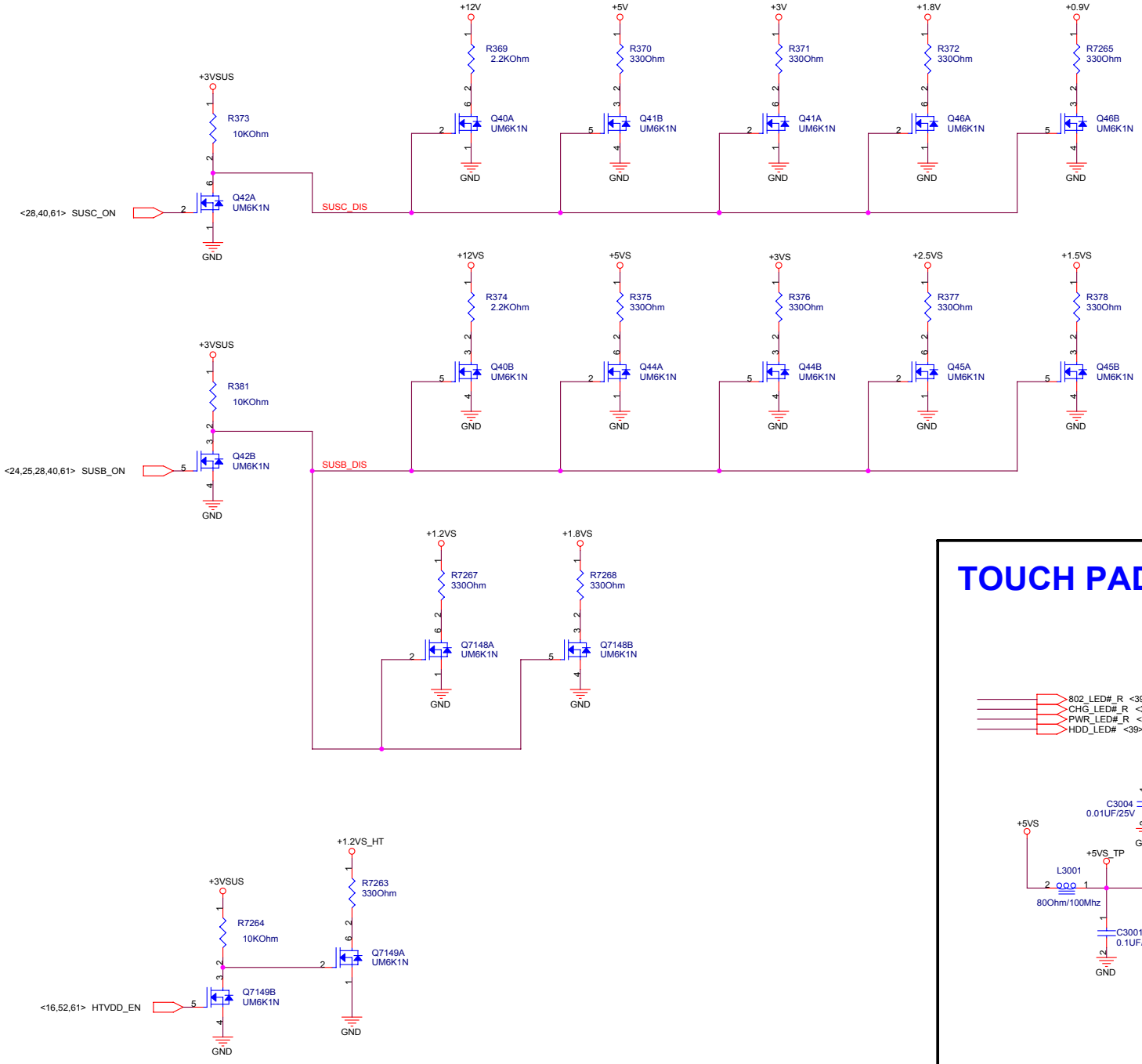
POWER SWITCH

PR UNMOUNT

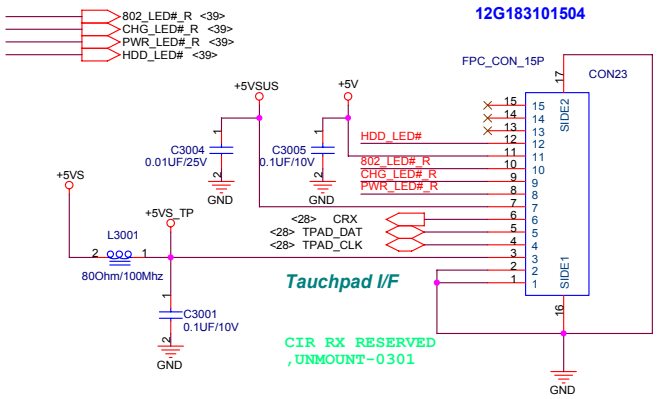


ASUSTeK COMPUTER INC	Title : POWER-ON SEQUENCE	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 40 of 63	

DISCHARGE CIRCUIT

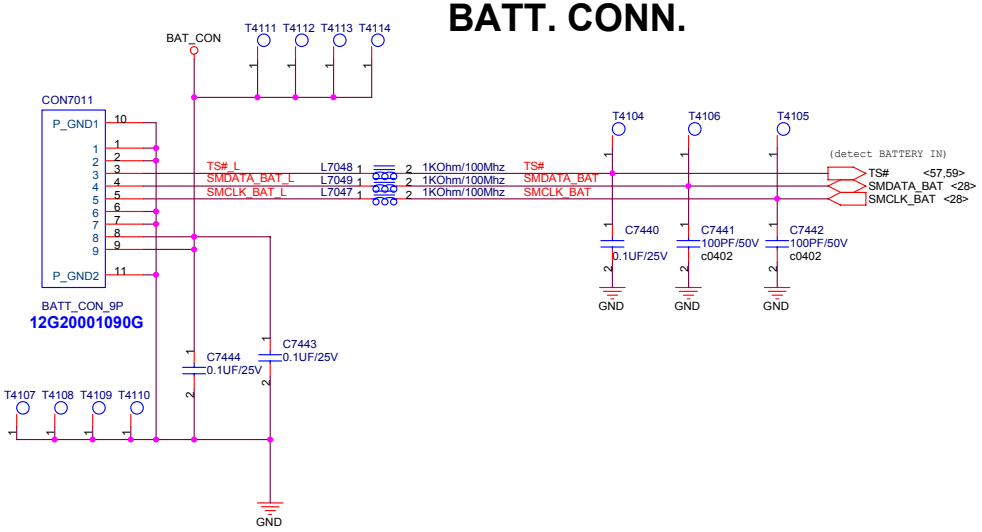


TOUCH PAD

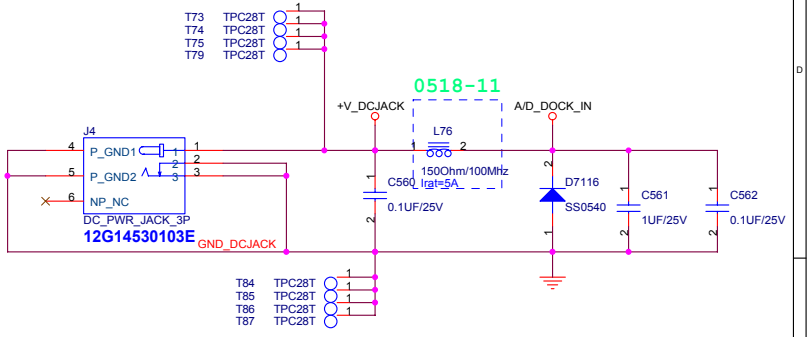


ASUSTeK COMPUTER INC	Title : Discharge Circuit & TP	
	Engineer: Bruce Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 41 of 63	

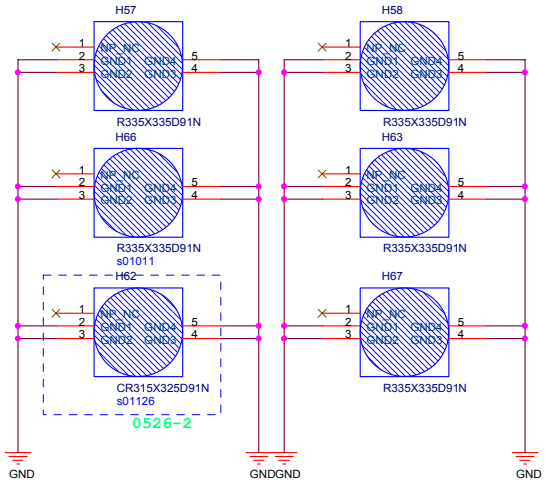
BATT. CONN.



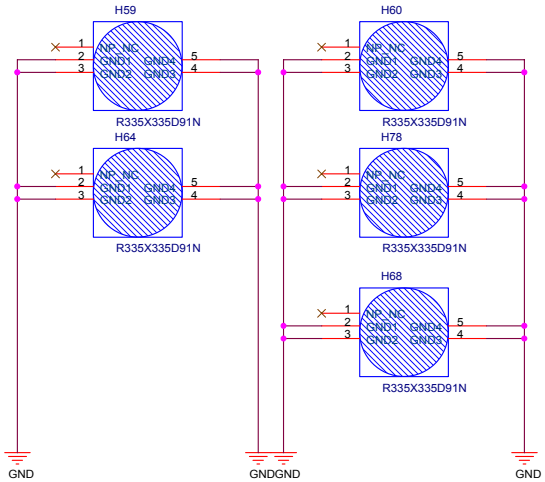
DC Power Jack



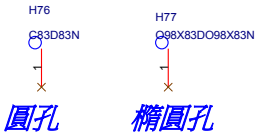
A Hole / TOP Side



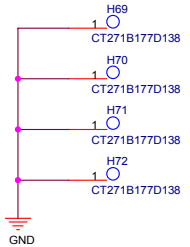
A Hole / Bottom Side



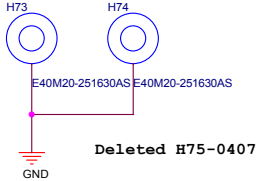
Drill Hole for Fix



F Hole for CPU

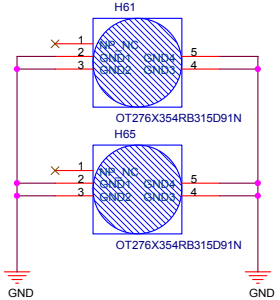


銅柱 Hole for VGA 13GNCF10M010

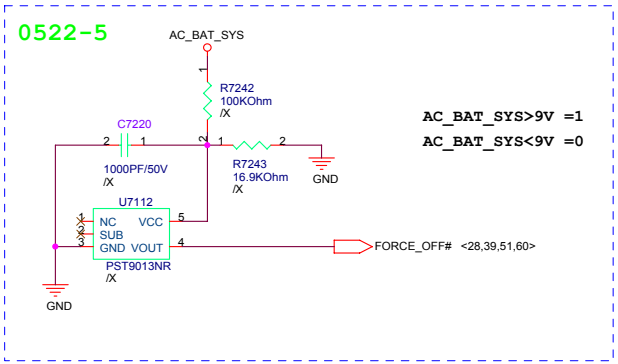


Deleted H75-0407

E Hole for Main board fix



Without Battery & Pull out Adapter



ASUSTeK COMPUTER INC	Title : DC IN & SCREW HOLE	
	Engineer: Bruce_Lee	
Size: Custom	Project Name: T12M	Rev: 1.1
Date: Tuesday, June 06, 2006	Sheet 42 of 63	

ASUSTek COMPUTER INC.	Title : N/A	
	Engineer: Sam_Wang	
Size: Custom	Project Name: F3M	Rev: 1.0
Date: Tuesday, June 06, 2006	Sheet 43 of 63	

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, June 06, 2006
Sheet	44 of 63

T12M ER Update History

0518

0518-1: R7351 unmounted for LPC debug massage display

0518-2: R7224 & C7207 umnounted for EC_ RST# timing impact,P-39

0518-3: Deleted OS#_OC P-U to RN76A for EC_ RST# timing impact,P-8

0518-4:Mount C7353 &C7354,R7413/R7415,R7418 for internal MIC,P-21

0518-5:H37 ,H38/H39 changed PN,P-24

0518-6:Mount R7522,P-39

0518-7:Correct KBC pin definiation in CON14,p-29

0518-8:C487 tolerance be changed to X5R,P-28

0518-9:CON25 unmounted,ASSY' part,p-25

0518-10:Removed "JP7103" for MDC power option,p-24

0518-11: "L76" be changed current rating to 5A,P-42

0518-12:Unmounted "R7195",p-26

0518-13:R131 be change to 2.4KOHM , R132 be changed to 1.47kohm For MAC Vref,p-18

0518-14:"R1205" P-U power be changed from"+3VS " to "+3VS_LCD" for white screen when sys. reboot, p-14

0518-15:Added in "R7572"&"LED20" for brightness improvement,p-39

0519

0519-1:Changed D-SUB Conn. by ME ,P-15

0522

0522-1:EC ADC parts unmount ,P-29

0522-2:R7233 change part from"1.2kohm"to "0ohm',p-8

0522-3:R? reserved 100kohm,p-14

0522-4:N/A

0522-5:UNMOUNT FOR COST DOWN,P-42

0522-6:RESERVERD R? FOR CRX,P-28

0522-7:RESERVERD R? FOR COST DOWN,P-40

0522-8:UNMOUNTED R7219 and mounted R7220 power seq. controlled by EC,P-40

0522-9:BT_ON# contorlled by EC,P-28 &P-19

0522-10:BL contorlled by EC form DAC to PWM,P-28

0522-11:UM6K1N body diode changed direction,p-28

0522-12:Changed R7196 from 10kohm to 100kohm and mount,p-26

0522-13:DDR termination resistor SWAP,P-7

0524

0524-1:1394 power changed from +3vs to +3v, resume form s3 detect fail,p-32

0524-2: C7404 changed to 0.47uf for pwr. up seq.,p-34

0524

0524-1:CE15 changed net-name by EMI,P-38

0524-2:C7496 added in CRX signal,P-28

0525

0525-1:Q7159 GND changed to GND_AUDIO,EMI,P-22

0525-2:H62 change part no.,p-42

0529

0529-1-:Added in R7590 between GND and GND_AUDIO,P-21

0529-2:Added in R7591 between GND and GND_JACK,P-22

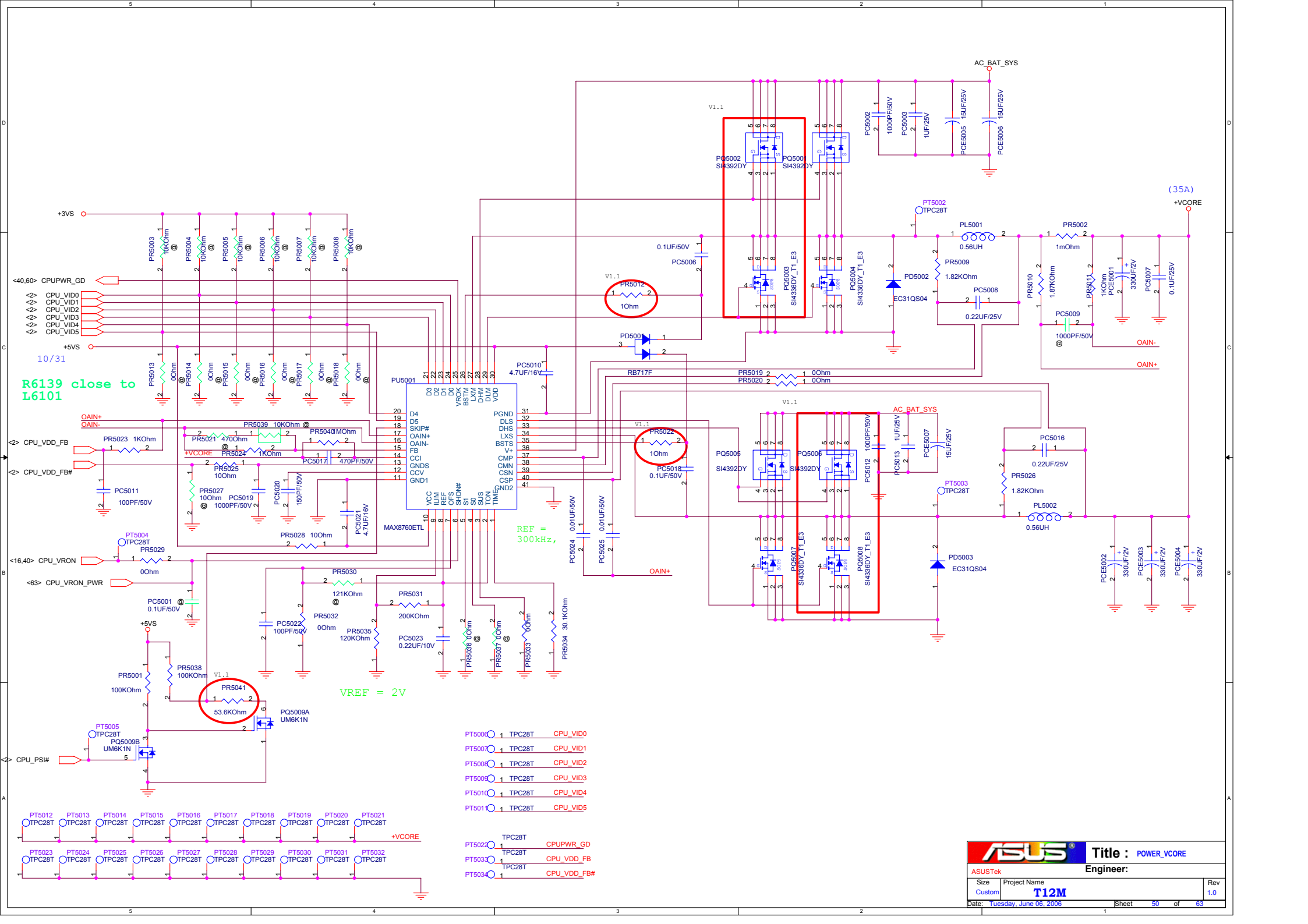
ASUSTek COMPUTER INC.	Title : N/A	
	Engineer: Sam_Wang	
Size: Custom	Project Name: F3M	Rev: 1.0
Date: Tuesday, June 06, 2006	Sheet 45 of 63	

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date:	Tuesday, June 06, 2006
Sheet	46 of 63

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date: Tuesday, June 06, 2006	Sheet 47 of 63

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date: Tuesday, June 06, 2006	Sheet 48 of 63

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date: Tuesday, June 06, 2006	Sheet 49 of 63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(35A)
+VCORE
+3VS
+5VS
<40,60> CPUPWR_GD
<2> CPU_VID0
<2> CPU_VID1
<2> CPU_VID2
<2> CPU_VID3
<2> CPU_VID4
<2> CPU_VID5
10/31
R6139 close to L6101
PU5001
MAX8760ETL
REF = 300kHz,
VREF = 2V
OAIN+
OAIN-
<2> CPU_VDD_FB
<2> CPU_VDD_FB#
<16,40> CPU_VRON
<63> CPU_VRON_PWR
<2> CPU_PSI#
PQ5002 SI4392DY
PQ5001 SI4392DY
PQ5005 SI4392DY
PQ5006 SI4392DY
PQ5003 SI4336DY_T1_E3
PQ5004 SI4336DY_T1_E3
PQ5007 SI4336DY_T1_E3
PQ5008 SI4336DY_T1_E3
PQ5009A UM6K1N
PQ5009B UM6K1N
PD5002 EC31QS04
PD5003 EC31QS04
PD5001 RB717F
PL5001 0.56UH
PL5002 0.56UH
PT5002 TPC28T
PT5003 TPC28T
PT5004 TPC28T
PT5005 TPC28T
PT5006 TPC28T CPU_VID0
PT5007 TPC28T CPU_VID1
PT5008 TPC28T CPU_VID2
PT5009 TPC28T CPU_VID3
PT5010 TPC28T CPU_VID4
PT5011 TPC28T CPU_VID5
PT5022 TPC28T CPUPWR_GD
PT5033 TPC28T CPU_VDD_FB
PT5034 TPC28T CPU_VDD_FB#
PT5012 PT5013 PT5014 PT5015 PT5016 PT5017 PT5018 PT5019 PT5020 PT5021 TPC28T
PT5023 PT5024 PT5025 PT5026 PT5027 PT5028 PT5029 PT5030 PT5031 PT5032 TPC28T
+VCORE
ASUS
Title : POWER_VCORE
ASUSTek
Engineer:
Size Custom
Project Name T12M
Rev 1.0
Date: Tuesday, June 06, 2006
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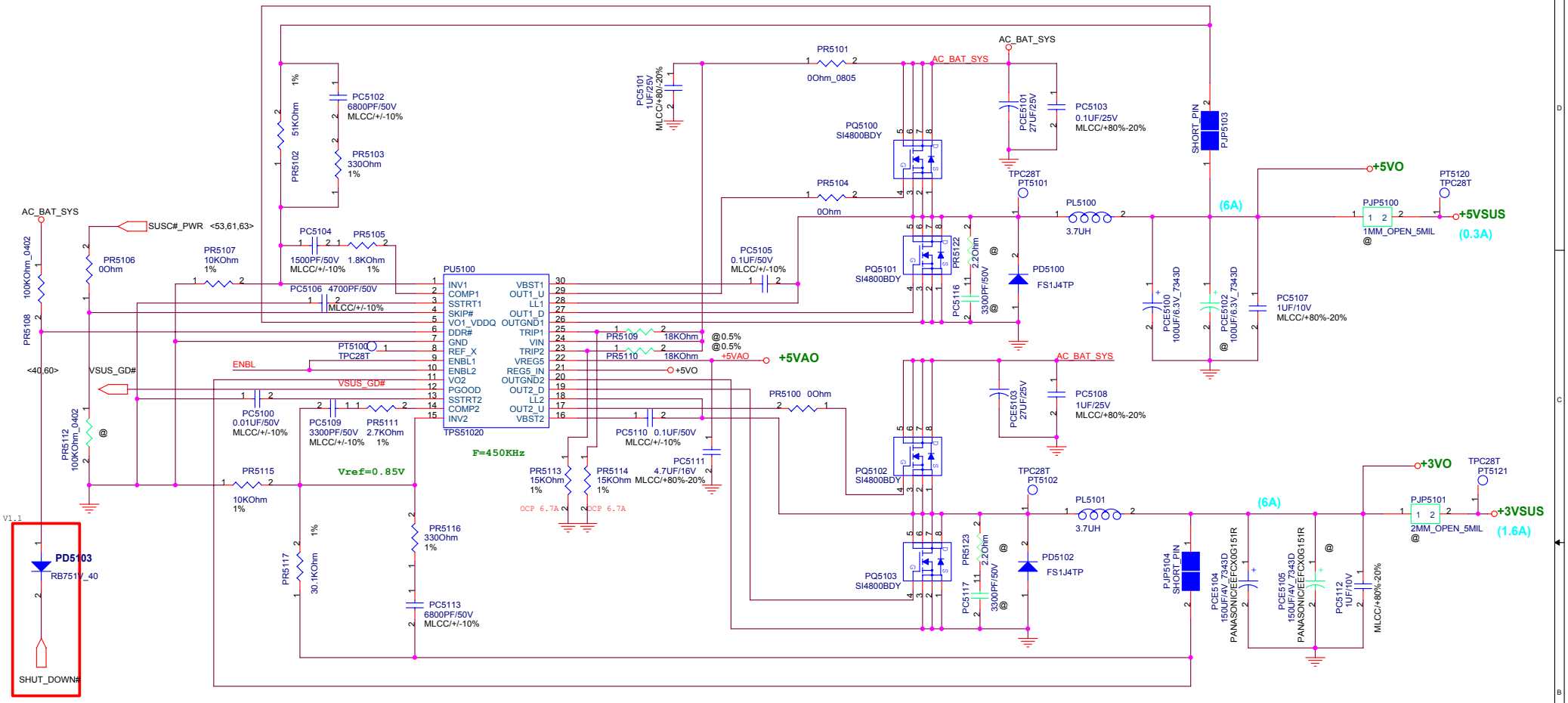
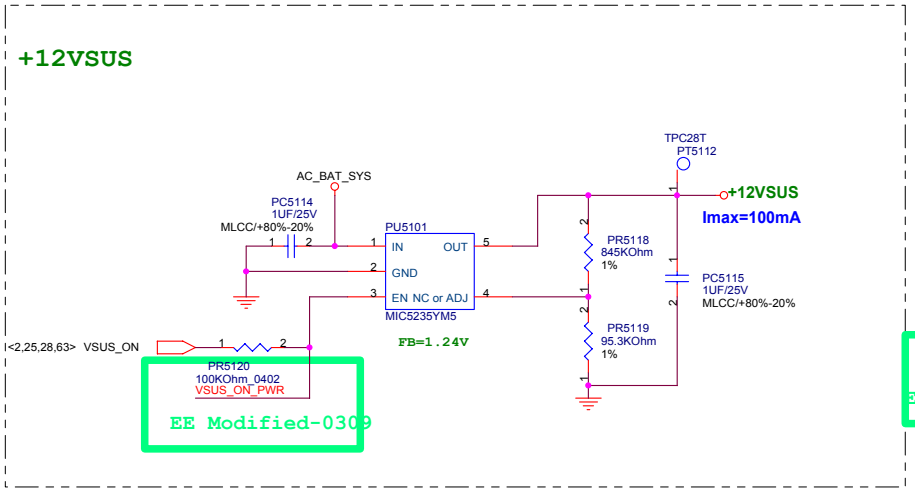
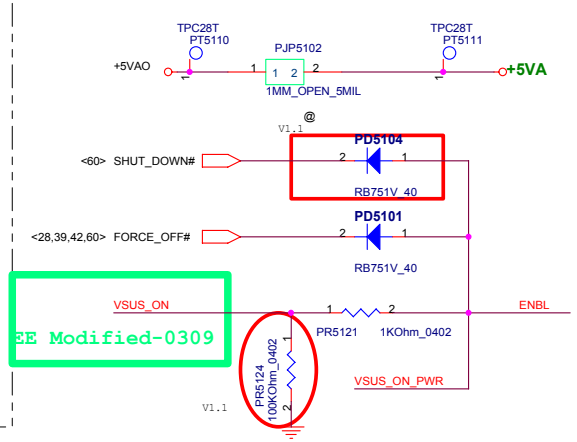
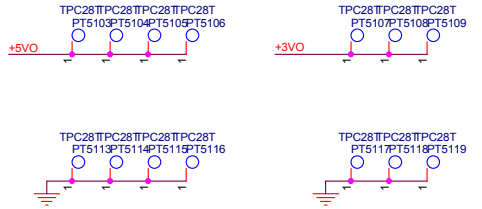








ASUS

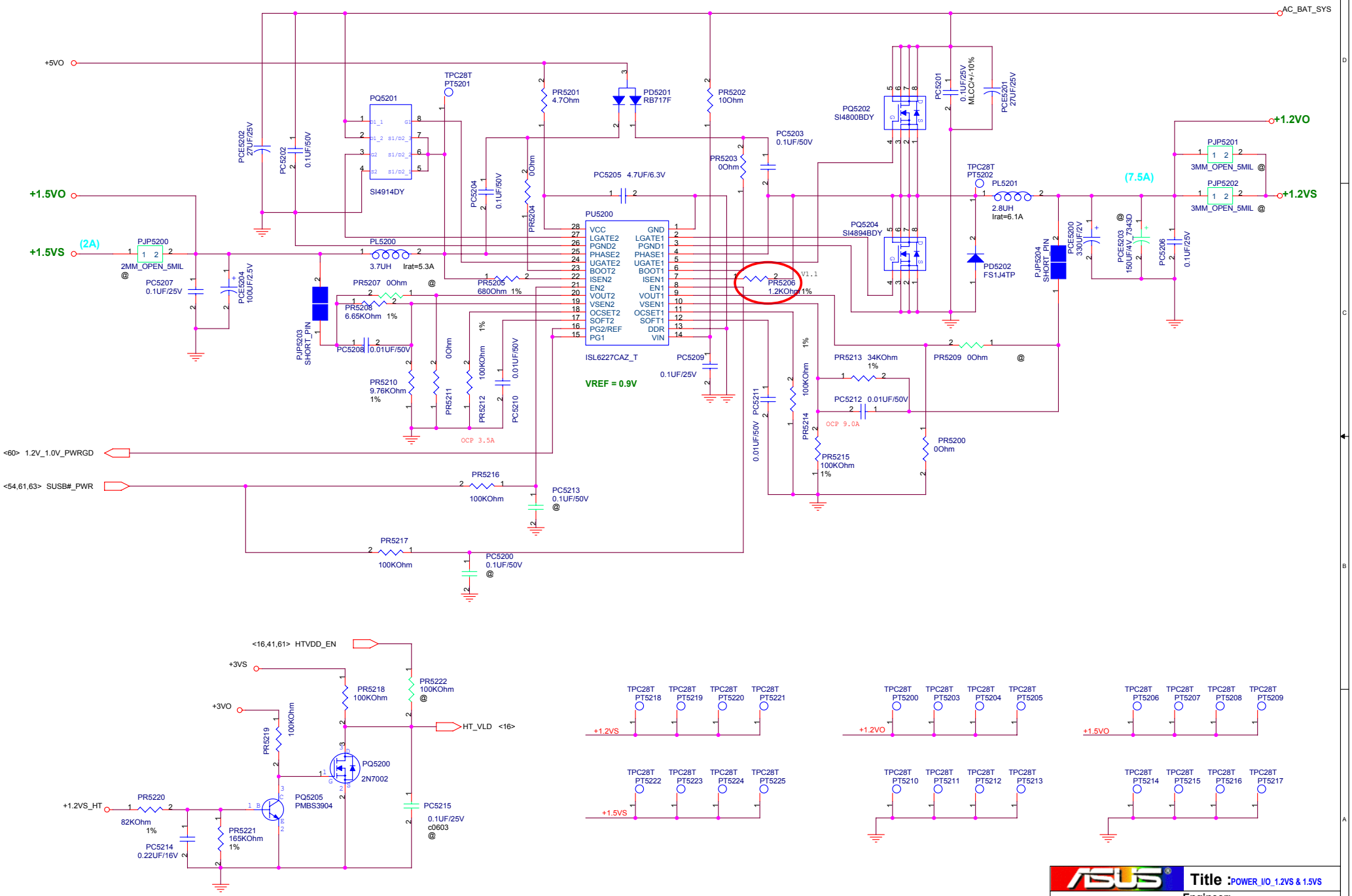
Title : POWER SYSTEM

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	T12M	1.0

Date: Tuesday, June 06, 2006 Sheet 51 of 63


AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
(2A)
PJP5200
2MM_OPEN_5MIL
@
PC5207
0.1UF/25V
PCE5204
100UF/2.5V
PCE5202
27UF/25V
PC5202
0.1UF/50V
PQ5201
SI4914DY
TPC28T
PT5201
PR5201
4.7Ohm
PD5201
RB717F
PR5202
10Ohm
PC5204
0.1UF/50V
PR5204
0Ohm
PC5205 4.7UF/6.3V
PR5203
0Ohm
PC5203
0.1UF/50V
PU5200
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
ISL6227CAZ_T
VREF = 0.9V
PL5200
3.7UH
Irat=5.3A
PR5205
680Ohm 1%
PR5206
1.2KOhm 1%
V1.1
PR5207 0Ohm @
PR5208
6.65KOhm 1%
PC5208 0.01UF/50V
PJP5203
SHORT_PIN
PR5210
9.76KOhm
1%
PR5211
0Ohm
PR5212
100KOhm
1%
PC5210
0.01UF/50V
OCP 3.5A
PC5209
0.1UF/25V
PQ5202
SI4800BDY
PC5201
0.1UF/25V
MLCC+/-10%
PCE5201
27UF/25V
PQ5204
SI4894BDY
TPC28T
PT5202
PL5201
2.8UH
Irat=6.1A
PD5202
FS1J4TP
PJP5204
SHORT_PIN
PCE5200
330UF/2V
PCE5203
150UF/4V_7343D
PC5206
0.1UF/25V
(7.5A)
@
PJP5201
3MM_OPEN_5MIL @
PJP5202
3MM_OPEN_5MIL @
+1.2VO
+1.2VS
PR5213 34KOhm
1%
PR5209 0Ohm @
PC5212 0.01UF/50V
OCP 9.0A
PC5211
0.01UF/50V
PR5214
100KOhm
1%
PR5215
100KOhm
1%
PR5200
0Ohm
<60> 1.2V_1.0V_PWRGD
<54,61,63> SUSB#_PWR
PR5216
100KOhm
PC5213
0.1UF/50V
@
PR5217
100KOhm
PC5200
0.1UF/50V
@
<16,41,61> HTVDD_EN
+3VS
+3VO
PR5218
100KOhm
PR5222
100KOhm
@
HT_VLD <16>
PR5219
100KOhm
PQ5200
2N7002
+1.2VS_HT
PR5220
82KOhm
1%
PQ5205
PMBS3904
PR5221
165KOhm
1%
PC5214
0.22UF/16V
PC5215
0.1UF/25V
c0603
@
TPC28T PT5218 TPC28T PT5219 TPC28T PT5220 TPC28T PT5221
+1.2VS
TPC28T PT5200 TPC28T PT5203 TPC28T PT5204 TPC28T PT5205
+1.2VO
TPC28T PT5206 TPC28T PT5207 TPC28T PT5208 TPC28T PT5209
+1.5VO
TPC28T PT5222 TPC28T PT5223 TPC28T PT5224 TPC28T PT5225
+1.5VS
TPC28T PT5210 TPC28T PT5211 TPC28T PT5212 TPC28T PT5213
TPC28T PT5214 TPC28T PT5215 TPC28T PT5216 TPC28T PT5217
Title :POWER_I/O_1.2VS & 1.5VS
<OrgName>
Engineer:
Size
Custom
Project Name
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Rev
1.0
Date: Tuesday, June 06, 2006
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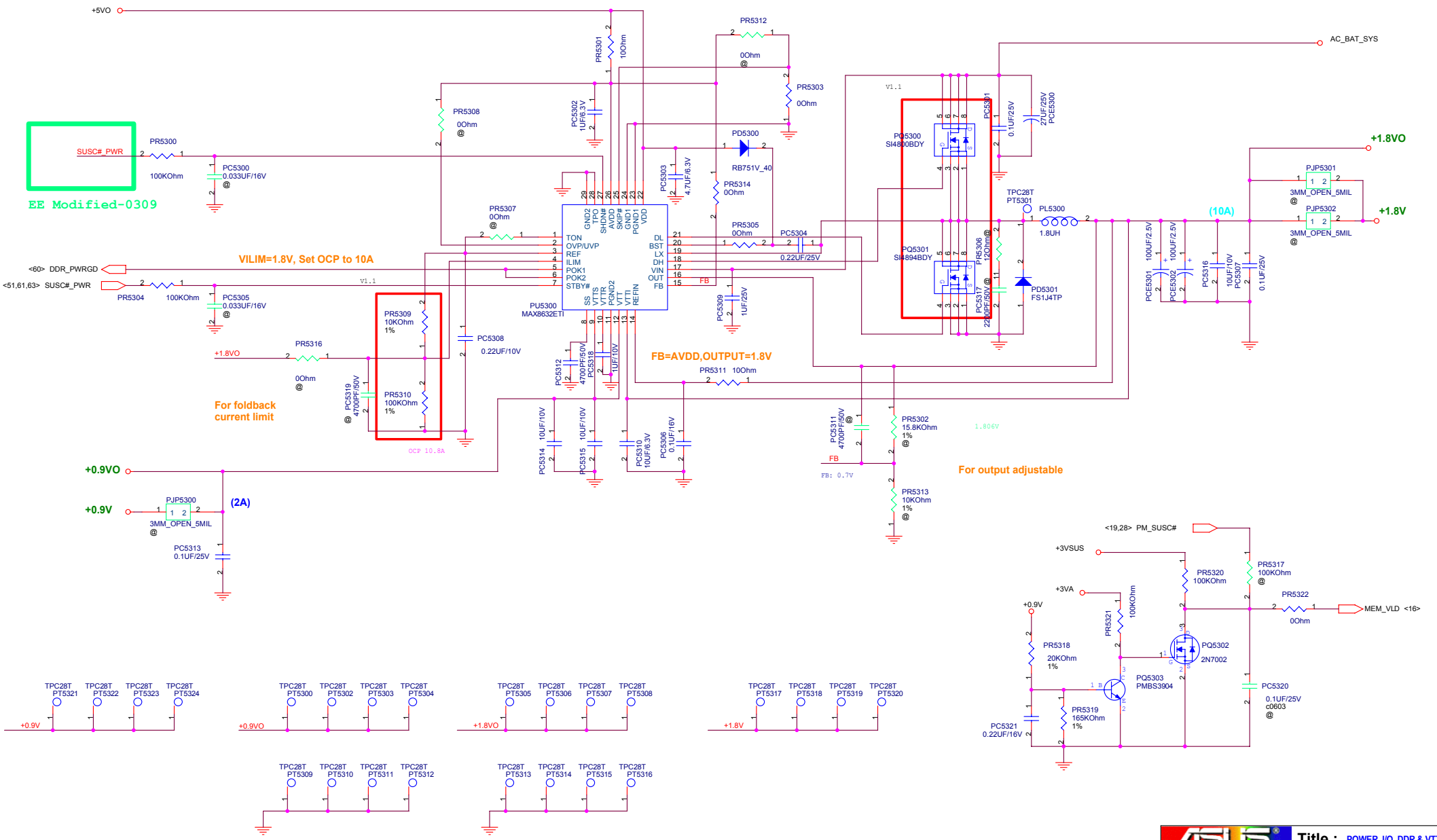
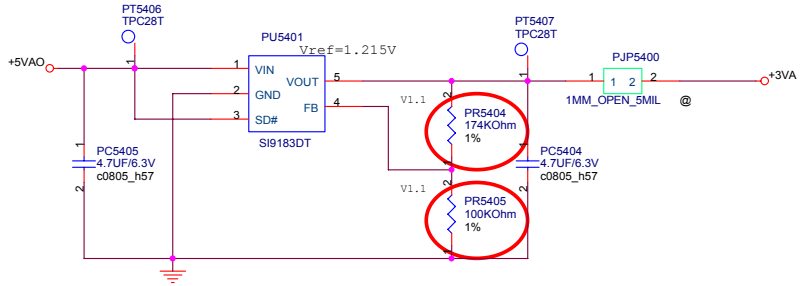
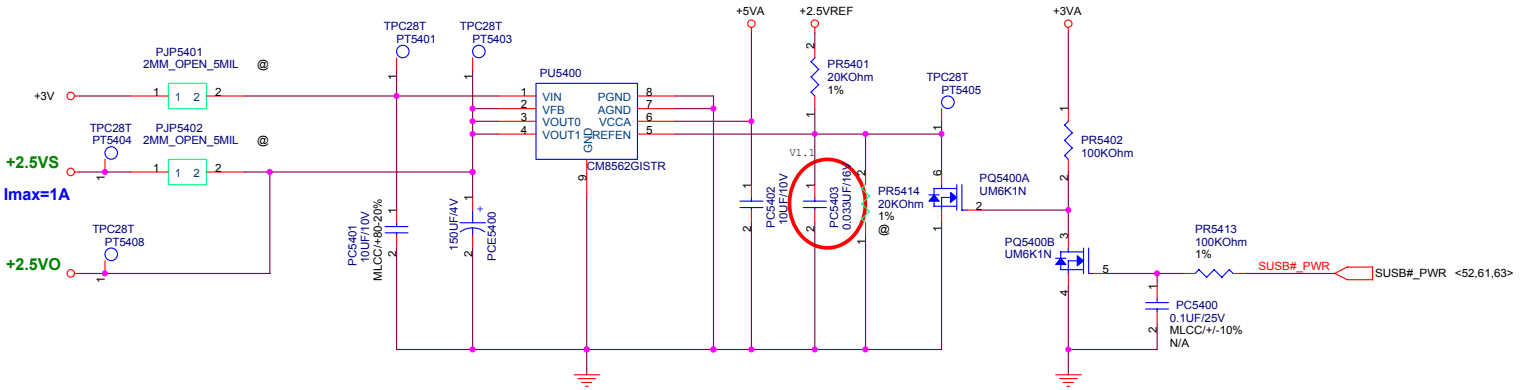


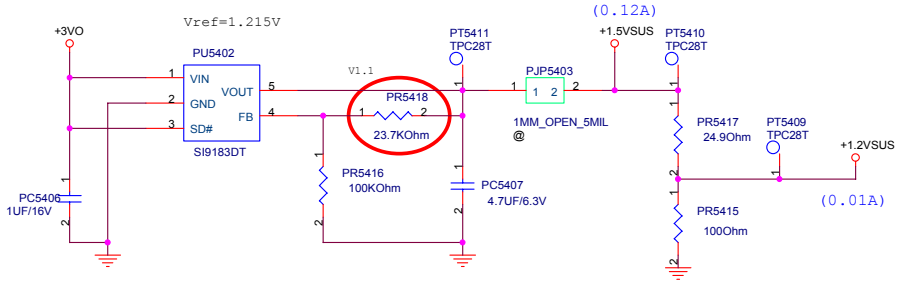
+3VAO



+2.5VS



+1.5VSUS&+1.2VSUS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12M	Rev: 1.0
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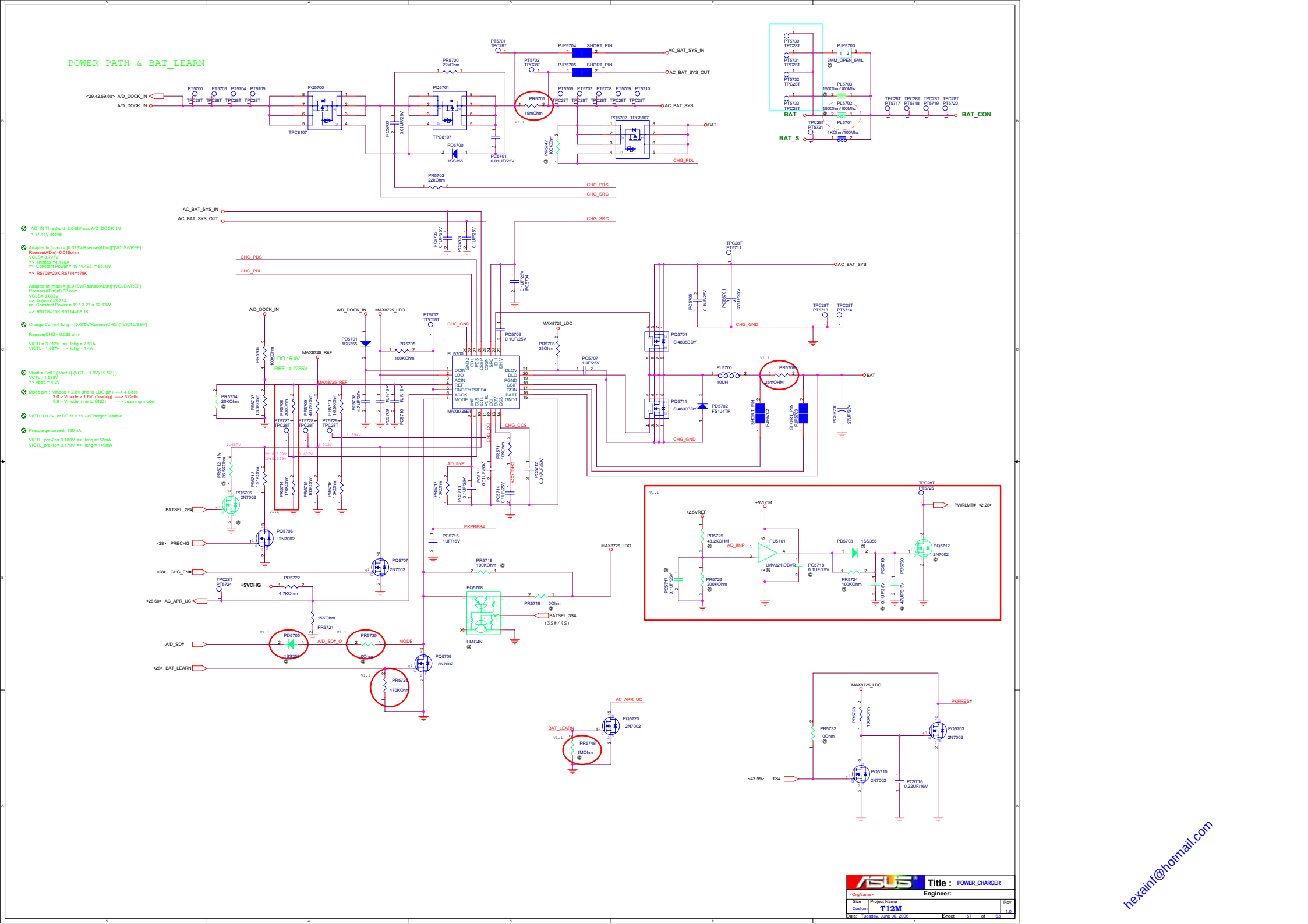
Size B	Document Number <Doc>
Rev	<RevCode>
Date: Tuesday, June 06, 2006	Sheet 55 of 63

Title	<Title>
Size B	Document Number <Doc>
Rev	<RevCode>
Date: Tuesday, June 06, 2006	Sheet 56 of 63


POWER PATH & BAT_LEARN
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
= 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.015ohm
VCLS= 3.797V
=> Iin(max)=4.495A
=> Constant Power = 19 *4.495 = 85.4W
=> R5708=20K,R5714=178K
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R5708=10K,R5714=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.012V => Ichg = 2.51A
VICTL= 1.687V => Ichg = 1.4A
Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
VICTL_pre-2p= 0.188V => Ichg =157mA
VICTL_pre-1p= 0.179V => Ichg = 149mA
A/D_DOCK_IN
AC_BAT_SYS_IN
AC_BAT_SYS_OUT
AC_BAT_SYS
BAT
BAT_S
BAT_CON
CHG_PDS
CHG_PDL
CHG_SRC
CHG_GND
CHG_CCS
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
PKPRES#
AD_IINP
BATSEL_2S#
BATSEL_3S#
(3S#/4S)
PRECHG
CHG_EN#
AC_APR_UC
+5VCHG
A/D_SD#
BAT_LEARN
MODE
TS#
PWRLMT# <2,28>
+2.5VREF
+5VLCM
Title : POWER_CHARGER
Engineer:
Project Name T12M
Rev 1.0
Date: Tuesday, June 06, 2006
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hexainf@hotmail.com

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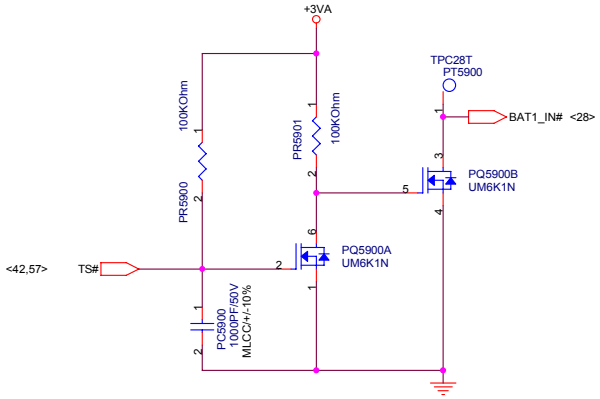
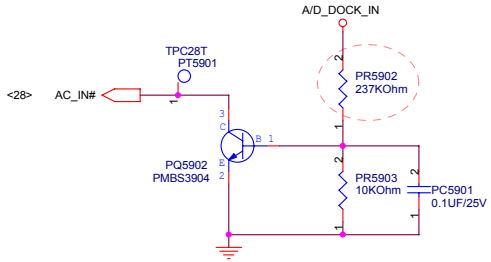
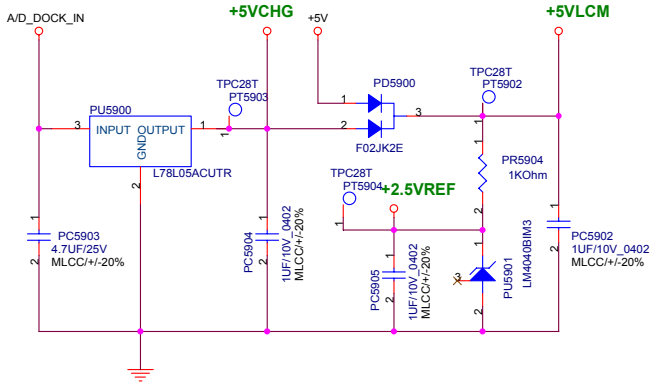
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER DETECT	
<OrgName>	Engineer:	
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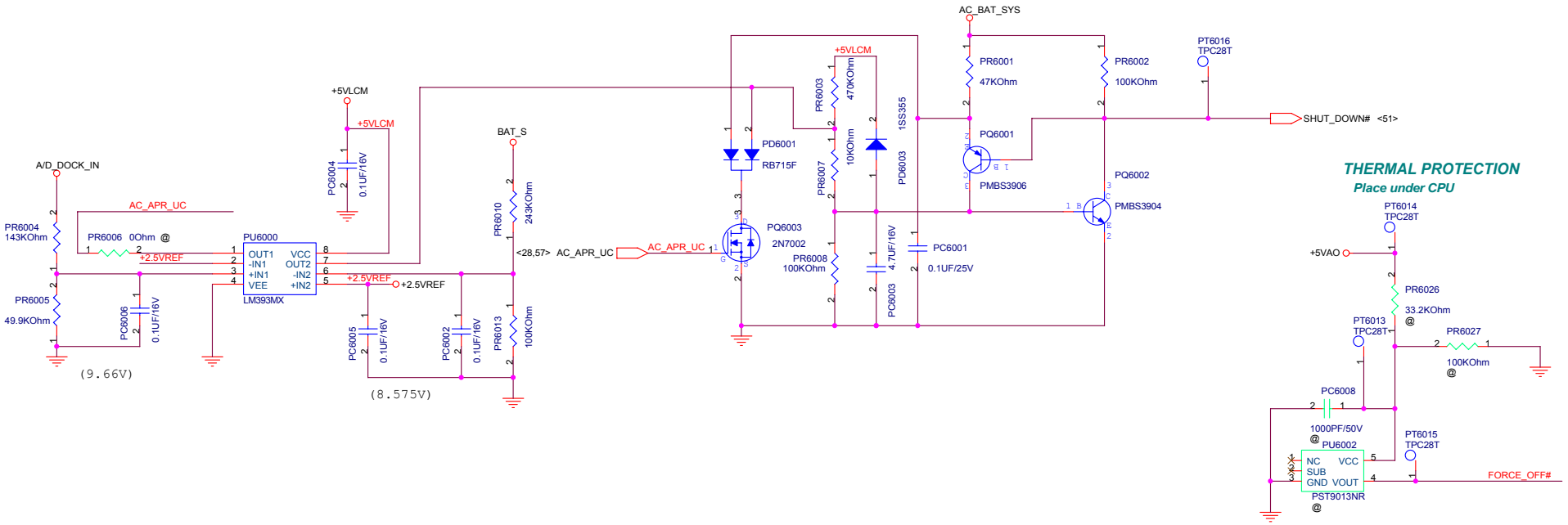
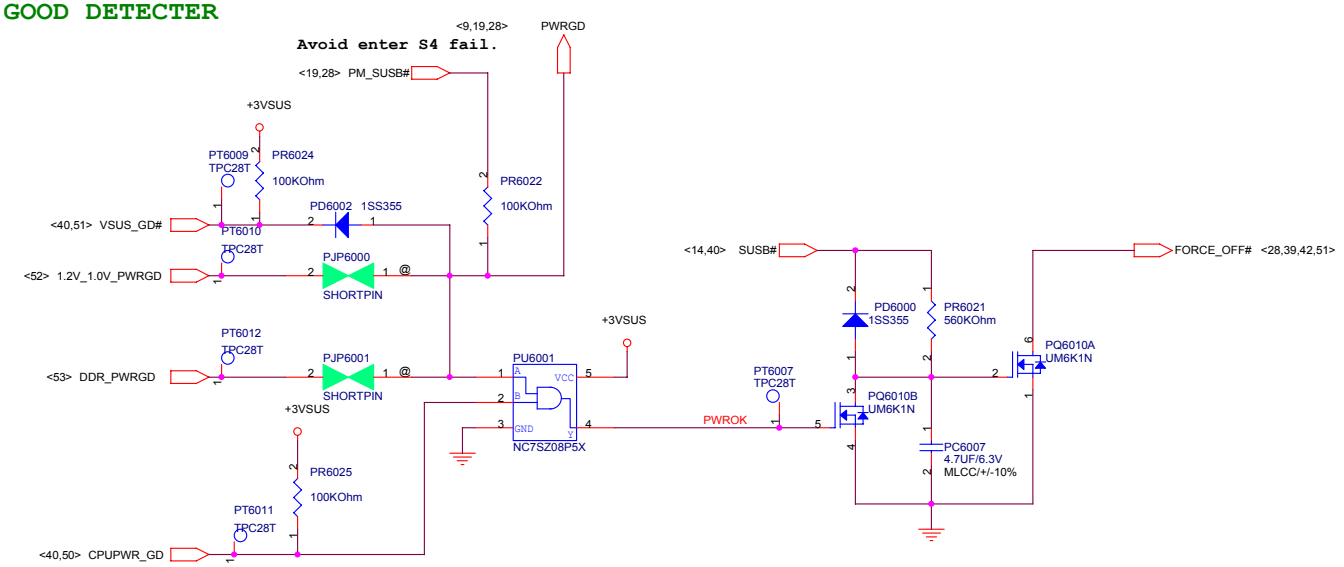
BATTERY ShutDown

V1.1

(H/W Battery low shutdown is 8.6V)



POWER GOOD DETECTER



ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12M	Rev: 1.0
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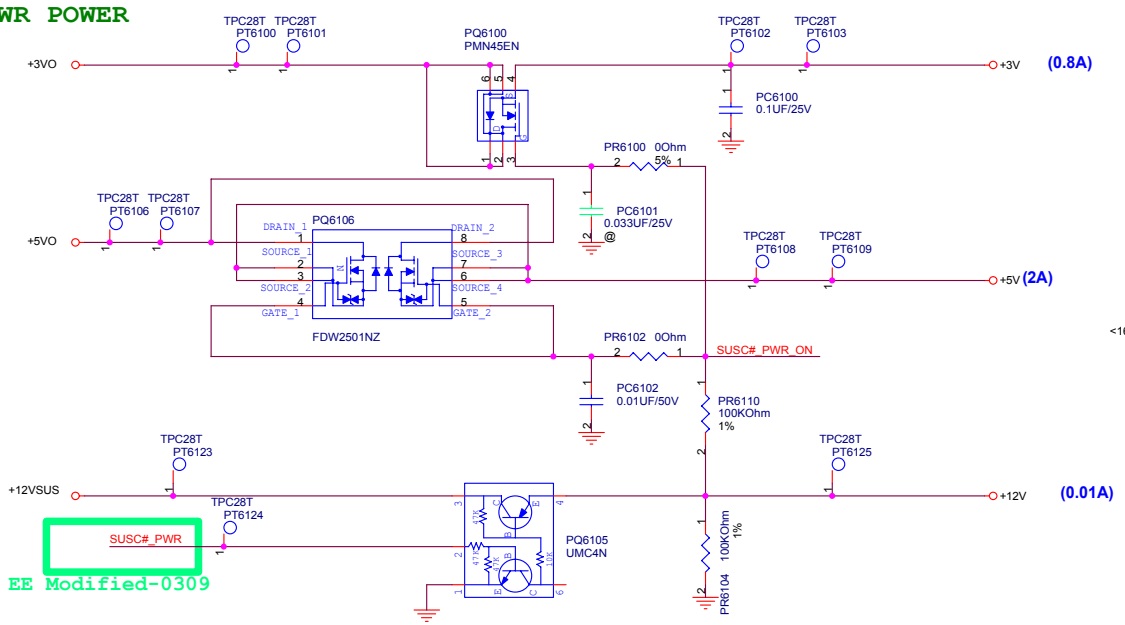
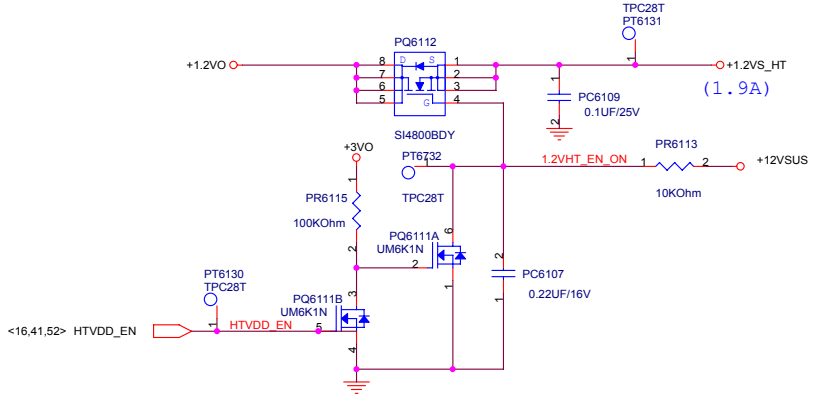
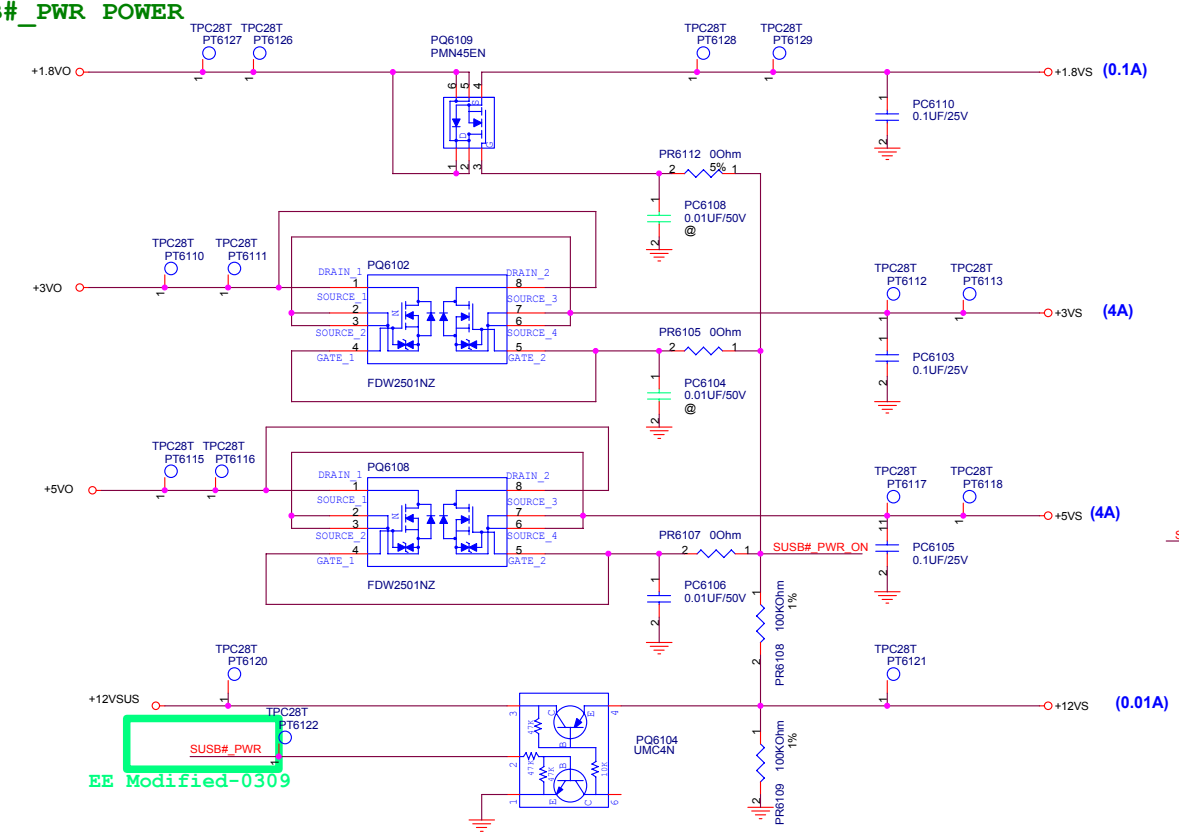
SUSC#_PWR POWER



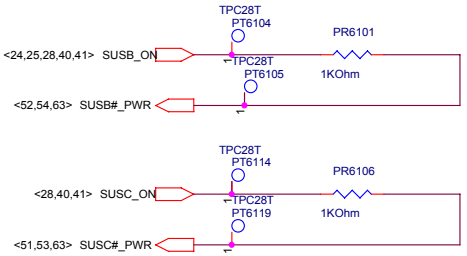
EE Modified-0309

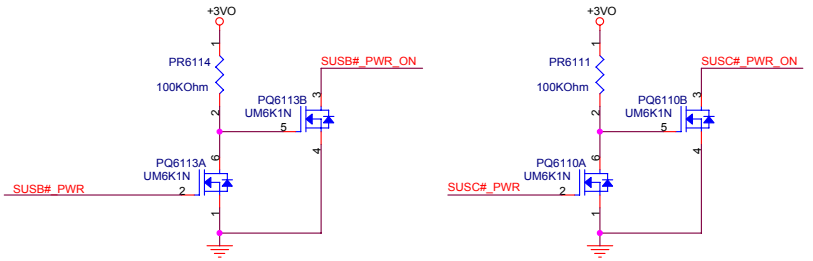


SUSB#_PWR POWER



EE Modified-0309





ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12M	Rev: 1.0
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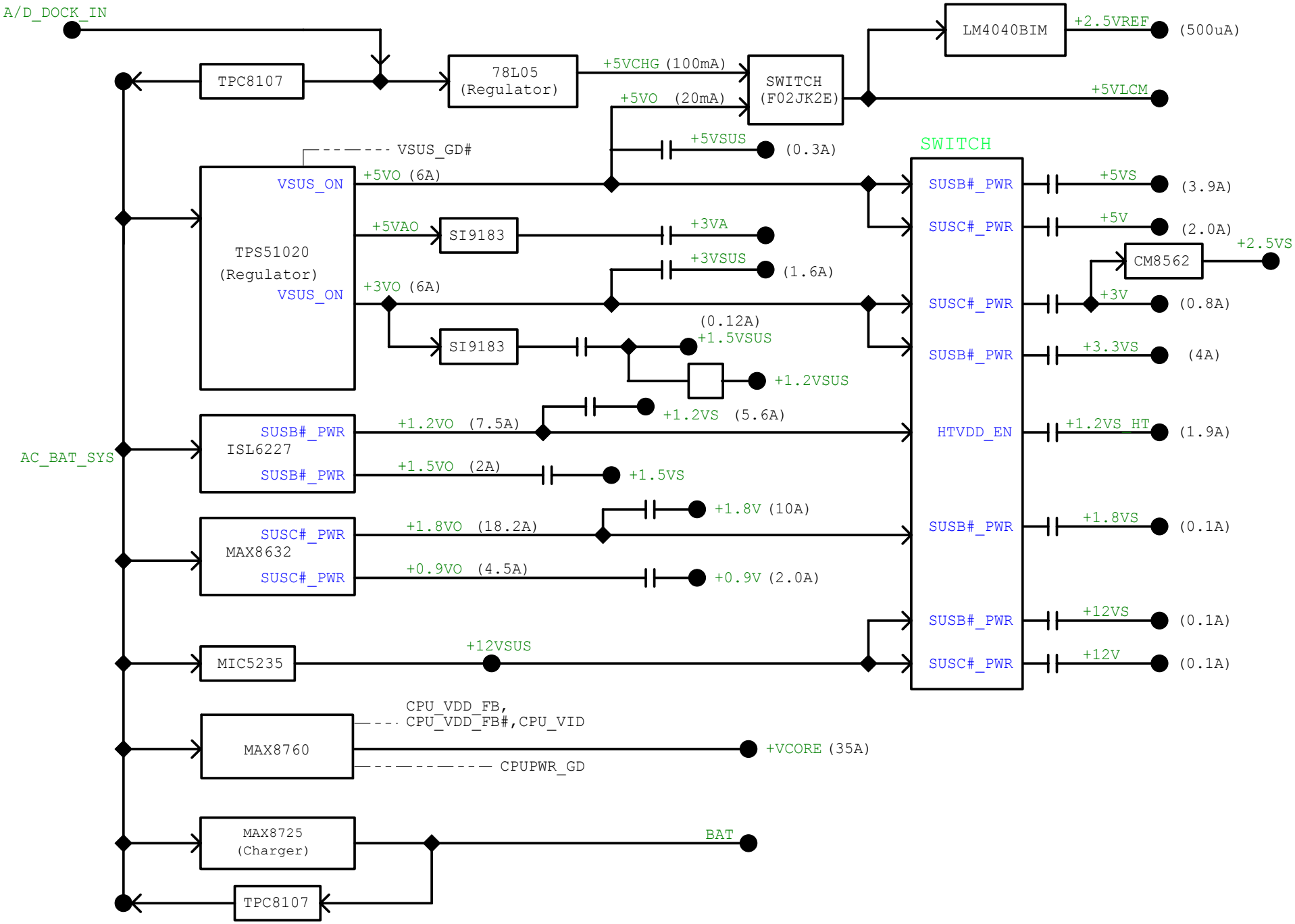

ASUS	Title : POWER_FLOWCHART	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12M	Rev: 1.0
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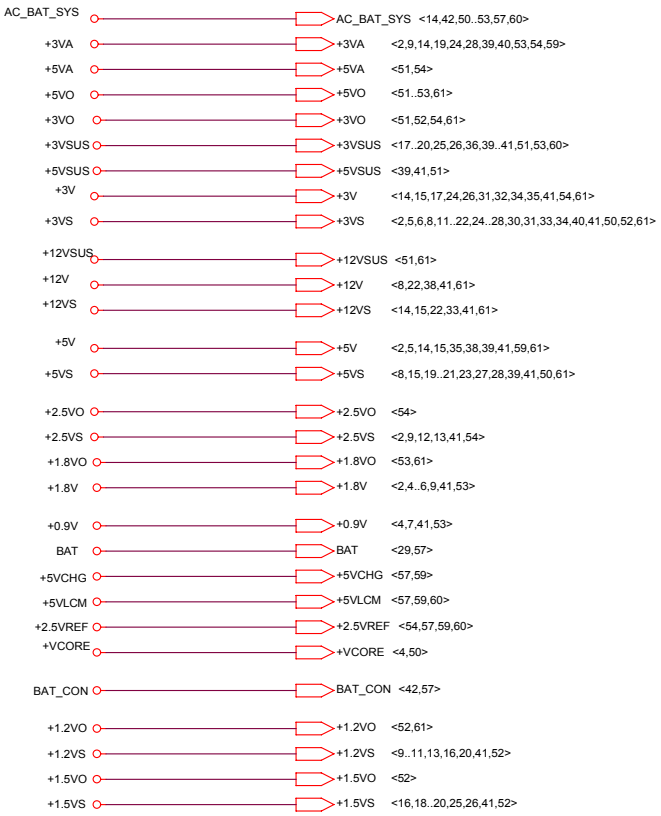
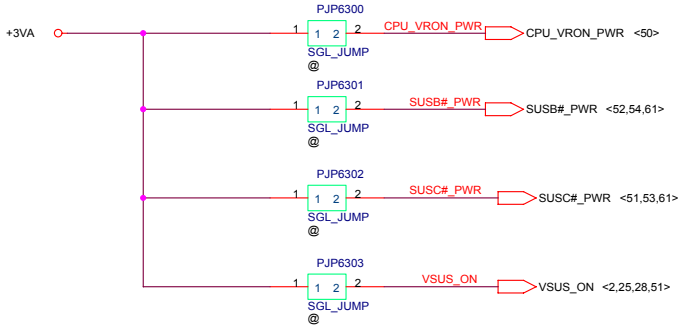


FOR POWER TEST



ASUS	Title : POWER SIGNAL	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12M	Rev: 1.0
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