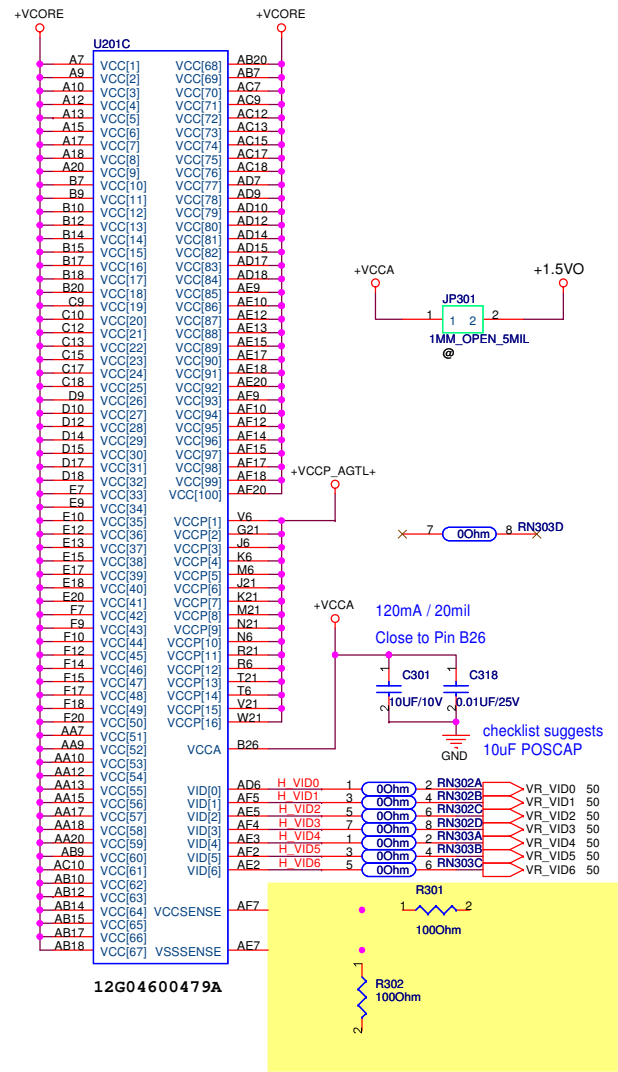


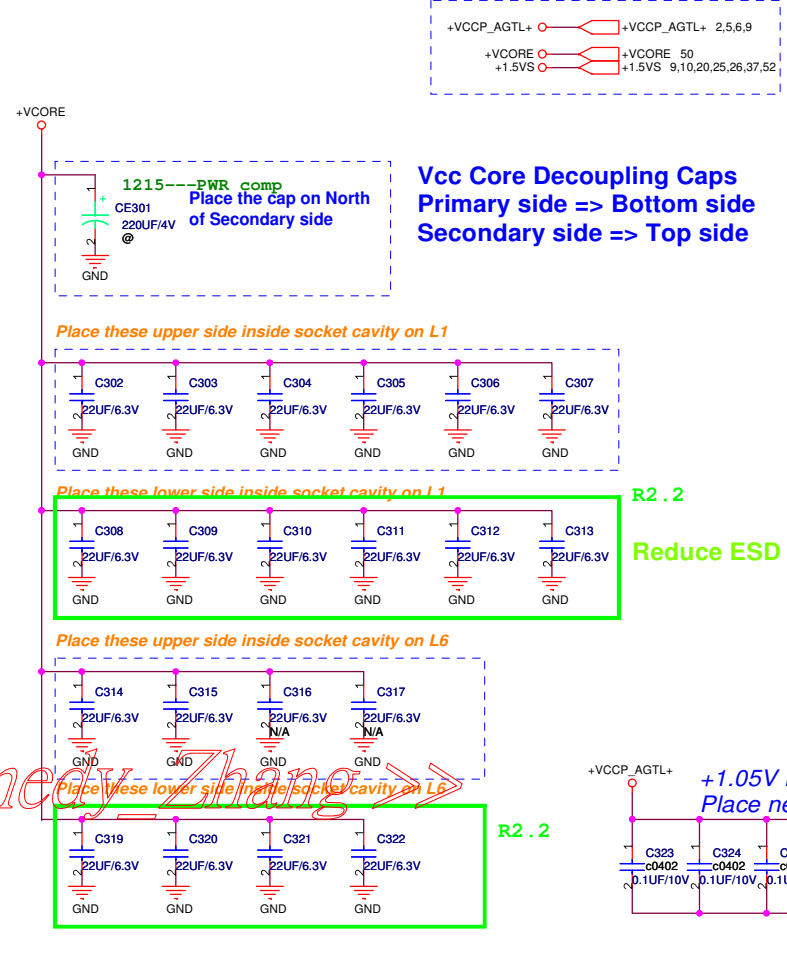
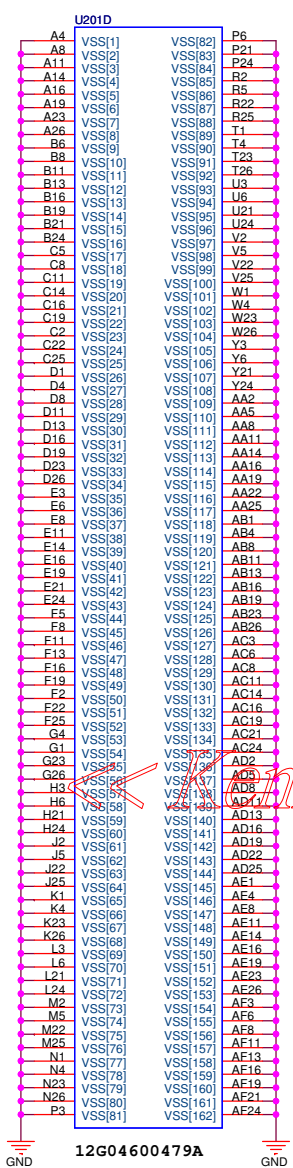


YUNAH FSB667	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

YUNAH FSB667	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
Min		Typ	Max
ICCP			2.5A



Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

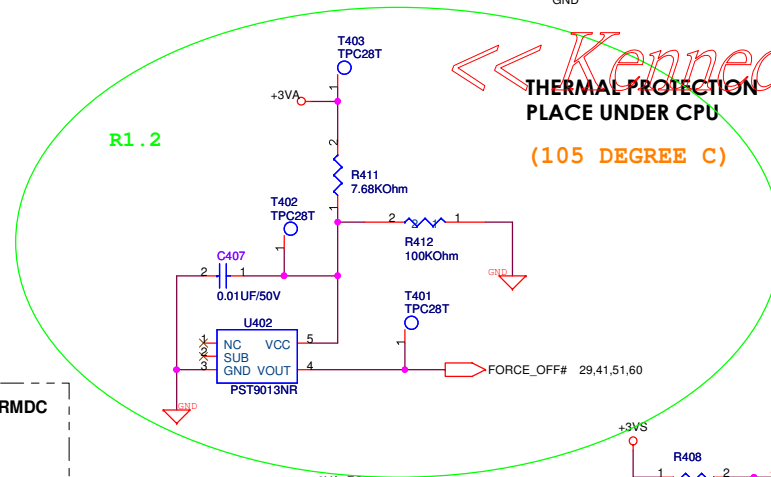
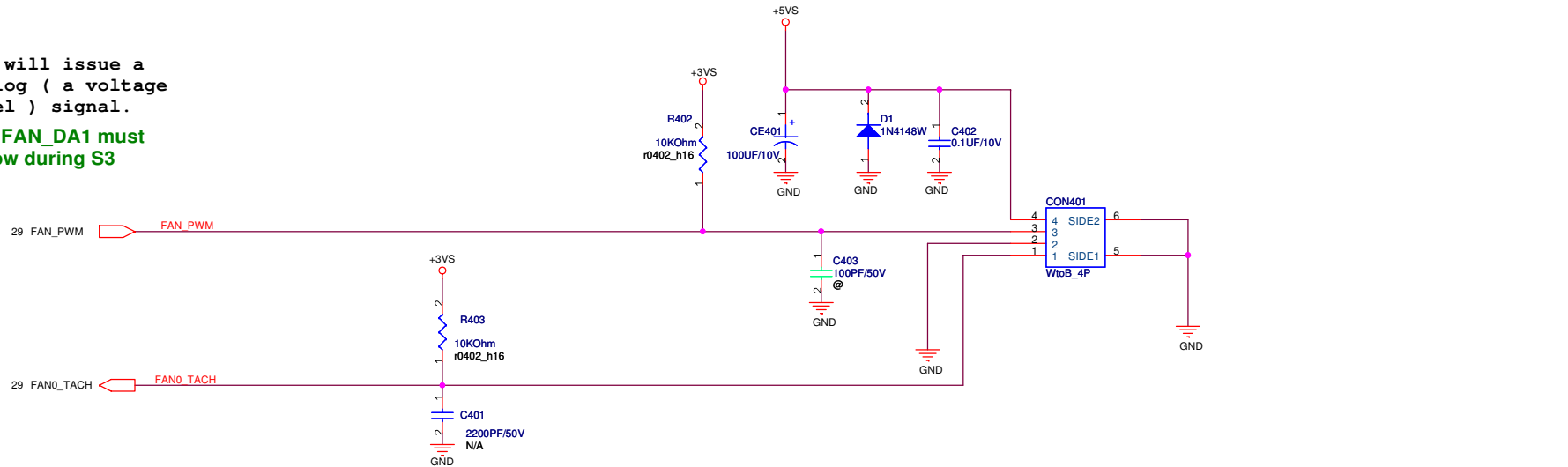


Fan Speed Control

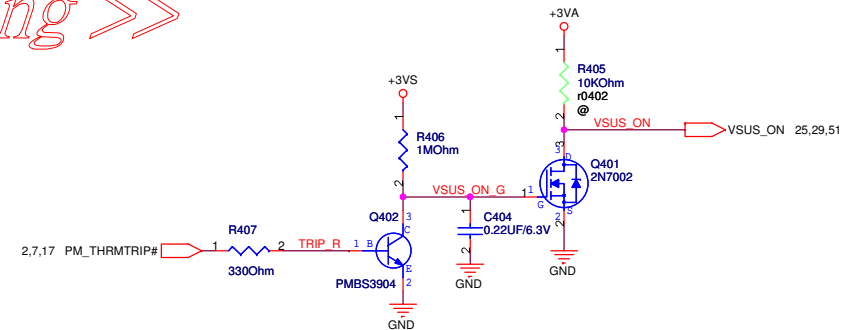
+5VS 13,19,20,21,22,28,29,30,37,38,50,61
 +3VS 5,7,9,11,12,13,14,15,19,20,21,22,23,25,26,27,28,29,30,31,32,33,37,39,40,42,43,50,52,60,61
 +3VA 12,20,22,29,37,38,40,54,59,63

KBC will issue a
 analog (a voltage
 level) signal.

SW: FAN_DA1 must
 be low during S3

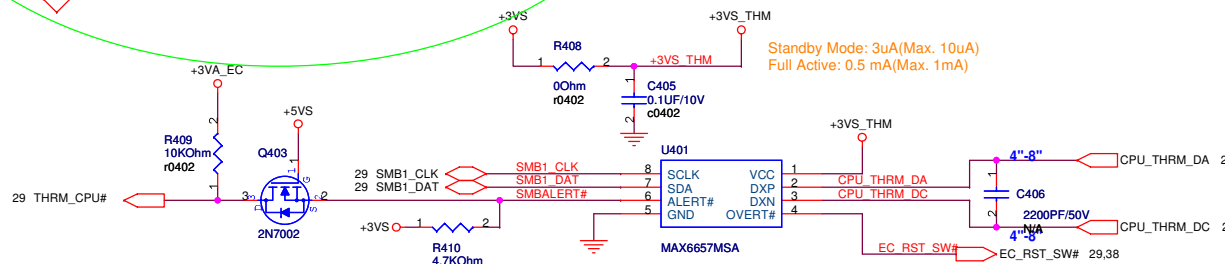


<< Kennedy_Zhang >>
 THERMAL PROTECTION
 PLACE UNDER CPU
 (105 DEGREE C)



Route H_THERMDA and H_THERMDC
 on the same layer

-----OTHER SIGNALS
 12 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 12 mils
 -----OTHER SIGNALS
 Avoid BPSB,Power

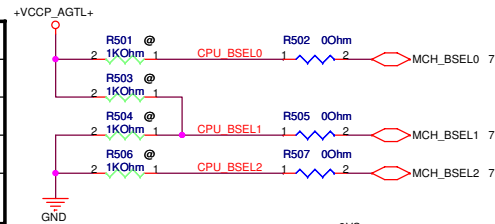


Standby Mode: 3uA(Max. 10uA)
 Full Active: 0.5 mA(Max. 1mA)

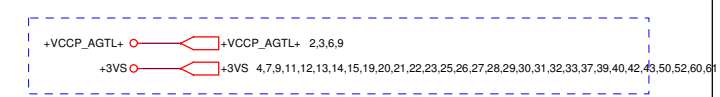
<Variant Name>

ASUS		Title : THER-SENSOR,FAN	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
A3	T12F		
Date: 星期五, 五月 15, 2007	Sheet 4	of 61	

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)	CLK_MCH_3GPLL(#)

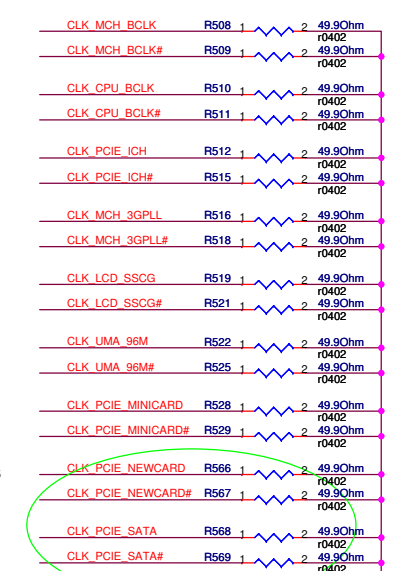


Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



Layout Note:
Place termination close to source IC

R2.0



R1.1

FREQ#1
0=PCIE_X 6/0 Not Controlled
1=PCIE_X 6/0 Controlled

FREQ#2
0=PCIE_X 8/1 Not Controlled
1=PCIE_X 8/1 Controlled

FREQ#3
0=PCIE_X 4/2 Not Controlled
1=PCIE_X 4/2 Controlled

FREQ#4
0=PCIE_X 7/5/3 Not Controlled
1=PCIE_X 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17, pin18=LCDCLK(96MHz) or
27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17, pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40, pin41=PREQ1#, PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519, Remove R550 R534

Internal Pull-Up Resistor

2 H_D#[0..63]

H_A#[31..3] 2

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING

5 CLK_MCH_BCLK	AG2	CLK_MCH_BCLK
5 CLK_MCH_BCLK#	AG1	CLK_MCH_BCLK#

CALISTOGA_Q137

HOST

H_A#_3	H9	H_A#3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	F9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	H13	H_A#14
H_A#_15	J15	H_A#15
H_A#_16	F14	H_A#16
H_A#_17	D12	H_A#17
H_A#_18	A11	H_A#18
H_A#_19	C11	H_A#19
H_A#_20	A12	H_A#20
H_A#_21	A13	H_A#21
H_A#_22	E13	H_A#22
H_A#_23	G13	H_A#23
H_A#_24	F12	H_A#24
H_A#_25	B12	H_A#25
H_A#_26	C14	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31	C14	H_A#31

H_ADS#	E8	H_ADS#
H_ADSTB#0	B9	H_ADSTB#0
H_ADSTB#1	C13	H_ADSTB#1
H_VREF	J13	H_VREF
H_BNR#	C6	H_BNR#
H_BPRI#	F6	H_BPRI#
H_BREQ#	G7	H_BREQ#
H_CPUREST#	B7	H_CPUREST#
H_DBUSY#	A7	H_DBUSY#
H_DEFER#	C3	H_DEFER#
H_DPWR#	J9	H_DPWR#
H_DRDY#	H8	H_DRDY#
H_DVREF	K13	H_DVREF

H_DINV#_0	J7	H_DINV#0
H_DINV#_1	W8	H_DINV#1
H_DINV#_2	U3	H_DINV#2
H_DINV#_3	AB10	H_DINV#3

H_DSTBN#0	K4	H_DSTBN#0
H_DSTBN#1	L7	H_DSTBN#1
H_DSTBN#2	Y5	H_DSTBN#2
H_DSTBN#3	AC4	H_DSTBN#3

H_DSTBP#0	K3	H_DSTBP#0
H_DSTBP#1	T6	H_DSTBP#1
H_DSTBP#2	AA5	H_DSTBP#2
H_DSTBP#3	AC5	H_DSTBP#3

H_HIT#	D3	H_HIT#
H_HITM#	D4	H_HITM#
H_LOCK#	B3	H_LOCK#

H_REQ#_0	D8	H_REQ#0
H_REQ#_1	G8	H_REQ#1
H_REQ#_2	B8	H_REQ#2
H_REQ#_3	F8	H_REQ#3
H_REQ#_4	A8	H_REQ#4

H_RS#_0	B4	H_RS#0
H_RS#_1	E6	H_RS#1
H_RS#_2	D6	H_RS#2

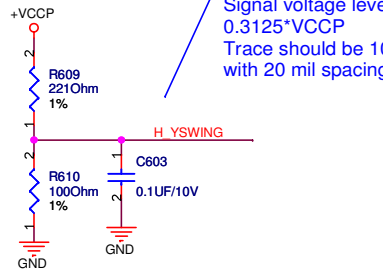
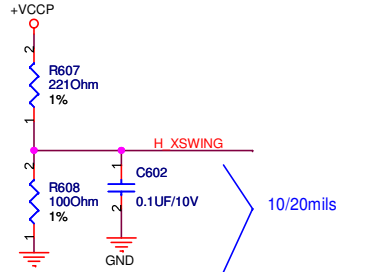
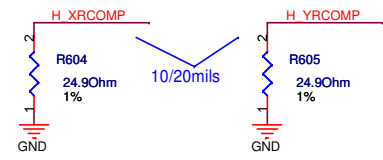
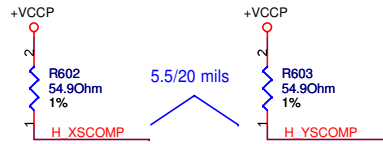
H_CPUSLP#	E3	H_CPUSLP#
H_TRDY#	E7	H_TRDY#

+VCCP_AGTL+
R601 100Ohm 1%
R606 200Ohm 1%
C601 0.1UF/10V

Layout Note:
0.1uF should be placed 100mils or less from GND pin.

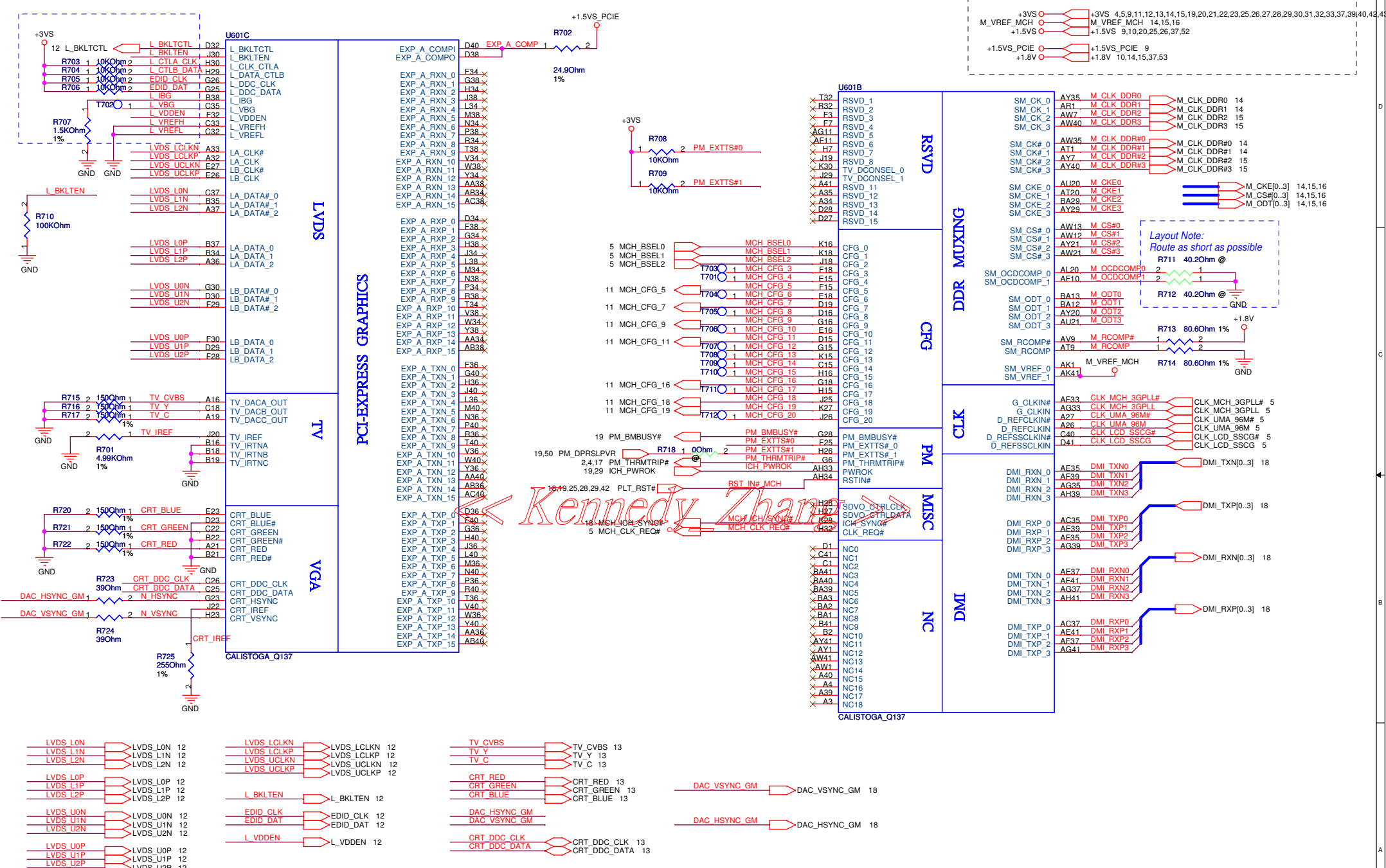
<< Kennedy Zhang >>

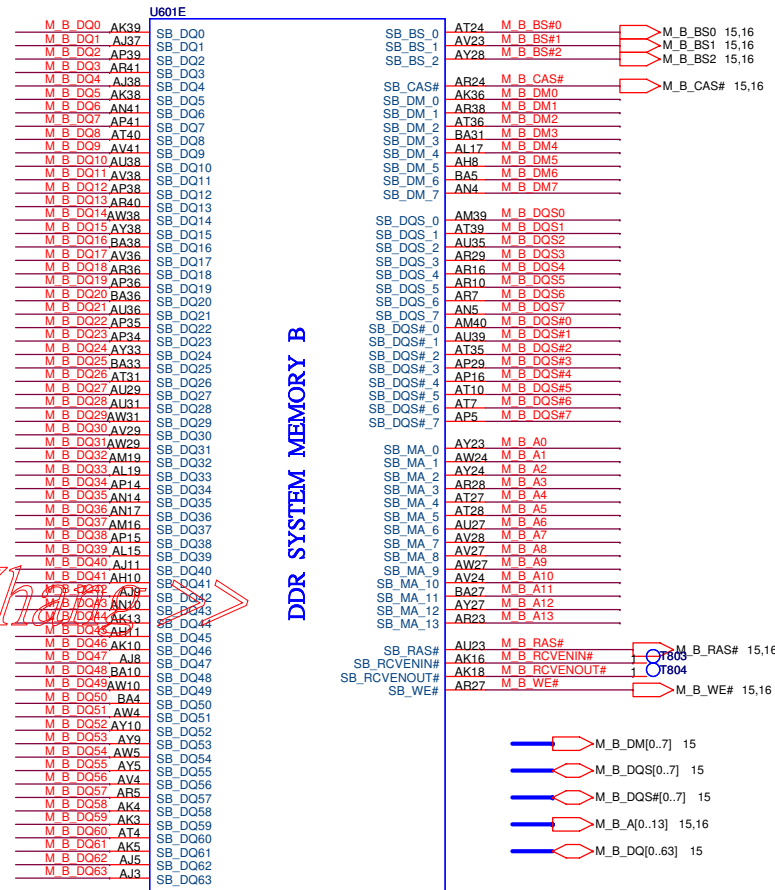
+VCCP 2,9,20,52
+VCCP_AGTL+ 2,3,5,9



Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing

ASUS		Title : Calistoga MCH (1)	
ASUSTek COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
B	T12F		
Date: 星期五, 五月 25, 2007	Sheet 6 of 61		





1.5VS

close to GMCH

Layout Note:
Caps should be on Top layer

120Ohm/100Mhz

L902

30Ohm/100Mhz

L901

80Ohm/100Mhz

L903

30Ohm/100Mhz

L904

30Ohm/100Mhz

L906

30Ohm/100Mhz

L907

120Ohm/100Mhz

L908

CE902
150UF/4V

CE903
470UF/2.5V

CE904 @

CE905 @

C902
10UF/10V

C903
10UF/10V

C904
0.1UF/10V

C905
10UF/10V

C909
0.1UF/10V

C912
0.1UF/10V

C918
0.1UF/10V

C923
22UF/6.3V

C924
0.1UF/10V

C927
22UF/6.3V

C928
0.1UF/10V

VCC3G

VCCA_3GPLL

VCCAUX
1900 mA

VCCA_DPLL A

VCCA_DPLL B

VCCA_HPLL
45 mA

VCCA_MPLL
45 mA

1500 mA

1.5VS_VCCAUX

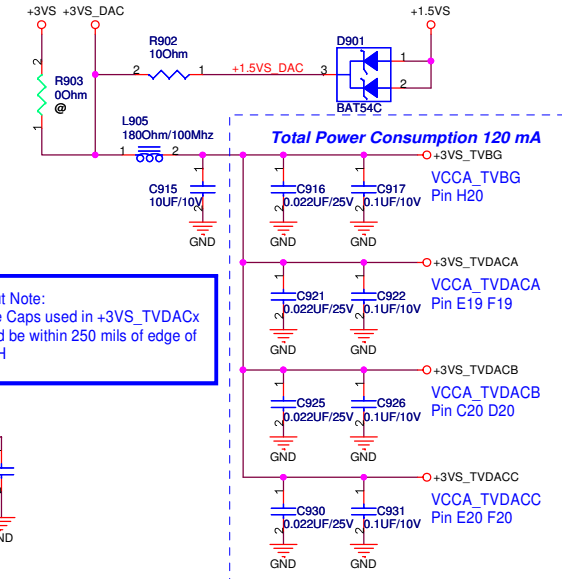
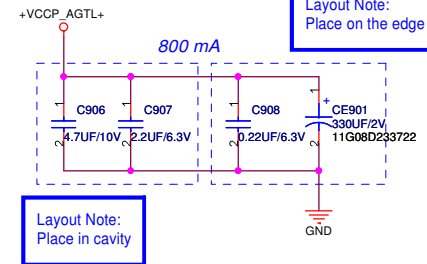
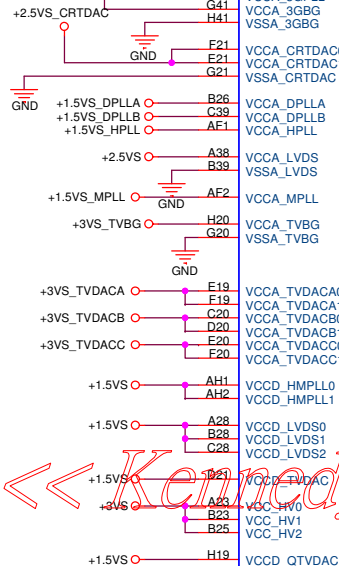
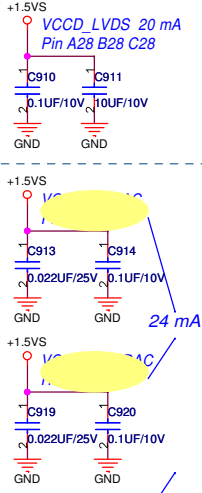
1.5VS_DPLLA

1.5VS_DPLLB

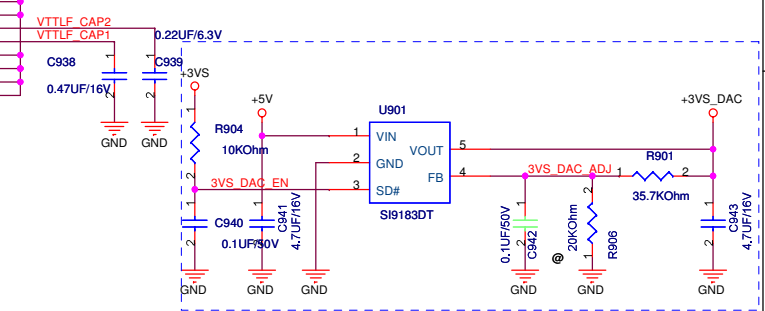
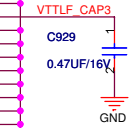
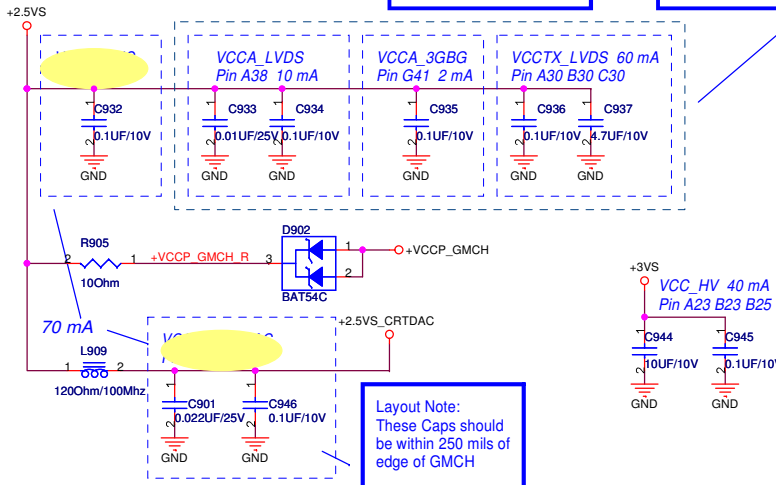
1.5VS_HPLL

1.5VS_MPLL

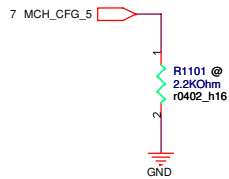
Layout Note:
0.1uF caps in 1



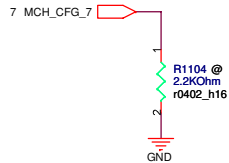
Layout Note:
These Caps used in +3VS_TVDACx
should be within 250 mils of edge of
GMCH



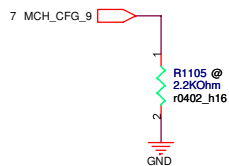
NOTE: 0.1UF CAPS USED IN +1.5VS,
+3.3VS
+2.5VS should be placed within
200 mils of edge.



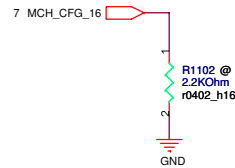
CFG5 : DMI X2 Select
 LOW = DMI X 2
HIGH = DMI X 4 (Default)



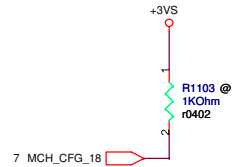
CFG7 : CPU STRAP
 LOW = Reserved
HIGH = Mobility CPU (Default)



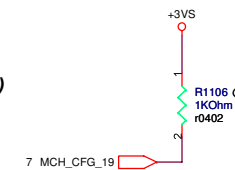
CFG9 : PCIE GRAPHIC LANE
 LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



CFG16 : FSB DYNAMIC ODT
 LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

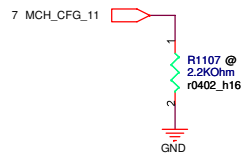


CFG18 : GMCH Core Voltage Level
 LOW = 1.05V
HIGH = 1.5V (default)

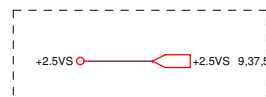


CFG19 : DMI LANE REVERSAL
 LOW = NORMAL
 HIGH = LANES REVERSED

<< Kennedy_Zhang >>



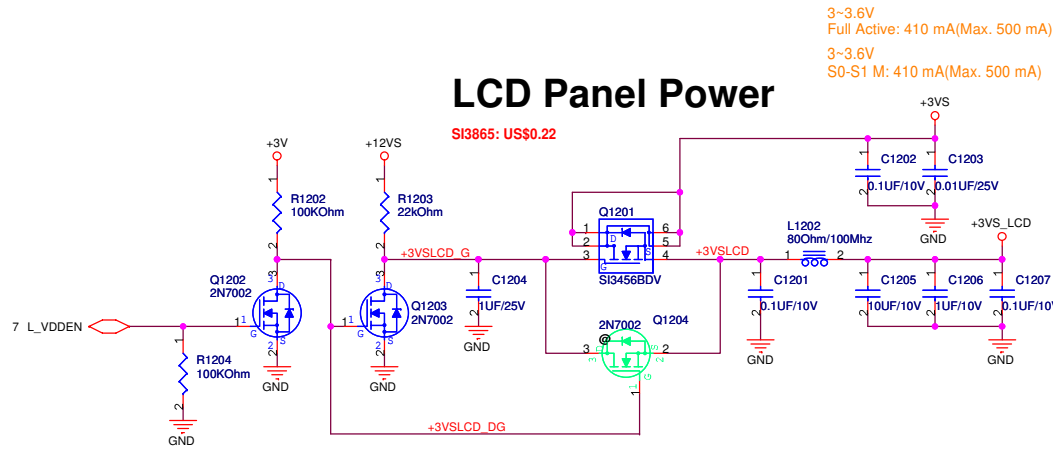
CFG11 : Reserved but need to be pull low



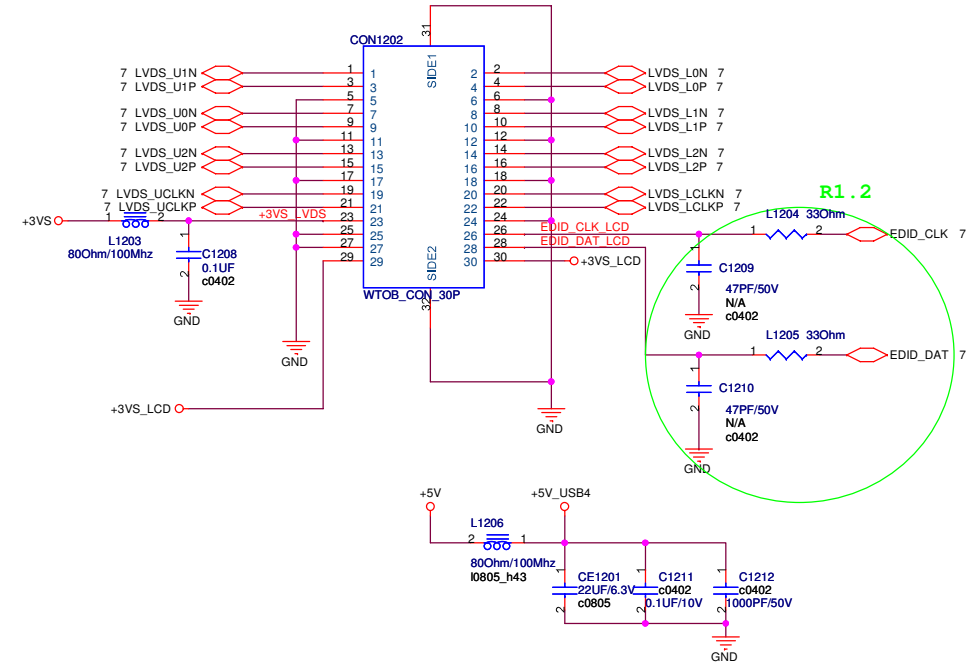
CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.

CFG All are sampled with respect to the leading edge of the GMCH PWROK		
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane	0 = Reverse Lanes 1 = Normal (Default)
11:10	Reversal	
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_C		
TRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

LCD Panel Power



LCD LVDS Interface



LCD Backlight Control

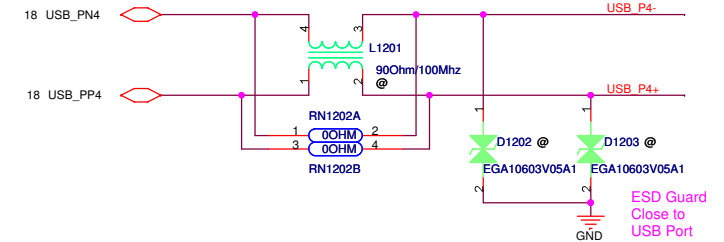
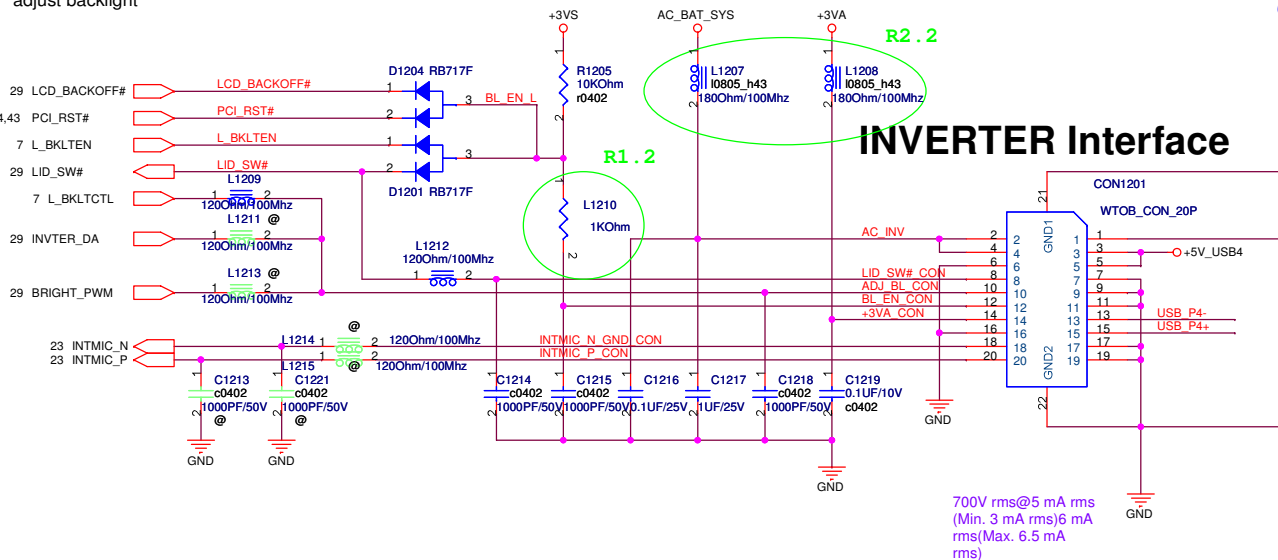
BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

*Inverter Board
built in 14.1W
LCD Panel*

<< Kennedy_Zhang >>

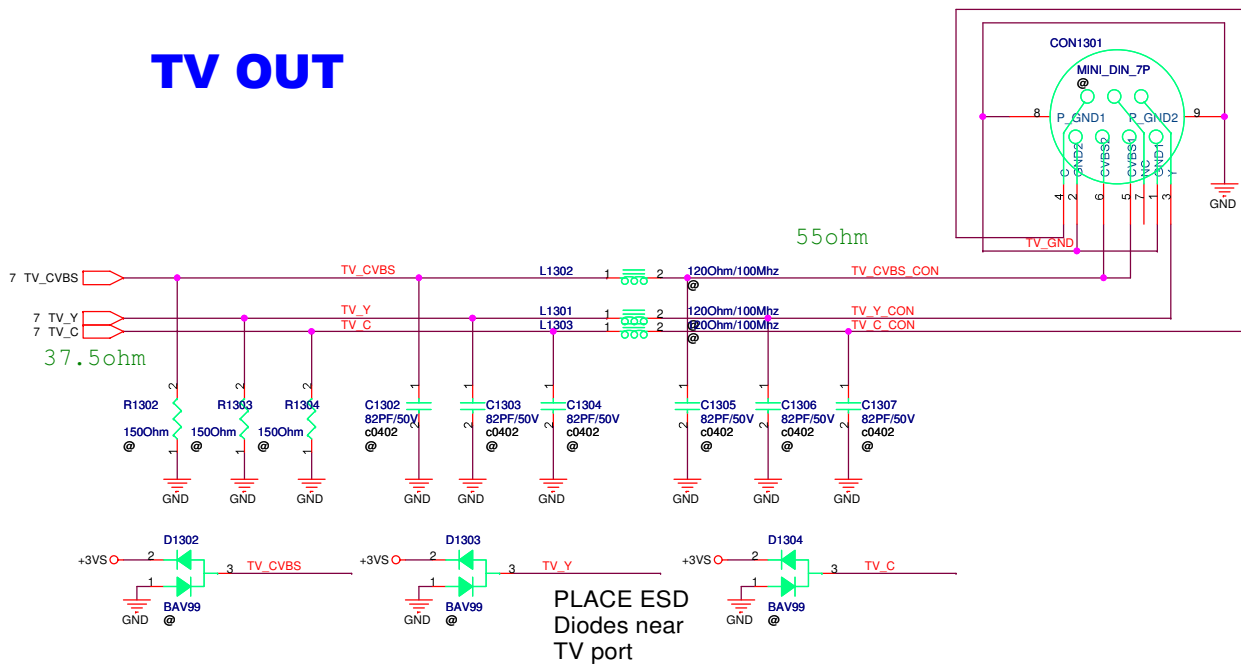
*USB4
For
CMOS
Camera*



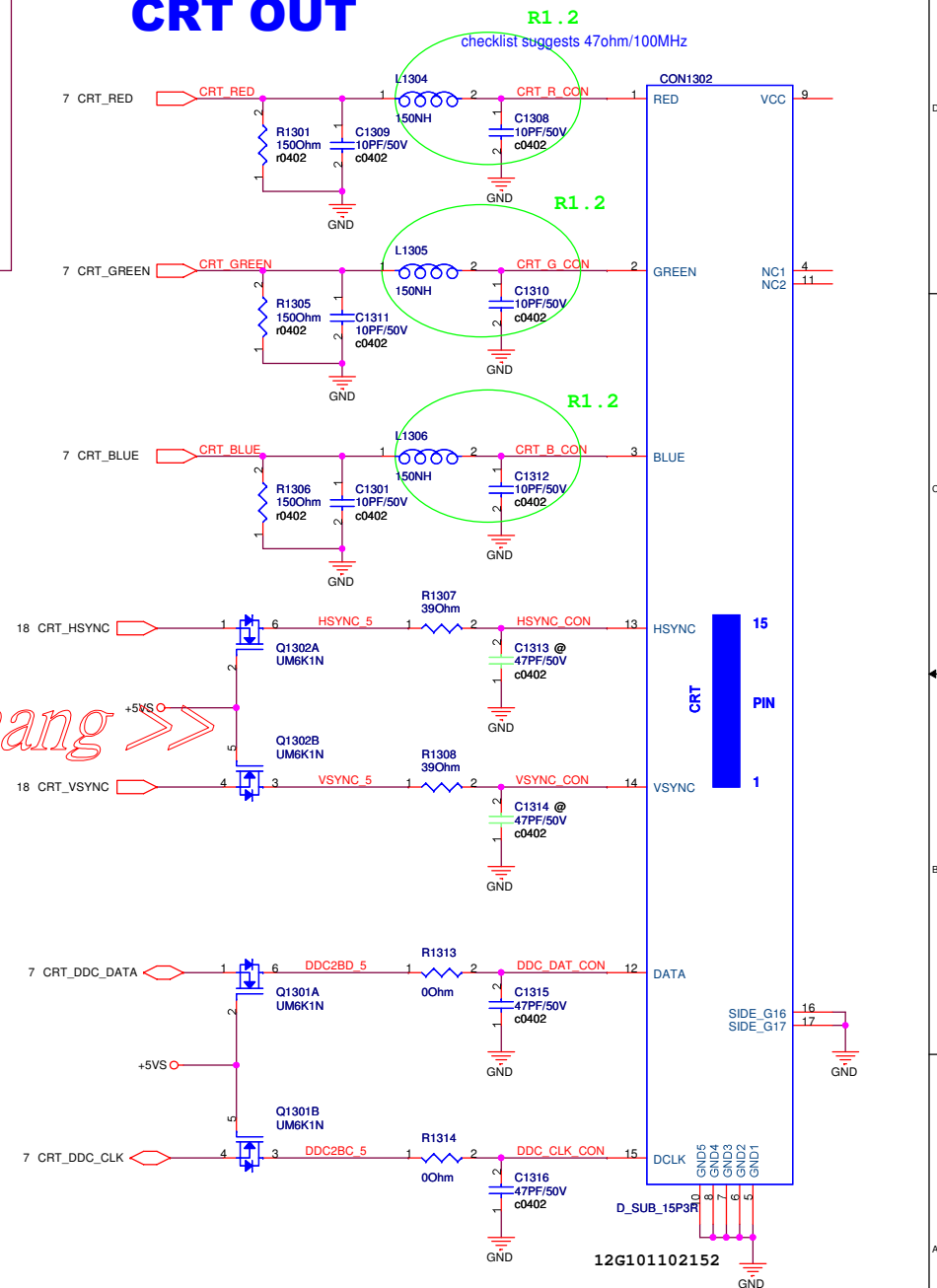
<Variant Name>

ASUS		Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
A3	T12F		
Date: 星期一, 五月 21, 2007	Sheet 12 of 61		

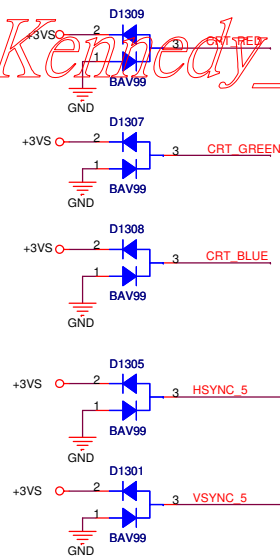
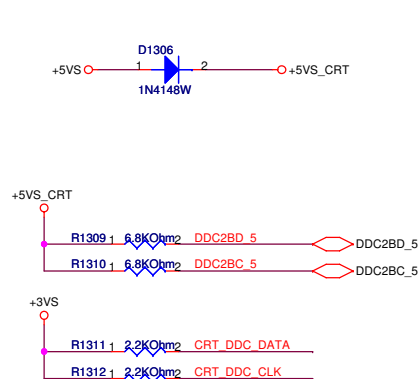
TV OUT



CRT OUT

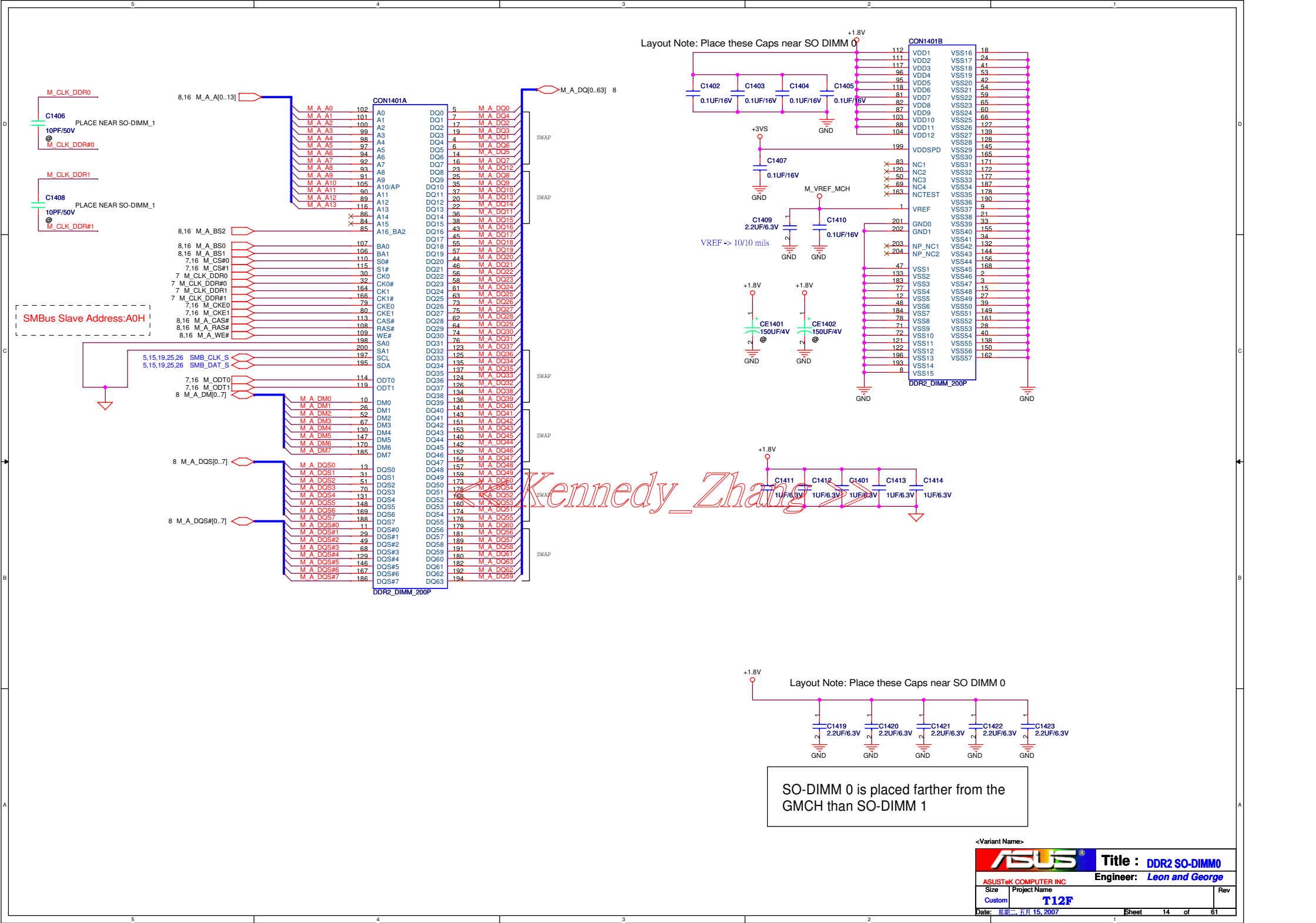


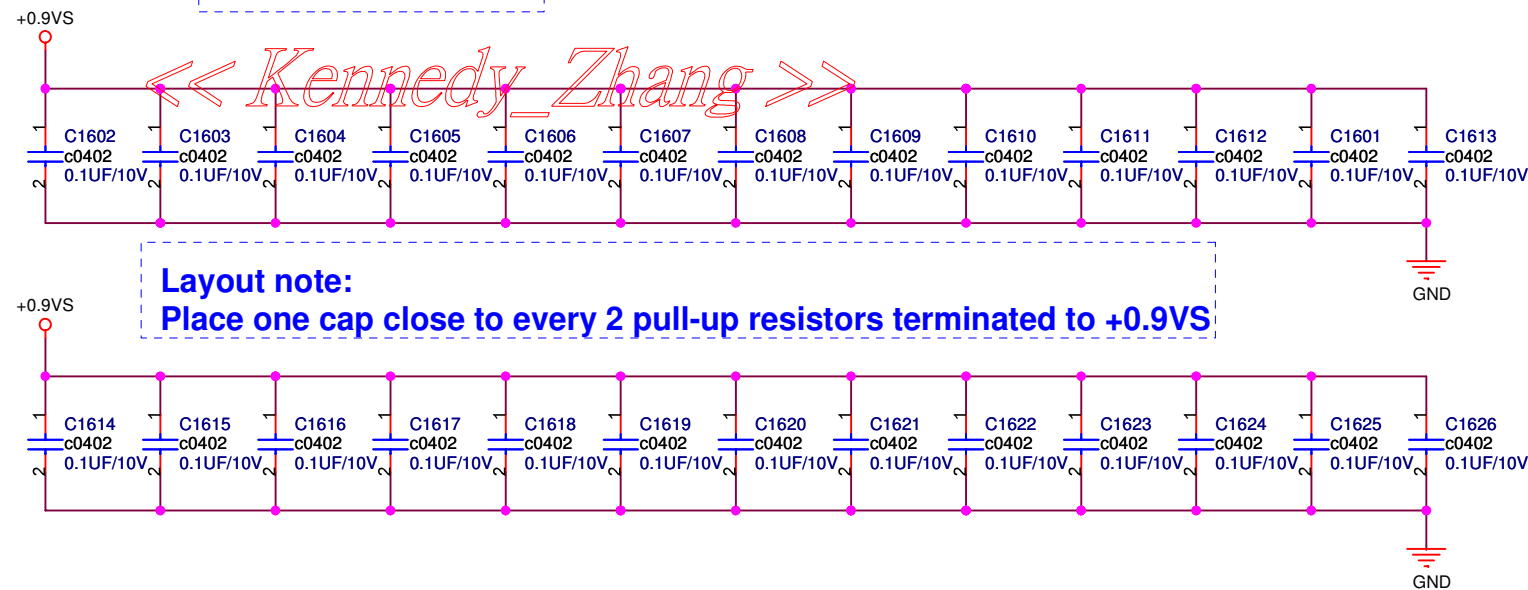
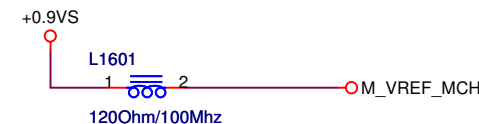
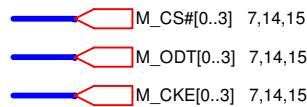
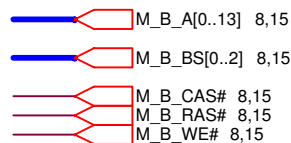
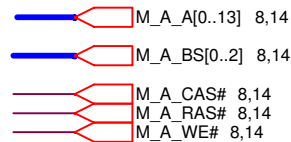
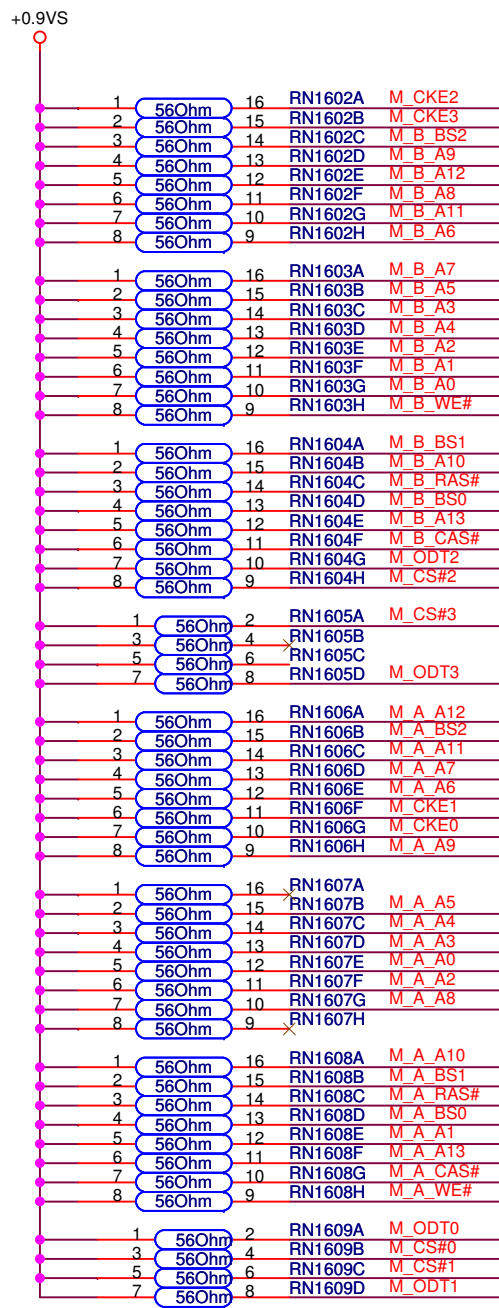
<< Kennedy_Zhang >>



<Variant Name>

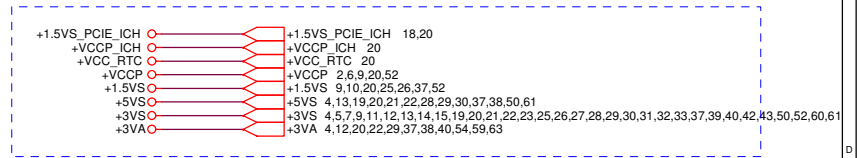
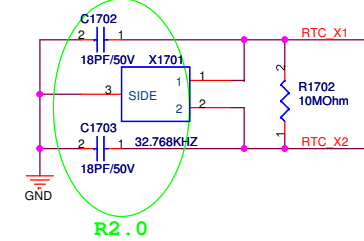
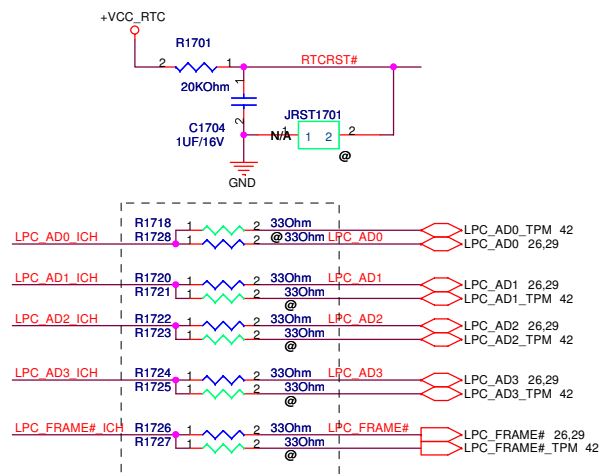
ASUS		Title : CRT & TV OUT	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
A3	T12F		
Date: 星期五, 五月 15, 2007		Sheet 13 of 61	



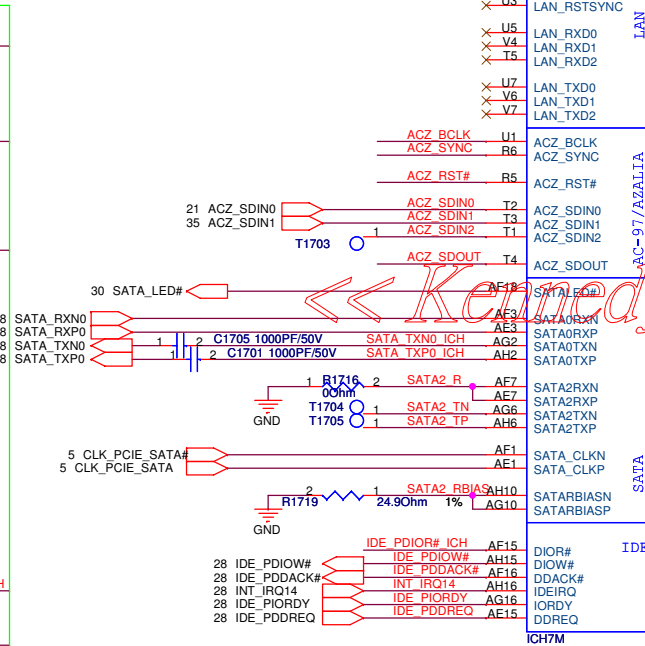
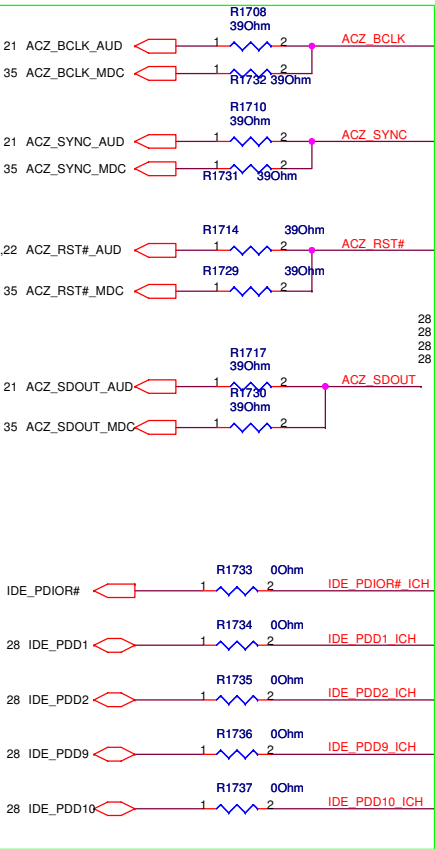


<Variant Name>

ASUS		Title : DDR2 TERM	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size A4	Project Name T12F	Rev	
Date: 星期二, 五月 15, 2007		Sheet	16 of 61

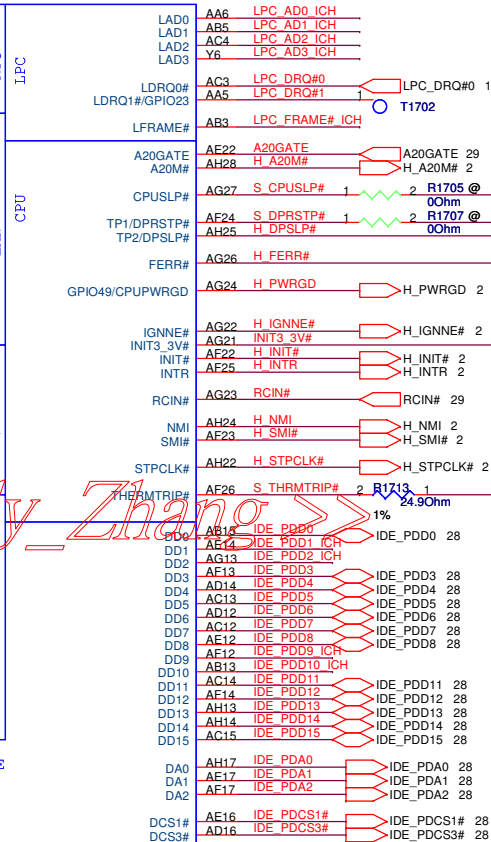


close to ICH7



R1.1

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17#			
GNT4#/GPIO48	PWROK rising	0 1 SPI 1 0 PCI 1 1 LPC	PU



DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ? 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ? 5% pull-up resistor has to be within 2" from the series resistor

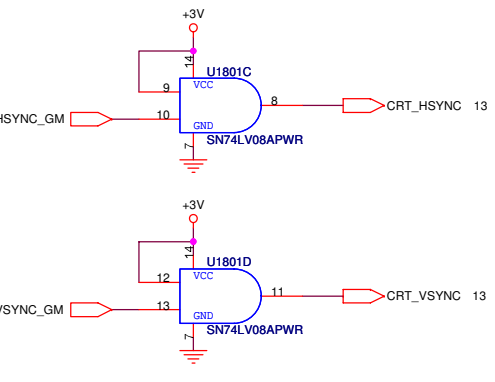
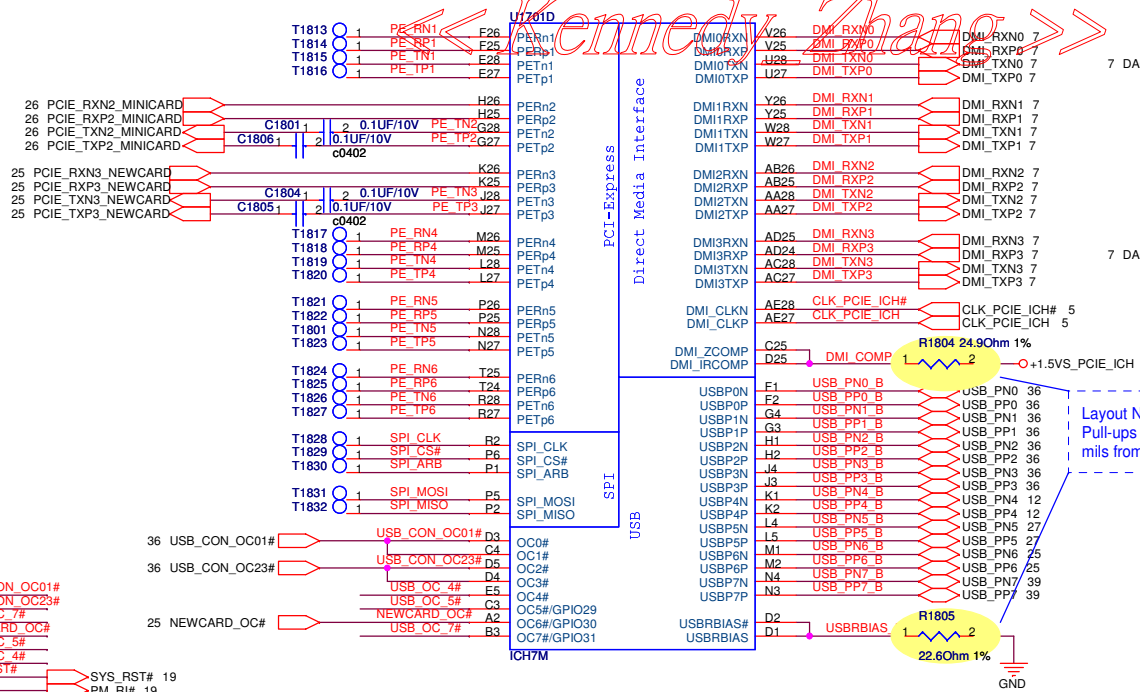
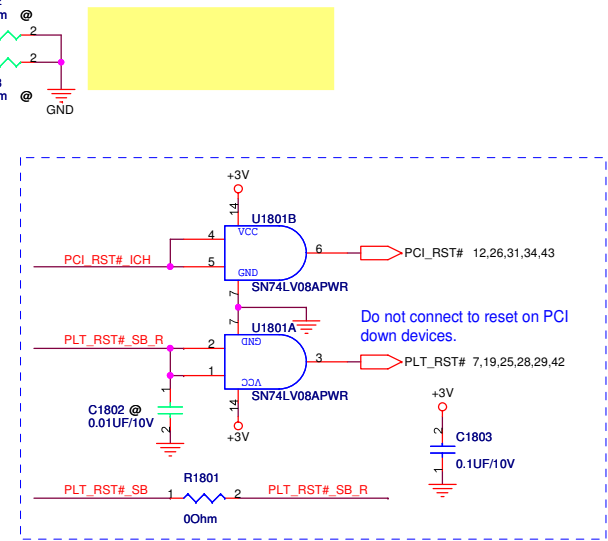
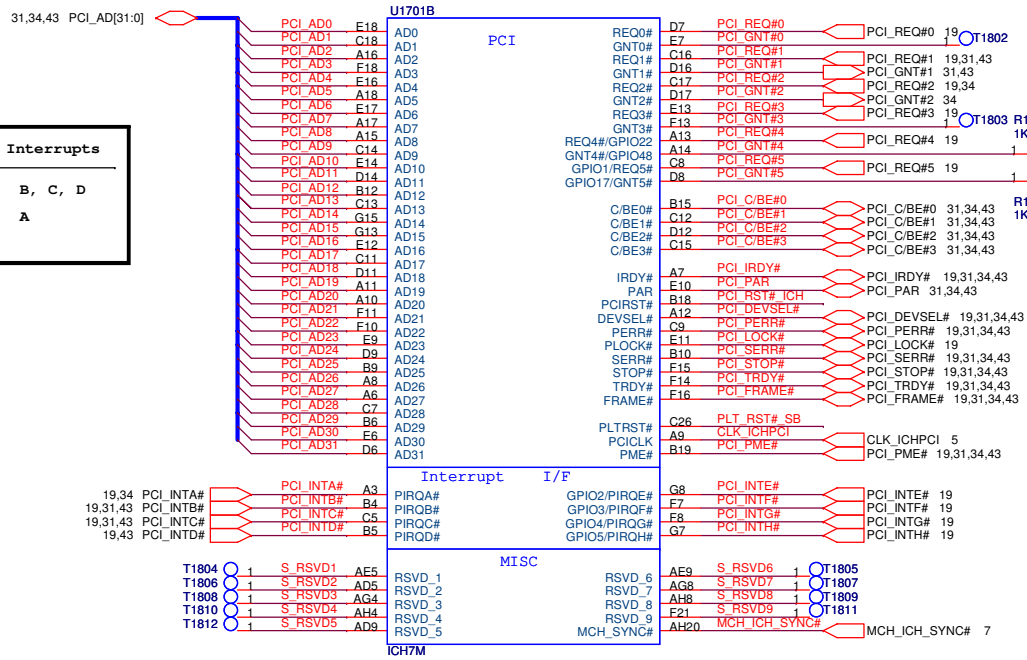
GPIO16 /DPRSLPVR	should not be pulled high	PD
GPIO25	RSRST# rising	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM
LINKALERT#		REQUIRE an external pull-up R
REQ[4:1]#	PWROK rising	Need PU
SATALED#		should not be pulled low
SPKR	PWROK rising	high: "No reboot" mode
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing

Variant Name

ASUS		Title : ICH7-M (1/4)	
ASUSTek COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
Custom	T12F		
Date: 星期五, 五月 18, 2007	Sheet	17	of 61

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A



USB Devices

- Port 0 CON3602
- Port 1 CON3603
- Port 2 CON3601
- Port 3 CON3601
- Port 4 CMOS Camara
- Port 5 BlueTooth
- Port 6 NewCard
- Port 7 FingerPrint

Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

<Variant Name>

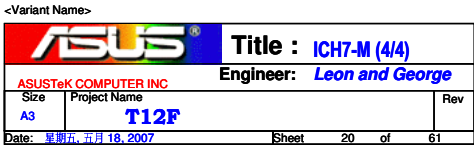
ASUS Title : ICH7-M (2/4)

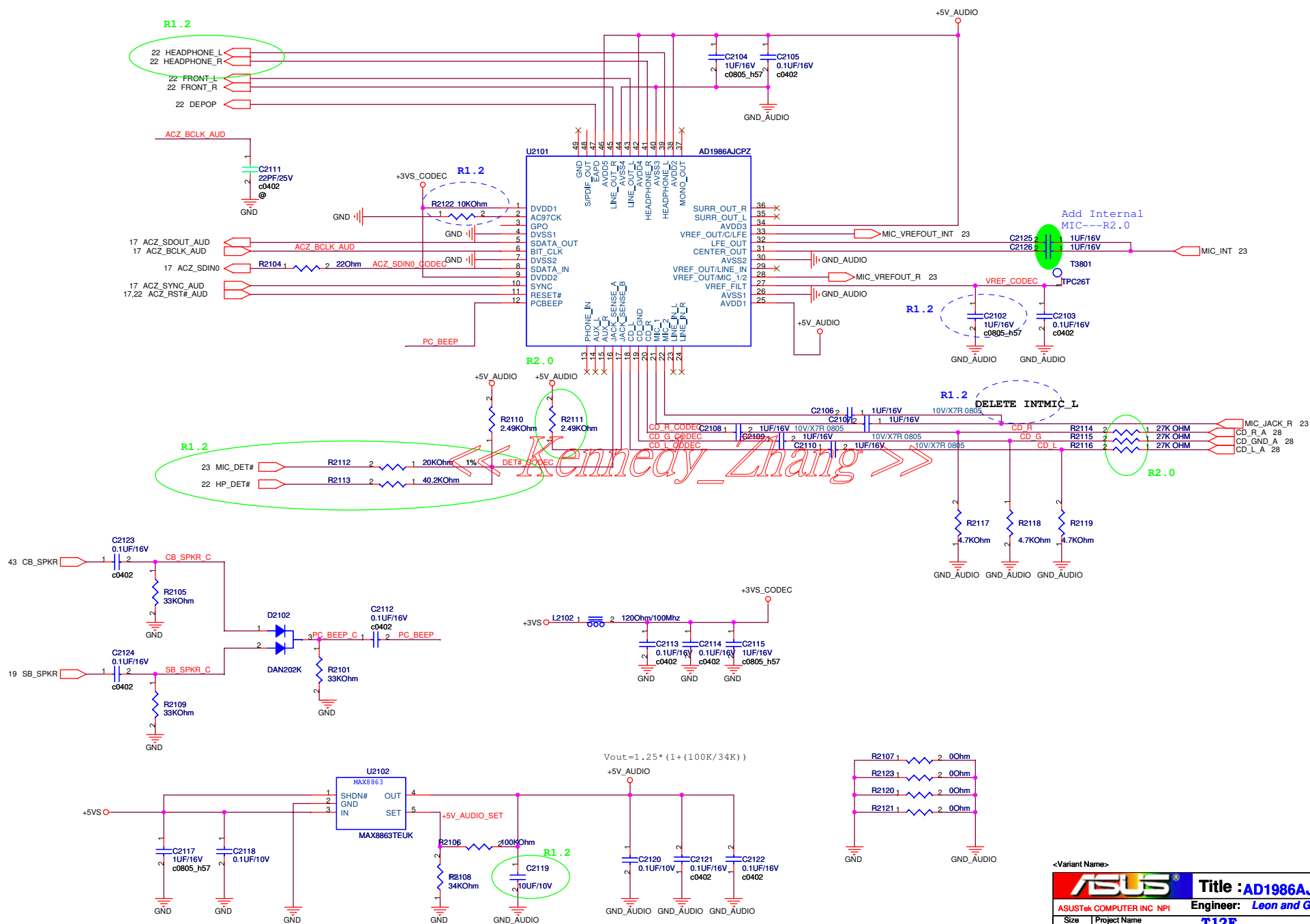
ASUSTek COMPUTER INC Engineer: Leon and George

Size Project Name

Custom T12F

Date: 星期二, 五月 15, 2007 Sheet 18 of 61





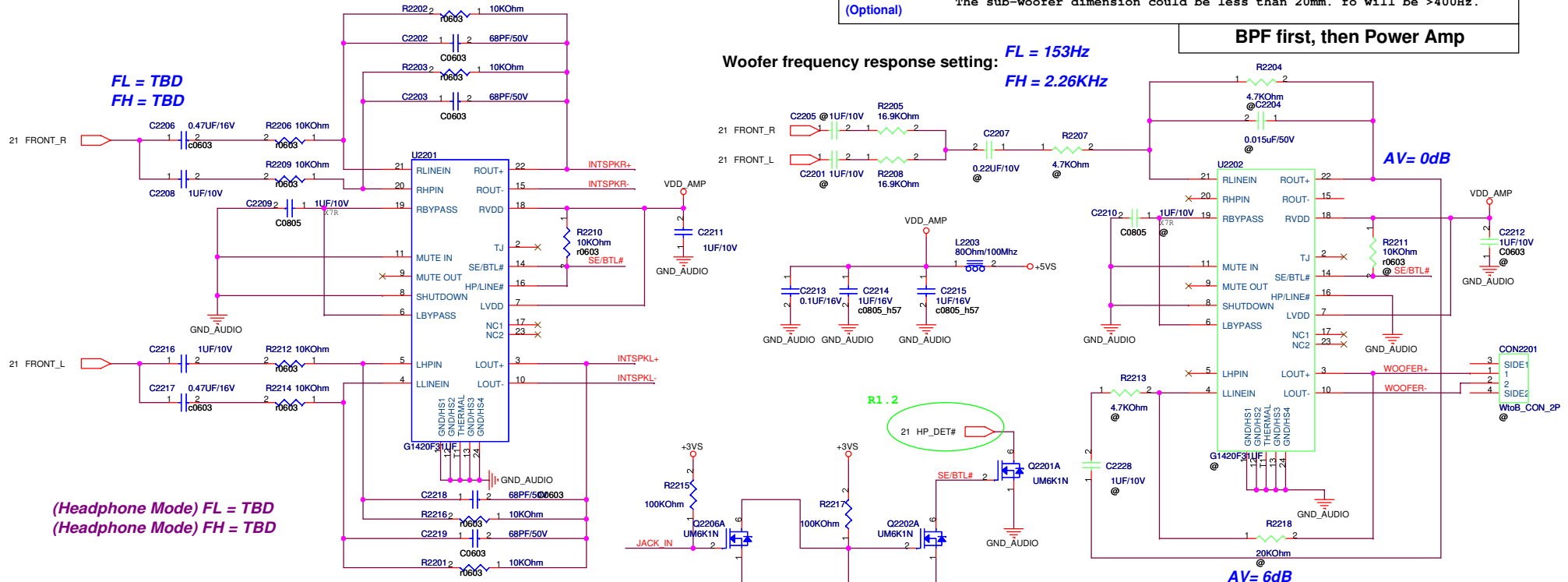
Woofer
(Optional)

The sub-woofer dimension could be less than 20mm. fo will be >400Hz.

BPF first, then Power Amp

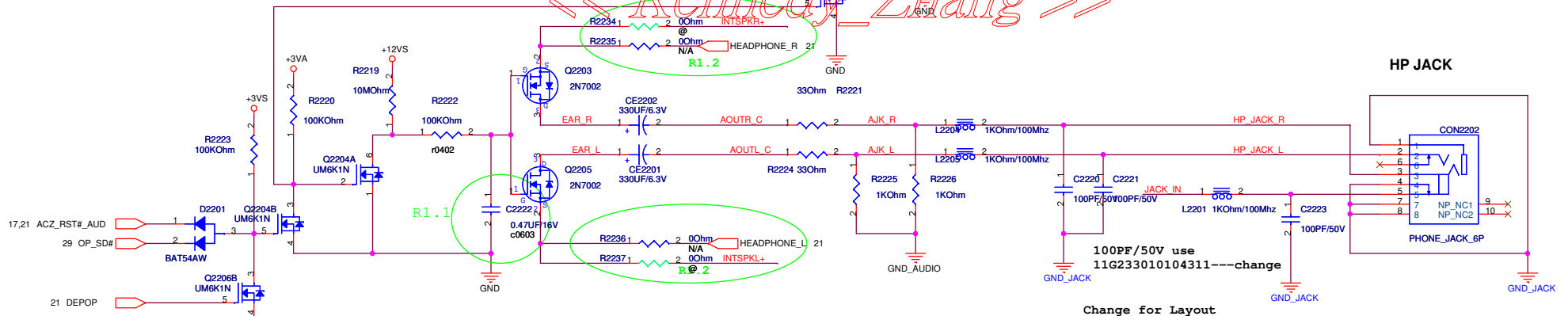
Woofer frequency response setting: $FL = 153\text{Hz}$
 $FH = 2.26\text{KHz}$

$FL = \text{TBD}$
 $FH = \text{TBD}$



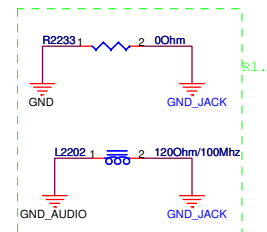
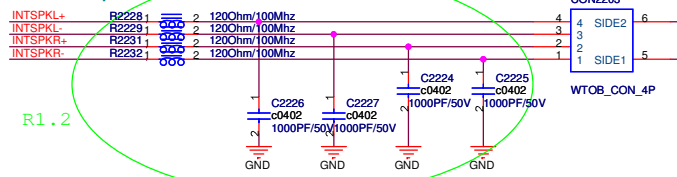
(Headphone Mode) $FL = \text{TBD}$
(Headphone Mode) $FH = \text{TBD}$

<< Kennedy Zhang >>

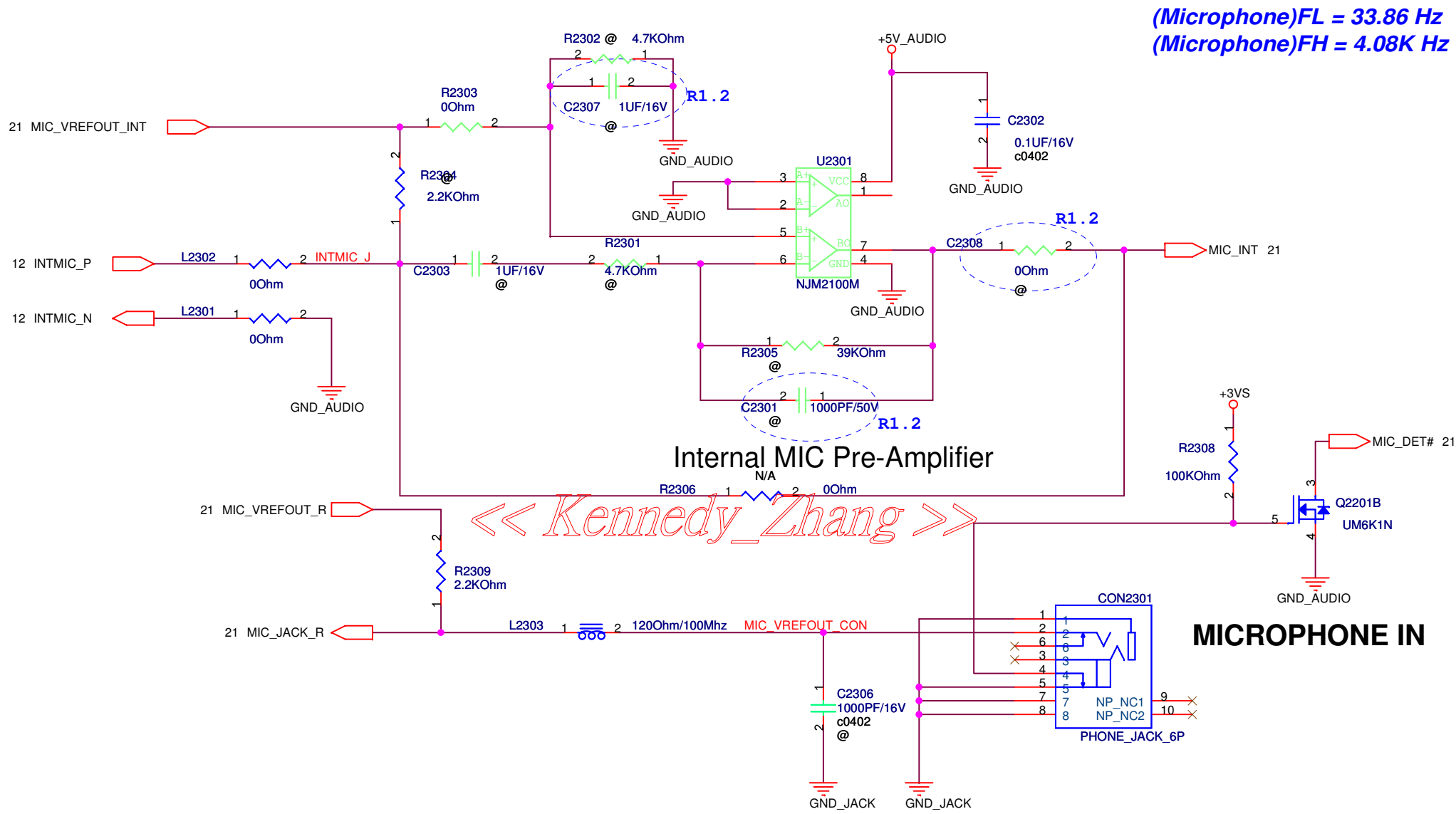


Change for Layout

To Internal Speaker Connector



<Variant Name>

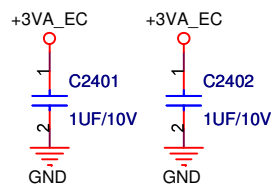


(Microphone)FL = 33.86 Hz
(Microphone)FH = 4.08K Hz

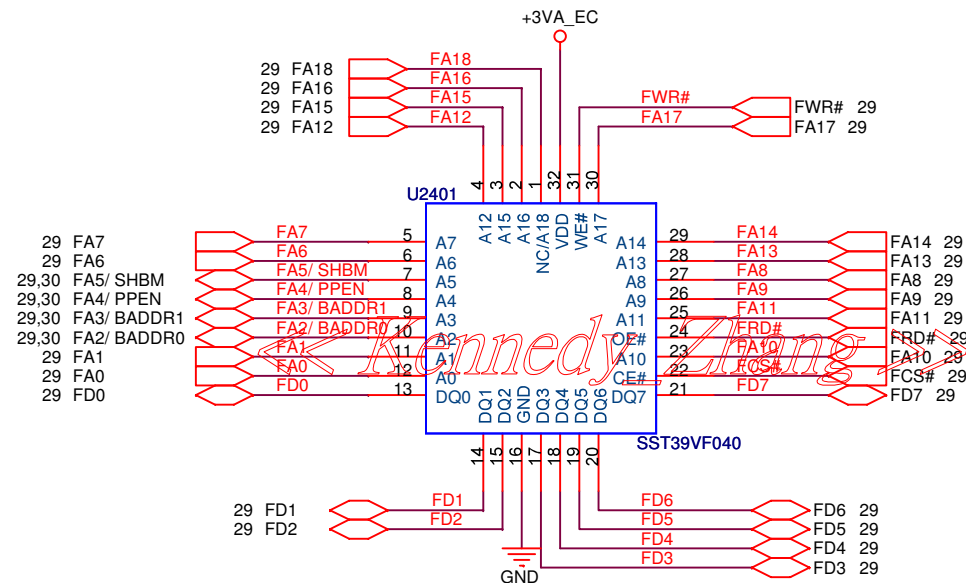
MICROPHONE IN

<Variant Name>

		Title : MIC Pre-AMP	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size A4	Project Name T12F	Rev	
Date: 星期一, 五月 21, 2007		Sheet	23 of 61

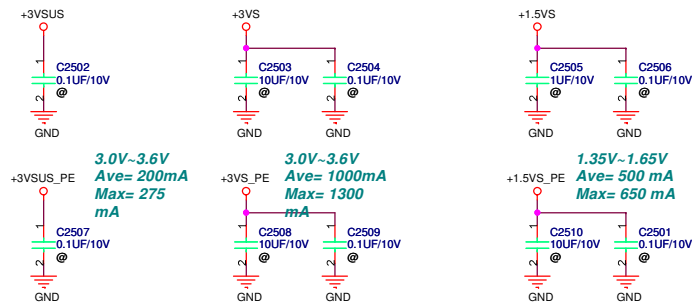
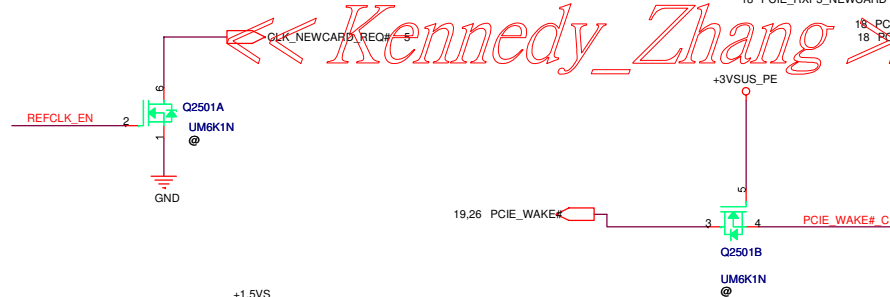
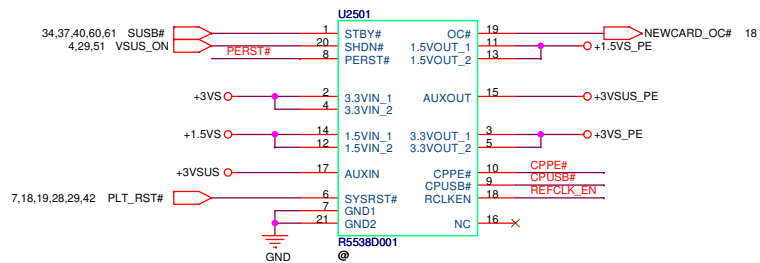
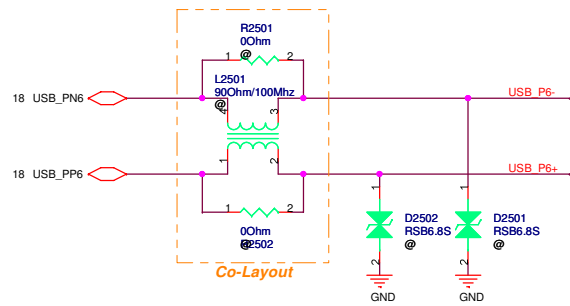


ISA ROM

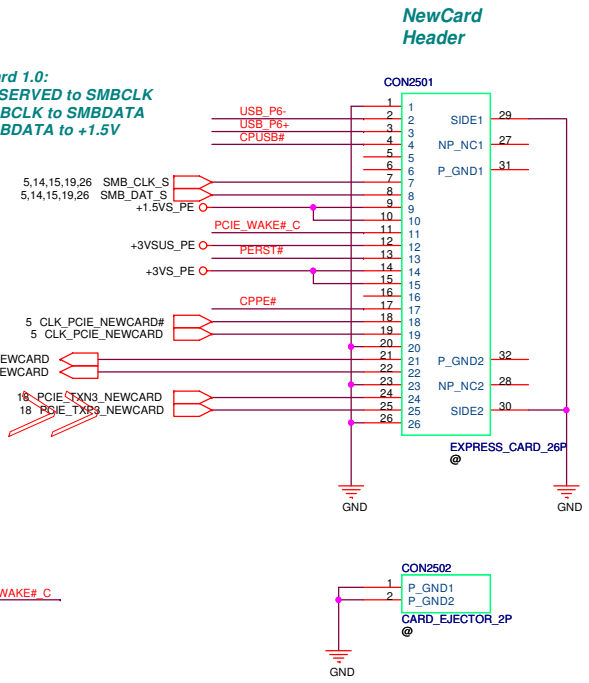


<Variant Name>

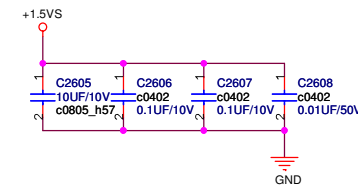
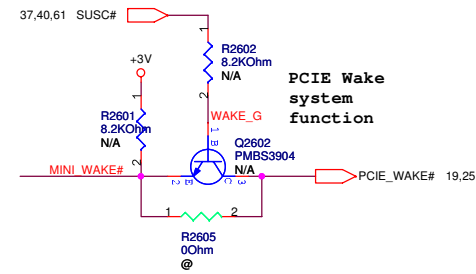
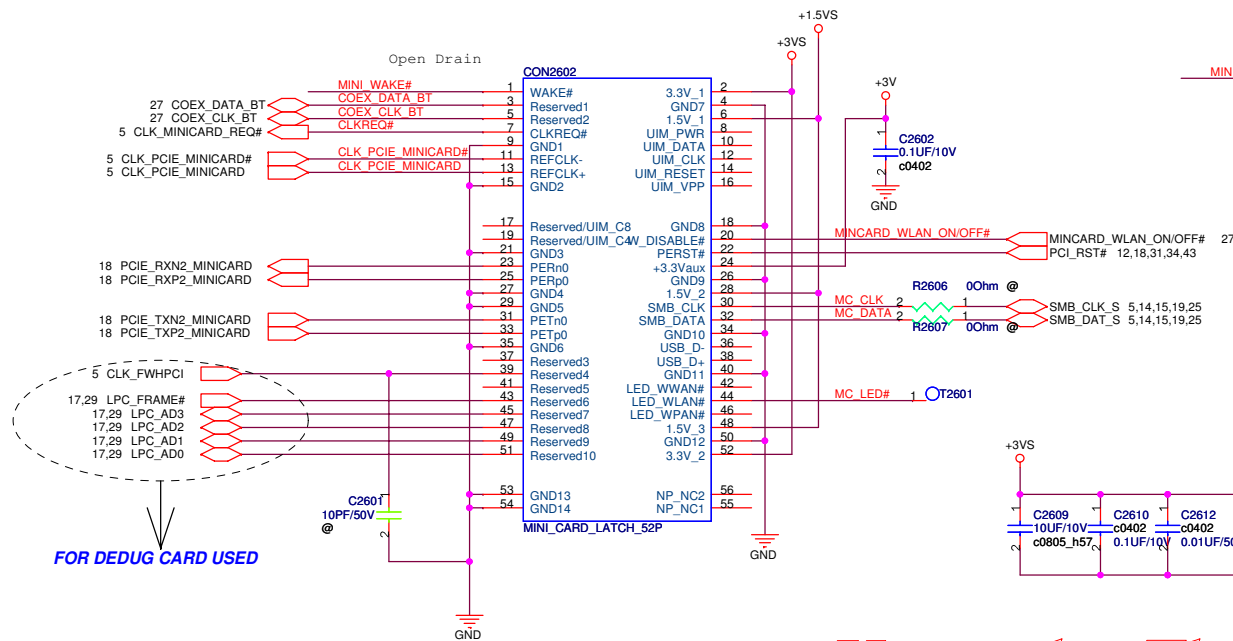
		Title : ISA ROM	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name		Rev
A4	T12F		
Date: 星期二, 五月 15, 2007		Sheet	24 of 61



!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



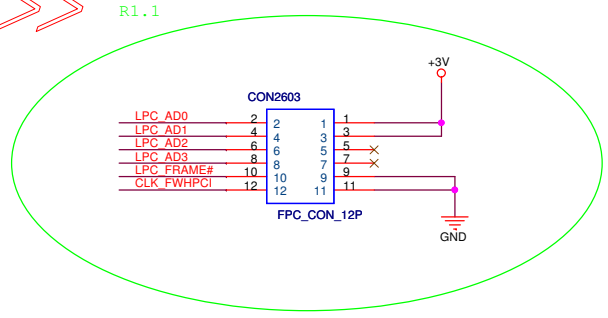
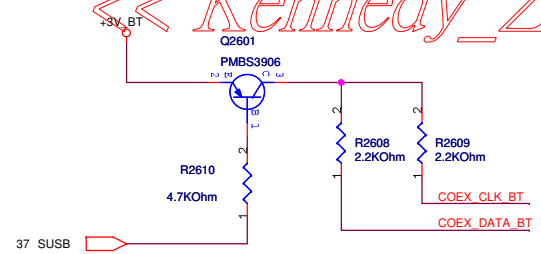
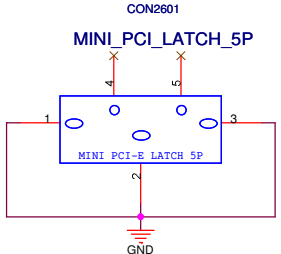
MINI PCIE X CONNECTOR



+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

Check O/D output or push pull

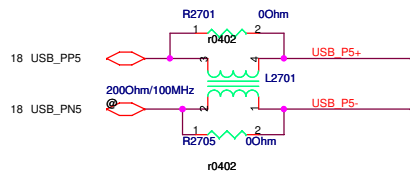
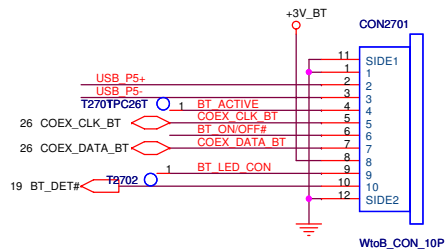
<< Kennedy_Zhang >>



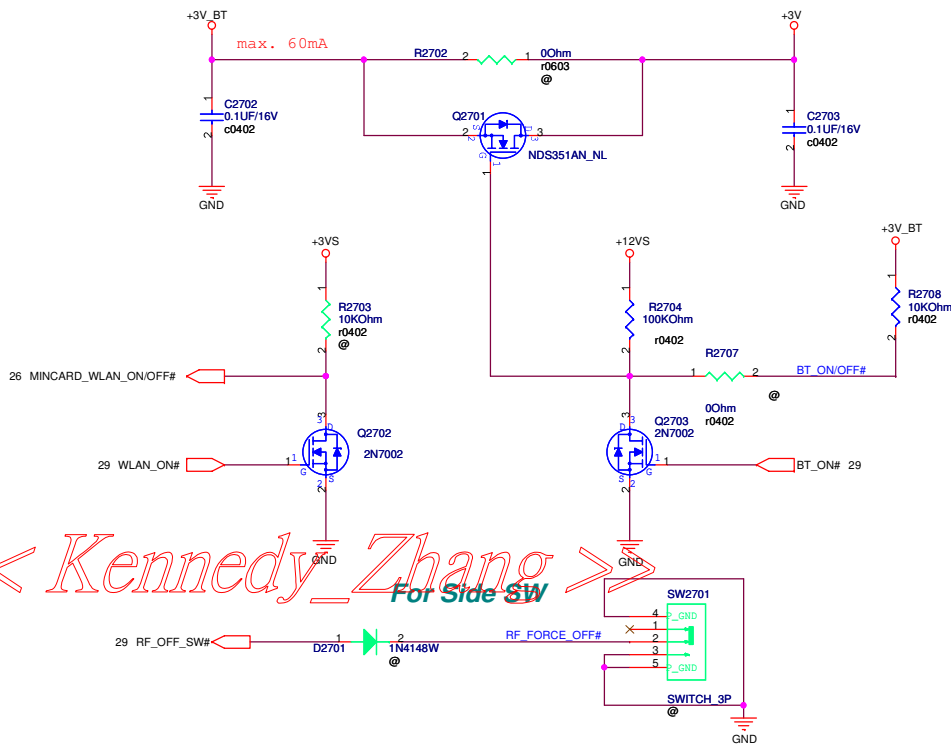
<Variant Name>

ASUS		Title : MINI PCIE X	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
A3	T12F		
Date: 星期二, 五月 15, 2007	Sheet 26 of 61		

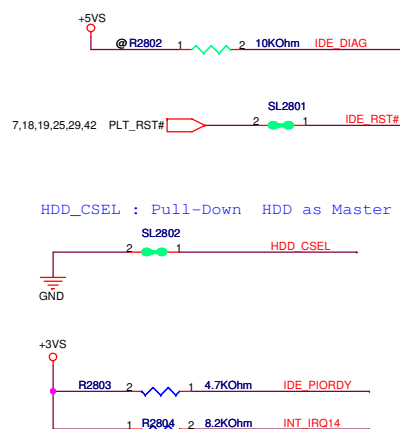
For Bluetooth



WLAN/BT ON/OFF Control

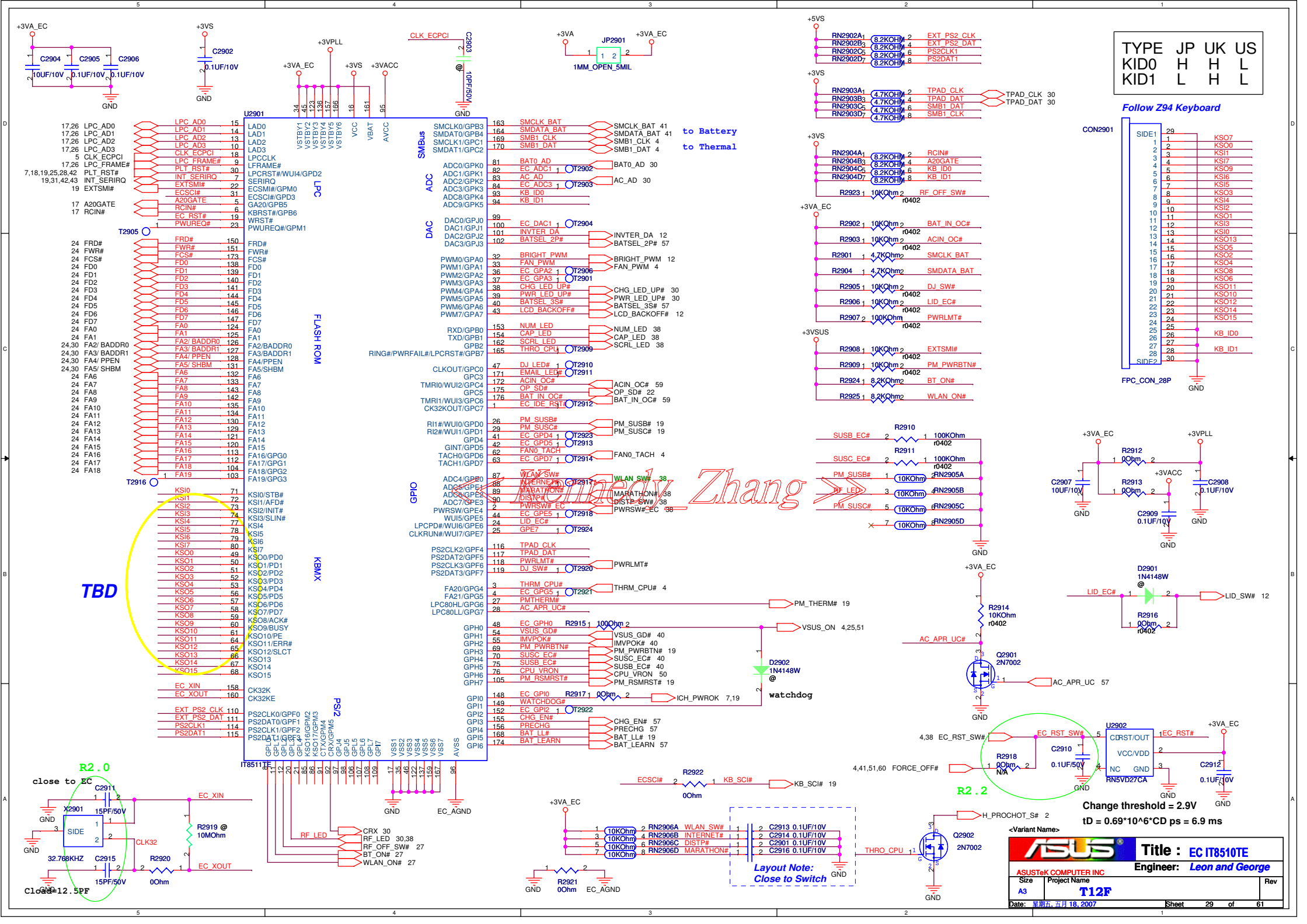


<< Kennedy_Zhang >>
For Side SW



<< Kennedy_Zhang >>

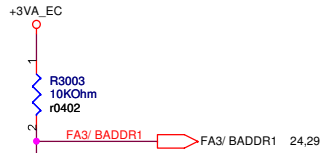
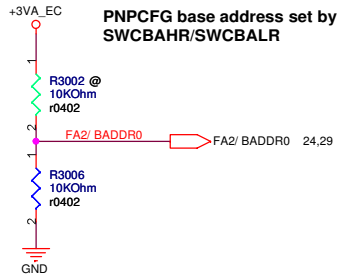
[illegible]



EC Hardware Strap

**Strap value sampled after
VSTBY power up reset**

**PNPCFG base address set by
SWCBAHR/SWCBALR**



BADDR[1:0]

No pull up:

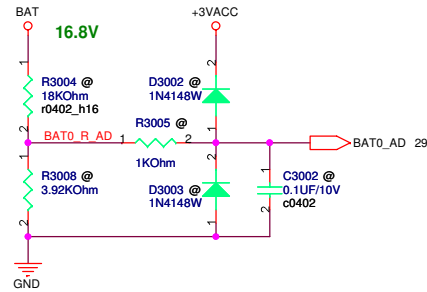
Ext 10K up on BADDR0:

Ext 10K up on BADDR1:

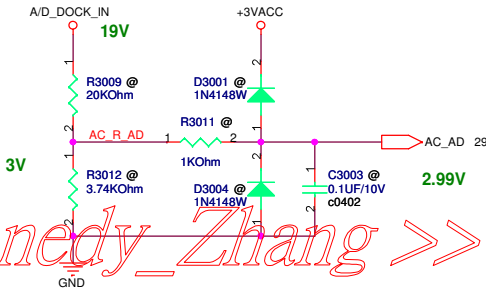
The register pair to access PNPCFG is 002Eh and 002Fh.
The register pair to access PNPCFG is 004Eh and 004Fh.
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

EC ADC

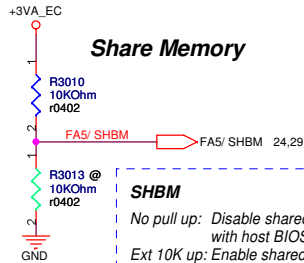
Battery



Adaptor



Share Memory



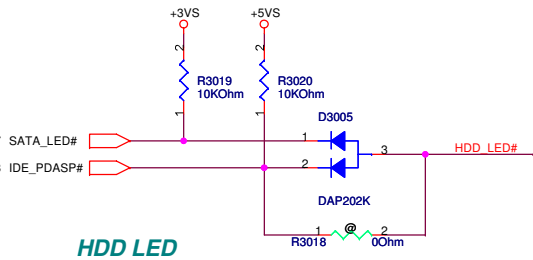
SHBM

No pull up: Disable shared memory with host BIOS
Ext 10K up: Enable shared memory with host BIOS

PPEN

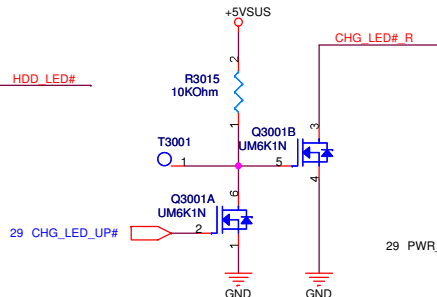
No pull up: Normal KBS interface pins are switched to parallel port interface for in-system programming.
Ext 10K up:

Touchpad

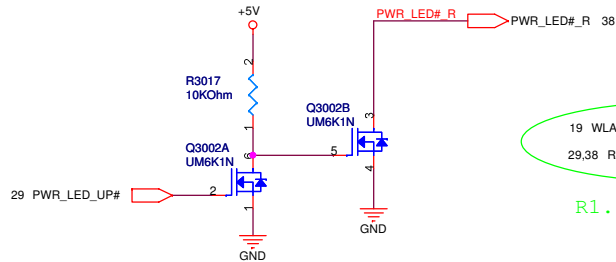


HDD LED

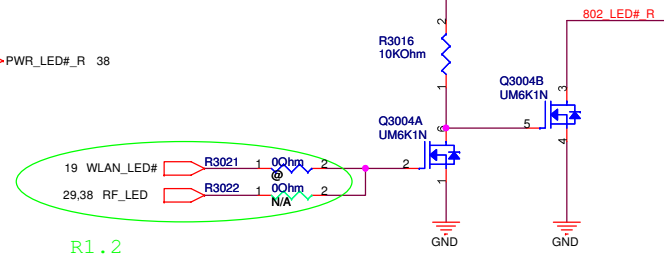
CHARGE LED



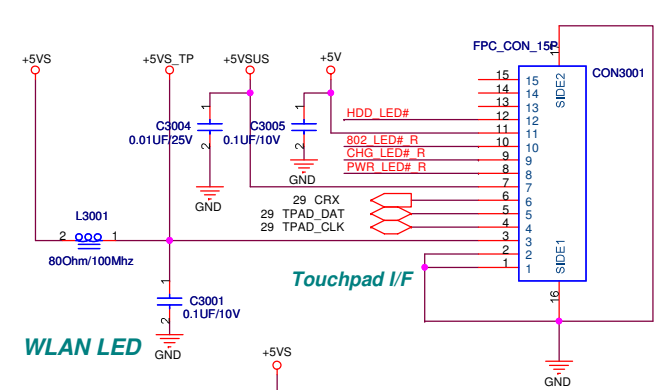
POWER LED



WLAN LED



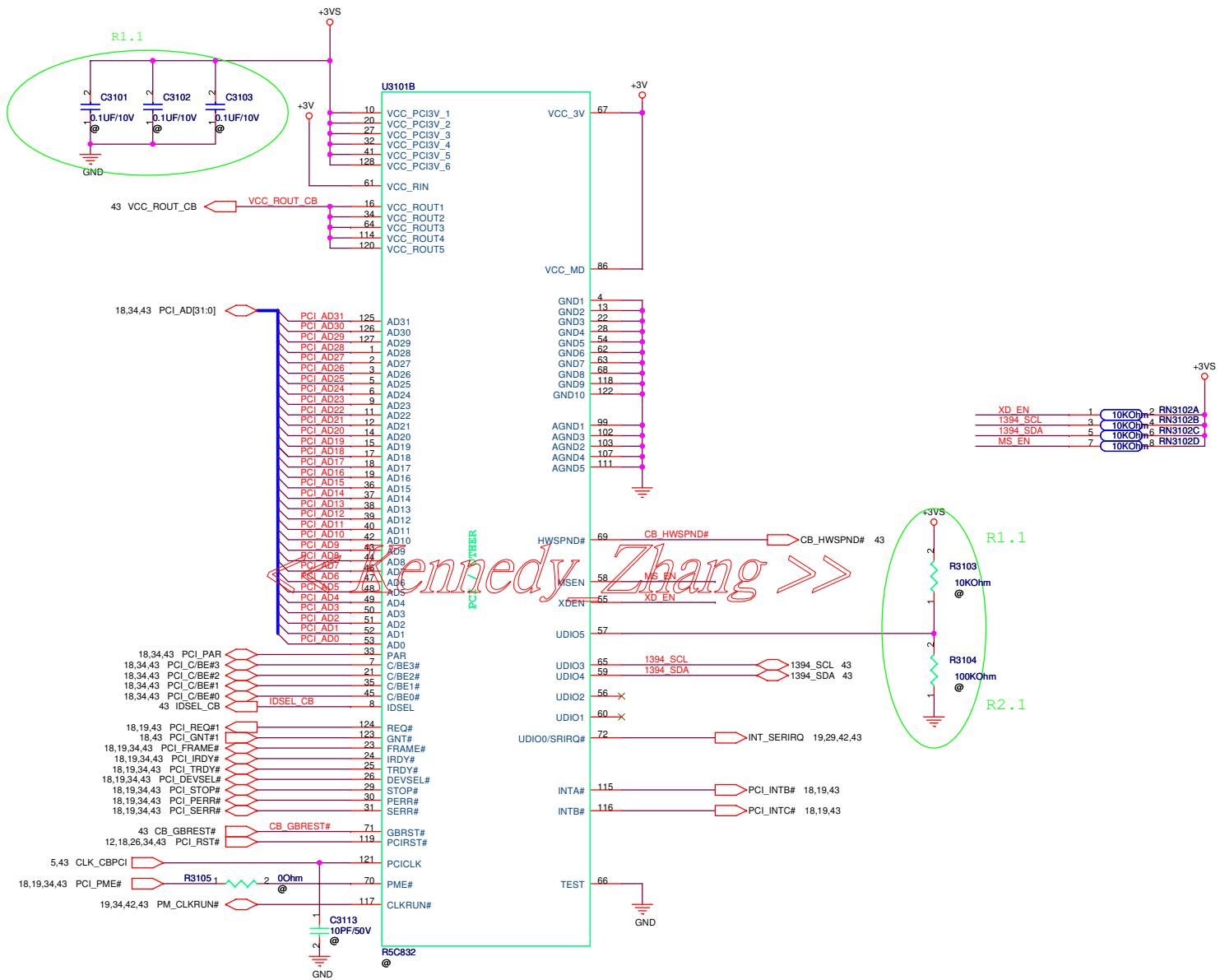
R1.2

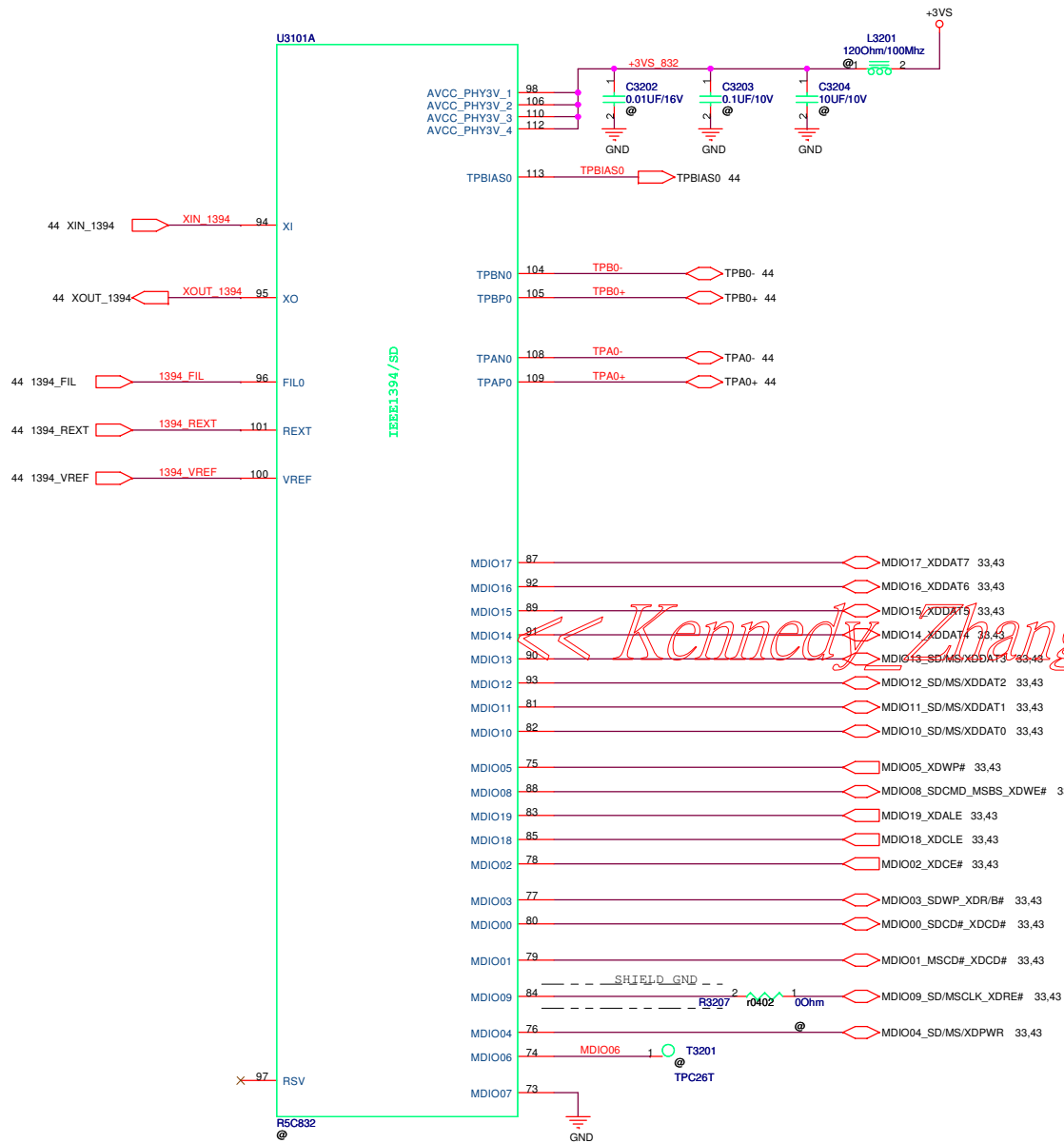


Touchpad I/F

<Variant Name>

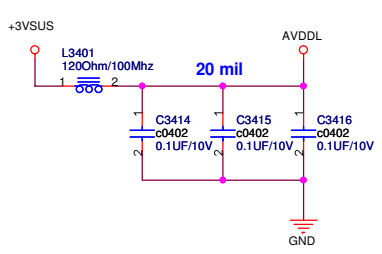
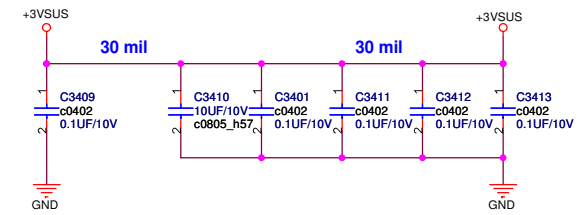
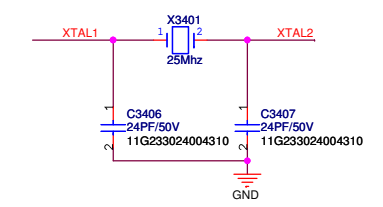
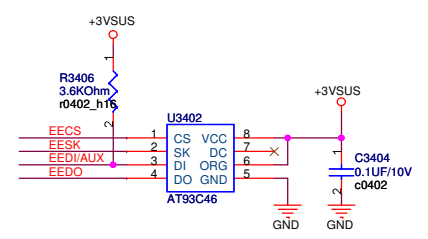
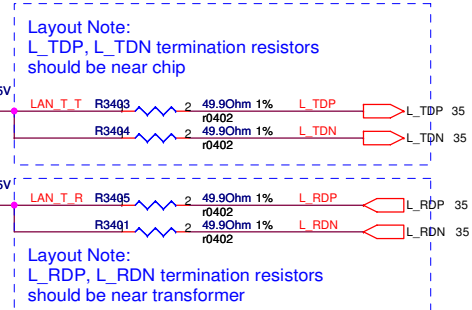
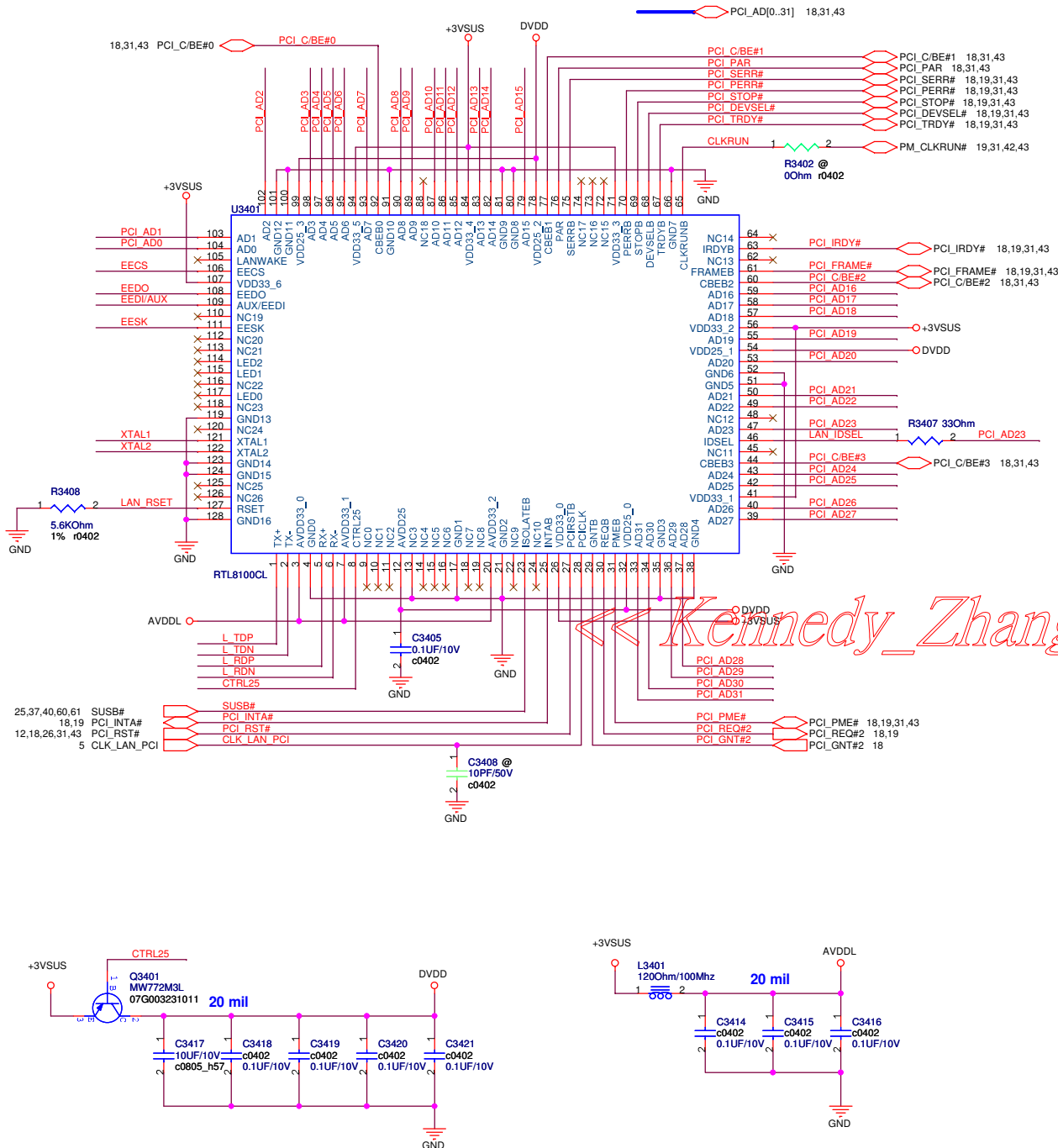
ASUS		Title : EC IT8510TE(2/2)	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
A3	T12F		
Date: 星期五, 五月 18, 2007		Sheet	30 of 61



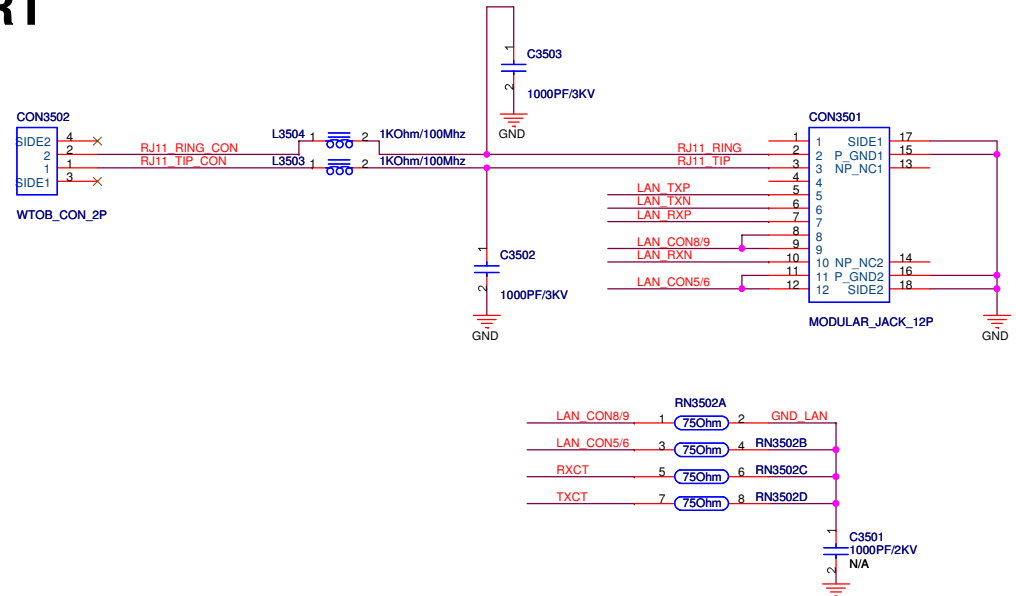
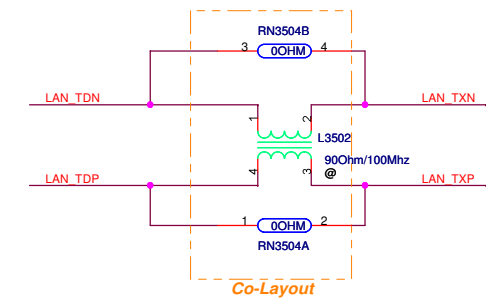
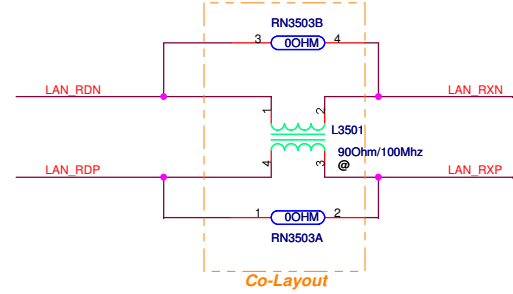
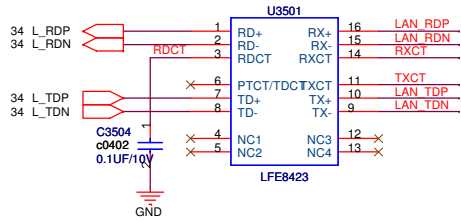


<Variant Name>

ASUS		Title : CARD1394-R5C832(2)	
ASUSTeK COMPUTER INC. NB1		Engineer: Leon and George	
Size	Project Name	Rev	
Custom	T12F		
Date: 底層二, 九月 15, 2007	Sheet 32	of 61	

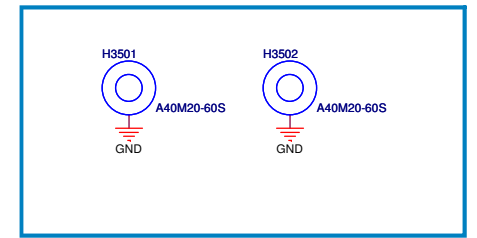
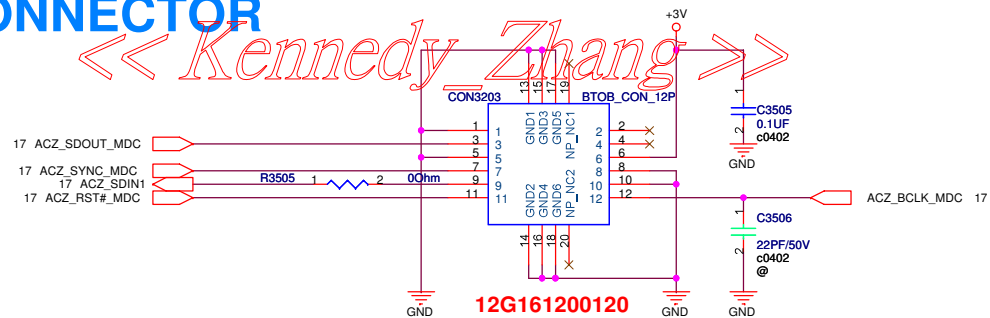


LAN PORT



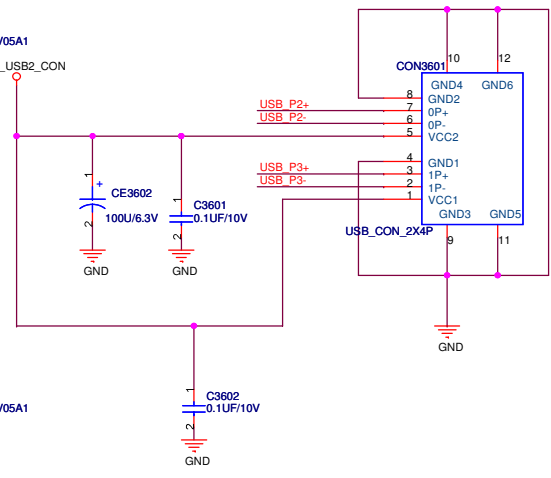
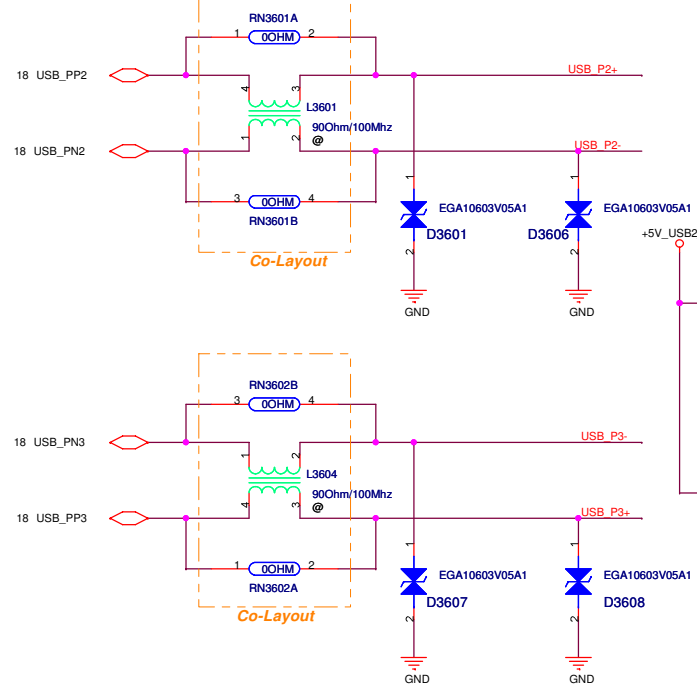
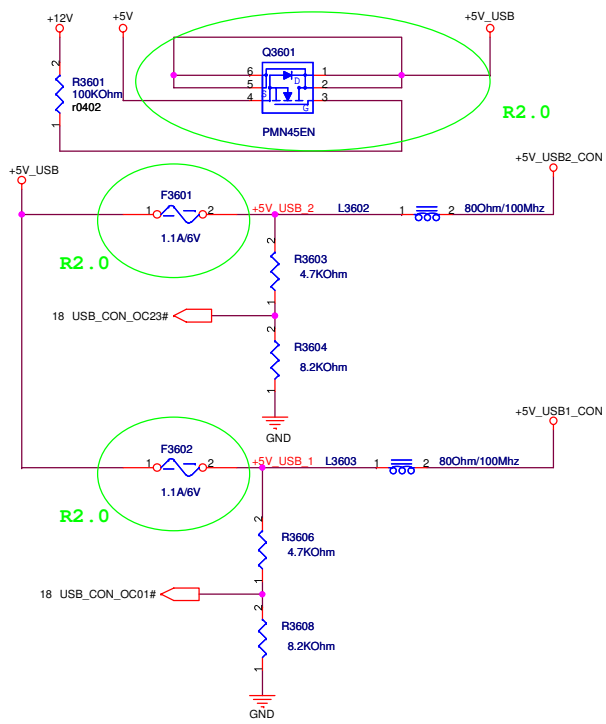
R1.2

MDC CONNECTOR

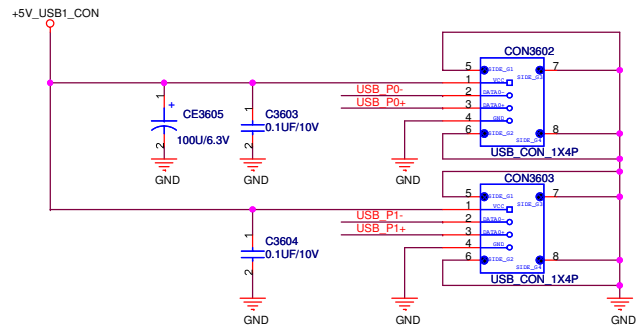
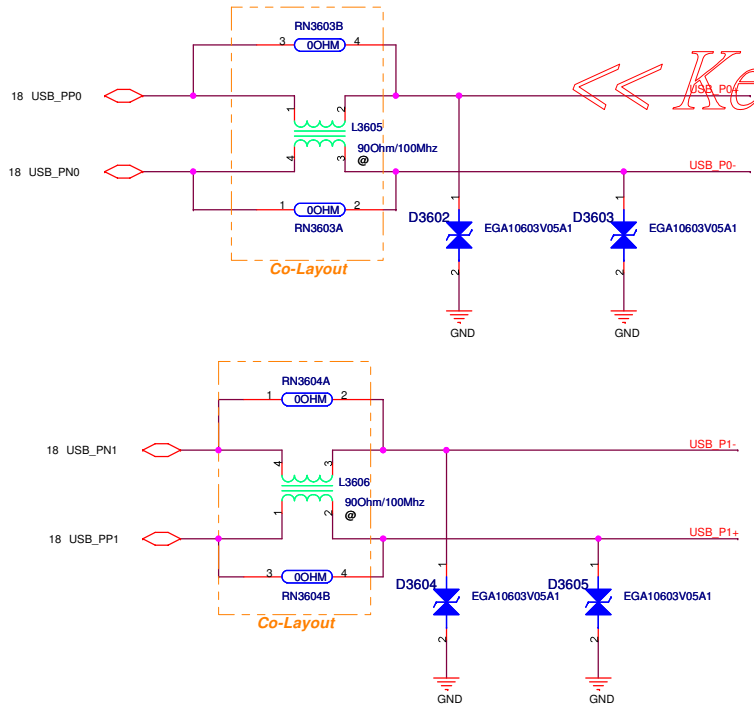


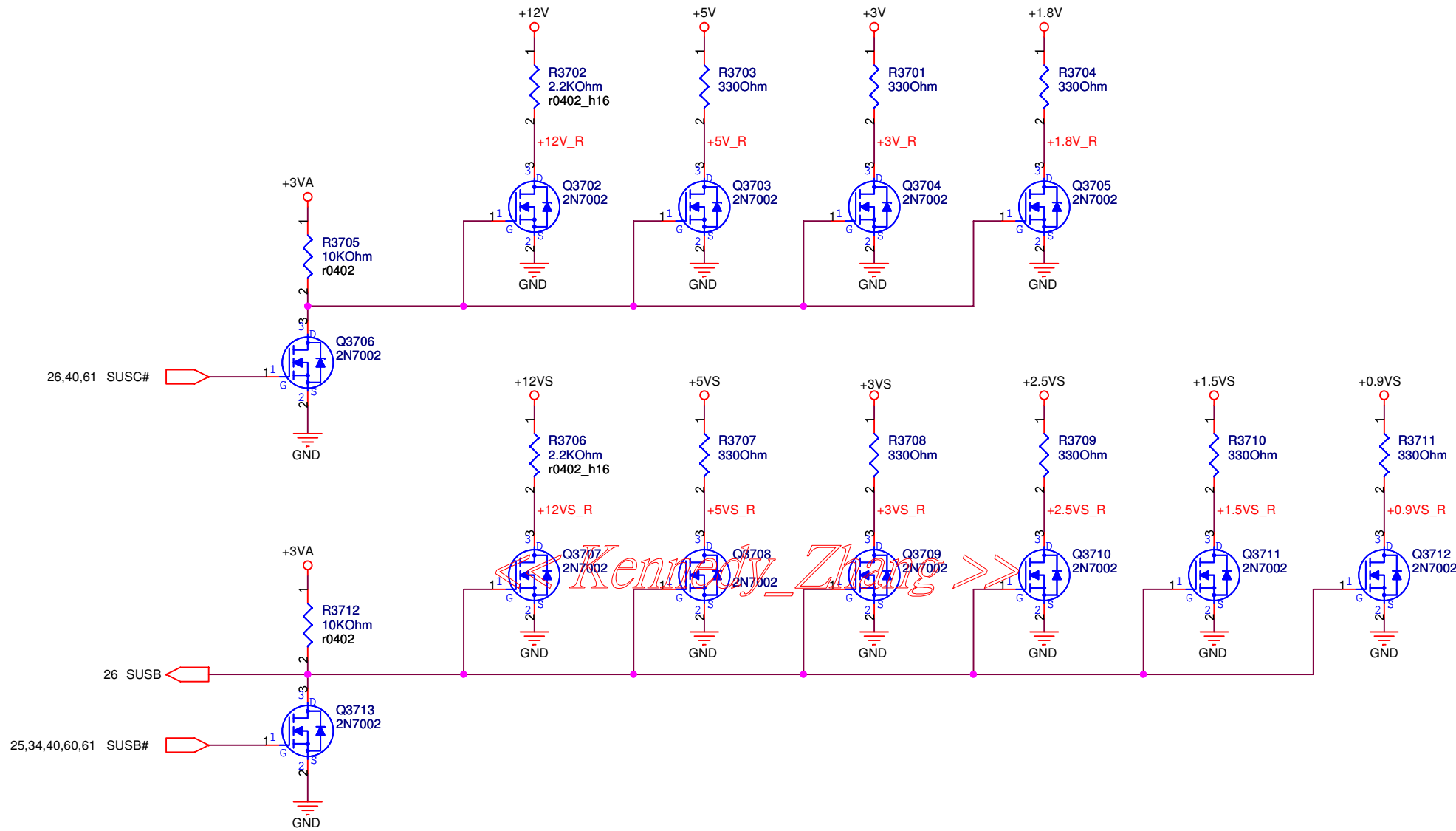
<Variant Name>

ASUS		Title : RJ11/45 & MDC	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
Custom	T12F		
Date: 星期五, 五月 15, 2007	Sheet 35 of 61		



<< Kennedy_Zhang >>

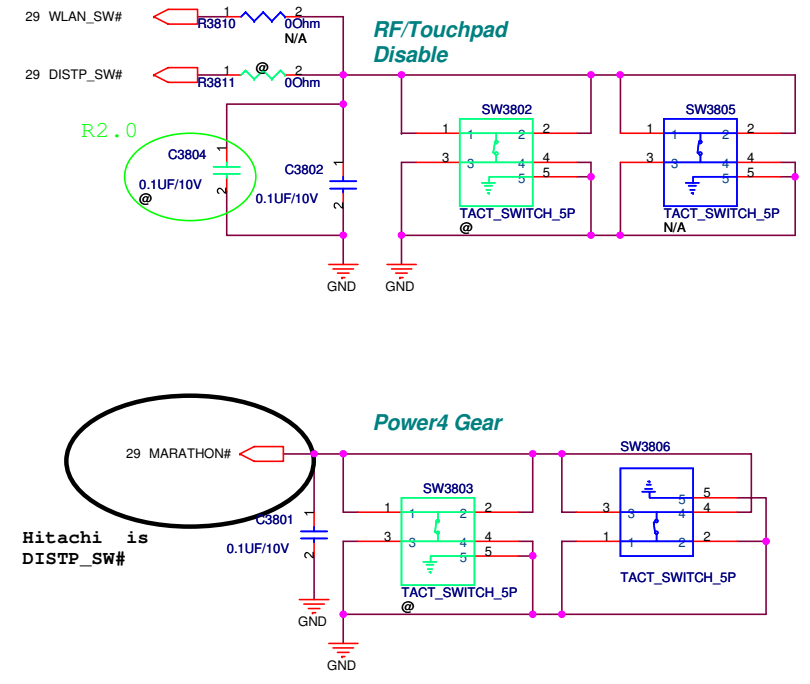
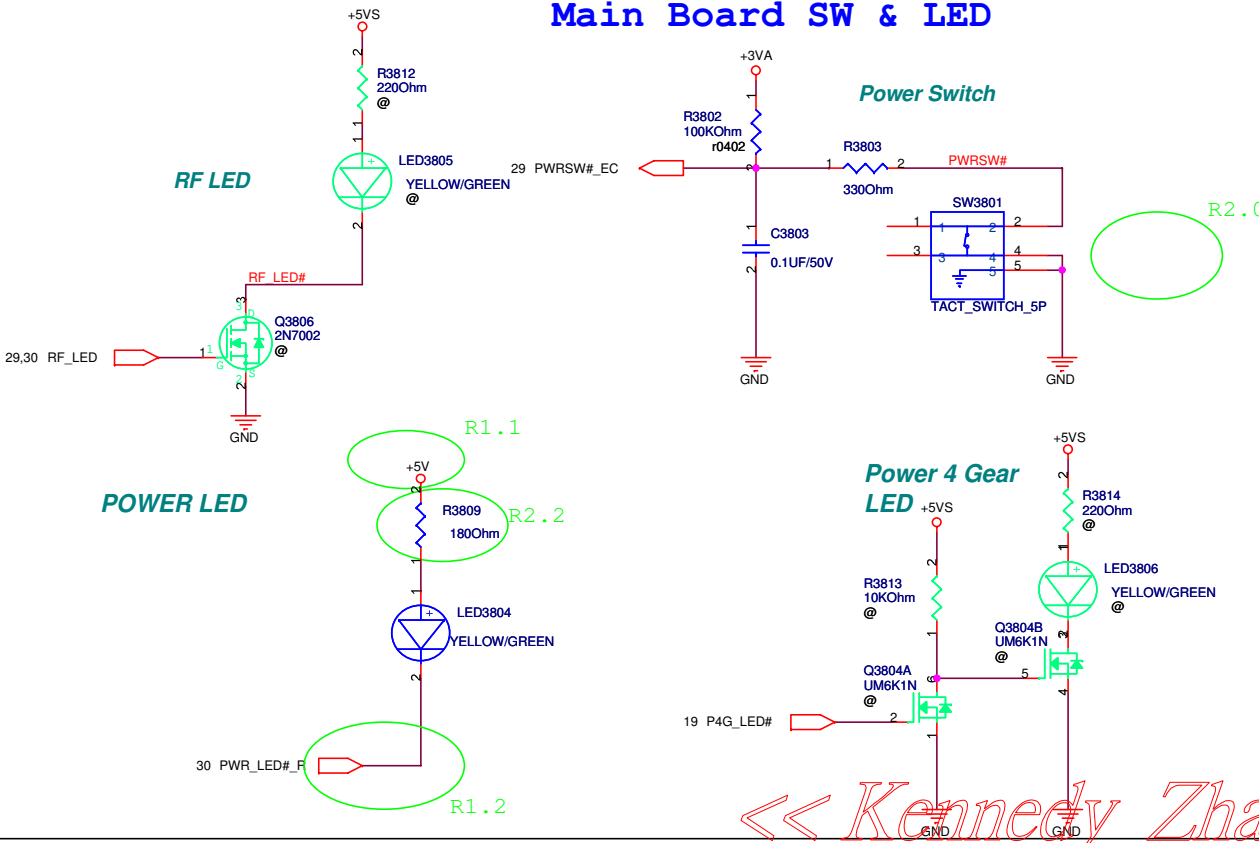




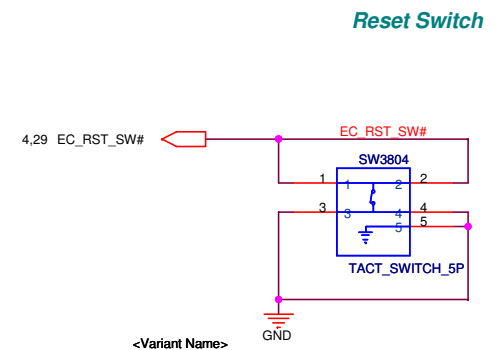
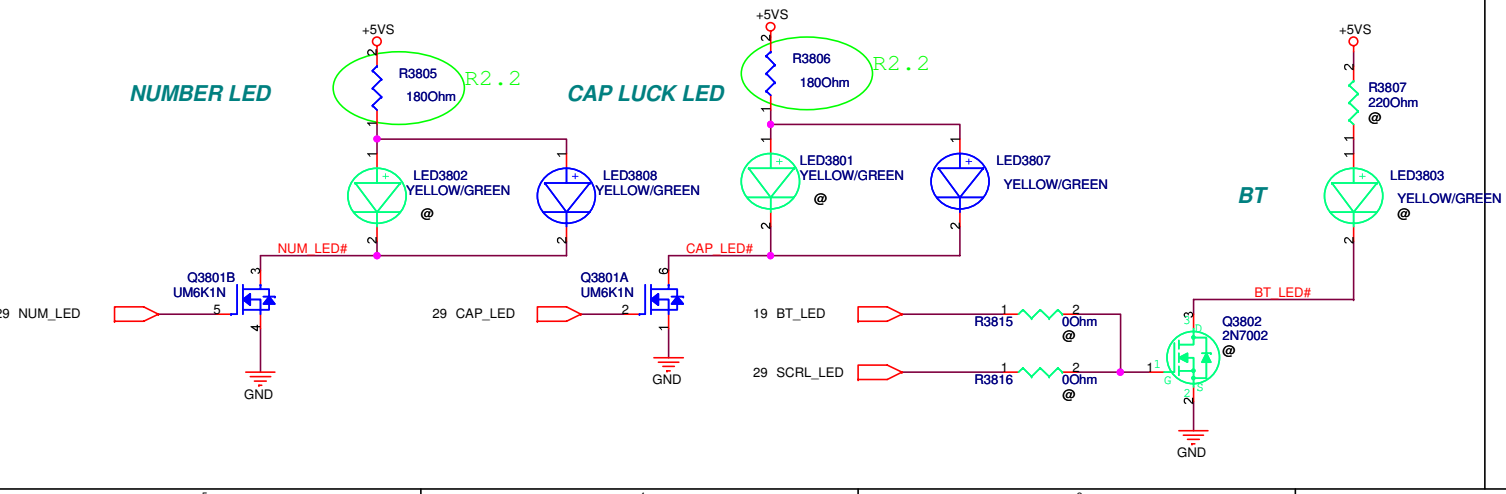
<Variant Name>

ASUS		Title : Discharge Circuit	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name		Rev
A4	T12F		
Date: 星期二, 五月 15, 2007		Sheet	37 of 61

Main Board SW & LED

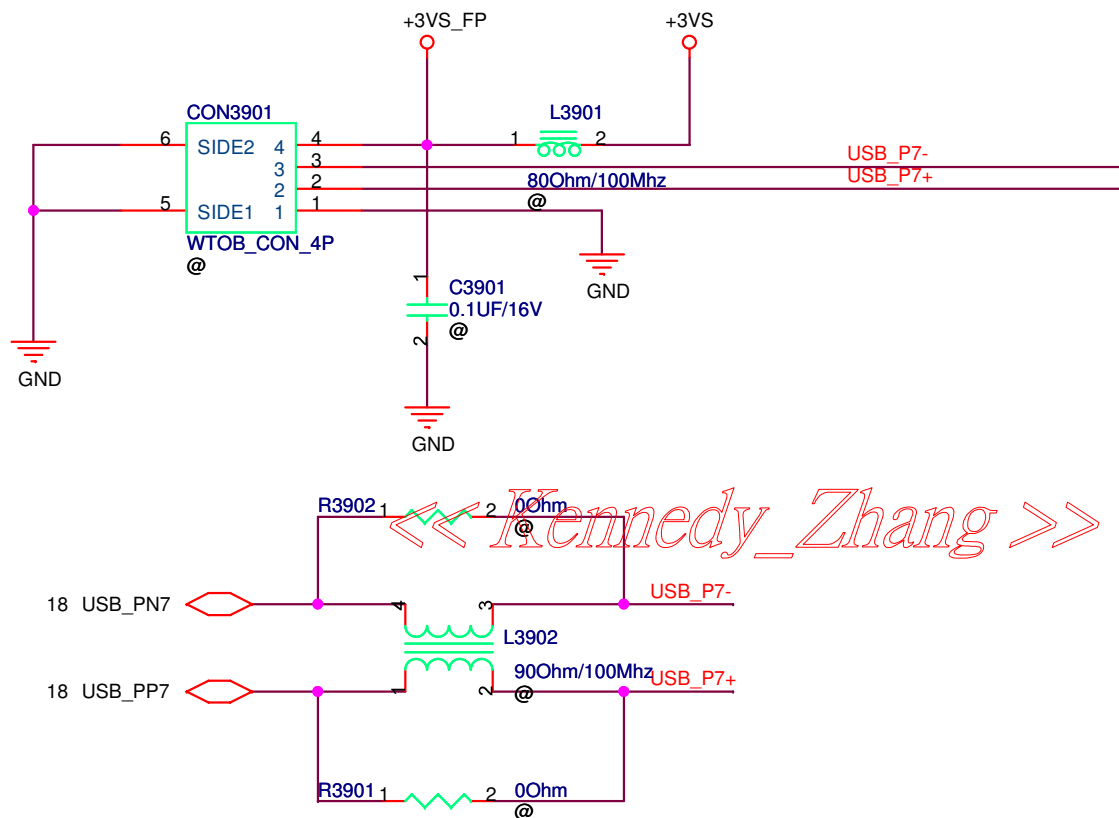


<< Kennedy_Zhang >>



<Variant Name>

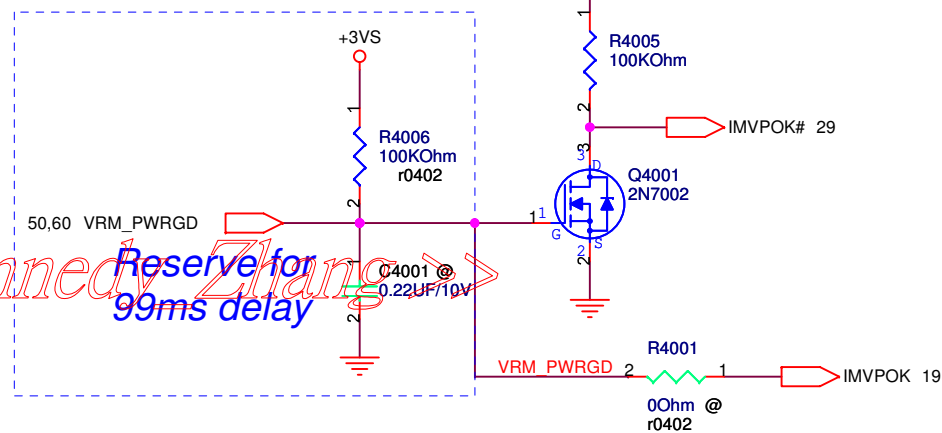
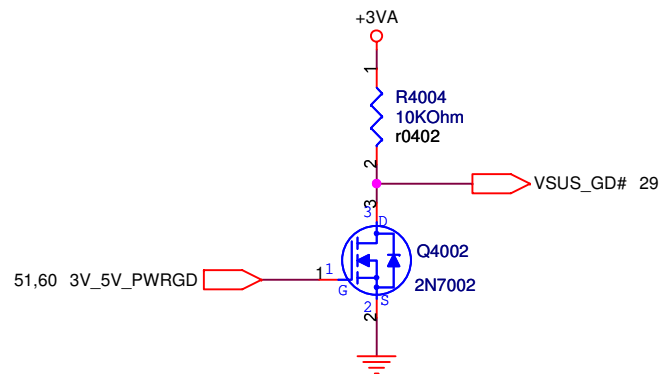
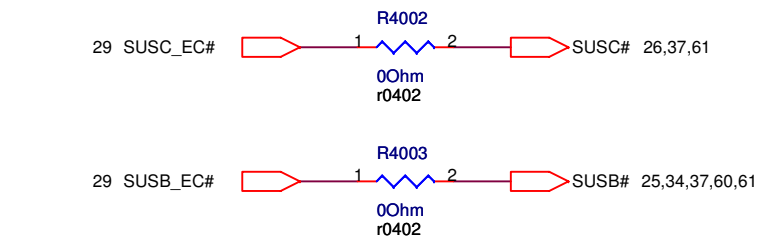
ASUS		Title :SW/LED	
ASUSTek COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
B	T12F		
Date: 星期五, 五月 18, 2007	Sheet 38 of 61		



<< Kennedy_Zhang >>

<Variant Name>

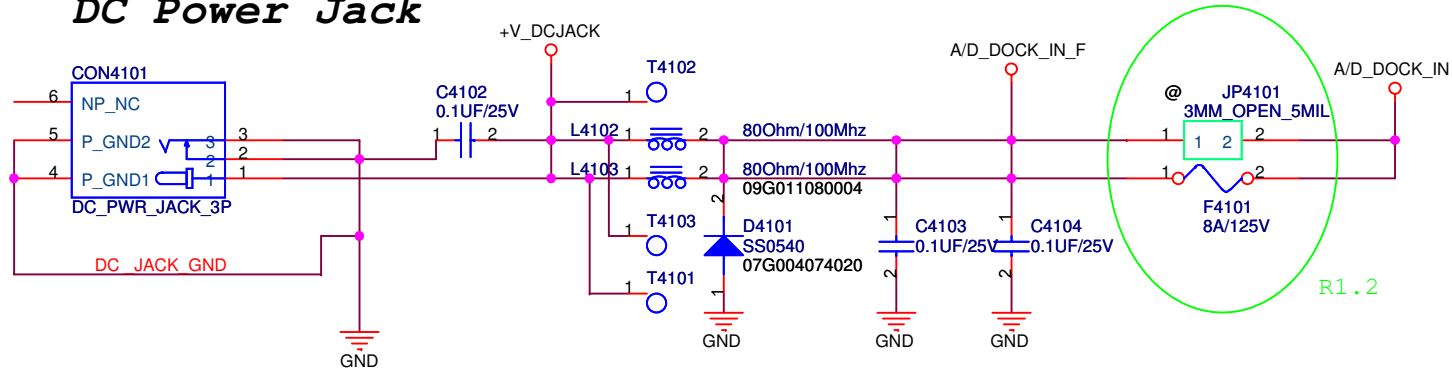
		Title : FINGER PRINT	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size A	Project Name T12F		Rev
Date: 星期二, 五月 15, 2007		Sheet 39 of 61	



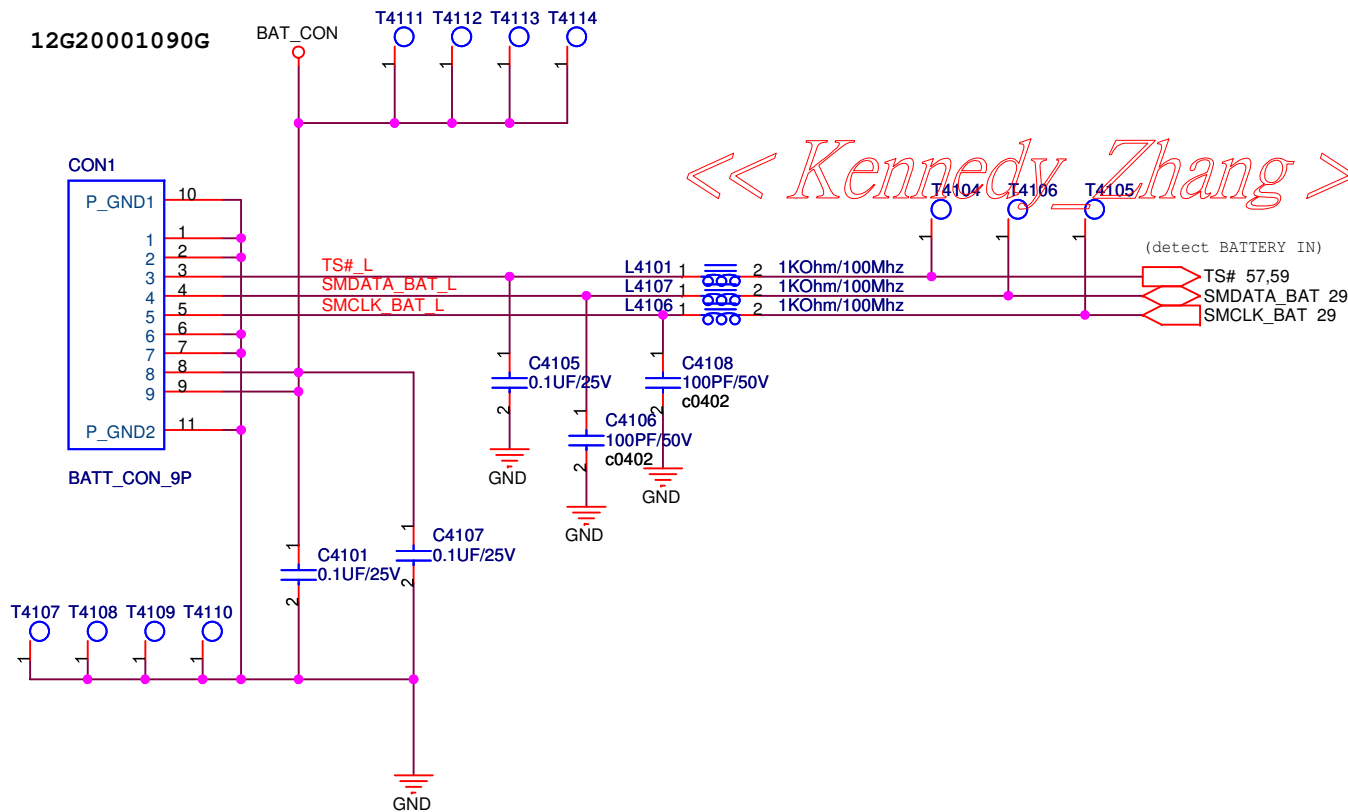
<Variant Name>

ASUS		Title : POWER-ON SEQ.	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size A4	Project Name T12F	Rev	
Date: 星期二, 五月 15, 2007		Sheet 40 of 61	

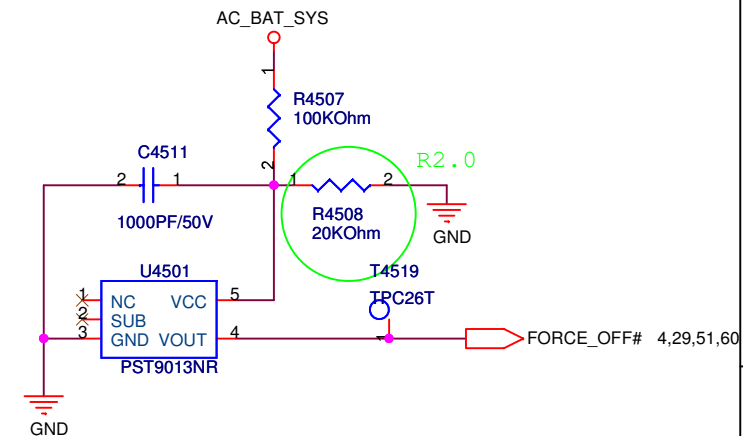
DC Power Jack



12G20001090G

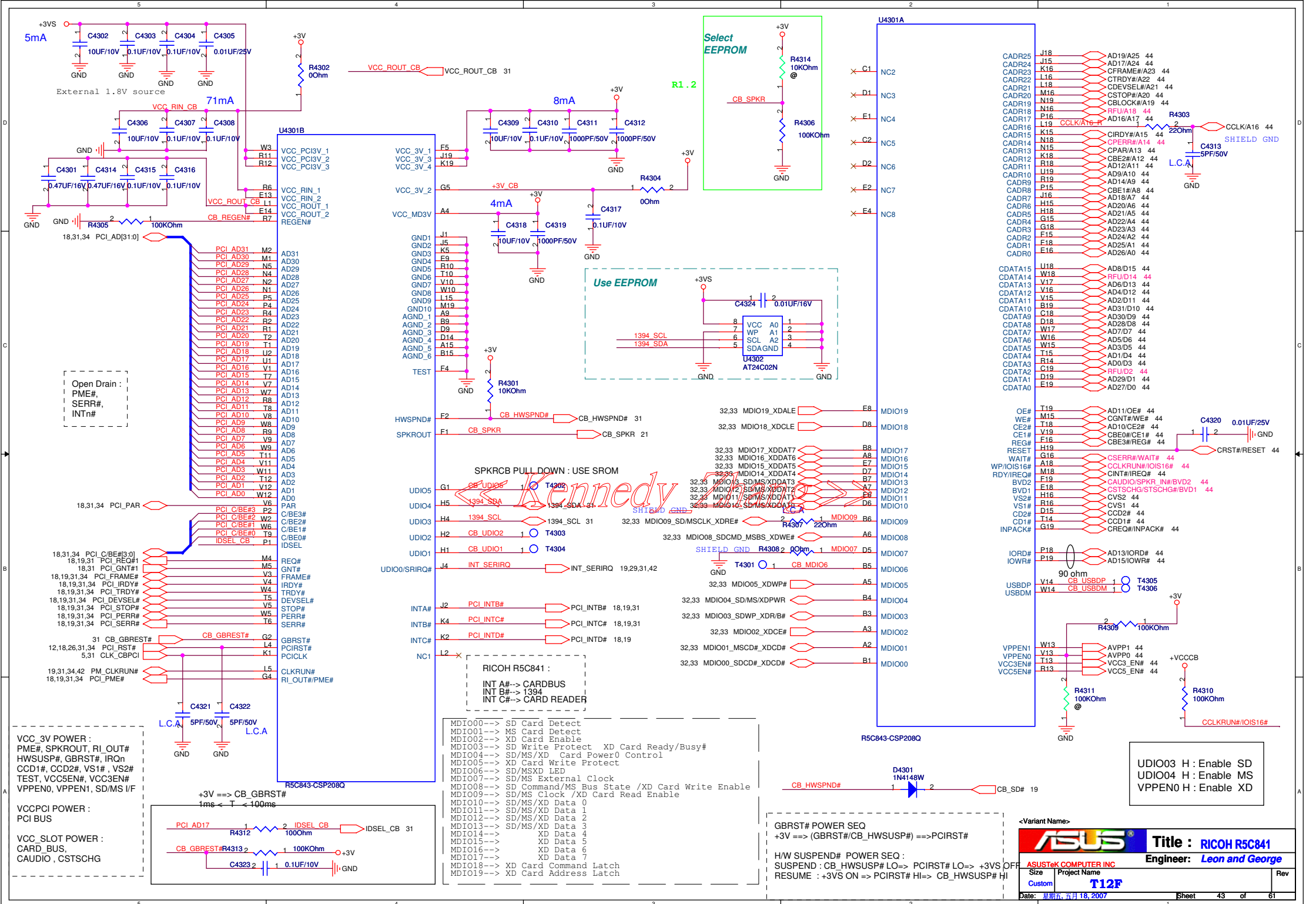


Without Battery & Pull out Adapter

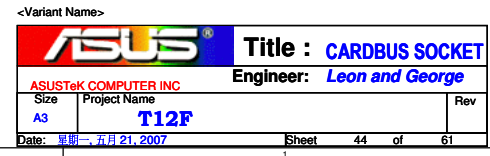


<Variant Name>

ASUS		Title : DC/ BATT IN	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size A4	Project Name T12F	Rev	
Date: 星期二, 五月 15, 2007	Sheet	41	of 61



CCD1#	CCD2#	
L	L	16bit
OTHER		32bit



5



3



2



100



100



3



100



R1.1

Page	Action	Reason
5	Add R566,R567,R568,R569 to divide voltage.	Clock GEN output voltage is too high.
17	Add R1733~R1737 (Reserve)	For EMI request
17	Add R1729~R1732	Add MDC feature
22	Change C2222 from 0.1uF to 0.47uF	Delay the HP turn-on timing to avoid noise at the system power on.
22	Add R2233 and L2202 to link the different GND	For EMI request
26	Add CON2603	Only use for debug, it will be deleted before MP
31	Add C3101~C3103	Reduce power rippler of R5C832
31	Add R3103	UDIO5 pull high to disable external EEPROM
35	Add CON3203 and MDC relative circuit	Add MDC feature
38	Change power LED power from +5VS to +5V	Slove LED can't flash in S3

R1.2

Page	Action	Reason
4	Add U402 and relative circuit.	Add hardware thermal protection circuit
12	Change L1204,L1205,C1209,1210	For EMI request
12	Change L1210 to 1k ohm	Reduce leakage current.
13	Change L1304~L1306 to 150nH and C1308 C1310 C1312 change to 10pF	Improve CRT signal
21	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
22	All R1.2 modification in this page	Follow ADI recommend vlaue to get Vista logo.
23	All R1.2 modification in this page	Improve microphone quality
30	Add R3022	Reserve RF_LED feature
38	Del Q3005 and link PWR_LED#_R to LED directly	Cost down
41	Add F4101 and JP4101	Reserve, normal use JP4101
43	Add R4314	Reserve, normal no use

R2.0

Page	Action	Reason
5	Change C516,C517 value	Tune up accuracy of 14.318MHZ.
17	Change C1702,C1703 value	Tune up accuracy of 32.768KHz.
21	Add R2111 to pull high	Avoid input pin NC.
29	Change C2911,C2915 value	Tune up accuracy of 32.768KHz.
36	Modify Q3601 circuit	Solve system will auto turn-on when remove USB HDD with external power.
38	Add C3804	For ESD request
41	Change R4508 from 16.9K to 20K ohm	Solve shutdown issue when plug-in AC jack in low battery mode.
10	Add CE1003	Reduce power rippler of +1.8V

R2.2

Page	Action	Reason
29	Add R2918 and change C2910 to 0.1uF	Solve CMOS clear issue.
33	Add C3306	Solve Type-H XD can't work normally.
38	Change R3805,R3806,R3809 to 180ohm(1/10W)	Improve Derating

R2.3

Page	Action	Reason
33	Change CON3301 to ALPS	Prevent card from being shaved by connector

<< Kennedy_Zhang >>

<Variant Name>

**ASUSTeK COMPUTER INC**

Title : HISTORY
Engineer: Leon and George

Size A3	Project Name T12F	Rev
Date: 星期二, 五月 15, 2007		Sheet 46 of 61

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM		48	GPH0	VSUS_ON	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/		55	GPH2	IMVPOK#	I
37	PWM3/GPA3	/		69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#		76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH7_PWROK	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCH_DOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GPI3	CHG_EN#	O
164	SMDAT0/GPB4	SMDATA_BAT	I/O	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RC_IN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O				
				8	GPL0	WLAN_ON#	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	11	GPL1	BT_ON#	O
170	SMDAT1/GPC2	SMB1_DAT	I/O	12	GPL2	RF_OFF_SW#	I
171	GPC3	/		20	GPL3	RF_LED	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	92	CRX	CRX	I/O
175	GPC5	OP_SD#	O				
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RI1#/WUI0/GPD0	PM_SUSB#	I				
29	RI2#/WUI1/GPD1	PM_SUSC#	I				
30	LPCRST#/WUI4//GPD2	PLT_RST#	I				
31	ECSCI#/GPD3	EXT_SCI#	O				
41	GPD4	/	I				
42	GINT/GPD5	/					
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#	I				
88	ADC5/GPE1	/	I				
89	ADC6/GPE2	MARATHON#	I				
90	ADC7/GPE3	DISTP_SW#	I				
2	PWRSW/GPE4	PWRSW#_EC	I				
44	WUI5/GPE5	/					
24	LPCPD#/WUI6/GPE6	LID_EC#	I				
25	CLKRUN#/WUI7/GPE7	/	O				
110	PS2CLK0/GPF0	/					
111	PS2DAT0/GPF1	/					
114	PS2CLK1/GPF2	/	I/O				
115	PS2DAT1/GPF3	/	I/O				
116	PS2CLK2/GPF4	TP_CLK					
117	PS2DAT2/GPF5	TP_DAT					
118	PS2CLK3/GPF6	PWRLMT#					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSPLVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	O
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUWVRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIe Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<< Kennedy Zhang >>

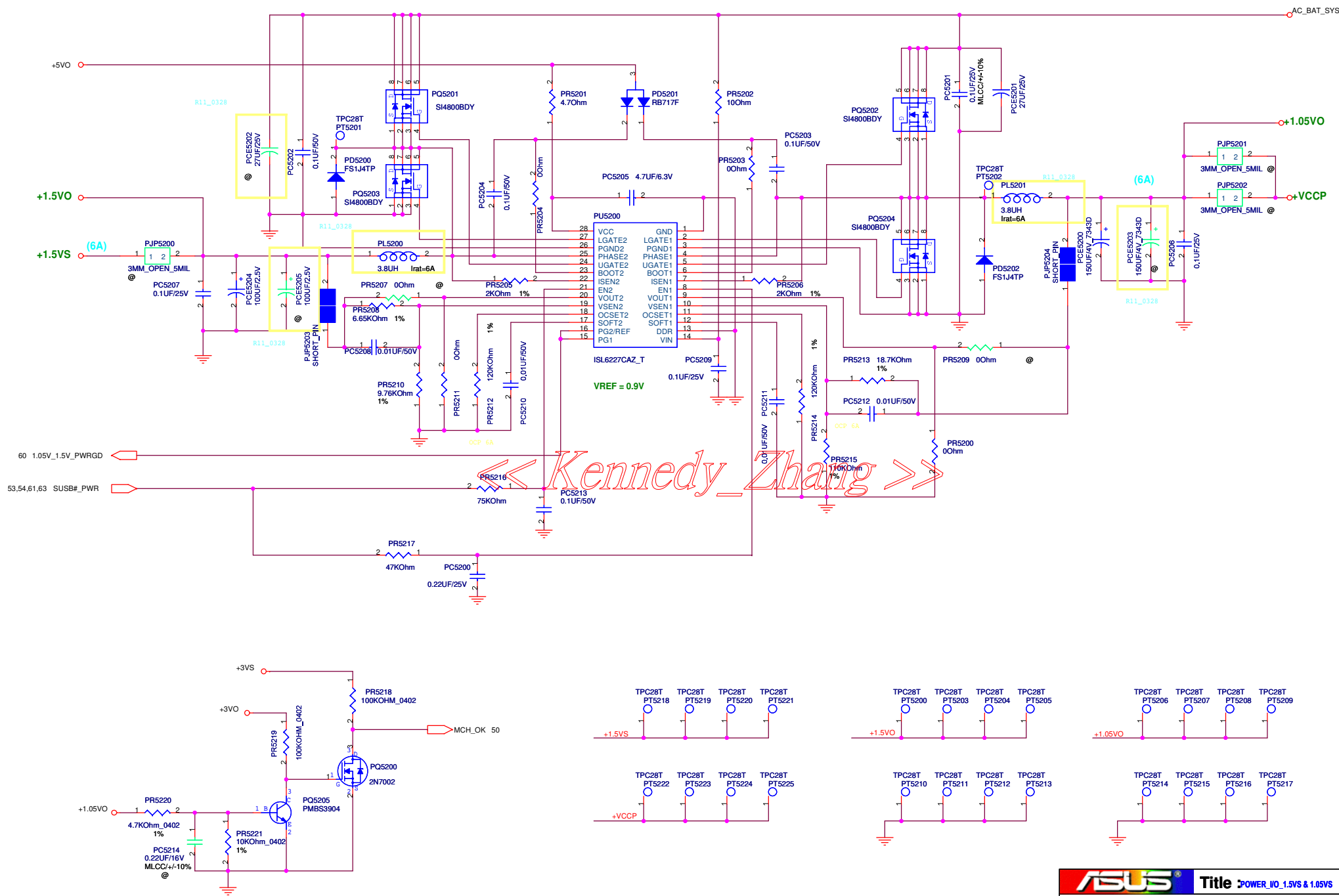
<Variant Name>

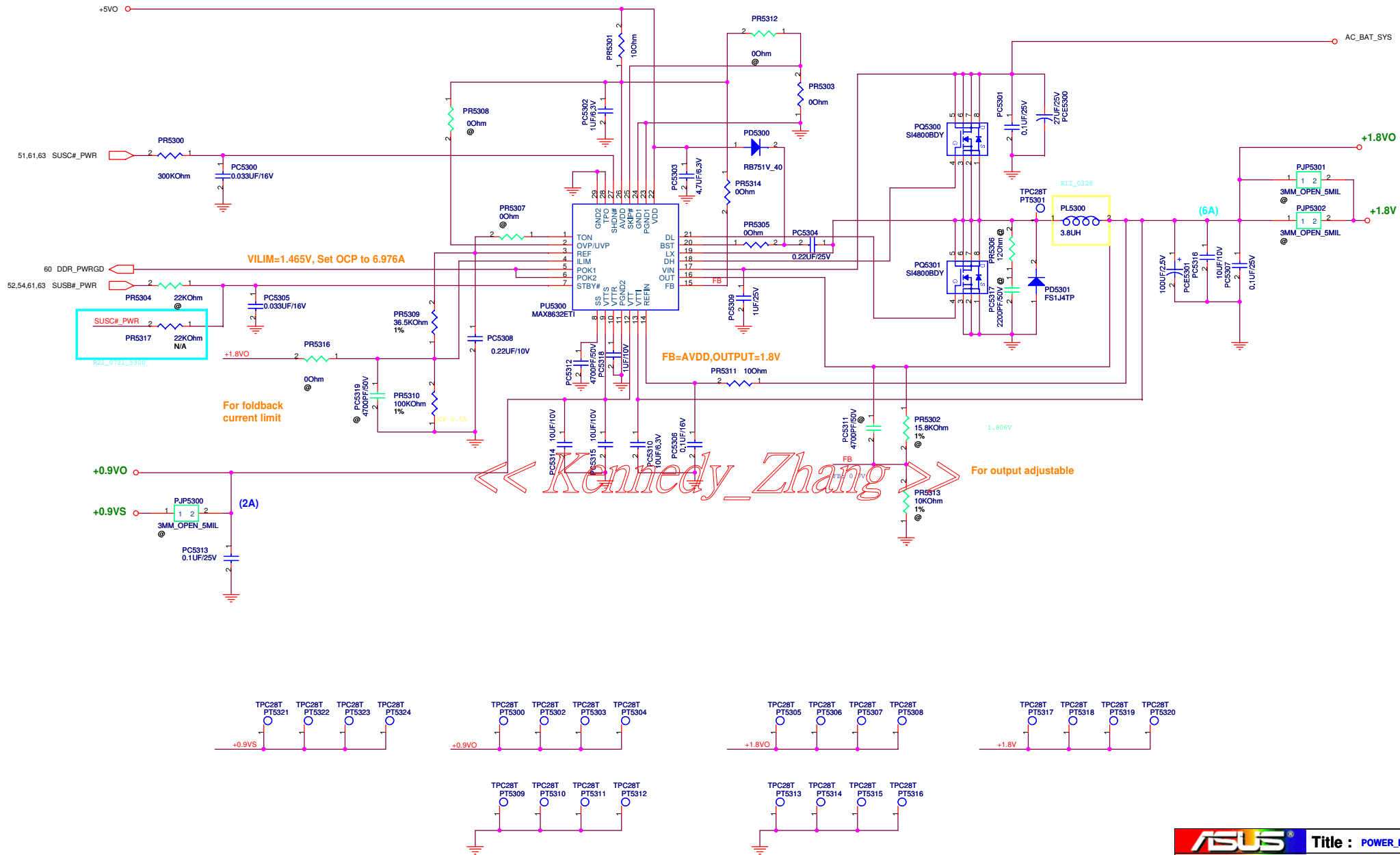
		Title : GPIO Setting	
ASUSTeK COMPUTER INC		Engineer: Leon and George	
Size	Project Name	Rev	
Custom	T12F		
Date: 2007.05.15		Sheet	48 of 61

<< Kennedy_Zhang >>

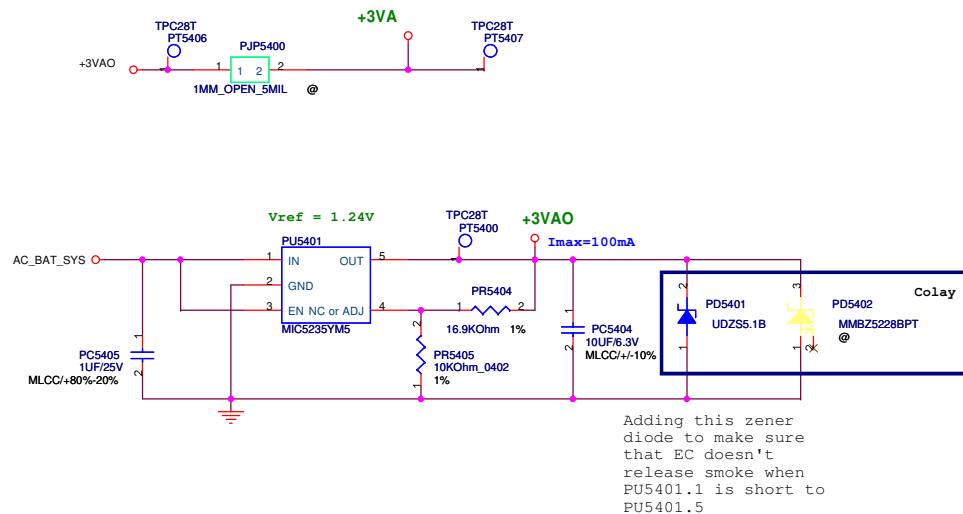
<Variant Name>		
		Title : N/A
ASUSTeK COMPUTER INC		Engineer: Leon and George
Size	Project Name	Rev
Custom	T12F	
Date: 星期五, 五月 15, 2007		Sheet 49 of 61





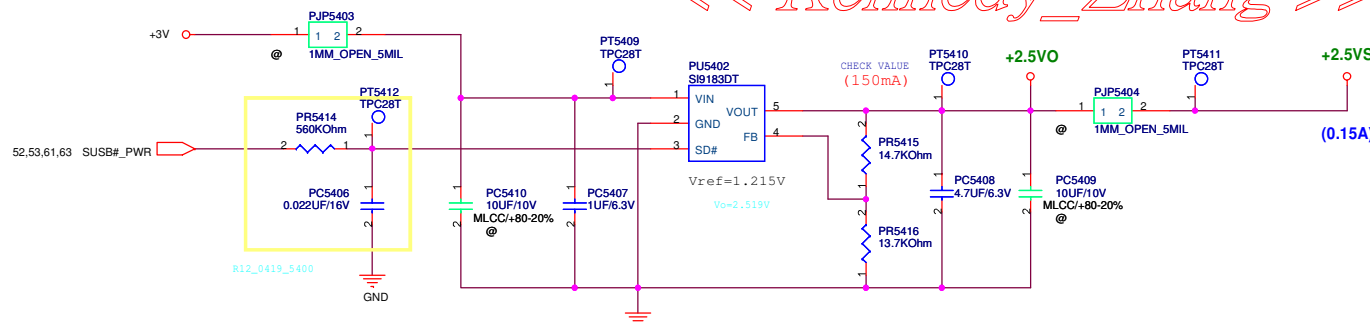


+3VAO

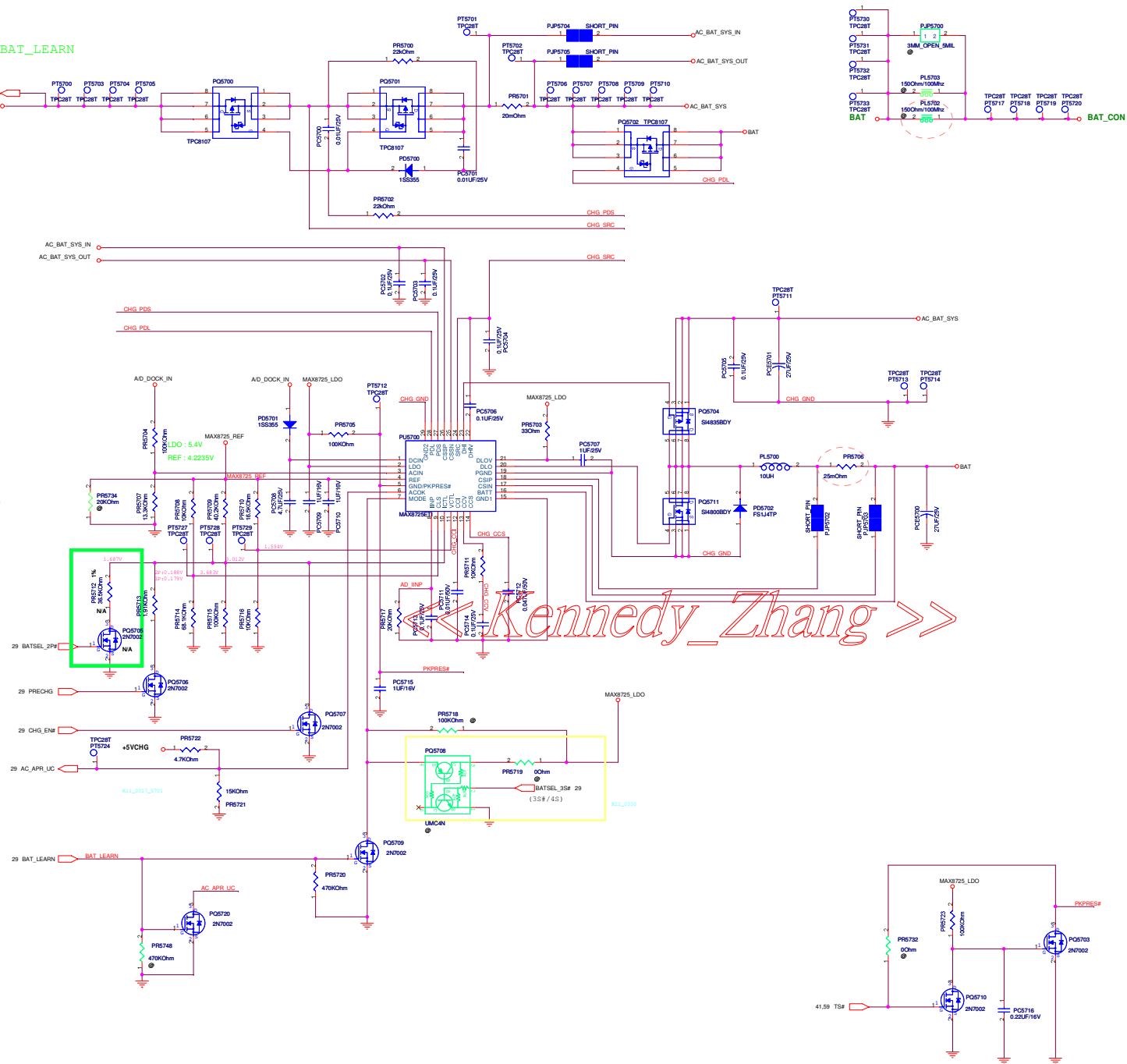


+2.5VS

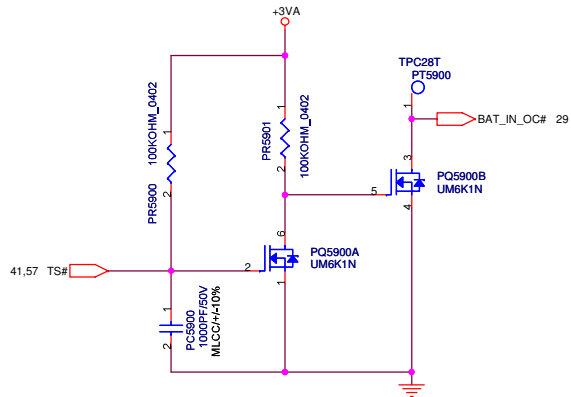
<< Kennedy_Zhang >>



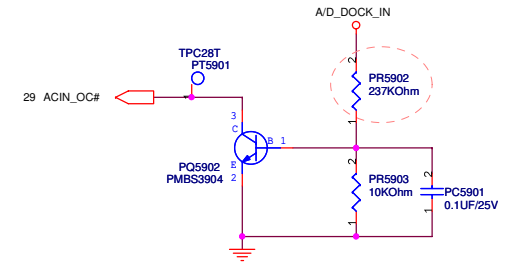
POWER PATH & BAT_LEARN



BATTERY IN DETECT

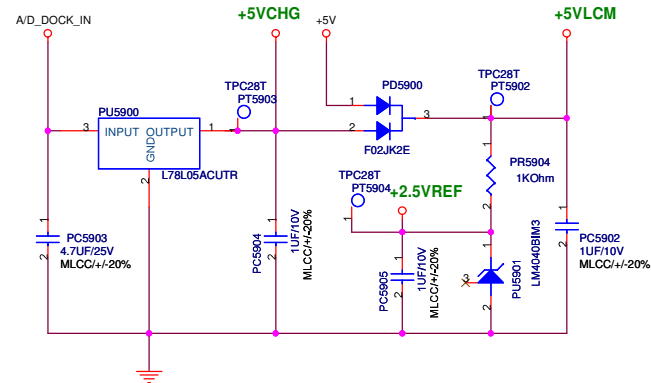


ADAPTER IN DETECT

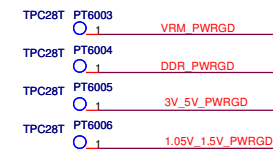


<< Kennedy_Zhang >>

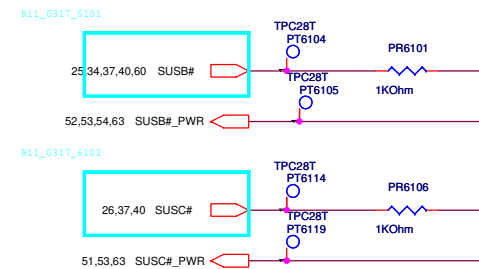
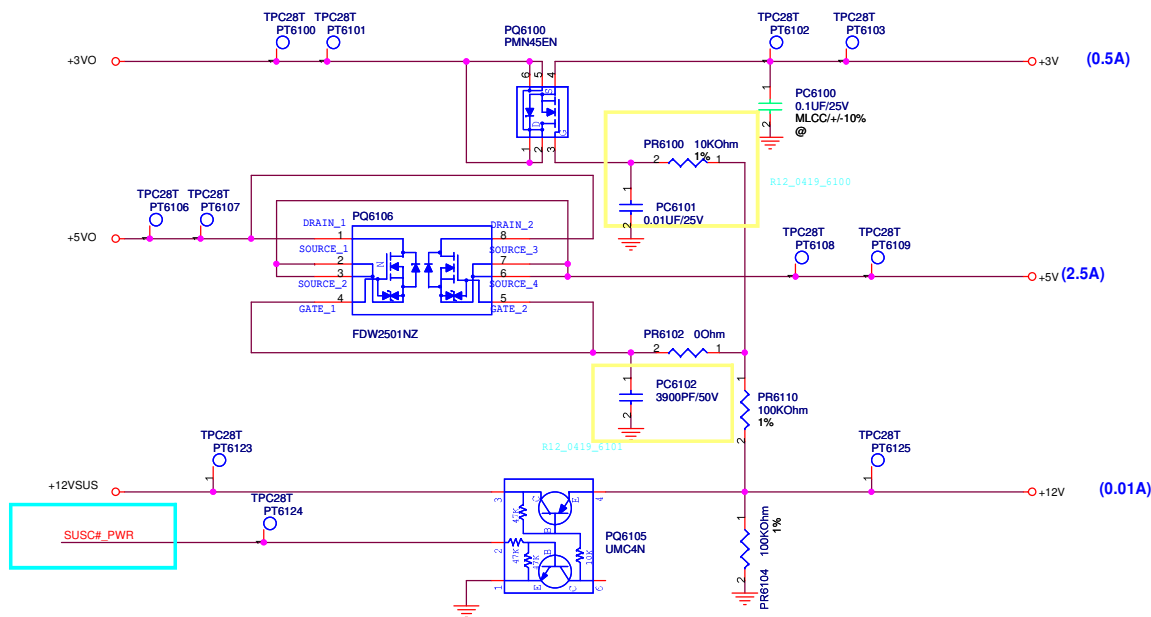
+5VLCM, +5VCHG & +2.5VREF



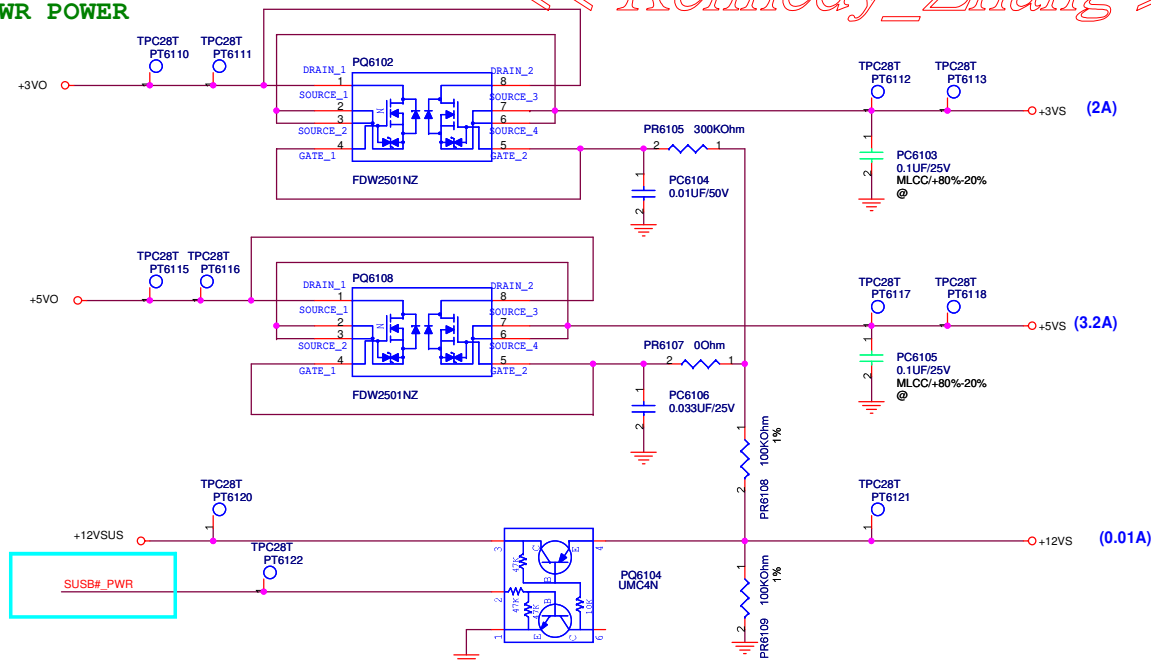
POWER GOOD DETECTOR



SUSC#_PWR POWER



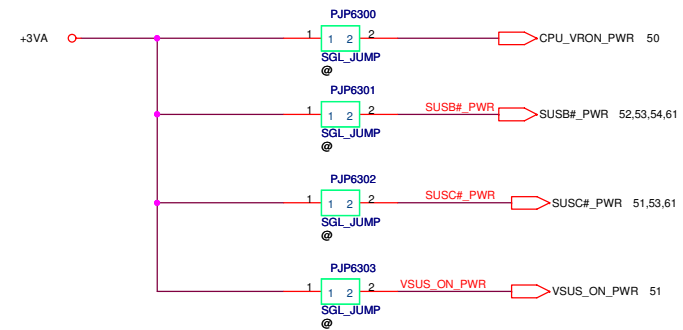
SUSB#_PWR POWER



<< Kennedy_Zhang >>



FOR POWER TEST



<< Kennedy_Zhang >>

