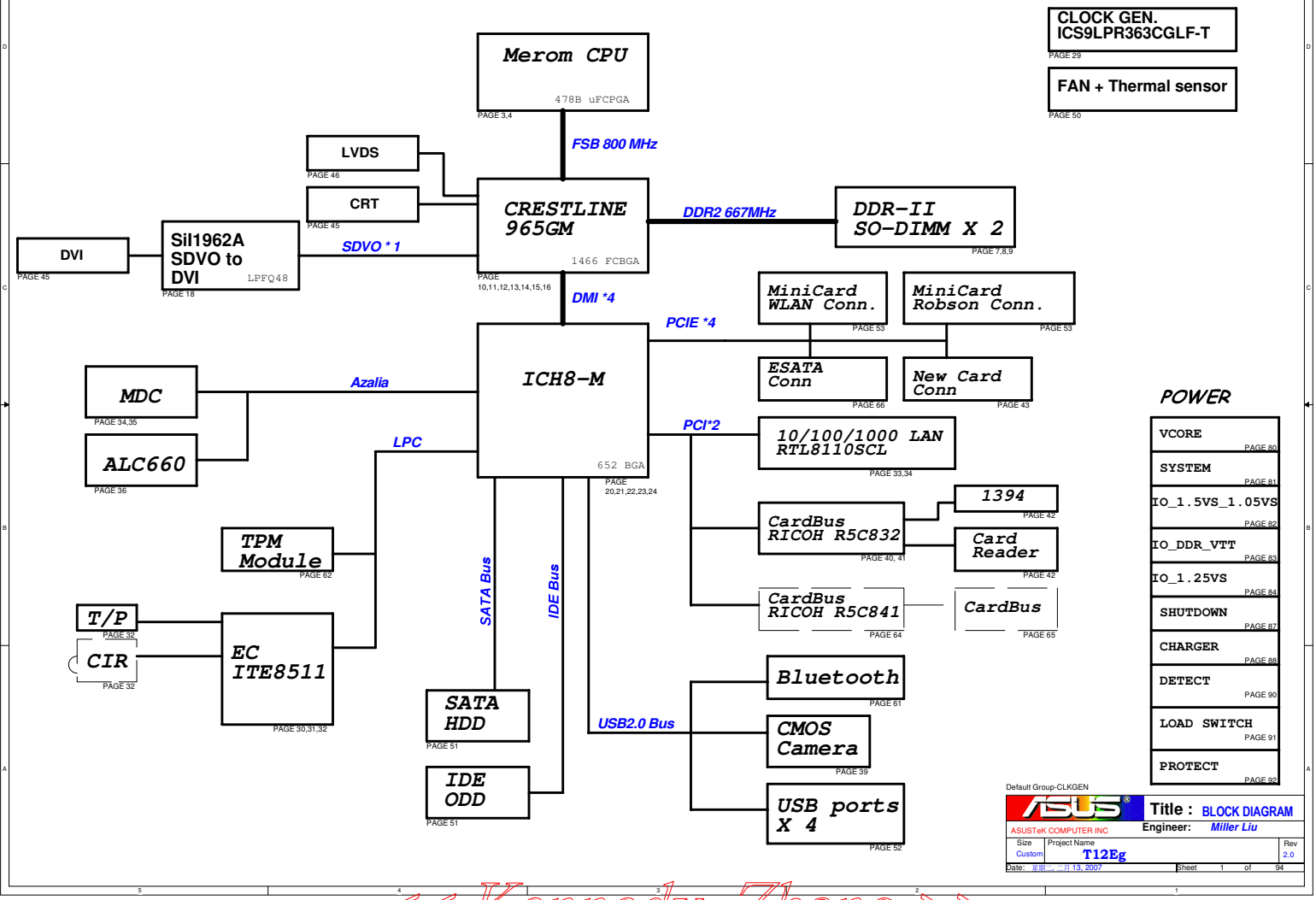
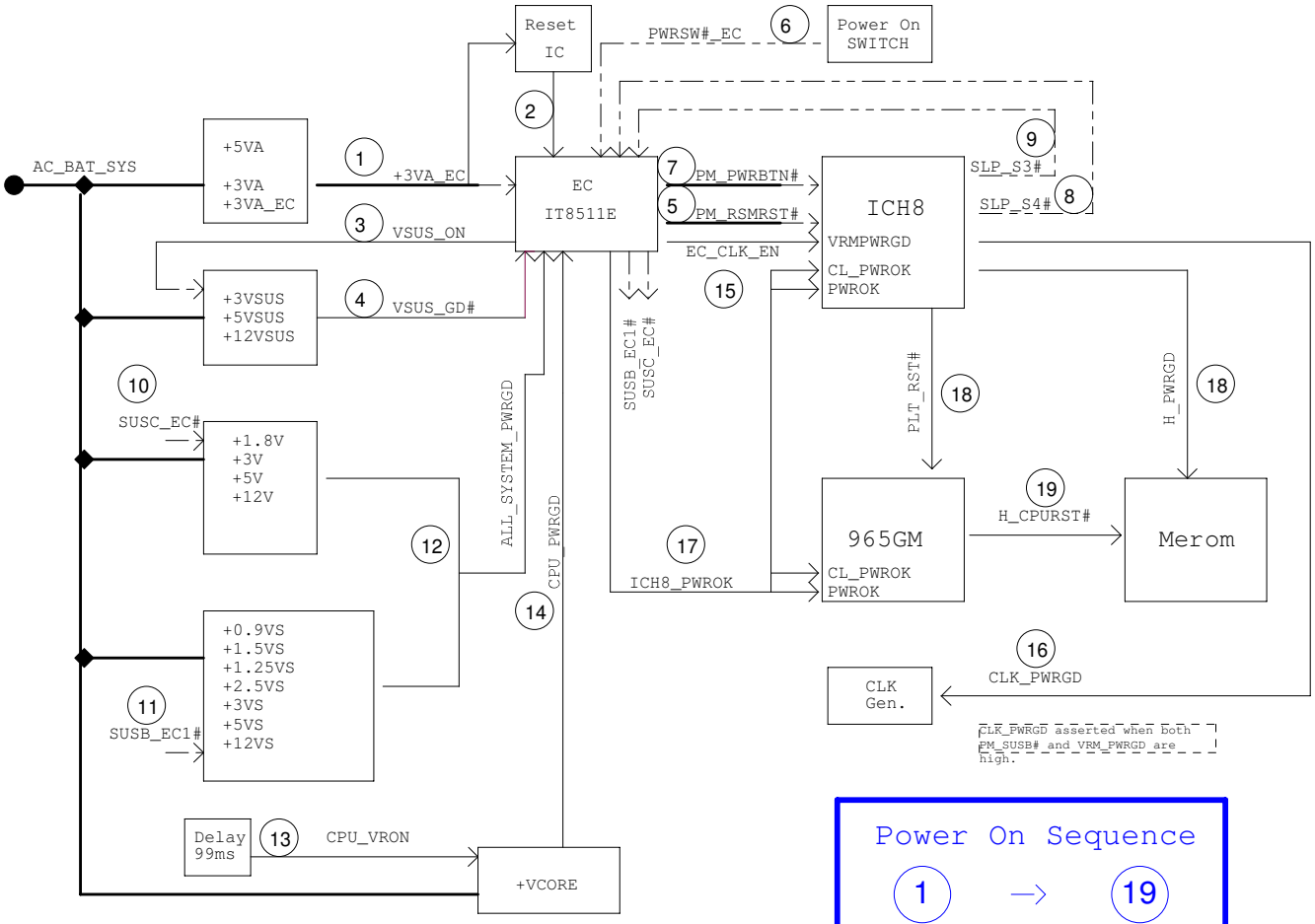
T12Eg Main BD. R2.0 BLOCK DIAGRAM





Default Group-CLKGEN

ASUSTeK COMPUTER INC

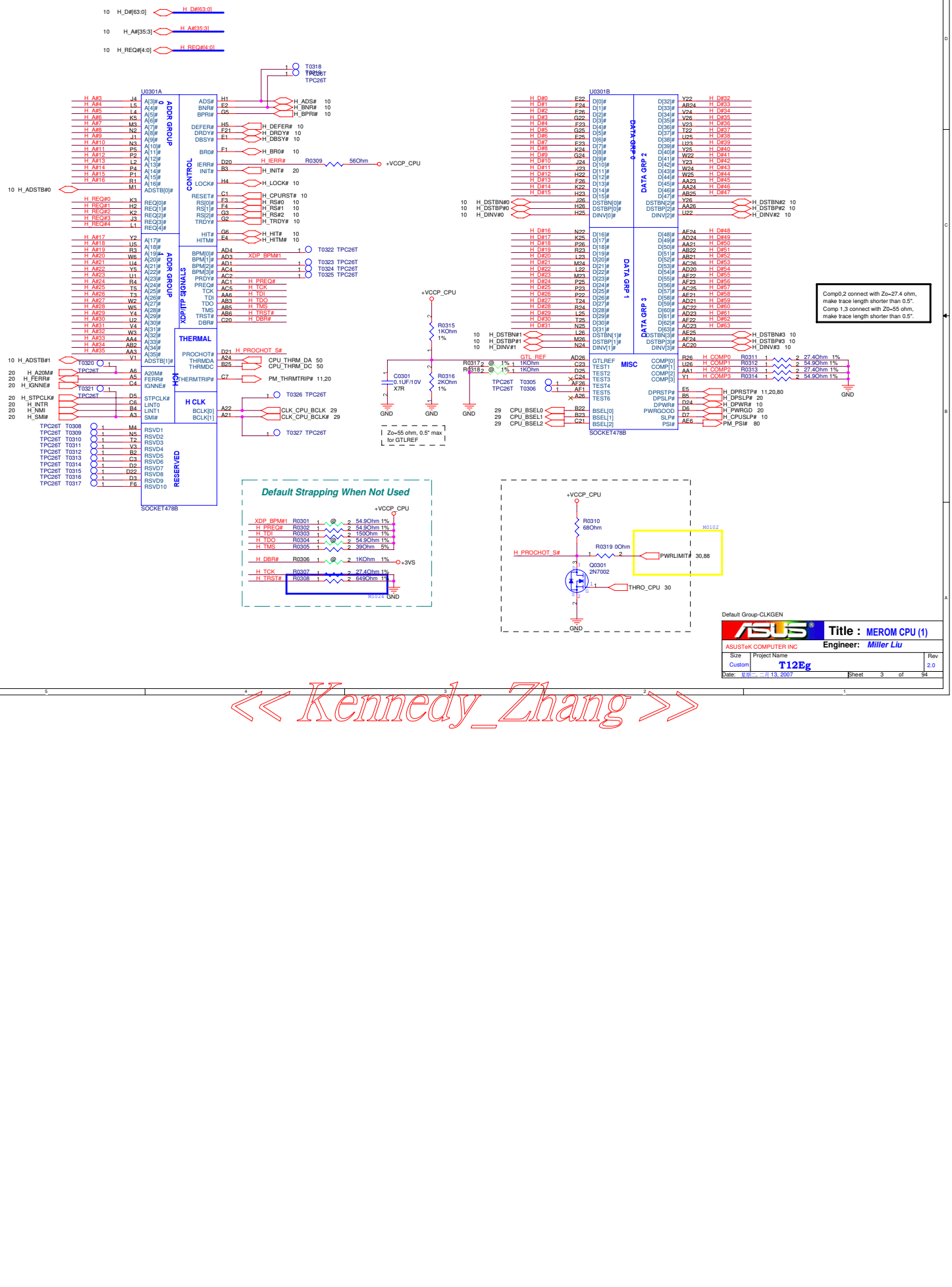
Title : PowerOn sequence

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 2 of 94

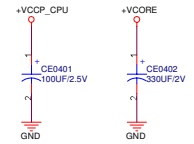
<< Kennedy_Zhang >>

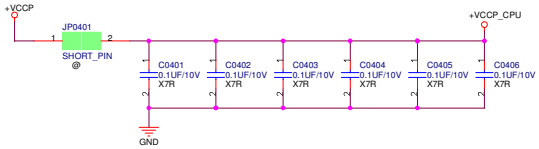


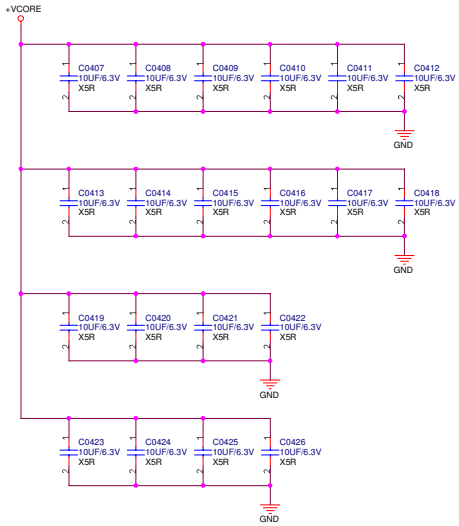
Decoupling guide from INTEL

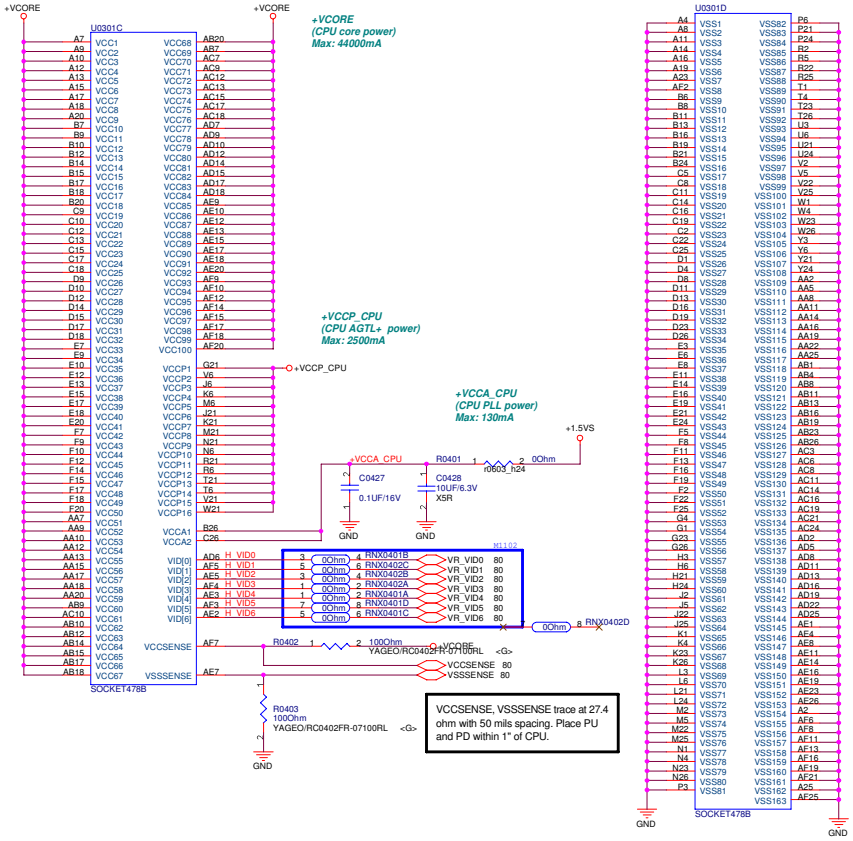
VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)









Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 4 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: *Miller Liu*

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 5 of 94

Default Group-CLKGEN

Title : NULL

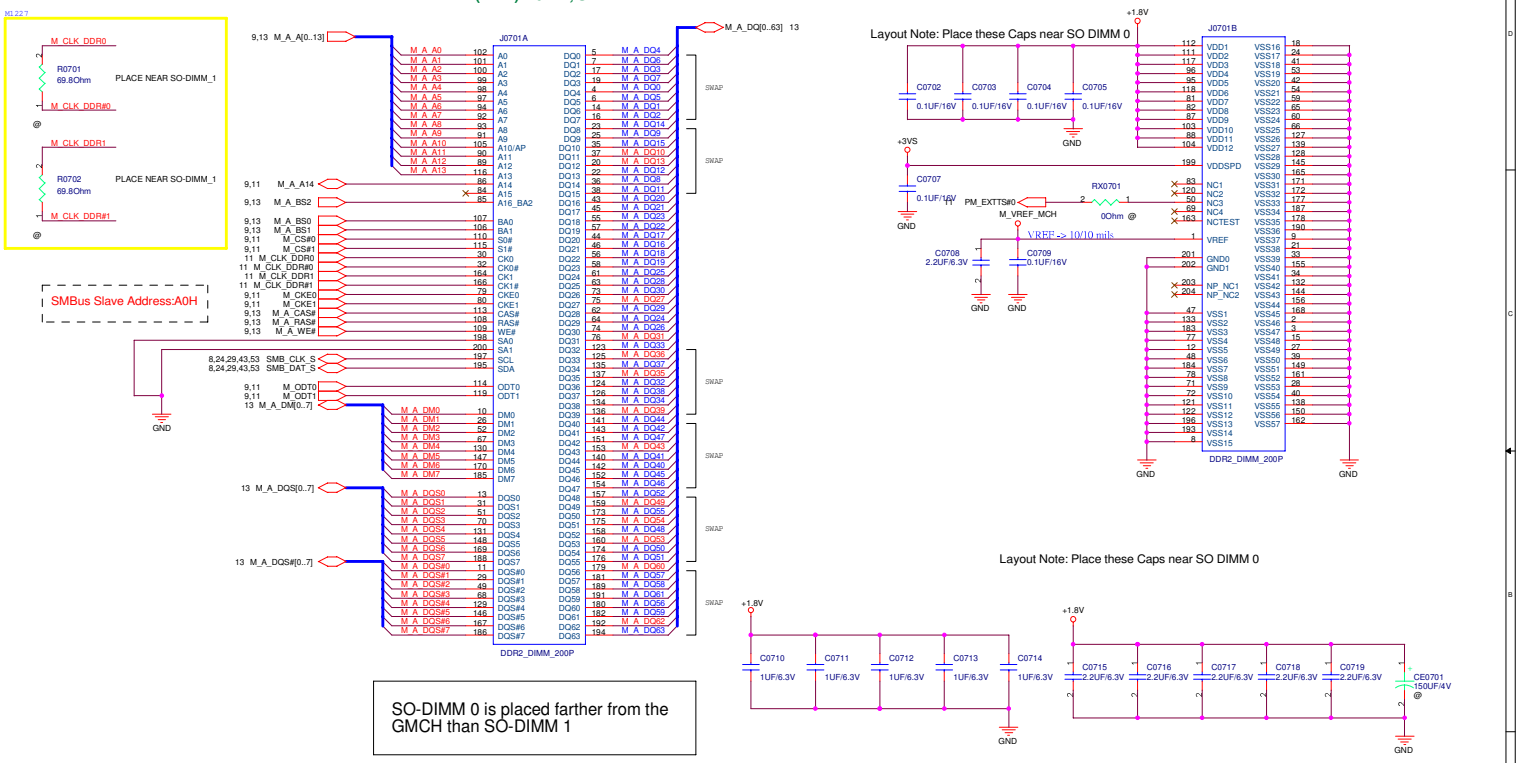
ASUSTeK COMPUTER INC

Engineer: *Miller Liu*

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 6 of 94

P/N: 12G025022004
(T12F) 4.0mm, STD



Default Group-CLKGEN

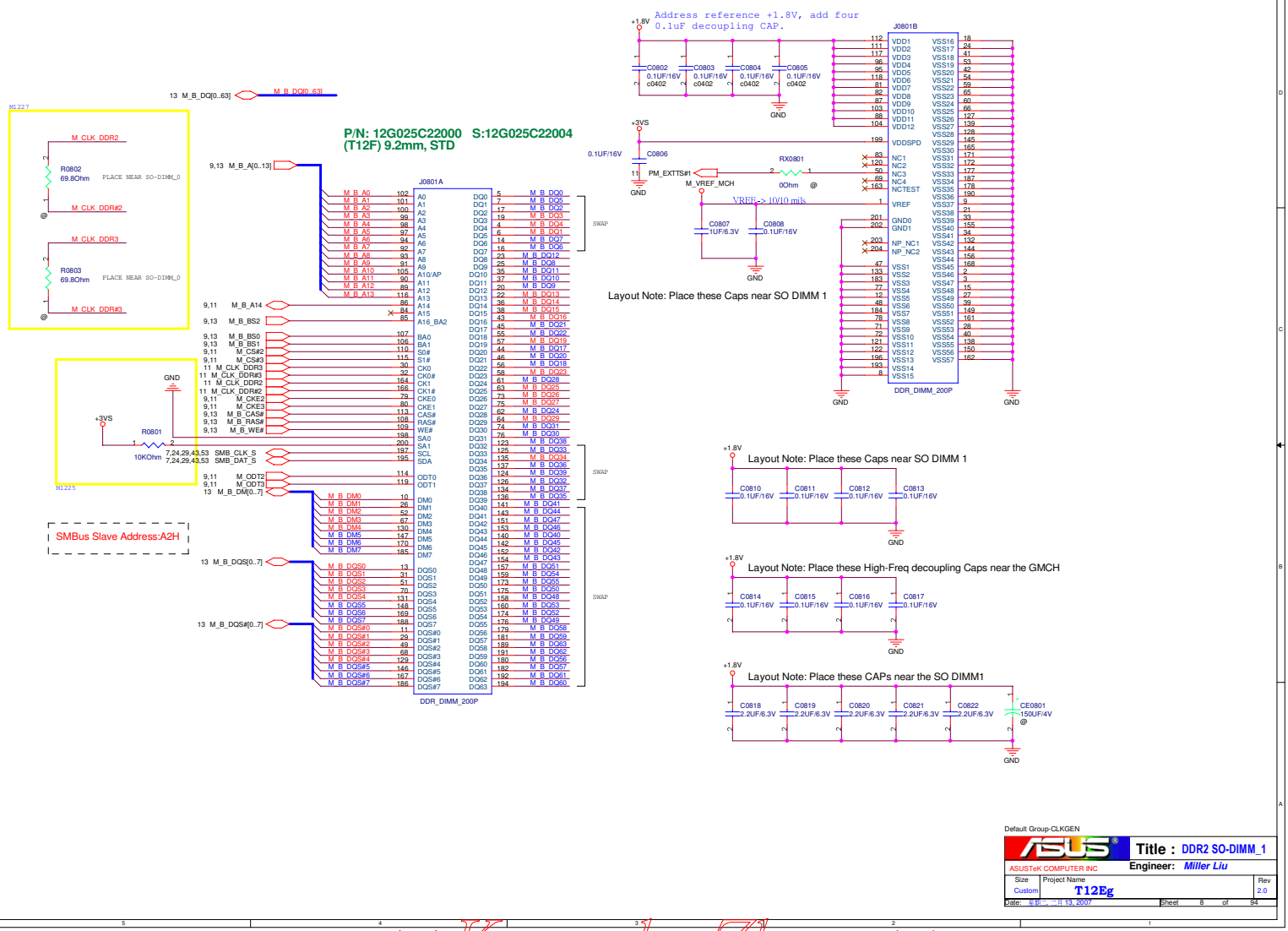
ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM_0

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 日期二, 一月 13, 2007 Sheet 7 of 94



Default Group-CLKGEN

Title :	DDR2 SO-DIMM_1
ASUSTeK COMPUTER INC	Engineer: Miller Liu
Size: Custom	Project Name: T12Eg
Rev: 2.0	
Date: 十月二十日 13, 2007	Sheet 8 of 94

<< Kennedy_Zhang >>

M_VREF_MCH
+0.9VS

M_VREF_MCH 7,8,11
+0.9VS 83

+0.9VS

M1114

RN0901A M_CKE3
RN0901B M_CKE2
RN0901C M_B_BS2
RN0901D M_B_A11
RN0901E M_B_A7
RN0901F
RN0901G M_B_A6
RN0901H M_B_A2

RN0902A M_B_A4
RN0902B M_B_BS1
RN0902C M_B_A0
RN0902D M_B_RAS#
RN0902E
RN0902F M_CS#2
RN0902G M_ODT2
RN0902H M_B_A13

RN0903A M_B_A12
RN0903B M_B_A9
RN0903C M_B_A8
RN0903D M_B_A5
RN0903E M_B_A3
RN0903F M_B_A1
RN0903G M_B_A10
RN0903H M_B_BS0

RN0904A M_B_WE#
RN0904B M_B_CAS#
RN0904C M_CS#3
RN0904D M_ODT3

RN0905A M_CKE0
RN0905B M_A_BS2
RN0905C M_A_A12
RN0905D M_A_A9
RN0905E M_A_A8
RN0905F M_CKE1
RN0905G M_A_A11
RN0905H

RN0906A M_A_A5
RN0906B M_A_A3
RN0906C M_A_A2
RN0906D M_A_A7
RN0906E M_A_A4
RN0906F M_A_A6
RN0906G M_A_A1
RN0906H M_A_A10

RN0907A M_A_BS0
RN0907B M_A_WE#
RN0907C M_A_A0
RN0907D M_A_BS1
RN0907E M_A_A13
RN0907F M_ODT0
RN0907G
RN0907H M_CS#0

RN0908A M_A_RAS#
RN0908B M_A_CAS#
RN0908C M_CS#1
RN0908D M_ODT1

56Ohm

M_B_A14 8,11

M_A_A14 7,11

M_A_A[0..13] 7,13
M_A_BS[0..2] 7,13
M_A_CAS# 7,13
M_A_RAS# 7,13
M_A_WE# 7,13

M_B_A[0..13] 8,13
M_B_BS[0..2] 8,13
M_B_CAS# 8,13
M_B_RAS# 8,13
M_B_WE# 8,13

M_CS#[0..3] 7,8,11
M_ODT[0..3] 7,8,11
M_CKE[0..3] 7,8,11

+1.8V

R0901
10KOhm
1%
@

83 0.9V_VTT_REF
R0903 0Ohm

R0902
10KOhm
1%
@

C0928
0.1UF/16V
@

M_VREF_MCH

GND

+0.9VS

C0901 C0902 C0903 C0904 C0905 C0906 C0907 C0908 C0909 C0910 C0911 C0912 C0913
c0402 0.1UF/10V

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+0.9VS

C0914 C0915 C0916 C0917 C0918 C0919 C0920 C0921 C0922 C0923 C0924 C0925 C0926
c0402 0.1UF/10V

GND

Default Group-CLKGEN

Title : DDR2 TERM

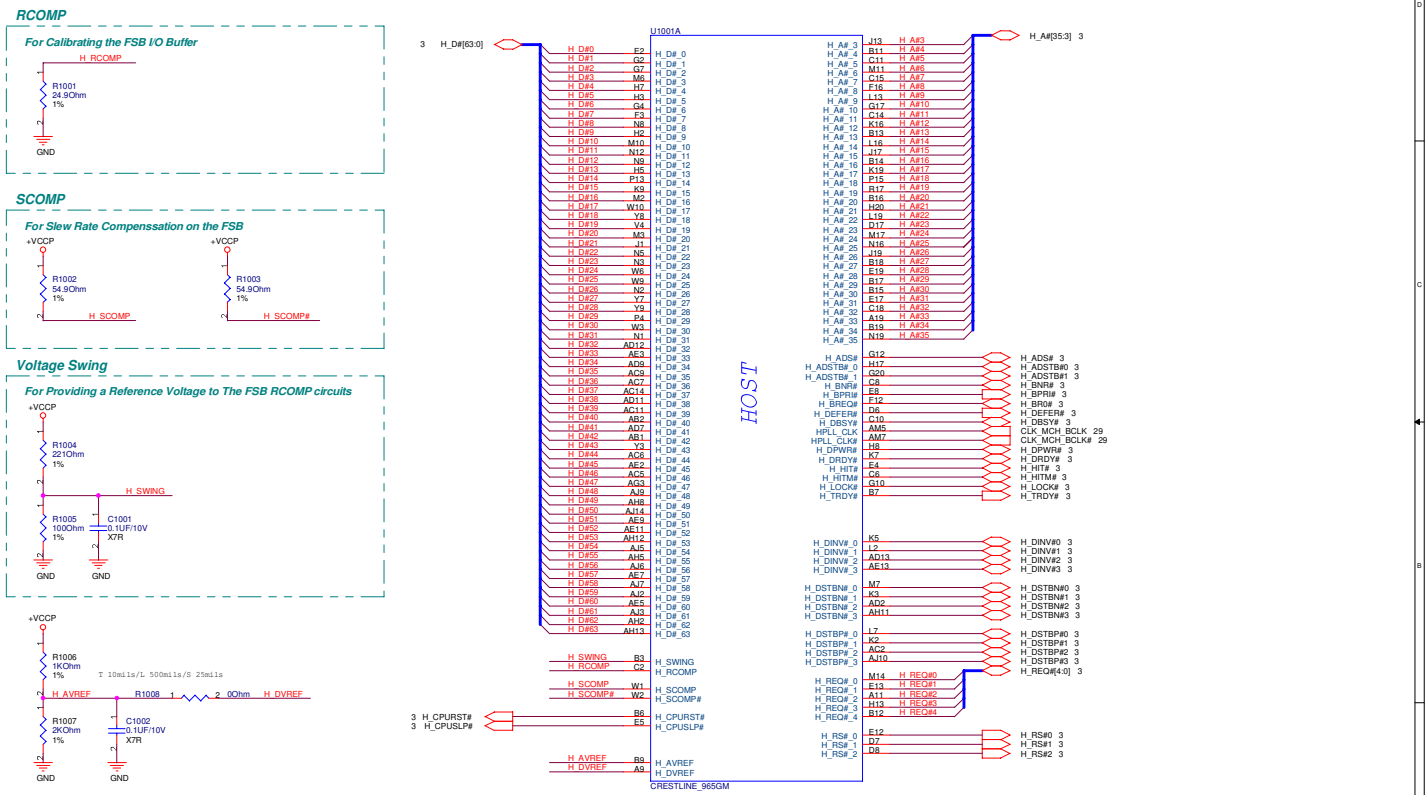
ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 一月 13, 2007 Sheet 9 of 94

<< Kennedy_Zhang >>



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

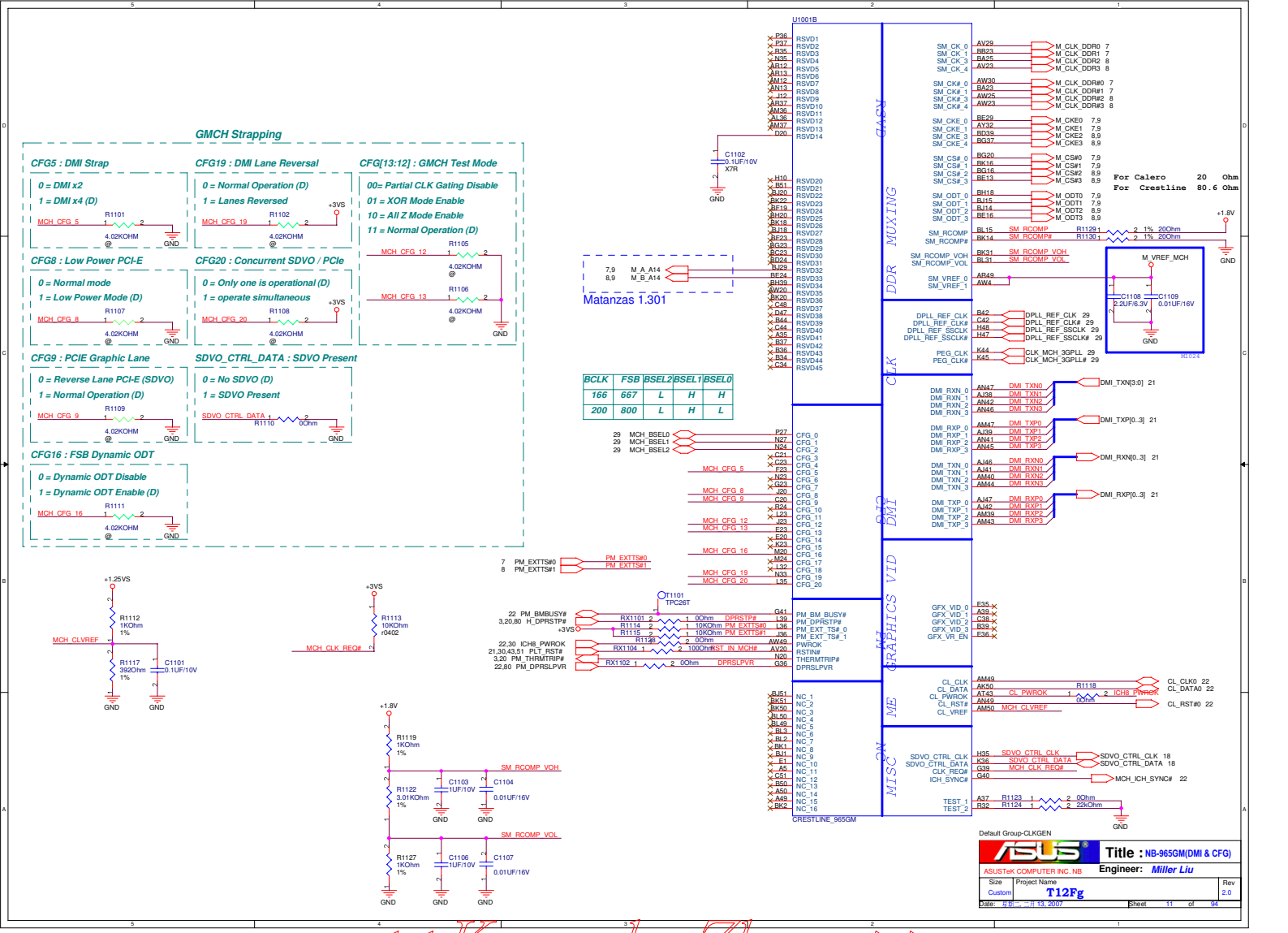
Title : NB-965GM (HOST)

Engineer: Miller Liu

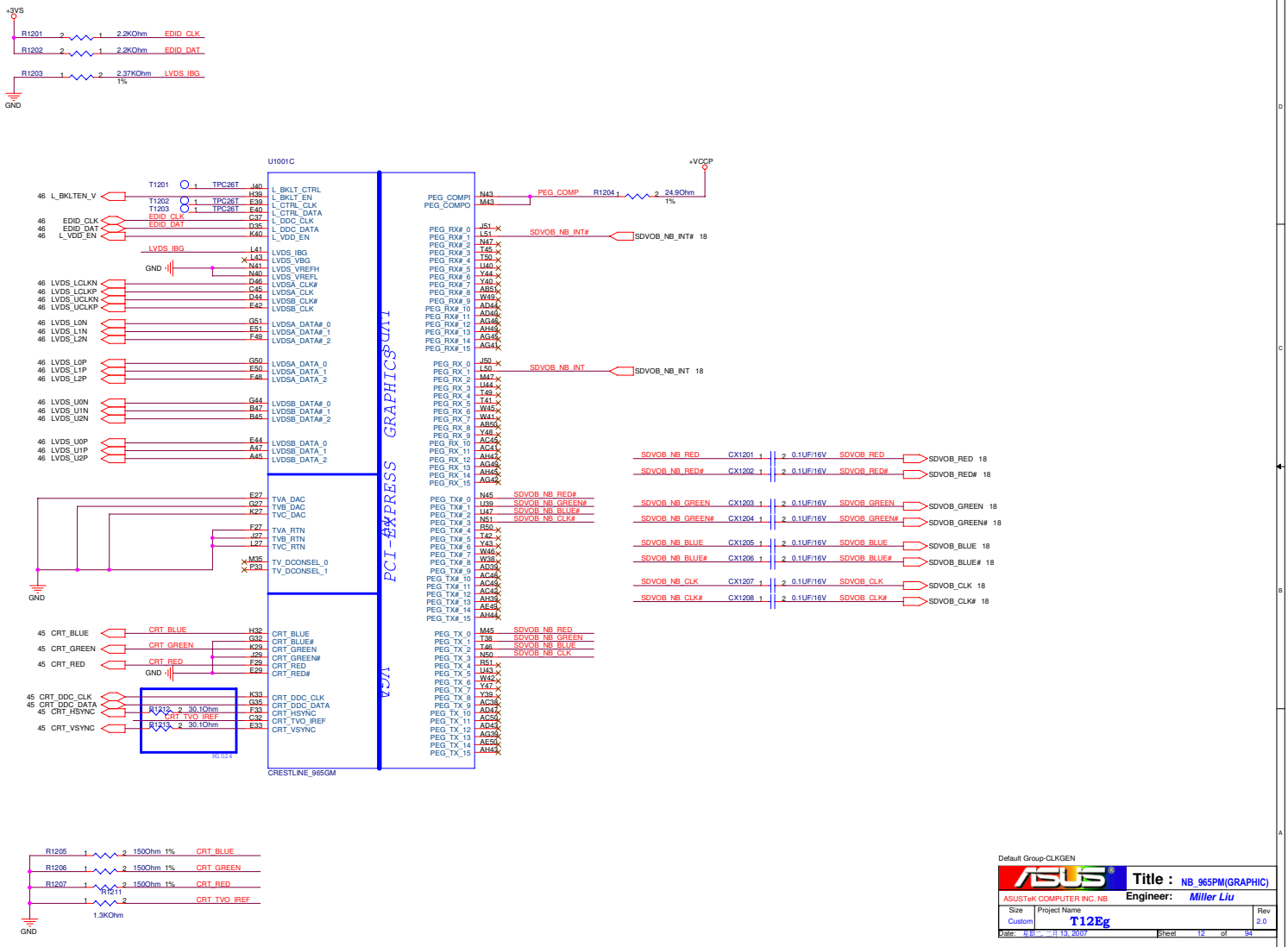
Size	Project Name	Rev
Custom	T12Fg	2.0

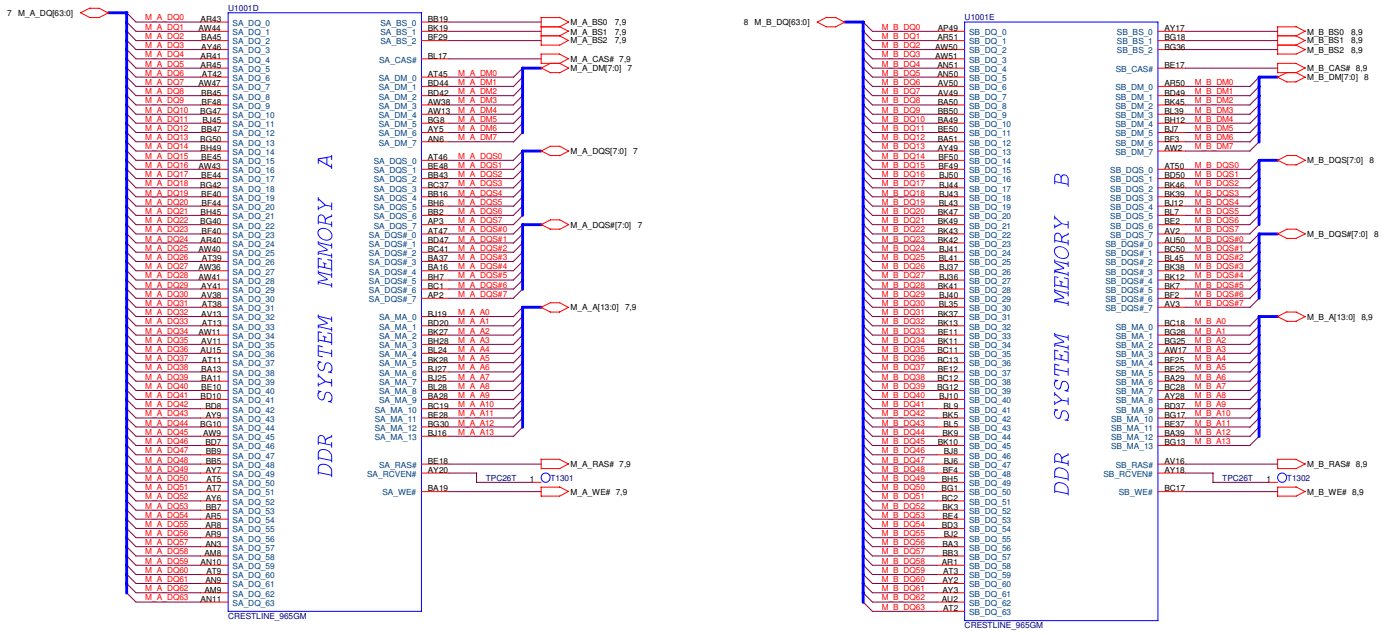
Date: 日 四 二 十 13, 2007 Sheet 10 of 94

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>





Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

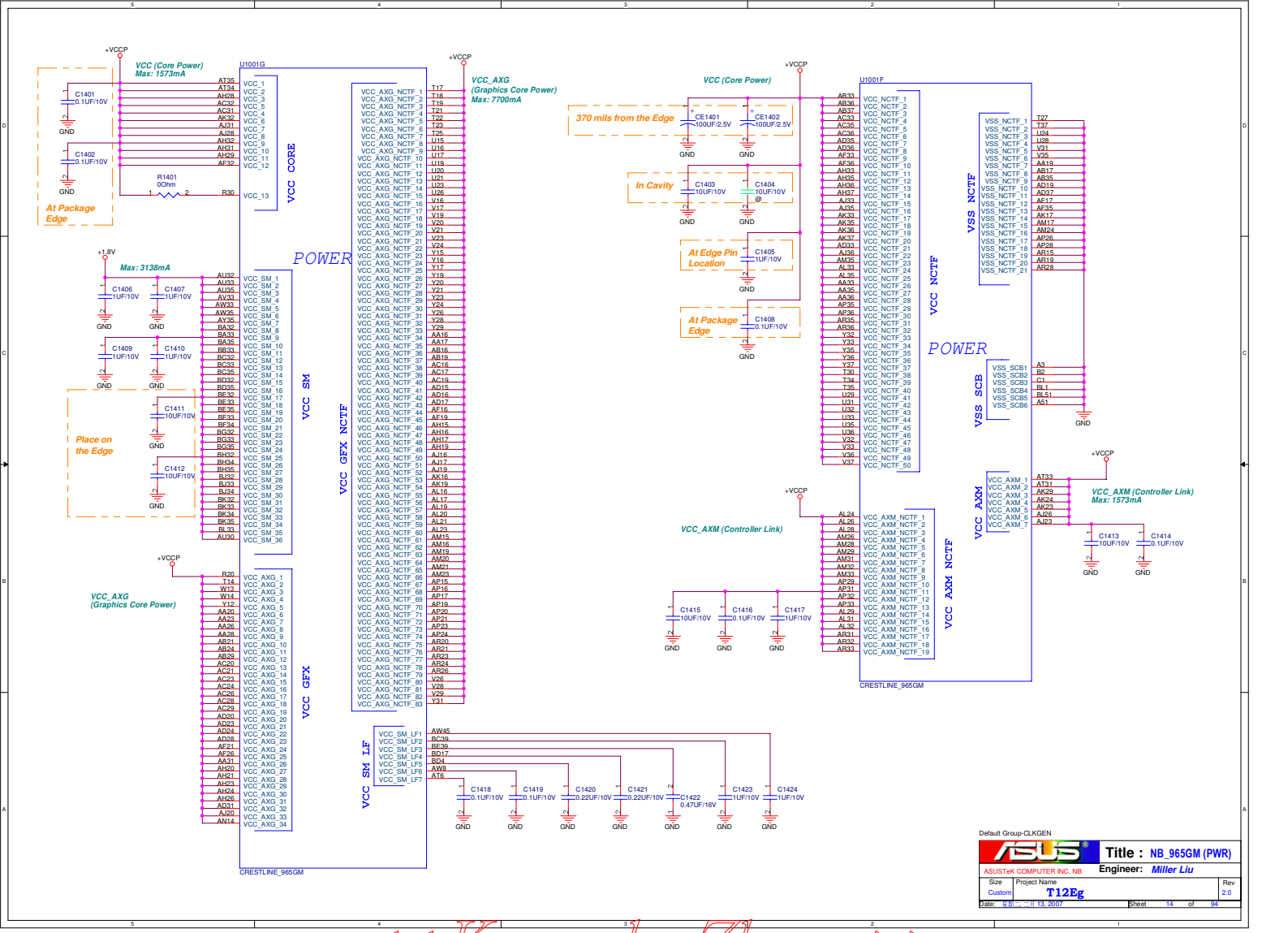
Title : NB-965PM(DDR2)

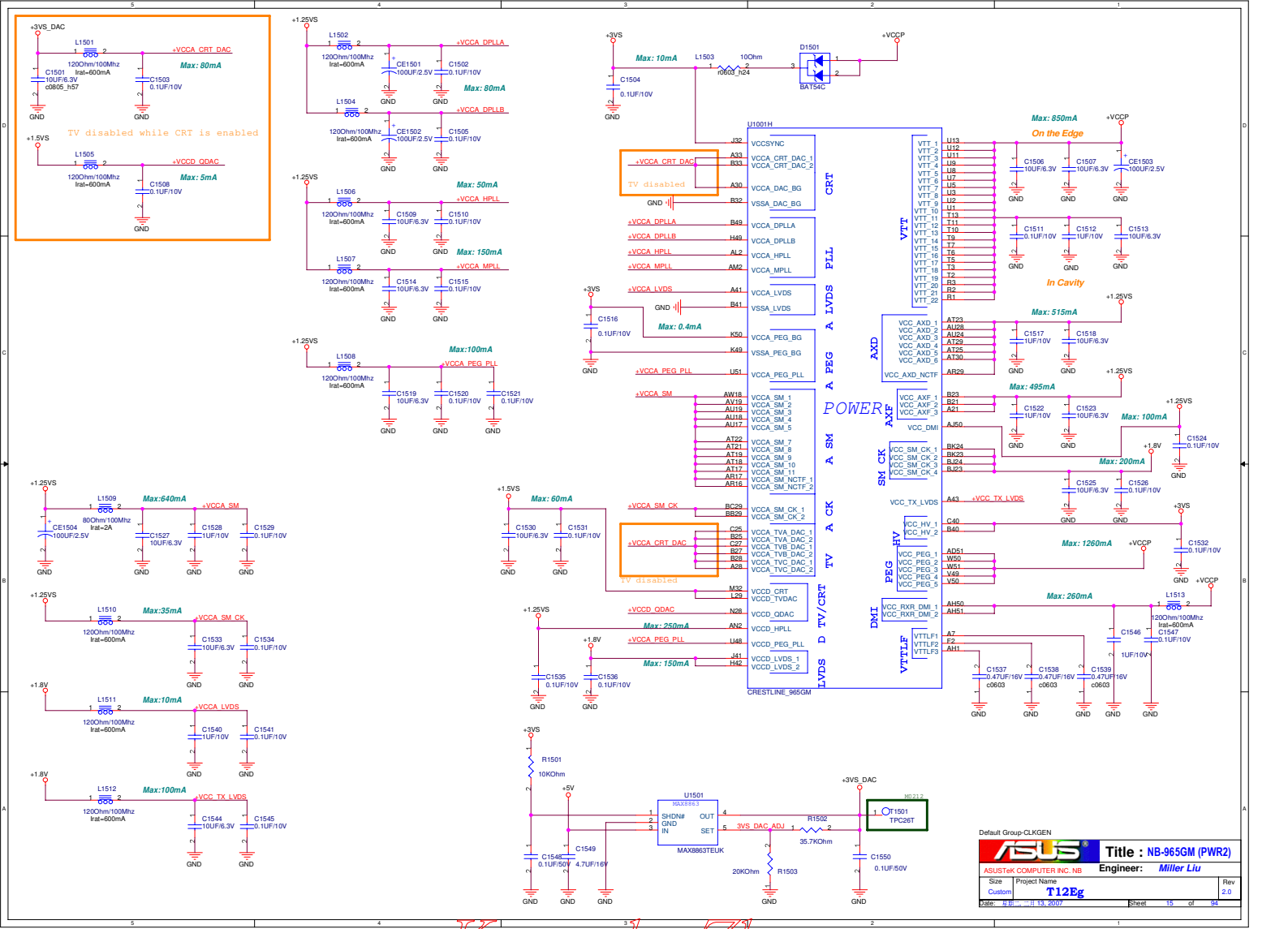
Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

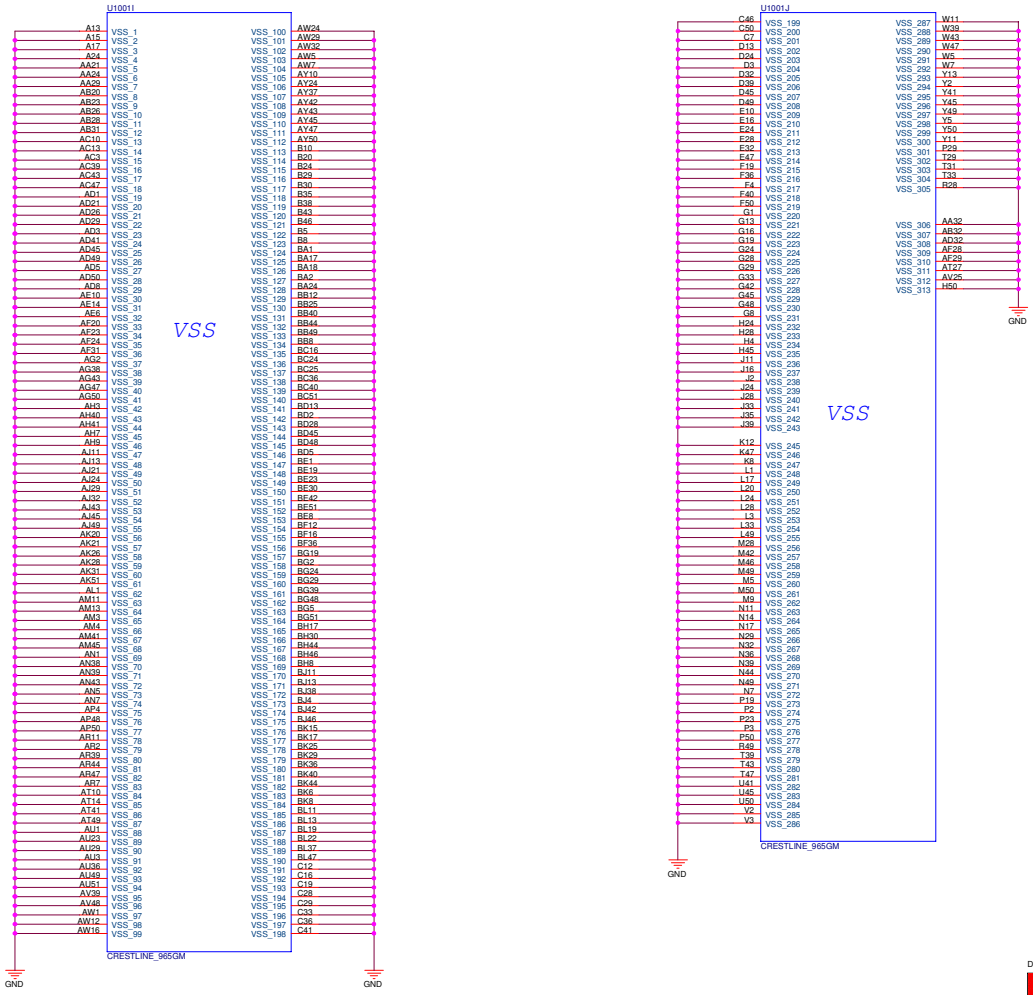
Date: 日 四 二 , 一 月 13, 2007 Sheet 13 of 94

<< Kennedy_Zhang >>





<< Kennedy_Zhang >>



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : NB_965GM (GND)	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 十月 二, 二月 13, 2007	Sheet 16 of 94	

<< Kennedy_Zhang >>

Default Group-CLKGEN

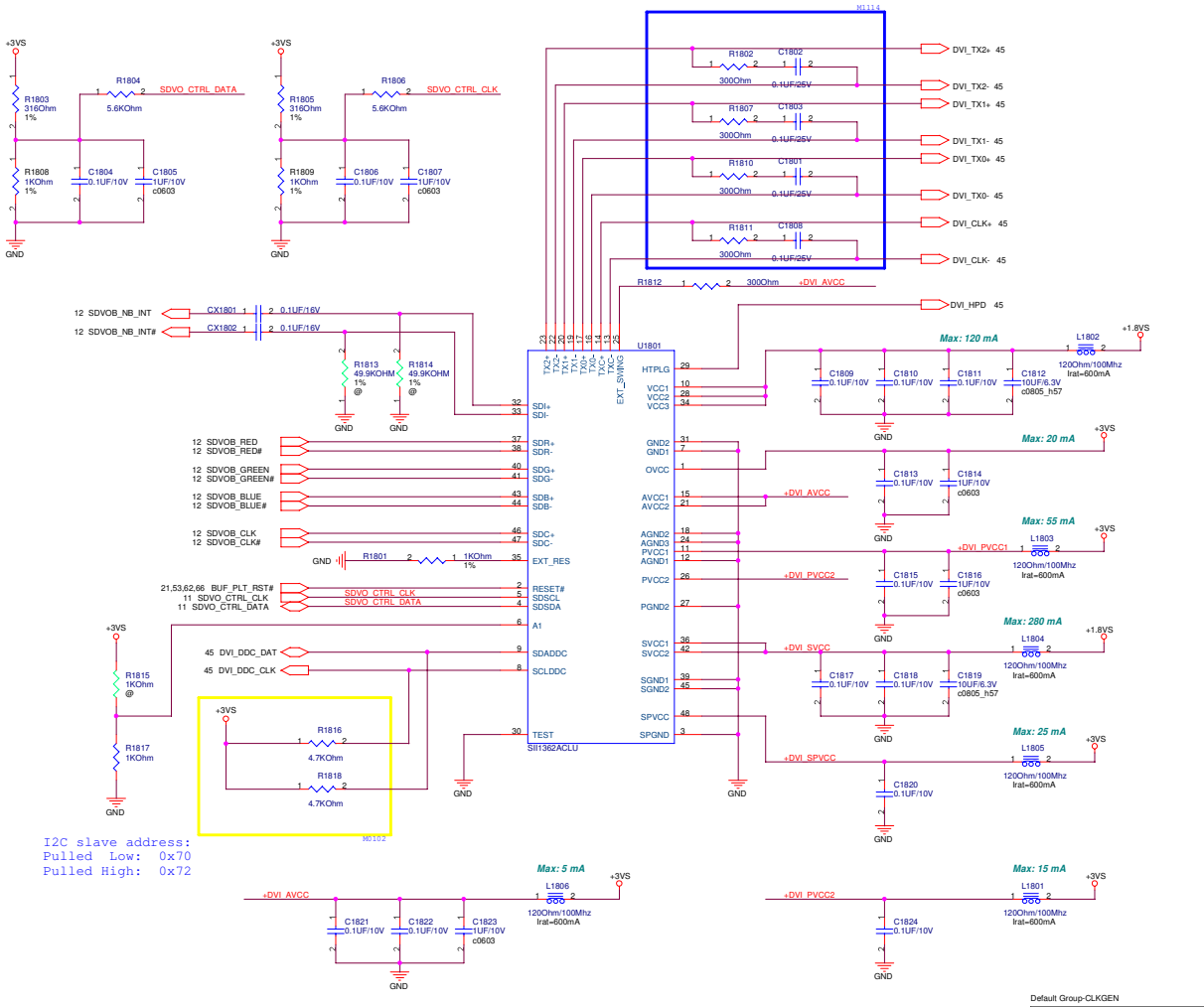
Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 17 of 94



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : Sil362A SDVO-DVI

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 一月 13, 2007 Sheet 18 of 94

<< Kennedy_Zhang >>

Default Group-CLKGEN

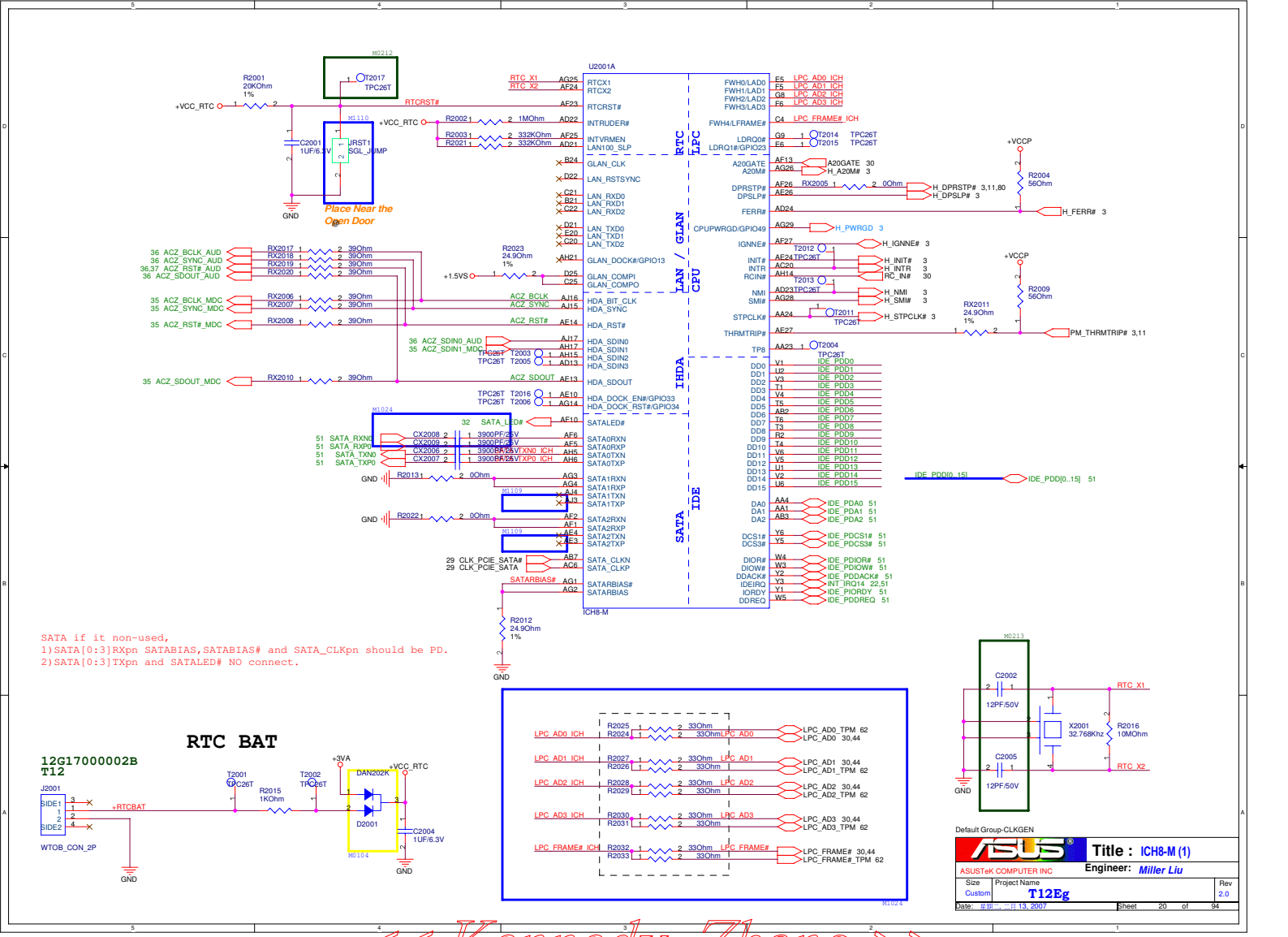
Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 19 of 94

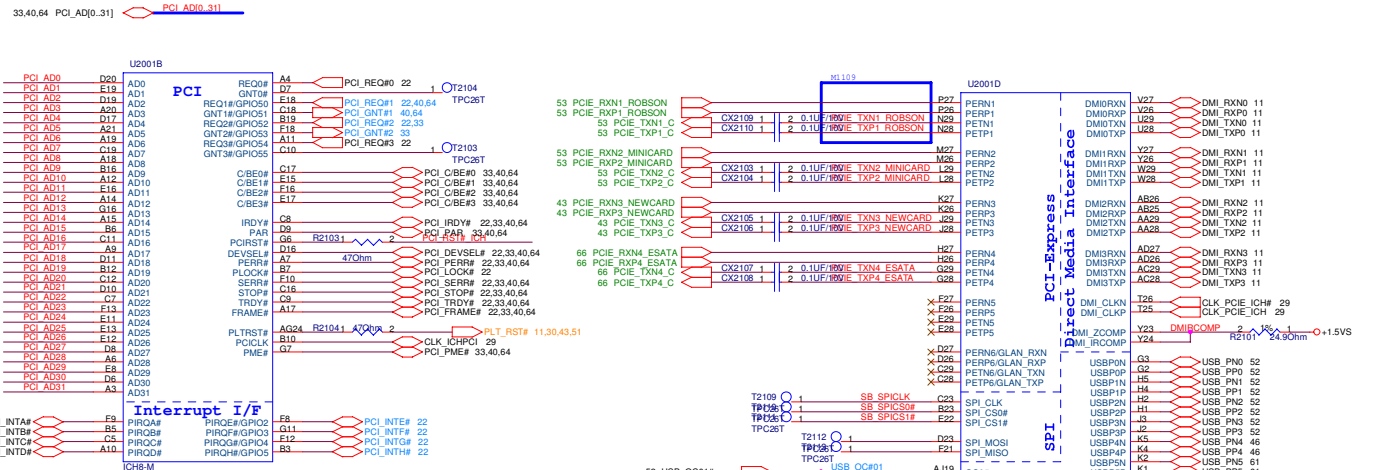


RTC BAT

12G17000002B
T12

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : ICH8-M (1)	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 星期二, 一月 13, 2007	Sheet 20 of 94	

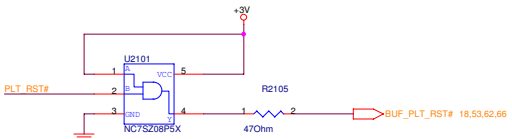


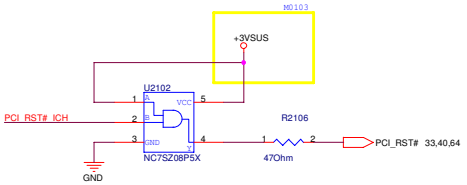
PCI Device

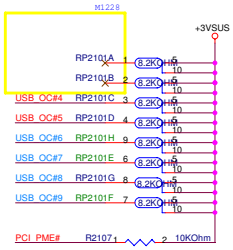
Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A

USB Devices

Port 0	CON5201
Port 1	CON5201
Port 2	CON5202
Port 3	CON5203
Port 4	CMOS Camara
Port 5	BlueTooth
Port 6	NewCard
Port 7	FingerPrint
Port 8	Mini PCIE Card







ICH8 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

Default Group-CLKGEN

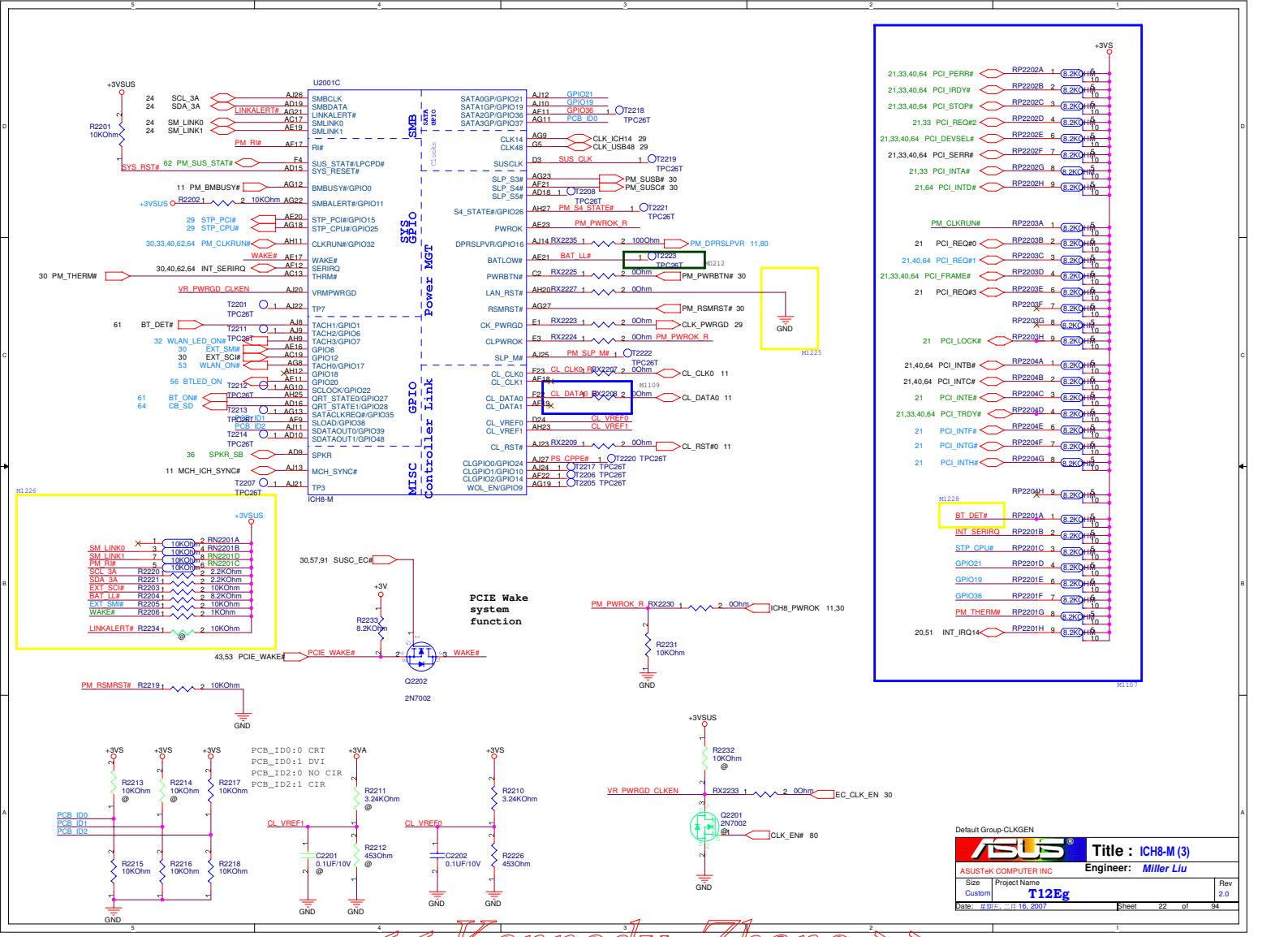
ASUSTeK COMPUTER INC

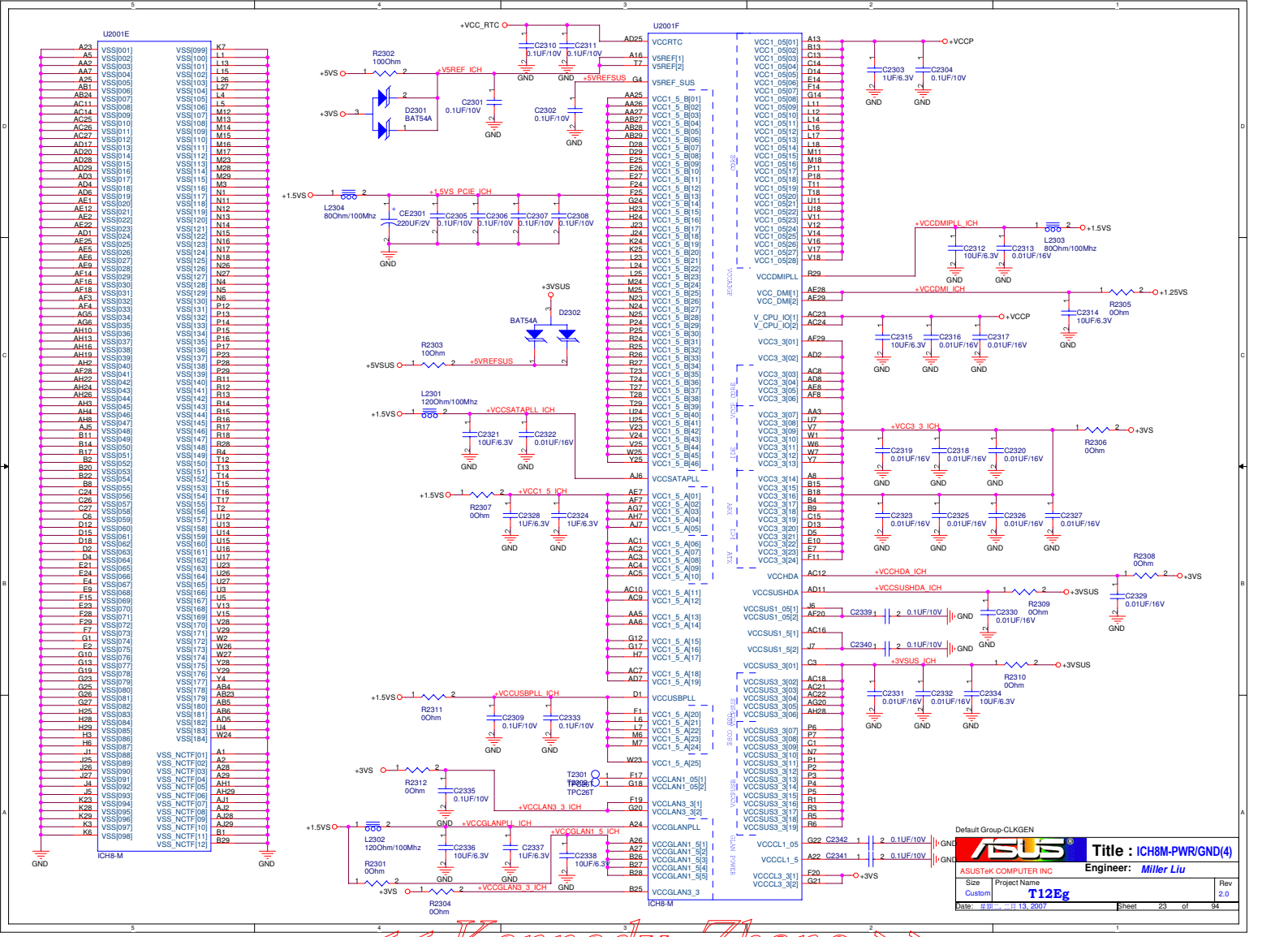
Title : ICH8-M (2)

Engineer: Miller Liu

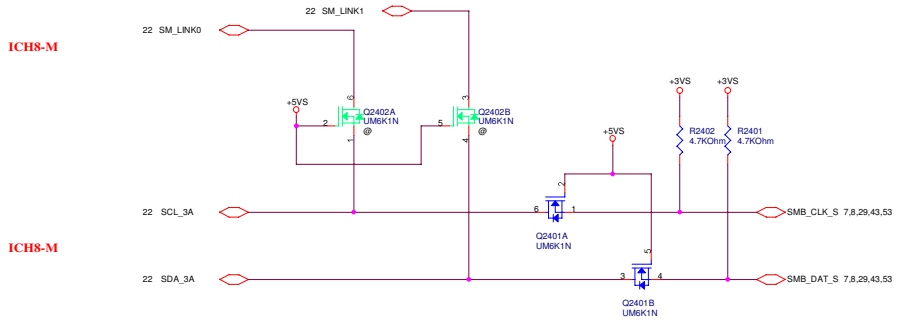
Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 一月 13, 2007 Sheet 21 of 94


U2001C
ICH8-M
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
+3VSUS
+3VS
+3V
+3VA
GND
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#/GPIO17
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
PCIE Wake system function
PCB_ID0:0 CRT
PCB_ID0:1 DVI
PCB_ID2:0 NO CIR
PCB_ID2:1 CIR
Default Group-CLKGEN
ASUSTeK COMPUTER INC
Title : ICH8-M (3)
Engineer: Miller Liu
Project Name
T12Eg
Rev 2.0
Sheet 22 of 94
<< Kennedy_Zhang >>



Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : ICH8M-Other

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 24 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Jeffrey Lai

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 25 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 26 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 27 of 94

Default Group-CLKGEN

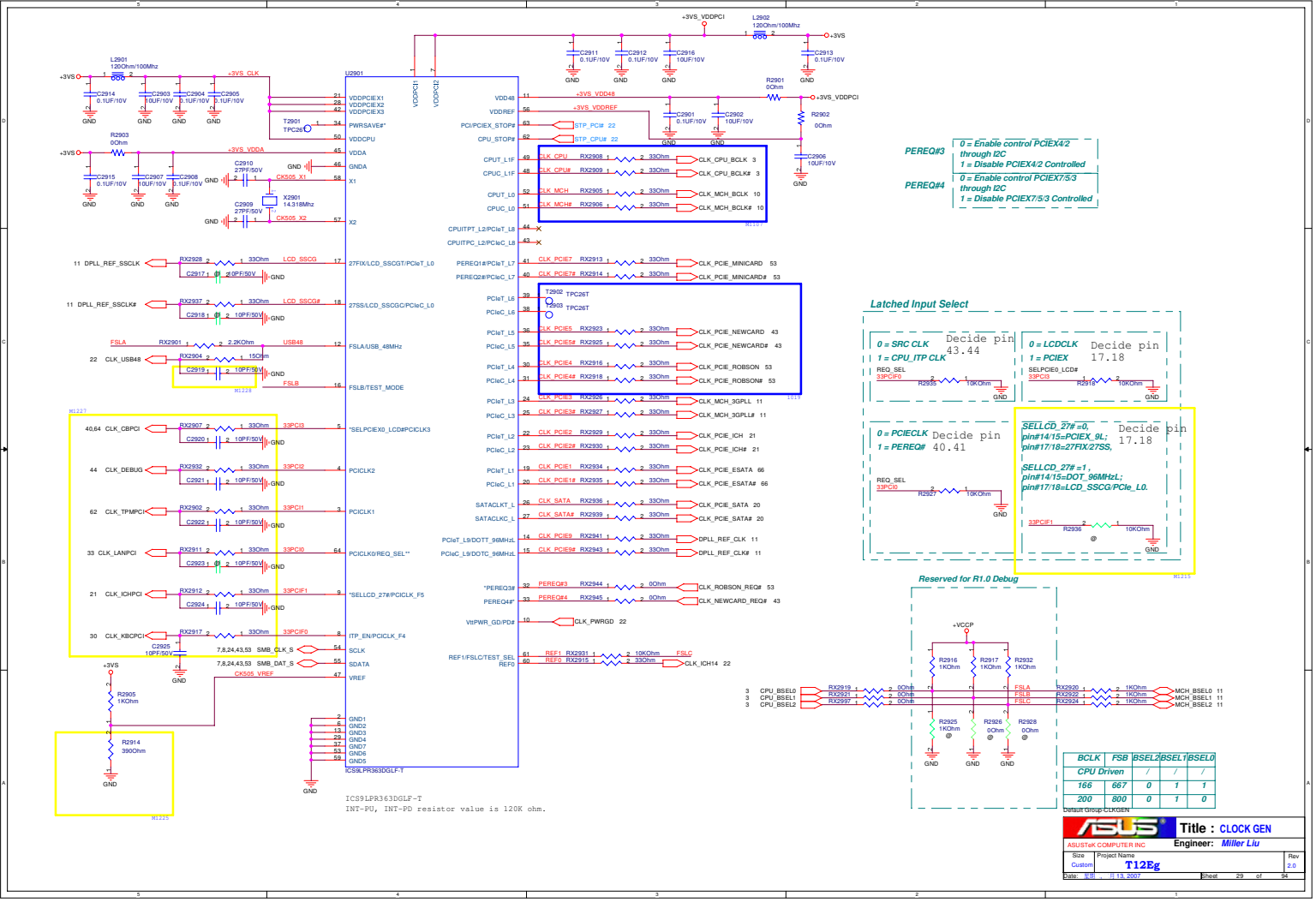
Title : NULL

ASUSTeK COMPUTER INC

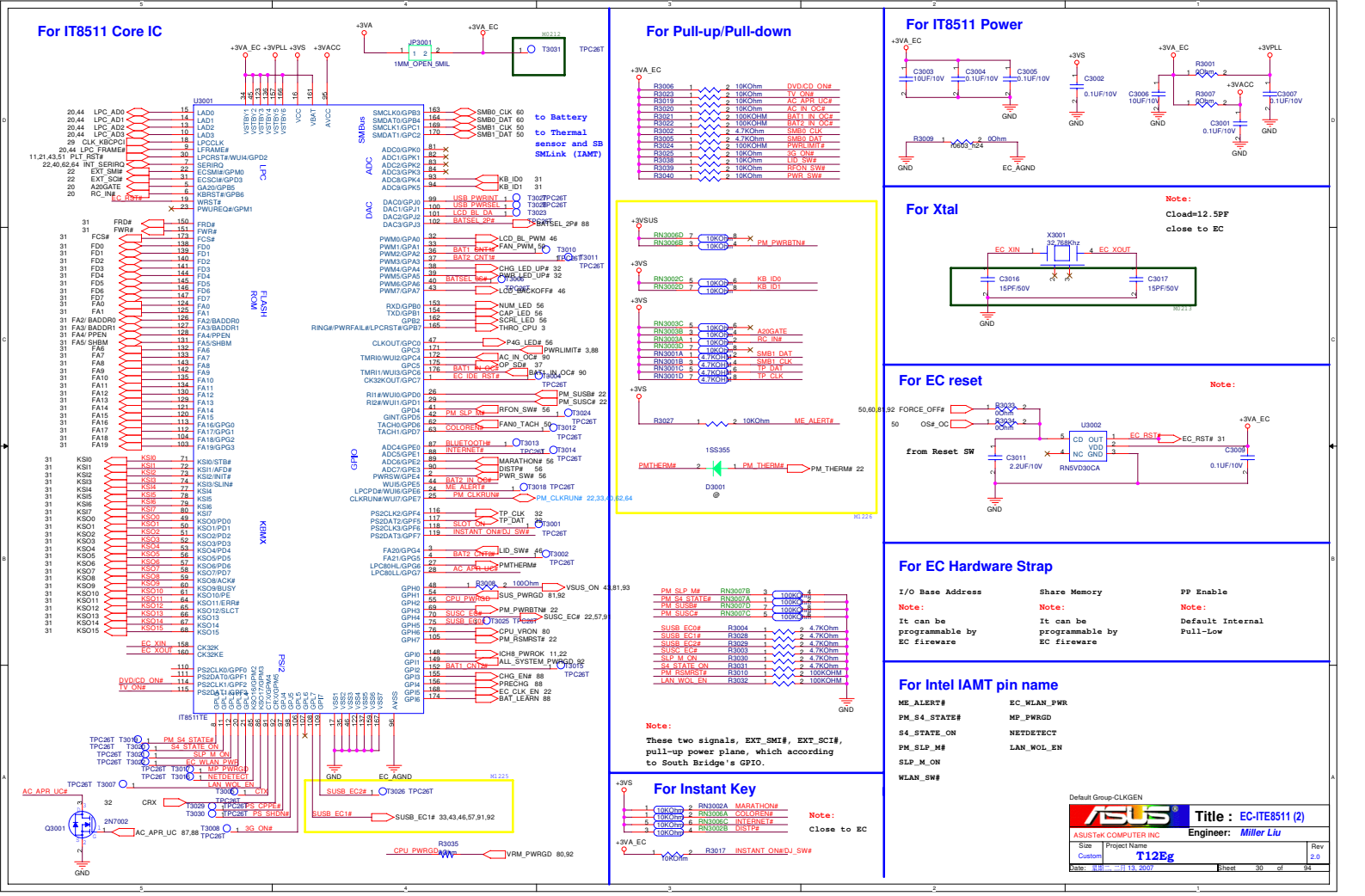
Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 28 of 94



<< Kennedy_Zhang >>

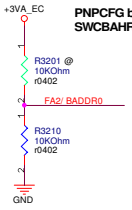


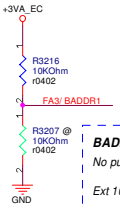
<< Kennedy_Zhang >>

EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

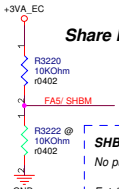




BADDR[1:0]

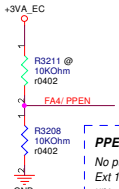
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

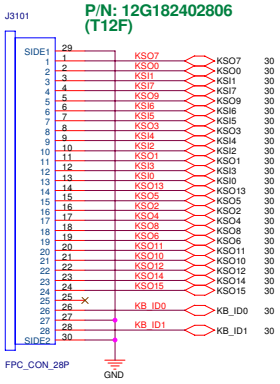


PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

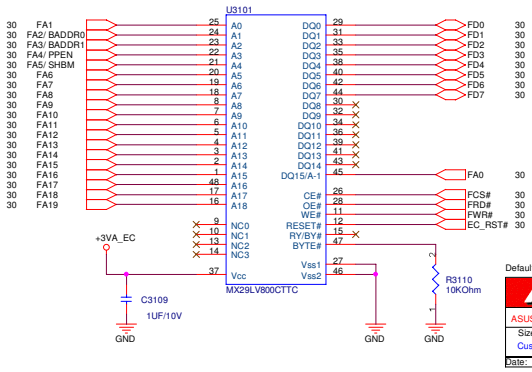
Keyboard Conn.

P/N: 12G182402806 (T12F)



For 8M bits ISA ROM

8M TSOP



Note:

If you use 8M bits ROM, you need to connect FA19 to EC side.

Default Group-CLKGEN

ASUSTeK COMPUTER INC

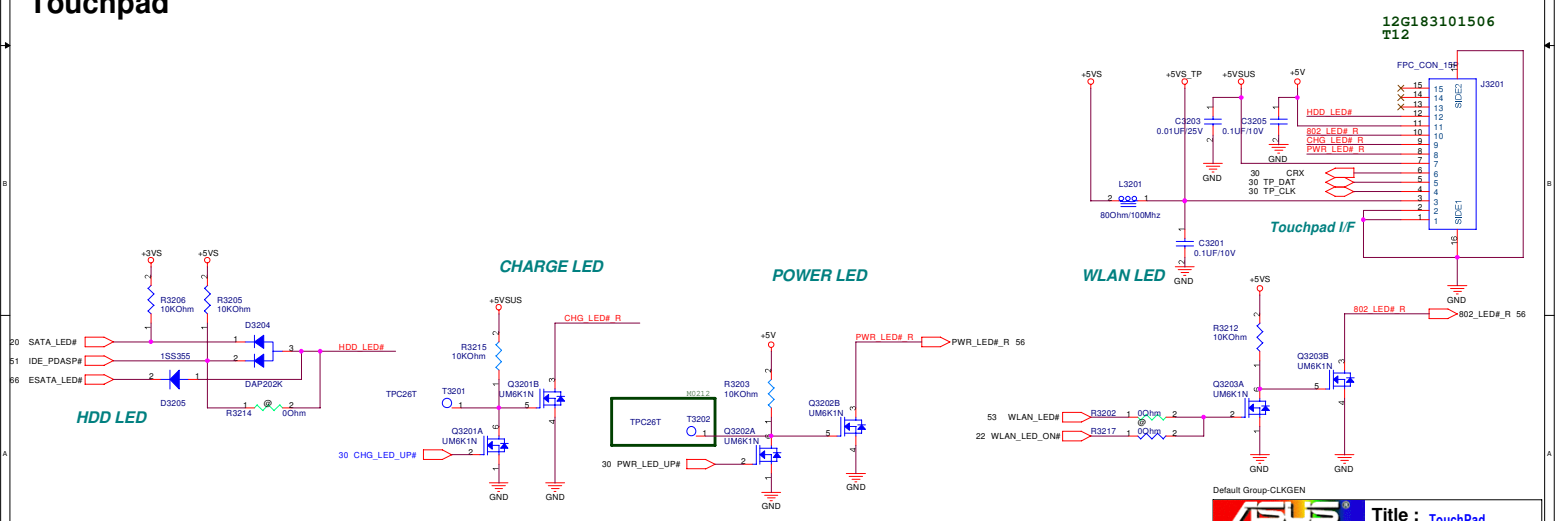
Title : EC-ITE8511(2)

Engineer: *Miller Liu*

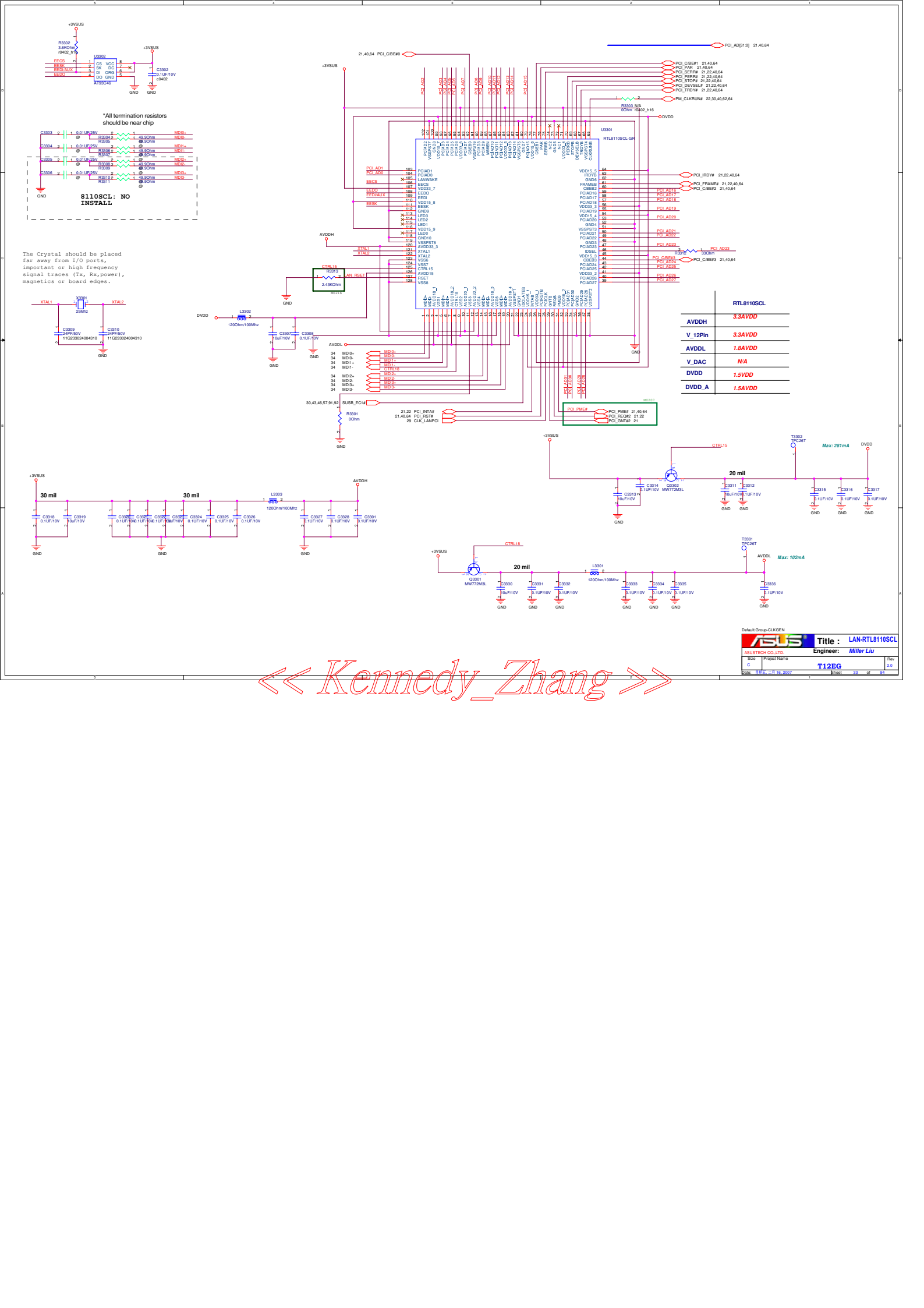
Size	Project Name	Rev
Custom	**T12Eg**	2.0

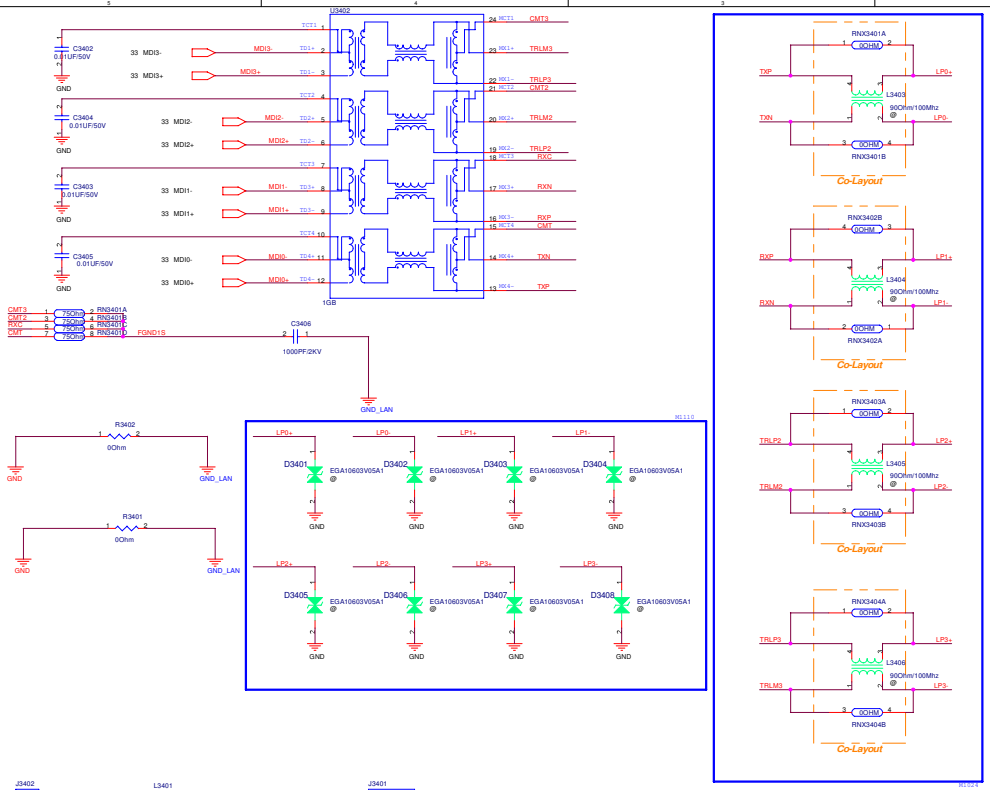
Date: 星期二, 一月 13, 2007 Sheet 31 of 94

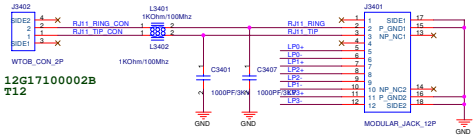
Touchpad



<< Kennedy_Zhang >>


*All termination resistors should be near chip
8110SCL: NO INSTALL
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
U3301
RTL8110SCL-GR
RTL8110SCL
AVDDH 3.3AVDD
V_12Pin 3.3AVDD
AVDDL 1.8AVDL
V_DAC N/A
DVDD 1.5VDD
DVDD_A 1.5AVDD
30 mil
20 mil
Max: 281mA
Max: 102mA
Default Group-CLKGEN
Title : LAN-RTL8110SCL
Engineer: Miller Liu
ASUSTeK CO.,LTD
Project Name T12EG
Rev 2.0
Sheet 33 of 94
<< Kennedy_Zhang >>





12G17100002B
T12

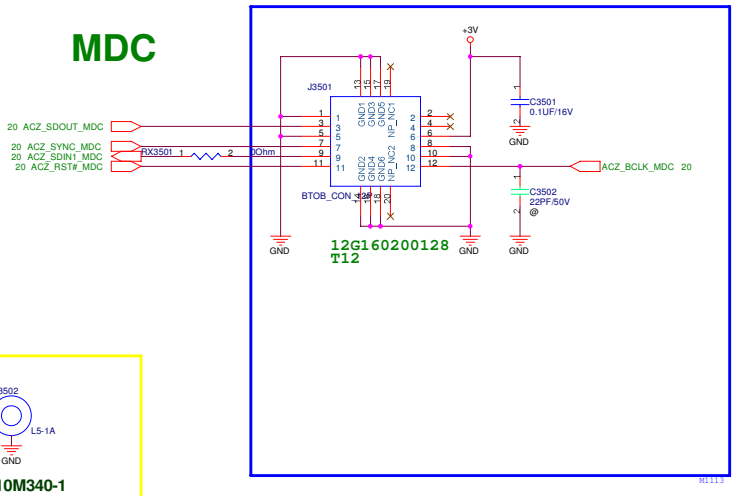
12G142111120
T12

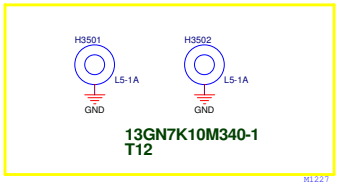
Default Group-CLKGEN

ASUSTECH CO.,LTD	Title :	RJ11/RJ45	
	Engineer:	Miller Liu	
Size: C	Project Name: T12EG		Rev: 2.0
Date: 年 05 月 13, 2007	Sheet 34 of 94		

<< Kennedy_Zhang >>

MDC

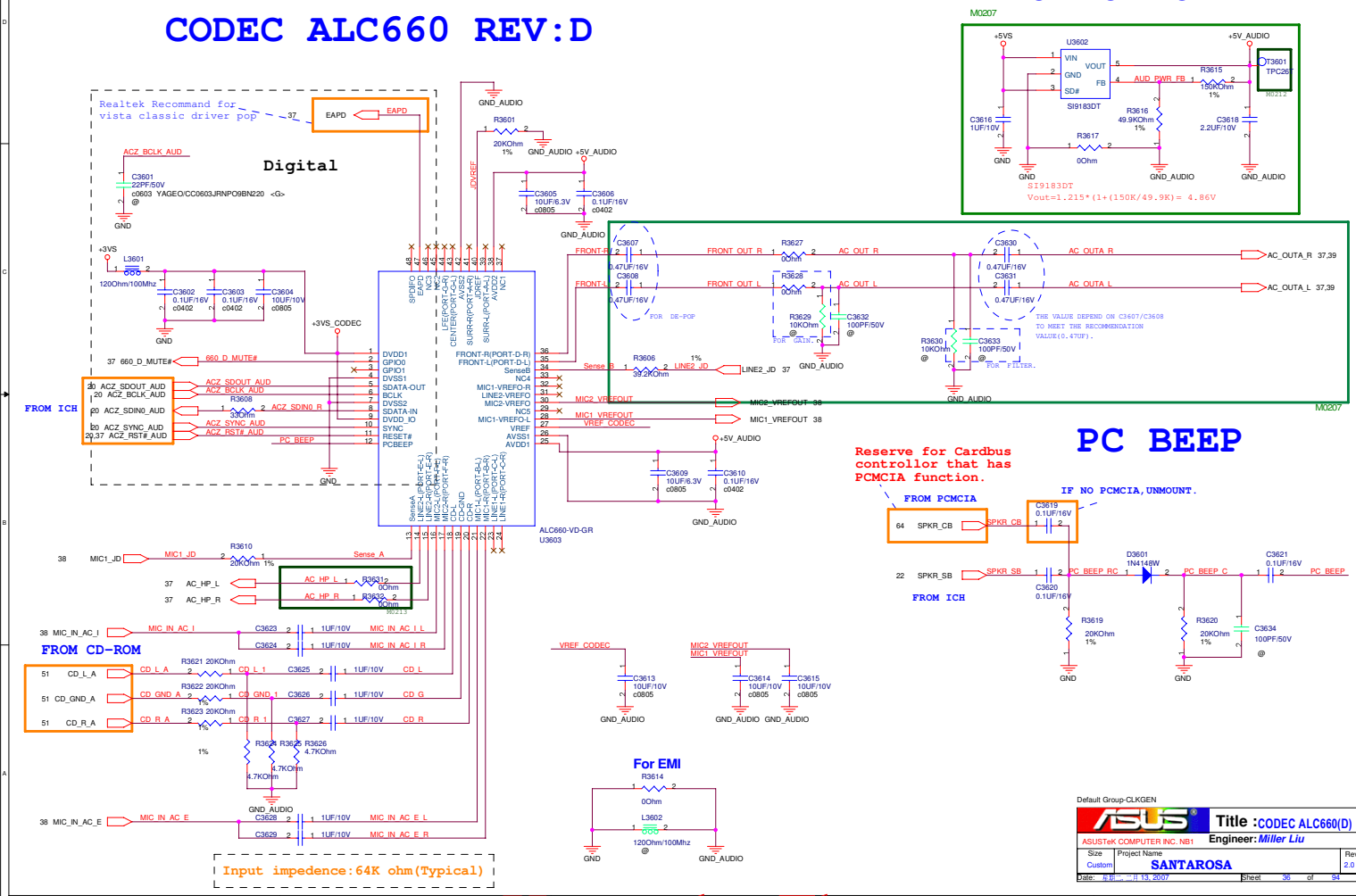




Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : MDC	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 一月 13, 2007	Sheet 35 of 94	

CODEC ALC660 REV:D



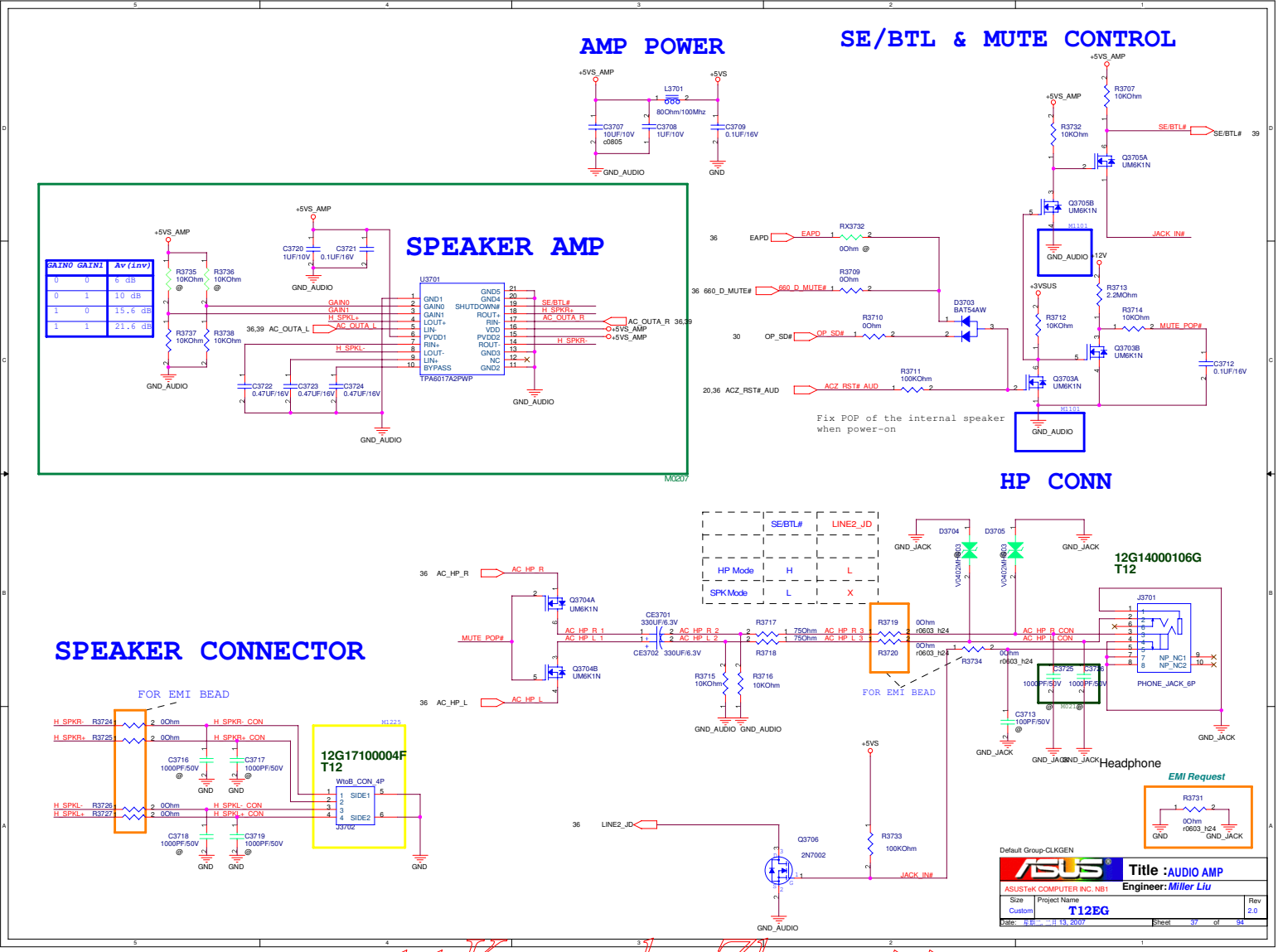
AUDIO POWER

PC BEEP

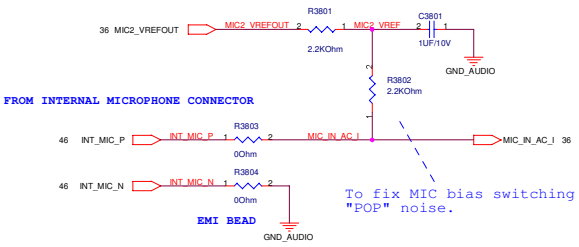
Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1	Title : CODEC ALC660(D)	
	Engineer: Miller Liu	
Size: Custom	Project Name: SANTAROSA	Rev: 2.0
Date: 日期, 二月 13, 2007	Sheet 36 of 94	

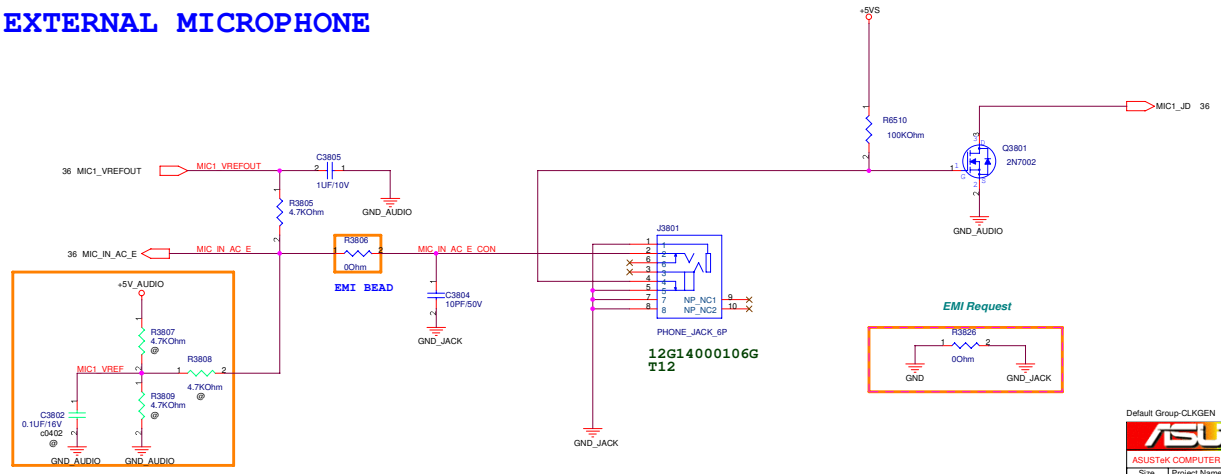
<< Kennedy_Zhang >>



INTERNAL MICROPHONE

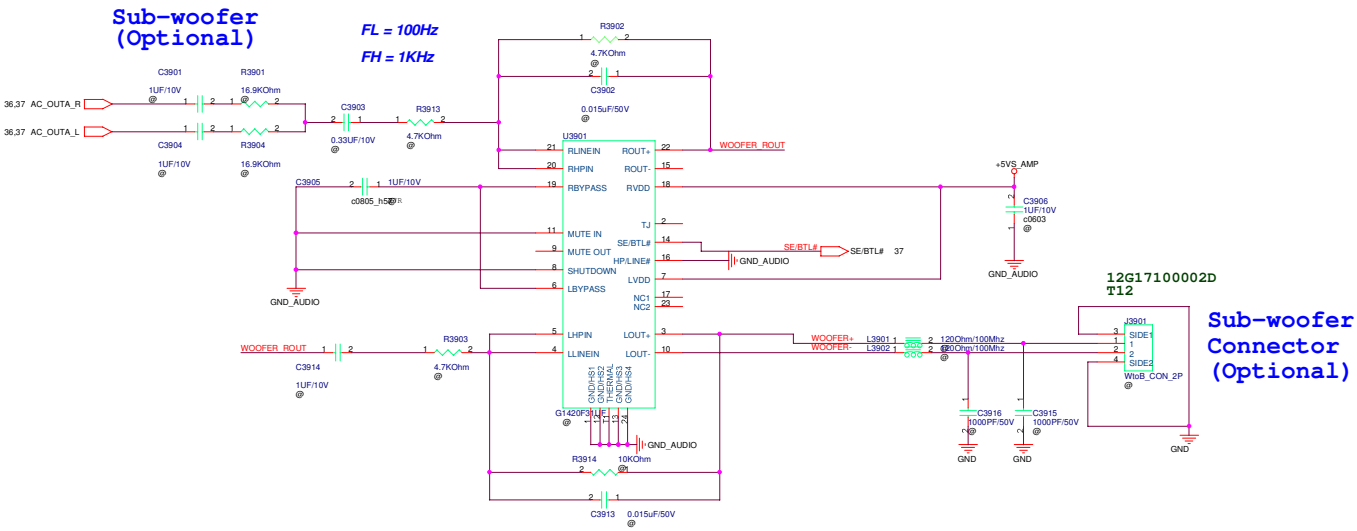


EXTERNAL MICROPHONE



Default Group-CLKGEN

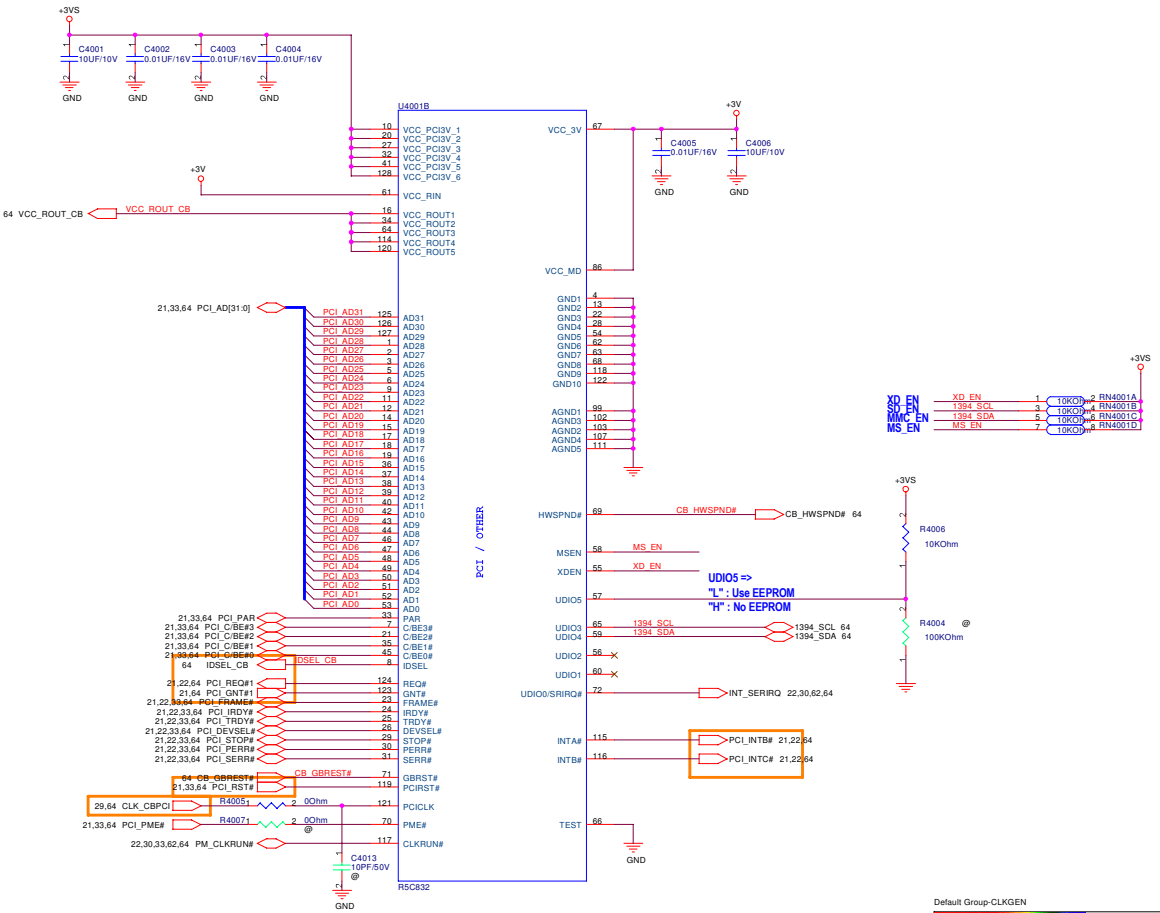
ASUSTeK COMPUTER INC. NB1	Title : MIC	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 十月 二十日 13, 2007	Sheet 38 of 94	



Default Group-CLKGEN

ASUSTek COMPUTER INC NPI	Title : Sub-Woofer		
	Engineer: Miller_Liu		
Size: Custom	Project Name: T12EG		Rev: 2.0
	P/N: <OrgAddr2>		
Date: 十月 13, 2007	Sheet 39 of 94		

<< Kennedy_Zhang >>



Default Group-CLKGEN

ASUSTeK COMPUTER INC

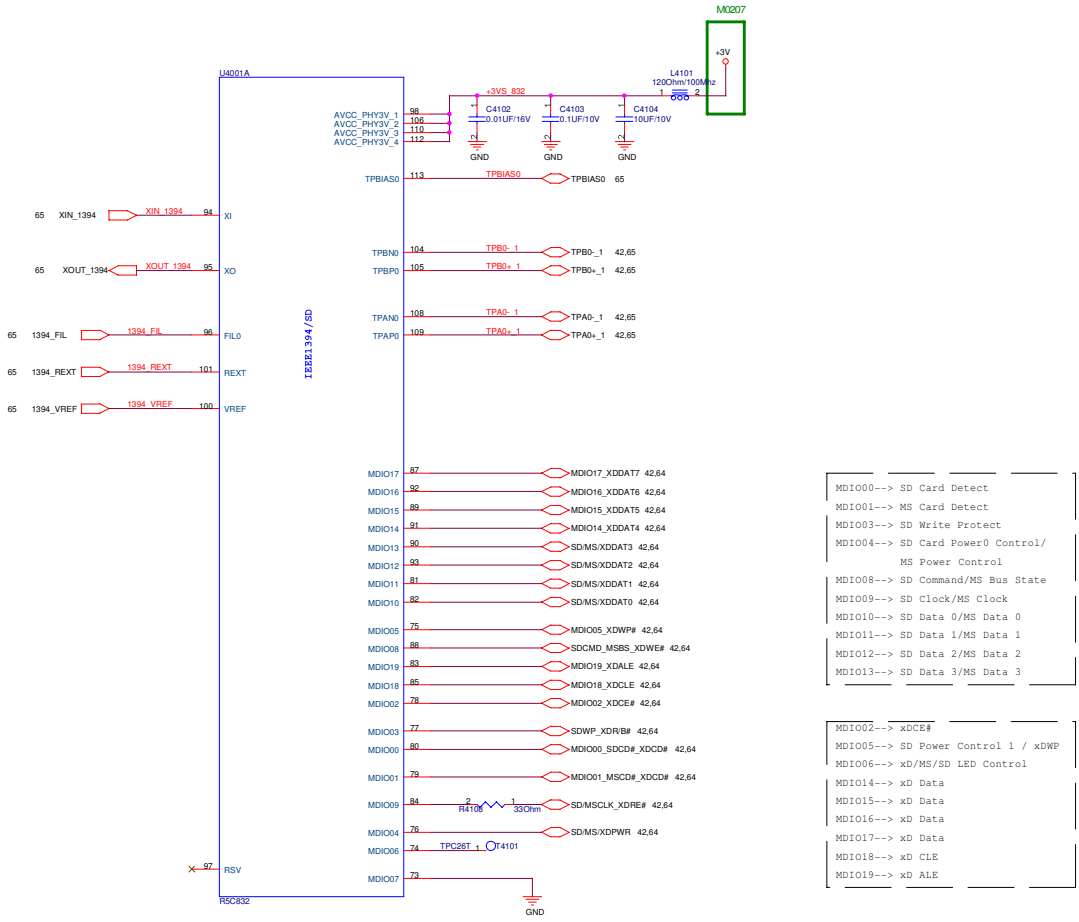
Title : CARDBUS R5C832 (1)

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期五, 月 16, 2007 Sheet 40 of 94

<< Kennedy_Zhang >>



Default Group-CLKGEN

Title: CARDBUS R5C832 (2)

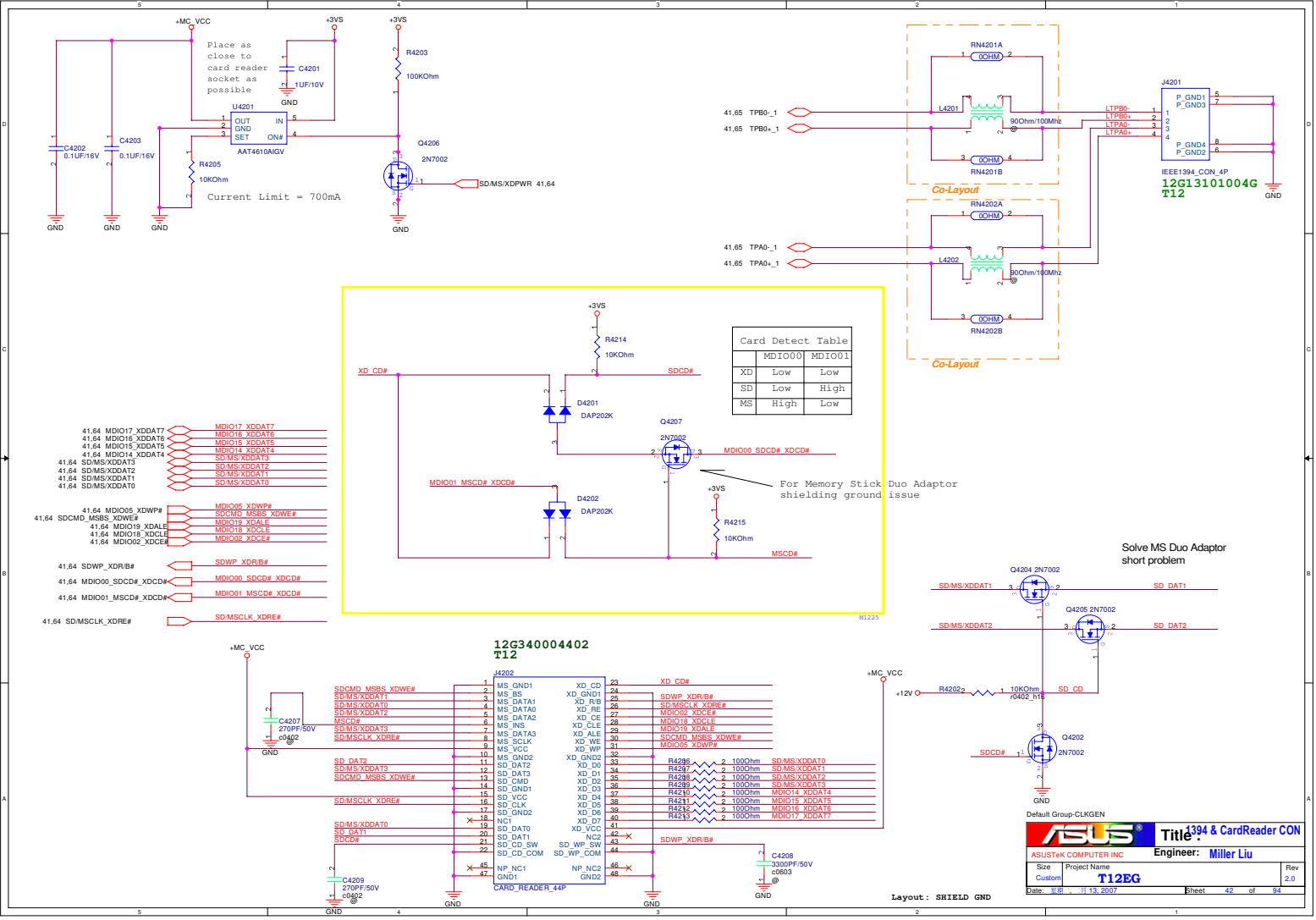
ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 十月 一日 13, 2007 Sheet 41 of 94

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC
Engineer: Miller Liu
Title : 1394 & CardReader CON
Size: Custom
Project Name: T12EG
Rev: 2.0
Date: 五月 13, 2007
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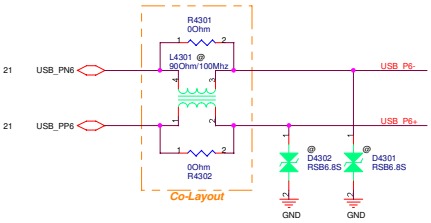
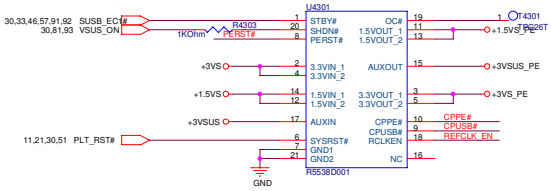
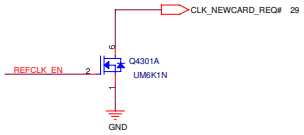
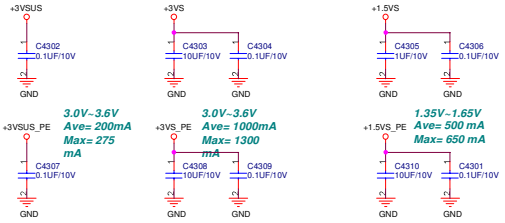


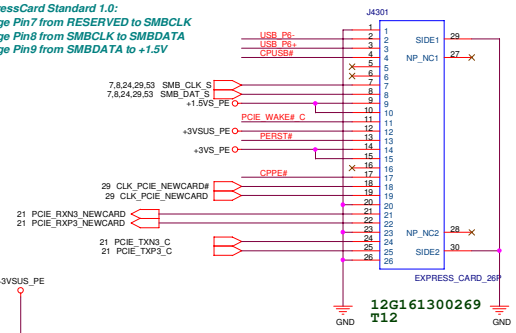


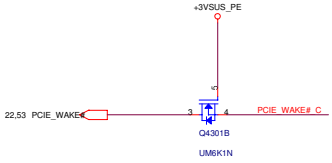


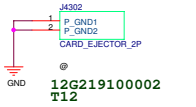


!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

NewCard Header

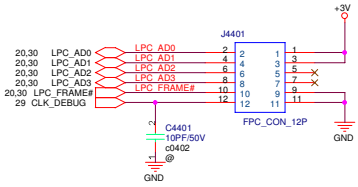






Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB1	Title : NEWCARD	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12F	Rev: 2.0
Date: 十月 二十日 13, 2007	Sheet 43 of 94	

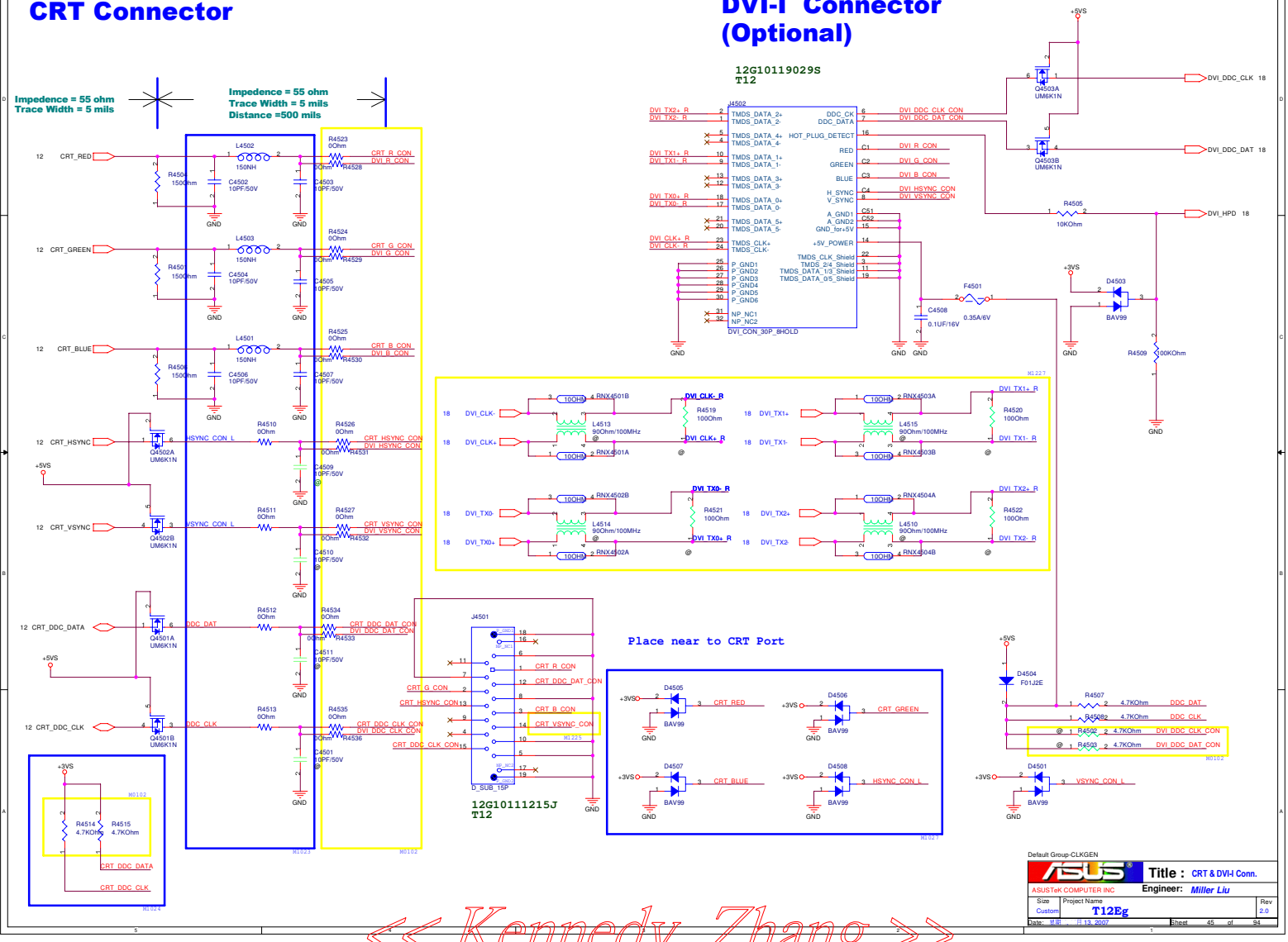


Default Group-CLKGEN

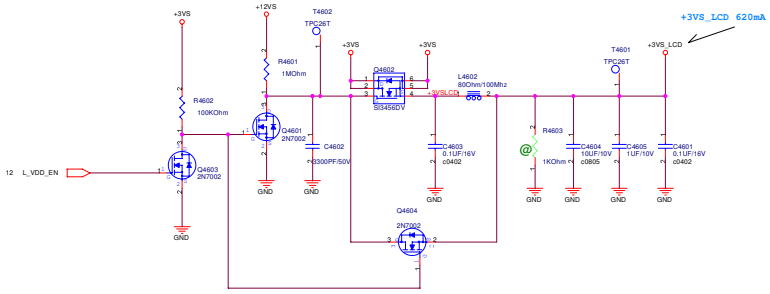
ASUSTeK COMPUTER INC. NB	Title : DEBUG	
	Engineer: *Miller Liu*	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 一月 13, 2007	Sheet 44 of 94	

CRT Connector

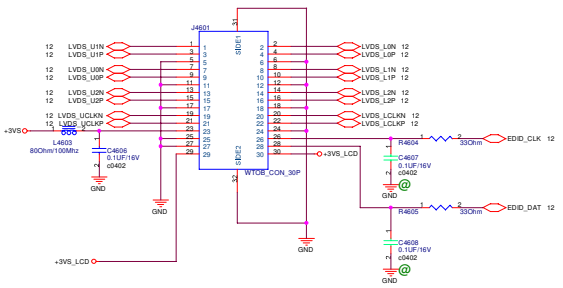
DVI-I Connector (Optional)



<< Kennedy_Zhang >>



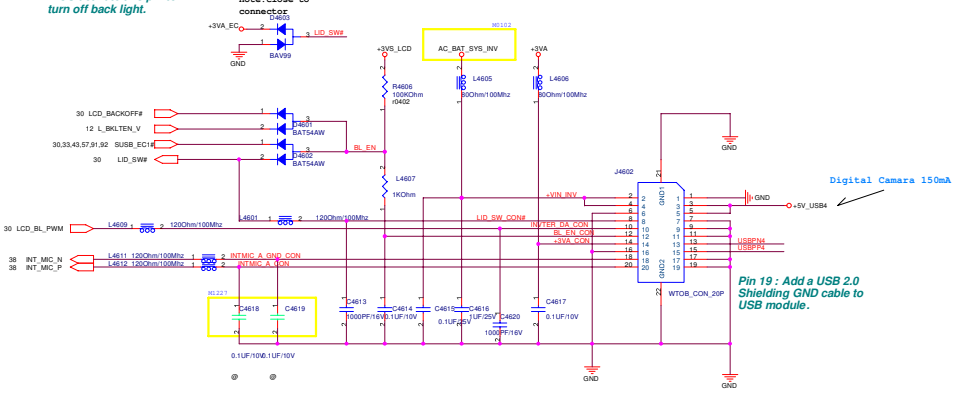
Pin define is the same as A7



LCD LVDS Interface

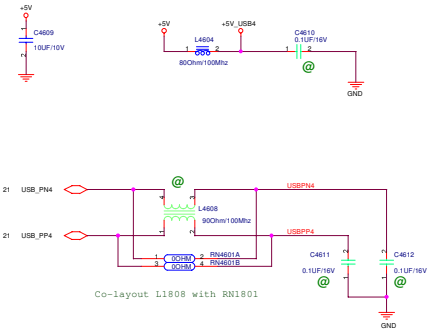
BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

Layout note:close to connector



Digital Camara 150mA

Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



Default Group:CLK/GEN

ASUSTeK COMPUTER INC	Title : LVDS & Inverter Conn.	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 星期二, 十月 16, 2007	Sheet 46 of 94	

Default Group-CLKGEN

Title : NULL

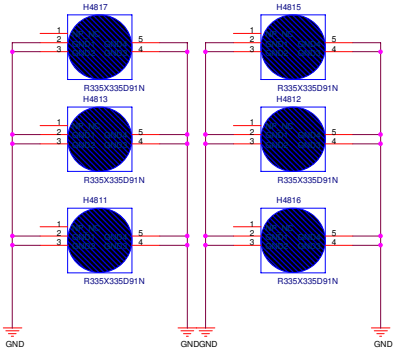
ASUSTeK COMPUTER INC

Engineer: Miller Liu

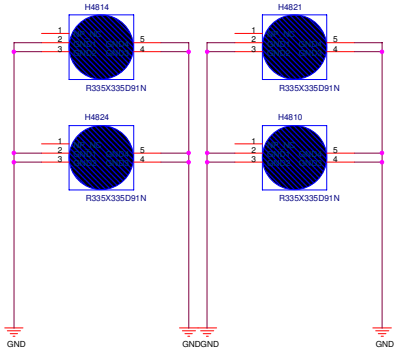
Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 47 of 94

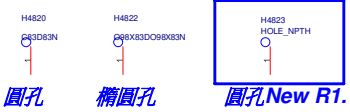
A Hole / TOP Side



A Hole / Bottom Side

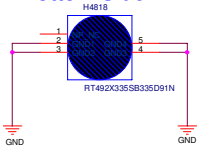


Drill Hole for Fix

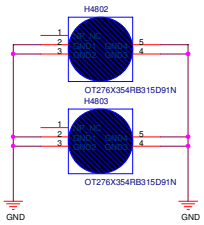


圓孔　　橢圓孔　　圓孔New R1.1

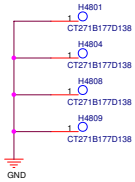
A Hole Special / Bottom Side



E Hole for Main board fix

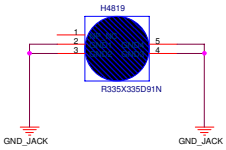


F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1

13GNJ510M170-1
T12



Default Group-CLKGEN

ASUSTek COMPUTER INC NPI	Title : SREW HOLE		
	Engineer: Miller Liu		
Size: Custom	Project Name: T12EG	P/N: <OrgAddr2>	Rev: 2.0
Date: 星期一, 一月 13, 2007	Sheet 48 of 94		

Default Group-CLKGEN

Title : NULL

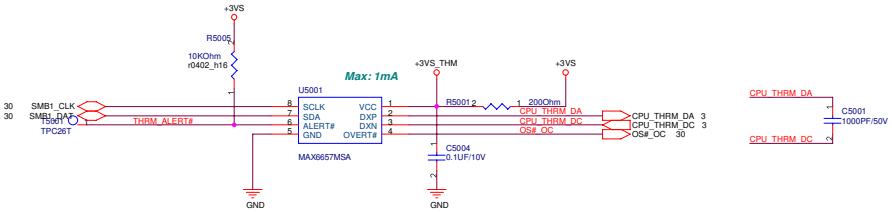
ASUSTeK COMPUTER INC

Engineer: Miller Liu

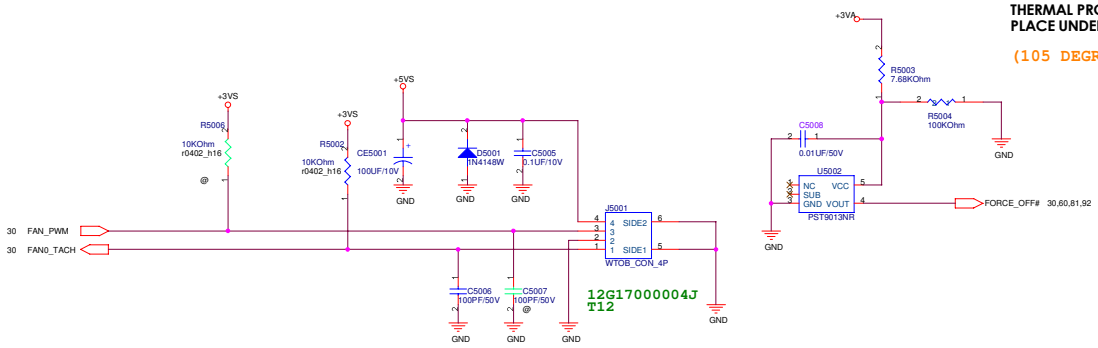
Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 49 of 94

Thermal Sensor



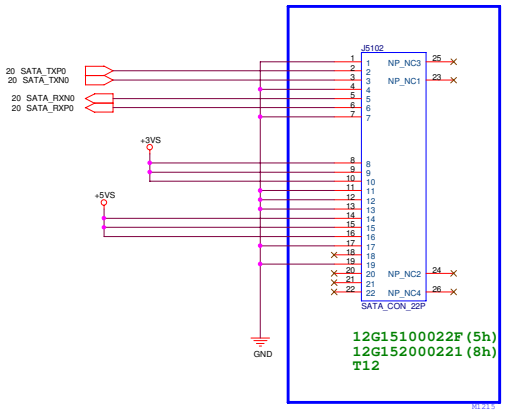
DC FAN Control

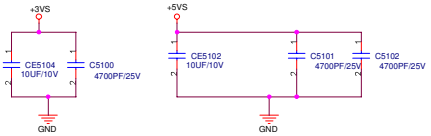


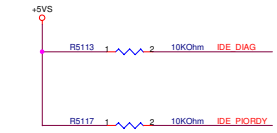
Default Group-CLKGEN

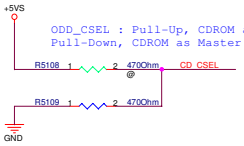
ASUSTeK COMPUTER INC. NB	Title : FAN	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 十月 二十日 13, 2007	Sheet 50 of 94	

SATA HDD

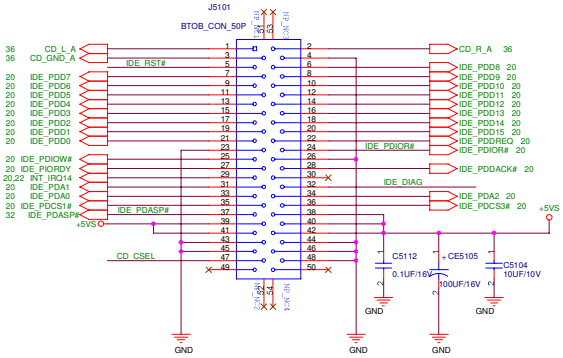








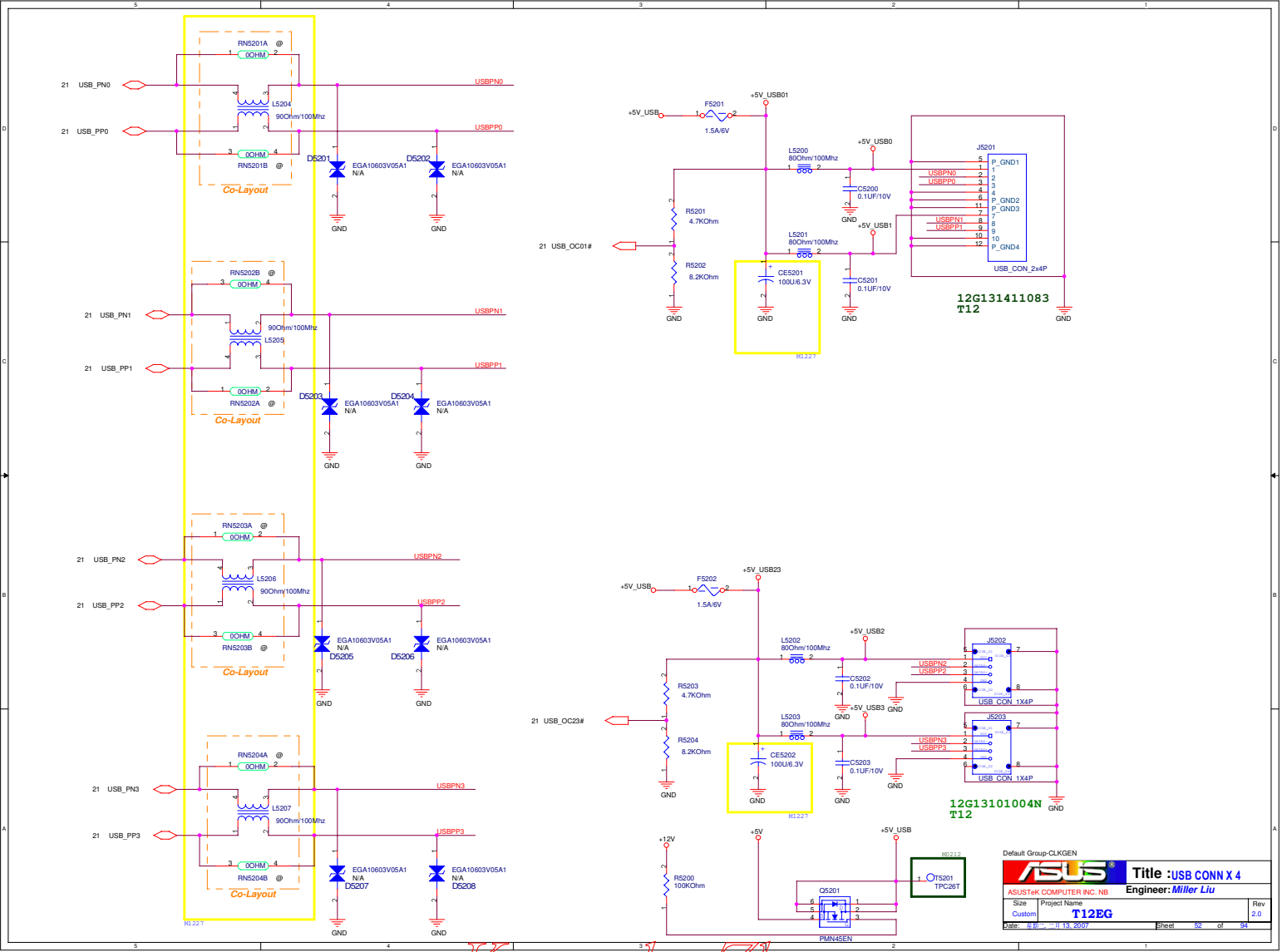
12G161210504
T12



CE5105 Only use 11G041210754

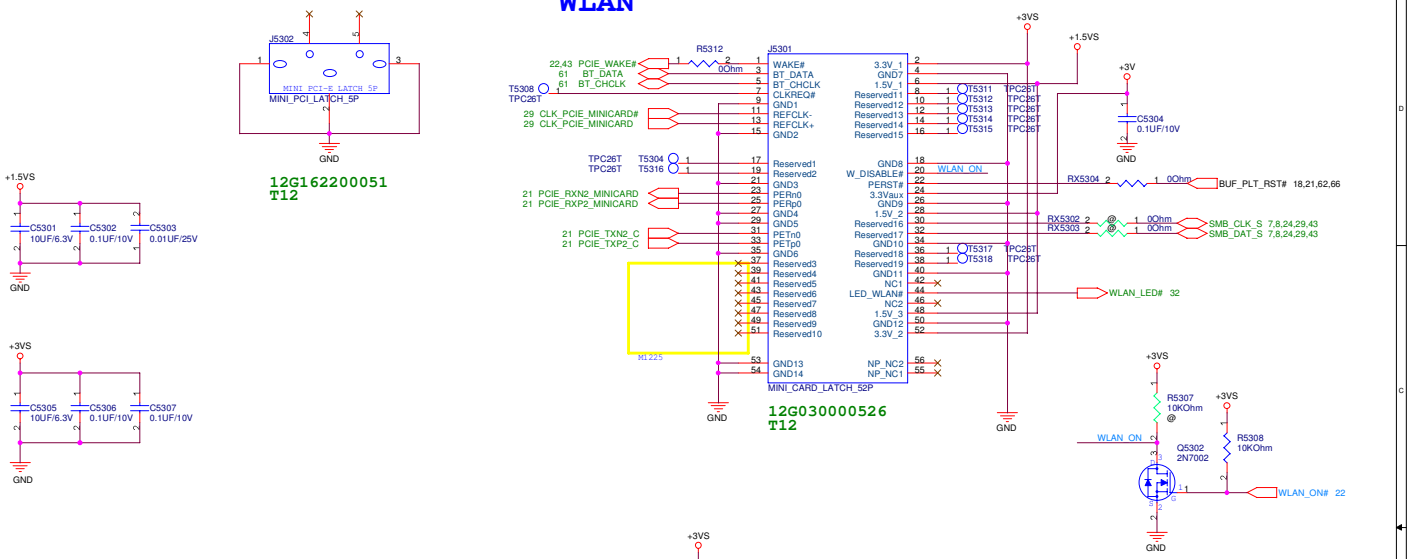
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 十月 13, 2007	Sheet 51 of 94	

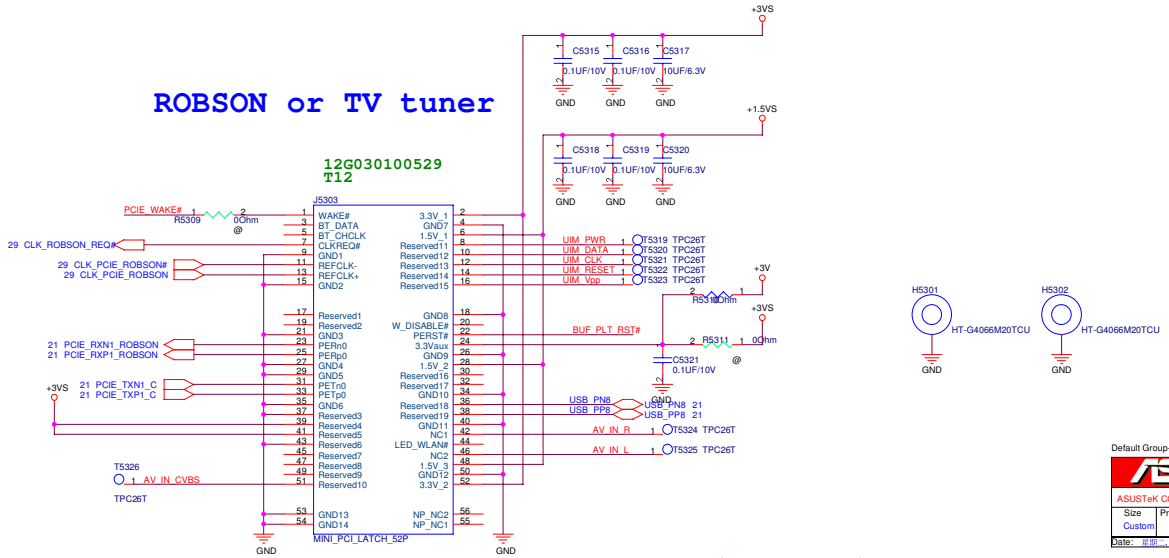


<< Kennedy_Zhang >>

WLAN



ROBSON or TV tuner



Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : MINICARD *2

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 一月 13, 2007 Sheet 53 of 94

<< Kennedy_Zhang >>

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 54 of 94

Default Group-CLKGEN

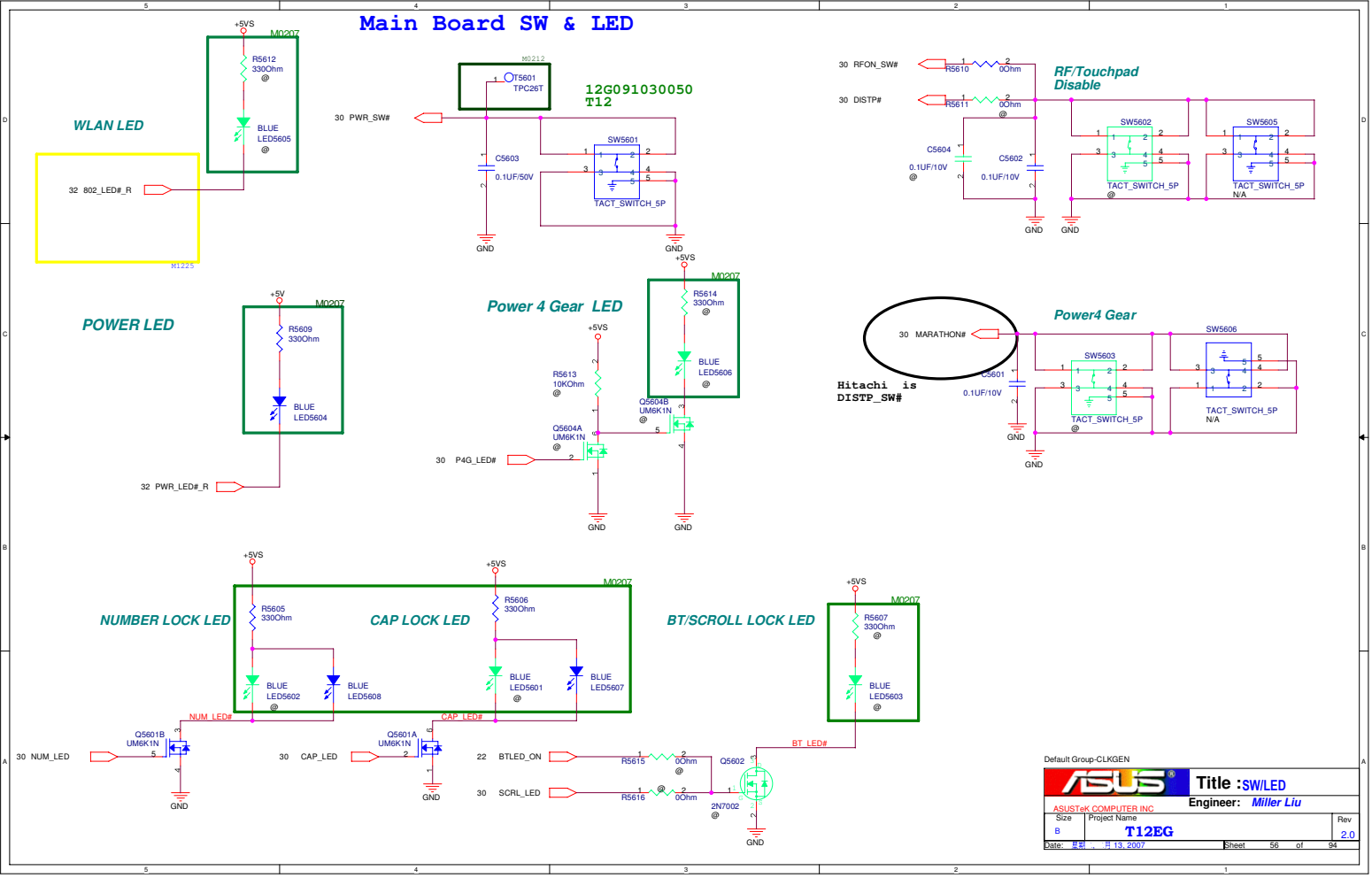
Title : NULL

ASUSTeK COMPUTER INC

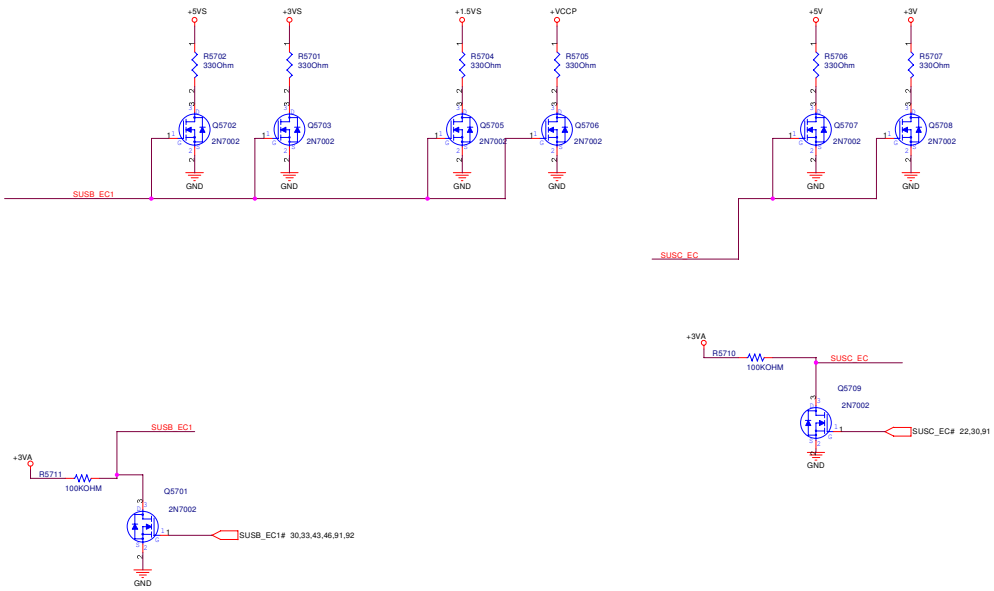
Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 55 of 94



<< Kennedy_Zhang >>



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

Title :DISCHARGE

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 四月 13, 2007 Sheet 57 of 94

<< Kennedy_Zhang >>

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 58 of 94

Default Group-CLKGEN

Title : NULL

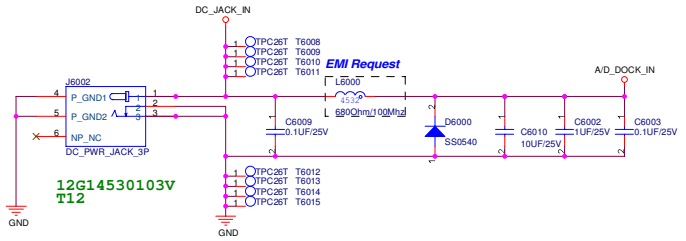
ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 59 of 94

DC-IN



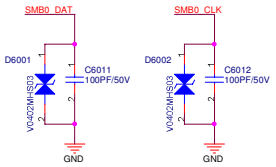
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# don't connect to Battery Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#, BAT2_CNT1#, BAT2_CNT2# must connect to Battery Connector.

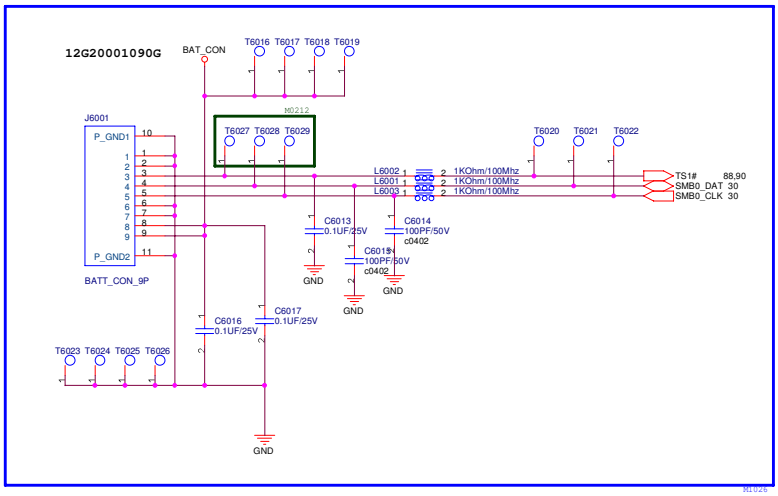


Note:

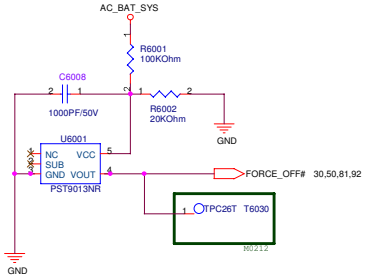
When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

Battery Connector



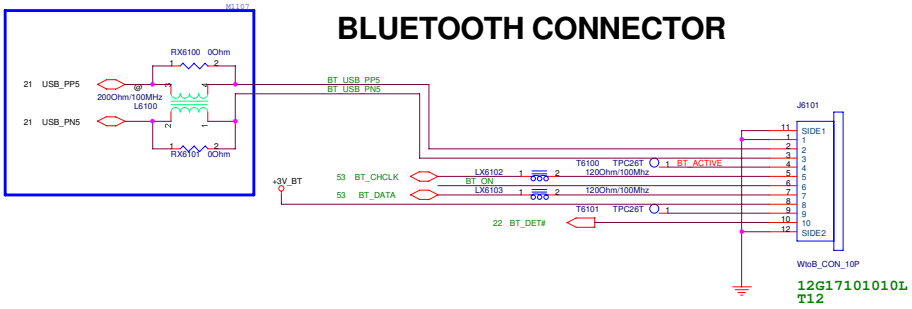
Without Battery & Pull out Adapter



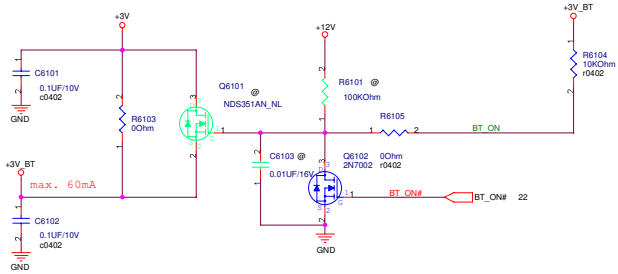
Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB	Title : DCIN/Batt conn.	
	Engineer: *Miller Liu*	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 星期二, 一月 13, 2007	Sheet 60 of 94	

BLUETOOTH CONNECTOR



12G17101010L
T12

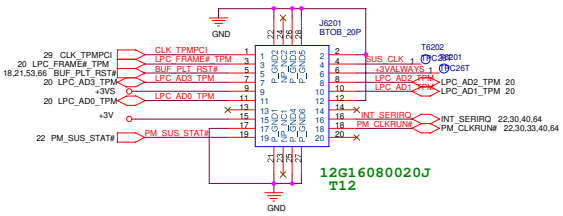


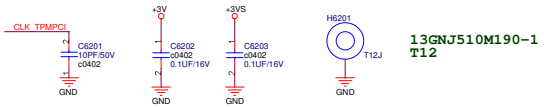
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 十月二十日 13, 2007	Sheet 61 of 94	

<< Kennedy_Zhang >>

TPM Connector





Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

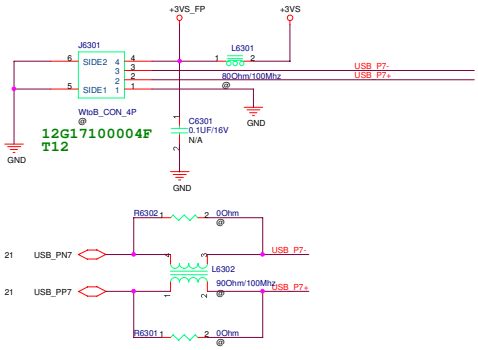
Title : TPM

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 日 13, 2007 Sheet 62 of 94

<< Kennedy_Zhang >>



Default Group-CLKGEN

ASUSTeK COMPUTER INC. NB

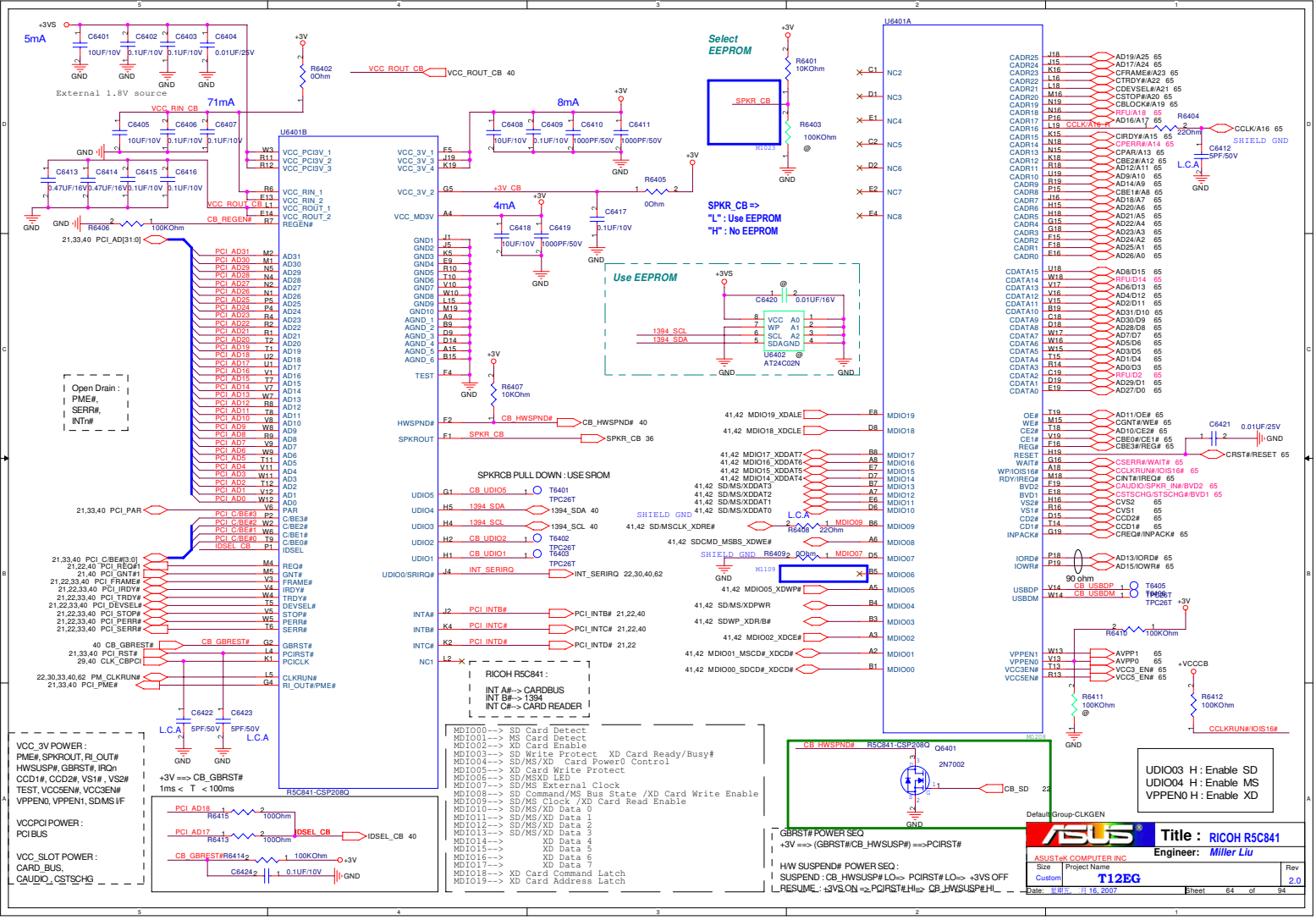
Title : Finger Print

Engineer: Miller Liu

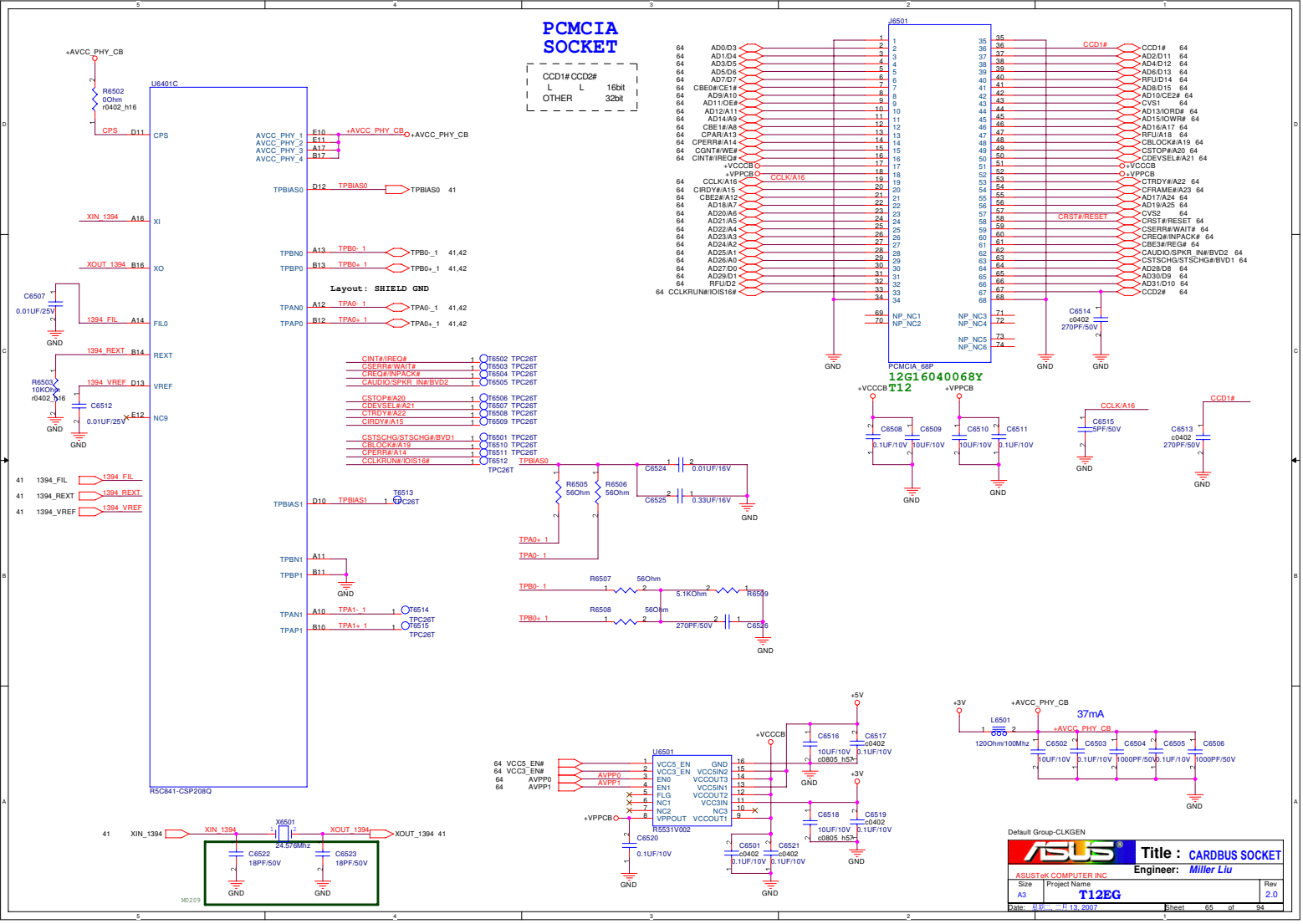
Size	Project Name	Rev
Custom	T12EG	2.0

Date: 日期 , 日 13, 2007 Sheet 63 of 94

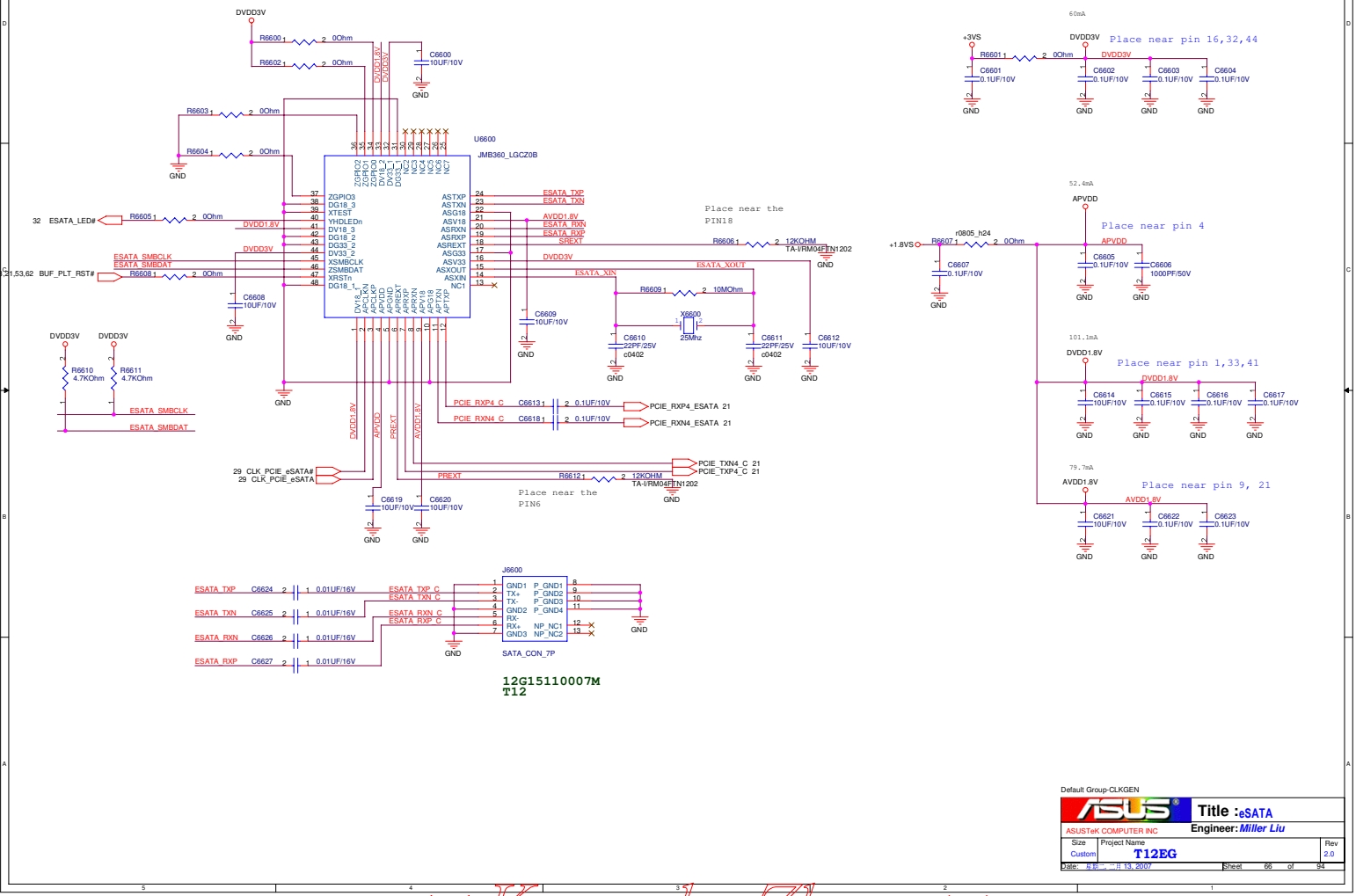
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



12G15110007M
T12

Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : eSATA	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12EG	Rev: 2.0
Date: 十月 二, 二十 13, 2007	Sheet 66 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD23	2	A
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

Default Group-CLKGEN

ASUSTeK COMPUTER INC

Title : RESOURCE

Engineer: Miller Liu

Size	Project Name	Rev
Custom	T12EG	2.0

Date: 星期二, 二月 13, 2007 Sheet 67 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 68 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 69 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 70 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 71 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 72 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 73 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 74 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 75 of 94

Default Group-CLKGEN

Title : Null

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
Custom	SANTAROSA	2.0

Date: 星期一, 一月 13, 2007 Sheet 76 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 77 of 94

Default Group-CLKGEN

Title : NULL

ASUSTeK COMPUTER INC

Engineer: Miller Liu

Size	Project Name	Rev
A	T12Eg	2.0

Date: 星期二, 二月 13, 2007 Sheet 78 of 94

Change Note:

R1.1 :

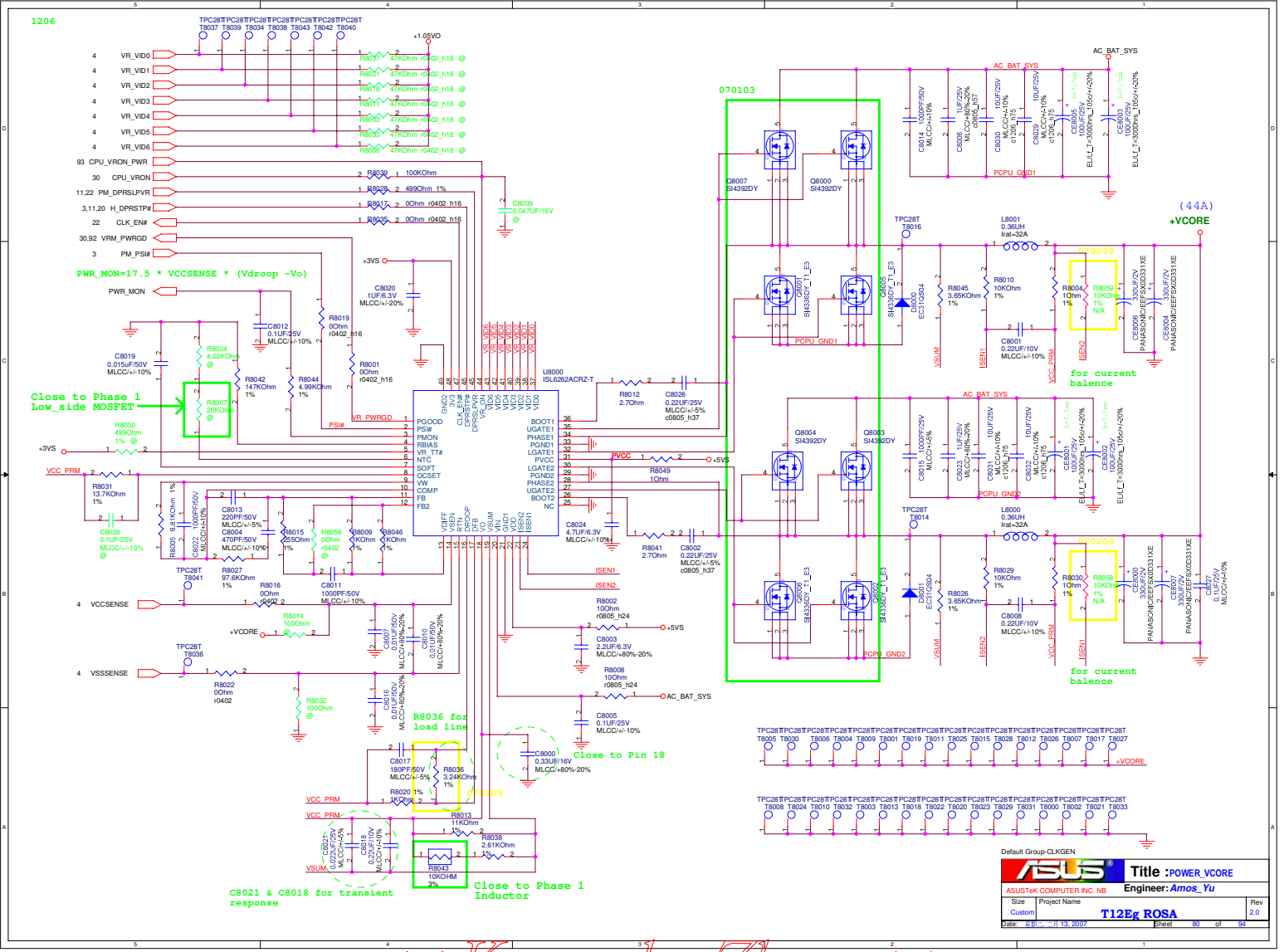
1. Change CON0801 SM-Bus address to A2.
2. Unmount R2936.(SELLCD_27# =1)
3. RX2227 connect to GND.(Do not use Intel LAN)
4. Add R6415 to connect PCI_AD18(for R5C832).
5. Remove CON5301 Debug Pin.
6. Change CON4501.14 to VSYNC_CON.
7. Change CON3702 pin define(RL SWAP).
8. Change R2914 from 220 ohm to 390 ohm.
9. Mount C2920-22,C2924,C2925,C4618-19,L5204-07, Unmount RN5201-04 for EMI requst.
10. Add R4517,R4517,R4518 to prevent CON4501 short ground issue.
11. Change C0701,C0706,C0801,C0809 to R0701,R0702,R0802,R0803(68.9 ohm).
12. Change RNX4501-04 from 0 to 22ohm, and add R4519-4522(100 ohm).
13. SWAP SUSB_EC1#,SUSB_EC2#.

R2.0 :

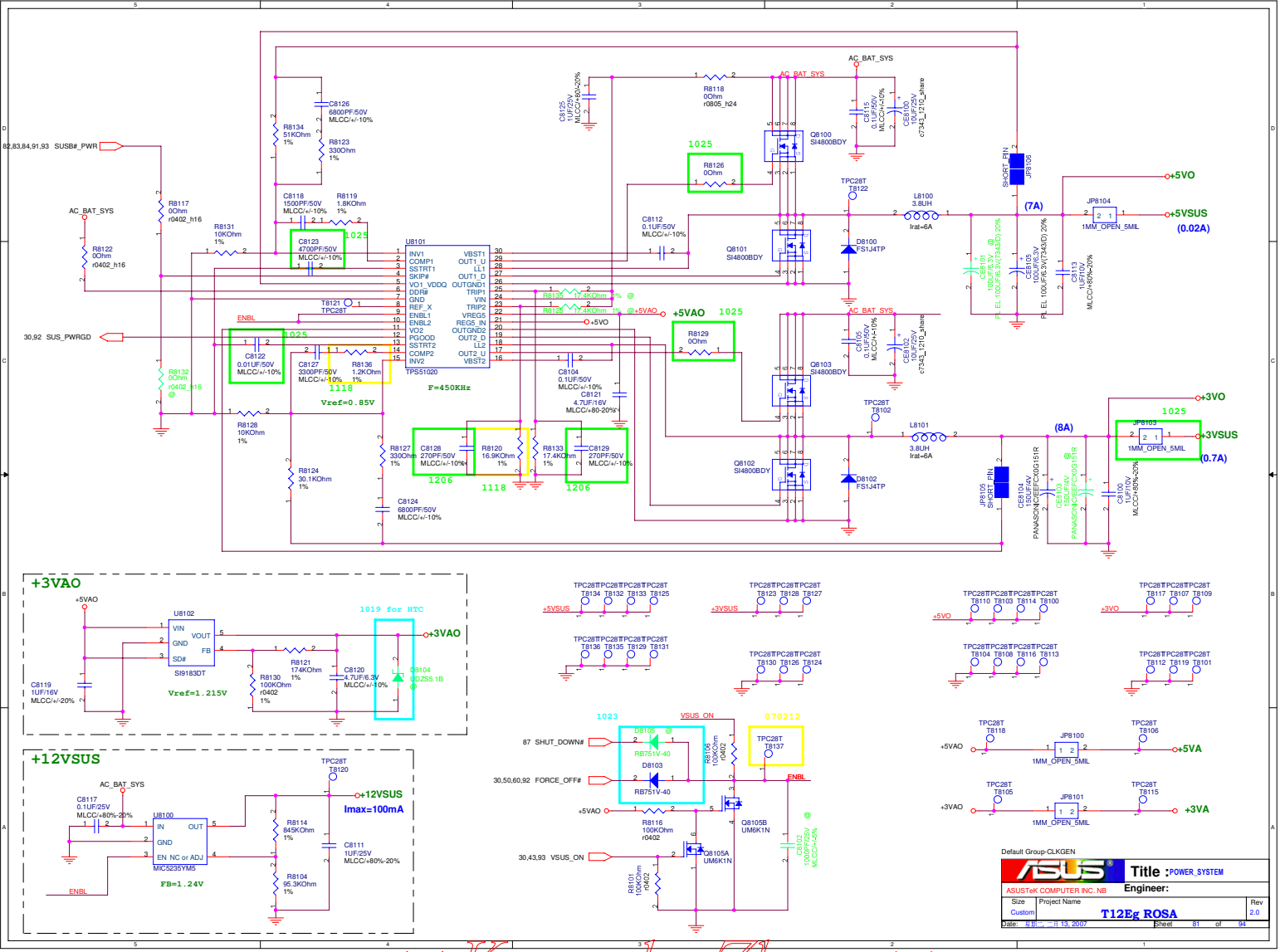
1.Change Audio LDO(P36) and Audio AMP(P37).
2.Change CB_SD# to CB_SD (high active) to fix windows progress bar issue(P64).
3.Change LED color from Green to Blue (P56).
4.Change +3VS_832 to connect +3V to fix 1394 S3 issue (P41).
5.Change C6522,C6523 from 20pf to 18pf (ITTI suggestion).(P65).
6.Change C2002,C2005 from 22pf to 12pf (FUJICOM suggestion).(P20).
7.Change C3016,C3017 from 5pf to 15pf (FUJICOM suggestion).(P30).
8.Change R3313 from 2.49K to 2.43K to fix LAN low output peak voltage issue.(P33).

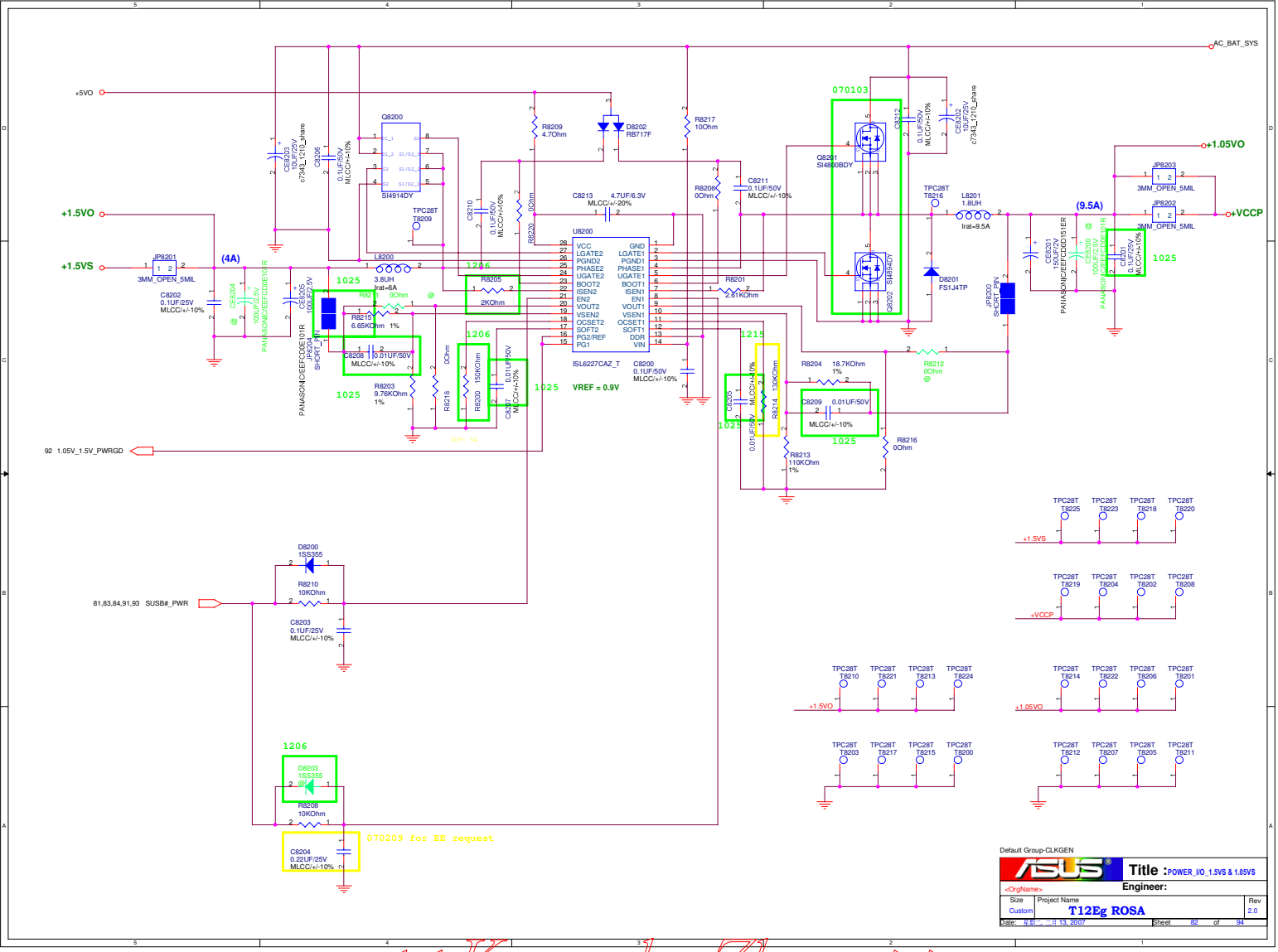
Default Group-CLKGEN

ASUSTeK COMPUTER INC	Title : NULL	
	Engineer: Miller Liu	
Size: Custom	Project Name: T12Eg	Rev: 2.0
Date: 十月 十一日 16, 2007	Sheet 79 of 94	

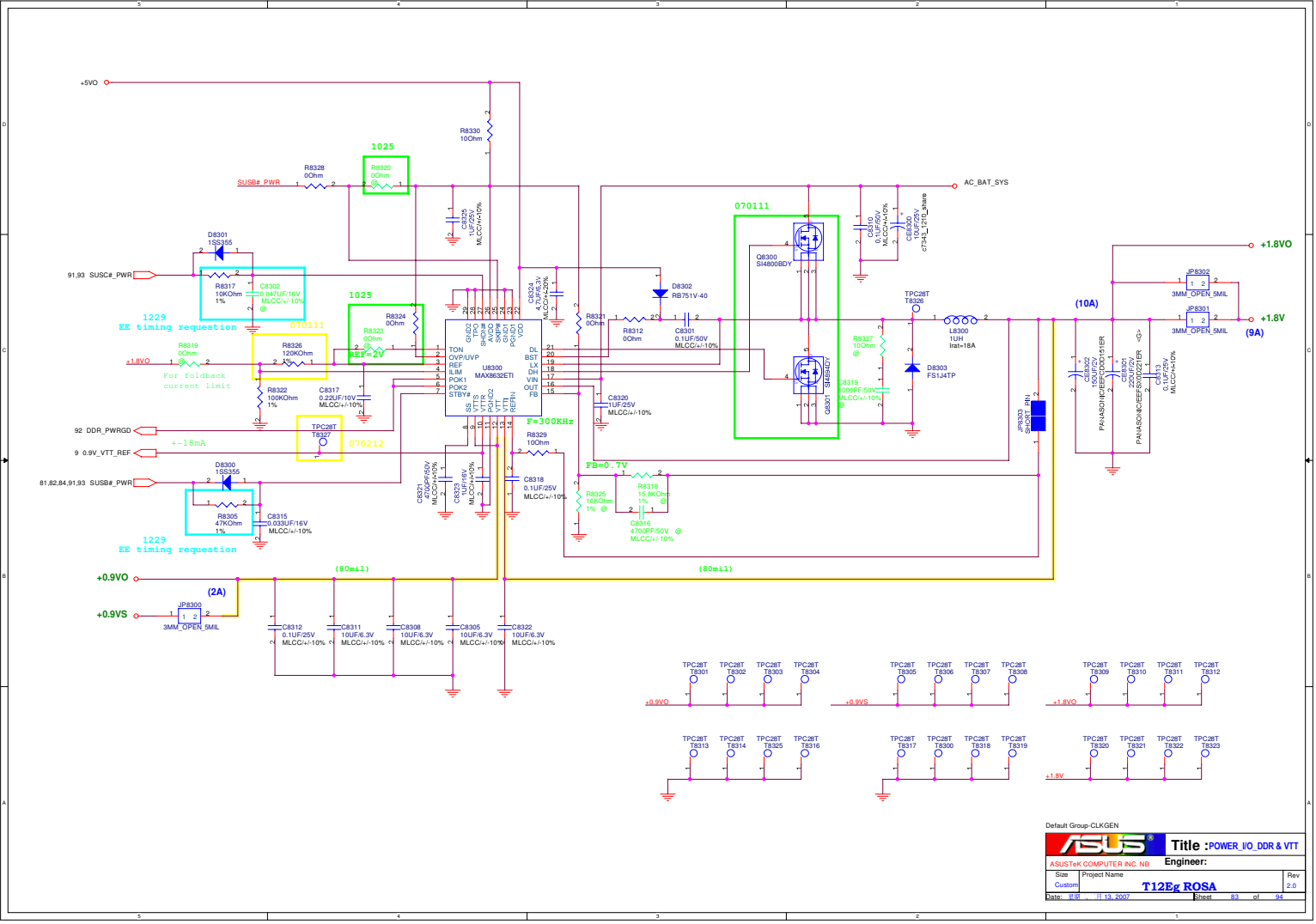


<< Kennedy_Zhang >>



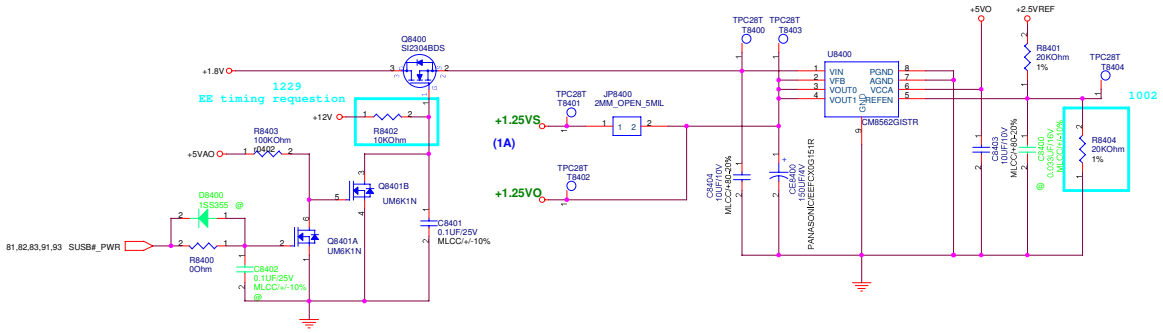


<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

+1.25VS



Default Group-CLKGEN

Title : POWER_I/O_1.25VS		
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 星期一, 二月 13, 2007	Sheet 84 of 94	

Default Group-CLKGEN

Title : POWER_VGA_CORE & RAM

Engineer:

<OrgName>

Size	Project Name	Rev
C	ROSA	1.1

Date: 星期二, 十月 13, 2007 Sheet 65 of 94

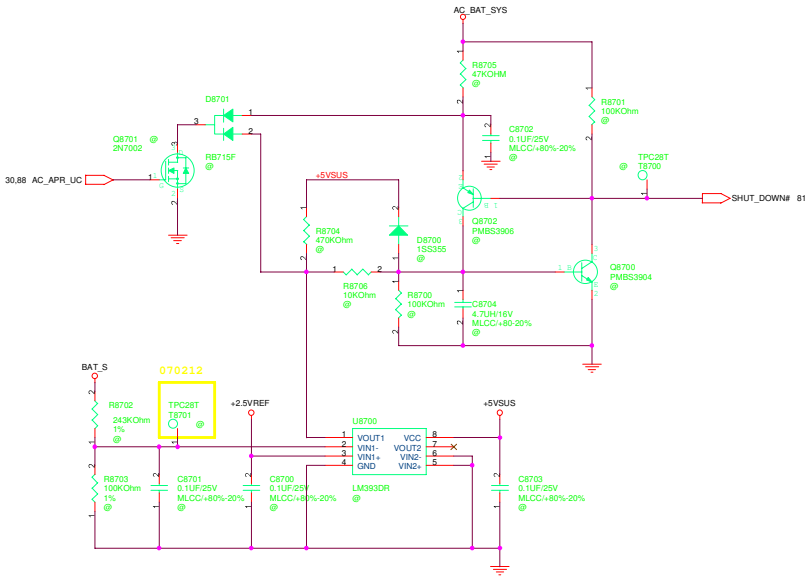
<< Kennedy_Zhang >>

Default Group-CLKGEN

<OrgName>	Title : N/A Engineer:	
Size: B	Project Name: ROSA	Rev: 1.1
Date: 星期一, 月 13, 2007	Sheet 86 of 94	

<< Kennedy_Zhang >>

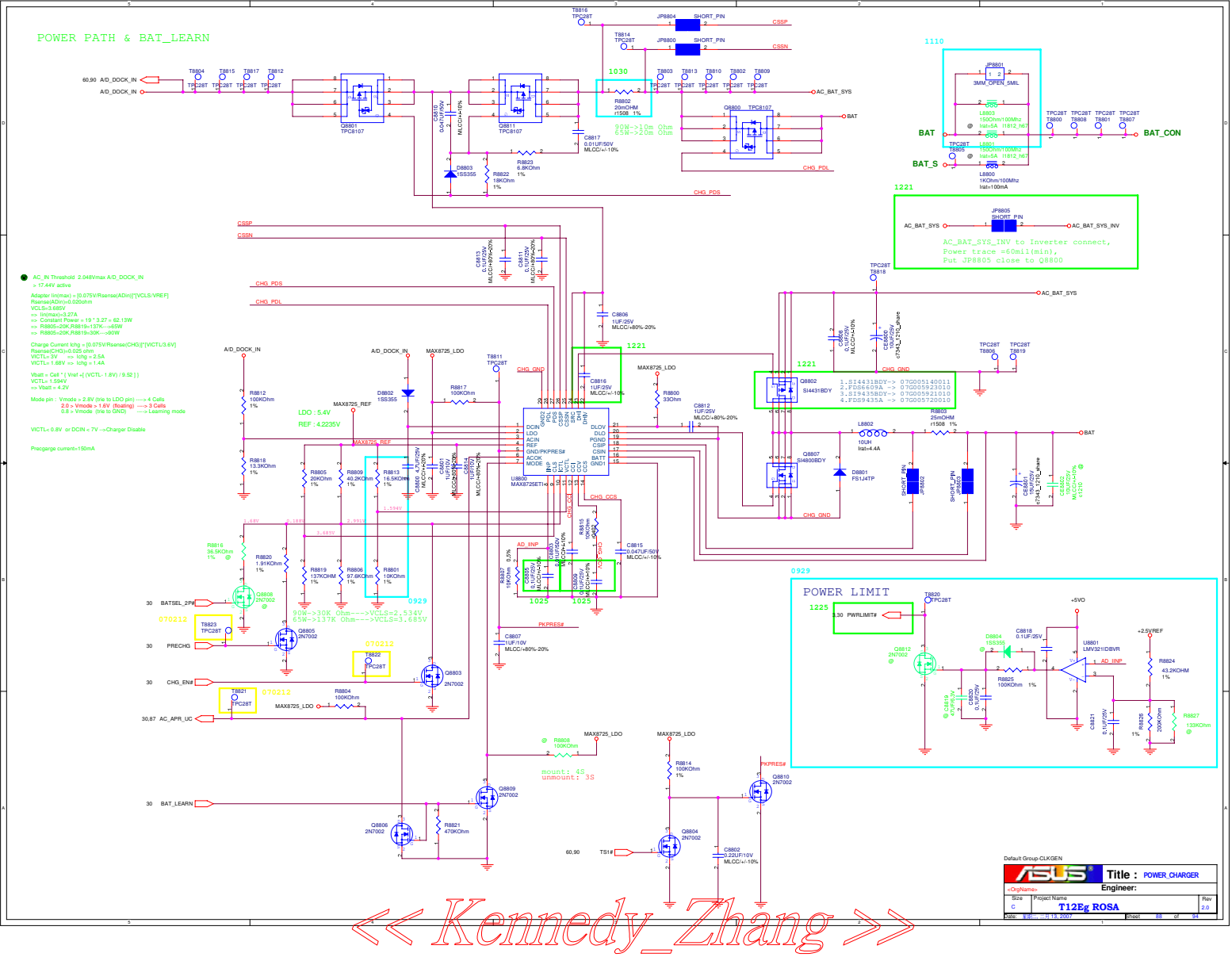
PIC only



Default Group-CLKGEN

ASUS	Title : POWER_SHUTDOWN#	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 日期二, 一月 13, 2007	Sheet 87 of 94	

<< Kennedy_Zhang >>


POWER PATH & BAT_LEARN
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.020ohm
VCLS=3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R8805=20K,R8819=137K-->65W
=> R8805=20K,R8819=39K-->90W
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL -1.8V) / 9.52]]
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (Yrie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (Yrie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=150mA
POWER LIMIT
AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800
90W->10m Ohm
65W->20m Ohm
90W->30K Ohm--->VCLS=2.534V
65W->137K Ohm--->VCLS=3.685V
mount: 4S
unmount: 3S
LDO : 5.4V
REF : 4.2235V
Default Group-CLKGEN
Title : POWER_CHARGER
Engineer:
T12Eg ROSA
Kennedy_Zhang

Default Group-CLKGEN

Title : N/A

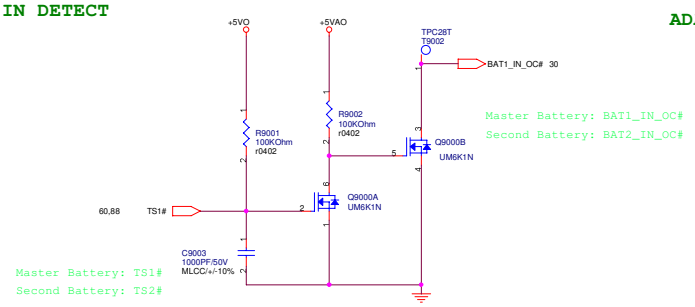
<OrgName>

Engineer:

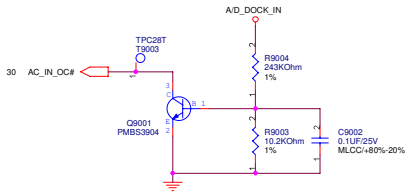
Size	Project Name	Rev
Custom	ROSA	1.1

Date: 星期二, 一月 13, 2007 Sheet 89 of 94

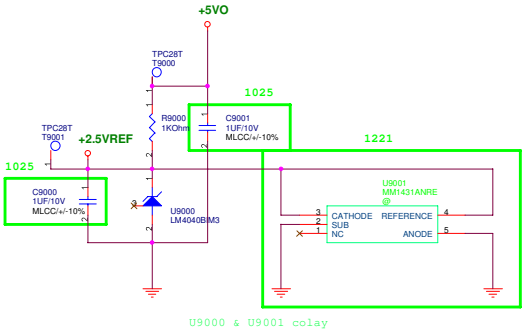
BATTERY IN DETECT



ADAPTER IN DETECT



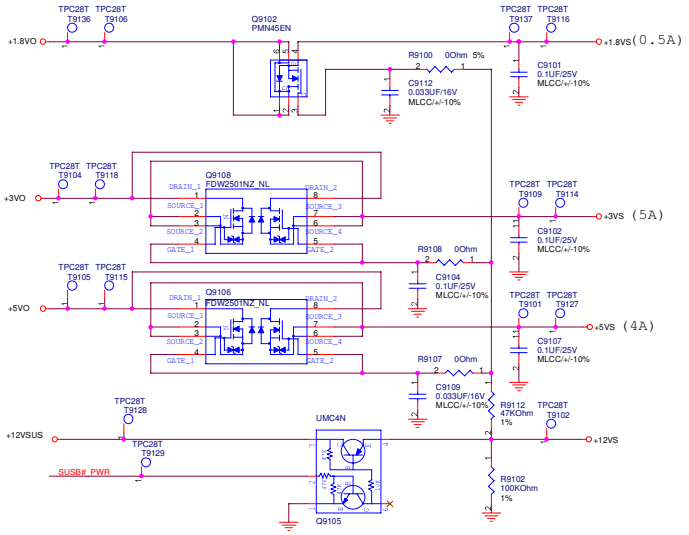
+2.5VREF



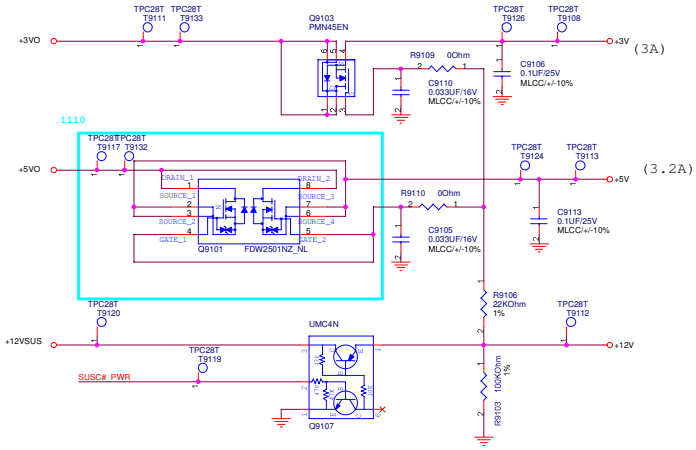
Default Group-CLKGEN

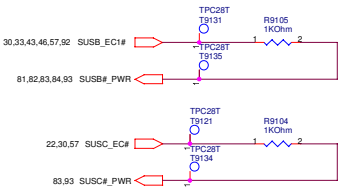
ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 十月 13, 2007	Sheet 90 of 94	

SUSB#_PWR POWER



SUSC#_PWR POWER

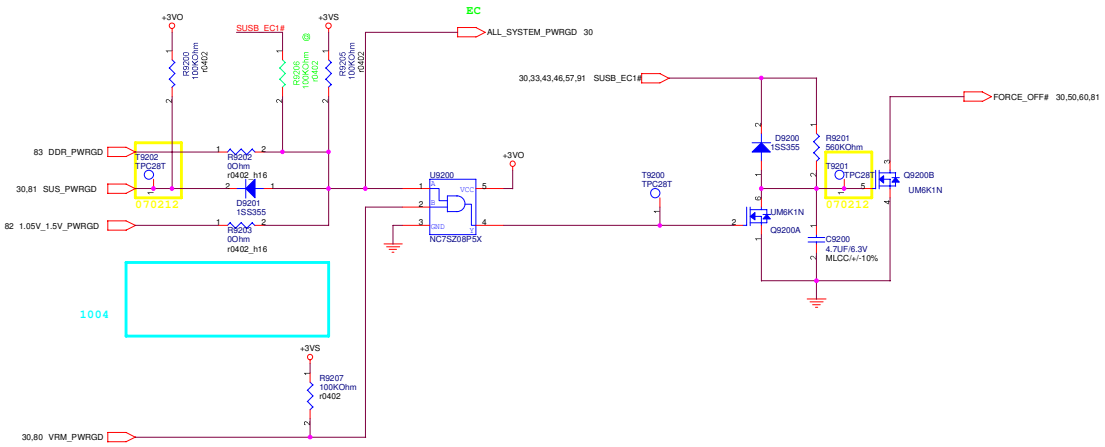




Default Group-CLKGEN

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 十月 13, 2007	Sheet 91 of 94	

POWER GOOD DETECTER



Default Group-CLKGEN

Title : POWER_PROTECT		
<OrgName>	Engineer:	
Size: Custom	Project Name: T12Eg ROSA	Rev: 2.0
Date: 日期二, 一月 13, 2007	Sheet 92 of 94	

AC_BAT_SYS — AC_BAT_SYS 60,80,81,82,83,87,88

BAT — BAT 88

BAT_CON — BAT_CON 60,88

+2.5VREF — +2.5VREF 84,87,88,90

+3VA — +3VA 20,22,30,46,50,57,81

+5VAO — +5VAO 81,84,90

+5VO — +5VO 81,82,83,84,88,90,91

+5VSUS — +5VSUS 23,32,81,87

+5V — +5V 15,32,46,52,56,57,65,91

+5VS — +5VS 23,24,32,36,37,38,45,50,51,56,57,80,91

+3VO — +3VO 81,91,92

+3VSUS — +3VSUS 21,22,23,30,33,37,43,81

+3V — +3V 21,22,35,40,41,44,53,57,61,62,64,65,91

+3VS — +3VS 3,7,8,11,12,15,18,22,23,24,29,30,32,36,40,42,43,45,46,50,51,53,57,62,63,64,66,80,91,92

+12VSUS — +12VSUS 81,91

+12V — +12V 37,42,52,61,84,91

+12VS — +12VS 46,91

+1.8VO — +1.8VO 83,91

+1.8V — +1.8V 7,8,9,11,14,15,83,84

+1.8VS — +1.8VS 18,66,91

+0.9VS — +0.9VS 9,83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,82

+VCCP — +VCCP 4,10,12,14,15,20,23,29,57,82

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 4,15,20,21,23,43,53,57,82

+VCORE — +VCORE 4,80

1004

+1.25VS — +1.25VS 11,15,23,84

FOR POWER TEST

070108

+3VA

JP9300 — SGL_JUMP — CPU_VRON_PWR 80

JP9301 — SGL_JUMP — SUSB#_PWR — SUSB#_PWR 81,82,83,84,91

JP9302 — SGL_JUMP — SUSC#_PWR — SUSC#_PWR 83,91

JP9303 — SGL_JUMP — VSUS_ON — VSUS_ON 30,43,81

Default Group-CLKGEN

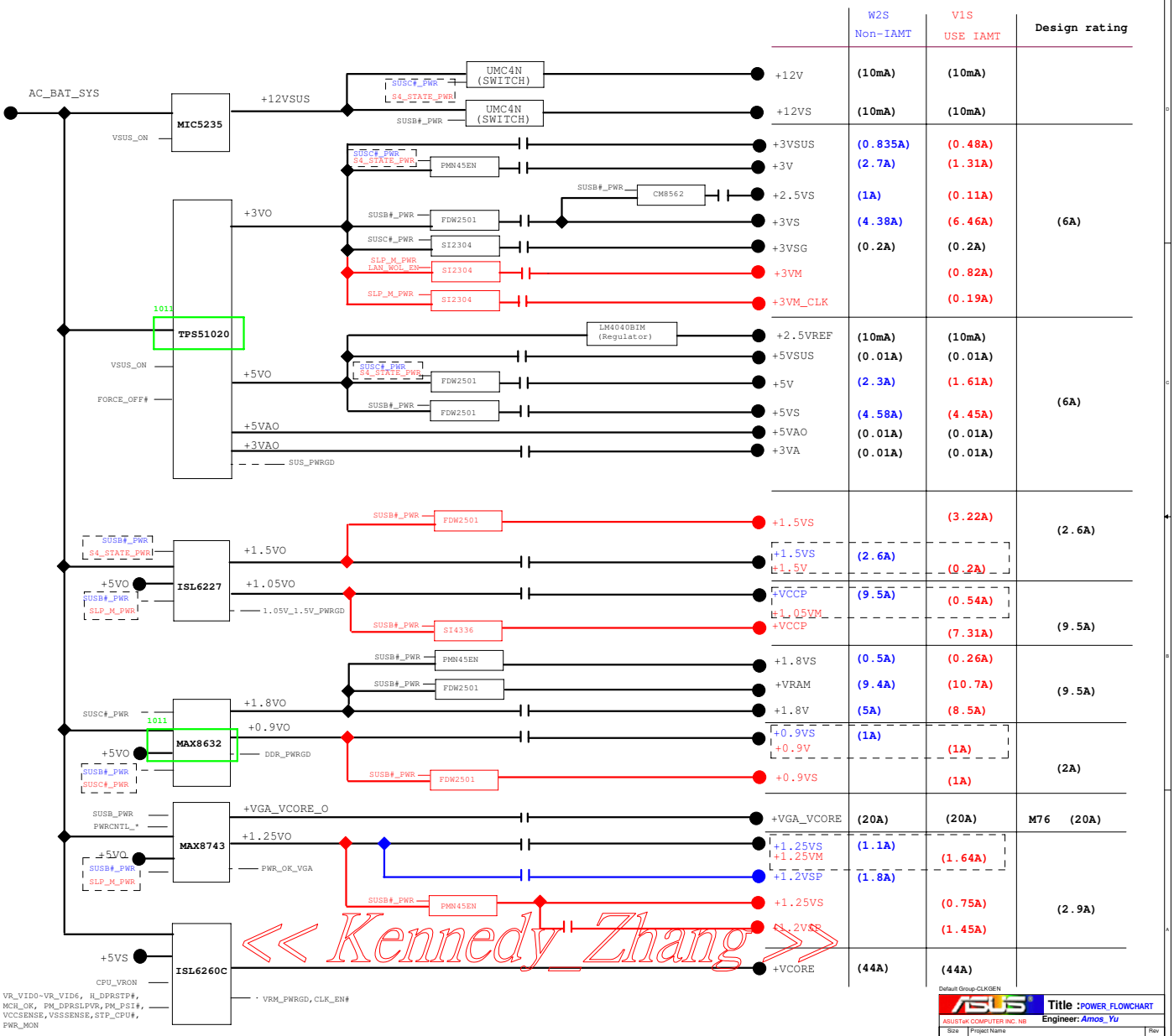
Title : POWER_SIGNAL

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12Eg ROSA	2.0

Date: 十月 13, 2007 Sheet 93 of 94

<< Kennedy_Zhang >>



	W2S Non-IAMT	V1S USE IAMT	Design rating
+12V	(10mA)	(10mA)	
+12VS	(10mA)	(10mA)	
+3VSUS	(0.835A)	(0.48A)	
+3V	(2.7A)	(1.31A)	
+2.5VS	(1A)	(0.11A)	
+3VS	(4.38A)	(6.46A)	(6A)
+3VSG	(0.2A)	(0.2A)	
+3VM		(0.82A)	
+3VM_CLK		(0.19A)	
+2.5VREF	(10mA)	(10mA)	
+5VSUS	(0.01A)	(0.01A)	
+5V	(2.3A)	(1.61A)	
+5VS	(4.58A)	(4.45A)	(6A)
+5VAO	(0.01A)	(0.01A)	
+3VA	(0.01A)	(0.01A)	
+1.5VS		(3.22A)	(2.6A)
+1.5VS	(2.6A)		
+1.5V		(0.2A)	
+VCCP	(9.5A)	(0.54A)	
+1.05VM			(9.5A)
+VCCP		(7.31A)	
+1.8VS	(0.5A)	(0.26A)	
+VRAM	(9.4A)	(10.7A)	(9.5A)
+1.8V	(5A)	(8.5A)	
+0.9VS	(1A)		
+0.9V		(1A)	(2A)
+0.9VS		(1A)	
+VGA_VCORE	(20A)	(20A)	M76 (20A)
+1.25VS	(1.1A)		
+1.25VM		(1.64A)	
+1.2VSP	(1.8A)		
+1.25VS		(0.75A)	(2.9A)
+1.2VSP		(1.45A)	
+VCORE	(44A)	(44A)	

Default Group:CLKGEN

ASUSTeK COMPUTER INC. NB

Title : POWER_FLOWCHART

Engineer: Amos_Yu

Size: Custom | Project Name: ROSA | Rev: 1.0

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