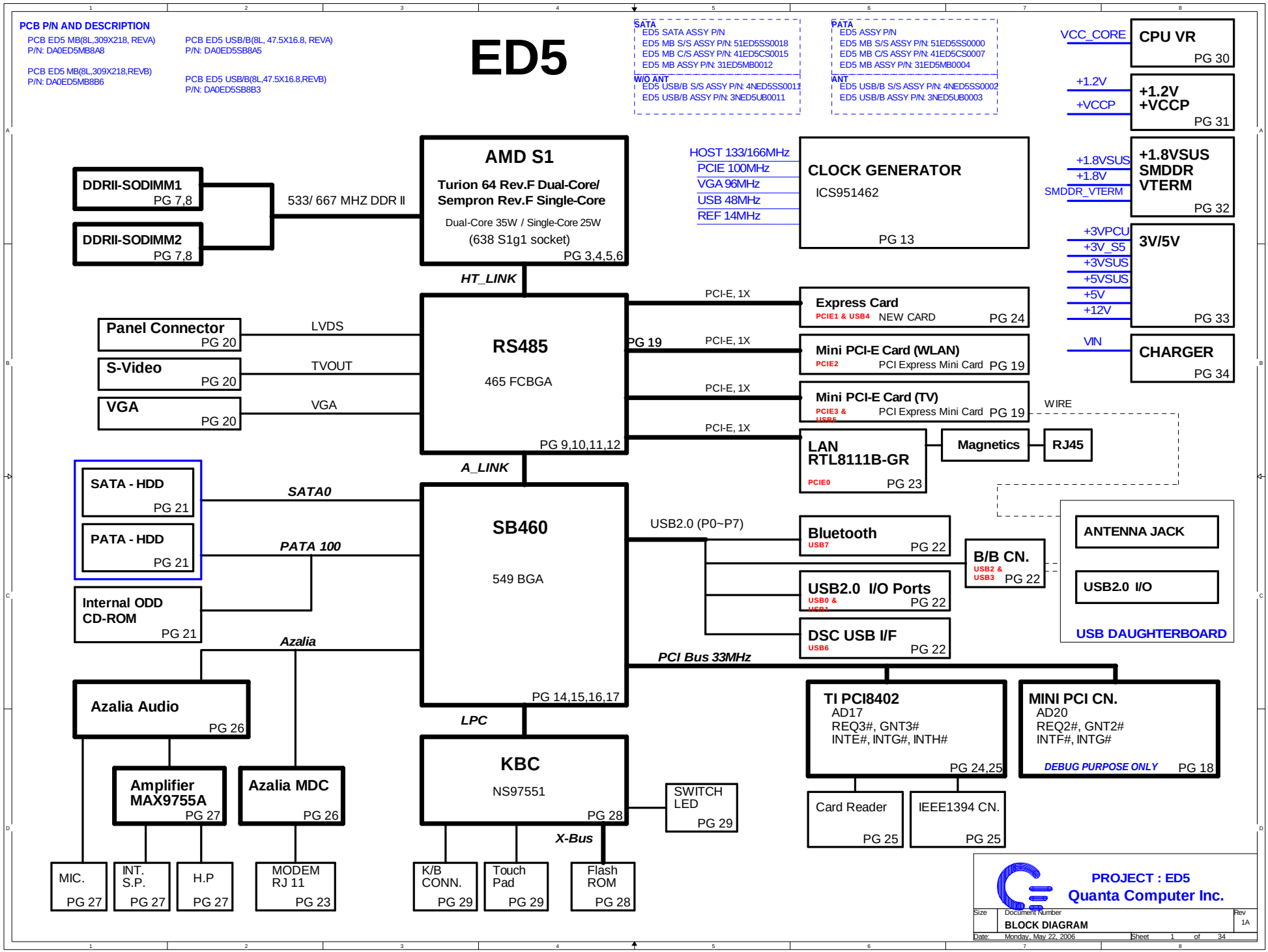
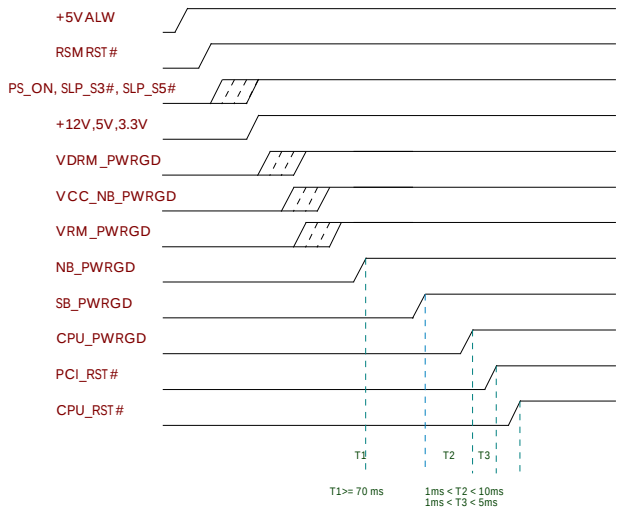


TABLE OF CONTENTS

	POWER	VOLTAGE	ACTIVE SCOPE	ROUTING	PAGE
SYSTEM	+12V	+12V	OFF IN S3-S5	PLANE	41
	-12V	-12V	OFF IN S3-S5	TRACE 20 MIL	41
	+5V	+5V	OFF IN S3-S5	PLANE	41
	+3.3V	+3.3V	OFF IN S3-S5	PLANE	41
	+5VALW	+5V	S0-S5	PLANE/ 50 MIL	41
	+3.3VALW	+3.3V	S0-S5	TRACE 30 MIL	41
	+1.8VALW	+2.5V	S0-S5	TRACE 30 MIL	21
	+5V_DUAL	+5V	S0-S5	PLANE/ 100 MIL	41
	+3.3V_DUAL	+3.3V	S0-S5	PLANE/ 50 MIL	41
CPU	VCCCORE	VID[0..6]	OFF IN S3-S5	PLANE+COPER	37
	VCCP	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VCCA	+1.5V	OFF IN S3-S5	TRACE 20 MIL	38
RC485 NB	VCC_NB	+1.2V/1.0V	OFF IN S3-S5	PLANE+COPER	39
	VDD_CPU	+1.05V	OFF IN S3-S5	PLANE+COPER	38
	VDD_MEM	+1.8V	S0-S3	PLANE+COPER	40
	VDD18	+1.8V	OFF IN S3-S5	TRACE 20 MIL	12
	VDDA18	+1.8V	OFF IN S3-S5	COPPER	12
	VDDA12	+1.2V	OFF IN S3-S5	PLANE+COPPER	12
	AVDD	+3.3V	OFF IN S3-S5	TRACE 20 MIL	11
	AVDDQ	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	PLVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LPVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	11
	LVDDR	+1.8V	OFF IN S3-S5	TRACE 30 MIL	11
	VDDR3	+3.3V	OFF IN S3-S5	TRACE 30 MIL	11
	VTT_DDR	+0.9V	OFF IN S3-S5	COPPER	40
	VDD_CLK	+3.3V	OFF IN S3-S5	COPPER	14
SB460 SB	+3.3V_SB	+3.3V	OFF IN S3-S5	PLANE	21
	+1.8V_SB	+1.8V	OFF IN S3-S5	PLANE	21
	+3.3VALW_SB	+3.3V	S0-S5	PLANE	21
	+1.8VALW_SB	+1.8V	S0-S5	PLANE	21
	+1.8V_SUB_PHY	+1.8V	S0-S5	TRACE 30 MIL	21
	AVDD_CK	+1.8V	OFF IN S3-S5	TRACE 10 MIL	21
	V5_REF	+5V	OFF IN S3-S5	TRACE 10 MIL	21
	CPU-PWR	+1.05V	OFF IN S3-S5	TRACE 20 MIL	21
	PCIE_PVDD	+1.8V	OFF IN S3-S5	TRACE 20 MIL	18
	PCIE_VDDR	+1.8V	OFF IN S3-S5	PLANE+COPER	18
	+1.8V_ATA	+1.8V	OFF IN S3-S5	PLANE	20
	PLLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	XTLVDD_ATA	+1.8V	OFF IN S3-S5	TRACE 20 MIL	20
	AVDD_USB_TX	+1.8V	S0-S5	PLANE+COPER	19
	AVDD_USB_RX	+1.8V	S0-S5	PLANE+COPER	19
	+3.3V_AVDDC	+3.3V	S0-S5	TRACE 20 MIL	19
	V_BAT	+3.0V	--	TRACE 10 MIL	18

BONEFISH POWER UP SEQUENCE



PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
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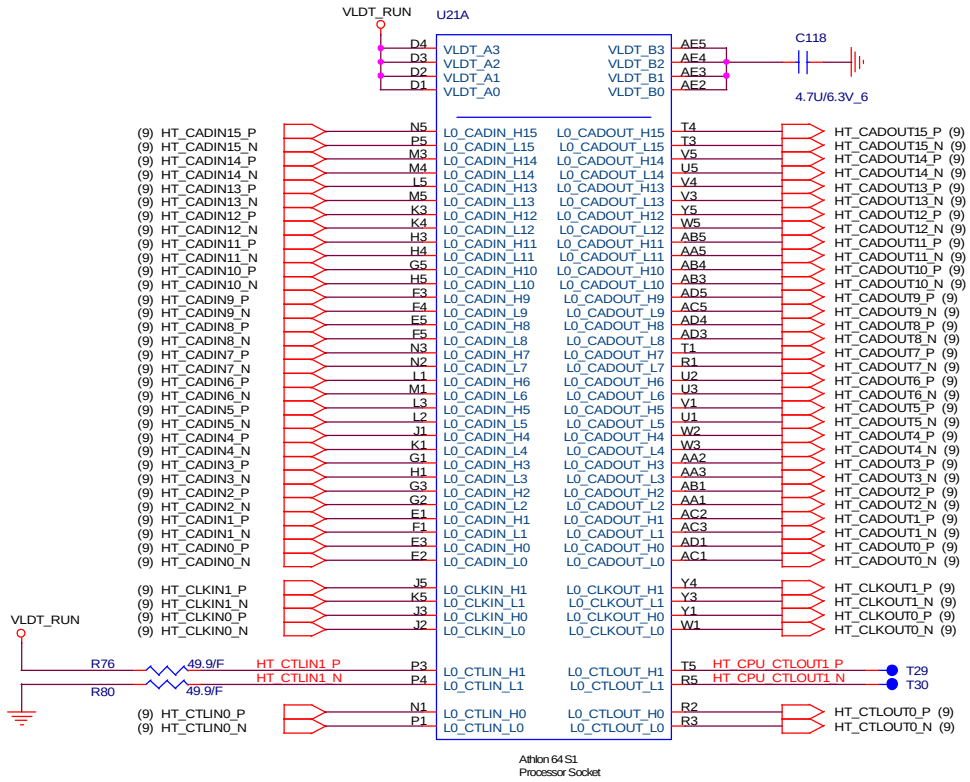
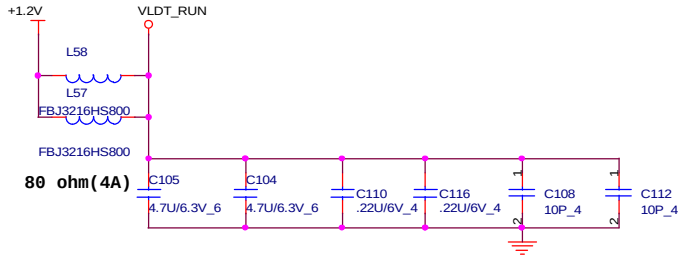
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



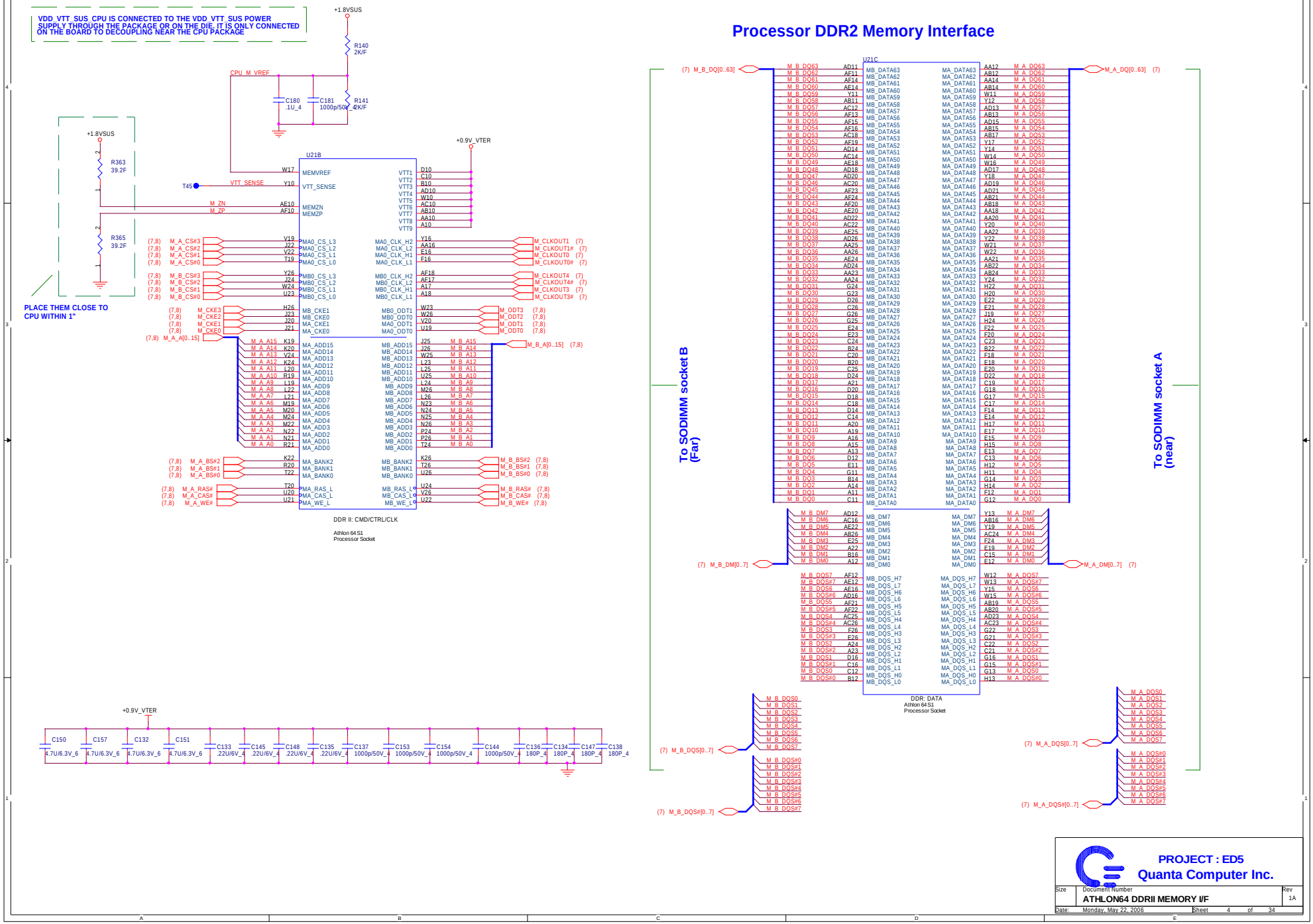


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
Date: Monday, May 22, 2006	Sheet 3 of 34	



ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

CPU_VDDA_RUN, L27 BLM18PG330SN1D, +2.5V
C163 4.7U/6.3V_6, C127 .22U/6V_4, C131 3900p/25V, C490 100U/6.3V_3528

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V R351 300, R349 *300, R347 300_4, CPU_SIC_R, CPU_SID_R

(13) CPUCLK C489 3900p/25V CPU_CLKIN_SC_P
R366 169F
(13) CPUCLK# C488 3900p/25V CPU_CLKIN_SC_N

VLDT_RUN
place them to CPU within 1"
R75 44.2F, R74 44.2F

To Power: (30) COREFB+V, (30) COREFB-

D3A:Add LEVEL-SHIFT circuit on PSI# that between CPU and POWER

+1.8V R545 10K_4, +3V R546 1K/F_4, PSI# Q39 MMBT3904, PWR_PSI# (39)

+1.8V R350 300_4, +3V, +1.8VSUS, R348 *4.7K/F_4 (ECN 2A Remove R348 for Power sequence), C487 .1U_4
(14,15) CPU_PWRGD, U20 NC7SZ08P5X_NL, CPU_ALL_PWROK

+1.8V R114 300_4, +1.8VSUS, C161 .1U_4
(11,14,15) LDT_STOP#, U9 NC7SZ08P5X_NL, CPU_LDTSTOP#

+1.8V R346 300_4, +1.8VSUS, C484 .1U_4
(14) LDT_RST#, (14,15,28) EC_PWRGD, R342 0_4, (11,28) NB_PWRGD, R343 0_4, U19 NC7SZ08P5X_NL, CPU_HT_RESET#

U21D

CPU_VDDA_RUN	F8 VDDA2	THERMTRIP_L	AF6 H_THERMTRIP#
	F9 VDDA1	PROCHOT_L	AC7 H_PROCHOT#
CPU_HT_RESET# T11	B7 RESET_L		
CPU_ALL_PWROK T11	A7 PWROK		
CPU_LDTSTOP# T46	F10 *LDTSTOP_L		
CPU_SIC_R	AF4 SIC	VID5	A5 VID5 (30)
CPU_SID_R	AF5 SID	VID4	C6 VID4 (30)
		VID3	A6 VID3 (30)
		VID2	A4 VID2 (30)
CPU_HTREF1	P6 HT_REF1	VID1	C5 VID1 (30)
CPU_HTREF0	R6 HT_REF0	VID0	B5 VID0 (30)
		CPU_PRESENT_L	AC6 CPU_PRESENT#
T10	F6 VDD_FB_H	PSI_L	A3 PSI#
	E6 VDD_FB_L		
T21 CPU_VDDIO_SUS_FB_H	W9 VDDIO_FB_H		
T23 CPU_VDDIO_SUS_FB_L	Y9 VDDIO_FB_L		
CPU_CLKIN_SC_P	A9 CLKIN_H		
CPU_CLKIN_SC_N	A8 CLKIN_L		
CPU_DBRDY	G10 DBRDY		
CPU_TMS	AA9 TMS	DBREQ_L	E10 CPU_DBREQ#
CPU_TCK	AC9 TCK		
CPU_TRST#	AD9 TRST_L		
CPU_TDI	AF9 TDI	TDO	AE9 CPU_TDO
CPU_TEST25_H_BYPASSCLK_H	E9 TEST25_H	TEST29_H	C9 CPU_TEST29_H_FBCLKOUT_P, R92 80.6F
CPU_TEST25_L_BYPASSCLK_L	E8 TEST25_L	TEST29_L	C8 CPU_TEST29_L_FBCLKOUT_N
CPU_TEST19_PLLTEST0	G9 TEST19		
CPU_TEST18_PLLTEST1	H10 TEST18		
	AA7 TEST13		
	C2 TEST9	TEST24	AE7 CPU_TEST24_SCANCLK1
T37 CPU_TEST17_BP3	D7 TEST17	TEST23	AD7 CPU_TEST23_TSTUPD T113
T35 CPU_TEST16_BP2	E7 TEST16	TEST22	AE8 CPU_TEST22_SCANSHIFTEN
CPU_TEST15_BP1	F7 TEST15	TEST21	AB8 CPU_TEST21_SCANEN
CPU_TEST14_BP0	C7 TEST14	TEST20	AF7 CPU_TEST20_SCANCLK2
CPU_TEST12_SCANSHIFTENB	AC8 TEST12		
		TEST28_H	J7 CPU_TEST28_H_PLLCHRZ_P
T26 CPU_TEST07_ANALOG_T	C3 TEST7	TEST28_L	H8 CPU_TEST28_L_PLLCHRZ_N T36, T44
T20 CPU_TEST6_DIECRACKMON	AA6 TEST6	TEST27	AF8 CPU_TEST27_SINGLECHAIN
CPU_TEST5_THERMDC	W7 TEST5	TEST26	AE6 CPU_TEST26_BURNIN#
CPU_TEST4_THERMDA	W8 TEST4	TEST10	K8 CPU_TEST10_ANALOGOUT T42
CPU_TEST3_GATE0	Y6 TEST3	TEST8	C4 CPU_TEST08_DIG_T T24
T19 CPU_TEST2_DRAIN0	AB6 TEST2		
T50 CPU_RSVD_MA0_CLK3_P	P20 RSVD0	RSVD8	H16 CPU_MA_RESET# T48
T58 CPU_RSVD_MA0_CLK3_N	P19 RSVD1	RSVD9	B18 CPU_MB_RESET# T49
T55 CPU_RSVD_MA0_CLK0_P	N20 RSVD2		
T56 CPU_RSVD_MA0_CLK0_N	N19 RSVD3	RSVD10	R3 CPU_RSVD_VIDSTRB1 T28
		RSVD11	C1 CPU_RSVD_VIDSTRB0 T25
		RSVD12	H6 CPU_RSVD_VDDNB_FB_P T32
		RSVD13	G6 CPU_RSVD_VDDNB_FB_N T40
		RSVD14	D5 CPU_RSVD_CORE_TYPE T31
		RSVD15	R24
		RSVD16	W18
		RSVD17	R23
		RSVD18	A8
		RSVD19	U18
		RSVD20	U19
T57 CPU_RSVD_MB0_CLK3_P	R26 RSVD4		
T52 CPU_RSVD_MB0_CLK3_N	R25 RSVD5		
T53 CPU_RSVD_MB0_CLK0_P	P22 RSVD6		
T54 CPU_RSVD_MB0_CLK0_N	R22 RSVD7		

MISC

AMD NPT S1 SOCKET
Processor Socket

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

+1.8V R70 330_4, +1.8VSUS, Q10 MMBT3904, R73 300_4, H_PROCHOT#, R72 *0_4, CPU_EC_PROCHOT# (28), CPU_PROCHOT# (15)

SB_THERMTRIP# (15), separated input voltage 0104, R90, EC_PWRGD, R86 4.7K/F_4, Q11 *MMBT3904, R78 *330_4, Q12 MMBT3904, R84 300_4, H_THERMTRIP#, THERM_SYS_PWR (33)

+1.8VSUS

CPU_TEST27_SINGLECHAIN	R359	300_4
CPU_TEST26_BURNIN#	R352	300_4
CPU_PRESENT#	R354	1K/F_4
CPU_TEST25_H_BYPASSCLK_H	R87	510/F_4
CPU_TEST21_SCANEN	R356	300_4
CPU_TEST20_SCANCLK2	R353	300_4
CPU_TEST24_SCANCLK1	R355	300_4
CPU_TEST22_SCANSHIFTEN	R357	300_4
CPU_TEST12_SCANSHIFTENB	R358	300_4
CPU_TEST15_BP1	R91	300_4
CPU_TEST14_BP0	R85	300_4
CPU_TEST25_L_BYPASSCLK_L	R82	510/F_4
CPU_TEST19_PLLTEST0	R89	300_4
CPU_TEST18_PLLTEST1	R123	300_4

IF no use which Net need pull-up or down

HDT CONNECTOR

+1.8VSUS, R363 220_4, R360 220_4, R362 220_4, R124 220_4
CPU_DBREQ# T47, CPU_DBRDY T43, CPU_TCK T34, CPU_TMS T41, CPU_TDI T38, CPU_TRST# T39, CPU_TDO T33, LDT_RST# T63

PUT CLOSE ON LAYOUT

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

CPU H/W MONITOR

15 MIL
Address 98H
+3V R341 47/F_6, 3V_THM, C477 .1U_4
U17 G781: VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND; KBSMDAT, KBSMCLK
CPU_TEST5_THERMDC, CPU_TEST4_THERMDA, C479 2200P/50V_4
10 mil trace / 10 mil space
R340 10K_4, Q23 2N7002E-LF, To SB GPIO, MAX6648_AL# (15)
ECN E3B Change from 10K to 4.7K, R338 4.7K/F_4, Q21 2N7002E-LF, MBDATA_CPU (28)
R339 4.7K/F_4, Q22 2N7002E-LF, MBCLK_CPU (28)
R345 10K_4, To FAN, MAX6648_OV# (29)

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	2A
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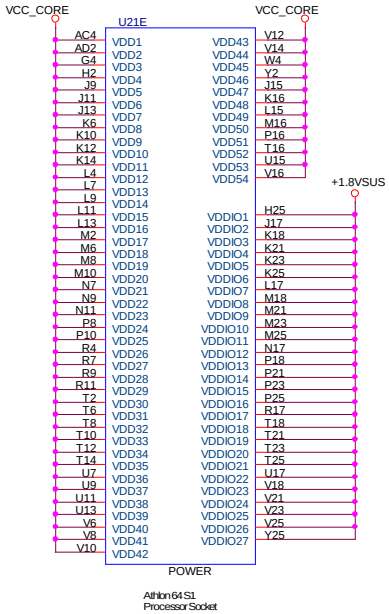

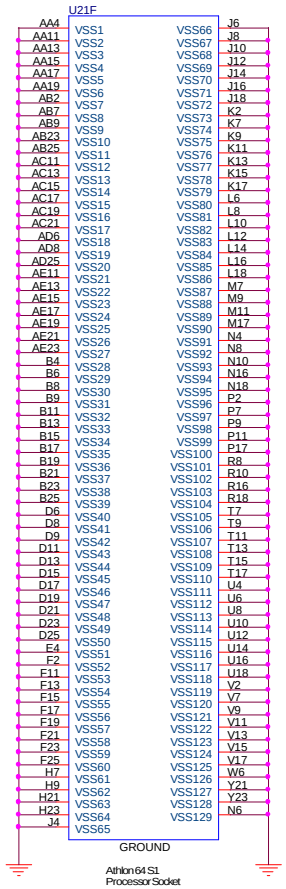

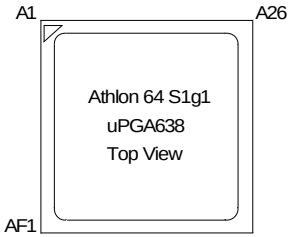

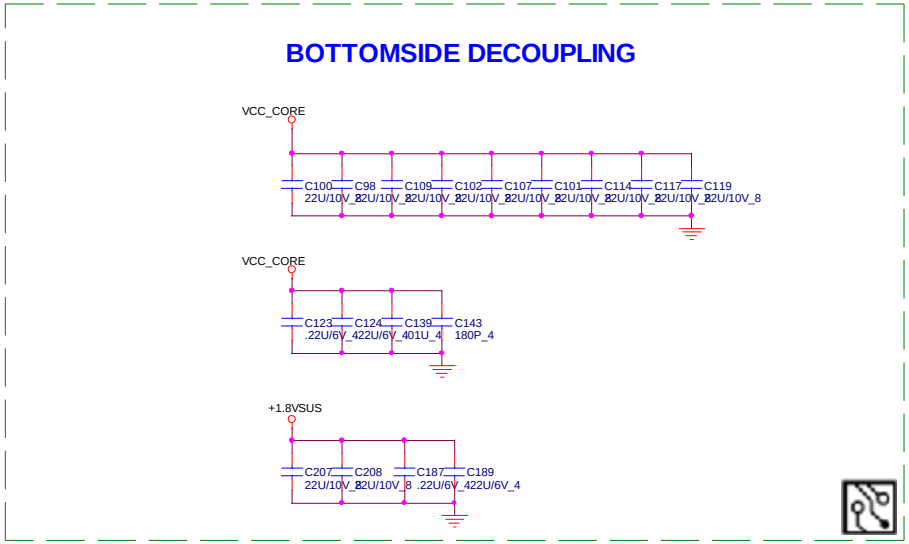

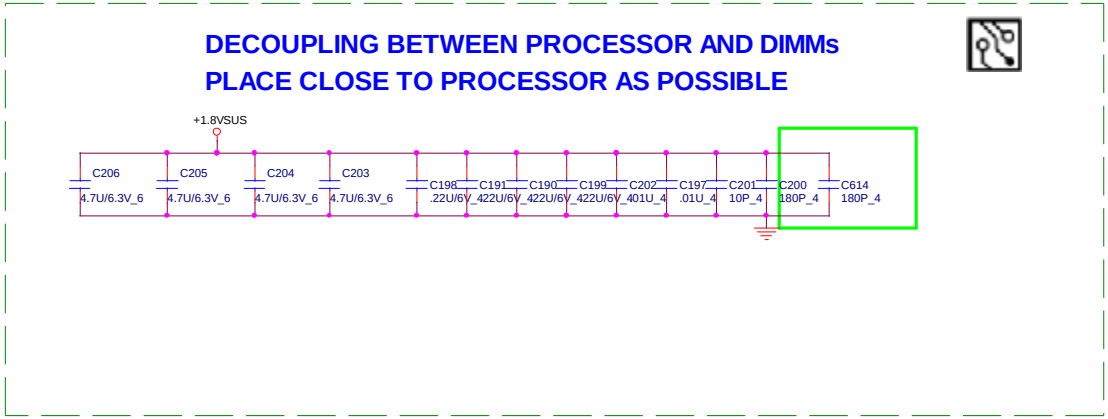

PROCESSOR POWER AND GROUND

PROJECT : ED5
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Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
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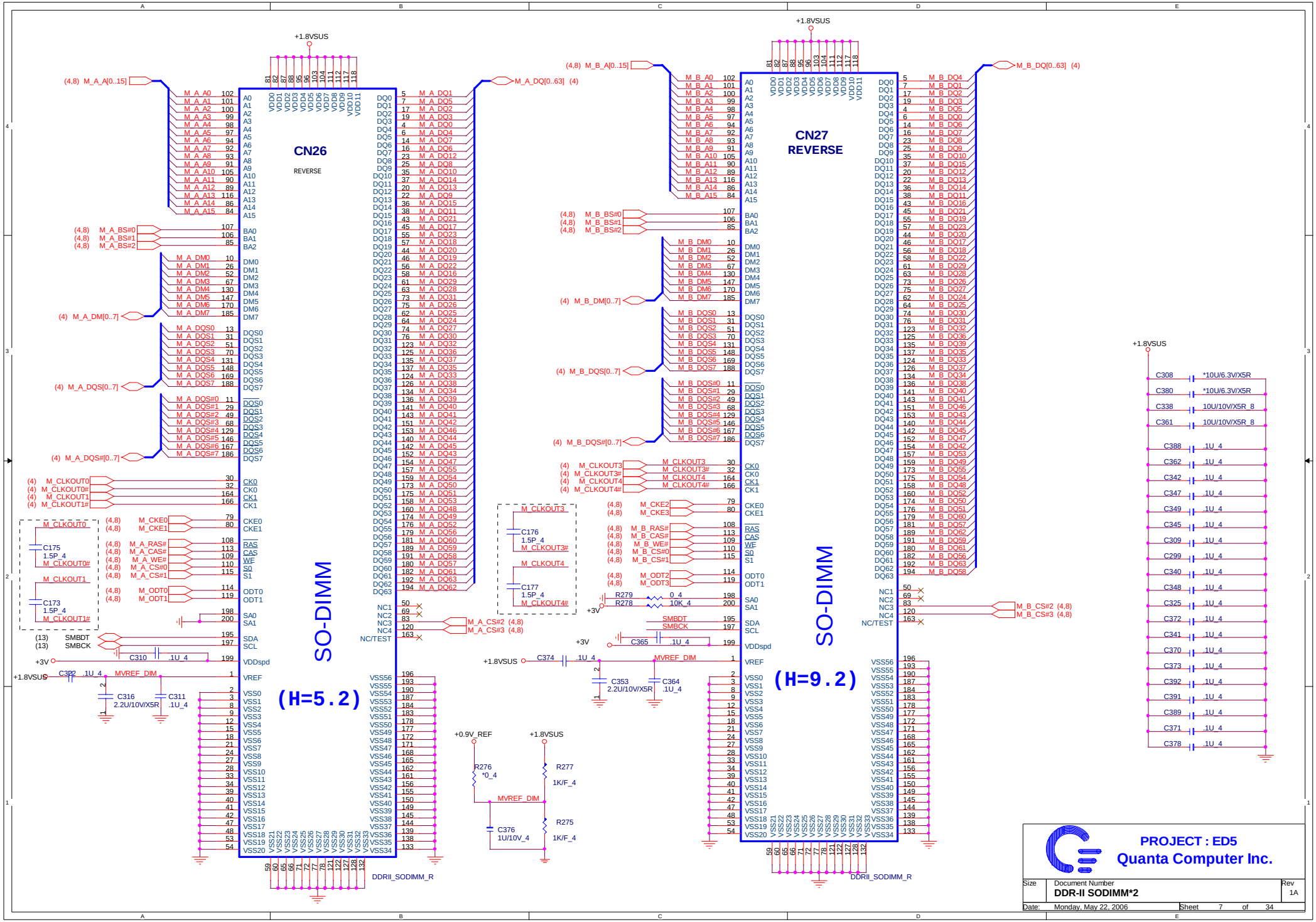

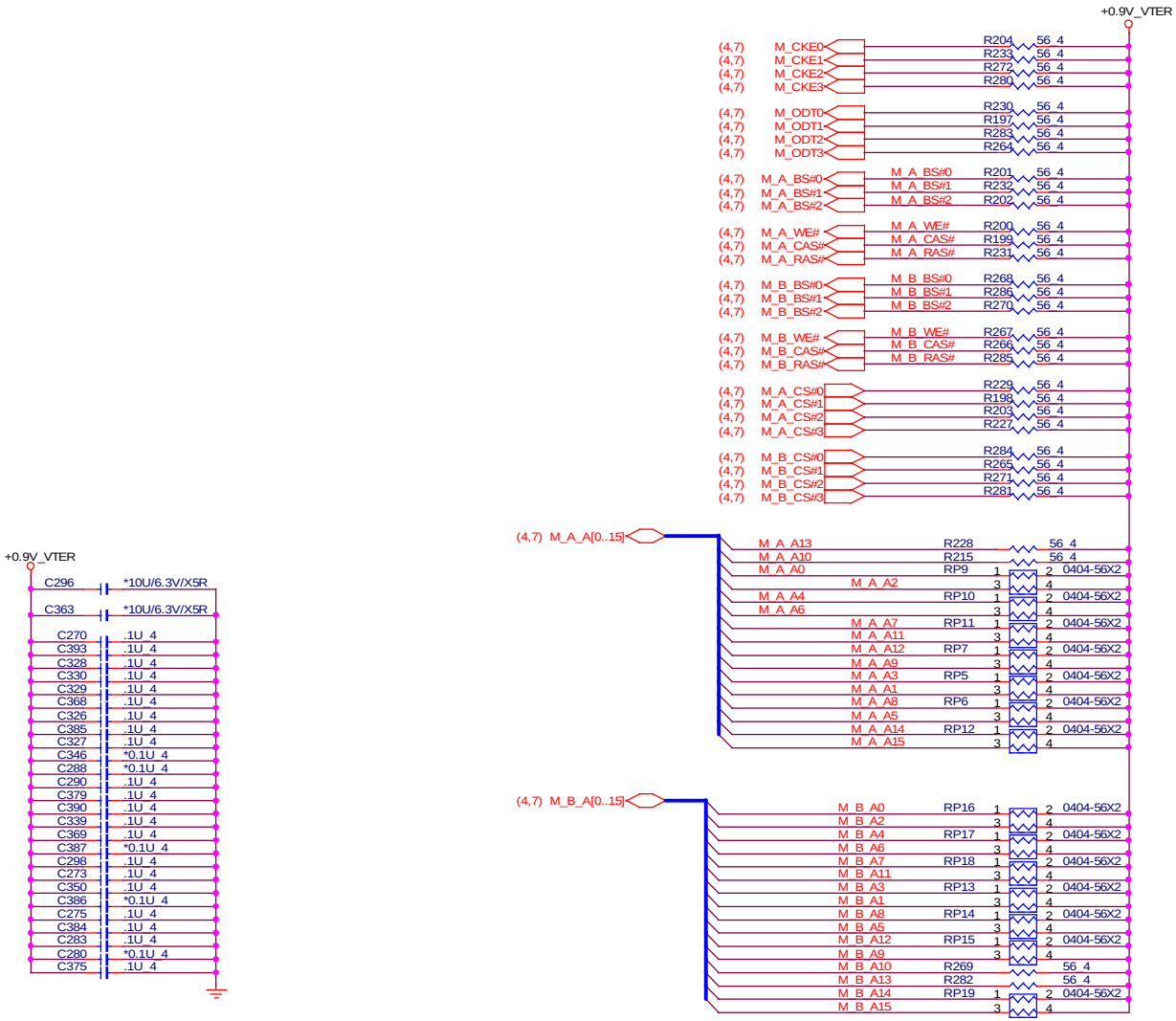

PROJECT : ED5
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Size	Document Number	Rev
	DDR-II TERMINATION	1A
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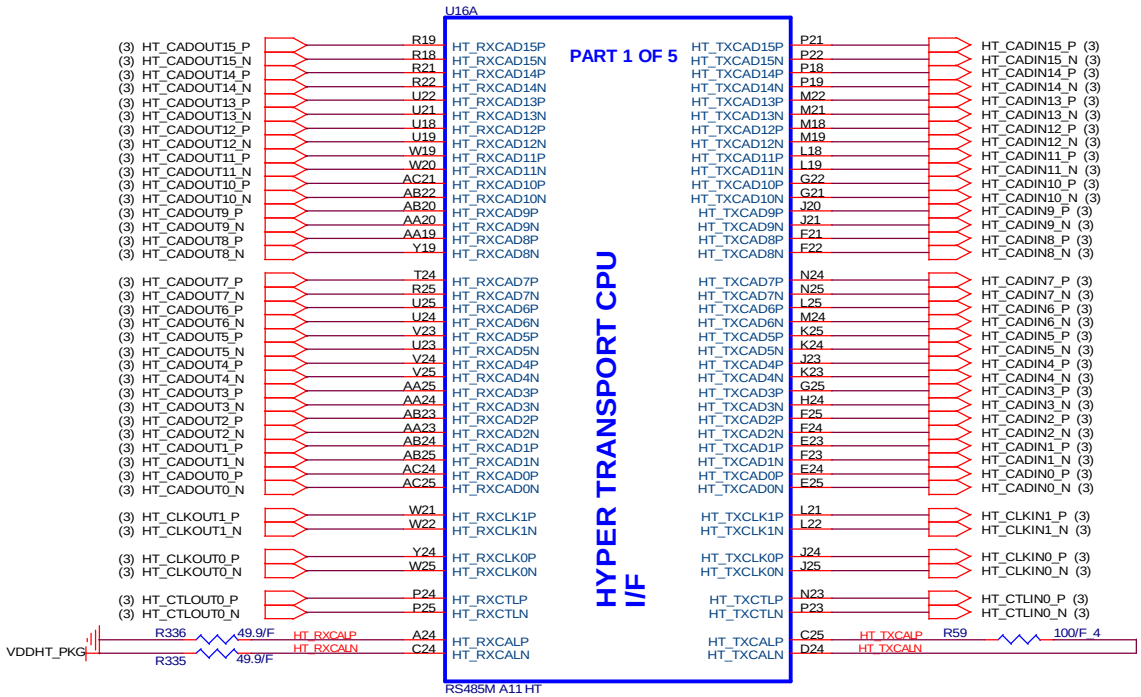

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-HT LINK0 I/F	1A
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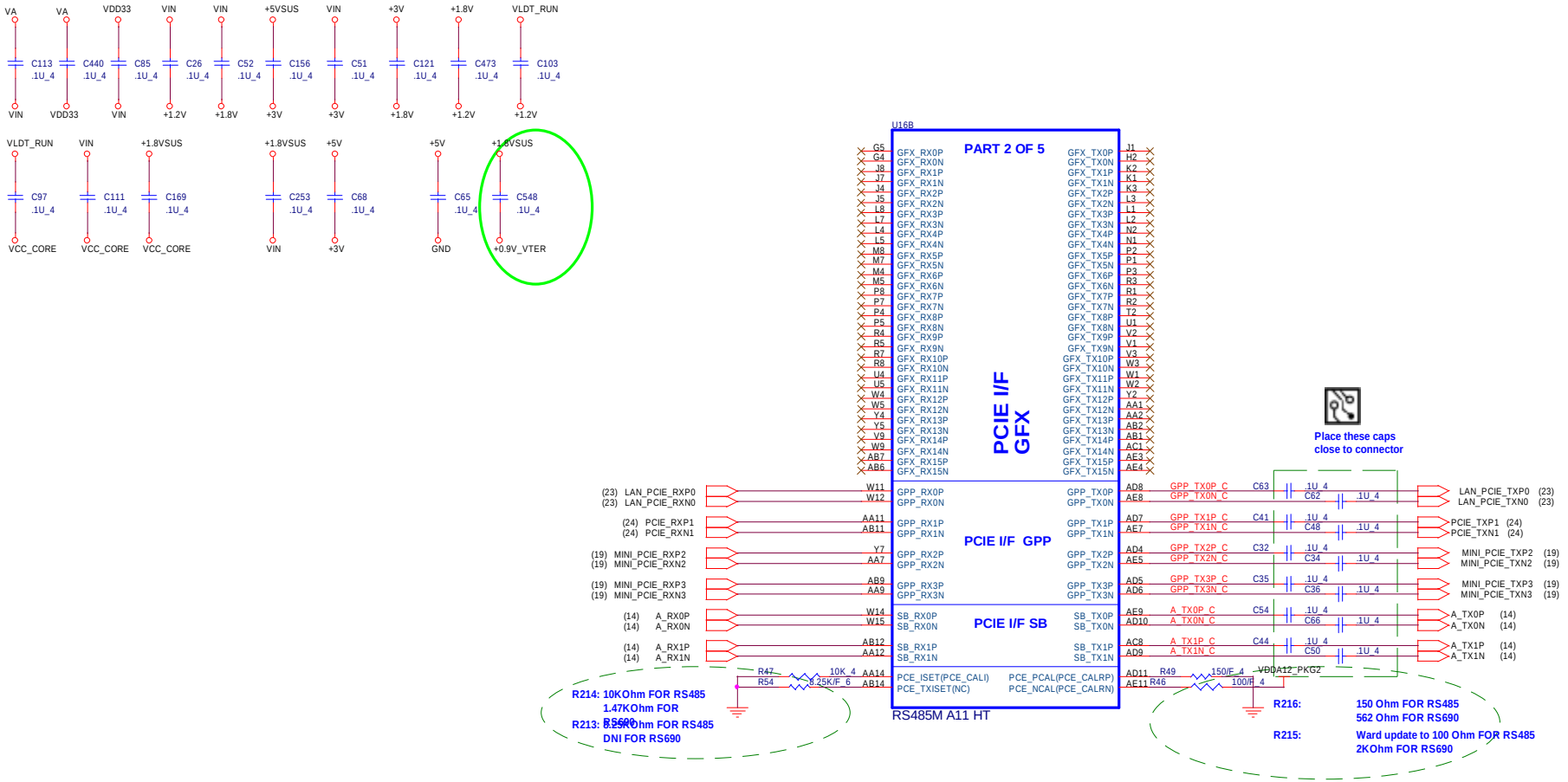

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-PCIE LINK I/F	1A
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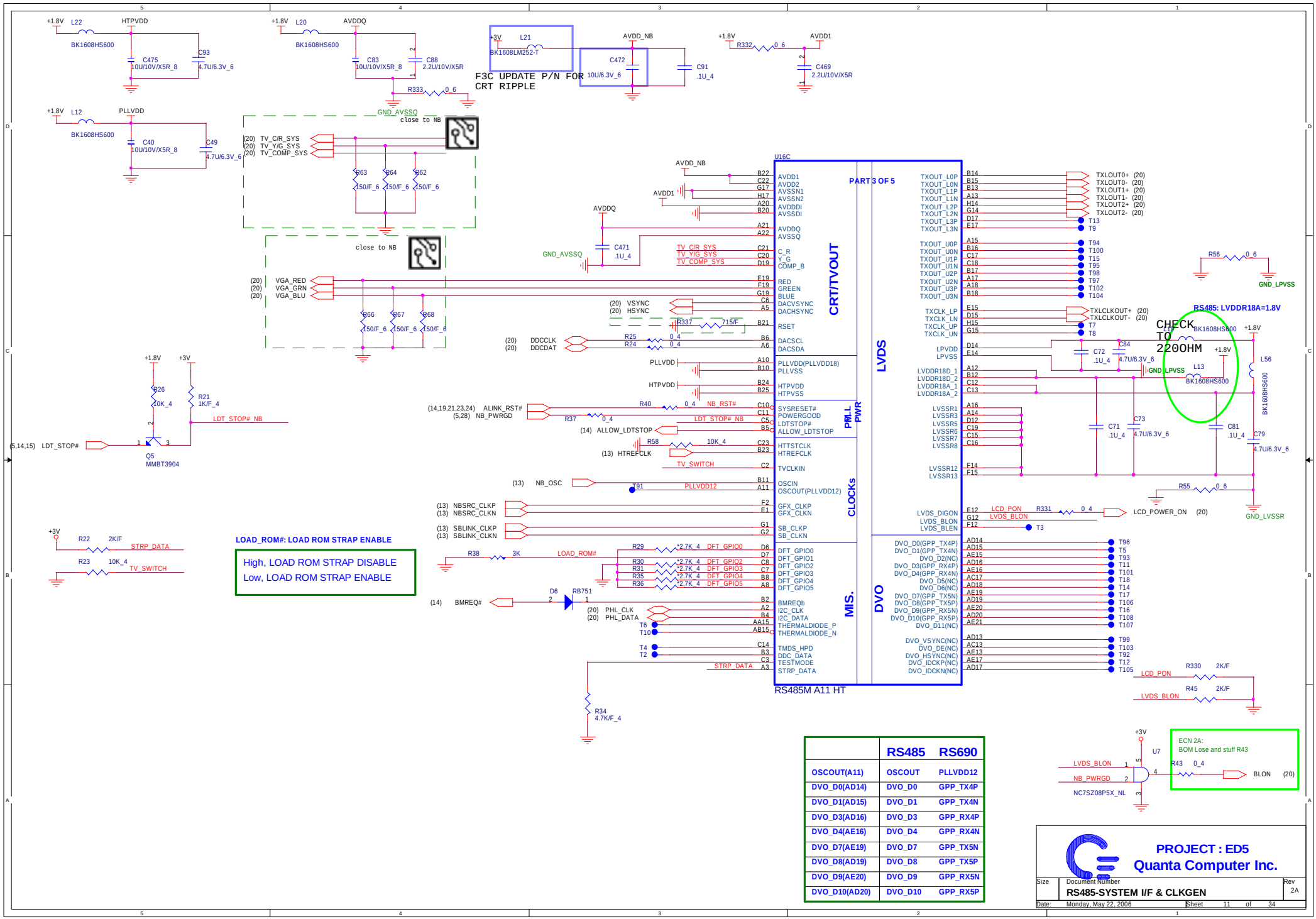
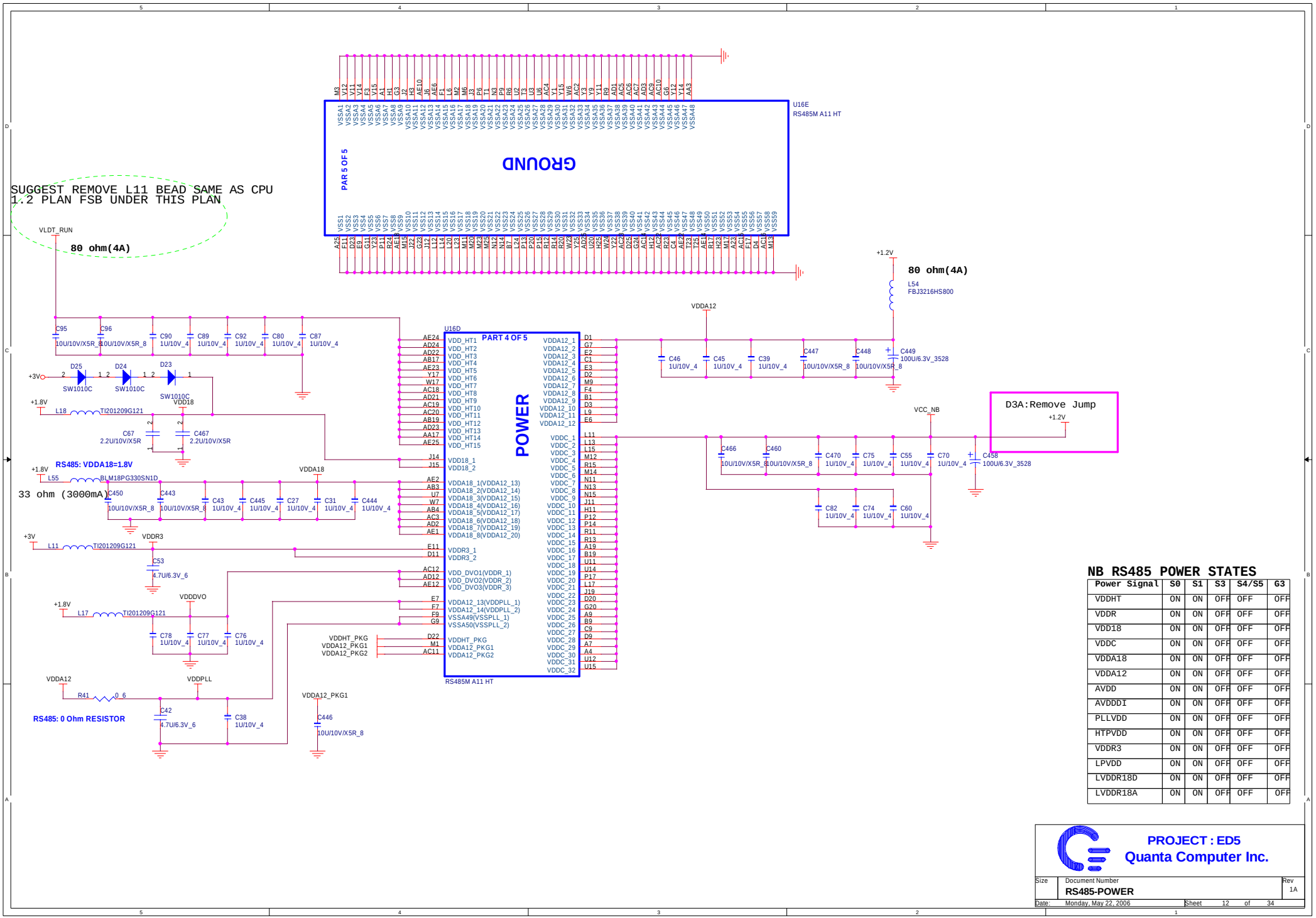


	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

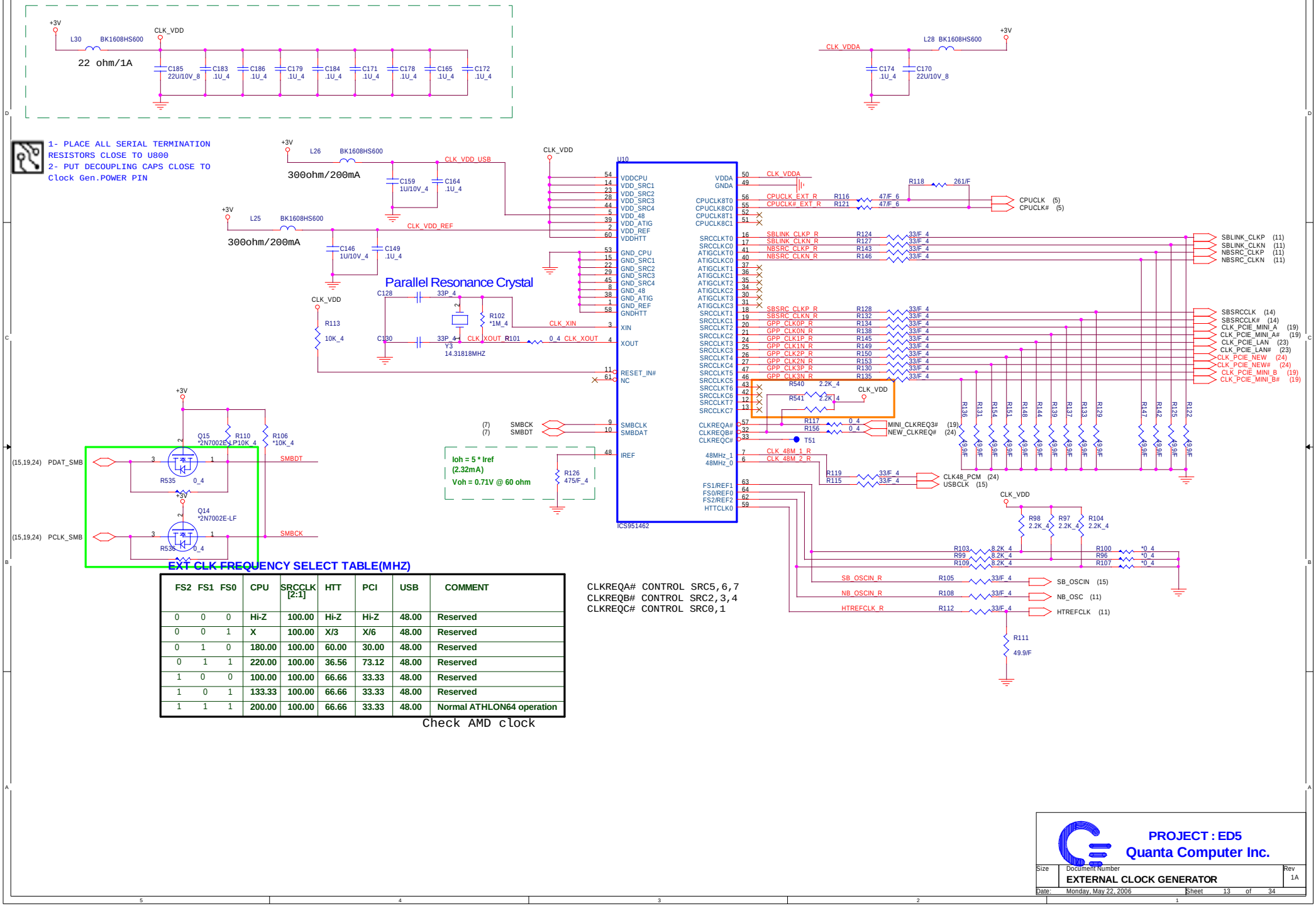


NB RS485 POWER STATES

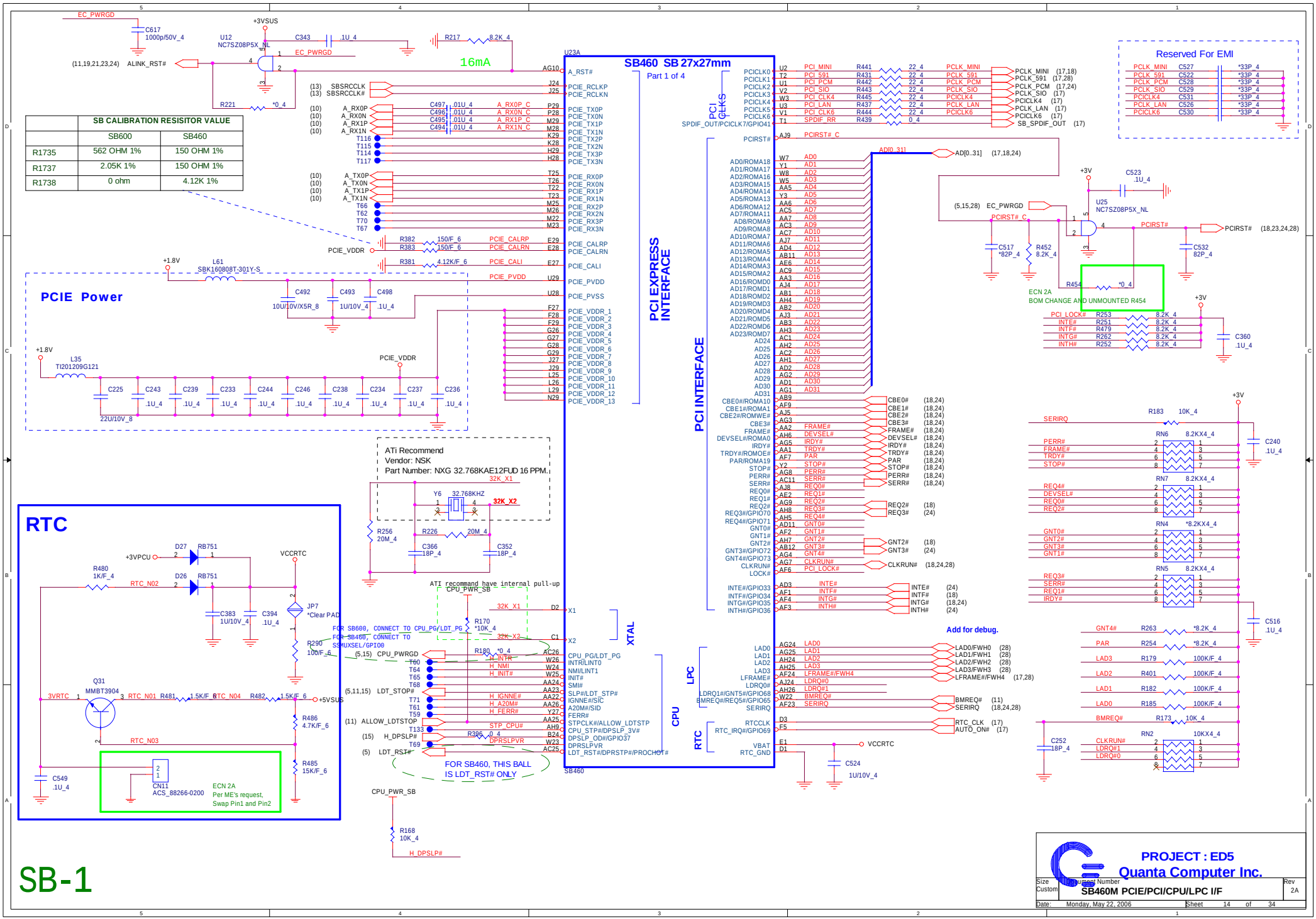
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

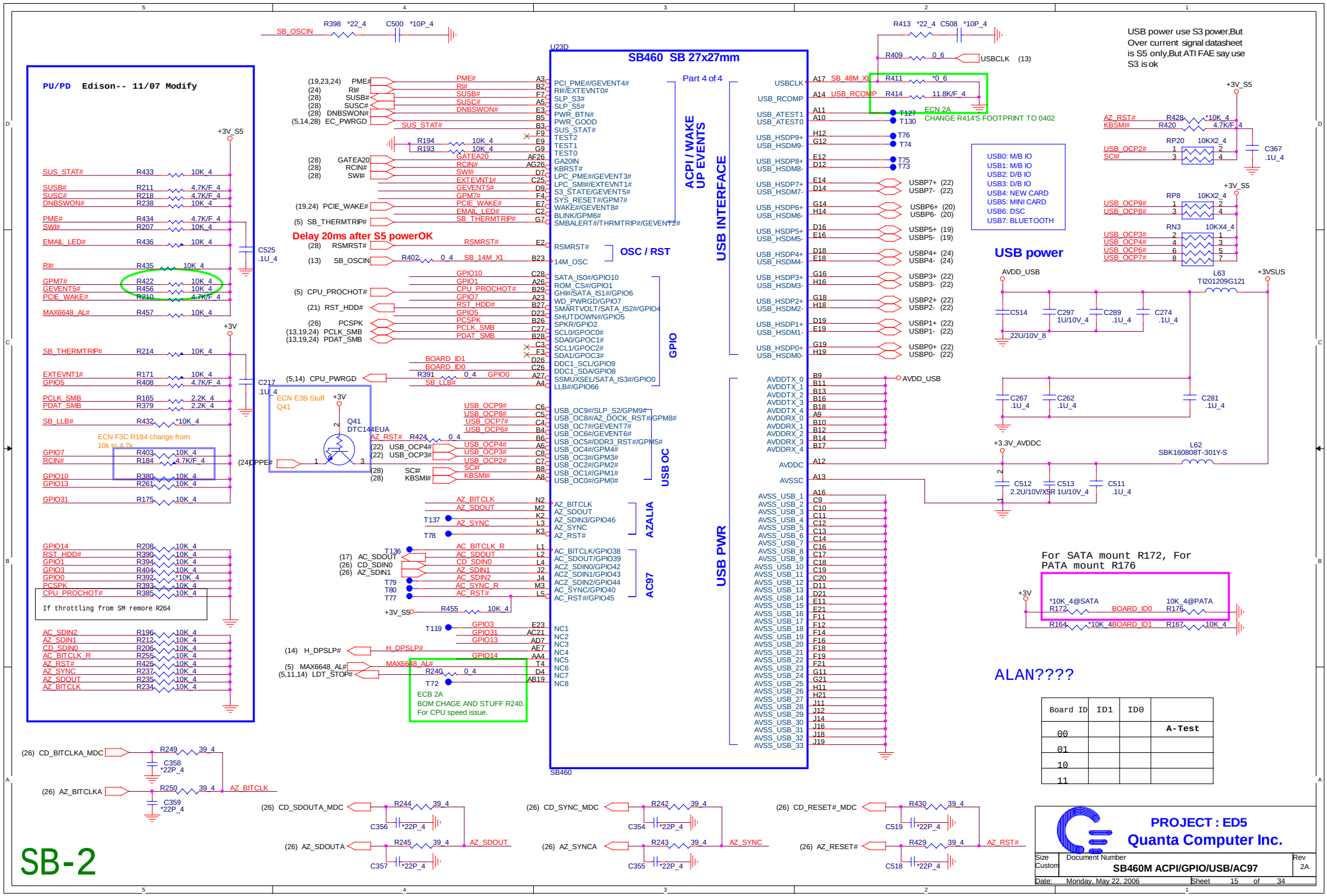
PROJECT : ED5
Quanta Computer Inc.

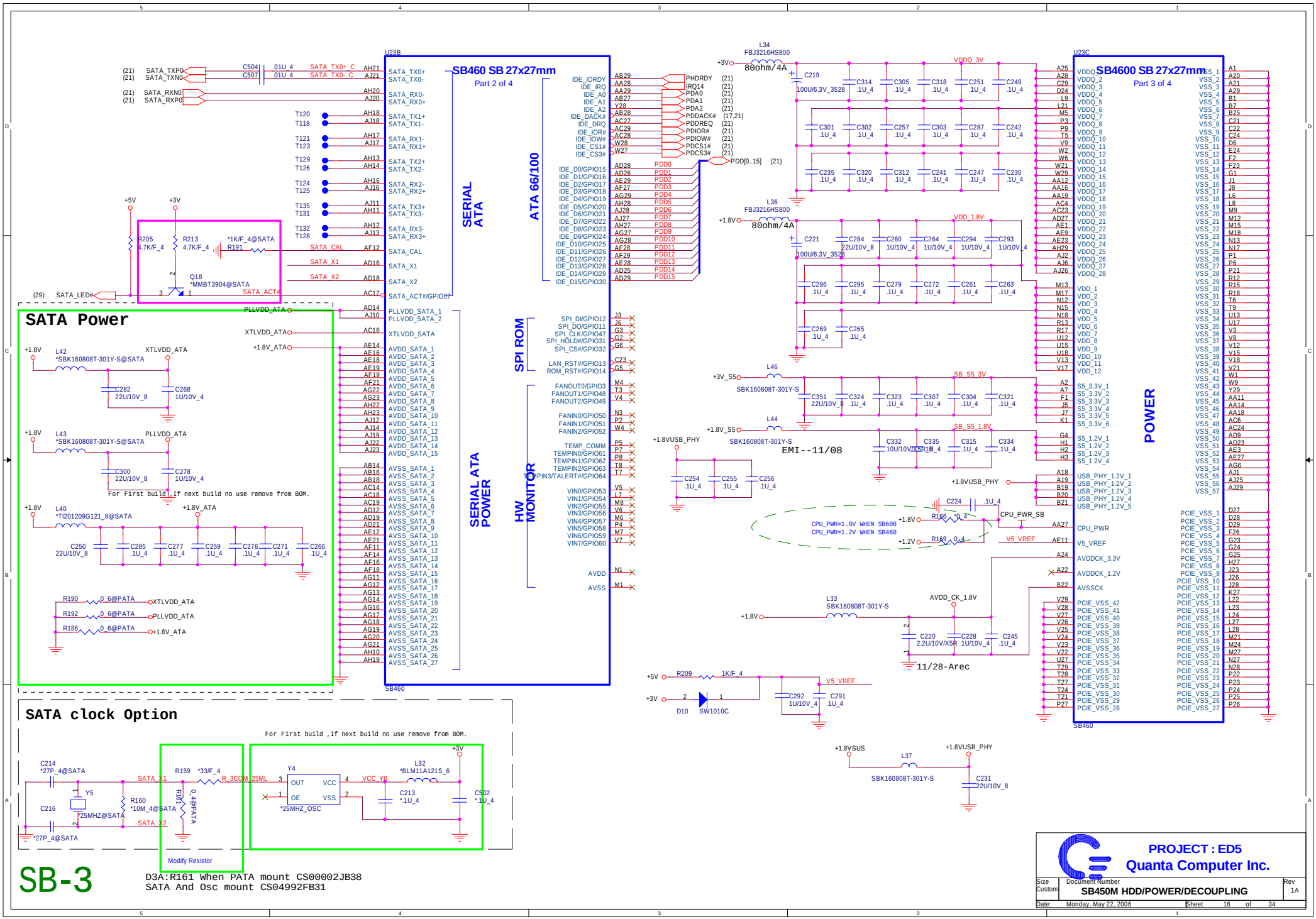
Size	Document Number	Rev
	RS485-POWER	1A
Date: Monday, May 22, 2006	Sheet 12 of 34	



FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



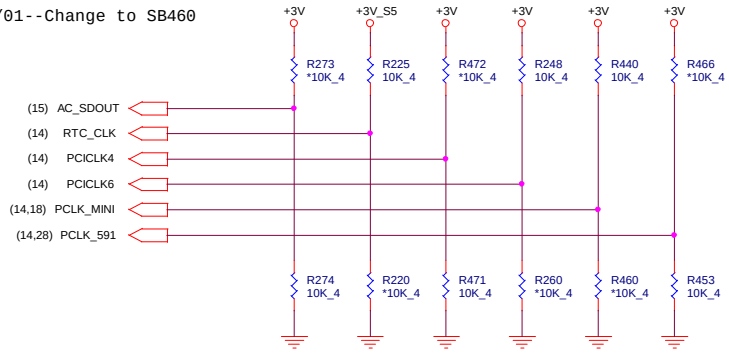




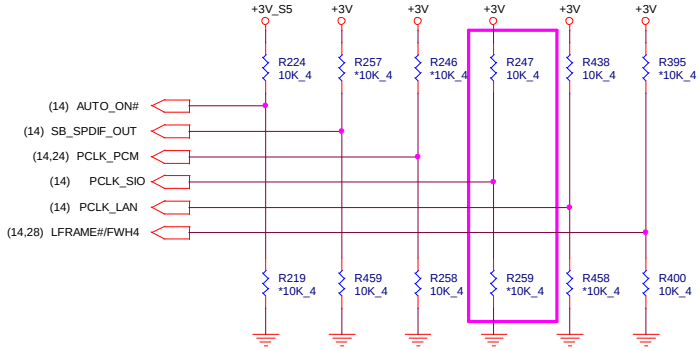
SB-3

D3A:R161 When PATA mount CS00002JB38
SATA And Osc mount CS04992FB31

Edison-11/01--Change to SB460



D3A:BOM change. R247: Stuff, R259: Un-stuff. Disable USB PHY POWERDOWN.

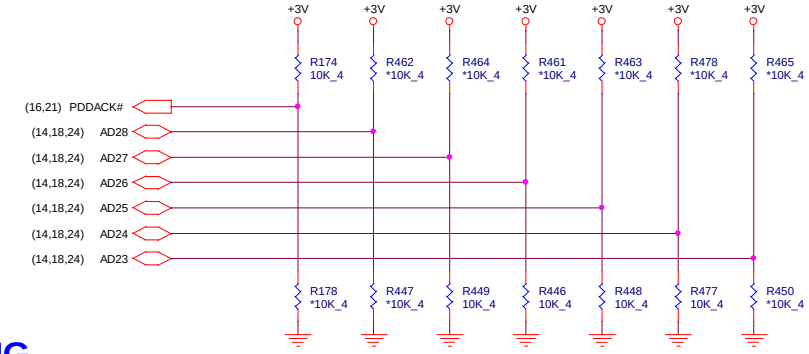


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCI_CLK0 / PCLK_591 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM; H, L = LPC TYPE I ROM; L, H = LPC TYPE II ROM DEFAULT; L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON# ACPWRON	SB_SPDIF_OUT SPDIF_OUT	PCLK_PCM PCI_CLK2	PCLK_SIO PCI_CLK3	PCLK_LAN PCI_CLK5	LFRAME# LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB-4

PROJECT : ED5
Quanta Computer Inc.

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Custom	SB460M STRAPS	1A
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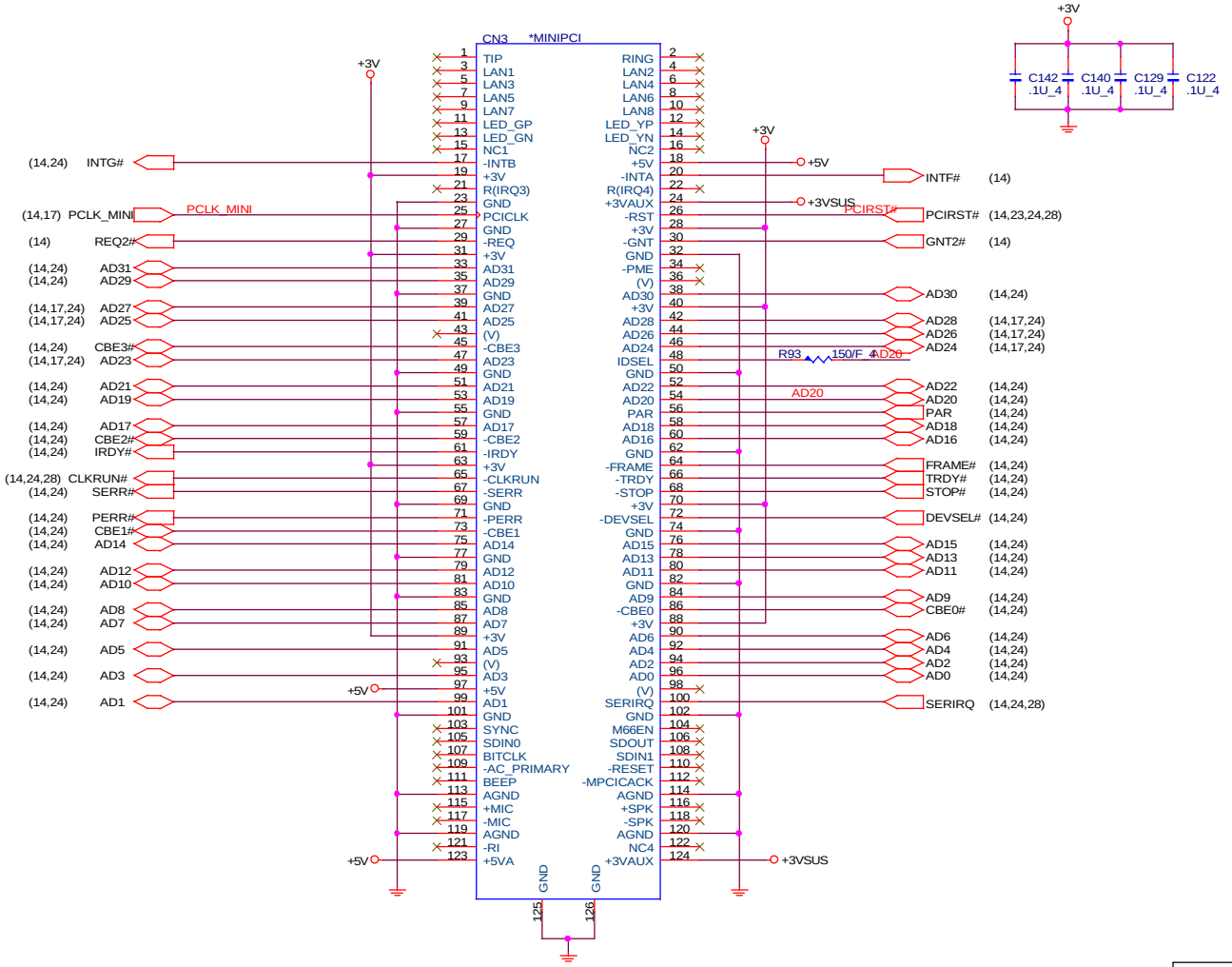
ID Select : AD20
Interrupt Pin : INTG# , INTF#
Request Indicate : REQ2#
Grant Indicate : GNT2#

DEBUG PURPOSE ONLY



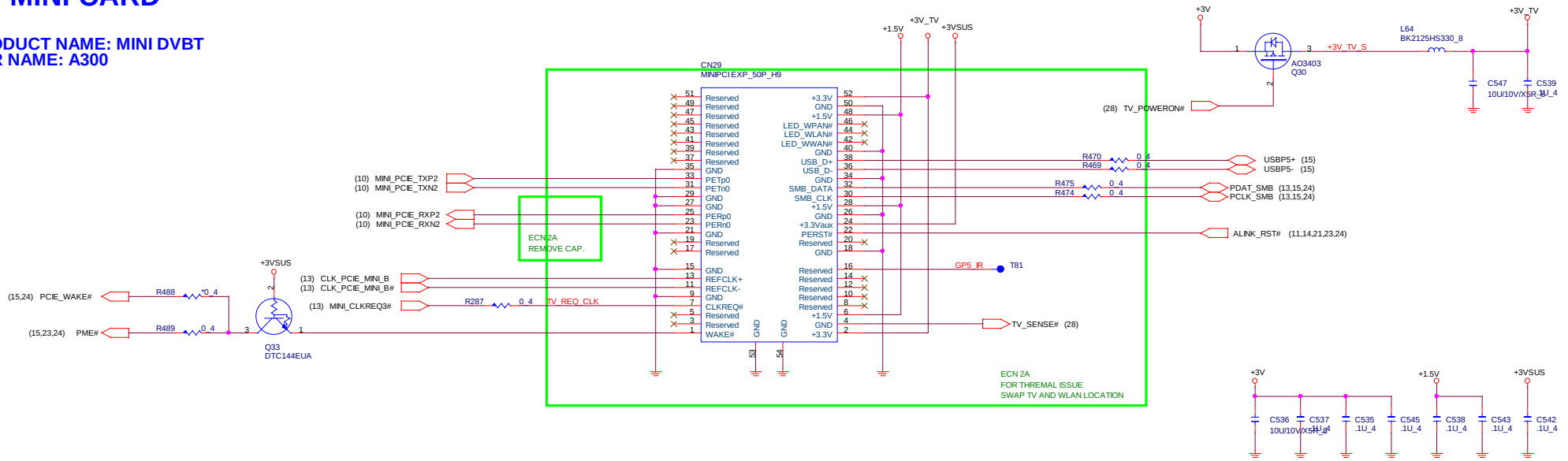
MPC

PROJECT : ED5
Quanta Computer Inc.

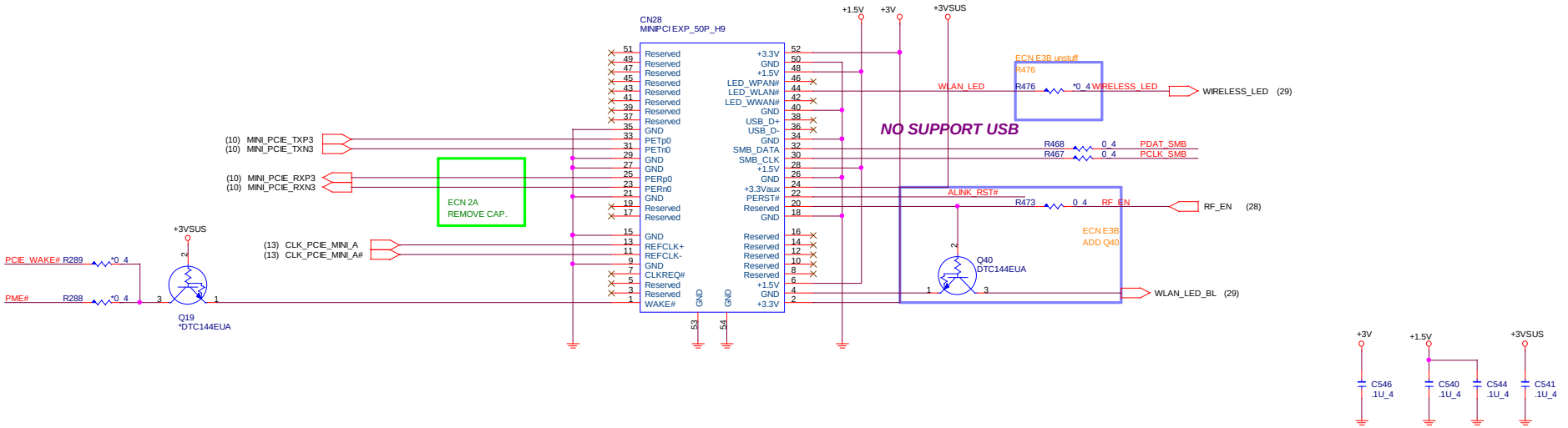
Size	Document Number	Rev
	MINI PCI CONNECTOR (DEBUG ONLY)	1A
Date: Monday, May 22, 2006	Sheet 18 of 34	

TV MINI CARD

PRODUCT NAME: MINI DVBT
MFR NAME: A300



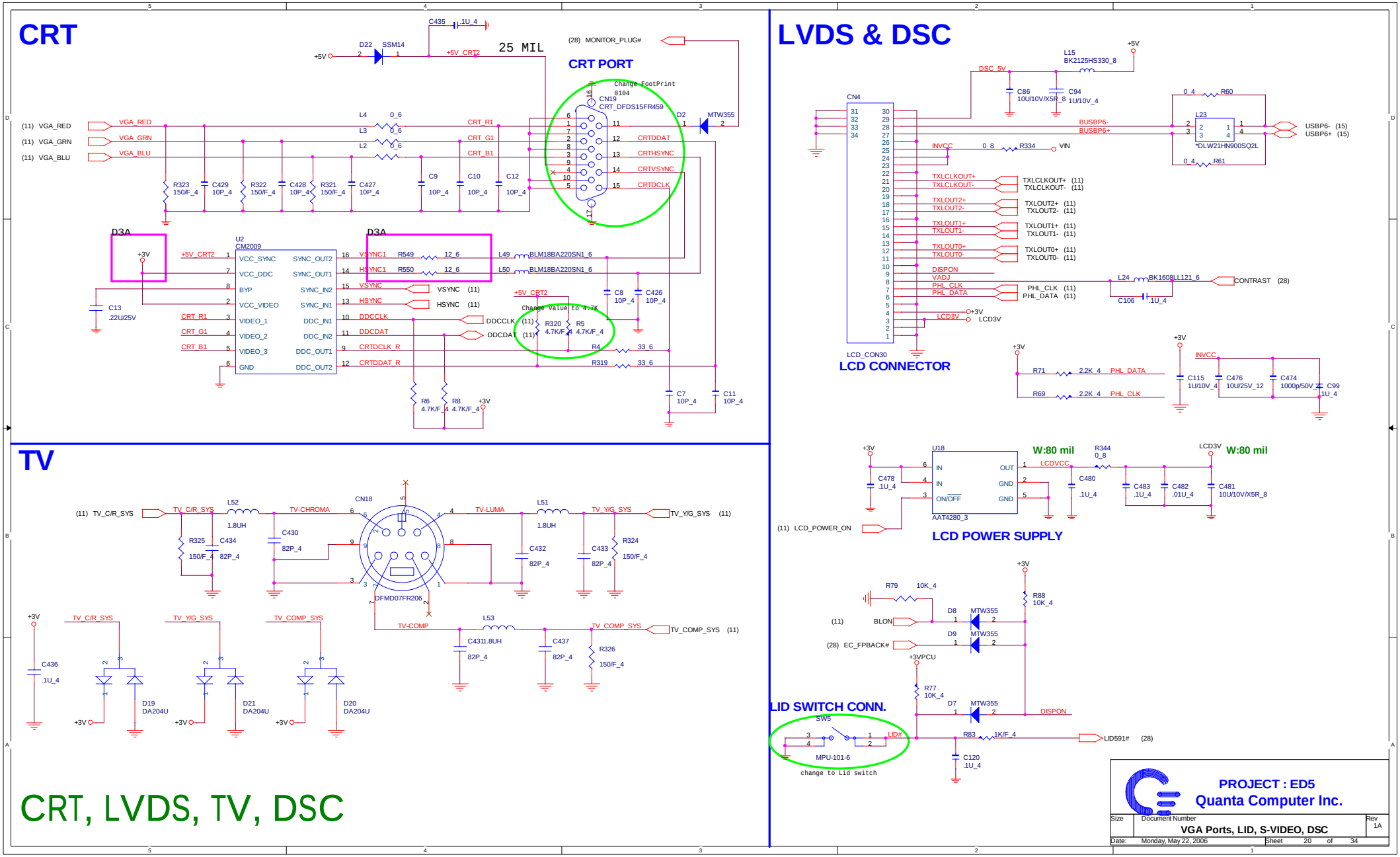
WLAN MINI CARD

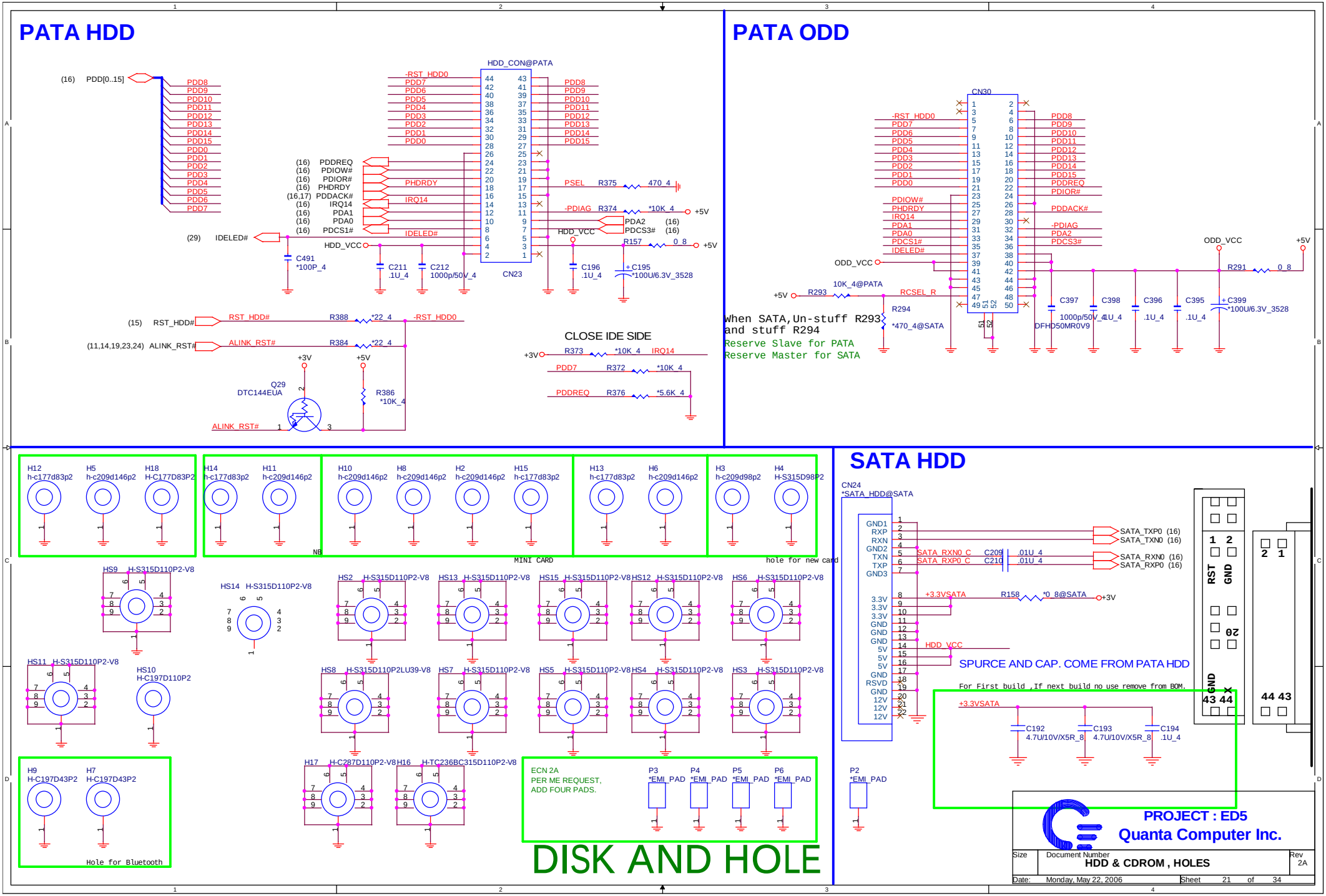


MINI CARD

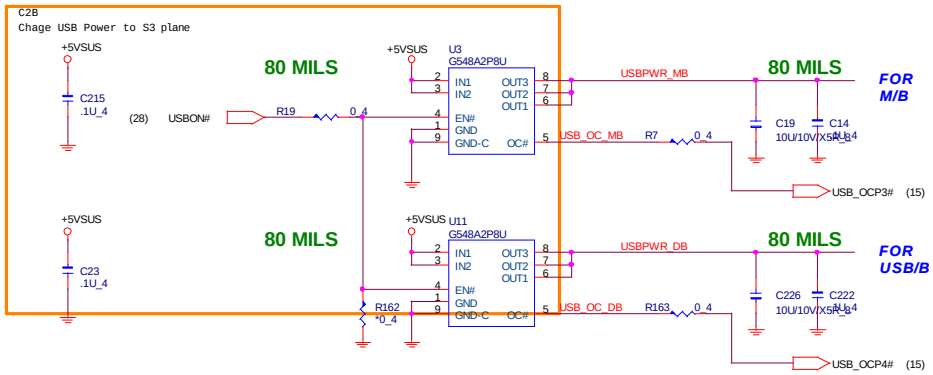
PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI CARD (WLAN AND TV)	2A
Date: Monday, May 22, 2006	Sheet 19 of 34	

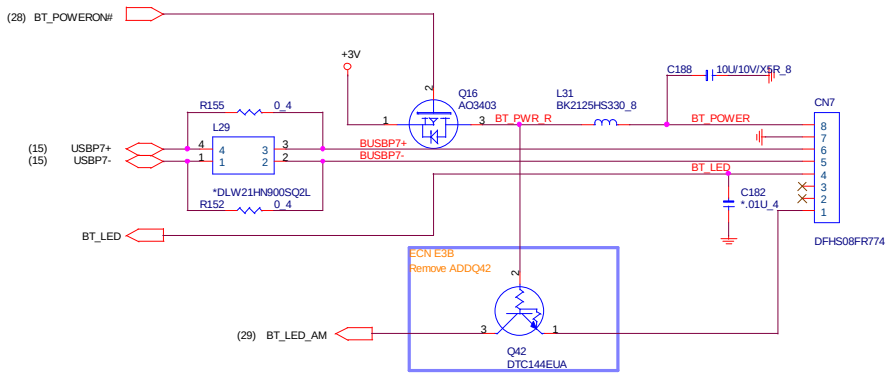




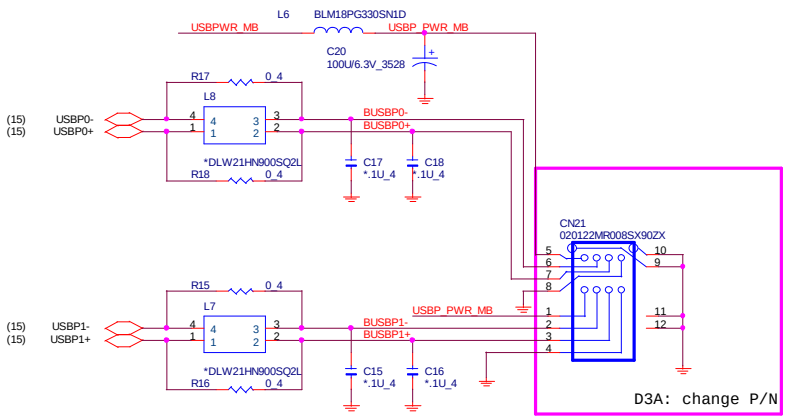
USB POWER SUPPLY



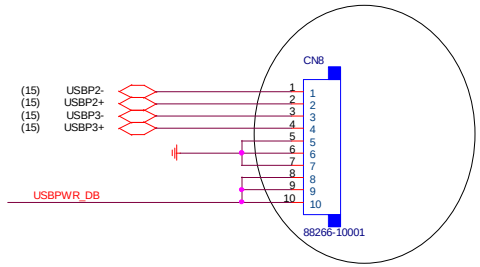
BLUETOOTH



USB I/O CONNECTORS



USB BAORD WIRE CONNECTOR



USB, BT, USB/B COONECTOR

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Quanta Computer Inc.

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	MINI PCI & USB PORT & BT	1A
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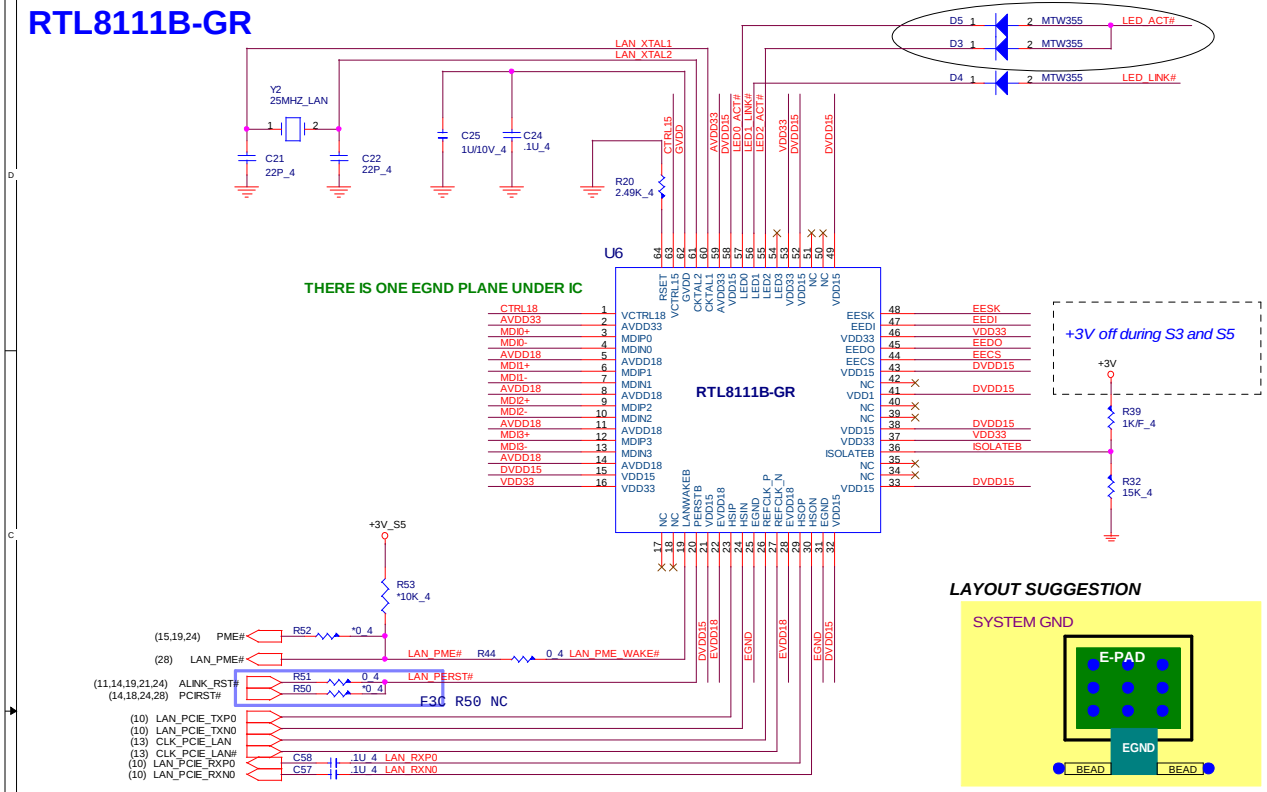
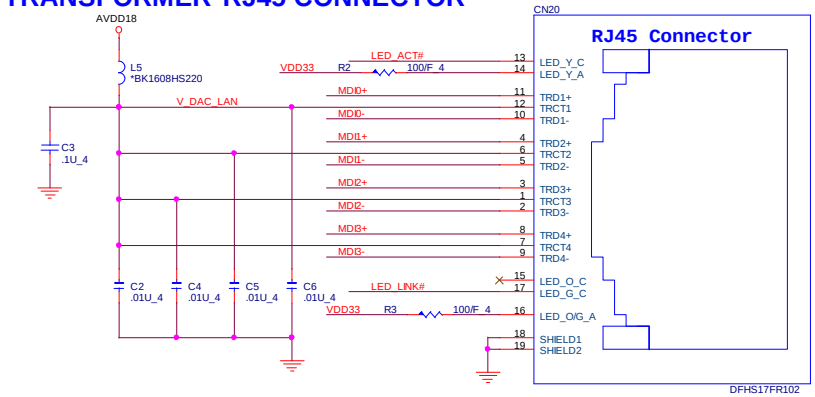
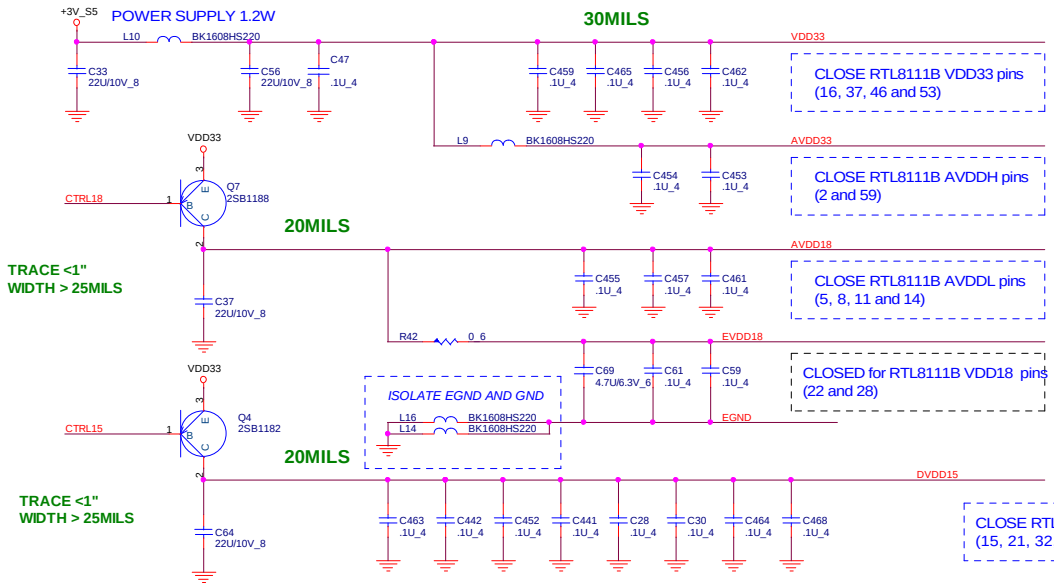
RTL8111B-GR



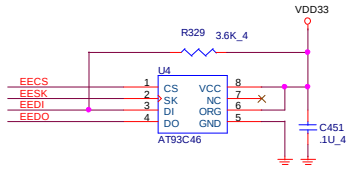
TRANSFORMER RJ45 CONNECTOR



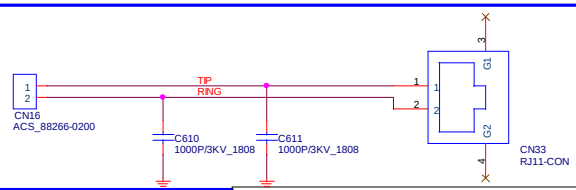
POWER SUPPLY



EEPROM



RJ11



LAN

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8111B-GR PCI-E & RJ11	1A
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PCI8402 PCI I/F

ID Select : AD17
Interrupt Pin : INTE# , INTG#, INTH#
Request Indicate : REQ3#
Grant Indicate : GNT3#

AD17 R405 150/F_4 PCM_IDSEL

ECN 2A
BOM CHANGE
REMOVE Y7 AND C509
STUFF R407

R407 0_4 CLK48_PCM (13)

Y7 OUT VDD GND OE *48MHz
CLK48M C509 *.1U_4 +3V

(14,17,18) AD[0..31] AD[0..31]

U24A PCIXX12_0
AD0 R11 AD1 P11 AD2 U11 AD3 V11 AD4 W11 AD5 R10 AD6 U10 AD7 V10 AD8 R9 AD9 U9 AD10 V9 AD11 W9 AD12 V8 AD13 U8 AD14 R8 AD15 W7 AD16 W4 AD17 T2 AD18 T1 AD19 R3 AD20 P5 AD21 R2 AD22 R1 AD23 P3 AD24 N3 AD25 N2 AD26 N1 AD27 M5 AD28 M6 AD29 M3 AD30 M2 AD31 M1
CLK48 F1
GRST K5 GRST# 8412
SUSPEND J5 8402_SUS# R415 10K_4 +3V
MFUNC0 G1 INTE# R416 0_4 INTE# (14)
MFUNC1 H5 INTG# INTG# (14,18)
MFUNC2 H2 INTH# INTH# (14)
MFUNC3 H1 SERIRQ SERIRQ (14,18,28)
MFUNC4 J1 3VSP R406 4.7K/F_4 +3V
MFUNC5 J2 FM_LED FM_LED (25)
MFUNC6 J3 CLKRUN# CLKRUN# (14,18,28)
PCLK L1 PCLK_PCM PCLK_PCM (14,17)
PRST K3 PCIRST# PCIRST# (14,18,23,28)
SPKROUT H3 PCMSPK PCMSPK (26)
RI_OUT/PME L5 PCM_PME# R189 *0_4 RI# (15)
SDA G3 SDA_CARD
SCL G2 SCL_CARD
LATCH C9
DATA B9
CLOCK A9
USB_EN E10 USB_EN# R427 *10K_4 +3V
PHY_TEST_MA P17 TEST_MA R216 4.7K/F_4 1394_AVDD
TEST0 P12
PSMODE C4 R417 10K_4 +3V
NC F5
(14,18) CBE0# W10 CBE1# V7 CBE2# U5 CBE3# P2
(14,18) PAR U7 DEVSEL# U6 FRAME# R6 GNT3# L2 PCM_IDSEL N5 IRDY# V5 PERR# R7 REQ3# L3 SERR# W6 STOP# V6 TRDY# W5
PAR DEVSEL FRAME GNT IDSEL IRDY PERR REQ SERR STOP TRDY
RSVD // VD0 // VCCD1#

Q17 DTC144EUA
R188 0_4 PME# (15,19,23)

PCLK_PCM R397 *22_4 PCLK_PCM_R C499 *10p_4
CLK48_PCM R399 *22_4 CLK48_PCM_R C501 *10p_4

U24B PCMCIA PORT
VCCB A15 VCCB J19
CAD31 // D10 C10 CAD30 // D9 A10 CAD29 // D1 E11 CAD28 // D8 E11 CAD27 // D0 C11 CAD26 // A0 B13 CAD25 // A1 C13 CAD24 // A2 A14 CAD23 // A3 B14 CAD22 // A4 B15 CAD21 // A5 E14 CAD20 // A6 A16 CAD19 // A25 D19 CAD18 // A7 E17 CAD17 // A24 E15 CAD16 // A17 H19 CAD15 // IOWR# H17 CAD14 // A9 J15 CAD13 // IORD# J18 CAD12 // A11 K15 CAD11 // OE# K17 CAD10 // CE2# K18 CAD9 // A10 L15 CAD8 // D15 L18 CAD7 // D7 L19 CAD6 // D13 M17 CAD5 // D6 M18 CAD4 // D12 N19 CAD3 // D5 M15 CAD2 // D11 N17 CAD1 // D4 N18 CAD0 // D3 P19
CC/BE3# // REG# E13 CC/BE2# // A12 E18 CC/BE1# // A8 H18 CC/BE0# // CE1# L17
CPAR // A13 H14 CDEVSEL# // A21 E19 CFRAME# // A23 E19 CGNT# // WE# G17 CINT# // READY(IREQ#) E12 CIRDY# // A15 E17 CPERR# // A14 G19 CREQ# // INPACK# C14 CSERR# // WAIT# C12 CSTOP# // A20 G18 CTRDY# // A22 G15
CCLK // A16 E18 CCLKRUN# // WP(IOIS16#) A11 CSTSCHG // BVD1(STSCHG#/RI#) A12 CBLOCK# // A19 H15 CRST# // RESET C15 CAUDIO // BVD2(SPKR#) B12
CCD1# // CD1# N15 CCD2# // CD2# B11 CVS1 // VS1# A13 CVS2 // VS2# B16
RSVD // A18 H17 RSVD // D2 B10 RSVD // D14 M19
PCIXX12_0

NEW CARD

NEW CARD HEADER: DFHD26MR074 (13081-1)
NEW CARD EJECTER: FBZF1026019 (130851-3)

CN6 FOXCONN_NEW_CARD
(10) PCIE_TXP1 (10) PCIE_TXN1
C126 .1U_4 PERP1
C125 .1U_4 PERN1
(10) PCIE_RXP1 (10) PCIE_RXN1
(13) CLK_PCIE_NEW (13) CLK_PCIE_NEW#
(15) CPPE# (13) NEW_CLKREQ#
CPPE#
+NEW_3V
NEW_PERST# RC
+NEW_3VAUX
NEWCARD_PCIE_WAKE#
+NEW_1.5V
(13,15,19) PDAT_SMB (13,15,19) PCLK_SMB
CPUSB#
(15) USBP4+ (15) USBP4-
R95 0_4 BUSBP4+
R94 0_4 BUSBP4-
GND5 GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND6

+3V_S5
Q13 DTC144EUA
(15,19) PCIE_WAKE# NEWCARD_PCIE_WAKE#

NEW CARD'S POWER SWITCH

U8 TPS2231PWG4
+3V +3V_S5 +1.5V
3.3VIN 3.3VIN 1.5VIN 1.5VIN AUXIN SYSRST# SHDN# RCLKEN NC GND
3.3VOUT 3.3VOUT 1.5VOUT 1.5VOUT AUXOUT STBY# CPPE# CPUSB# PERST# OC#
+NEW_3V +NEW_3VAUX +NEW_1.5V CPPE# CPUSB# NEW_PERST#
(11,14,19,21,23) ALINK_RST#
R553 28.7K/F NEW_PERST# NEW_PERST#_RC
C618 3900p/25V

F3C: Add RC delaly on new of NEW_PERST#

CPPE# : (Internal Pull Up , active low when card support PCIE)
CPUSB# : (Internal Pull Up , active low when card support USB)
SHDN# : (Internal Pull Up)

+3V +3V_S5 +1.5V +NEW_3VAUX +NEW_3V +NEW_1.5V
C155 .1U_4 C141 .1U_4 C158 .1U_4 C152 .1U_4 C168 10U/10V/X5R C160 .1U_4 C166 .1U_4 C167 10U/10V/X5R C162 .1U_4

IEEE1394 EEPROM

+3V
R389 2.2K_4 R387 2.2K_4
SDA_CARD SCL_CARD
U22 24LC08
SDA SCL WP GND VCC A0 A1 A2
C506 .1U_4 +3V

+3V
R181 22K/F_4 GRST# 8412
C232 .22U/6V_4

> 2 ms > 0 ns
VCC
GRST#
PRST# > 100 us
PCLK

IEEE1394 & NEW CARD

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	PCI8402-1 & NEW CARD	2A
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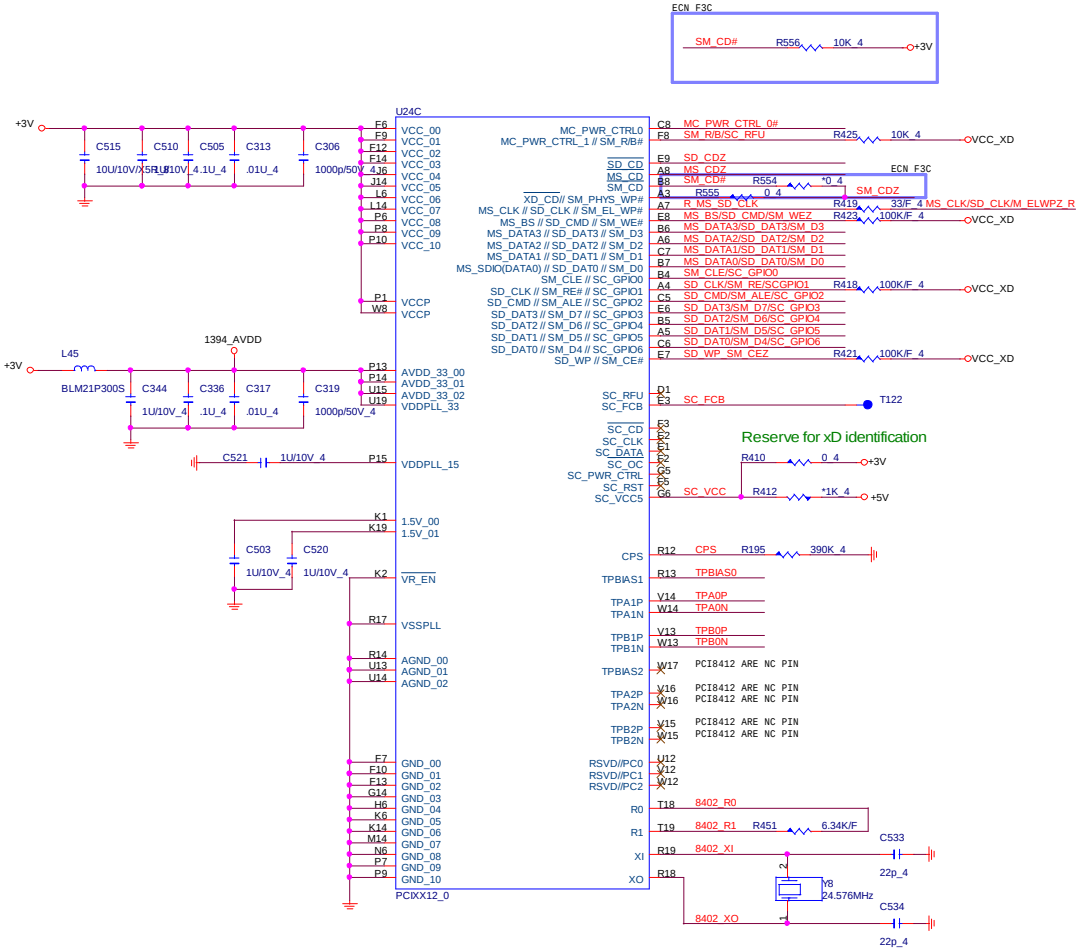
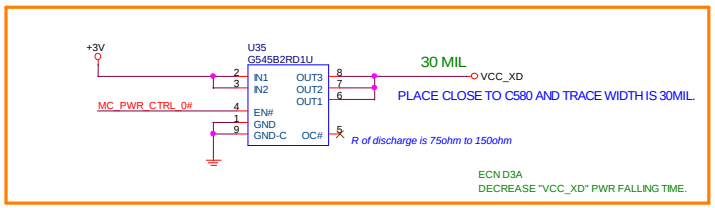
PCI8402 I/F OF 1394 & CARD READER



MEMORY CARD READED POWER CONTROL (IC SOLUTION FOR C-TEST)

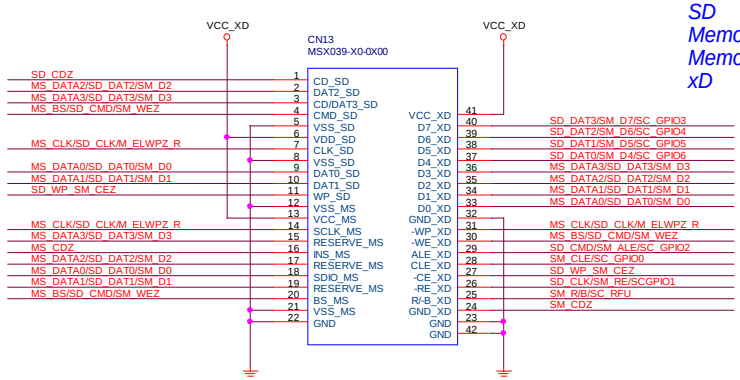


IEEE1394 & CARD REDER

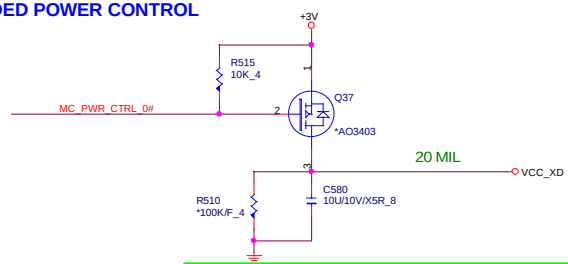
5 IN 1 MEMORY CARD READER

Support :

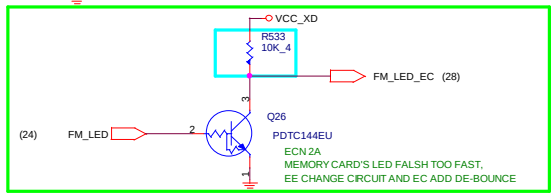
MMC
SD
Memory Stick
Memory Stick Pro
xD



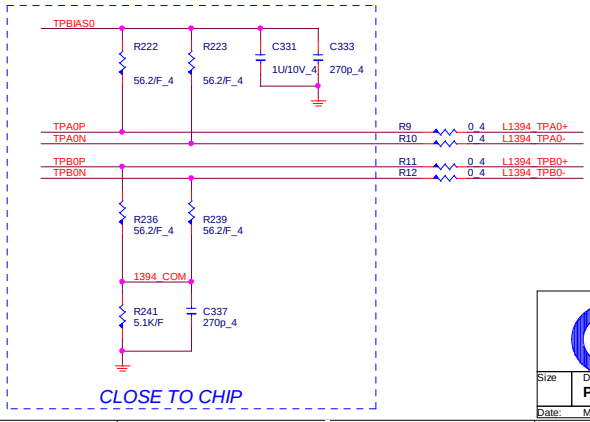
MEMORY CARD READED POWER CONTROL

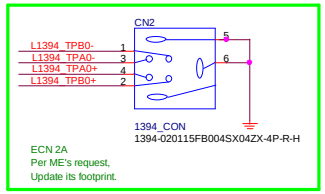


MEMORY CARD READED LED INDICATE



IEEE1394 CONNECTOR





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Quanta Computer Inc.

Size	Document Number	Rev
	PCI8402-2 (1394 & 5 IN 1)	2A
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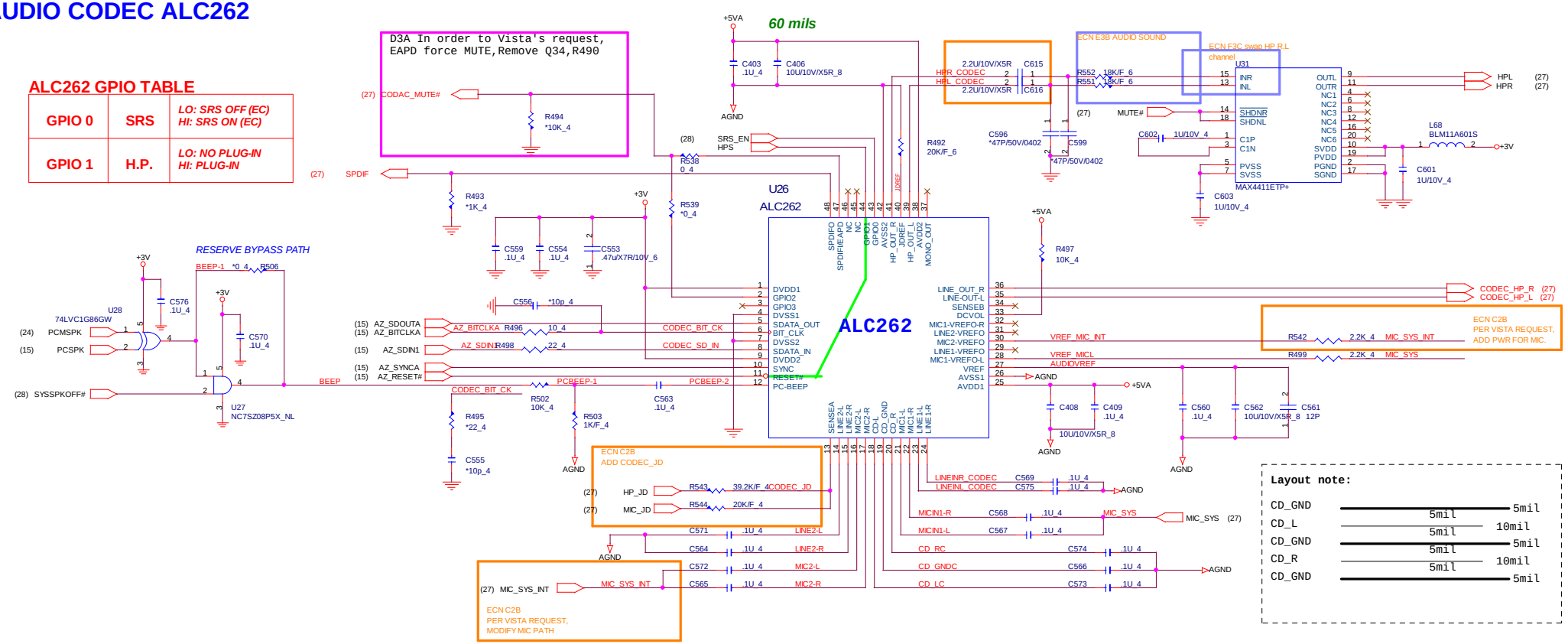
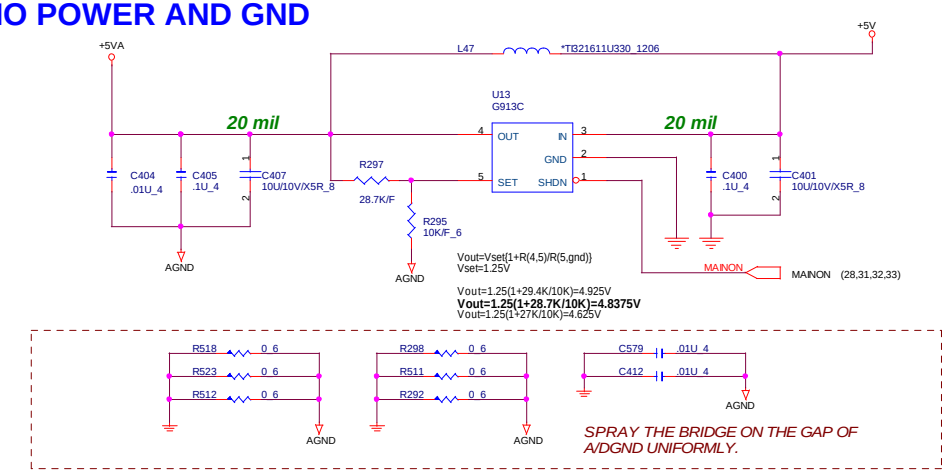
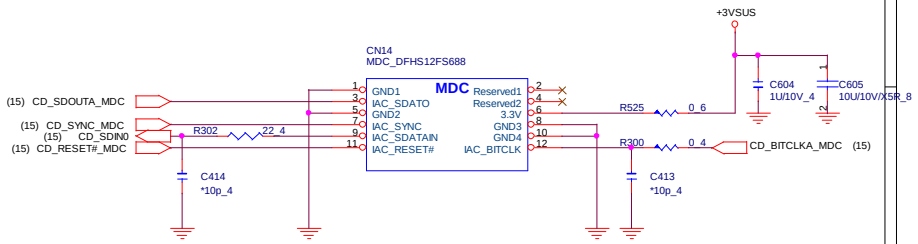
AUDIO CODEC ALC262



AUDIO POWER AND GND



AZALIA MDC INTERFACE



AUDIO CODEC & MDC

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	AUDIO CODEC ALC262 AND MDC	2A
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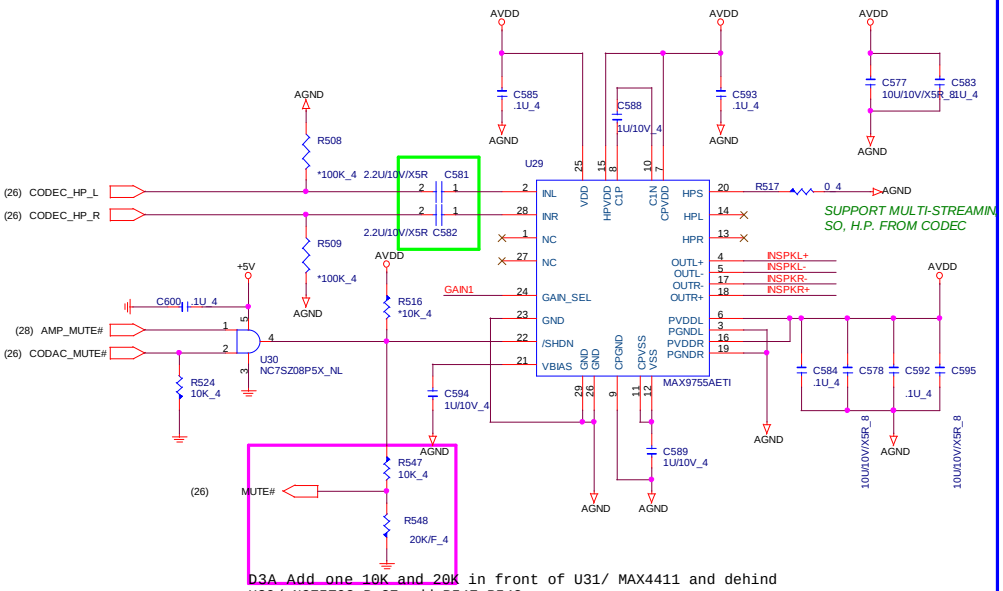
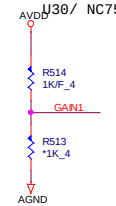
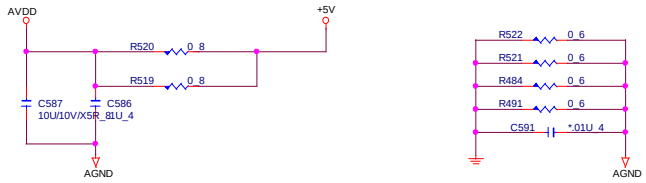
AUDIO AMP. (MAX9755)



D3A Add one 10K and 20K in front of U31/ MAX4411 and dehind U30/ NC75Z08 P.27 add R547,R548

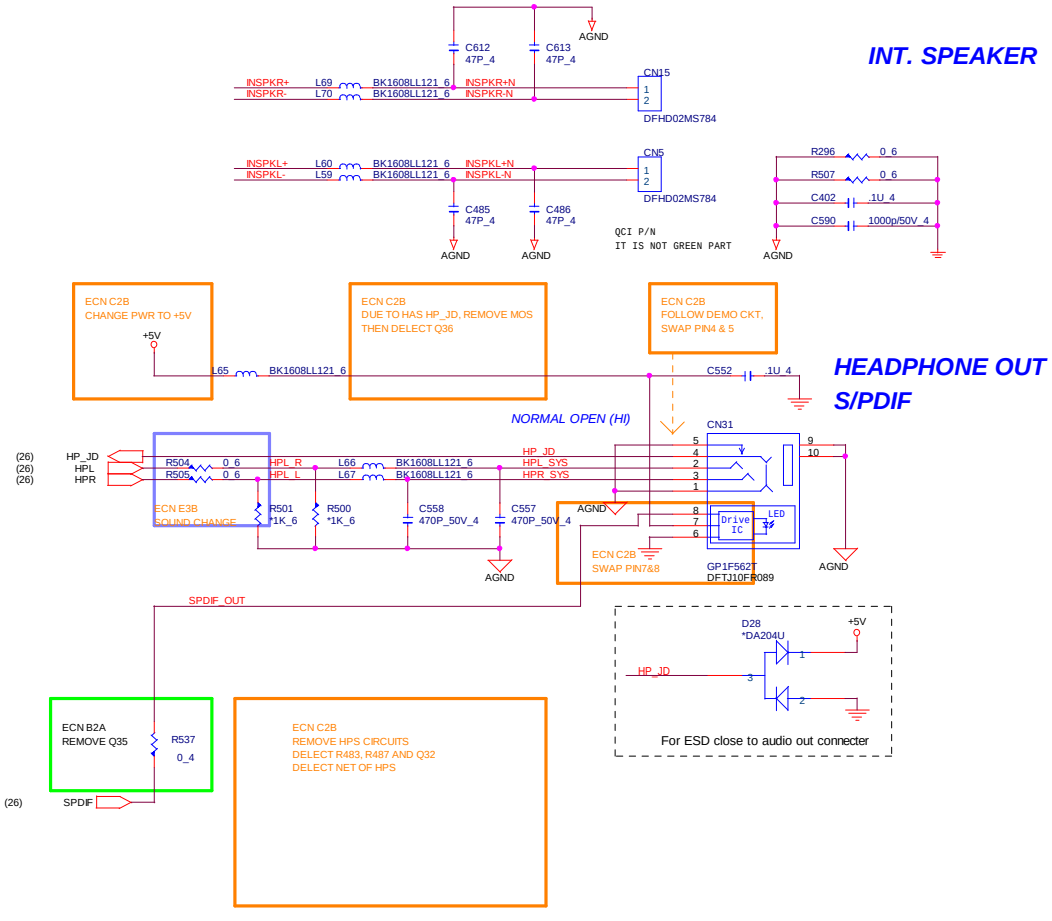


GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



AMP. POWER SUPPLY

AUDIO JACK



AUDIO AMP. & JACK

PROJECT : ED5
Quanta Computer Inc.

Size	Document Number	Rev
	AMP. & JACK	1A
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