DOTHAN/ALVISO-GM(PM)/ATI M24 BLOCK DIAGRAM

SUB-BOARD

- INSTANT KEY BOARD
- AUDIO DJ BOARD
- MIC BOARD

POWER

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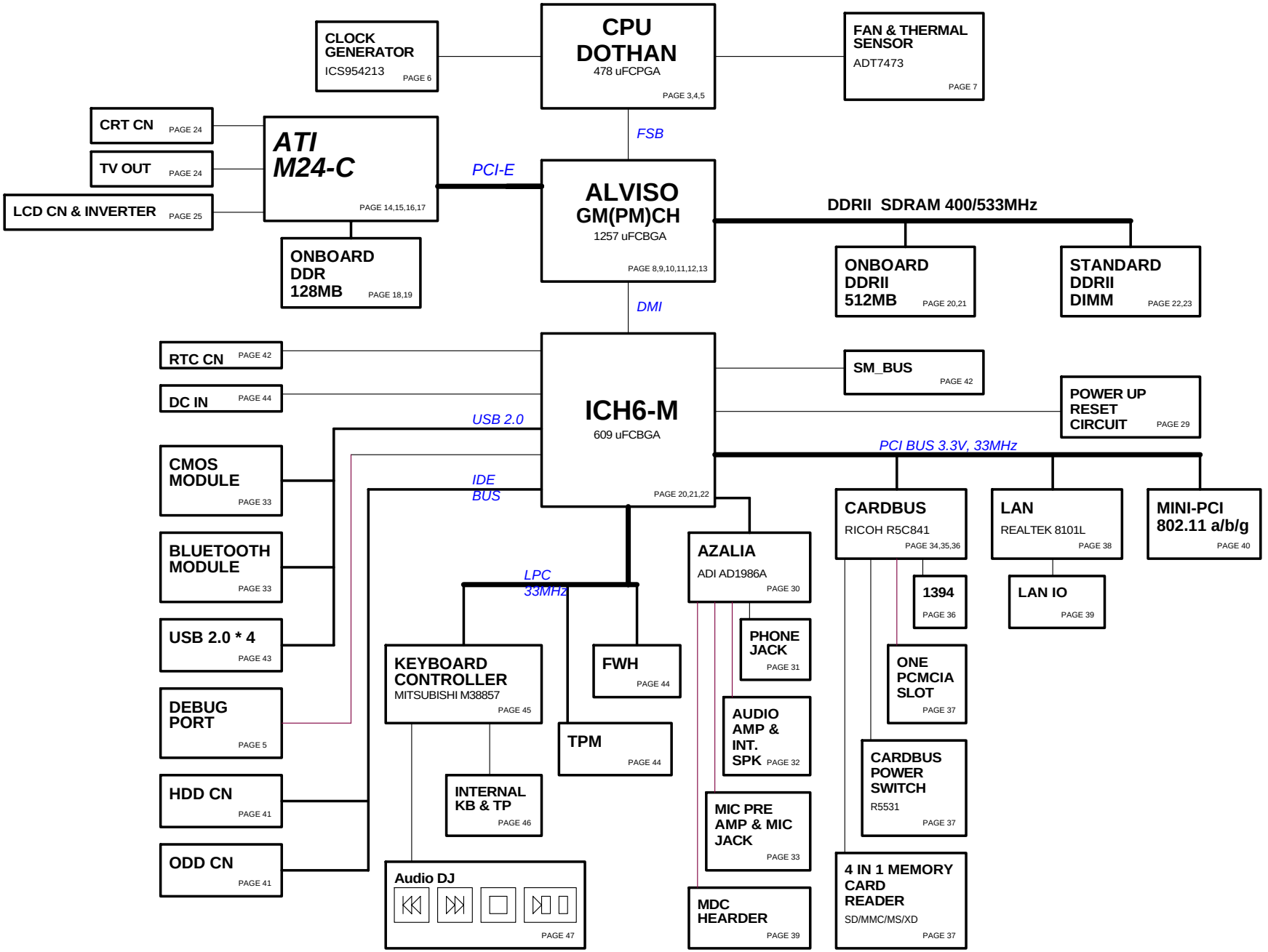
- SYSTEM 3VO/5VO PAGE 49
- 1.2V/1.5V/1.8V/1.05V PAGE 50
- 1.5VA/0.9VS PAGE 51
- BATLOW/SD# PAGE 52
- CHARGE PAGE 53
- BAT CON PAGE 54
- PIC16C54 PAGE 55
- LOAD Switch PAGE 56
- VGA VCORE PAGE 57



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME : <Doc>
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DESIGN ENGINEER :

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40	MiniPCI		
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42	SM_BUS & RTC CN		
43	4*USB2.0 Conn		
44	DCIN JACK & FWH & TPM		
45	Keyboard Controller (M3885)		
46	LEDs & Internal KB & TP		
47	Audio DJ		
48	VCORE		
49	SYSTEM		
50	2.5V & 1.5V & 1.8V & 1.05V		
51	1.5VA & DDR2 & 3VALWAYS_P		
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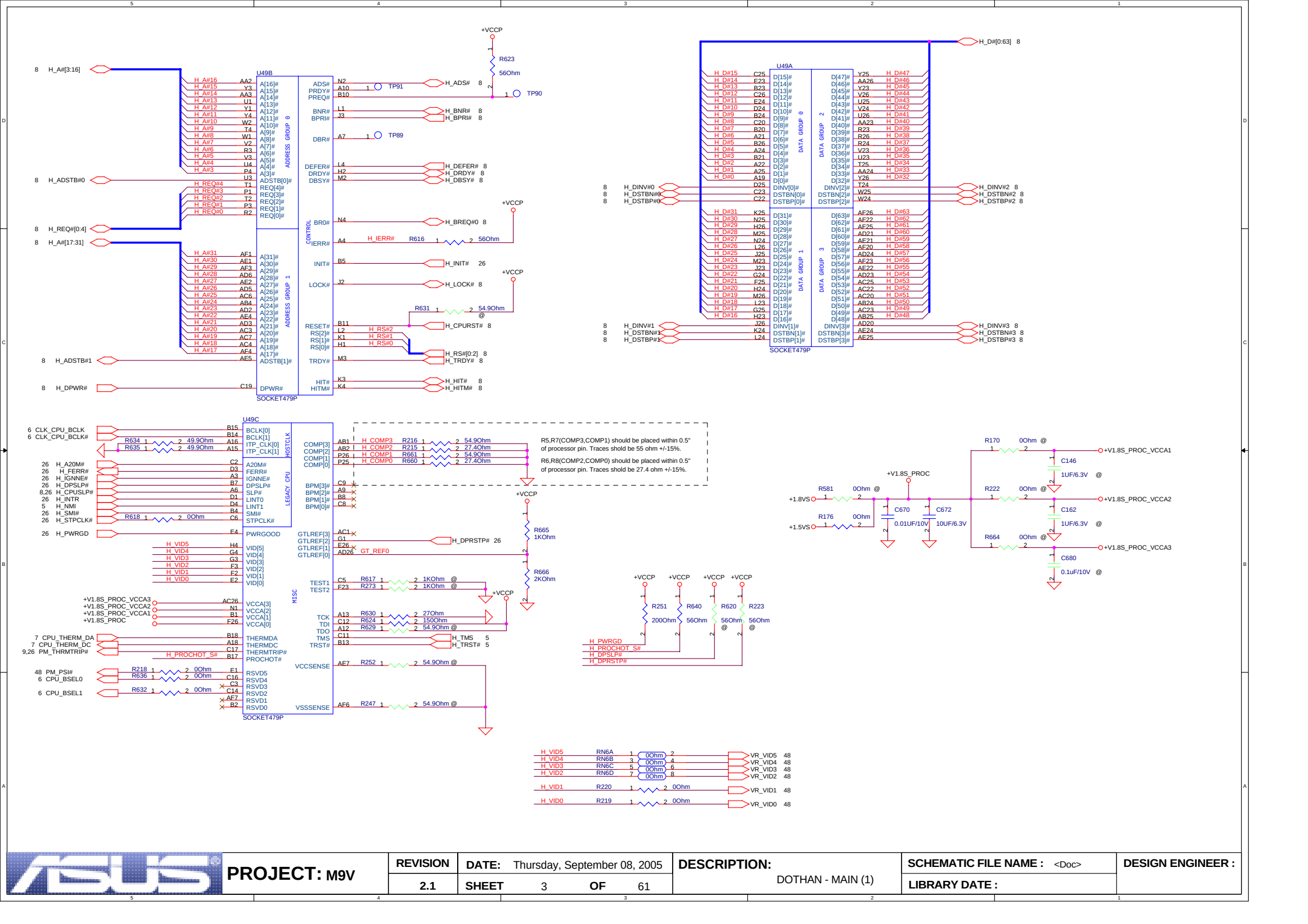
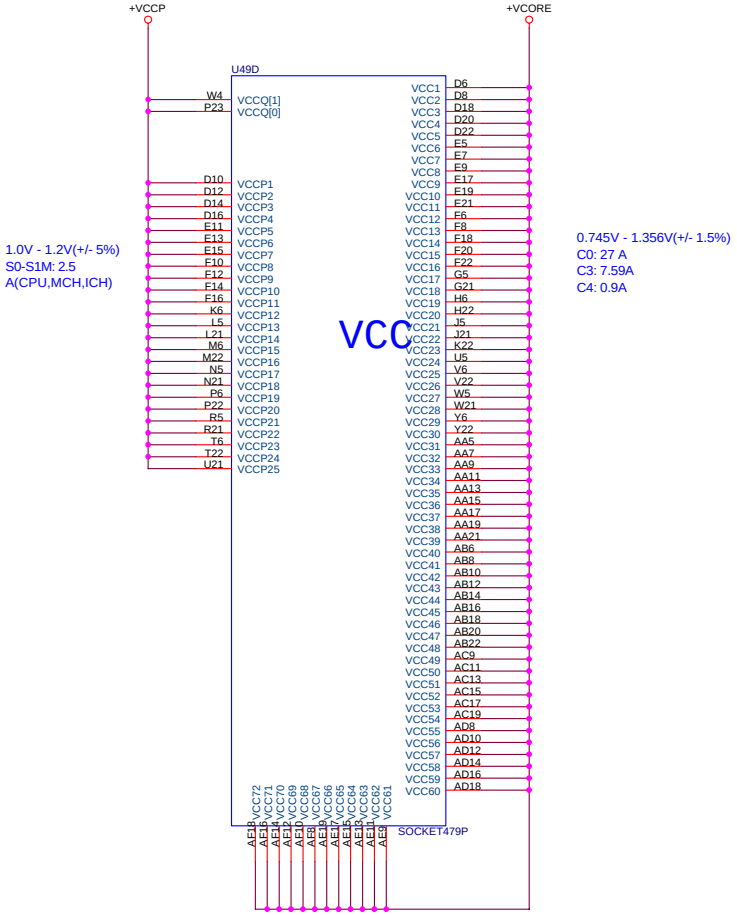
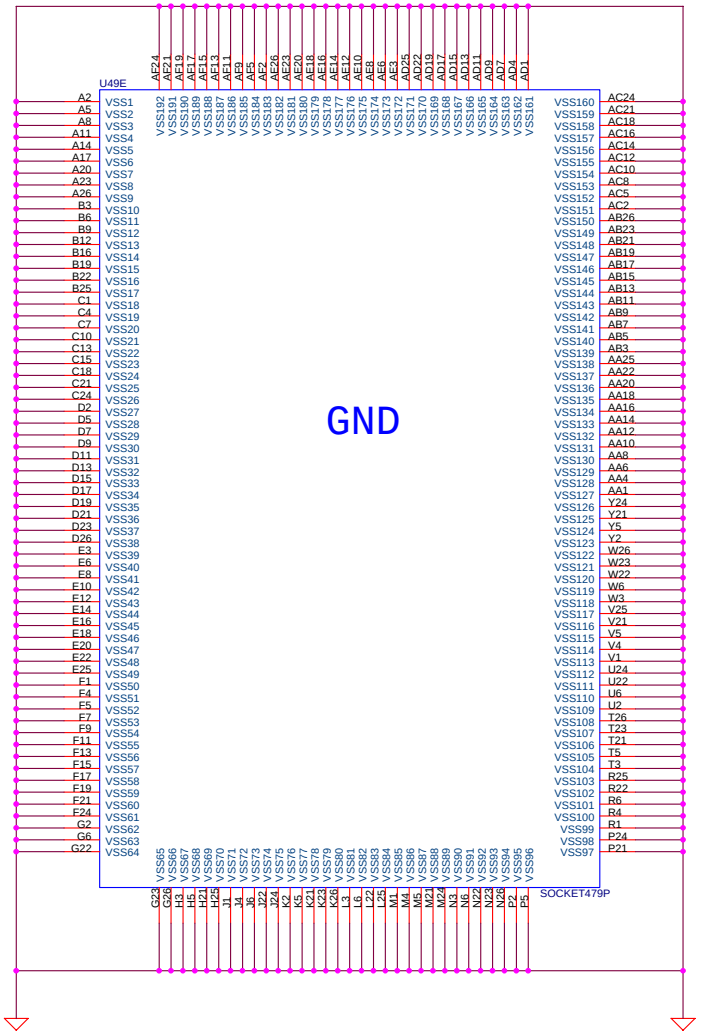
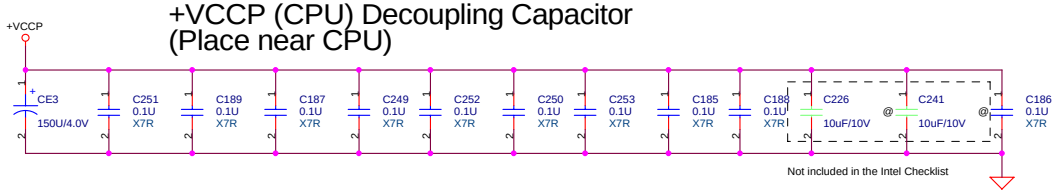


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: DOTHAN - MAIN (1)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 3 OF 61		LIBRARY DATE :	



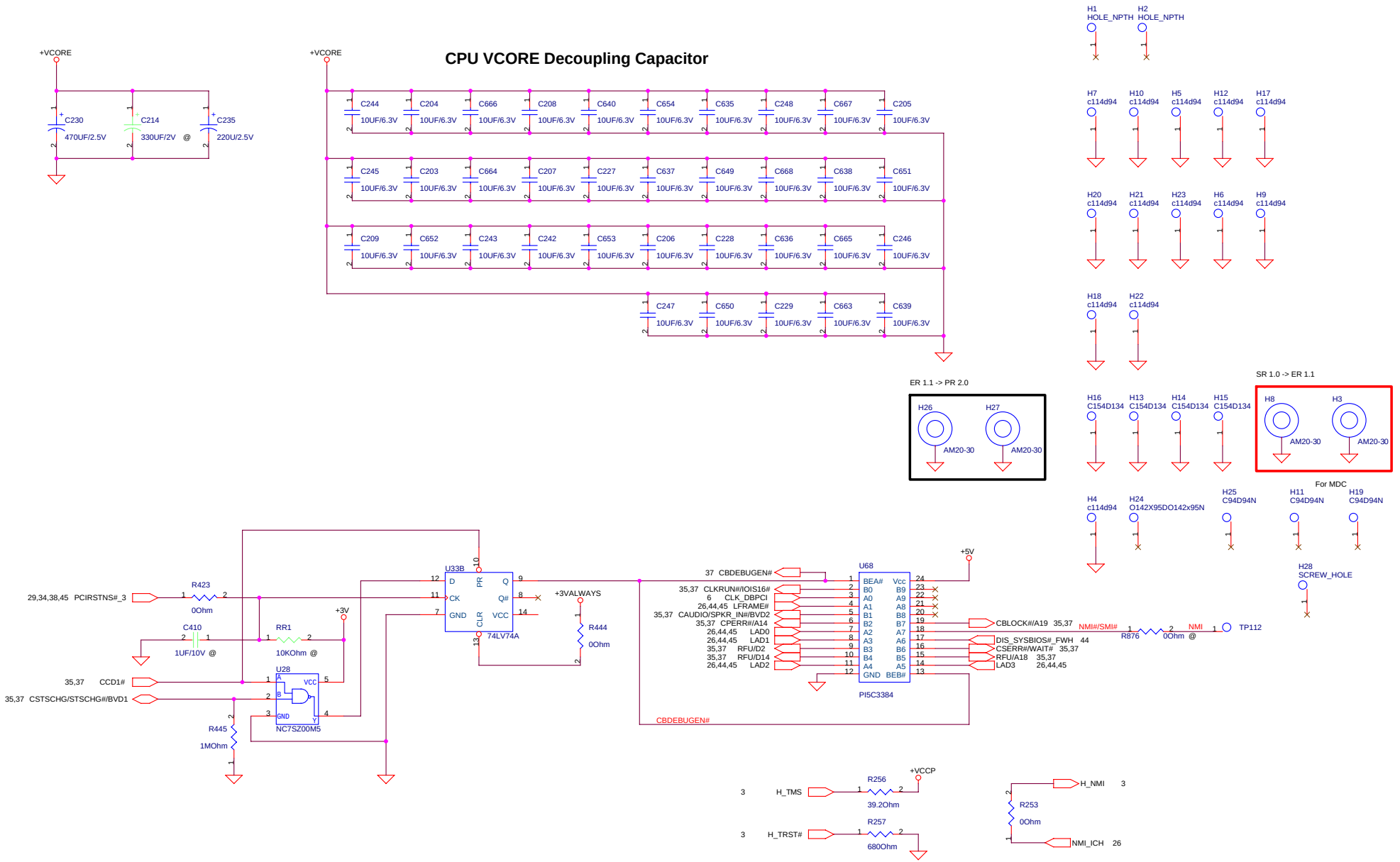


+VCCP (CPU) Decoupling Capacitor (Place near CPU)



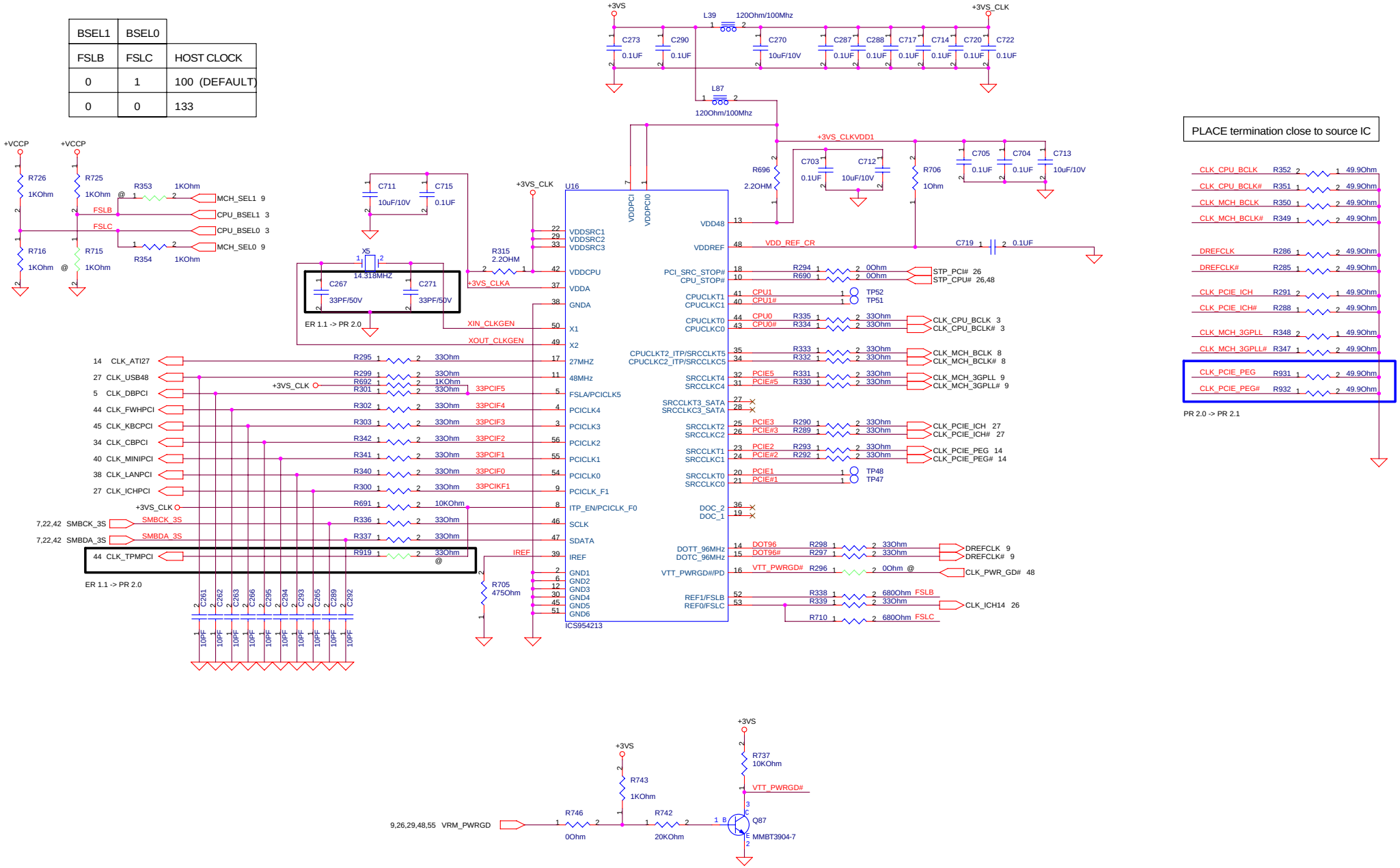
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: DOTHAN - POWER&GND (2)	SCHEMATIC FILE NAME : <Doc>
		SHEET 4 OF 61		LIBRARY DATE :

DESIGN ENGINEER :



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CPU CAPS& DEBUG CARD	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 5 OF 61		LIBRARY DATE :	

BSEL1	BSEL0	
FSLB	FSLC	HOST CLOCK
0	1	100 (DEFAULT)
0	0	133



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CLOCK GENERATOR	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
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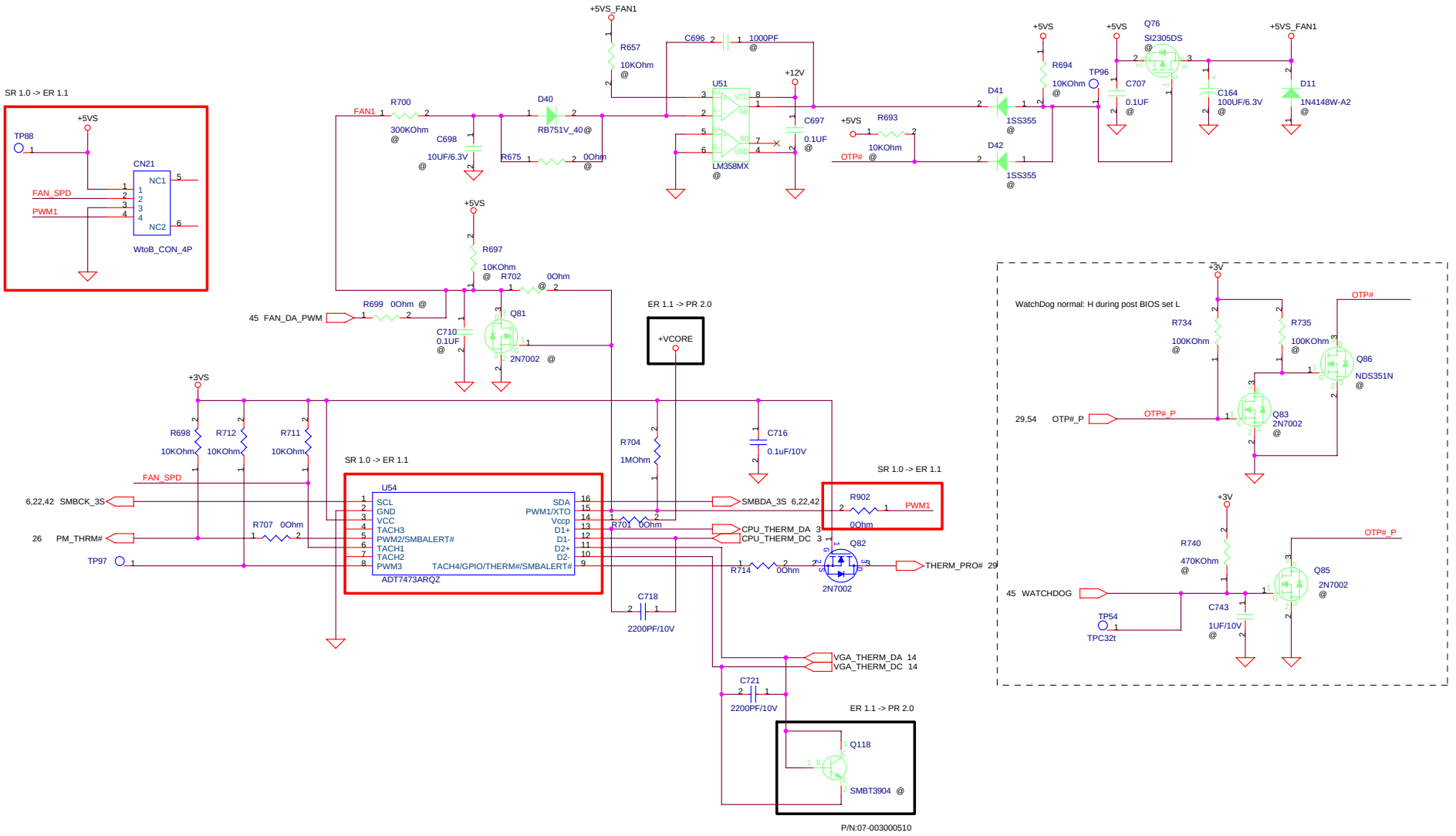
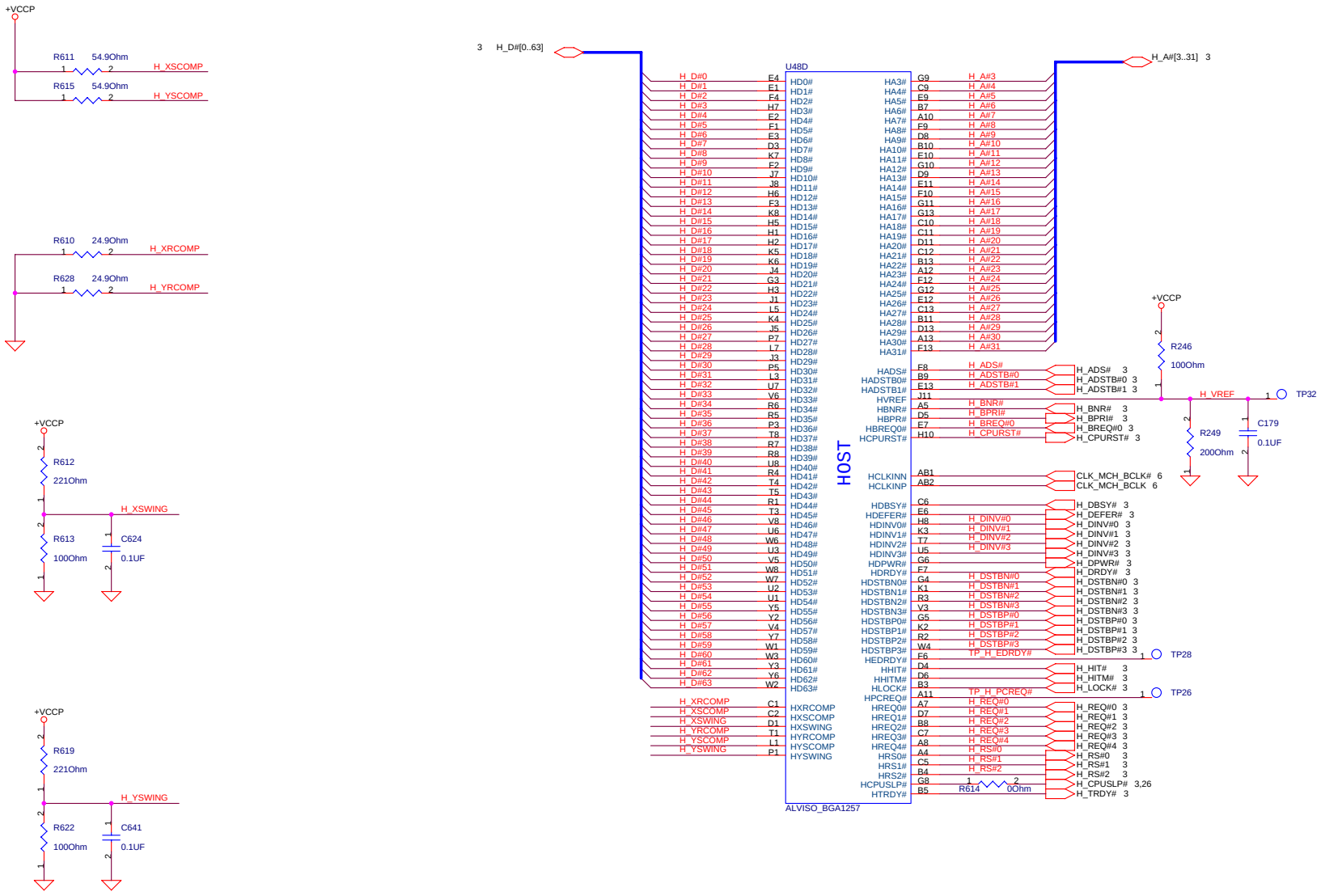
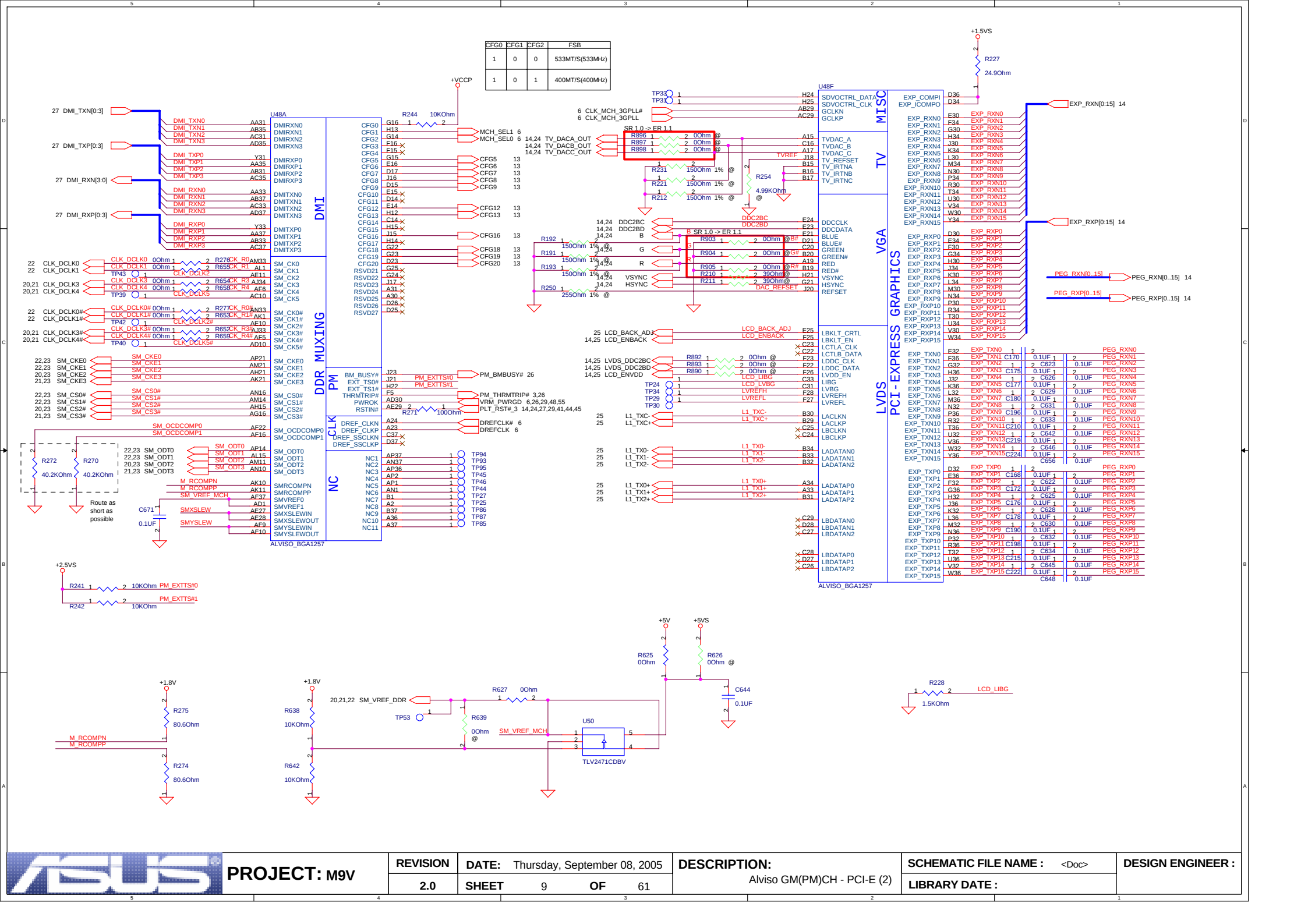
FAN



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: FAN & THERMAL SENSOR	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 7 OF 61		LIBRARY DATE :	



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: Alviso GM(PM)CH - HOST (1)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 8 OF 61		LIBRARY DATE :	



PROJECT: M9V	REVISION: 2.0	DATE: Thursday, September 08, 2005	DESCRIPTION: Alviso GM(PM)CH - PCI-E (2)
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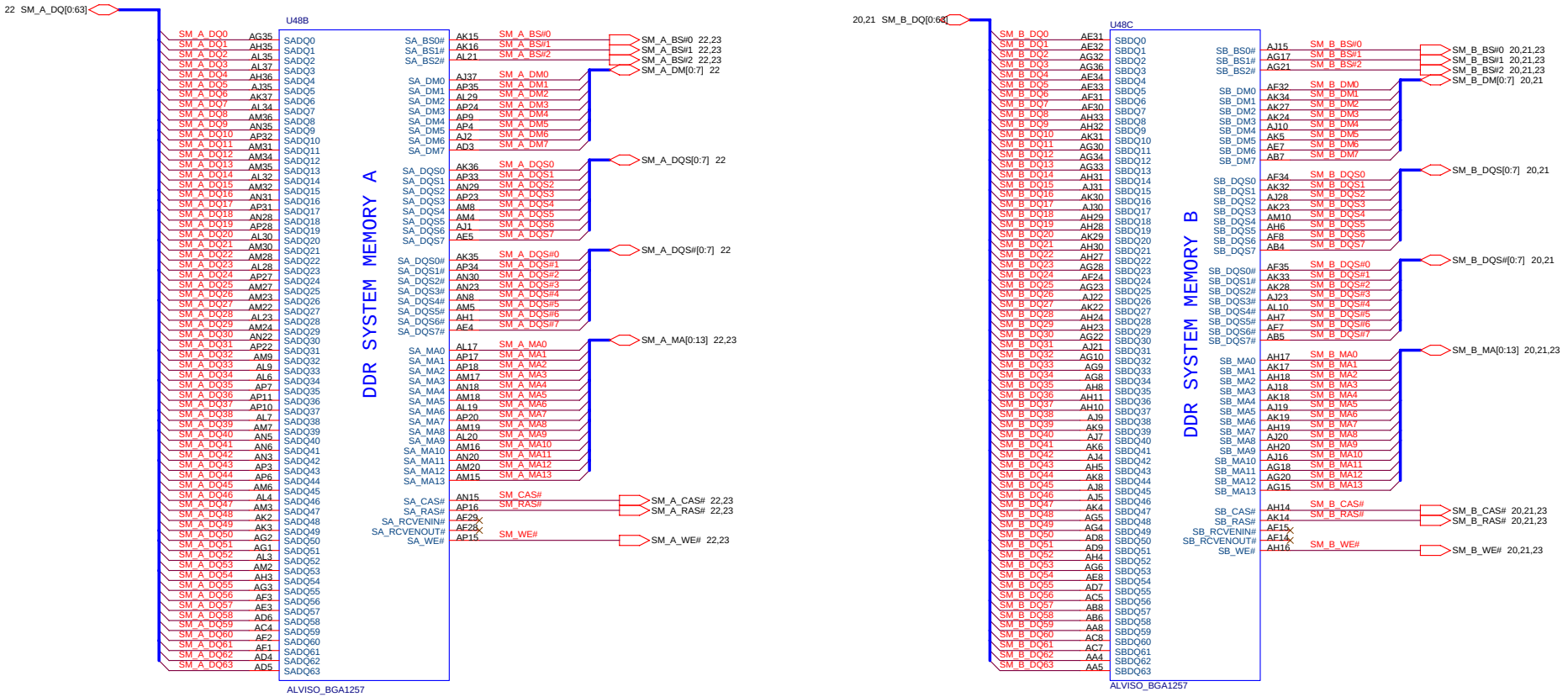
			DESIGN ENGINEER :



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: Alviso GM(PM)CH - DDR (3)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
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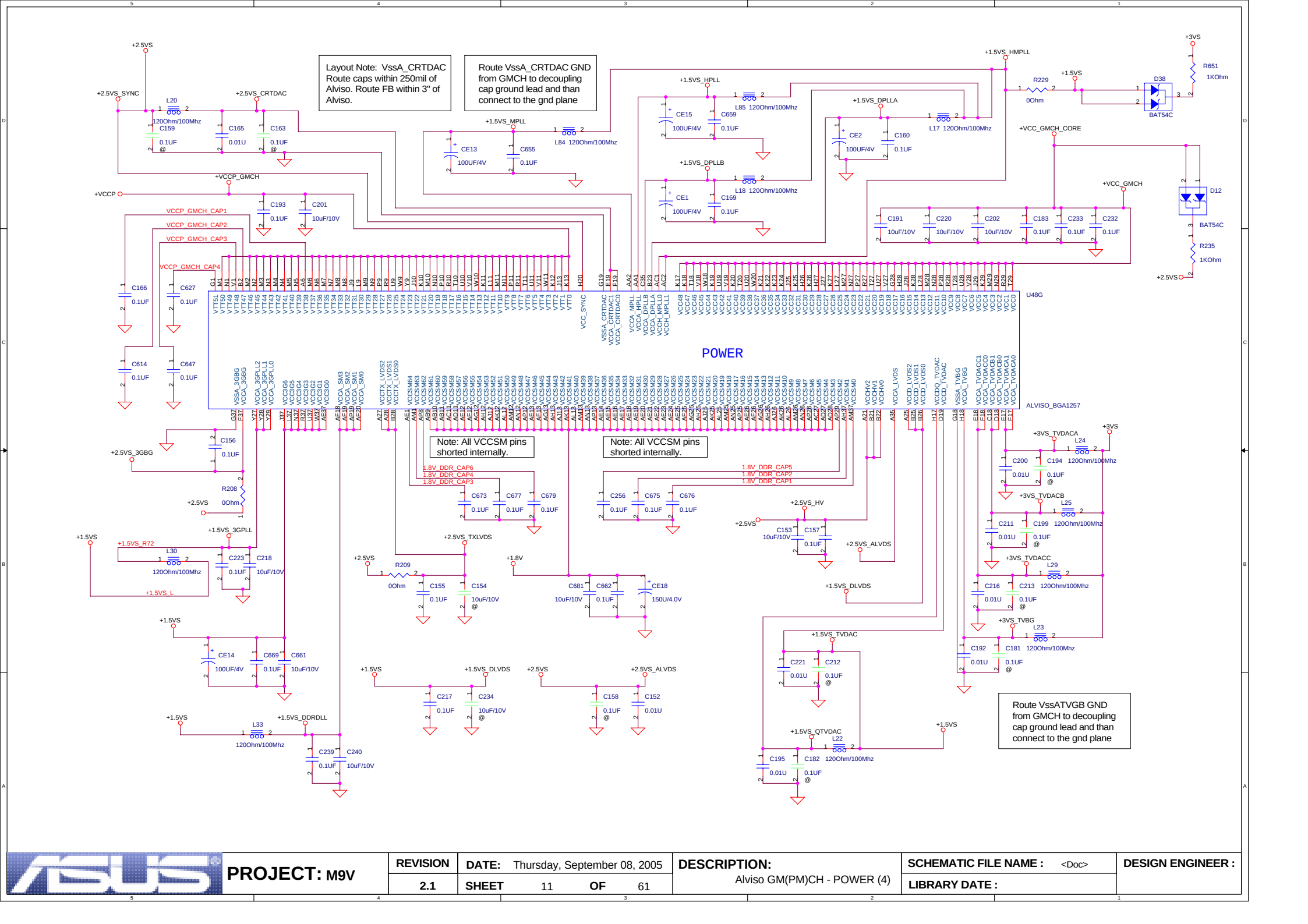
Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
POWER
U48G
ALVISO_BGA1257
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
+2.5VS
+2.5VS_SYNC
+2.5VS_CRTDAC
+2.5VS_3GBG
+2.5VS_HV
+2.5VS_ALVDS
+1.5VS
+1.5VS_HMPLL
+1.5VS_HPLL
+1.5VS_MPLL
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_3GPLL
+1.5VS_DLVDS
+1.5VS_TVDAC
+1.5VS_QTVDAC
+1.5VS_DDRDLL
+2.5VS_TXLVDS
+1.8V
+3VS
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
+3VS_TVBG
+VCCP
+VCCP_GMCH
+VCC_GMCH_CORE
+VCC_GMCH
VCCP_GMCH_CAP1
VCCP_GMCH_CAP2
VCCP_GMCH_CAP3
VCCP_GMCH_CAP4
1.8V_DDR_CAP6
1.8V_DDR_CAP4
1.8V_DDR_CAP3
1.8V_DDR_CAP5
1.8V_DDR_CAP2
1.8V_DDR_CAP1
+1.5VS_R72
+1.5VS_L
L20 120Ohm/100Mhz
L85 120Ohm/100Mhz
L84 120Ohm/100Mhz
L18 120Ohm/100Mhz
L17 120Ohm/100Mhz
L30 120Ohm/100Mhz
L33 120Ohm/100Mhz
L24 120Ohm/100Mhz
L25 120Ohm/100Mhz
L29 120Ohm/100Mhz
L23 120Ohm/100Mhz
L22 120Ohm/100Mhz
R651 1KOhm
R229 0Ohm
R208 0Ohm
R209 0Ohm
R235 1KOhm
D38 BAT54C
D12 BAT54C
C159 0.1UF @
C165 0.01U
C163 0.1UF @
CE15 100UF/4V
C659 0.1UF
CE13 100UF/4V
C655 0.1UF
CE2 100UF/4V
C160 0.1UF
CE1 100UF/4V
C169 0.1UF
C193 0.1UF
C201 10uF/10V
C191 10uF/10V
C220 10uF/10V
C202 10uF/10V
C183 0.1UF
C233 0.1UF
C232 0.1UF
C166 0.1UF
C627 0.1UF
C614 0.1UF
C647 0.1UF
C156 0.1UF
C673 0.1UF
C677 0.1UF
C679 0.1UF
C256 0.1UF
C675 0.1UF
C676 0.1UF
C153 10uF/10V
C157 0.1UF
C223 0.1UF
C218 10uF/10V
C155 0.1UF
C154 10uF/10V @
C681 10uF/10V
C662 0.1UF
CE18 150U/4.0V
CE14 100UF/4V
C669 0.1UF
C661 10uF/10V
C217 0.1UF
C234 10uF/10V @
C158 0.1UF @
C152 0.01U
C239 0.1UF
C240 10uF/10V
C200 0.01U
C194 0.1UF @
C211 0.01U
C199 0.1UF @
C216 0.01U
C213 0.1UF @
C192 0.01U
C181 0.1UF @
C221 0.01U
C212 0.1UF @
C195 0.01U
C182 0.1UF @
PROJECT: M9V
REVISION 2.1
DATE: Thursday, September 08, 2005
SHEET 11 OF 61
DESCRIPTION: Alviso GM(PM)CH - POWER (4)
SCHEMATIC FILE NAME : <Doc>
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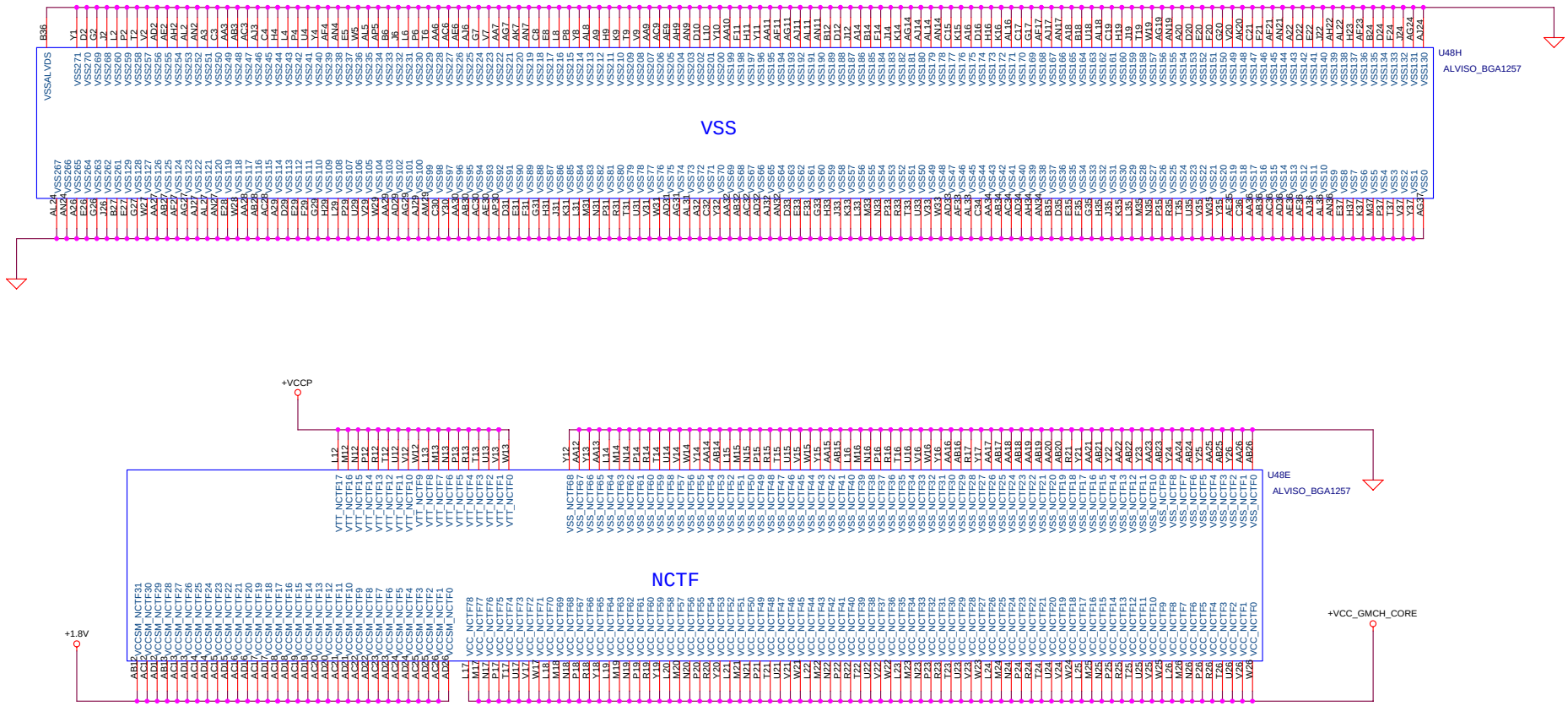
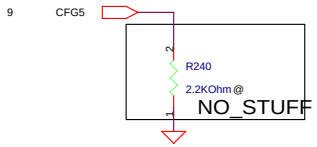
DESIGN ENGINEER :

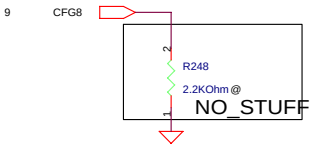


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: Alviso GM(PM)CH - GND (5)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 12 OF 61		LIBRARY DATE :	

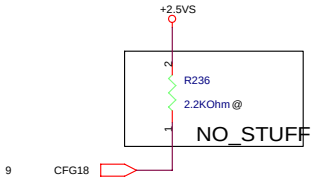
CFG5 : DMI x2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



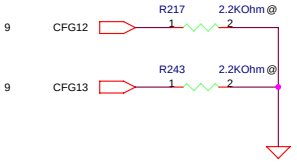
CFG8 : PCI-X POWER SAVING
LOW = PCI-X Power Saving
HIGH = (Default)



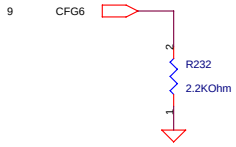
CFG18 : GMCH core VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V



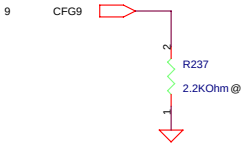
CFG12 : XOR/ALL Z test straps
CFG13 : XOR/ALL Z test straps
LOW LOW = Reserved
LOW HIGH = XOR Mode Enabled
HIGH LOW = All Z Mode Enabled
HIGH HIGH = Normal Operation (Default)



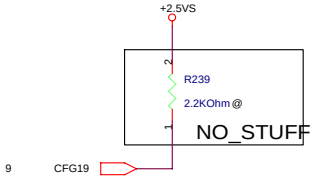
CFG6 : DDR vs DDR2 select
LOW = DDR2
HIGH = DDR (Default)



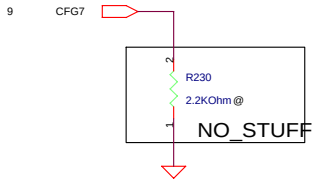
CFG9 : PCI Express Graphic Lane Reversal
LOW = Reverse Lane
HIGH = Normal Operation (Default)



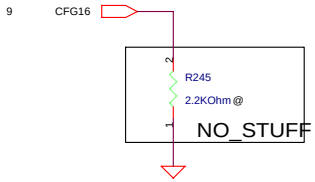
CFG19 : CPU VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V



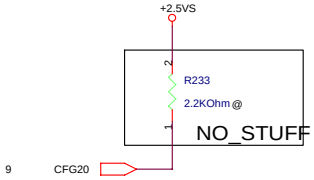
CFG7 : CPU Strap
LOW = Reserved
HIGH = Dothan (Default)



CFG16 : FSB Dynamic ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



CFG20 : SDVO Present
LOW = No SDVO device present (Default)
HIGH = SDVO device present



CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

SDVOCRTL_DATA LOW = No SDVO device present (Default)

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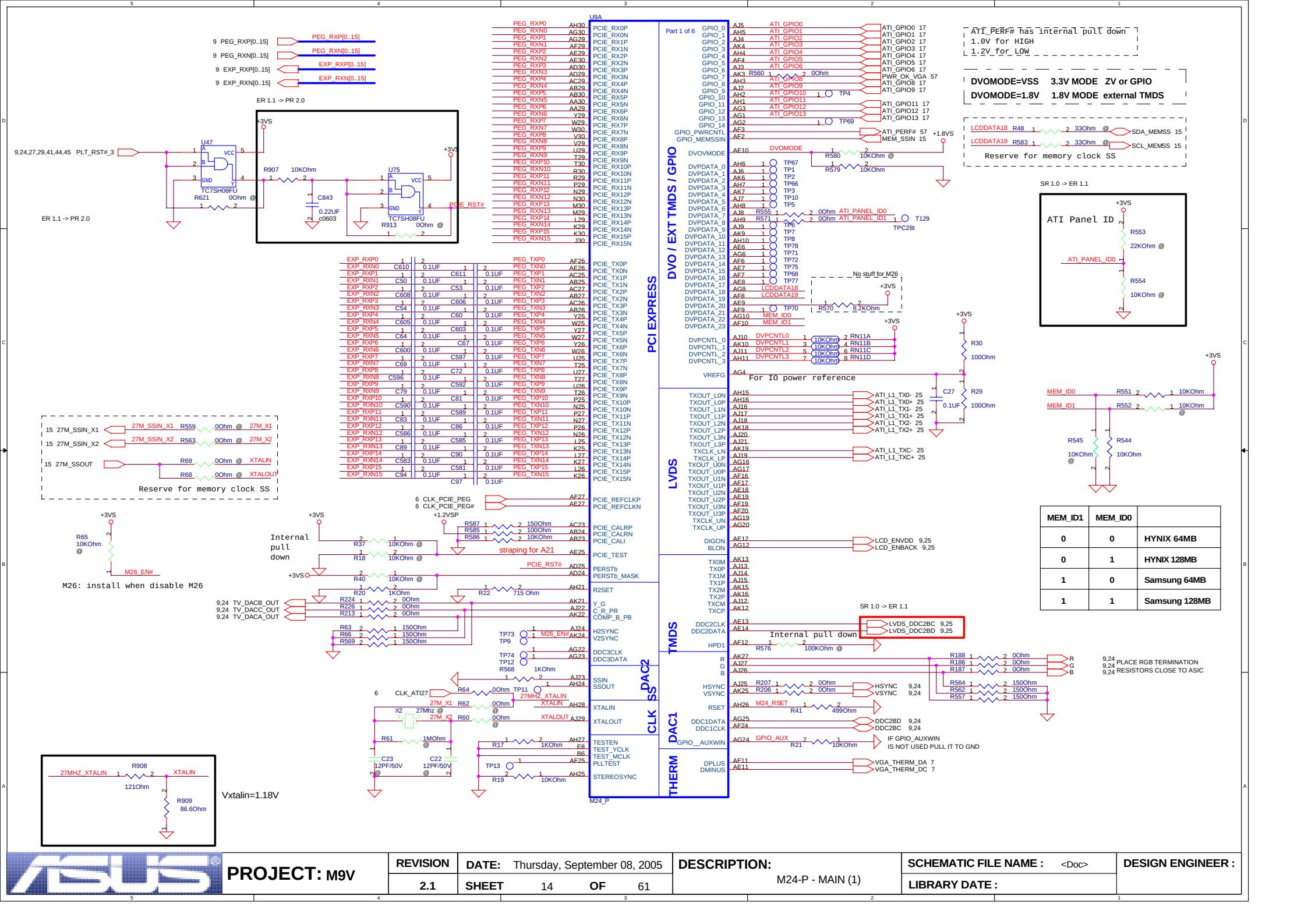

MEM_ID1	MEM_ID0	
0	0	HYNIX 64MB
0	1	HYNIX 128MB
1	0	Samsung 64MB
1	1	Samsung 128MB

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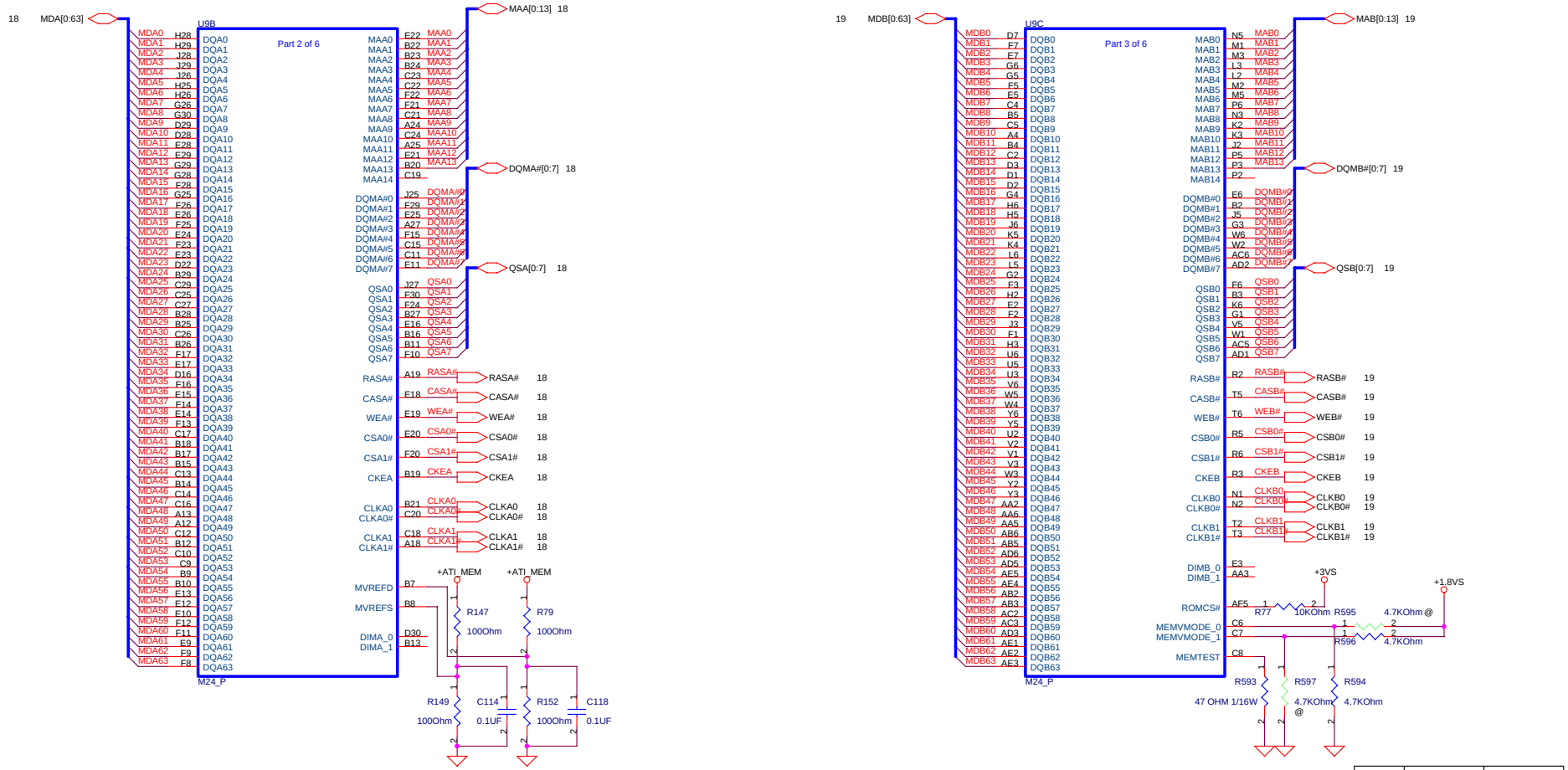
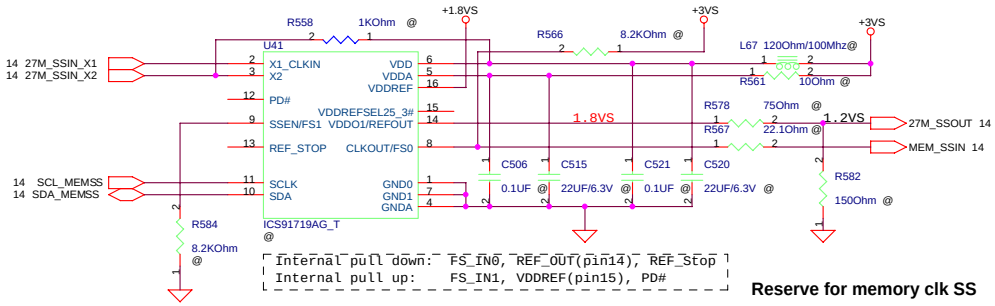


VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+1.8VS
2.5V	+1.8VS	GND



Reserve for memory clk SS

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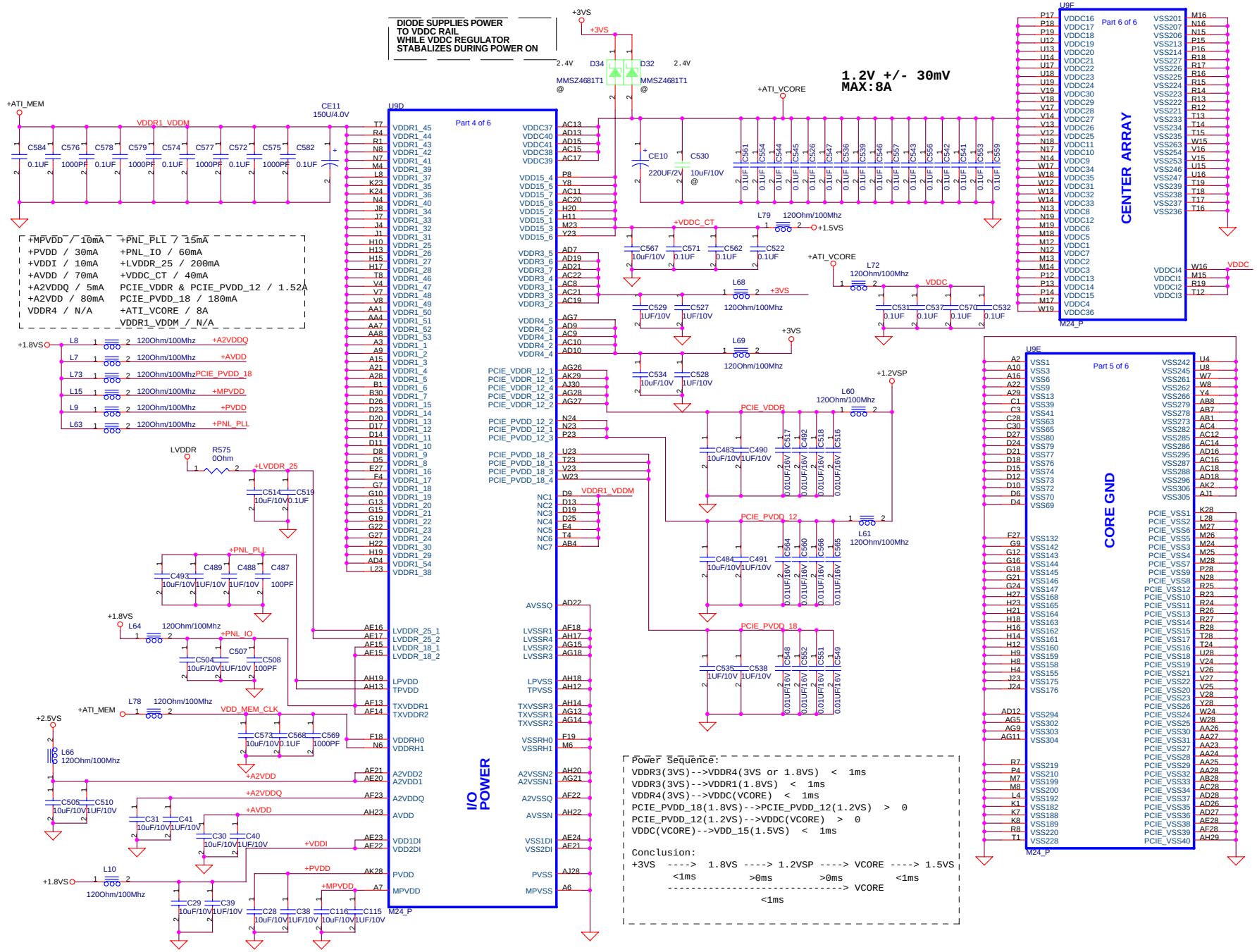

PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: M24-P - POWER (3)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
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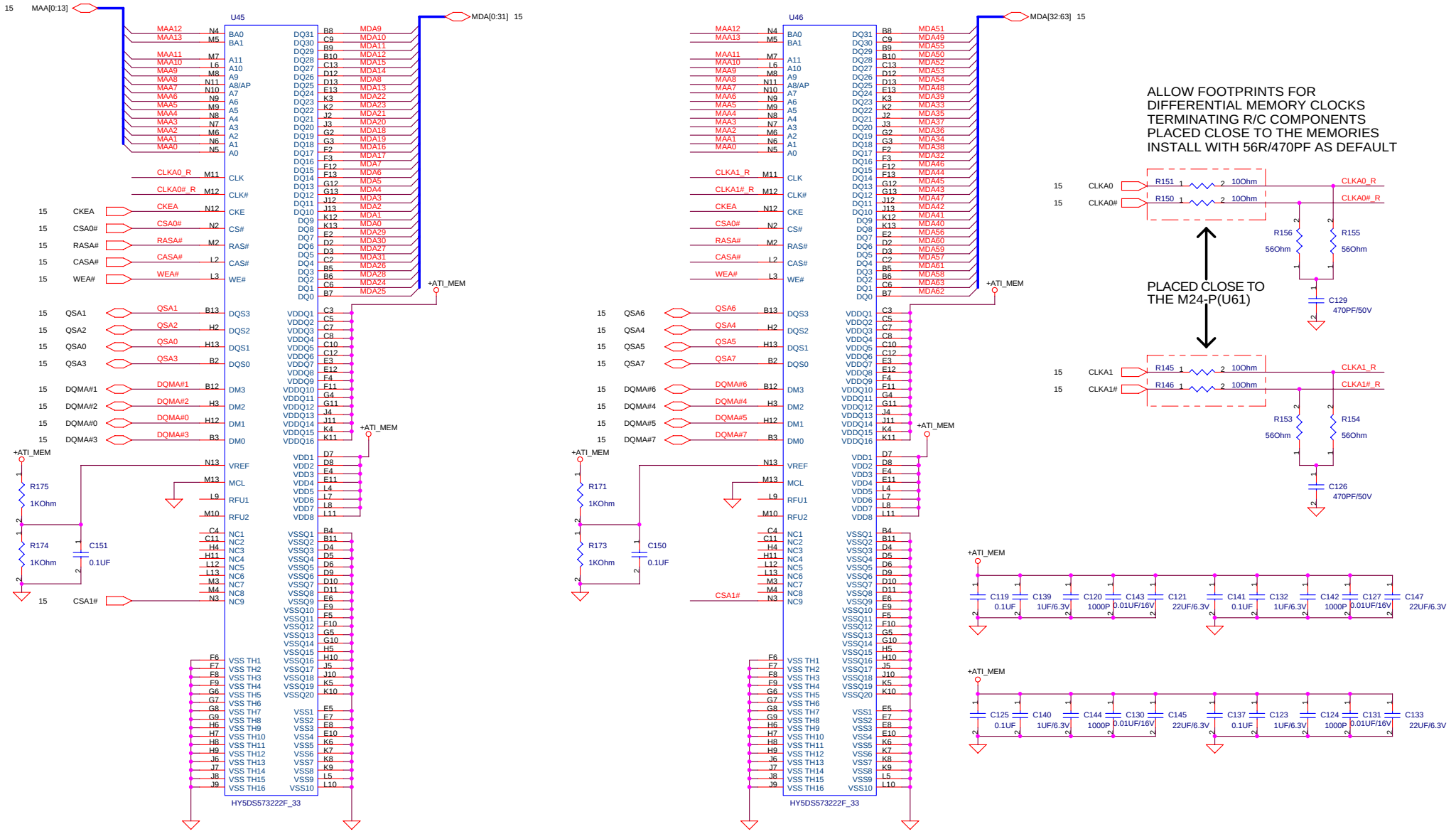
OPTION STRAPS

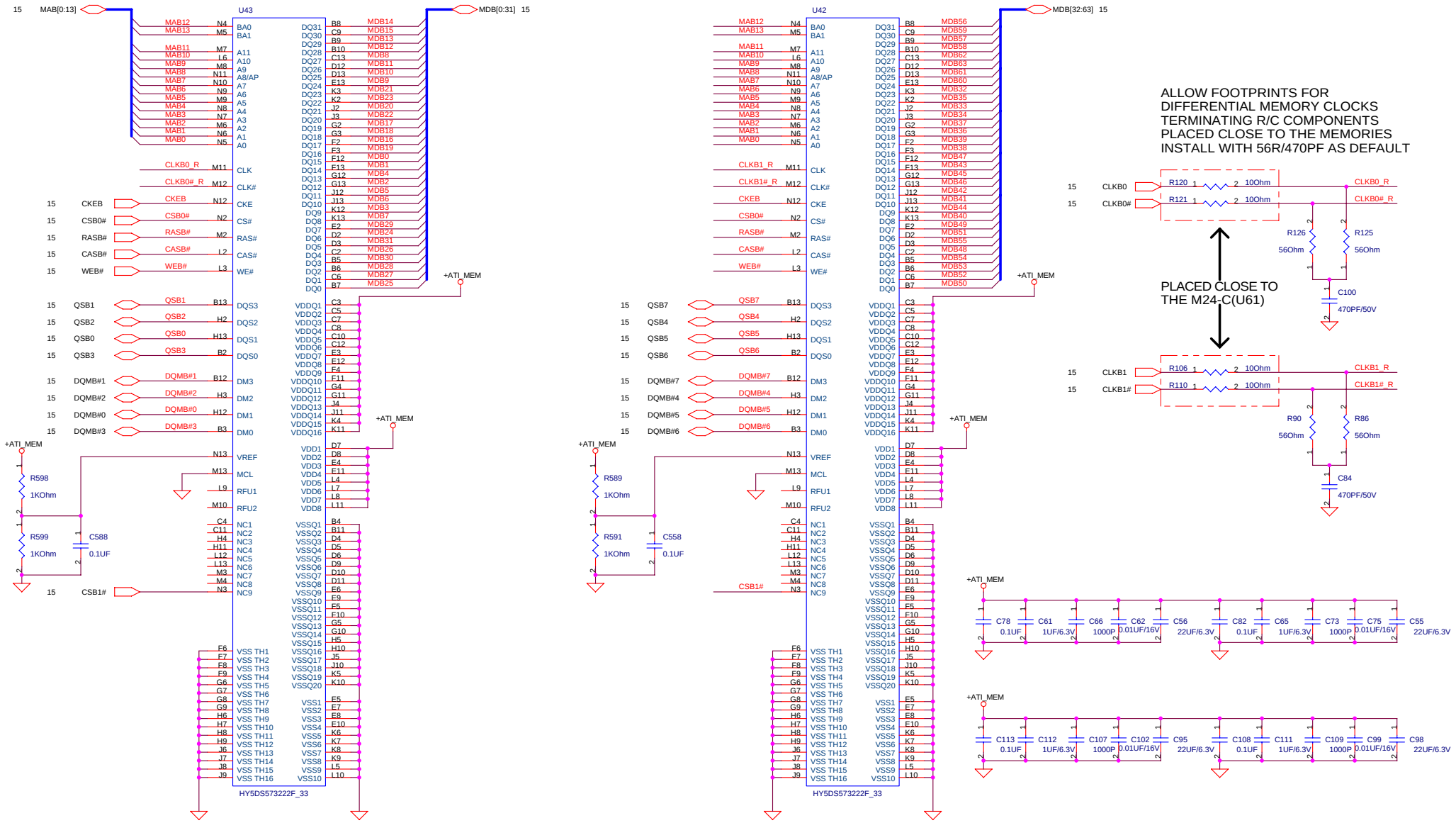
GPIO[0:13] : Internal PD

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing	0
B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de_emphasis enable	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal	00
B_PTX_IEXT	GPIO4	**0: normal mode** **1: extra current in Tx output stage**	0
FORCE_COMPLIANCE	GPIO5	Force chip to go to compliance state quickly for test purposes	0
B_PPLL_BW	GPIO6	0: Full PLL Bandwidth 1: Reduce PLL Bandwidth	0
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	0000
	DVPDATA_20	0: Slave VIP host port device peesent 1: No slave VIP host port device	0

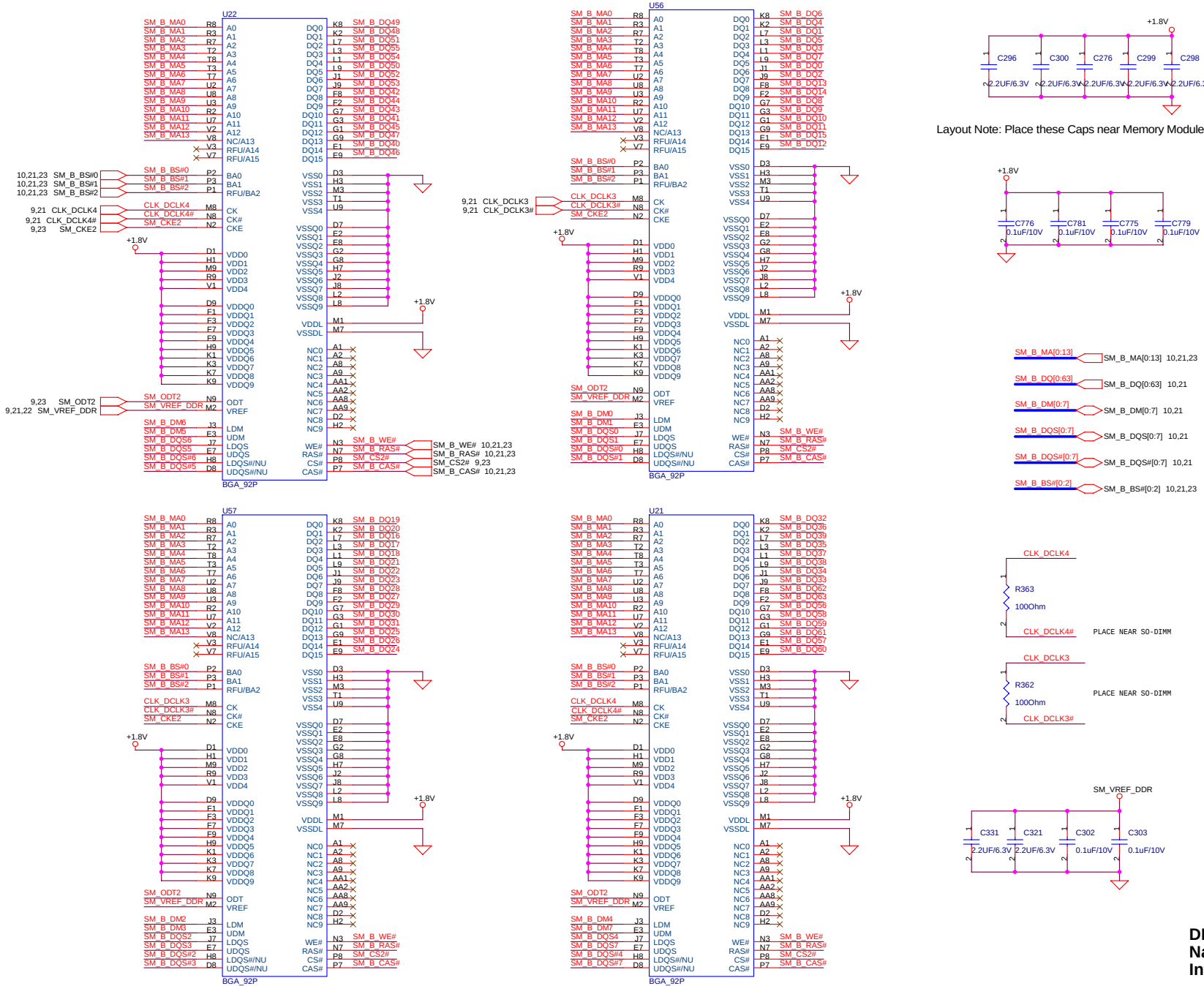
M26: GPIO11 is memory aperture (0=128M 1=256M)



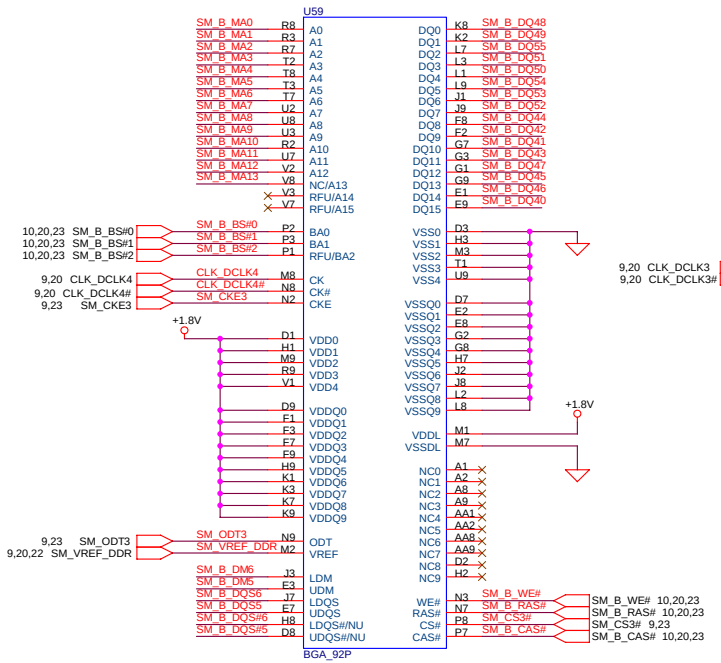
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: M24-C - DDR MEMORY A	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 18 OF 61		LIBRARY DATE :	

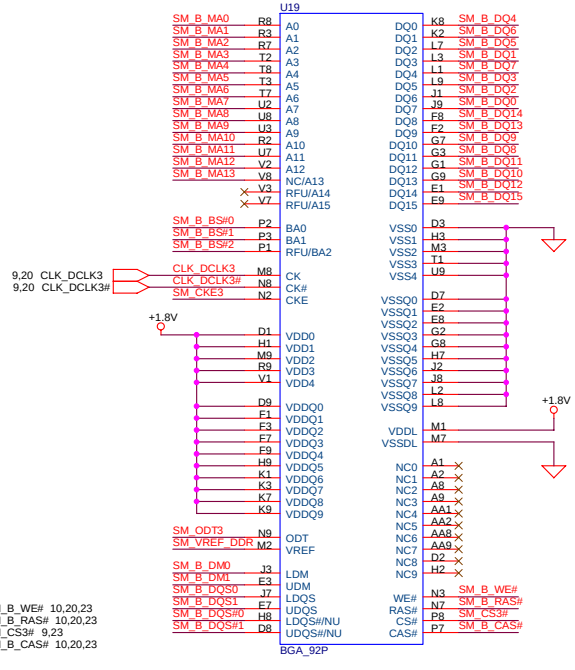


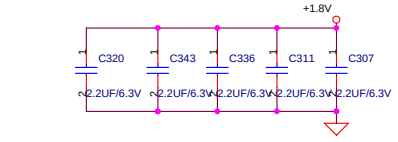
PROJECT: M9V	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** M24-C - DDR MEMORY B	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 19 **OF** 61		**LIBRARY DATE :**	



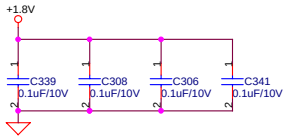
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: DDR2 (1)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 20 OF 61		LIBRARY DATE :	

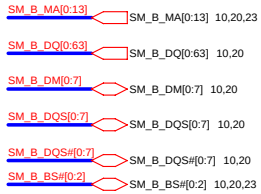


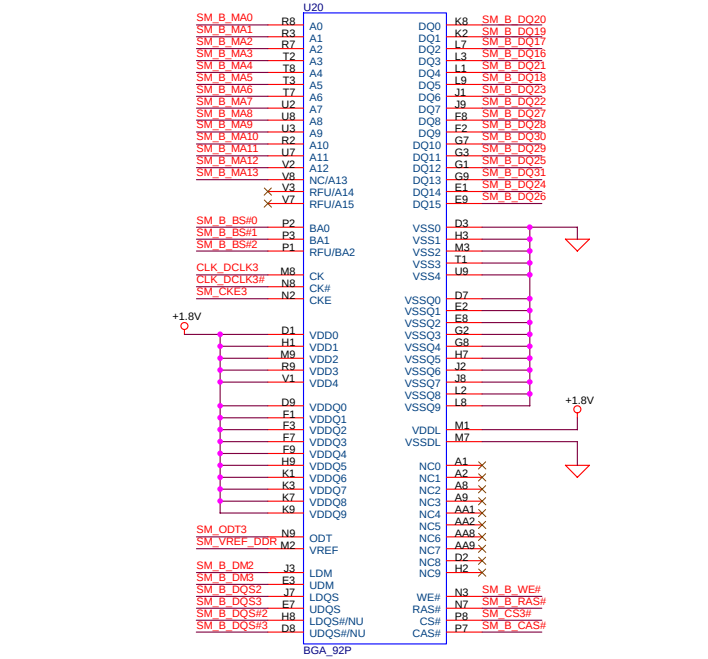


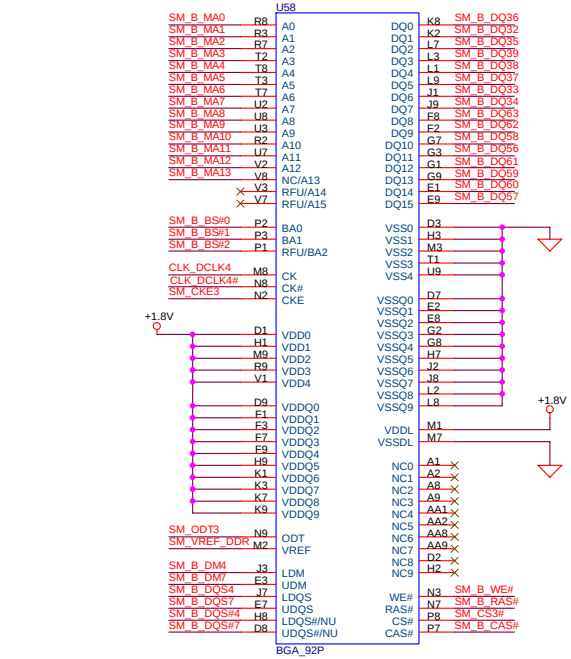


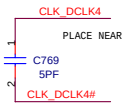
Layout Note: Place these Caps near Memory Module

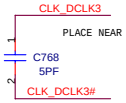


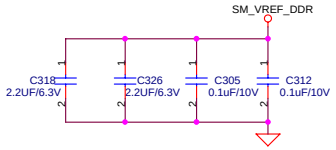












PROJECT: M9V	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** DDR2 (2)	**SCHEMATIC FILE NAME :** <Doc>
		SHEET 21 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :

SM_A_DQ[63:0] 10

SM_A_MA[13:0] 10,23

SM_A_DM[7:0] 10

SM_A_DQS[0:7]

SM_A_DQS[0:7] 10

SM_A_DQS#[0:7]

SM_A_DQS#[0:7] 10

NO STUFF

*

CLK_DCLK0

C723

PLACE NEAR SO-DIMM_1

10P @

CLK_DCLK0#

CLK_DCLK1

C724

PLACE NEAR SO-DIMM_1

10P @

CLK_DCLK1#

10,23 SM_A_MA[0:13]

SM_A_DQ[0:63] 10

CN28A

SM_A_MA0	102	A0	DQ0	5	SM_A_DQ0
SM_A_MA1	101	A1	DQ1	7	SM_A_DQ1
SM_A_MA2	100	A2	DQ2	17	SM_A_DQ2
SM_A_MA3	99	A3	DQ3	19	SM_A_DQ7
SM_A_MA4	98	A4	DQ4	4	SM_A_DQ4
SM_A_MA5	97	A5	DQ5	6	SM_A_DQ1
SM_A_MA6	94	A6	DQ6	14	SM_A_DQ6
SM_A_MA7	92	A7	DQ7	16	SM_A_DQ3
SM_A_MA8	93	A8	DQ8	23	SM_A_DQ13
SM_A_MA9	91	A9	DQ9	25	SM_A_DQ12
SM_A_MA10	105	A10/AP	DQ10	35	SM_A_DQ10
SM_A_MA11	90	A11	DQ11	37	SM_A_DQ11
SM_A_MA12	89	A12	DQ12	20	SM_A_DQ8
SM_A_MA13	116	A13	DQ13	22	SM_A_DQ9
	86	A14	DQ14	36	SM_A_DQ14
	84	A15	DQ15	38	SM_A_DQ15
10,23 SM_A_BS#2	85	A16_BA2	DQ16	43	SM_A_DQ16
			DQ17	45	SM_A_DQ20
			DQ18	55	SM_A_DQ22
10,23 SM_A_BS#0	107	BA0	DQ19	57	SM_A_DQ23
10,23 SM_A_BS#1	106	BA1	DQ20	44	SM_A_DQ17
9,23 SM_CS0#	110	S0#	DQ21	46	SM_A_DQ21
9,23 SM_CS1#	115	S1#	DQ22	56	SM_A_DQ18
9 CLK_DCLK0	30	CK0	DQ23	58	SM_A_DQ19
9 CLK_DCLK0#	32	CK0#	DQ24	61	SM_A_DQ24
9 CLK_DCLK1	164	CK1	DQ25	63	SM_A_DQ25
9 CLK_DCLK1#	166	CK1#	DQ26	73	SM_A_DQ27
9,23 SM_CKE0	79	CKE0	DQ27	75	SM_A_DQ31
9,23 SM_CKE1	80	CKE1	DQ28	62	SM_A_DQ29
10,23 SM_A_CAS#	113	CAS#	DQ29	64	SM_A_DQ28
10,23 SM_A_RAS#	108	RAS#	DQ30	74	SM_A_DQ26
10,23 SM_A_WE#	109	WE#	DQ31	76	SM_A_DQ30
	198	SA0	DQ32	123	SM_A_DQ32
	200	SA1	DQ33	125	SM_A_DQ33
6,7,42 SMBCK_3S	197	SCL	DQ34	135	SM_A_DQ39
6,7,42 SMBDA_3S	195	SDA	DQ35	137	SM_A_DQ34
			DQ36	124	SM_A_DQ36
9,23 SM_ODT0	114	ODT0	DQ37	126	SM_A_DQ37
9,23 SM_ODT1	119	ODT1	DQ38	134	SM_A_DQ38
10 SM_A_DM[0..7]			DQ39	136	SM_A_DQ35
SM_A_DM0	10	DM0	DQ40	141	SM_A_DQ45
SM_A_DM1	26	DM1	DQ41	143	SM_A_DQ40
SM_A_DM2	52	DM2	DQ42	151	SM_A_DQ47
SM_A_DM3	67	DM3	DQ43	153	SM_A_DQ46
SM_A_DM4	130	DM4	DQ44	140	SM_A_DQ44
SM_A_DM5	147	DM5	DQ45	142	SM_A_DQ41
SM_A_DM6	170	DM6	DQ46	152	SM_A_DQ43
SM_A_DM7	185	DM7	DQ47	154	SM_A_DQ42
10 SM_A_DQS[0..7]			DQ48	157	SM_A_DQ49
SM_A_DQS0	13	DQS0	DQ49	159	SM_A_DQ48
SM_A_DQS1	31	DQS1	DQ50	173	SM_A_DQ55
SM_A_DQS2	51	DQS2	DQ51	175	SM_A_DQ54
SM_A_DQS3	70	DQS3	DQ52	158	SM_A_DQ52
SM_A_DQS4	131	DQS4	DQ53	160	SM_A_DQ53
SM_A_DQS5	148	DQS5	DQ54	174	SM_A_DQ50
SM_A_DQS6	169	DQS6	DQ55	176	SM_A_DQ51
SM_A_DQS7	188	DQS7	DQ56	179	SM_A_DQ56
SM_A_DQS#0	11	DQS#0	DQ57	181	SM_A_DQ60
SM_A_DQS#1	29	DQS#1	DQ58	189	SM_A_DQ63
SM_A_DQS#2	49	DQS#2	DQ59	191	SM_A_DQ62
SM_A_DQS#3	68	DQS#3	DQ60	180	SM_A_DQ61
SM_A_DQS#4	129	DQS#4	DQ61	182	SM_A_DQ57
SM_A_DQS#5	146	DQS#5	DQ62	192	SM_A_DQ58
SM_A_DQS#6	167	DQS#6	DQ63	194	SM_A_DQ59
SM_A_DQS#7	186	DQS#7			

DDR_DIMM_200P

R328 10KOhm

R329 10KOhm

+3VS

C700 0.1UF

C699 0.1UF

+1.8V

CN28B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR_DIMM_200P

M_VREF_DIMM1

9,20,21 SM_VREF_DDR

C657 2.2uF/6.3V

C643 0.1UF

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C286 0.1UF

C285 0.1UF

C284 0.1UF

C283 0.1UF

Layout Note: Place these Caps near SO DIMM 1

+1.8V

C278 2.2uF/6.3V

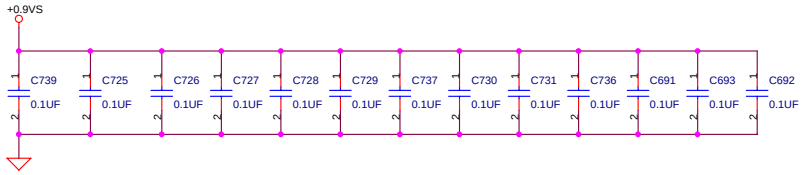
C277 2.2uF/6.3V

C279 2.2uF/6.3V

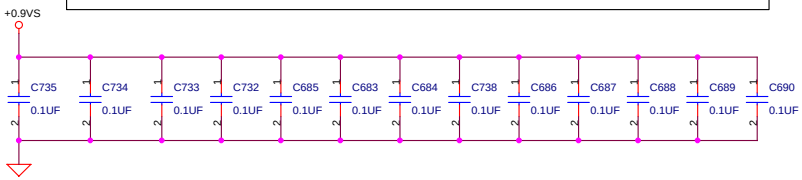
C275 2.2uF/6.3V

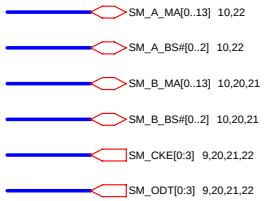
C274 2.2uF/6.3V

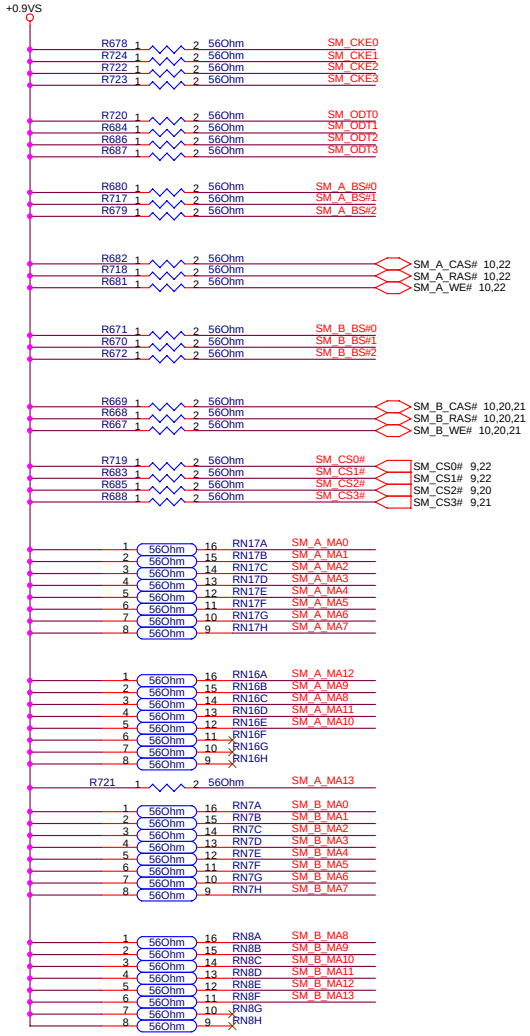
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	SHEET 22 OF 61	DESCRIPTION: STANDARD DDR2 SO-DIMM	SCHEMATIC FILE NAME : <Doc> LIBRARY DATE :	DESIGN ENGINEER :



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



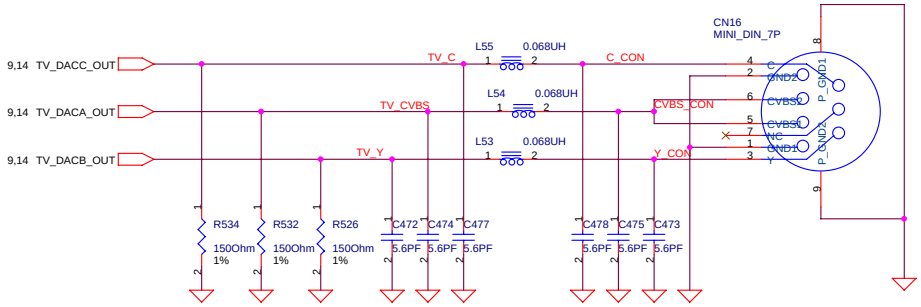


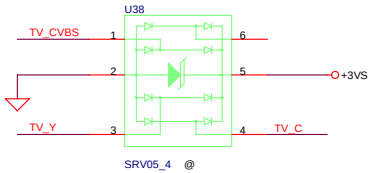


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME : <Doc>
		SHEET 23 OF 61		LIBRARY DATE :

DESIGN ENGINEER :

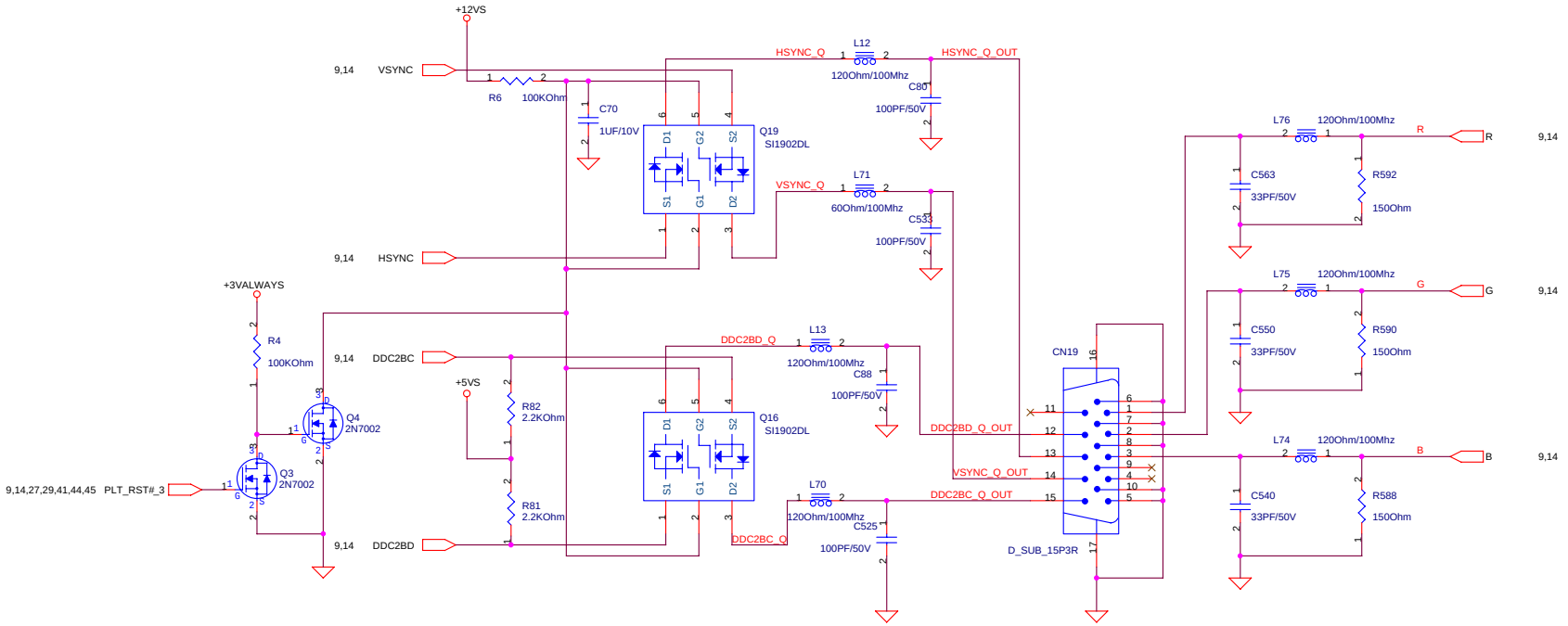
TV OUT



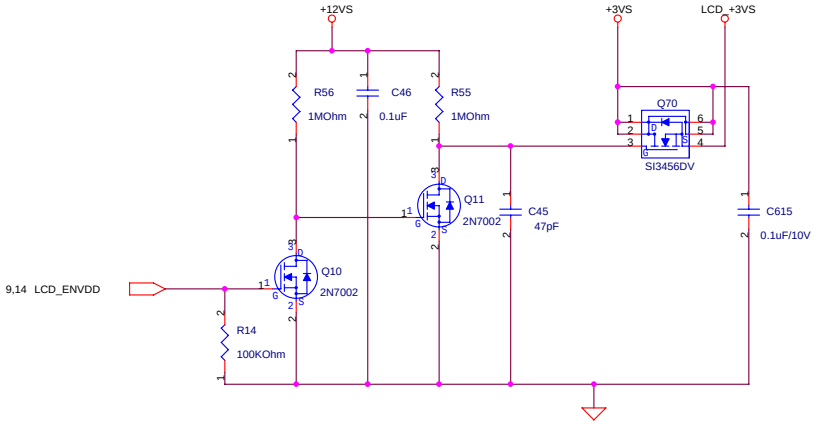


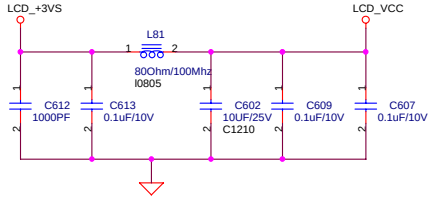
PLACE ESD Diodes near U44

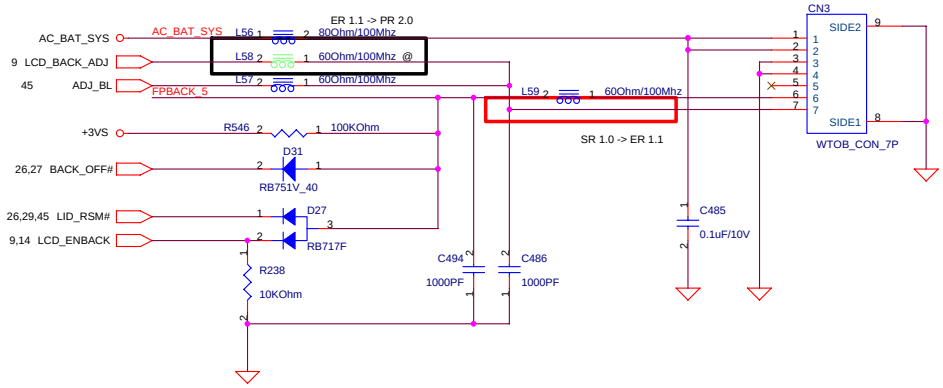
CRT Connector

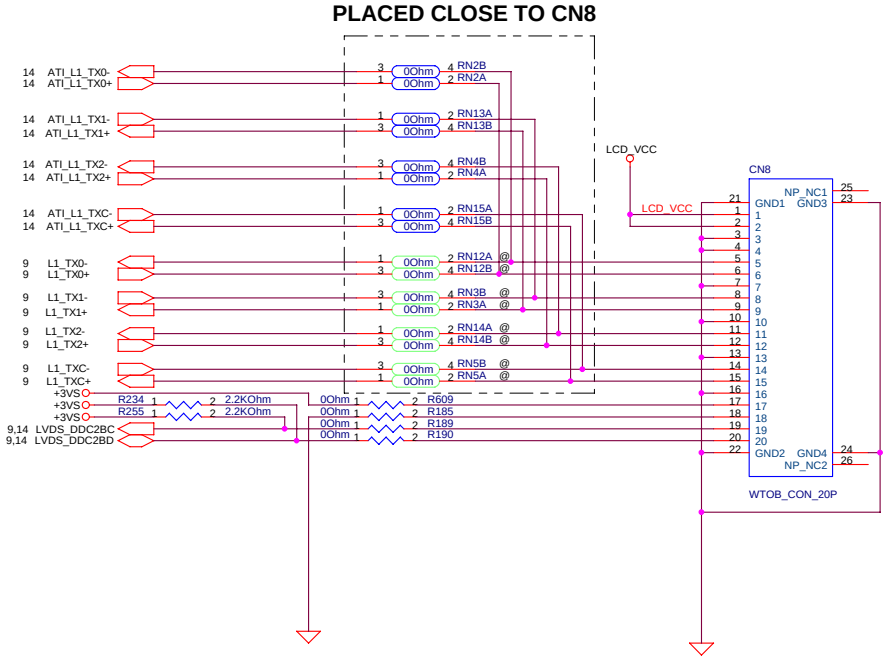


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CRT & TV OUT	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 24 OF 61		LIBRARY DATE :	

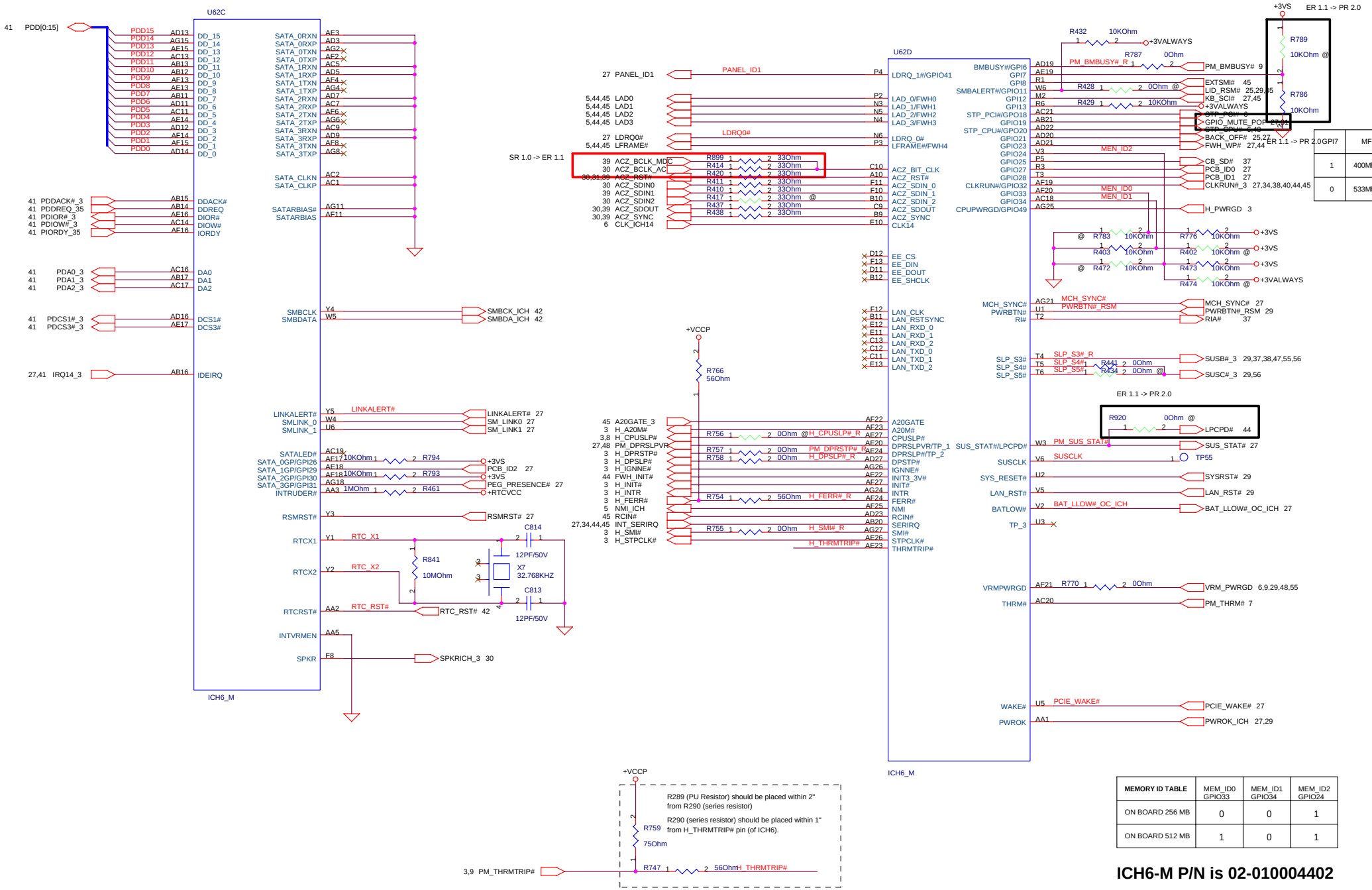








PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: LCD & INVERTER	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 25 OF 61		LIBRARY DATE :	



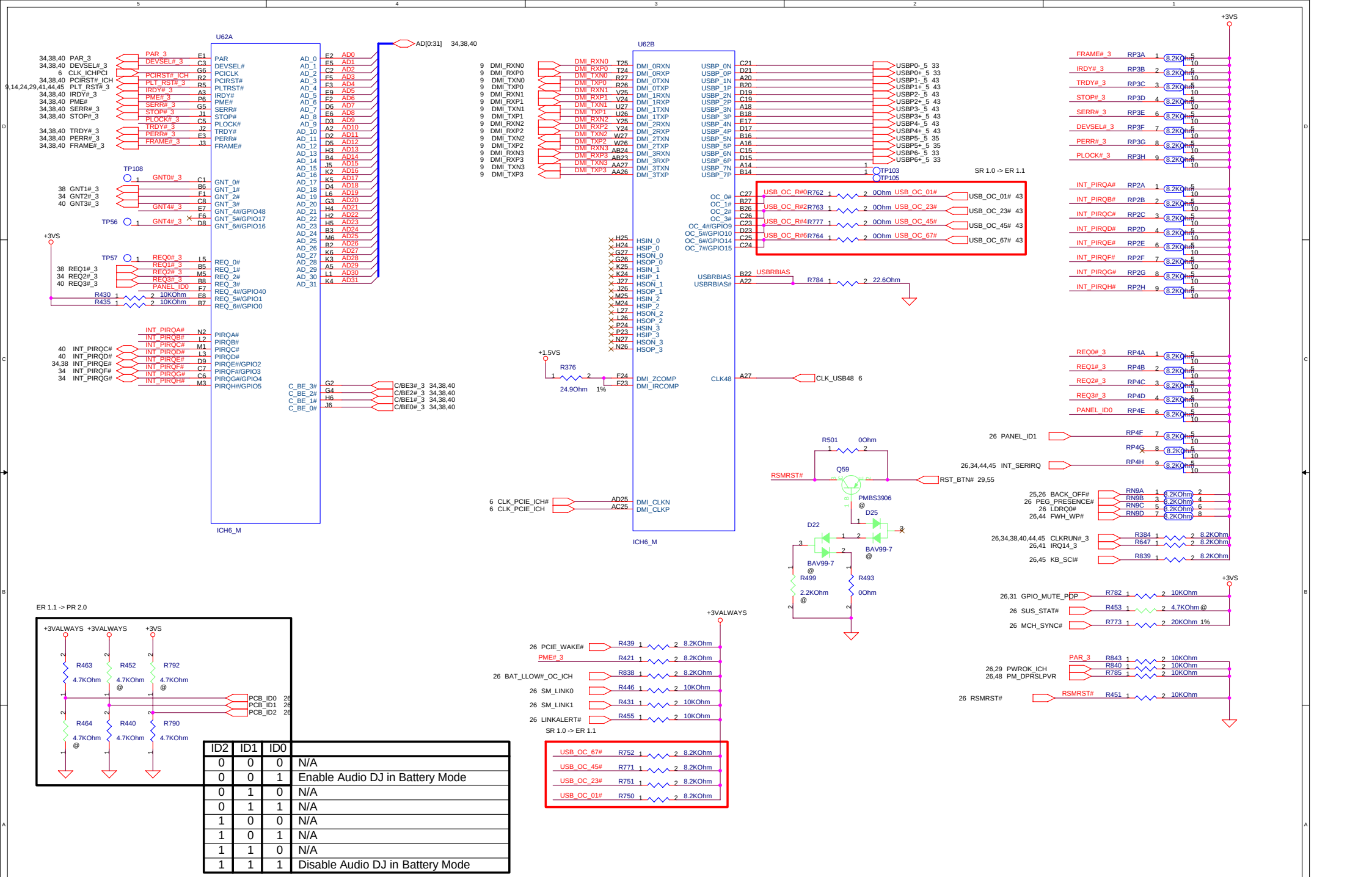
GPI7	MF
1	400Mhz
0	533Mhz

MEMORY ID TABLE	MEM_ID0 GPIO33	MEM_ID1 GPIO34	MEM_ID2 GPIO24
ON BOARD 256 MB	0	0	1
ON BOARD 512 MB	1	0	1

ICH6-M P/N is 02-010004402

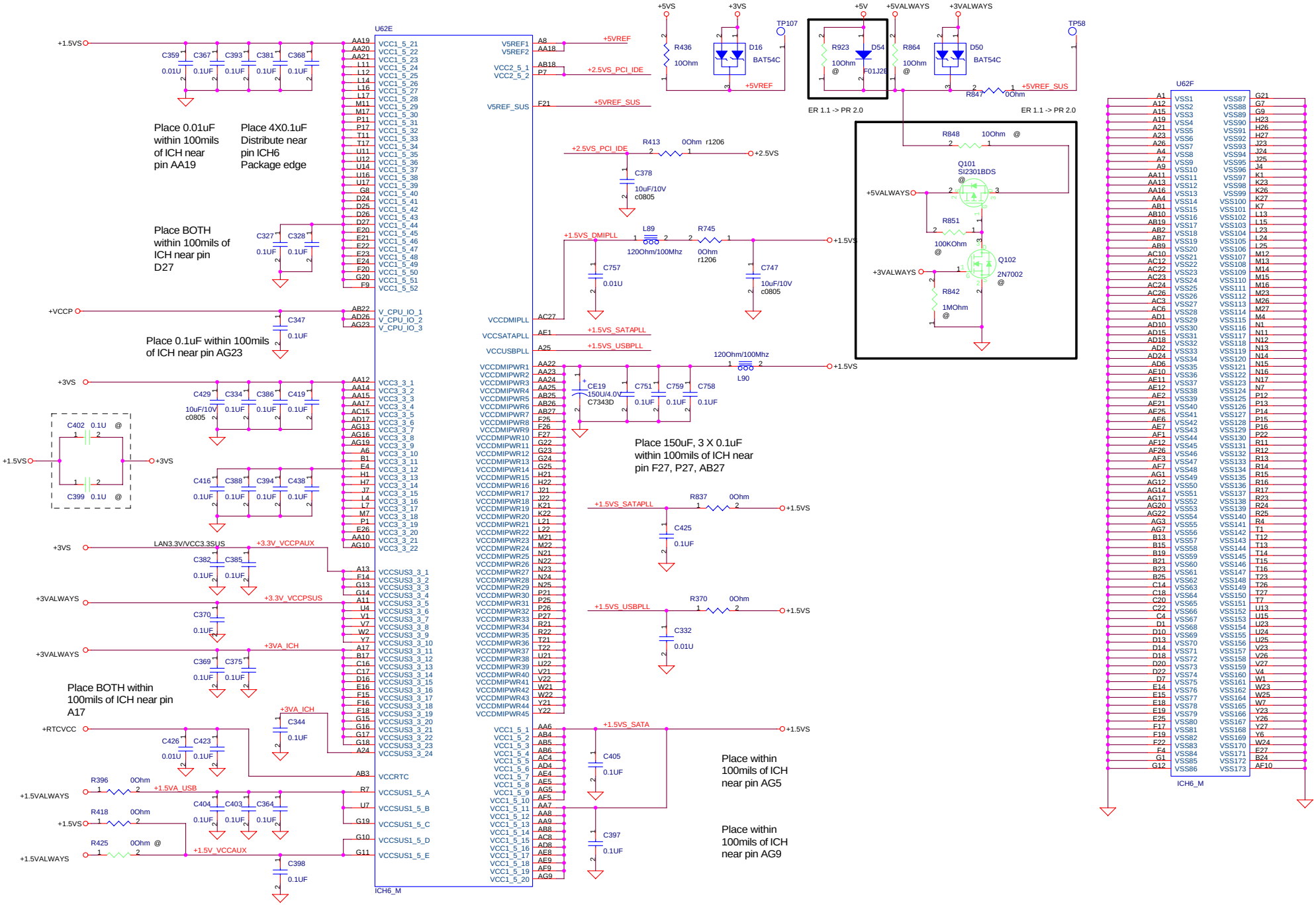
ASUS	**PROJECT: M9V**	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** ICH6M - LPC & IDE (1)	**SCHEMATIC FILE NAME :** <Doc>
			SHEET 26 **OF** 61		**LIBRARY DATE :**

DESIGN ENGINEER :

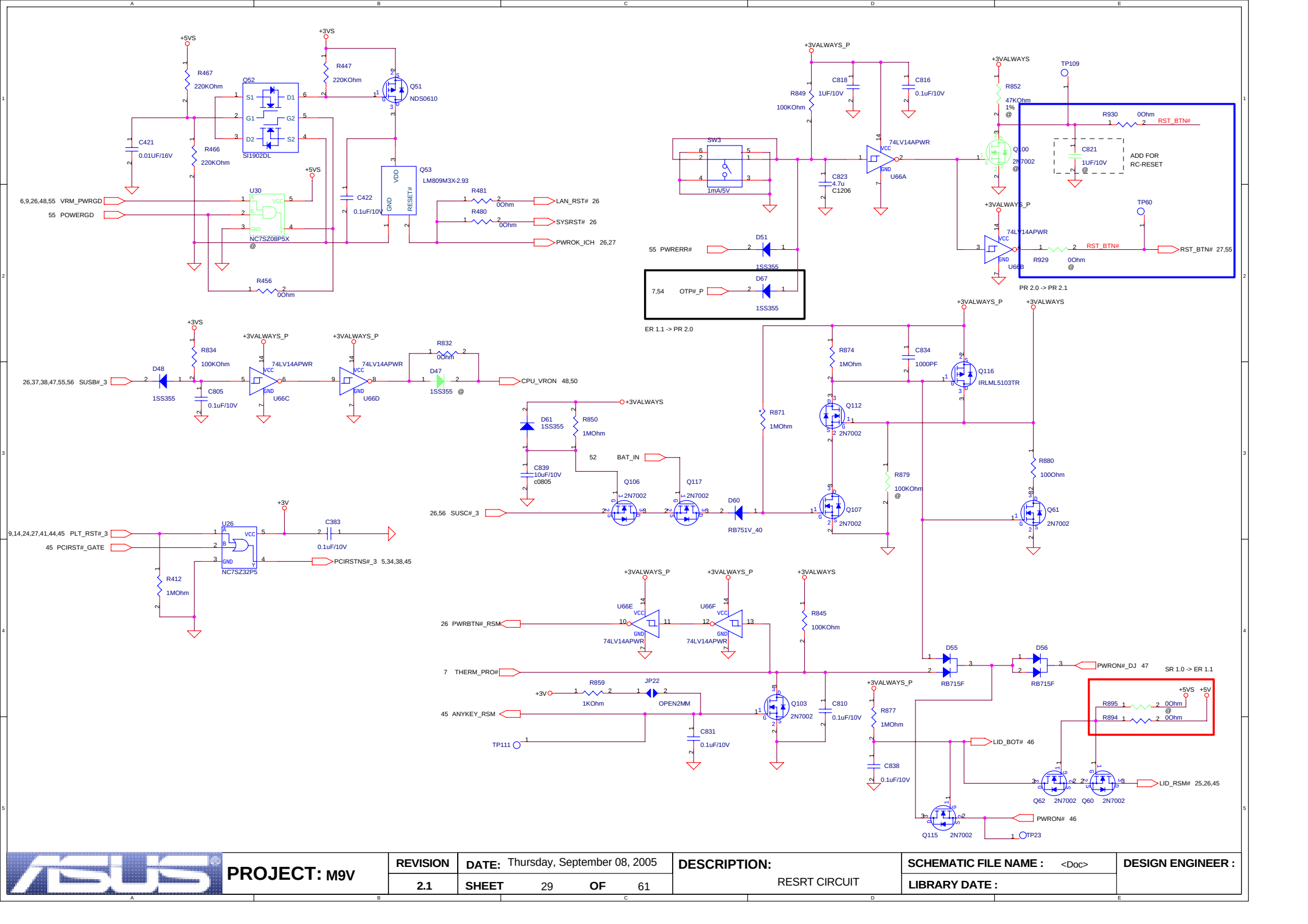


ID2	ID1	ID0	
0	0	0	N/A
0	0	1	Enable Audio DJ in Battery Mode
0	1	0	N/A
0	1	1	N/A
1	0	0	N/A
1	0	1	N/A
1	1	0	N/A
1	1	1	Disable Audio DJ in Battery Mode

PROJECT: M9V	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** ICH6M - USB&PCI-E&PMIO (2)
		SHEET 27 **OF** 61	**SCHEMATIC FILE NAME :** <Doc>
			LIBRARY DATE :
			DESIGN ENGINEER :

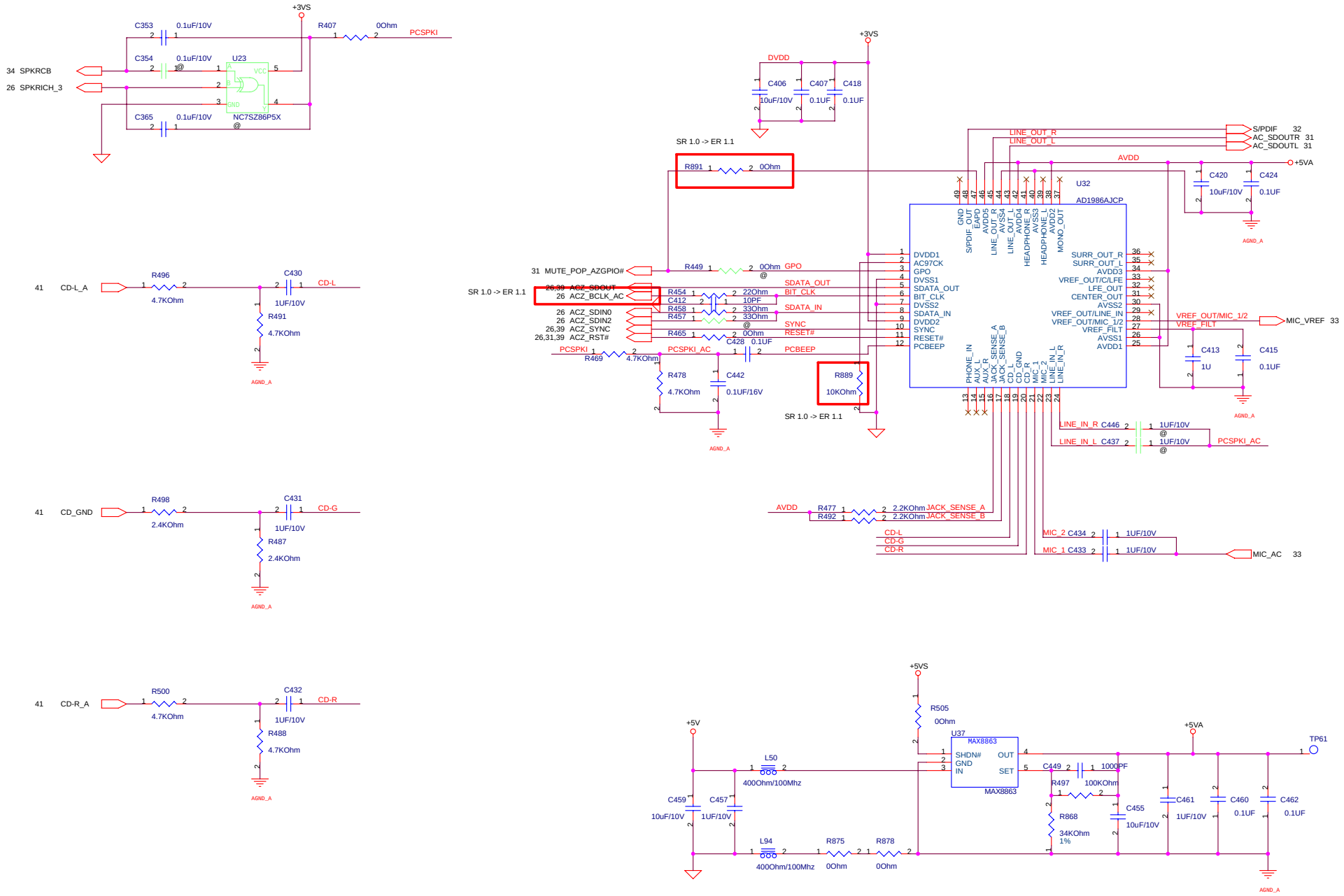


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: ICH6M - PWR & GND (3)	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 28 OF 61		LIBRARY DATE :	

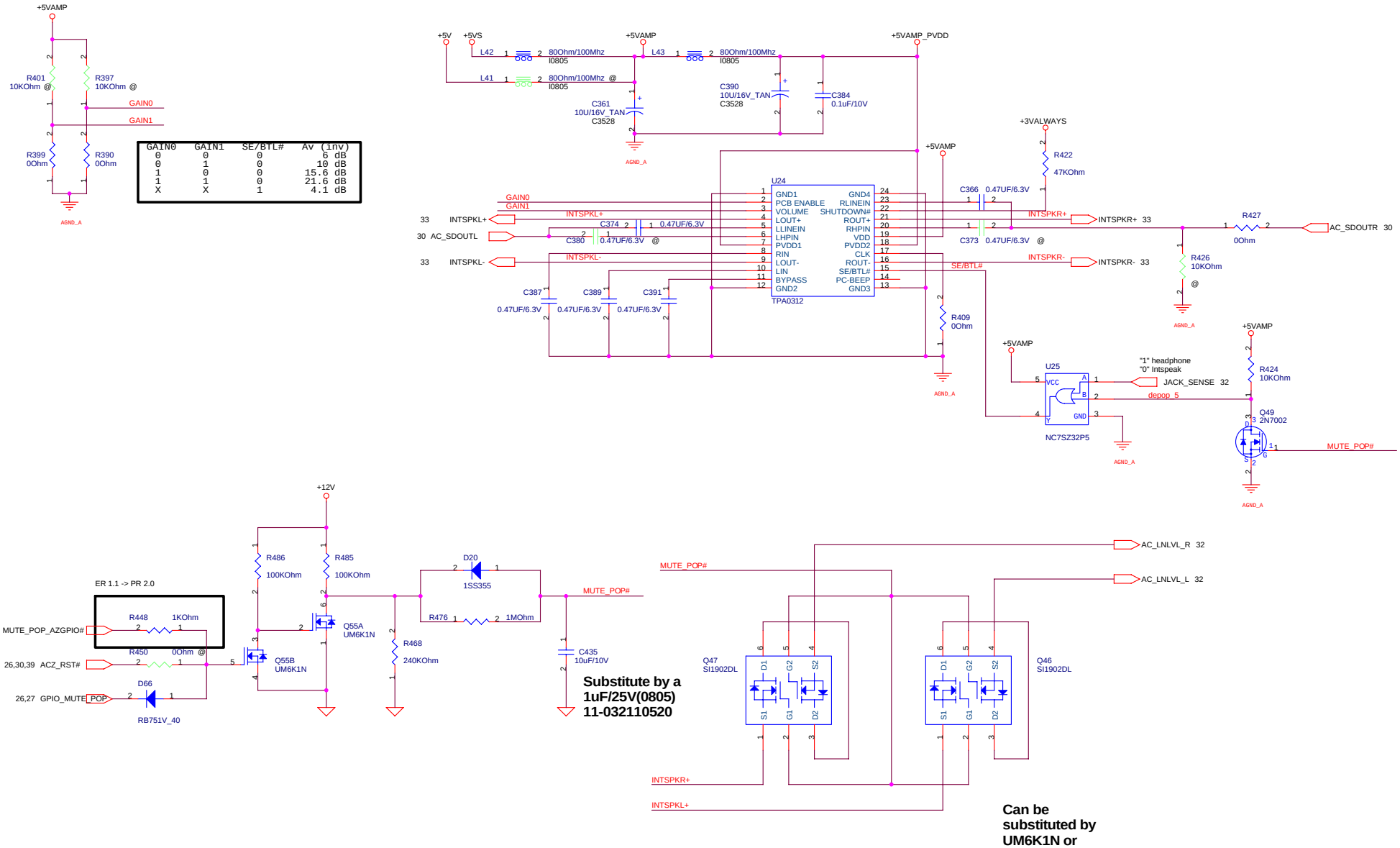


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: RESRT CIRCUIT	SCHEMATIC FILE NAME : <Doc>
		SHEET 29 OF 61		LIBRARY DATE :

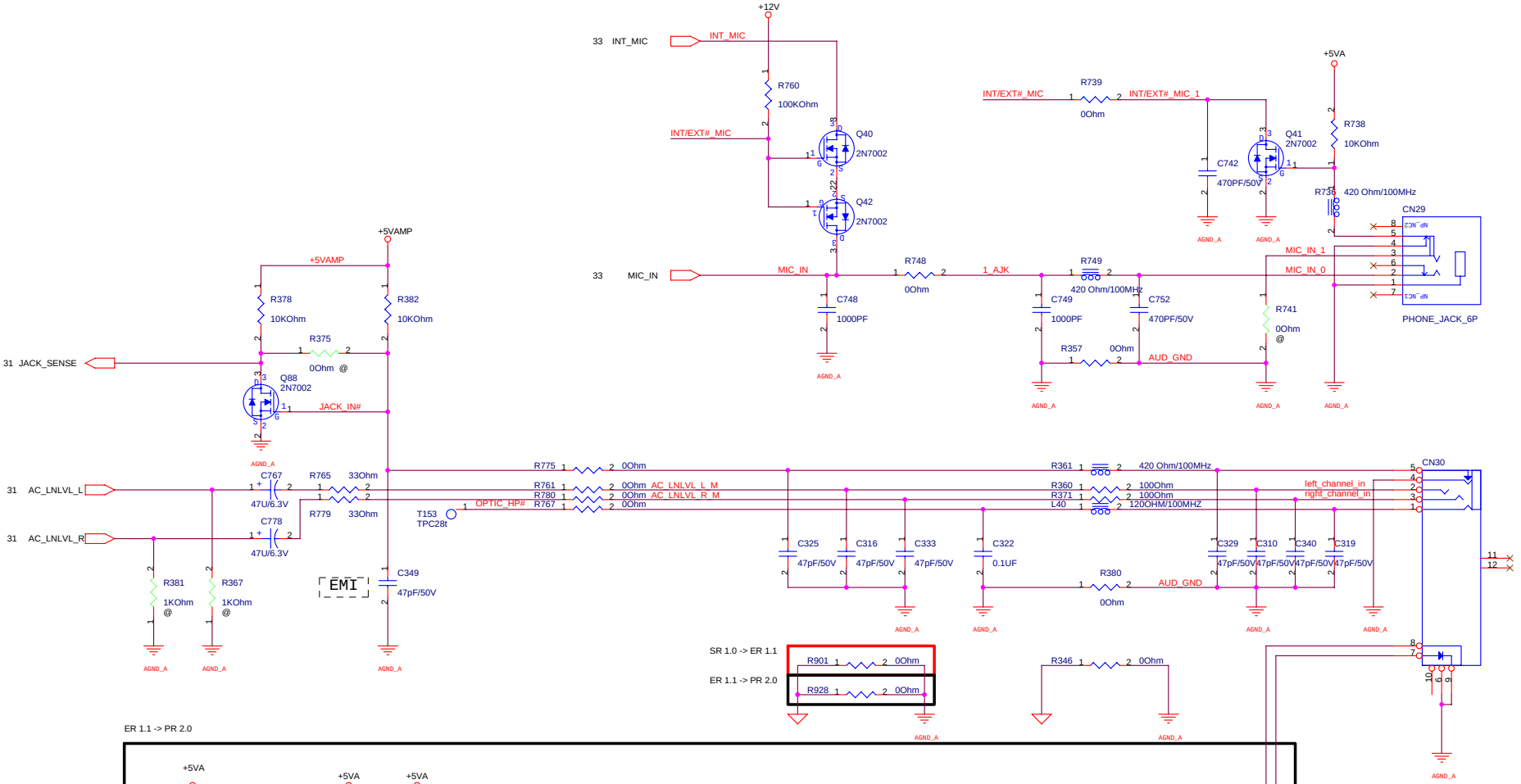
DESIGN ENGINEER :



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: AZALIA AD1986A	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 30 OF 61		LIBRARY DATE :	



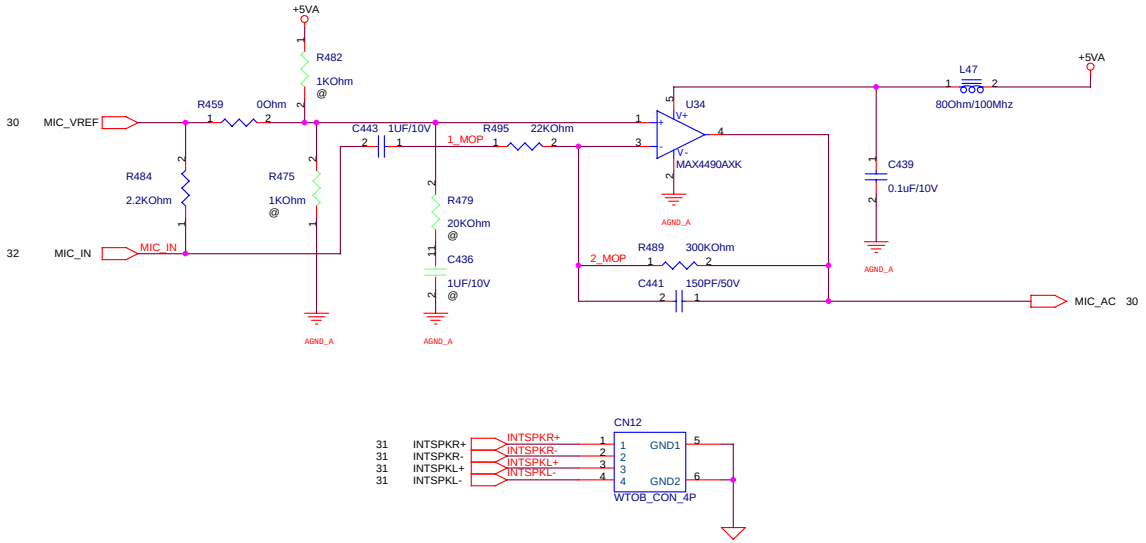
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: AUDIO AMP & INT SPK	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 31 OF 61		LIBRARY DATE :	



JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT

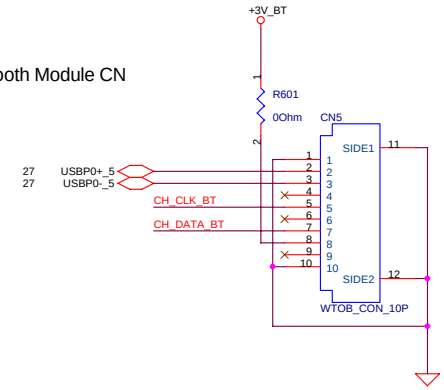
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: PHONE JACK	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 32 OF 61		LIBRARY DATE :	

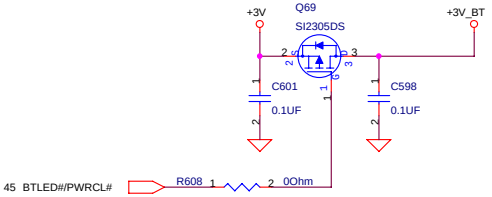
MIC PreAmp & Mic Jack

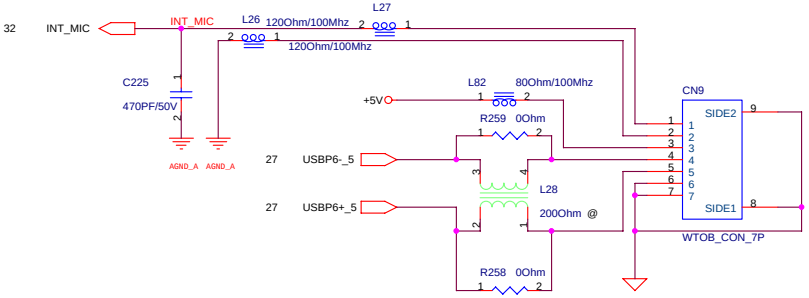


External Modules

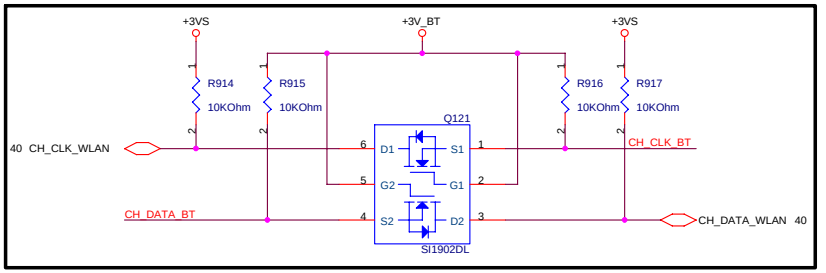
Bluetooth Module CN



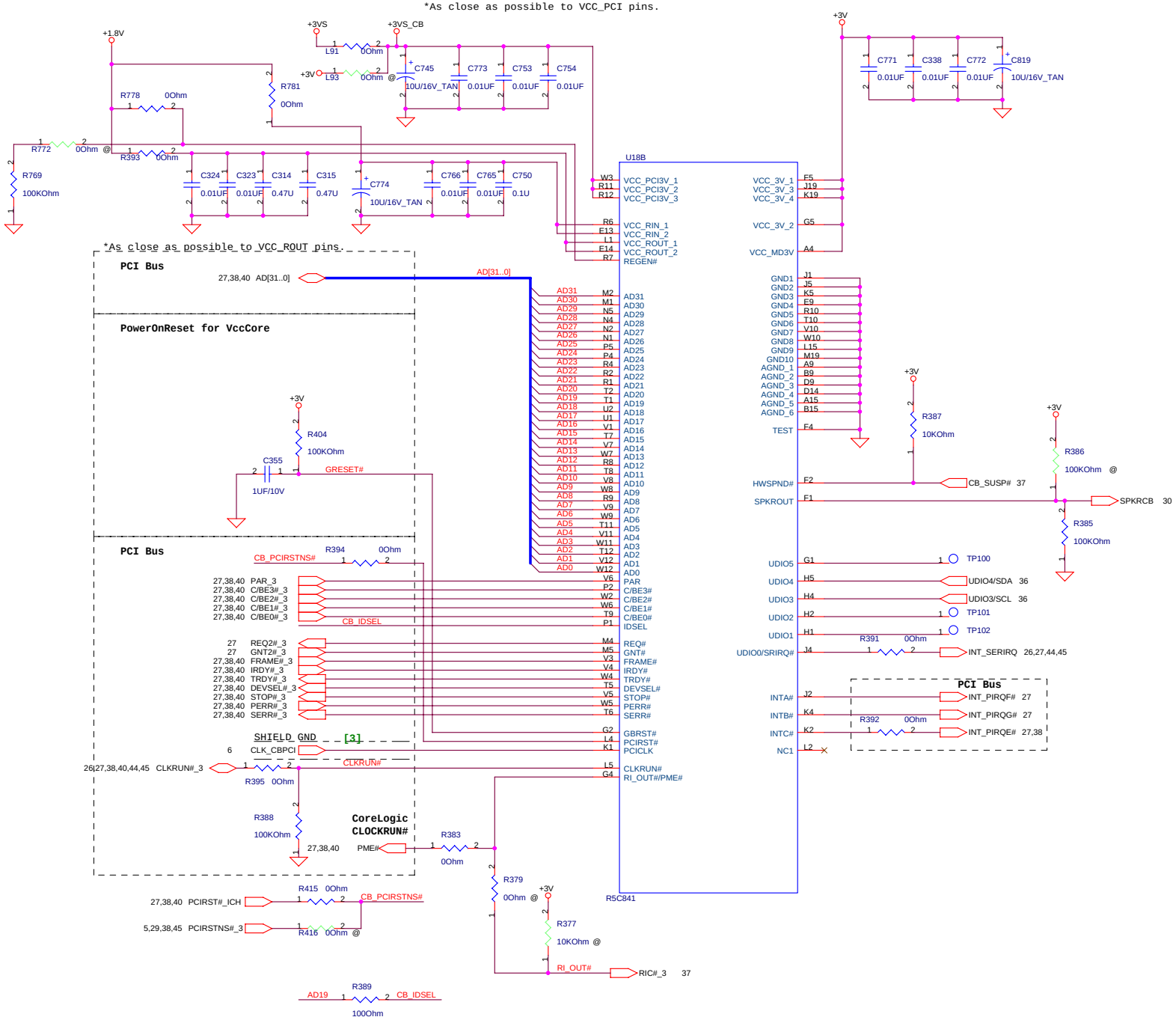




ER1.1 -> PR2.0



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: MIC PRE AMP & MIC JACK & ExtCN	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 33 OF 61		LIBRARY DATE :	



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_B	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 34 OF 61		LIBRARY DATE :	

[1] NOT INSTALLED

[2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.

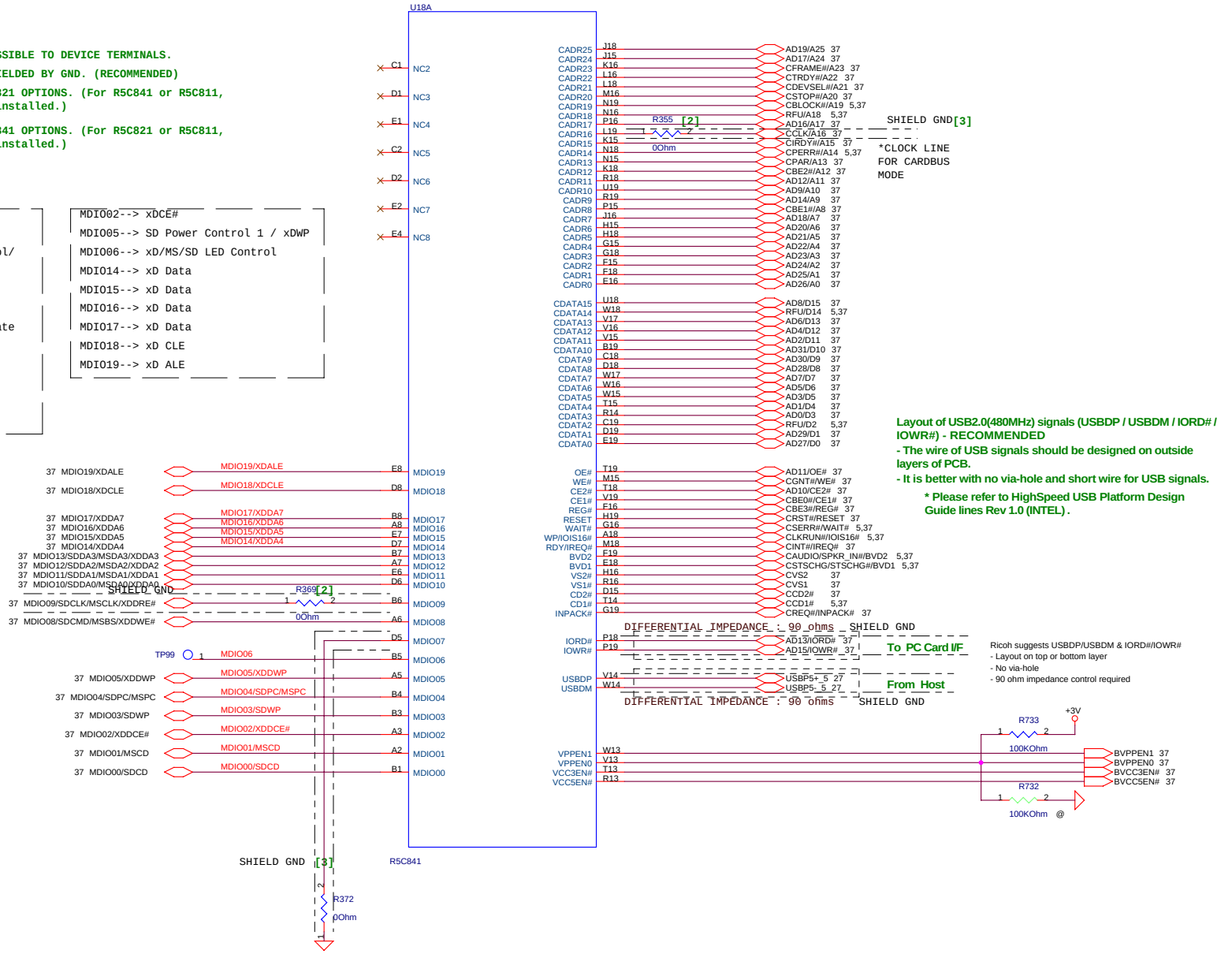
[3] CLK LINES : SHIELDED BY GND. (RECOMMENDED)

[4] R5C851 and R5C821 OPTIONS. (For R5C841 or R5C811, these parts are NOT installed.)

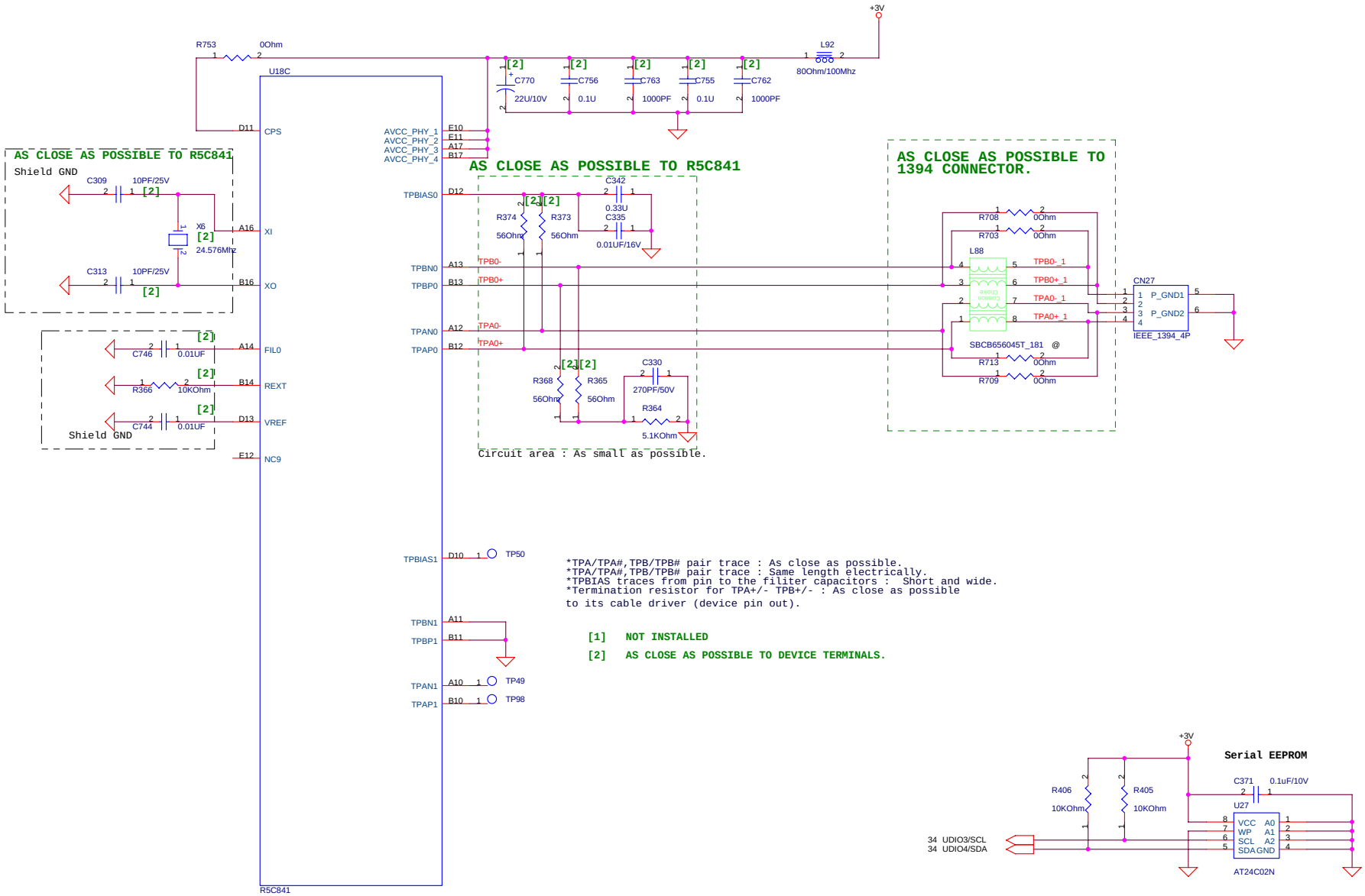
[5] R5C851 and R5C841 OPTIONS. (For R5C821 or R5C811, these parts are NOT installed.)

MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/ MS Power Control
MDIO07--> SD External Clock/ MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

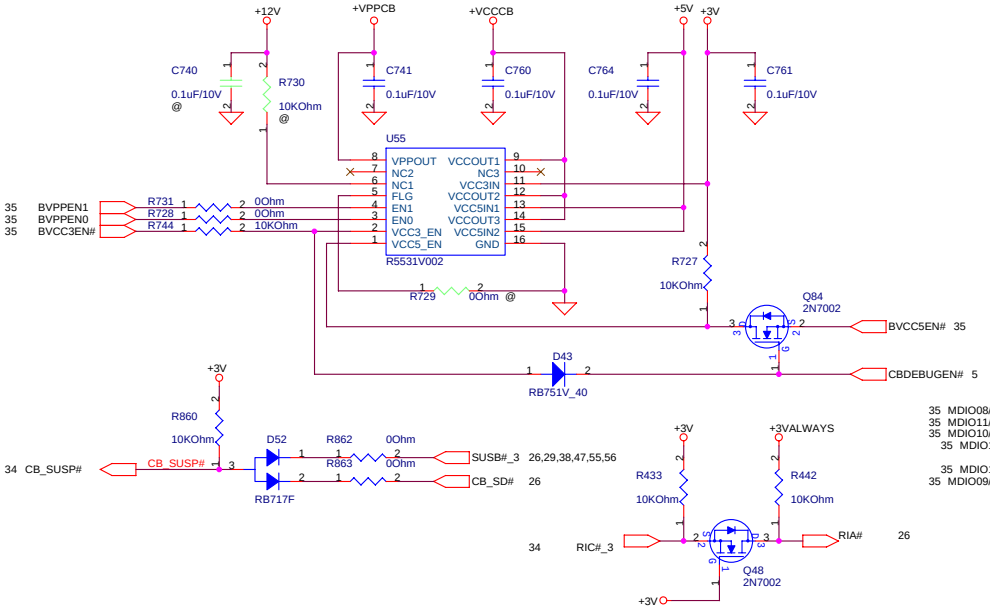


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_A	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 35 OF 61		LIBRARY DATE :	

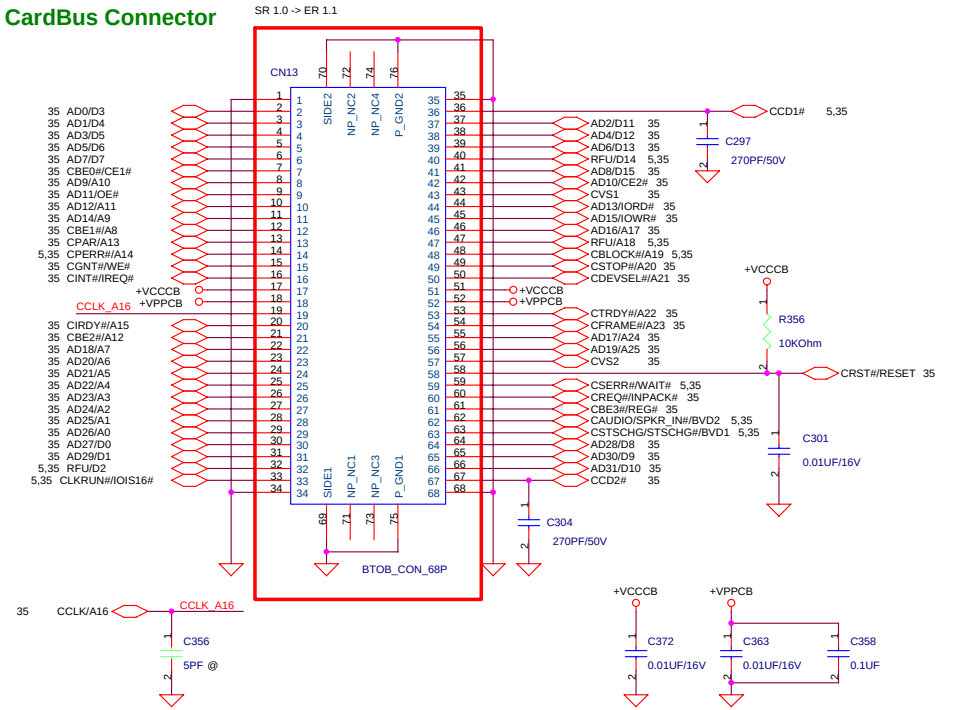


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: CardBus RICOH R5C841/PCI_C	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 36 OF 61		LIBRARY DATE :	

Power Switch



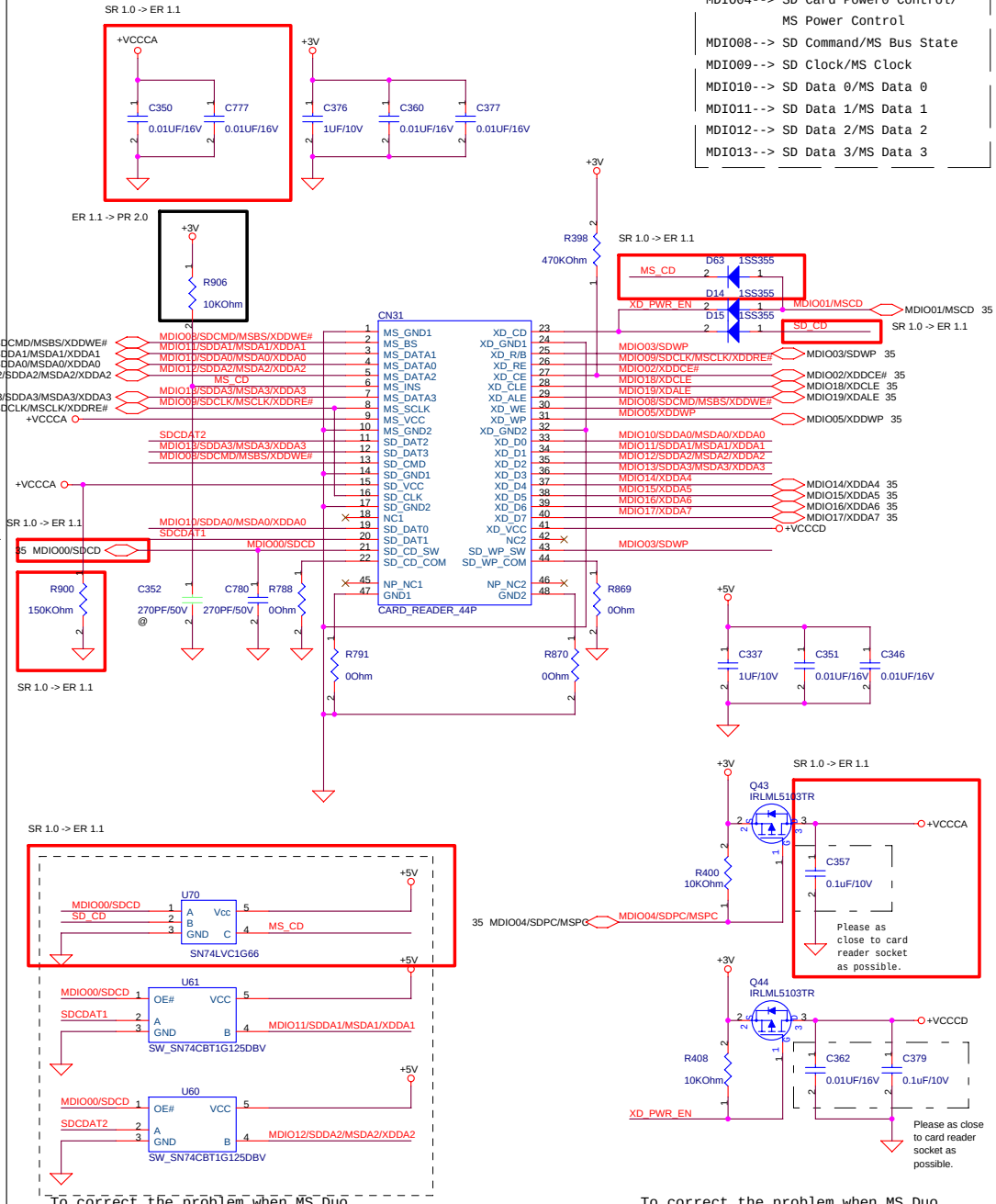
CardBus Connector



SD/MMC/MS/MS-PRO Card Reader Socket

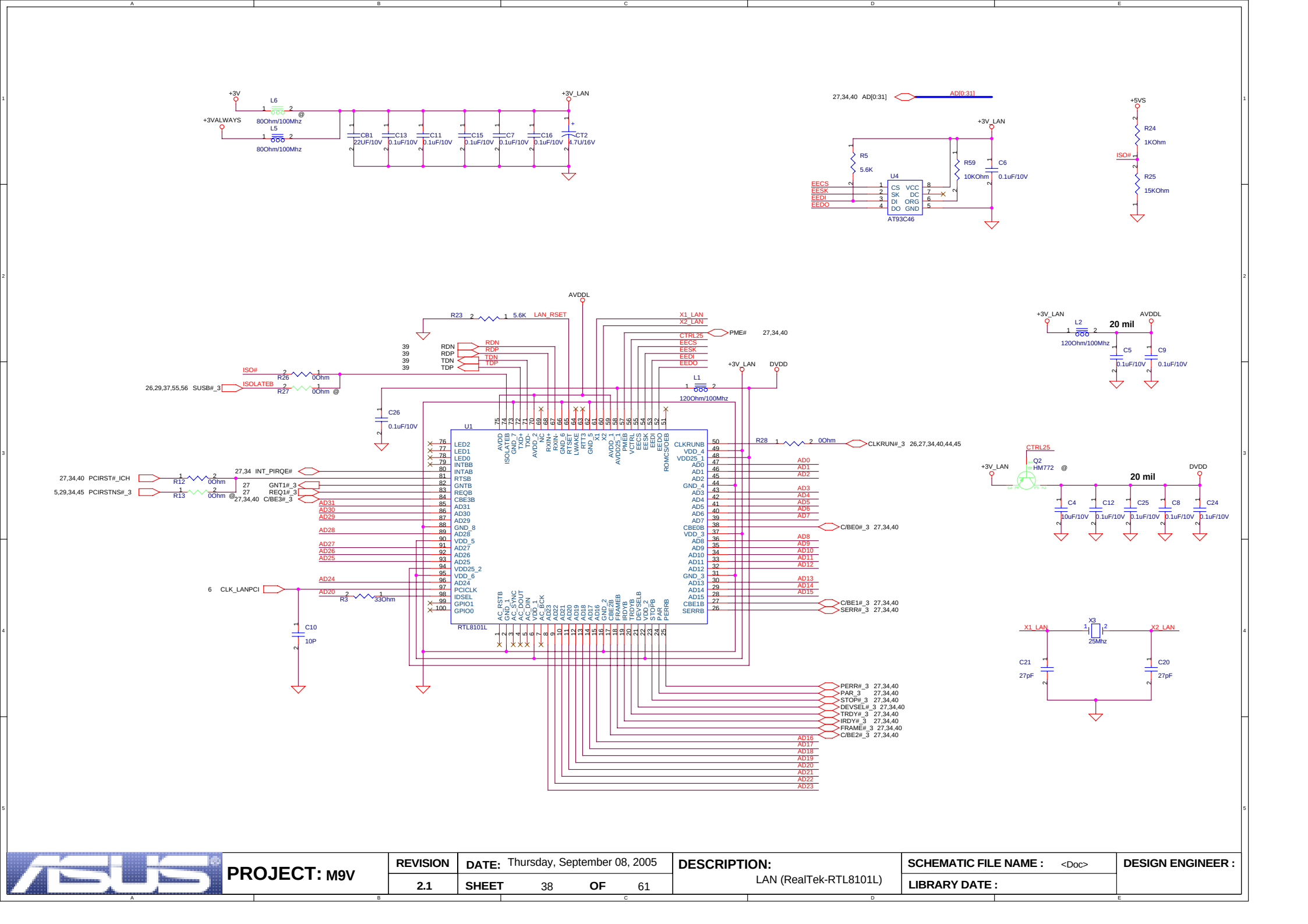
[3] CLK LINE : SHIELDED BY GND. (RECOMMENDED) [5] R5C841 OPTIONS.

```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```



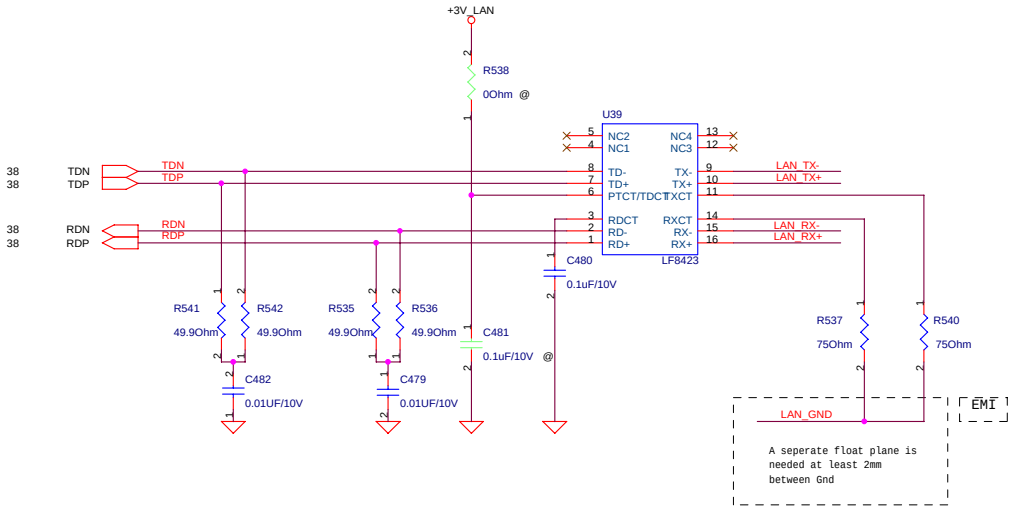
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: Cardbus & CardReader & PwrSw	SCHEMATIC FILE NAME : <Doc>
		SHEET 37 OF 61		LIBRARY DATE :

DESIGN ENGINEER :



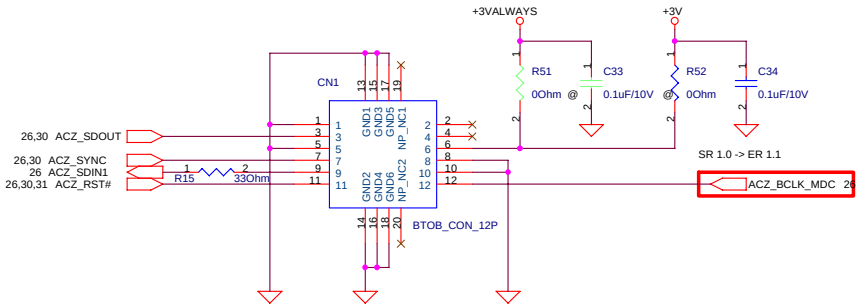
PROJECT: M9V	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** LAN (RealTek-RTL8101L)	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 38 **OF** 61		**LIBRARY DATE :**	

Transformer

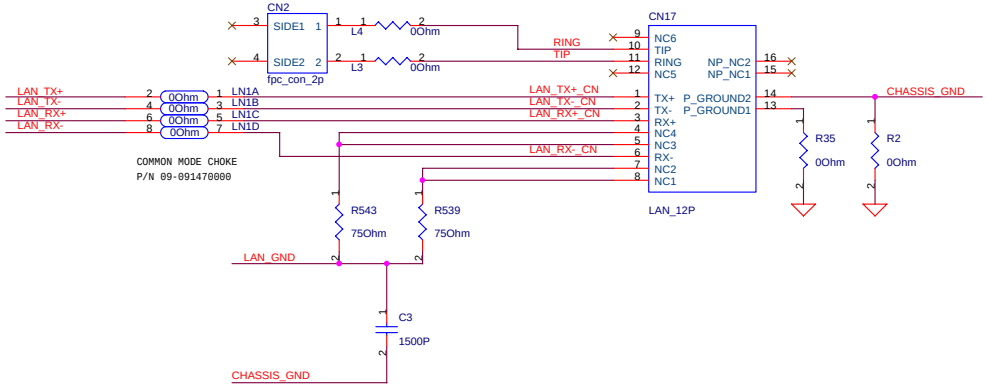


MDC Connector

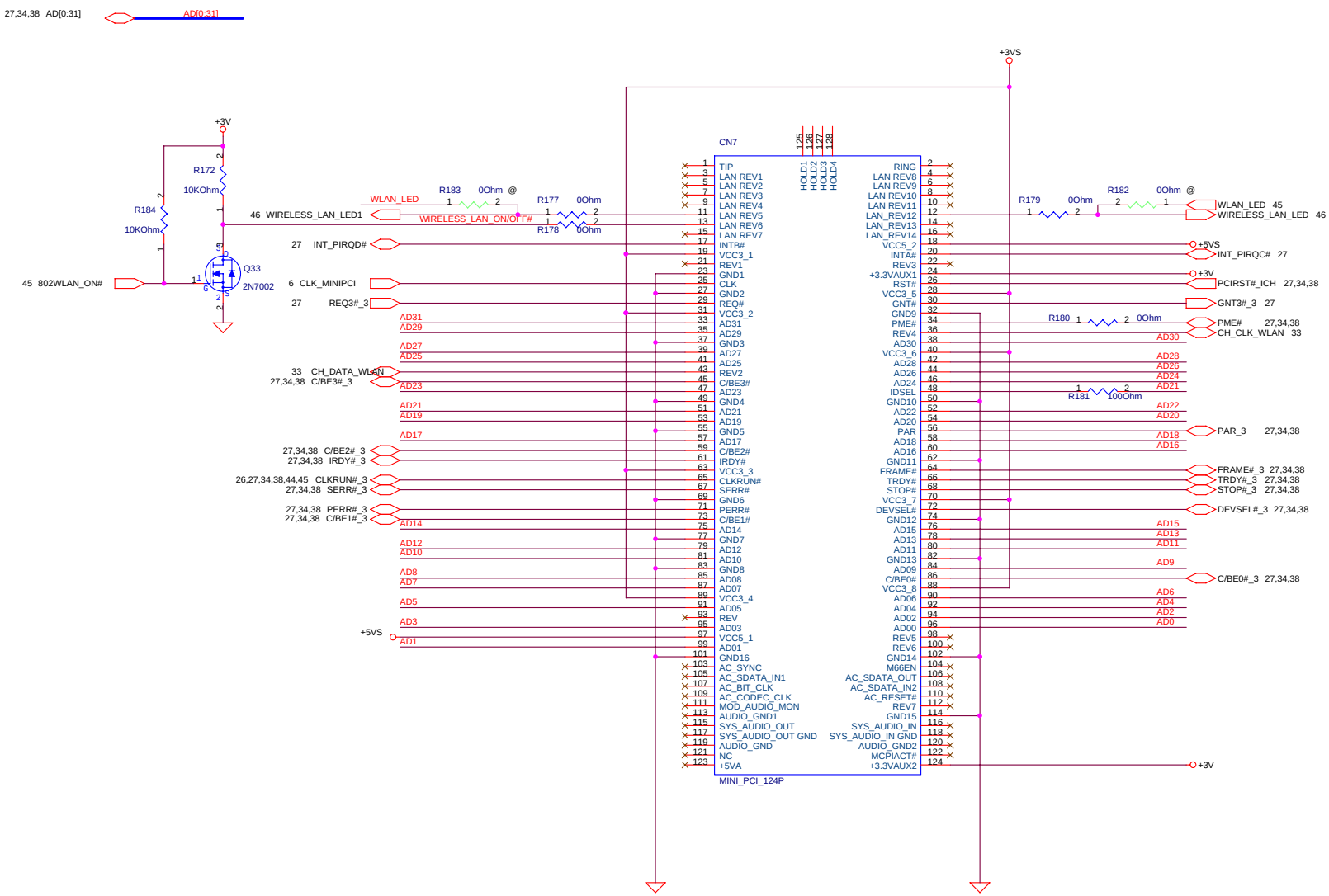
FOR MDC



RJ11/RJ45 Connector

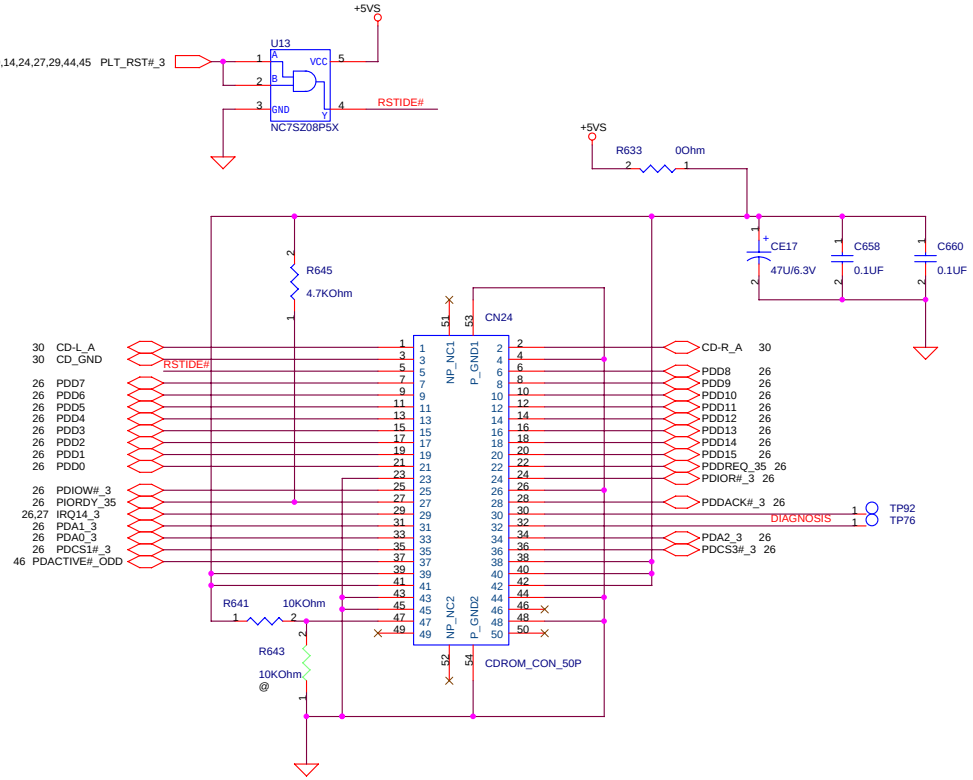


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: LAN IO & MDC	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 39 OF 61		LIBRARY DATE :	

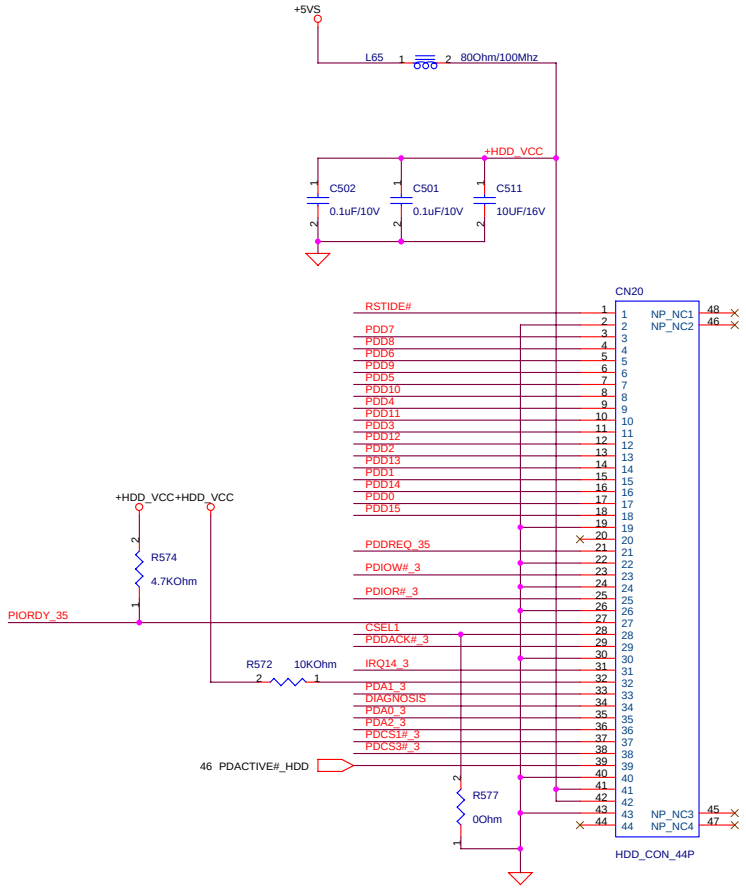


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: MiniPCI	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 40 OF 61		LIBRARY DATE :	

ODD Connector

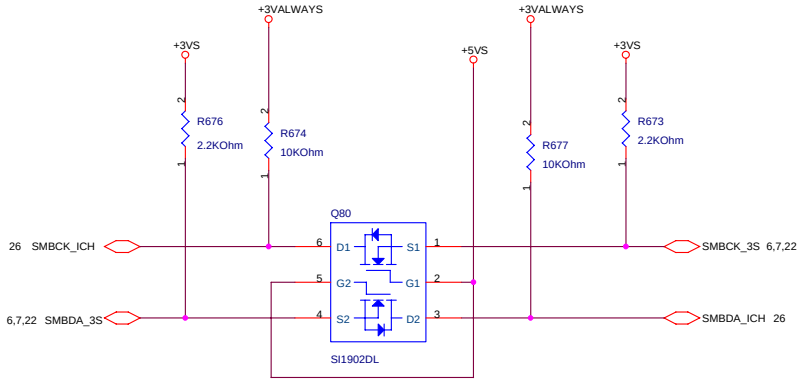


HDD Connector

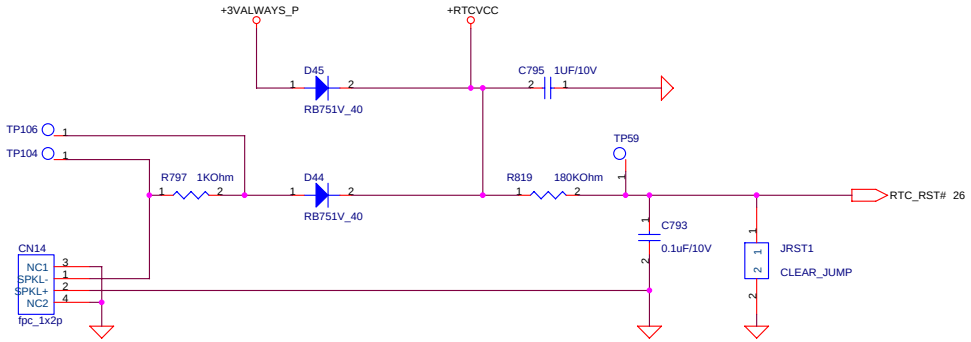


PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: HDD & CDROM CN	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 41 OF 61		LIBRARY DATE :	

SM BUS



RTC Connector



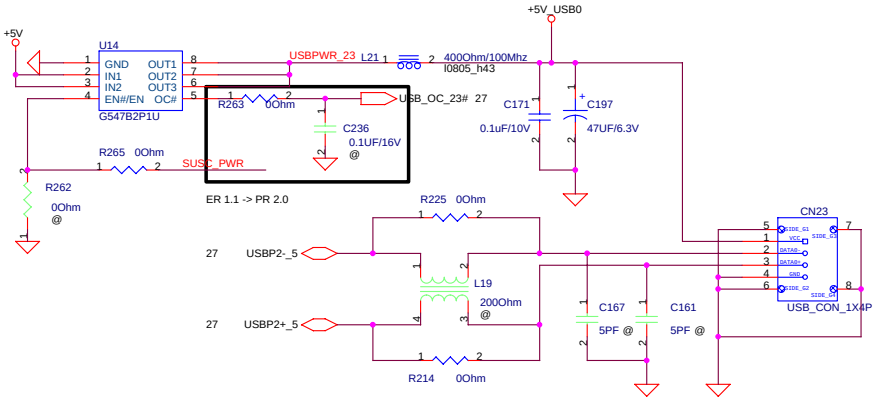
+V1.8S_PROC_VCCA3 — +V1.8S_PROC_VCCA3 3
+V1.8S_PROC_VCCA2 — +V1.8S_PROC_VCCA2 3
+V1.8S_PROC_VCCA1 — +V1.8S_PROC_VCCA1 3
+V1.8S_PROC — +V1.8S_PROC 3
+VCCP — +VCCP 3,4,5,6,8,9,11,12,26,28,50
+1.8VS — +1.8VS 3,14,15,16,56,57
+1.5VS — +1.5VS 3,9,11,16,27,28,50
+VCORE — +VCORE 4,5,7,48
+3V — +3V 5,7,29,33,34,35,36,37,38,39,40,43,44,45,46,47,51,56
+5V — +5V 5,9,28,29,30,31,33,37,43,45,46,47,56,57
+3VALWAYS — +3VALWAYS 5,24,26,27,28,29,31,37,38,39,45,47,51
+3VS — +3VS 6,7,11,14,15,16,17,22,24,25,26,27,28,29,30,33,34,40,43,44,45,47,48,51,56,57
+3VS_CLK — +3VS_CLK 6
+5VS — +5VS 7,9,24,28,29,30,31,38,40,41,43,45,46,47,56
+12V — +12V 7,31,32,37,49,56
+2.5VS — +2.5VS 9,11,13,16,28,50,57
+1.8V — +1.8V 9,11,12,20,21,22,34,50,51
+2.5VS_SYNC — +2.5VS_SYNC 9,11,13,16,28,50,57
+2.5VS_CRTDAC — +2.5VS_CRTDAC 11
+1.5VS_MPLL — +1.5VS_MPLL 11
+VCCP_GMCH — +VCCP_GMCH 3,4,5,6,8,9,11,12,26,28,50
+2.5VS_3GBG — +2.5VS_3GBG 11
+1.5VS_3GPLL — +1.5VS_3GPLL 11
+1.5VS_DDRDLL — +1.5VS_DDRDLL 11
+1.5VS_DLVDS — +1.5VS_DLVDS 3,9,11,16,27,28,50
+2.5VS_ALVDS — +2.5VS_ALVDS 9,11,13,16,28,50,57
+2.5VS_HV — +2.5VS_HV 9,11,13,16,28,50,57
+1.5VS_TVDAC — +1.5VS_TVDAC 3,9,11,16,27,28,50
+1.5VS_QTVDAC — +1.5VS_QTVDAC 11
+3VS_TVDACA — +3VS_TVDACA 11
+3VS_TVDACB — +3VS_TVDACB 11
+3VS_TVDACC — +3VS_TVDACC 11
+3VS_TVBG — +3VS_TVBG 11
+1.5VS_HPLL — +1.5VS_HPLL 11
+1.5VS_DPLLB — +1.5VS_DPLLB 11
+1.5VS_DPLLA — +1.5VS_DPLLA 11
+1.5VS_HMPLL — +1.5VS_HMPLL 11
+VCC_GMCH_CORE — +VCC_GMCH_CORE 11,12,50,51
+VCC_GMCH — +VCC_GMCH 11,12,50,51
SM_VREF_DDR — SM_VREF_DDR 9,20,21,22
M_VREF_DIMM1 — M_VREF_DIMM1 9,20,21,22
+0.9VS — +0.9VS 23,51
+12VS — +12VS 24,25,56
LCD_+3VS — LCD_+3VS 25
LCD_VCC — LCD_VCC 25
AC_BAT_SYS — AC_BAT_SYS 25,48,49,50,51,52,53,57
+RTCVCC — +RTCVCC 26,28
+1.5VALWAYS — +1.5VALWAYS 28,51
+5VALWAYS — +5VALWAYS 28,50
+3VALWAYS_P — +3VALWAYS_P 29,46,47,51
+5VA — +5VA 30,32,33
+5VAMP — +5VAMP 31,32
+5VAMP_PVDD — +5VAMP_PVDD 31
+3V_BT — +3V_BT 33
+3VS_CB — +3VS_CB 34
+VCCCA — +VCCCA 37
+VCCCD — +VCCCD 37
+VCCCB — +VCCCB 37
+VPPCB — +VPPCB 37

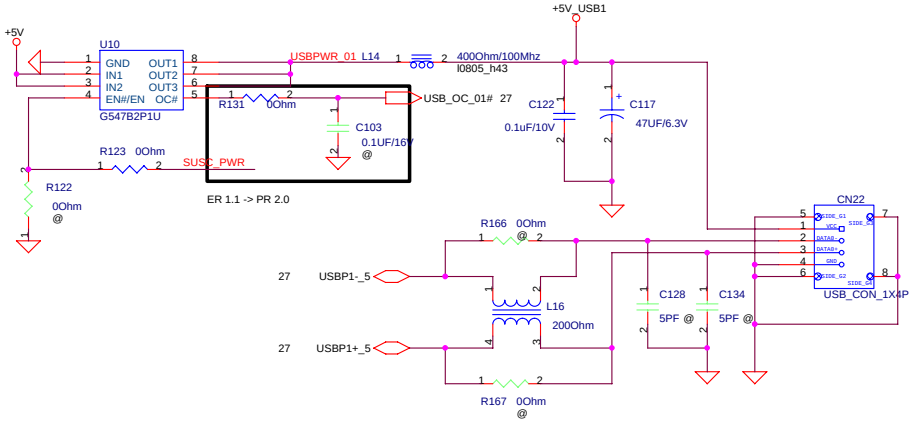
+5VS_FAN1 — +5VS_FAN1 7
+3V_LAN — +3V_LAN 38,39
AVDDL — AVDDL 38
DVDD — DVDD 38
+HDD_VCC — +HDD_VCC 41
+5V_USB0 — +5V_USB0 43
+5V_USB1 — +5V_USB1 43
+5V_USB2 — +5V_USB2 43
+5V_USB3 — +5V_USB3 43
A/D_DOCK_IN — A/D_DOCK_IN 44,52,53
+5VLCM — +5VLCM 45,46,52,55
+1.2VSP — +1.2VSP 14,16,57
+ATI_MEM — +ATI_MEM 15,16,18,19,56
LVDDR — LVDDR 16,57
+ATI_VCORE — +ATI_VCORE 16,57

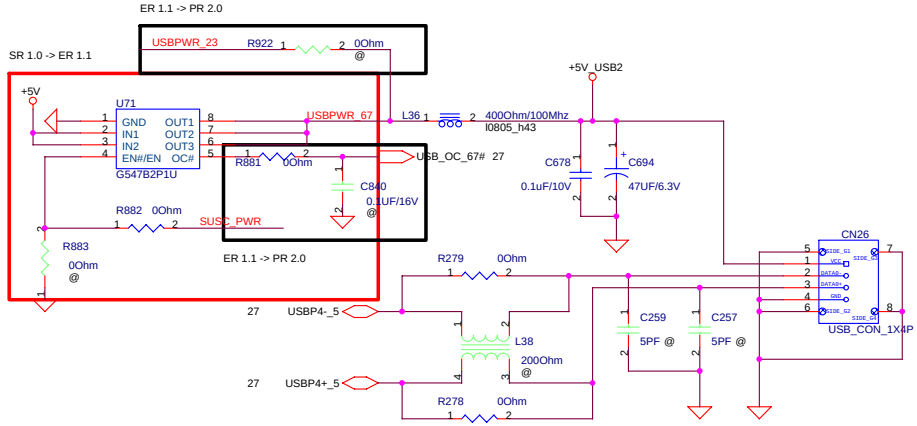
POWER

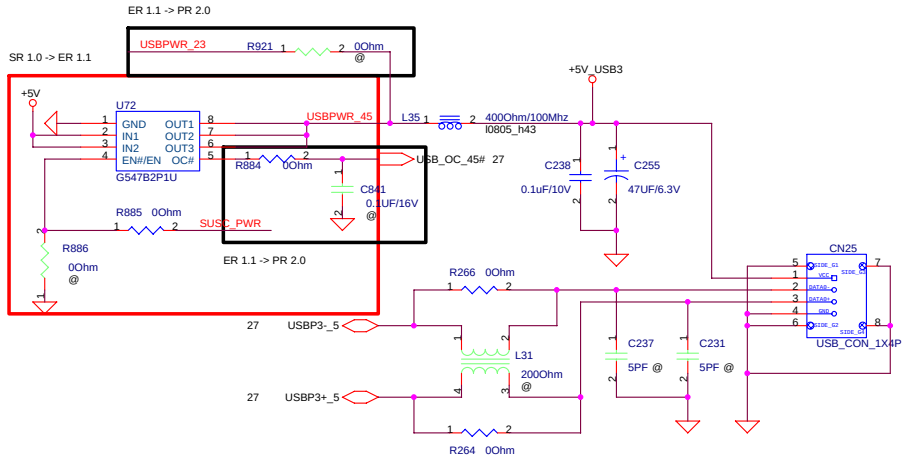
+3VO — +3VO 48,49,50,56
+5VO — +5VO 48,49,50,52,56
+3VAO — +3VAO 49,51,55,56
+5VAO — +5VAO 49
+12VO — +12VO 7,31,32,37,49,56
VREF5 — VREF5 50,54,56
+2.5VO — +2.5VO 50
+1.8VO — +1.8VO 50,56
+1.5VO — +1.5VO 50
+1.05VO — +1.05VO 50
+1.5VAO — +1.5VAO 51
A/D_VIN — A/D_VIN 52,53
A/D_VIN_O — A/D_VIN_O 52,53
BAT — BAT 52,53,54
+5VCHG — +5VCHG 52,53
+2.5VREF — +2.5VREF 52
BAT_S — BAT_S 52,54
MAX1909_LDO — MAX1909_LDO 53

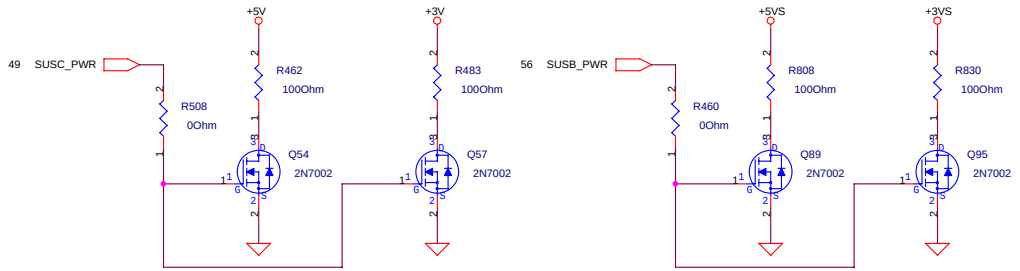
PROJECT: M9V	REVISION 2.0	DATE: Thursday, September 08, 2005	DESCRIPTION: SM_BUS & RTC CN
		SHEET 42 OF 61	SCHEMATIC FILE NAME : <Doc>
			LIBRARY DATE :
			DESIGN ENGINEER :







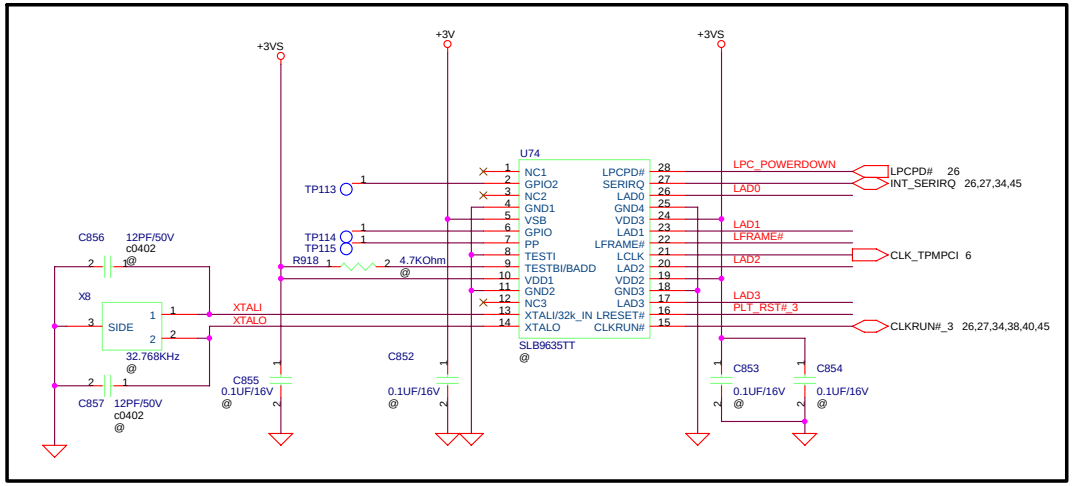




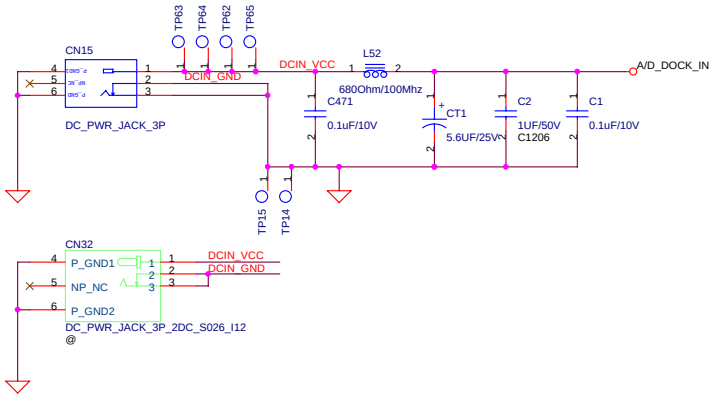
PROJECT: M9V	**REVISION** 2.1	**DATE:** Thursday, September 08, 2005	**DESCRIPTION:** 4*USB2.0 CN	**SCHEMATIC FILE NAME :** <Doc>	**DESIGN ENGINEER :**
		SHEET 43 **OF** 61		**LIBRARY DATE :**	

TPM 1.2 Infieon

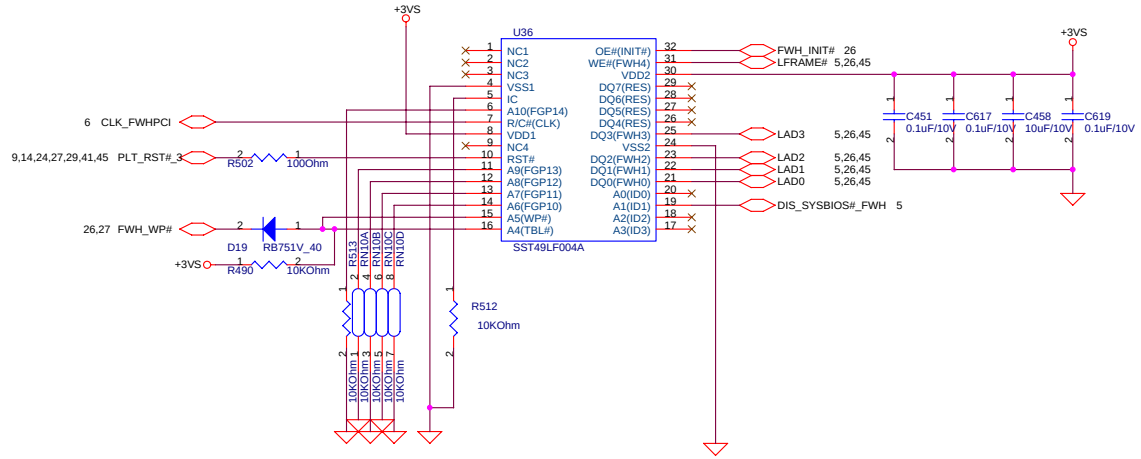
ER 1.1 -> PR 2.0



DCIN JACK

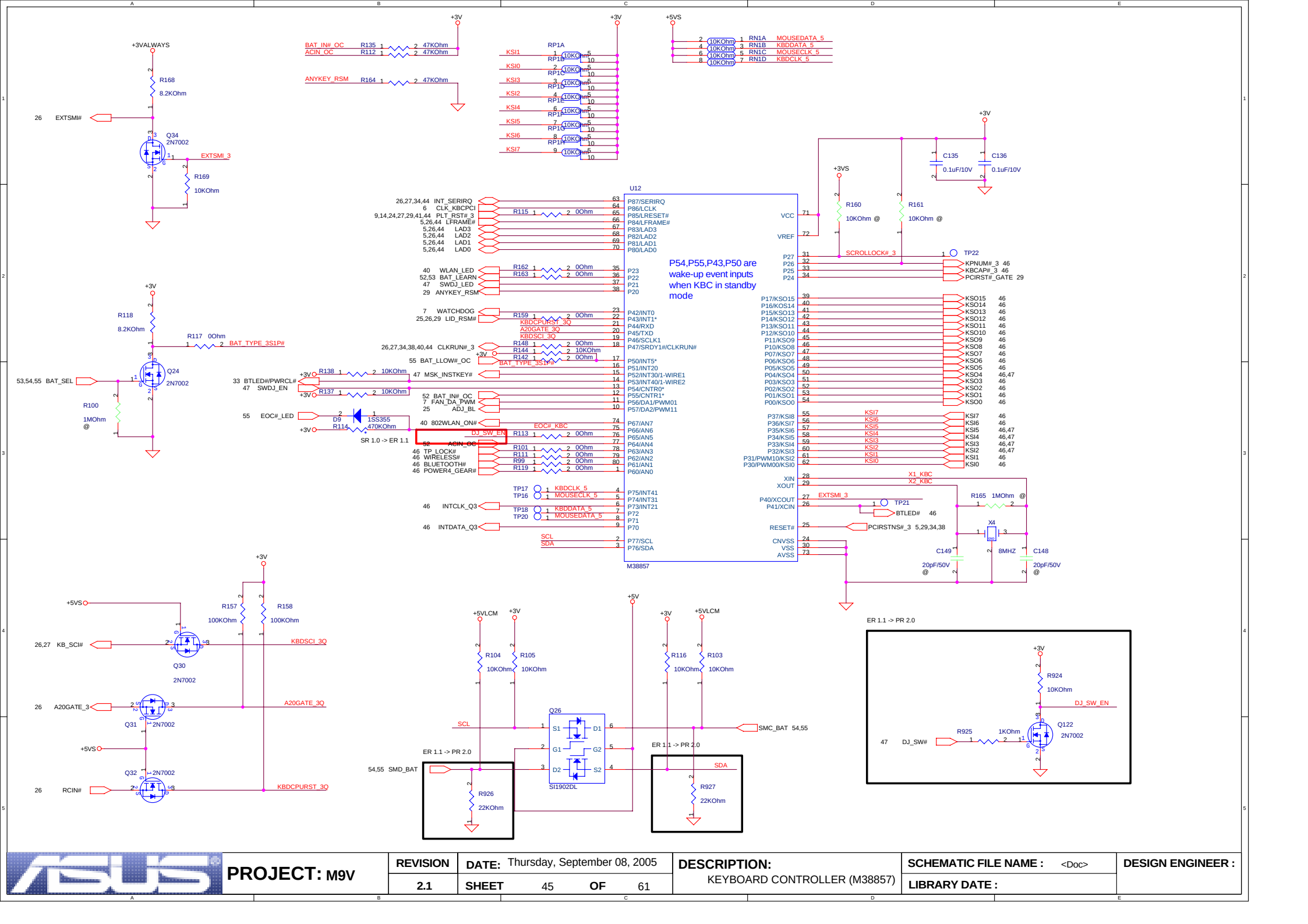


FWH



PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: DCIN Jack & FWH	SCHEMATIC FILE NAME : <Doc>
		SHEET 44 OF 61		LIBRARY DATE :

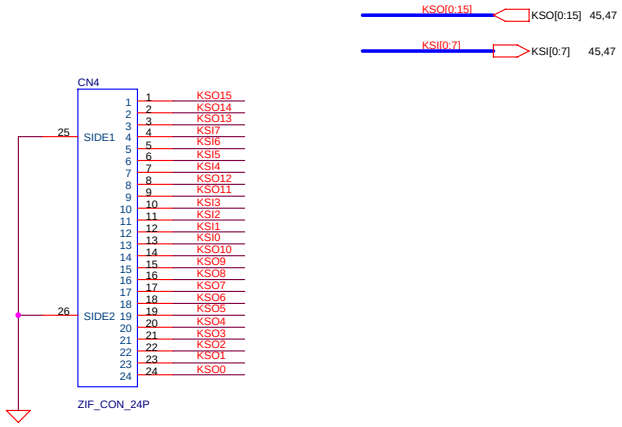
DESIGN ENGINEER :



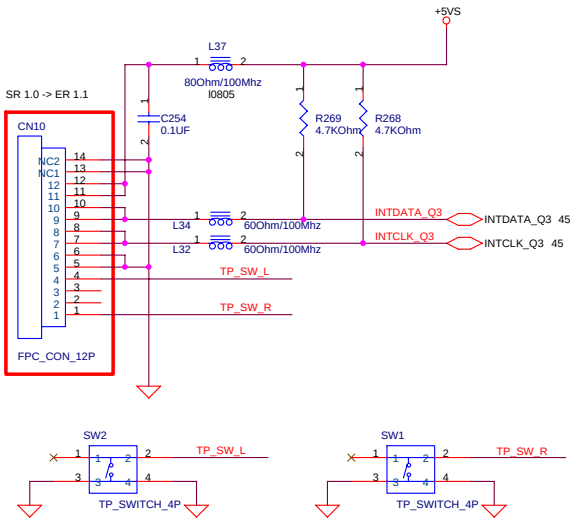
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: KEYBOARD CONTROLLER (M38857)	SCHEMATIC FILE NAME : <Doc>
		SHEET 45 OF 61		LIBRARY DATE :

DESIGN ENGINEER :

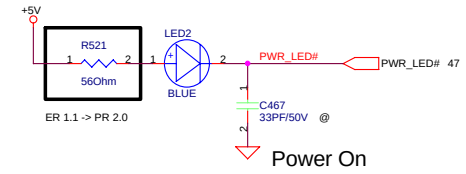
Internal Keyboard



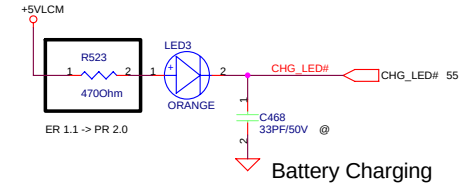
TP



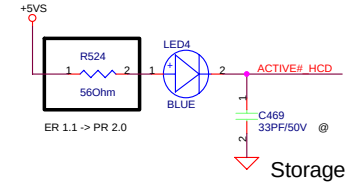
LEDs



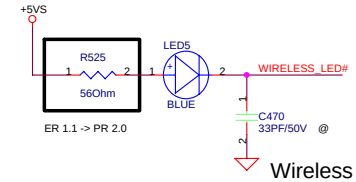
Power On



Battery Charging

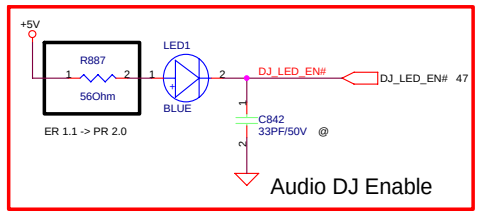


Storage Access

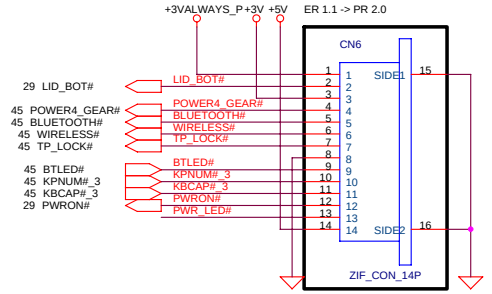


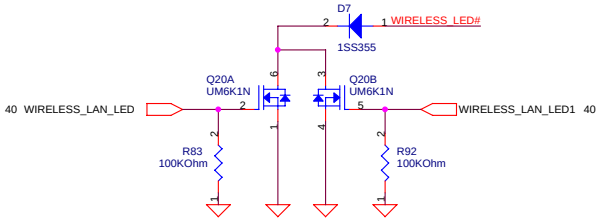
Wireless Enabling

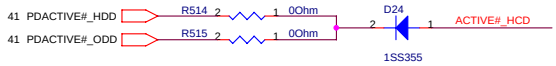
SR 1.0 -> ER 1.1



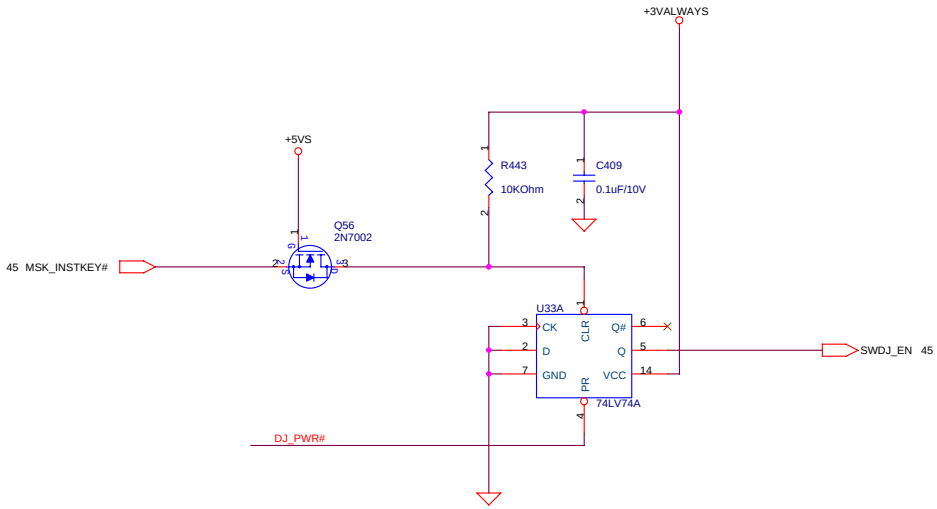
Audio DJ Enable

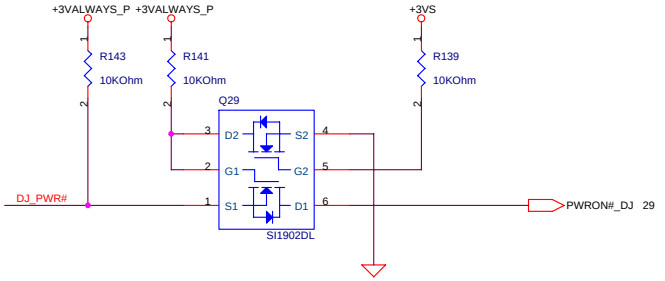


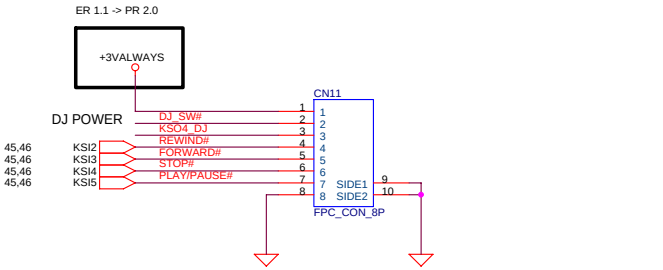


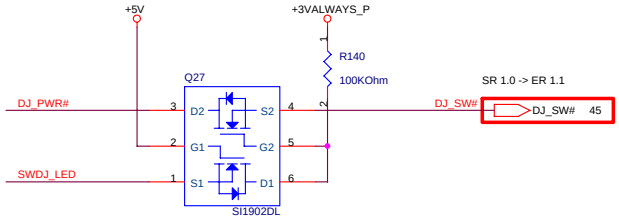


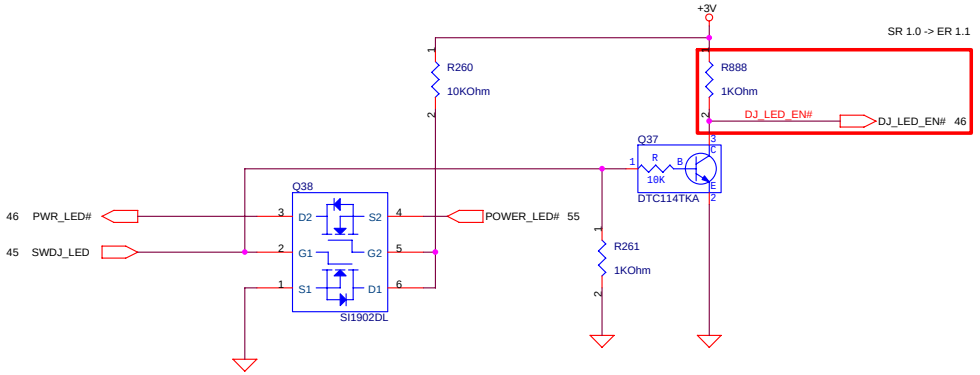
PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: LEDs & Internal KB TP	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 46 OF 61		LIBRARY DATE :	



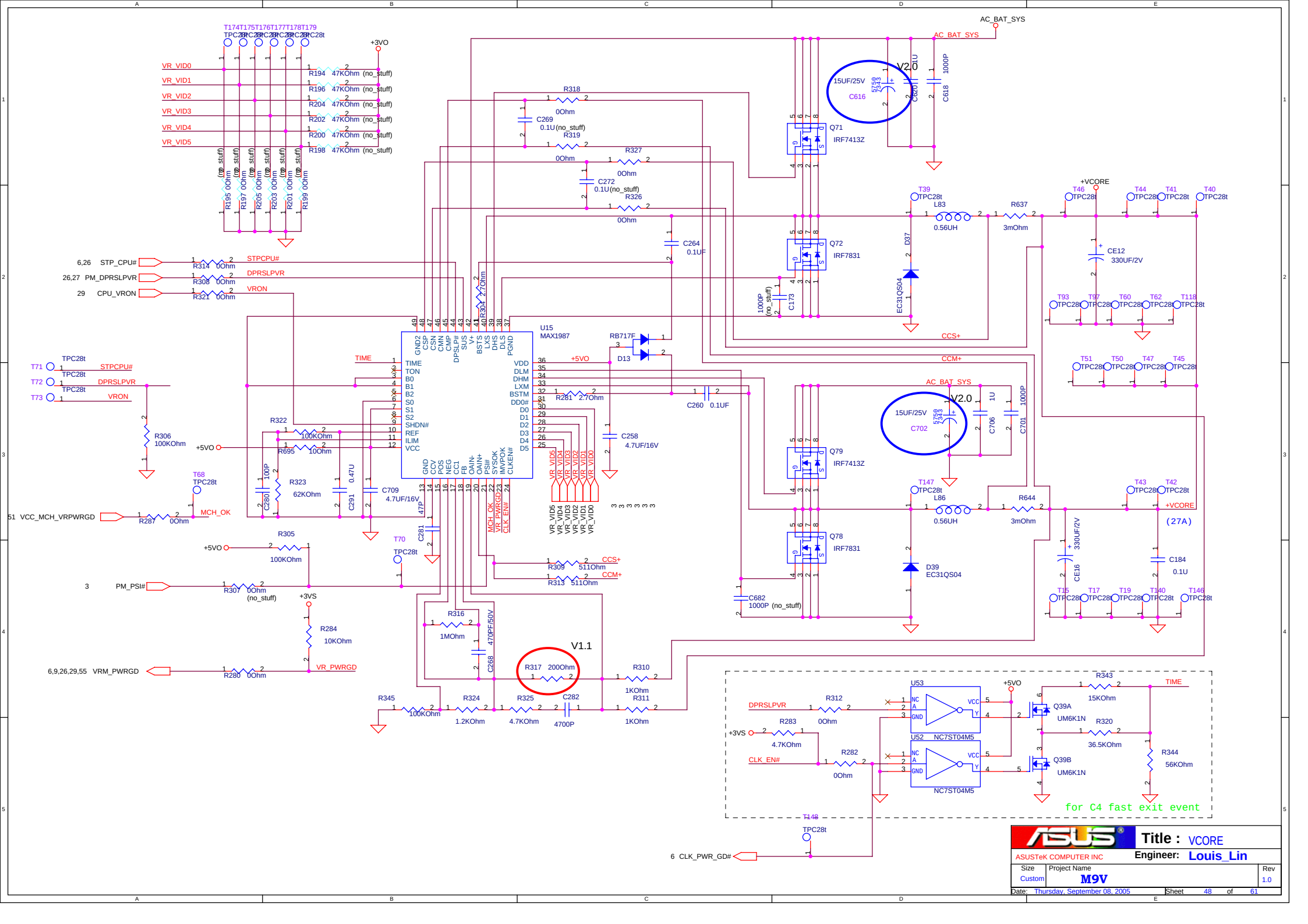








PROJECT: M9V	REVISION 2.1	DATE: Thursday, September 08, 2005	DESCRIPTION: AUDIO DJ	SCHEMATIC FILE NAME : <Doc>	DESIGN ENGINEER :
		SHEET 47 OF 61		LIBRARY DATE :	


AC_BAT_SYS
+3VO
+5VO
+3VS
+VCORE
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
R194 47KOhm (no_stuff)
R196 47KOhm (no_stuff)
R204 47KOhm (no_stuff)
R202 47KOhm (no_stuff)
R200 47KOhm (no_stuff)
R198 47KOhm (no_stuff)
R195 0Ohm (no_stuff)
R197 0Ohm (no_stuff)
R205 0Ohm (no_stuff)
R203 0Ohm (no_stuff)
R201 0Ohm (no_stuff)
R199 0Ohm (no_stuff)
6,26 STP_CPU# STPCPU#
26,27 PM_DPRSLPVR DPRSLPVR
29 CPU_VRON VRON
U15
MAX1987
TIME
R322 100KOhm
R695 10Ohm
R323 62KOhm
C280 10P
C291 0.47U
C709 4.7UF/16V
R306 100KOhm
R287 0Ohm
MCH_OK
R305 100KOhm
R307 0Ohm (no_stuff)
PM_PSI#
R284 10KOhm
R280 0Ohm
VR_PWRGD
6,9,26,29,55 VRM_PWRGD
R318 0Ohm
C269 0.1U (no_stuff)
R319 0Ohm
R327 0Ohm
C272 0.1U (no_stuff)
R326 0Ohm
C264 0.1UF
R304 2.7Ohm
RB717F
D13
R281 2.7Ohm
C260 0.1UF
C258 4.7UF/16V
C281 47P
T70
R309 511Ohm
R313 511Ohm
CCS+
CCM+
R316 1MOhm
C268 470PF/50V
R317 200Ohm
R310 1KOhm
R311 1KOhm
R345 100KOhm
R324 1.2KOhm
R325 4.7KOhm
C282 4700P
V1.1
Q71 IRF7413Z
Q72 IRF7831
Q79 IRF7413Z
Q78 IRF7831
C616 15UF/25V
C620 1U
C618 1000P
C173 1000P (no_stuff)
D37 EC31QS04
C682 1000P (no_stuff)
C702 15UF/25V
C706 1U
C701 1000P
D39 EC31QS04
V2.0
T39 TPC28t
L83 0.56UH
R637 3mOhm
CE12 330UF/2V
T147 TPC28t
L86 0.56UH
R644 3mOhm
CE16 330UF/2V
C184 0.1U
(27A)
T71 TPC28t STPCPU#
T72 TPC28t DPRSLPVR
T73 TPC28t VRON
T68 TPC28t MCH_OK
U53
U52 NC7ST04M5
NC7ST04M5
R312 0Ohm
R283 4.7KOhm
R282 0Ohm
CLK_EN#
R343 15KOhm
R320 36.5KOhm
R344 56KOhm
Q39A UM6K1N
Q39B UM6K1N
TIME
for C4 fast exit event
T148 TPC28t
6 CLK_PWR_GD#
Title : VCORE
ASUSTeK COMPUTER INC
Engineer: Louis_Lin
Size Custom
Project Name M9V
Rev 1.0
Date: Thursday, September 08, 2005
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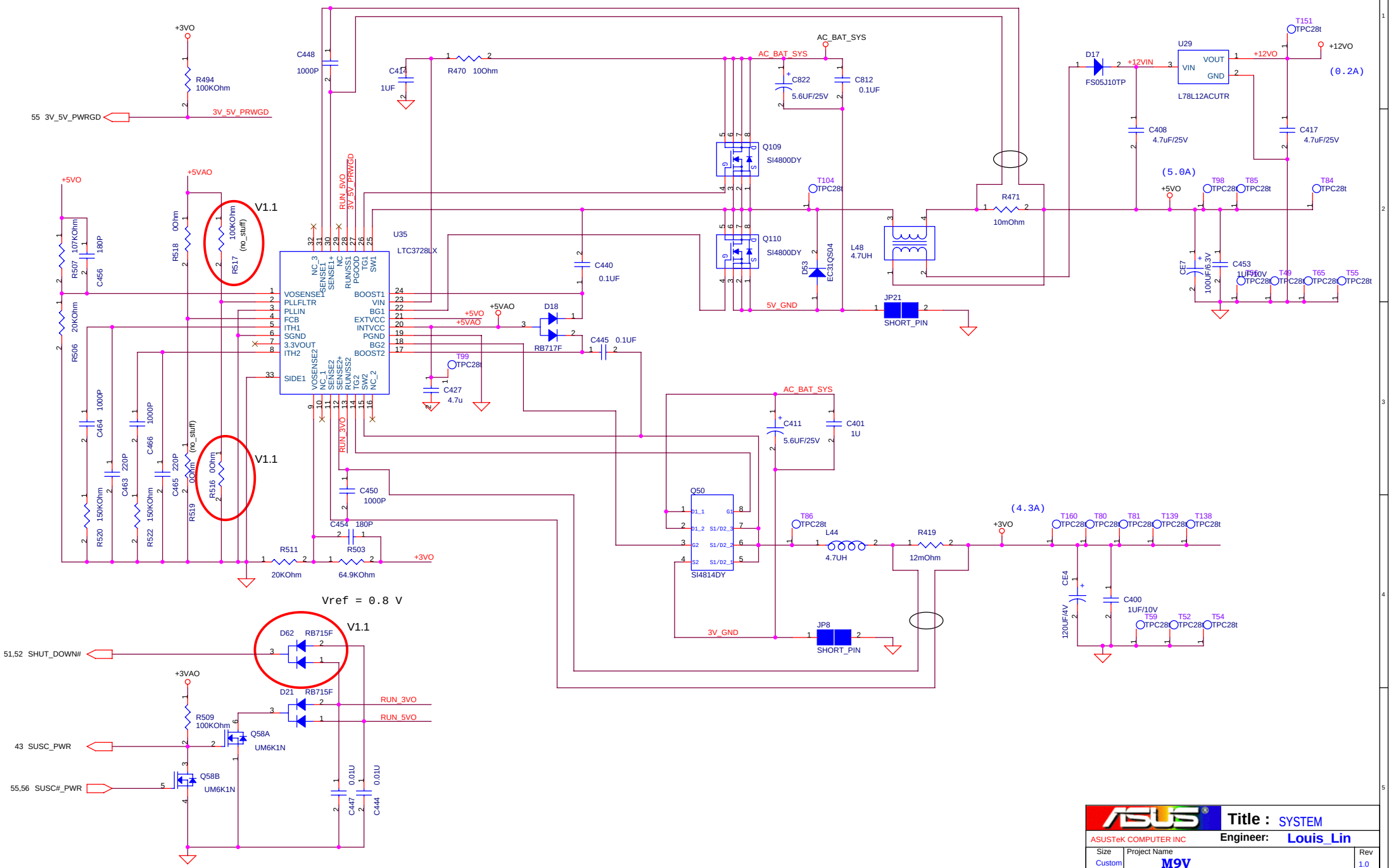
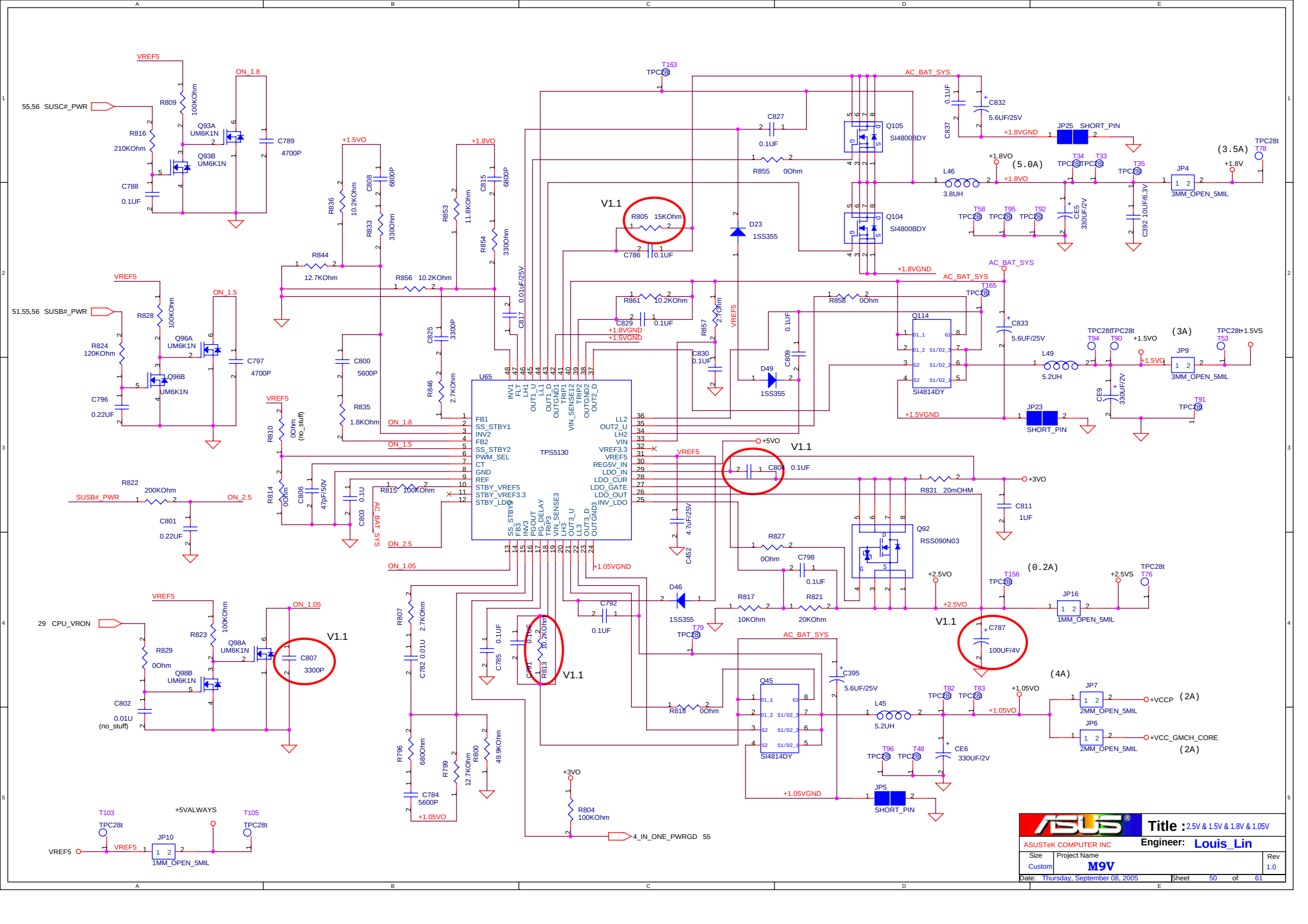
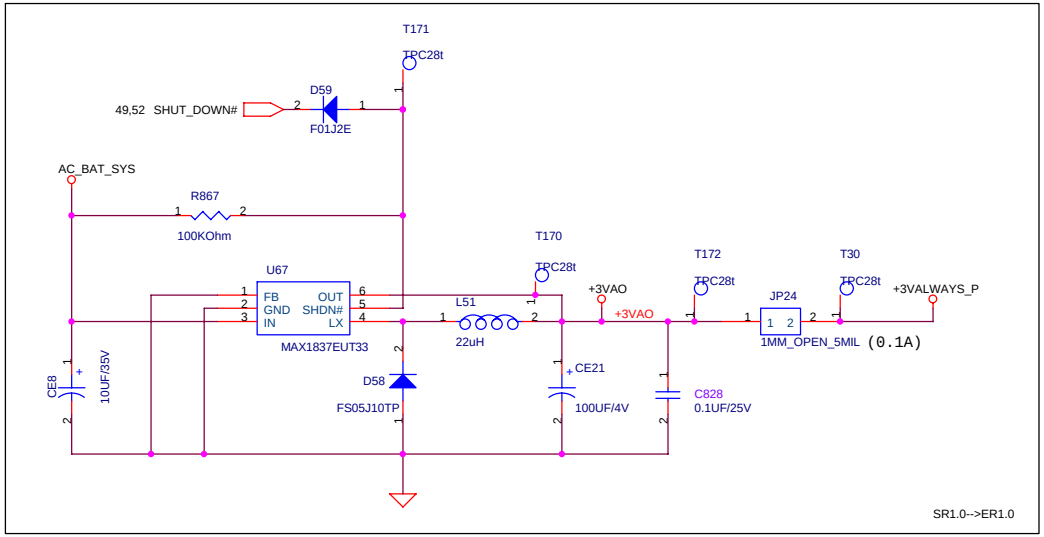
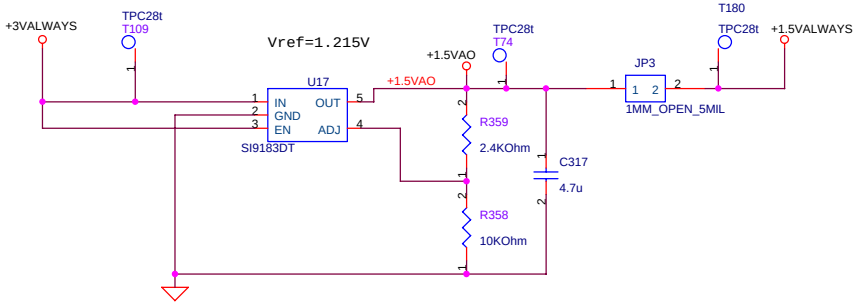
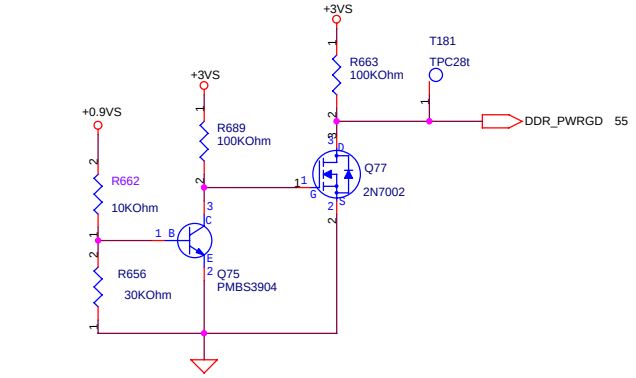


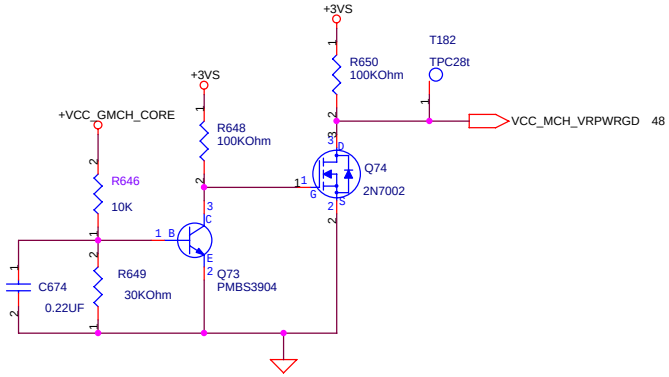
ASUSTeK COMPUTER INC	Title : SYSTEM	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 49 of 61	

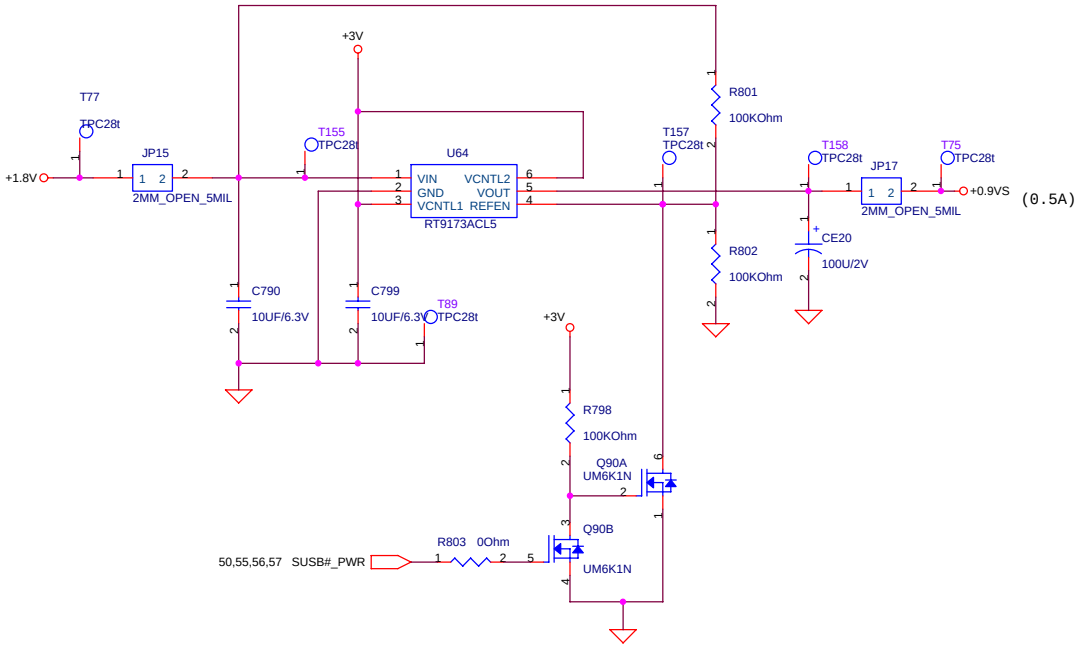

TPS5130
U65
VREF5
ON_1.8
ON_1.5
ON_2.5
ON_1.05
AC_BAT_SYS
+1.8VGND
+1.5VGND
+1.05VGND
+5VO
+3VO
+2.5VO
+1.8VO
+1.5VO
+1.05VO
+2.5VS
+1.5VS
+5VALWAYS
+VCCP
+VCC_GMCH_CORE
55,56 SUSC#_PWR
51,55,56 SUSB#_PWR
SUSB#_PWR
29 CPU_VRON
4_IN_ONE_PWRGD 55
V1.1
(3.5A)
(5.0A)
(3A)
(0.2A)
(4A)
(2A)
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Louis_Lin
Size: Custom
Project Name: M9V
Rev: 1.0
Date: Thursday, September 08, 2005
Sheet 50 of 61



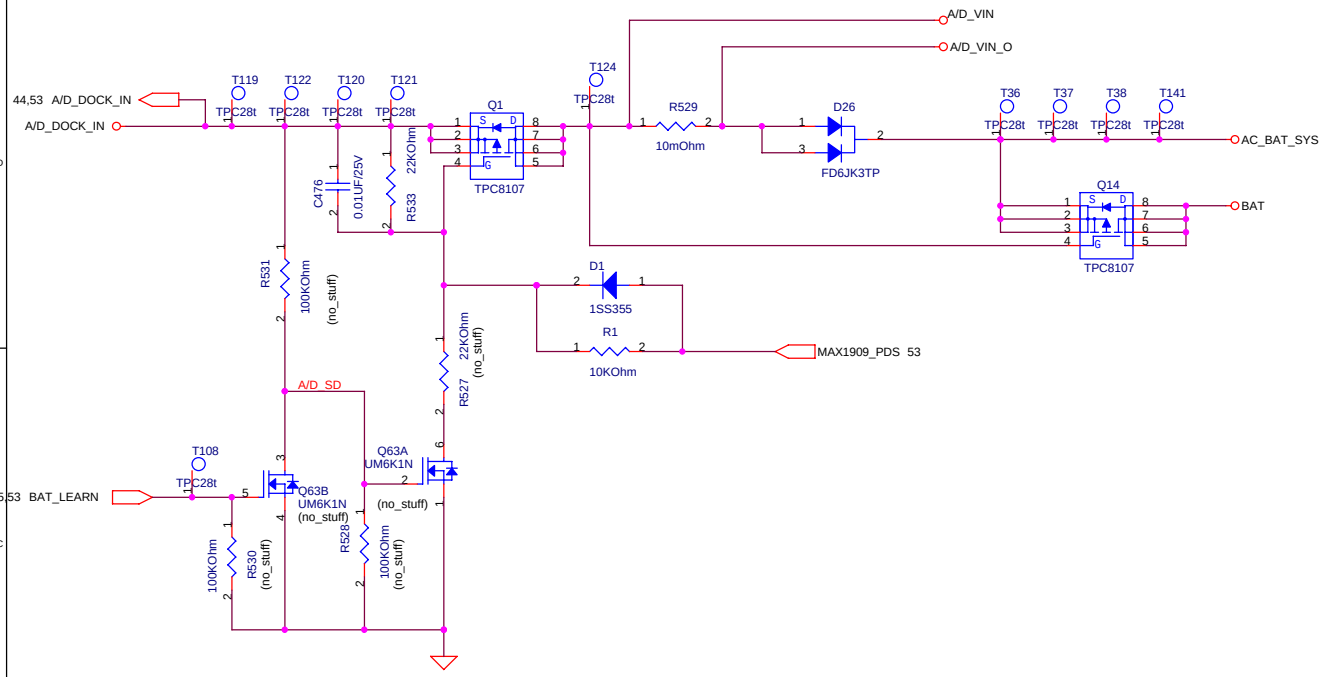




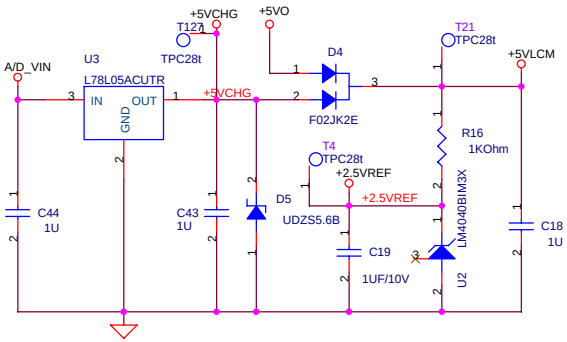




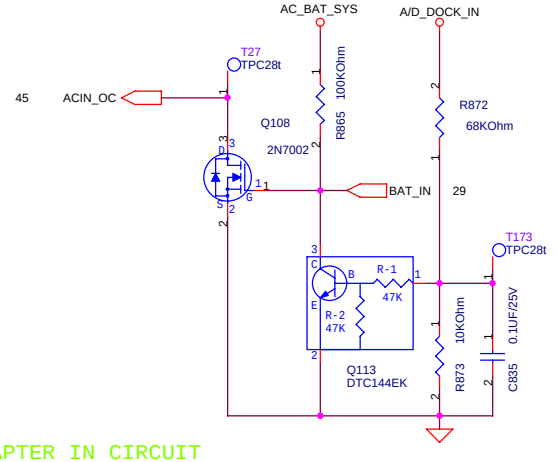
ASUSTeK COMPUTER INC	Title : 1.5VA & DDR2	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 51 of 61	



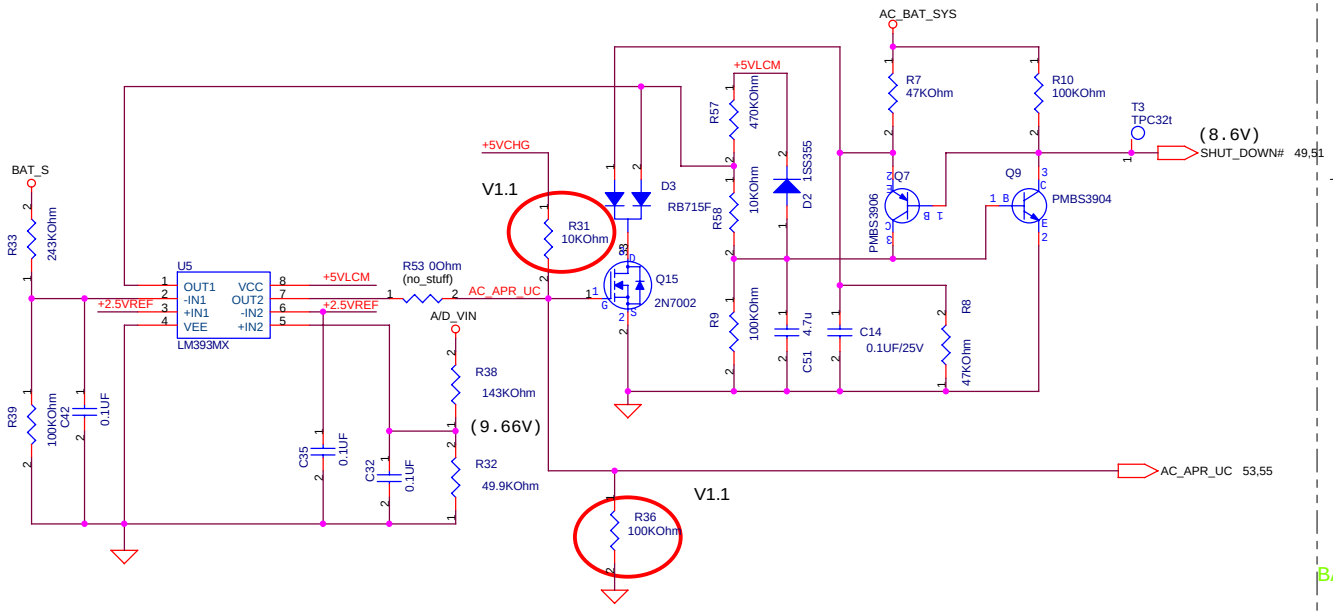
AC_BAT_SYS, BATTERY LEARN CIRCUIT



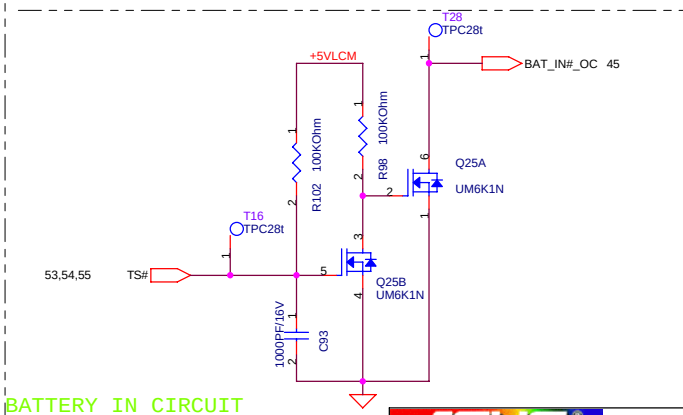
+5VCHG, +5VLCM, +2.5VREF



ADAPTER IN CIRCUIT

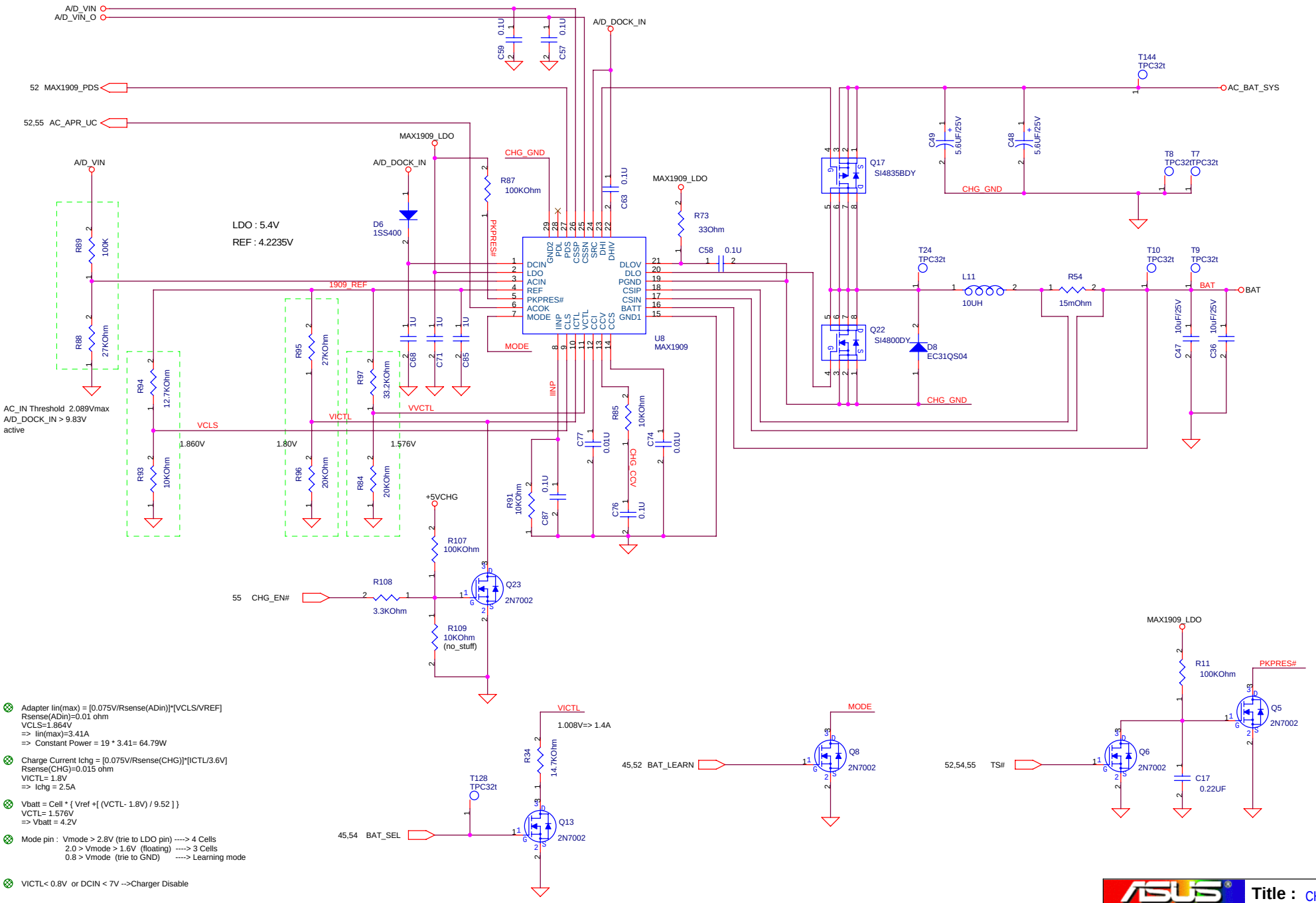


AC_IN & BATTERY SHUT_DOWN



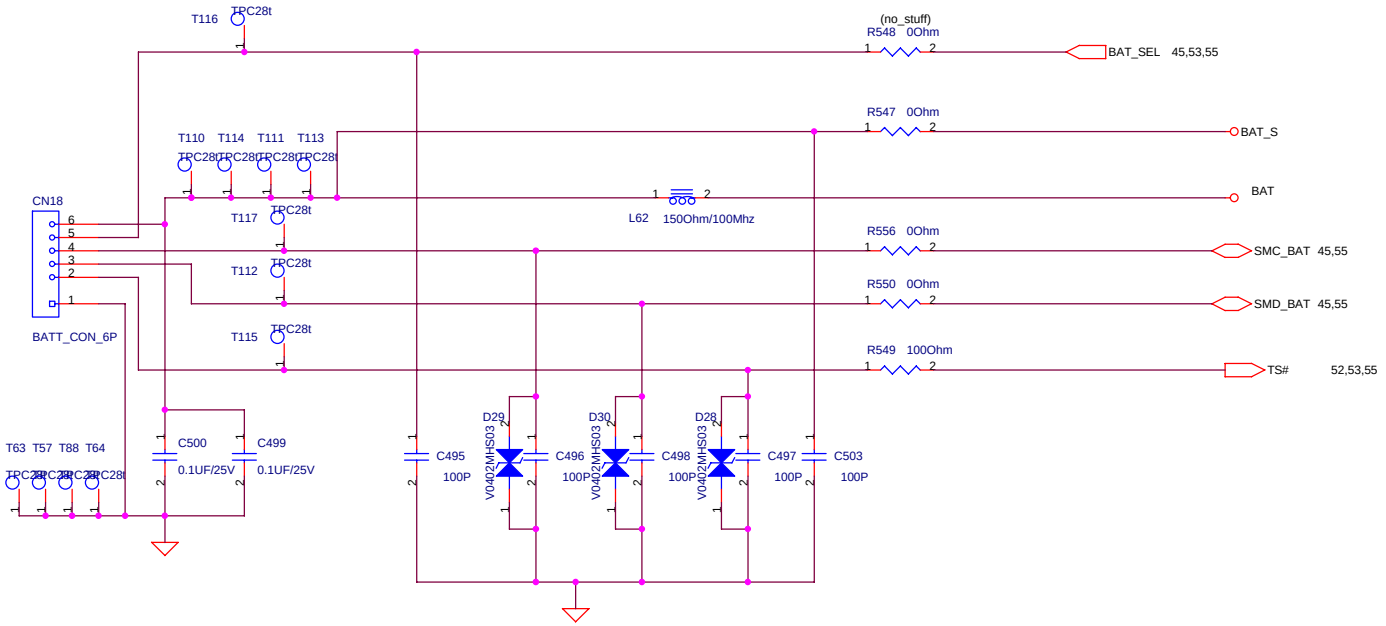
BATTERY IN CIRCUIT

ASUSTeK COMPUTER INC	Title : BATLOW/SD#	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 52 of 61	



- Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
  Rsense(ADin)=0.01 ohm
  VCLS=1.864V
  => Iin(max)=3.41A
  => Constant Power = 19 * 3.41= 64.79W
- Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
  Rsense(CHG)=0.015 ohm
  VICTL= 1.8V
  => Ichg = 2.5A
- Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
  VCTL= 1.576V
  => Vbatt = 4.2V
- Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
  2.0 > Vmode > 1.6V (floating) ----> 3 Cells
  0.8 > Vmode (trie to GND) ----> Learning mode
- VICTL< 0.8V or DCIN < 7V -->Charger Disable
- Pre_CHG_V = 3.1V
  Pre_CHG_I = 300mA

ASUSTeK COMPUTER INC	Title : CHARGER	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 53 of 61	

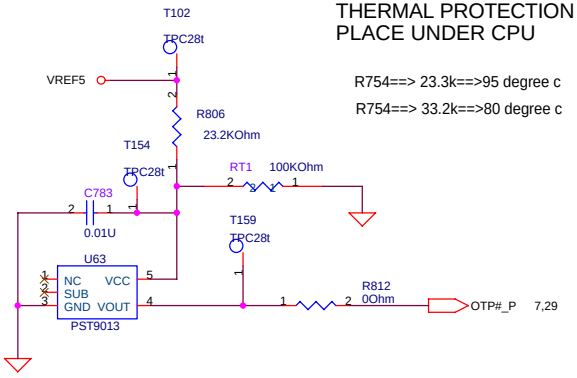


95 DEGREE C

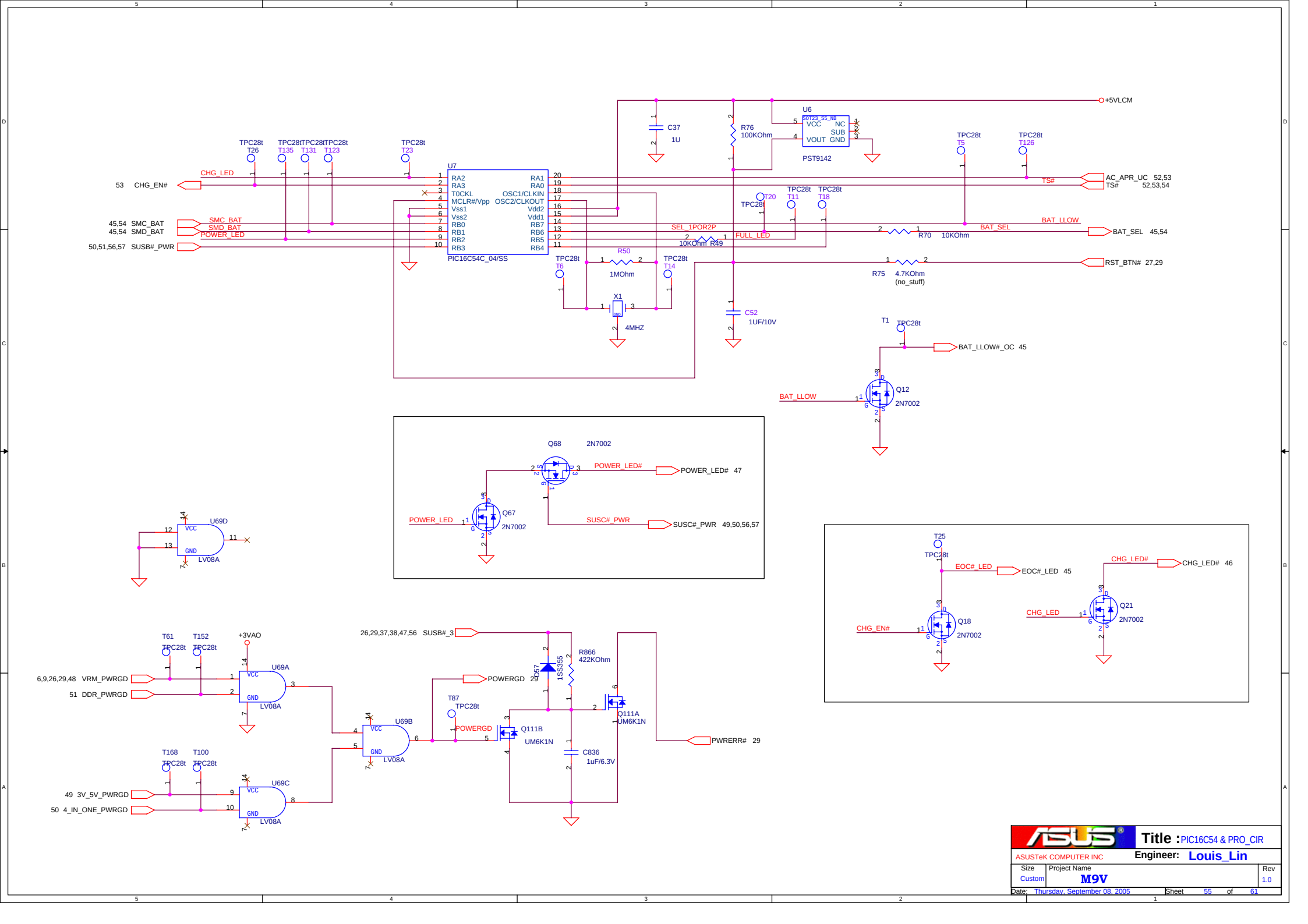
THERMAL PROTECTION
PLACE UNDER CPU

R754==> 23.3k==>95 degree c

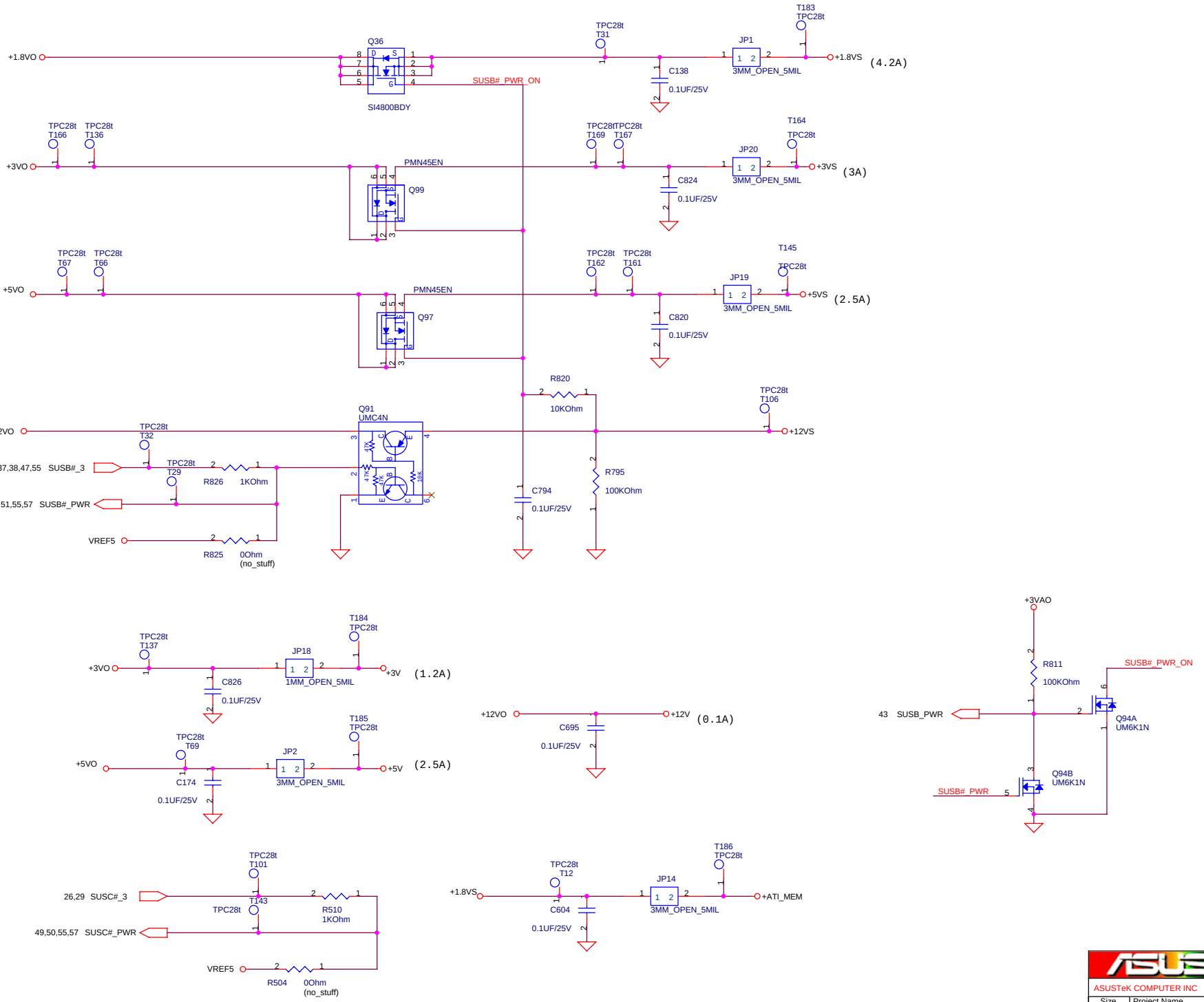
R754==> 33.2k==>80 degree c



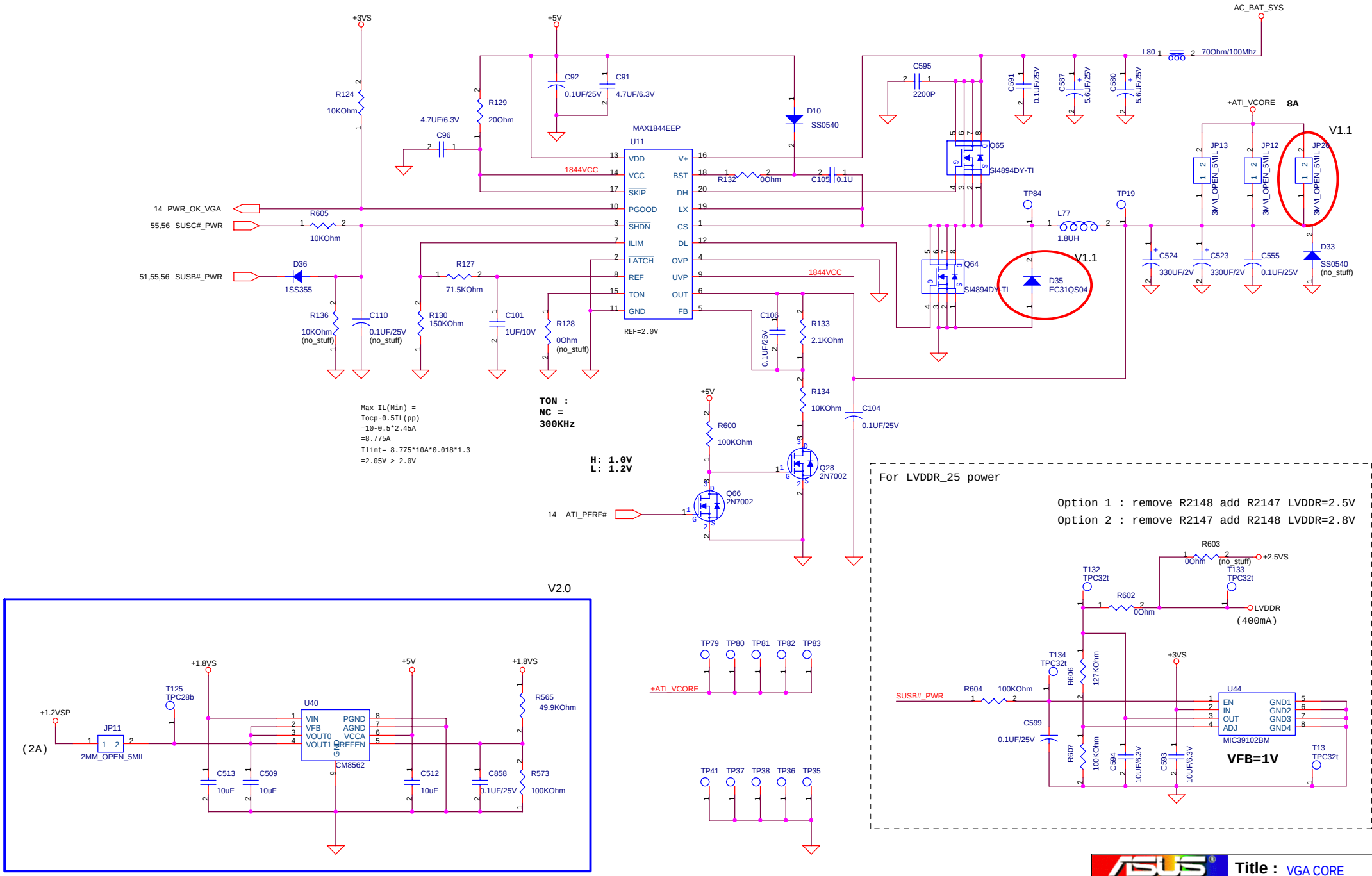
ASUSTeK COMPUTER INC	Title : BAT CONNECT	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 54 of 61	



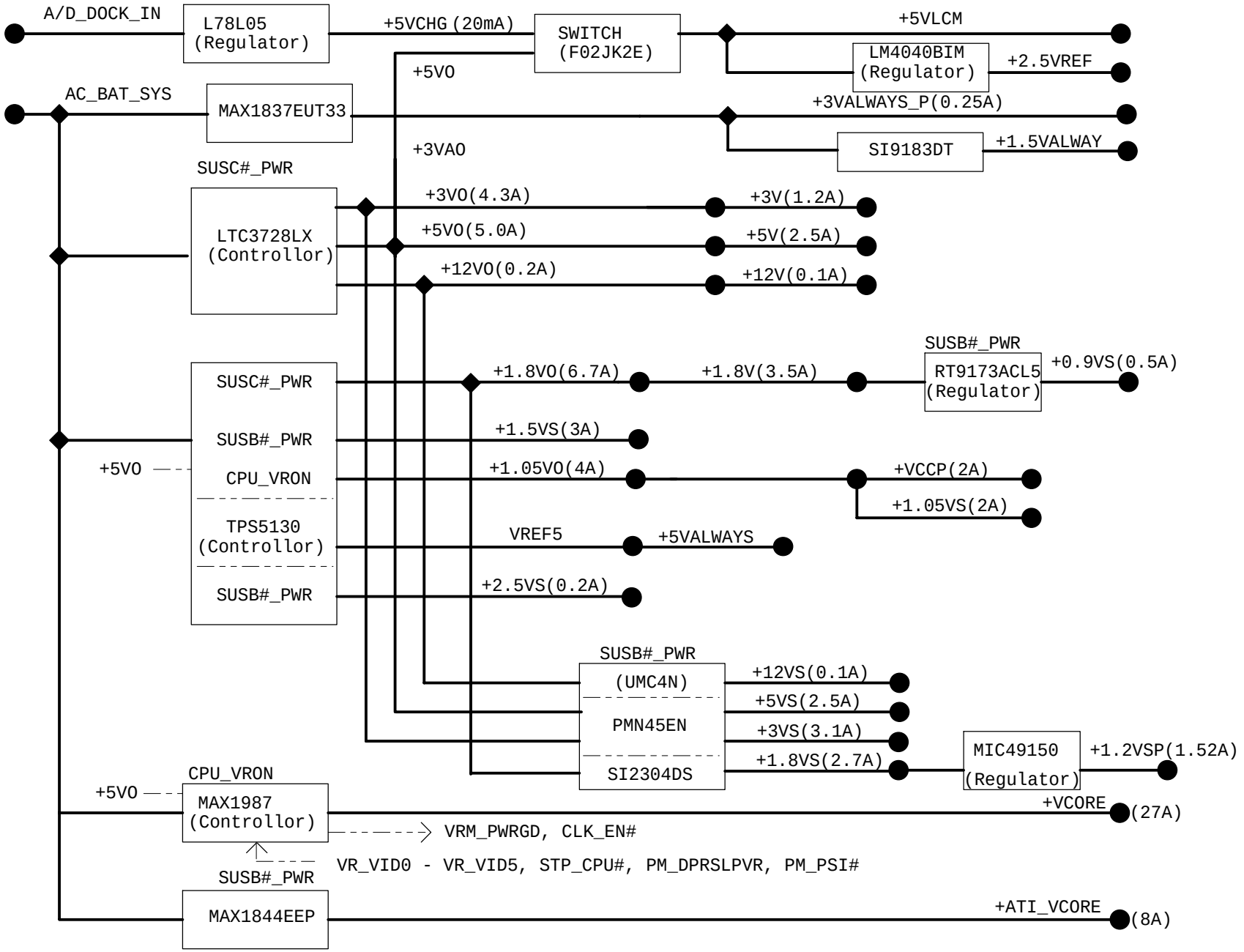
ASUSTeK COMPUTER INC	Title : PIC16C54 & PRO_CIR	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 55 of 61	



ASUSTeK COMPUTER INC	Title : LOAD SWITCH	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 56 of 61	



ASUSTeK COMPUTER INC	Title : VGA CORE		
	Engineer: Louis_Lin		
Size: Custom	Project Name: M9V		Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 57 of 61		



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Louis_Lin	
Size: Custom	Project Name: M9V	Rev: 1.0
Date: Thursday, September 08, 2005	Sheet 58 of 61	

POWER REVISION HISTORY

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REVISION HISTORY

SR -> ER	Page5,Page7,Page9,Page14,Page25,Page26,Page27,Page30
	Page37,Page39,Page43,Page45,Page46,Page47
	AUDIO CODEC REALTEK ALC880 ---> ADI AD1986A
	RENAME
	ADD U70, DEL C396, CHANGE CN21 3P--->4P, CHANGE U54
	ADT7460--->ADT7473, CHANGE CN13, DEL R768, DEL R774,
	CHANGE CN10(P1<->P12), CHANGE CN3(P5<->P7), ADD U71, R881,
	R882, R883, C840, U72, R884, R885, R886, C841
	DEL R267, ADD R887, R888, C842
	ADD U32.P2 R889, R890, R891, DJ_SW# -> U12.P76
	ADD R892, R893, R894, R895, R896, R897, R898
	ADD R899, R900, R901, R902
	ADD R903, R904, R905
ER -> PR	Page5,Page6,Page7,Page14,Page25,Page26,Page27,Page28
	Page32,Page33,Page37,Page43,Page44,Page45,Page46
	Page47
	ADD R906
	ADD R907, R908, R909, C843, U75, R913
	CHANGE U47 +5VS TO +3VS
	ADD SPDIF Circuit
	ADD R914, R915, R916, R917, Q121
	ADD TPM Circuit, R919, R920, R921, R922
	ADD R923, R924, R925
	CHANGE C267, C271 12PF/50V--->33PF/50V
	ADD Q118, R701 CONNECT TO Vcore
	ADD D67, R926, R927, R928
	CHANGE PCB_ID0~2
	CHANGE R521, R523, R524, R525, R887
	CHANGE CN6 13P--->14P, CN11 +3VS--->+3VALWAYS
PCB P/N	MAIN BOARD 08-29MV0020I,08-29MV0020W
	INSTANT KEY BOARD 08-29MV01207,08-29MV0120P
	AUDIO DJ BOARD 08-29MV02207,08-29MV0220P
	MIC BOARD 08-29MV03207,08-29MV0320P

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+3V
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
CPU_VRON	O	+3V
VRM_PWRGD	I	+3V
CPU_STP#	O	+3V
CHG_LED	I	+3V
RST_BTN#	O	+3V
OTP_RESET#	I	+3V
SHUT_DOWN#	I	+3V
+V5_LCM	PWR	+5V
PM_SLPDLY_S3#	O	+3V
PM_SLP_S4#	O	+3V
BAT_LEARN	I	+3V
BAT_LLOW#_OC	I	+3V
BAT1_IN#_OC	I	+3V
BAT2_IN#_OC	I	+3V
ACIN_OC	I	+3V
CHG_EN_OC	I	+3V
PM_DPRSLPVR	O	+3V
ACIN_3VA	I	+3V
+5VAO	PWR	+3V
EN_+3VALWAYS	O	+3V
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMCLK_BAT1	IO	+3V
SMDATA_BAT1	IO	+3V
SMCLK_BAT2	IO	+3V
SMDATA_BAT2	IO	+3V
BAT_LOW#	I	+5VLCM
1.5V_PWRGD	I	+3V
1.8V_PWRGD	I	+3V

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.32A
+VCC_GMCH	1.05V	3.9A
+0.9VS	1.25V	2.28A
+1.5VS	1.5V	4.69A
+1.5VA	1.5V	270 mA
+1.8V	1.8V	7.89A
+1.8VS	1.8V	3.2A
+2.5VS	2.5V	200 mA
+3VS	3.3V	2.69A
+3V	3.3V	2.17A
+3VA	3.3V	435 mA
+5VS	5V	5.37A
+5V	5V	4.3A
+12V	12V	50 mA
+12VS	12V	10 mA
ATI_+VCORE	1.0V - 1.2V	8 A
+1.2VSP	1.2V	1.5 A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/IN3/BOT	14 mils
IN1/IN2	16.5 mils

37.5 OHM	WIDTH
TOP/IN3/BOT	8.5 mils
IN1/IN2	10 mils

42 OHM	WIDTH
TOP/IN3/BOT	7 mils
IN1/IN2	8.5 mils

55 OHM	WIDTH
TOP/IN3/BOT	4 mils
IN1/IN2	4.5 mils

60 OHM	WIDTH
TOP/IN3/BOT	3 mils
IN1/IN2	4 mils

Differential

70 OHM	WIDTH/SPACE
TOP/IN3/BOT	8 mils/ 5 mils
IN1/IN2	8 mils/ 4.5 mils

90 OHM	WIDTH/SPACE
TOP/IN3/BOT	5 mils/ 8 mils
IN1/IN2	5 mils/ 6 mils

100 OHM	WIDTH/SPACE
TOP/IN3/BOT	4 mils/ 9 mils
IN1/IN2	4.5 mils/ 7.5 mils

PCI INTERFACE

PCI_REQ#

LAN	PCI_REQ#1
CB&1394	PCI_REQ#2
MINIPCI	PCI_REQ#3

IDSEL

LAN	PCI_AD16
CB&1394	PCI_AD17
MINIPCI	PCI_AD19

PCB STACK-UP

PCB THICKNESS: 1.2 mm

L1	TOP
L2	GND1
L3	IN1
L4	IN2
L5	VCC
L6	IN3
L7	GND2
L8	BOT

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SIGNAL	IN:	VR_VID0 - 5 PM_DPRSLPVR STP_CPU# PM_PSI# IMVP_VR_ON
	OUT:	DELAY_VR_PWRGD VR_PWDGD_CK410#
POWER	IN:	AC_BAT_SYS +5VO +3VO
	OUT:	+VCORE

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SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12VO +3VO +5VO

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SIGNAL	IN:	SUSB#_PWR SUSC#_PWR
POWER	IN:	AC_BAT_SYS +3VO
	OUT:	+1.8V +1.5V +2.5V +VCC_GMCH_CORE +5VALWAYS +3VALWAYS

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SIGNAL	IN:	SUSB#_PWR
	OUT:	VCC_MCH_VRPWRGD IMVP_VR_ON
POWER	IN:	+3VA +3V +1.8V +VCC_GMCH_CORE
	OUT:	+0.9VS +1.5VA +VCCP