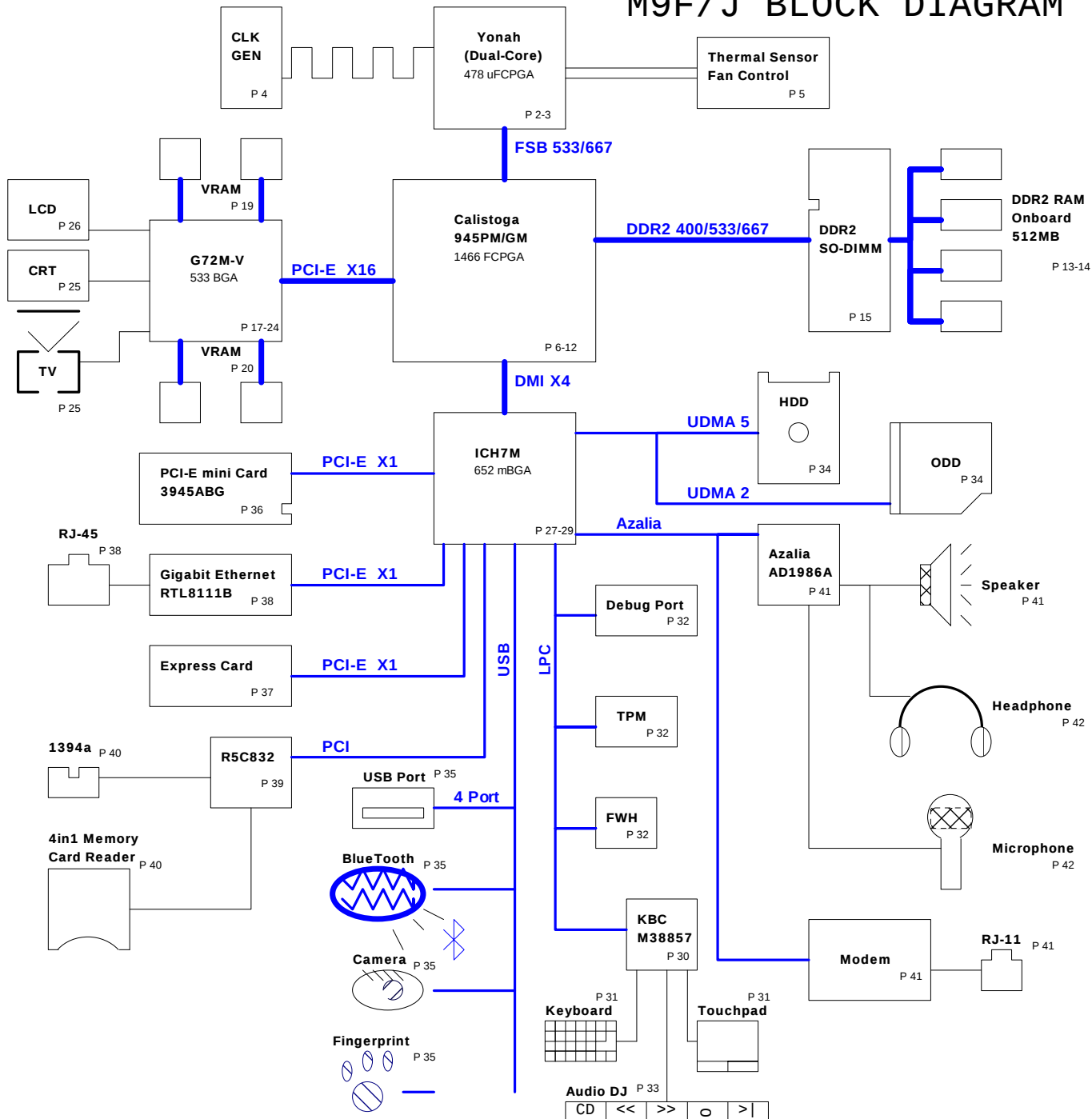
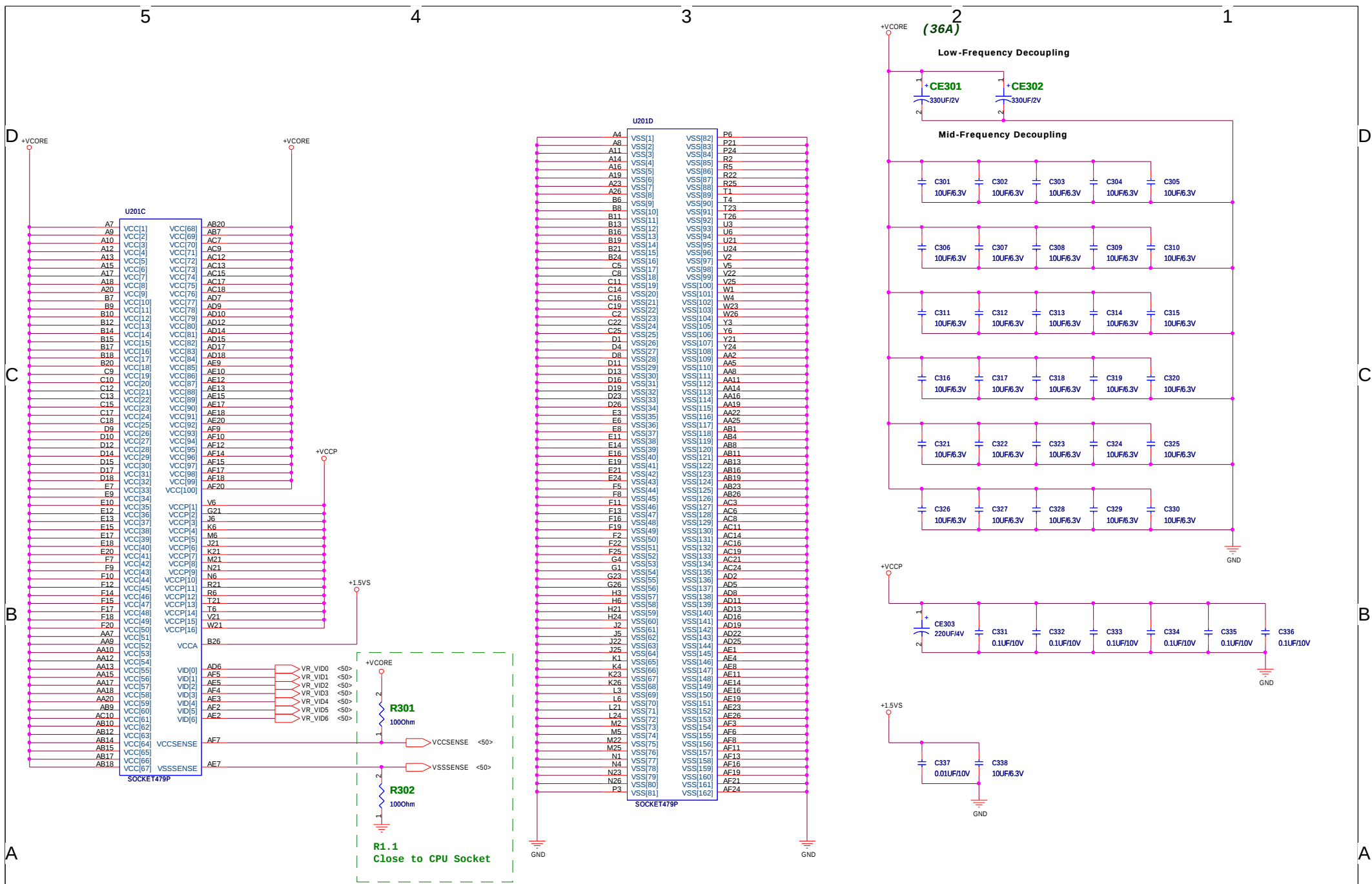


M9F/J BLOCK DIAGRAM

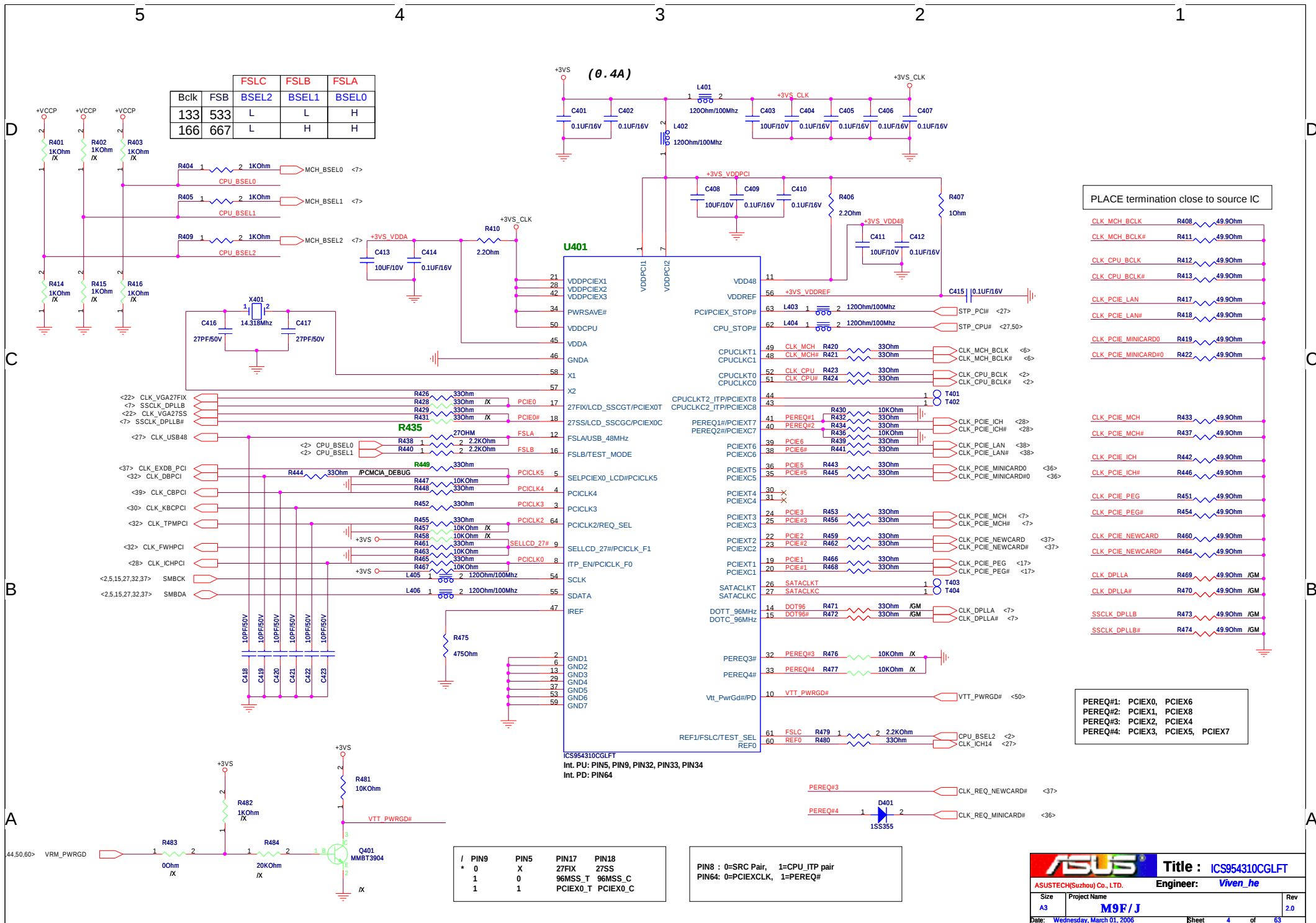
Content

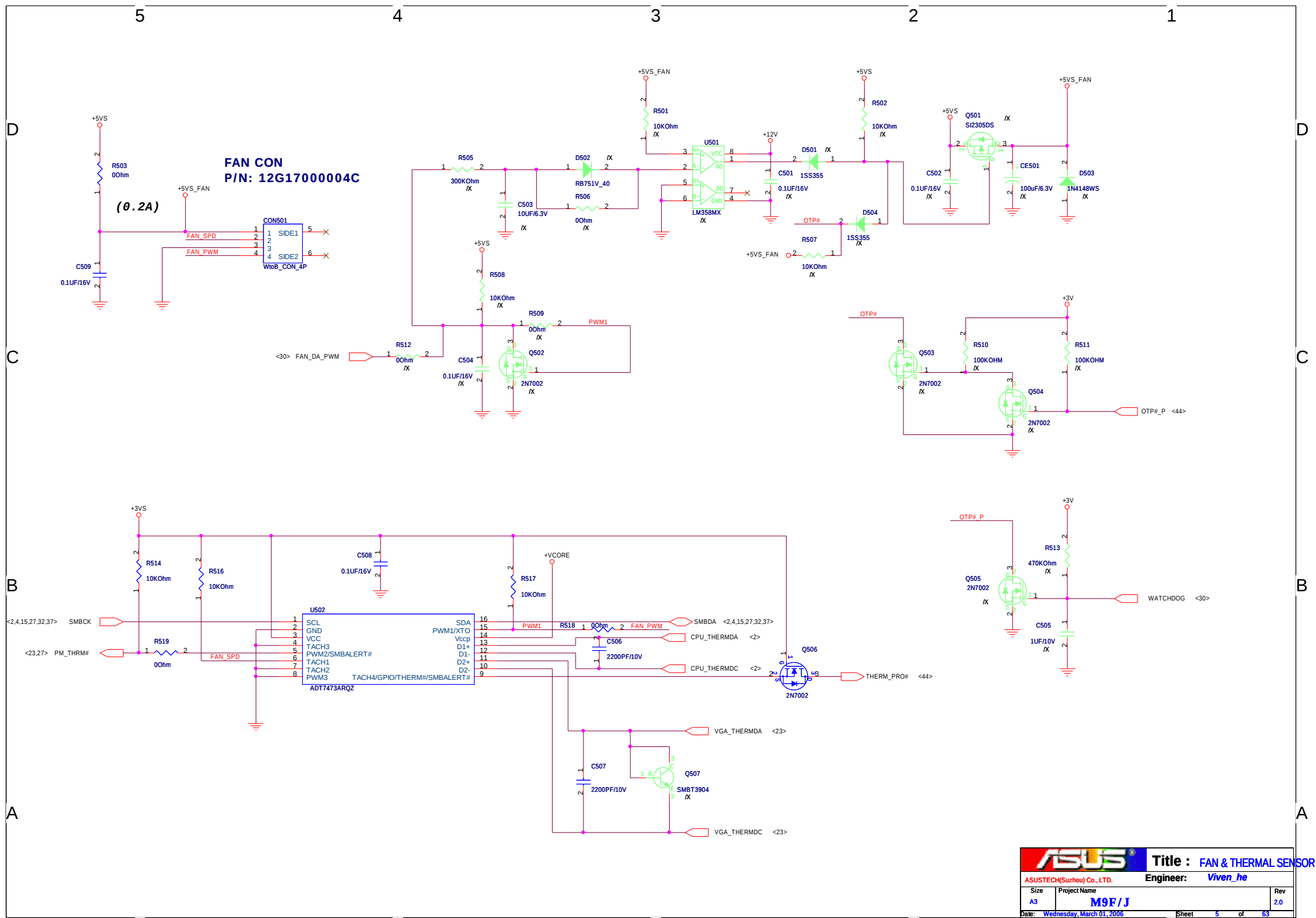
01. Block Diagram & Content
02. Yonah - Host
03. Yonah - Power/GND
04. Clock Gen - ICS954310CGLFT
05. Thermal Sensor & Fan
06. Calistoga - Host
07. Calistoga - DMI
08. Calistoga - PCIE
09. Calistoga - SysMEM
10. Calistoga - Power-1
11. Calistoga - Power-2
12. Calistoga - GND
13. DDR2 Onboard CHA-1
14. DDR2 Onboard CHA-2
15. DDR2 Slot CHB
16. DDR2 Termination
17. G72M-V - PCIE
18. G72M-V - FB I/F
19. G72M-V - VRAM1
20. G72M-V - VRAM2
21. G72M-V - LVDS
22. G72M-V - CRT/TV OUT
23. G72M-V - GPIO
24. G72M-V - STRAPING&GND
25. CRT & TV CON
26. LCD & INVERTER
27. ICH7M - Azalia/IDE/PM
28. ICH7M - PCI/PCI-E/USB
29. ICH7M - Power/GND
30. KBC - M38857
31. Keyboard & Touchpad & LED
32. TPM & FWH & Debug
33. Audio DJ
34. HDD & ODD CON
35. USB
36. mini Card
37. Express Card
38. Gigabit Ethernet - RTL8111B
39. R5C832
40. 4-IN-1 Card & 1394a CON
41. Azalia Codec & Modem CON
42. Audio Amplifier & Depop
43. Audio Jack
44. Power Sequence
45. Power Discharge
46. DC-IN & BAT-IN
47. Screw Hole
48. Dummy
49. Dummy
50. POWER_VCORE
51. POWER_SYSTEM
52. POWER_I/O_1.5VO & 1.05VO
53. POWER_I/O_DDR & VTT
54. POWER_I/O_+3VAO & +2.5VS
55. POWER_VGA_CORE
56. POWER_VGA_+1.2VS
57. POWER_CHARGER
58. POWER_PIC
59. POWER_DETECT
60. POWER_PROTECT
61. POWER_LOAD SWITCH
62. POWER_FLOWCHART
63. POWER_SIGNAL





		FSLC	FSLB	FSLA
Bclk	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H





5

4

3

2

1

STRAPPING CONFIGURATION

CFG[17:3] - Internal pull-up

CFG[20:18] - Internal pull-down

R705 2.2KOhm /X DMI_SEL

CFG5 - DMI x2 Select
0 = DMI x2
1 = DMI x4 (default)

R710 2.2KOhm /X CPU_STRAP

CFG7 - CPU Strap
0 = Reserved
1 = Mobile CPU (default)

R711 2.2KOhm PCIE_RVS

CFG9 - PCI-E Lane Reversal
0 = Reverse Lanes
1 = Normal (default)

R714 2.2KOhm /X TEST_MD0

R715 2.2KOhm /X TEST_MD1

CFG[13:12] - XOR/ALLZ
00 = Partial CLOCK Gating Disable
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal (default)

R718 2.2KOhm /X DYN_ODT

CFG16 - FSB Dynamic ODT
0 = Disabled
1 = Enabled (default)

+3VS

R723 1KOhm /X VCC_SEL

CFG18 - GMCH VCC Select
0 = 1.05V (default)
1 = 1.5V

R725 1KOhm /X DMI_RVS

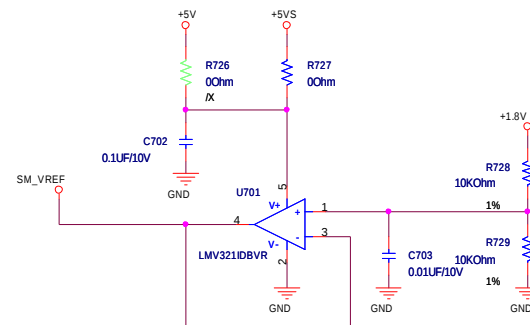
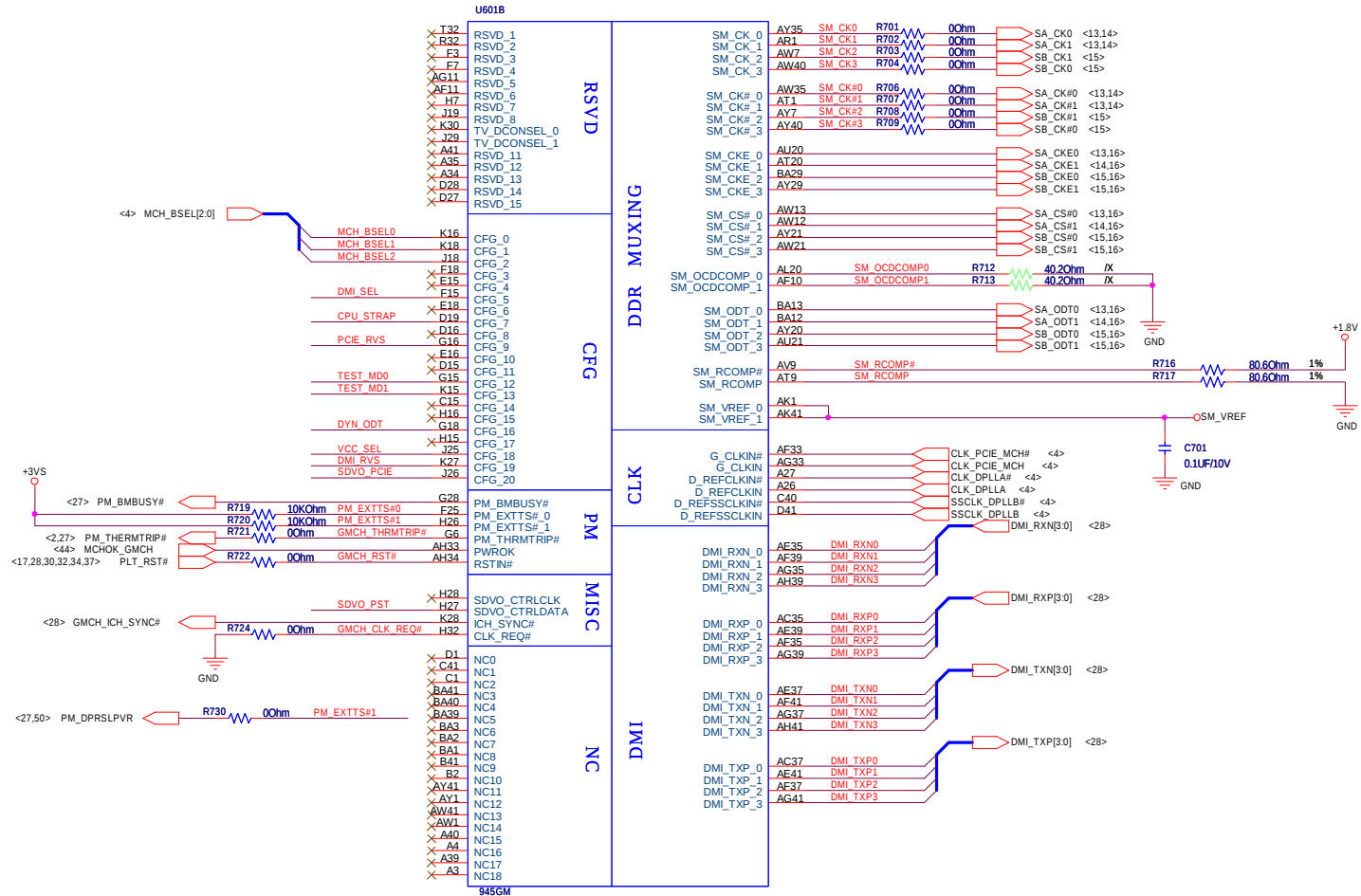
CFG19 - DMI Lane Reversal
0 = Normal (default)
1 = Reverse Lanes

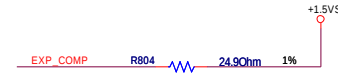
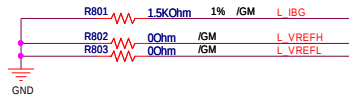
T701 1 TPC28T SDVO_PCIE

CFG20 - SDVO/PCIE Concurrent
0 = Only SDVO or PCIE x1 is operational (default)
1 = SDVO and PCIE x1 are operating simultaneously via PEG port

T702 1 TPC28T SDVO_PST

SDVO_CTRLDATA - SDVO Present
0 = No SDVO Card Present (default)
1 = SDVO Card Present





D

D

C

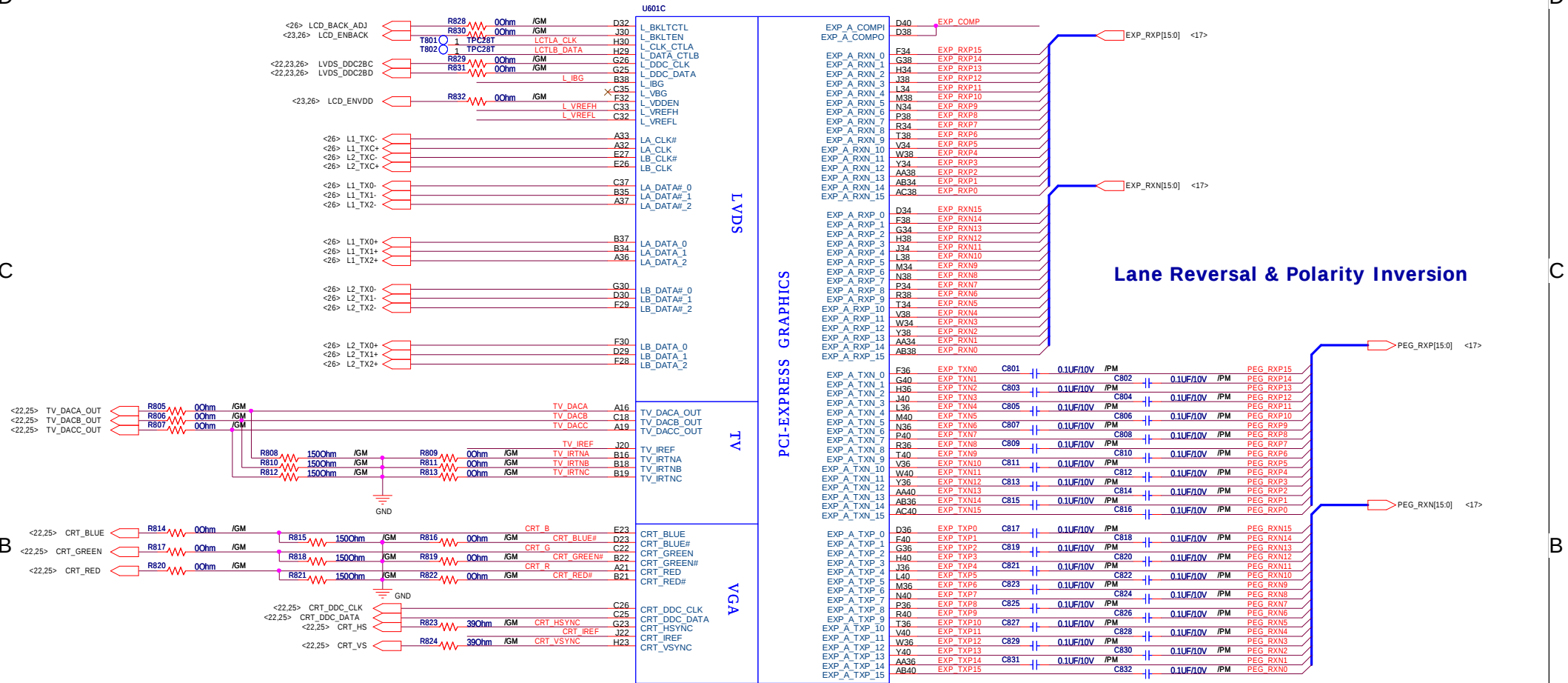
C

B

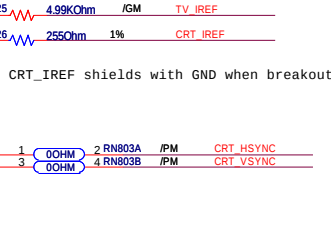
B

A

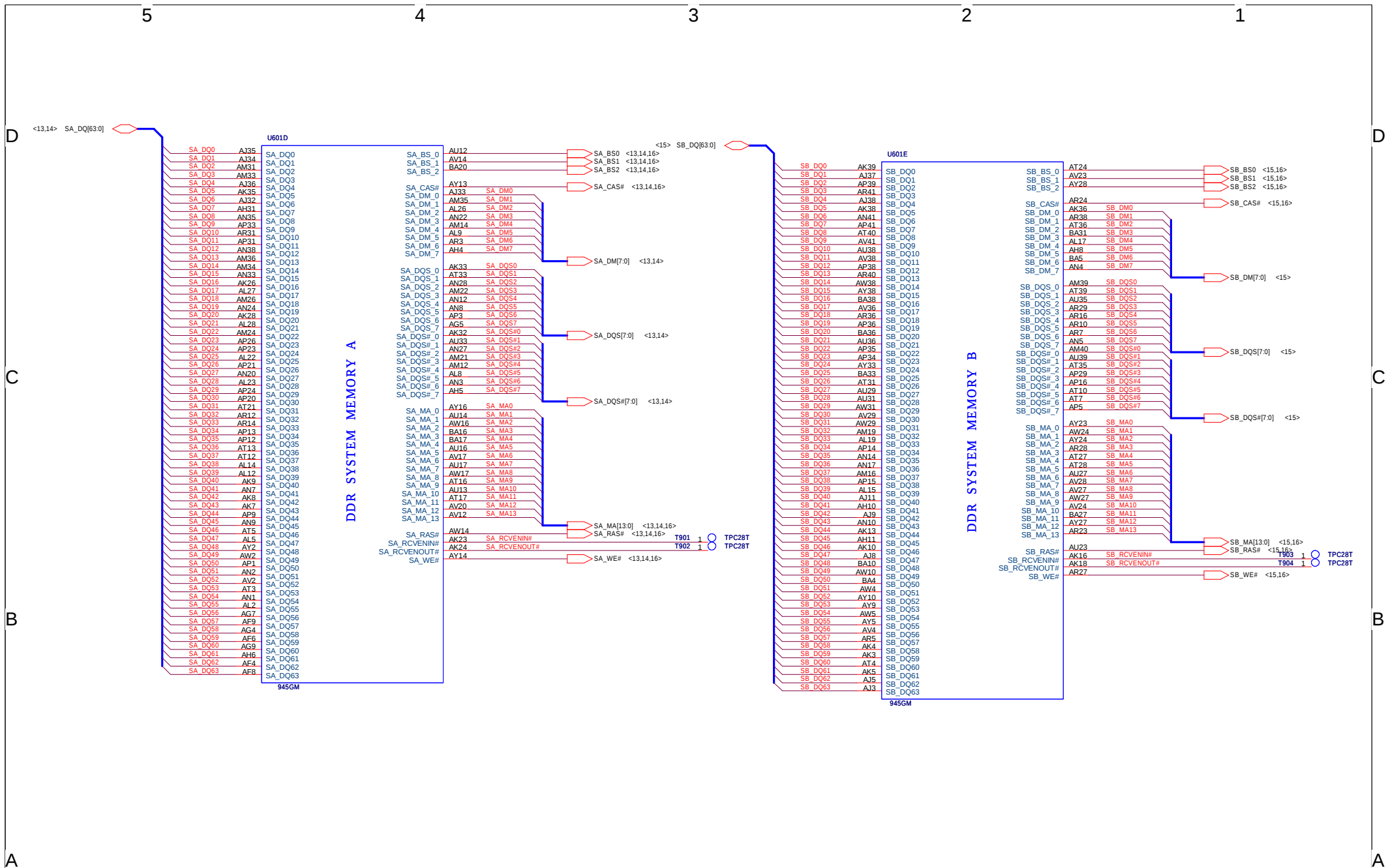
A

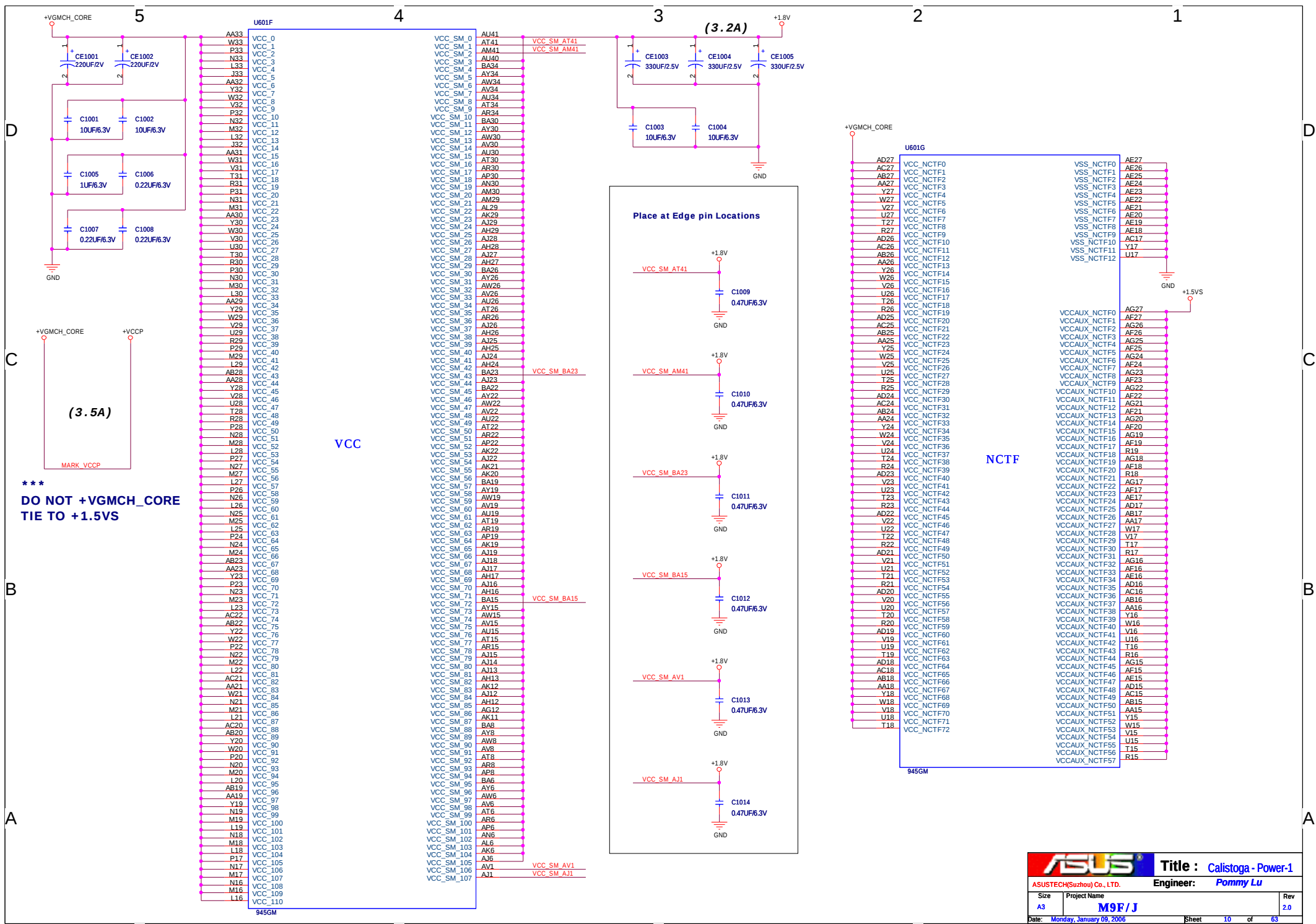


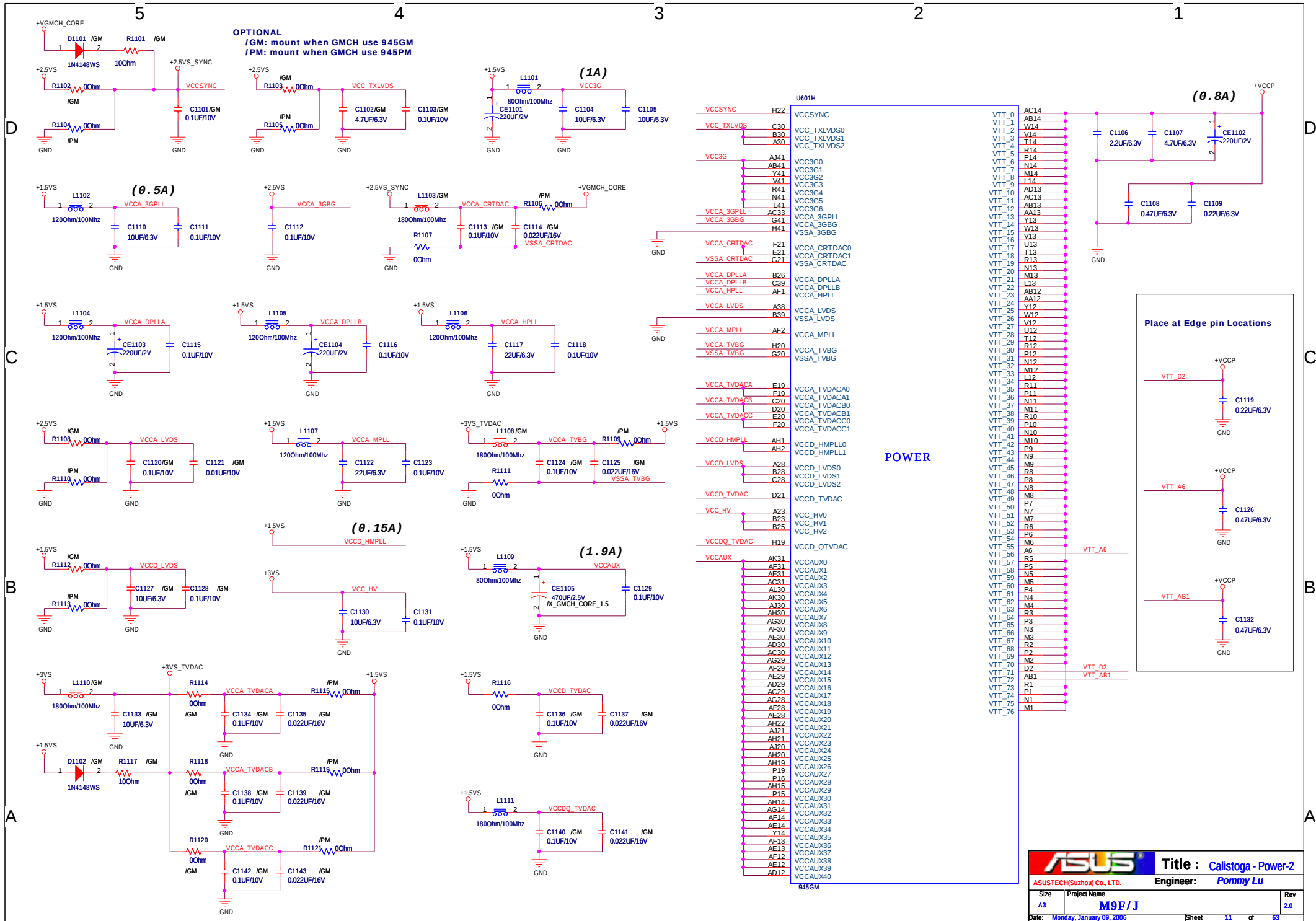
OPTIONAL
/GM: mount when GMCH use 945GM
/PM: mount when GMCH use 945PM

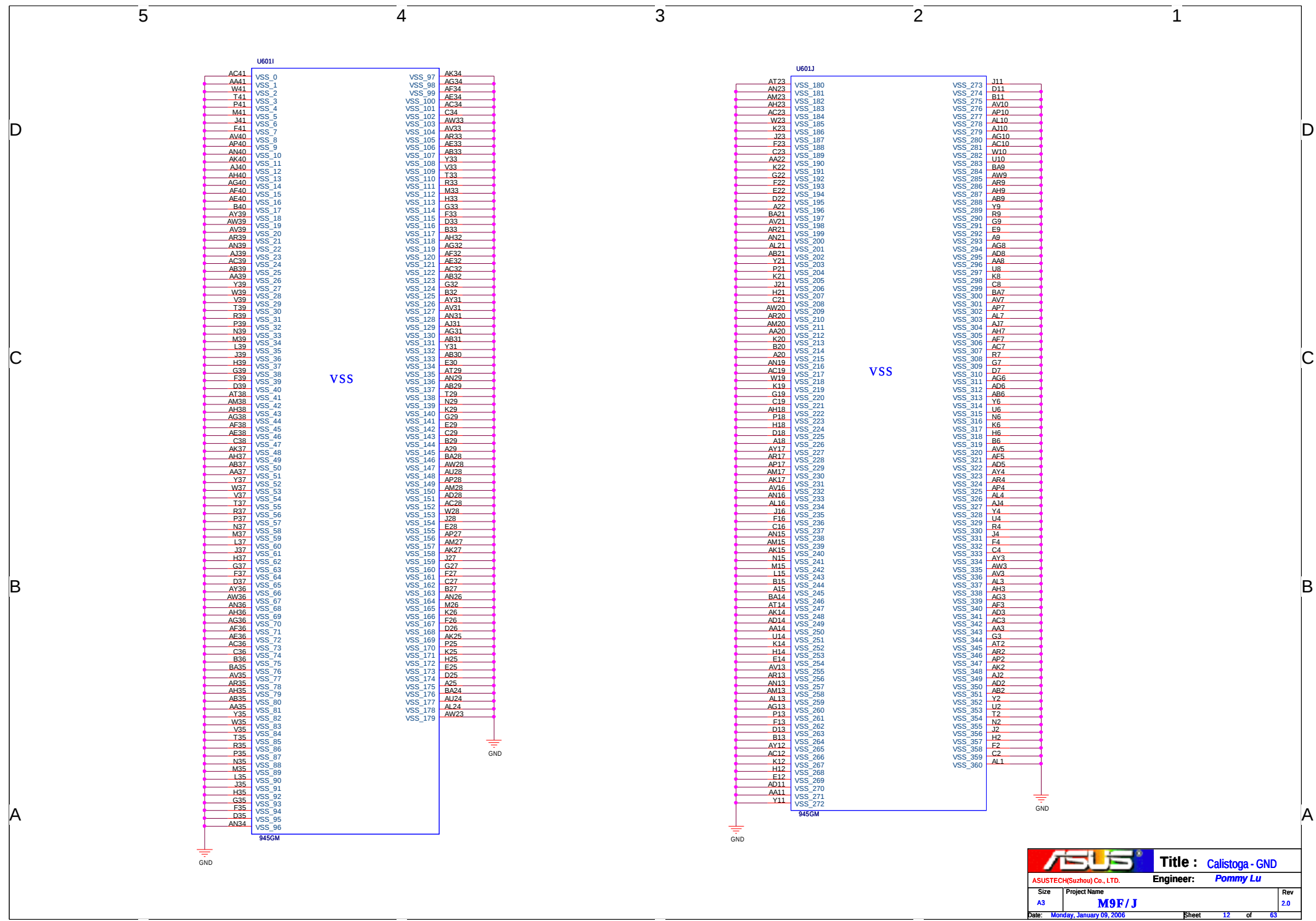


CRT_IREF shields with GND when breakout









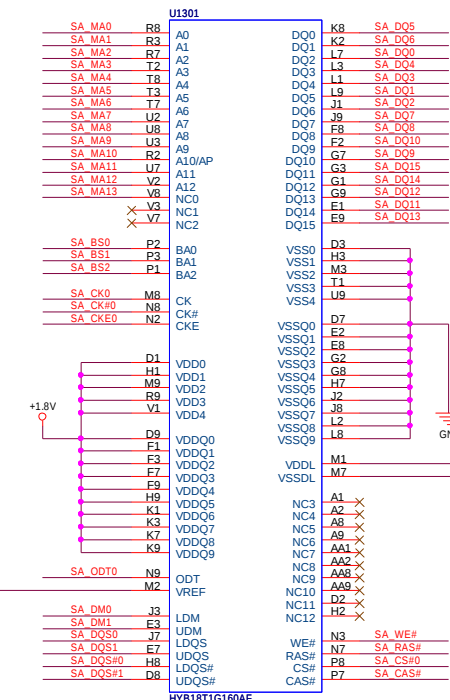
5

4

3

2

1

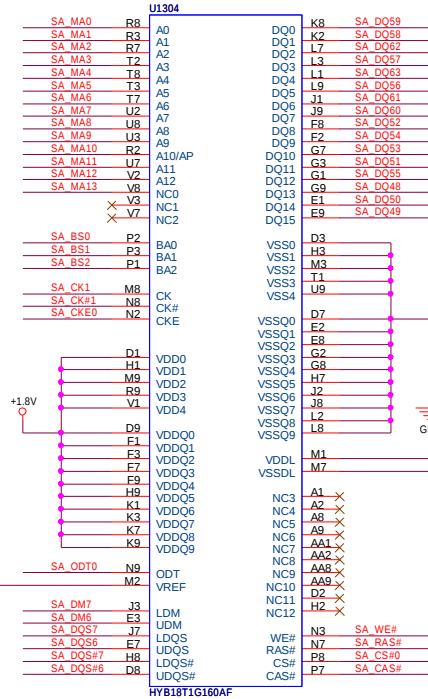
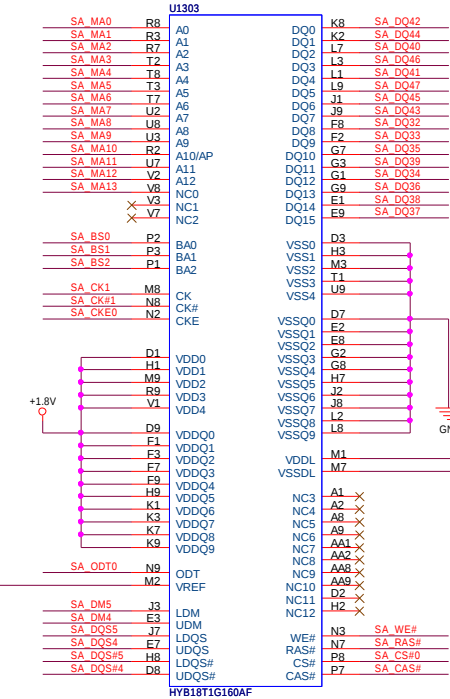
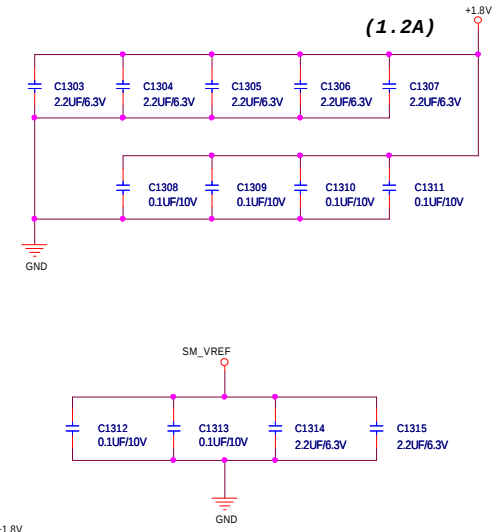
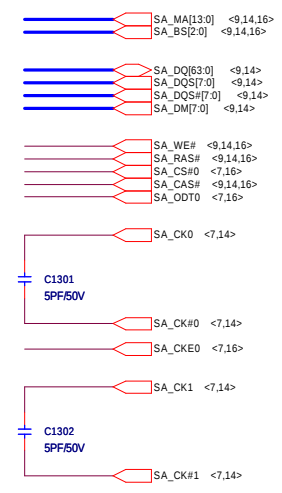
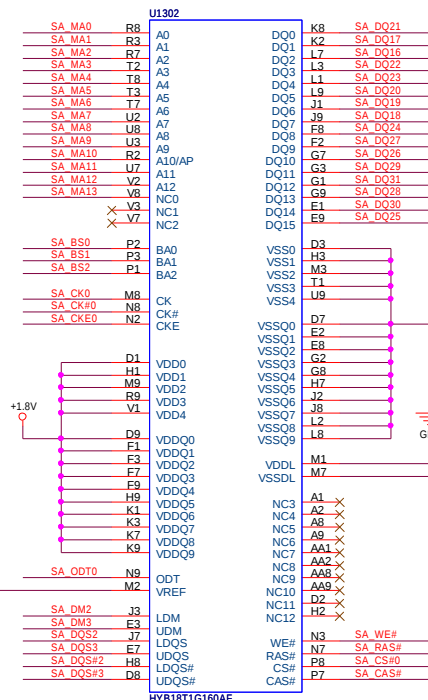


On Board 256MB
DDR2 533 32Mx16-3.7
P/N: 03G15073B010 (1st)
03G15133E110 (2nd)

On Board 512MB
DDR2 533 32Mx16-3.7
P/N: 03G15073B010 (1st)
03G15133E110 (2nd)

On Board 512MB
DDR2 667 32Mx16-3
P/N: (null)

On Board 1GB
DDR2 533 64Mx16-3.7
P/N: 03G15163E010





5

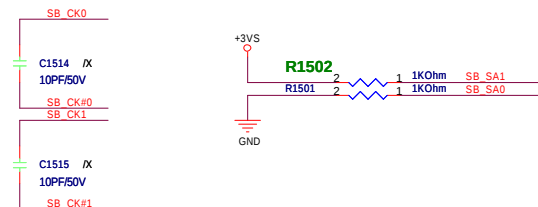
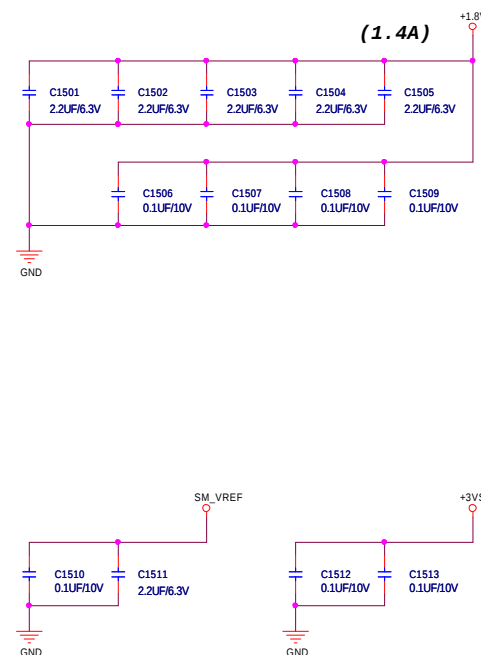
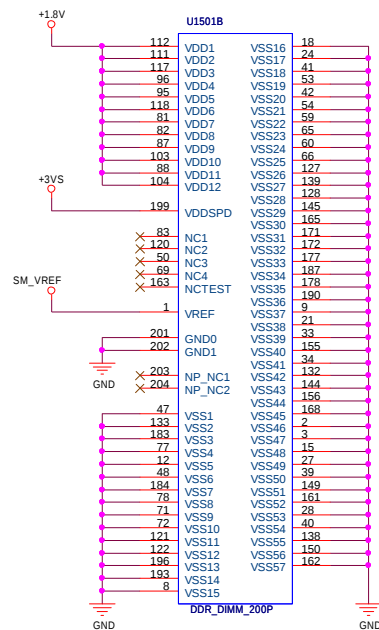
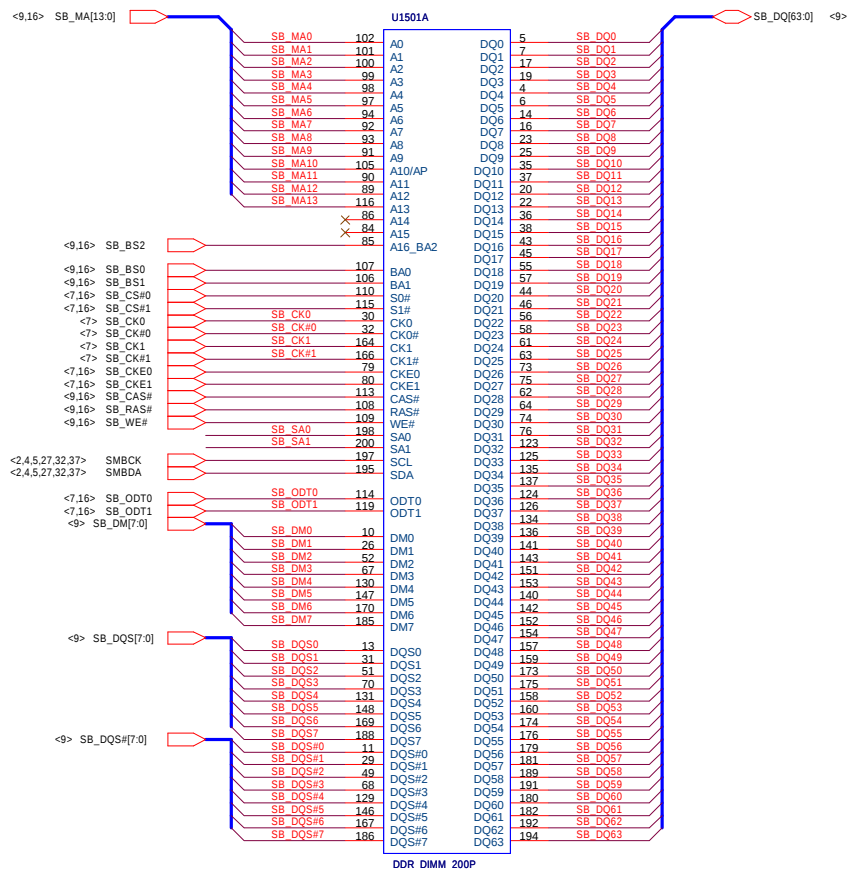
4

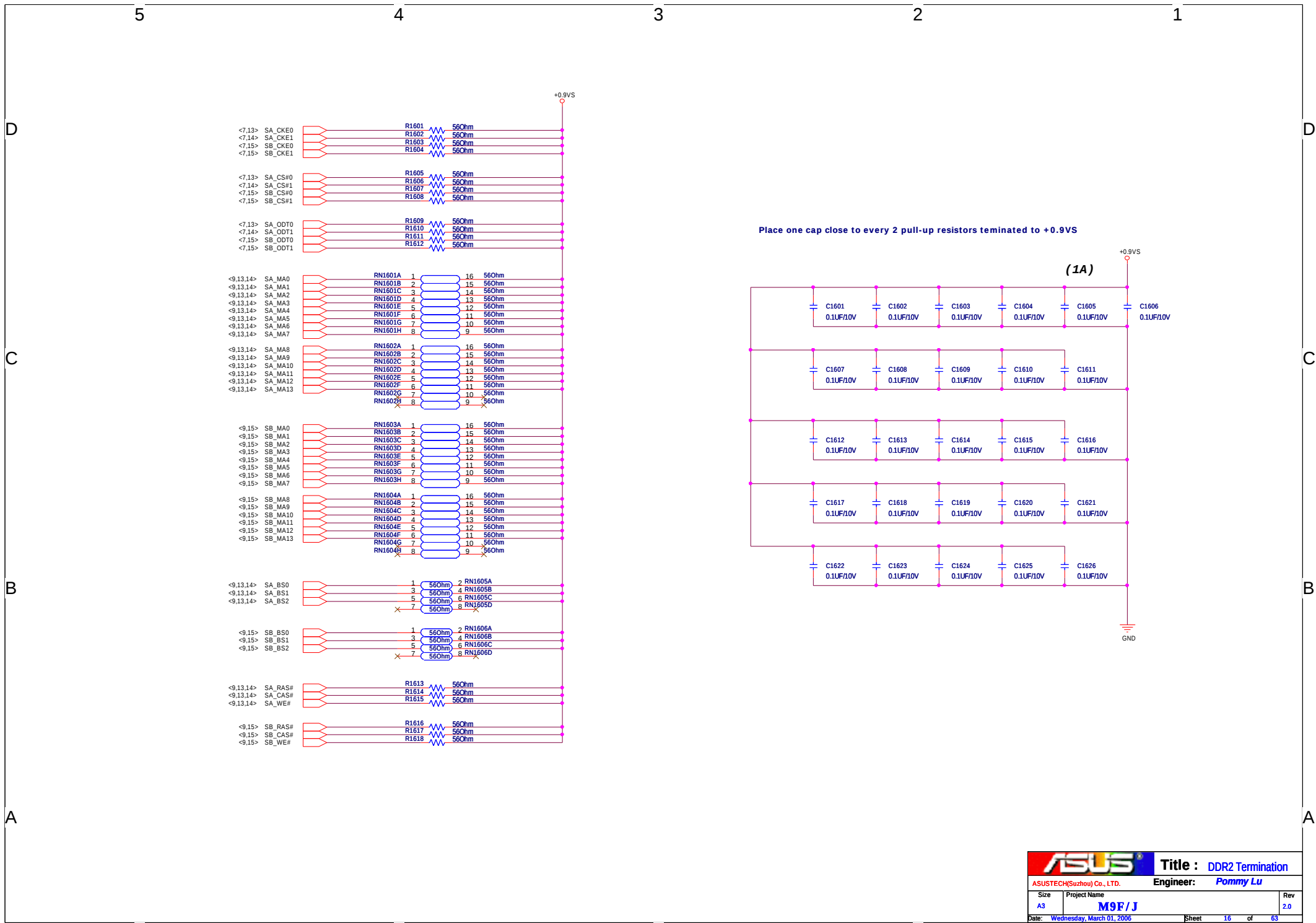
3

2

1

P/N: 12G025122007





5

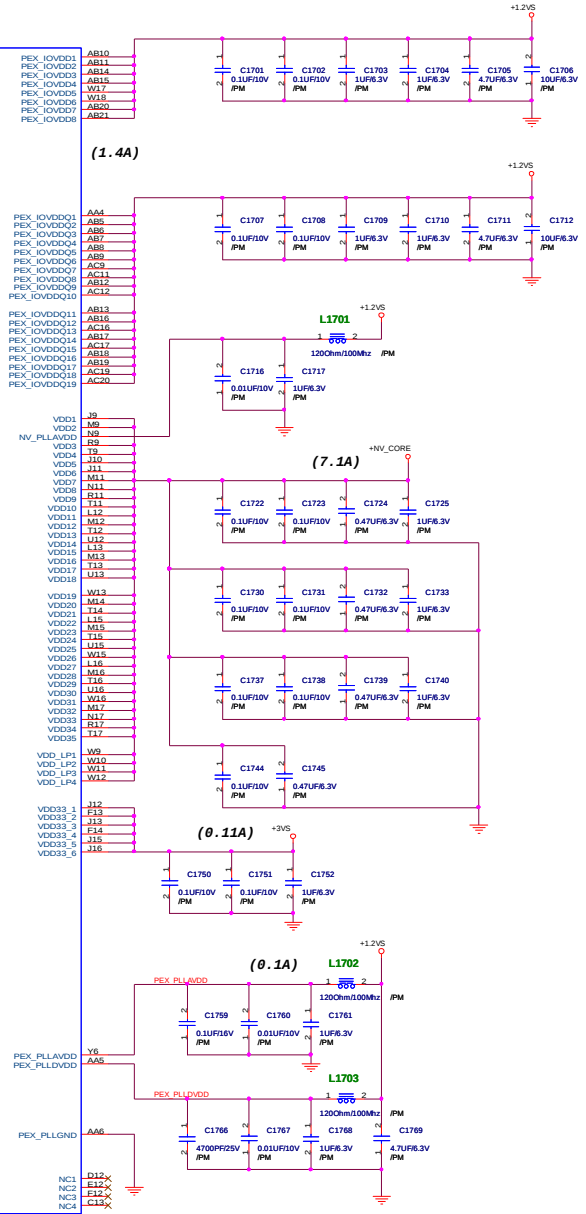
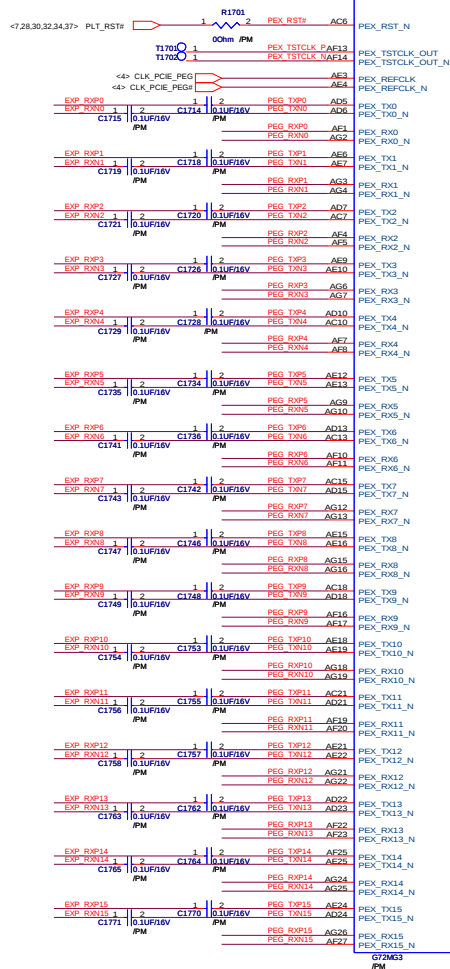
4

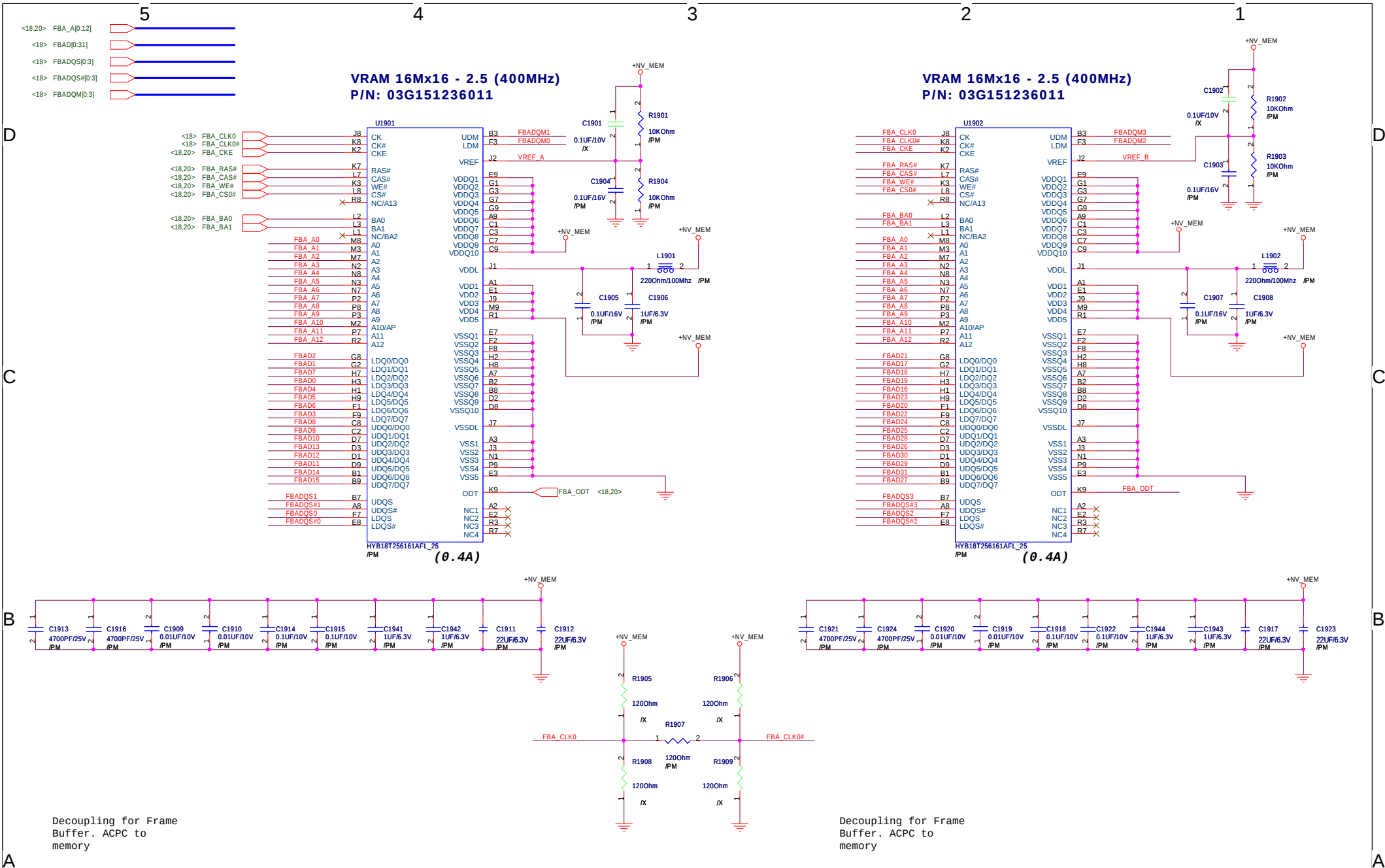
3

2

1

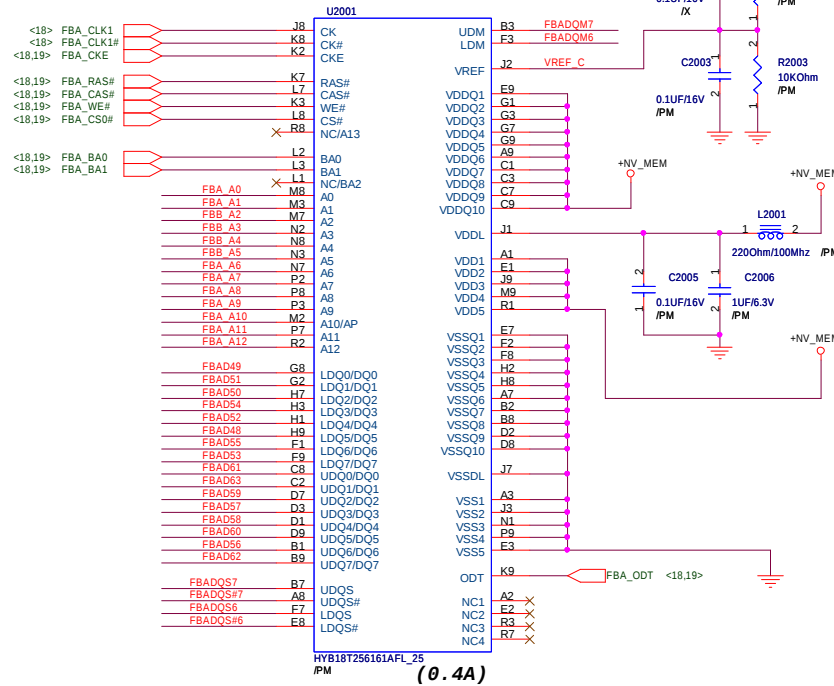
G72M-V P/N: 02G190009311



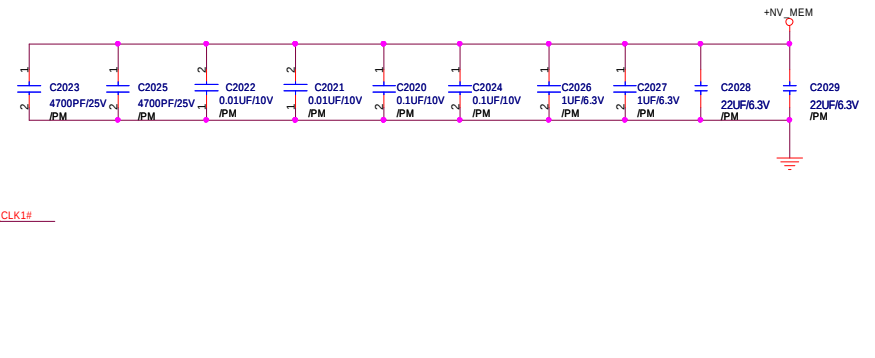
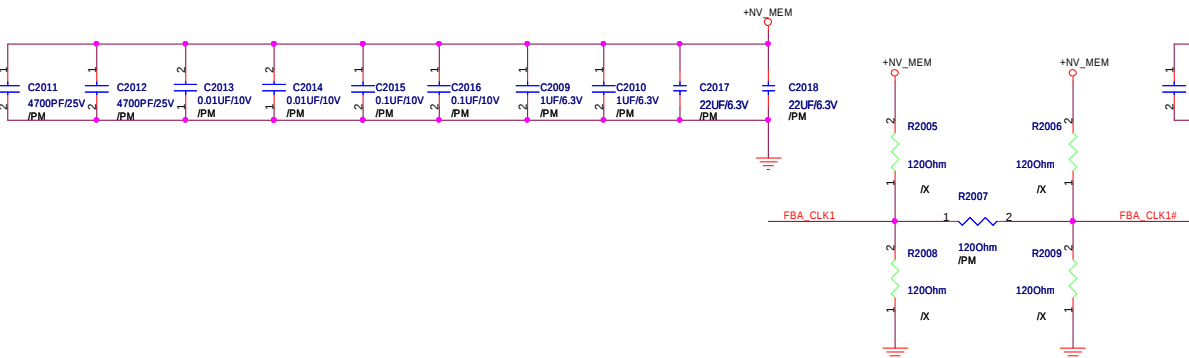
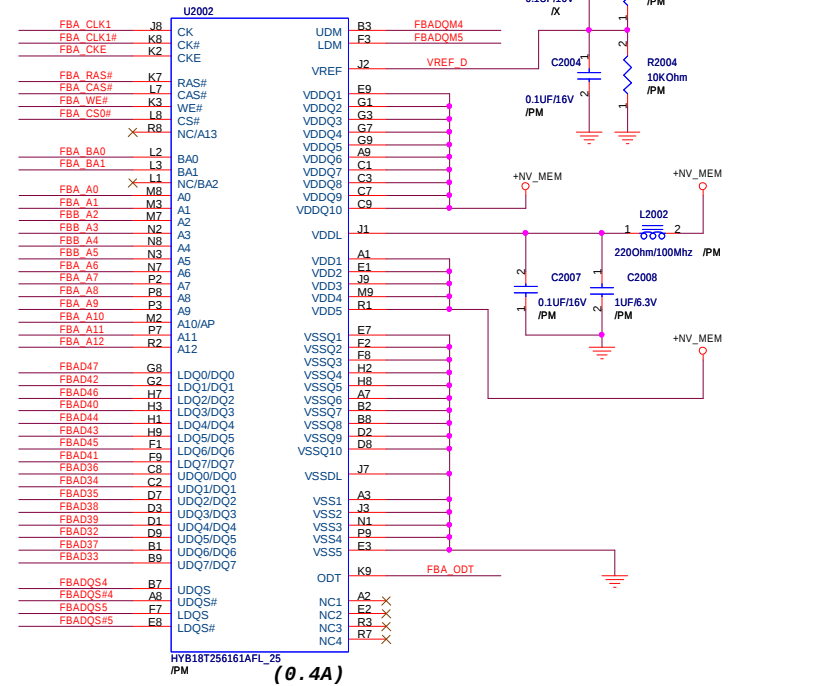


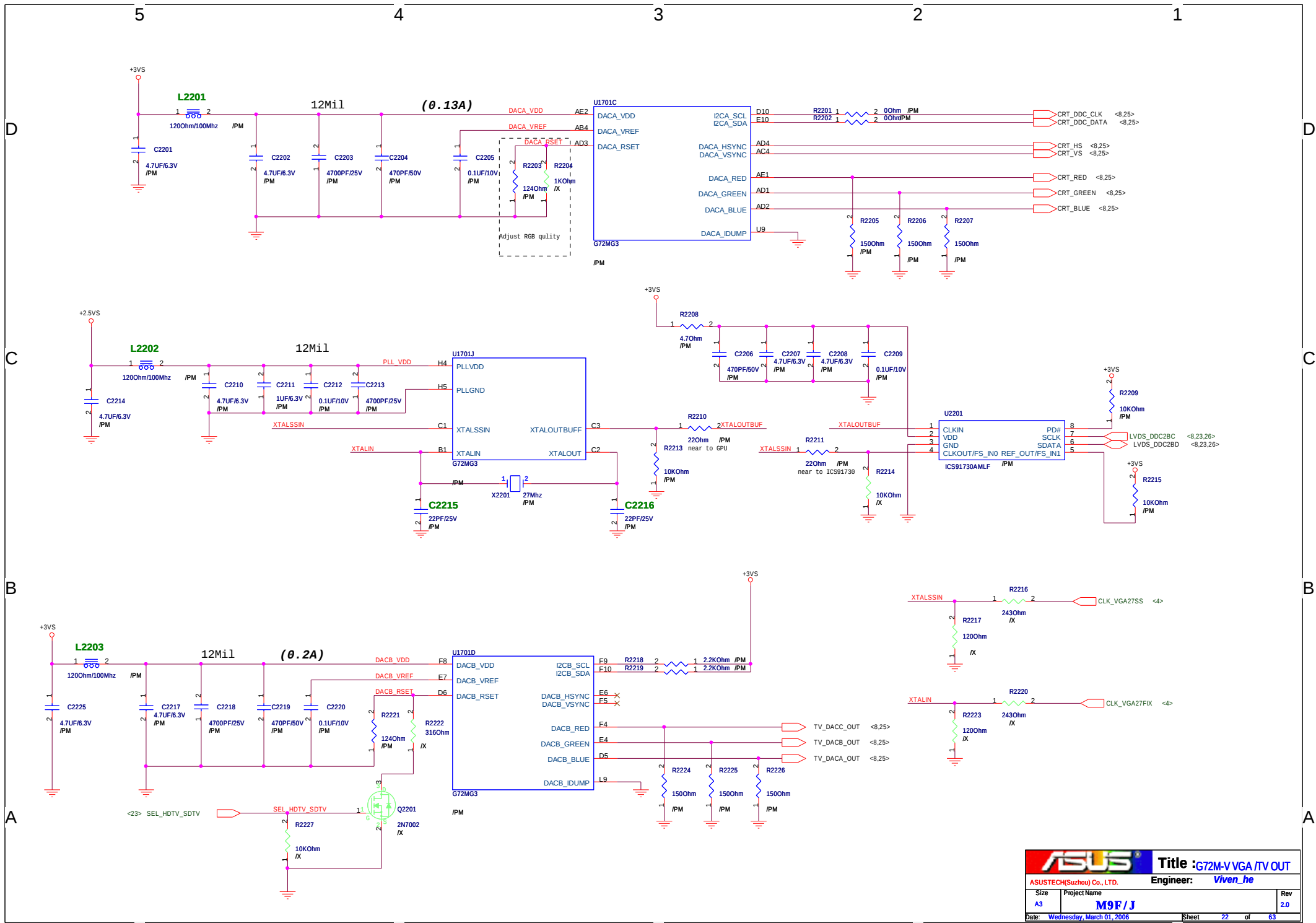
<18,19> FBA_A[0:12]
 <18> FBAD[32:63]
 <18> FBADQS[4:7]
 <18> FBB_A[2:5]
 <18> FBADQS[4:7]
 <18> FBADQM[4:7]

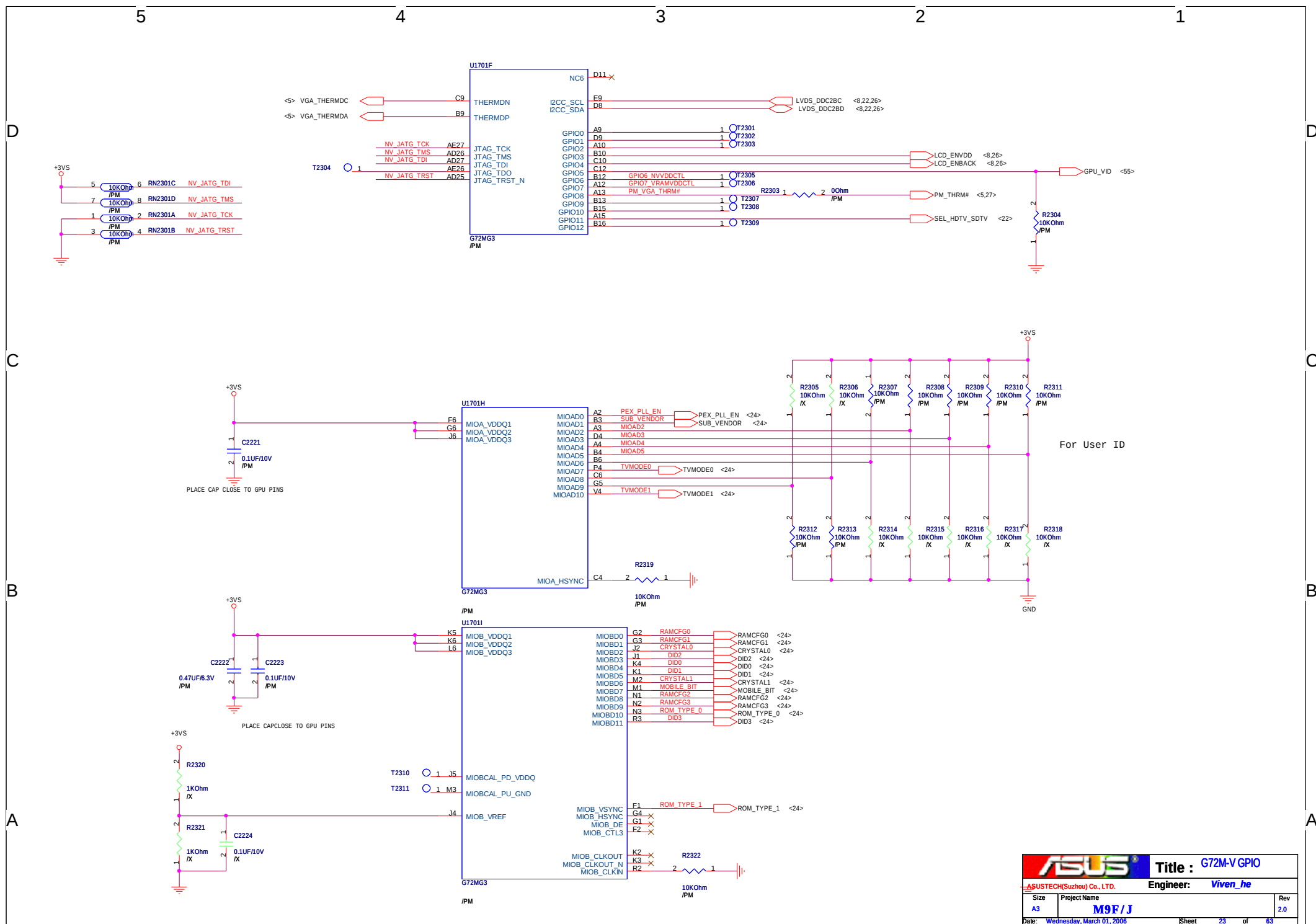
VRAM 16Mx16 - 2.5 (400MHz)
P/N: 03G151236011

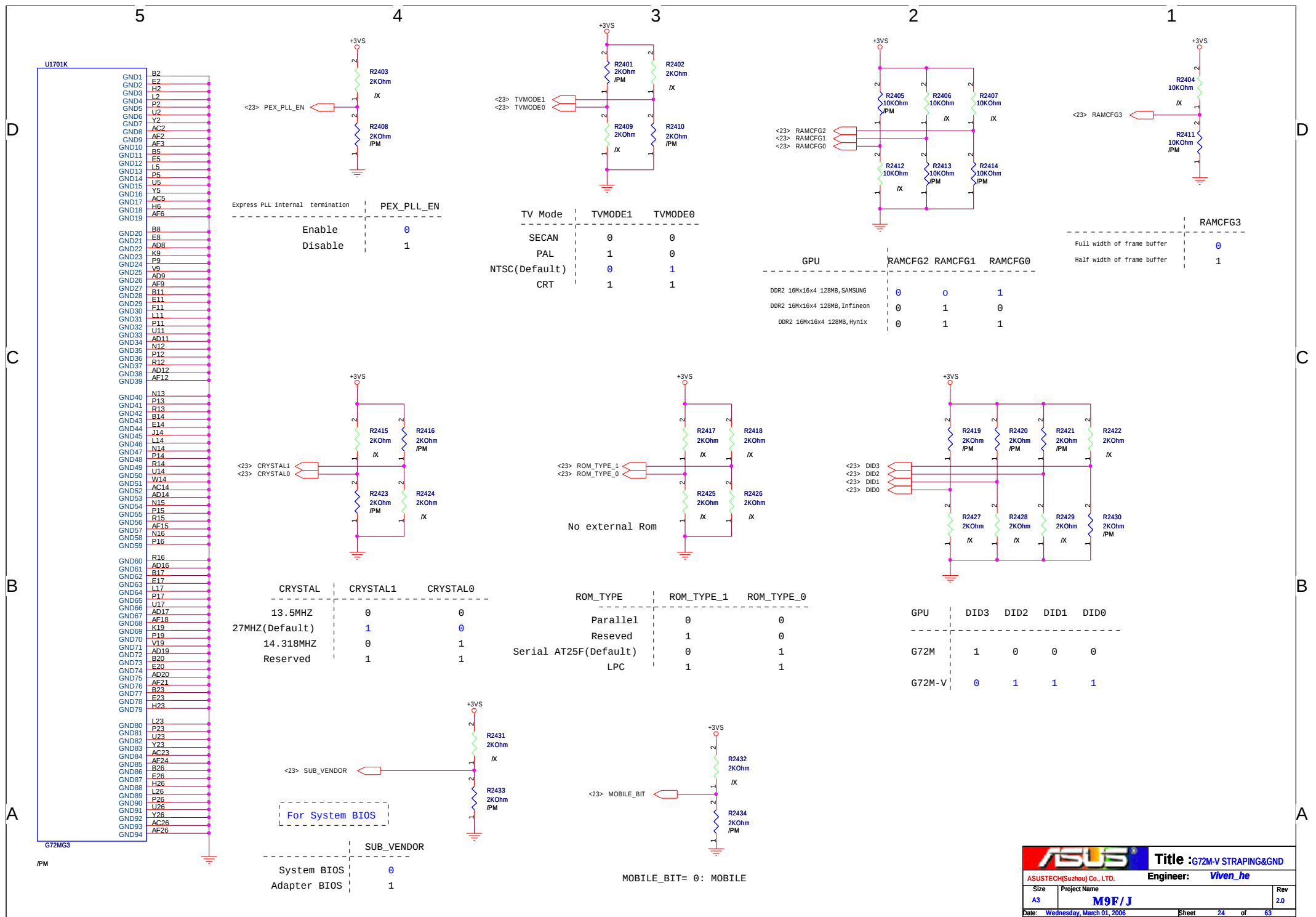


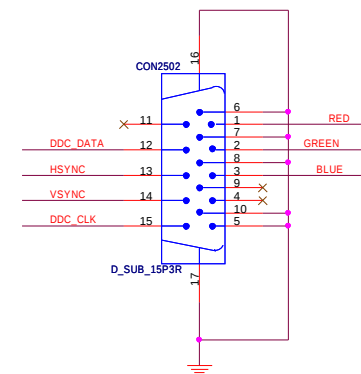
VRAM 16Mx16 - 2.5 (400MHz)
P/N: 03G151236011

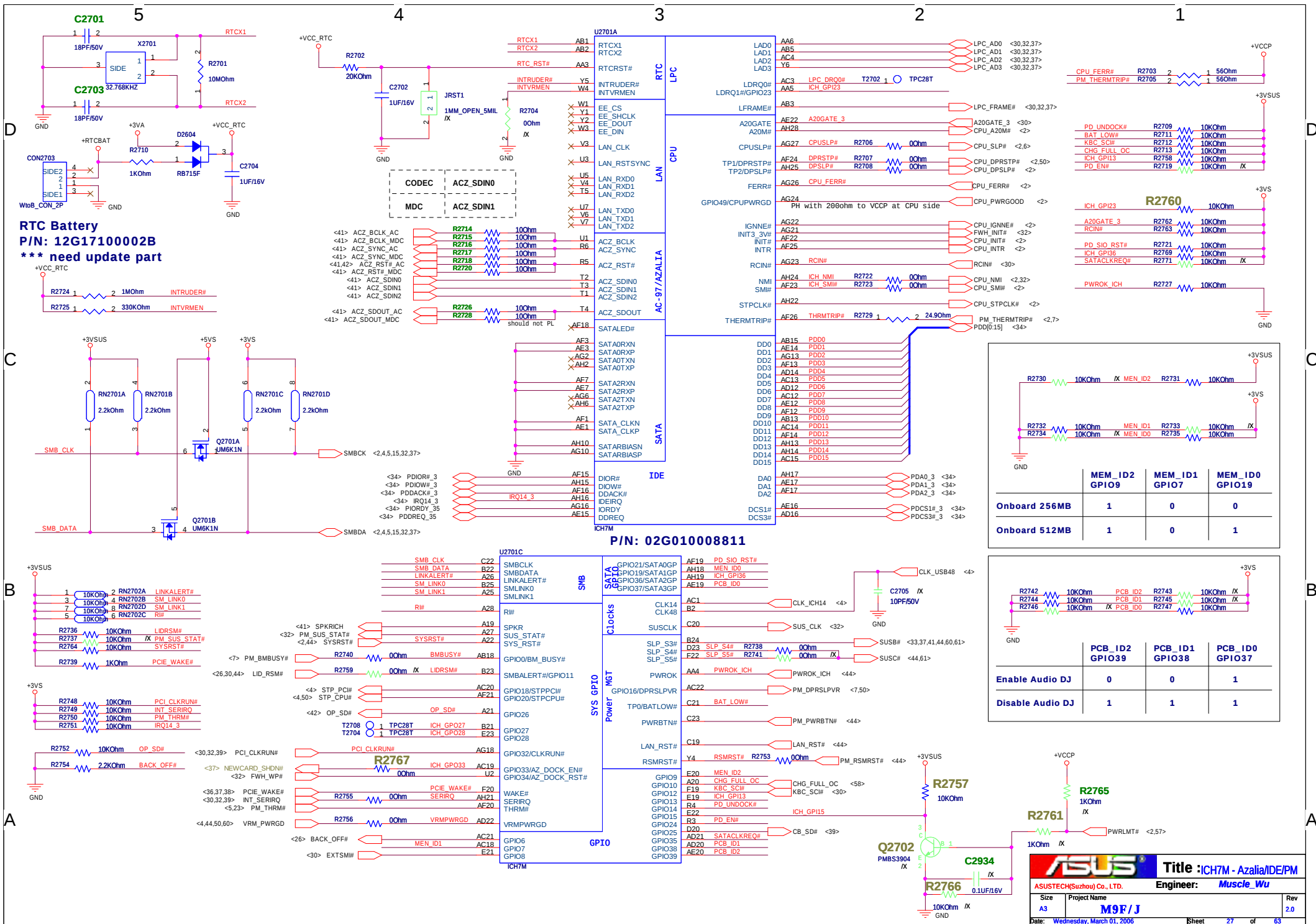












5

4

3

2

1

D

D

C

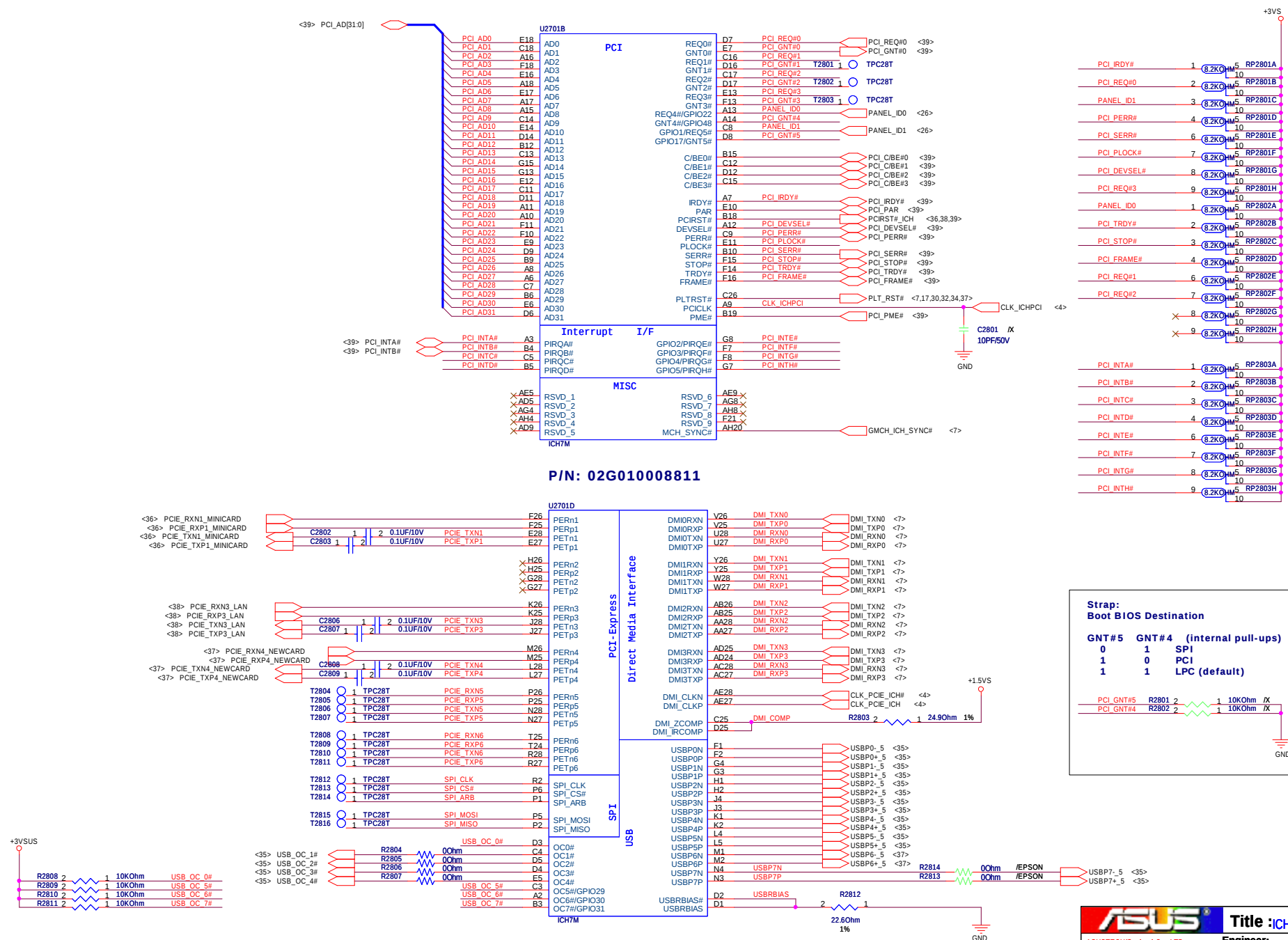
C

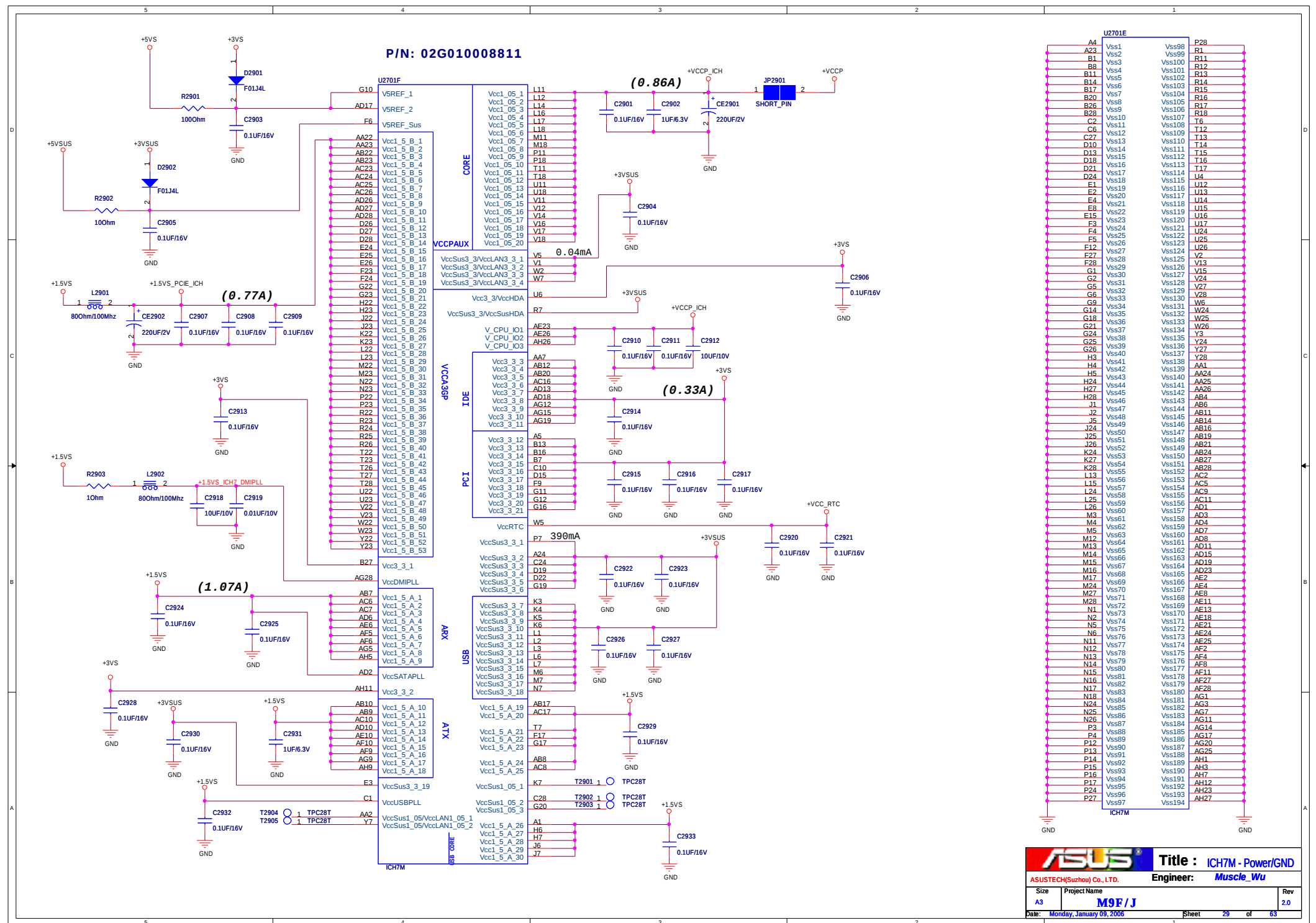
B

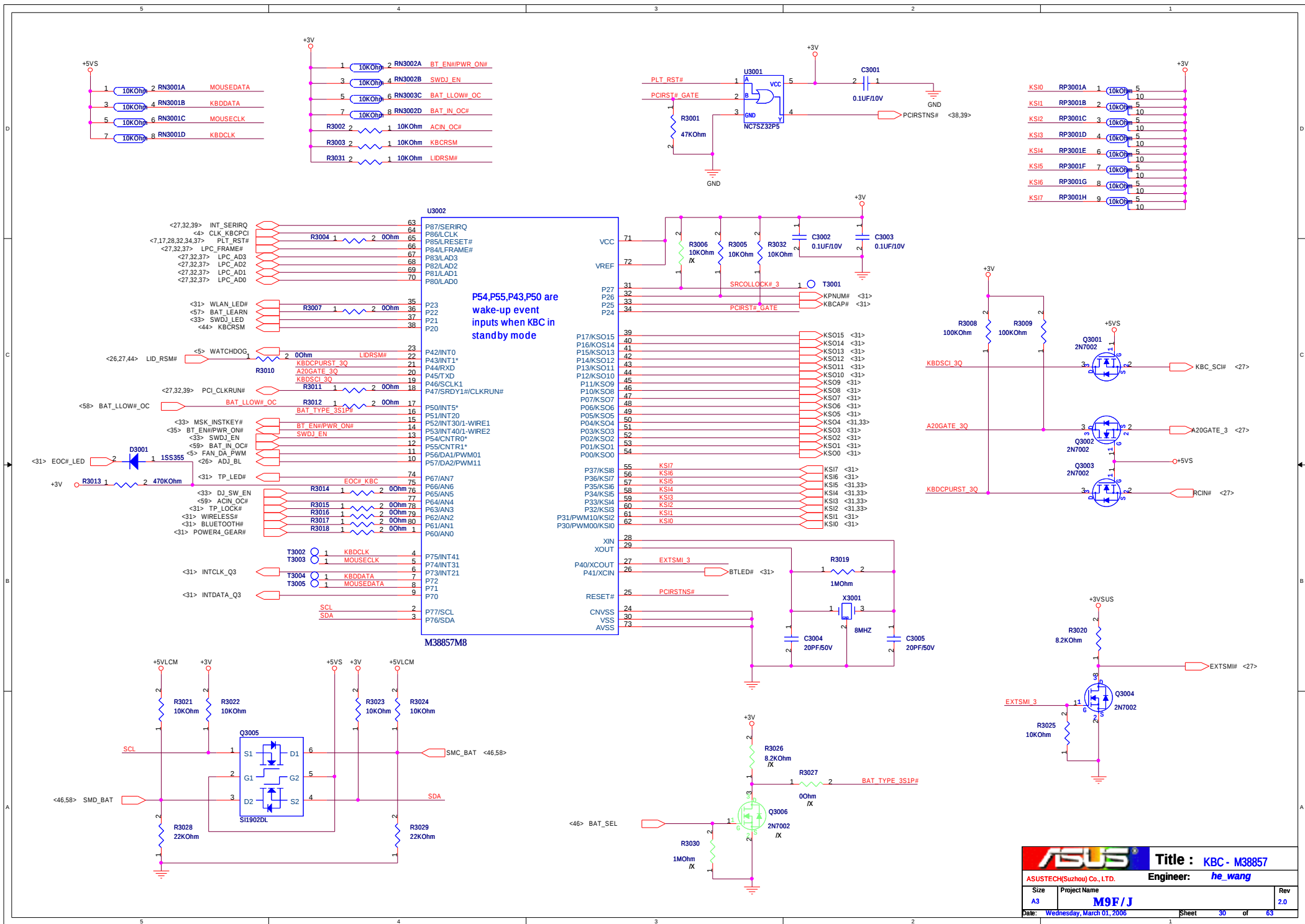
B

A

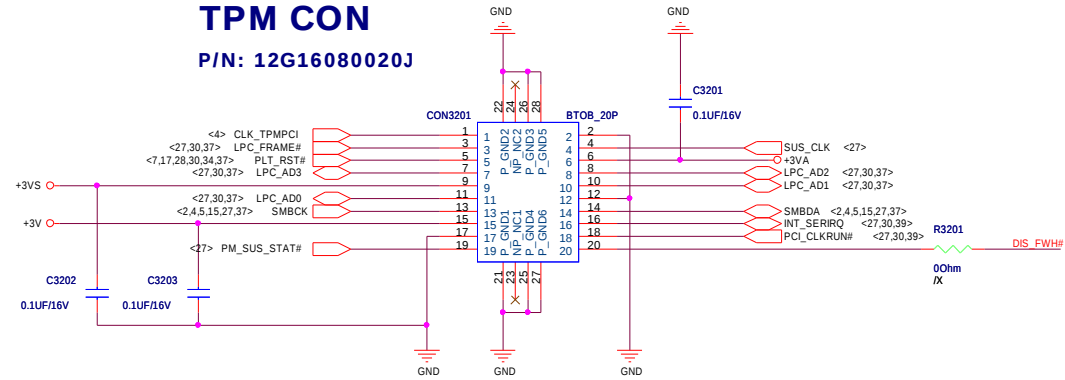
A



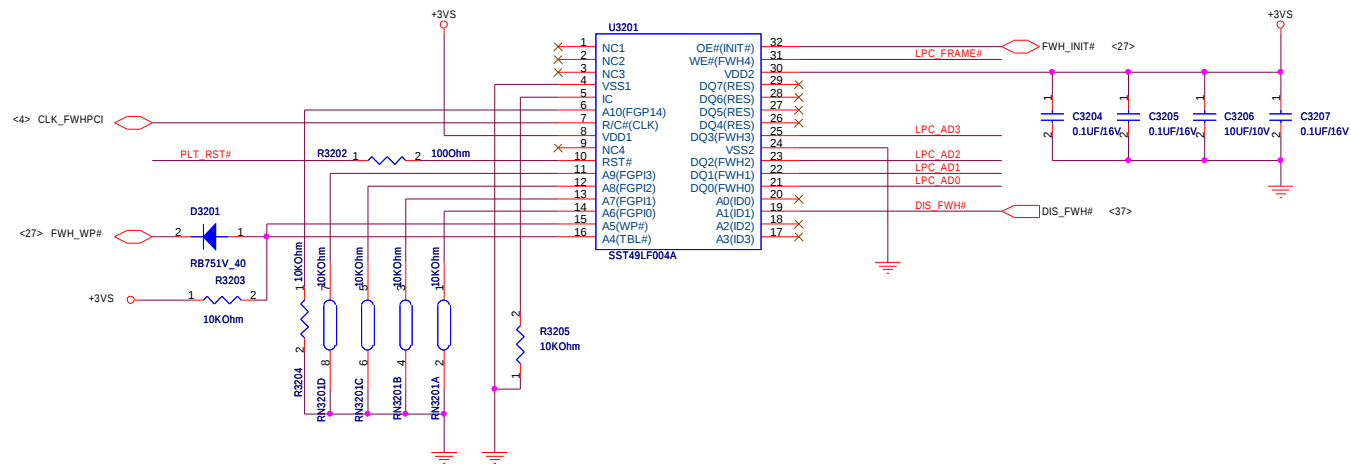




P/N: 12G16080020J

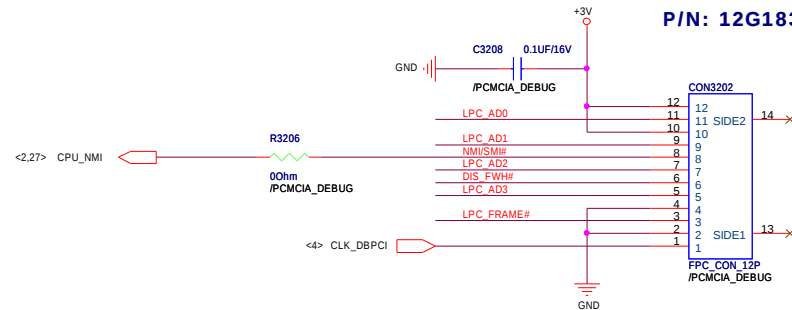


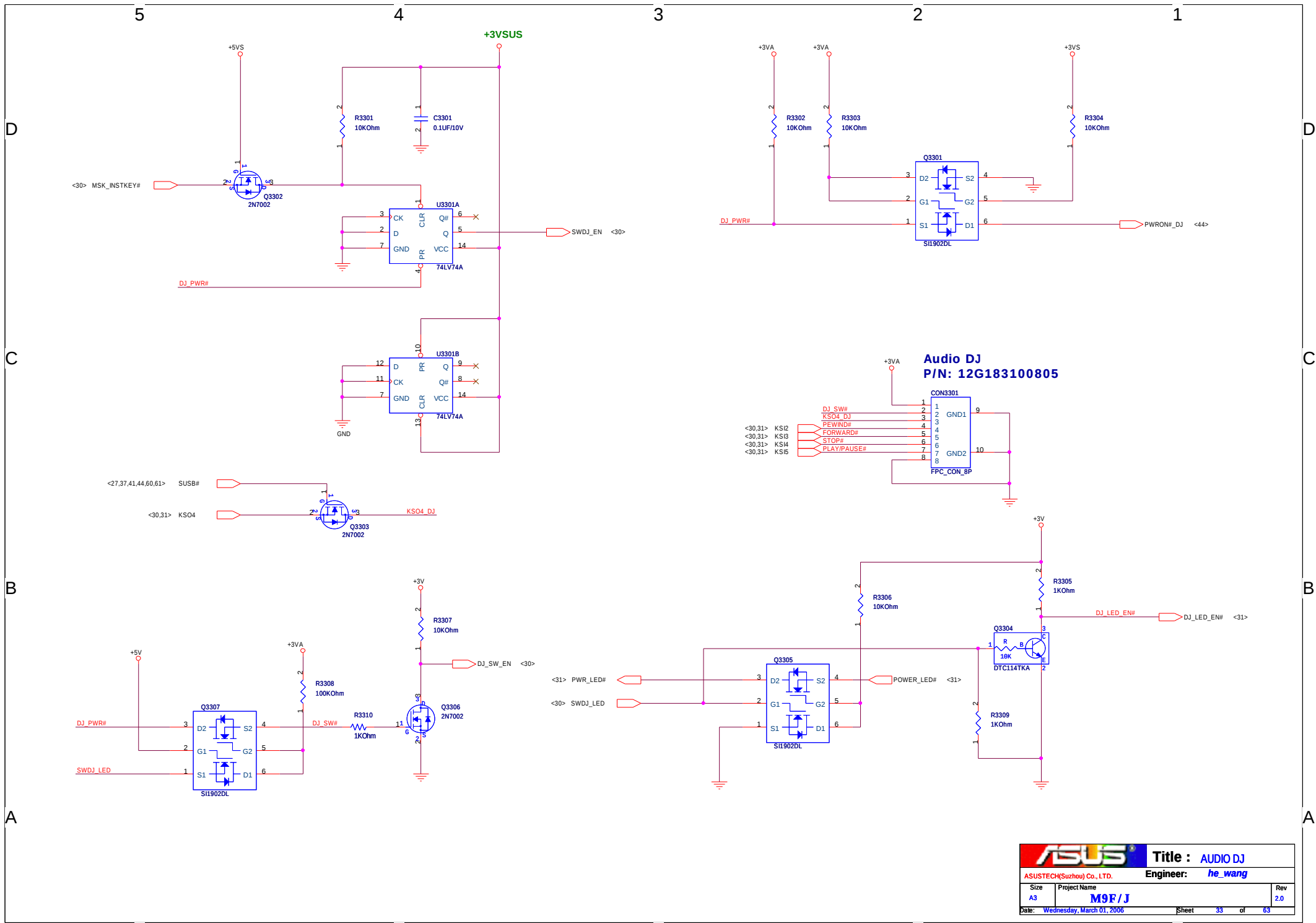
FWH

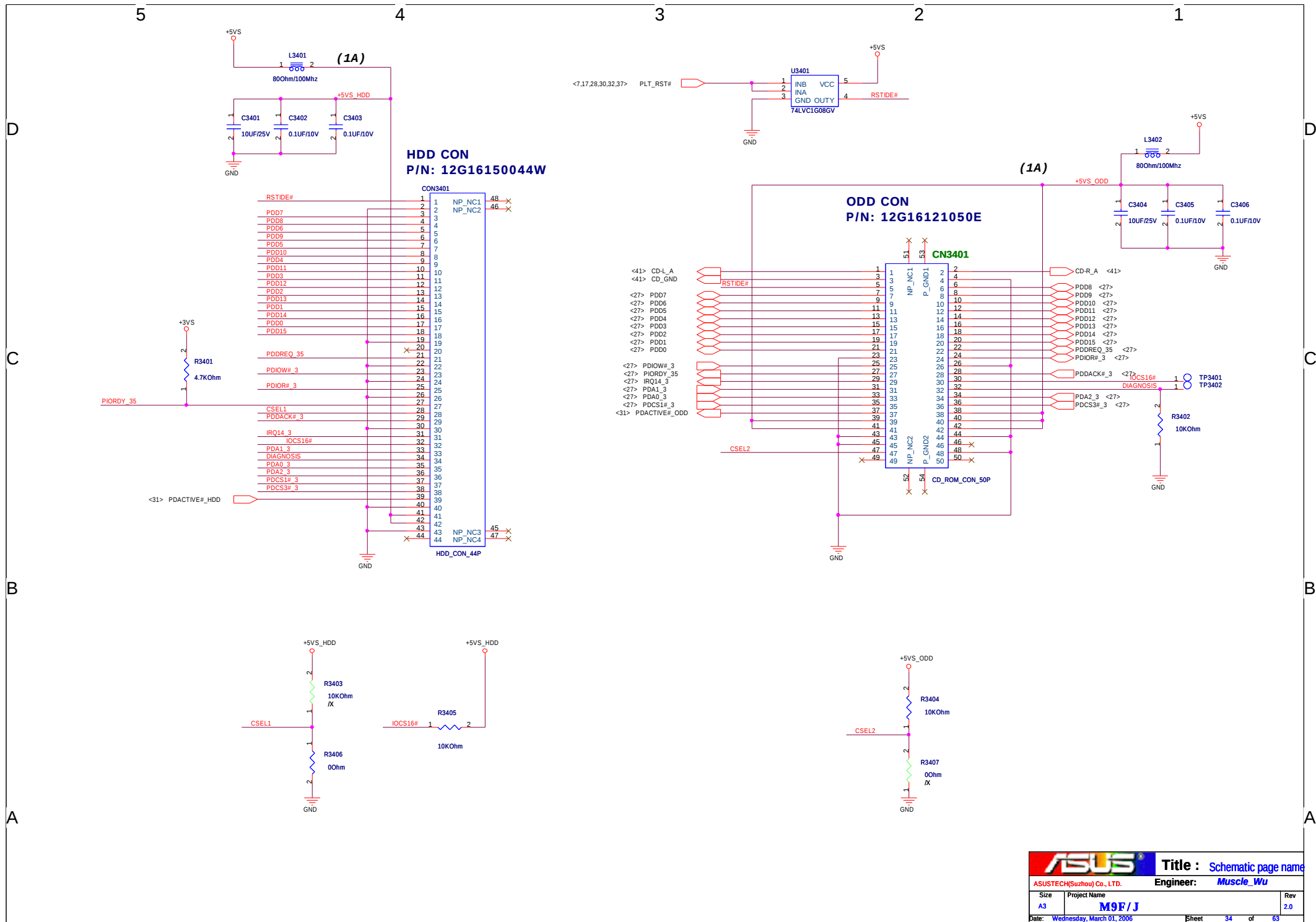


DEBUG PORT (CONNECT WITH FFC)

P/N: 12G183101206







5

4

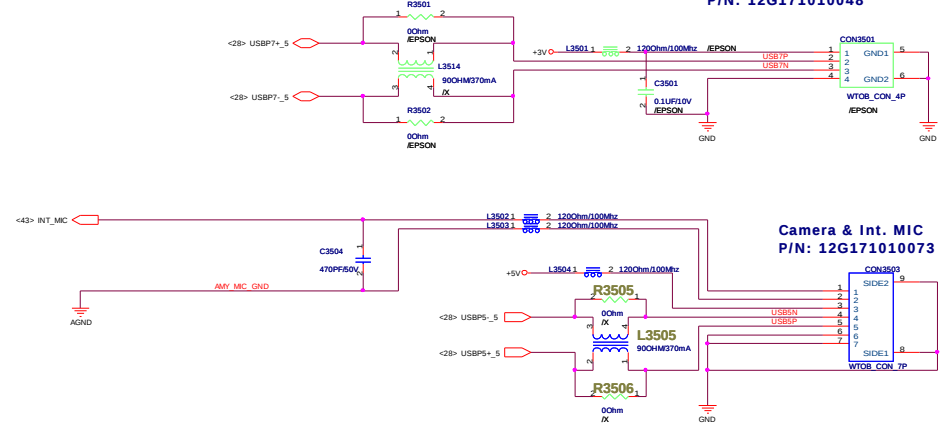
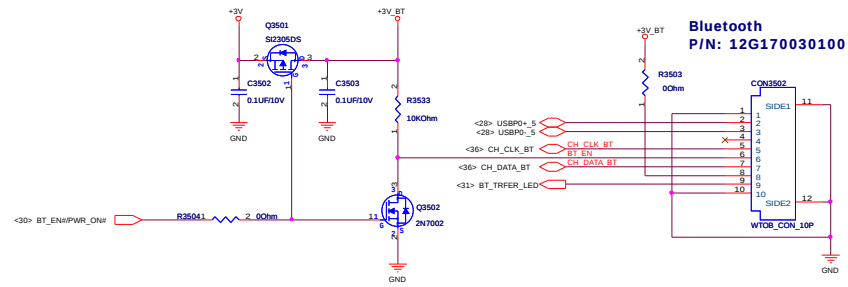
3

2

1

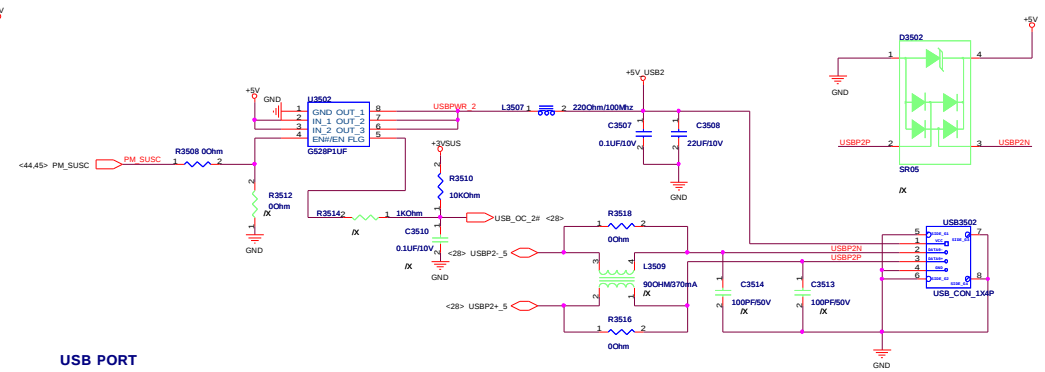
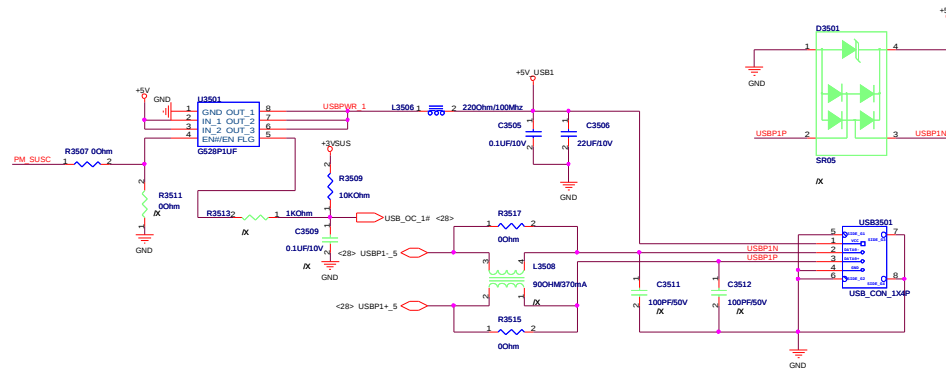
D

D



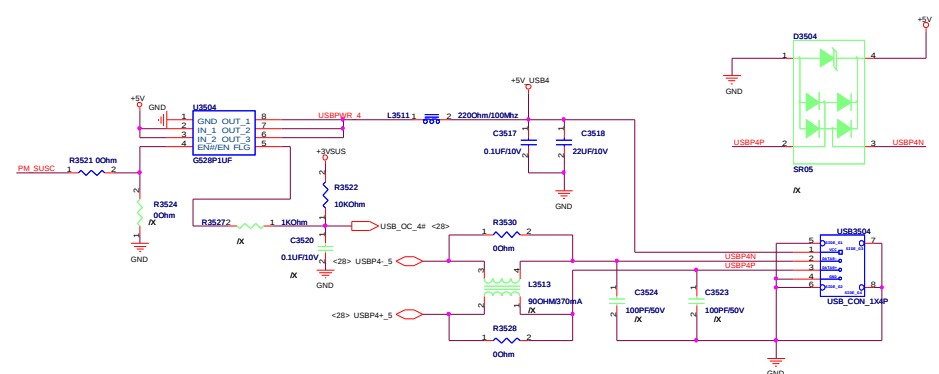
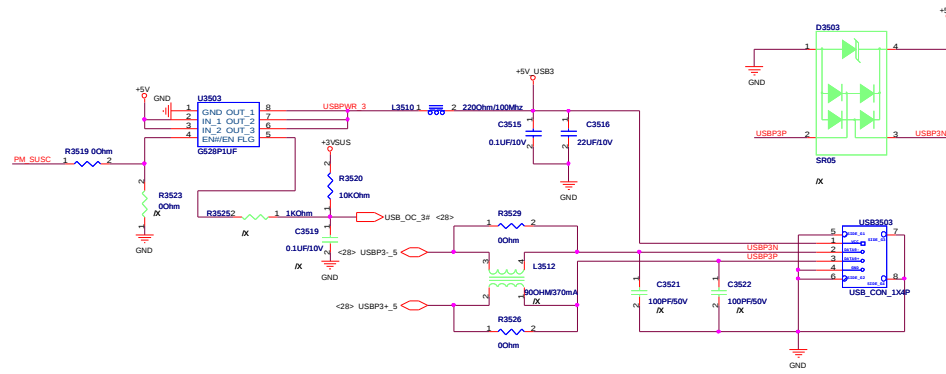
C

C



B

B



A

A

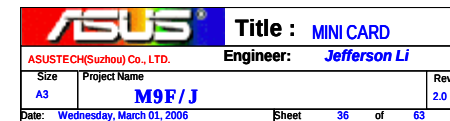
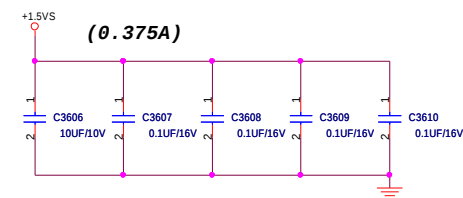
5

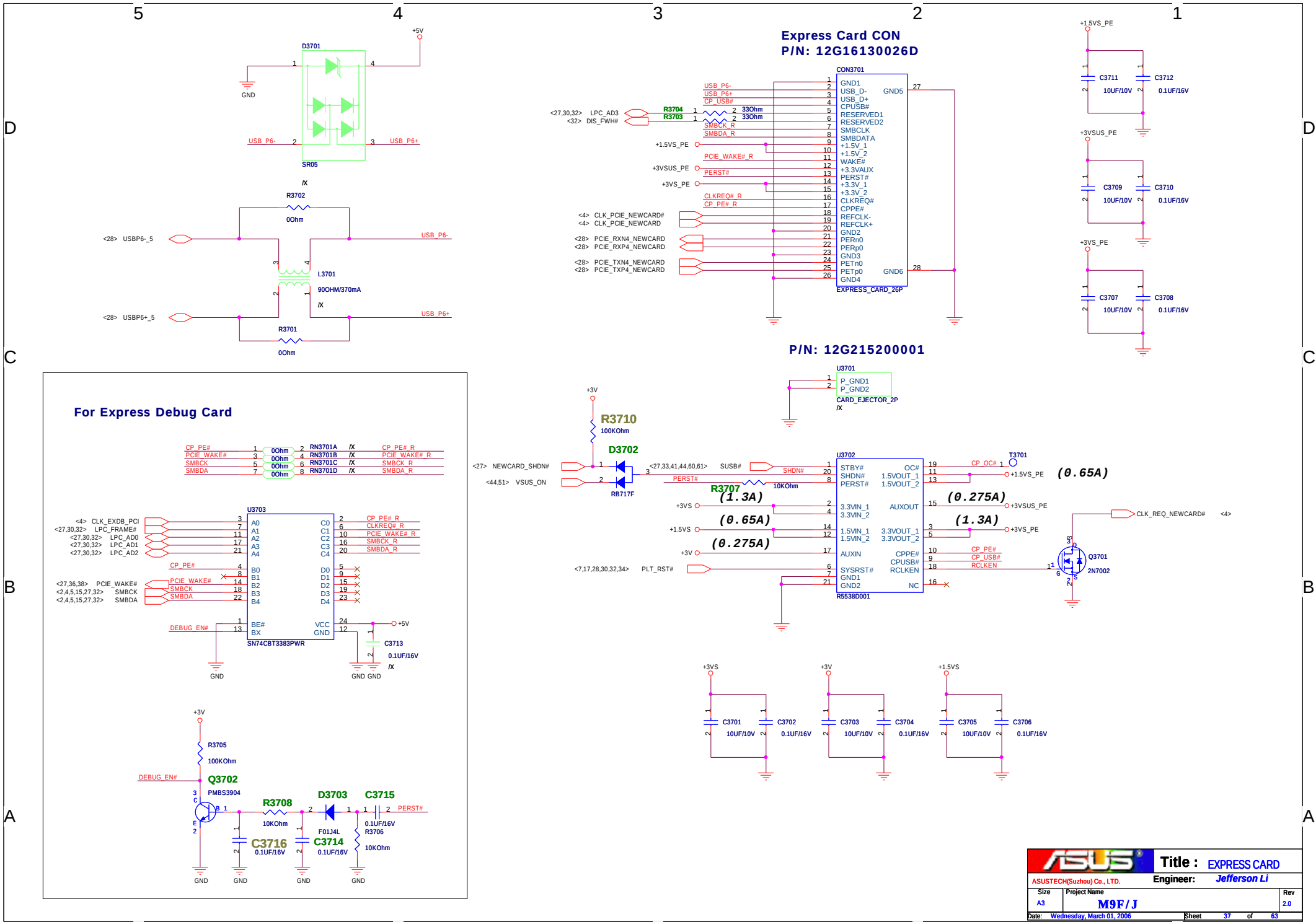
4

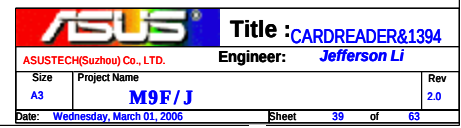
3

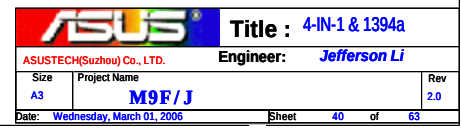
2

1



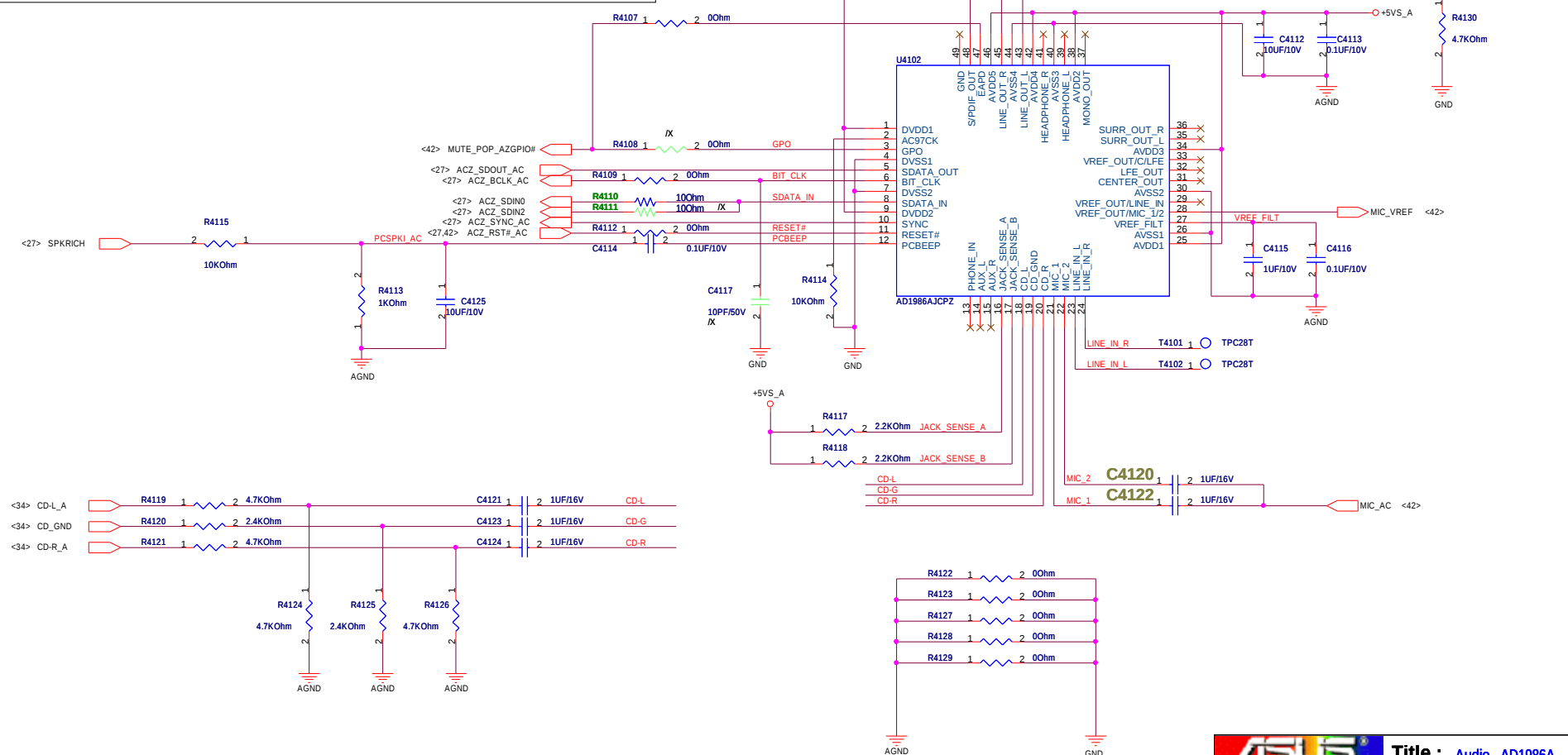
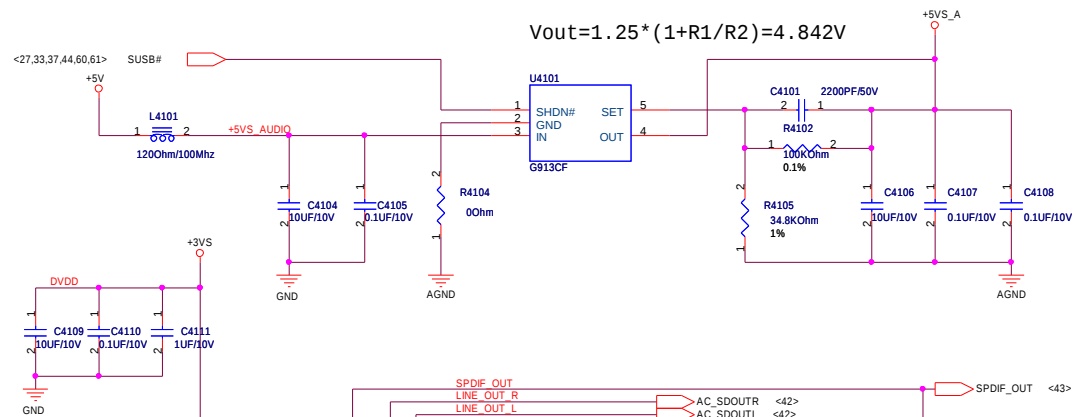
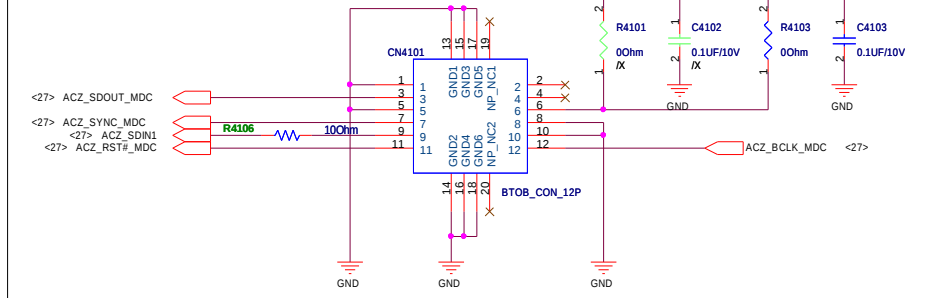


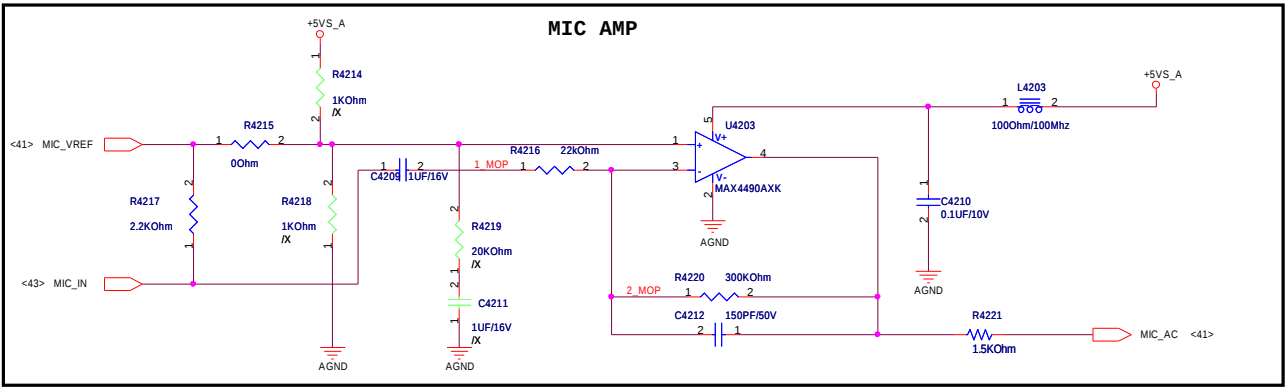
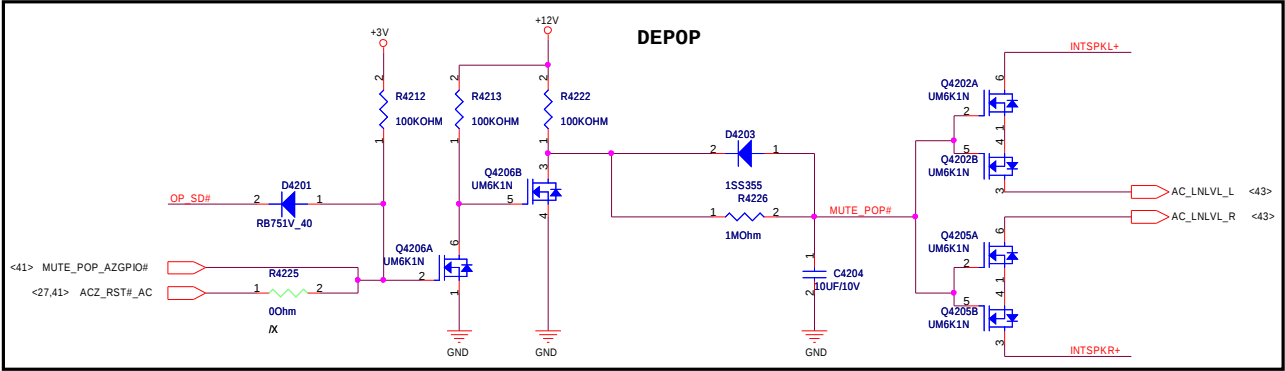
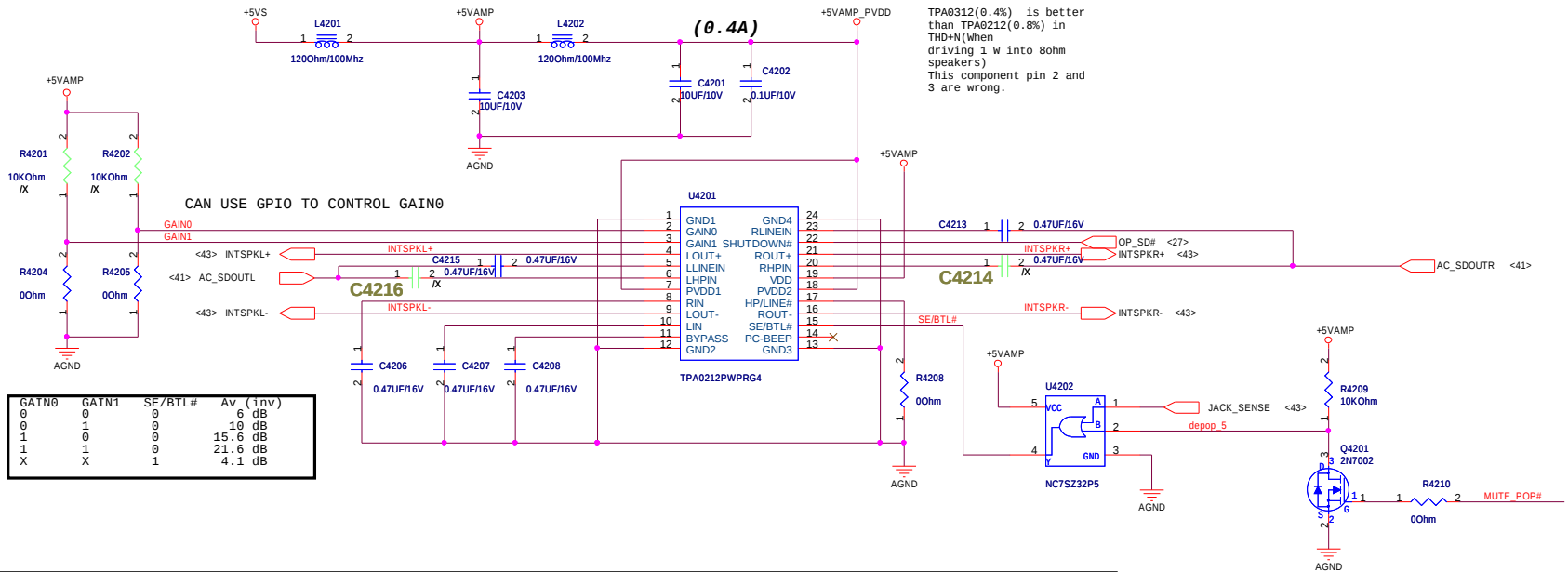


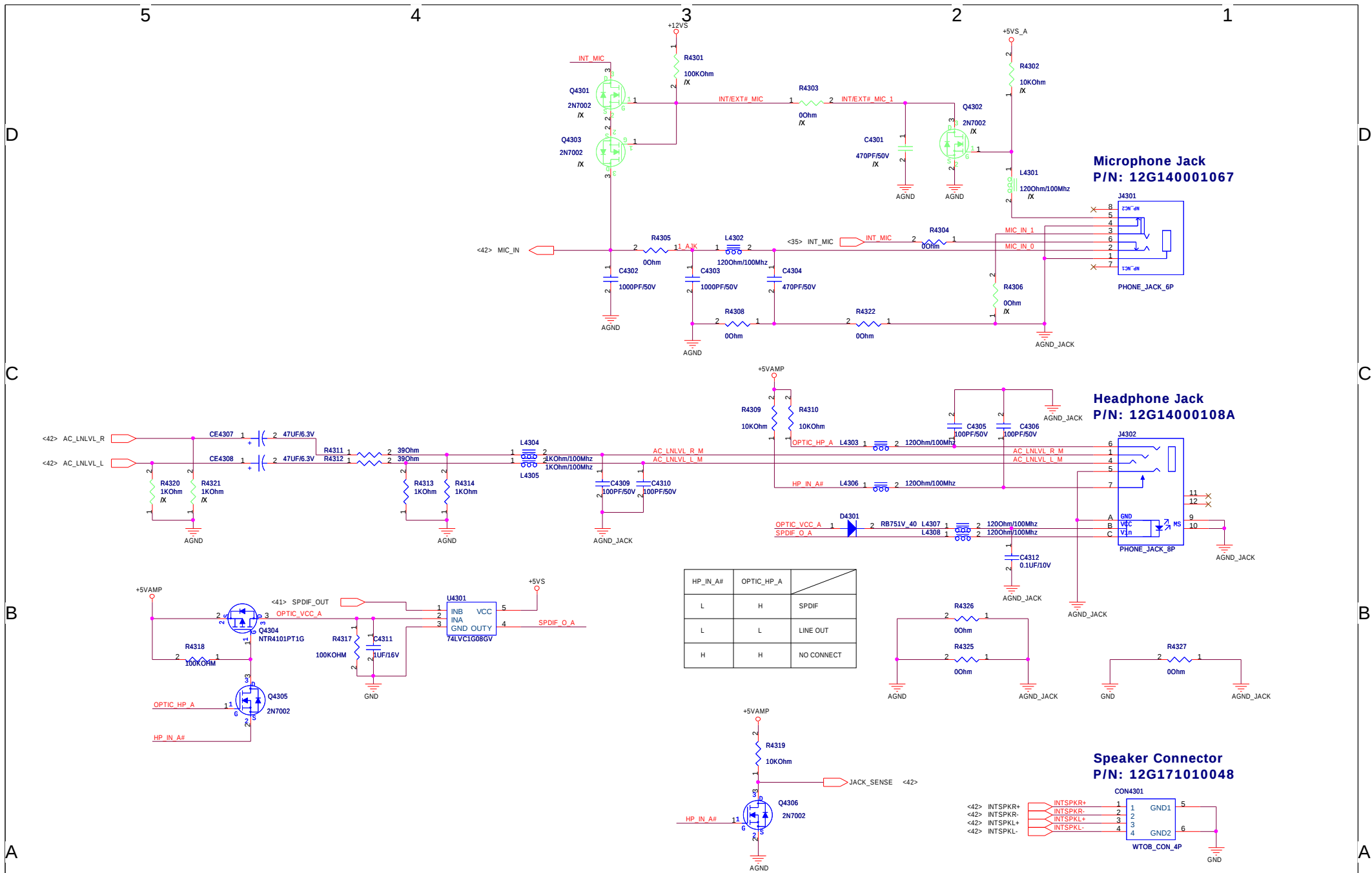


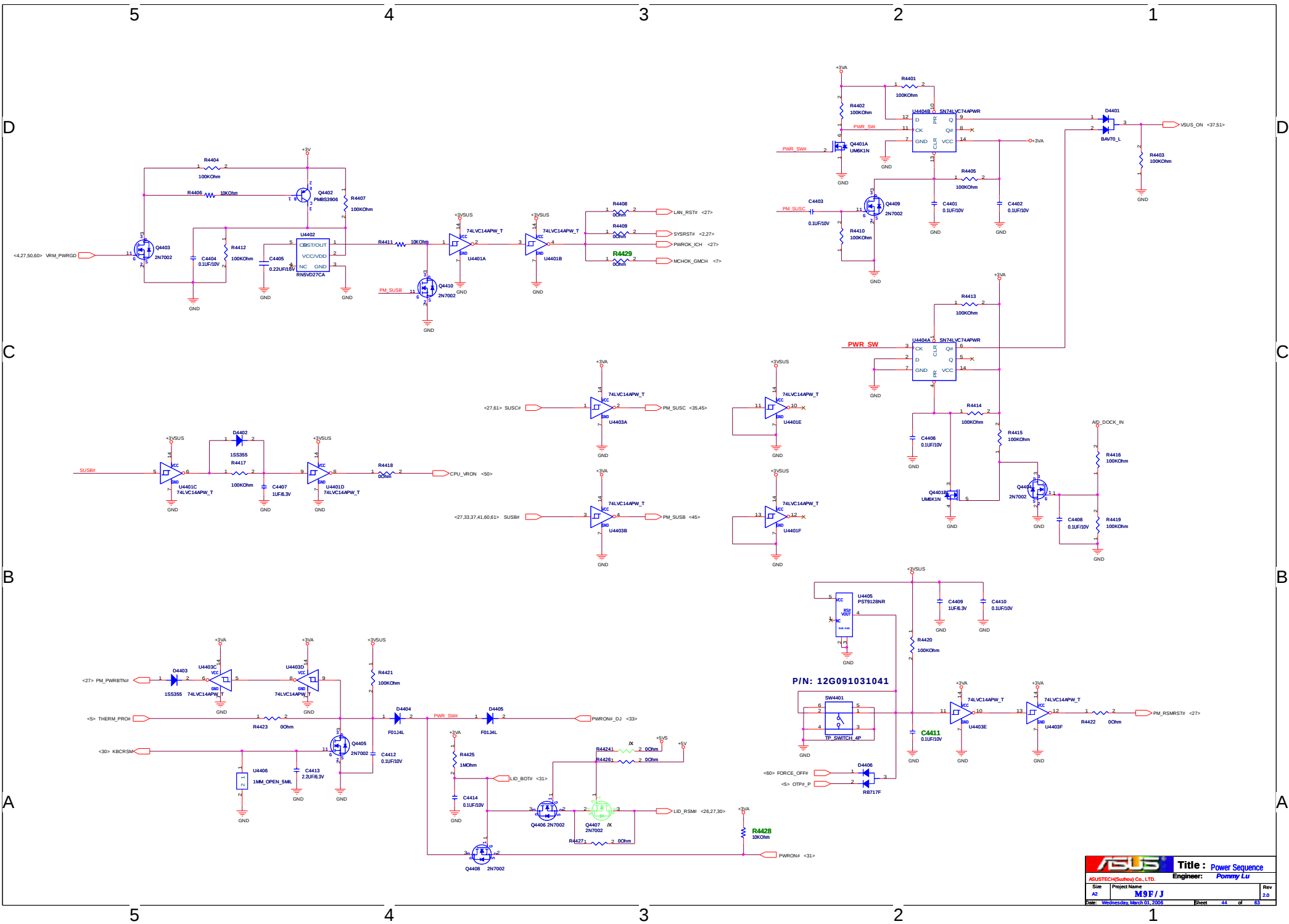
Modem CON

P/N: 12G161200120









5

4

3

2

1

D

C

B

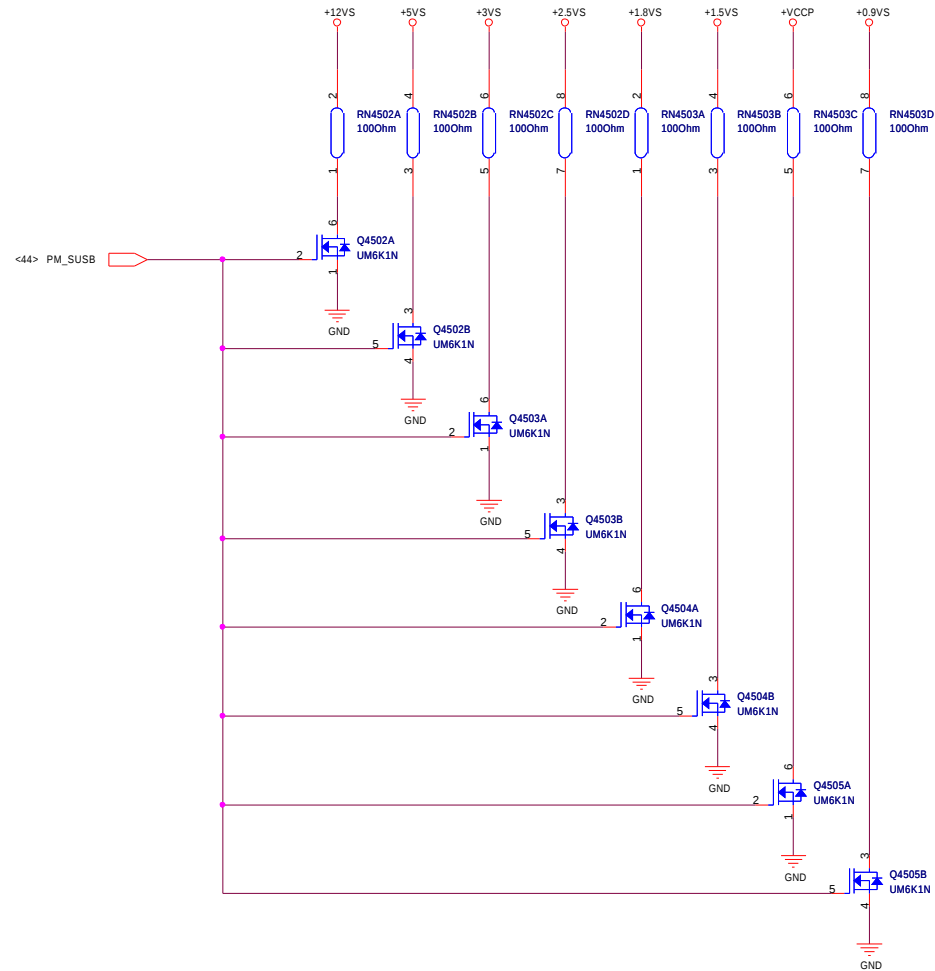
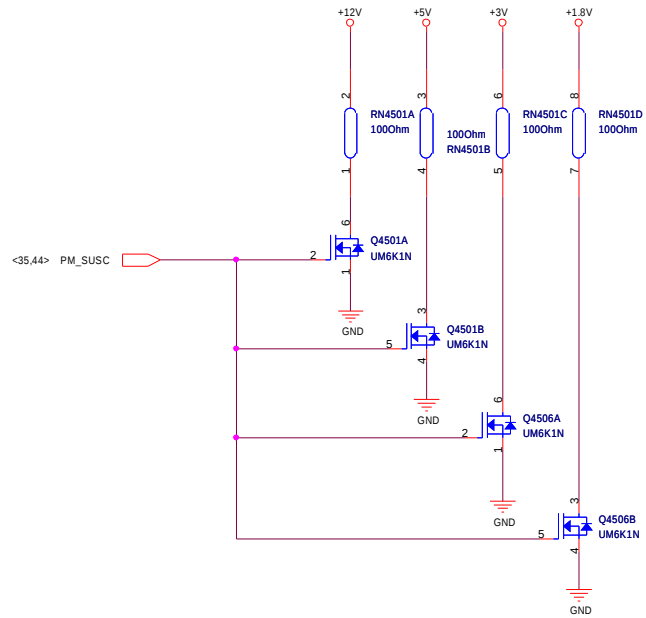
A

D

C

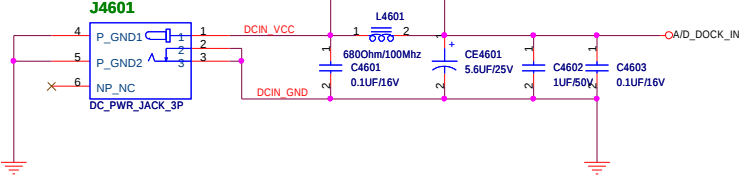
B

A



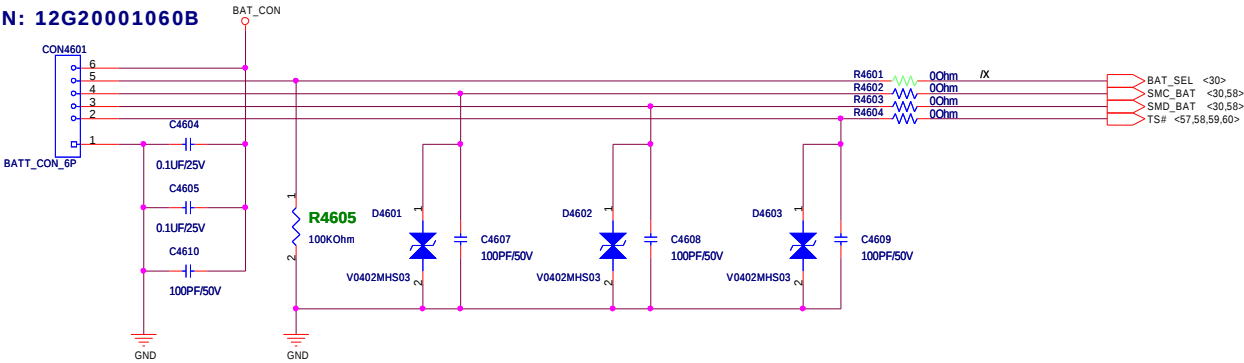
DC-IN

P/N: 12G14530103E



Battery-IN

P/N: 12G20001060B



5

4

3

2

1

A

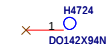
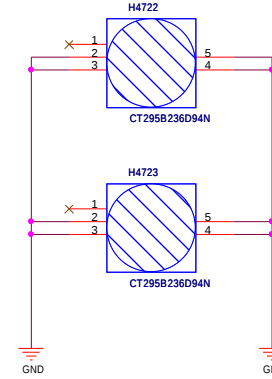
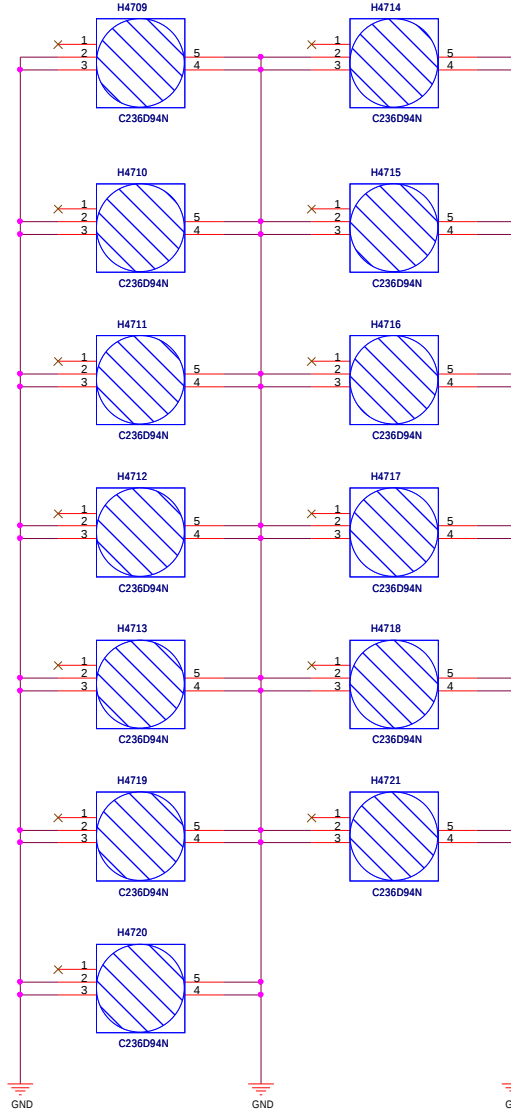
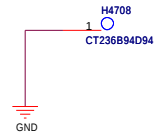
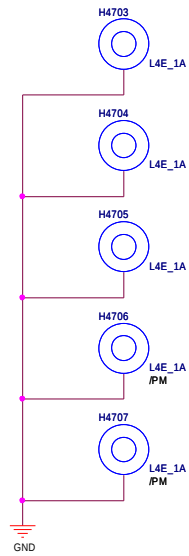
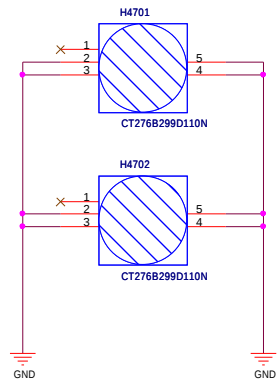
B

E

F

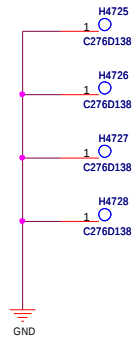
J

L

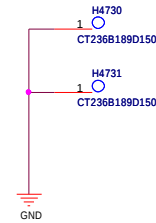


O

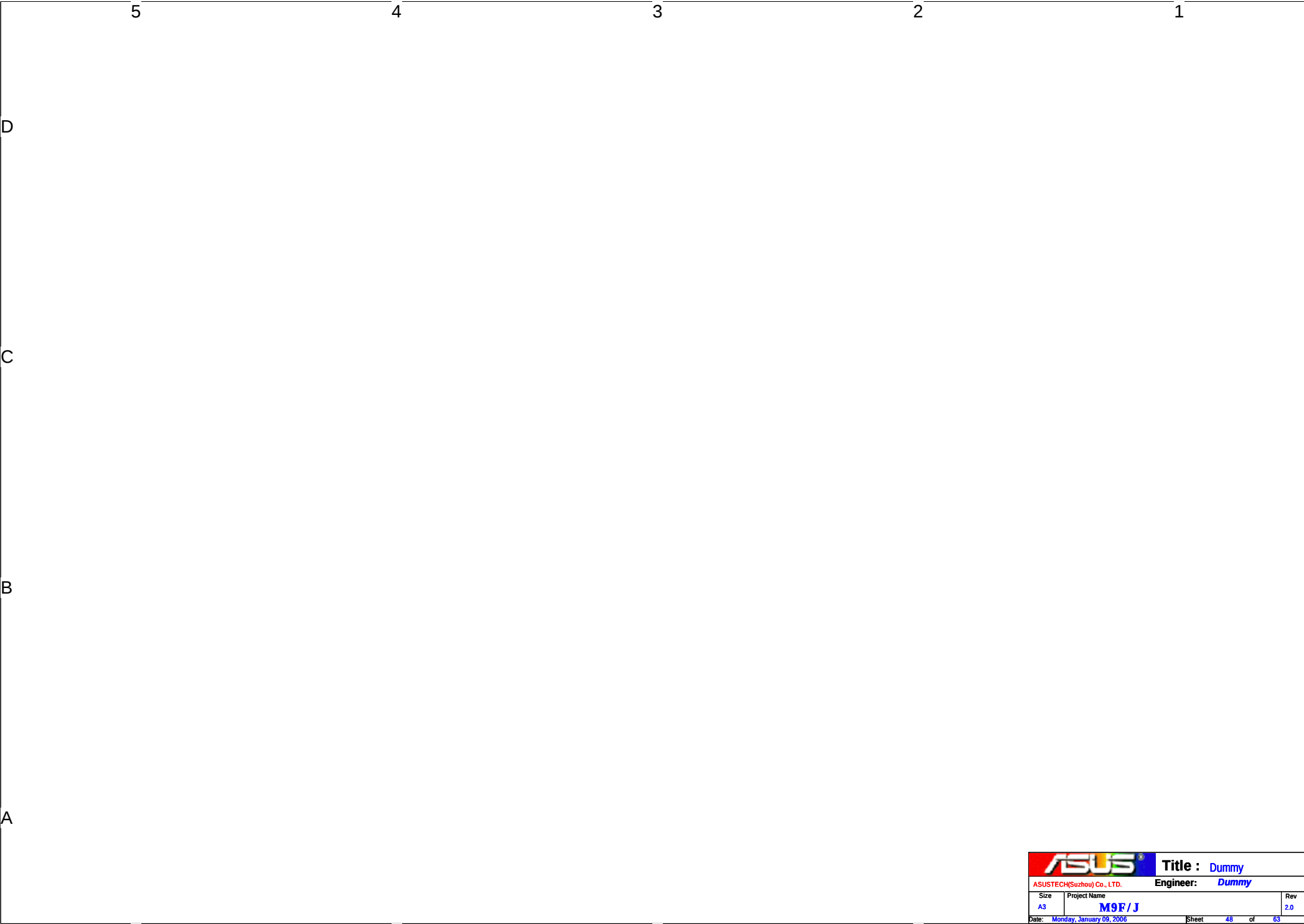
CPU Heat Sink Bracket Holes

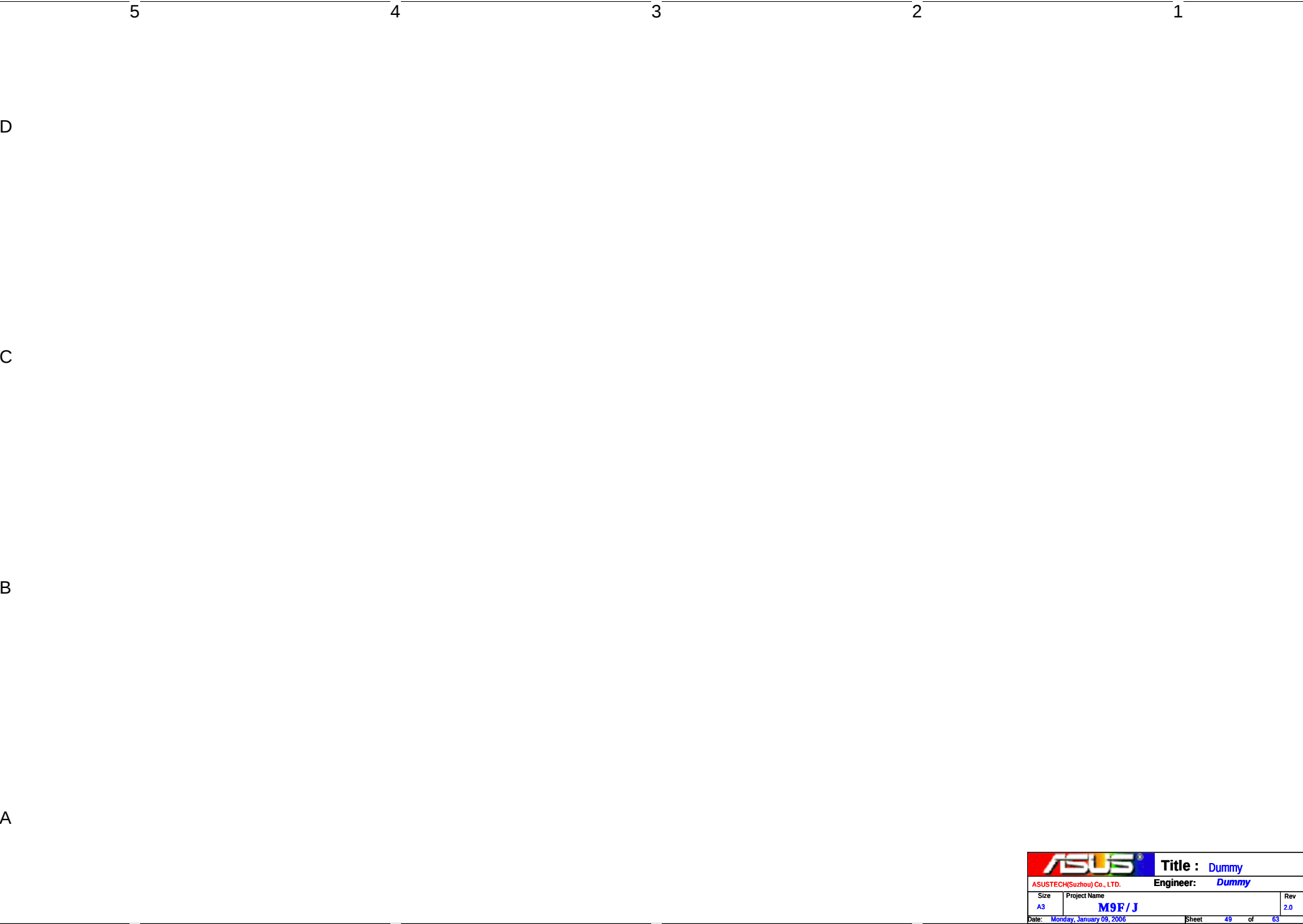


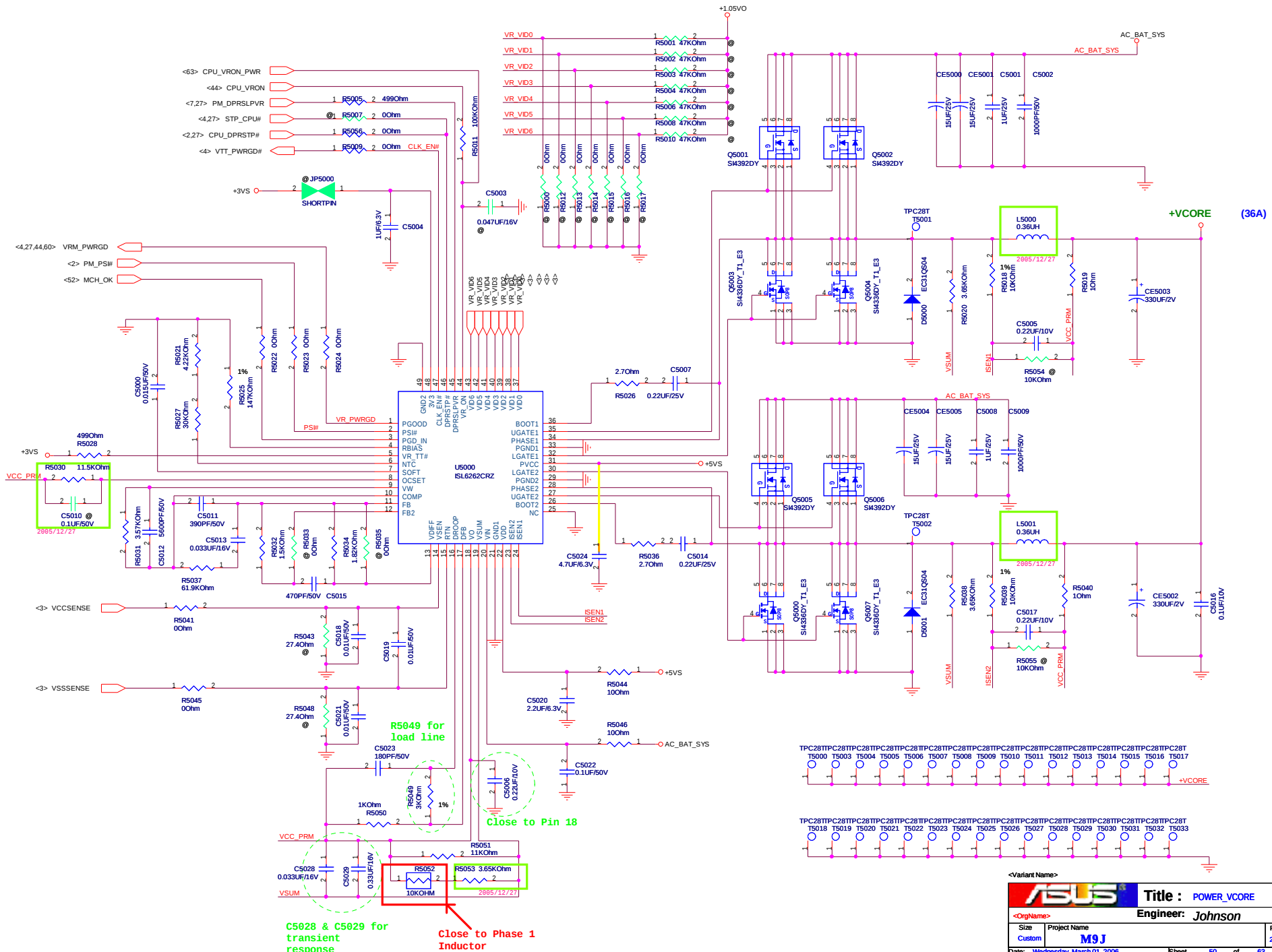
Mini Card Latch Nuts



ASUS		Title : Screw Hole	
ASUSTECH(Suzhou) Co., LTD.		Engineer: Pommy Lu	
Size	Project Name	Rev	
A3	M9F/J	2.0	
Date: Thursday, February 23, 2006		Sheet	47 of 63

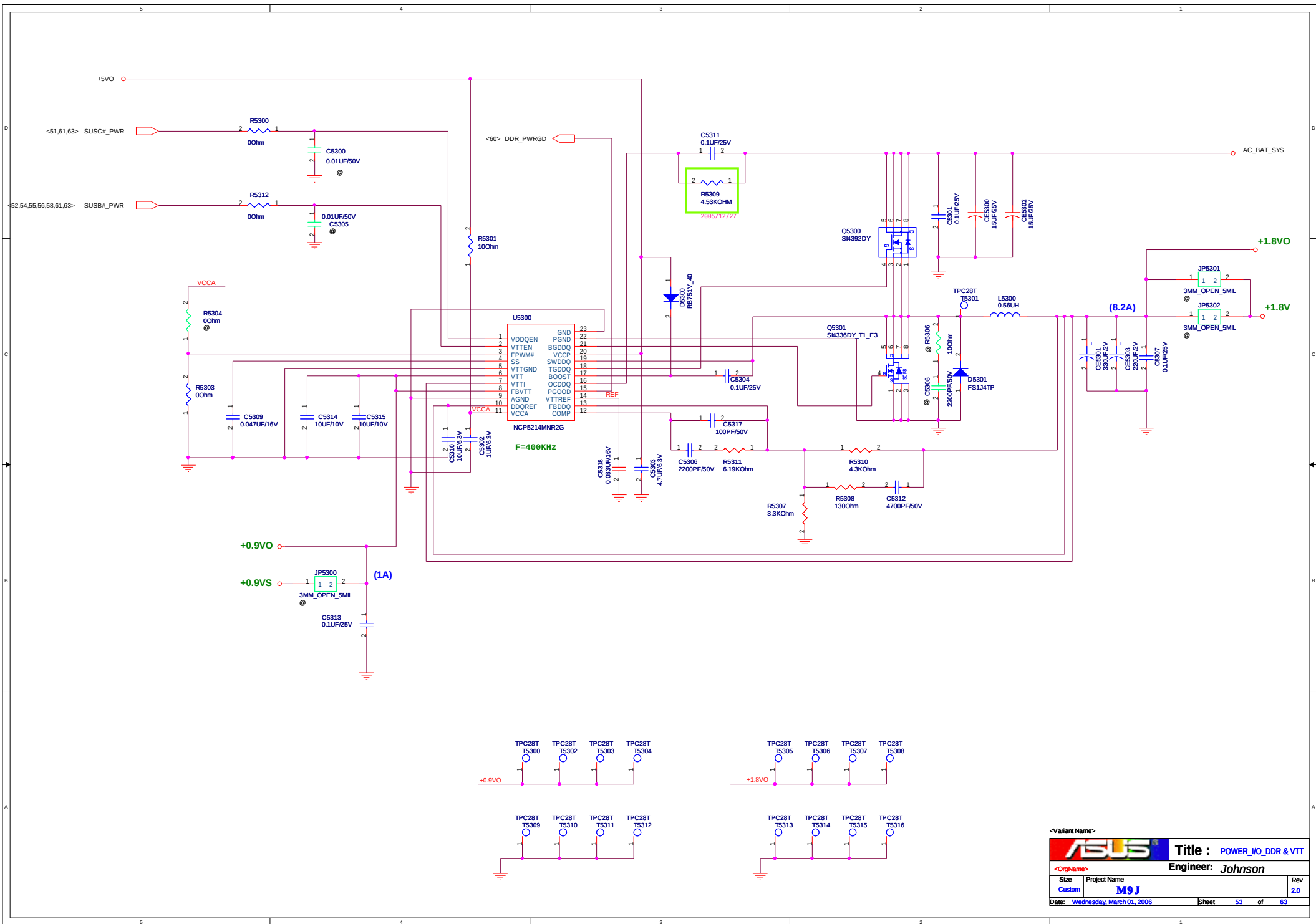






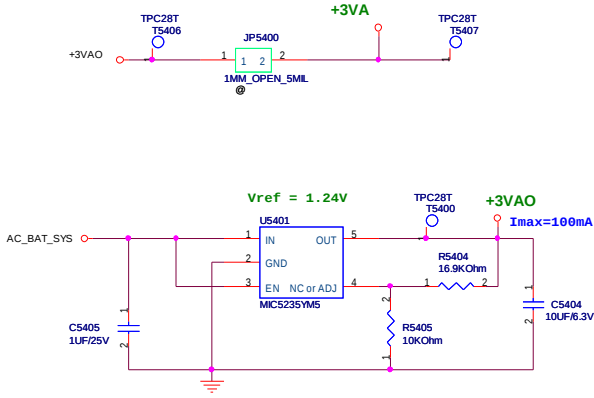
<Variant Name>

ASUS		Title : POWER_VCORE	
<OrigName>		Engineer: Johnson	
Size	Project Name	M9J	Rev 2.0
Custom			
Date:	Wednesday, March 01, 2006	Sheet	50 of 63

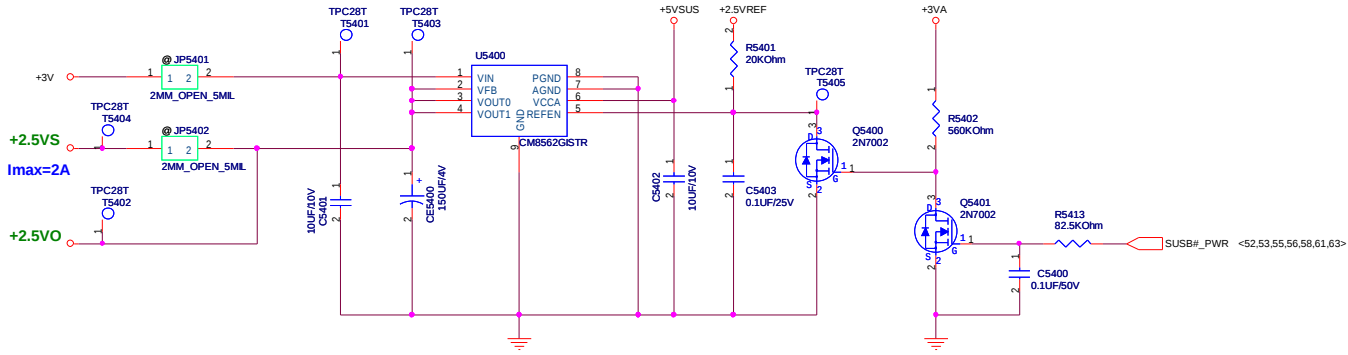


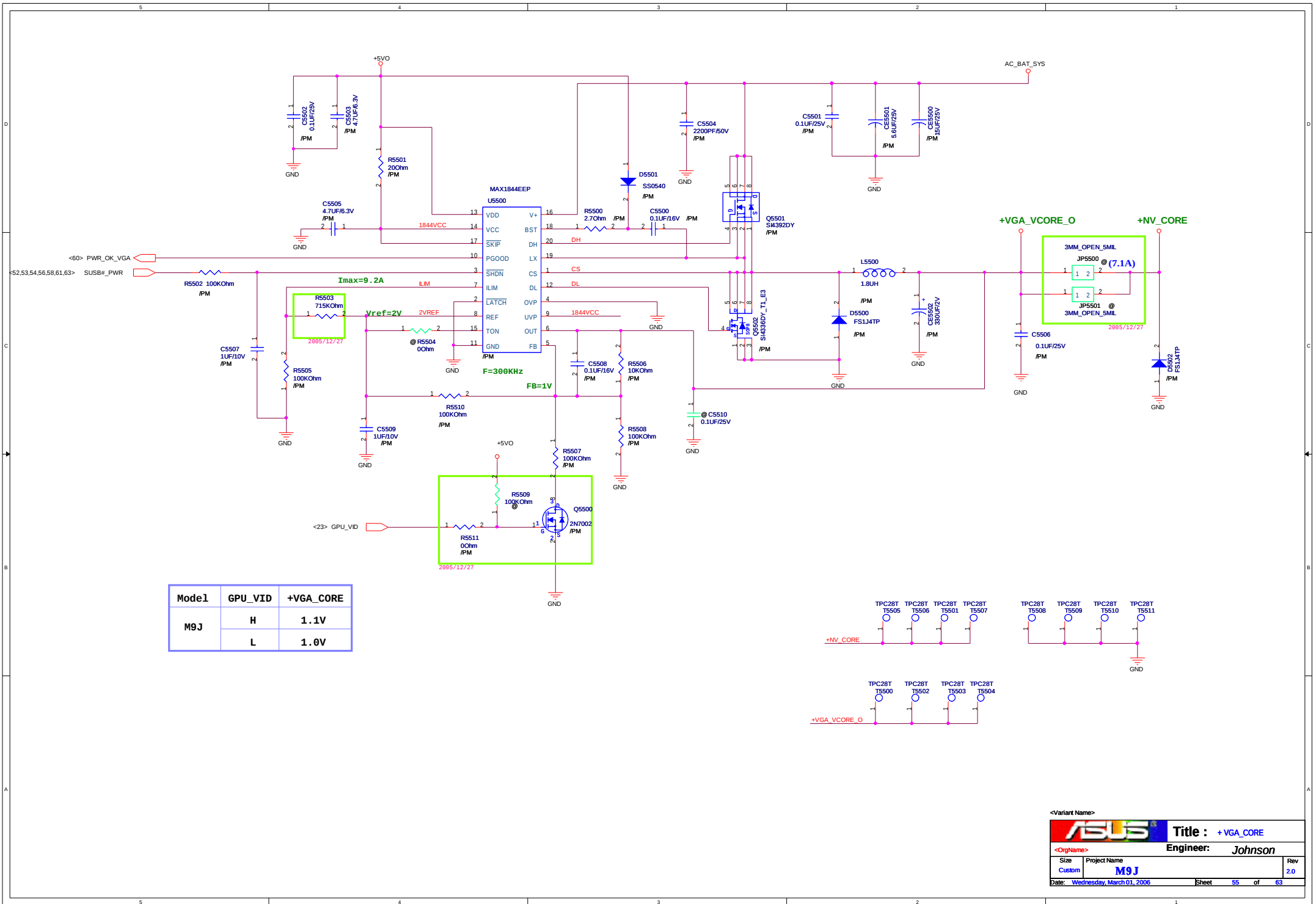
<Variant Name>		ASUS		Title : POWER_VO_DDR & VTT	
<OrigName>		Project Name		Engineer: Johnson	
Size	Custom	M9J		Rev	2.0
Date: Wednesday, March 01, 2006		Sheet		53	of 63

+3VAO

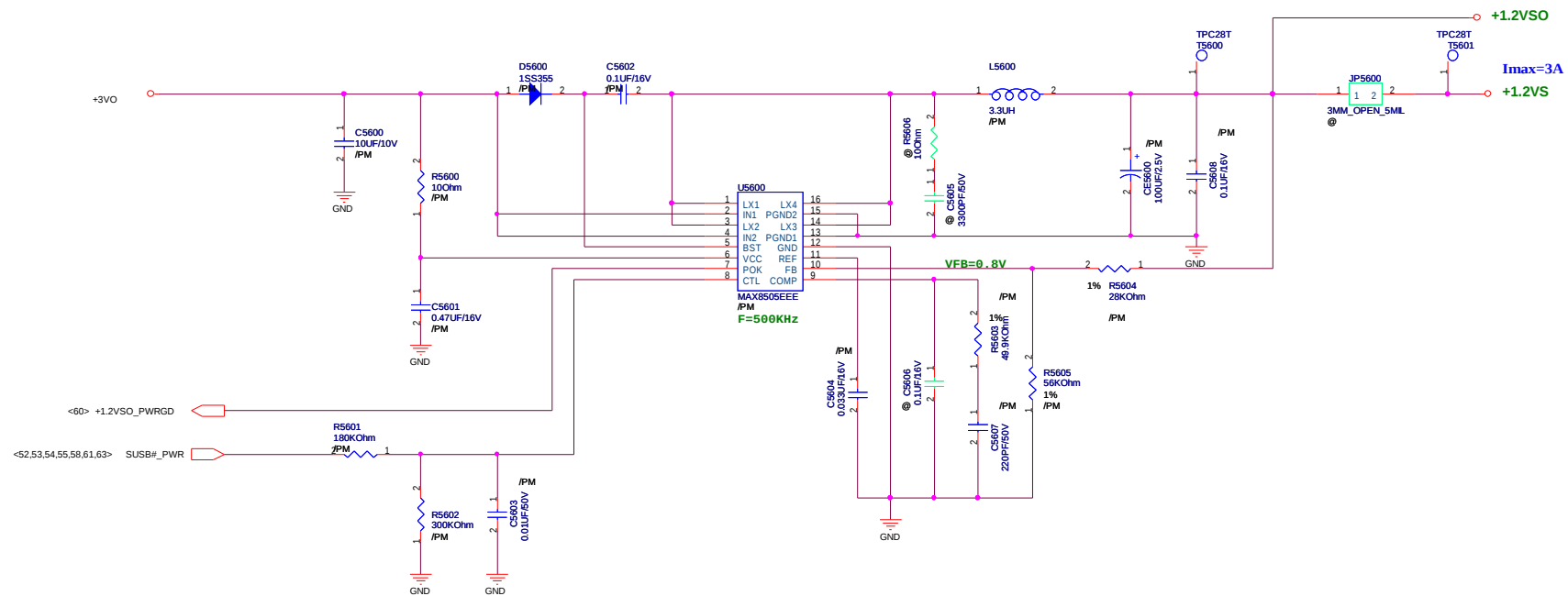


+2.5VS

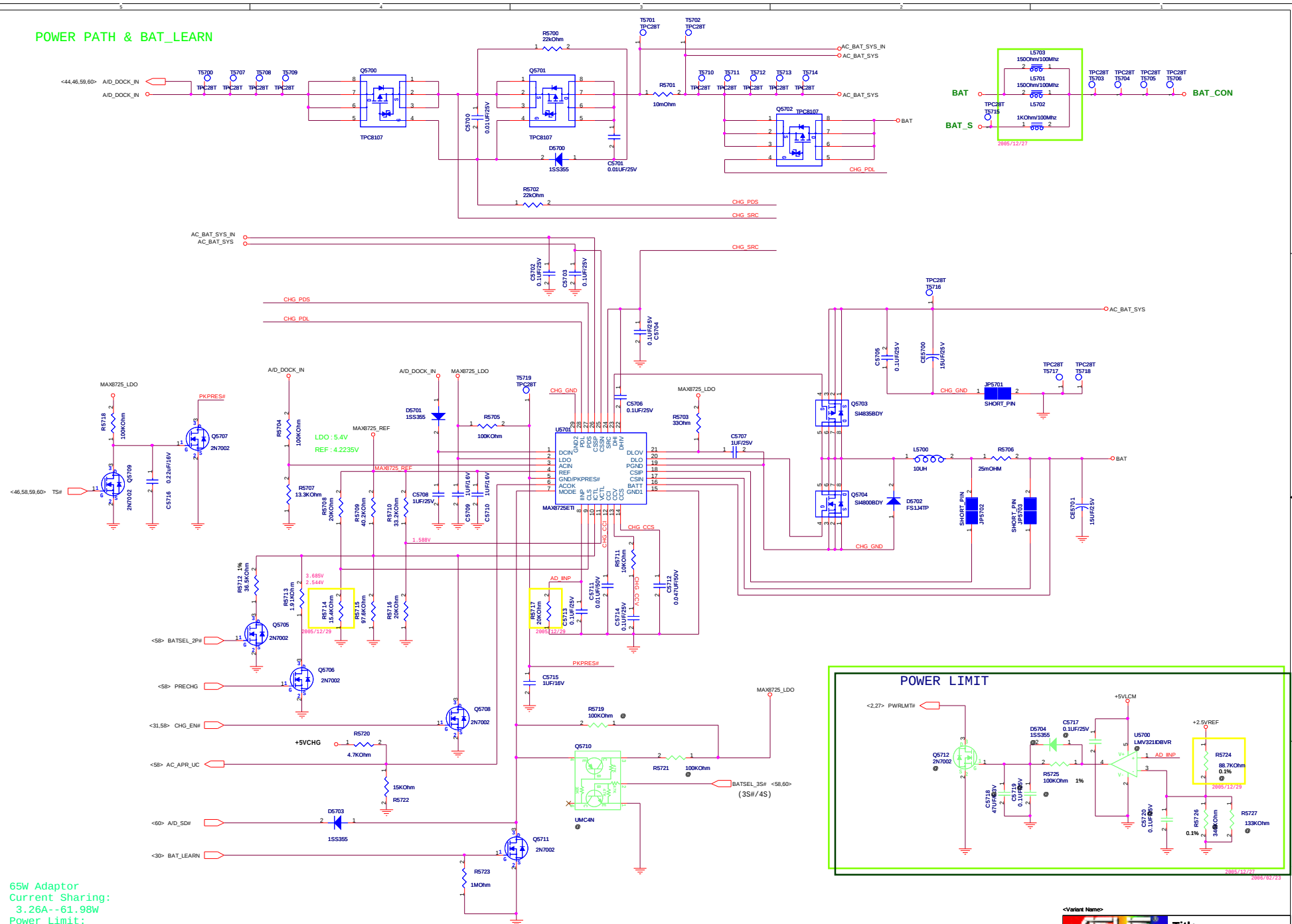




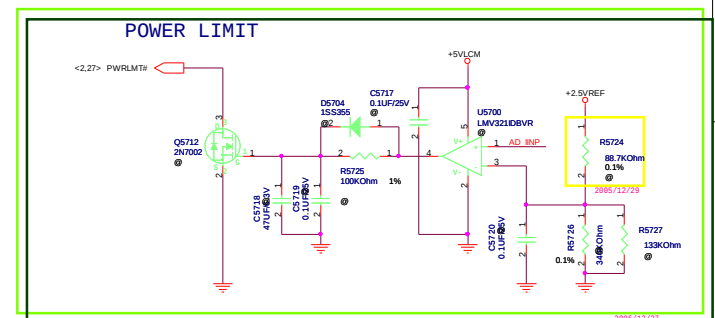
+1.2VSP



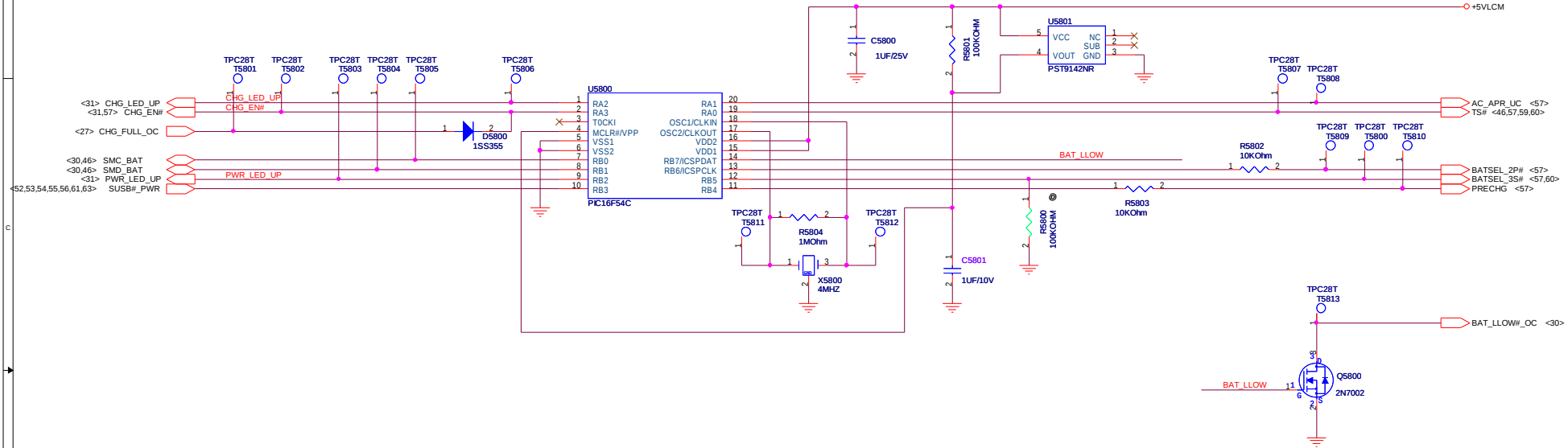
POWER PATH & BAT_LEARN



```
65W Adaptor
Current Sharing:
 3.26A--61.98W
Power Limit:
 3.305A--62.8W
```



PIC16F54C

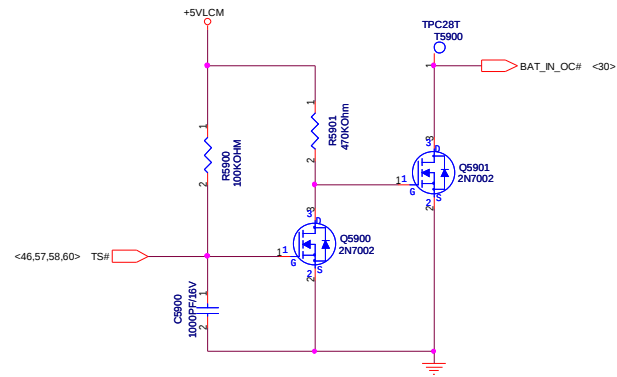


When BAT_LLOW#_OC is active, system entry S4

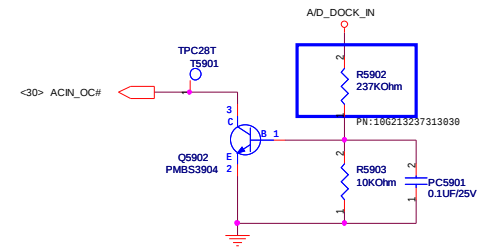
<Variant Name>

ASUS		Title : POWER_PIC	
Engineer: Johnson			
Size	Project Name	Rev	
Custom	M9J	2.0	
Date: Wednesday, March 01, 2006	Sheet	58	of 63

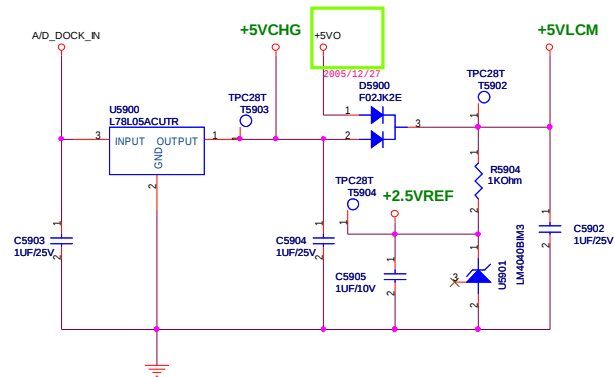
BATTERY IN DETECT



ADAPTER IN DETECT



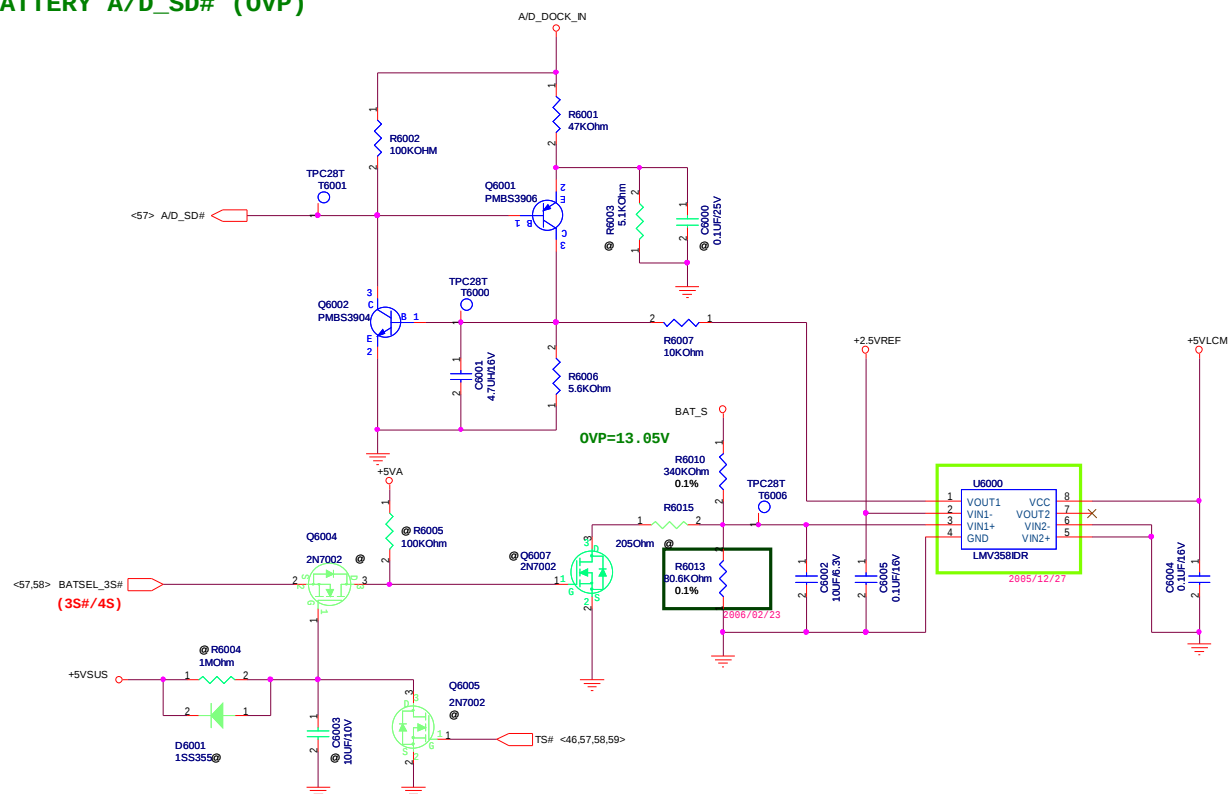
+5VLCM, +5VCHG & +2.5VREF



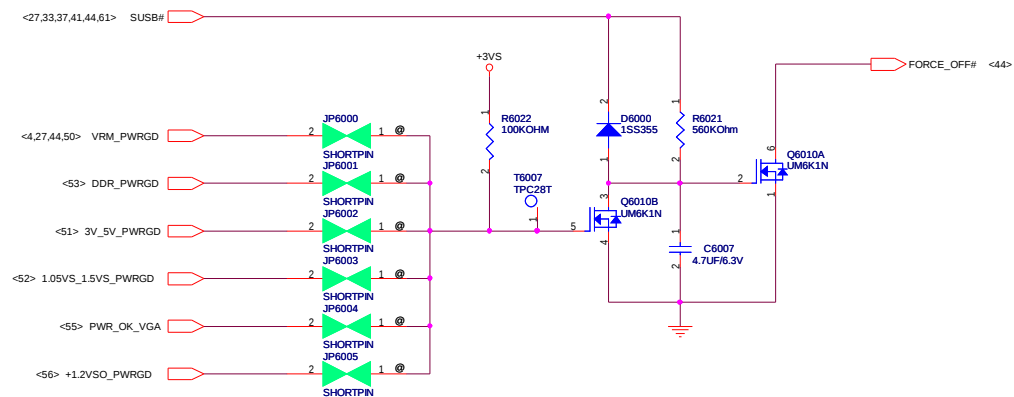
<Variant Name>

ASUS		Title : POWER_DETECT	
<OrigName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	M9J	2.0	
Date: Wednesday, March 01, 2006		Sheet	59 of 63

BATTERY A/D_SD# (OVP)



POWER GOOD DETECTOR



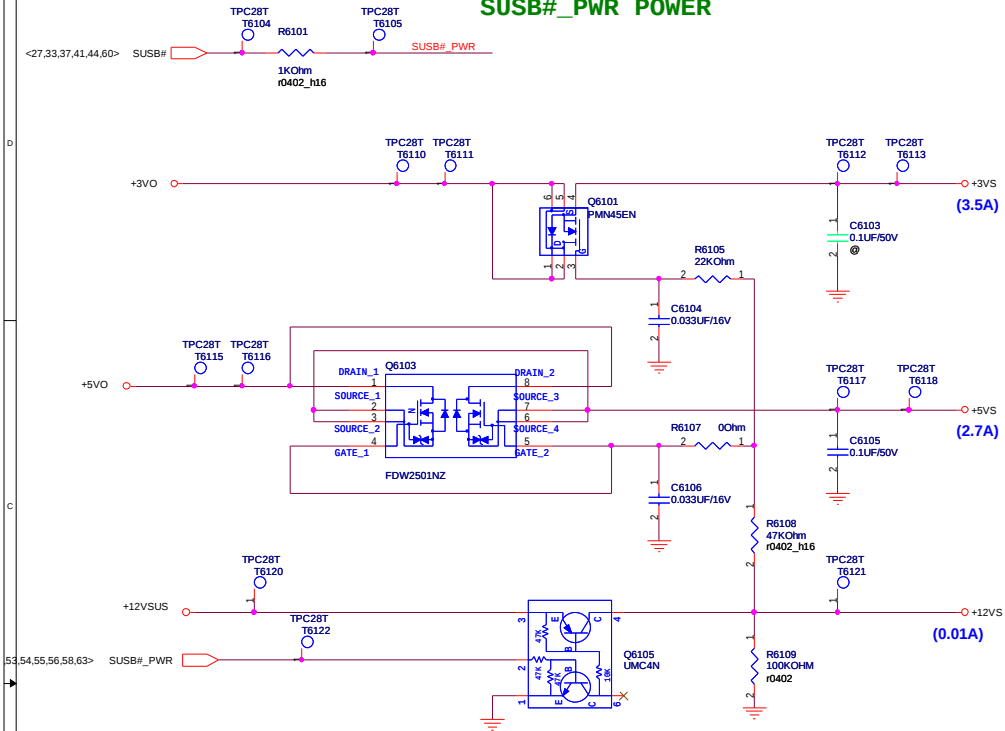
TPC28T T6002  1 VRM_PWRGD

TPC28T T6003  1 DDR_PWRGD

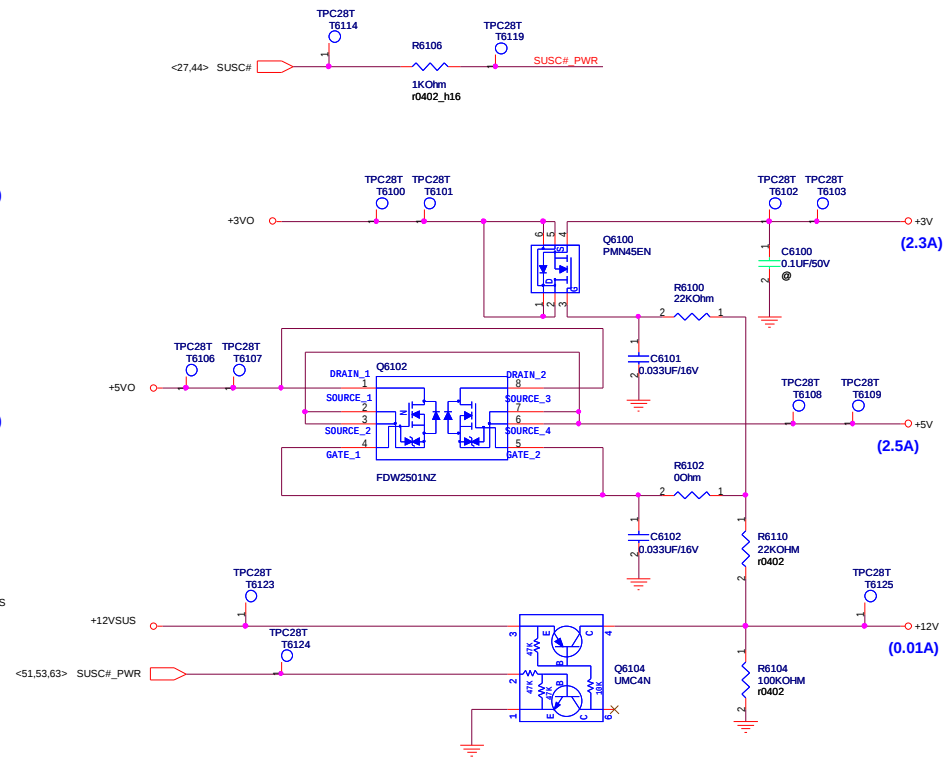
TPC28T T6004  1 3V_5V_PWRGD

TPC28T T6005  1 1.05VS_1.5VS_PWRGD

SUSB#_PWR POWER

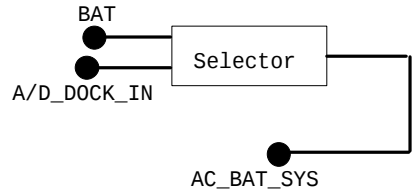
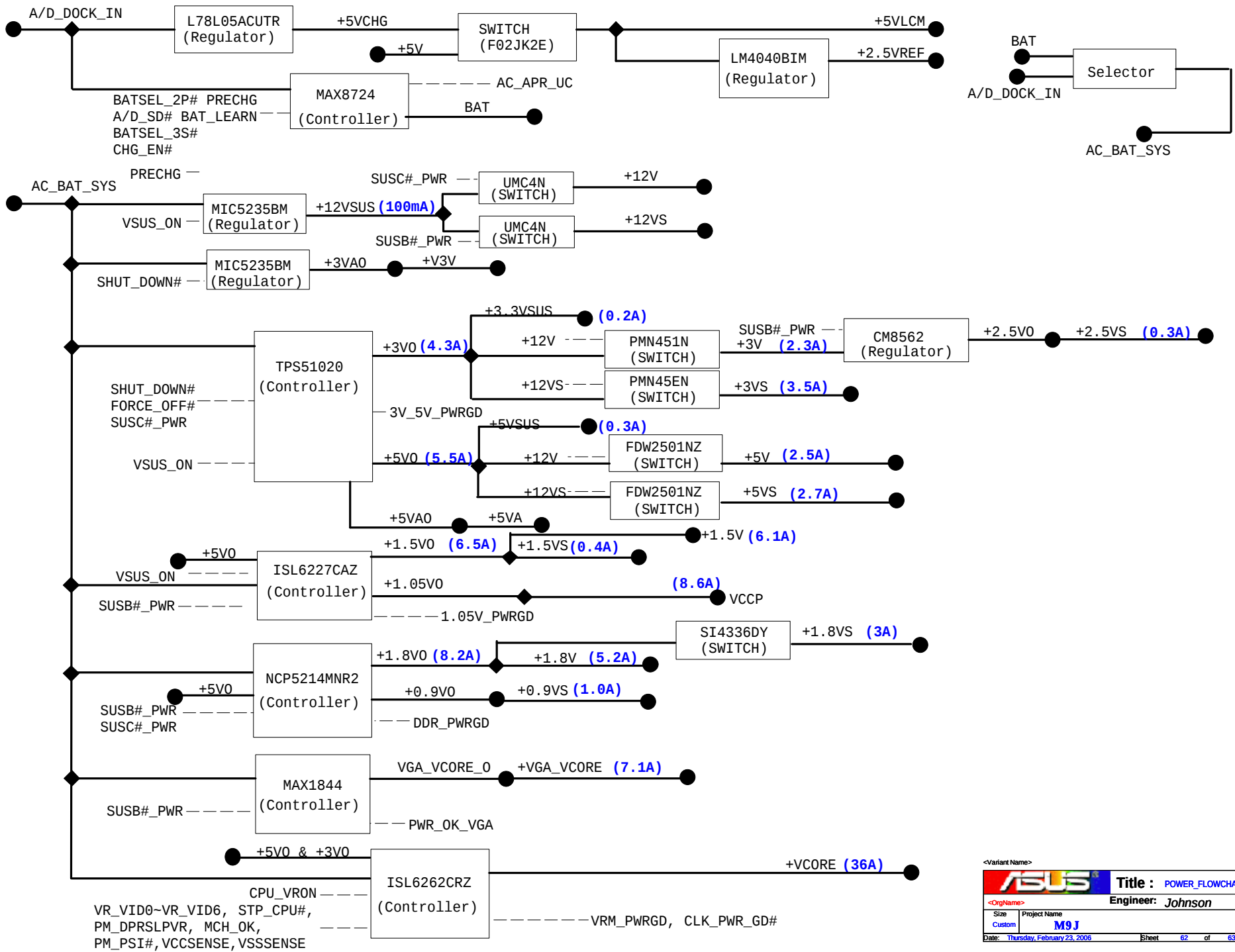


SUSC#_PWR POWER

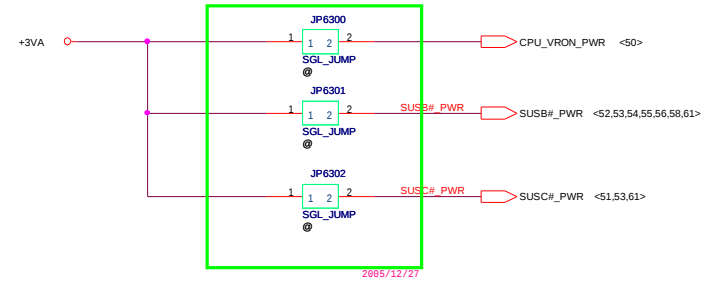
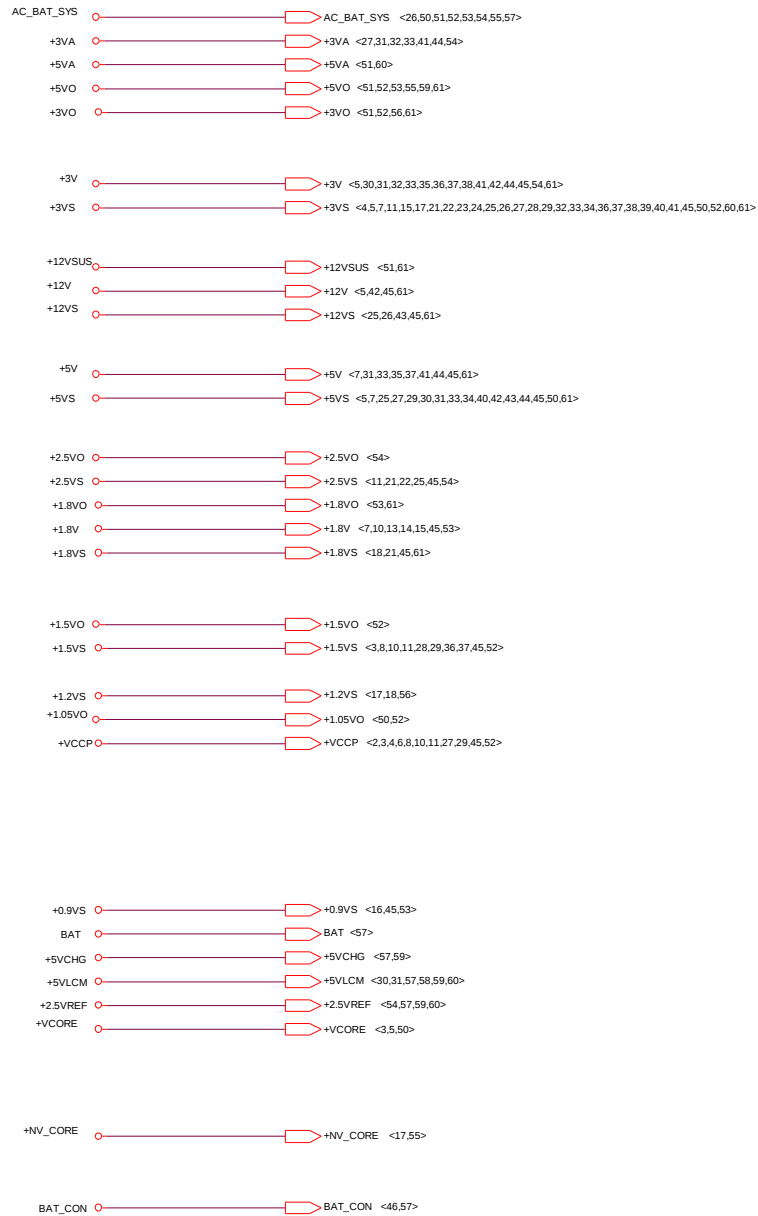


<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
<OrigName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	M9J	2.0	
Date: Wednesday, March 01, 2006	Sheet	61	of 63



FOR POWER TEST



MODIFY LIST

2000/02/23
1.Unmount Power Limit Circuit
2.Modify OVP Circuit
3.Change R6013 to 0.1% resistor

<Variant Name>

ASUS		Title : POWER_SIGNAL	
<OrigName>		Engineer: Johnson	
Size	Project Name	Rev	
Custom	M9J	2.0	
Date: Wednesday, March 01, 2006		Sheet	63 of 63