F9E SCHEMATIC Revision 2.02

SYSTEM PAGE REF.

POWER PAGE REF.

<Variant Name>

ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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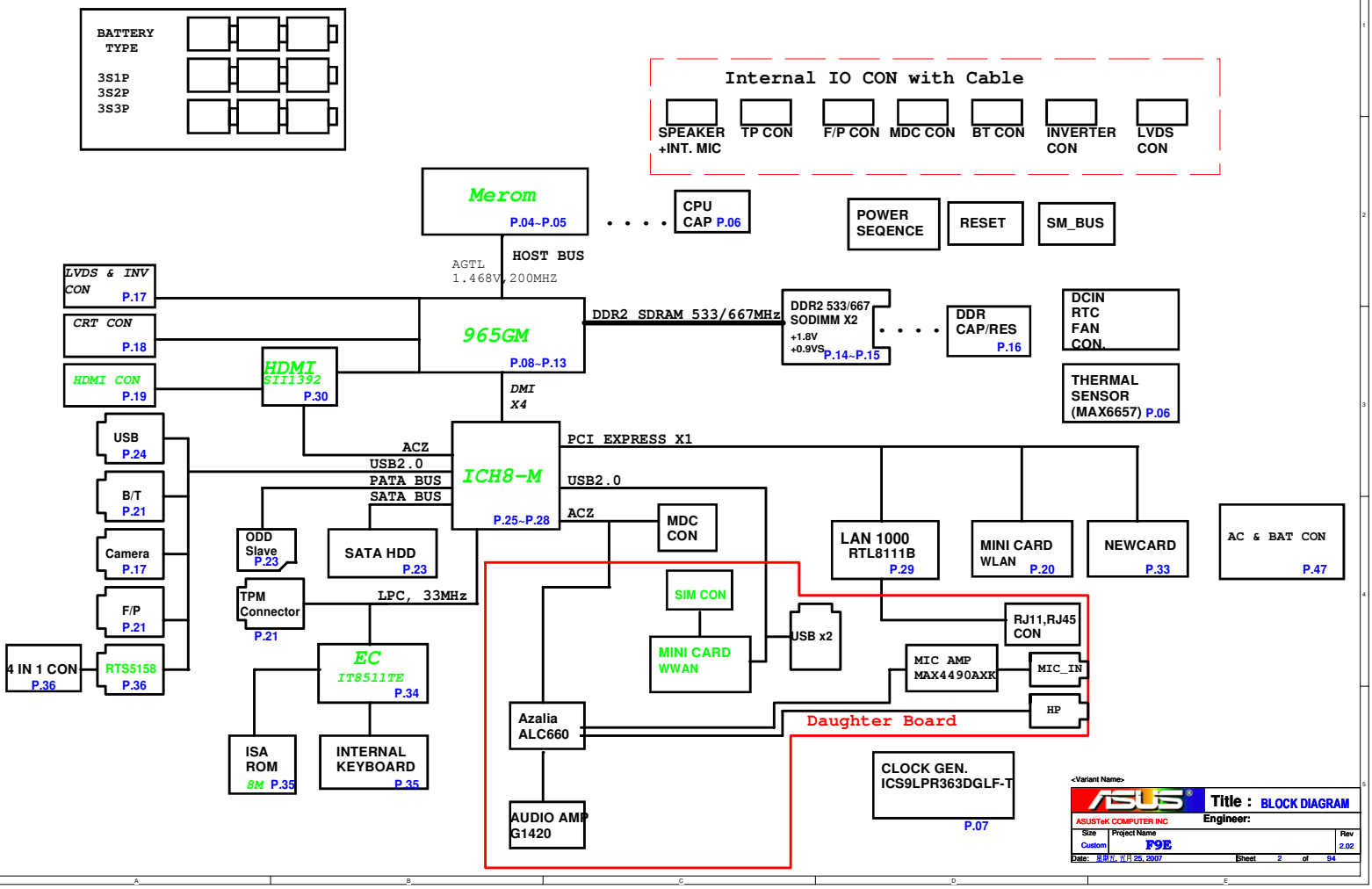
<< Kennedy_Zhang >>

F9E BLOCK DIAGRAM



<< Kennedy_Zhang >>

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	PWRLIMIT#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/0
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

ICH8M_GPIO

Pin.	Default_RST#	Use As	Signal Name	Power	Mux
GPIO 00	i	GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	0 GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	Hi-Z GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	0 GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i	0 GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i	GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	Hi-Z GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	Hi-Z GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat.	Hi-Z Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i	GPI	KBC_SCI#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat.	GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	Hi-Z GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat.	1 Native	STP_PCI#	+3VSUS	STP_PCI#, No-GPIO in Mobile
GPIO 16	Nat.	0 Native	PM_DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	1 GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	freq 4K GPO	N/A	+3VS	N/A
GPIO 19	i	GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	1 GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i	GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i	GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat.	Native	N/A	+3VS	LDRQ1#
GPIO 24	O	Hi-Z GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED), Not Cleared by CF9h RST event.
GPIO 25	Nat.	1 Native	STP_CPU#	+3VS	STP_CPU#, No-GPIO in Mobile
GPIO 26	Nat.	GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	0 GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	0 GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat.	Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat.	Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat.	Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	0 Native	PM_CLKRUN#	+3VS	CLKRUN#, No-GPIO in Mobile
GPIO 33	O	1 GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	0 GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	0 GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i	GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	0 GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i	GPI	PCB_ID1	+3VS	SLOAD

Pin	Default_RST#	Use As	Signal Name	Power	Mux
GPIO 39	i	GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat.	Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a	N/A	N/A	N/A	No implement
GPIO 48	i	1 Native		+3VS	SDATAOUT1
GPIO 49	Nat.	Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat.	Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat.	1 Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat.	Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat.	1 Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat.	Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat.	1 Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

ASUSTeK COMPUTER INC

Title : Schematic Info.

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9E	2.02

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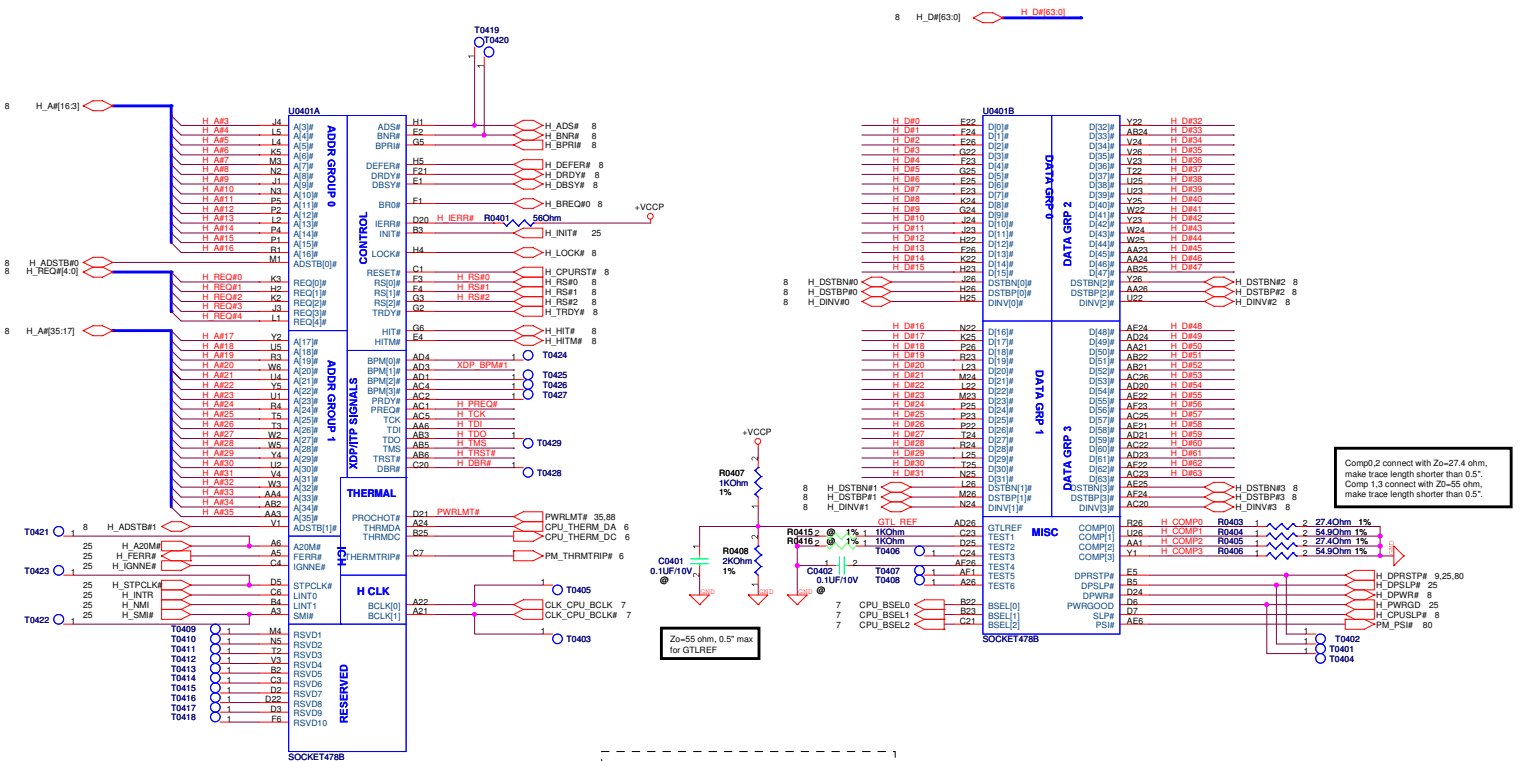

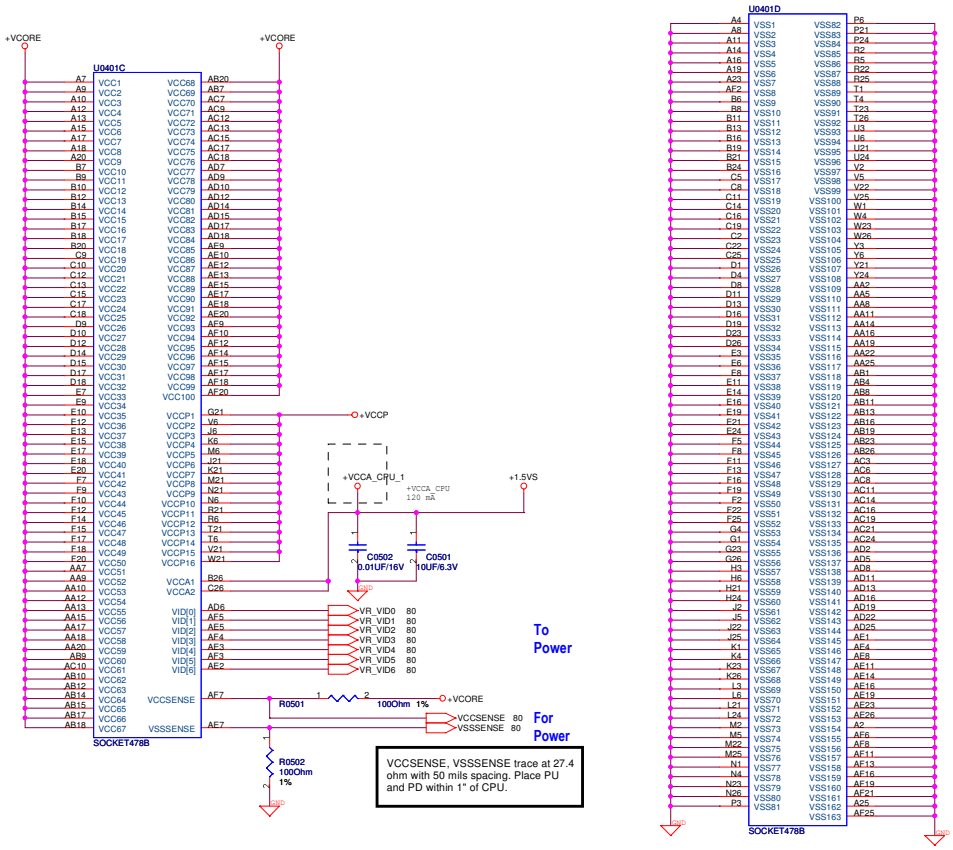

<Variant Name>

ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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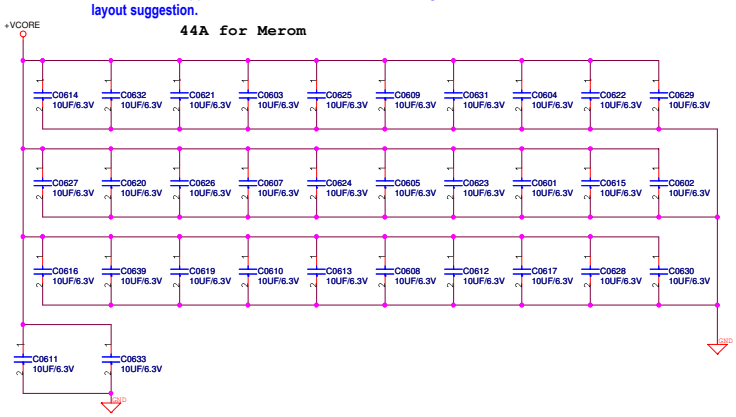
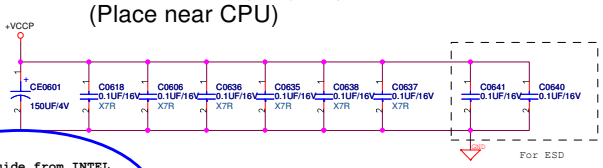
Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom



+VCCP Decoupling Capacitor (Place near CPU)

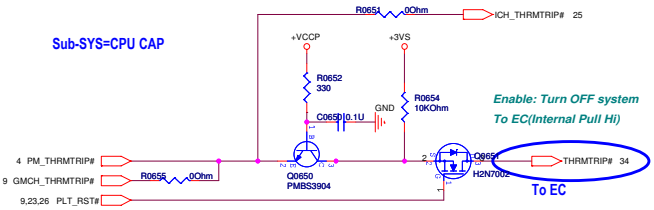


Decoupling guide from INTEL

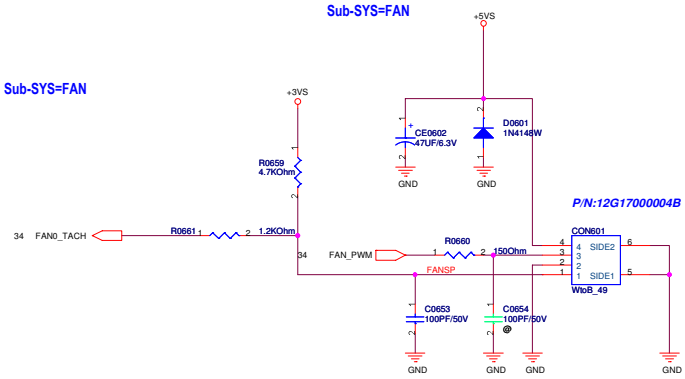
VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it ! _0907

Sub-SYS=CPU CAP

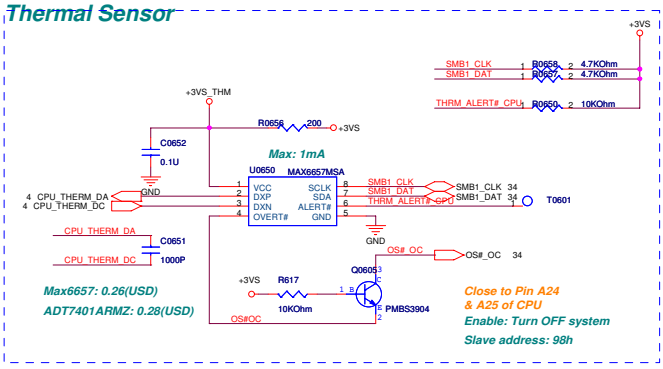


Sub-SYS=FAN

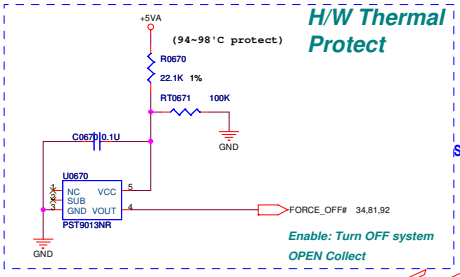


Sub-SYS=FAN

Thermal Sensor



H/W Thermal Protect



Sub-SYS=CPU

<Variant Name>

ASUSTeK COMPUTER INC

Title : CPU CAP, Thermal Senor

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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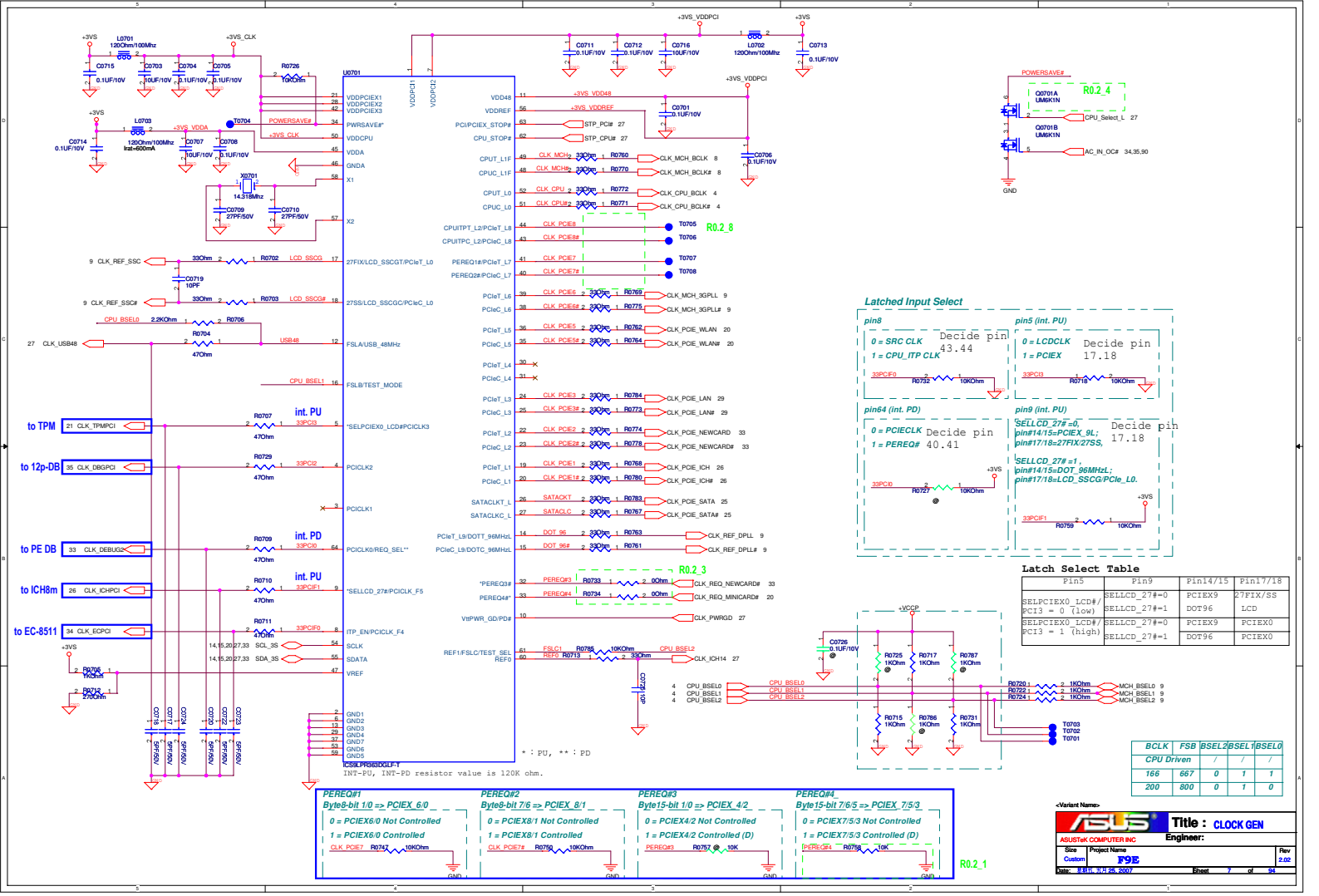

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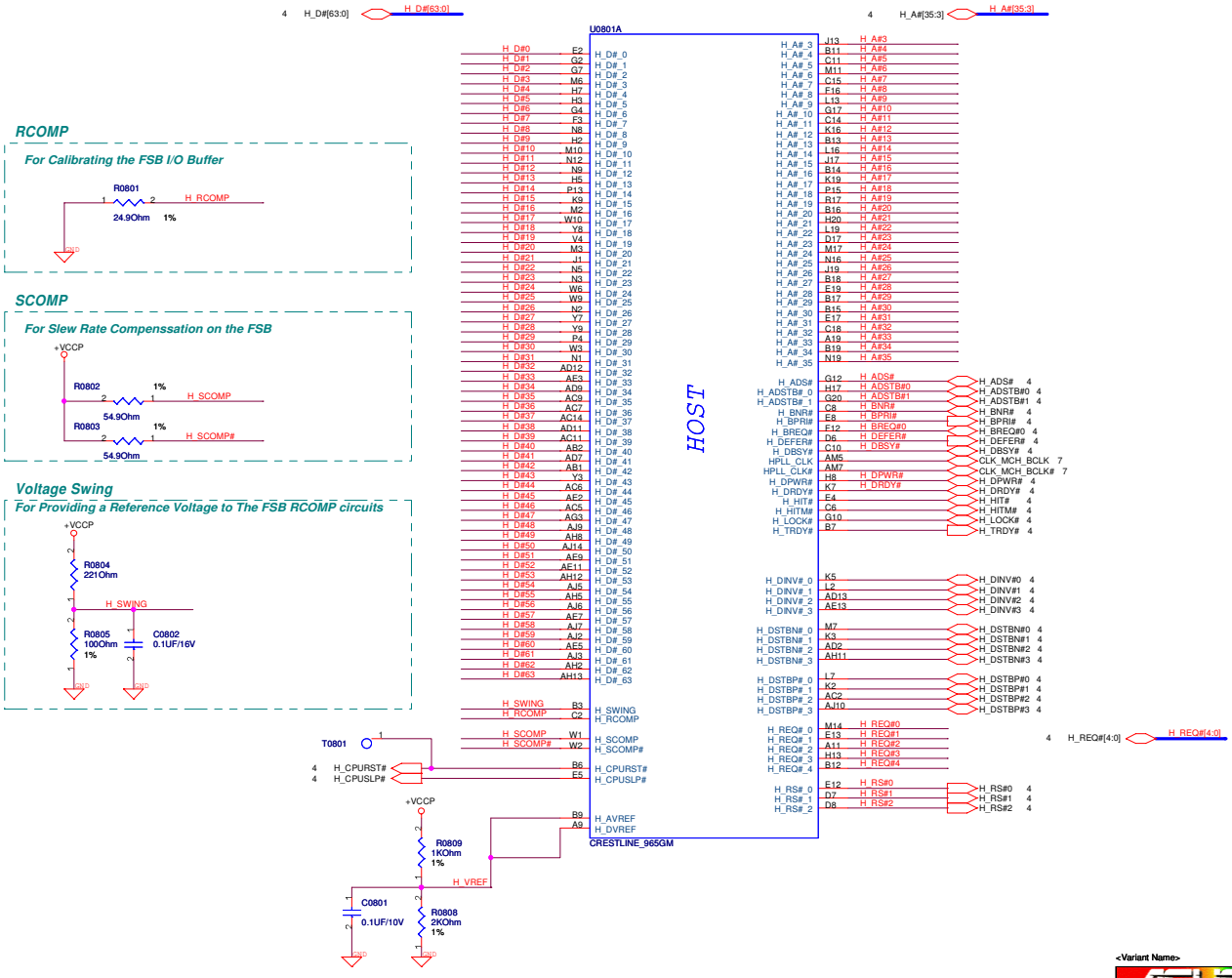

<Variant Name>

ASUSTeK COMPUTER INC

Title : 965GM – CPU (1)

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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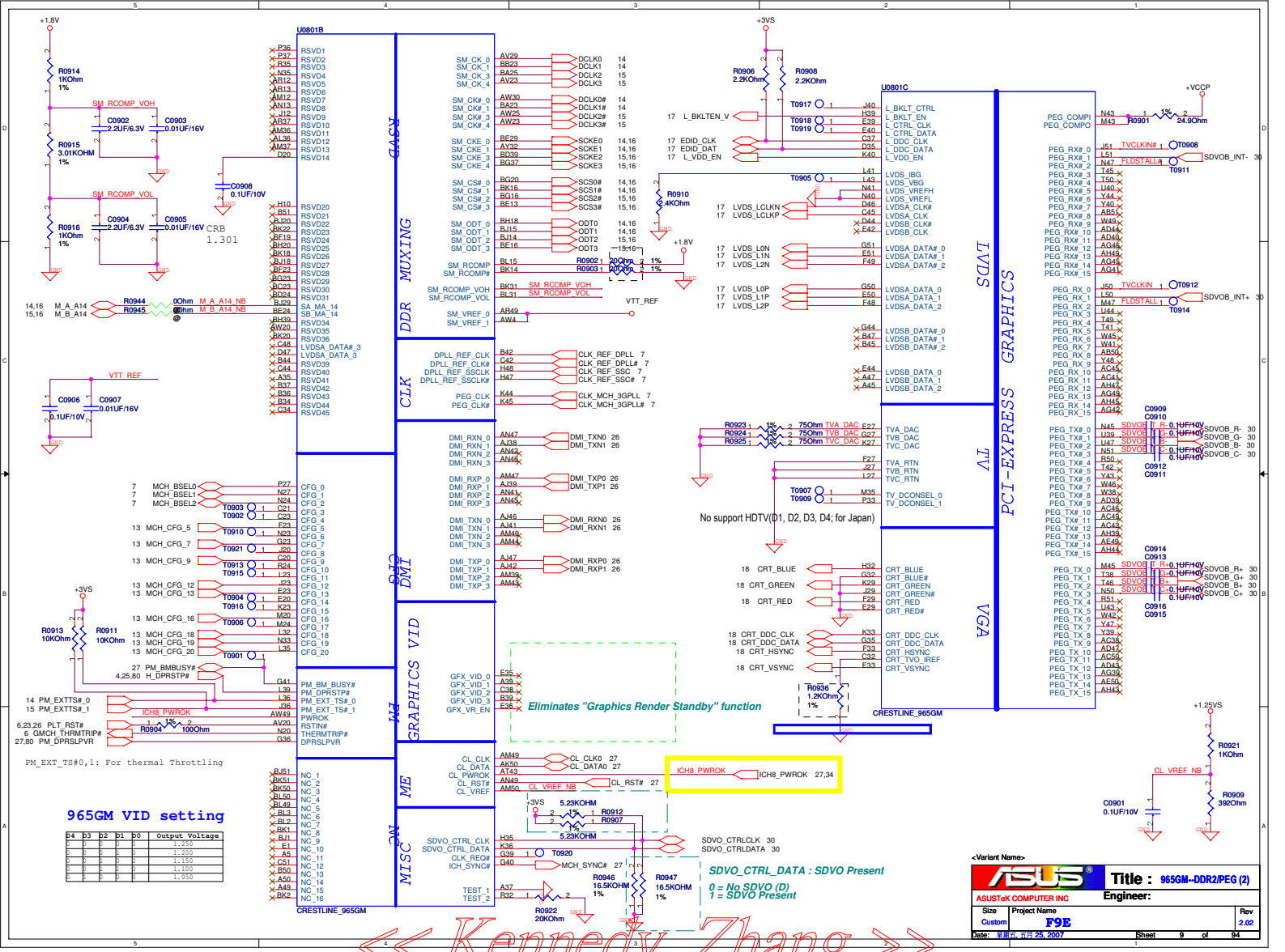
U0801B
U0801C
CRESTLINE_965GM
CRB 1.301
SM_RCOMP_VOH
SM_RCOMP_VOL
VTT_REF
M_A_A14_NB
M_B_A14_NB
ICH8_PWROK
CL_VREF_NB
SDVO_CTRL_DATA : SDVO Present
0 = No SDVO (D)
1 = SDVO Present
Eliminates "Graphics Render Standby" function
No support HDTV(D1, D2, D3, D4; for Japan)
PM_EXT_TS#0,1: For thermal Throttling
965GM VID setting
D4 D3 D2 D1 D0 Output Voltage
0 0 0 0 0 1.250
0 0 0 0 1 1.200
0 0 0 1 0 1.150
0 0 0 1 1 1.100
0 0 1 0 0 1.050
Title : 965GM--DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: F9E
Rev: 2.02
Date: 星期六, 五月 26, 2007
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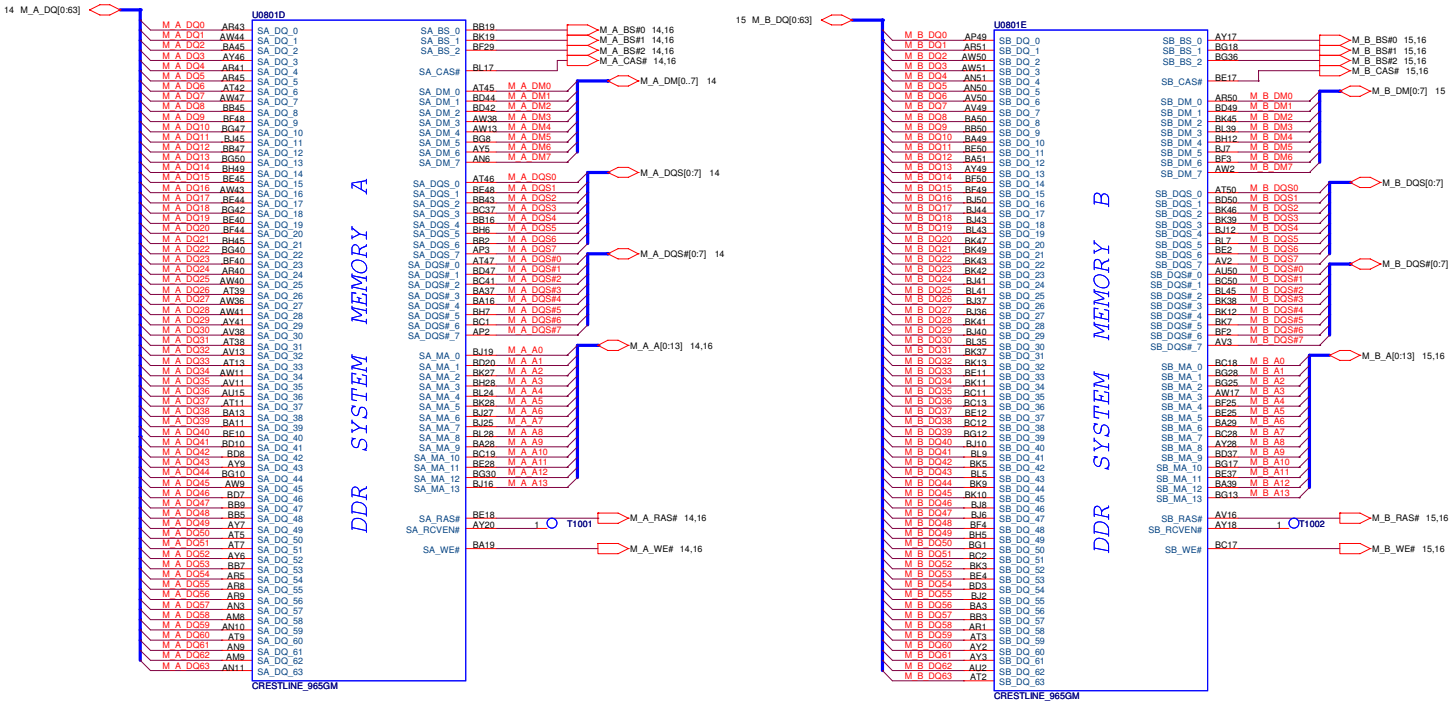
<Variant Name>
<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC

Title : 965GM-DDR2 bus (3)

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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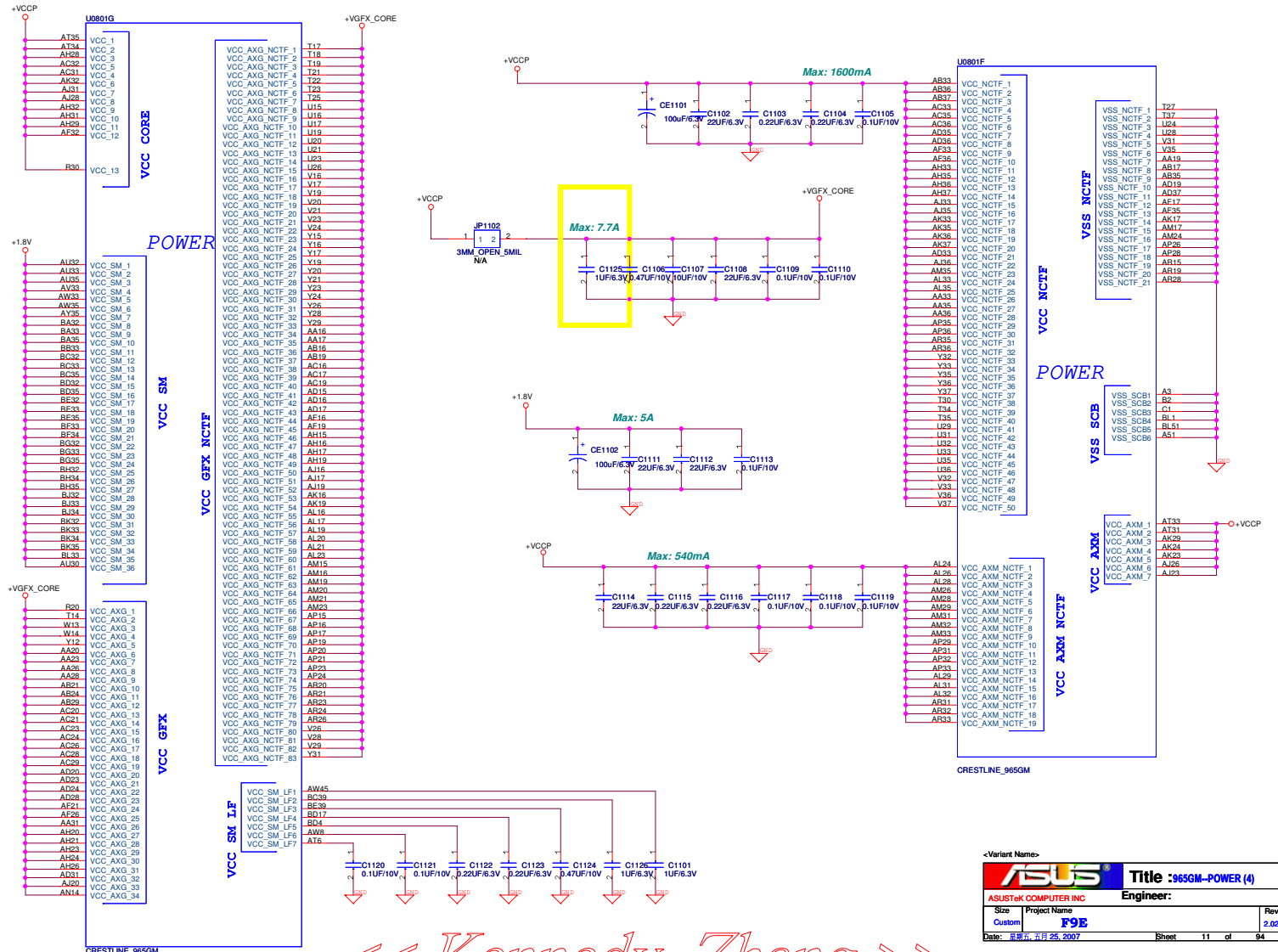

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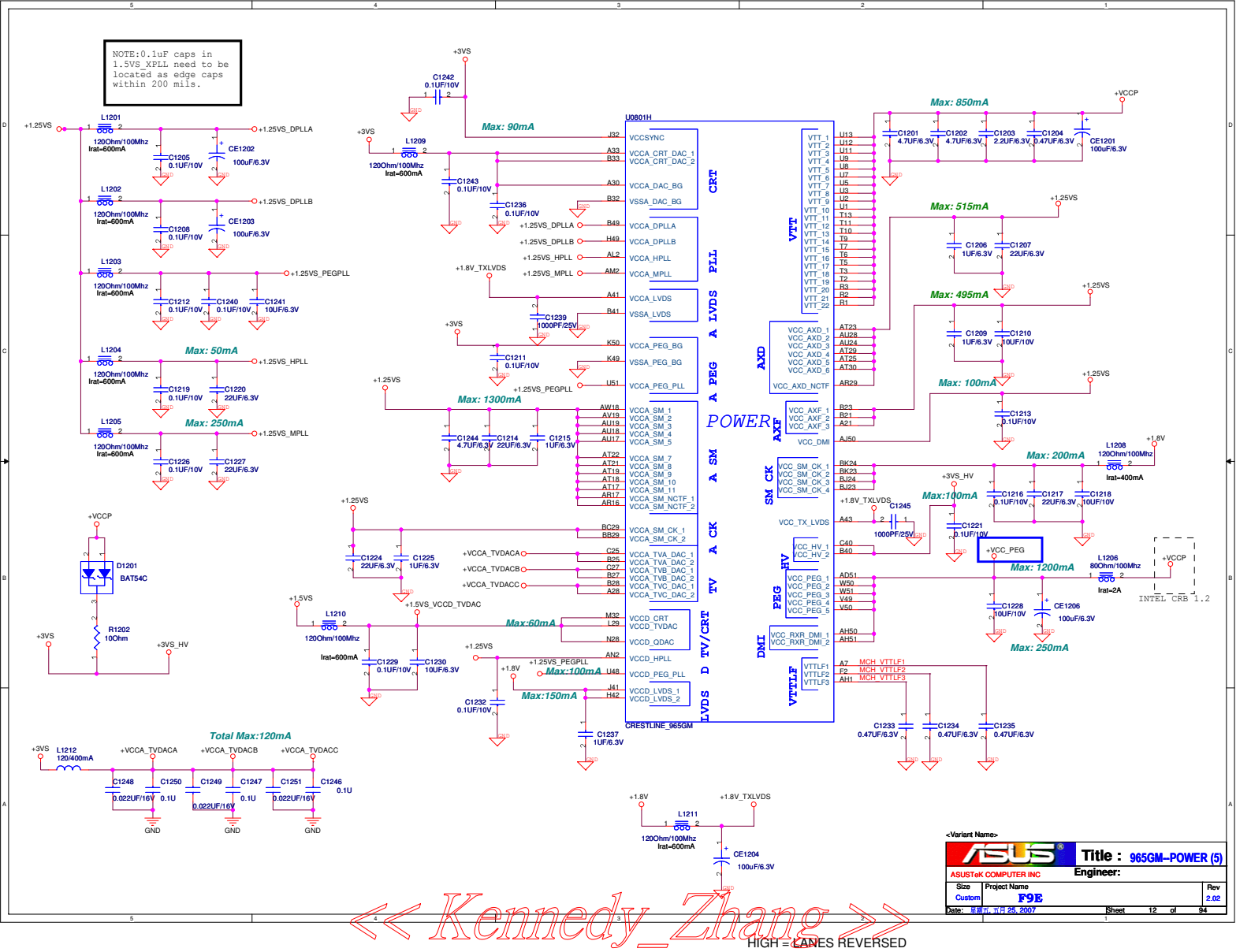
NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
POWER
U0801H
CRESTLINE_965GM
Max: 90mA
Max: 850mA
Max: 515mA
Max: 495mA
Max: 50mA
Max: 100mA
Max: 1300mA
Max: 200mA
Max: 250mA
Max: 1200mA
Max:60mA
Max:100mA
Max:150mA
Total Max:120mA
Title : 965GM-POWER (5)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: F9E
Rev: 2.02
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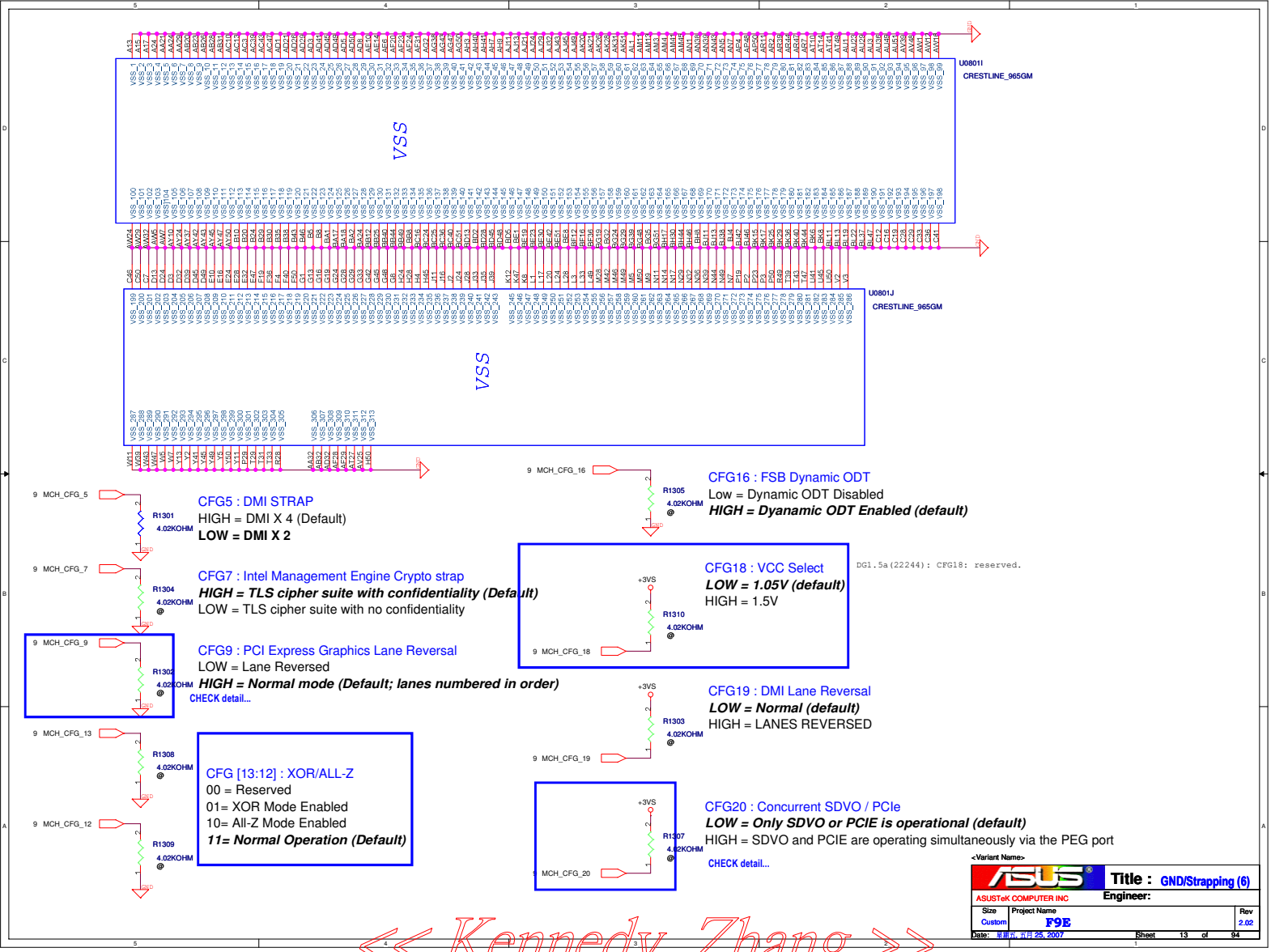
HIGH = LANES REVERSED


U0801I
CRESTLINE_965GM
VSS
U0801J
CRESTLINE_965GM
VSS
9 MCH_CFG_5
R1301
4.02KOHM
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2
9 MCH_CFG_7
R1304
4.02KOHM
@
CFG7 : Intel Management Engine Crypto strap
HIGH = TLS cipher suite with confidentiality (Default)
LOW = TLS cipher suite with no confidentiality
9 MCH_CFG_9
R1302
4.02KOHM
@
CHECK detail...
CFG9 : PCI Express Graphics Lane Reversal
LOW = Lane Reversed
HIGH = Normal mode (Default; lanes numbered in order)
9 MCH_CFG_13
R1308
4.02KOHM
@
9 MCH_CFG_12
R1309
4.02KOHM
@
CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)
9 MCH_CFG_16
R1305
4.02KOHM
@
CFG16 : FSB Dynamic ODT
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)
+3VS
R1310
4.02KOHM
@
9 MCH_CFG_18
CFG18 : VCC Select
LOW = 1.05V (default)
HIGH = 1.5V
DG1.5a(22244): CFG18: reserved.
+3VS
R1303
4.02KOHM
@
9 MCH_CFG_19
CFG19 : DMI Lane Reversal
LOW = Normal (default)
HIGH = LANES REVERSED
+3VS
R1307
4.02KOHM
@
MCH_CFG_20
CFG20 : Concurrent SDVO / PCIe
LOW = Only SDVO or PCIE is operational (default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port
CHECK detail...
<Variant Name>
ASUSTeK COMPUTER INC
Title : GND/Strapping (6)
Engineer:
Size: Custom
Project Name: F9E
Rev: 2.02
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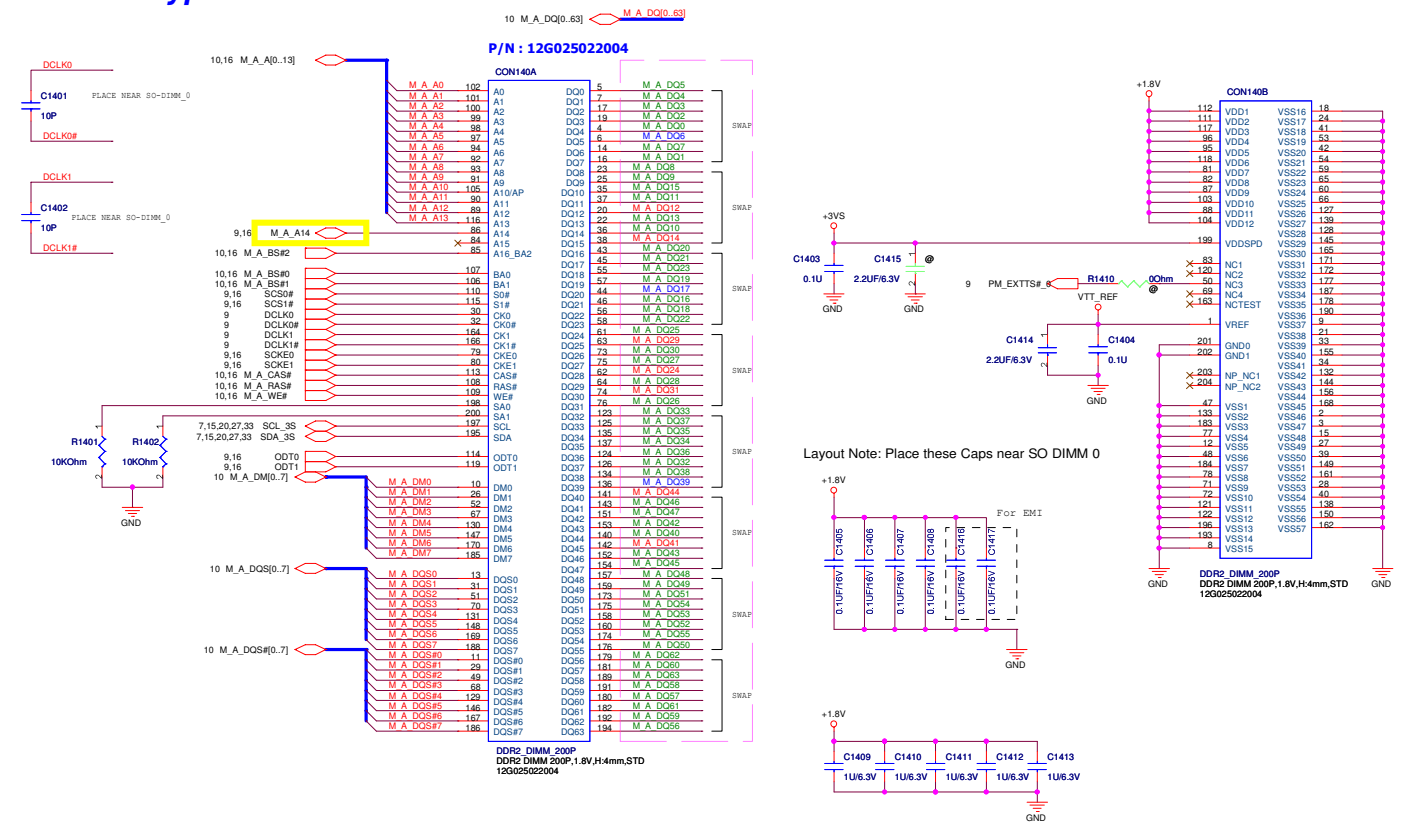
Standard Type



Layout Note: Place these Caps near SO DIMM 0

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM 0

Engineer:

Size	Project Name	Rev
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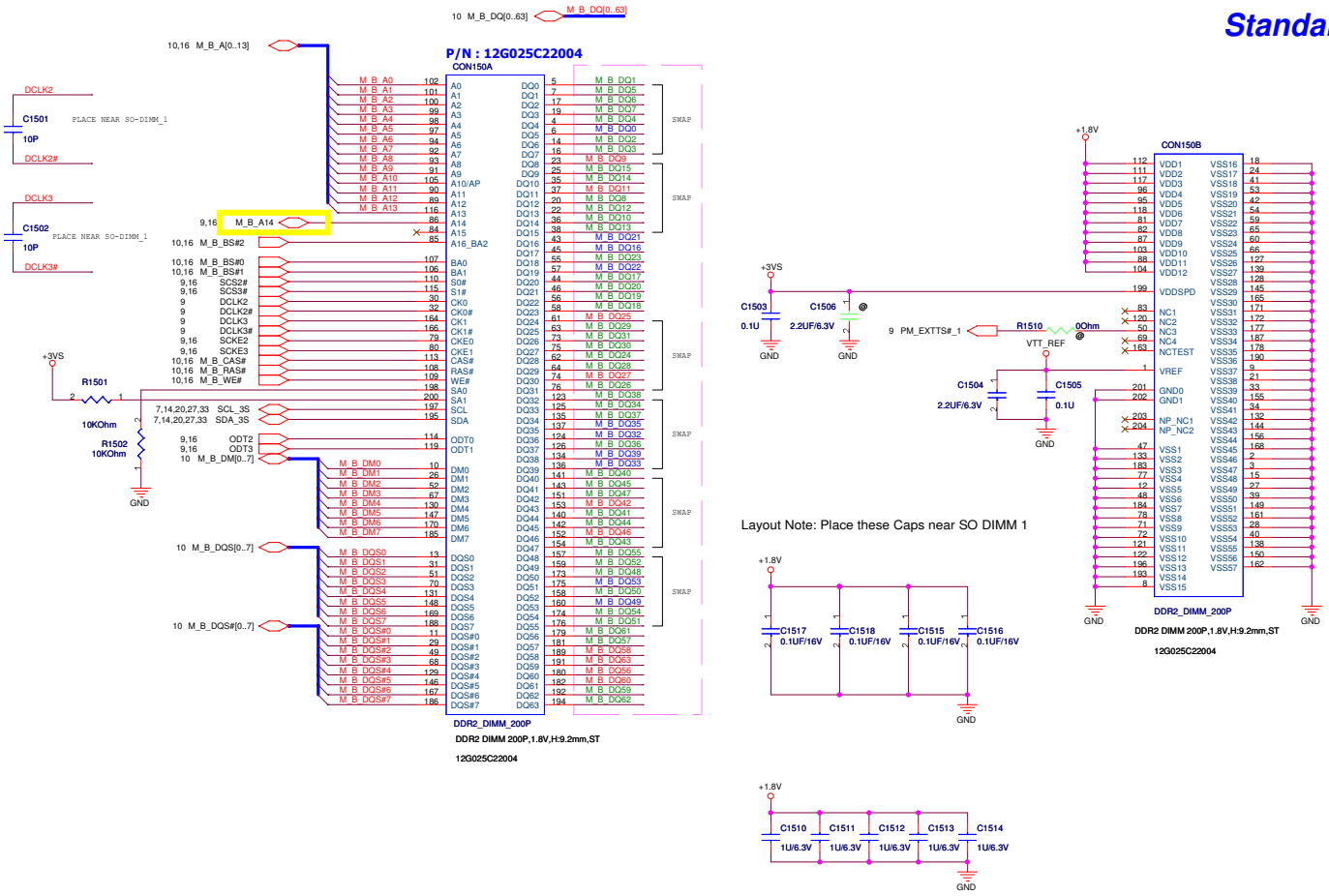
Standard Type



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM_1

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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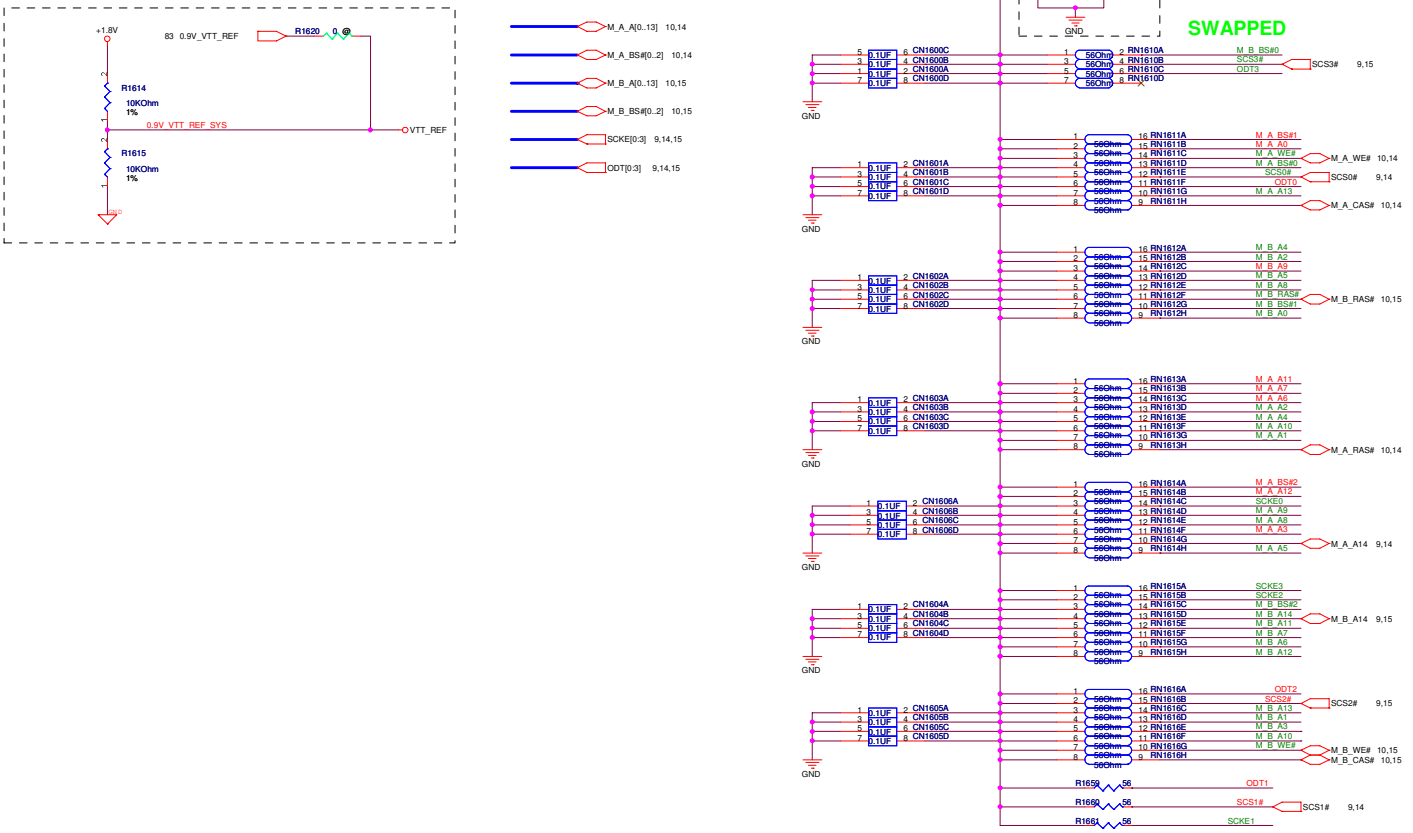

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 ADDR TERM

Engineer:

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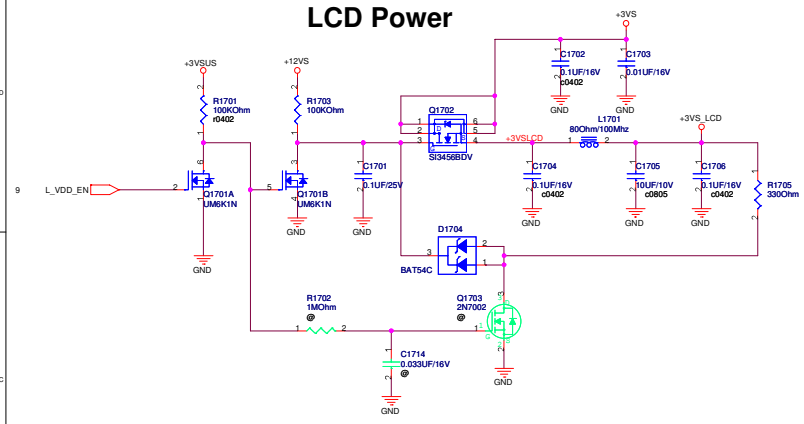
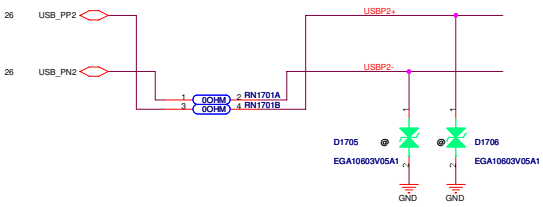
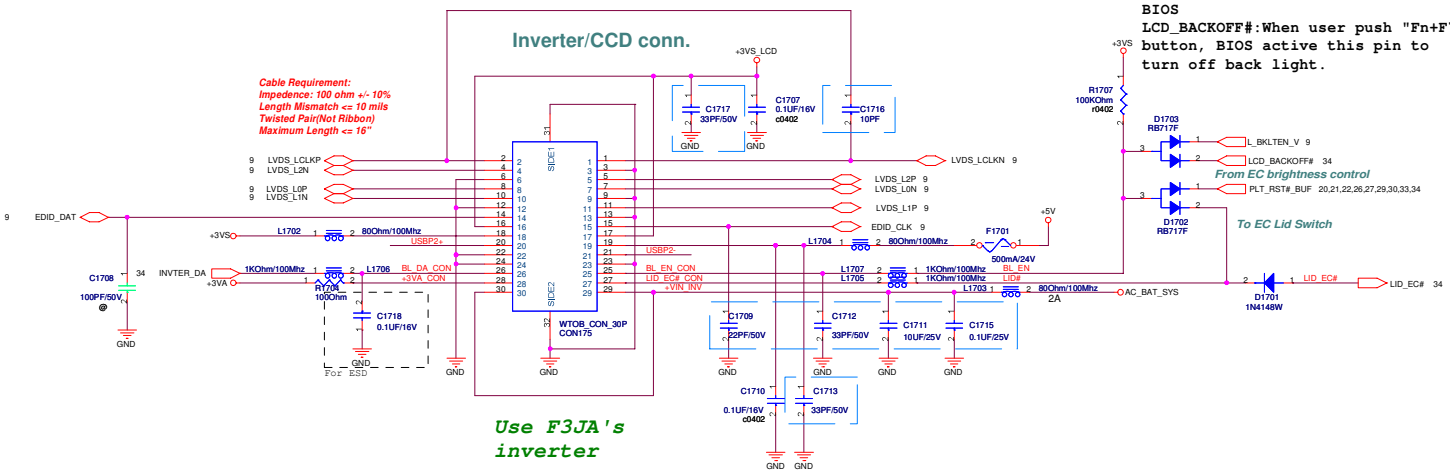
LCD Power





Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

From EC brightness control

To EC Lid Switch

Use F3JA's inverter

<Variant Name>

ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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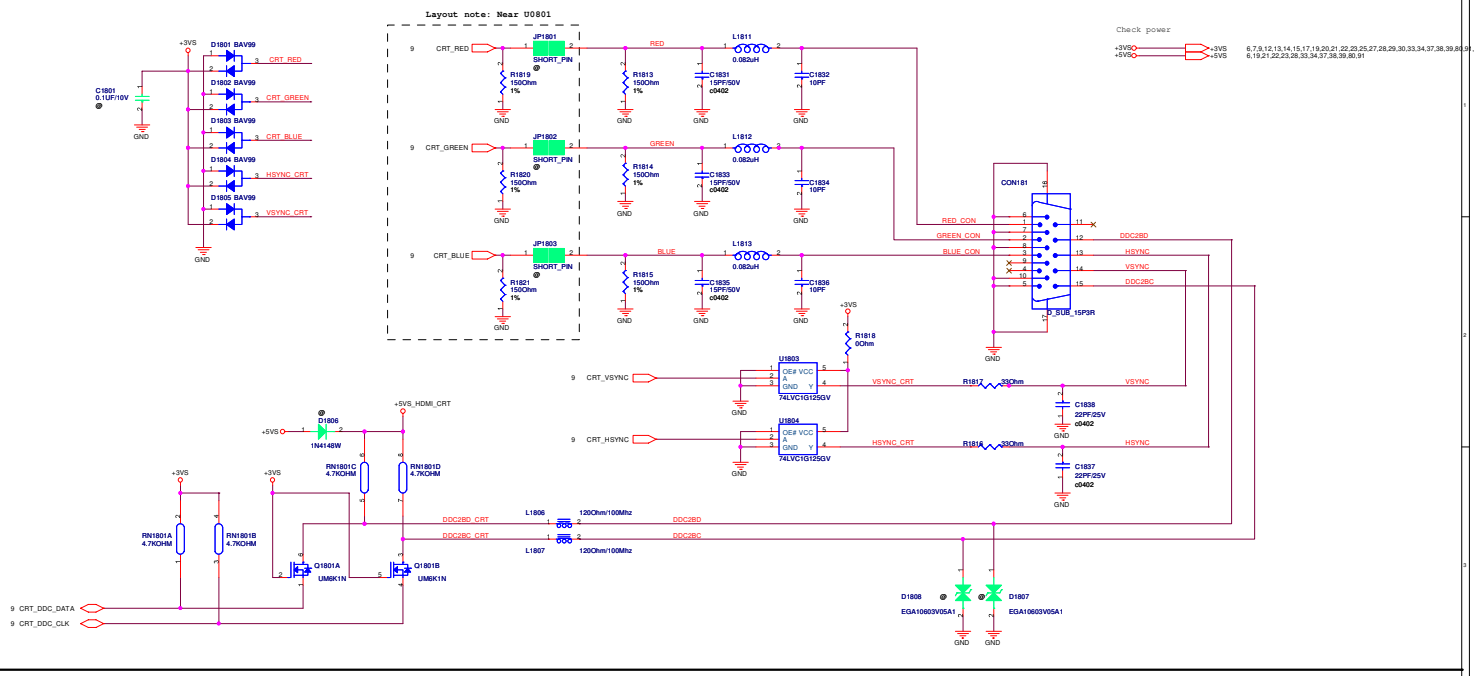


TV

<Variant Name>

ASUSTeK COMPUTER INC

Title : CRT

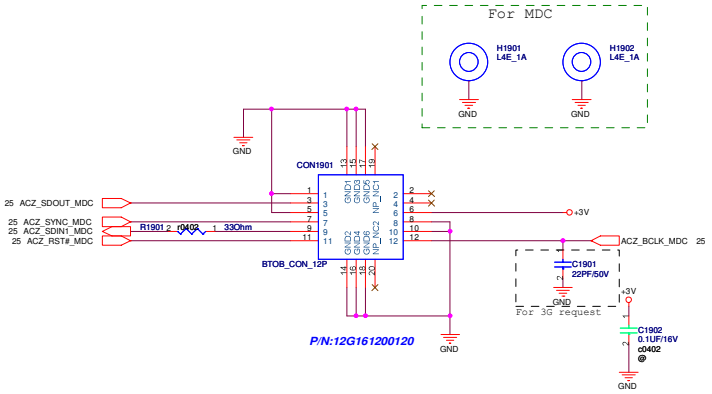
Engineer:

Size	Project Name	Rev
C	P9B	2.02

Date: 日 四月 26, 2007 Sheet 18 of 94

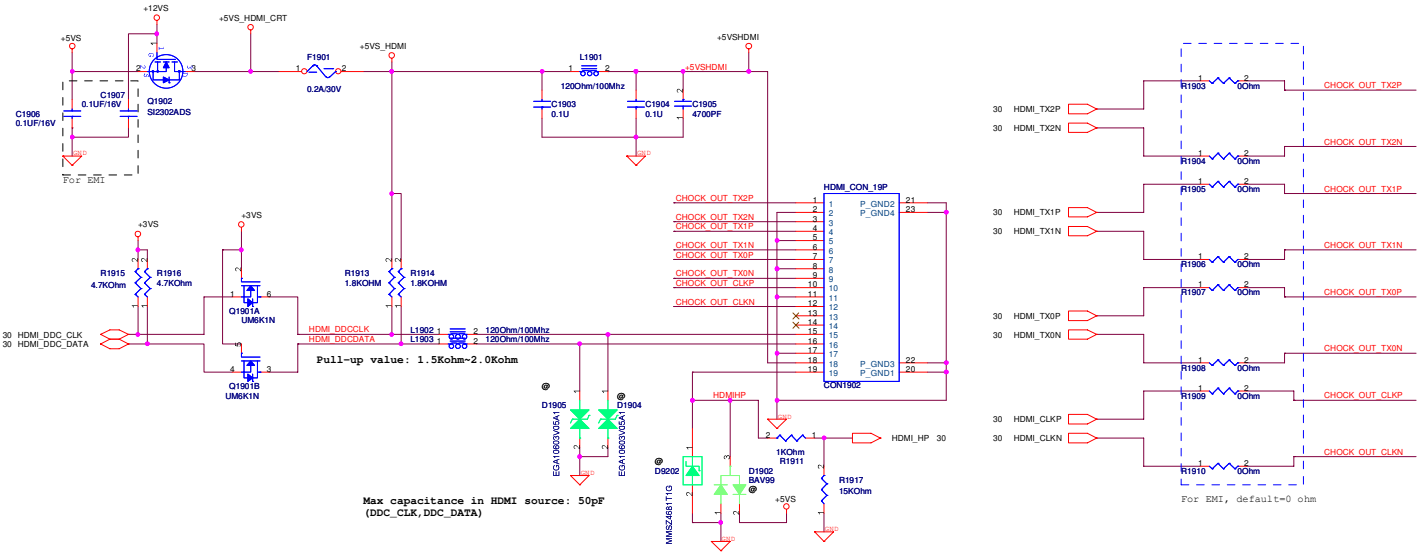
<< Kennedy_Zhang >>

MDC CON.



TP1 voltage spec: 4.8V~5.3V

HDMI CON.



Note:
1. L1901,L1902,L1903: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant pins of SII1392.

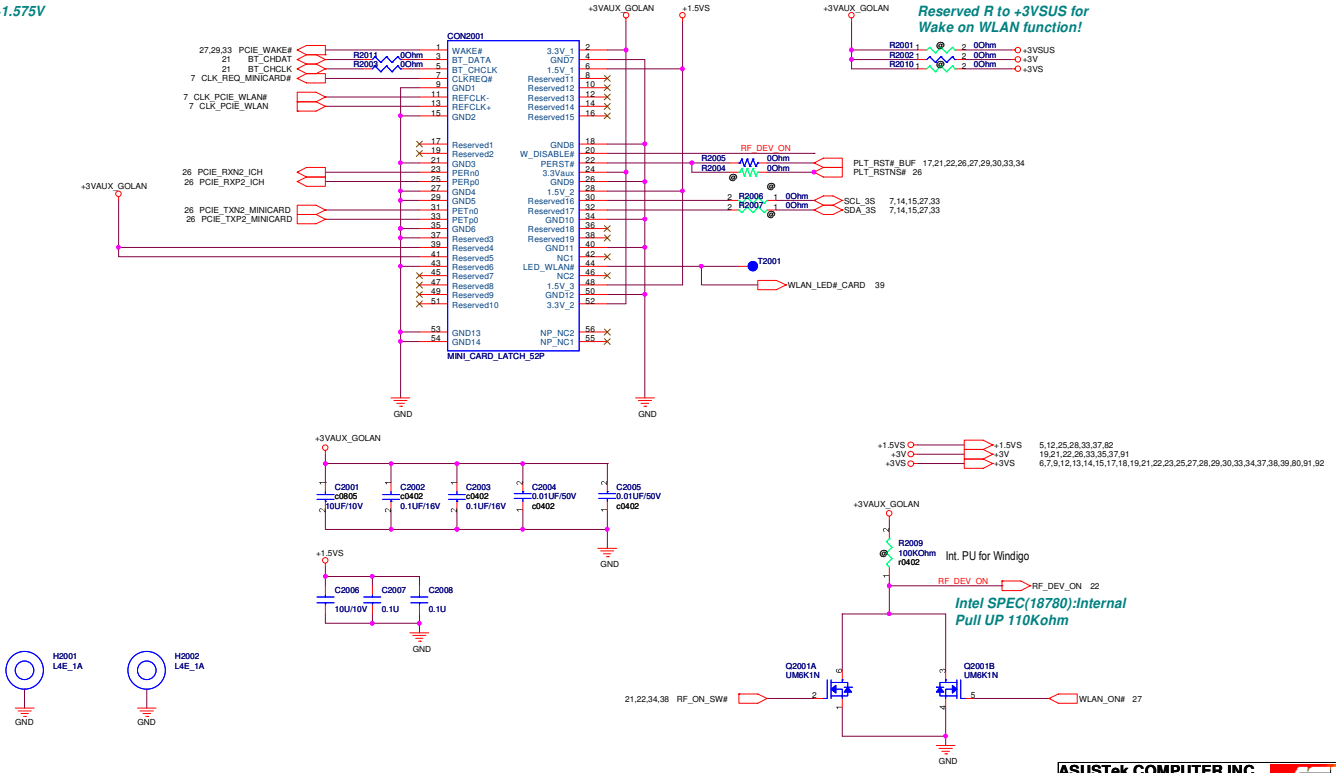
ASUSTek COMPUTER INC.		
4 Fl., No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC		
Title: MDC,HDMI CON		
Size: Custom	Document Number: F9E	Rev: 2.02
Date: 星期六, 六月 25, 2007	Sheet 19 of 94	

<< Kennedy_Zhang >>

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

P/N : 12G030000523

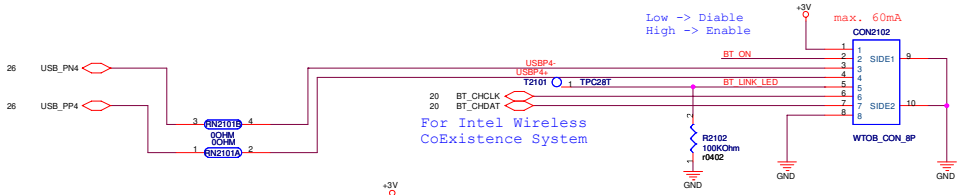
WLAN

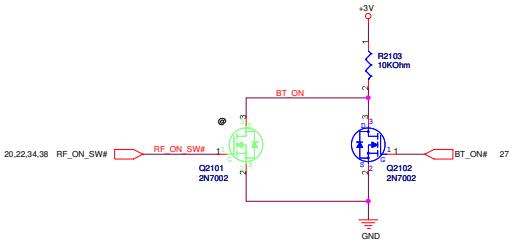


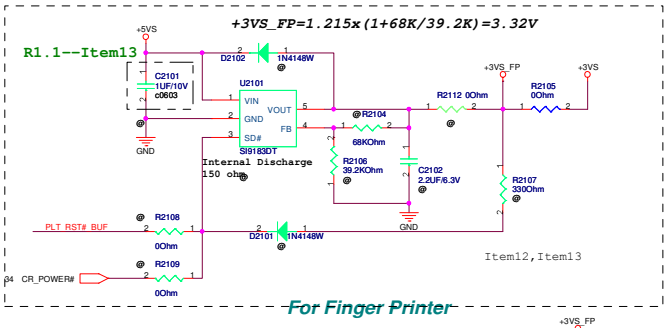
H2001 L4E_1A
H2002 L4E_1A
GND

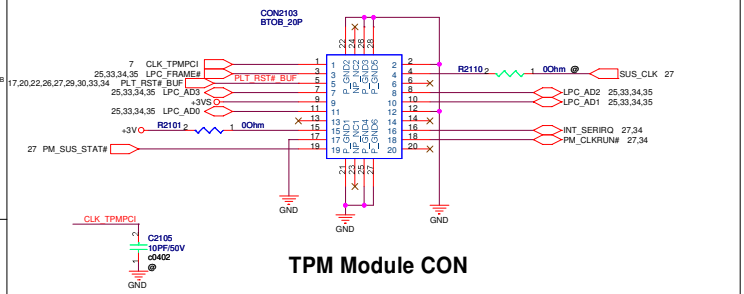
ASUSTek COMPUTER INC.		
4 FL, No.150, Li-Te Rd, Peitou, Taipei,Taiwan, ROC		
Title: MINI CARD--(1)		
Size: Custom	Document Number: F9E	Rev: 2.02
Date: 星期五, 六月 25, 2007	Sheet 20 of 94	

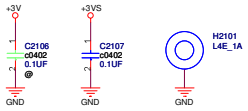
<< Kennedy_Zhang >>

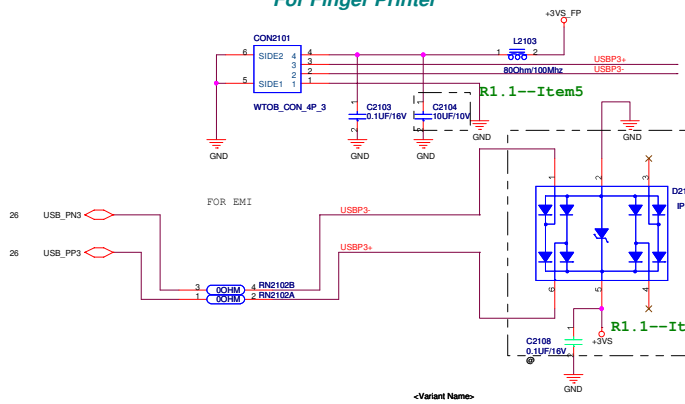












<variant_name>

ASUSTeK COMPUTER INC

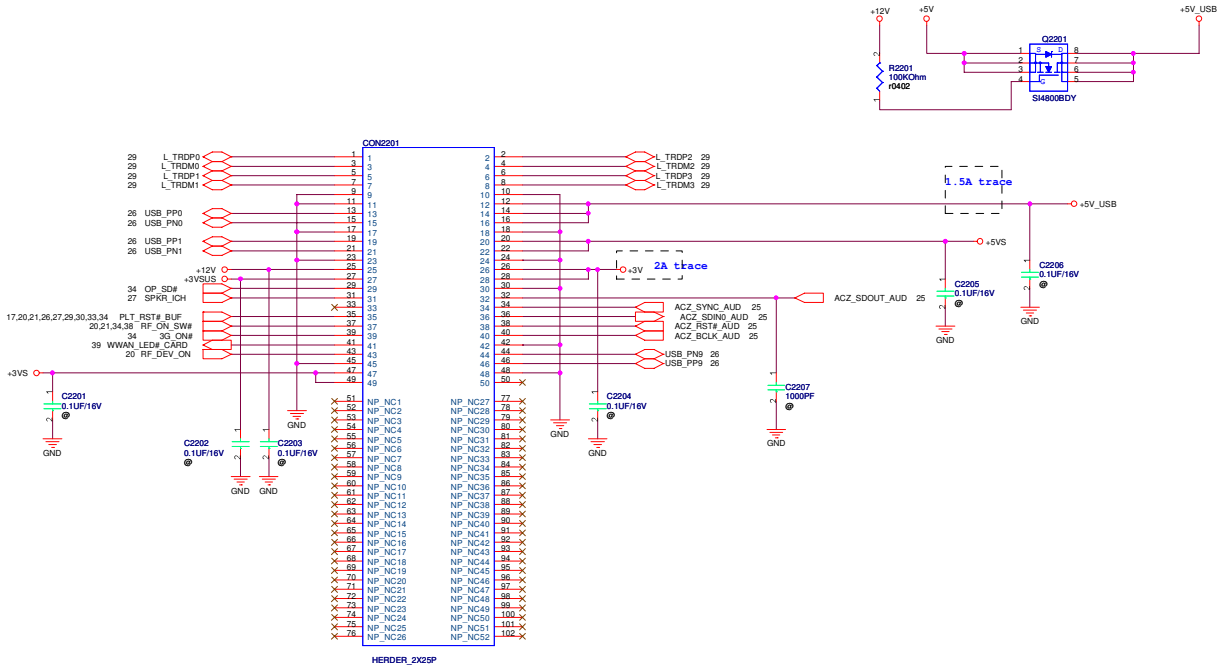
Title : B/T,F/P& TPM

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 21 of 65

<< Kennedy_Zhang >>



<Variant Name>

Title : B TO B CONN(M)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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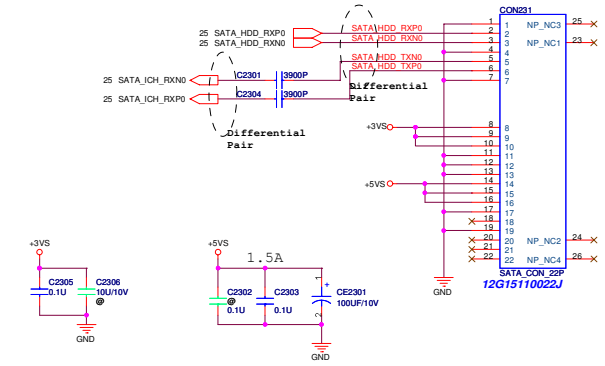
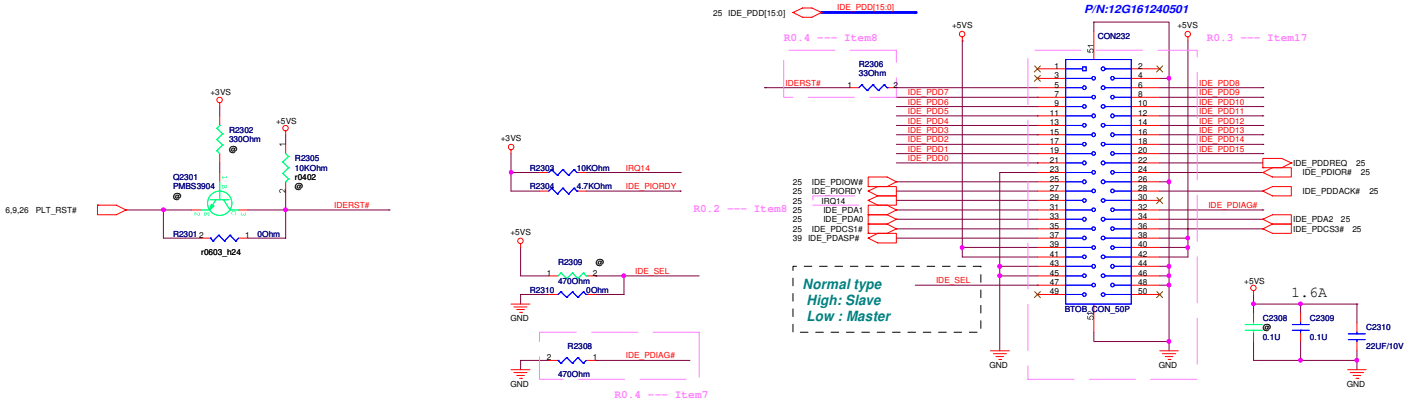
<< Kennedy_Zhang >>

SATA HDD CON



PATA CD-ROM CON



<Variant Name>

ASUSTeK COMPUTER INC

Title : HDD & CDROM

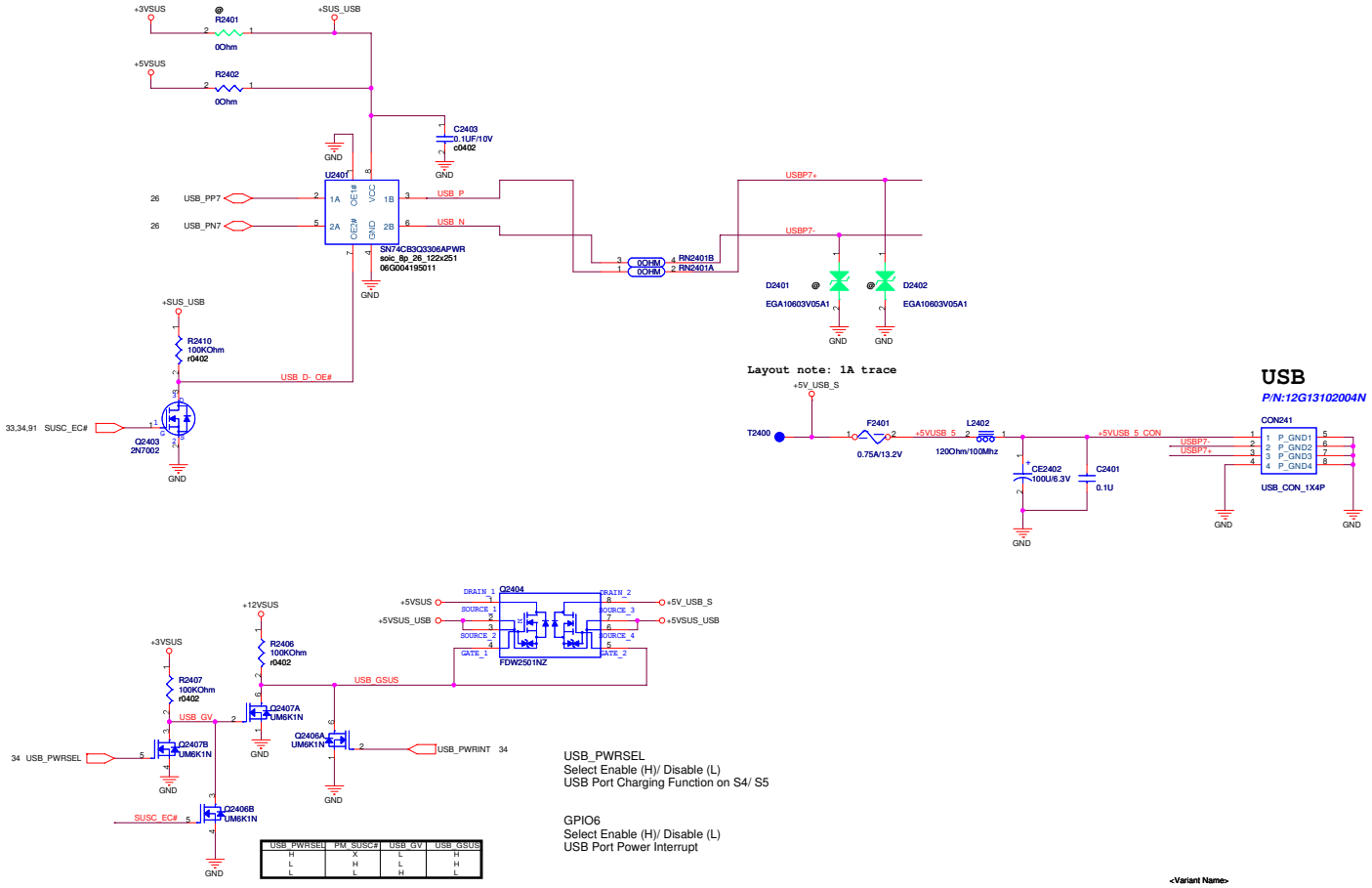
Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 十月 25, 2007 Sheet 23 of 94

<< Kennedy_Zhang >>

+SUS_USB:
+3VSUS for 06G016071010,SN74CB3Q3306APWR,cost=H
+5VSUS for 06G004195011,SN74CBTD3306PWR,cost=L



USB_PWRSEL	PM_SUSC#	USB_GV	USB_GSUS
H	X	L	H
L	H	L	H
L	L	H	L

USB_PWRSEL
Select Enable (H)/ Disable (L)
USB Port Charging Function on S4/ S5

GPIO6
Select Enable (H)/ Disable (L)
USB Port Power Interrupt

USB

P/N:12G13102004N

<Variant Name>

Title : USB PORTS

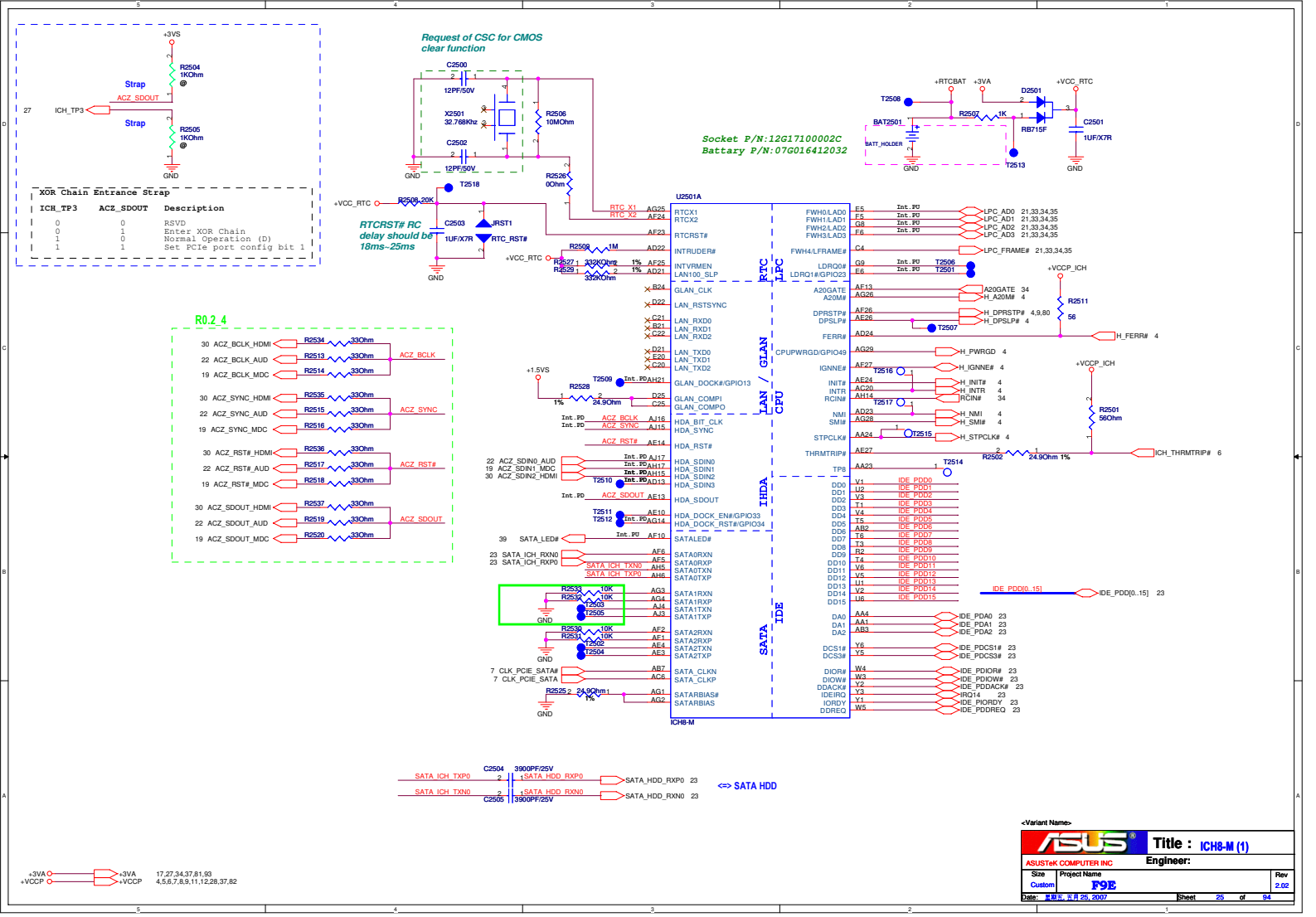
ASUSTeK COMPUTER INC

Engineer:

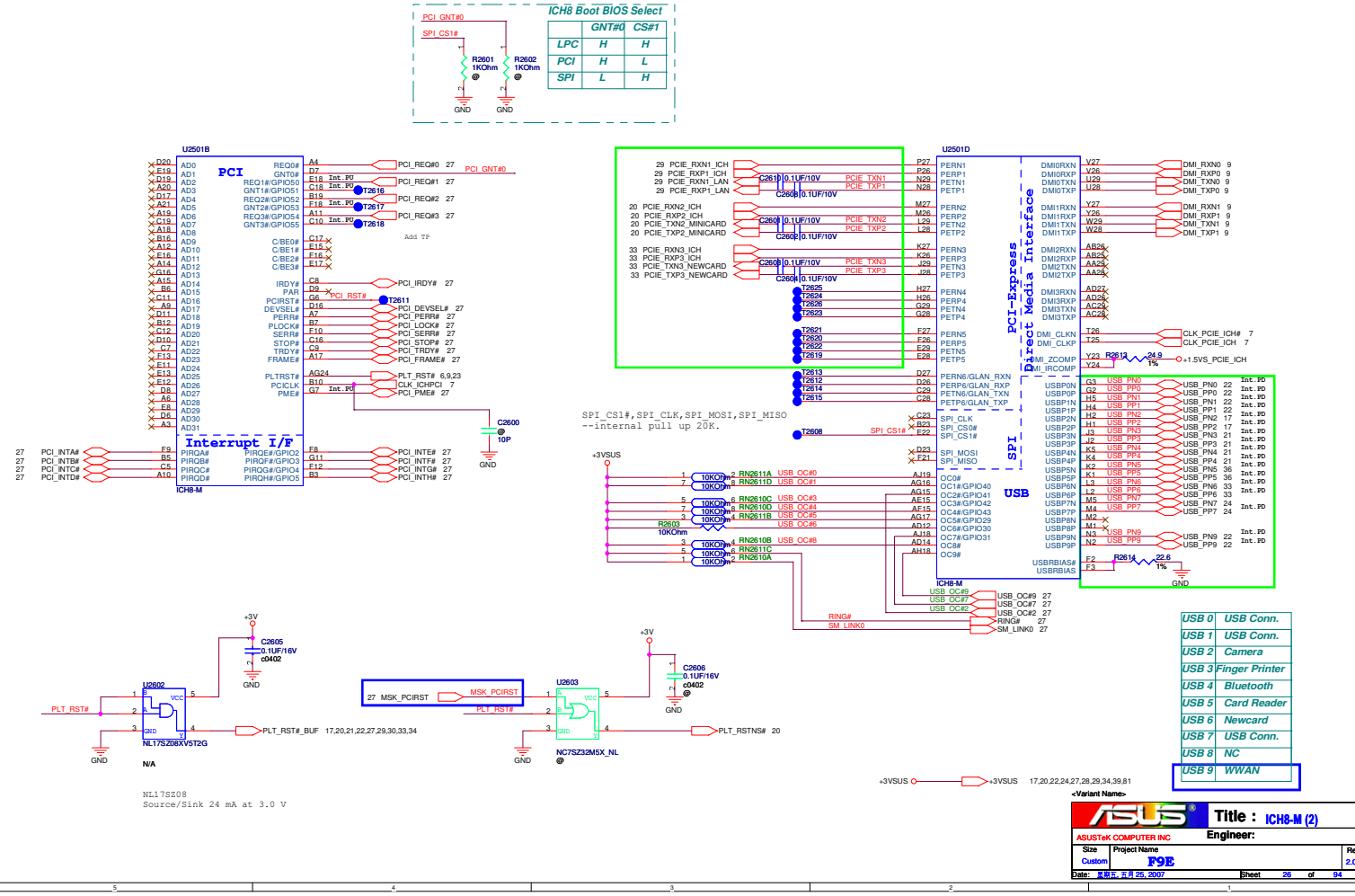
Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 24 of 94

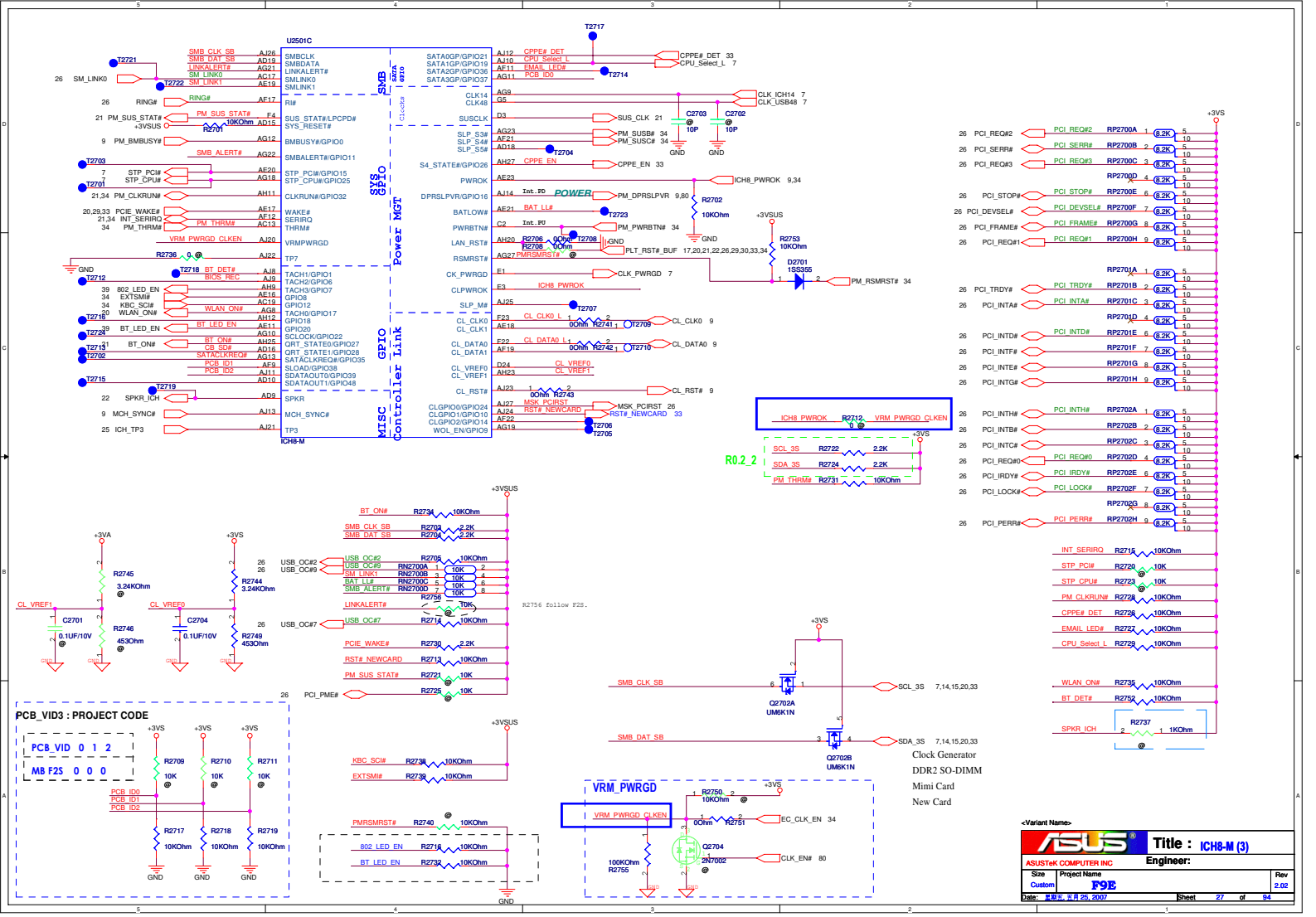
<< Kennedy_Zhang >>



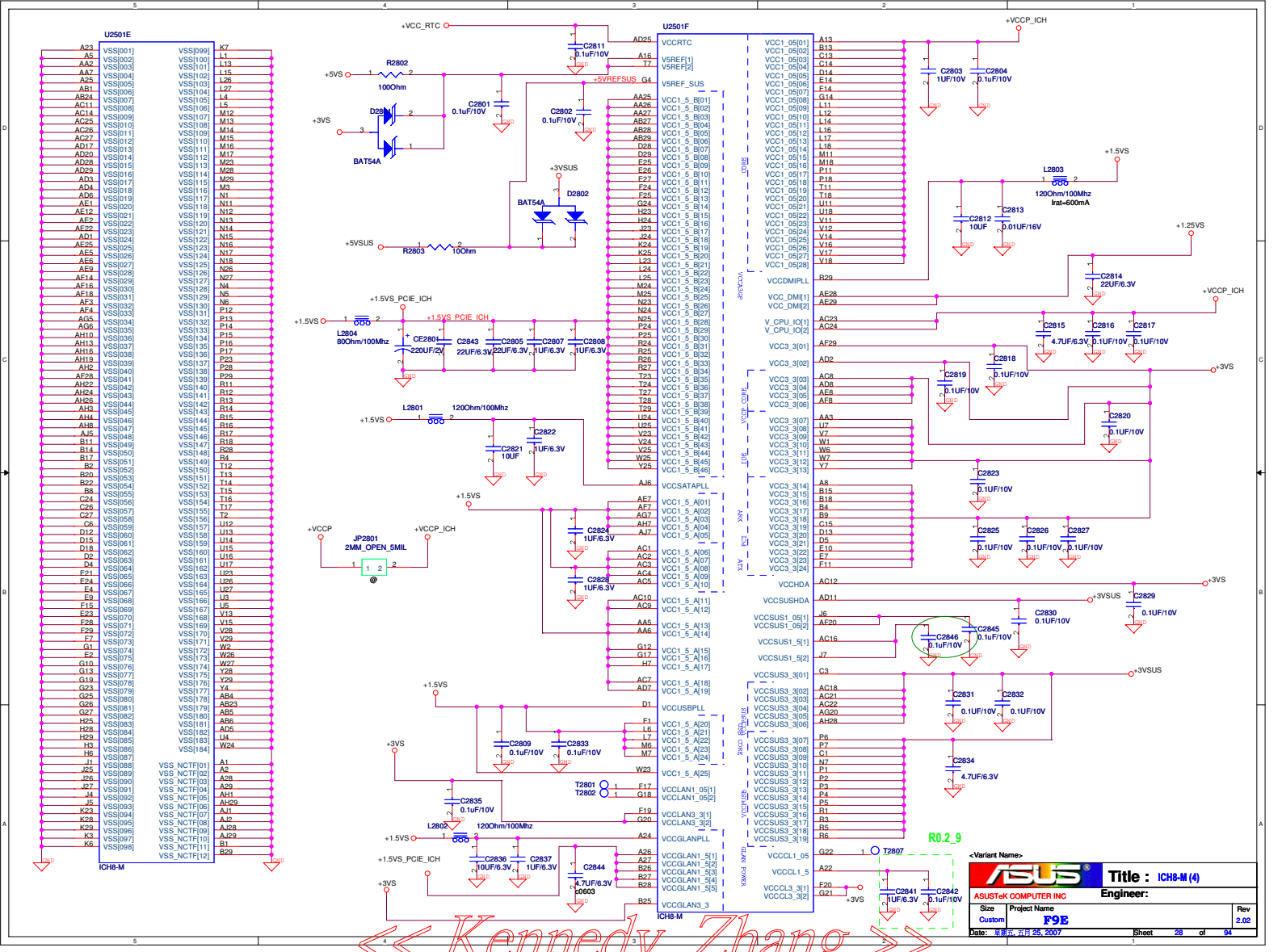
<< Kennedy_Zhang >>

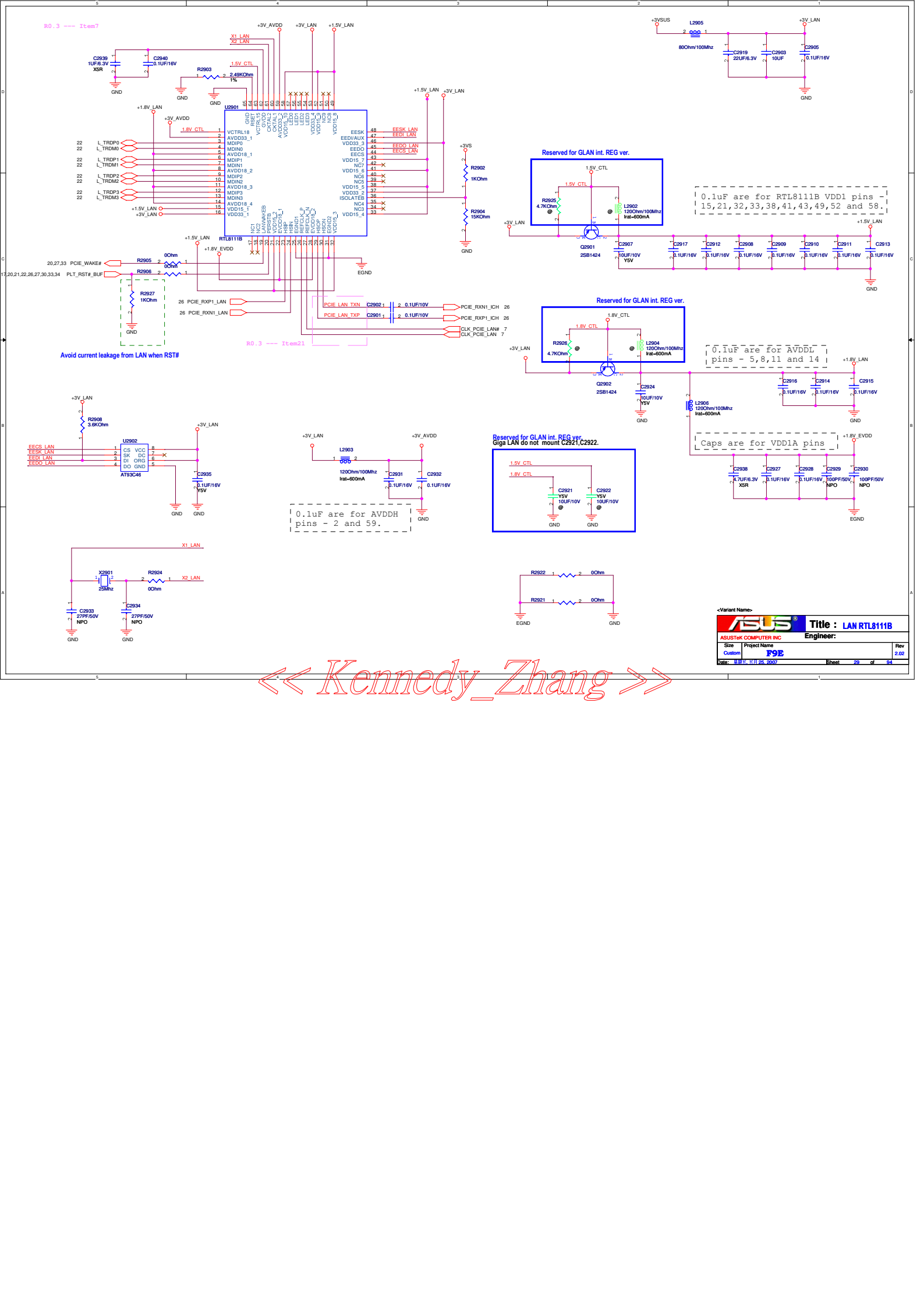


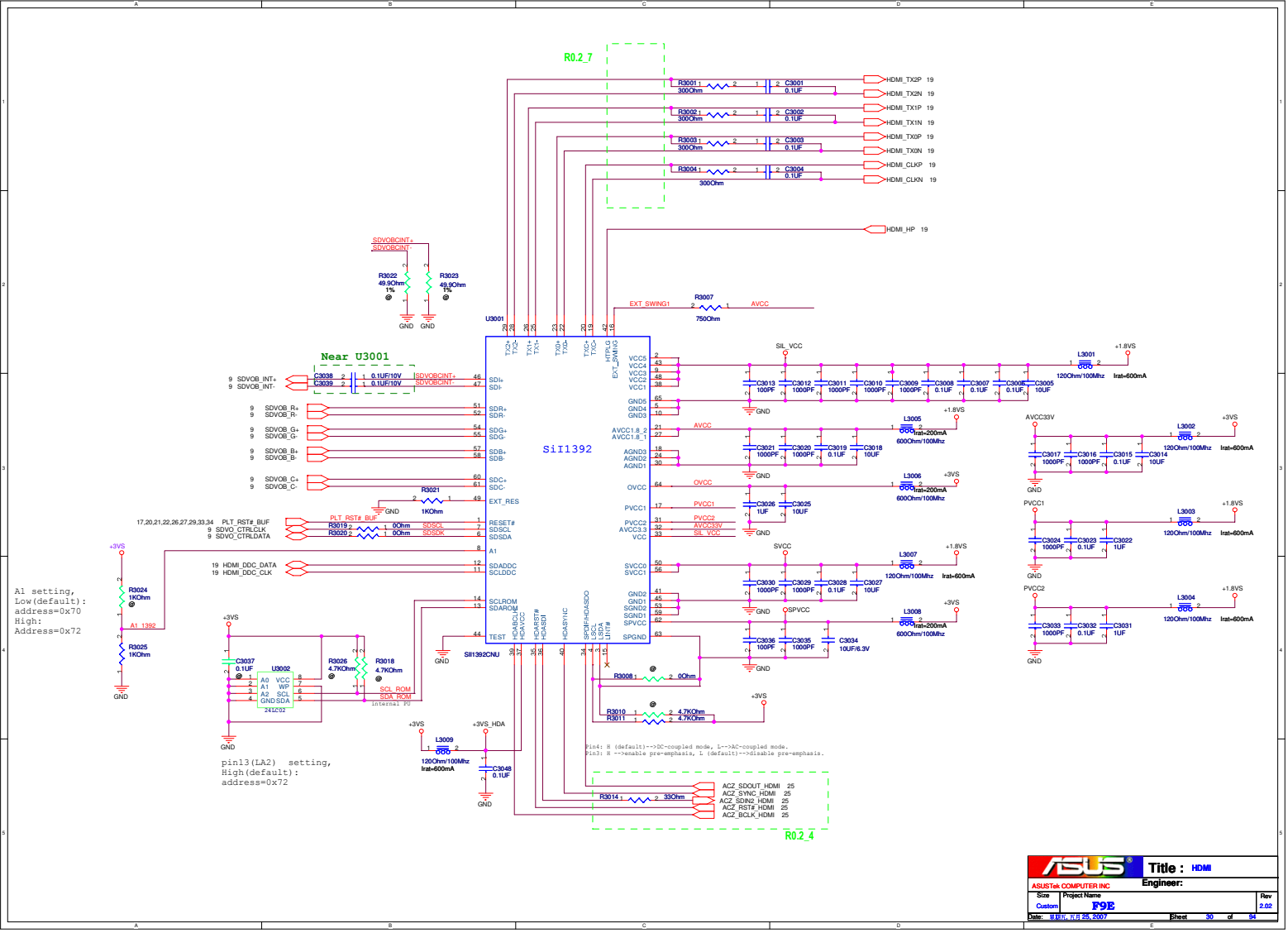
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>


U2501E
ICH8-M
U2501F
ICH8-M
+VCC_RTC
+5VS
+3VS
+5VSUS
+5VREFSUS
+1.5VS
+1.5VS_PCIE_ICH
+VCCP
+VCCP_ICH
+1.25VS
+3VSUS
R2802
100Ohm
R2803
100ohm
D2801
BAT54A
D2802
BAT54A
L2801
120Ohm/100Mhz
L2802
120Ohm/100Mhz
L2803
120Ohm/100Mhz
Irat=600mA
L2804
80Ohm/100Mhz
JP2801
2MM_OPEN_5MIL
T2801
T2802
T2807
R0.2_9
<Variant Name>
Title : ICH8-M (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
F9E
Rev
2.02
Date: 星期五, 五月 25, 2007
Sheet 28 of 94
<< Kennedy_Zhang >>


R0.3 --- Item7
RTL8111B
U2901
U2902
AT93C46
Avoid current leakage from LAN when RST#
Reserved for GLAN int. REG ver.
Reserved for GLAN int. REG ver.
Giga LAN do not mount C2921,C2922.
0.1uF are for RTL8111B VDD1 pins - 15,21,32,33,38,41,43,49,52 and 58.
0.1uF are for AVDDL pins - 5,8,11 and 14
Caps are for VDD1A pins
0.1uF are for AVDDH pins - 2 and 59.
R0.3 --- Item21
Title : LAN RTL8111B
ASUSTeK COMPUTER INC
Engineer:
Project Name F9E
Sheet 29 of 94
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

Title : EMPTY

ASUSTek COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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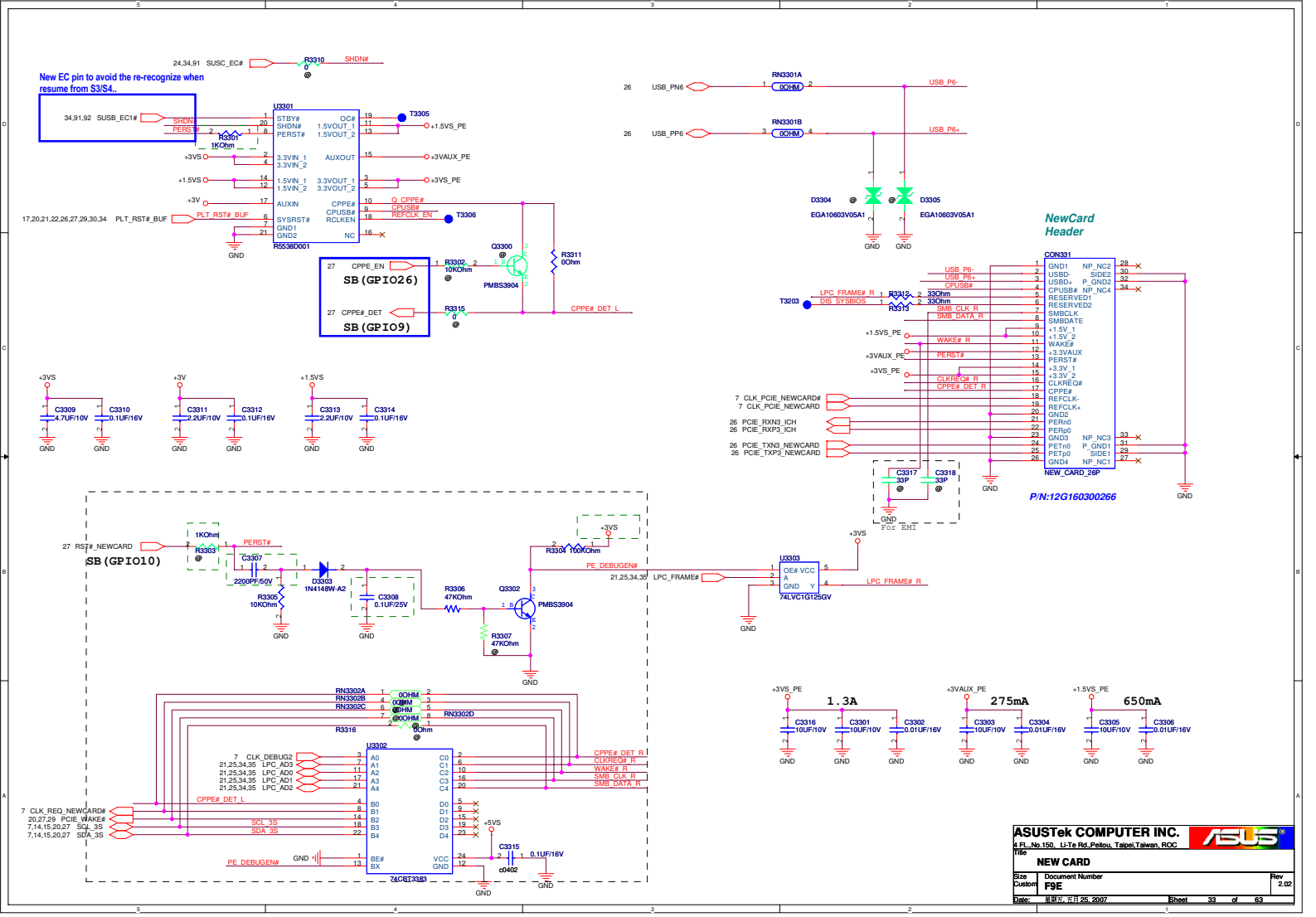
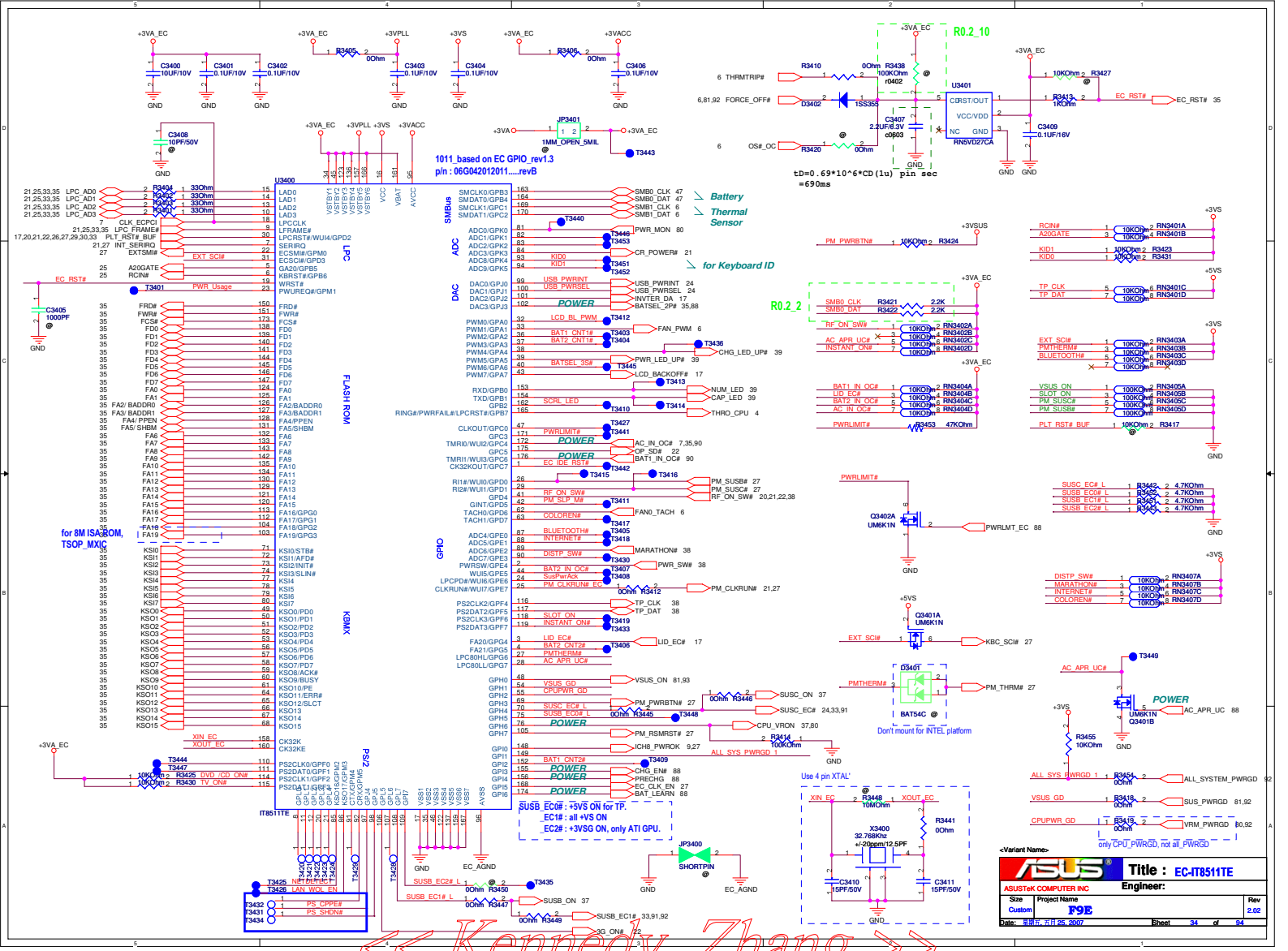


<< Kennedy_Zhang >>


R0.2_10
R0.2_2
U3400
IT8511TE
1011_based on EC GPIO_rev1.3
p/n : 06G040212011.....revB
Battery
Thermal Sensor
for Keyboard ID
POWER
for 8M ISA ROM, TSOP_MXIC
SUSB_EC0# : +5VS ON for TP.
_EC1# : all +VS ON
_EC2# : +3VSG ON, only ATI GPU.
Use 4 pin XTAL'
Don't mount for INTEL platform
only CPU_PWRGD, not all_PWRGD
tD=0.69*10^6*CD(1u) pin sec
=690ms
Title : EC-IT8511TE
ASUSTeK COMPUTER INC
Engineer:
Project Name
F9E
Rev
2.02
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<Variant Name>
Kennedy_Zhang

EC Hardware Strapping

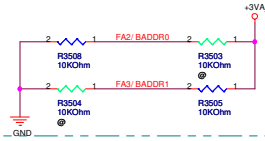
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

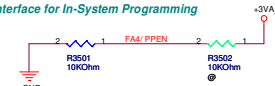


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

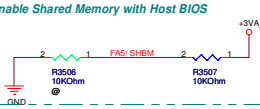
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

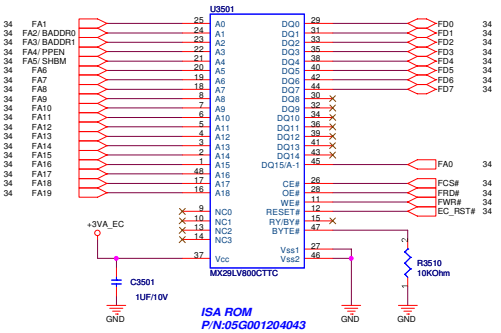
0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



ISA ROM_TSOP

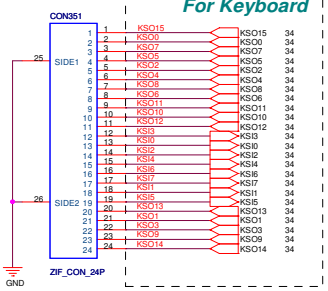
8M TSOP _ MXIC

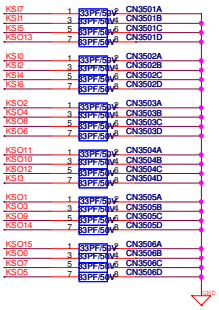


ISA ROM
P/N:05G001204043

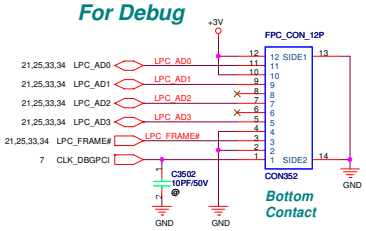
For Keyboard

P/N:12G182402404



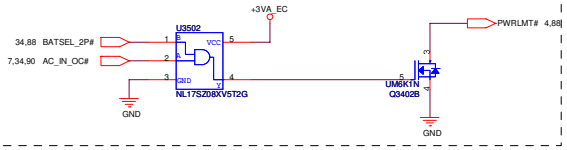


For Debug



Bottom Contact

PWRLMT Circuit: For 65W adaptor.



<Variant Name>

ASUSTeK COMPUTER INC

Title : ISA_ROM&KB conn

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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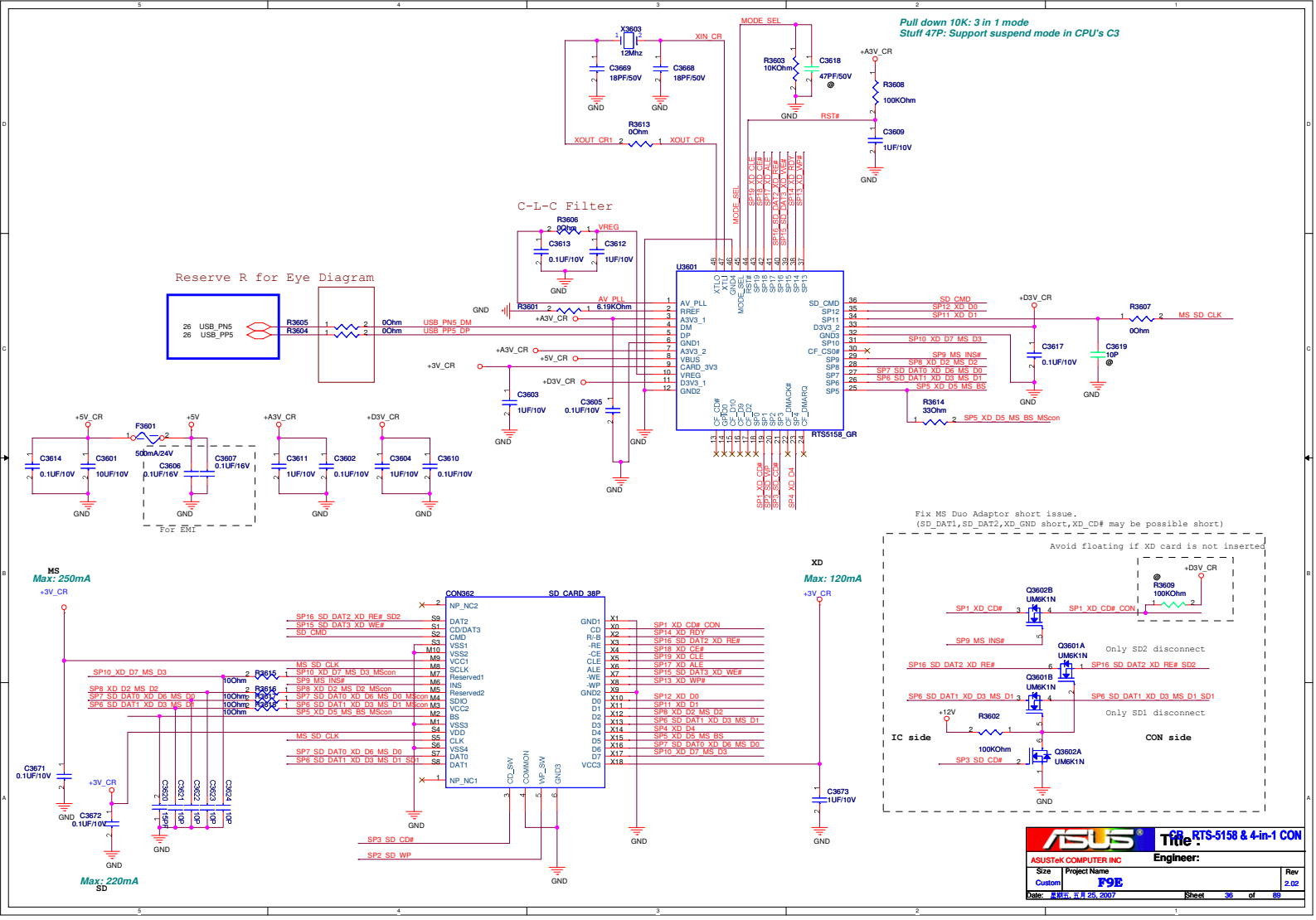
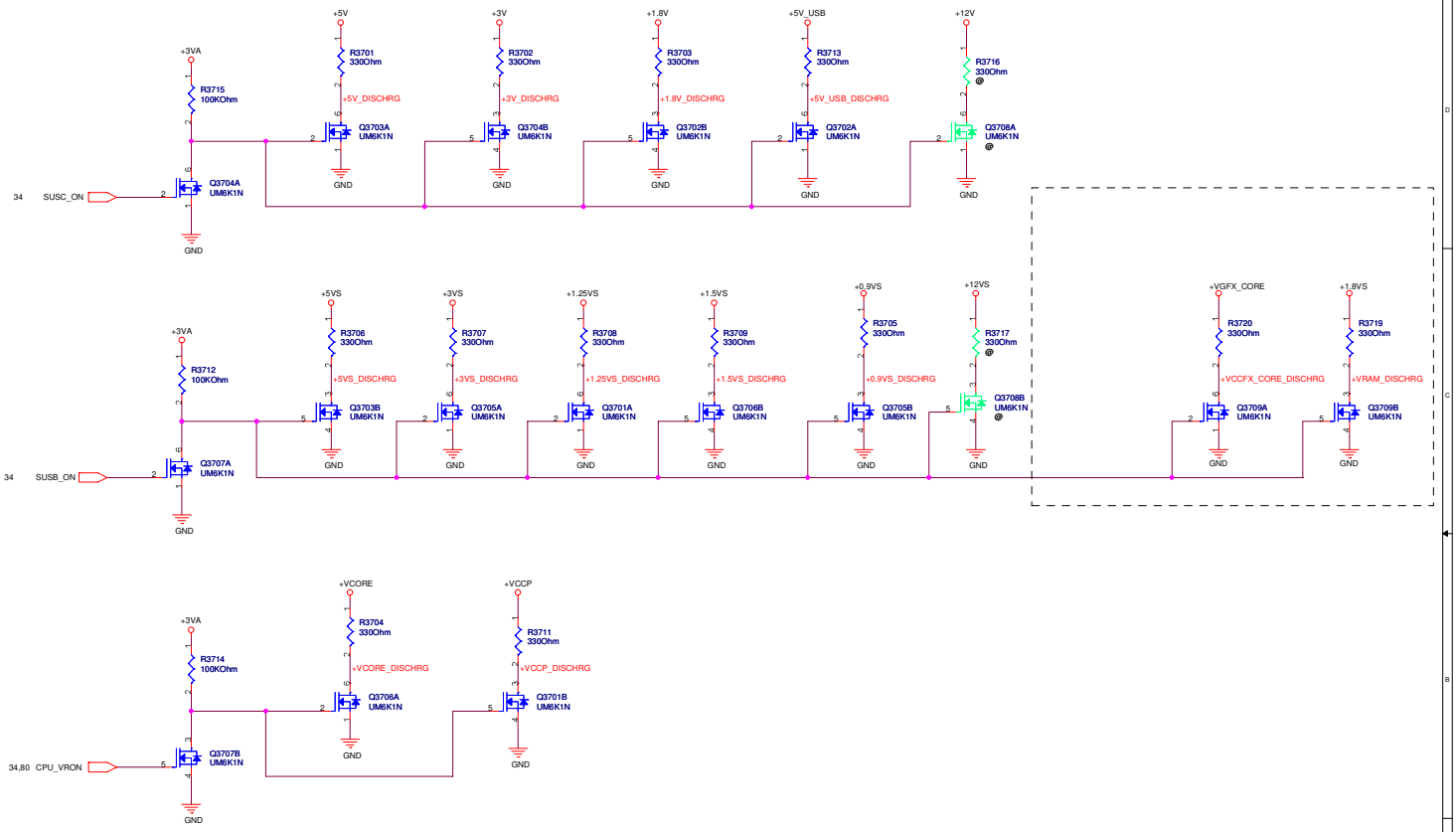
<< Kennedy_Zhang >>

GND GND



<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC

Title : DISCHARGE

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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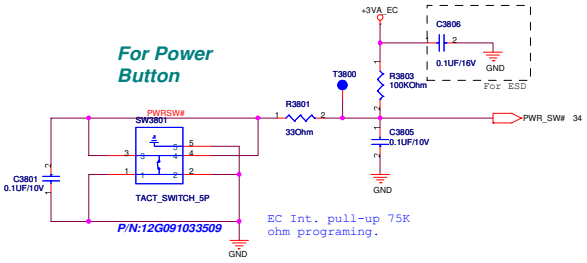
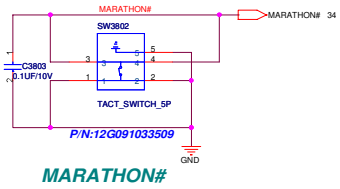
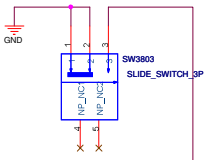
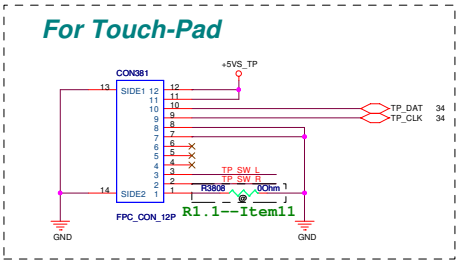
<< Kennedy_Zhang >>

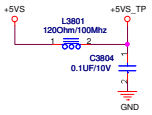


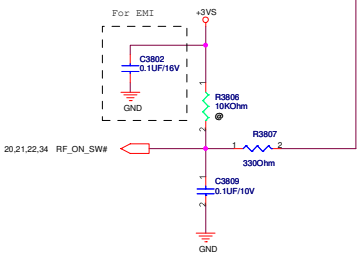


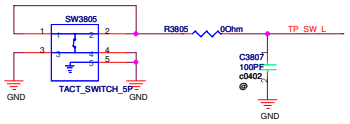


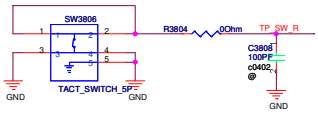
BT/WLAN SW







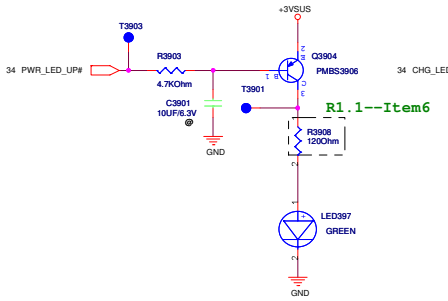




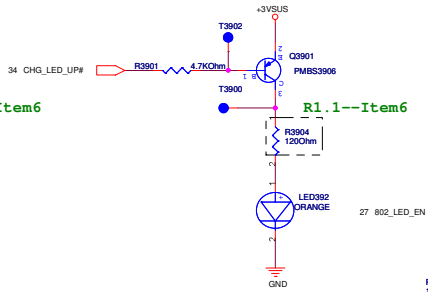
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	Engineer:
Size: Custom	Project Name: F9E	Rev: 2.02
Date: 星期六, 六月 25, 2007	Sheet 38 of 94	

For PWR LED

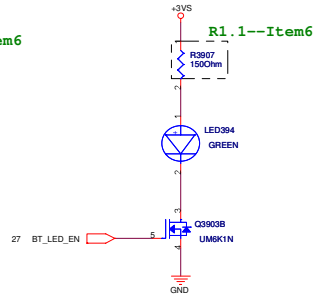


For BATTERY LED

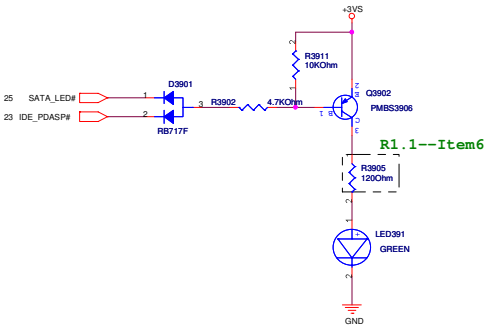


For WireLess LED

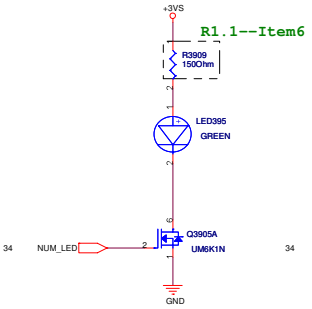
For BT LED



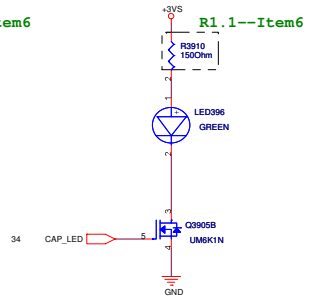
For SATA/IDE LED



For Num Lock



For Cap. Lock



<Variant Name>

ASUSTeK COMPUTER INC	Title : LEDs	
	Engineer:	
Size: Custom	Project Name: F9E	Rev: 2.02
Date: 星期五, 五月 25, 2007	Sheet 39 of 94	

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C	F9E	2.02

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<< Kennedy_Zhang >>

<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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<Variant Name>

Title : EMPTY

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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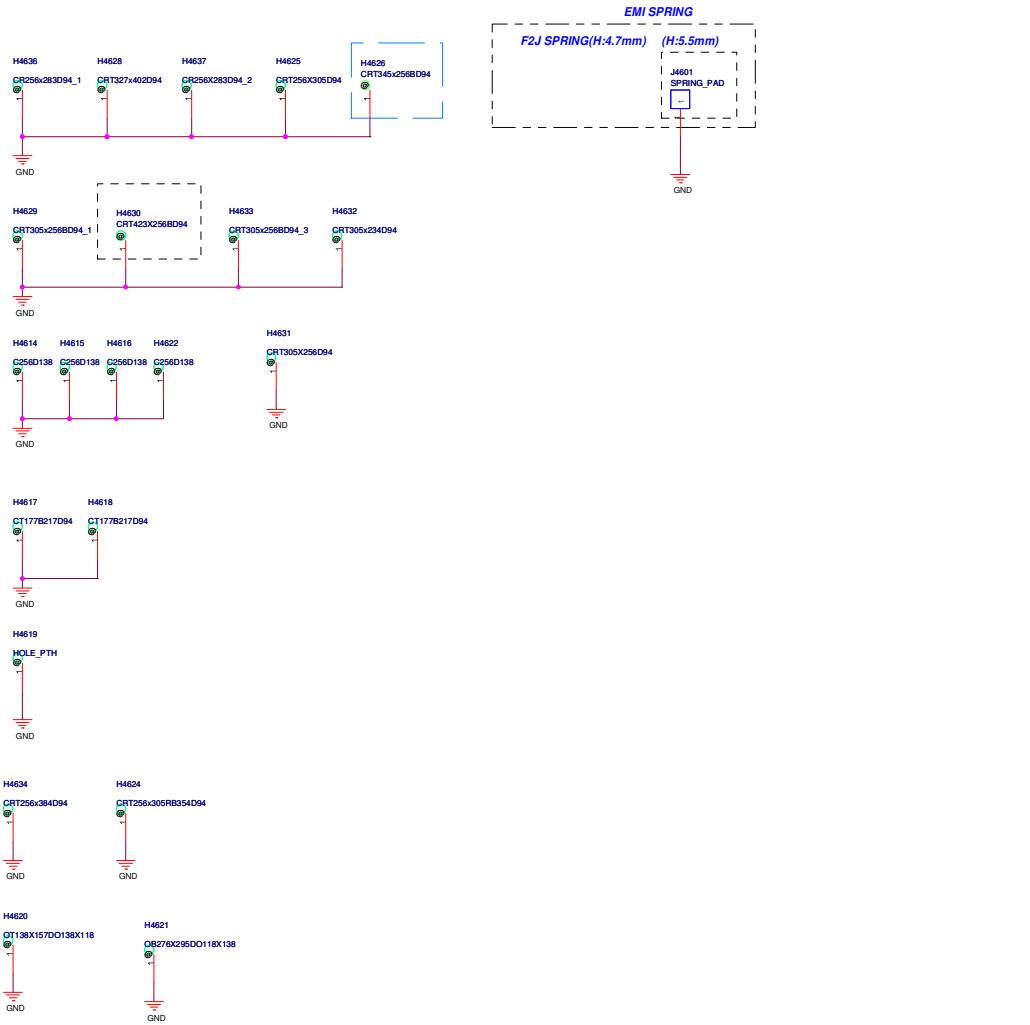

<Variant Name>

ASUSTeK COMPUTER INC

Title : HDD & CDROM

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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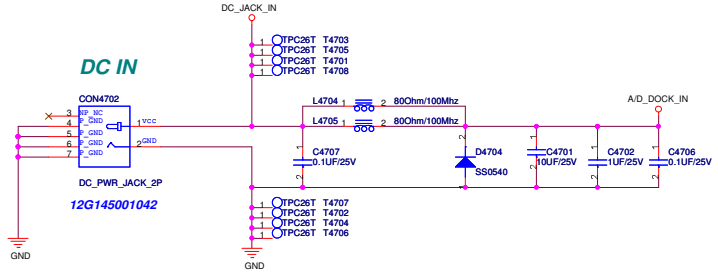
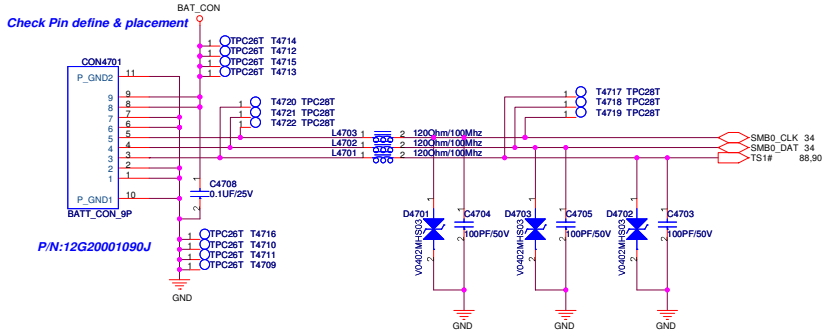
<< Kennedy_Zhang >>

DC IN



BAT IN



<Variant Name>

ASUSTeK COMPUTER INC

Title : DC & BAT IN

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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F9E R0.1 => R0.2

(Release on 2006/12/07)

1. Page7: Mount R0758 for PCIE 7, 5, 3 not controlled.

2. Page27,34: For SM bus signal quality improvement.
   Change R2722, R2724, R3421 & R3422 to 2.2 k ohm.

3. Page7: Change D0701,D0702 to R0733,R0734.
   Because U3302 is changed from +5V to +5Vs. (No S3 leackage)

4. Page25,30: Move resistor from page 30 to page 25 for layout guide.
   ACZ_SDOUT_HDMI: R3012-->R2537
   ACZ_RST#_HDMI : R3015-->R2536
   ACZ_SYNC_HDMI : R3013-->R2535
   ACZ_BCLK_HDMI : R3016-->R2534

5. P.08: Delete 0ohm R0927,R0930,R0931,R0933,R0935;
   Add resistors according to Intel's MCH sighting 306022.
   R0948: GVR_VID1 (Intel's MCH GFX_VID0) 22-kΩ pull-down
   R0949: GVR_VID2 (Intel's MCH GFX_VID1) 22-kΩ pull-down
   R0950: GVR_VID3 (Intel's MCH GFX_VID2) 22-kΩ pull-up to 3.3VS
   R0951: GVR_VID4 (Intel's MCH GFX_VID3) 22-kΩ pull-down

   P.86 GVR_VR_EN: Select option B,reserved option A.
   Option A: Route GMCH_GFX_VR_EN signal to graphic VR enable pin.
   Add a 30-kΩ pull-up to 3.3S V and a 100-kΩ pull-down on the board on this signal.
   Option B: Leave GMCH_GFX_VR_EN no connect and route SLP_S3# to GFX VR Enable pin.

6. Fixed component name:
   P.04: R402 -->R0402
   P.06: CE3601-->CE0602
   P.07: Q701A -->Q0701A.
   P.34: Q9202 -->Q3402

7. Delete unused net:
   P.30: HDMITX0P,HDMITX0N,
   HDMITX1P,HDMITX1N,
   HDMITX2P,HDMITX2N,
   HDMICLKP,HDMICLKN,

8. P.07: Delete R0765,R0766,R0781,R0782 for useless.

9. P.28: Mount C2841,C2842 for Intel's recommendation.

10. P.34: DNI R3438.

11. Updade page 14,15,17,23,29,36 as F9S.

F9E R0.2 => R0.3

(Release on 2007/01/02)

1. P.07: Exchange net CLK_DEBUG2 & CLK_ECPCI to follow with F9S.
2. P.11: Change JP1102,JPT103 from 2MM_OPEN_5MIL to 3MM_OPEN_5MIL for high current.
3. P.27: Delete redundant net CPPE_EN
4. P.19: Correct HDMI_HP type from output to input for net connection.
5. P.26: Rename PCIE_TXN1_LAN,PCIE_TXP1_LAN to PCIE_RXN1_LAN,PCIE_RXP1_LAN to follow F9S
6. P.34: Add net PWR_MON for power monitor of VCORE
7. P.34: Add R3423,R3431 for EC spec. (KID0,KID1)
8. P.34: DNI R3455 for EC spec.
9. P.34: Del R3426 because it can be NC in EC spec.

F9E R0.3 => R0.4

(Release on 2007/01/10)

1. P.88: CE8800.CE8801change toPOSCAP(chemicn 27uF/25V-->15uF/25v).
   for layout's high limit .
2. P.80: CE8005 change from (chemicon 27uF/25V*1) to POSCAP
   CE8003.CE8005 (15uF/25V *2) for layout's high limit .
3. P.80: Change colay MOSFET Q8000~Q8007.Q8600.Q8601.Q8408 11pcs
   to standard SO-8 for 6 layer PCB layout.
4. P.86: 1.Update F9E power schematic at P86 to combine power and signal ground
   because different ground is difficult for layout.
5. P.86: Connect R8636.2,R8635.1 to U8600.31 for pull up correction.
6. P.81: Update R8134 from 51kohm to 49.9kohm to adjust +5VO feedback.(5.18V-->5.09V)
7. P.25: Change BAT2501 from 12G171000002C to 12G201100200 for layout and costdown.
8. P.27: DNI R2740 and add R2740,D2701 to prevent auto power on issue.
9. P.19: Correction net: Exchange HDMI_DDC_DATA,HDMI_DDC_CLK
10. P.19: Delete redundant resistor R1912.
11. P.25: Change C2500,C2502 from 22pF to 15pF to meet XTAL requirement
12. P.09: Change R0936 from 1.3k ohm to 1.2k ohm to increase VGA Vpp.
13. P.36: Change page 36 for spec change. (RTS5117-->RTS5158)
14. P.88: DNI R8808 for 3S battery.
15. P.86: Delete JP8304 for layout.
16. P.86: Add JP8805 to avoid to pull BAT feedback signal to BAT power.
17. P.30: Add +3VS_HDA to ensure power trace and move C3408 from +3VS to +3VS_HDA
18. P.30: Add R3407 and connect GFX_VR_PWRIN to EC's GPK2 port for future use
19. P.09,P.13,P.26 : Change DMI from X4 to X2.
    Delete DMI_TXN2,DMI_TXP2,DMI_RXN2,DMI_RXP2,DMI_TXN3,DMI_TXP3,DMI_RXN3,DMI_RXP3
    Mount R1301 to select DMIX2

F9E R0.4 => R0.41

(Release on 2007/01/12)

1. P.07: Change X701 from 07G010Q01431 to 07G010S01430 for layout.
2. P.20: Correct H2001,H2002 to follow F9S.
3. P.25: Change components for layout:
   a. X2501: 07G010303270-->07G010413277,(315x150-->272x55)
   b. C2500: 11G232022004320-->11G233012004030,(22p-->12p)
   c. C2502: 11G232022004320-->11G233012004030,(22p-->12p)
4. Correct component name: Q9201B -->Q1901B
5. Combine 2 H2N7002 to 1 UM6K1N:
   a. P.20: Q2001-->Q2001A,Q2002-->Q2001B
   b. P.27: Q2702-->Q2702A,Q2703-->Q2702B
   c. P.34,P.35: Q3402-->Q3402A,Q3501-->Q3402B
   d. P.88: Q8806-->Q8806A,Q8809-->Q8806B
      Q8805-->Q8805A,Q8803-->Q8805B
      Q8808-->Q8808A,Q8812-->Q8808B
6. P.06: Correct component name Q605 -->Q0605
7. P80,P84,P86: SO8 footprint not colay
   Q8001~Q8007,Q8408,Q8600,Q8601
8. P80,P88: DNI D8000,D8001,D8801 for costdown
9. P.18: Fix: Add R1819,R1820,R1821 for layout.

F9E R0.41 => R0.42

(Release on 2007/01/15)

1. P.30: Fix: Change R3009 from 4.7Kohm to 0ohm.
2. P.30: Fix: Change R3006 from 10Kohm to 15Kohm.
3. P.30: Fix: Delete C3040~C3047 because of redundant.
4. P.19,20: For CTS test:
   a. P.19: Delete C1906,C1907.
   b. P.19: Add D1904,D1905 as ESD backup solution.
   c. P.19: Change Q1901A_2,Q1901B_5 gate votage(+5Vs-->+3Vs).
   d. P.19,18: Delete D1901,DNI D1806,AddQ1902.
      Net change: +5VS_HDM,+5VS_CRT-->+5VS_HDMI_CRT
   e. P.19: Change L1902,L1903. (600Ohm/100Mhz-->120Ohm/100Mhz)
   f. P.19: Change R1913,R1914. (2.2K-->1.8K)
   g. P.19,P.30: Move R3006-->R1917
   h. P.30: Change L3002,L3004,L3009.(600ohm/100Mhz-->120ohm/100Mhz)
5. P.12: Add Layout note: MCH_VTTLF1,MCH_VTTLF2,MCH_VTTLF3 is power trace.
6. P.81: Add JP8107,JP8108,Separate +5VO7+3VO output and discharge path

F9E R0.42 => R0.43

(Release on 2007/01/20)

1. Update power signal open pin to DNI and display.
2. P.14,P.15: SWAP M_A_DQ[0..63),M_B_DQ[0..63] for layout.
3. P9: Add net name M_A_A14_NB,M_B_A14_NB for layout.
4. P36: Change net name DM-->USB_PN5_DM,DP-->USB_PN5_DP for layout.
5. P46: Add CPU serew hole H4622.
6. P46: Delete C4600~C4604 for no use.
7. P11: Delete JP1101 for layout.
8. P30: Change R3007 from 10G2127500140300E to 10G2127500140300 for BOM.
9. P09: Change R0923,R0924,R0925 from 10G21275R014030DE to 10G21375R013010 for BOM.
10. P30: Change C3037 from 11-034310410 to 11G2321104161S0 for BOM.
11. P30: Fix: Change R3008 from 4.7Kohm@ to 0 ohm@.

F9E R0.43 => R0.44

(Release on 2007/01/23)

1. P.15: Swap M_B_DQ60,M_B_DQ57 for layout.
2. P.11: Correct +VCCP_GMCH to +VCCP.
3. P.16: Swap DDR termination signal for layout.
4. P.88: Change Q8802 from SI4431BDY to FDS6609A for cost down..
5. P.82: Delete JP8205 to meet layout request.
6. P.19,P.24: Correct D1904,D1905,D2400,D2401 from RSB6.8S to EGA10603V05A1.

F9E R0.44 => R0.45

(Release on 2007/01/24)

1. P.07: Change clock gen(U0701) from 06G011408011 to 06G011408012
2. For spec update to support S4/S5 USB charge function:
   a. P.81,P.91: Correct power raiting
      +5VA-->0.01A,+5VO-->7.252A,+5VSUS-->0.501A,
      +5VS-->5.251A,+12VS-->0.01A,+5V-->1.5A
   b. P.22,P24: Q2402-->Q2201,R2404-->R2201.
   c. P.24: Update Page 24.
   d. P.34: Add net USB_PWRINT,USB_PWRSEL

F9E R0.45 => R0.46

(Release on 2007/01/29)

1. P.26,P.27: Swap for layout
   a. SwapRN2700,R2705,R2714,RN2610,RN2611
   b. Delete RN2612,add R2603.
2. P.81,P.82,P.83: Change CE8100 CE8102 CE8202 CE8203 CE8300 CE8301
   for layout limit high
3. P.22: Add PLT_RST# BUF for Sierra WWAN compatible.
4. P.07: Add C07T8(10P) and C0725(10P) to meet edge rate spec.
5. P.07: Change R0707 from 33 ohm to 27 ohm to meet edge rate spec.

F9E R0.46 => R0.47

(Release on 2007/01/29)

1. P.24: Add R2401,R2402@ for test cost down solution.
2. P.27,P.31: Swap for layout: RP2700,RP2701,RP2702,RN3405

F9E R0.47 => R0.48

(Release on 2007/01/30)

1. P.22: Pin assignment change for I/O board:
   +3V: pin47,49 -->pin26,28; +3VS: pin26,28-->pin47,49
2. P.22: Add C2201~C2206 for EMI request
3. P21,P.24: Swap L2401,RN2101,RN3302.7,RN3302.8 for layout

F9E R0.48 => R0.49

(Release on 2007/02/1)

1. P.28: Change C2821 size from 0805 to 0603 for layout.
2. P.28: R2410_1: +3VSUS-->+SUS_USB for the better Vih.
3. P.22: DNI C2201~C2206.
4. P.21: Move C2108 to connect D2103.5 for EMI request
5. P.36: Add C36198 for EMI request
6. P.18: Add C1801@,D1807@,D1808@ for EMI request
7. P.18: Add D1705@,D1706@ for EMI request
8. P.24: Add D2401@,D2402@ for EMI request
9. P.36: Add C0726@ for EMI request

F9E R0.49 => R0.5

(Release on 2007/02/5)

1. P.12: Update +1.25VS_current description for Intel's spec update.
   Ivcc_axd: 200mA-->515mA,Ivcc_axf: 350mA-->495mA
2. P.46: Delete J4600 for EMI request.

F9E R0.5 => R1.0

(Release on 2007/02/14)

Rename to R1.0,the content is the same as R0.5.
S/R Gerber out revision.

<Variant Name>

ASUSTeK COMPUTER INC

Title : History(1)

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 48 of 94

F9E R1.0 => R1.1

(Release on 2007/03/09)

1. P.81: Change CE8101 from un-mount to mount and CE8105 from mount to un-mount to make output choke to place close to output capacitor.
2. P.82: Change R8201 to 1KOHM for OCP issue
3. P.86: Change R8619 to 8.06KOHM for load line issue.
4. P.86: Change R8620 and R8627 to 30.1OHM for common part issue.
5. P.17: OCP polyswitch(F1701) change to 07G014050102(RAYCHEM 500mA).
6. P.17: R1705 change from 100ohm to 390 ohm to meet CMO discharge timming(8ms)(spec >5ms).
7. P.20: Change CON2001 to 12G030000523 for WLAN's thermal.
8. P.24: Change U2401 to 06G004195011,unmount R2401, mount R2402 for costdown.
9. P.34: Mount R3455 to meet EC's timing requirement.
   (ALL_SYSTEM_PWRGD-->110ms-->CPU_VRON)

(Release on 2007/03/20)
10. P.36: Add Q3601,Q3602,R3602,R3609 to fix MS Duo adaptor short issue
11. P.36: Add C3620~C3624,R3614~R3618 for MS timing.
12. P.47: Change C4701 from 11G234110612510 to 11G234210612320
    for F9DC capacitor burning issue.
13. P.07: Change R0712 from 220ohm to 270ohm for clock signal quality
14. Change footprint for layout request: H1901,H1902,J4601,U9200,U8801
15. For EMI request: Add C1416,C1417,C1601,C1602,C3606,C3802

(Release on 2007/03/23)
16. P.82: Mount CE8200 for +1.05VO to provide VCCGFX.
17. P.83: Add C8314 for EMI solution.
18. P.86: Unmount all components of Page 86 for +1.05VO to provide VCCGFX for costdown
    P.11: Unmount JP1103,mount JP1102
    P.09: Unmount R0948~R0951
19. P.82: Change C8213 from Yageo to Taiyo for AVL issue.
20. P.84: Change C8407 from 2200pf to 22nf for timing issue.
21. P.92: Unmout R9205 for timing issue.(R3455 has 10K pull up already)
22. For EMI solution: Add C8025,C8029,C1906,C1907,C33188,C3317@;Change R2405 to L2402

(Release on 2007/03/26)
23. P.17: R1705 from 390 ohm change to 330 ohm for CMO LCD power off sequence
24. For 3G team request:(solution as F9S)
    P.07: Add C0719,C0721;mount C0717,C0718,C0720,C0722,C0723,C0724
    P.14,P15: Mount C1401,C1402,C1501,C1502
    P.17: Add C1715,C1716,C1717 and mount C1710
    Change C1709(100pF-->22pF),C1711(1uF-->10uF),C1712(100pF-->33pF),C1713(10uF-->33pF)
    P.35: Add C3503~C3526.
25. P.27: Reserve R2737 for system auto power on when we do not install DIMM and CPU
26. P.46: Modify H4626 screw hole for ME request.
27. For CRT signal quality:
    P.18: Change C1832,C1834,C1836.(22pF-->10pF)
    P.18: Mount C1831,C1833,C1835.(5pF-->15pF)

(Release on 2007/03/27)
28. P.29: Change C2919(22uF-->10uF),C2903(0.1uF-->10uF),mount C2921,C2922
    to keep LAN voltage level stable
29. P.88: Change Q8802 from FDS6609A to FDS9435A due to FDS6609A will EOL.
30. P.88: Mount C8818 for power limit to enter later and exit fast
31. P.07: Delete C0721,change C0719(33pF-->10pF) connection method for 3G team request

(Release on 2007/03/28)
32. P.29: Change C2903 size from 0805 to 0603 for limit high
33. P.21: Mount R2101 for stable of input password.
34. P.36: Unmount R3609 for cost down.

F9E_R1.1=>_R2.0

(Release on 2007/05/03)

1. P.21: Unmount C2921,C2922 to remove power audio noise.
2. Intel 965GM eliminates "Graphics Render Standby" function (Document#655320):
   2-1. P.37: Change discharage net name: +VCCFX_CORE-->+VGFX_CORE
   2-2. P.86: Delete all components and nets of Page 86.
   2-3. P.09: Delete net GVR_VR_EN,GVR_VID[1..4]
   2-4. P.09: Delete componeNt R0948~R0951
   2-5. P.11: Delete net +VCCFX_CORE and JP1103
   2-6. P.34: Delete net GFX_VR_PWRIN,R3407;add test point T3453.
   2-7. P.92: Delete R9204.

3. Short 0 ohm by trace for cost down:
   3-1. Delete RN0501,RN0502,net H_VID[0..6].
4. DeleteC3503~C3526,add CN3501~CN3506 for cost down.

F9E_R1.1=>_R2.01

(Release on 2007/05/15)
1. For EMI request:
   1-1. P.36: Add C3607. (at +5V)
   1-2. P.18: Change C1832,C1834,C1836 from 10pF to 15pF.
   1-3. P.22,P.34: Reserved C2207,C3405,DNI.(For ESD)
   1-4. P.6,P.17,P.38: Add C0640,C0641,C1718,C3806.(For ESD)
2. For factory request,no L-pad (co-lay):
   P.17,P.19,P.21,P.24,P.33: Remove L1709,L1904~L1907,L2101,L2102,L2401,L3301
3. Update power budget for power request to meet test spec. (3.3V,5V,VCCP)
4. P.17: Change L1708 to R1704 for costdown.
5. P.07: Change C0723 from 33pF to 10pF for waveform.
6. P.24: Change L2402 from Irat=600mA to 2A for protect L2402.
7. P.07: Add T0701~T0703,mount R0715,R0717,R0731 for factory ATS test.
8 Add Test point for factory request:
   T0701,T0702,T0703,T2518,T2719,T3436,T3443,T3449,T4717,T4718,T4719,T4720,T4721,T4722
   T8044,T8045,T8046,T8047,T8048,T8049,T8050,T9201,T9202,T9203,T9204,T9205
9 Remove 0 ohm to cost down,please layout help to short it:
  R0719,R0721,R0723,R0807,R0917,R0920,R0926,R0942,R1902,R2008,R2111,R2512,
  R2747,R2748,R3009,R3308,R3432,R3433,R3509

F9E_R2.01=>_R2.02

(Release on 2007/05/25)
P.07: For clock signal quality:
   C0718, C0717, C0724, C0720, C0722,C0723 -->5pF
   R0704,R0707, R0709, R0711, R0729, R0710 -->47ohm
P.18: For Change C1832,C1834,C1836 from 15pF to 10pF signal quality: (Same as E/R)
P.19: Mount C1901 for 3G team request

<Variant Name>

ASUSTeK COMPUTER INC

Title : History(2)

Engineer:

Size	Project Name	Rev
Custom	F9E	2.02

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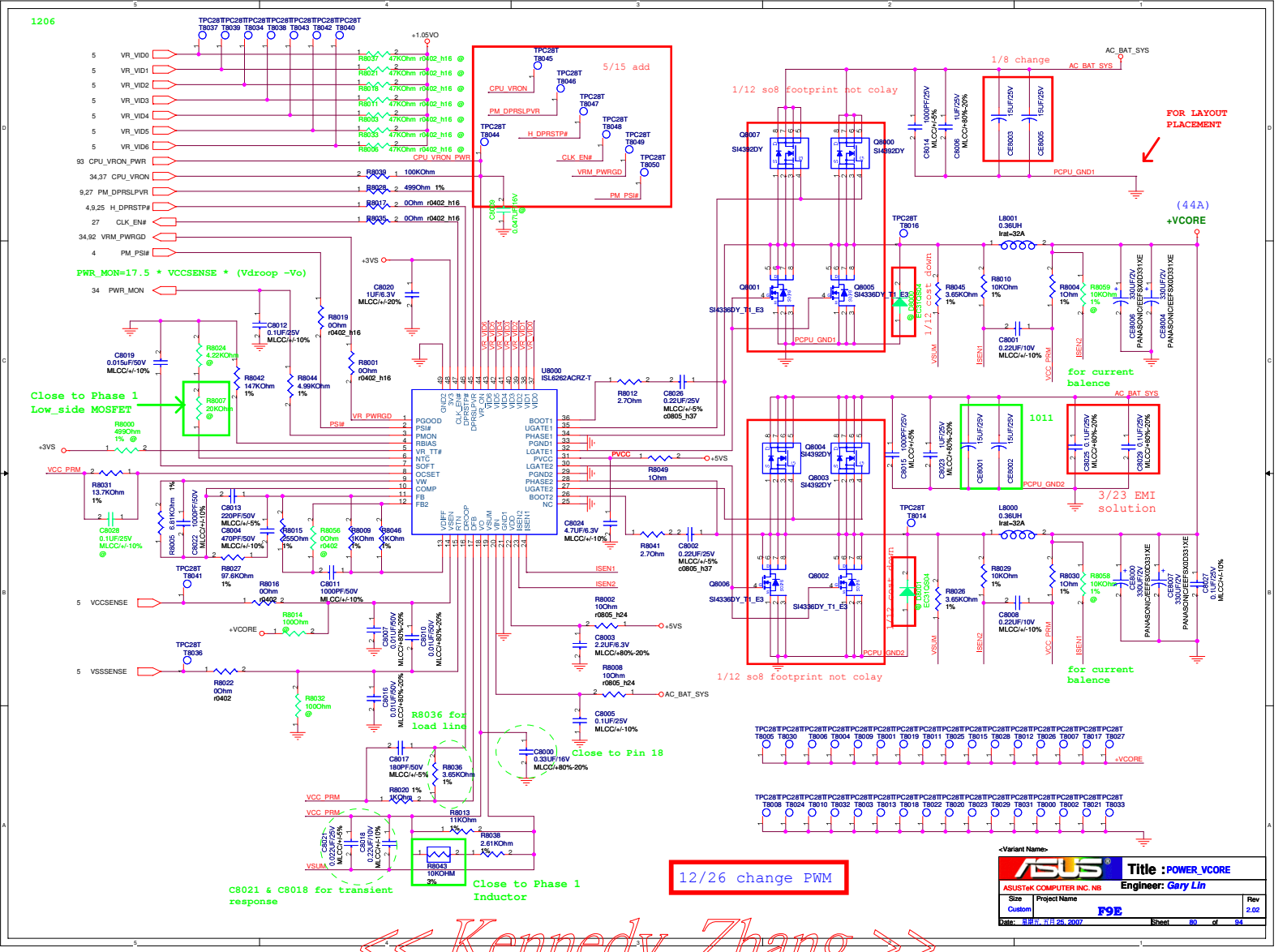


Title : POWER_VCORE

ASUSTeK COMPUTER INC. NB

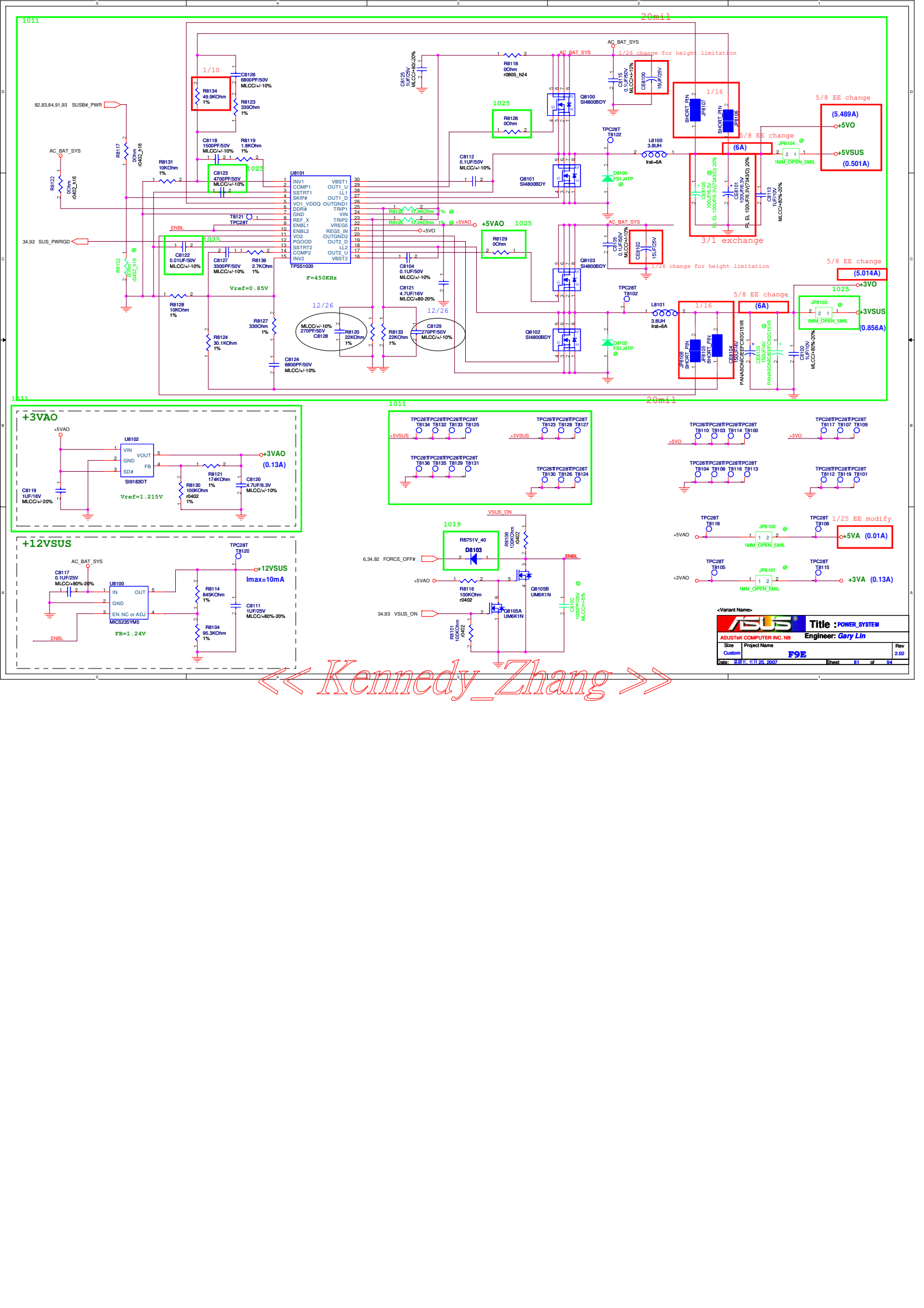
Engineer: Gary Lin

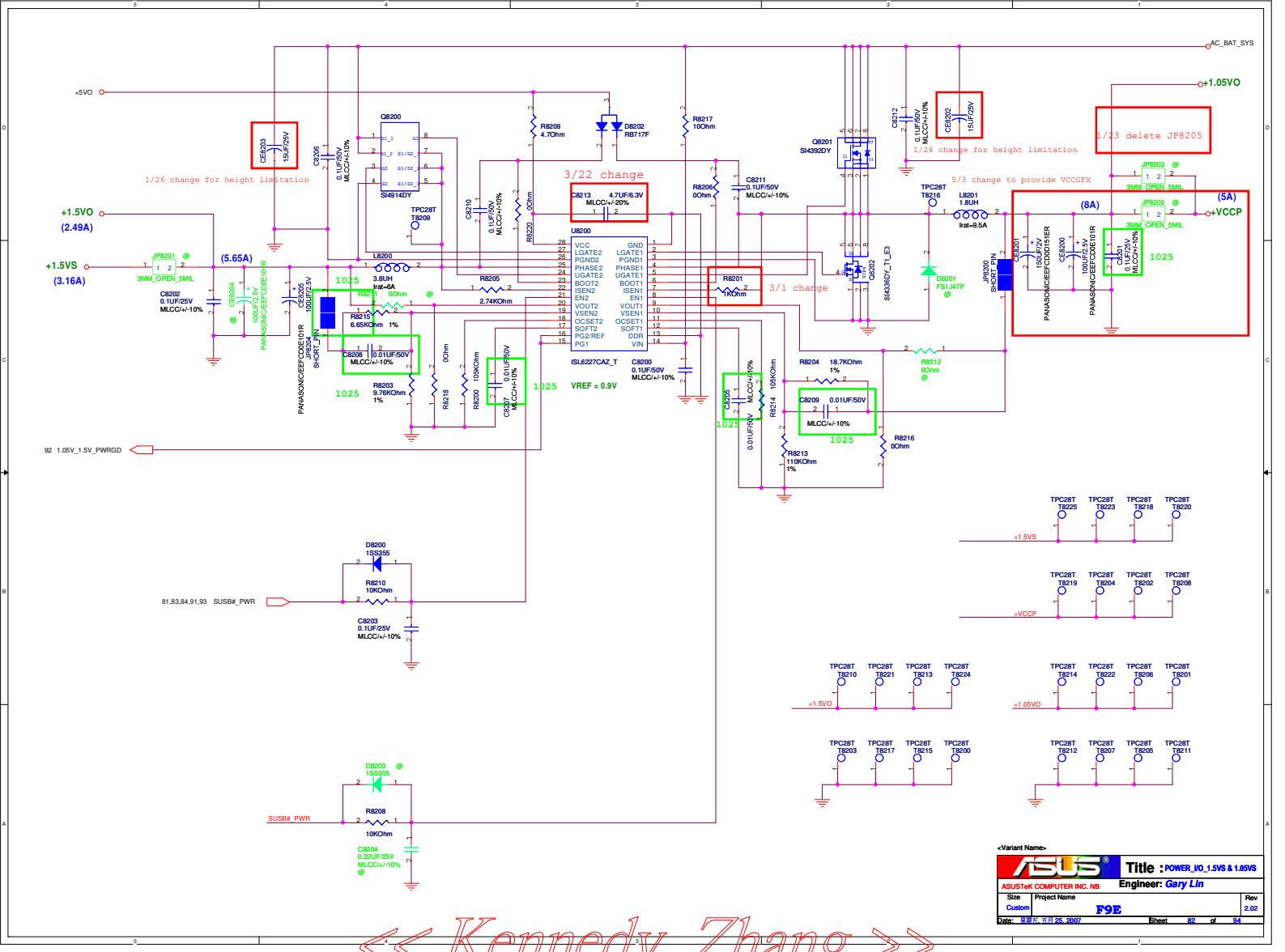
Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 五月 25, 2007 Sheet 80 of 94

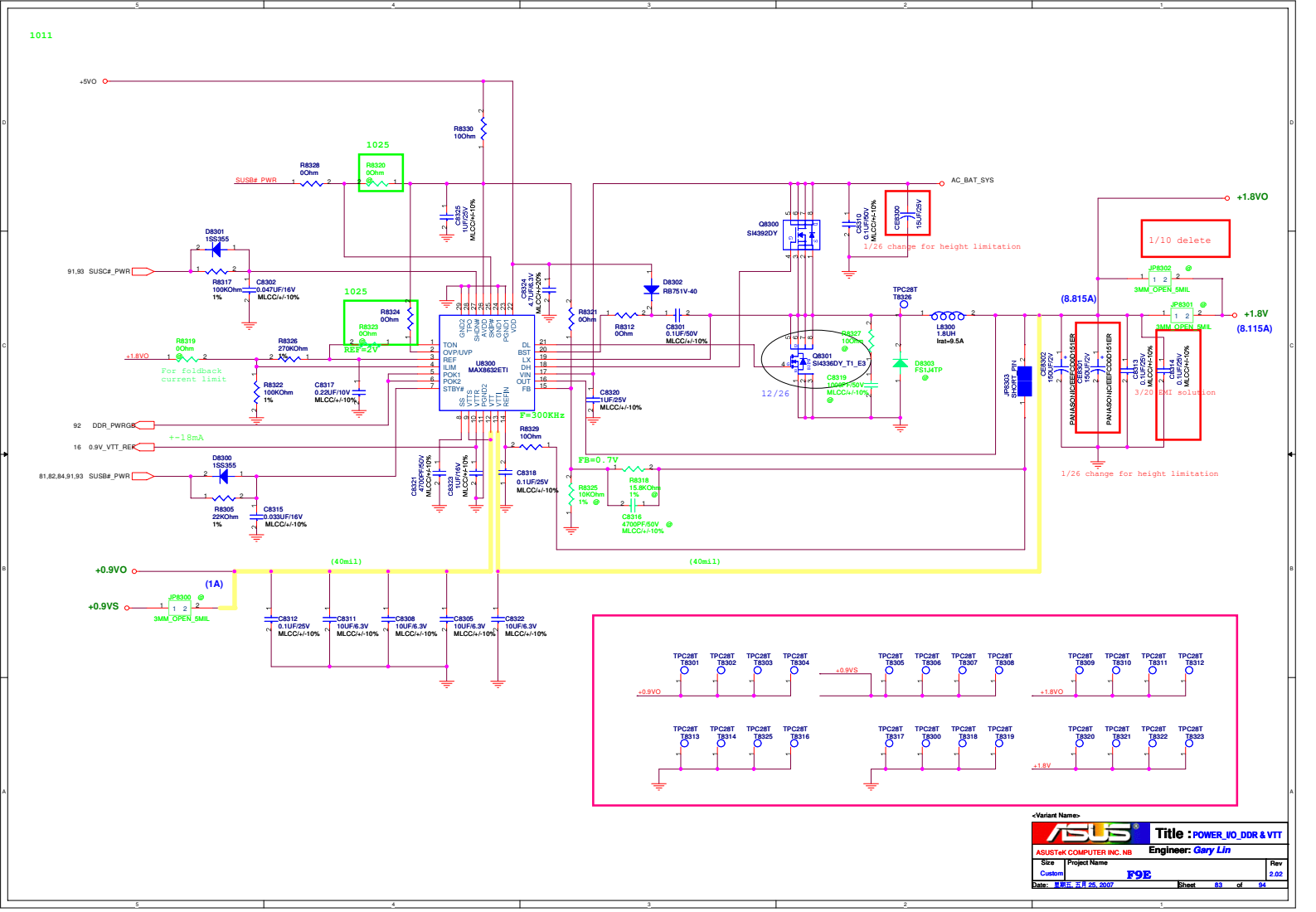
<Variant Name>

<< Kennedy_Zhang >>


1011
20mil
AC_BAT_SYS
1/26 change for height limitation
82,83,84,91,93 SUSB#_PWR
34,92 SUS_PWRGD
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
1025
1/10
1/16
3/1 exchange
5/8 EE change
(5.489A)
+5VO
+5VSUS
(0.501A)
(6A)
(5.014A)
+3VO
+3VSUS
(0.856A)
+3VAO
(0.13A)
U8102
SI9183DT
Vref=1.215V
+12VSUS
Imax=10mA
U8100
MIC5235YM5
FB=1.24V
1019
VSUS_ON
6,34,92 FORCE_OFF#
RB751V_40
D8103
Q8105B
UM6K1N
Q8105A
UM6K1N
1/25 EE modify
+5VA (0.01A)
+3VA (0.13A)
1MM_OPEN_5MIL
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Gary Lin
Project Name
F9E
Rev
2.02
Date: 星期五, 六月 25, 2007
Sheet 81 of 94
<Variant Name>
<< Kennedy_Zhang >>



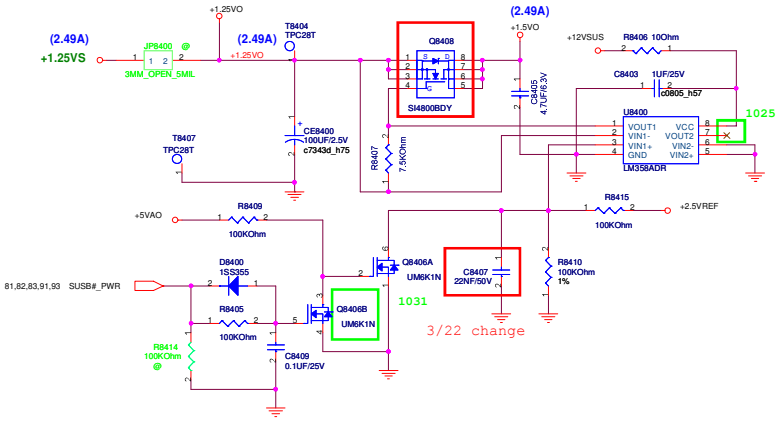
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

+1.25VS

1/12 so8 footprint not colay



1019

Delete +2.5VS

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_+1.25VS

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 84 of 94

<< Kennedy_Zhang >>

delete +VRAM &VGA_core

<Variant Name>

Title : POWER_VGA_CORE & RAM

ASUSTeK COMPUTER INC. NB

Engineer: Gary Lin

Size	Project Name	Rev
C	P9E	2.02

Date: 日 四月 26, 2007 Sheet 85 of 94

<< Kennedy_Zhang >>

5/3 delete this page by EE request

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_+VCCFX_CORE(NA)
	Engineer: Gary Lin
Size: B	Project Name: F9E
Rev: 2.02	
Date: 星期五, 五月 25, 2007	Sheet 86 of 94

<< Kennedy_Zhang >>

<Variant Name>

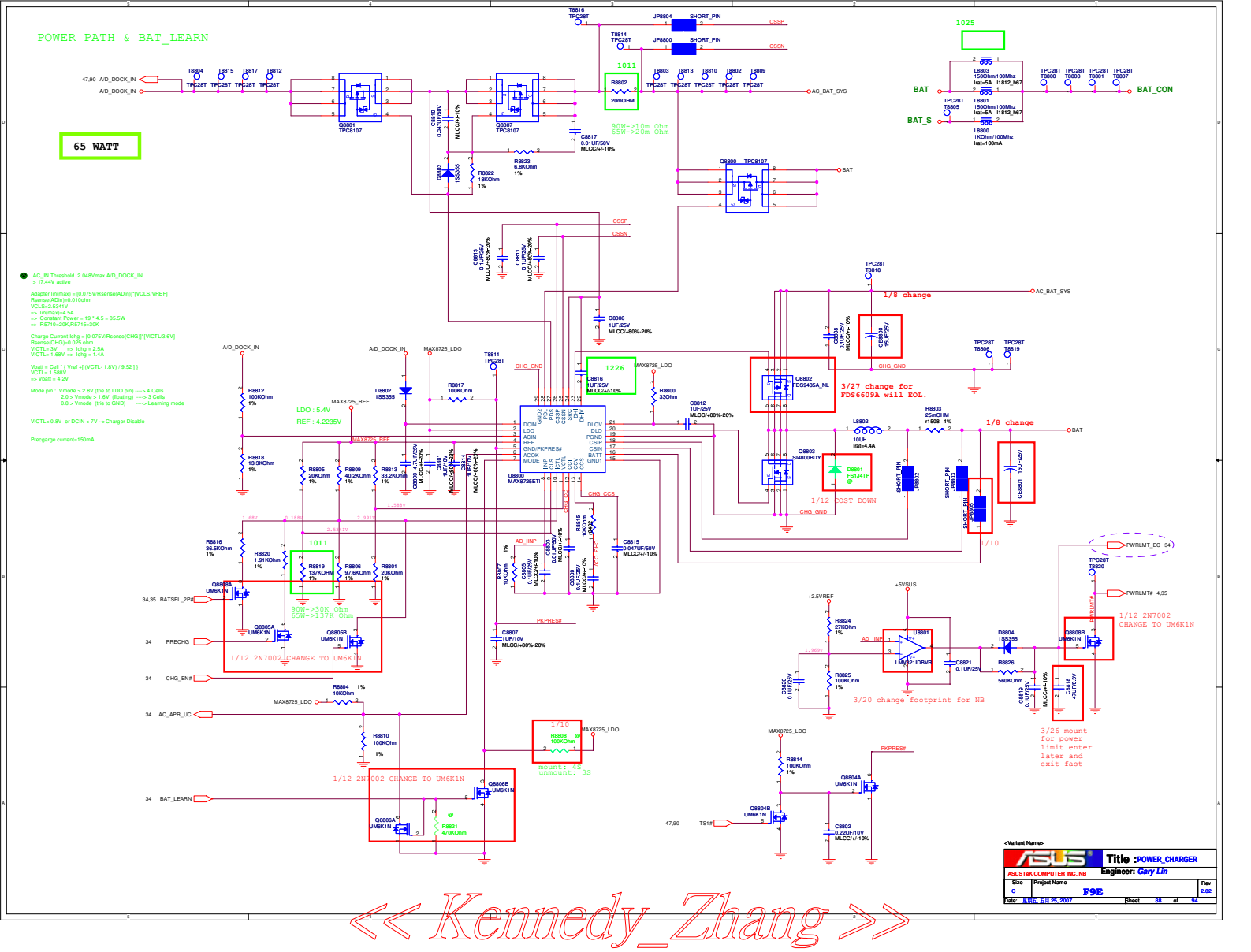
Title : POWER_SHUTDOWN#

ASUSTeK COMPUTER INC. NB

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期六, 十月 25, 2007 Sheet 87 of 94



<Variant Name>

Title : N/A

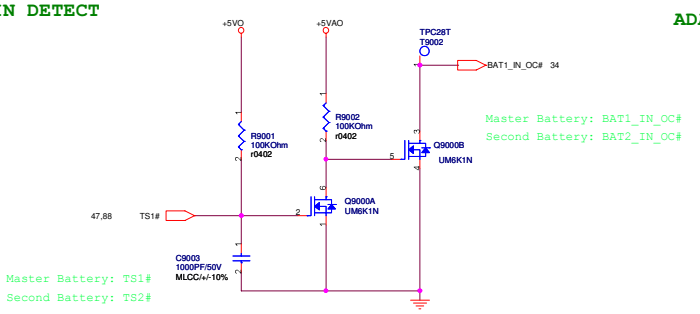
ASUSTeK COMPUTER INC. NB

Engineer: Gary Lin

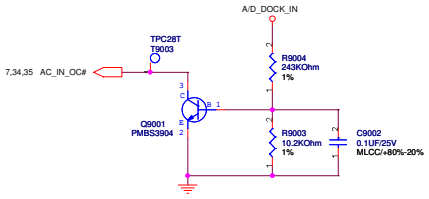
Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 十月 25, 2007 Sheet 89 of 94

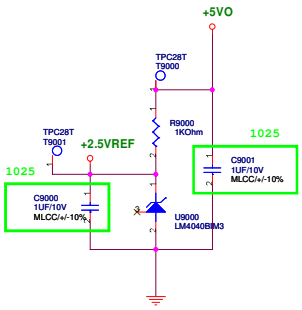
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_DETECT

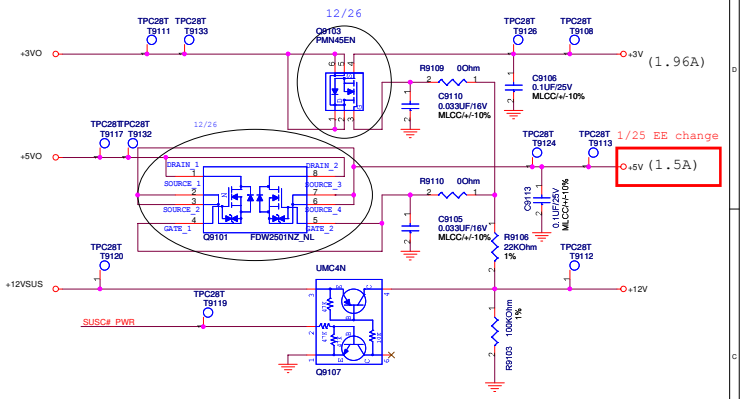
Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9E	2.02

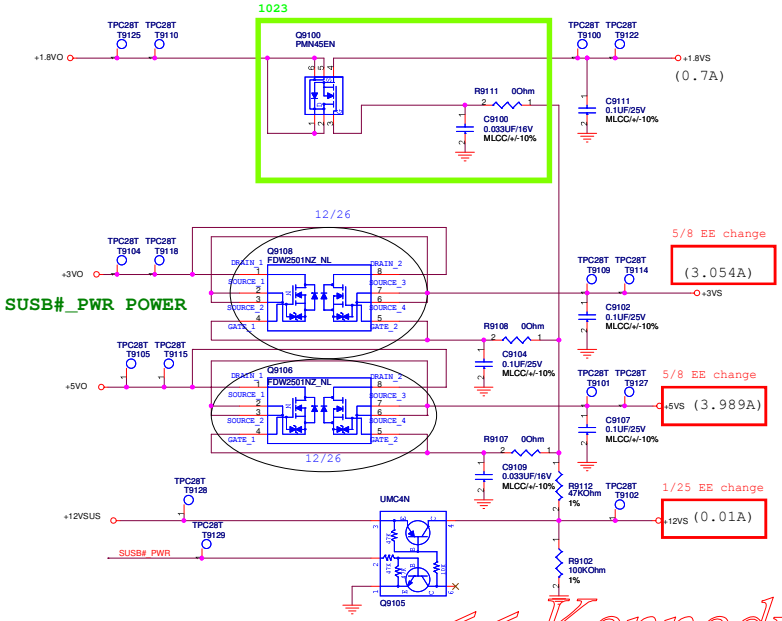
Date: 星期五, 十月 25, 2007 Sheet 90 of 94

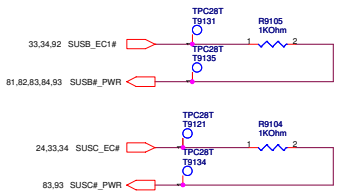
<< Kennedy_Zhang >>

SUSC#_PWR POWER



SUSB#_PWR POWER





ASUSTeK COMPUTER INC. NB

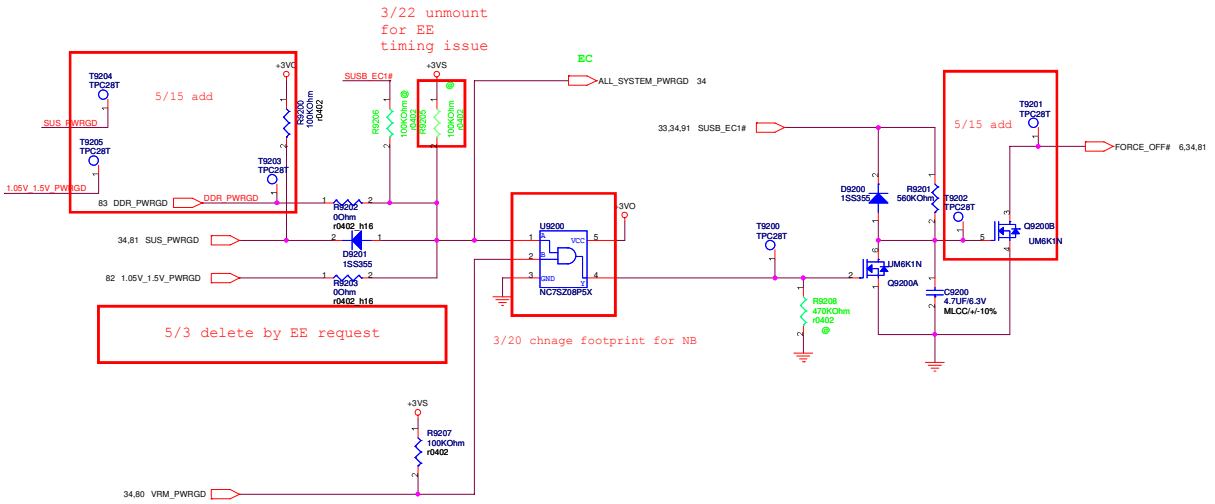
Title : POWER_LOAD SWITCH

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_PROTECT	
	Engineer: Gary Lin	
Size: Custom	Project Name: F9E	Rev: 2.02
Date: 星期五, 六月 25, 2007	Sheet 82 of 94	

AC_BAT_SYS	AC_BAT_SYS	17,80,81,82,83,88
BAT	BAT	88
BAT_CON	BAT_CON	47,88
+2.5VREF	+2.5VREF	84,88,90
+3VA	+3VA	17,25,27,34,37,81
+5VAO	+5VAO	81,84,90
+5VO	+5VO	81,82,83,90,91
+5VSUS	+5VSUS	24,28,81,88
+5V	+5V	17,22,36,37,91
+5VS	+5VS	6,18,19,21,22,23,28,33,34,37,38,39,80,91
+3VO	+3VO	81,91,92
+3VSUS	+3VSUS	17,20,22,24,26,27,28,29,34,39,81
+3V	+3V	19,20,21,22,26,33,35,37,91
+3VS	+3VS	6,7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,30,33,34,37,38,39,80,91,92
+12VSUS	+12VSUS	24,81,84,91
+12V	+12V	22,36,37,91
+12VS	+12VS	17,19,37,91
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	9,11,12,14,15,16,37,83
+1.8VS	+1.8VS	30,37,91
+0.9VS	+0.9VS	16,37,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	80,82
+VCCP	+VCCP	4,5,6,7,8,9,11,12,28,37,82
+1.5VO	+1.5VO	82,84
+1.5VS	+1.5VS	5,12,20,25,28,33,37,82

1023 delete +2.5VO

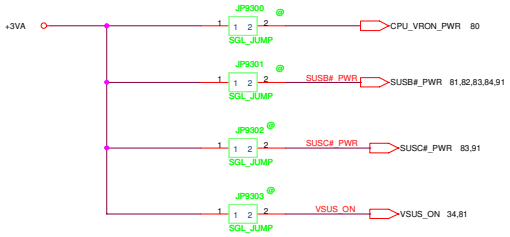
+VCORE	+VCORE	5,6,37,80

delete VRAM 1.2VSP VGA

+1.25VS	+1.25VS	9,12,28,37,84

5/3 delete by EE request

FOR POWER TEST



<Variant Name>

ASUSTeK COMPUTER INC. NB

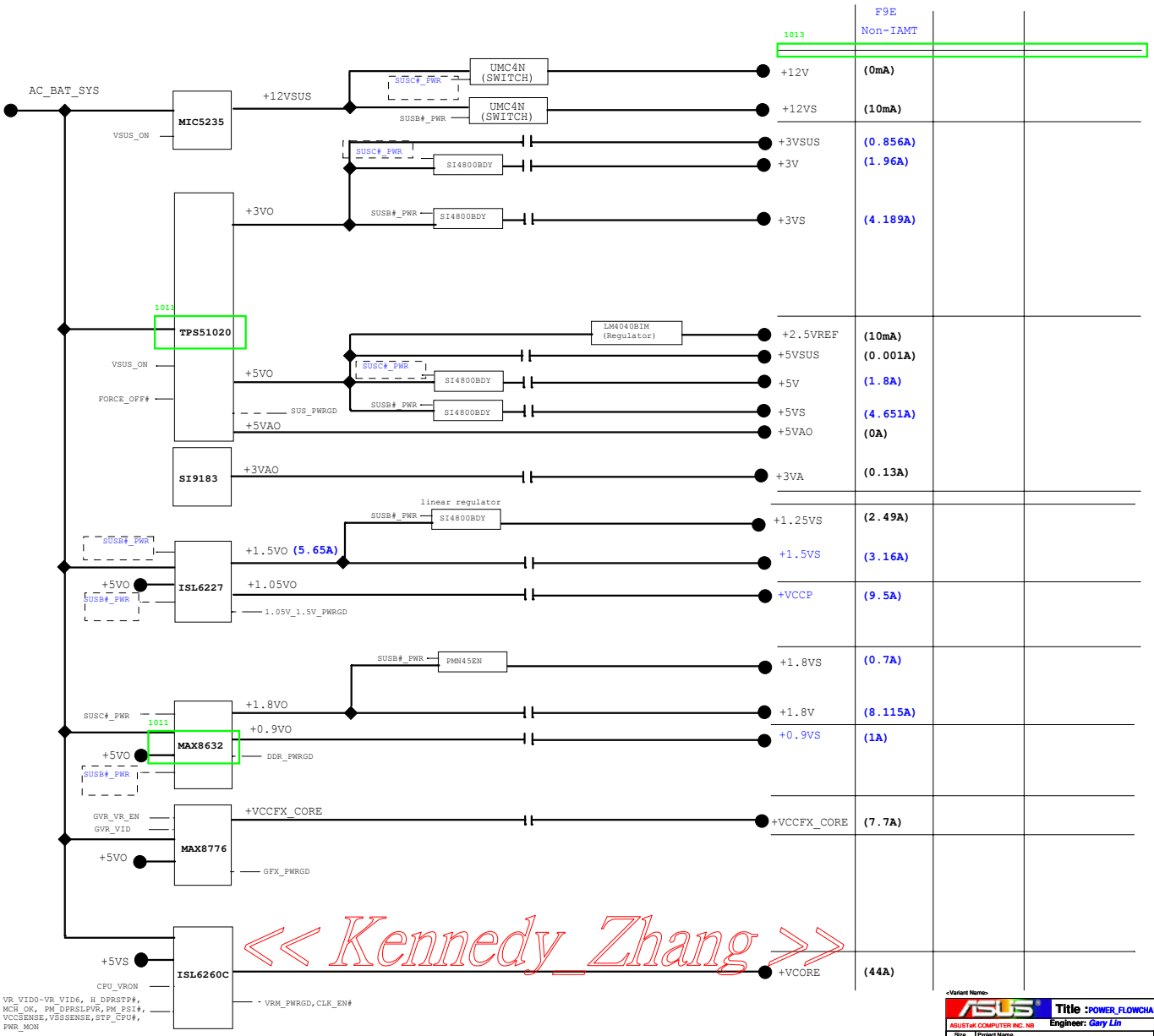
Title : POWER_SIGNAL

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F9E	2.02

Date: 星期五, 六月 25, 2007 Sheet 93 of 94

<< Kennedy_Zhang >>


F9E
Non-IAMT
1013
AC_BAT_SYS
MIC5235
VSUS_ON
+12VSUS
SUSC#_PWR
UMC4N (SWITCH)
SUSB#_PWR
UMC4N (SWITCH)
+12V
(0mA)
+12VS
(10mA)
SUSC#_PWR
SI4800BDY
+3VSUS
(0.856A)
+3V
(1.96A)
+3VO
SUSB#_PWR
SI4800BDY
+3VS
(4.189A)
1013
TPS51020
VSUS_ON
FORCE_OFF#
LM4040BIM (Regulator)
+2.5VREF
(10mA)
+5VSUS
(0.001A)
SUSC#_PWR
+5VO
SI4800BDY
+5V
(1.8A)
SUSB#_PWR
SI4800BDY
+5VS
(4.651A)
SUS_PWRGD
+5VAO
+5VAO
(0A)
SI9183
+3VAO
+3VA
(0.13A)
linear regulator
SUSB#_PWR
SI4800BDY
+1.25VS
(2.49A)
SUSB#_PWR
+1.5VO (5.65A)
+1.5VS
(3.16A)
+5VO
ISL6227
+1.05VO
+VCCP
(9.5A)
SUSB#_PWR
1.05V_1.5V_PWRGD
SUSB#_PWR
PMN45EN
+1.8VS
(0.7A)
+1.8VO
SUSC#_PWR
+1.8V
(8.115A)
1011
+0.9VO
MAX8632
+0.9VS
(1A)
+5VO
DDR_PWRGD
SUSB#_PWR
GVR_VR_EN
GVR_VID
+VCCFX_CORE
+VCCFX_CORE
(7.7A)
MAX8776
+5VO
GFX_PWRGD
<< Kennedy_Zhang >>
+5VS
ISL6260C
CPU_VRON
VR_VID0~VR_VID6, H_DPRSTP#, MCH_OK, PM_DPRSLPVR,PM_PSI#, VCCSENSE,VSSSENSE,STP_CPU#, PWR_MON
VRM_PWRGD,CLK_EN#
+VCORE
(44A)
<Variant Name>
Title : POWER_FLOWCHART
ASUSTeK COMPUTER INC. NB
Engineer: Gary Lin
Size
Custom
Project Name
F9E
Rev
2.02
Date: 日 四月 15 25, 2007
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