F80Q SCHEMATIC Revision 2.00

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91	91_POWER_LOAD SWITCH
92	92_POWER_PROTECT
93	93_POWER_SIGNAL
94	94_POWER_FLOWCHART

<Variant Name>

ASUSTeK COMPUTER INC

Title : PAGE REF.

Engineer: CH Lin

Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 1 of 59

F80Q BLOCK DIAGRAM

BATTERY TYPE

3S1P
3S2P

Internal IO CON with Cable for MB

TP CON | MDC CON | BT CON | INVERTER CON | LVDS CON

SPEAKER | INT. MIC CON

Penryn P.04~P.05 — CPU CAP P.06

HOST BUS

FSB 667 MHz

POWER SEQENCE | RESET | SM_BUS

LVDS & INV CON P.17

CRT CON P.18

NOTHBRIDGE CANTIGA P.08~P.13

DDR2 SDRAM 667/800MHz

DDR2 667/800 SODIMM X2

+1.8V
+0.9VS P.14~P.15

DDR CAP/RES P.16

DCIN
RTC
FAN
CON.

THERMAL SENSOR (MAX6657) P.06

Part Number: 02G010022500
Part Name & Spec:C.S 88CTPM (B2) INTEL PM45 QT78 897258 QS

DMI Interface

ICH9-M P.25~P.28

Part Number: 02G010015340
Part Name & Spec:C.S ICH9M (A3) INTEL QT09 895652

USB x4 P.24

B/T P.21

Camera P.17

F/P P.21

4 IN 1 CON P.36

AU6371 P.36

USB2.0
SATA BUS
SATA BUS

PCI EXPRESS X1

ACZ

MDC CON

ODD Slave P.23

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TPM Connector P.21

LPC, 33MHz

EC *ITE8512* P.34

SPI ROM *8M* P.34

INTERNAL KEYBOARD P.35

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AUDIO AMP TPA6017 P.41

LAN 10/100 RTL8101E P.29

MINI CARD WLAN P.20

NEWCARD P.33

MINI CARD Robson P.31

RJ11,RJ45 CON P.30

MIC_IN

HP

AC & BAT CON P.47

CLOCK GEN. ICS9LPR363DGLF-T P.07

<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM
Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 2 of 59

EC-IT8752 GPIO SETTING

Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
29	PWM1/GPA1	CHG_LED_UP#	
32	PWM2/GPA2	BATSEL_3S#	
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
75	GPI1	VSUS_GD	I
76	GPI2	ALL_SYS_PWRGD	
77	GPI3	CPUPWR_GD	O
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
126	GPB7	PM_RSMRST#	O
64	GPC3	PM_PWRBTN#	O
136	TMRI0/WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	TMRI1/WUI3/GPC6	BAT1_IN_OC#	I
20	CK32KOUT/GPC7	RF_ON_SW#	I
22	RI1#/WUI0/GPD0	PWRLIMIT#	
25	RI2#/WUI1/GPD1	PM_SUSC#	O
37	GINT/GPD5	LCD_BACKOFF#	O
53	TACH0/GPD6	FAN0_TACH	O
23	ADC4/GPE0	VSUS_ON	O
94	ADC5/GPE1	SUSC_EC#	O
95	ADC6/GPE2	SUSB_EC1#	I
96	ADC7/GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	LPCPD#/WUI6/GPE6	LID_EC#	I
121	GPG1	PM_SUSB#	I
105	GPH0	PM_CLKRUN#	
108	GPH3	BAT_LEARN	O
110	GPH5	NUM_LED#	O
111	GPH6	CAP_LED#	O
99	PS2CLK1/GPF2	MARATHON#	I
101	PS2CLK2/GPF4	TP_CLK	O
102	PS2DAT2/GPF5	TP_DAT	I/0
124	SMCLK0/GPB3	SMB0_CLK	O
125	SMDAT0GPB4	SMB0_DAT	I/O
129	SMCLK1/GPC1	SMB1_CLK	I
130	SMDAT1/GPC2	SMB1_DAT	I/O
131	GPF6	THRO_CPU	O
84	GPJ0	EC_CLK_EN	O
85	GPJ1	ICH8_PWROK	O
87	GPJ3	BATSEL_2P#	O
26	GPD2	PLT_RST_BUF#	I
27	GPD3	EXT_SCI#	O
19	GPD4	EXTSMI#	O
142	GPB5	A20GATE	O
4	GPB6	RCIN#	O

Pin	Pin Name	Signal Name	Type

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)

ICH8M_GPIO

Pin.	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 00	i		GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	H-Z	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	0	GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i	0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i		GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	H-Z	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat.	H-Z	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i		GPI	KBC_SCI#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat.		GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat.	1	Native	STP_PCI#	+3VSUS	STP_PCI# , No-GPIO, in Mobile
GPIO 16	Nat.	0	Native	PM_DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	freq 1K	GPO	N/A	+3VS	N/A
GPIO 19	i		GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i		GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i		GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat.		Native	N/A	+3VS	LDRQ1#
GPIO 24	O	H-Z	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED) , Not Cleared by CF9h RST event.
GPIO 25	Nat.	1	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO, in Mobile
GPIO 26	Nat.		GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat.		Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat.		Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat.		Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO, in Mobile
GPIO 33	O	1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i		GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i		GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 39	i		GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat.		Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a		N/A	N/A	N/A	No implement
GPIO 48	i	1	Native		+3VS	SDATAOUT1
GPIO 49	Nat.		Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat.		Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat.	1	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat.		Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat.	1	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat.		Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat.	1	Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

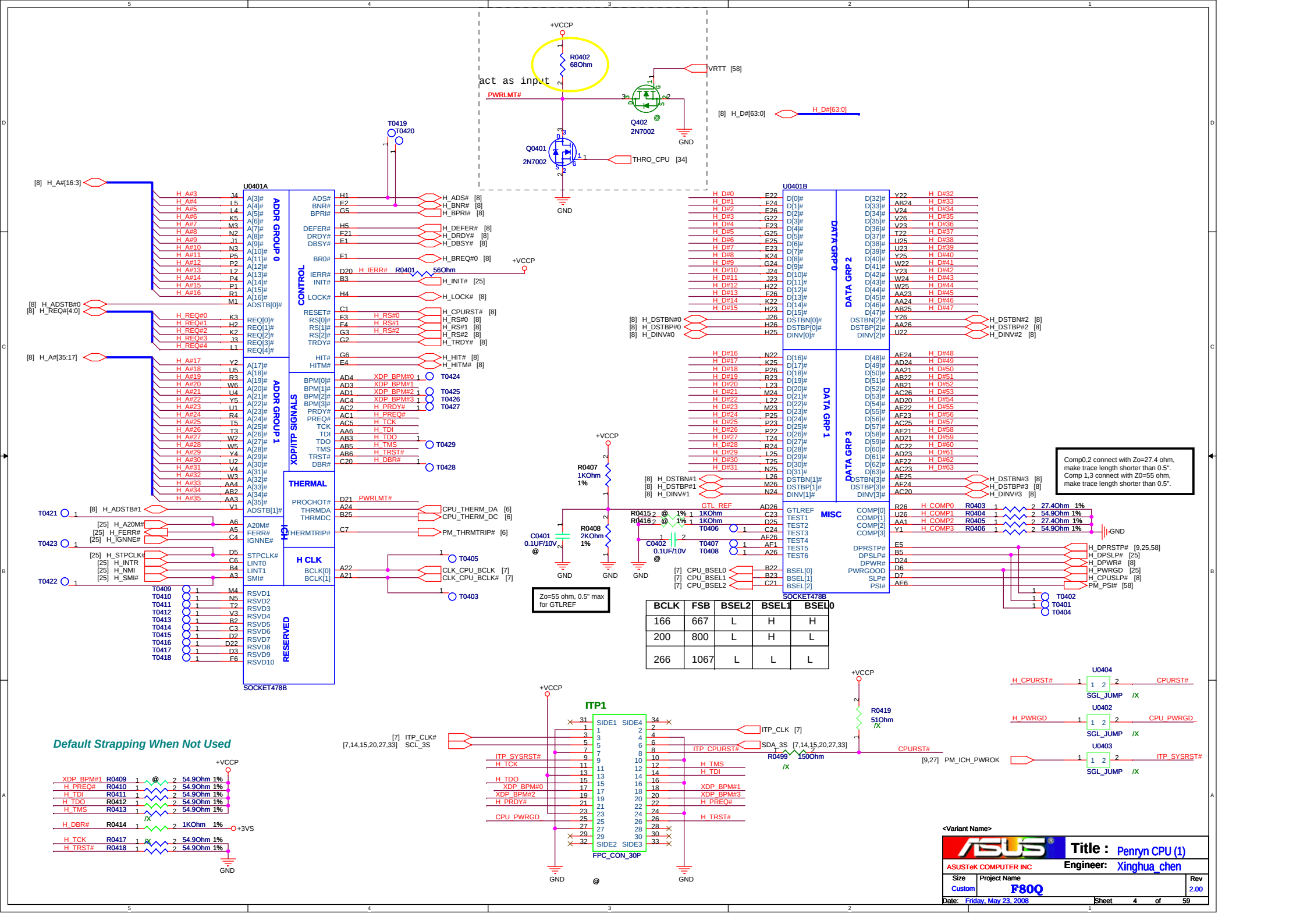
ASUSTeK COMPUTER INC

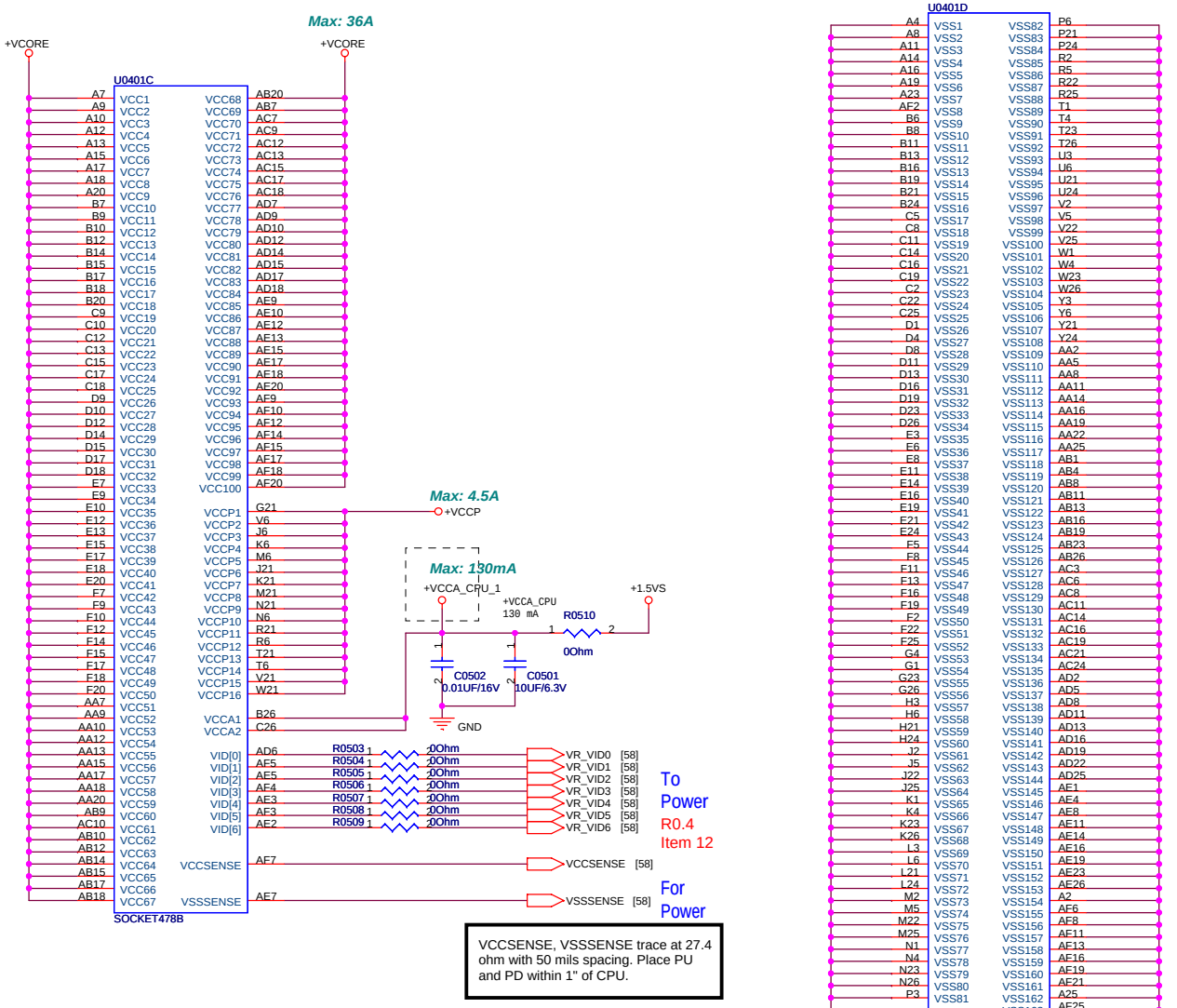
Title : Schematic Info.

Engineer: CH Lin

Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 3 of 59


act as input
PWRLMT#
R0402 68Ohm
Q402 2N7002
Q0401 2N7002
VRTT [58]
THRO_CPU [34]
H_D#[63:0]
GND
U0401A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
SOCKET478B
U0401B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
SOCKET478B
R0407 1KOhm 1%
R0408 2KOhm 1%
C0401 0.1UF/10V
C0402 0.1UF/10V
GTL_REF
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".
BCLK FSB BSEL2 BSEL1 BSEL0
166 667 L H H
200 800 L H L
266 1067 L L L
Default Strapping When Not Used
ITP1
FPC_CON_30P
R0419 51Ohm
R0499 150Ohm
U0404
U0402
U0403
SGL_JUMP
Title : Penryn CPU (1)
ASUSTeK COMPUTER INC
Engineer: Xinghua_chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 4 of 59



<Variant Name>

ASUSTeK COMPUTER INC

Title : Penryn CPU (2)

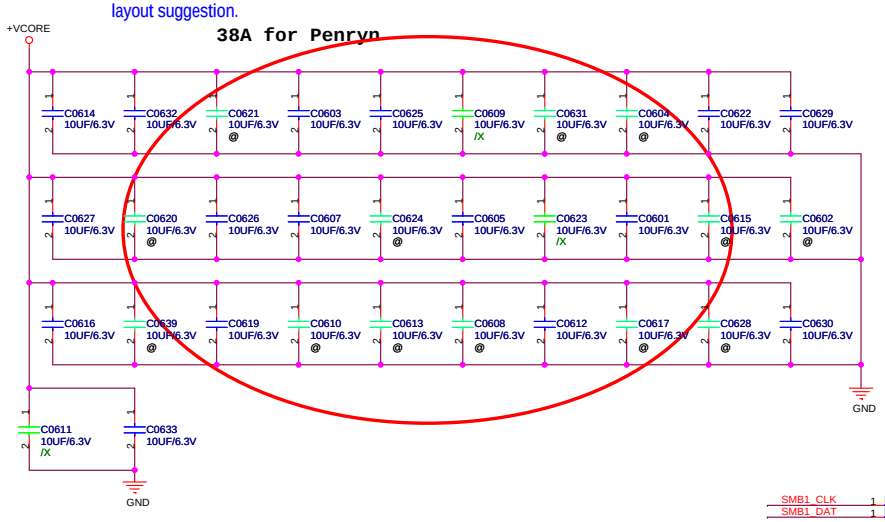
Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

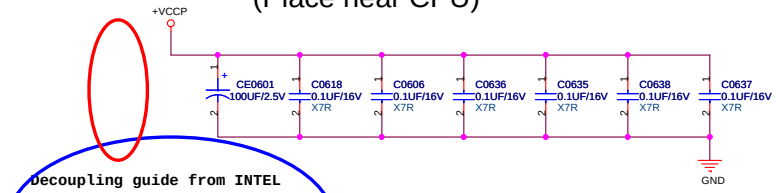
Date: Friday, May 23, 2008 Sheet 5 of 59

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)

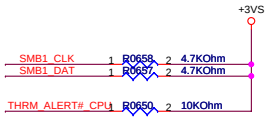


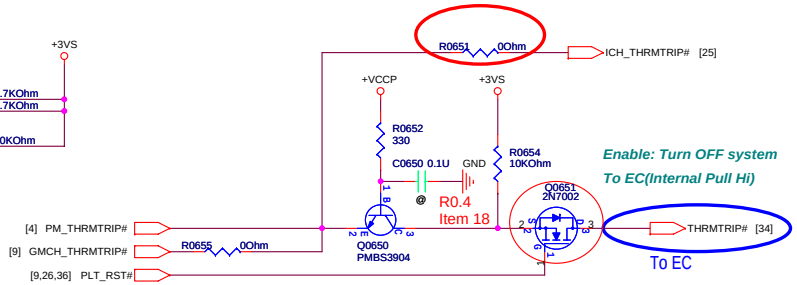
Decoupling guide from INTEL

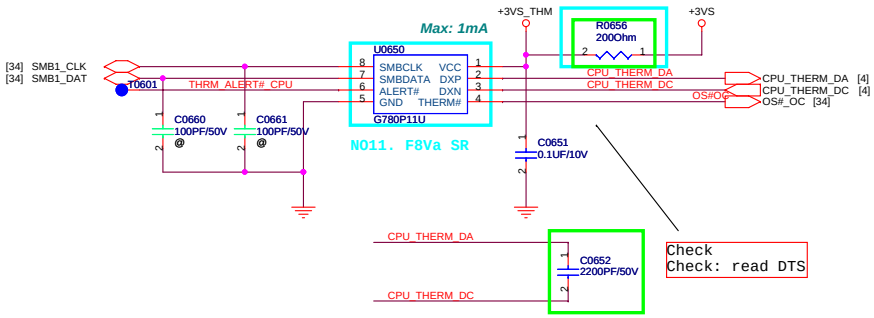
VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it ! _0907

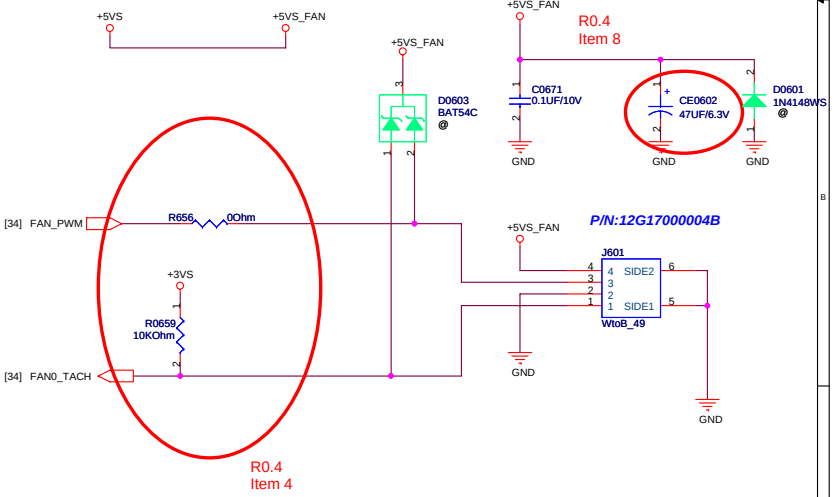
Thermal Sensor



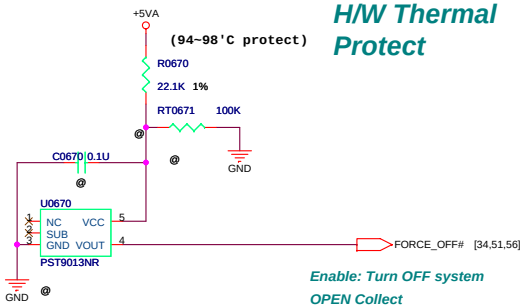




Sub-SYS=FAN



H/W Thermal Protect



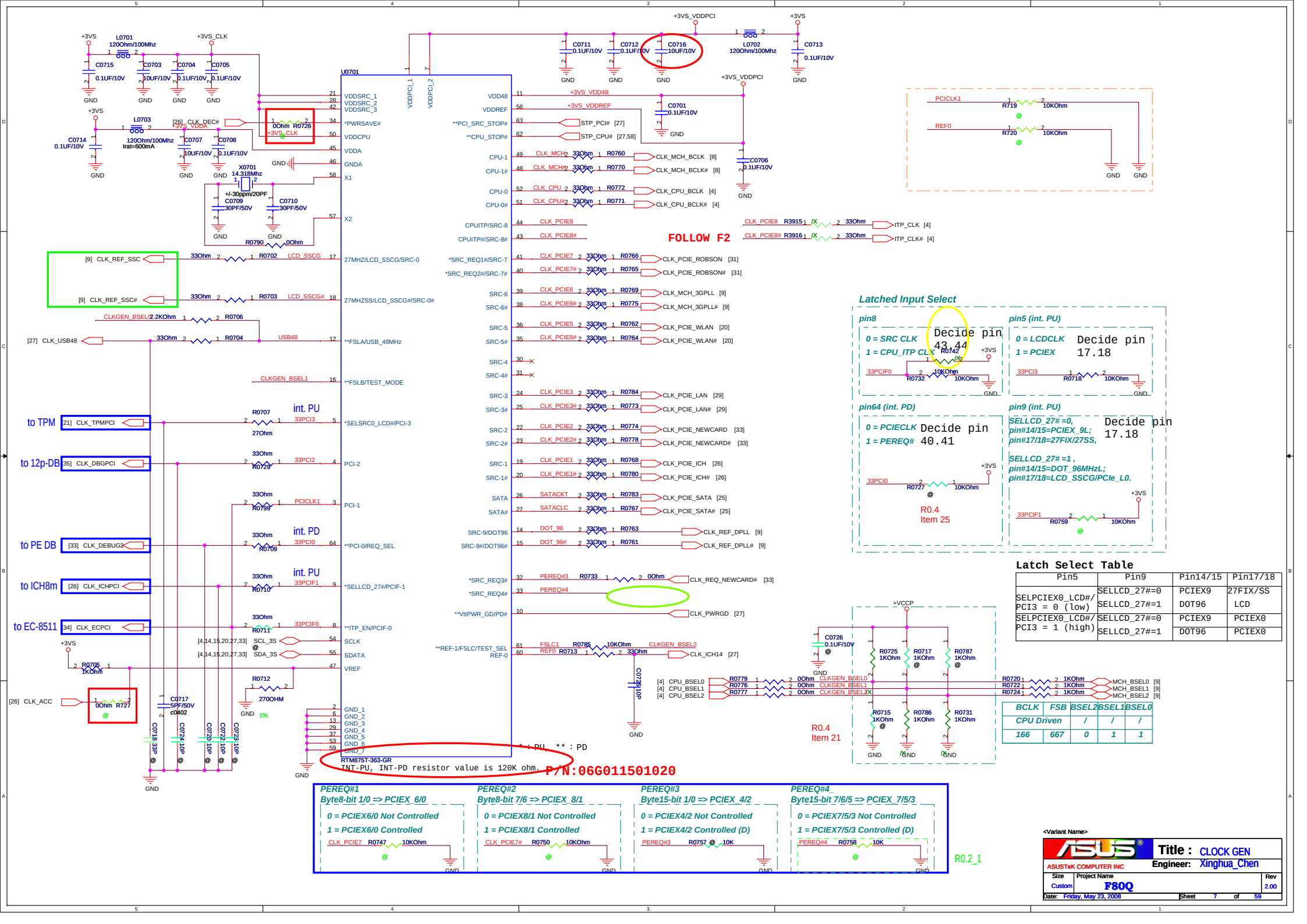
Sub-SYS=CPU

Enable: Turn OFF system
OPEN Collect

<Variant Name>

CPU CAP, Thermal Senor

ASUSTeK COMPUTER INC	Title :	Engineer: Xinghua_Chen	
Size: Custom	Project Name: F80Q		Rev: 2.00
Date: Friday, May 23, 2008	Sheet 6 of 59		


U0701
RTM875T-363-GR
INT-PU, INT-PD resistor value is 120K ohm.
P/N:06G011501020
* : PU, ** : PD
FOLLOW F2
int. PU
int. PD
to TPM
to 12p-DB
to PE DB
to ICH8m
to EC-8511
Latched Input Select
pin8
0 = SRC CLK
1 = CPU_ITP CLK
Decide pin 43.44
pin5 (int. PU)
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
pin64 (int. PD)
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
pin9 (int. PU)
SELLCD_27# =0, pin#14/15=PCIEX_9L; pin#17/18=27FIX/27SS,
SELLCD_27# =1 , pin#14/15=DOT_96MHzL; pin#17/18=LCD_SSCG/PCIe_L0.
Decide pin 17.18
R0.4 Item 25
R0.4 Item 21
Latch Select Table
Pin5 | Pin9 | Pin14/15 | Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low) | SELLCD_27#=0 | PCIEX9 | 27FIX/SS
SELLCD_27#=1 | DOT96 | LCD
SELPCIEX0_LCD#/ PCI3 = 1 (high) | SELLCD_27#=0 | PCIEX9 | PCIEX0
SELLCD_27#=1 | DOT96 | PCIEX0
BCLK | FSB | BSEL2 | BSEL1 | BSEL0
CPU Driven | / | / | /
166 | 667 | 0 | 1 | 1
PEREQ#1 Byte8-bit 1/0 => PCIEX_6/0
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2 Byte8-bit 7/6 => PCIEX_8/1
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3 Byte15-bit 1/0 => PCIEX_4/2
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4_ Byte15-bit 7/6/5 => PCIEX_7/5/3
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
R0.2_1
<Variant Name>
Title : CLOCK GEN
Engineer: Xinghua_Chen
ASUSTeK COMPUTER INC
Size: Custom
Project Name: F80Q
Rev: 2.00
Date: Friday, May 23, 2008
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[4] H_D#[63:0] H_D#[63:0]

[4] H_A#[35:3] H_A#[35:3]

U0801A

RCOMP

For Calibrating the FSB I/O Buffer

R0801 H_RCOMP 24.9Ohm 1% GND

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

+VCCP R0804 221Ohm H_SWING R0805 100Ohm 1% C0802 0.1UF/16V GND GND

T0801 R0815 0Ohm R0807 0Ohm [4] H_CPURST# [4] H_CPUSLP#

+VCCP R0809 1KOhm 1% H_VREF C0801 0.1UF/10V R0808 2KOhm 1% GND GND

H_D#0	F2	H_D#_0	H_A#_3	A14	H_A#3
H_D#1	G8	H_D#_1	H_A#_4	C15	H_A#4
H_D#2	F8	H_D#_2	H_A#_5	F16	H_A#5
H_D#3	E6	H_D#_3	H_A#_6	H13	H_A#6
H_D#4	G2	H_D#_4	H_A#_7	C18	H_A#7
H_D#5	H6	H_D#_5	H_A#_8	M16	H_A#8
H_D#6	H2	H_D#_6	H_A#_9	J13	H_A#9
H_D#7	F6	H_D#_7	H_A#_10	P16	H_A#10
H_D#8	D4	H_D#_8	H_A#_11	R16	H_A#11
H_D#9	H3	H_D#_9	H_A#_12	N17	H_A#12
H_D#10	M9	H_D#_10	H_A#_13	M13	H_A#13
H_D#11	M11	H_D#_11	H_A#_14	E17	H_A#14
H_D#12	J1	H_D#_12	H_A#_15	P17	H_A#15
H_D#13	J2	H_D#_13	H_A#_16	F17	H_A#16
H_D#14	N12	H_D#_14	H_A#_17	G20	H_A#17
H_D#15	J6	H_D#_15	H_A#_18	B19	H_A#18
H_D#16	P2	H_D#_16	H_A#_19	J16	H_A#19
H_D#17	L2	H_D#_17	H_A#_20	E20	H_A#20
H_D#18	R2	H_D#_18	H_A#_21	H16	H_A#21
H_D#19	N9	H_D#_19	H_A#_22	J20	H_A#22
H_D#20	L6	H_D#_20	H_A#_23	L17	H_A#23
H_D#21	M5	H_D#_21	H_A#_24	A17	H_A#24
H_D#22	J3	H_D#_22	H_A#_25	B17	H_A#25
H_D#23	N2	H_D#_23	H_A#_26	L16	H_A#26
H_D#24	R1	H_D#_24	H_A#_27	C21	H_A#27
H_D#25	N5	H_D#_25	H_A#_28	J17	H_A#28
H_D#26	N6	H_D#_26	H_A#_29	H20	H_A#29
H_D#27	P13	H_D#_27	H_A#_30	B18	H_A#30
H_D#28	N8	H_D#_28	H_A#_31	K17	H_A#31
H_D#29	L7	H_D#_29	H_A#_32	B20	H_A#32
H_D#30	N10	H_D#_30	H_A#_33	F21	H_A#33
H_D#31	M3	H_D#_31	H_A#_34	K21	H_A#34
H_D#32	Y3	H_D#_32	H_A#_35	L20	H_A#35
H_D#33	AD14	H_D#_33			
H_D#34	Y6	H_D#_34			
H_D#35	Y10	H_D#_35			
H_D#36	Y12	H_D#_36			
H_D#37	Y14	H_D#_37			
H_D#38	Y7	H_D#_38			
H_D#39	W2	H_D#_39			
H_D#40	AA8	H_D#_40			
H_D#41	Y9	H_D#_41			
H_D#42	AA13	H_D#_42			
H_D#43	AA9	H_D#_43			
H_D#44	AA11	H_D#_44			
H_D#45	AD11	H_D#_45			
H_D#46	AD10	H_D#_46			
H_D#47	AD13	H_D#_47			
H_D#48	AE12	H_D#_48			
H_D#49	AE9	H_D#_49			
H_D#50	AA2	H_D#_50			
H_D#51	AD8	H_D#_51			
H_D#52	AA3	H_D#_52			
H_D#53	AD3	H_D#_53			
H_D#54	AD7	H_D#_54			
H_D#55	AE14	H_D#_55			
H_D#56	AF3	H_D#_56			
H_D#57	AC1	H_D#_57			
H_D#58	AE3	H_D#_58			
H_D#59	AC3	H_D#_59			
H_D#60	AE11	H_D#_60			
H_D#61	AE8	H_D#_61			
H_D#62	AG2	H_D#_62			
H_D#63	AD6	H_D#_63			
H_SWING	C5	H_SWING			
H_RCOMP	E3	H_RCOMP			
		H_CPURST#			
		H_CPUSLP#			
	A11	H_AVREF			
	B11	H_DVREF			

HOST

CANTIGA_CHIPSET

H_ADS#	H12	H_ADS#	H_ADS# [4]
H_ADSTB#_0	B16	H_ADSTB#0	H_ADSTB#0 [4]
H_ADSTB#_1	G17	H_ADSTB#1	H_ADSTB#1 [4]
H_BNR#	A9	H_BNR#	H_BNR# [4]
H_BPRI#	F11	H_BPRI#	H_BPRI# [4]
H_BREQ#	G12	H_BREQ#0	H_BREQ#0 [4]
H_DEFER#	E9	H_DEFER#	H_DEFER# [4]
H_DBSY#	B10	H_DBSY#	H_DBSY# [4]
HPLL_CLK	AH7		CLK_MCH_BCLK [7]
HPLL_CLK#	AH6		CLK_MCH_BCLK# [7]
H_DPWR#	J11	H_DPWR#	H_DPWR# [4]
H_DRDY#	F9	H_DRDY#	H_DRDY# [4]
H_HIT#	H9		H_HIT# [4]
H_HITM#	E12		H_HITM# [4]
H_LOCK#	H11		H_LOCK# [4]
H_TRDY#	C9		H_TRDY# [4]

H_DINV#_0	J8	H_DINV#0 [4]
H_DINV#_1	L3	H_DINV#1 [4]
H_DINV#_2	Y13	H_DINV#2 [4]
H_DINV#_3	Y1	H_DINV#3 [4]
H_DSTBN#_0	L10	H_DSTBN#0 [4]
H_DSTBN#_1	M7	H_DSTBN#1 [4]
H_DSTBN#_2	AA5	H_DSTBN#2 [4]
H_DSTBN#_3	AE6	H_DSTBN#3 [4]
H_DSTBP#_0	L9	H_DSTBP#0 [4]
H_DSTBP#_1	M8	H_DSTBP#1 [4]
H_DSTBP#_2	AA6	H_DSTBP#2 [4]
H_DSTBP#_3	AE5	H_DSTBP#3 [4]

H_REQ#_0	B15	H_REQ#0	
H_REQ#_1	K13	H_REQ#1	
H_REQ#_2	F13	H_REQ#2	
H_REQ#_3	B13	H_REQ#3	
H_REQ#_4	B14	H_REQ#4	
H_RS#_0	B6	H_RS#0	H_RS#0 [4]
H_RS#_1	F12	H_RS#1	H_RS#1 [4]
H_RS#_2	C8	H_RS#2	H_RS#2 [4]

[4] H_REQ#[4:0] H_REQ#[4:0]

Part Number: 02G010022500

Part Name & Spec:C.S 88CTPM (B2) INTEL PM45 QT78 897258 QS

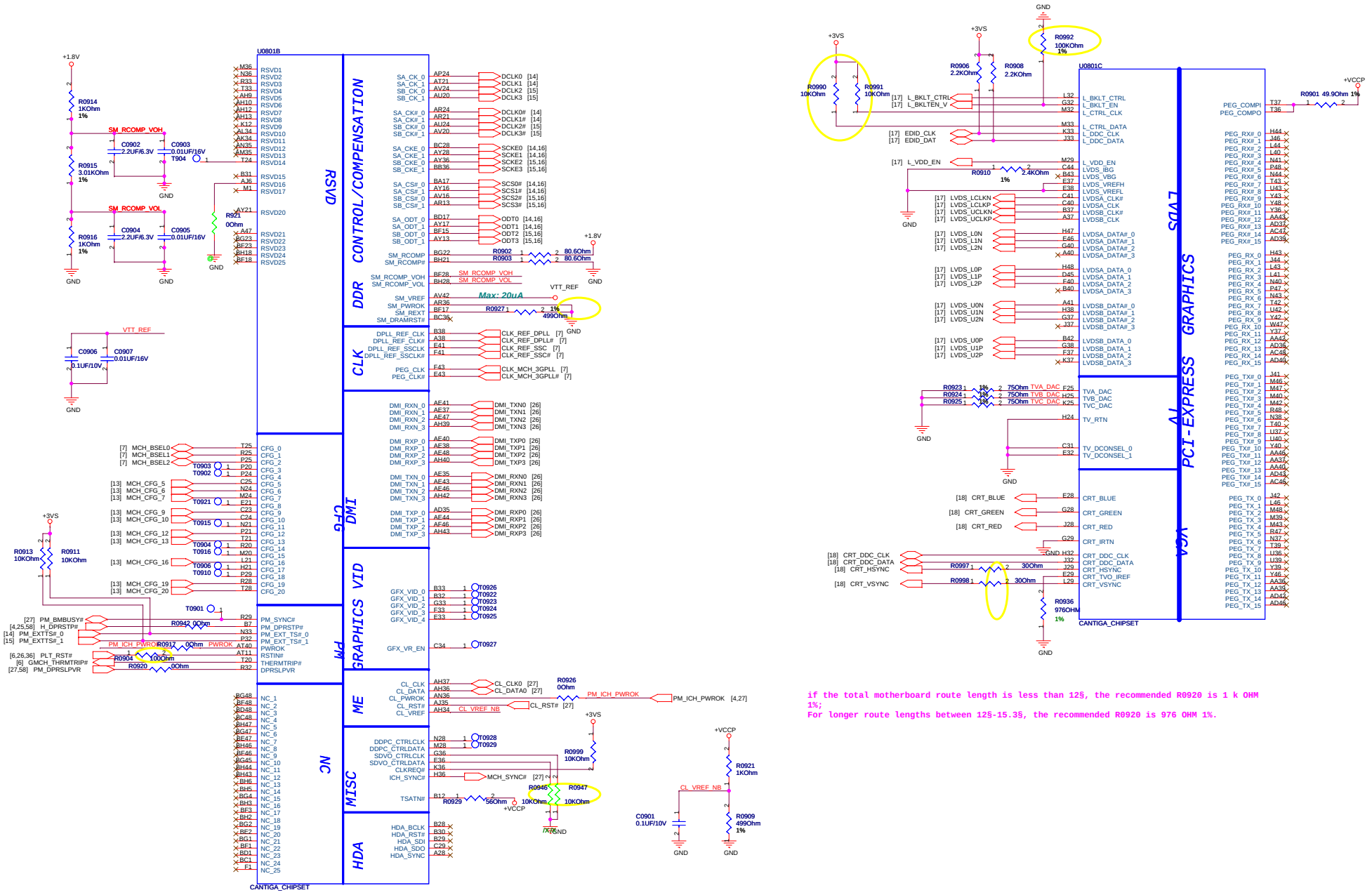
<Variant Name>

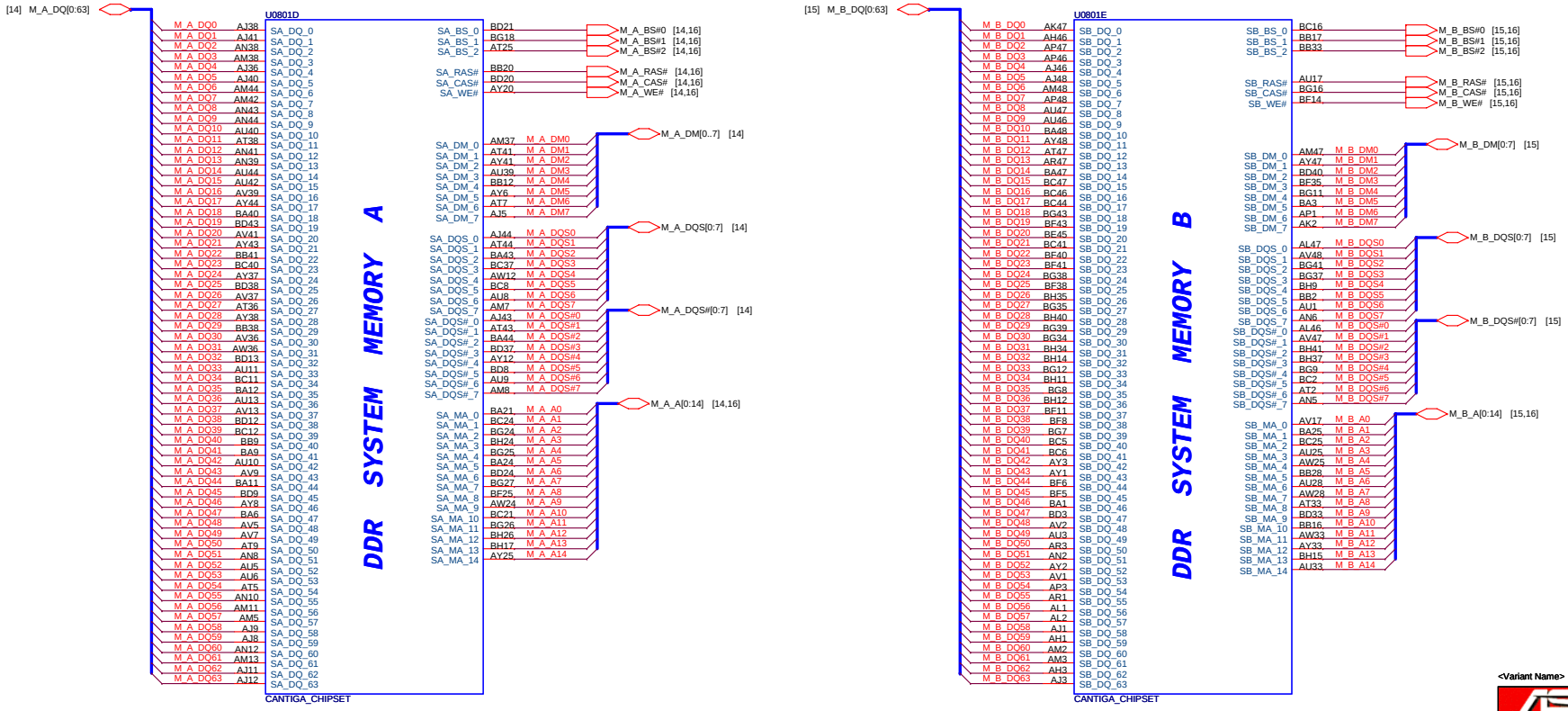
Title : Cantiga -- CPU (1)

ASUSTeK COMPUTER INC Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 8 of 59


U0801B
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
VID
GRAPHICS
PM
ME
MISC
HDA
NC
CANTIGA_CHIPSET
U0801C
LVDS
PCI-EXPRESS
GRAPHICS
VGA
CANTIGA_CHIPSET
SM_RCOMP_VOH
SM_RCOMP_VOL
VTT_REF
Max: 20uA
PM_ICH_PWROK
CL_VREF_NB
if the total motherboard route length is less than 12§, the recommended R0920 is 1 k OHM 1%;
For longer route lengths between 12§-15.3§, the recommended R0920 is 976 OHM 1%.
<Variant Name>
Title : Cantiga-DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer: Xinghua_Chen
Size: Custom
Project Name: F80Q
Rev: 2.00
Date: Friday, May 23, 2008
Sheet 9 of 59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M_A_DQ1 AJ41
M_A_DQ2 AN38
M_A_DQ3 AM38
M_A_DQ4 AJ36
M_A_DQ5 AJ40
M_A_DQ6 AM44
M_A_DQ7 AM42
M_A_DQ8 AN43
M_A_DQ9 AN44
M_A_DQ10 AU40
M_A_DQ11 AT38
M_A_DQ12 AN41
M_A_DQ13 AN39
M_A_DQ14 AU44
M_A_DQ15 AU42
M_A_DQ16 AV39
M_A_DQ17 AY44
M_A_DQ18 BA40
M_A_DQ19 BD43
M_A_DQ20 AV41
M_A_DQ21 AY43
M_A_DQ22 BB41
M_A_DQ23 BC40
M_A_DQ24 AY37
M_A_DQ25 BD38
M_A_DQ26 AV37
M_A_DQ27 AT36
M_A_DQ28 AY38
M_A_DQ29 BB38
M_A_DQ30 AV36
M_A_DQ31 AW36
M_A_DQ32 BD13
M_A_DQ33 AU11
M_A_DQ34 BC11
M_A_DQ35 BA12
M_A_DQ36 AU13
M_A_DQ37 AV13
M_A_DQ38 BD12
M_A_DQ39 BC12
M_A_DQ40 BB9
M_A_DQ41 BA9
M_A_DQ42 AU10
M_A_DQ43 AV9
M_A_DQ44 BA11
M_A_DQ45 BD9
M_A_DQ46 AY8
M_A_DQ47 BA6
M_A_DQ48 AV5
M_A_DQ49 AV7
M_A_DQ50 AT9
M_A_DQ51 AN8
M_A_DQ52 AU5
M_A_DQ53 AU6
M_A_DQ54 AT5
M_A_DQ55 AN10
M_A_DQ56 AM11
M_A_DQ57 AM5
M_A_DQ58 AJ9
M_A_DQ59 AJ8
M_A_DQ60 AN12
M_A_DQ61 AM13
M_A_DQ62 AJ11
M_A_DQ63 AJ12
SA_DQ_0
SA_DQ_1
SA_DQ_2
SA_DQ_3
SA_DQ_4
SA_DQ_5
SA_DQ_6
SA_DQ_7
SA_DQ_8
SA_DQ_9
SA_DQ_10
SA_DQ_11
SA_DQ_12
SA_DQ_13
SA_DQ_14
SA_DQ_15
SA_DQ_16
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SA_DQ_56
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SA_DQ_58
SA_DQ_59
SA_DQ_60
SA_DQ_61
SA_DQ_62
SA_DQ_63
DDR SYSTEM MEMORY A
CANTIGA_CHIPSET
SA_BS_0 BD21
SA_BS_1 BG18
SA_BS_2 AT25
SA_RAS# BB20
SA_CAS# BD20
SA_WE# AY20
M_A_BS#0 [14,16]
M_A_BS#1 [14,16]
M_A_BS#2 [14,16]
M_A_CAS# [14,16]
M_A_WE# [14,16]
SA_DM_0 AM37 M_A_DM0
SA_DM_1 AT41 M_A_DM1
SA_DM_2 AY41 M_A_DM2
SA_DM_3 AU39 M_A_DM3
SA_DM_4 BB12 M_A_DM4
SA_DM_5 AY6 M_A_DM5
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SA_DM_7 AJ5 M_A_DM7
M_A_DM[0..7] [14]
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SA_DQS_4 AW12 M_A_DQS4
SA_DQS_5 BC8 M_A_DQS5
SA_DQS_6 AU8 M_A_DQS6
SA_DQS_7 AM7 M_A_DQS7
M_A_DQS[0:7] [14]
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SA_DQS#_1 AT43 M_A_DQS#1
SA_DQS#_2 BA44 M_A_DQS#2
SA_DQS#_3 BD37 M_A_DQS#3
SA_DQS#_4 AY12 M_A_DQS#4
SA_DQS#_5 BD8 M_A_DQS#5
SA_DQS#_6 AU9 M_A_DQS#6
SA_DQS#_7 AM8 M_A_DQS#7
M_A_DQS#[0:7] [14]
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SA_MA_1 BC24 M_A_A1
SA_MA_2 BG24 M_A_A2
SA_MA_3 BH24 M_A_A3
SA_MA_4 BG25 M_A_A4
SA_MA_5 BA24 M_A_A5
SA_MA_6 BD24 M_A_A6
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SA_MA_8 BF25 M_A_A8
SA_MA_9 AW24 M_A_A9
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SA_MA_11 BG26 M_A_A11
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SB_DQ_63
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CANTIGA_CHIPSET
SB_BS_0 BC16
SB_BS_1 BB17
SB_BS_2 BB33
SB_RAS# AU17
SB_CAS# BG16
SB_WE# BF14
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M_B_BS#1 [15,16]
M_B_BS#2 [15,16]
M_B_RAS# [15,16]
M_B_CAS# [15,16]
M_B_WE# [15,16]
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SB_DM_2 BD40 M_B_DM2
SB_DM_3 BF35 M_B_DM3
SB_DM_4 BG11 M_B_DM4
SB_DM_5 BA3 M_B_DM5
SB_DM_6 AP1 M_B_DM6
SB_DM_7 AK2 M_B_DM7
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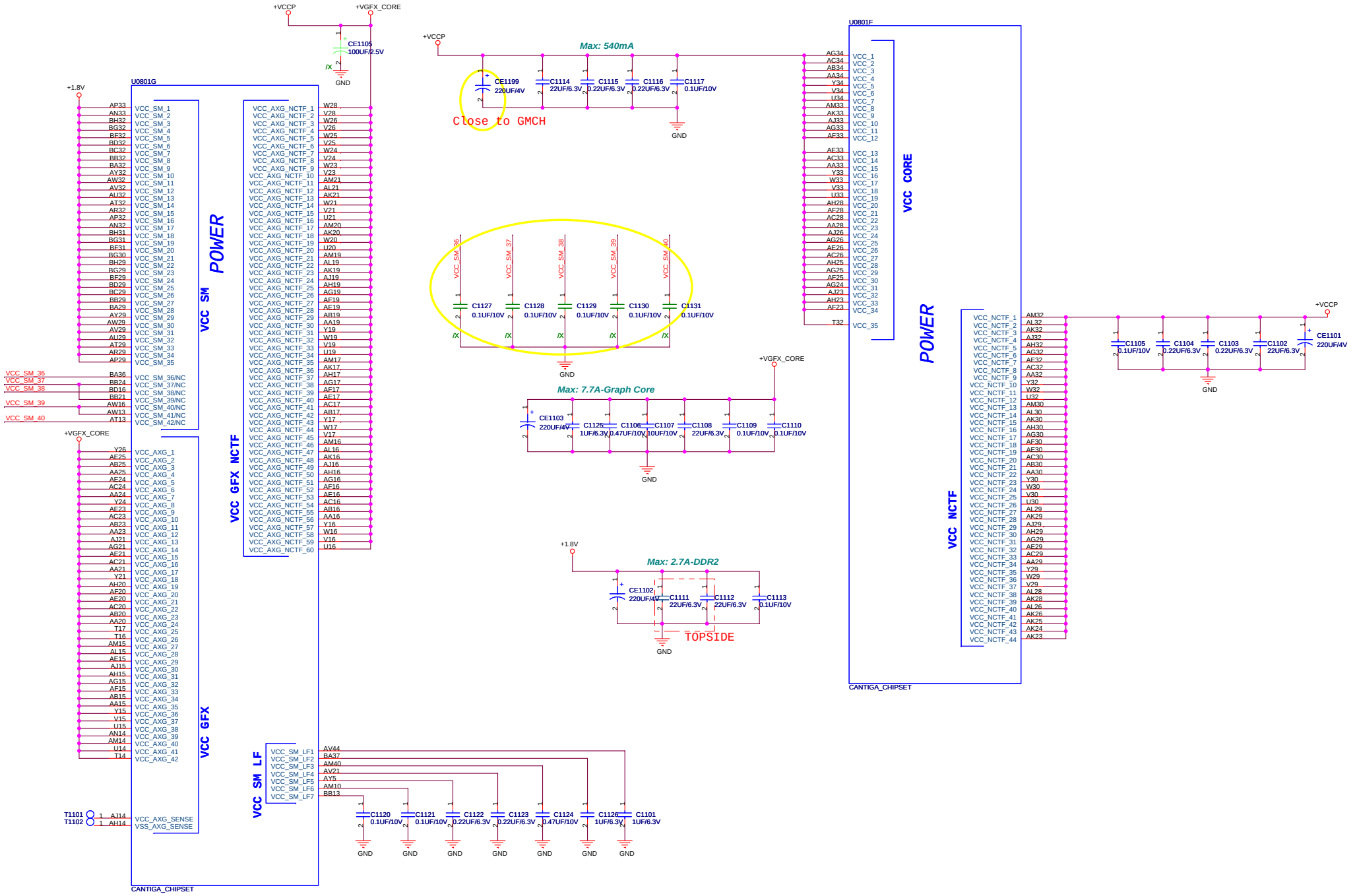
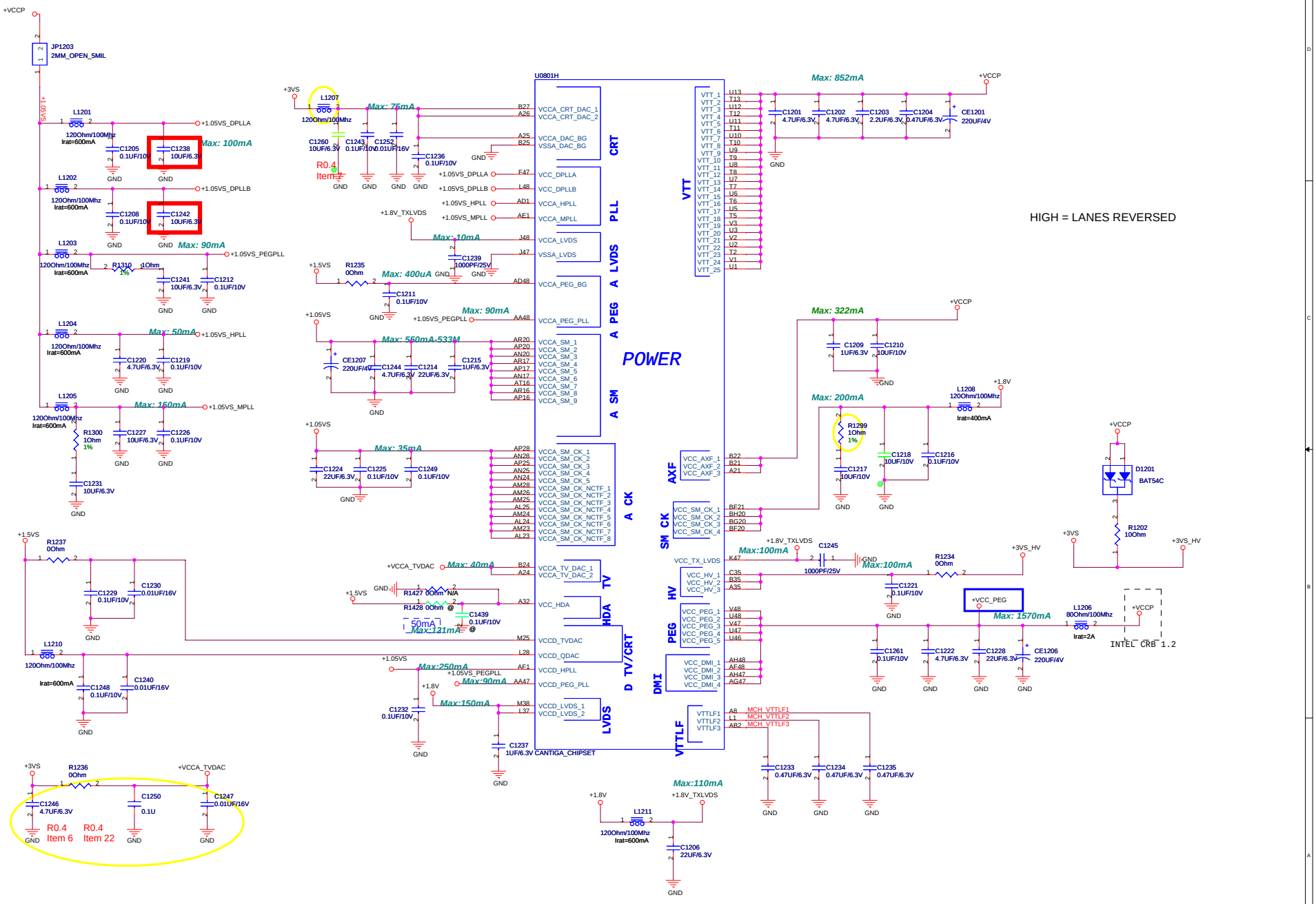
SB_DQS_1 AV48 M_B_DQS1
SB_DQS_2 BG41 M_B_DQS2
SB_DQS_3 BG37 M_B_DQS3
SB_DQS_4 BH9 M_B_DQS4
SB_DQS_5 BB2 M_B_DQS5
SB_DQS_6 AU1 M_B_DQS6
SB_DQS_7 AN6 M_B_DQS7
M_B_DQS[0:7] [15]
SB_DQS#_0 AL46 M_B_DQS#0
SB_DQS#_1 AV47 M_B_DQS#1
SB_DQS#_2 BH41 M_B_DQS#2
SB_DQS#_3 BH37 M_B_DQS#3
SB_DQS#_4 BG9 M_B_DQS#4
SB_DQS#_5 BC2 M_B_DQS#5
SB_DQS#_6 AT2 M_B_DQS#6
SB_DQS#_7 AN5 M_B_DQS#7
M_B_DQS#[0:7] [15]
SB_MA_0 AV17 M_B_A0
SB_MA_1 BA25 M_B_A1
SB_MA_2 BC25 M_B_A2
SB_MA_3 AU25 M_B_A3
SB_MA_4 AW25 M_B_A4
SB_MA_5 BB28 M_B_A5
SB_MA_6 AU28 M_B_A6
SB_MA_7 AW28 M_B_A7
SB_MA_8 AT33 M_B_A8
SB_MA_9 BD33 M_B_A9
SB_MA_10 BB16 M_B_A10
SB_MA_11 AW33 M_B_A11
SB_MA_12 AY33 M_B_A12
SB_MA_13 BH15 M_B_A13
SB_MA_14 AU33 M_B_A14
M_B_A[0:14] [15,16]
<Variant Name>
Title : Cantiga--DDR2 bus (3)
ASUSTeK COMPUTER INC
Engineer: Xinghua_Chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 10 of 59



<variant_name>

ASUSTeK COMPUTER INC	Title : Cantiga--POWER (4)	
	Engineer: Xinghua_chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 11 of 59	



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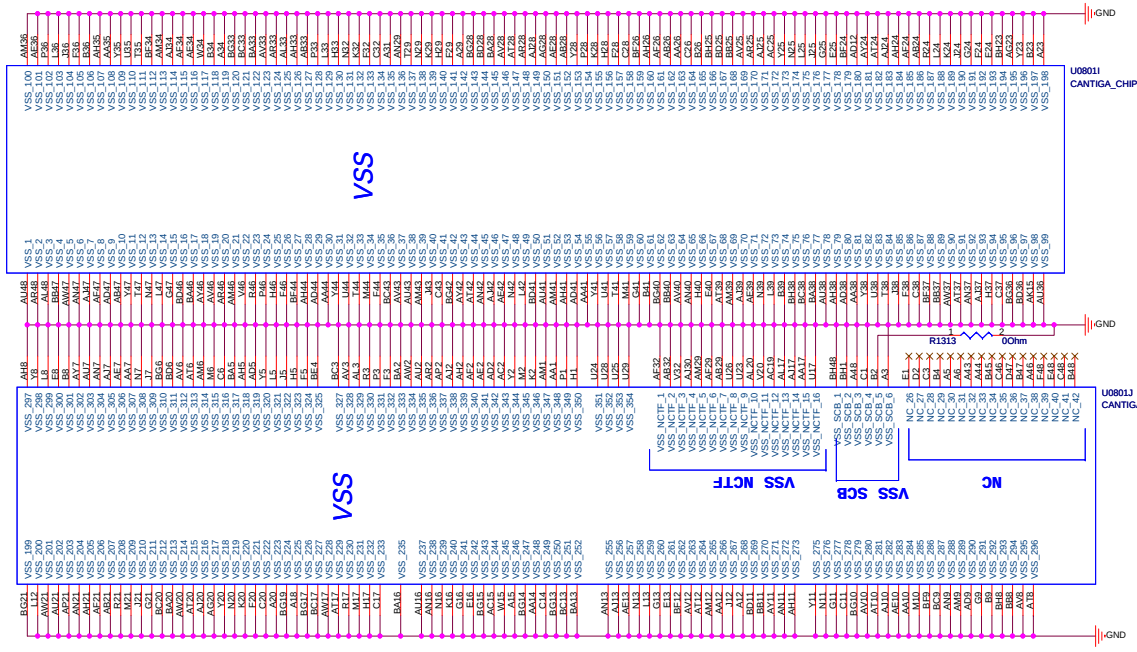
ASUSTeK COMPUTER INC	Title : Cantiga--POWER (5)	
	Engineer: Xinghua_chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 12 of 59	



[9] MCH_CFG_5

R0.4
Item 20

R1301
2.21KOhm
@

GND

CFG5 : DMI STRAP

HIGH = DMI X 4 (Default)

LOW = DMI X 2

[9] MCH_CFG_6

R1306
2.21KOhm
@

GND

CFG6 : Integrated TPM Host Interface

HIGH = iTPM disable (Default)

LOW = iTPM enable

[9] MCH_CFG_7

R1304
2.21KOhm
@

GND

CFG7 : Intel Management Engine Crypto strap

HIGH = TLS cipher suite with confidentiality (Default)

LOW = TLS cipher suite with no confidentiality

[9] MCH_CFG_9

R1302
2.21KOhm
@

GND

CFG9 : PCI Express Graphics Lane Reversal

LOW = Lane Reversed

HIGH = Normal mode (Default; lanes numbered in order)

CHECK detail...

[9] MCH_CFG_13

R1399
2.21KOhm
@

GND

CFG [13:12] : XOR/ALL-Z

00 = Reserved

01= XOR Mode Enabled

10= All-Z Mode Enabled

11= Normal Operation (Default)

[9] MCH_CFG_12

R1309
2.21KOhm
@

GND

[9] MCH_CFG_16

R1305
2.21KOhm
@

GND

CFG16 : FSB Dynamic ODT

Low = Dynamic ODT Disabled

HIGH = Dyanamic ODT Enabled (default)

[9] MCH_CFG_10

R1308
2.21KOhm
@

GND

CFG10 : PCIe Loopback

HIGH = Disable (Default)

LOW = Enable

+3VS

[9] MCH_CFG_19

R1303
4.02KOHM
@

CFG19 : DMI Lane Reversal

LOW = Normal (default)

HIGH = LANES REVERSED

+3VS

[9] MCH_CFG_20

R1307
4.02KOHM
@

CFG20 : Concurrent SDVO / PCIe

LOW = Only SDVO or PCIE is operational (default)

HIGH = SDVO and PCIE are operating simultaneously via the PEG port

CHECK detail...

<Variant Name>

Title : GND/Strapping (6)

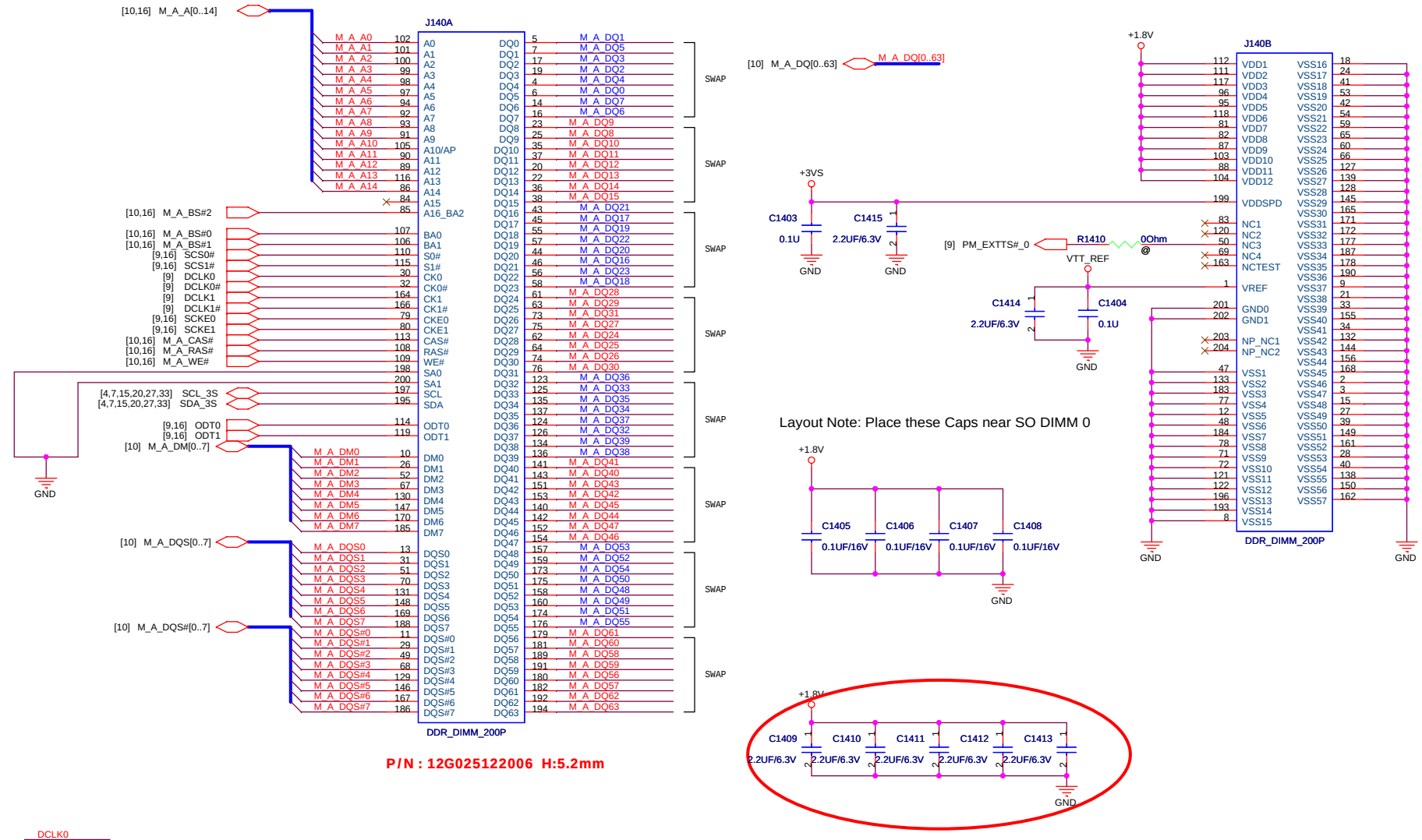
ASUSTeK COMPUTER INC

Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 13 of 59

Reverse Type



<Variant Name>

ASUSTeK COMPUTER INC

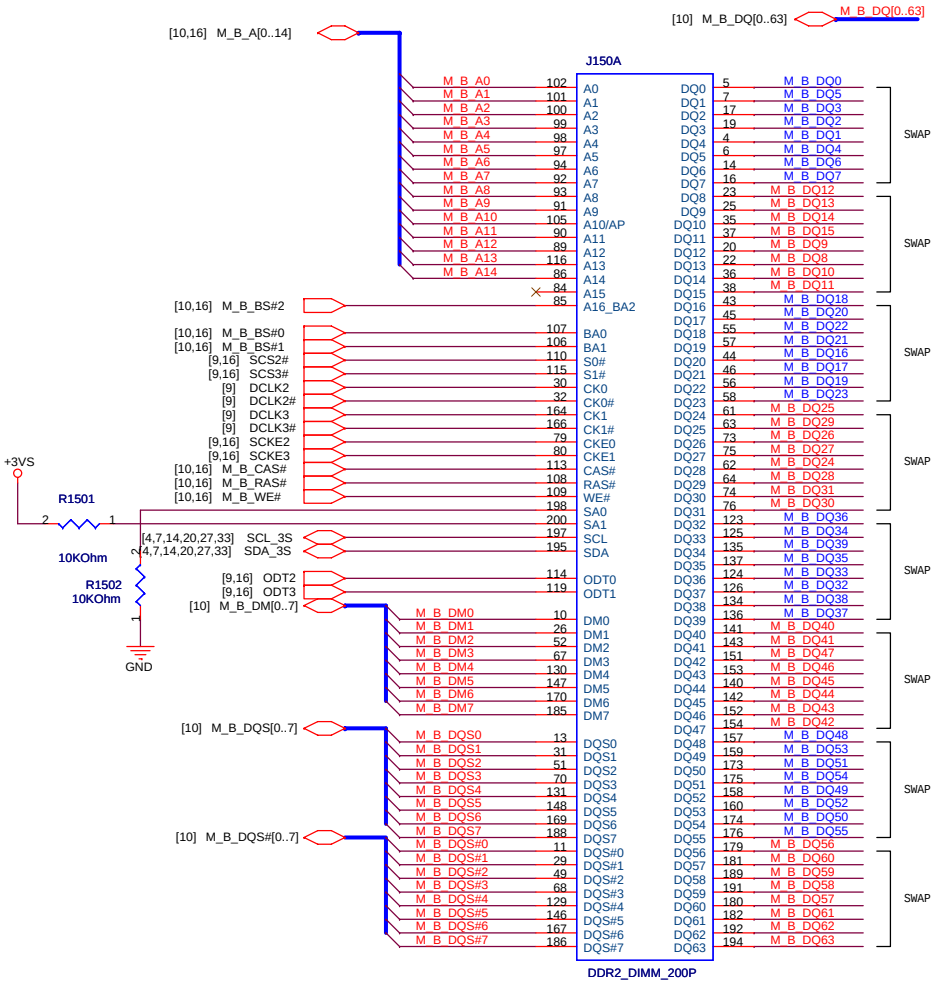
Title : DDR SO-DIMM 0

Engineer: Xinghua_Chen

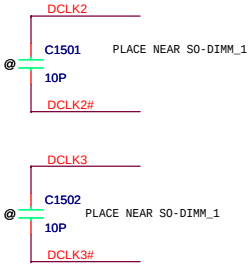
Size	Project Name	Rev
Custom	F80Q	2.00

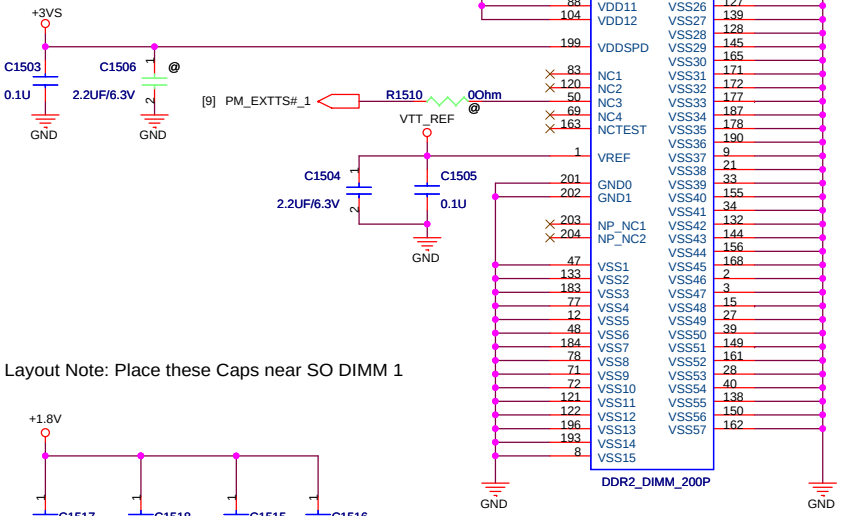
Date: Friday, May 23, 2008 Sheet 14 of 59

Reverse Type

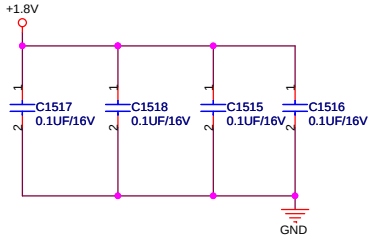


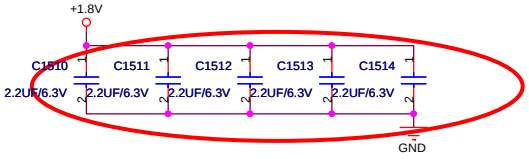
P/N : 12G025C22002 H:9.2mm





Layout Note: Place these Caps near SO DIMM 1



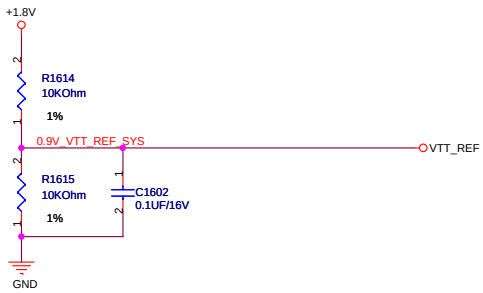


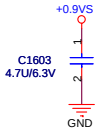
<Variant Name>

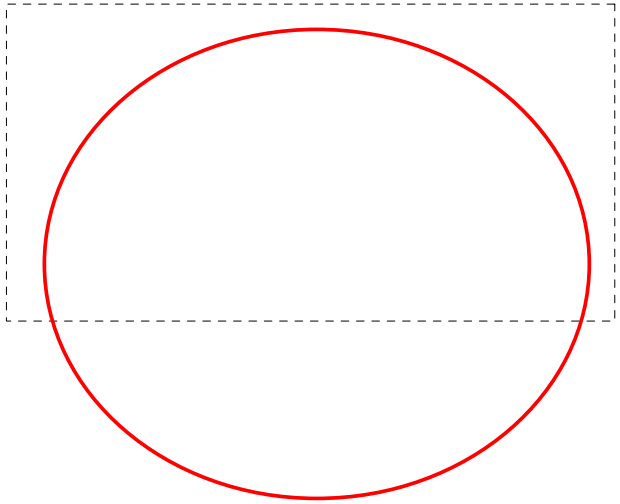
ASUSTeK COMPUTER INC	Title : DDR SO-DIMM_1	
	Engineer: Xinghua_Chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 15 of 59	

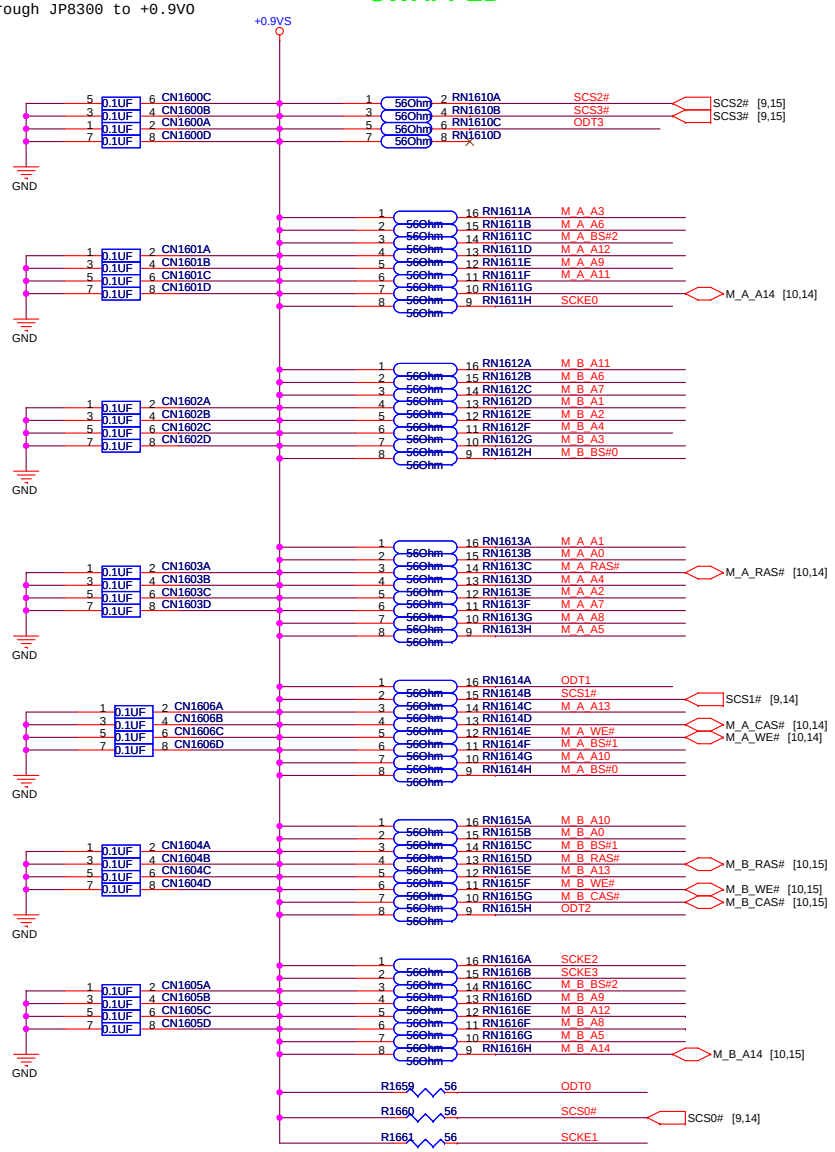
SWAPPED

+0.9VS through JP8300 to +0.9VO









Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

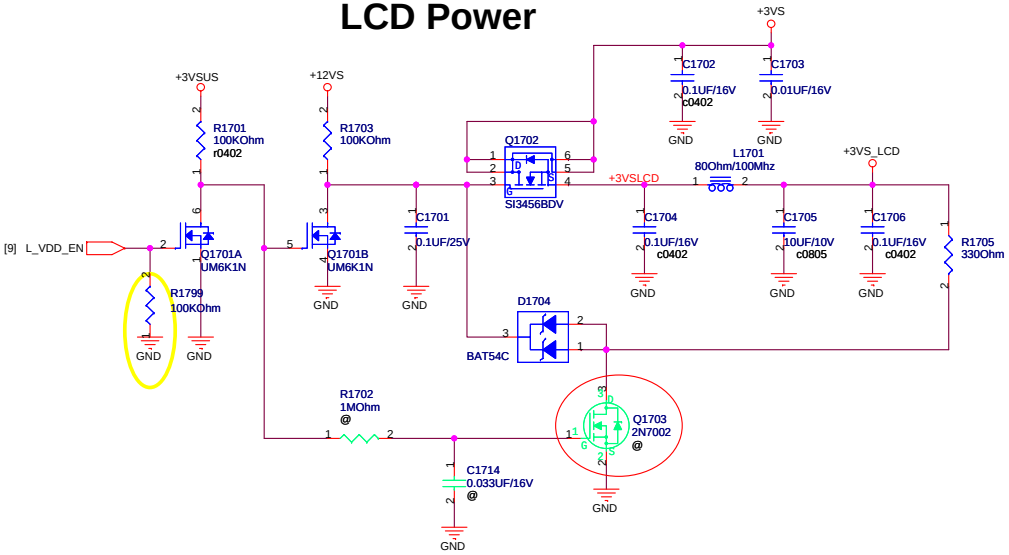
Title : DDR2 ADDR TERM

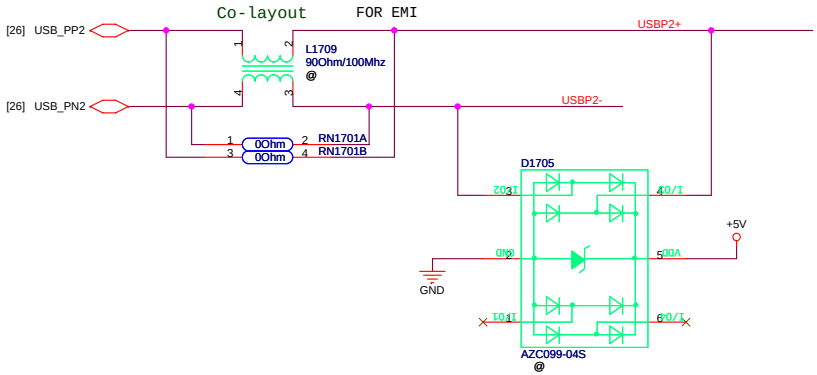
Engineer: CH Lin

Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 16 of 59

LCD Power

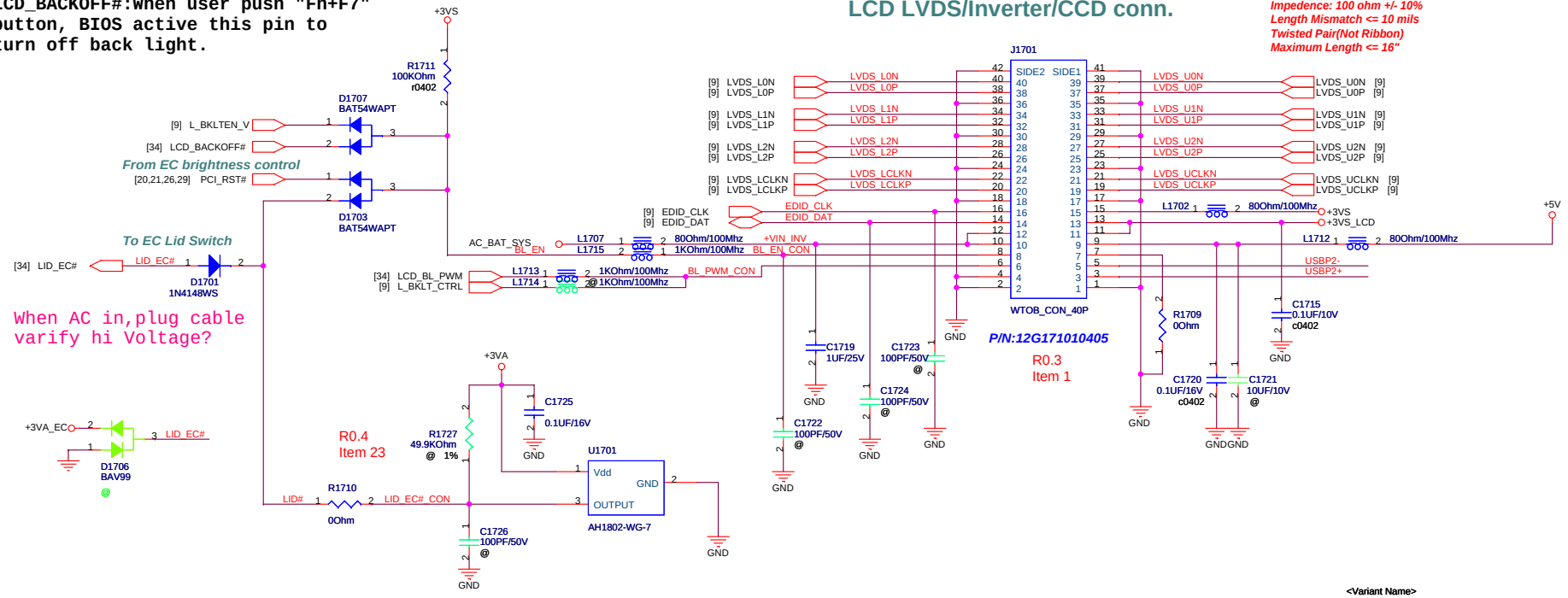




BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

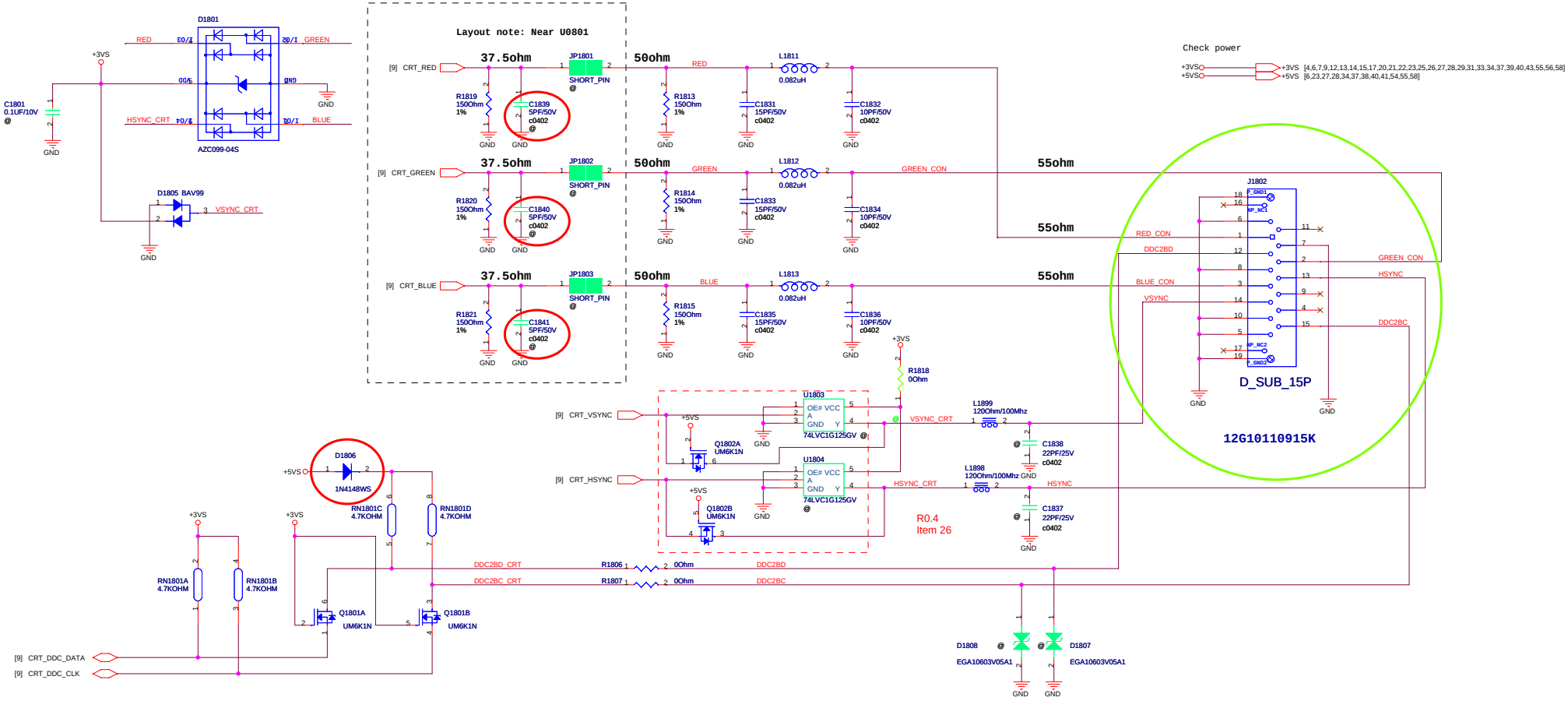
LCD LVDS/Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Xinghua_Chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 17 of 59	



<Variant Name>

ASUSTeK COMPUTER INC

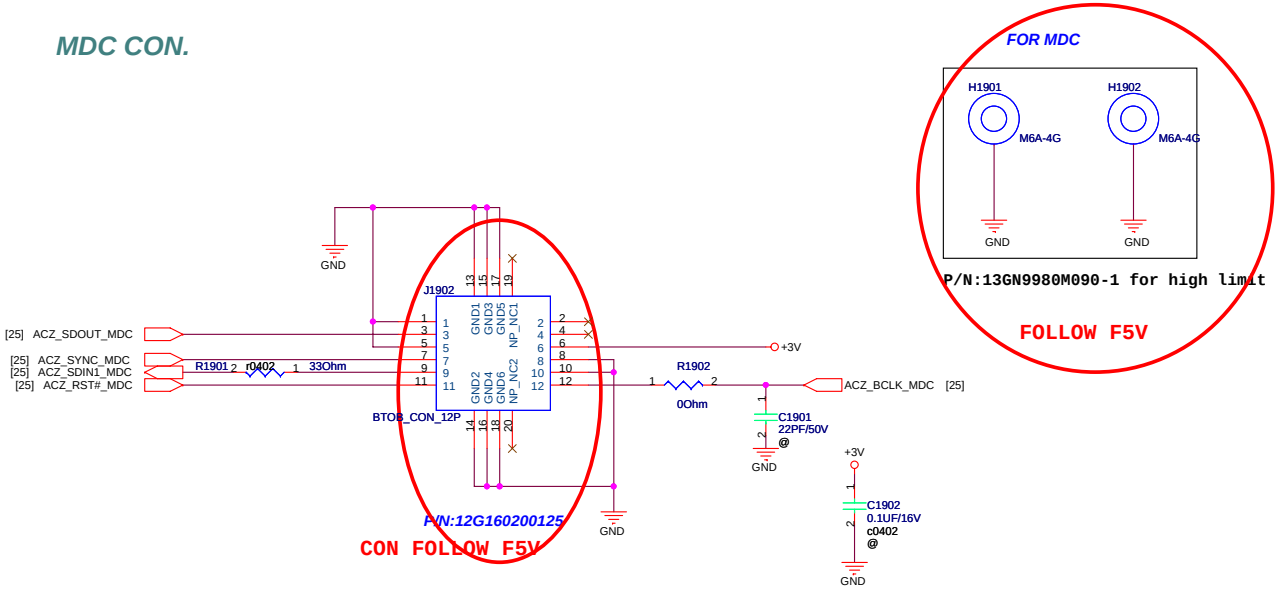
Title : CRT

Engineer: Xinghua_Chen

Size	Project Name	Rev
C	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 18 of 59

MDC CON.



ASUSTek COMPUTER INC.			
Li-Te Rd.,Peitou, Taipei,Taiwan, ROC			
Title: MDC CON		Xinghua_Chen	
Size: Custom	Document Number: F80Q		Rev: 2.00
Date: Friday, May 23, 2008	Sheet 19 of 59		

Reserved R to +3VSUS for
Wake on WLAN function!

+3VAUX_GOLAN
R2002 1 @ 2 0Ohm +3V
R2010 1 2 0Ohm +3VS

+3VAUX
R2001 1 @ 2 0Ohm +3VSUS
R2003 1 2 0Ohm +3V
R2004 1 @ 2 0Ohm +3VS

+1.5VS +1.5VS [5,12,25,28,31,33,37,40,52]
+3V +3V [19,21,26,33,34,35,36,37,55]
+3VS +3VS [4,6,7,9,12,13,14,15,17,18,21,22,23,25,26,27,28,29,31,33,34,37,39,40,43,55,56,58]

+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

WLAN

P/N : 12G03000052B

R2008 0Ohm 1 2 WLAN_WAKE#
R2014 0Ohm
R2012 0Ohm
T2003

[27,29,33] PCIE_WAKE#
[21] BT_CHDAT
[21] BT_CHCLK
[7] CLK_PCIE_WLAN#
[7] CLK_PCIE_WLAN
[26] PCIE_RXN2_ICH
[26] PCIE_RXP2_ICH
[26] PCIE_RXN2_MINICARD
[26] PCIE_RXP2_MINICARD

J2001 MINI_PCI_LATCH_52P

1	WAKE#	3.3V_1	2
3	BT_DATA	GND7	4
5	BT_CHCLK	1.5V_1	6
7	CLKREQ#	Reserved11	8
9	GND1	Reserved12	10
11	REFCLK-	Reserved13	12
13	REFCLK+	Reserved14	14
15	GND2	Reserved15	16
17	Reserved1	GND8	18
19	Reserved2	W_DISABLE#	20
21	GND3	PERST#	22
23	PERn0	3.3Vaux	24
25	PERp0	GND9	26
27	GND4	1.5V_2	28
29	GND5	Reserved16	30
31	PETn0	Reserved17	32
33	PETp0	GND10	34
35	GND6	Reserved18	36
37	Reserved3	Reserved19	38
39	Reserved4	GND11	40
41	Reserved5	NC1	42
43	Reserved6	LED_WLAN#	44
45	Reserved7	NC2	46
47	Reserved8	1.5V_3	48
49	Reserved9	GND12	50
51	Reserved10	3.3V_2	52
53	GND13	NP_NC2	56
54	GND14	NP_NC1	55

+3VAUX_GOLAN +1.5VS +3VAUX GND GND

RF_DEV_ON
R2018 0Ohm PCI_RST# [17,21,26,29]
R2017 0Ohm SCL_3S [4,7,14,15,27,33]
R2015 0Ohm SDA_3S [4,7,14,15,27,33]
T2004

H2001 A40M20-64AS GND
H2002 A40M20-64AS GND

+3VAUX_GOLAN
R2009 100KOhm r0402 *Intel SPEC(18780):Internal Pull UP 110Kohm* Int. PU for Windigo
D2102 1SS355
WLAN_ON [26]
[21,34,38] RF_ON_SW#
Q2001 2N7002

+3VAUX_GOLAN
C2001 c0805 10UF/10V
C2002 c0402 0.1UF/16V
C2003 c0402 0.1UF/16V
C2004 0.01UF/50V c0402
C2005 0.01UF/50V c0402
GND

+1.5VS
C2006 10U/10V
C2007 0.1U
C2008 0.1U
GND

ASUSTek COMPUTER INC.
Li-Te Rd.,Peitou, Taipei,Taiwan, ROC

Title: MINI CARD--(1)
Xinghua_chen
Size: Custom
Document Number: F80Q
Rev: 2.00
Date: Friday, May 23, 2008
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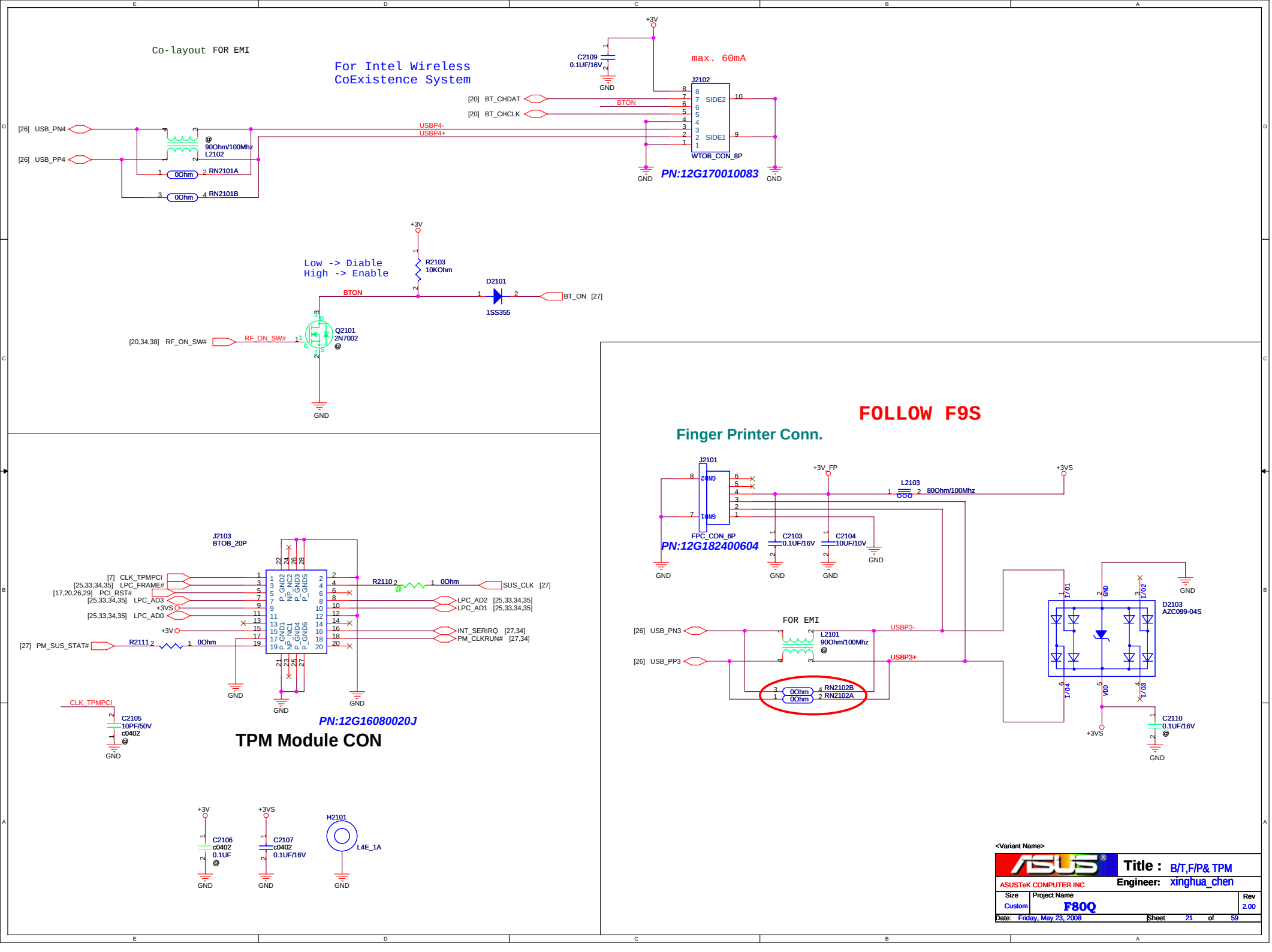
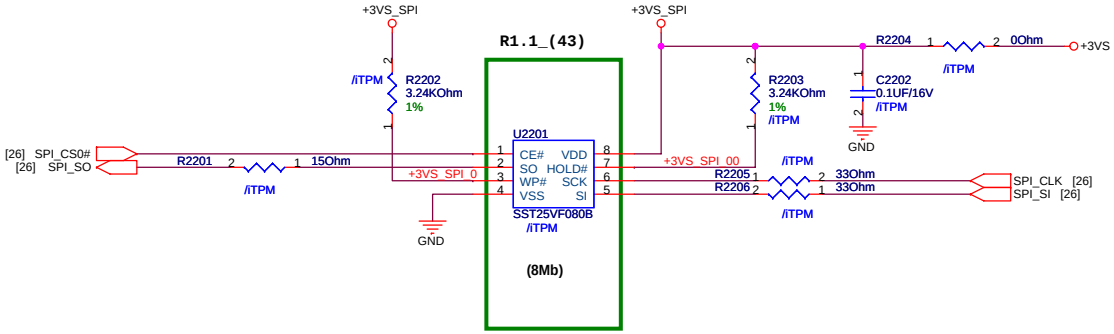

Co-layout FOR EMI
For Intel Wireless
CoExistence System
max. 60mA
C2109
0.1UF/16V
+3V
GND
J2102
WTOB_CON_8P
SIDE2
SIDE1
[20] BT_CHDAT
[20] BT_CHCLK
BTON
USBP4-
USBP4+
[26] USB_PN4
[26] USB_PP4
@
90Ohm/100Mhz
L2102
0Ohm
RN2101A
RN2101B
PN:12G170010083
Low -> Diable
High -> Enable
R2103
10KOhm
D2101
1SS355
BT_ON [27]
Q2101
2N7002
[20,34,38] RF_ON_SW#
RF_ON_SW#
FOLLOW F9S
Finger Printer Conn.
J2101
FPC_CON_6P
PN:12G182400604
+3V_FP
+3VS
L2103
80Ohm/100Mhz
C2103
0.1UF/16V
C2104
10UF/10V
FOR EMI
[26] USB_PN3
[26] USB_PP3
L2101
90Ohm/100Mhz
RN2102B
RN2102A
D2103
AZC099-04S
C2110
0.1UF/16V
J2103
BTOB_20P
[7] CLK_TPMPCI
[25,33,34,35] LPC_FRAME#
[17,20,26,29] PCI_RST#
[25,33,34,35] LPC_AD3
[25,33,34,35] LPC_AD0
+3VS
[27] PM_SUS_STAT#
R2111
R2110
SUS_CLK [27]
LPC_AD2 [25,33,34,35]
LPC_AD1 [25,33,34,35]
INT_SERIRQ [27,34]
PM_CLKRUN# [27,34]
CLK_TPMPCI
C2105
10PF/50V
c0402
PN:12G16080020J
TPM Module CON
C2106
c0402
0.1UF
C2107
c0402
0.1UF/16V
H2101
L4E_1A
<Variant Name>
Title : B/T,F/P& TPM
ASUSTeK COMPUTER INC
Engineer: xinghua_chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 21 of 59

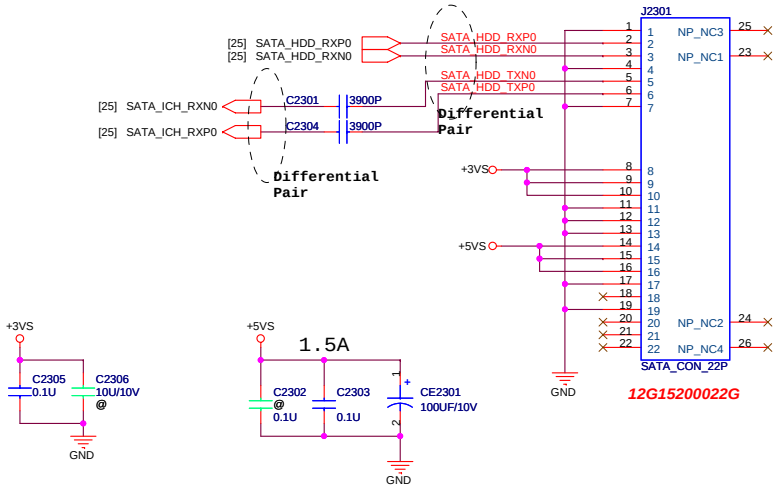
If don't support iTPM,unstuff these



<Variant Name>

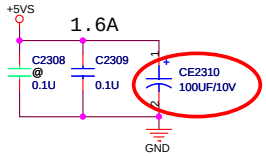
ASUSTeK COMPUTER INC	Title : iTPM	
	Engineer: Xinghua_chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 22 of 59	

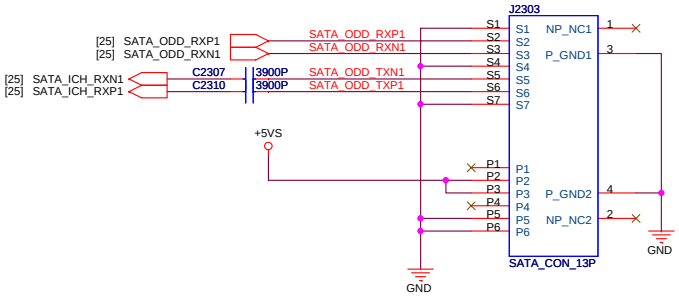
SATA HDD CON



SATA CD-ROM CON

P/N:12G15100013J



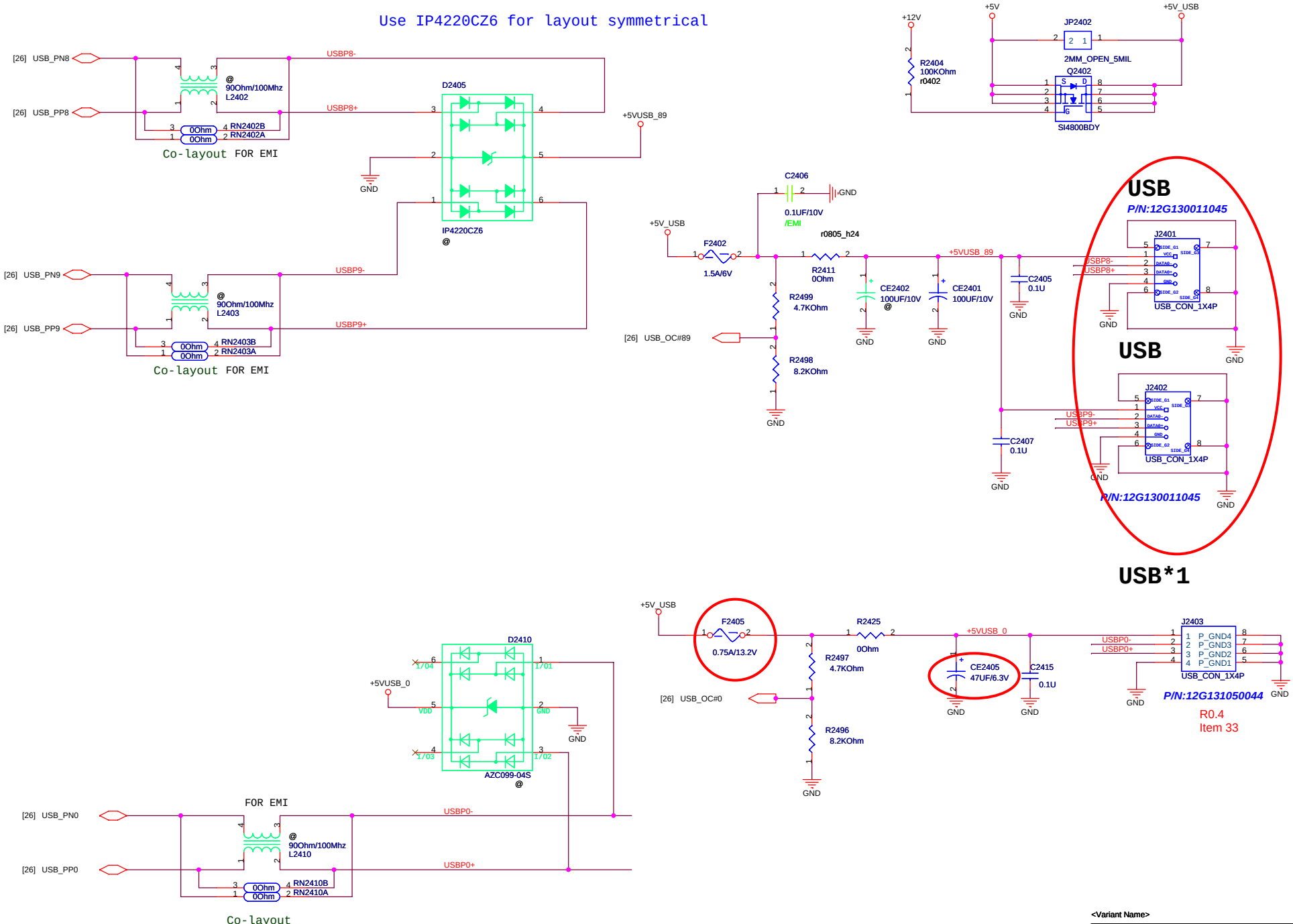


PATA ODD:
Mount R2301,R2303,R2304,R2310,R2308,R2306

<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: Xinghua_Chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 23 of 59	

Use IP4220CZ6 for layout symmetrical



<Variant Name>

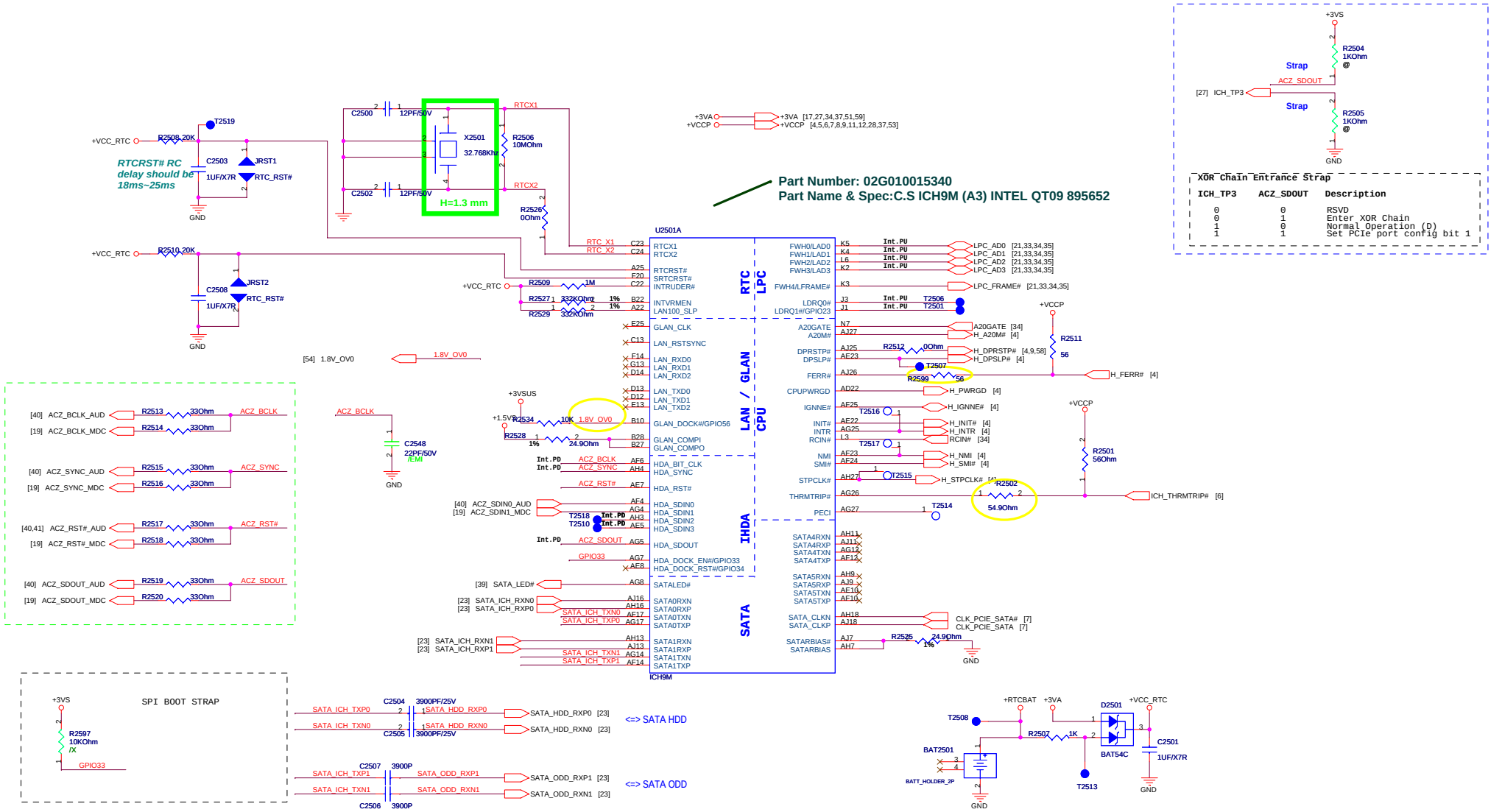
ASUSTeK COMPUTER INC

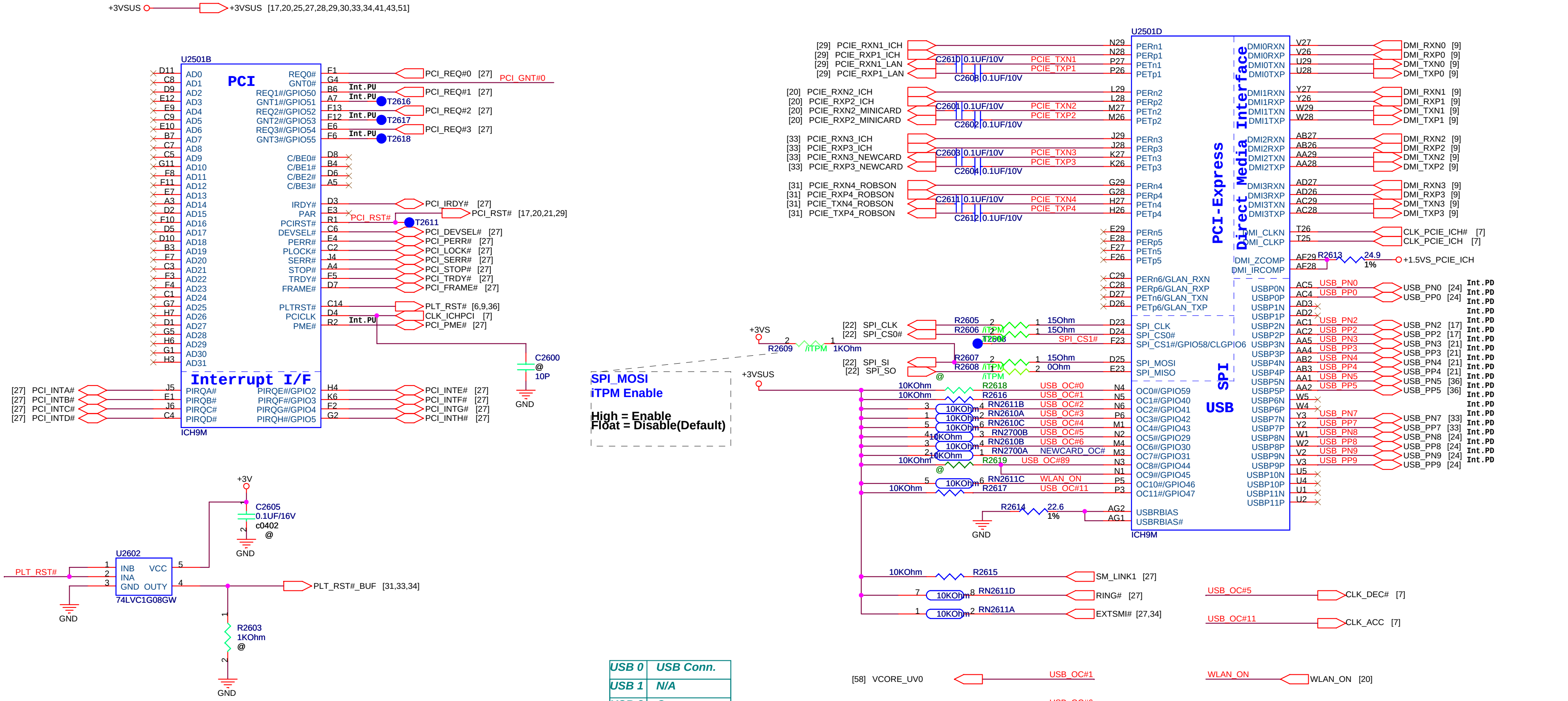
Title : USB PORTS

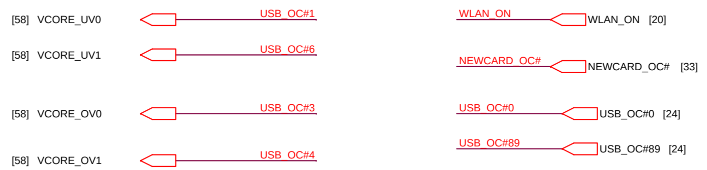
Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F80Q	2.00

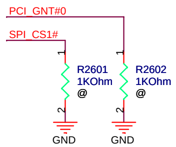
Date: Friday, May 23, 2008 Sheet 24 of 59


RTCRST# RC delay should be 18ms~25ms
H=1.3 mm
Part Number: 02G010015340
Part Name & Spec:C.S ICH9M (A3) INTEL QT09 895652
U2501A
ICH9M
RTC
LPC
GLAN
LAN / GLAN CPU
IHDA
SATA
SPI BOOT STRAP
<=> SATA HDD
<=> SATA ODD
Strap
XOR Chain Entrance Strap
ICH_TP3 ACZ_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (D)
1 1 Set PCIe port config bit 1
<Variant Name>
Title : ICH9-M (1)
ASUSTeK COMPUTER INC
Engineer: Xinghua_chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 25 of 59





USB 0	USB Conn.
USB 1	N/A
USB 2	Camera
USB 3	Finger Printer
USB 4	Bluetooth
USB 5	Card Reader
USB 6	N/A
USB 7	Newcard
USB 8	USB Conn.
USB 9	USB Conn.



ICH8 Boot BIOS Select

	GNT#0	CS#1
LPC	H	H
PCI	H	L
SPI	L	H

<Variant Name>

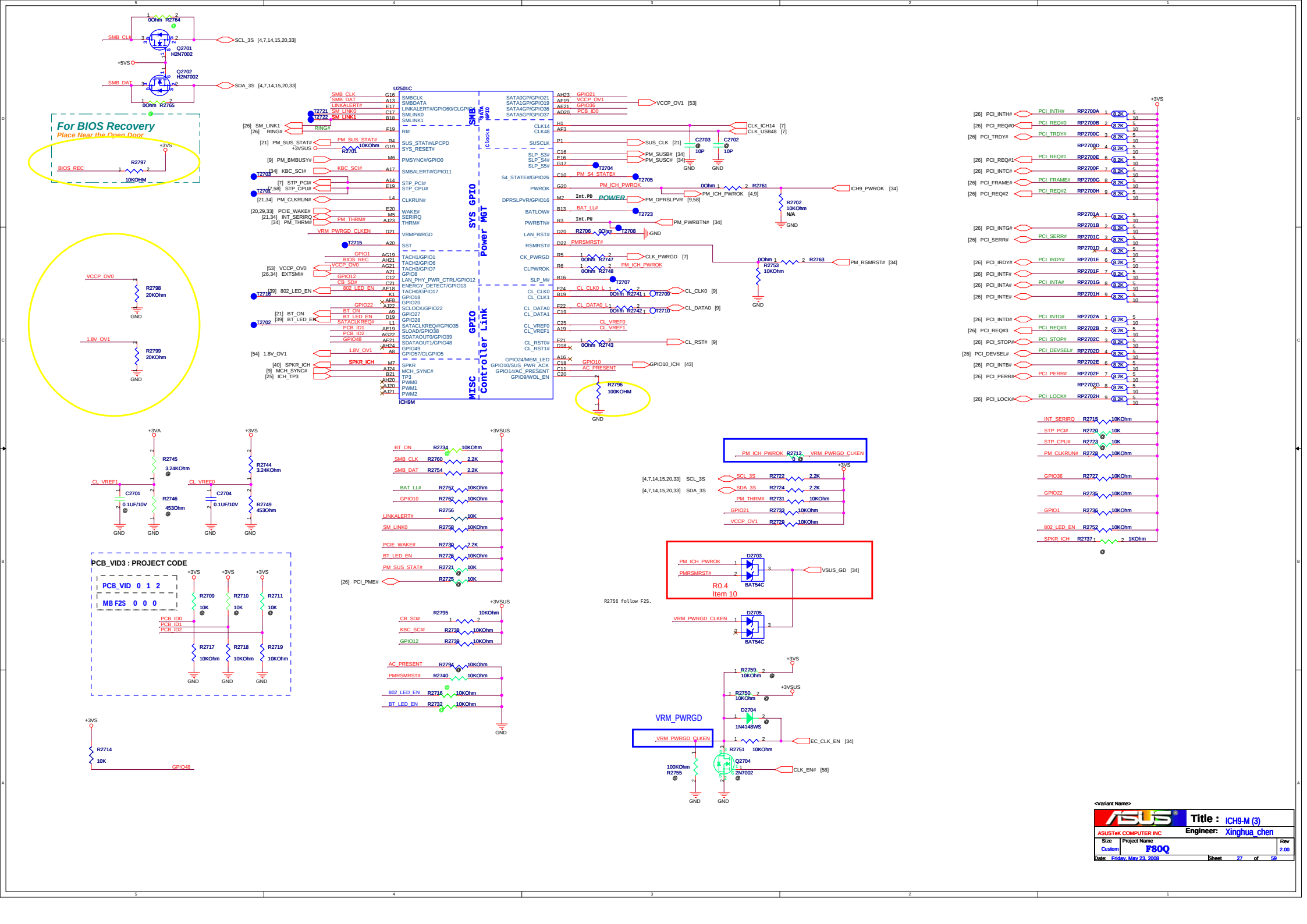
ASUSTeK COMPUTER INC

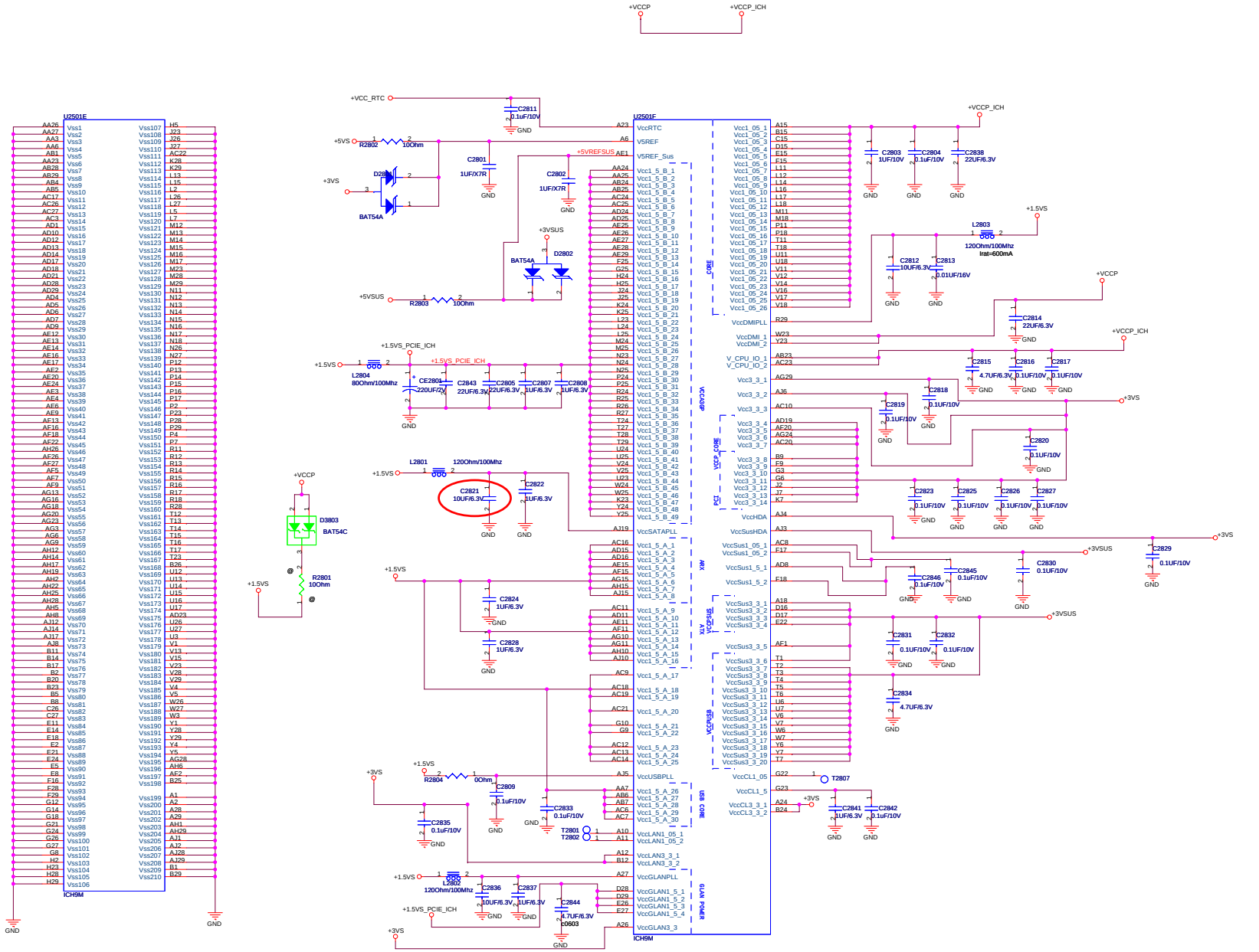
Title : ICH9-M (2)

Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 26 of 59

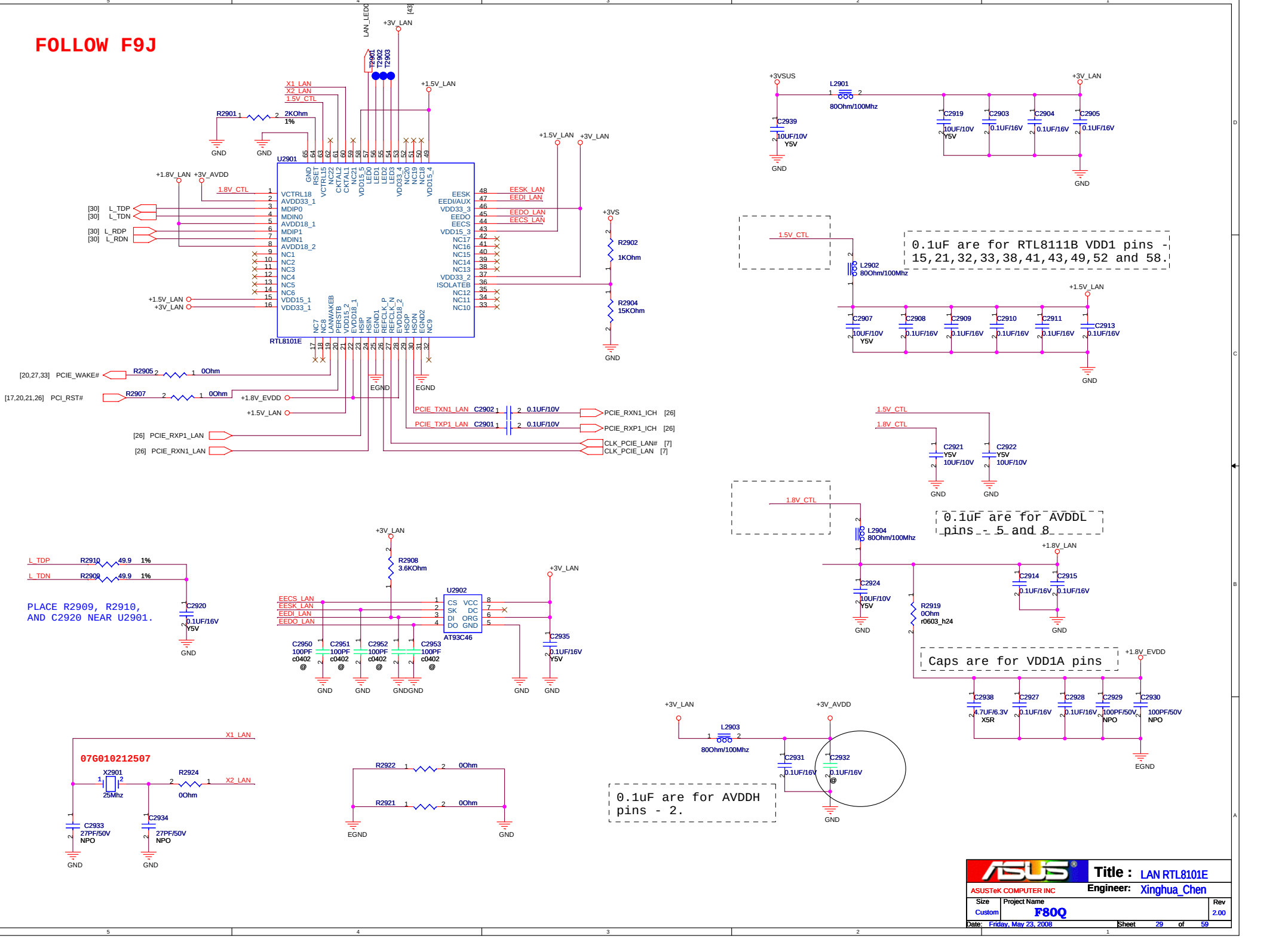

For BIOS Recovery
Place Near the Open Door
BIOS_REC
R2797
10KOHM
+3VS
SMB_CLK
SMB_DAT
Q2701
H2N7002
Q2702
H2N7002
SCL_3S [4,7,14,15,20,33]
SDA_3S [4,7,14,15,20,33]
R2764
R2765
0Ohm
U2501C
ICH9M
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO5
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SMB
SMLink
GPIO
IC Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
GPIO21
VCCP_OV1
GPIO36
PCB_ID0
CLK_ICH14 [7]
CLK_USB48 [7]
SUS_CLK [21]
PM_SUSB# [34]
PM_SUSC# [34]
PM_S4_STATE#
PM_ICH_PWROK
PM_DPRSLPVR [9,58]
BAT_LL#
PM_PWRBTN# [34]
PMRSMRST#
CLK_PWRGD [7]
PM_ICH_PWROK
CL_CLK0 [9]
CL_DATA0 [9]
CL_VREF0
CL_VREF1
CL_RST# [9]
GPIO10
AC_PRESENT
GPIO10_ICH [43]
ICH9_PWROK [34]
PM_RSMRST# [34]
R2796
100KOHM
R2702
10KOhm
N/A
R2753
10KOhm
R2763
R2706
R2708
R2747
R2748
R2741
R2742
R2743
T2707
T2709
T2710
T2723
T2704
T2705
T2715
T2716
T2702
T2721
T2722
SM_LINK0
SM_LINK1
RING#
PM_SUS_STAT#
R2701
KBC_SCI#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THRM#
VRM_PWRGD_CLKEN
GPIO1
BIOS_REC
VCCP_OV0
GPIO12
CB_SD#
802_LED_EN
BT_ON
BT_LED_EN
SATACLKREQ#
PCB_ID1
PCB_ID2
GPIO48
1.8V_OV1
SPKR_ICH
PM_MBBUSY#
PM_SUS_STAT#
+3VSUS
C2703
C2702
10P
GND
R2798
20KOhm
R2799
20KOhm
VCCP_OV0
1.8V_OV1
R2745
3.24KOhm
R2744
3.24KOhm
R2746
453Ohm
R2749
453Ohm
C2701
C2704
0.1UF/10V
CL_VREF1
CL_VREF0
+3VA
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB F2S 0 0 0
R2709
R2710
R2711
R2717
R2718
R2719
10K
10KOhm
R2714
GPIO48
R2734
R2760
R2754
R2757
R2762
R2756
R2758
R2730
R2726
R2721
R2725
R2795
R2738
R2739
R2794
R2740
R2716
R2732
2.2K
10K
10KOhm
[26] PCI_PME#
[53] VCCP_OV0
[26,34] EXTSMI#
[39] 802_LED_EN
[21] BT_ON
[39] BT_LED_EN
[54] 1.8V_OV1
[40] SPKR_ICH
[9] MCH_SYNC#
[25] ICH_TP3
[26] SM_LINK1
[26] RING#
[21] PM_SUS_STAT#
+3VSUS
[9] PM_MBBUSY#
[34] KBC_SCI#
[7] STP_PCI#
[7,58] STP_CPU#
[21,34] PM_CLKRUN#
[20,29,33] PCIE_WAKE#
[21,34] INT_SERIRQ
[34] PM_THRM#
VRM_PWRGD_CLKEN
PM_ICH_PWROK R2712 VRM_PWRGD_CLKEN
0 @
[4,7,14,15,20,33] SCL_3S
[4,7,14,15,20,33] SDA_3S
SCL_3S R2722 2.2K
SDA_3S R2724 2.2K
PM_THRM# R2731 10KOhm
GPIO21 R2733 10KOhm
VCCP_OV1 R2728 10KOhm
R2756 follow F2S.
PM_ICH_PWROK
PMRSMRST#
D2703
BAT54C
VSUS_GD [34]
R0.4
Item 10
VRM_PWRGD_CLKEN
D2705
BAT54C
VRM_PWRGD
D2704
1N4148WS
R2759
R2750
R2751
EC_CLK_EN [34]
100KOhm
R2755
Q2704
2N7002
CLK_EN# [58]
[26] PCI_INTH#
[26] PCI_REQ#0
[26] PCI_TRDY#
[26] PCI_REQ#1
[26] PCI_INTC#
[26] PCI_FRAME#
[26] PCI_REQ#2
[26] PCI_INTG#
[26] PCI_SERR#
[26] PCI_IRDY#
[26] PCI_INTF#
[26] PCI_INTA#
[26] PCI_INTE#
[26] PCI_INTD#
[26] PCI_REQ#3
[26] PCI_STOP#
[26] PCI_DEVSEL#
[26] PCI_INTB#
[26] PCI_PERR#
[26] PCI_LOCK#
RP2700A
RP2700B
RP2700C
RP2700D
RP2700E
RP2700F
RP2700G
RP2700H
RP2701A
RP2701B
RP2701C
RP2701D
RP2701E
RP2701F
RP2701G
RP2701H
RP2702A
RP2702B
RP2702C
RP2702D
RP2702E
RP2702F
RP2702G
RP2702H
8.2K
INT_SERIRQ R2715 10KOhm
STP_PCI# R2720 10K
STP_CPU# R2723 10K
PM_CLKRUN# R2729 10KOhm
GPIO36 R2727 10KOhm
GPIO22 R2735 10KOhm
GPIO1 R2736 10KOhm
802_LED_EN R2752 10KOhm
SPKR_ICH R2737 1KOhm
+3VS
GND
<Variant Name>
Title : ICH9-M (3)
ASUSTeK COMPUTER INC
Engineer: Xinghua_chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 27 of 59



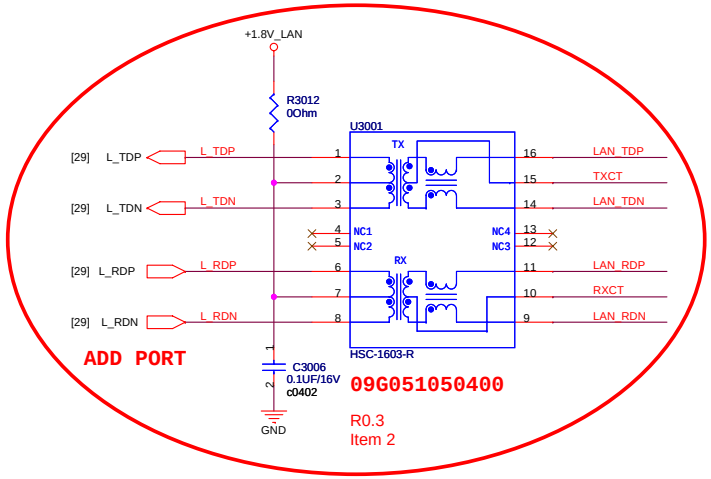
<variant_name>

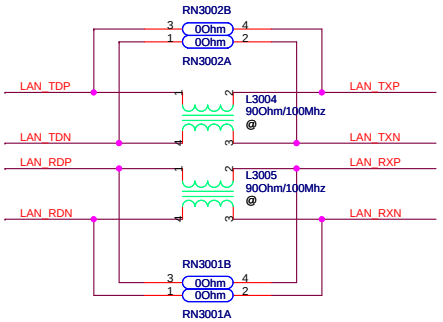
ASUSTeK COMPUTER INC	Title : ICH9-M (4)		
	Engineer: Xinghua_Chen		
Size: Custom	Project Name: P80Q		Rev: 2.00
Date: Friday, May 23, 2008	Sheet 28 of 59		

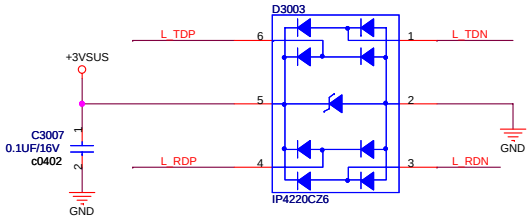
FOLLOW F9J

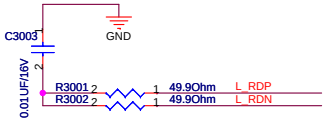


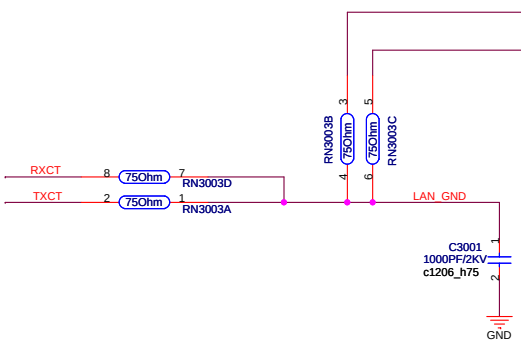
ASUSTeK COMPUTER INC	Title : LAN RTL8101E		
	Engineer: Xinghua_Chen		
Size: Custom	Project Name: F80Q		Rev: 2.00
Date: Friday, May 23, 2008	Sheet 29 of 59		



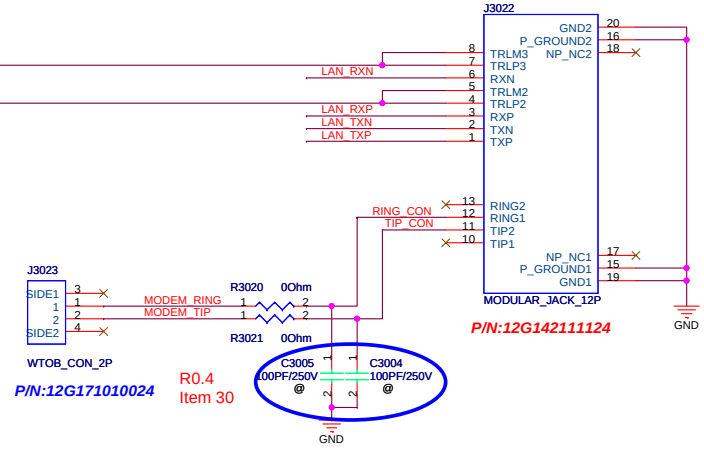








For RJ-45/RJ-11

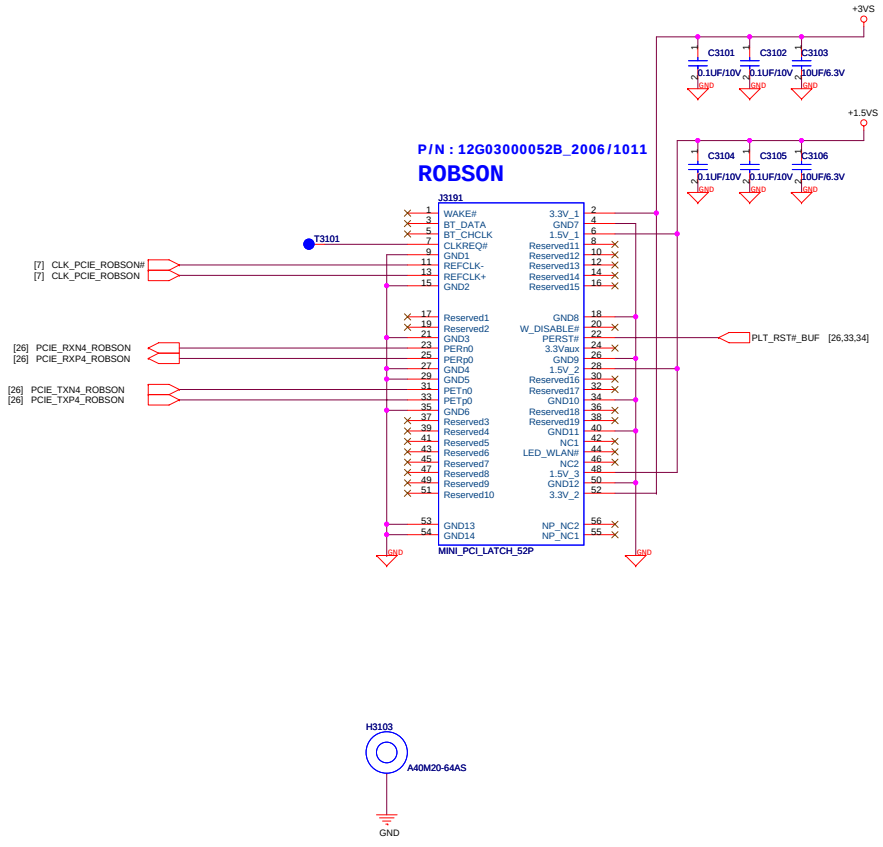


R0.4
Item 30

<Variant Name>

ASUSTeK COMPUTER INC	Title : TRANSFORMER	
	Engineer:	
Size: Custom	Project Name: F80L	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 30 of 59	

ROBSON only



<Variant Name>

ASUSTeK COMPUTER INC.

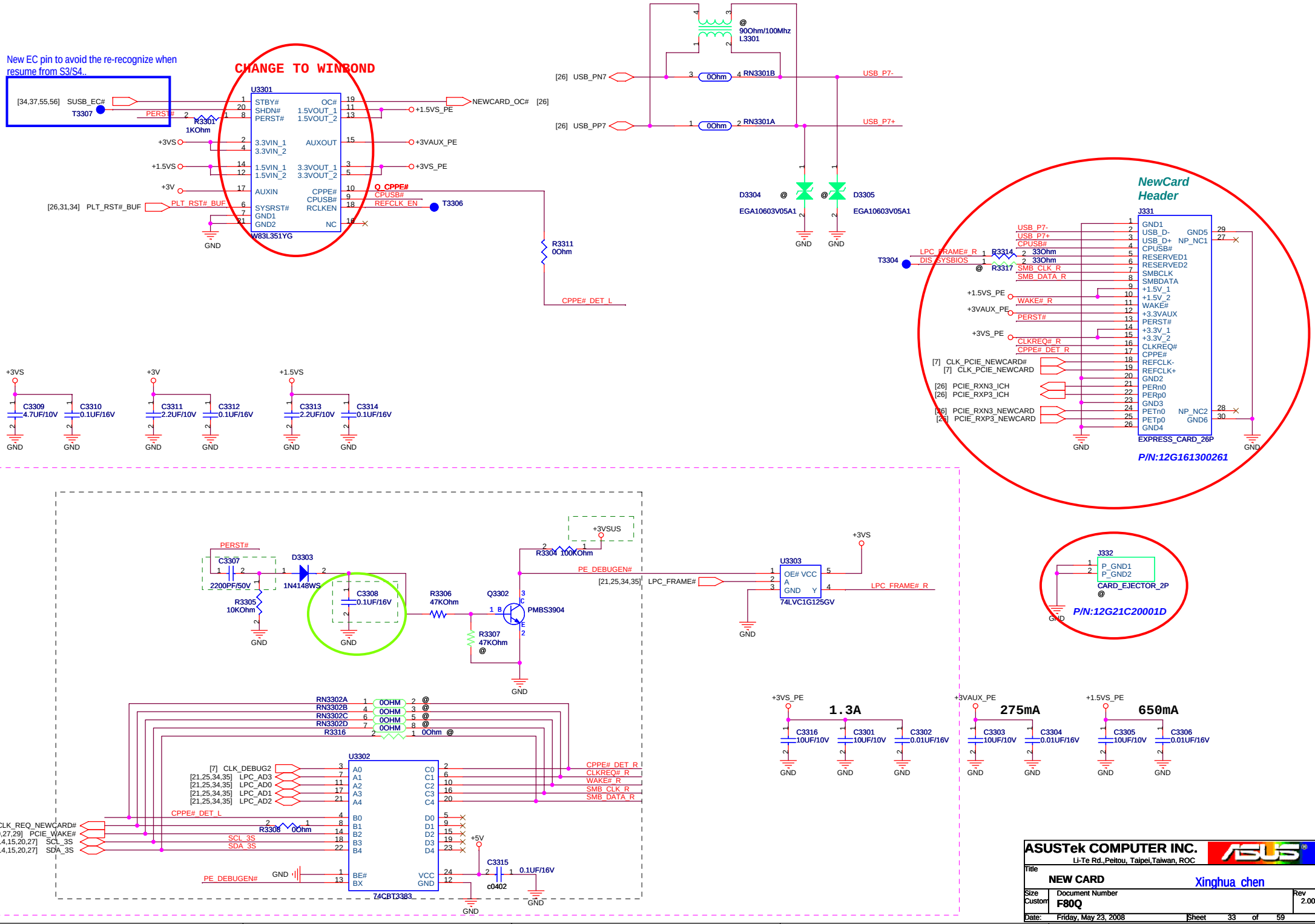
Title : ROBSON

Engineer:

Size	Project Name	Rev
C	F80L	2.00

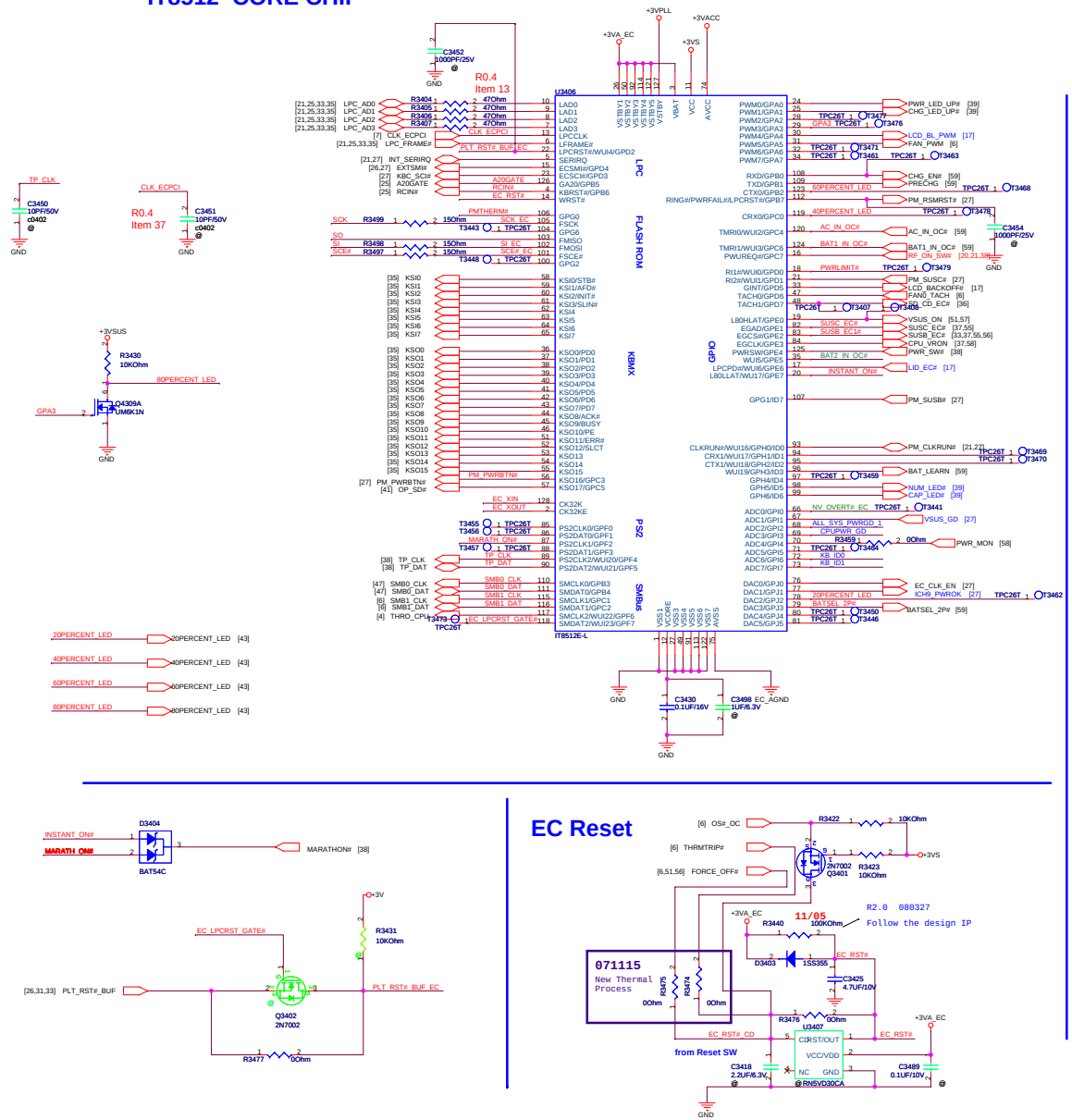
Date: Friday, May 23, 2008 Sheet 31 of 59

Title	EMPTY
Size: A	Document Number: F80L
Rev: 2.00	
Date: Friday, May 23, 2008	Sheet 32 of 59

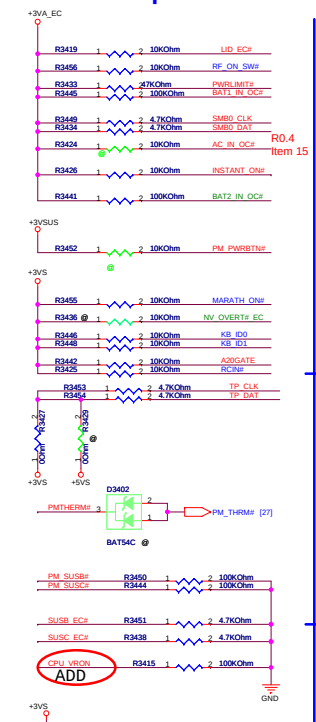


ASUSTek COMPUTER INC.			
Li-Te Rd.,Peitou, Taipei,Taiwan, ROC			
Title: NEW CARD		Xinghua_chen	
Size: Custom	Document Number: F80Q		Rev: 2.00
Date: Friday, May 23, 2008	Sheet 33 of 59		

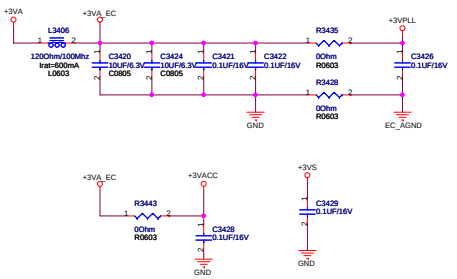
IT8512 CORE CHIP



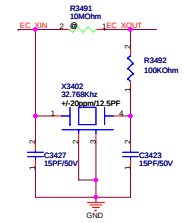
EC Pull-Up/Down



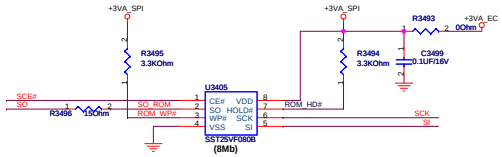
EC Power



EC XTAL



SPI ROM



EC Reset

<Variant Name>

ASUSTeK COMPUTER INC

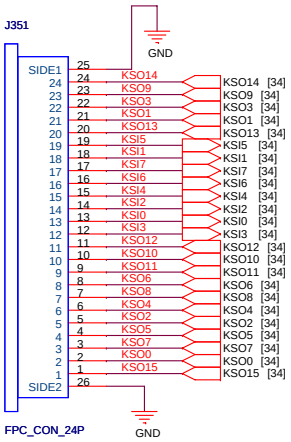
Title : EC-ITE8512

Engineer: Xinghua_Chen

Size	Project Name	Rev
Custom	F80Q	2.00

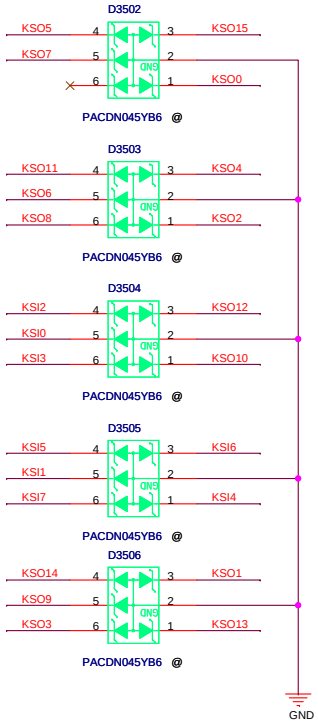
Date: Friday, May 23, 2008 Sheet 34 of 59

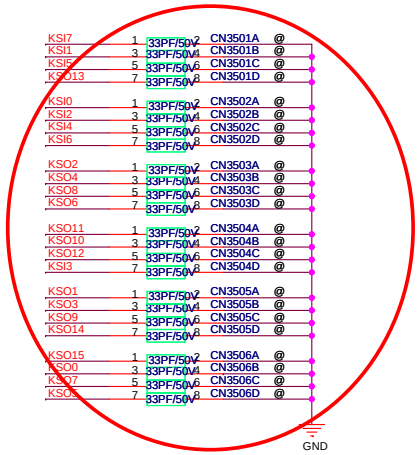
For Keyboard



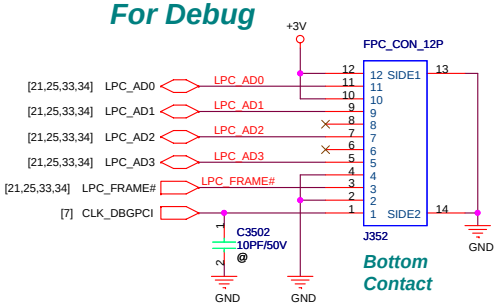
P/N:12G182002408

T53 KB MATRIX





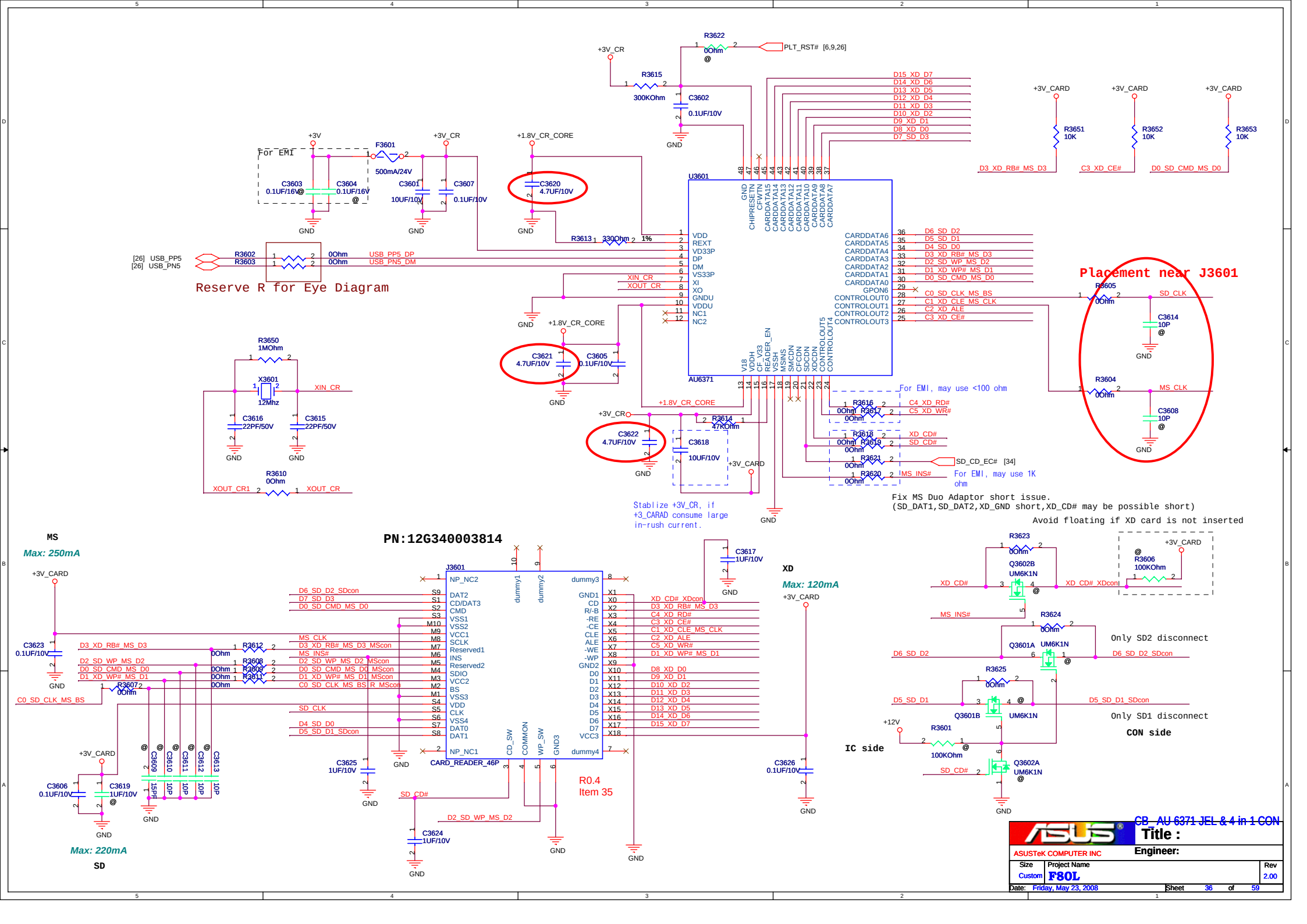
For Debug

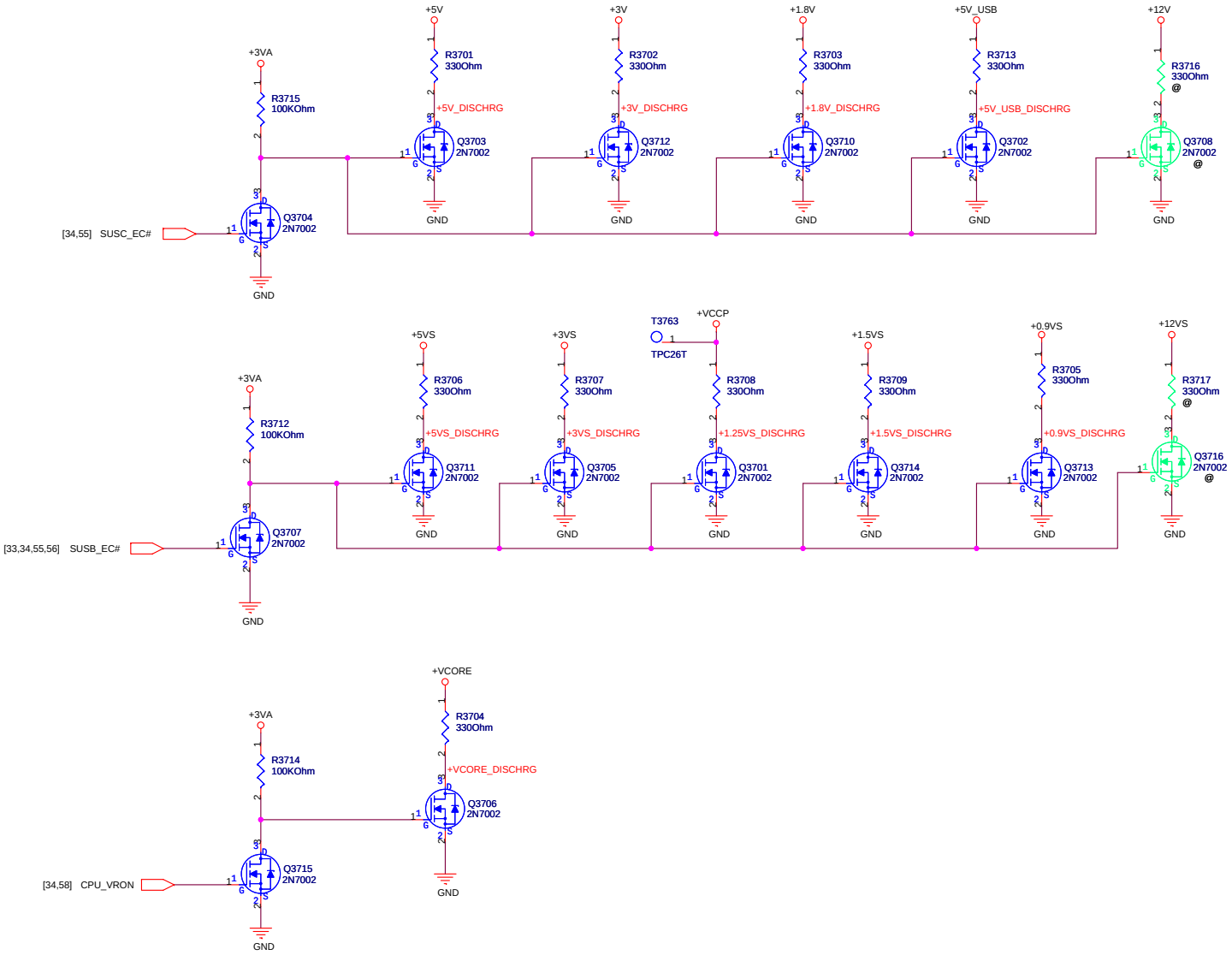


Bottom Contact

<Variant Name>

ASUSTeK COMPUTER INC	Title : KB conn	
	Engineer: CH Lin	
Size: Custom	Project Name: F80L	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 35 of 59	


PN:12G340003814
Reserve R for Eye Diagram
Placement near J3601
Stablize +3V_CR, if +3_CARAD consume large in-rush current.
Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)
Avoid floating if XD card is not inserted
MS
Max: 250mA
SD
Max: 220mA
XD
Max: 120mA
IC side
CON side
Only SD2 disconnect
Only SD1 disconnect
R0.4
Item 35
U3601
AU6371
J3601
CARD_READER_46P
ASUSTeK COMPUTER INC
Title : CB_AU 6371 JEL & 4 in 1 CON
Engineer:
Size Custom
Project Name F80L
Rev 2.00
Date: Friday, May 23, 2008
Sheet 36 of 59



<Variant Name>

ASUSTeK COMPUTER INC

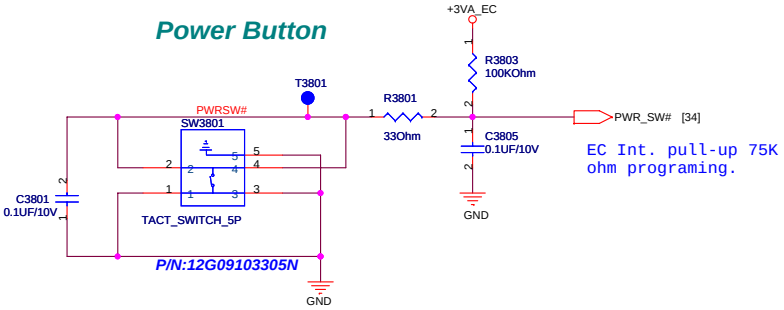
Title : DISCHARGE

Engineer: CH Lin

Size	Project Name	Rev
Custom	F80L	2.00

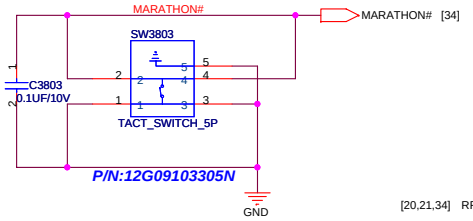
Date: Friday, May 23, 2008 Sheet 37 of 59

Power Button

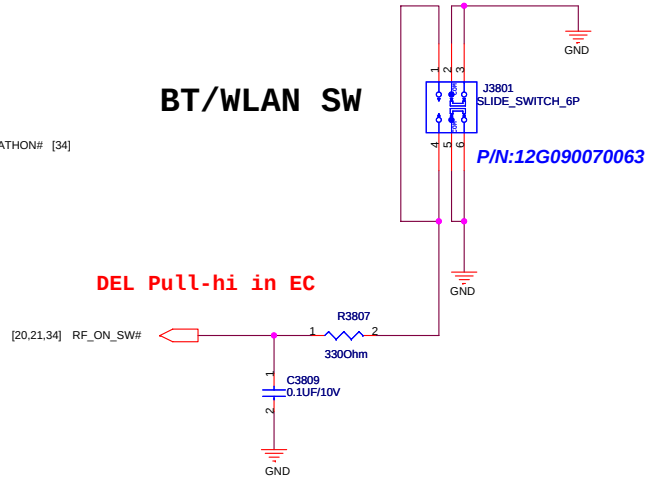


EC Int. pull-up 75K ohm programing.

MARATHON#



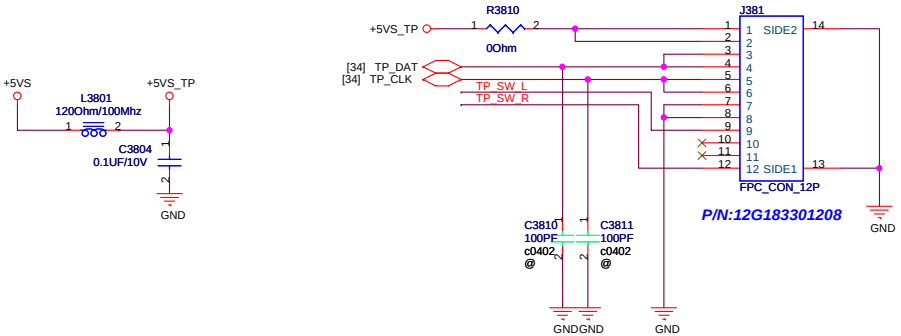
BT/WLAN SW

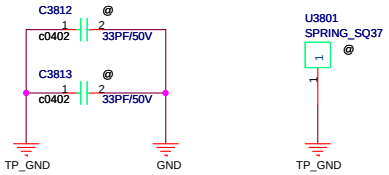


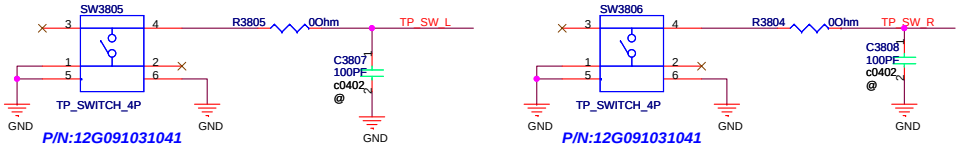
Touch-Pad

TOUCH PAD CNT Follow W7

R0.4
Item 28



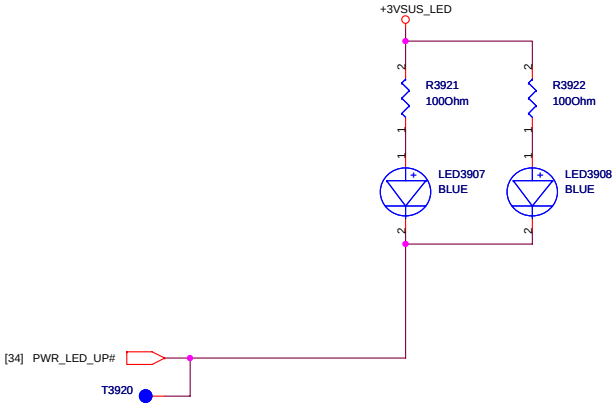




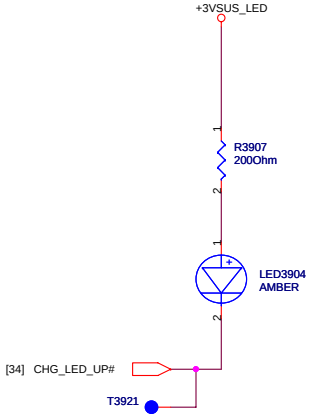
<Variant Name>

ASUSTeK COMPUTER INC	Title : KEY & LED	
	Engineer: Xighua_chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 38 of 59	

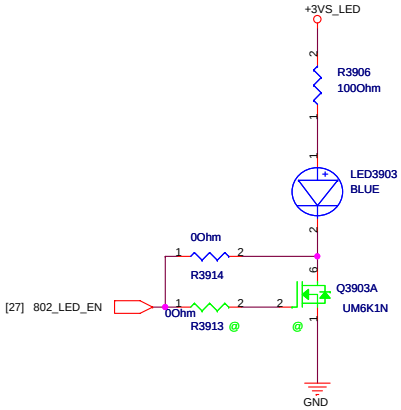
PWR LED



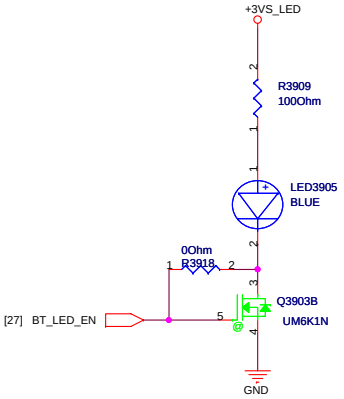
For BATTERY LED



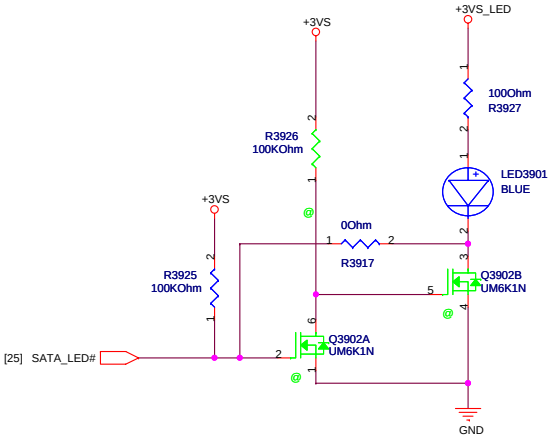
WireLess LED



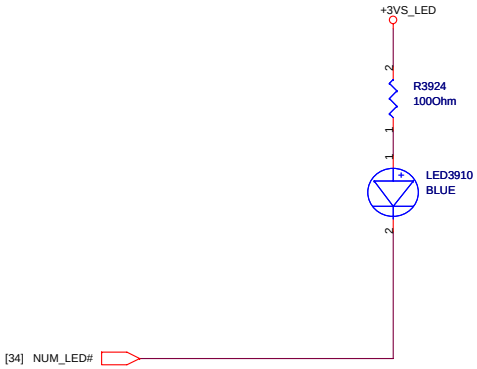
BT LED



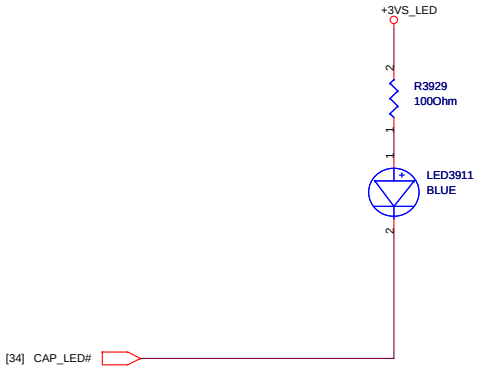
SATA/IDE LED



Num Lock



Cap. Lock



<Variant Name>

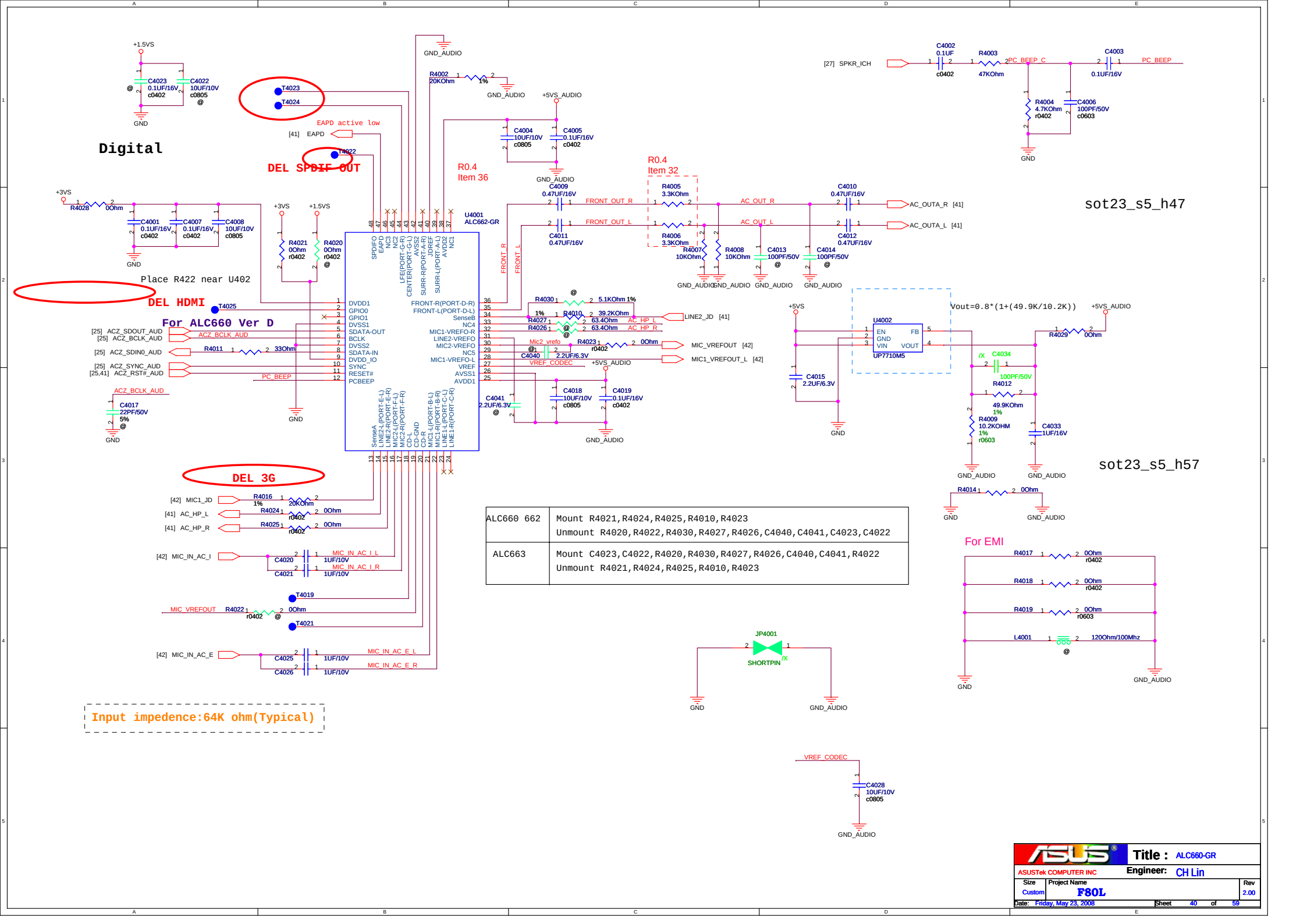
Title : LEDs

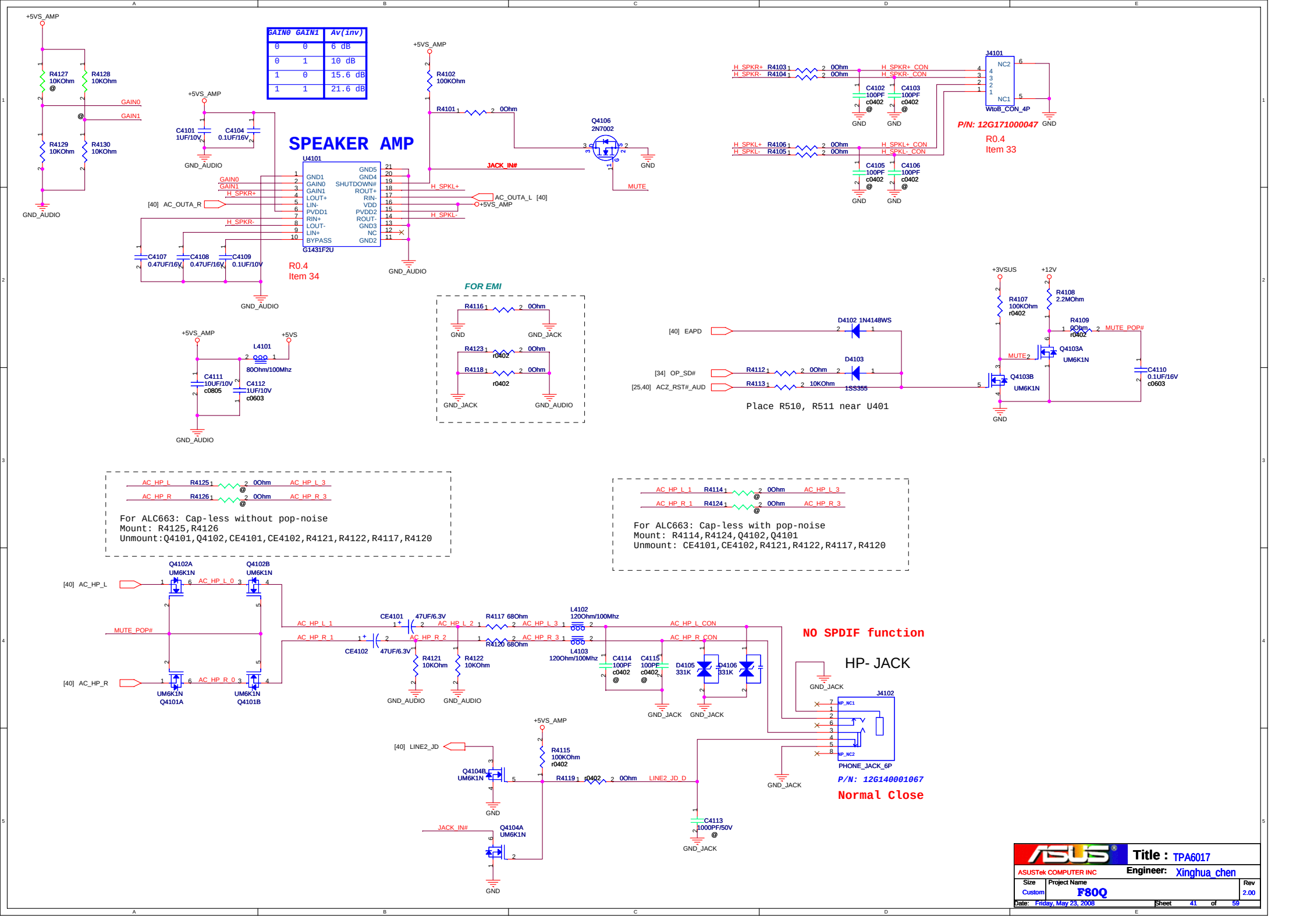
ASUSTeK COMPUTER INC

Engineer: Xinghua_Chen

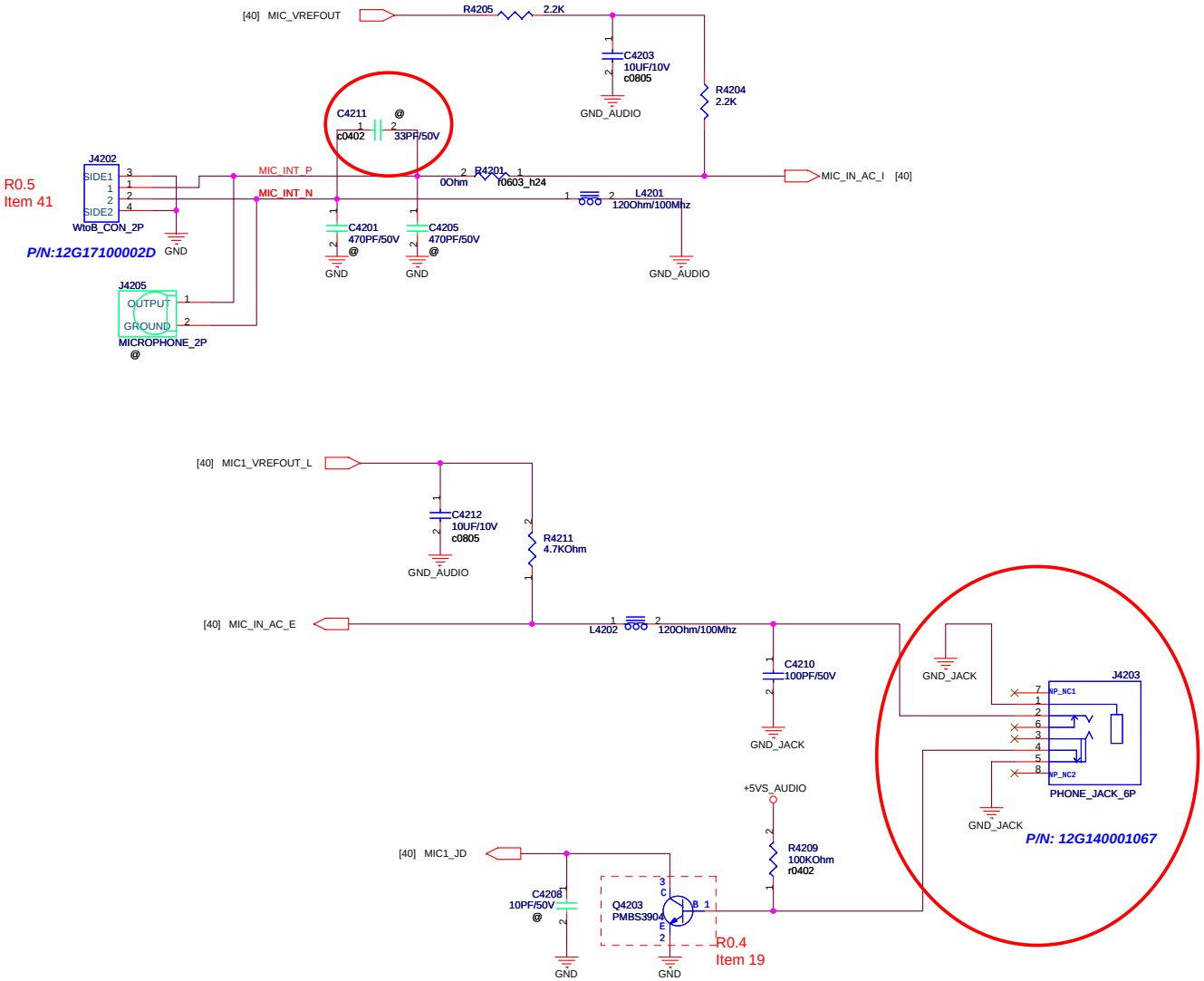
Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 39 of 59


Digital
DEL SPDIF OUT
EAPD active low
[41] EAPD
R0.4
Item 36
R0.4
Item 32
sot23_s5_h47
sot23_s5_h57
Place R422 near U402
DEL HDMI
For ALC660 Ver D
DEL 3G
U4001
ALC662-GR
U4002
UP7710M5
Vout=0.8*(1+(49.9K/10.2K))
[27] SPKR_ICH
PC_BEEP_C
PC_BEEP
AC_OUTA_R [41]
AC_OUTA_L [41]
LINE2_JD [41]
MIC_VREFOUT [42]
MIC1_VREFOUT_L [42]
[42] MIC1_JD
[41] AC_HP_L
[41] AC_HP_R
[42] MIC_IN_AC_I
[42] MIC_IN_AC_E
[25] ACZ_SDOUT_AUD
[25] ACZ_BCLK_AUD
[25] ACZ_SDIN0_AUD
[25] ACZ_SYNC_AUD
[25,41] ACZ_RST#_AUD
Input impedence:64K ohm(Typical)
For EMI
JP4001
SHORTPIN
VREF_CODEC
ALC660 662
Mount R4021,R4024,R4025,R4010,R4023
Unmount R4020,R4022,R4030,R4027,R4026,C4040,C4041,C4023,C4022
ALC663
Mount C4023,C4022,R4020,R4030,R4027,R4026,C4040,C4041,R4022
Unmount R4021,R4024,R4025,R4010,R4023
Title : ALC660-GR
ASUSTek COMPUTER INC
Engineer: CH Lin
Size: Custom
Project Name: F80L
Rev: 2.00
Date: Friday, May 23, 2008
Sheet 40 of 59

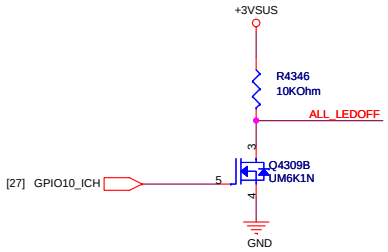

GAIN0 GAIN1 Av(inv)
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
SPEAKER AMP
U4101
G1431F2U
R0.4
Item 34
FOR EMI
Place R510, R511 near U401
P/N: 12G171000047
R0.4
Item 33
For ALC663: Cap-less without pop-noise
Mount: R4125,R4126
Unmount:Q4101,Q4102,CE4101,CE4102,R4121,R4122,R4117,R4120
For ALC663: Cap-less with pop-noise
Mount: R4114,R4124,Q4102,Q4101
Unmount: CE4101,CE4102,R4121,R4122,R4117,R4120
NO SPDIF function
HP- JACK
P/N: 12G140001067
Normal Close
Title : TPA6017
ASUSTek COMPUTER INC
Engineer: Xinghua_chen
Size Custom
Project Name F80Q
Rev 2.00
Date: Friday, May 23, 2008
Sheet 41 of 59

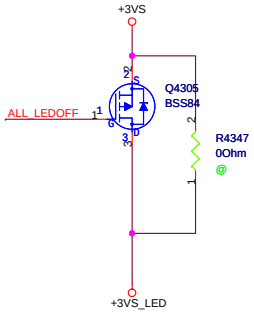
Internal MIC Pre-Amplifier

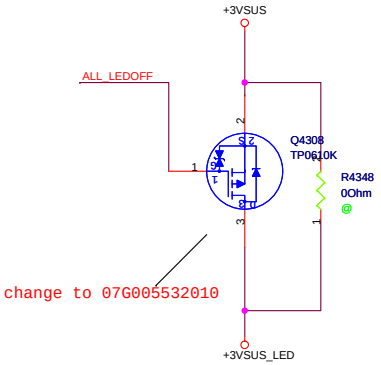


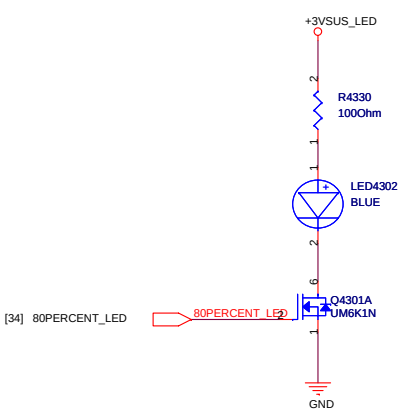
<Variant Name>

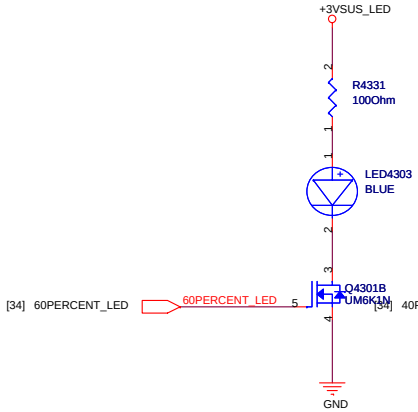
ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: Xinghua_Chen	
Size: Custom	Project Name: F80Q	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 42 of 59	

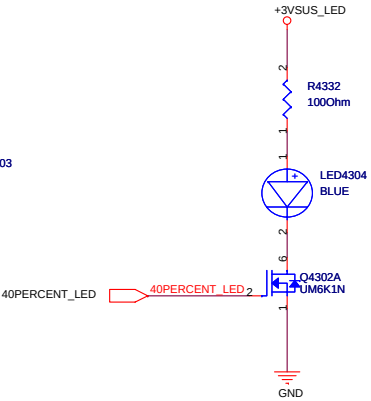


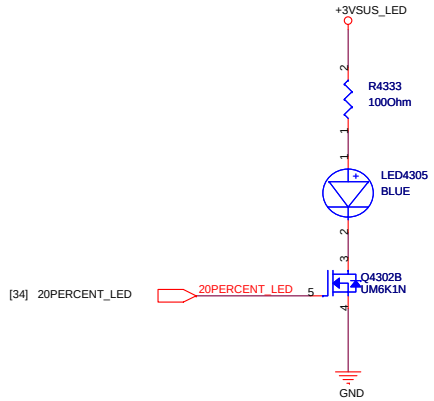


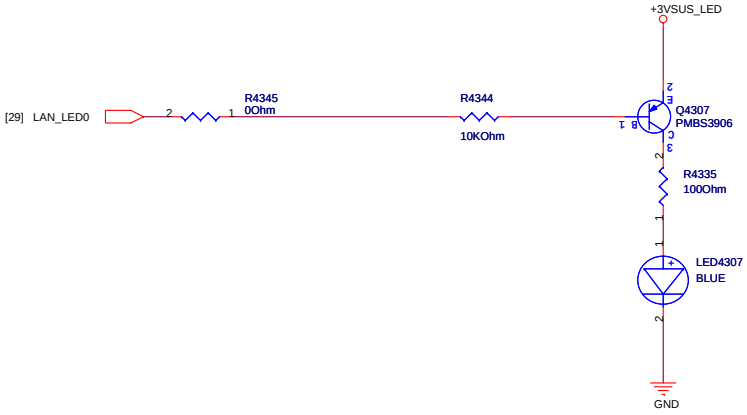












add LED1,LED2,LED3 test points

<Variant Name>

Title : BATTERY&LAN LED

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F80Q	2.00

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<Variant Name>

Title : empty

ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F80Q	2.00

Date: Friday, May 23, 2008 Sheet 44 of 59

<Variant Name>

Title : EMPTY

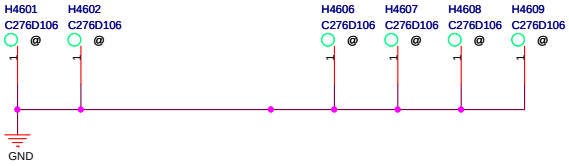
ASUSTeK COMPUTER INC

Engineer:

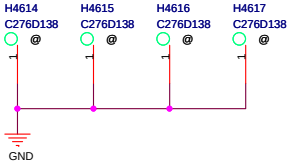
Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 45 of 59

A



B



C

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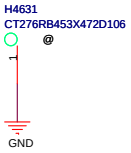
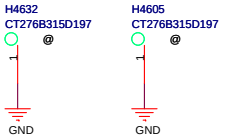
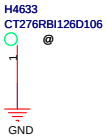


J

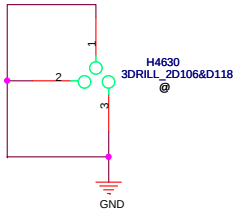


K

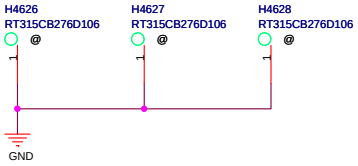


E

H



G



<Variant Name>

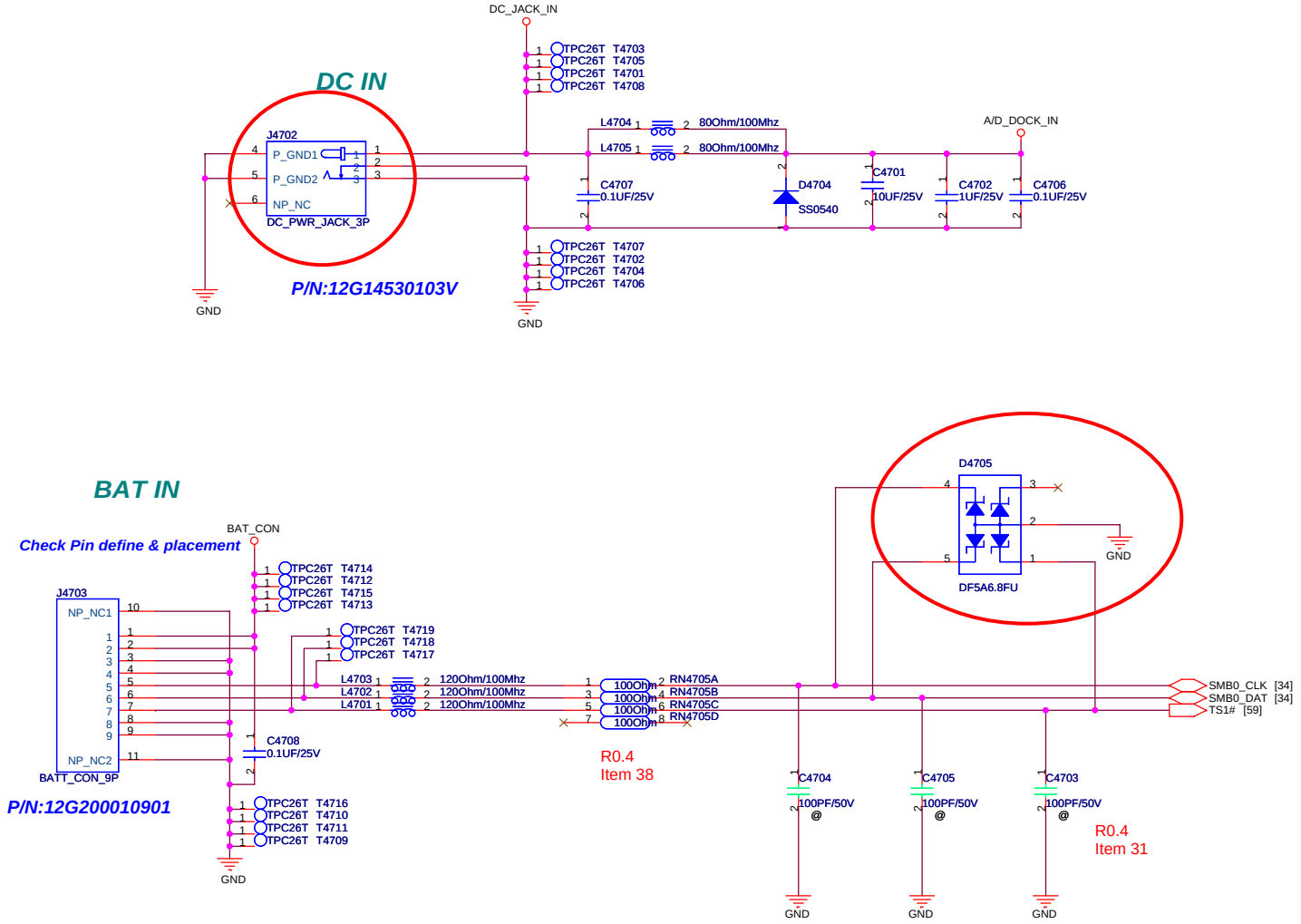
ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: CH Lin

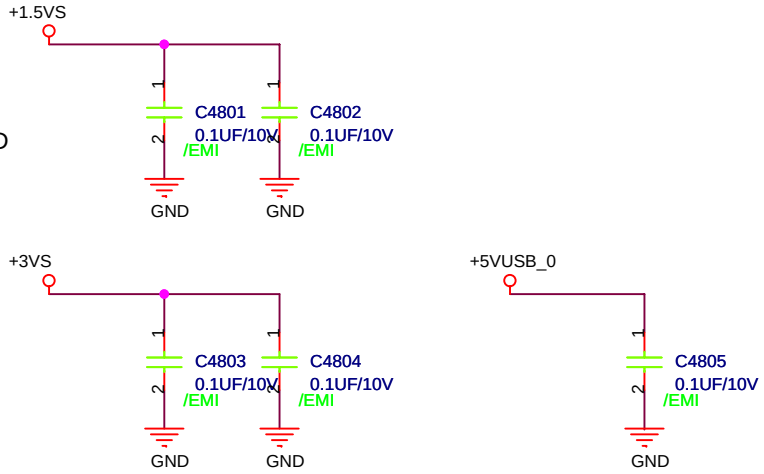
Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 46 of 59



<Variant Name>

ASUSTeK COMPUTER INC	Title : DC & BAT IN	
	Engineer: CH Lin	
Size: Custom	Project Name: F80L	Rev: 2.00
Date: Friday, May 23, 2008	Sheet 47 of 59	



Title :	EMI
<OrgName>	Engineer: Xinghua_Chen
Size: A4	Project Name: F80Q
Rev: <RevC	
Date: Friday, May 23, 2008	Sheet 48 of 59

<Variant Name>

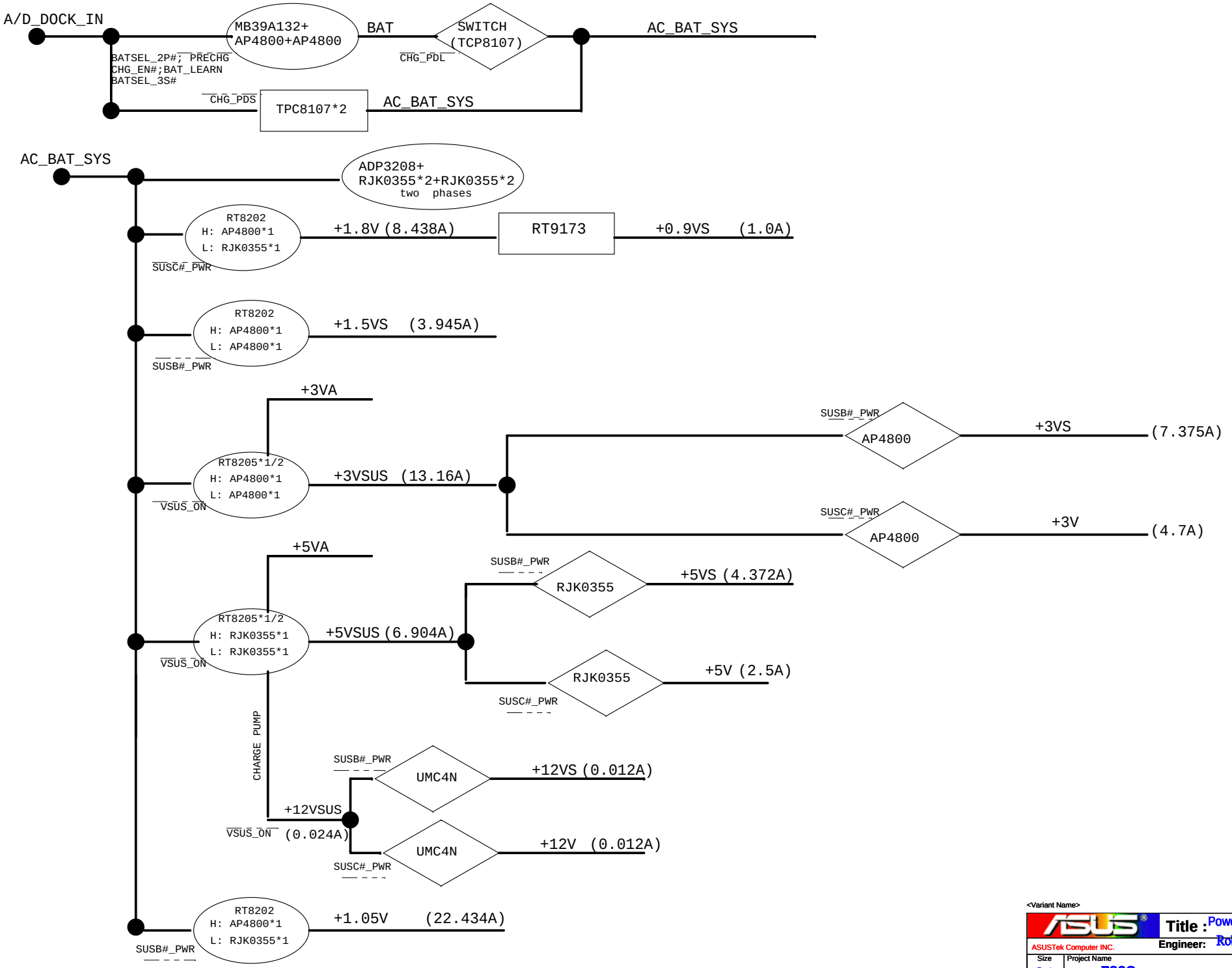
Title : History(2)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F80L	2.00

Date: Friday, May 23, 2008 Sheet 49 of 59



<Variant Name>

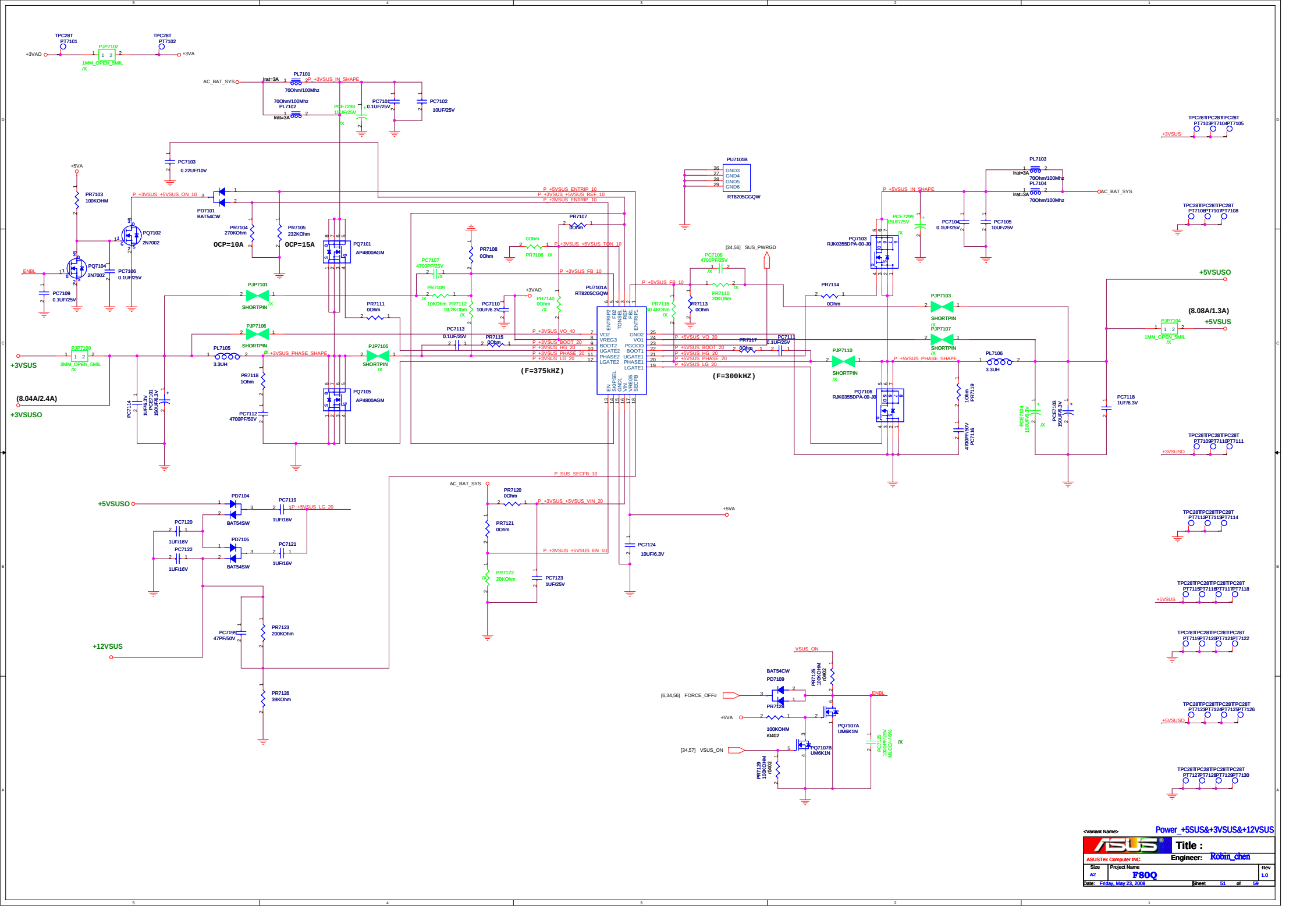
ASUSTek Computer INC.

Title : Power_Flow

Engineer: Robin_chen

Size	Project Name	Rev
Custom	F80Q	1.0

Date: Friday, May 23, 2008 Sheet 50 of 59



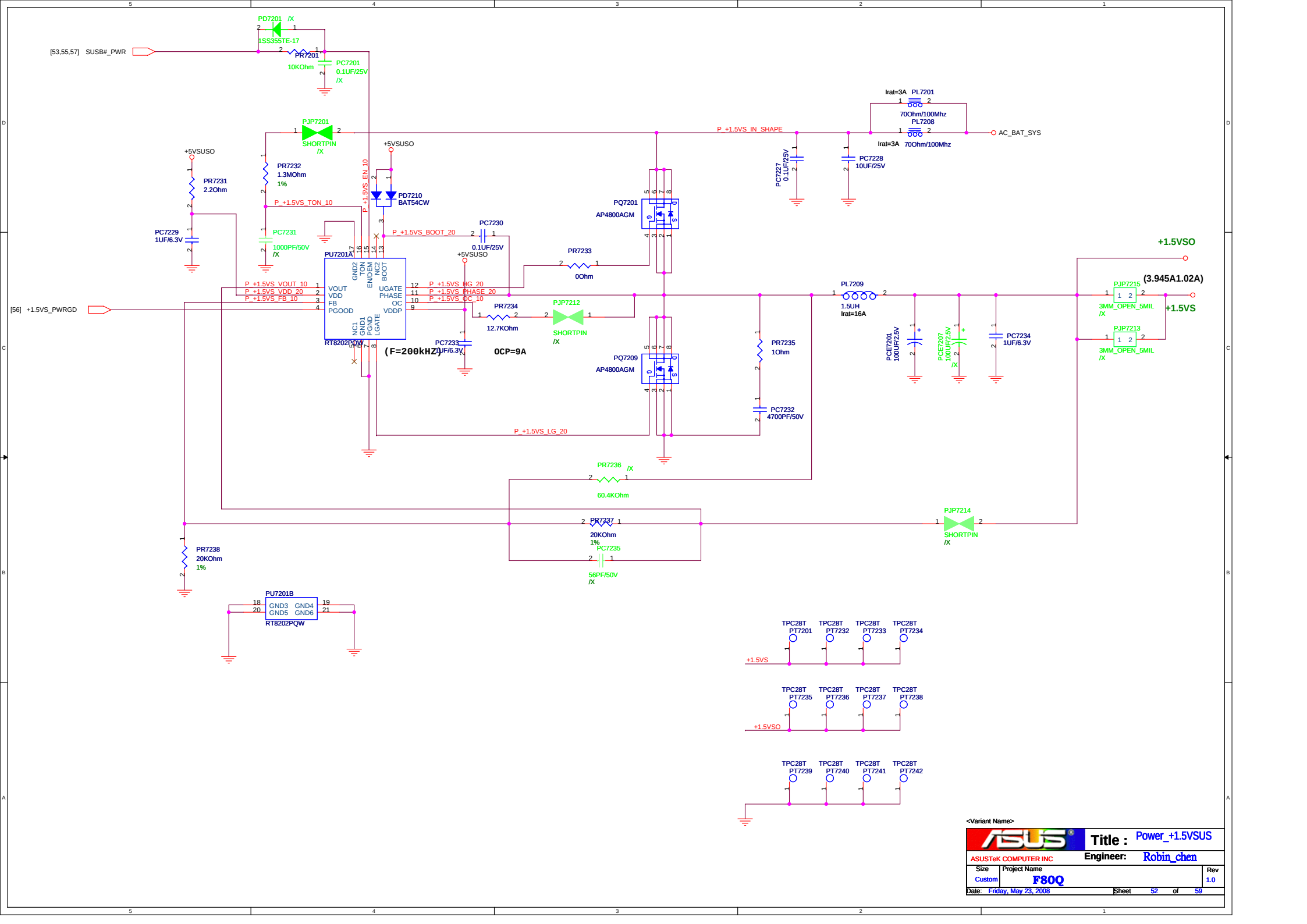
<Variant Name> Power_+5SUS&+3VSUS&+12VSUS

Title :

ASUSTek Computer INC. Engineer: Robin_chen

Size: A2 | Project Name: F80Q | Rev: 1.0

Date: Friday, May 23, 2008 | Sheet 51 of 59



<Variant Name>

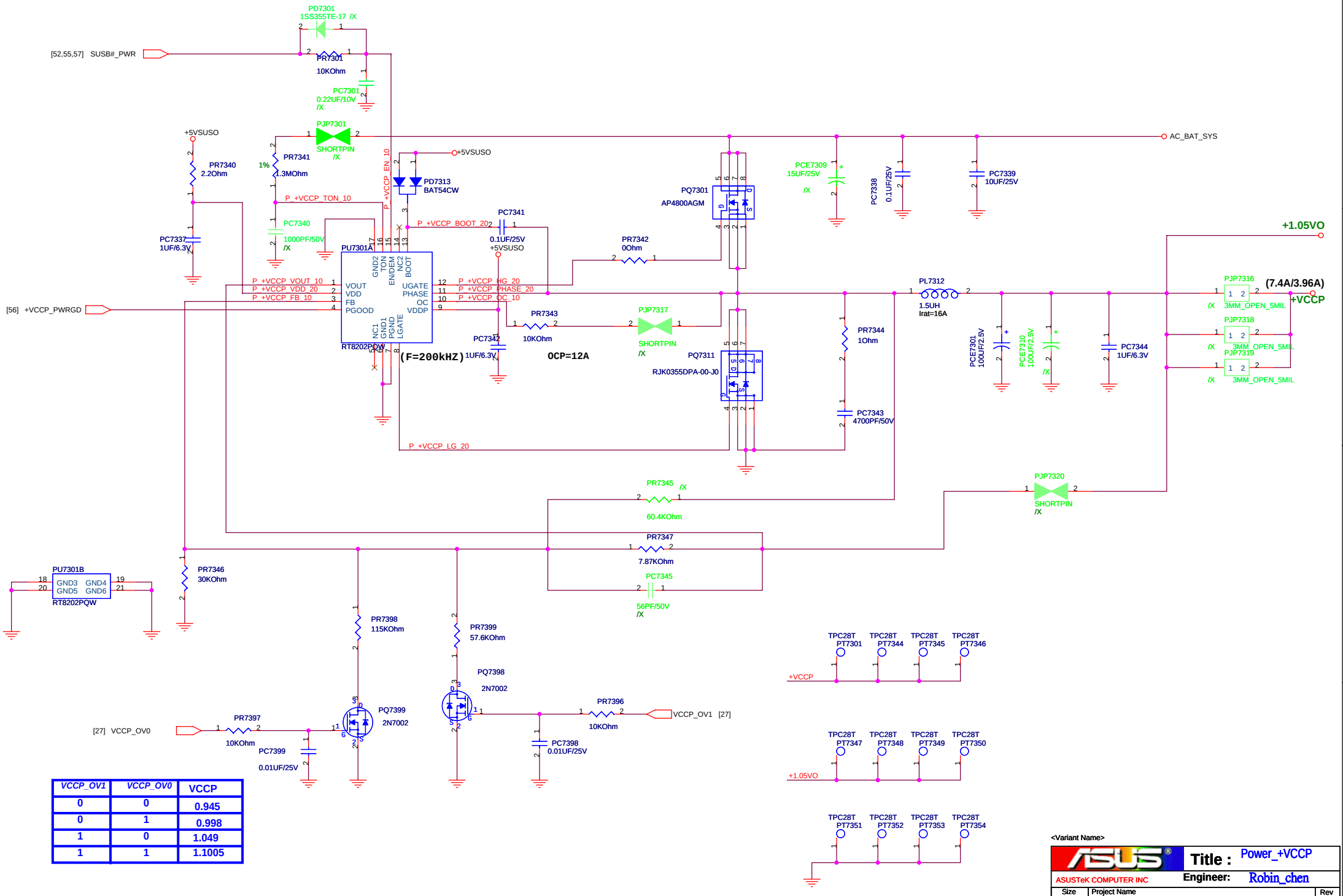
ASUSTeK COMPUTER INC

Title : Power_+1.5VSUS

Engineer: Robin_chen

Size	Project Name	Rev
Custom	F80Q	1.0

Date: Friday, May 23, 2008 Sheet 52 of 59



VCCP_OV1	VCCP_OV0	VCCP
0	0	0.945
0	1	0.998
1	0	1.049
1	1	1.1005

<Variant Name>

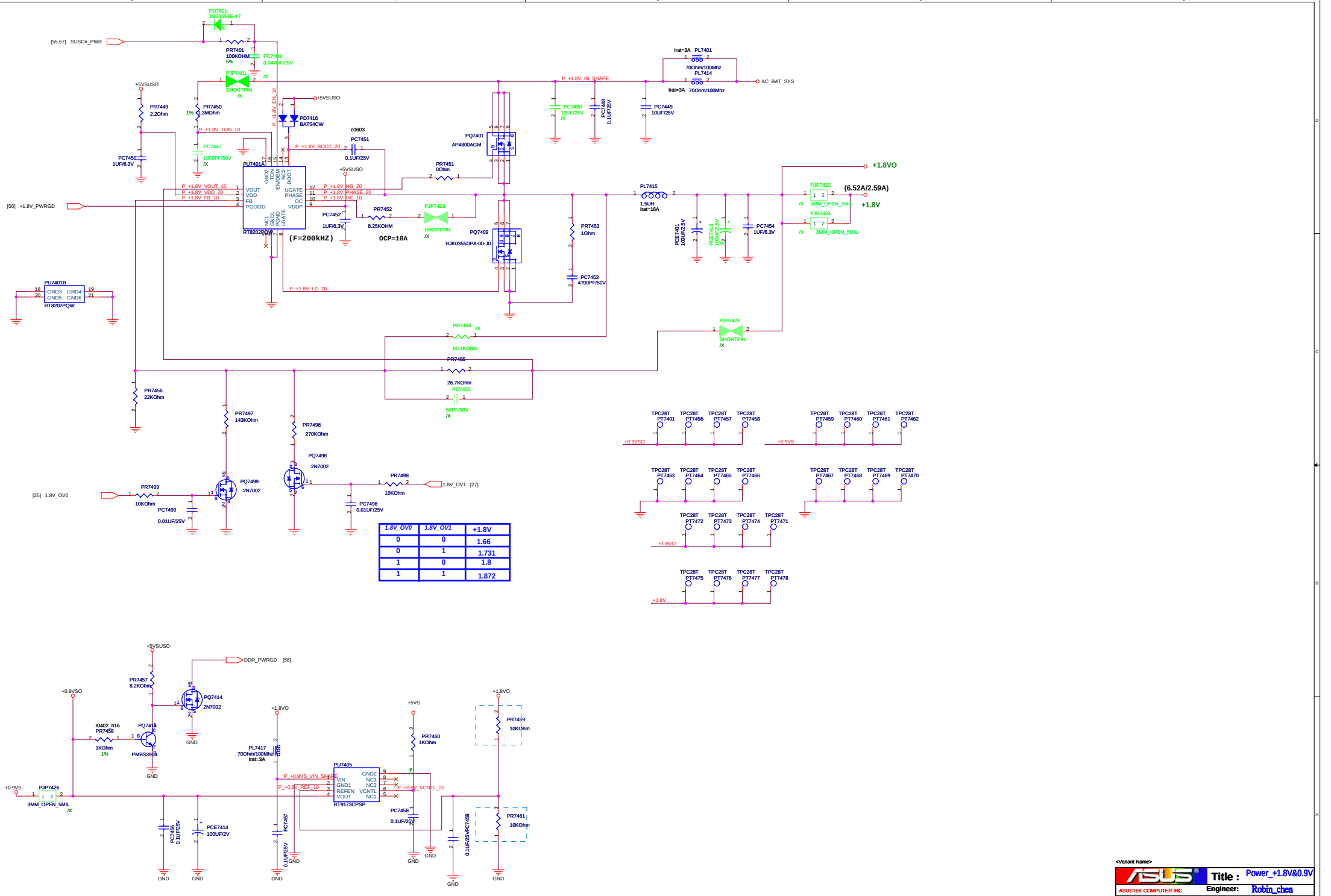
ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer: Robin_chen

Size	Project Name	Rev
A3	F80Q	1.0

Date: Friday, May 23, 2008 Sheet 53 of 59



1.8V_OV0	1.8V_OV1	+1.8V
0	0	1.66
0	1	1.731
1	0	1.8
1	1	1.872

<Variant Name>

ASUSTeK COMPUTER INC

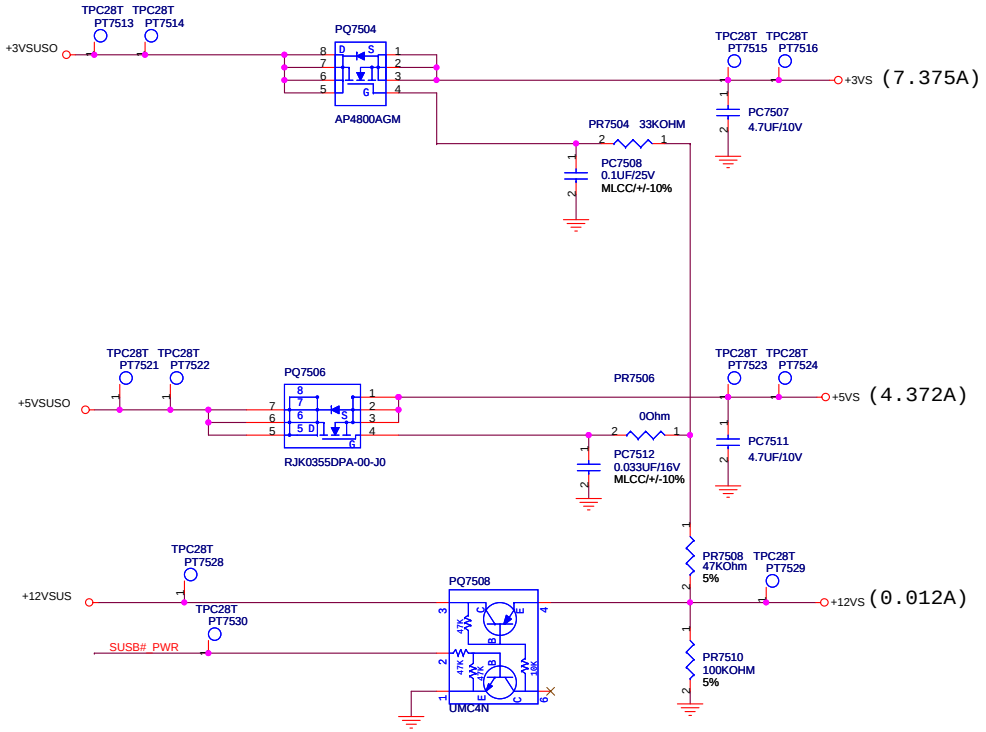
Title : Power_+1.8V&0.9V

Engineer: Robin_chen

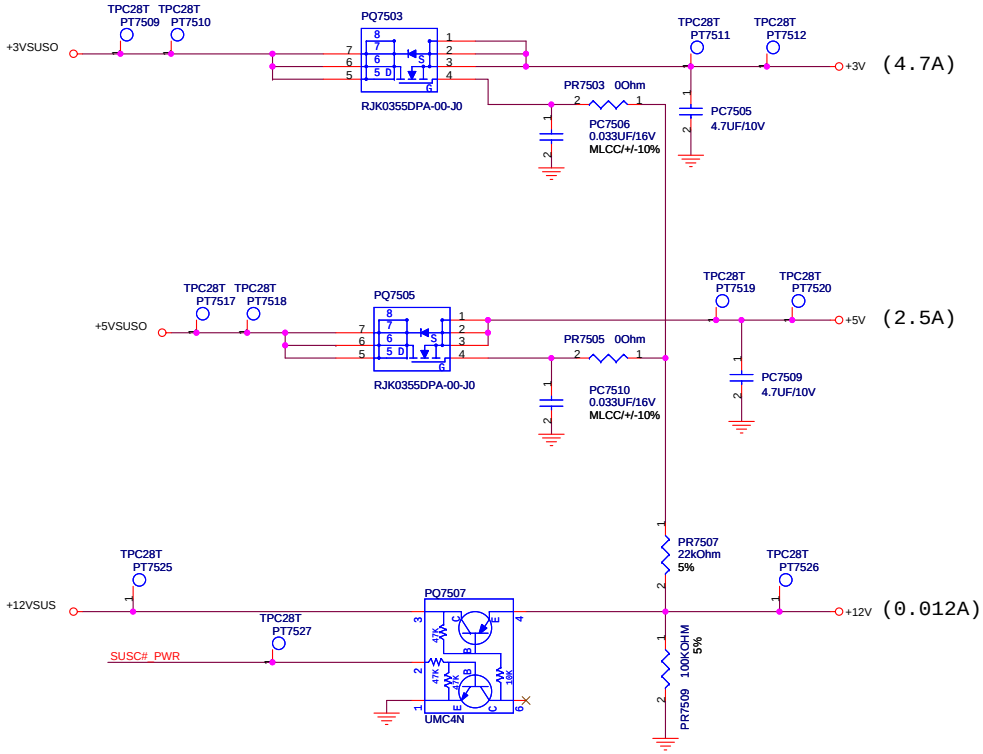
Size	Project Name	Rev
A2	F80Q	1.0

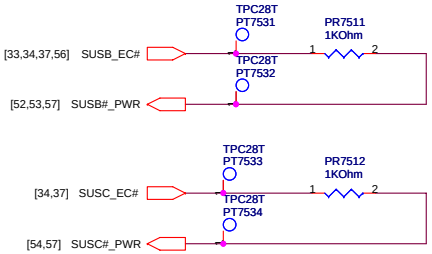
Date: Friday, May 23, 2008 Sheet 54 of 59

SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

ASUSTeK COMPUTER INC

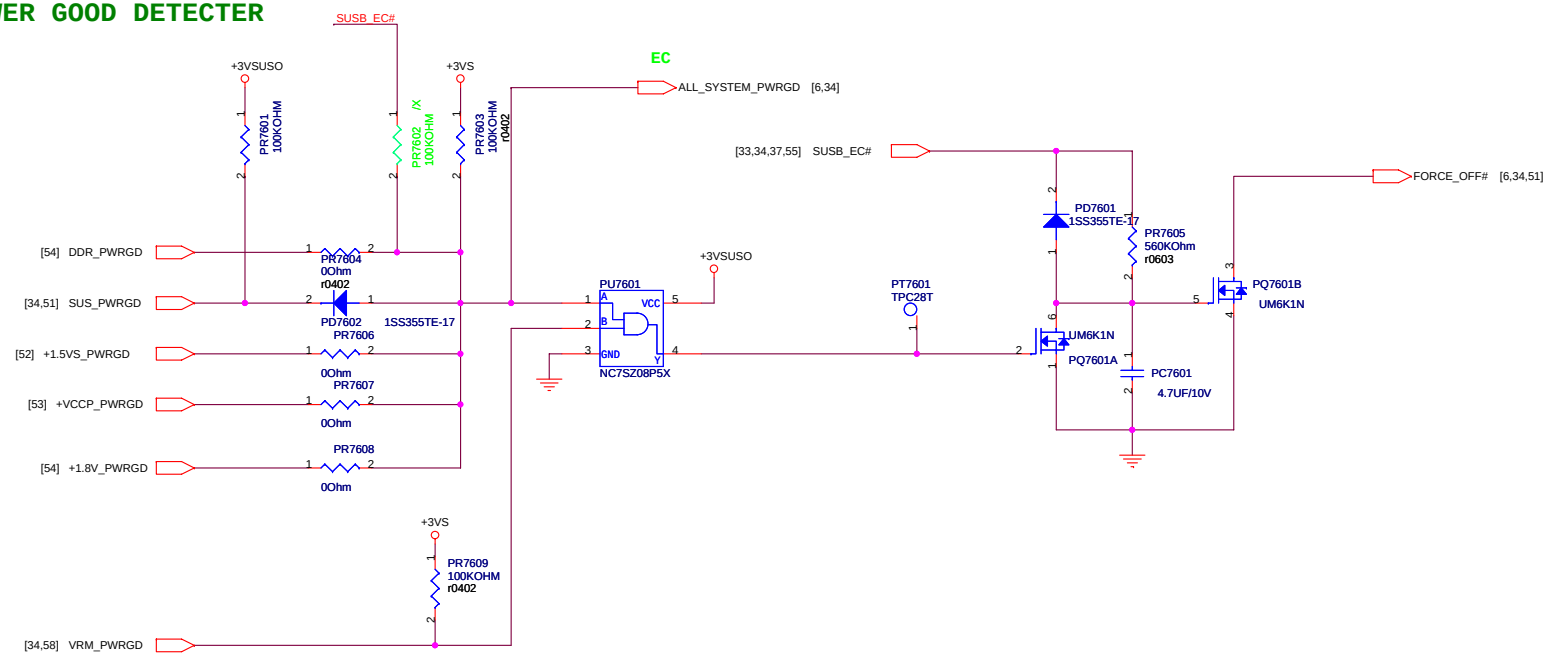
Title : Power_Load_Switch

Engineer: Robin_chen

Size	Project Name	Rev
Custom	F80Q	1.0

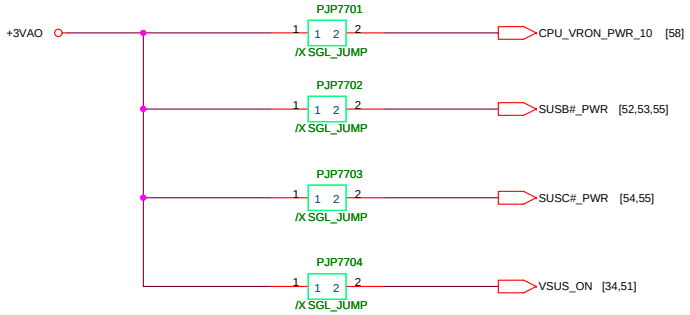
Date: Friday, May 23, 2008 Sheet 55 of 59

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_good_detecter	
	Engineer: Robin_chen	
Size: Custom	Project Name: F80Q	Rev: 1.0
Date: Friday, May 23, 2008	Sheet 56 of 59	



<Variant Name>

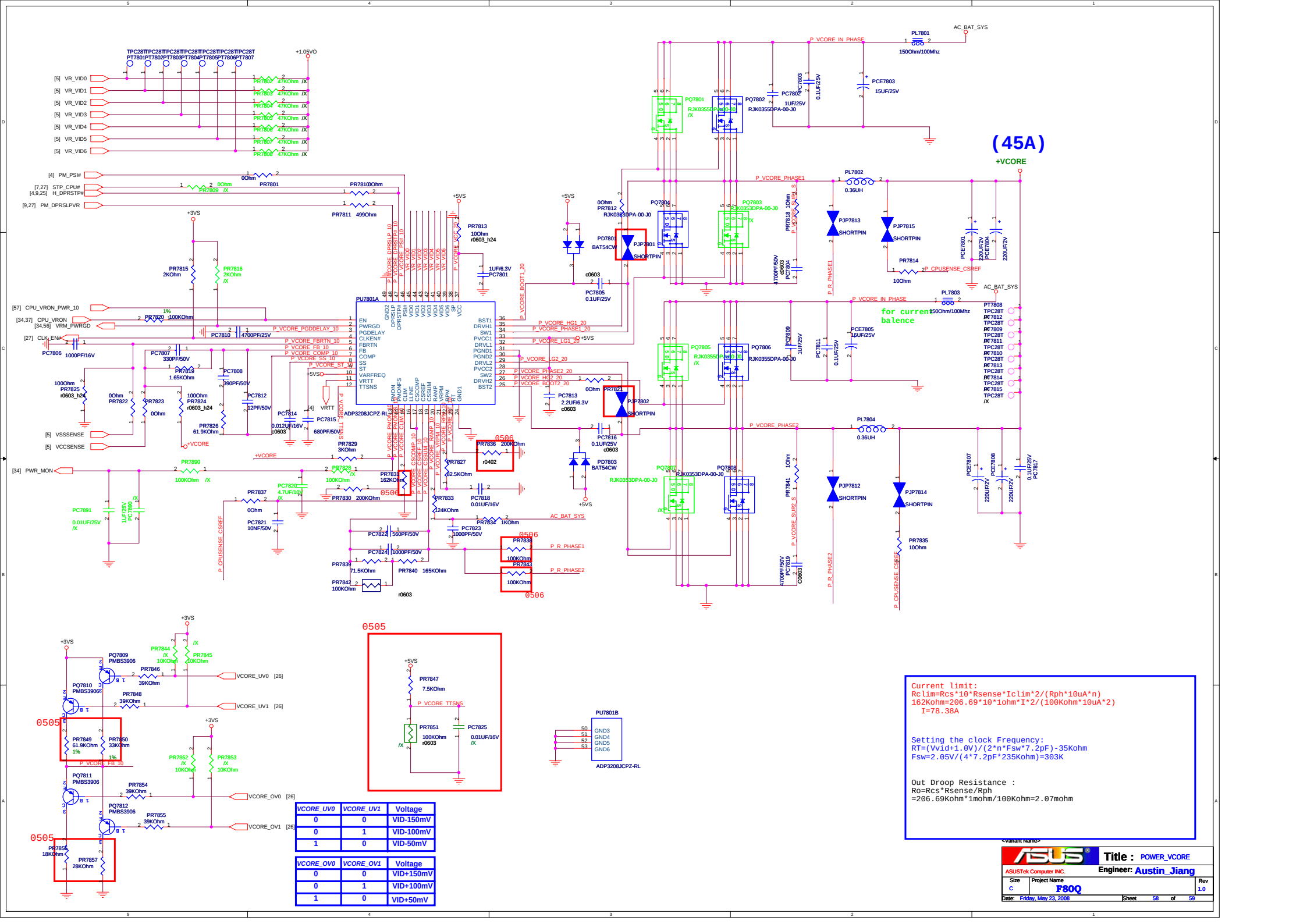
ASUSTeK COMPUTER INC

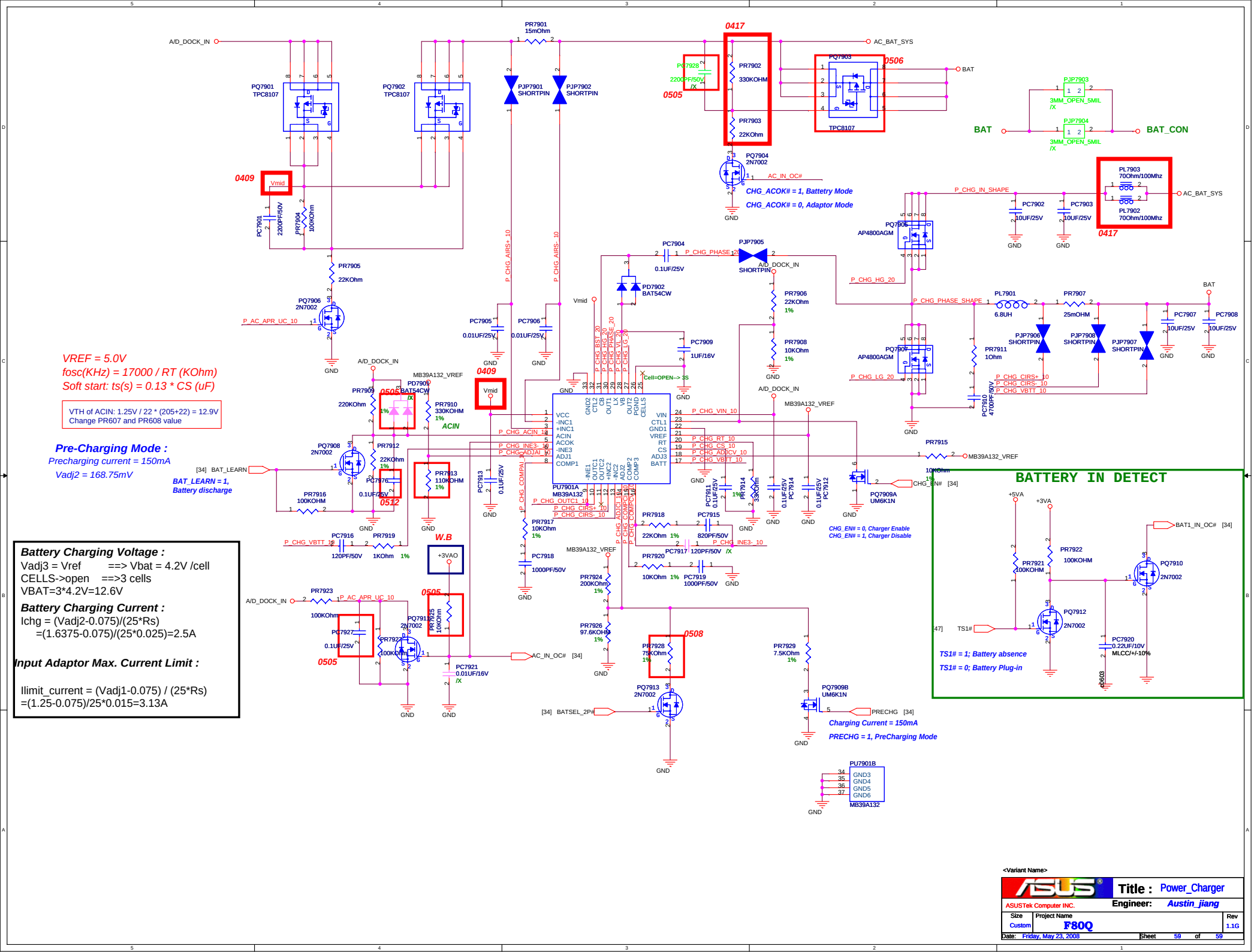
Title : Power_for_test

Engineer: Robin_chen

Size	Project Name	Rev
Custom	F80Q	1.0

Date: Friday, May 23, 2008 Sheet 57 of 59


(45A)
+VCORE
for current balence
Current limit:
Rclim=Rcs*10*Rsense*Iclim*2/(Rph*10uA*n)
162Kohm=206.69*10*1ohm*I*2/(100Kohm*10uA*2)
I=78.38A
Setting the clock Frequency:
RT=(Vvid+1.0V)/(2*n*Fsw*7.2pF)-35Kohm
Fsw=2.05V/(4*7.2pF*235Kohm)=303K
Out Droop Resistance :
Ro=Rcs*Rsense/Rph
=206.69Kohm*1mohm/100Kohm=2.07mohm
VCORE_UV0 VCORE_UV1 Voltage
0 0 VID-150mV
0 1 VID-100mV
1 0 VID-50mV
VCORE_OV0 VCORE_OV1 Voltage
0 0 VID+150mV
0 1 VID+100mV
1 0 VID+50mV
Title : POWER_VCORE
ASUSTek Computer INC.
Engineer: Austin_Jiang
Size C
Project Name F80Q
Rev 1.0
Date: Friday, May 23, 2008
Sheet 58 of 59



<Variant Name>			
ASUSTek Computer INC.	Title : Power_Charger		
	Engineer: Austin_jiang		
Size: Custom	Project Name: F80Q		Rev: 1.1G
Date: Friday, May 23, 2008	Sheet 59 of 59		