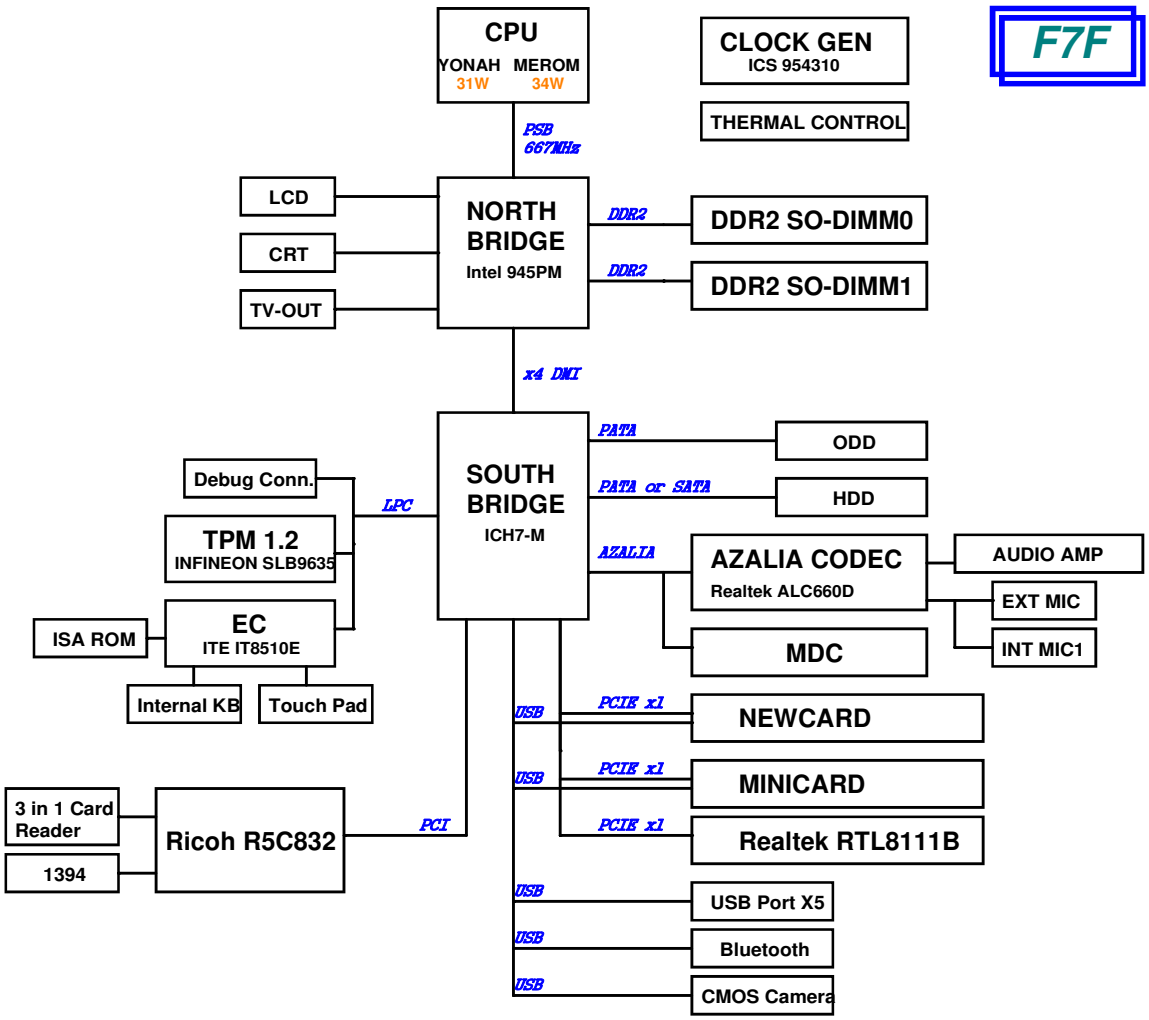


ASUSTek Computer INC. NB1

Title : Block Diagram

Engineer: Frank Wang

Size	Project Name	Rev
Custom	F7F	2.0

Date: 星期 二, 十月 15, 2007 Sheet 1 of 89

<< Kennedy_Zhang >>

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	/	
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	/	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	BT_ON#	O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	
115	PS2DAT1/GPF3	/	
116	PS2CLK2/GPF4	TP_CLK	I/0
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	/	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BTLED_ON	O
AC18	GPIO07	WLAN_LED_EN	O
E21	GPIO08	EXTSMI#	I
E20	GPIO09	/	
A20	GPIO10	WLAN_ON#	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	CB_SD#	O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	TP_LEDON	O
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	CPU_SELECT	O
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	/	
R3	GPIO24	/	
D20	GPIO25	/	
A21	GPIO26/EL_RSVD	/	
B21	GPIO27/EL_STATE0	BT_DET#	
E23	GPIO28/EL_STATE1	/	
C3	GPIO29/OC#5	USB_OC#5	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC#7	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	PANEL_ID0	I
AH19	GPIO36/SATA2GP	PANEL_ID1	I
AE19	GPIO37/SATA3GP	PCB_ID0	I
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	C
R5C832 CARD READER	AD17	0	C
R5C832 1394	AD17	0	B
R5C841 CARD READER	AD18	1	C
R5C841 1394	AD18	1	B
Mini PCI Card	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)

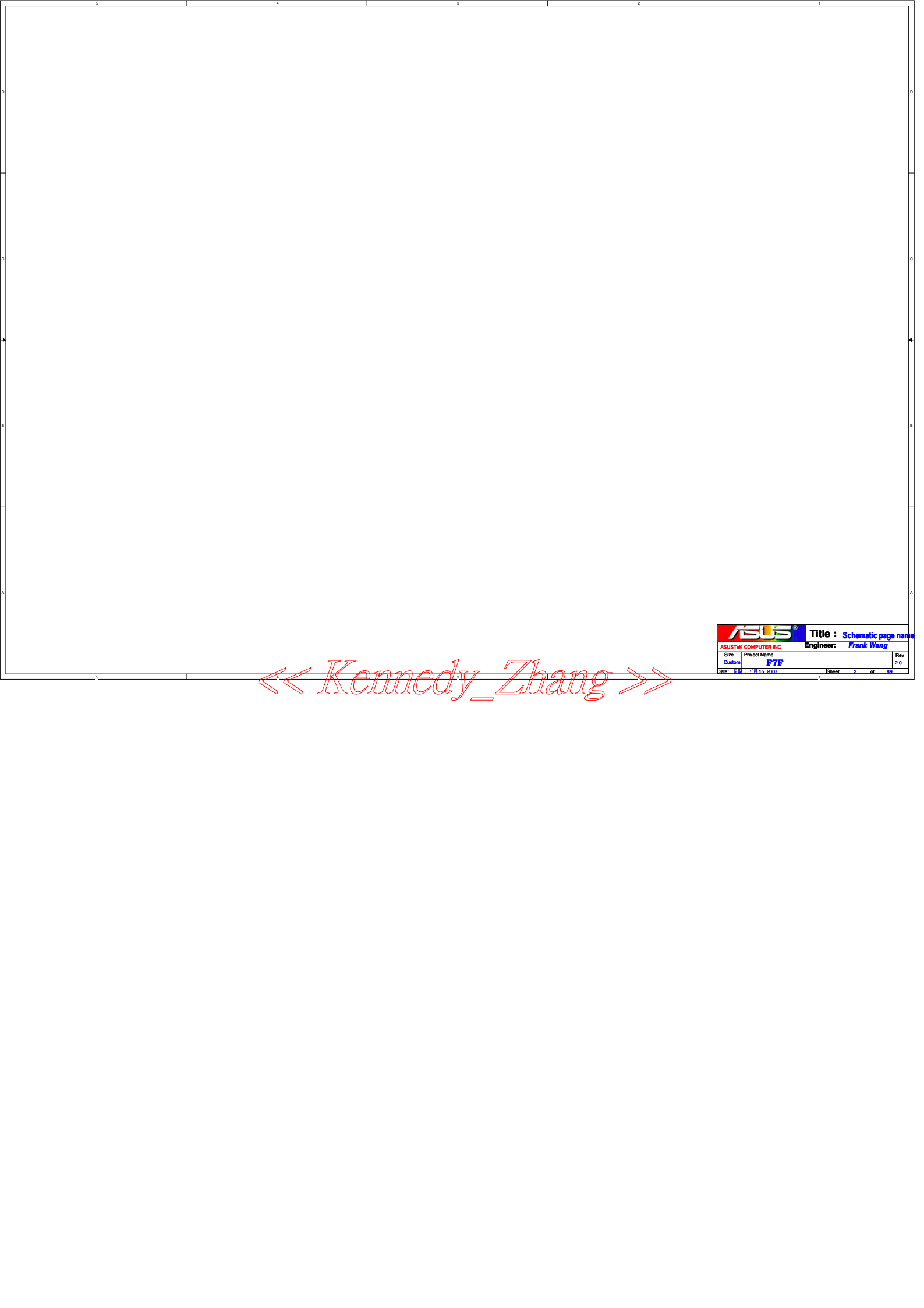
ASUSTek Computer INC. NB1

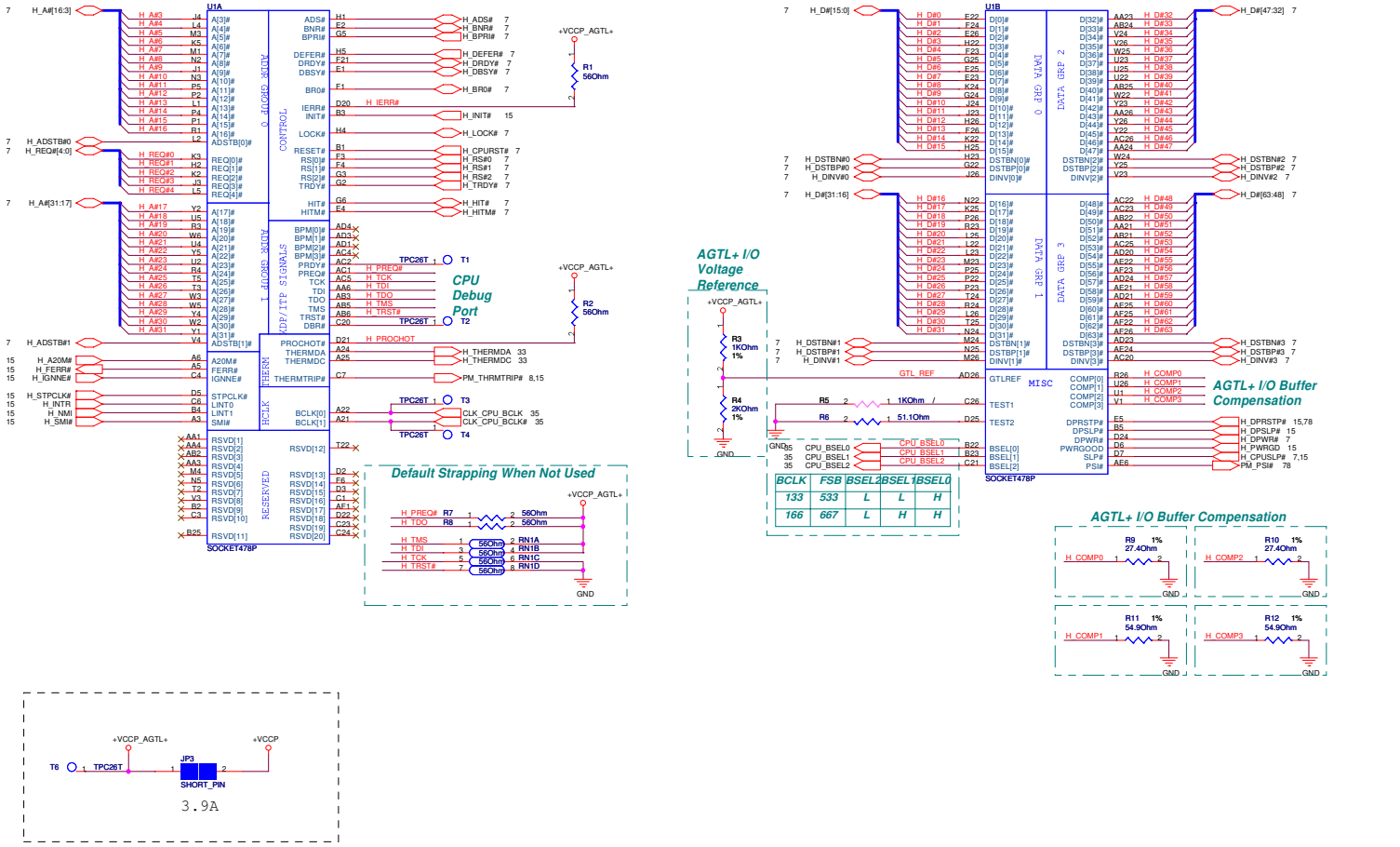
Title : System Setting

Engineer: Frank Wang

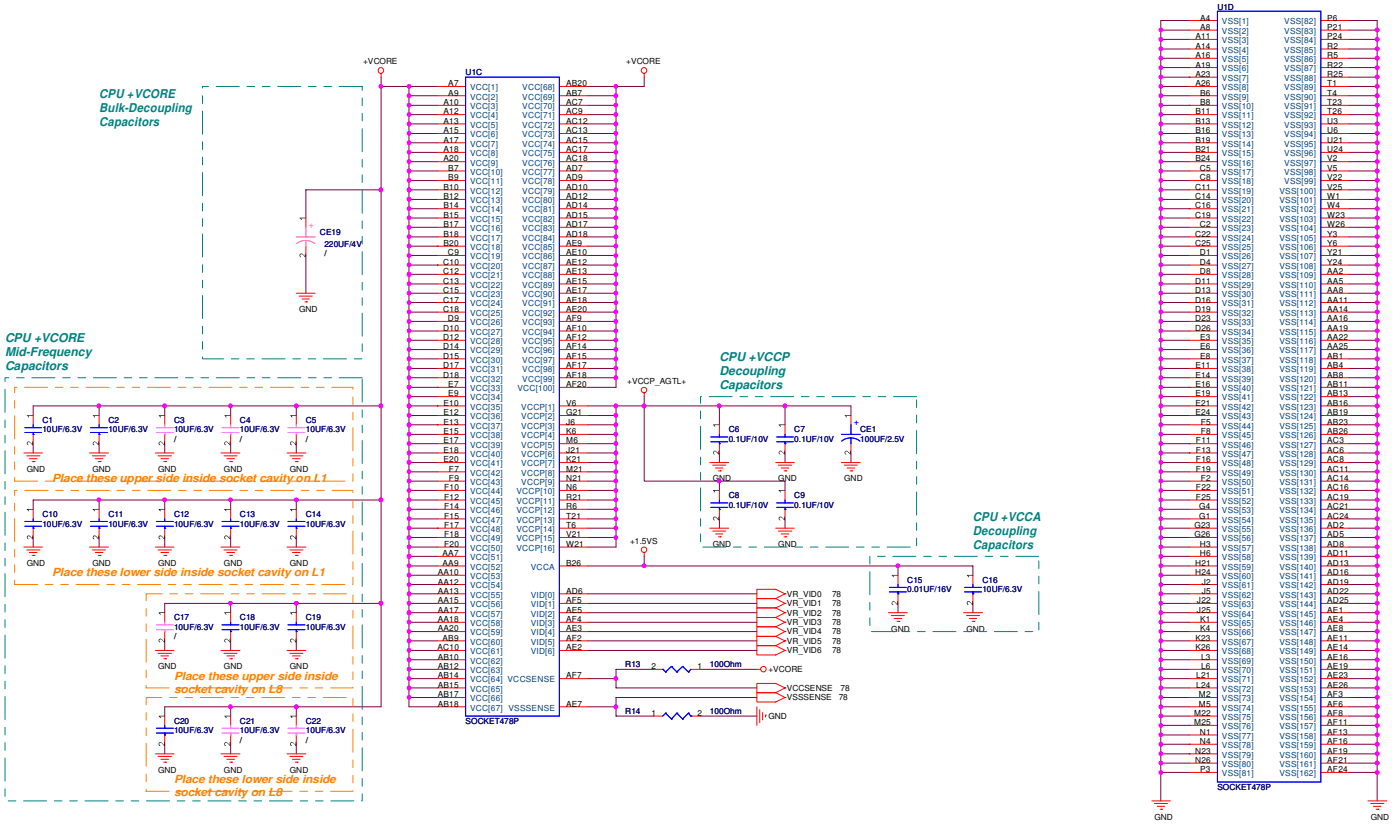
Size: Custom | Project Name: FTF | Rev: 2.0

Date: 星期 二, 十月 15, 2007 | Sheet 2 of 89



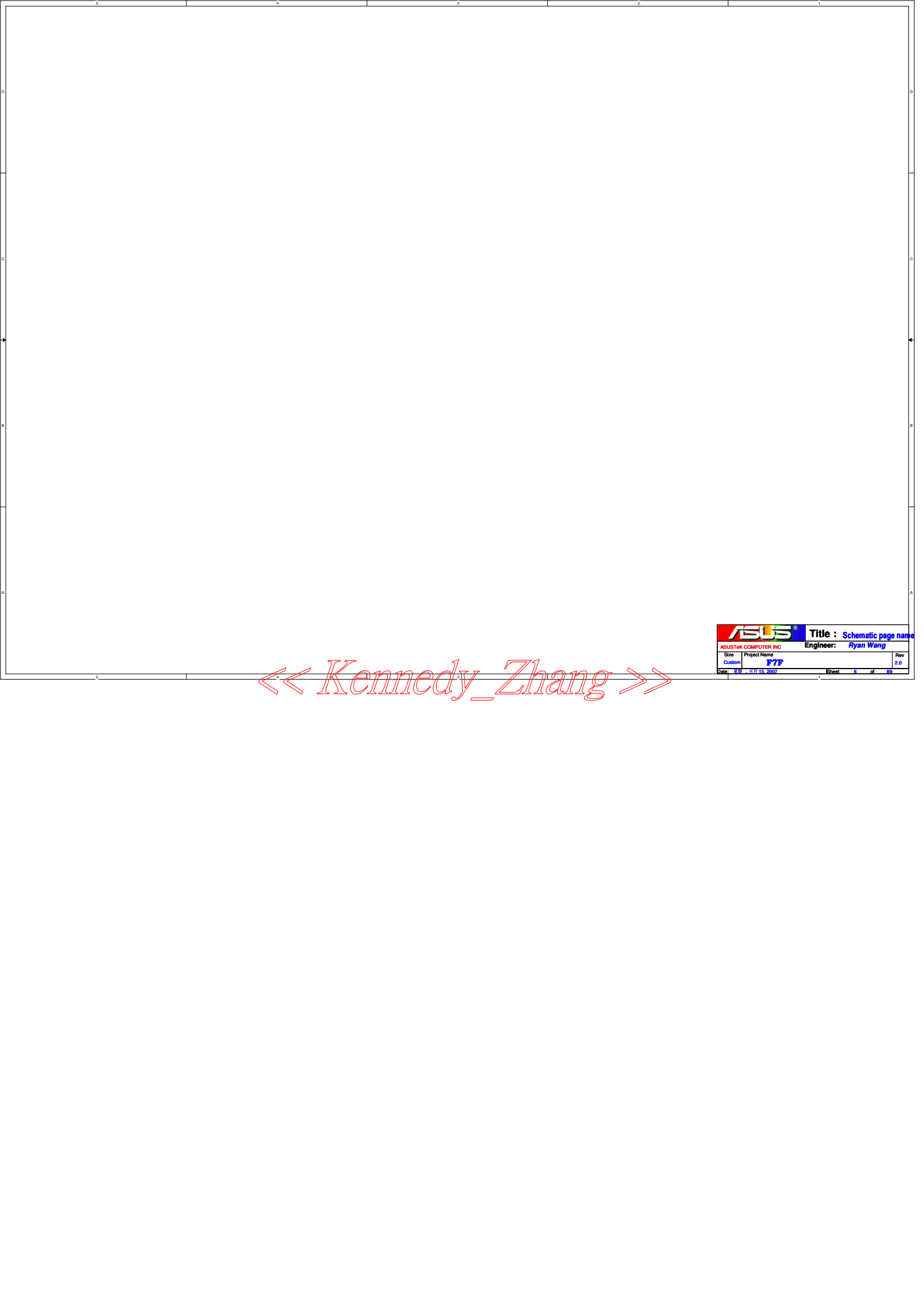


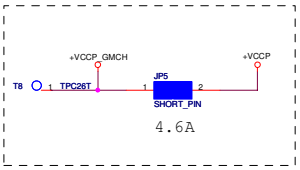
ASUSTeK COMPUTER INC. NB1	Title : CPU-YONAH(HOST)		
	Engineer: Frank Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007		Sheet 4 of 89	

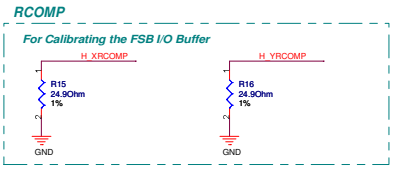


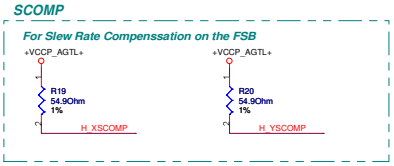
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
R1F: 10UF *16
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4

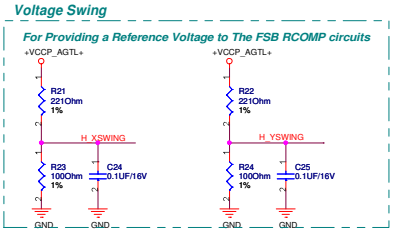
ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: F7F		Rev: 2.0
Date: 星期 二 十月 15, 2007		Sheet 5 of 89	

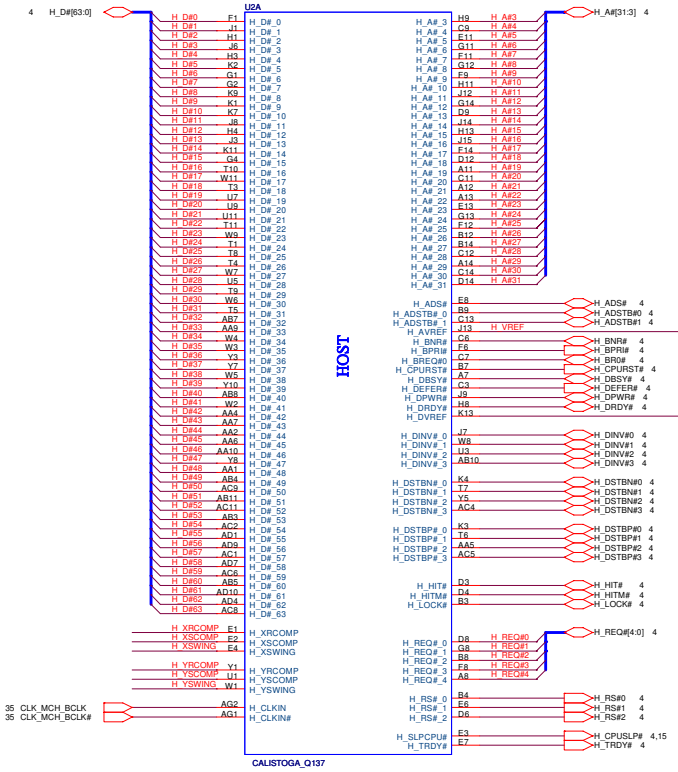


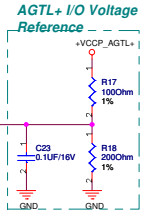












ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(HOST)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 7 of 89		

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GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — R25 1KOhm — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU
1 = Mobile CPU (D)

MCH_CFG_7 — R26 1KOhm — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)

MCH_CFG_15 — R27 1KOhm — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)

MCH_CFG_9 — R30 1KOhm — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R31 1KOhm — GND

CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)

MCH_CFG_10 — R34 1KOhm — GND

CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V

MCH_CFG_18 — R35 1KOhm — +2.5VS

CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)

MCH_CFG_11 — R37 1KOhm — GND

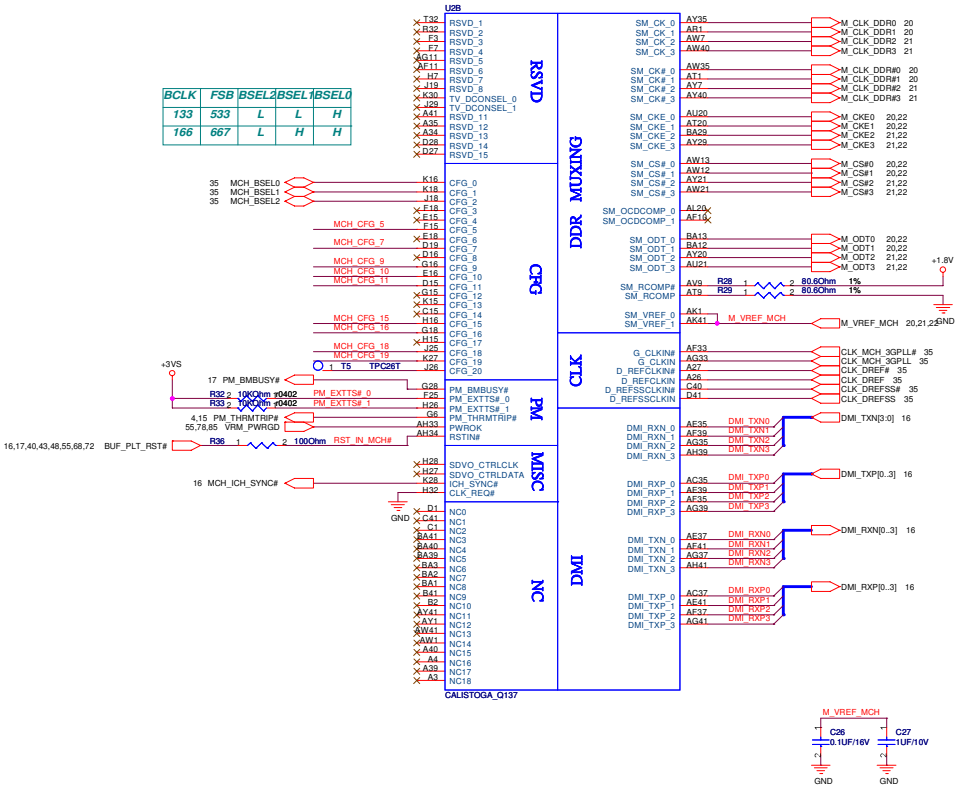
CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

MCH_CFG_19 — R38 1KOhm — +2.5VS

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



Title :	NB-945GM(DMI & CFG)		
ASUSTeK COMPUTER INC. NB1	Engineer:	Ryan Wang	
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 8	of 89	

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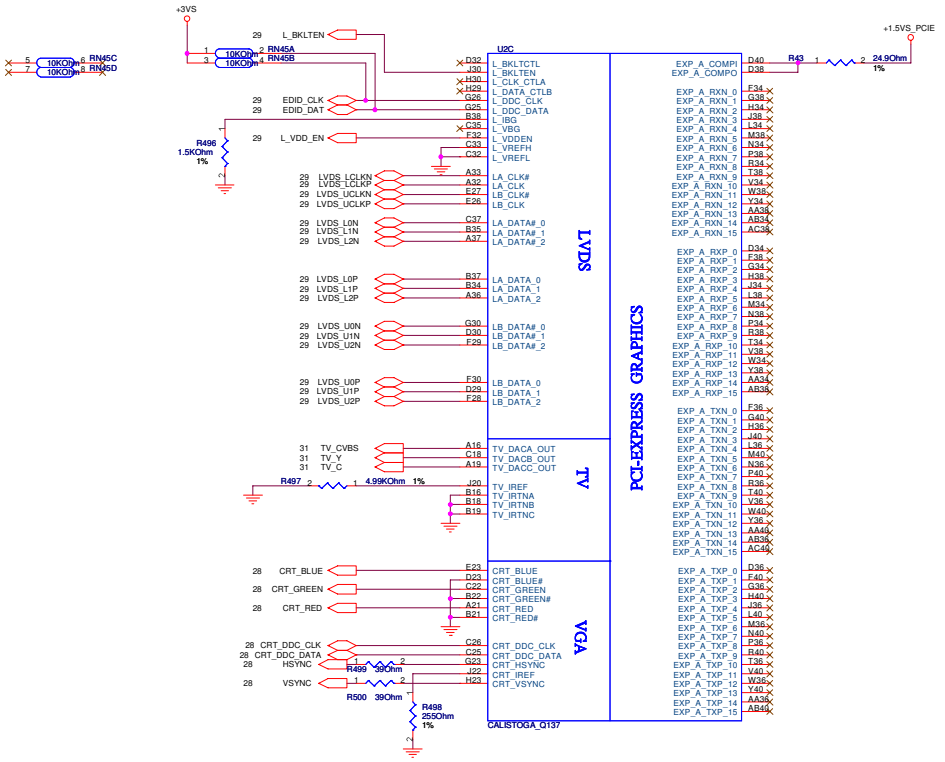
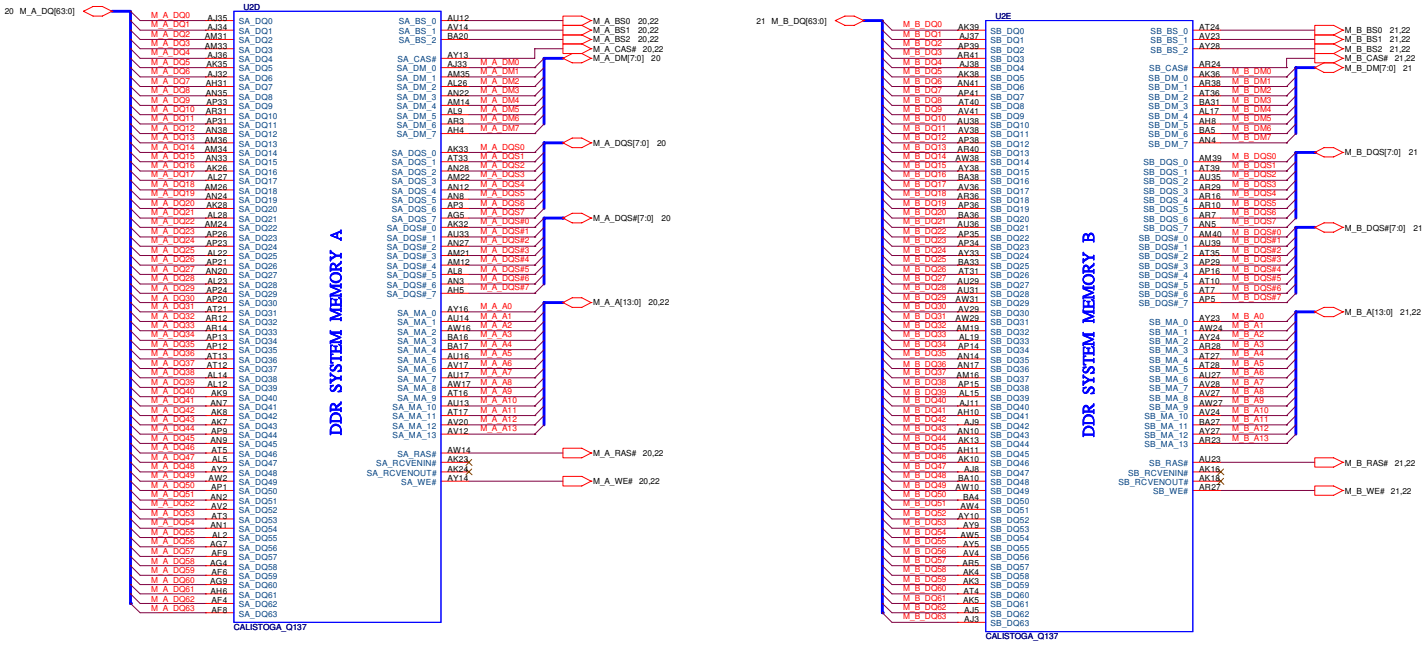
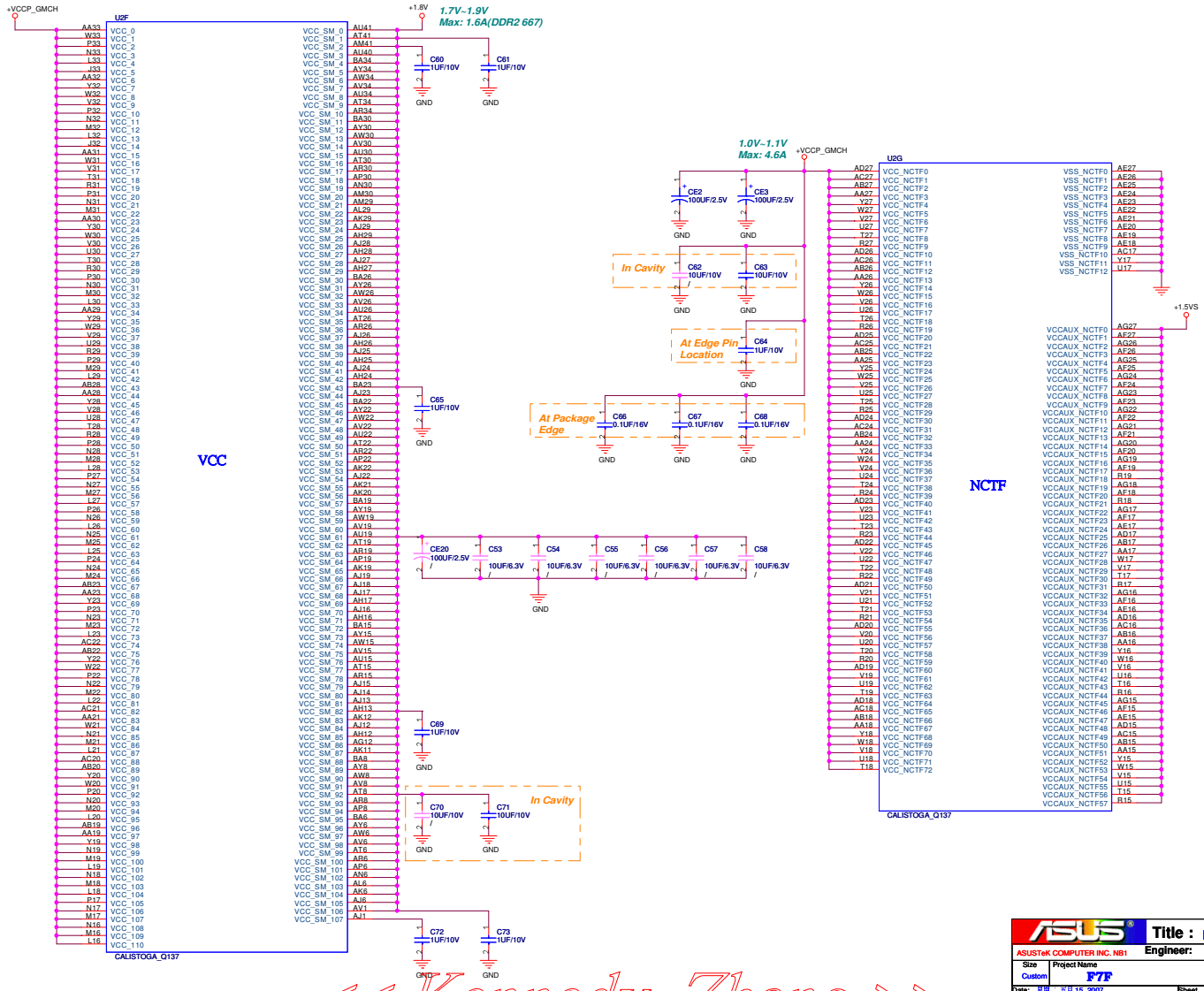


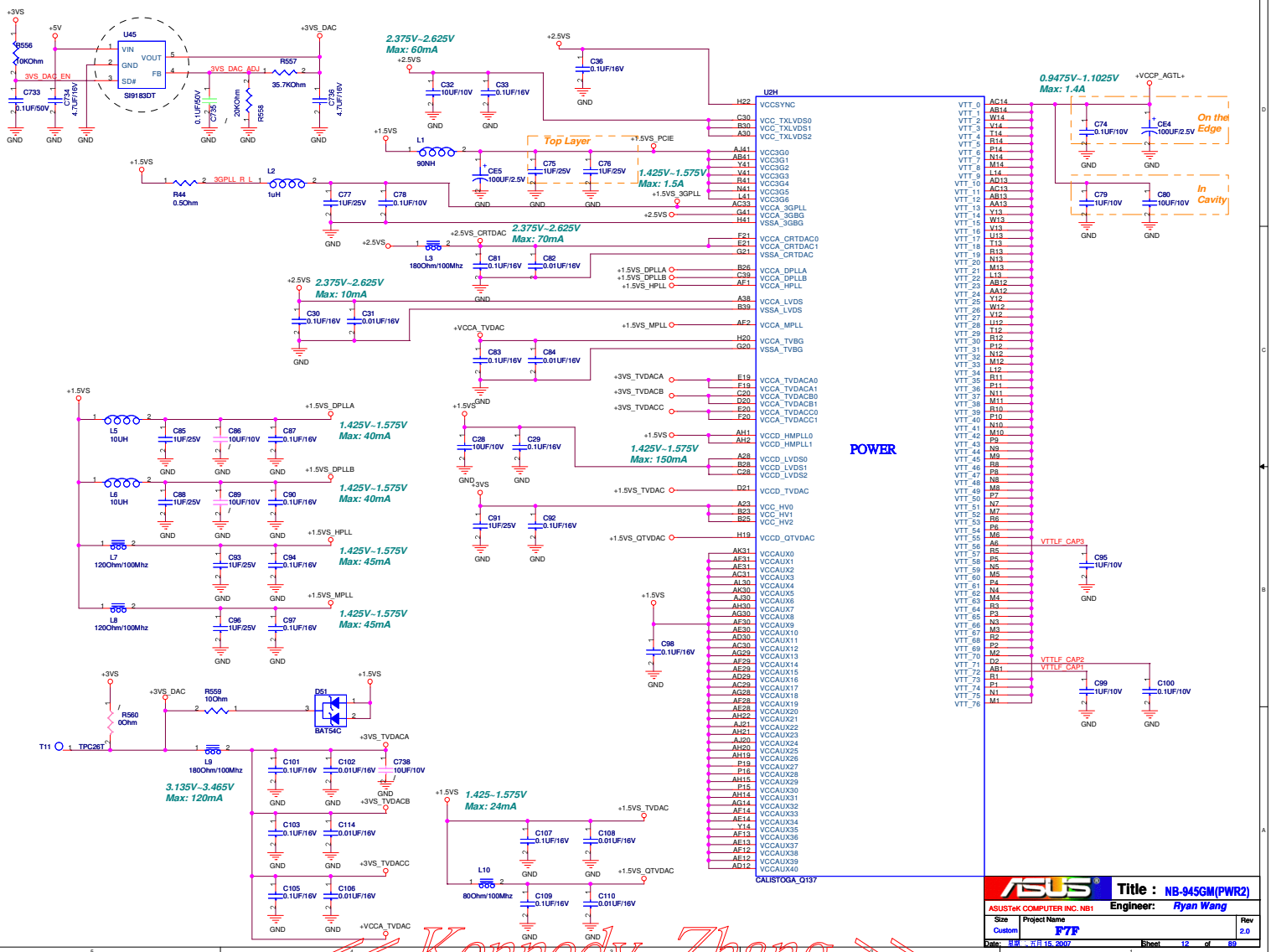
ASUSTeK COMPUTER INC. NB1	Title : NB_945GM(GRAPHIC)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 9 of 89		



ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(DDR2)	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 10 of 89	



ASUSTeK COMPUTER INC. NB1	Title : NB-945GM(PWR)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007		Sheet 11 of 89	


POWER
U2H
CALISTOGA_Q137
U45
SI9183DT
2.375V~2.625V
Max: 60mA
Top Layer
1.425V~1.575V
Max: 1.5A
2.375V~2.625V
Max: 70mA
2.375V~2.625V
Max: 10mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 40mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 45mA
1.425V~1.575V
Max: 150mA
3.135V~3.465V
Max: 120mA
1.425~1.575V
Max: 24mA
0.9475V~1.1025V
Max: 1.4A
On the Edge
In Cavity
ASUSTeK COMPUTER INC. NB1
Title : NB-945GM(PWR2)
Engineer: Ryan Wang
Project Name FTF
Rev 2.0
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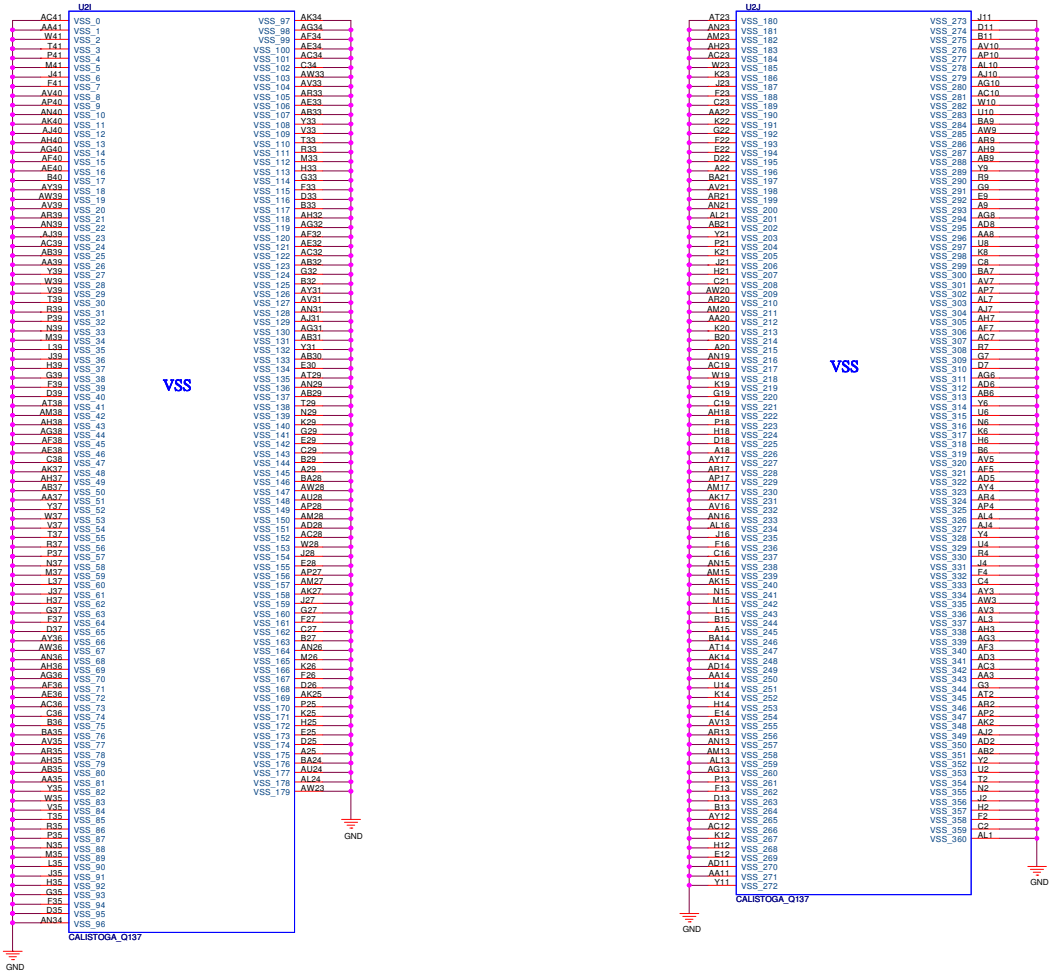
<< Kennedy_Zhang >>



Title :	NB-945GM(GND)
ASUSTeK COMPUTER INC. NB1	Engineer: Ryan Wang
Size: Custom	Project Name: FTF
Rev: 2.0	
Date: 星期 二, 十月 15, 2007	Sheet 13 of 89

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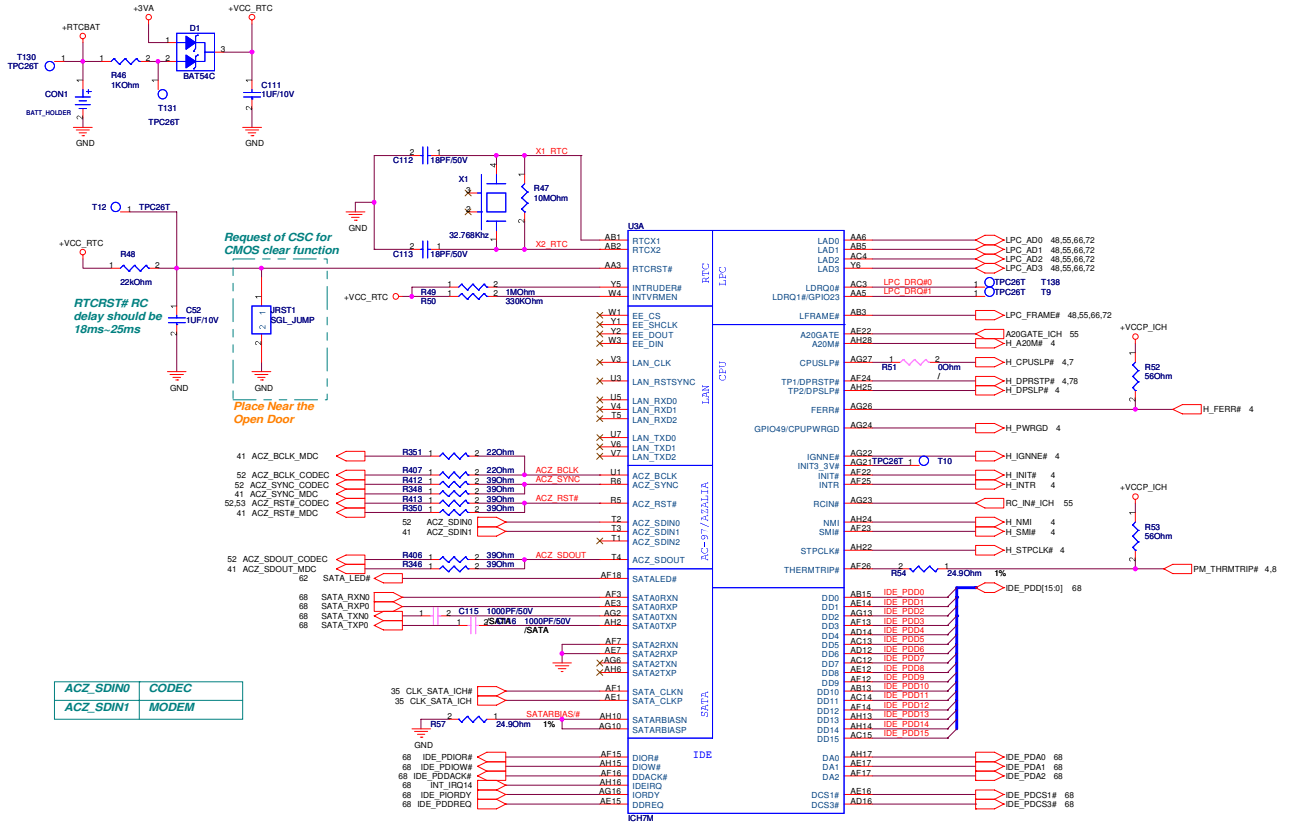

ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM

ASUSTeK COMPUTER INC. NB1

Title : SB-ICH7-M(1)

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

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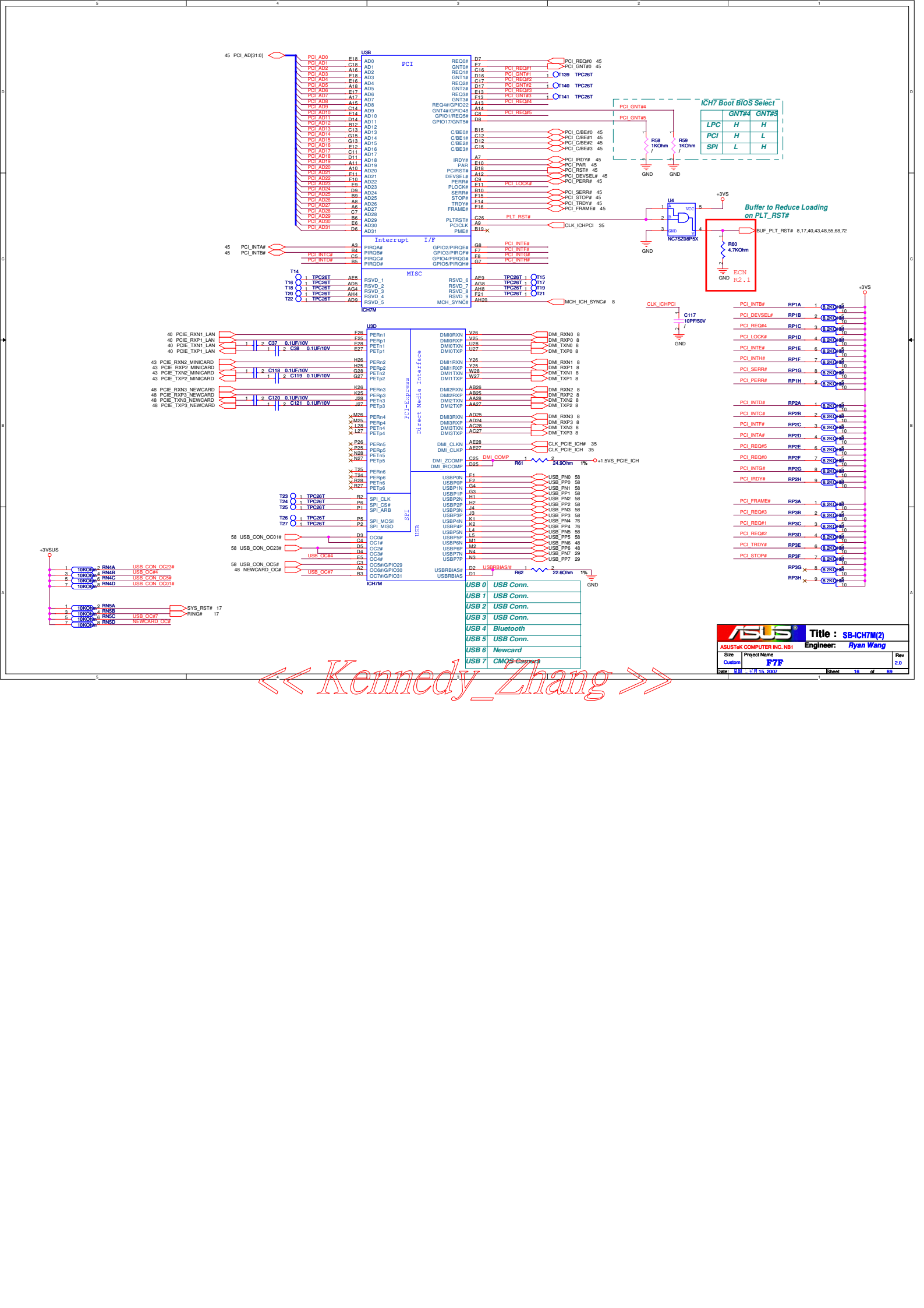
U3B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
Buffer to Reduce Loading on PLT_RST#
U4
NC7SZ08P5X
R60 4.7KOhm
ECN R2.1
U3D
PCI-Express
Direct Media Interface
SPI
USB
USB 0 USB Conn.
USB 1 USB Conn.
USB 2 USB Conn.
USB 3 USB Conn.
USB 4 Bluetooth
USB 5 USB Conn.
USB 6 Newcard
USB 7 CMOS Camera
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan Wang
Size Custom
Project Name FTF
Rev 2.0
Date: 星期 二 十月 15, 2007
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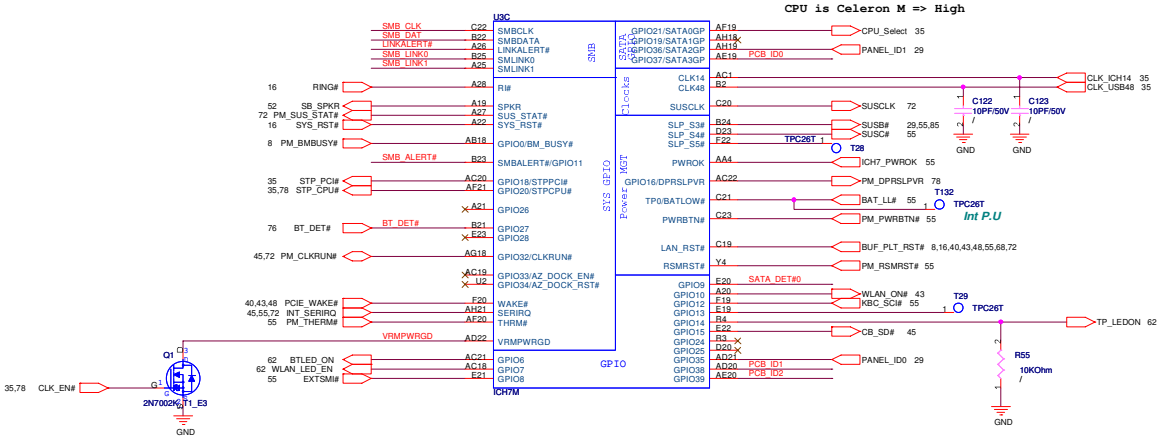
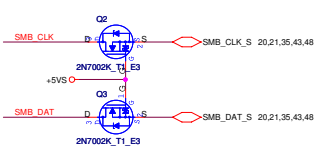
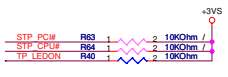
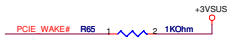
<< Kennedy_Zhang >>

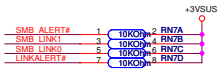
CPU_Select :
CPU is Pentem M => Low
CPU is Celeron M => High

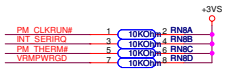


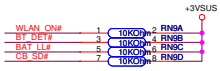


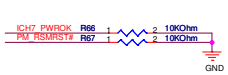


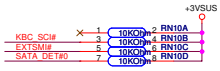


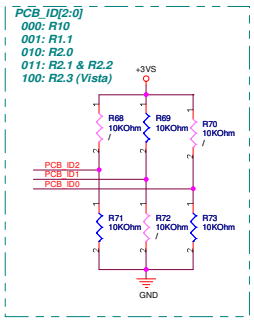






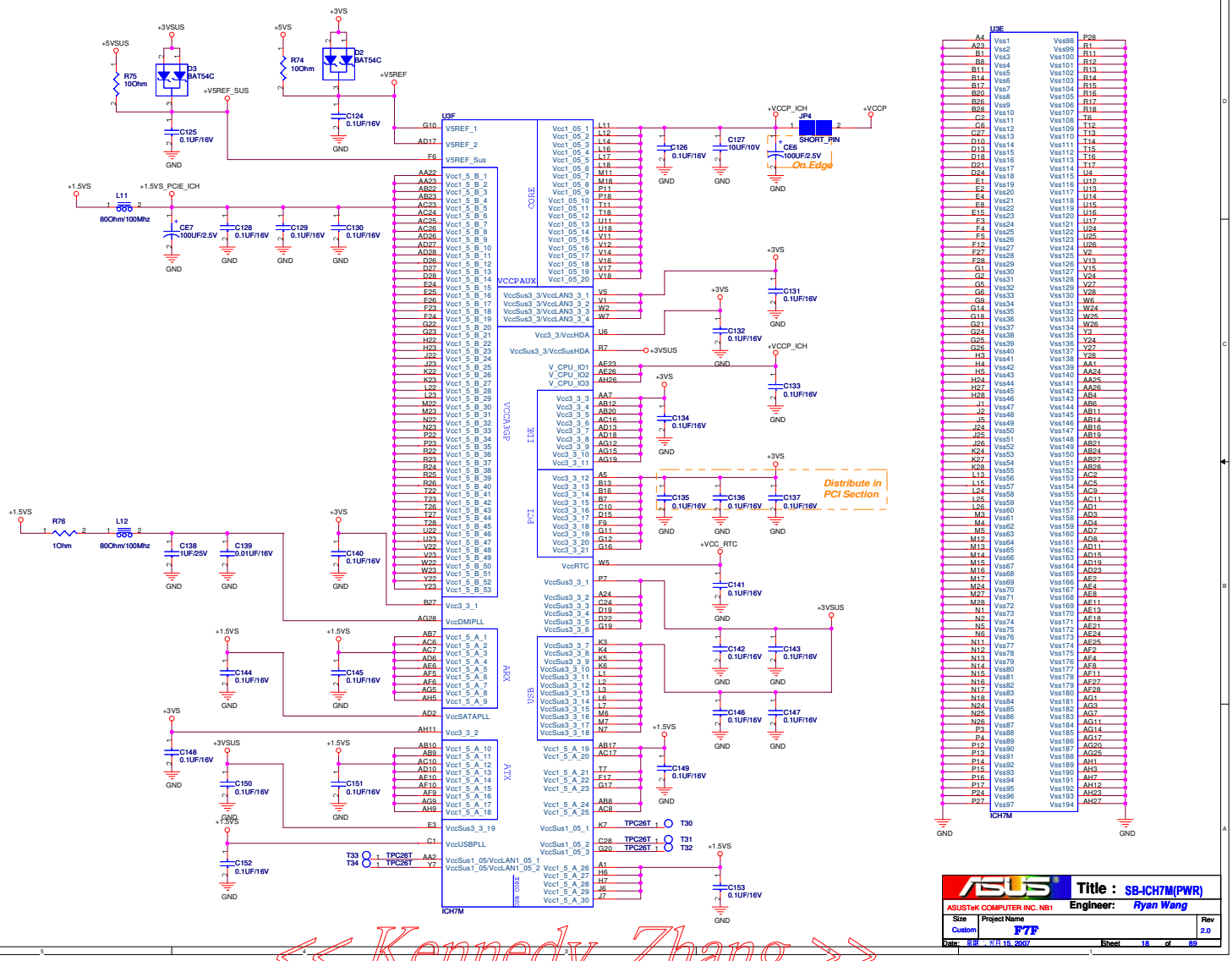






ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(3)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: F7F		Rev: 2.0
Date: 星期 二 十月 15, 2007		Sheet 17 of 89	

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC. NB1

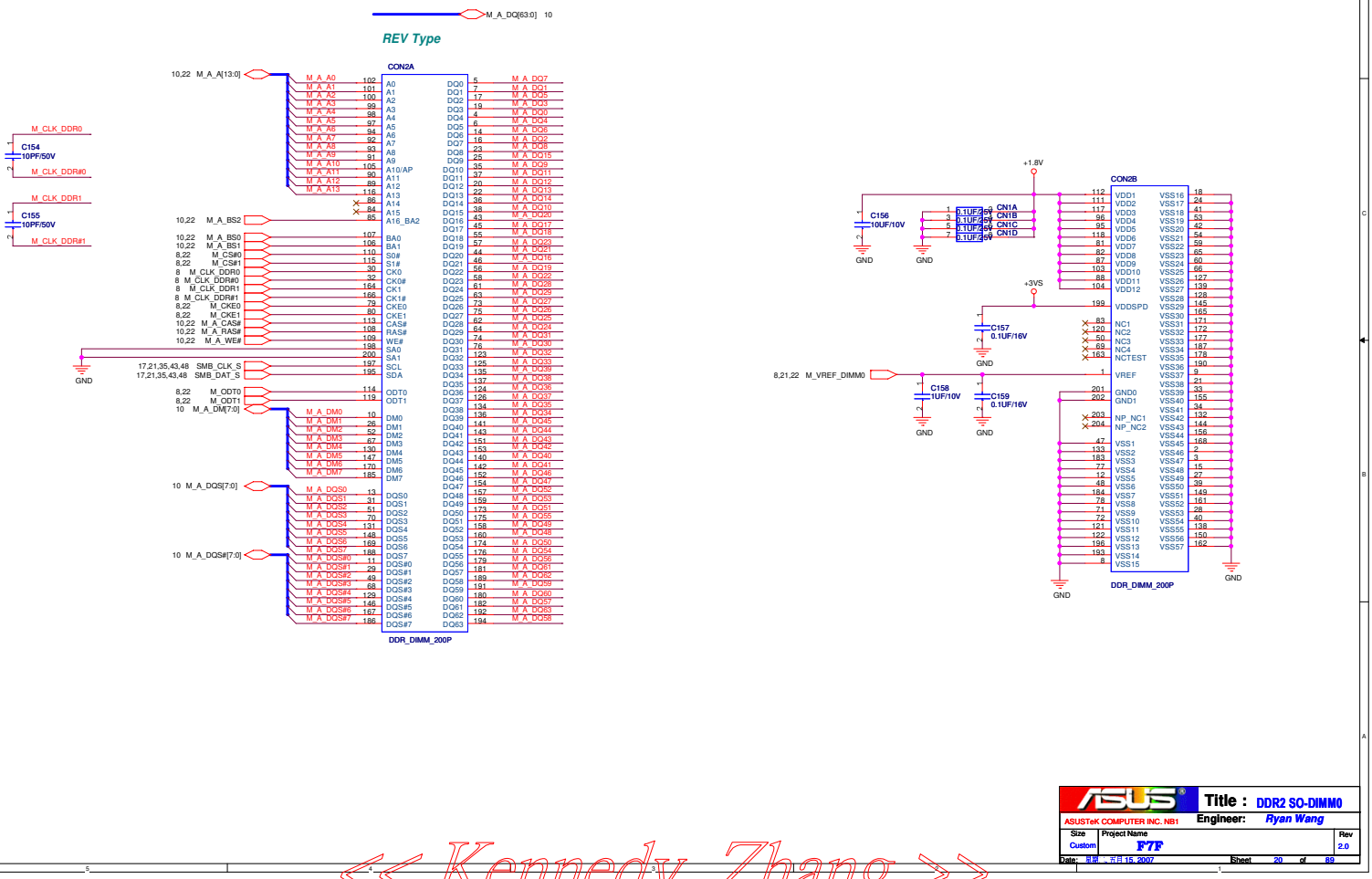
Title : SB-ICH7M(PWR)

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二 十月 15, 2007 Sheet 18 of 89

<< Kennedy_Zhang >>

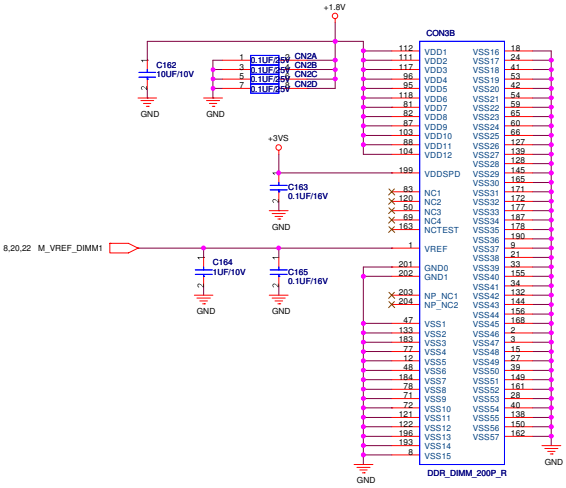


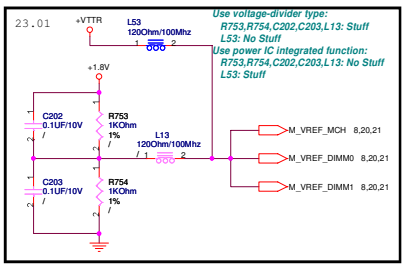
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM0		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 六月 15, 2007	Sheet 20 of 89		

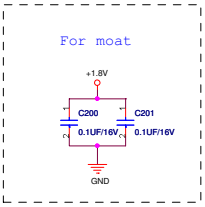
<< Kennedy_Zhang >>

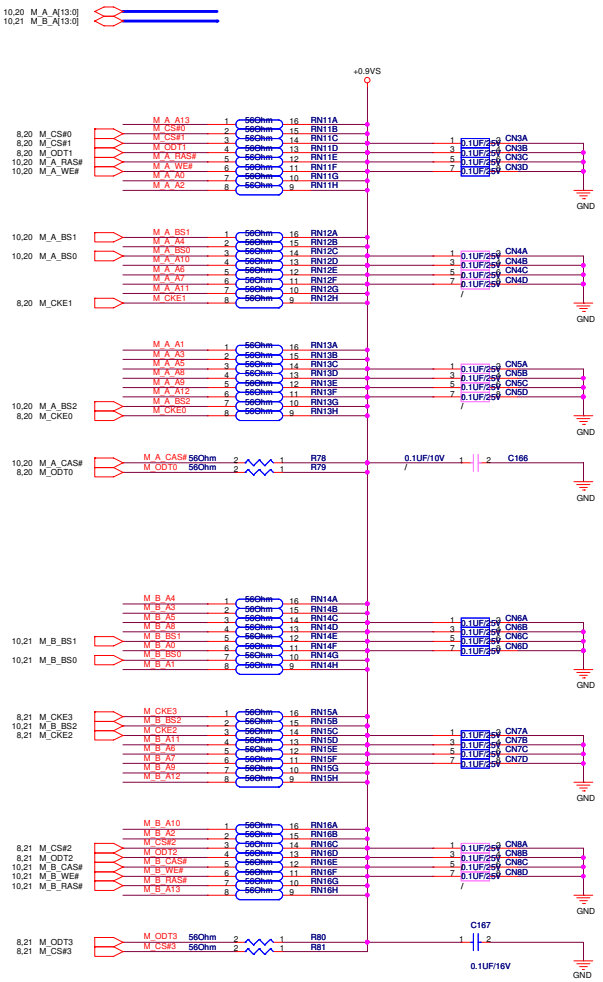
M_B_DQ[63:0] 10

STD Type









ASUSTeK COMPUTER INC. NB1

Title : DDR2 TERMINATION

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

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ASUSTeK COMPUTER INC	Title : Schematic page name	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 23 of 89	

Title :

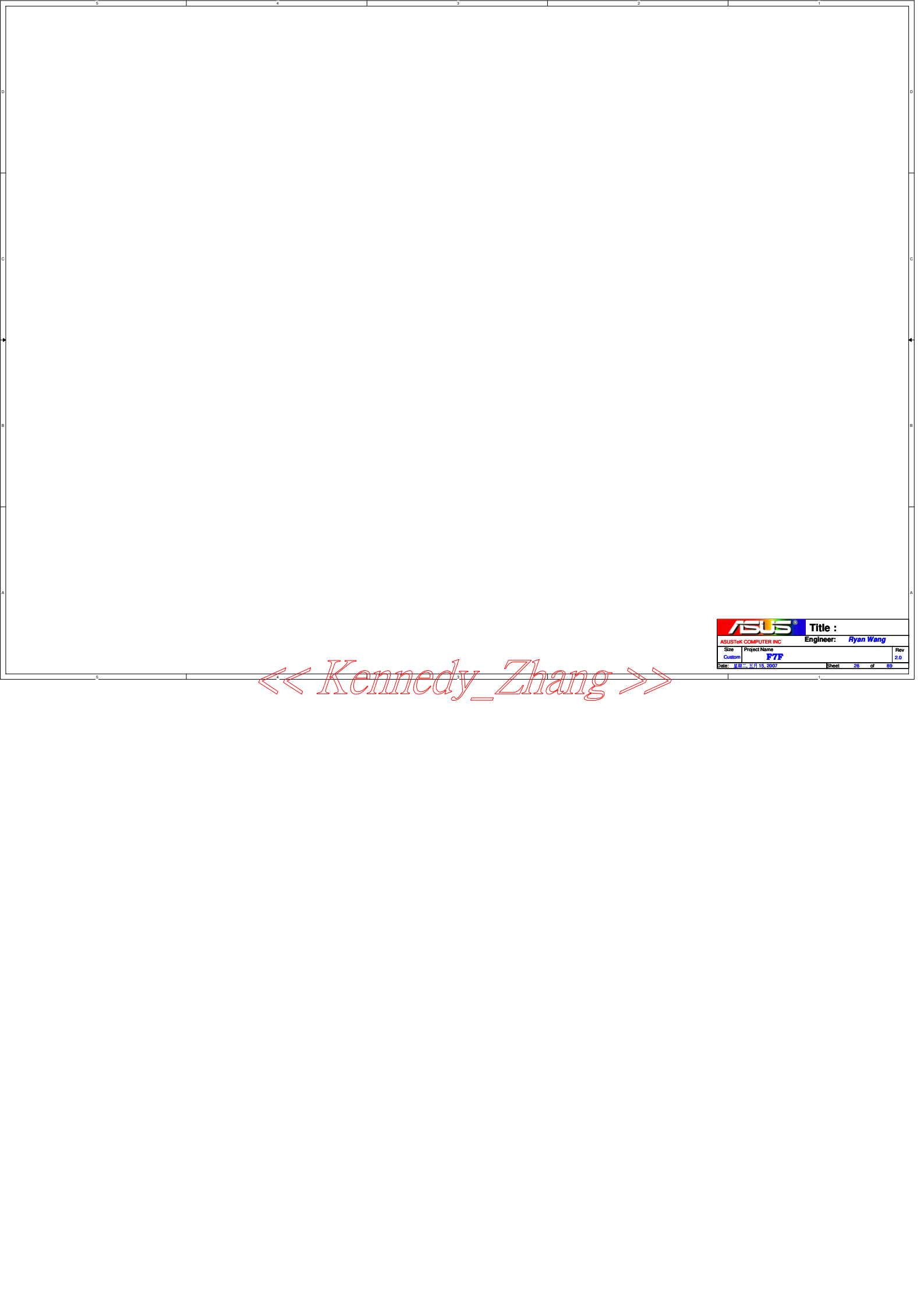
ASUSTek COMPUTER INC

Engineer: Ryan Wang

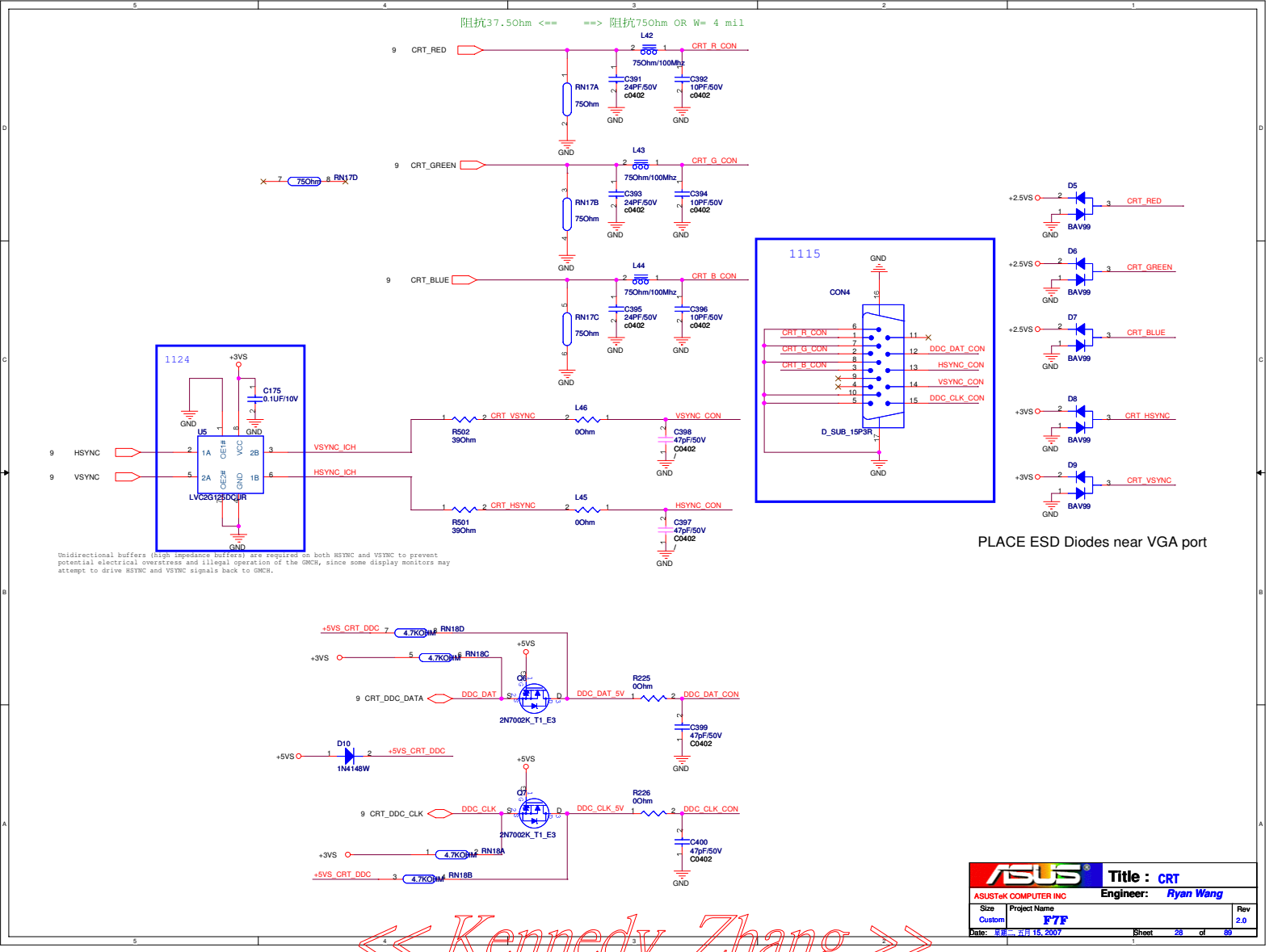
Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 十月 15, 2007 Sheet 24 of 89

ASUSTek COMPUTER INC	Title: Schematic page name		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 25 of 89		



ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Ryan Wang		
Size: C	Project Name: FTP		Rev: 2.0
Date: 星期一, 十月 15, 2007	Sheet 27 of 69		



ASUSTeK COMPUTER INC

Title : CRT

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	F7F	2.0

Date: 星期二, 五月 15, 2007 Sheet 28 of 89

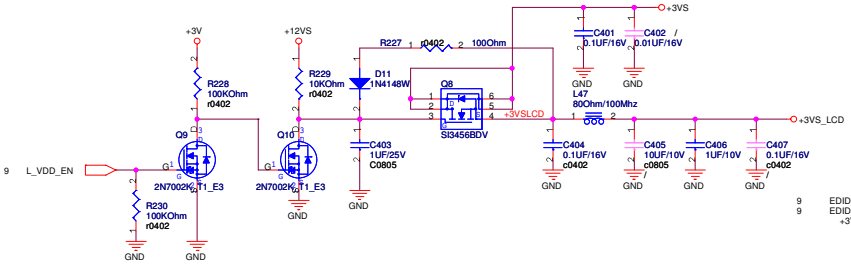
<< Kennedy_Zhang >>

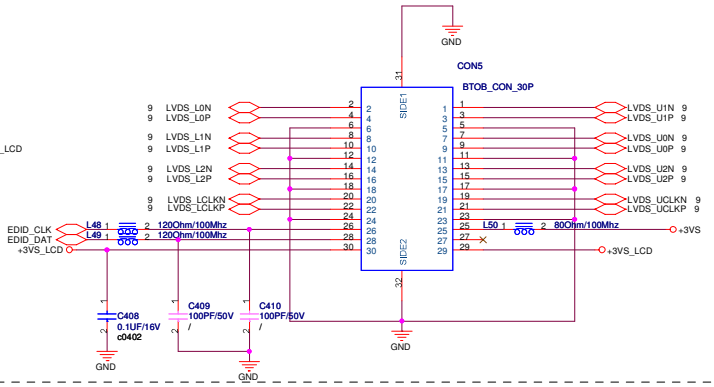
LCD Backlight Control

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

LCD Power



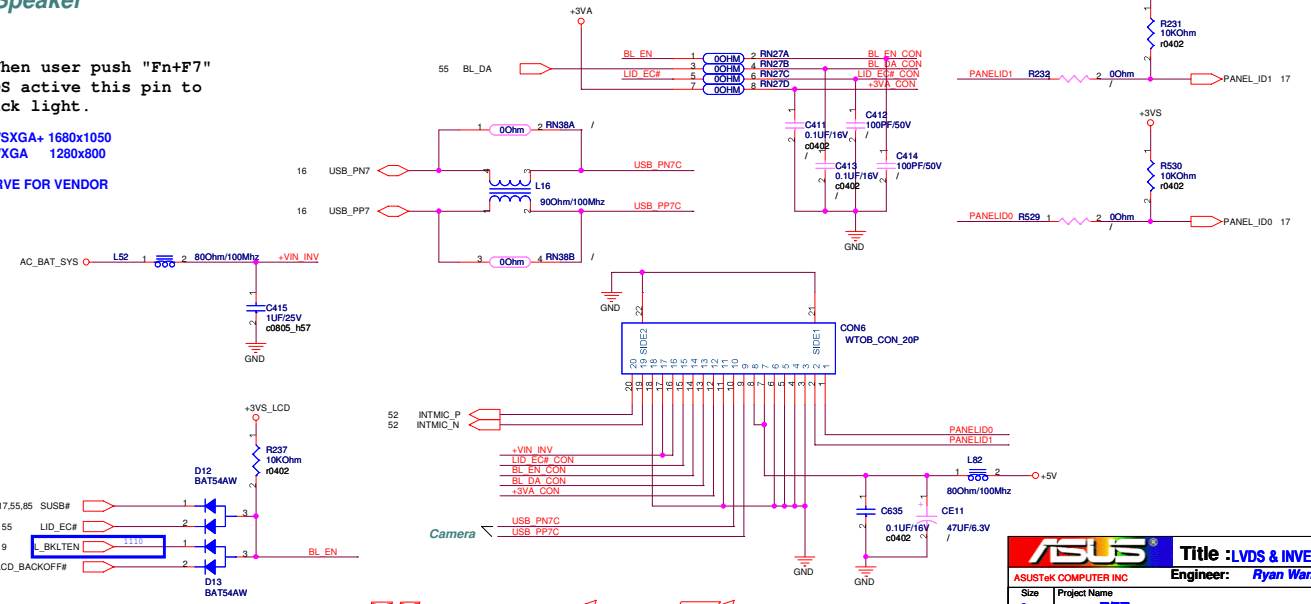


INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR



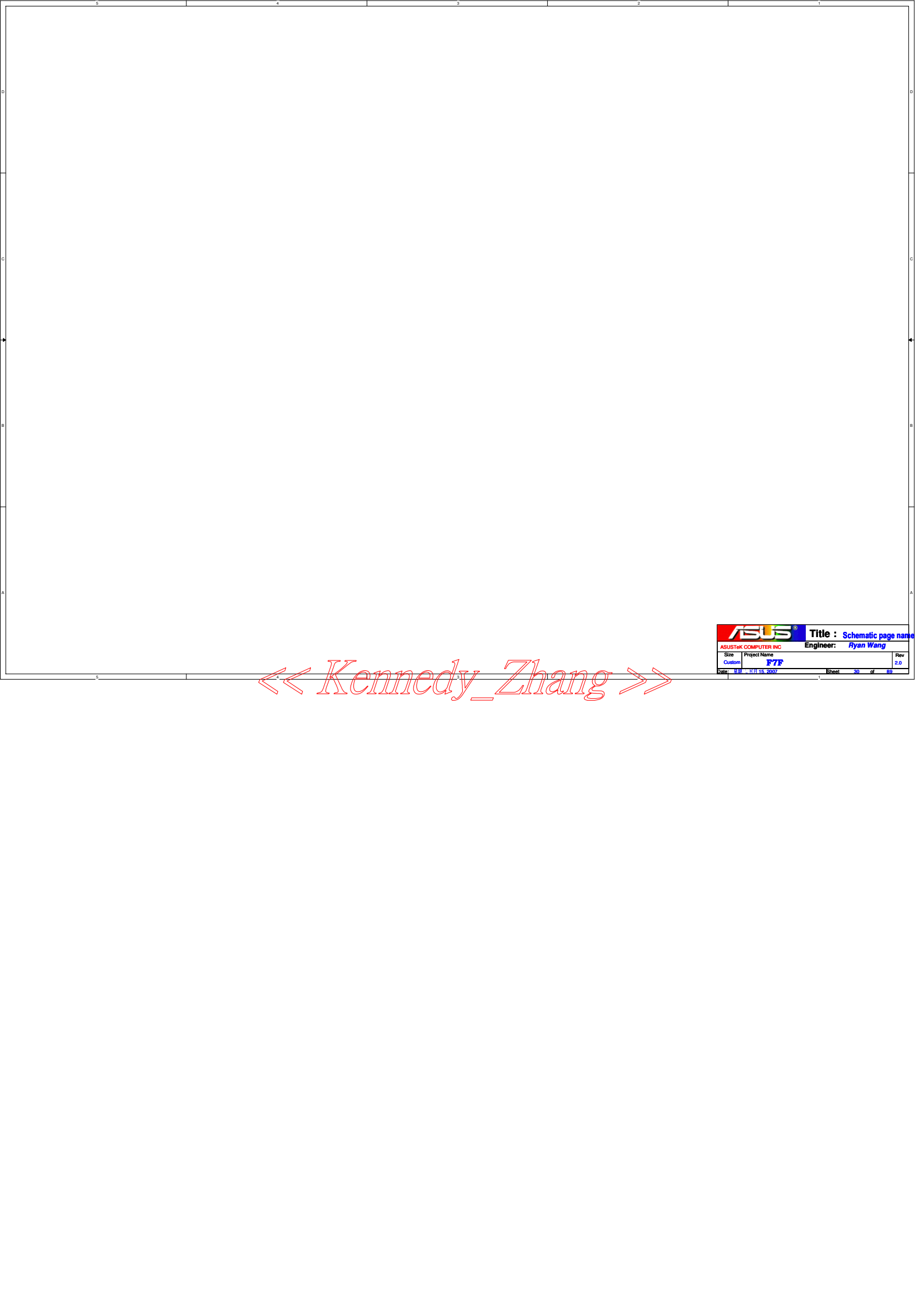
ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

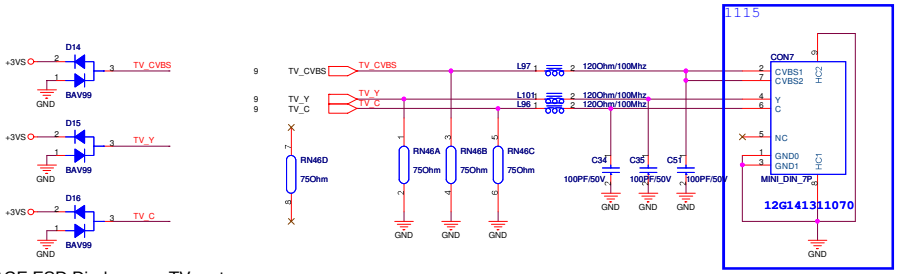
Engineer: Ryan Wang

Size	Project Name	Rev
Custom	F7F	2.0

Date: 星期二, 五月 15, 2007 Sheet 29 of 89



TV OUT



PLACE ESD Diodes near TV port

ASUSTeK COMPUTER INC	Title : TV OUT & AV_IN		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 31 of 89		

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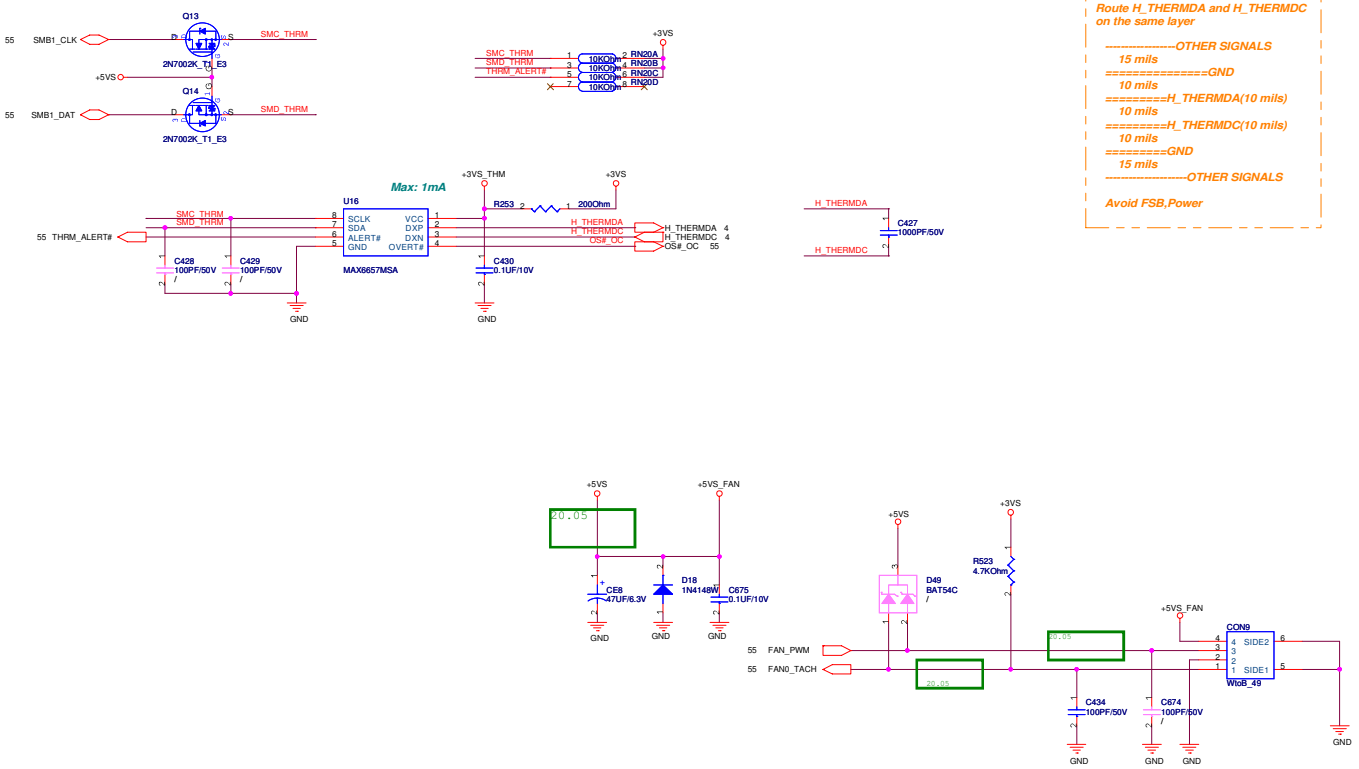
Thermal Sensor



ASUSTeK COMPUTER INC. NB1	Title : THER SENSOR & FAN		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 33 of 89		

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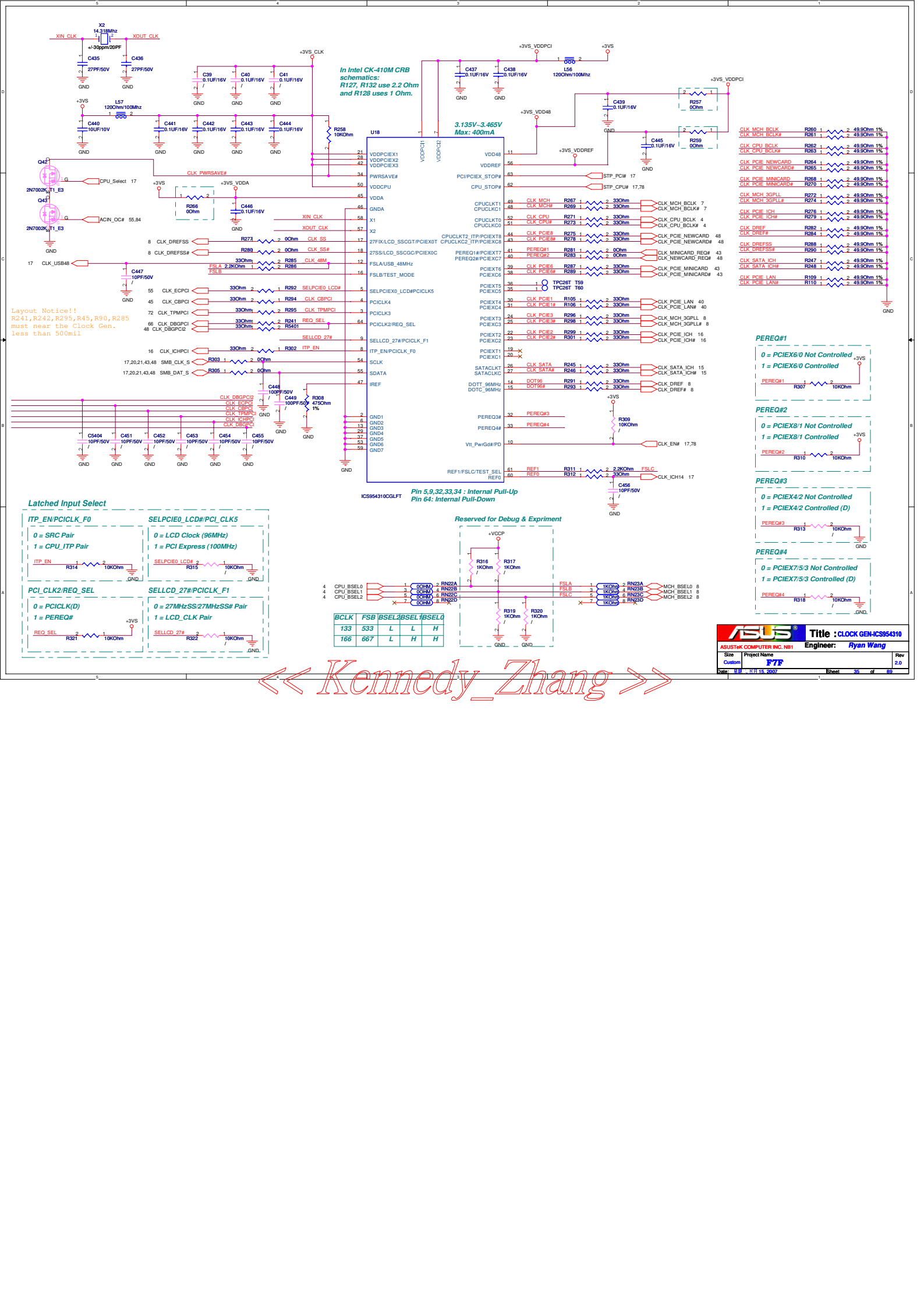
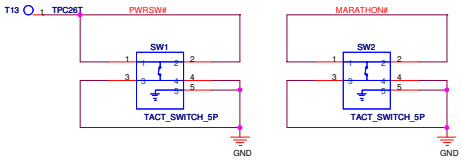
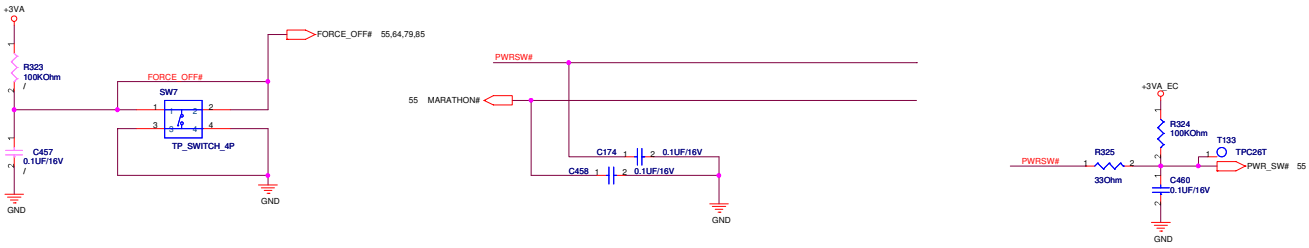
ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 34 of 89		

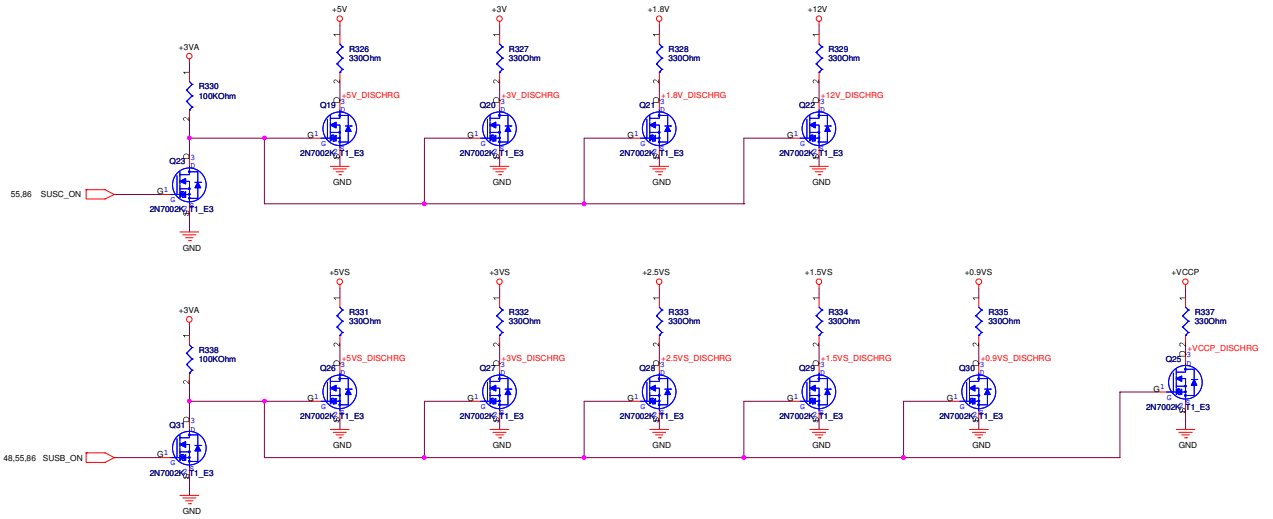

In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128 uses 1 Ohm.
3.135V~3.465V
Max: 400mA
U18
ICS954310CGLFT
Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down
Layout Notice!!
R241,R242,R295,R45,R90,R285 must near the Clock Gen. less than 500mil
Latched Input Select
ITP_EN/PCICLK_F0
0 = SRC Pair
1 = CPU_ITP Pair
SELPCIE0_LCD#/PCI_CLK5
0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)
PCI_CLK2/REQ_SEL
0 = PCICLK(D)
1 = PEREQ#
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
Reserved for Debug & Expriment
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
PEREQ#1
0 = PCIEX6/0 Not Controlled
1 = PCIEX6/0 Controlled
PEREQ#2
0 = PCIEX8/1 Not Controlled
1 = PCIEX8/1 Controlled
PEREQ#3
0 = PCIEX4/2 Not Controlled
1 = PCIEX4/2 Controlled (D)
PEREQ#4
0 = PCIEX7/5/3 Not Controlled
1 = PCIEX7/5/3 Controlled (D)
Title : CLOCK GEN-ICS954310
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan Wang
Size: Custom
Project Name: FTF
Rev: 2.0
Date: 星期 二, 十月 15, 2007
Sheet 35 of 89
<< Kennedy_Zhang >>



SHUT_DOWN#



ASUSTeK COMPUTER INC	Title : Power on & Res Freq	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 37 of 89	



Title : DISCHARGE & EMI CAP

ASUSTeK COMPUTER INC. NB1

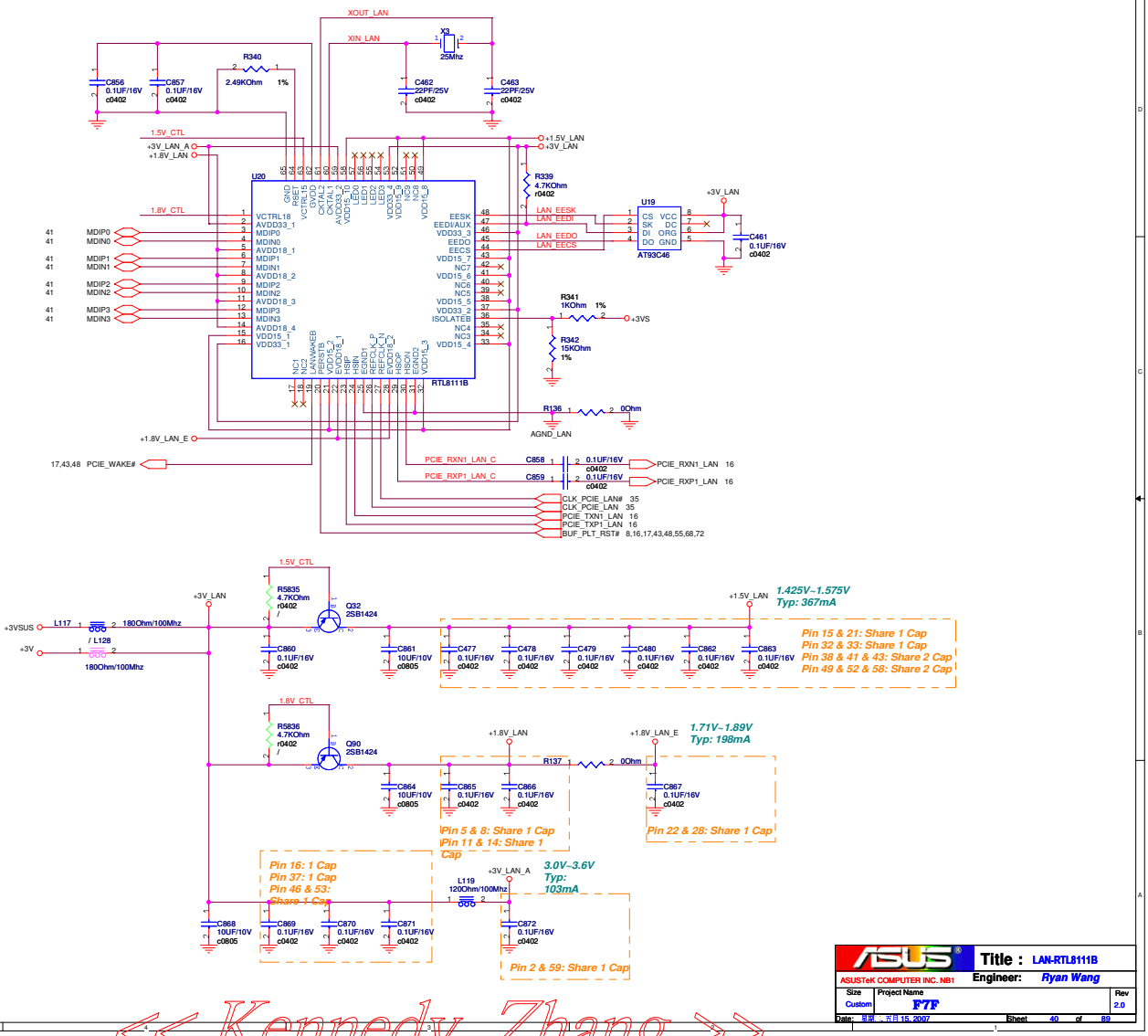
Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 六月 15, 2007 Sheet 38 of 89

<< Kennedy_Zhang >>

ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 39 of 89		



ASUSTeK COMPUTER INC. NB1	Title : LAN-RTL8111B		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 40 of 89		

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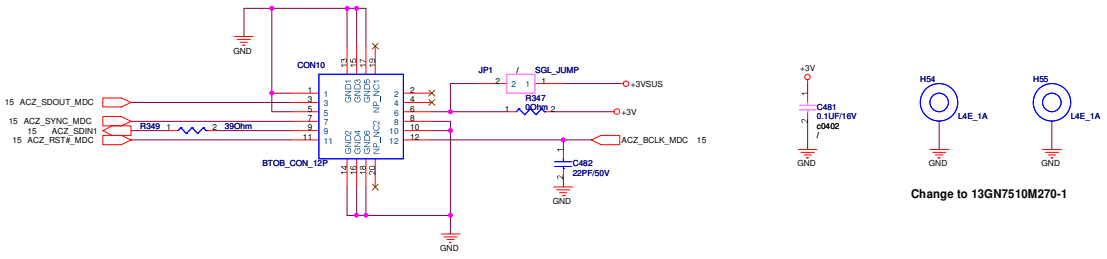
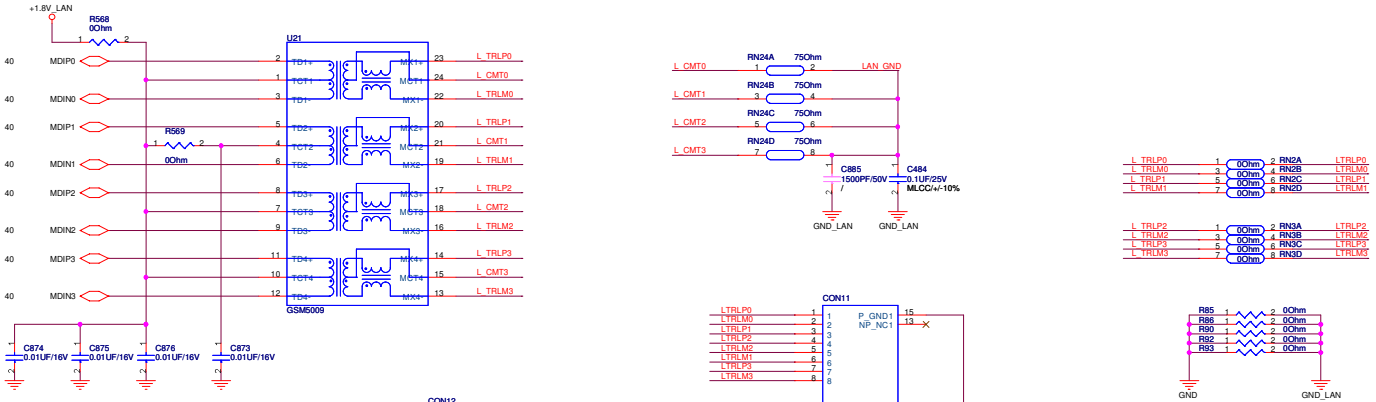
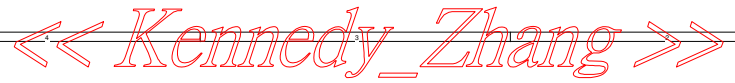
MDC CONN.



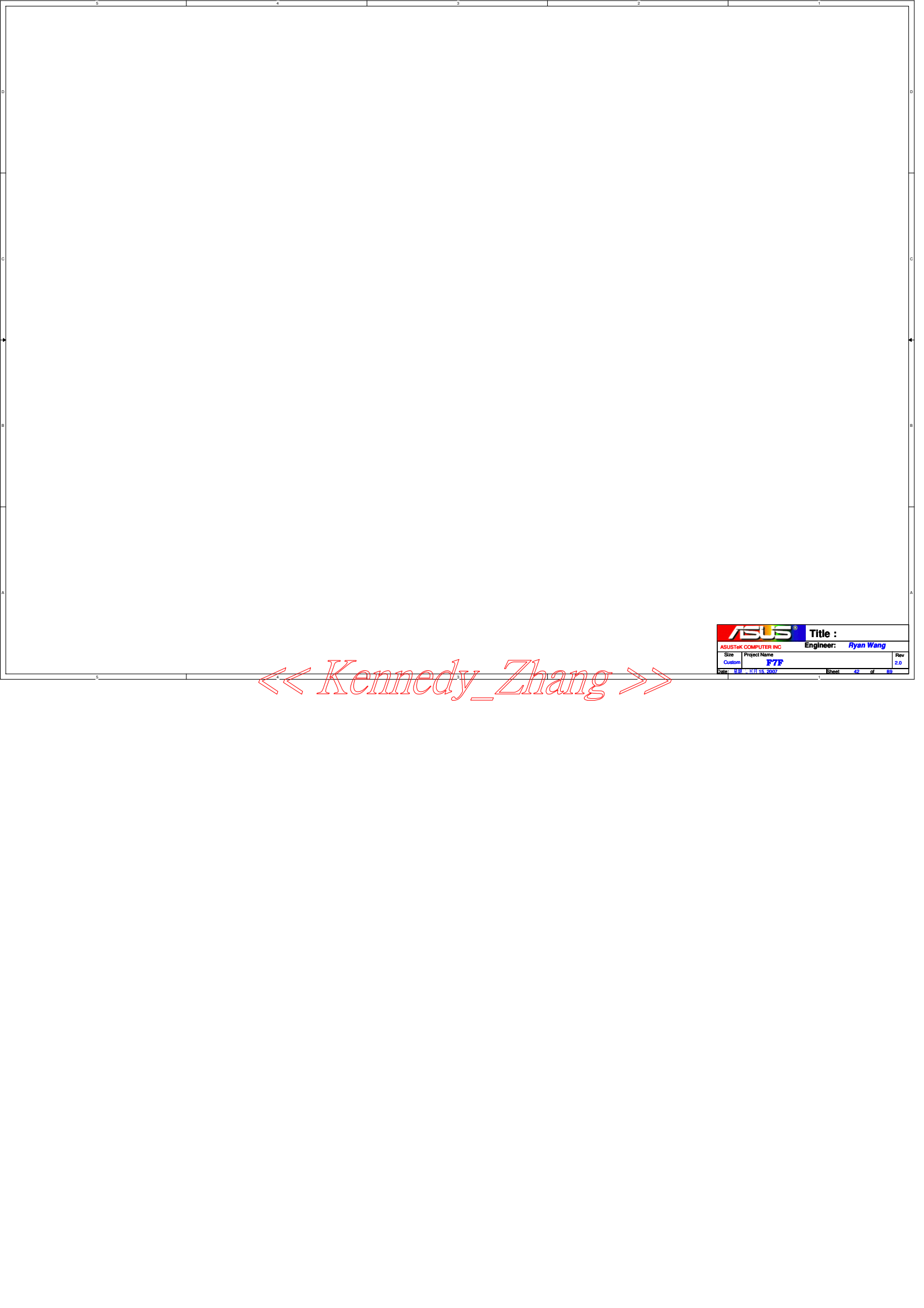
Change to 13GN7510M270-1

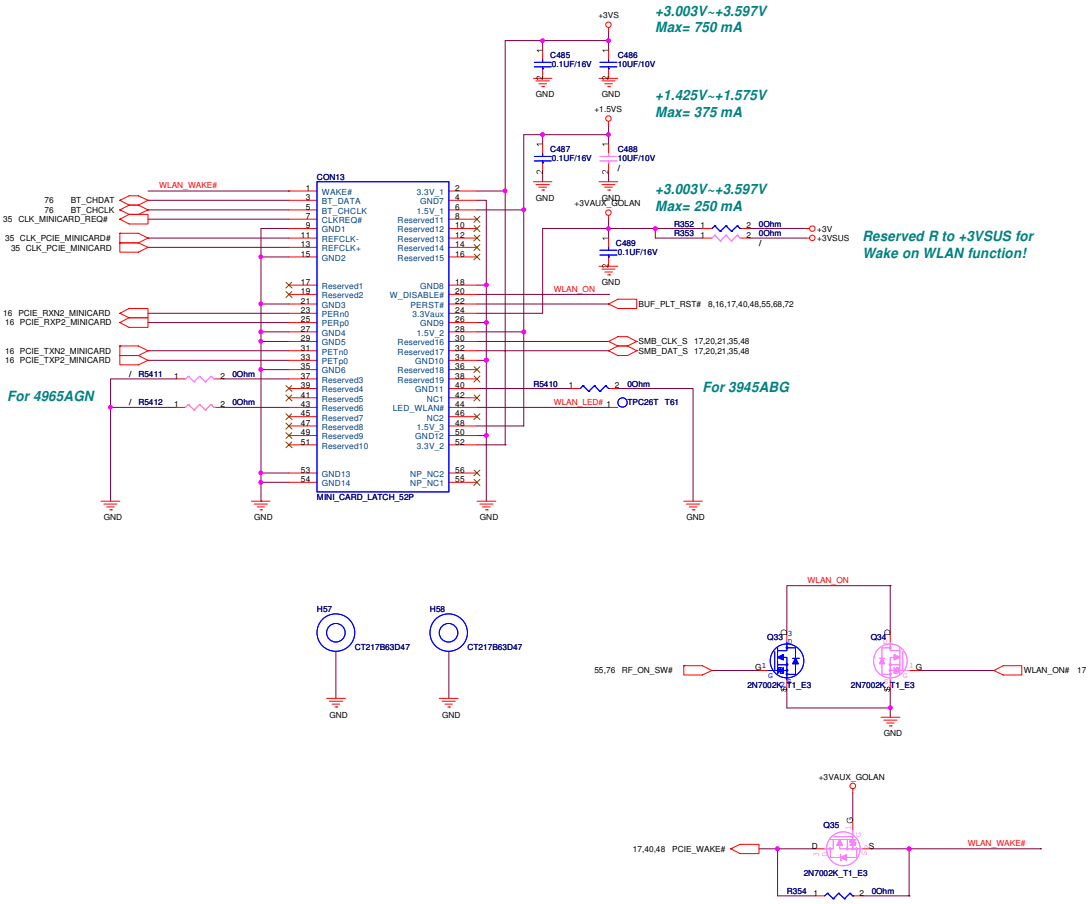
LAN CONN.





ASUSTeK COMPUTER INC. NB1	Title : MDC & RJ45+11		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二 十月 15, 2007		Sheet 41 of 89	





ASUSTeK COMPUTER INC. NB1	Title : MINICARD	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 43 of 89	

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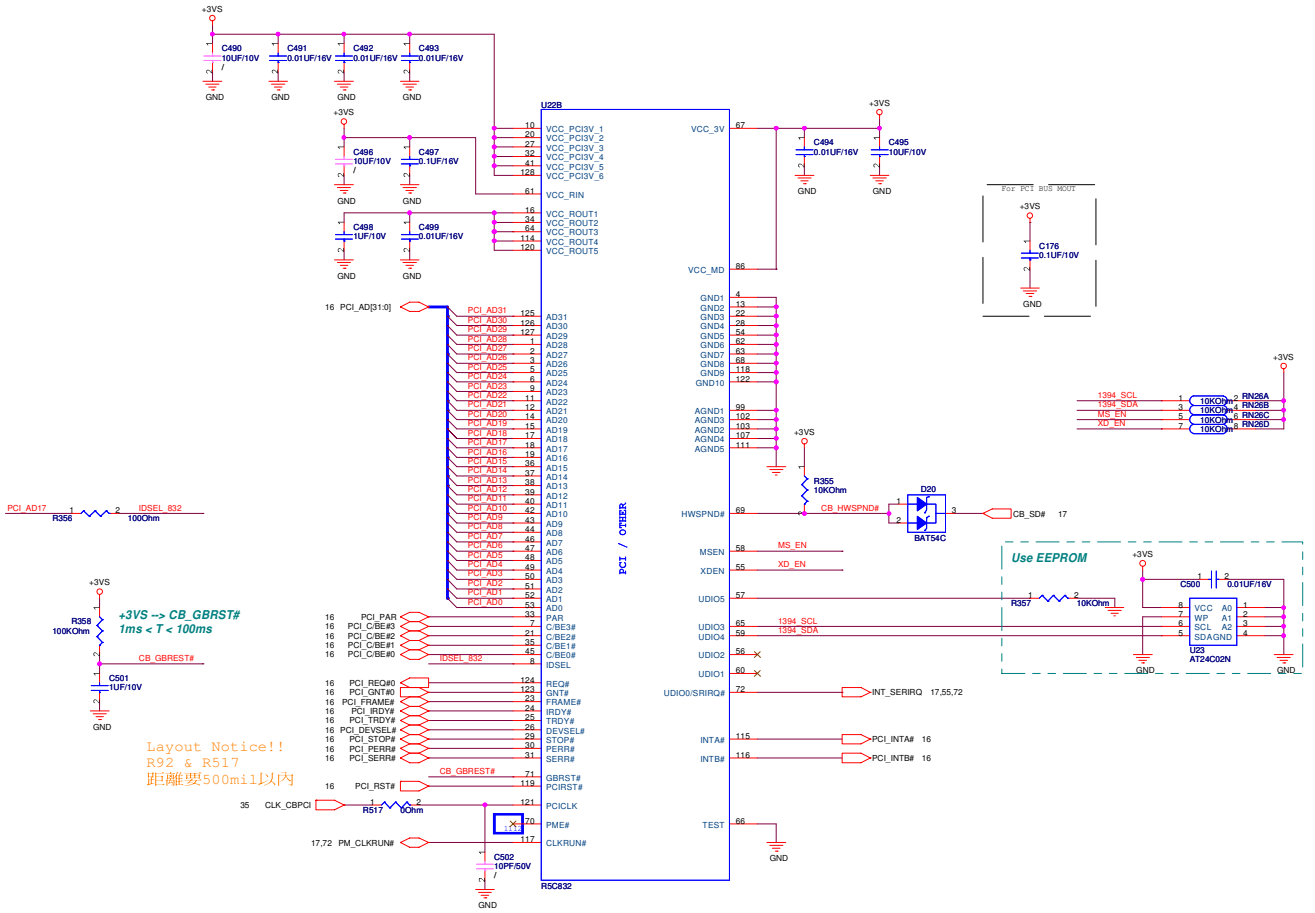
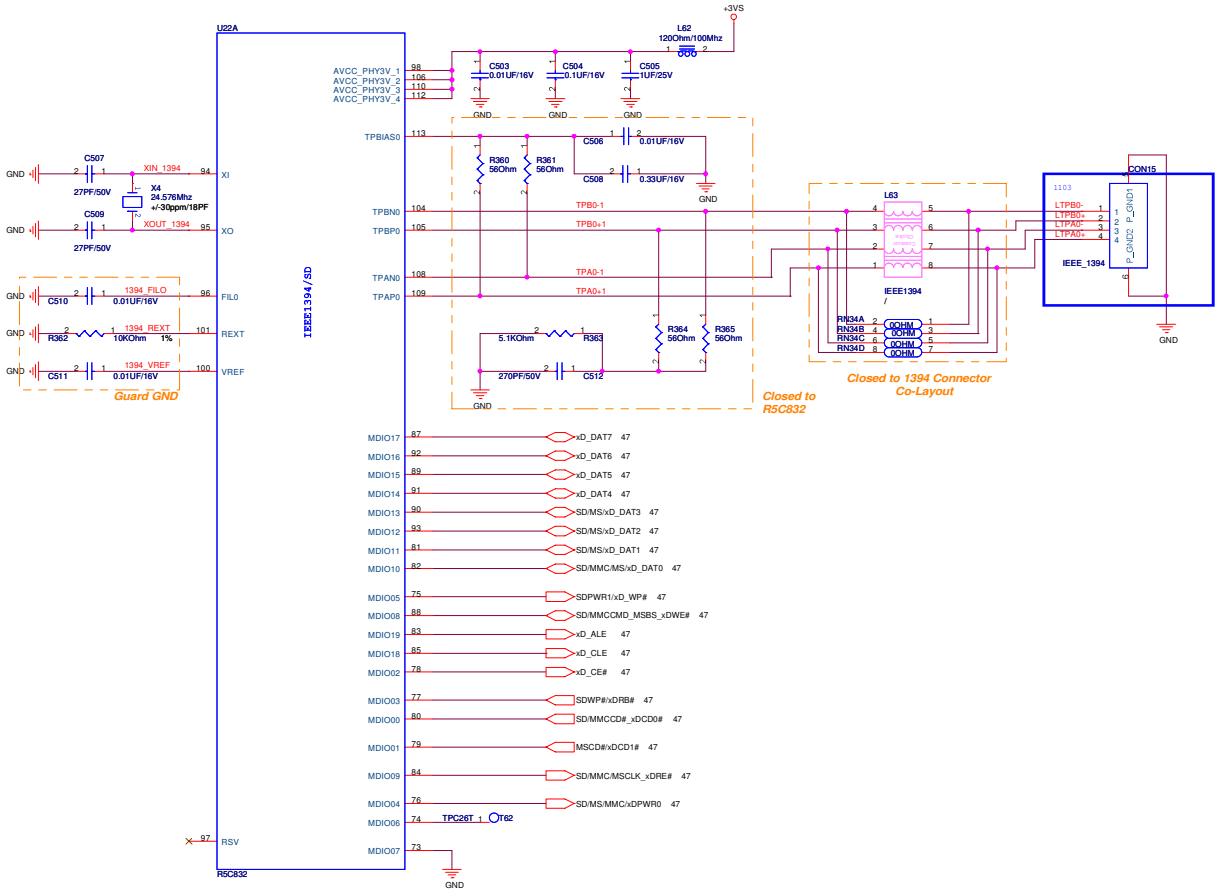
ASUSTeK COMPUTER INC	Title :		
	Engineer:	Ryan Wang	
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 44 of 89		



ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(1)		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二 六月 15, 2007	Sheet 45 of 89		

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC. NB1

Title : CARD1394-R5C832(2)

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 十月 15, 2007 Sheet 46 of 89

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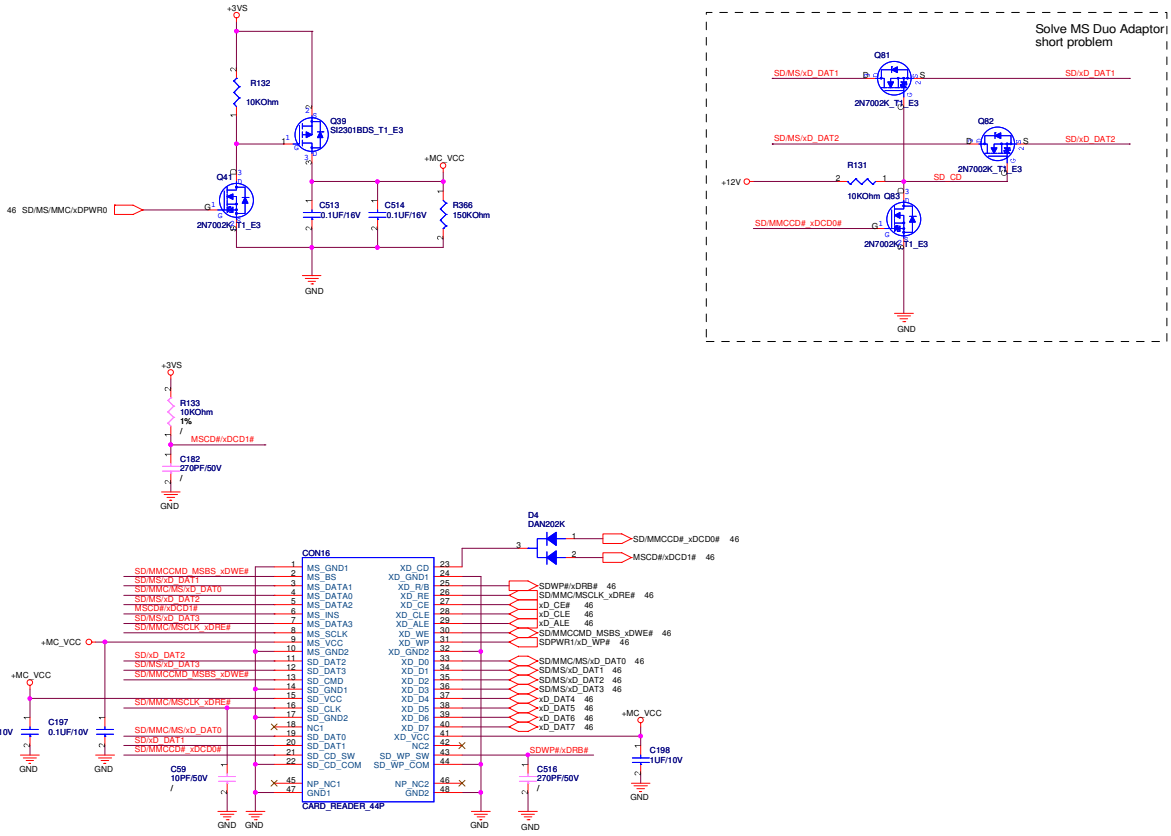
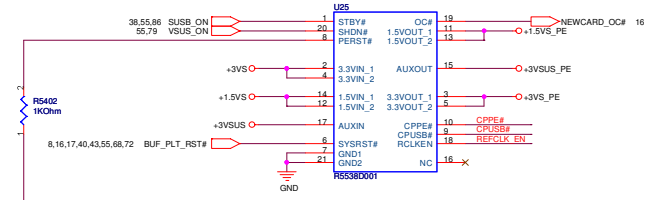
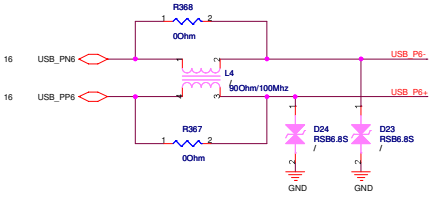
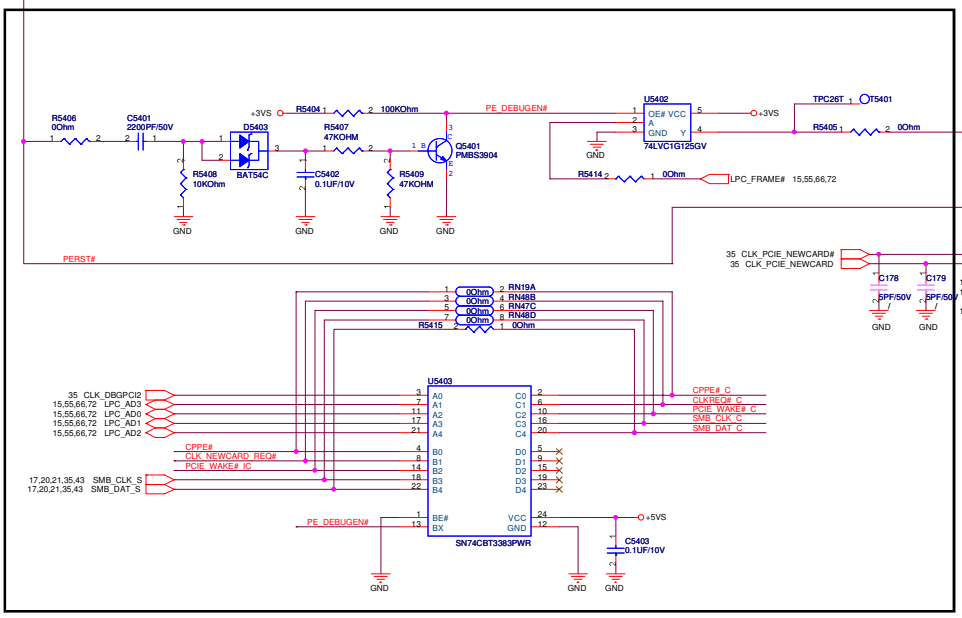


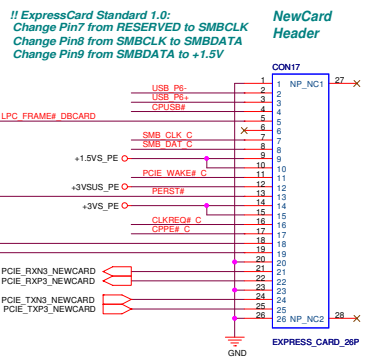
ASUSTeK COMPUTER INC	Title: 4 in 1 CARD READER		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 47 of 89		

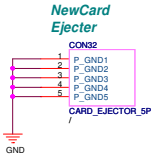
<< Kennedy_Zhang >>

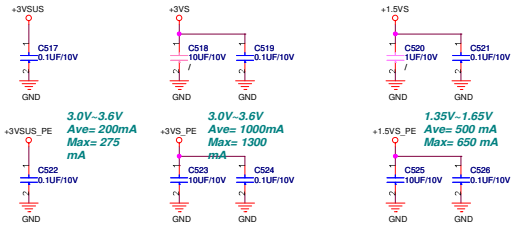


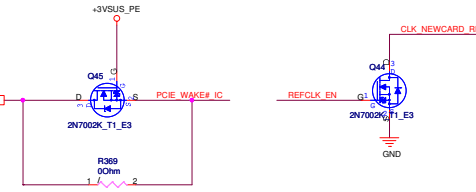


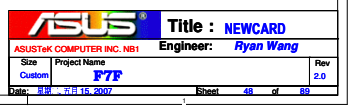


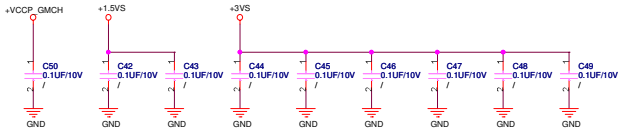


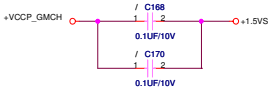


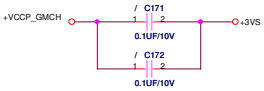












Title : PCMCIA SOCKET A

ASUSTeK COMPUTER INC

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 十月 15, 2007 Sheet 50 of 89

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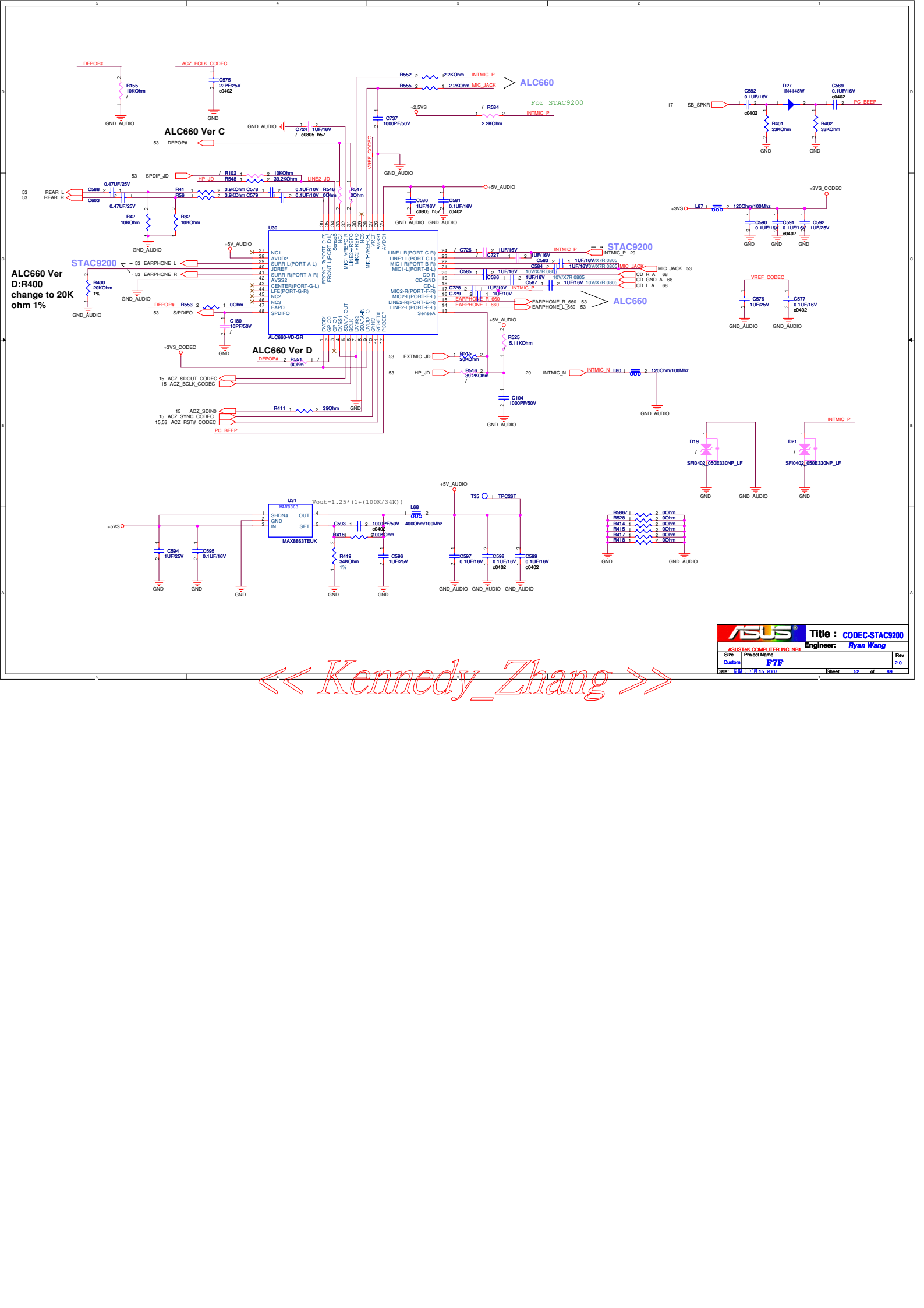
ASUSTeK COMPUTER INC	Title : F3J		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 51 of 89		


ALC660 Ver C
ALC660 Ver D
ALC660 Ver D:R400 change to 20K ohm 1%
STAC9200
ALC660
For STAC9200
U30
ALC660-VD-GR
U31
MAX8863
MAX8863TEUK
Vout=1.25*(1+(100K/34K))
Title : CODEC-STAC9200
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan Wang
Project Name FTF
Rev 2.0
Date: 星期 二 十月 15, 2007
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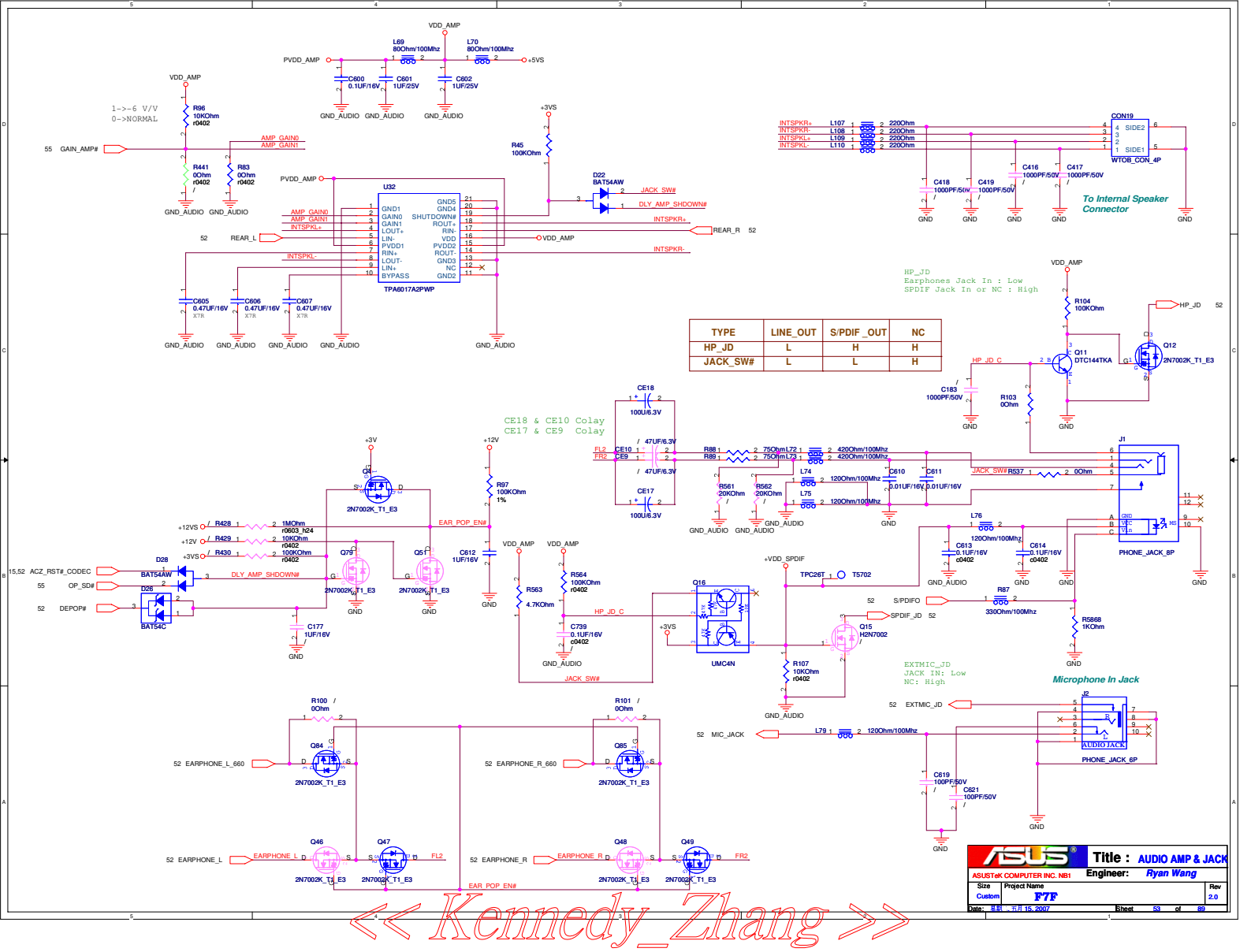
<< Kennedy_Zhang >>


VDD_AMP
PVDD_AMP
+5VS
+3VS
+12VS
+12V
+3V
GND_AUDIO
GAIN_AMP#
AMP_GAIN0
AMP_GAIN1
REAR_L
REAR_R
INTSPKL+
INTSPKL-
INTSPKR+
INTSPKR-
JACK_SW#
DLY_AMP_SHDOWN#
EAR_POP_EN#
HP_JD_C
SPDIF_JD
EXTMIC_JD
MIC_JACK
EARPHONE_L
EARPHONE_R
FL2
FR2
ACZ_RST#_CODEC
OP_SD#
DEPOP#
1->6 V/V
0->NORMAL
U32
TPA6017A2PWP
GAIN0
GAIN1
LOUT+
LIN-
PVDD1
RIN+
LOUT-
LIN+
BYPASS
SHUTDOWN#
ROUT+
RIN-
VDD
PVDD2
ROUT-
GND3
NC
GND2
GND1
GND4
GND5
CON19
WTOB_CON_4P
SIDE1
SIDE2
To Internal Speaker Connector
HP_JD
Earphones Jack In : Low
SPDIF Jack In or NC : High
TYPE
LINE_OUT
S/PDIF _OUT
NC
HP_JD
L
H
H
JACK_SW#
L
L
H
CE18 & CE10 Colay
CE17 & CE9 Colay
EXTMIC_JD
JACK IN: Low
NC: High
Microphone In Jack
PHONE_JACK_8P
PHONE_JACK_6P
AUDIO JACK
2N7002K_T1_E3
BAT54AW
BAT54C
UMC4N
TPC26T
T5702
H2N7002
DTC144TKA
R96 10KOhm r0402
R441 0Ohm r0402
R83 0Ohm r0402
R45 100KOhm
R97 100KOhm 1%
R104 100KOhm
R103 0Ohm
R428 1MOhm r0603_h24
R429 10KOhm r0402
R430 100KOhm r0402
R563 4.7KOhm
R564 100KOhm r0402
R107 10KOhm r0402
R87 330Ohm/100Mhz
R5868 1KOhm
R100 0Ohm
R101 0Ohm
L69 80Ohm/100Mhz
L70 80Ohm/100Mhz
L107 220Ohm
L108 220Ohm
L109 220Ohm
L110 220Ohm
L74 120Ohm/100Mhz
L75 120Ohm/100Mhz
L76 120Ohm/100Mhz
L79 120Ohm/100Mhz
R88 75OhmL72 420Ohm/100Mhz
R89 75OhmL73 420Ohm/100Mhz
C600 0.1UF/16V
C601 1UF/25V
C602 1UF/25V
C605 0.47UF/16V X7R
C606 0.47UF/16V X7R
C607 0.47UF/16V X7R
C418 1000PF/50V
C419 1000PF/50V
C416 1000PF/50V
C417 1000PF/50V
C183 1000PF/50V
C177 1UF/16V
C612 1UF/16V
C739 0.1UF/16V c0402
C610 0.01UF/16V
C611 0.01UF/16V
C613 0.1UF/16V c0402
C614 0.1UF/16V c0402
C619 100PF/50V
C621 100PF/50V
CE18 100U/6.3V
CE10 47UF/6.3V
CE9 47UF/6.3V
CE17 100U/6.3V
R561 20KOhm
R562 20KOhm
Q84
Q85
Q46
Q47
Q48
Q49
Q79
Q5
Q4
Q11
Q12
Q15
Q16
D22 BAT54AW
D28 BAT54AW
D26 BAT54C
J1
J2
Title : AUDIO AMP & JACK
ASUSTeK COMPUTER INC. NB1
Engineer: Ryan Wang
Size: Custom
Project Name: F7F
Rev: 2.0
Date: 年月 15, 2007
Sheet 53 of 89
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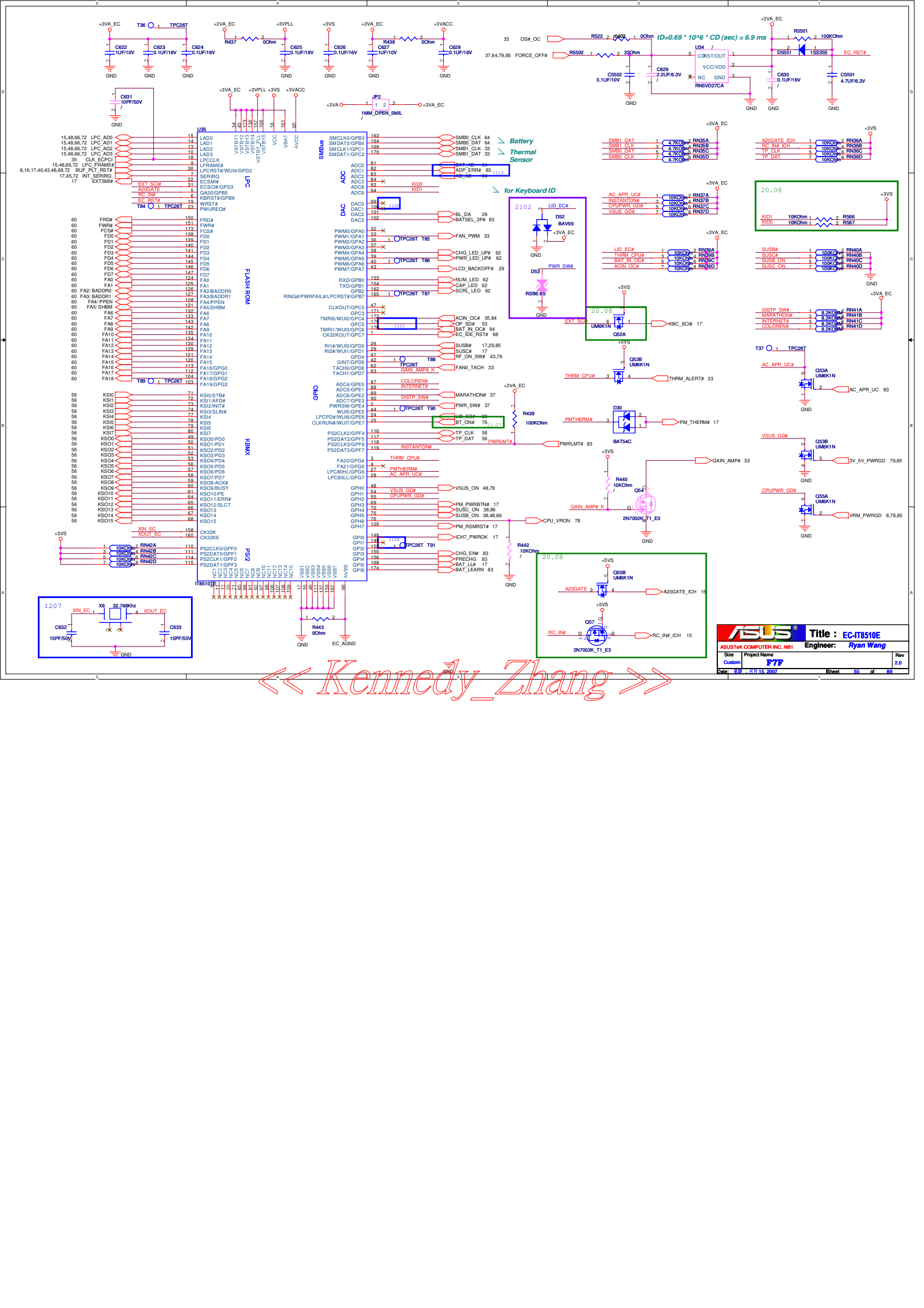
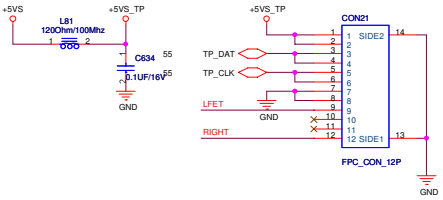
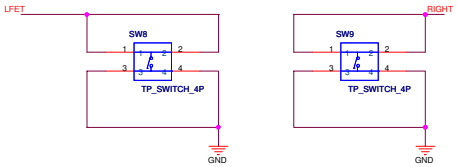
ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 54 of 89		

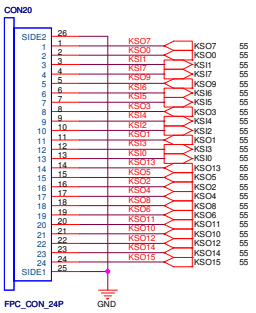

U35
IT8510E/F
KBMX
FLASH ROM
LPC
SMBus
ADC
DAC
GPIO
PS/2
Battery
Thermal Sensor
for Keyboard ID
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
ASUSTeK COMPUTER INC. NB1
Title : EC-IT8510E
Engineer: Ryan Wang
Project Name FTF
Rev 2.0
Sheet 55 of 89
Kennedy_Zhang

For Touch-Pad





For Keyboard(24Pin) None KID



ASUSTeK COMPUTER INC. NB1

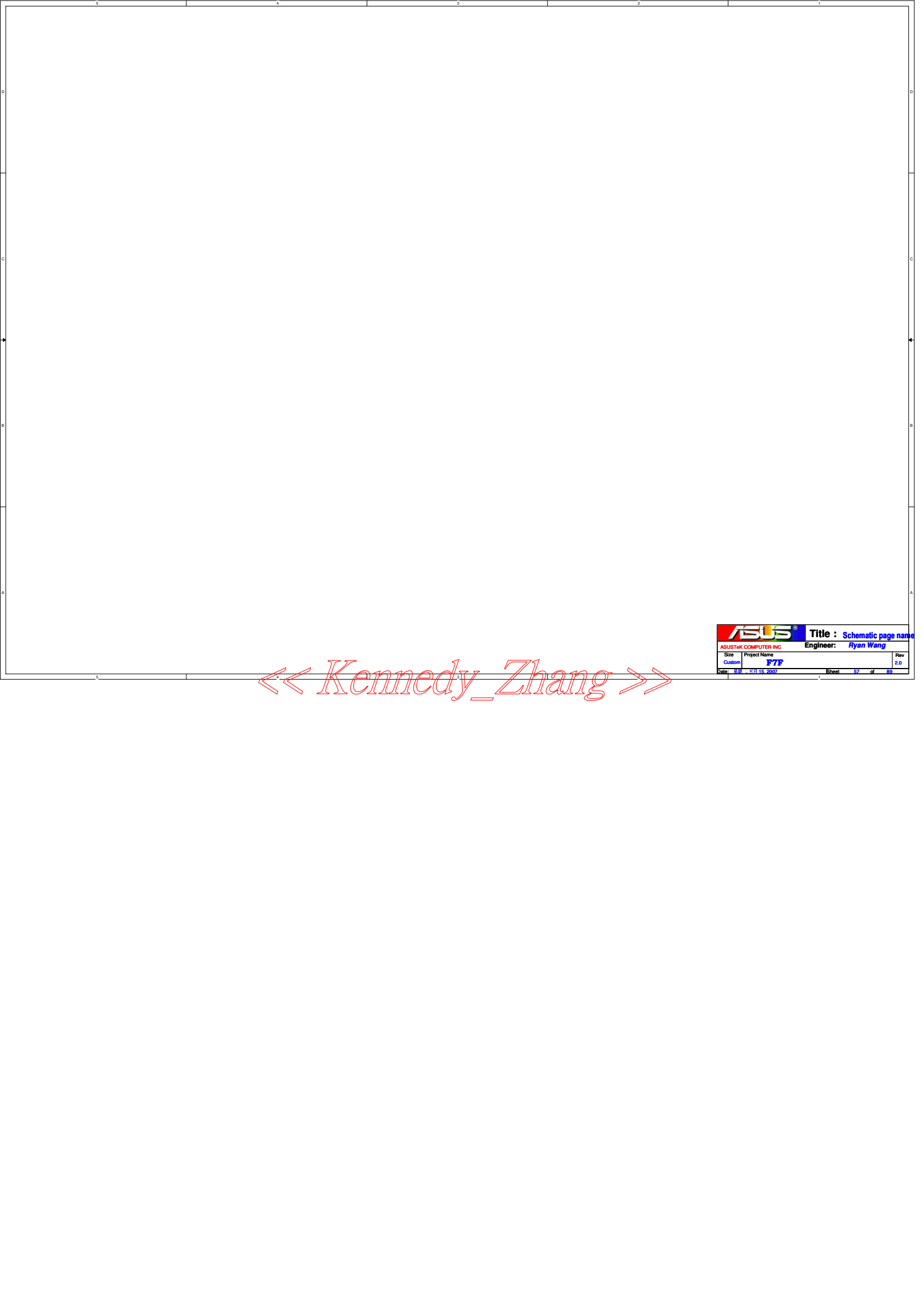
Title : Touch Pad & KB

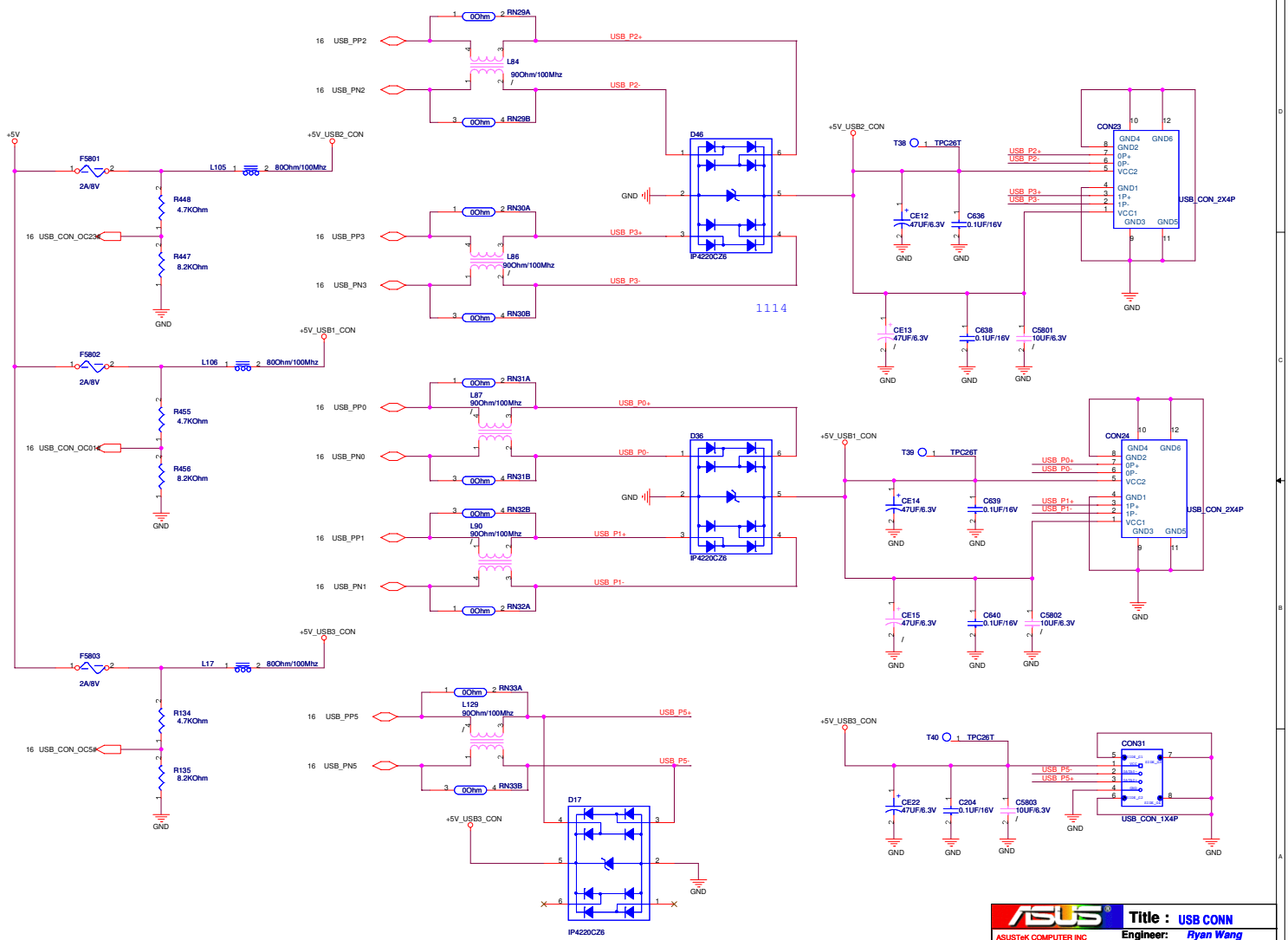
Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二 十月 15, 2007 Sheet 56 of 89

<< Kennedy_Zhang >>





ASUSTeK COMPUTER INC

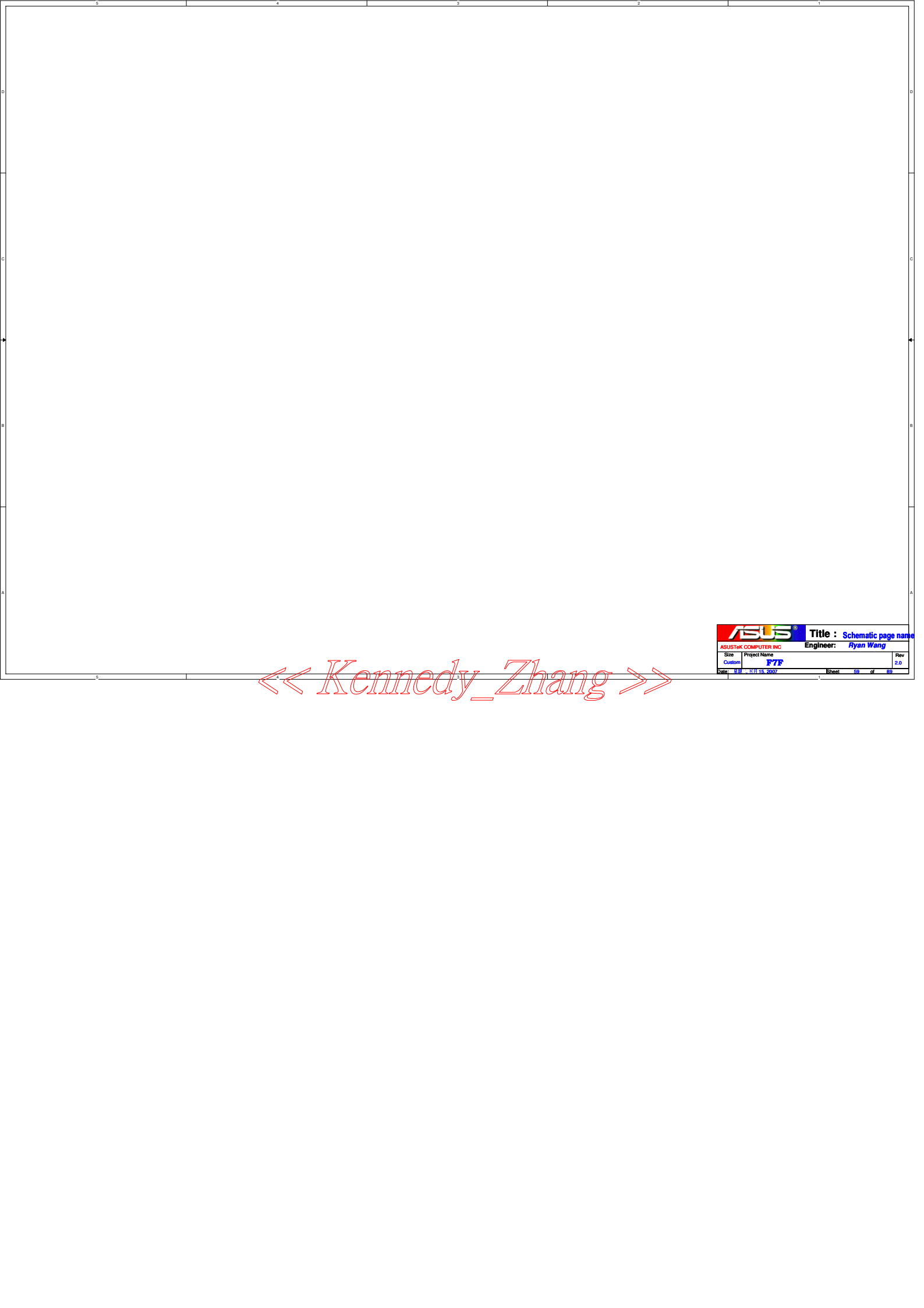
Title : USB CONN

Engineer: Ryan Wang

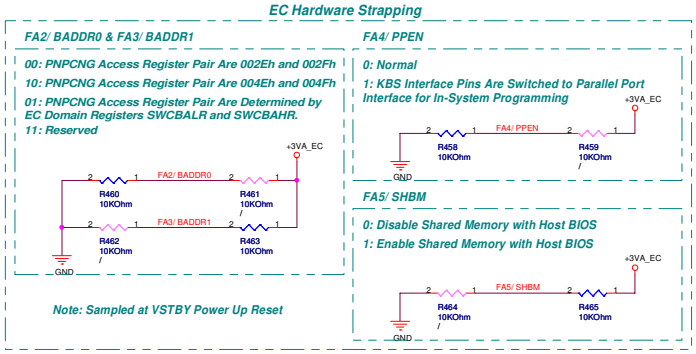
Size	Project Name	Rev
Custom	FTF	2.0

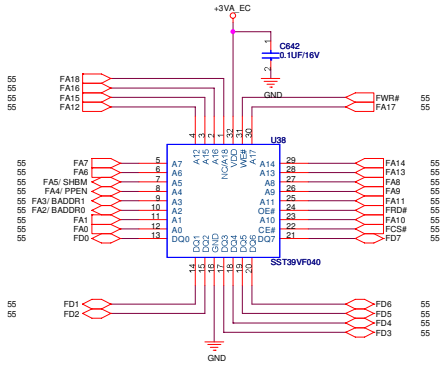
Date: 星期 二 十月 15, 2007 Sheet 58 of 89

<< Kennedy_Zhang >>



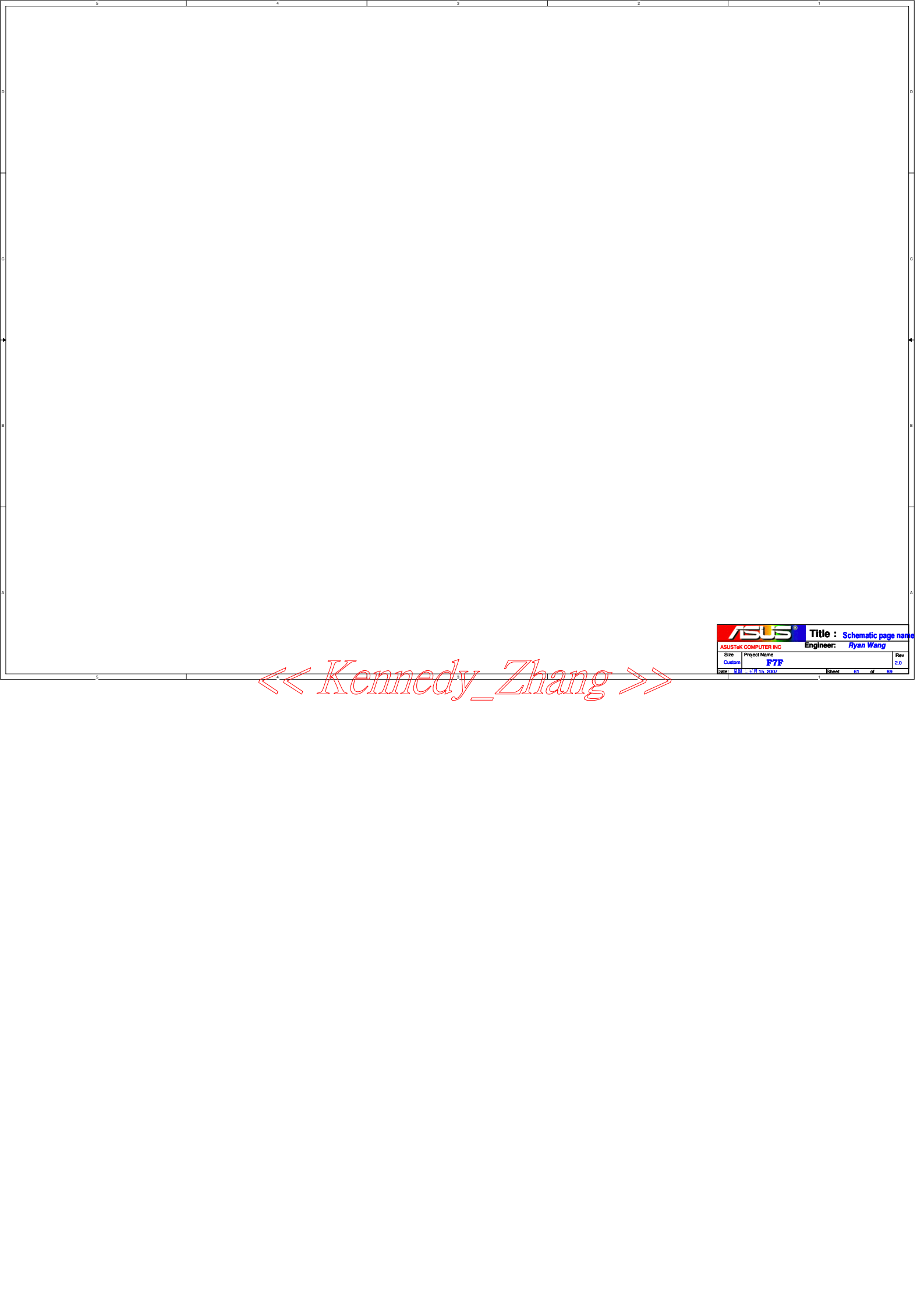
ISA ROM





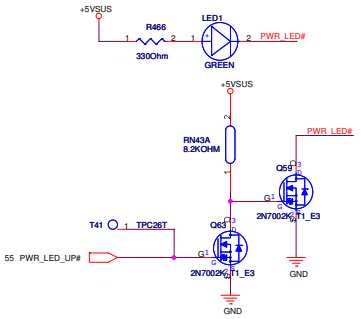
ASUSTeK COMPUTER INC. NB1	Title : ISA ROM		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007		Sheet 60 of 89	

<< Kennedy_Zhang >>



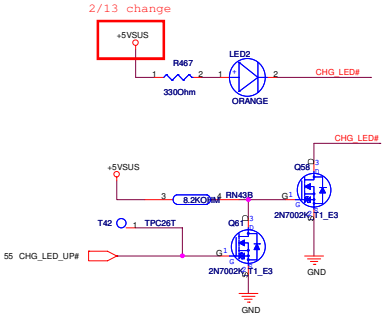
For LED

For POWER LED

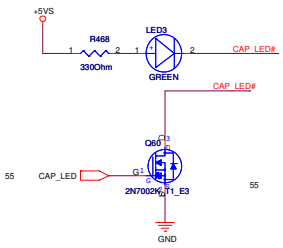


For BATTERY LED

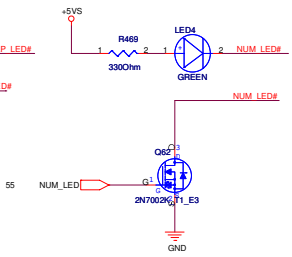
2/13 change



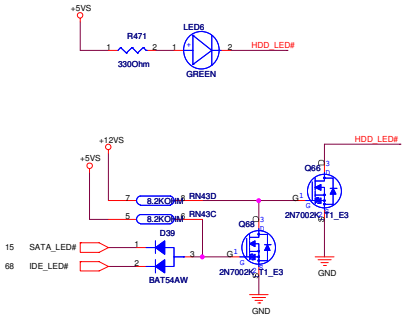
for Cap. Lock



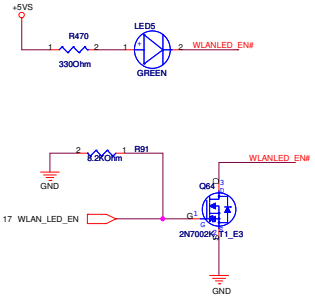
for Num Lock



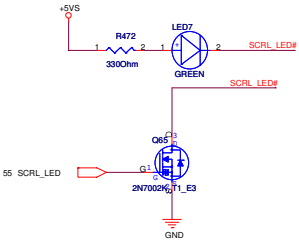
For SATA/IDE LED



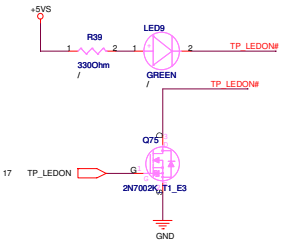
For WireLess LED



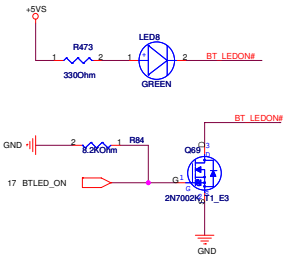
for Scroll Lock



for Touch Pad

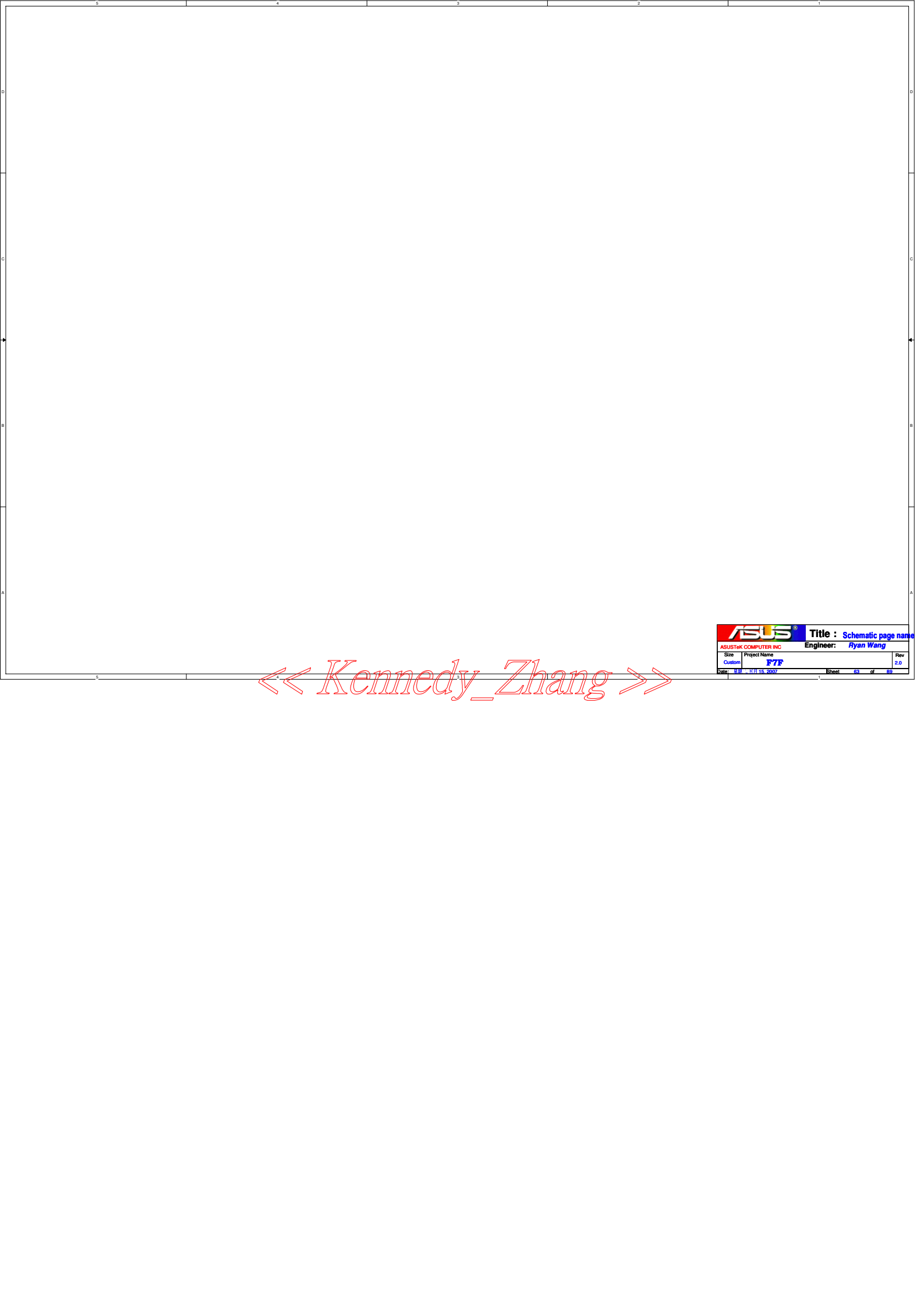


For BT LED

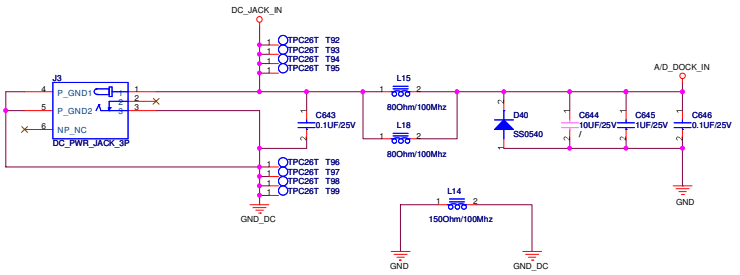


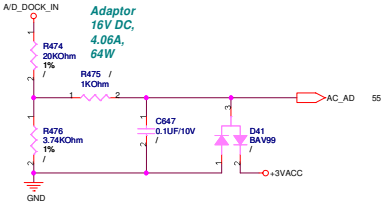
ASUSTeK COMPUTER INC	Title : LED	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 62 of 89	

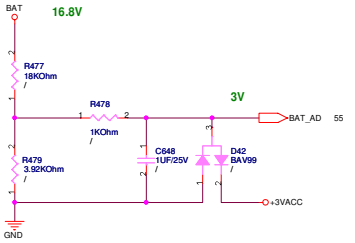
<< Kennedy_Zhang >>



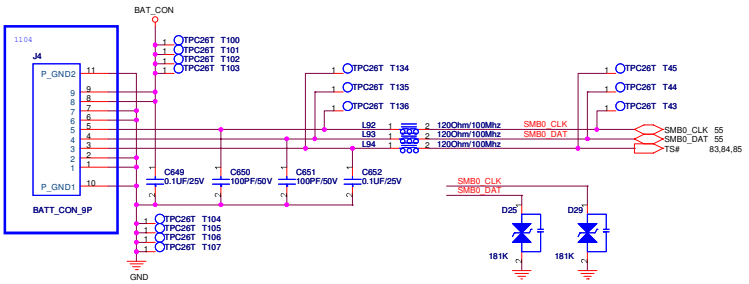
DC IN



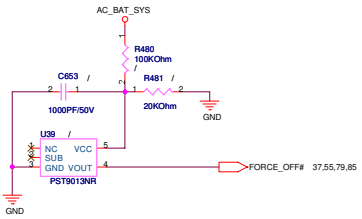




BAT IN

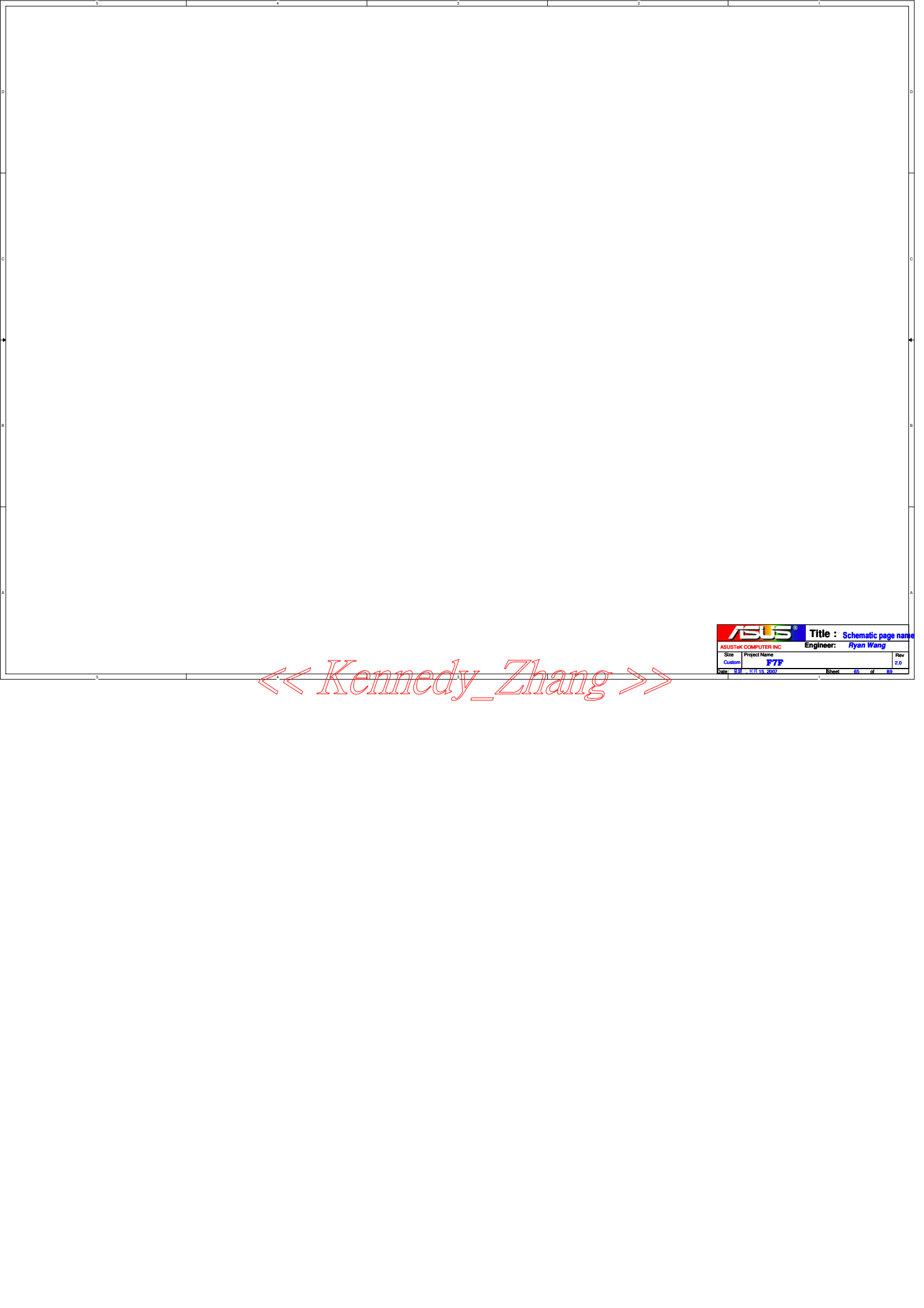


Without Battery & Pull out Adapter

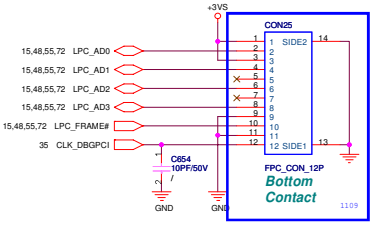


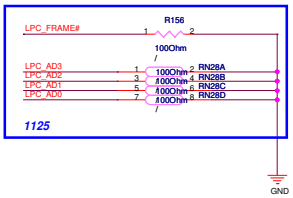
ASUSTeK COMPUTER INC. NB1	Title : DC & BAT IN		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 64 of 89		

<< Kennedy_Zhang >>



For Debug





ASUSTeK COMPUTER INC	Title : Debug CONN.	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二 十月 15, 2007	Sheet 66 of 89	

Title : Schematic page name

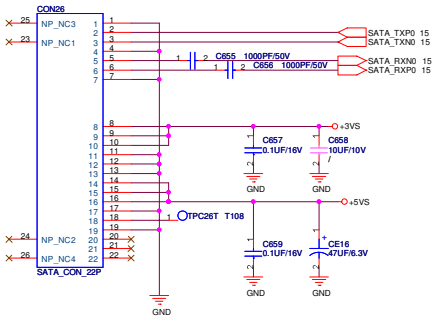
ASUSTeK COMPUTER INC

Engineer: Ryan Wang

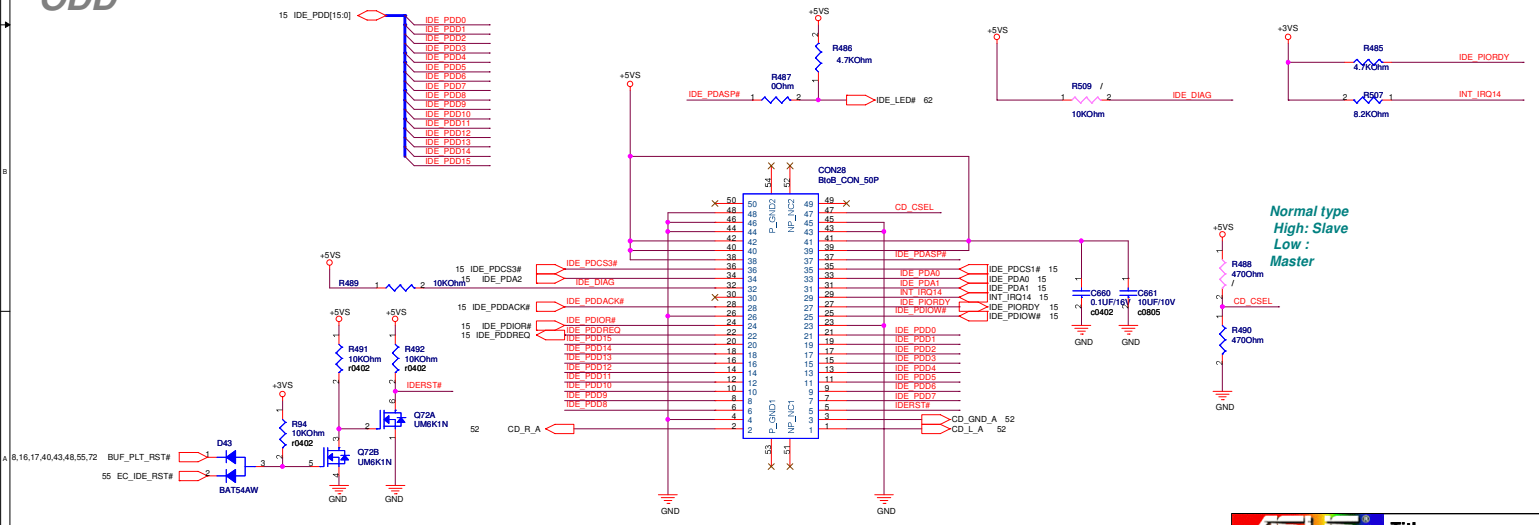
Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 十月 15, 2007 Sheet 67 of 89

SATA HDD



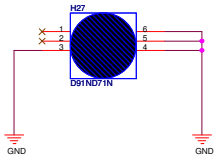
ODD



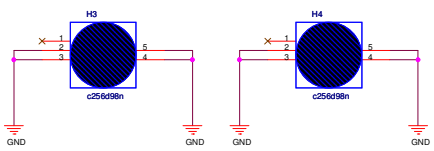
ASUSTeK COMPUTER INC. NB1	Title : HDD & ODD		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 68 of 89		

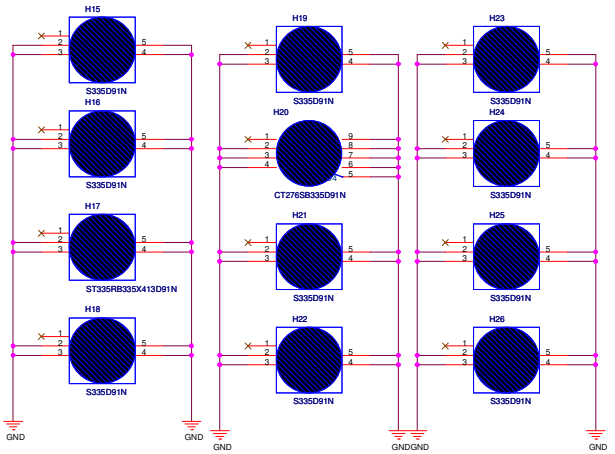
ASUSTeK COMPUTER INC	Title : Schematic page name		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 69 of 89		

FOR LEFT UNDER

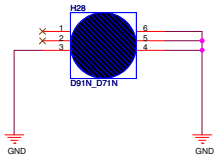


FOR FAN

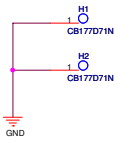




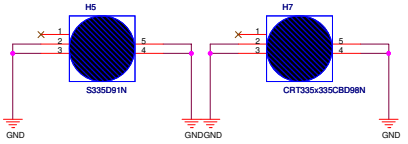
FOR RIGHT UP



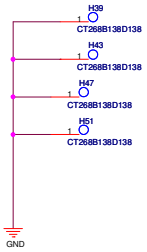
FOR FAN



FOR SCREW HOLE

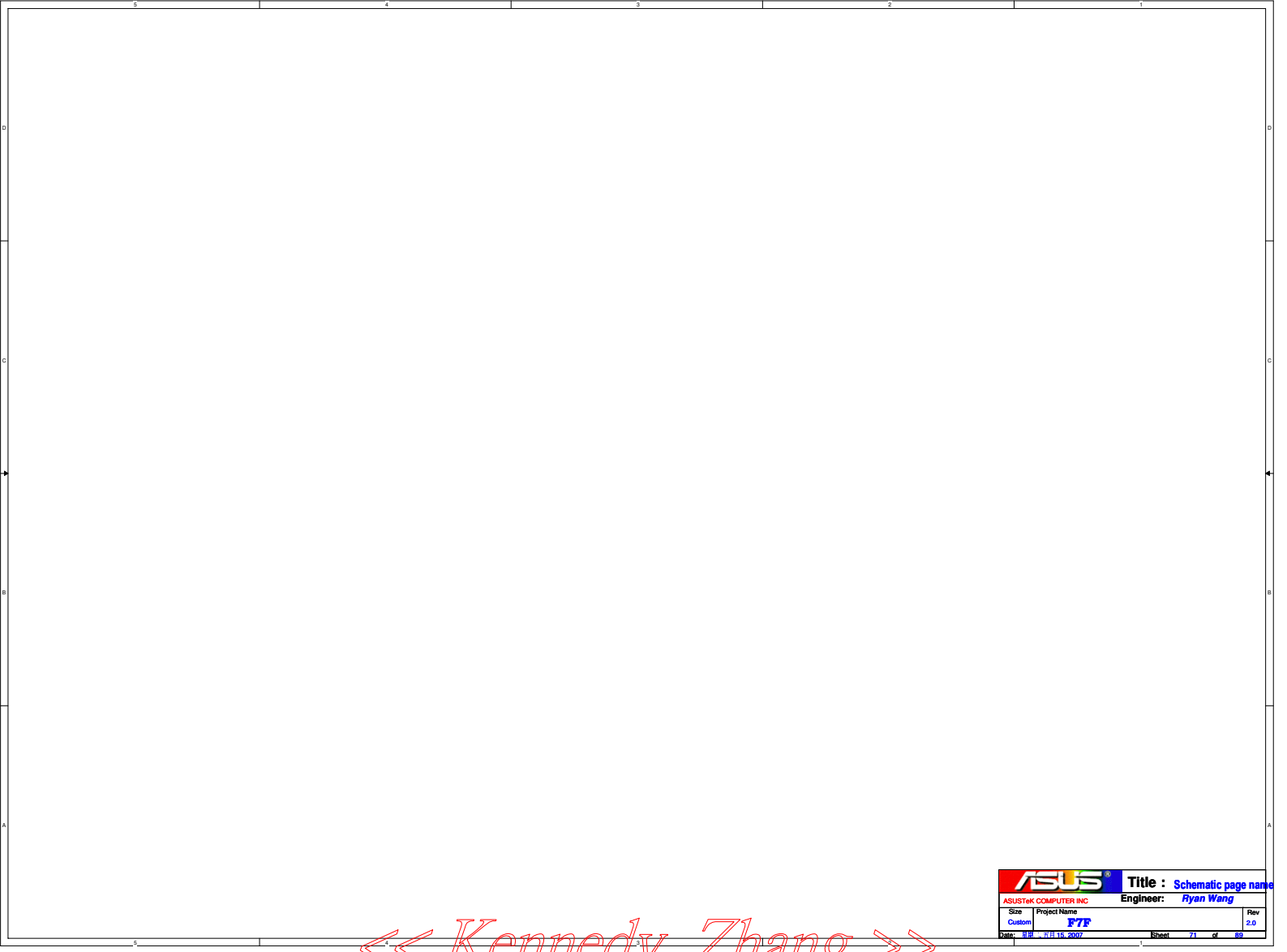


FOR CPU



ASUSTeK COMPUTER INC	Title : SREW HOLE		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 70 of 89		

<< Kennedy_Zhang >>



Title : Schematic page name

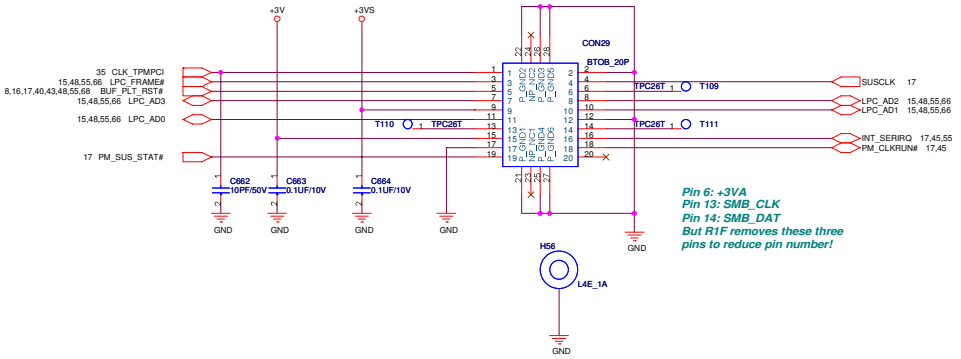
ASUSTeK COMPUTER INC

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

Date: 星期 二, 十月 15, 2007 Sheet 71 of 89

For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

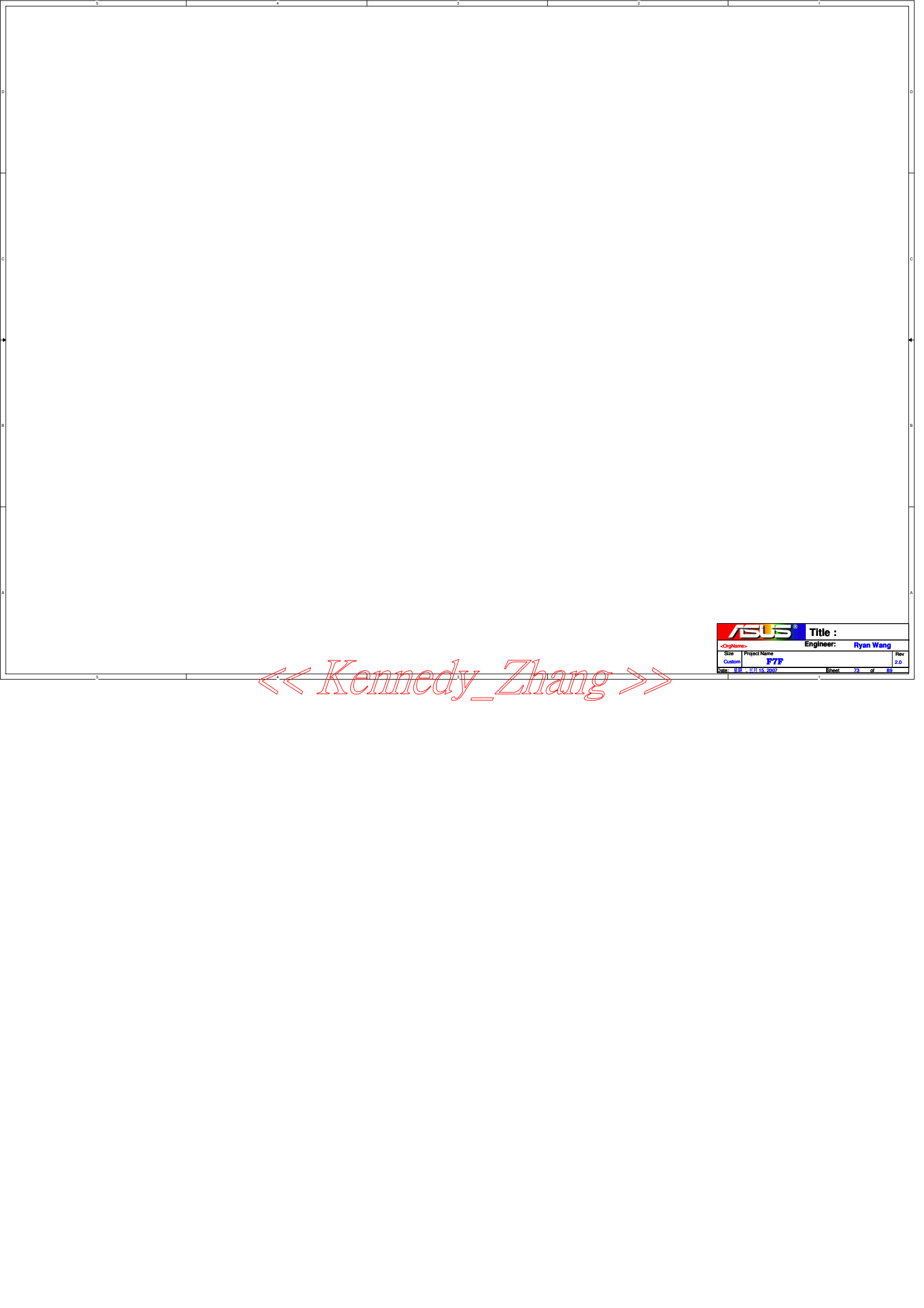
ASUSTeK COMPUTER INC

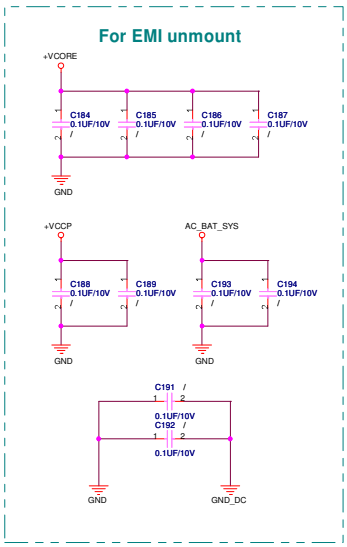
Title : TPM

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	2.0

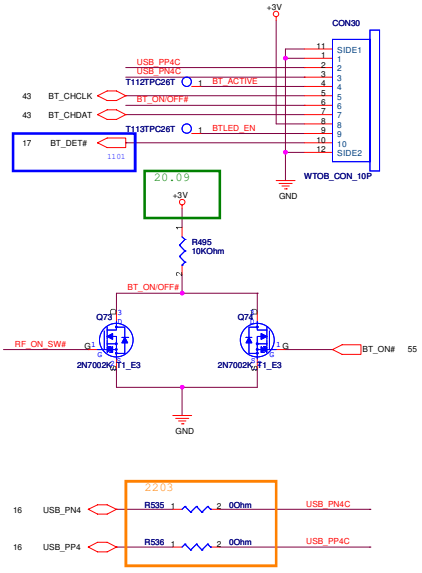
Date: 星期 二 十月 15, 2007 Sheet 72 of 89


Title :
Engineer: Ryan Wang
<OrgName>
Size
Custom
Project Name
F7F
Rev
2.0
Date: 星期 一, 五月 15, 2007
Sheet 73 of 89
<< Kennedy_Zhang >>

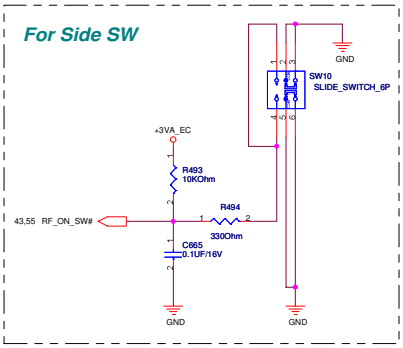


ASUSTeK COMPUTER INC	Title : EMI	
	Engineer: Ryan Wang	
Size: Custom	Project Name: FTF	Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 74 of 89	

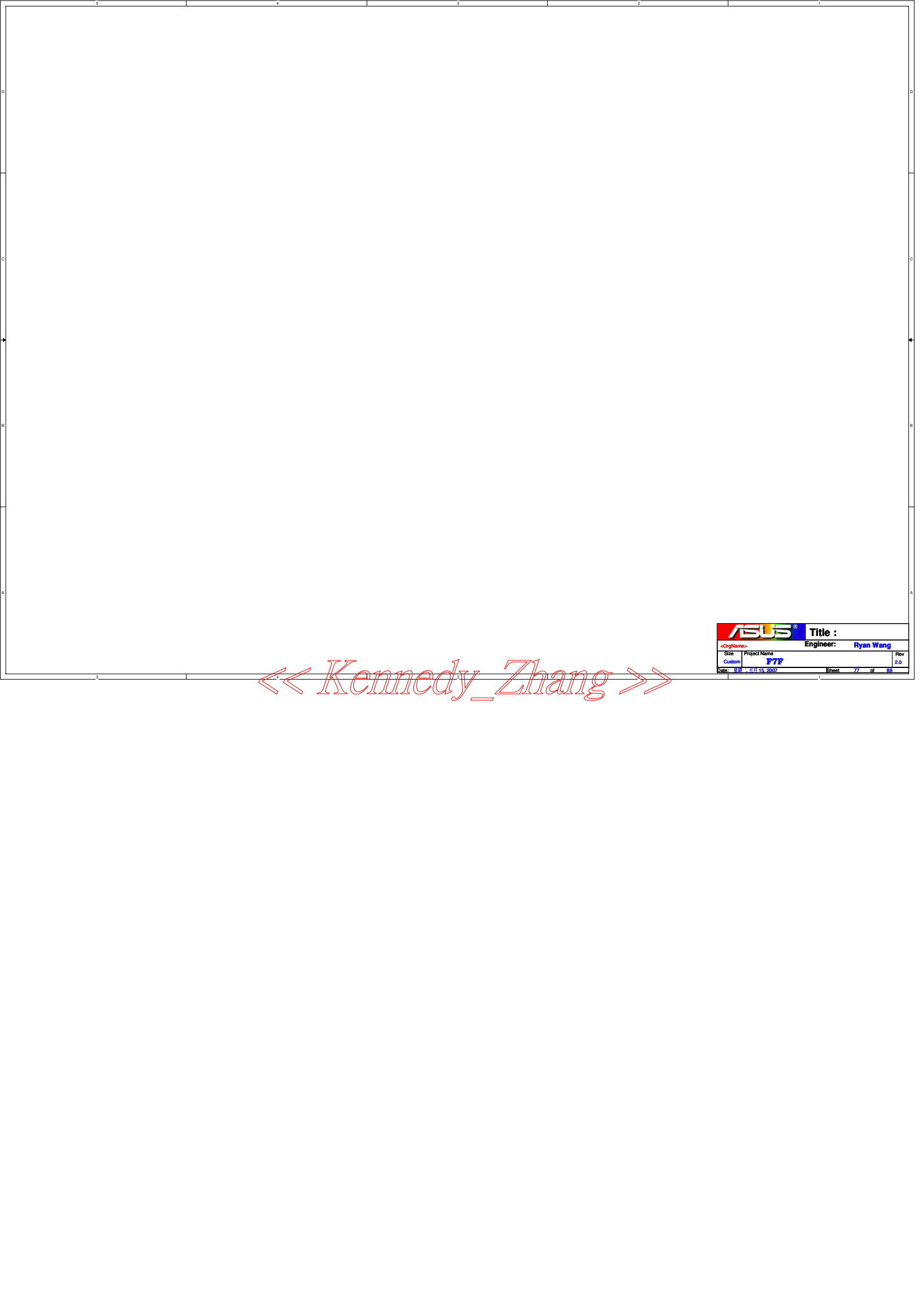
For Bluetooth



For Side SW



ASUSTeK COMPUTER INC	Title : Blue Tooth		
	Engineer: Ryan Wang		
Size: Custom	Project Name: FTF		Rev: 2.0
Date: 星期 二, 十月 15, 2007	Sheet 76 of 89		


Title :
Engineer: Ryan Wang
<OrgName>
Size
Custom
Project Name
F7F
Rev
2.0
Date: 星期 一, 五月 15, 2007
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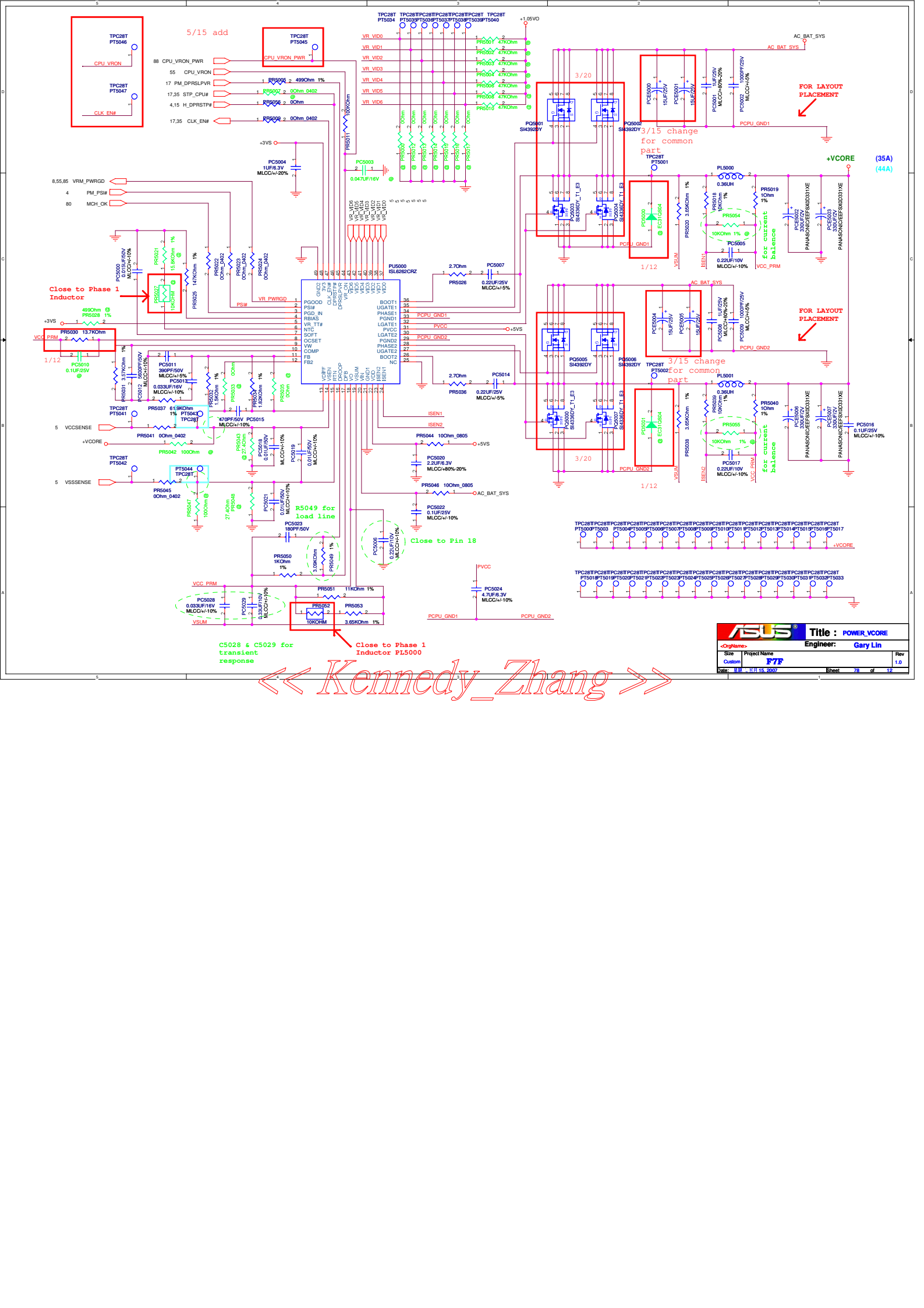
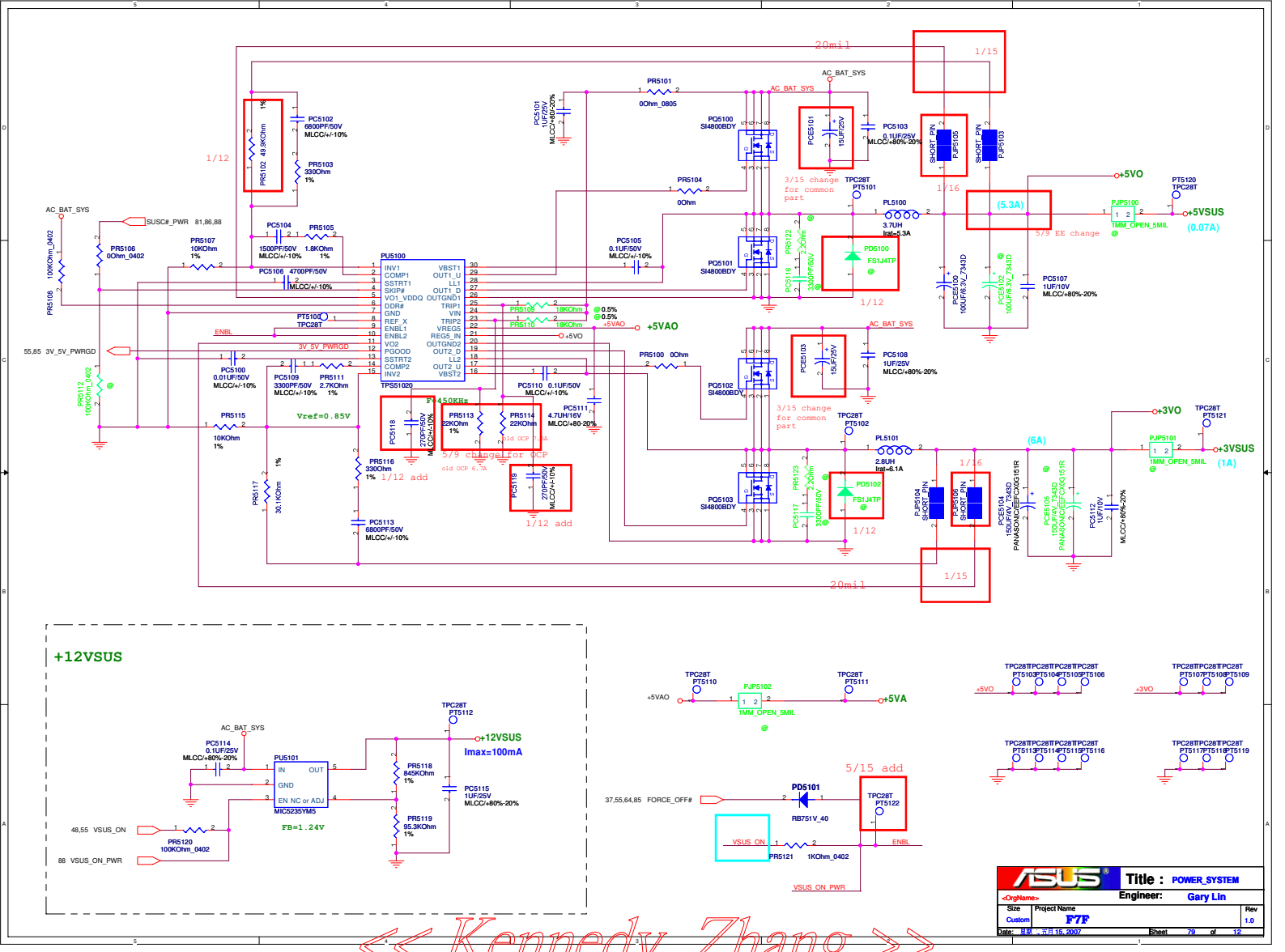
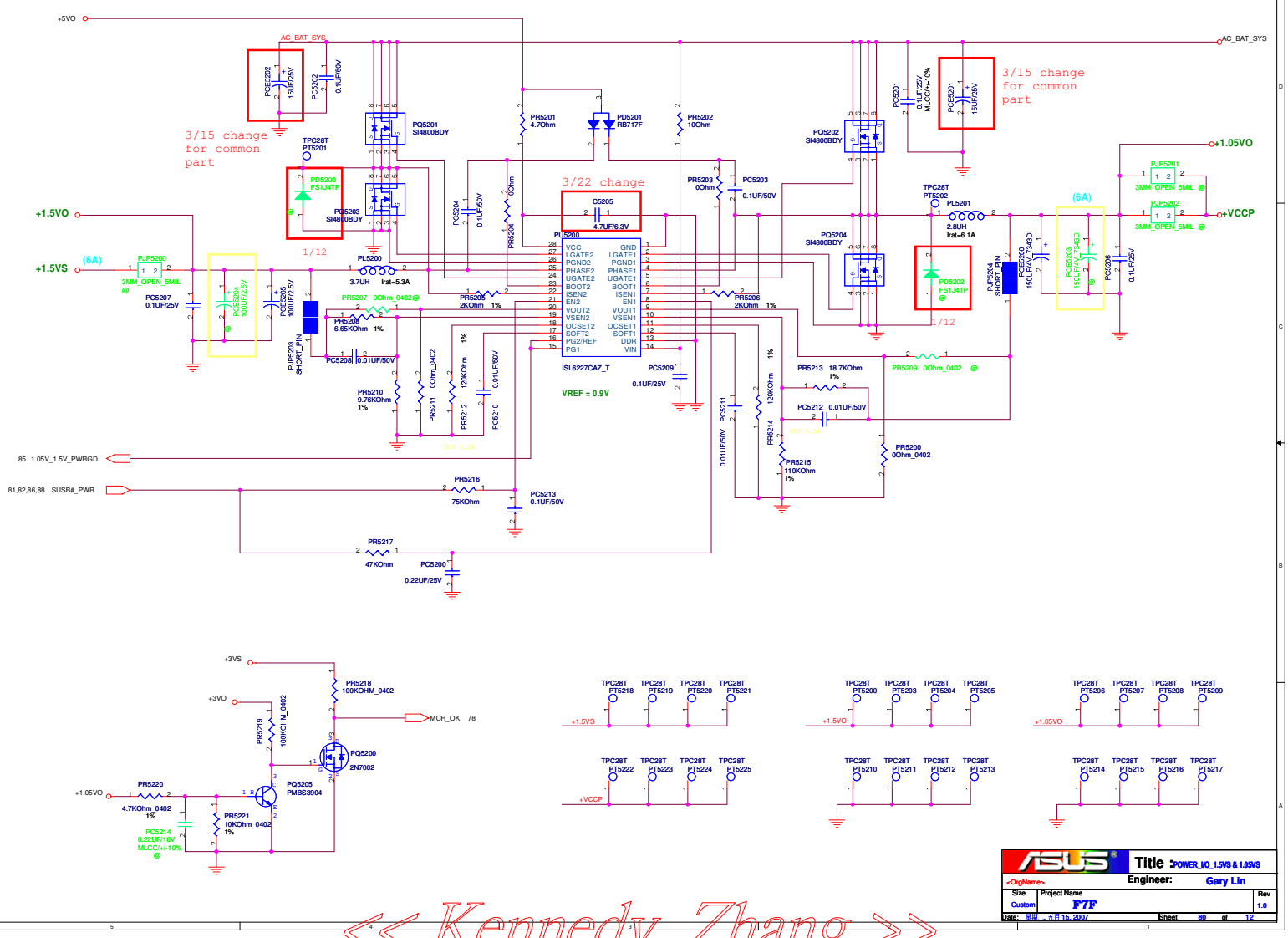
<< Kennedy_Zhang >>


5/15 add
CPU_VRON_PWR
CPU_VRON
PM_DPRSLPVR
STP_CPU#
H_DPRSTP#
CLK_EN#
+3VS
VRM_PWRGD
PM_PSI#
MCH_OK
Close to Phase 1 Inductor
PSI#
VR_PWRGD
VCC_PRM
VCCSENSE
VSSSENSE
+VCORE
R5049 for load line
Close to Pin 18
Close to Phase 1 Inductor PL5000
C5028 & C5029 for transient response
3/15 change for common part
FOR LAYOUT PLACEMENT
for current balance
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
PVCC
+5VS
+1.05VO
VSUM
ISEN1
ISEN2
+VCORE (35A)
(44A)
Title : POWER_VCORE
Engineer: Gary Lin
Project Name F7F
Rev 1.0
Sheet 78 of 12
Date: 星期 一 五月 15, 2007
<< Kennedy_Zhang >>



Title :	POWER_SYSTEM		
Engineer:	Gary Lin		
<OrgName>			
Size: Custom	Project Name: F7F		Rev: 1.0
Date: 星期一 十月 15, 2007		Sheet 79 of 12	

<< Kennedy_Zhang >>



Title :POWER_I/O_1.5VS & 1.05VS

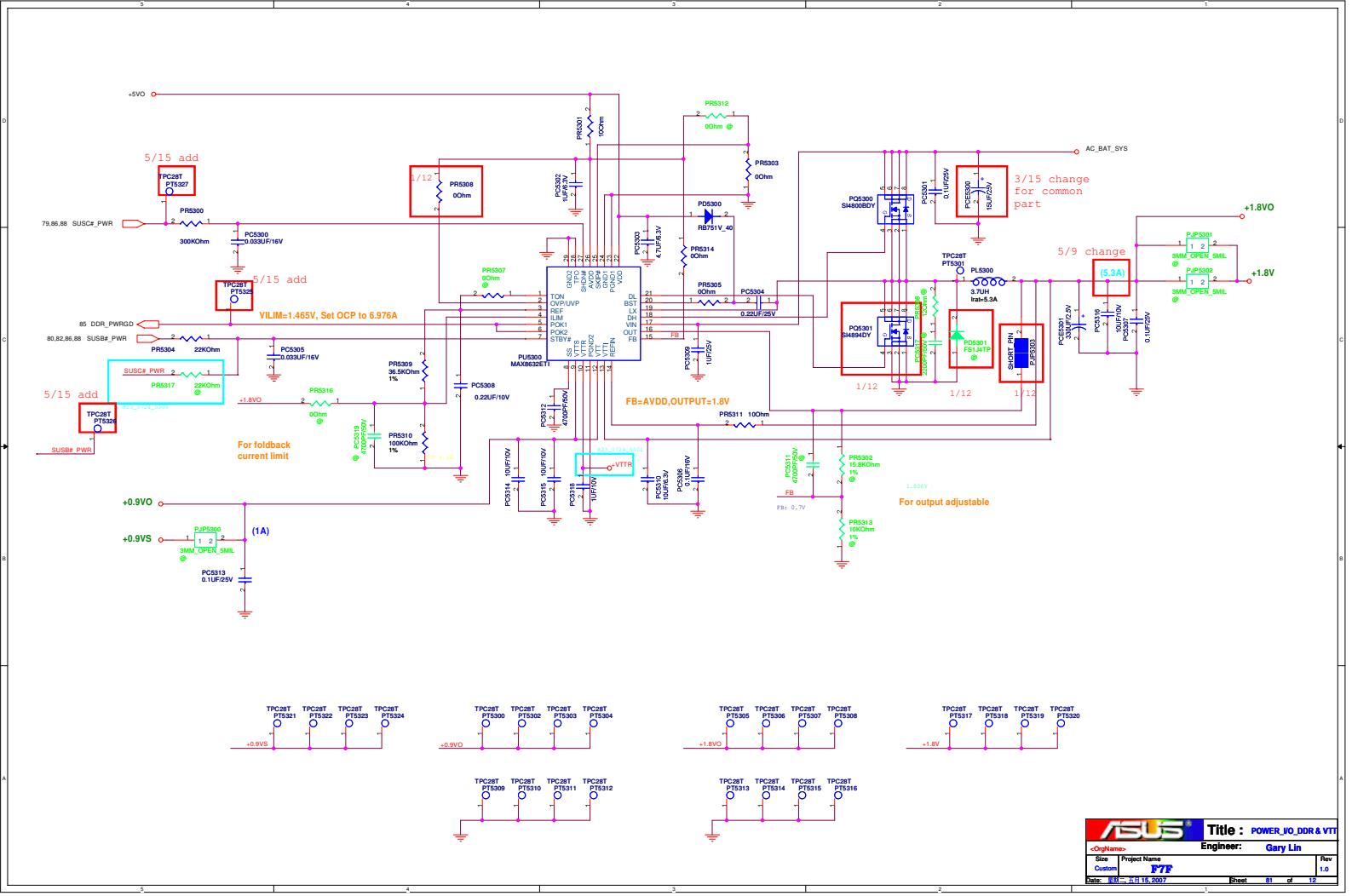
<OrgName>

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F7F	1.0

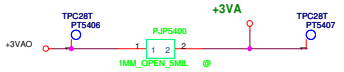
Date: 星期 一 五月 15, 2007 Sheet 80 of 12

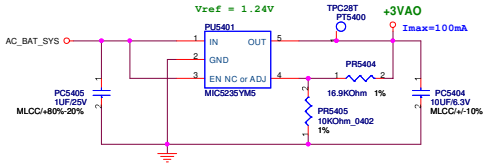
<< Kennedy_Zhang >>



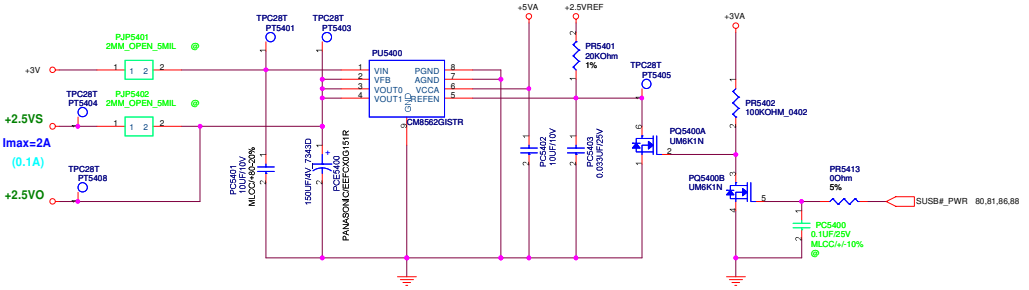
<< Kennedy_Zhang >>

+3VAO



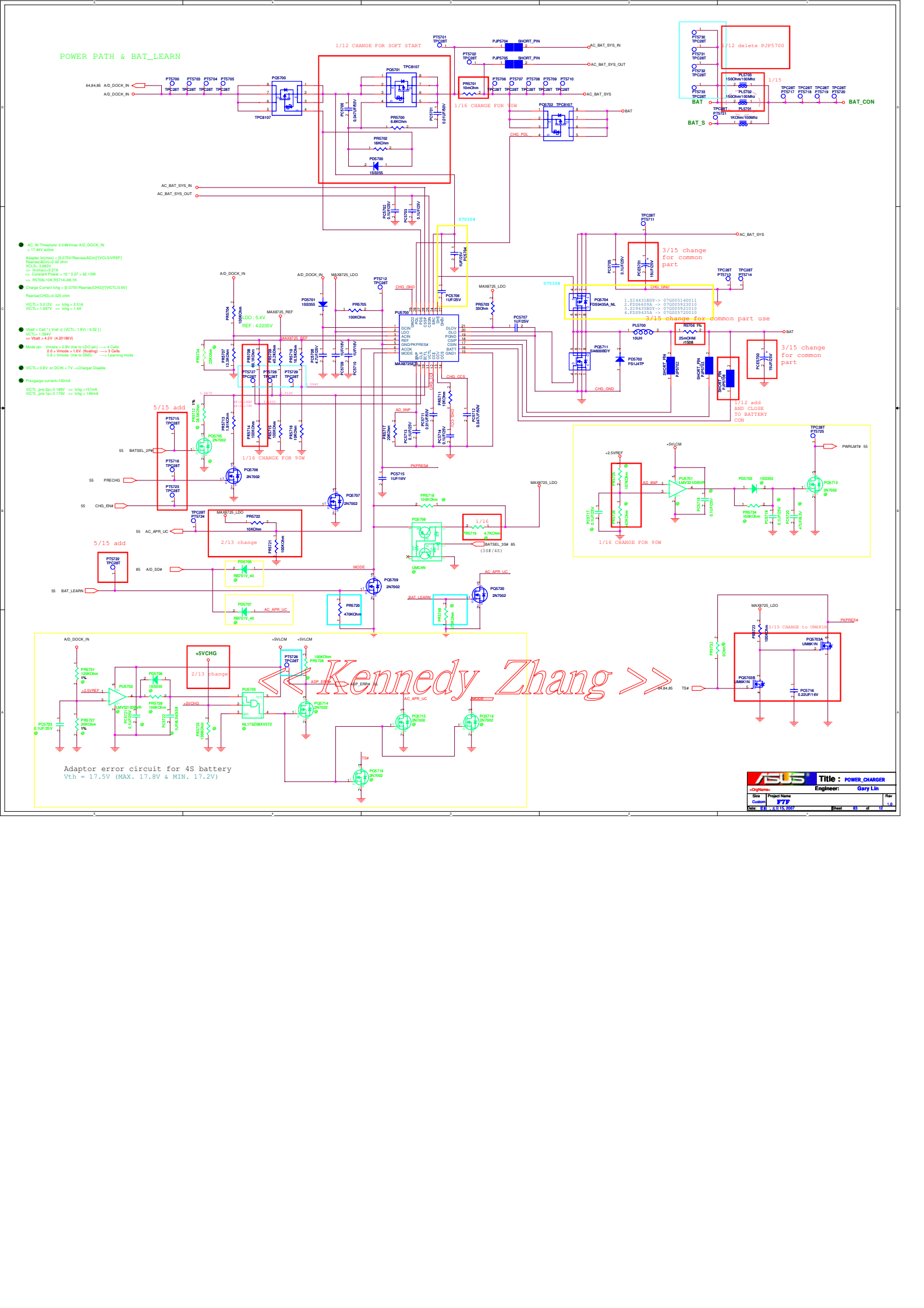


+2.5VS

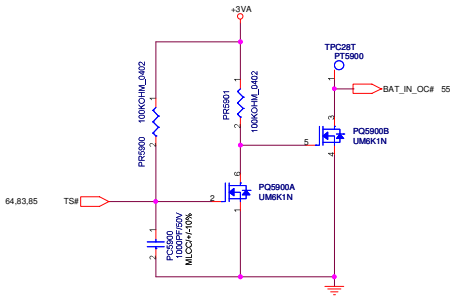


ASUS	Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer: Gary Lin		
Size: Custom	Project Name: F7F		Rev: 1.0
Date: 星期 一, 五月 15, 2007	Sheet 82 of 12		

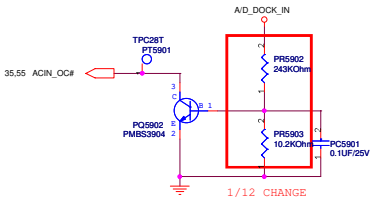
<< Kennedy_Zhang >>


POWER PATH & BAT_LEARN
1/12 CHANGE FOR SOFT START
1/16 CHANGE FOR 90W
1/12 delete PJP5700
3/15 change for common part
3/15 change for common part use
1/12 add AND CLOSE TO BATTERY CON
5/15 add
2/13 change
1/16 CHANGE FOR 90W
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R5708=10K,R5714=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.012V => Ichg = 2.51A
VICTL= 1.687V => Ichg = 1.4A
Vbatt = Cell * [Vref +[(VCTL- 1.8V) / 9.52]]
VCTL= 1.584V
=> Vbatt = 4.2V (4.20186V)
Mode pin : Vmode > 2.8V (Hiz to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (tie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V ->Charger Disable
Precgarge current=150mA
VICTL_pre-2p= 0.188V => Ichg =157mA
VICTL_pre-1p= 0.179V => Ichg = 149mA
LDO : 5.4V
REF : 4.2235V
Adaptor error circuit for 4S battery
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)
<<Kennedy Zhang>>
Title : POWER_CHARGER
Engineer: Gary Lin
Project Name: FTF
Rev: 1.0
Sheet 85 of 12

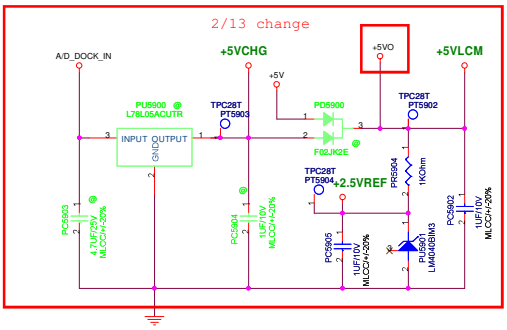
BATTERY IN DETECT

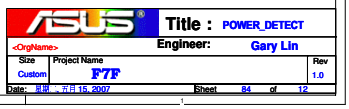


ADAPTER IN DETECT

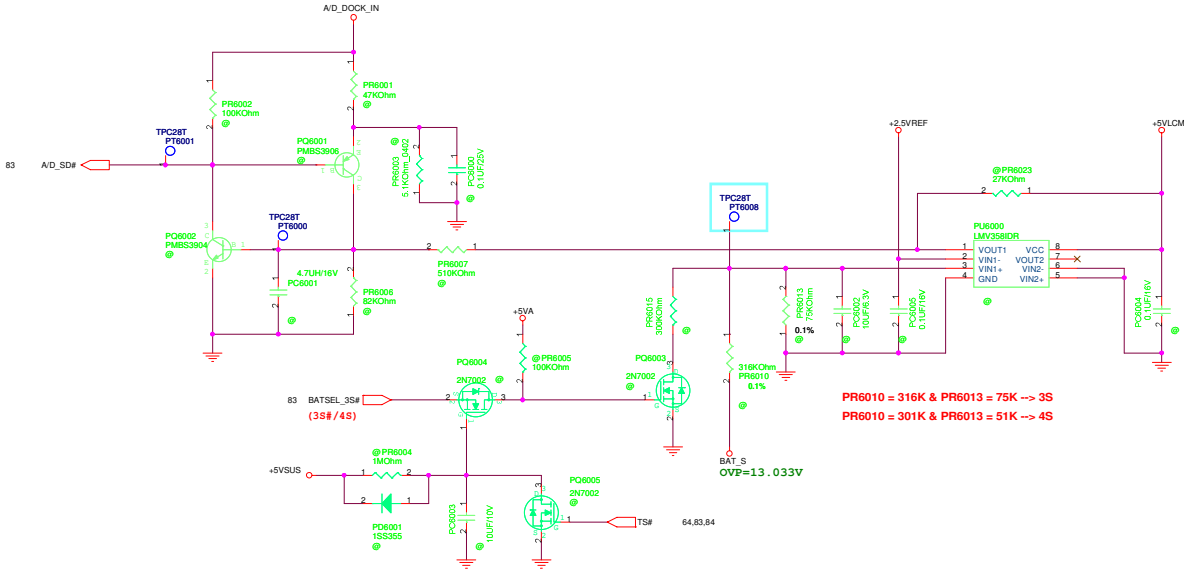


+5VLCM, +5VCHG & +2.5VREF

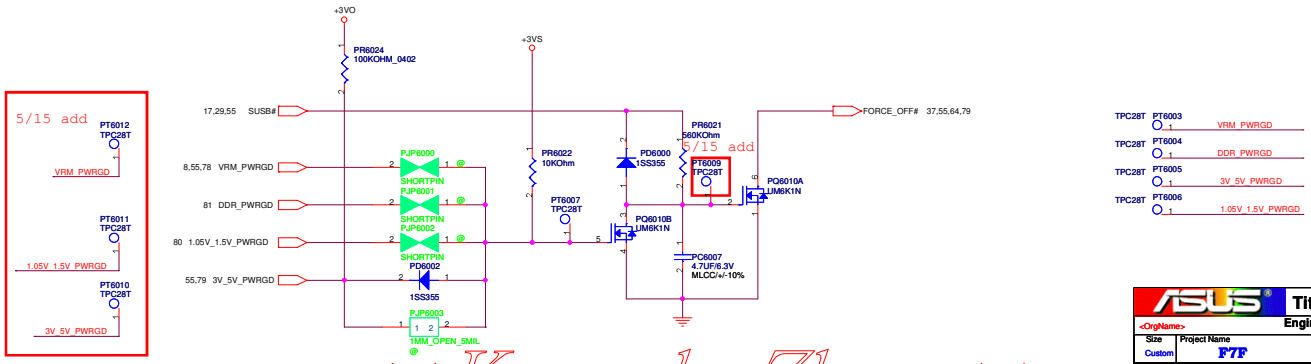




BATTERY A/D_SD# (OVP)



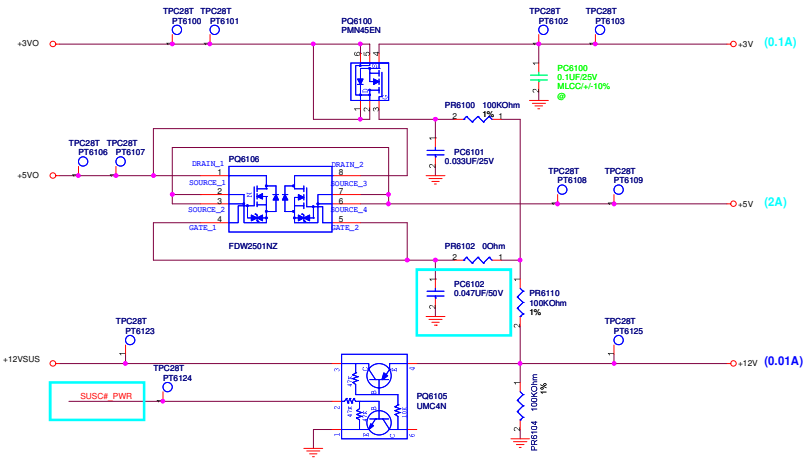
POWER GOOD DETECTER

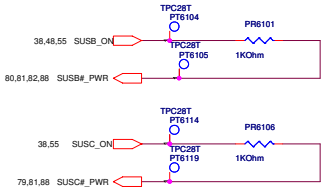


Title : POWER_PROTECT			
<OrgName>	Engineer: Gary Lin		
Size: Custom	Project Name: F7F		Rev: 1.0
Date: 星期 一, 五月 15, 2007	Sheet 85 of 12		

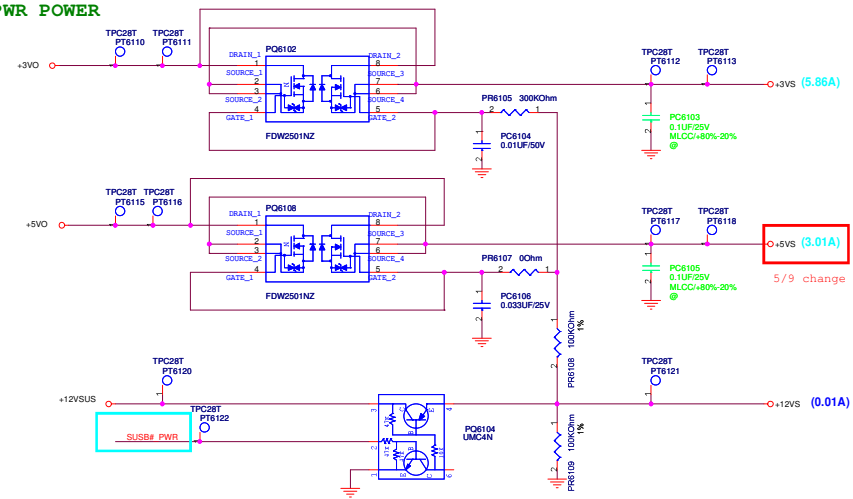
<< Kennedy_Zhang >>

SUSC#_PWR POWER

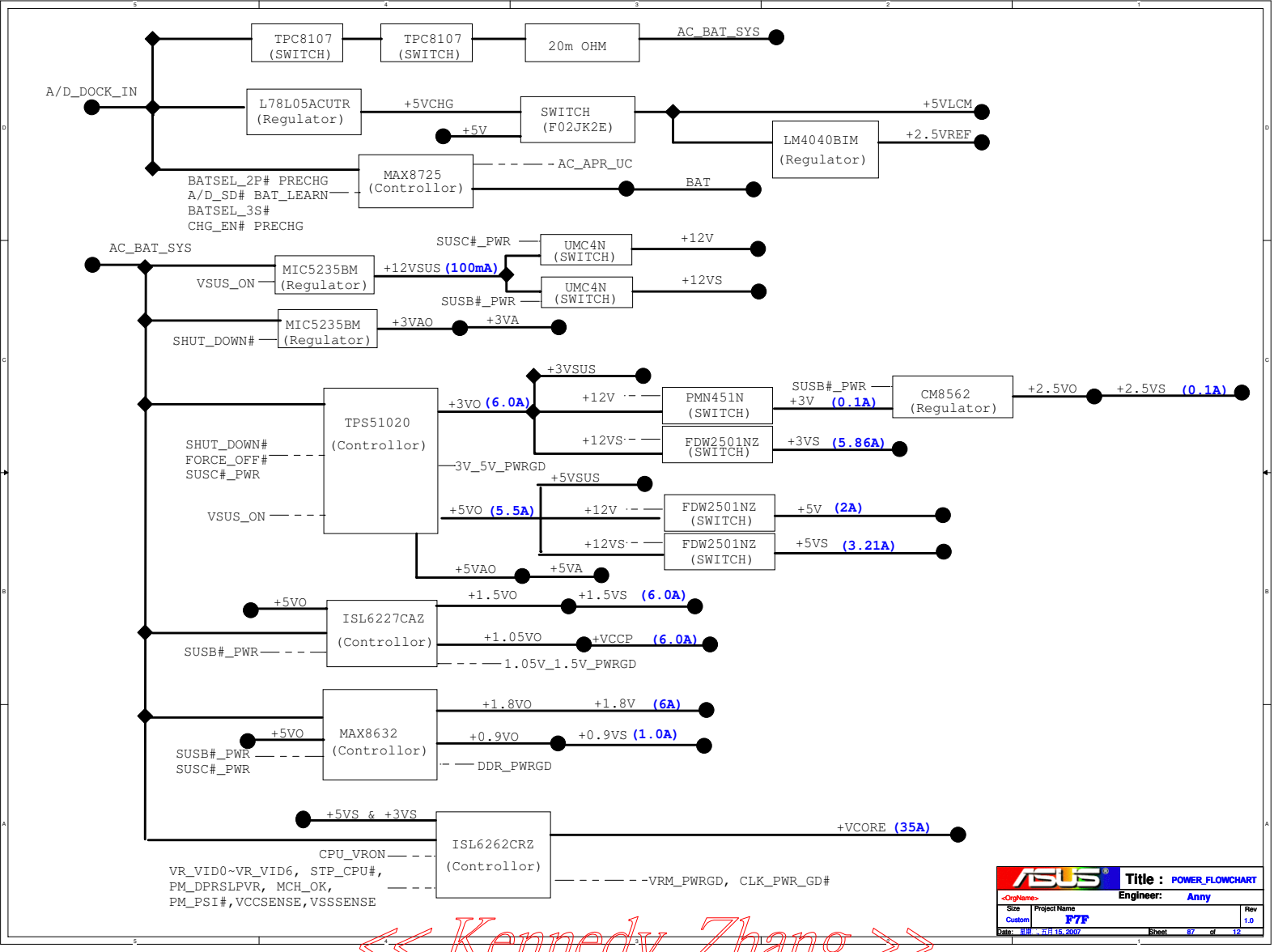




SUSB#_PWR POWER



Title : POWER_LOAD SWITCH			
<OrgName>	Engineer: Gary Lin		
Size: Custom	Project Name: F7F		Rev: 1.0
Date: 星期一 十月 15, 2007	Sheet 86 of 12		



AC_BAT_SYS — AC_BAT_SYS 29,64,74,78,79,80,81,82,83

+3VA — +3VA 15,29,37,38,55,82,84

+5VA — +5VA 79,82,85

+5VO — +5VO 79,80,81,83,84,85,86

+3VO — +3VO 79,80,85,86

+3VSUS — +3VSUS 16,17,18,40,41,43,48,79

+5VSUS — +5VSUS 18,62,79,85

+3V — +3V 29,38,40,41,43,53,72,76,82,86

+3VS — +3VS 8,9,12,16,17,18,20,21,28,29,31,33,35,38,40,43,45,46,47,48,50,52,53,55,66,68,72,78,80,85,86

+12VSUS — +12VSUS 79,86

+12V — +12V 38,47,53,86

+12VS — +12VS 29,53,62,86

+5V — +5V 12,29,38,58,84,86

+5VS — +5VS 17,18,28,33,38,48,52,53,55,56,62,68,78,86

+2.5VO — +2.5VO 82

+2.5VS — +2.5VS 8,12,28,38,52,82

+1.8VO — +1.8VO 81

+1.8V — +1.8V 8,11,20,21,22,38,81

+VCCP — +VCCP 4,7,18,35,38,74,80

+VCCP_AGTL+ — +VCCP_AGTL+ 4,5,7,12

+VCCP_GMCH — +VCCP_GMCH 7,11,50

+VCCP_ICH — +VCCP_ICH 15,18

+0.9VS — +0.9VS 22,38,81

BAT — BAT 64,83

+5VCHG — +5VCHG 83,84

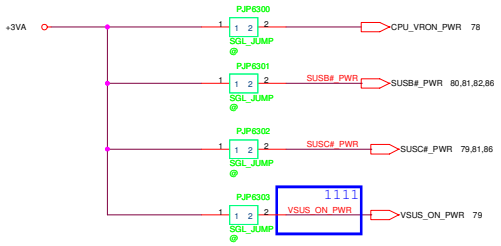
+5VLCM — +5VLCM 79,80,81,83,84,85,86

+2.5VREF — +2.5VREF 82,83,84,85

+VCORE — +VCORE 5,74,78

BAT_CON — BAT_CON 64,83

FOR POWER TEST



ASUS

Title : POWER_SIGNAL

<OrgName>

Engineer: Gary Lin

Size	Project Name	Rev
Custom	F7F	1.0

Date: 星期 一, 五月 15, 2007 Sheet 88 of 12

<< Kennedy_Zhang >>

Rev	Date	Description
1.0	11/28/2005	1. Initial release.
1.1	01/13/2006	1. For RF Switch disable, BT can't detect by Wireless console issue, add BT detect pin. Page 17,74. 2. Change C676,C677 Package size. Page 41. 3. Fix 1394 connector pin reverse issue. Page 46. 4. Fix Battery connector ping reverse issue. Page 64. 5. Add Capacity CE20, C53, C54, C55, C56, C57, C58, for 3DMark screen become to one color and hang issue. Page 11. 6. Change L51 Package size. Page 29. 7. Change X1 & X6 for cost down. Page 15,55. 8. Remove Fan 3 pin design circuit. Page 33,55. 9. Fix debug connector pin reverse issue. Page 66. 10. Fix LID Switch can't disable backlight issue, change NB BL_EN net name to BKLTEN. Page 9,29. 11. Fix VSUS_ON_PWR and SUSC#PWR Net connect issue. Page 88. 12. Remove Cardbus PME signal for R5C832. Page 45. 13. Add AC Adaptor Voltage Error Signal to EC, and EC will show the abnormal by LED. Page 55. 14. Remove L107,D37,CE17,CE18 for cost down. Page 58. 15. Change Connector CON15,J2,CON11,CON17,CON27,CON22&CON7&CON8,J3&J4. Page 28,53,41,48,68,31,22,64. 16. Modify Audio schematic Change C578,C579 to 0.47UF and remove R403,R404,R405,R398,R399,R408,R409,R410,C603,C604. Page 52,53. 17. Change R351 to 22 ohm. Page 15. 18. Add C59 for EMI. Page 47. 19. Charger circuit add component. Page 83. 20. Change TPLED_ON GPIO pin from GPIO19 to GPIO14 and R55 10K ohm pull low. Page 17. 21. Depop circuit remove OP_SD# control function. Page 53,55. 22. Add Mic. Preamplifer circuit. Page 52. 23. Change CE9,CE10 position for pop noise. Page 53. 24. Add buffer U5 for HSYNC and VSYNC of CRT signal. Page 9,28. 25. Add RN28,R156 near debug connector to be LPC terminal resistor. Page 66. 26. Change R233,R234,R235,R236 to L107,L108,L109,L110 for EMI. Page 53.
2.0		1. Colay Audio circuit for STAC9200 and ALC660. Remove Mic. Pre-Amplifer circuit. Page 52,53. 2. Modify minicard latch connector to nut.(H57,H58) Page 43. 3. Change SATA Connector. Page 68. 4. Add +3V LDO circuit for TV_DAC Power. Page 12.

Rev	Date	Description
		5. Remove R96,R97,R524 for Fan circuit. Page 33. 6.Add some test point for factory request. 7.Change BT_ON# from SB GPIO to EC GPIOE7. Page 17,55. 8.Add MOS for EC leakage of electricity issue.Page 55. 9.Change BT logic power from +3VS to +3V for WHQL S3 test .Page 76. 10.For Lan -ve test issue,add terminal resistor near the transformer .Page 41. 11.For ACZ RST will let Sigmatel codec GPIO0 high issue, add C177 to deplay depop time to avoid pop from speaker .Page 53.
2.1	04/24/2006	1.Change internal Mic. bias voltage from +5V_AUDIO to +2.5VS. Page 52. 2.Add D52,D53 to protect EC. Page 55. 3.Add C178,C179 for new card clock. Page 48. 4.Add H1,H2 for Fan. Page 70. 5.Remove RN2,RN3 for Vcore VID. ESD Request. Page 5. 6.Add R87 for moat issue. Page 53.
2.2	05/25/2006	1.Change CarBus R5C841 1394 Pull High from TPB to TPA. Page 50. 2.Add U46,C742,C743,R572,R573,R574 LDO circuit for internal Mic. Pull high +2VS. Add R575,C745 for + 3.Remove L17,L64,L84,L86,L87,L90 Co-Lay circuit. Page 76,48,58.
2.3	07/24/2006	1.Change DDR2 VREF Voltage from 0.9VS to 0.9V. Add L53,PR5317 from Power IC and R753,R754,C202,C203 from 1.8V. Page 22,81. 2.Change C59 connect from MS_DAT0 to MSCLK. Page 47. 3.Add R88,R89 for VISTA cost down with 100uF. Page 53. 4.For EMI Request, add C180 to SPDIF signal and near the codec. Page 52.

ASUSTek COMPUTER INC

Title : History

Engineer: Ryan Wang

Size	Project Name	Rev
Custom	FTF	1.0

Date: 星期 二, 十月 15, 2007 Sheet 89 of 12