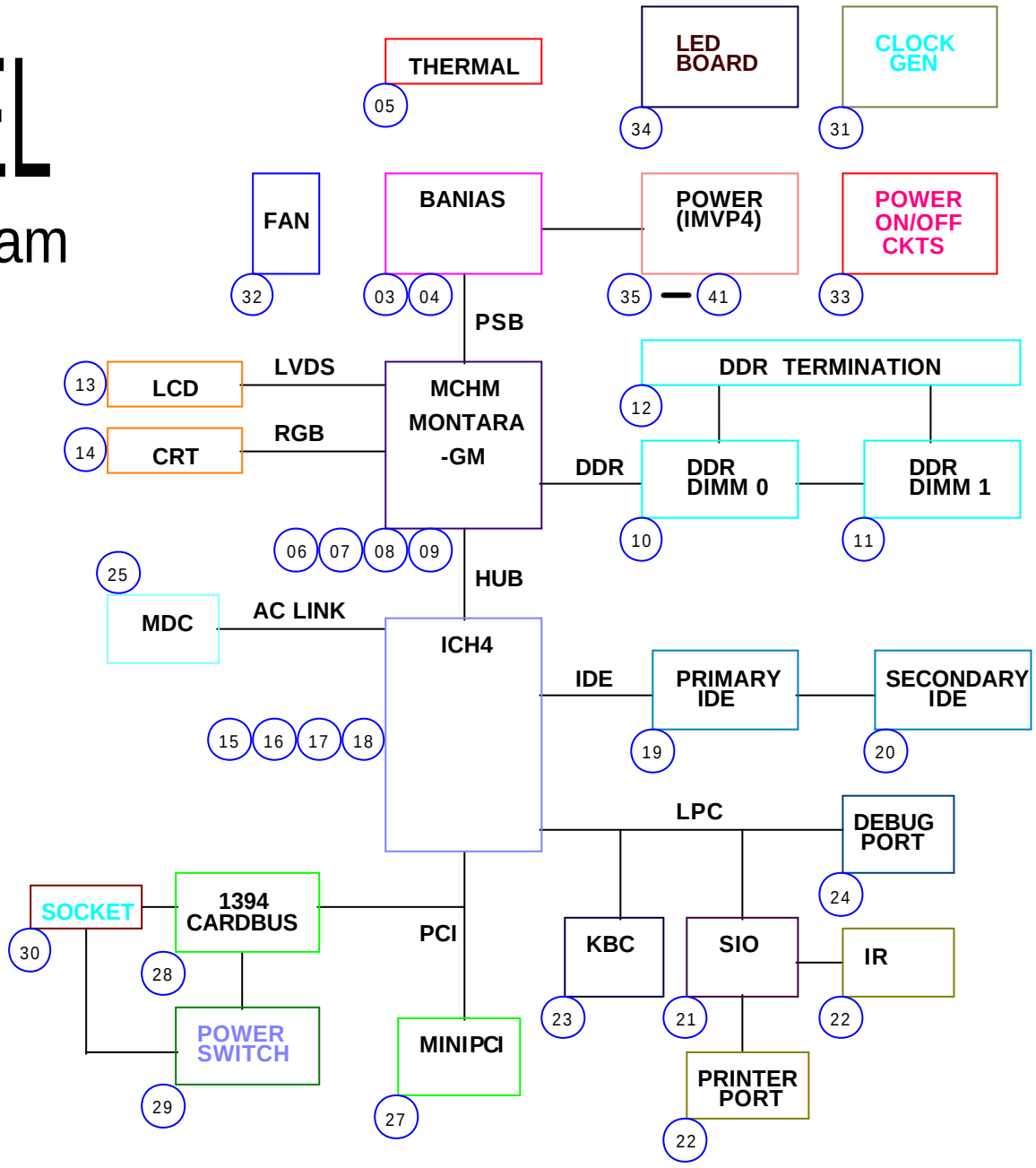
CARMEL

Block Diagram



26

IO BOARD

DC-DC JACK	MODEM
FWH	LAN PHY
USB PORT	MIC
OP	AC97

PORTBAR CON

PS2	LAN CON
PRINTER PORT	USB PORT

FILE LIST

01

REV. LIST

02

60-N4LMB1000-A01P

PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: BLOCK DIAGRAM	SCHEMATIC FILE NAME :
		SHEET 1 OF		LIBRARY DATE :
				DESIGN ENGINEER :

REVISION LIST

R1.0 2002/09/02 Initial

R1.1 2002/12/07 1) Pull ACIN_OC(R531) high to +V3.3
2) Pull BAT1_IN#_OC(R532) high to +V3.3
3) Pull BAT2_IN#_OC(R533) high to +V3.3
4) Change Q90 to U57(same P/N:06-004600000)
5) U46 Pin6 connected to +V3.3SUS

R1.2 2002/12/27

PCB STACK-UP

PCB THICKNESS: 1.2 mm

L1 TOP
L2 GND1
L3 IN1
L4 IN2
L5 VCC
L6 IN3
L7 GND2
L8 BOT

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	22 mils
IN1/IN3	16 mils

37.5 OHM	WIDTH
TOP/BOT	13.5 mils
IN1/IN3	10 mils

42 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN3	8.5 mils

55 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN3	5 mils

75 OHM	WIDTH
TOP/BOT	2.5 mils
IN1/IN3	2 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	8 mils/ 4 mils
IN1/IN3	8 mils/ 3.5 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 5 mils
IN1/IN3	5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	4 mils/ 6 mils
IN1/IN3	4.25 mils/ 5.75 mils

PCI INTERFACE

PCI_REQ#

CB&1394	PCI_REQ#0
MINIPCI	PCI_REQ#1

IDSEL

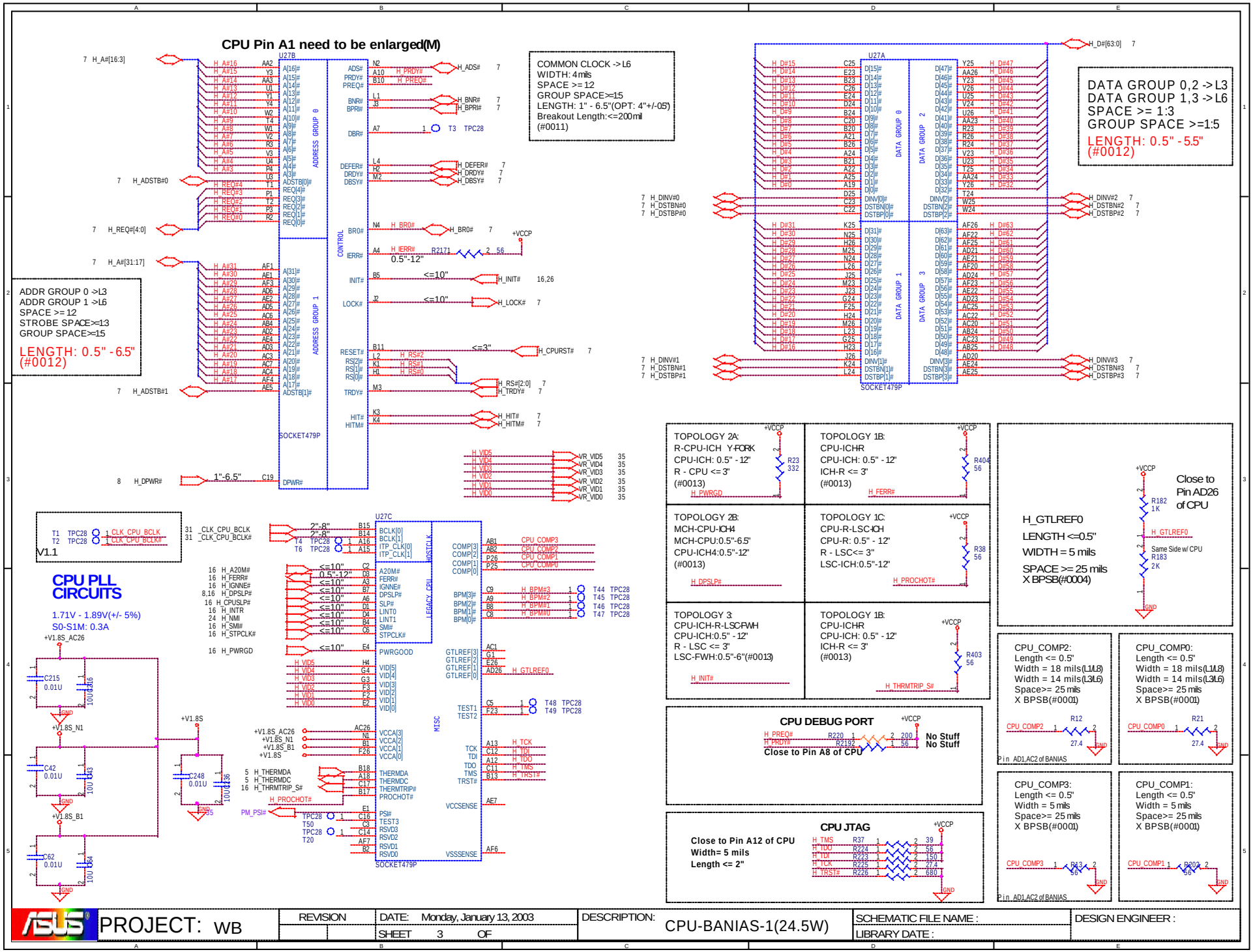
MINIPCI	PCI_AD20
CB&1394	PCI_AD21

POWER INTERFACE

SIGNALS	TYPE	POWER
CLK_EN#	I	+V3.3
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
1.5V_PWRGD	I	+V3.3
1.8V_PWRGD	I	+V3.3
CPU_VRON	O	+V3.3
VRM_PWRGD	I	+V3.3
PM_STPCPU#	O	+V3.3
CHG_LED	I	+V3.3
RST_BTN#	O	+V3.3
OTP_RESET#	I	+V3.3
SHUT_DOWN#	I	+V3.3
+V5_LCM	PWR	+V5
PM_SLPDLY_S3#	O	+V3.3
PM_SLP_S4#	O	+V3.3
BAT_LEARN	I	+V3.3
BAT_LLOW#_OC	I	+V3.3
BAT1_IN#_OC	I	+V3.3
BAT2_IN#_OC	I	+V3.3
ACIN_OC	I	+V3.3
CHG_EN_OC	I	+V3.3
PM_DPRSLPVR	O	+V3.3
ACIN_3VA	I	+V3.3
+5VAO	PWR	+V3.3
EN_+3VALWAYS	O	+V3.3
AC_BAT_SYS	PWR	DC
A/D_DOCK_IN	PWR	DC
SMC_BAT1	IO	+V3.3
SMD_BAT1	IO	+V3.3
SMC_BAT2	IO	+V3.3
SMD_BAT2	IO	+V3.3
BAT_LOW#	I	+V5_LCM

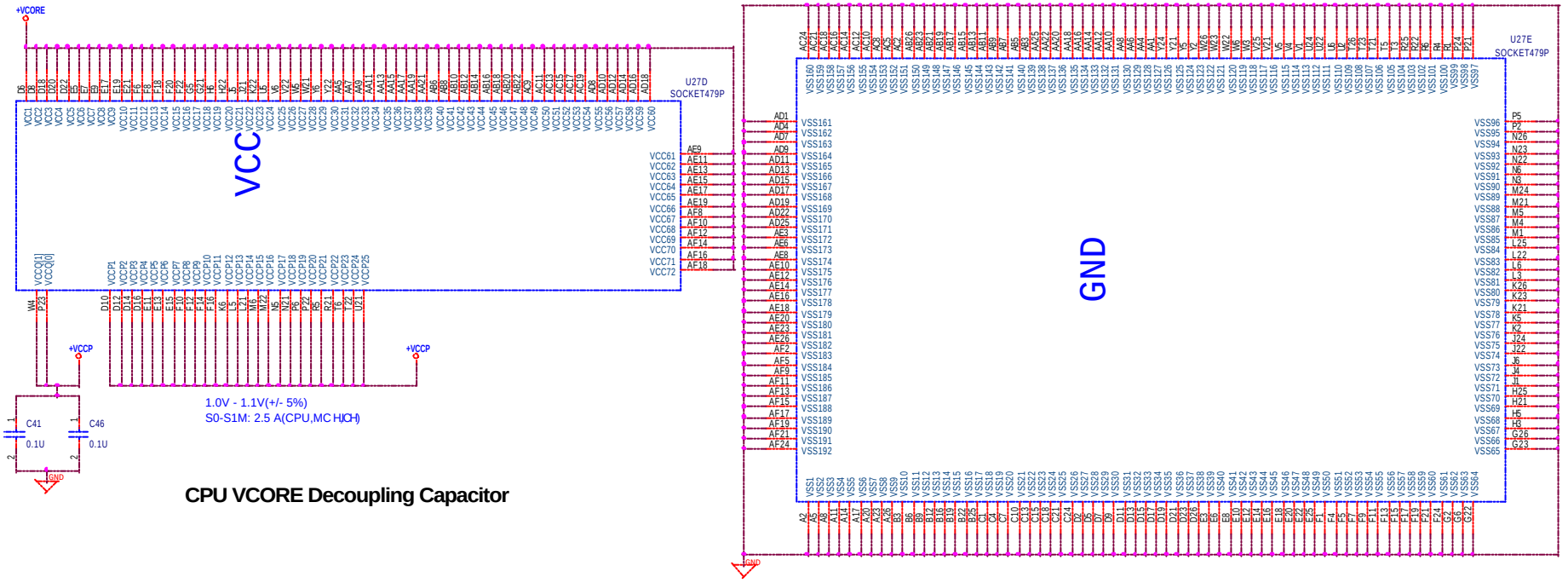
POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	1.46V	25A
+VCCP	1.05V	2.5A
+V1.2S	1.2V	2.5A
+V1.25S	1.25V	0.5A
+V1.5S	1.5V	1.32A
+V1.5	1.5V	30 mA
+V1.5SUS	1.5V	64 mA
+V1.8S	1.8V	0.3 A
+V2.5	2.5V	6.68A
+V3.3S	3.3V	1.732A
+V3.3	3.3V	1.515A
+V3.3SUS	3.3V	14 mA
+V5S	5V	2.5A
+V5	5V	3.75A
+V5SUS	5V	0.5A
+V12	12V	0.25A
+V12S	12V	0.25A

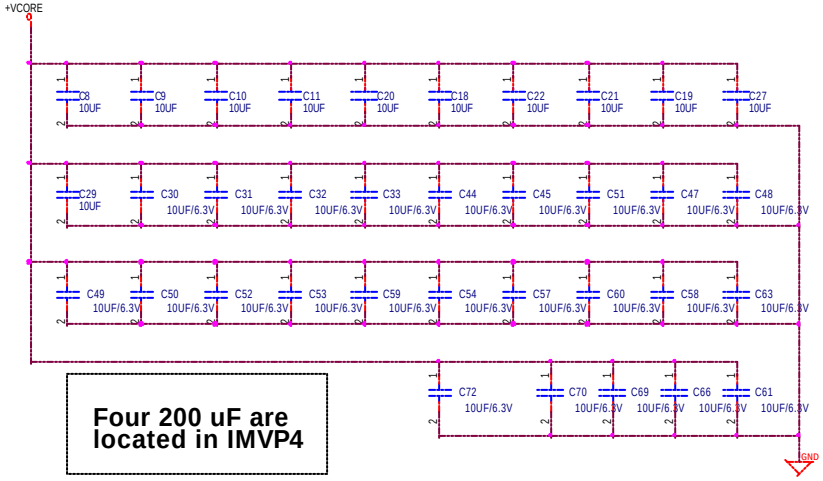

CPU Pin A1 need to be enlarged(M)
COMMON CLOCK -> L6
WIDTH: 4mils
SPACE >= 12
GROUP SPACE>=15
LENGTH: 1" - 6.5"(OPT: 4"+/-.05")
Breakout Length:<=200mil
(#0011)
ADDR GROUP 0 ->L3
ADDR GROUP 1 ->L6
SPACE >= 12
STROBE SPACE>=13
GROUP SPACE>=15
LENGTH: 0.5" - 6.5"
(#0012)
DATA GROUP 0,2 -> L3
DATA GROUP 1,3 -> L6
SPACE >= 1:3
GROUP SPACE >=1:5
LENGTH: 0.5" - 5.5"
(#0012)
U27B
U27A
U27C
SOCKET479P
TOPOLOGY 2A:
R-CPU-ICH Y-FORK
CPU-ICH: 0.5" - 12"
R - CPU <= 3"
(#0013)
TOPOLOGY 1B:
CPU-ICHR
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
TOPOLOGY 2B:
MCH-CPU-ICH4
MCH-CPU:0.5"-6.5"
CPU-ICH4:0.5"-12"
(#0013)
TOPOLOGY 1C:
CPU-R-LSC-ICH
CPU-R: 0.5" - 12"
R - LSC<= 3"
LSC-ICH:0.5"-12"
TOPOLOGY 3:
CPU-ICH-R-LSC-FWH
CPU-ICH:0.5" - 12"
R - LSC <= 3"
LSC-FWH:0.5"-6"(#0013)
TOPOLOGY 1B:
CPU-ICHR
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)
H_GTLREF0
LENGTH <=0.5"
WIDTH = 5 mils
SPACE >= 25 mils
X BPSB(#0004)
Close to Pin AD26 of CPU
CPU PLL CIRCUITS
1.71V - 1.89V(+/- 5%)
S0-S1M: 0.3A
CPU DEBUG PORT
Close to Pin A8 of CPU
No Stuff
No Stuff
CPU JTAG
Close to Pin A12 of CPU
Width= 5 mils
Length <= 2"
CPU_COMP2:
Length <= 0.5"
Width = 18 mils(L1/L8)
Width = 14 mils(L3/L6)
Space>= 25 mils
X BPSB(#0001)
CPU_COMP0:
Length <= 0.5"
Width = 18 mils(L1/L8)
Width = 14 mils(L3/L6)
Space>= 25 mils
X BPSB(#0001)
CPU_COMP3:
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
CPU_COMP1:
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)
Pin AD1,AC2 of BANIAS
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 3 OF
DESCRIPTION: CPU-BANIAS-1(24.5W)
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :

HFM(1.3GHz-1.7GHz): 1.468V
LFM(600MHz): 0.956V

0.745V - 1.356V(+/- 1.5%)
C0: 25 A
C3: 7.59A
C4: 0.9A



CPU VCORE Decoupling Capacitor



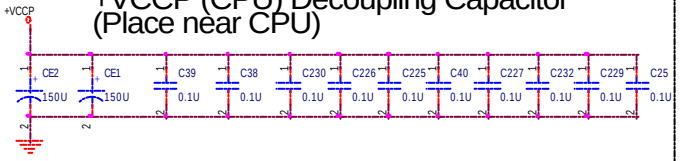
Four 200 uF are located in IMVP4

Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

+VCCP (CPU) Decoupling Capacitor (Place near CPU)

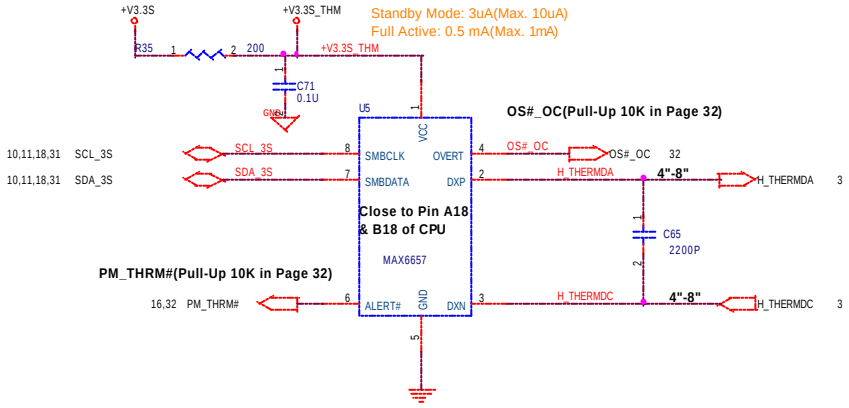


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: CPU-BANIAS-2(24.5W)	SCHEMATIC FILE NAME :
		SHEET 4 OF		LIBRARY DATE :
				DESIGN ENGINEER :

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
12 mils
----------OTHERSIGNALS

Avoid BPSB,Power



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: THERMAL	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 5 OF		LIBRARY DATE :	

Thermal Power: ~ 3.8W

LxWxH=37.5x37.5x2.58

U35B

DDR SYSTEM MEMORY

10,11,12 _DDR_DATA[63:0]

10,11,12 _DDR_CB[7:0]

DDR_DQS[8:0] 10,11,12

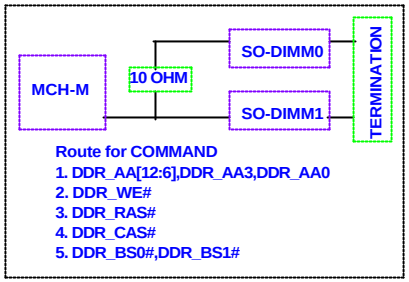
DDR_DM[8:0] 10,11,12

DDR_AA[12:0] 10,11,12

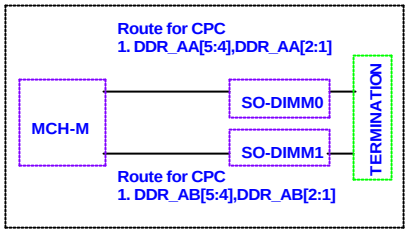
DDR_AB[2:1] 11,12

DDR_AB[5:4] 11,12

(MCH-Sighting041)
M-GM system memory interface generates single pulse CKE events which may cause Intermittent hangs and display corruptions when using Micron and Infineon S0-DIMMs.

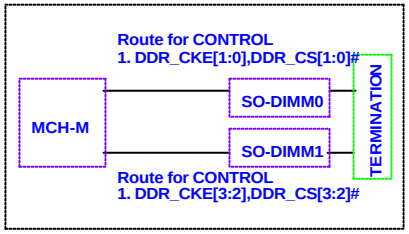


Route for COMMAND
1. DDR_AA[12:6],DDR_AA3,DDR_AA0
2. DDR_WE#
3. DDR_RAS#
4. DDR_CAS#
5. DDR_BS0#,DDR_BS1#



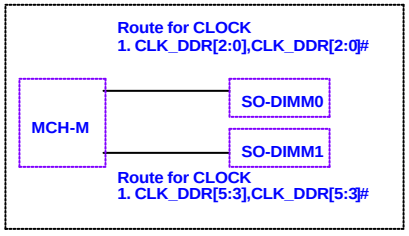
Route for CPC
1. DDR_AA[5:4],DDR_AA[2:1]

Route for CPC
1. DDR_AB[5:4],DDR_AB[2:1]



Route for CONTROL
1. DDR_CKE[1:0],DDR_CS[1:0]#

Route for CONTROL
1. DDR_CKE[3:2],DDR_CS[3:2]#

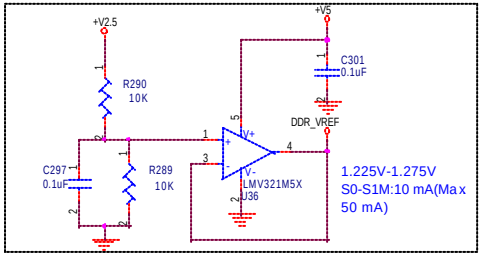


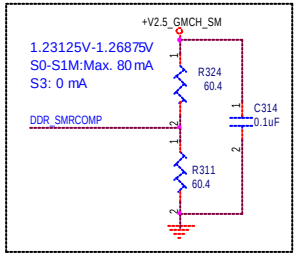
Route for CLOCK
1. CLK_DDR[2:0],CLK_DDR[2:0]#

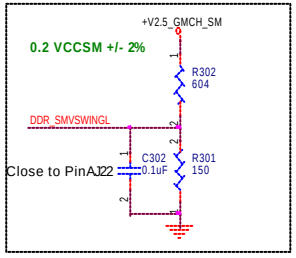
Route for CLOCK
1. CLK_DDR[5:3],CLK_DDR[5:3]#

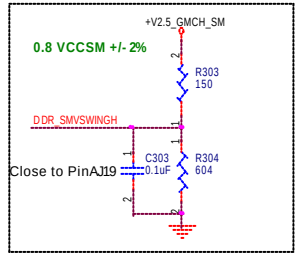
1.23125V-1.26875V
S0-S1M:Max. 80 mA
S3: 0 mA

Intel suggested that DDR_VREF should be turned off in S3-S5. But measure the leakage because there is no +V2.5S.









PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: MONTARA_GM-1(3.8W)	SCHEMATIC FILE NAME :
		SHEET 6 OF		LIBRARY DATE :
				DESIGN ENGINEER :

MCH_HLZCOMP:
Length <= 0.5"
Width = 18 mils(L1/L8)
Width = 14 mils(L3/L6)
Space>= 25 mils
X BPSB(#0002)

MCH_HYRCOMP:
Length <= 0.5"
Width = 18 mils(L1/L8)
Width = 14 mils(L3/L6)
Space>= 25 mils
X BPSB(#0002)

MCH_HXRCOMP:
Length <= 0.5"
Width = 18 mils(L1/L8)
Width = 14 mils(L3/L6)
Space>= 25 mils
X BPSB(#0002)

MCH_HYSWING:
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%
Close to PinH28

MCH_HXSWING:
Length <= 0.5"
Width = 15 mils
Space>= 25 mils
X BPSB(#0005)
1/3(+VCCP) +/- 2%
Close to PinB20

U35A LxWxH=37.5x37.5x2.58

HOST

HUB I/F

MONTARA_GML

0.8V +/- 2%

0.343V- 0.357V(Typ. 0.35V)

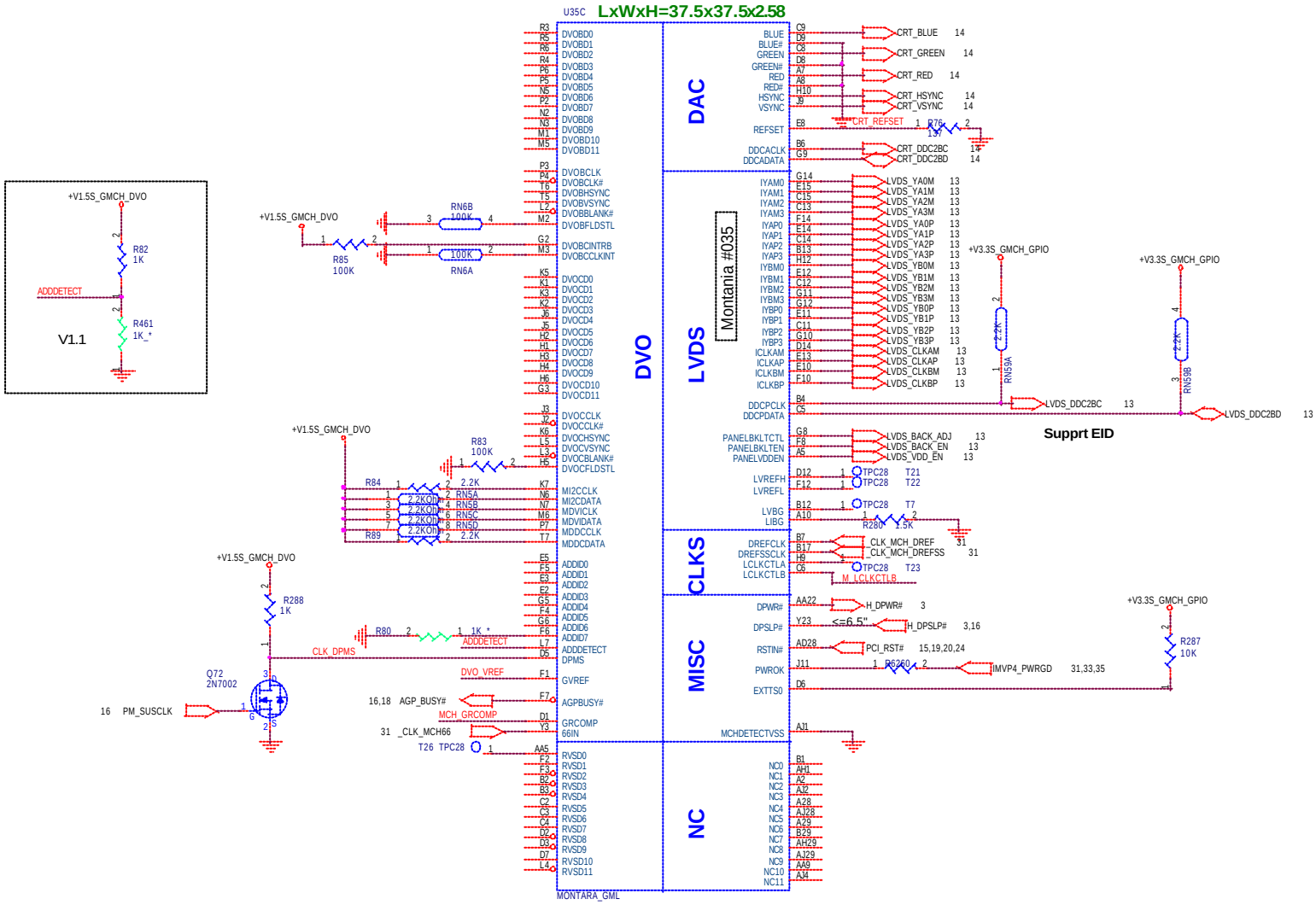
V1.1

MCH_HAVREF:
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%

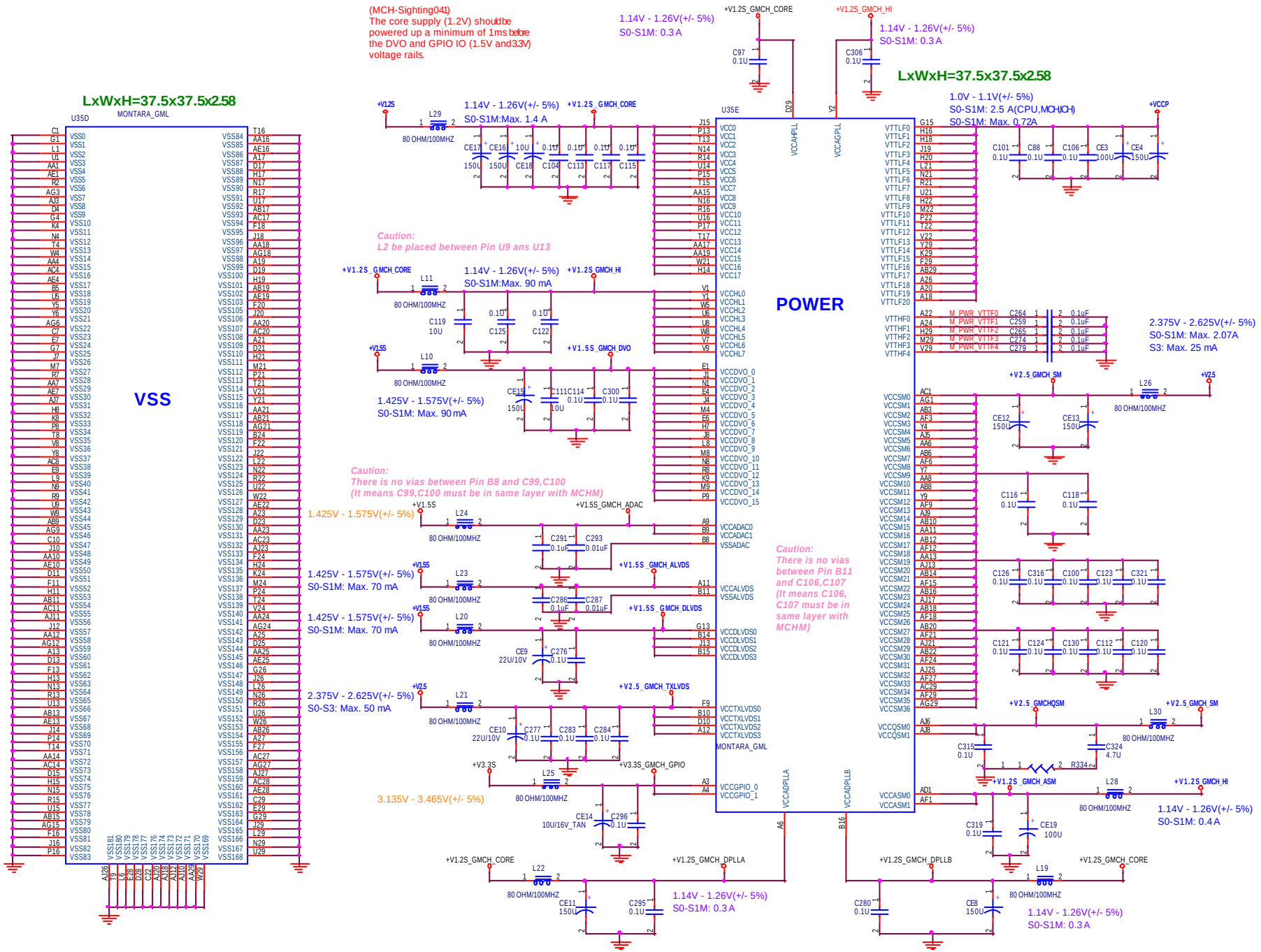
MCH_HCCVREF:
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%

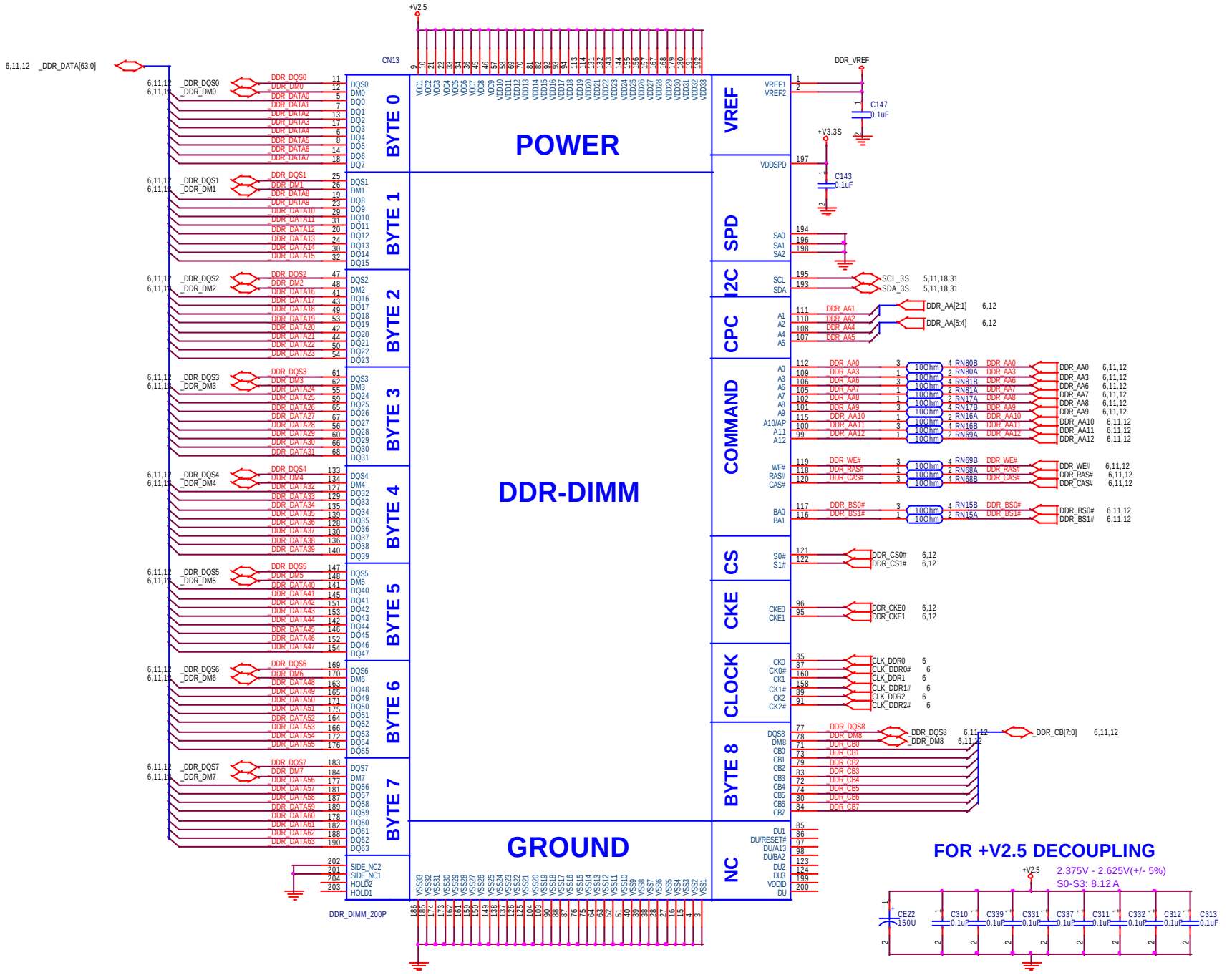
MCH_HDVREF:
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0003)
2/3(+VCCP) +/- 2%

PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: MONTARA_GM-2(3.8W)	SCHEMATIC FILE NAME :
		SHEET 7 OF		LIBRARY DATE :
				DESIGN ENGINEER :

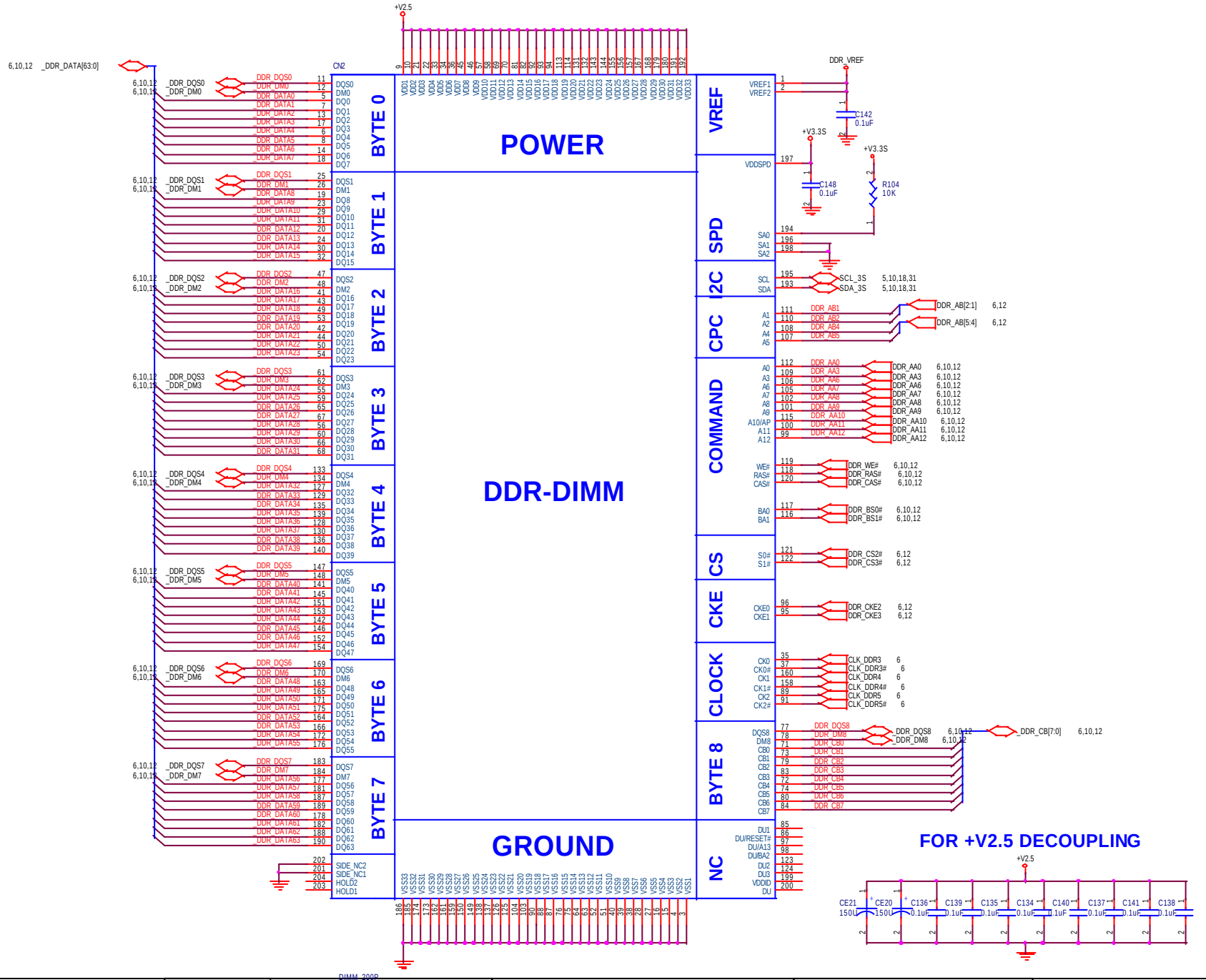


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: MONTARA_GM-3(3.8W)	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 8 OF		LIBRARY DATE :	


(MCH-Sighting041)
The core supply (1.2V) should be powered up a minimum of 1ms before the DVO and GPIO IO (1.5V and 3.3V) voltage rails.
LxWxH=37.5x37.5x2.58
U35D
MONTARA_GML
VSS
POWER
U35E
LxWxH=37.5x37.5x2.58
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
1.14V - 1.26V(+/- 5%)
S0-S1M:Max. 1.4 A
1.14V - 1.26V(+/- 5%)
S0-S1M:Max. 90 mA
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 90 mA
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 70 mA
1.425V - 1.575V(+/- 5%)
S0-S1M: Max. 70 mA
2.375V - 2.625V(+/- 5%)
S0-S3: Max. 50 mA
3.135V - 3.465V(+/- 5%)
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
1.0V - 1.1V(+/- 5%)
S0-S1M: 2.5 A(CPU,MCHICH)
S0-S1M: Max. 0.72A
2.375V - 2.625V(+/- 5%)
S0-S1M: Max. 2.07A
S3: Max. 25 mA
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.4 A
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
1.14V - 1.26V(+/- 5%)
S0-S1M: 0.3 A
Caution:
L2 be placed between Pin U9 ans U13
Caution:
There is no vias between Pin B8 and C99,C100
(It means C99,C100 must be in same layer with MCHM)
Caution:
There is no vias between Pin B11 and C106,C107
(It means C106, C107 must be in same layer with MCHM)
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 9 OF
DESCRIPTION: MONTARA_GM-4(3.8W)
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :

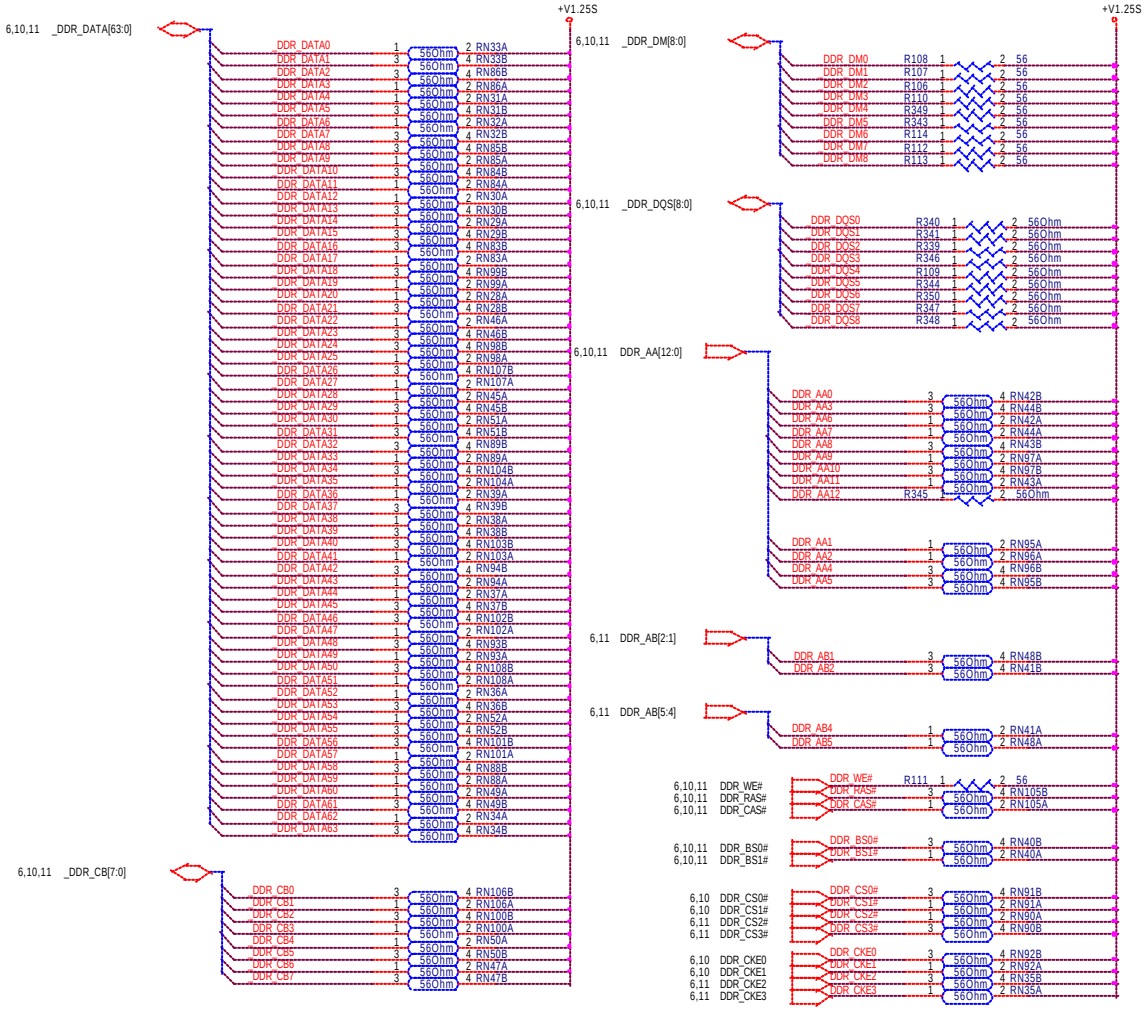


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: DDR200 SO-DIMM 0	SCHEMATIC FILE NAME :
		SHEET 10 OF		LIBRARY DATE :
				DESIGN ENGINEER :

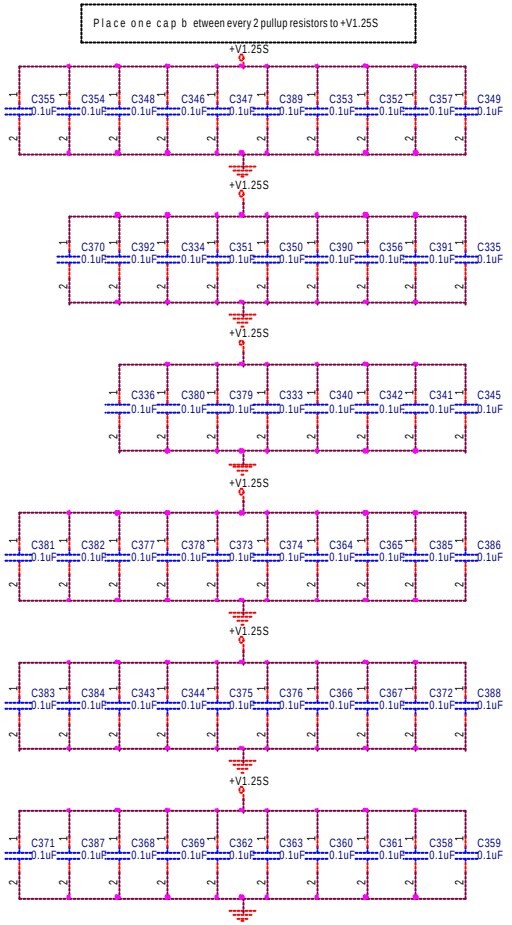


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: DDR200 SO-DIMM 1	SCHEMATIC FILE NAME :
		SHEET 11 OF		LIBRARY DATE :
				DESIGN ENGINEER :

DDR TERMINATION



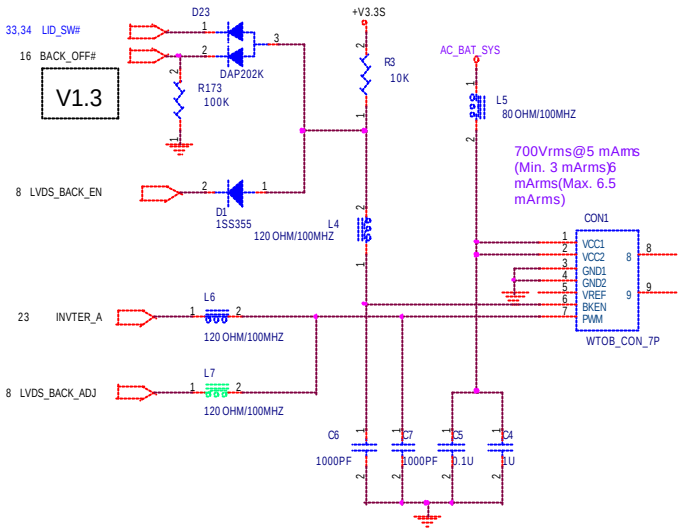
FOR +V1.25S DECOUPLING



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: DDR200 TERMINATION	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 12 OF		LIBRARY DATE :	

LCD Backlight Control

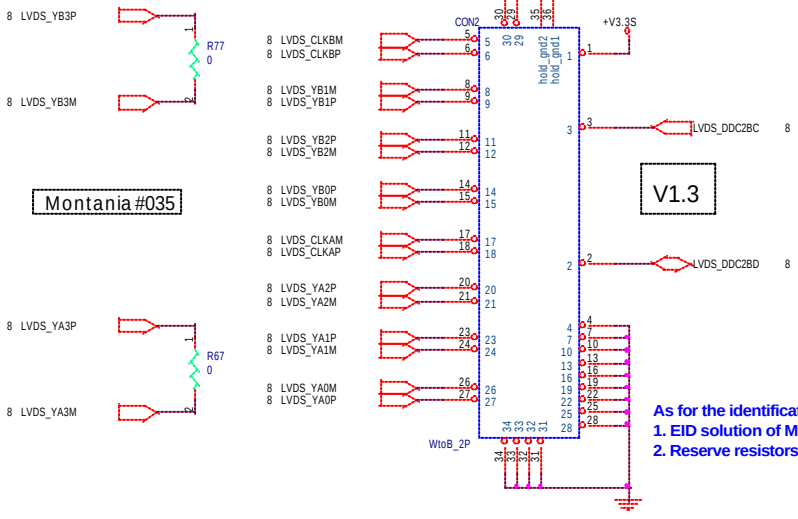
LCD Backlight will be turned off:
1) Lid Switch be pressed(ME)
2) BACK_OFF# asserted(ICH4 GPIO)
3) LCD_BACK_EN
disaasserted(GMCH)



LCD LVDS Interface

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

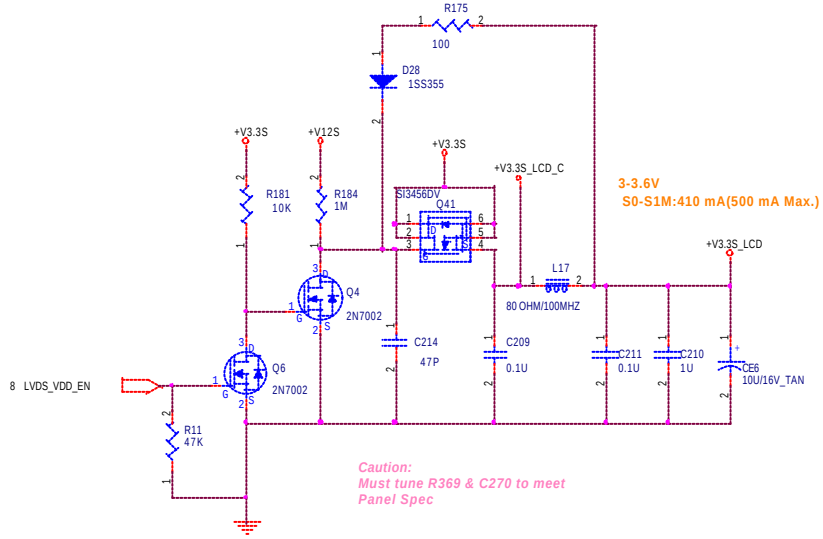
3V-3.6V
Full
Active:
410
mA(Max.
500 mA)



As for the identification of LCD,we use:
1. EID solution of Montara-GM
2. Reserve resistors for Panel ID

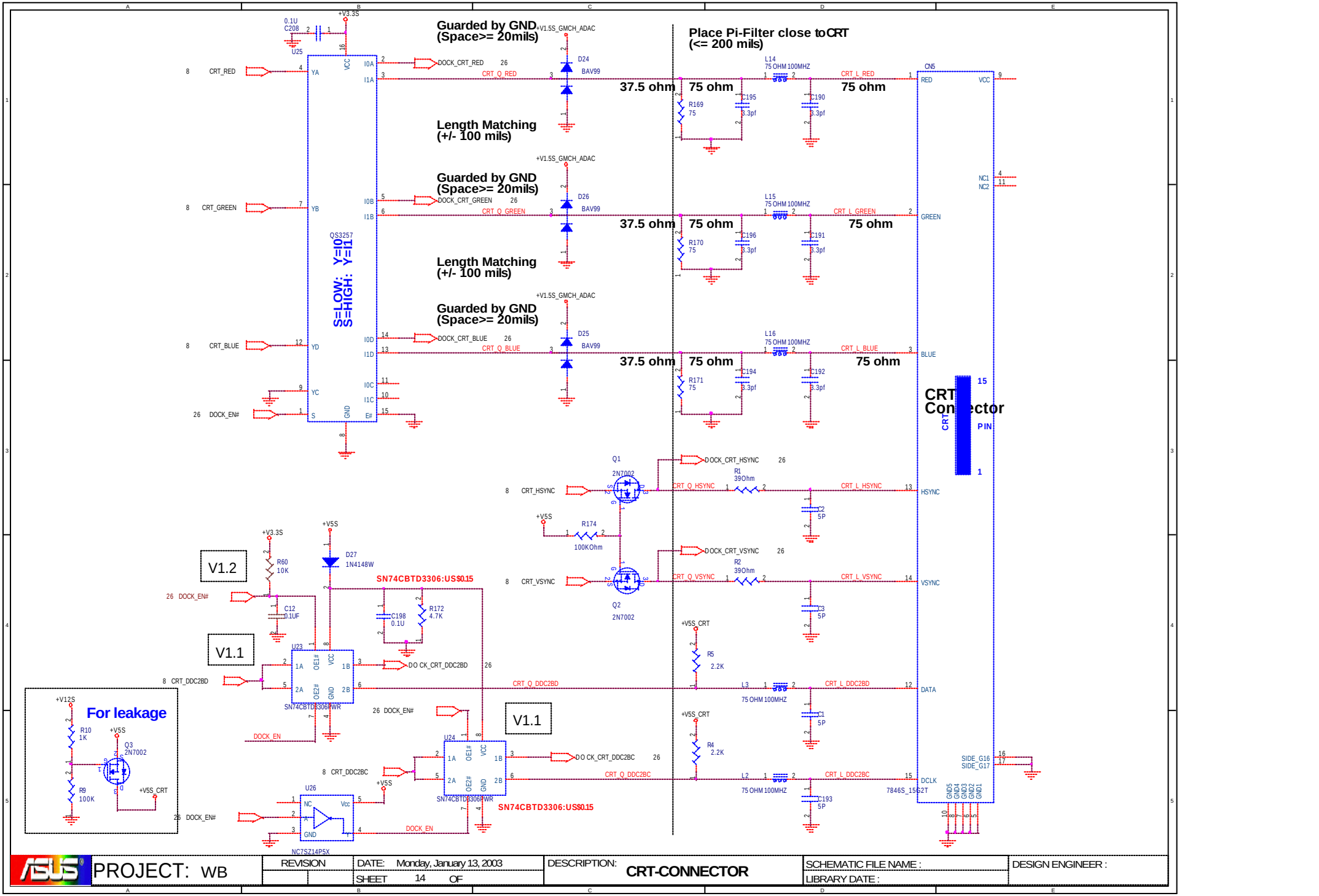
LCD Power

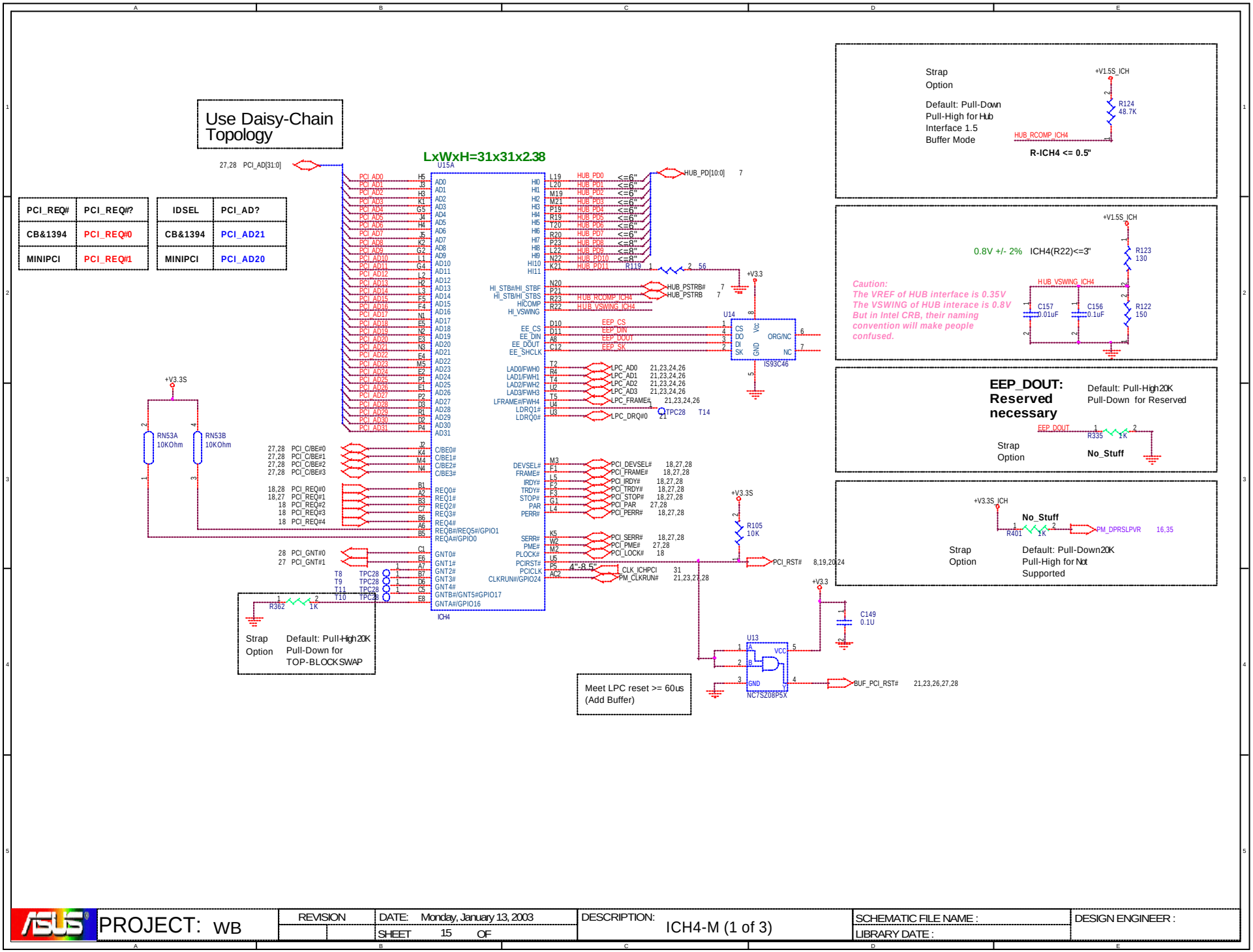
SI3865: US$0.22



Caution:
Must tune R369 & C270 to meet
Panel Spec

PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: LVDS & BACKLIGHT	SCHEMATIC FILE NAME :
		SHEET 13 OF		LIBRARY DATE :
				DESIGN ENGINEER :


Guarded by GND (Space>= 20mils)
Place Pi-Filter close to CRT (<= 200 mils)
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
Length Matching (+/- 100 mils)
Guarded by GND (Space>= 20mils)
37.5 ohm
75 ohm
75 ohm
S=LOW: Y=I0
S=HIGH: Y=I1
CRT_RED
CRT_GREEN
CRT_BLUE
DOCK_EN#
DOCK_CRT_RED
DOCK_CRT_GREEN
DOCK_CRT_BLUE
CRT_Q_RED
CRT_Q_GREEN
CRT_Q_BLUE
CRT_L_RED
CRT_L_GREEN
CRT_L_BLUE
CRT_HSYNC
CRT_VSYNC
DOCK_CRT_HSYNC
DOCK_CRT_VSYNC
CRT_Q_HSYNC
CRT_Q_VSYNC
CRT_L_HSYNC
CRT_L_VSYNC
CRT_DDC2BD
CRT_DDC2BC
CRT_Q_DDC2BD
CRT_Q_DDC2BC
CRT_L_DDC2BD
CRT_L_DDC2BC
DOCK_CRT_DDC2BD
DOCK_CRT_DDC2BC
DOCK_EN
CRT Connector
PIN 15
PIN 1
V1.2
V1.1
V1.1
For leakage
SN74CBTD3306:US$0.15
SN74CBTD3306:US$0.15
NC7SZ14P5X
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 14 OF
DESCRIPTION: CRT-CONNECTOR
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: ICH4-M (1 of 3)
		SHEET 15 OF	

SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :

USB SIGNALS
X Clock Signals
| USB+ - USB-| <=150mils
Pair Width/Space: 4/4.5mils
Impedence: 90 ohm(differential)
Other Signals Space: >=20mils
Clock Signals Sapce>=50mils

USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"

V1.1

LxWxH=31x31x2.38

LxWxH=31x31x2.38

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"
Match: <= 500 mils

ICH4__R1__T__R2__AMC
AC97
Outer Layer: 5 mils AC97-(T): 0.1"- 6"
Inner Layer: 4 mils R2-(T): 0.1"- 0.4"
W/S= 1:1 AMC-R2: 0.9"-5.6"
ICH4-R1: 0.9"- 7.6" (#0011)
R1-(T): 0.1"- 0.4"

Strap Option
Default: Pull-Down20K
Pull-High for No Reboot

G3: 5uA

RC time delay should be 10-20 ms

RTC CIRCUITRY

RTC Circuits:
RTC_RST#, RTC_VBIAS,RTC_X1,RTC_X2
Width= 5 mils
Length<=1"
Need GND Guard

Measure duty-cycle of SUSCLK (Pin AA4) must be in 30-70%

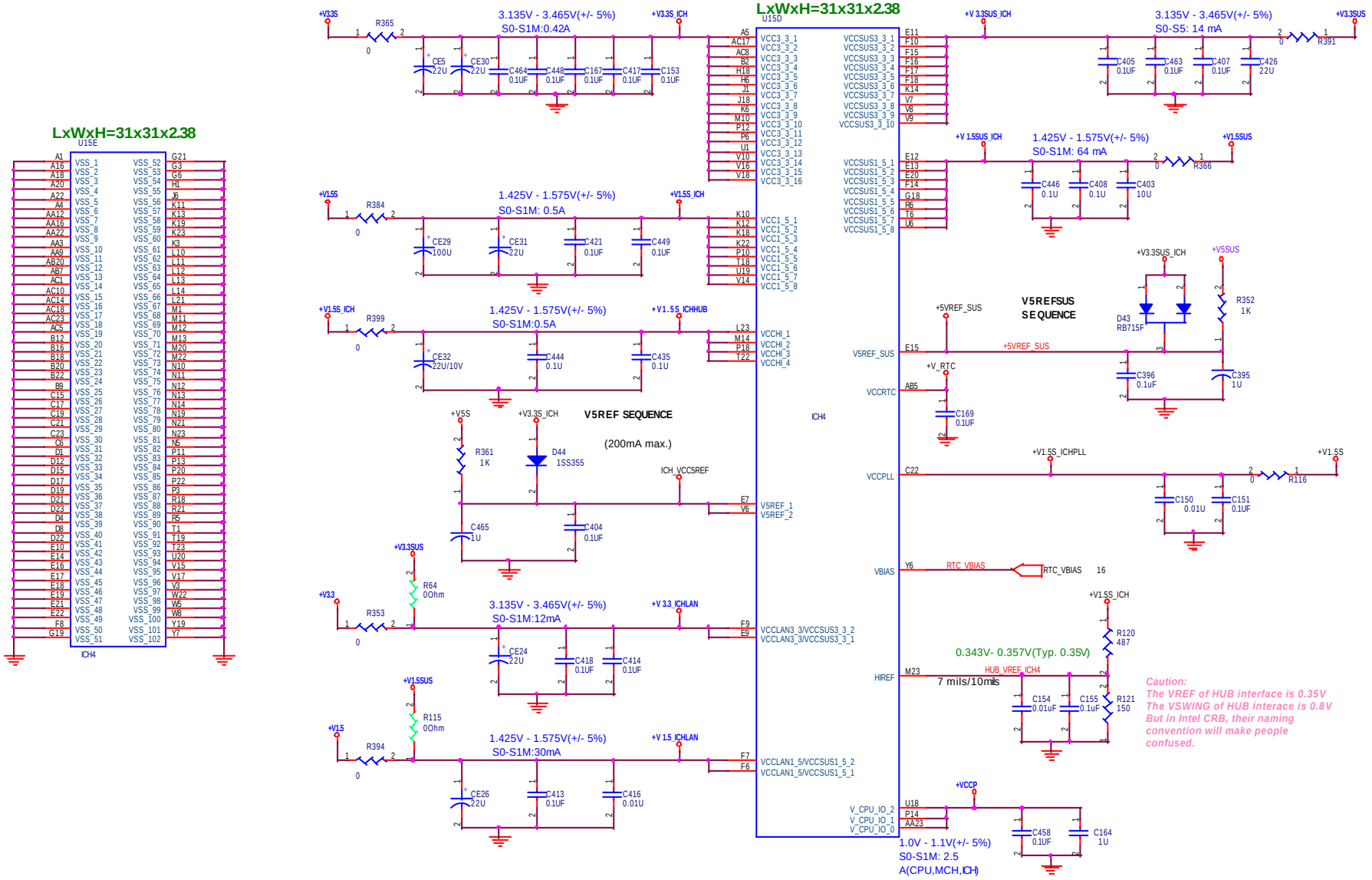
Vpeak-peak of RTC_X1<1V

AC97 SDOUT & SYNC
ICH4__T__R2__AMC
R1
AC97
Outer Layer: 5 mils AC97-R1: <=5.6"
Inner Layer: 4 mils R2-(T): 0.1"- 0.4"
W/S= 1:1 AMC-R2:
ICH4-(T): 1"- 8" 0.9"-5.6"
R1-(T): 0.1"- 0.4" (#0012)

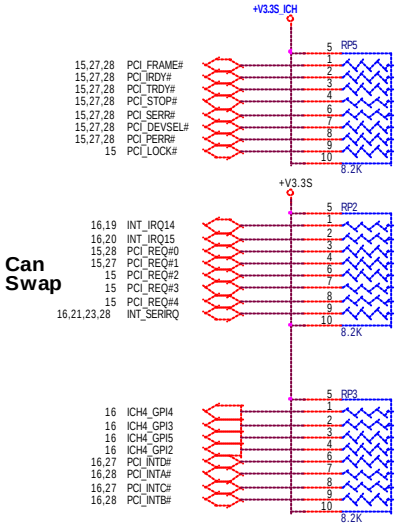
Strap Option: Default: Pull-Down20K; Pull-High for CPUSAFE_MODE

AC97 SDIN
ICH4__R2__AMC
AC97
Outer Layer: 5 mils
Inner Layer: 4 mils
W/S= 1:1
ICH4-R2: 0.9"- 13.6"
AC97-R2: 0.1"-0.4"
(#0013)

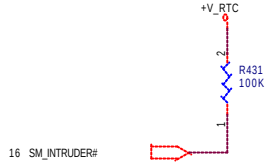
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: ICH4-M (2 of 3)(2.9W)	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 16 OF		LIBRARY DATE :	



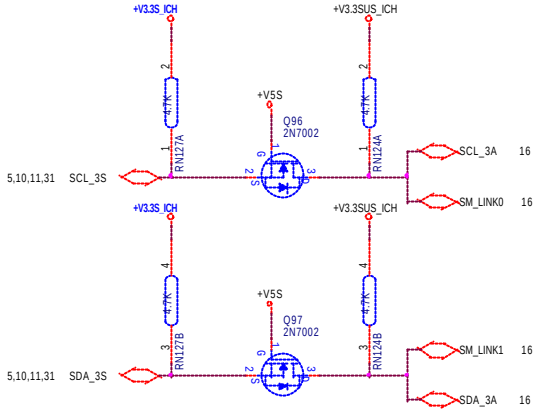
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: ICH4-M (3 of 3)(2.9W)	SCHEMATIC FILE NAME :
		SHEET 17 OF		LIBRARY DATE :
				DESIGN ENGINEER :

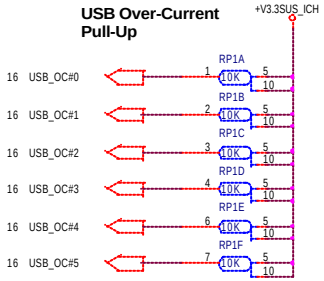


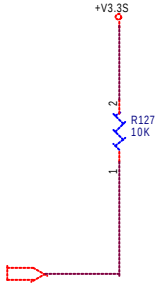
Can Swap



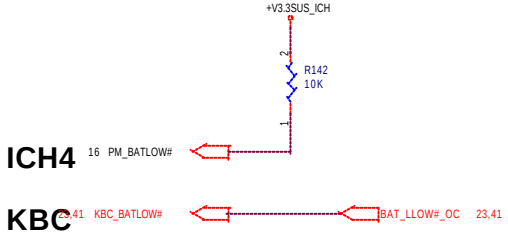
ICH4 SMLink & SMbus must be tied together







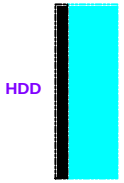
BATTERY LOW



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: ICH4-M PULLUPS	SCHEMATIC FILE NAME :
		SHEET 18 OF		LIBRARY DATE :
				DESIGN ENGINEER :

PRIMARY HDD

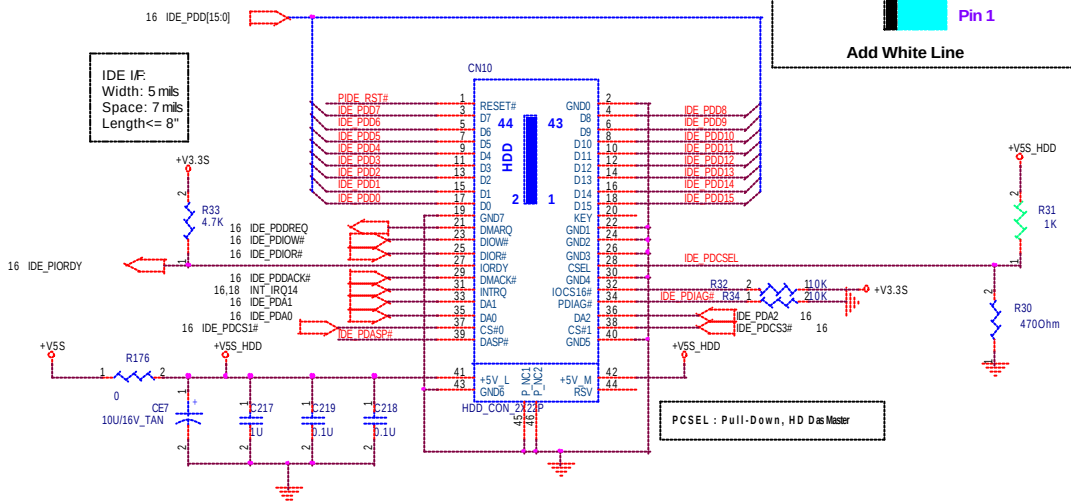
Due to ME change this connector 180 degree
We must mark the direction of this connector as following:



Add White Line

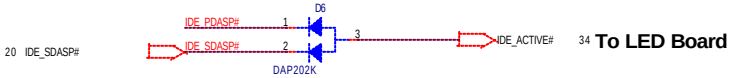
4.75-5.25V
S0-S1M:1.3A(Typ)0.54A(Max.) Write
S0-S1M:0.7A(Typ)0.5 A(Max.) Read

IDE I/F:
Width: 5 mils
Space: 7 mils
Length<= 8"



PCSEL : Pull-Down, HD Das Master

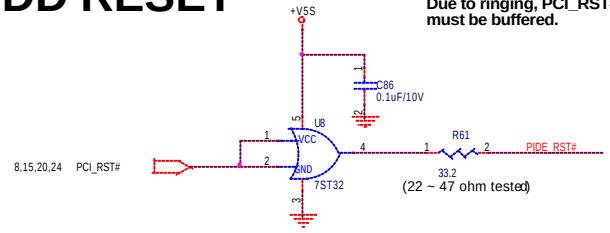
HDD LED



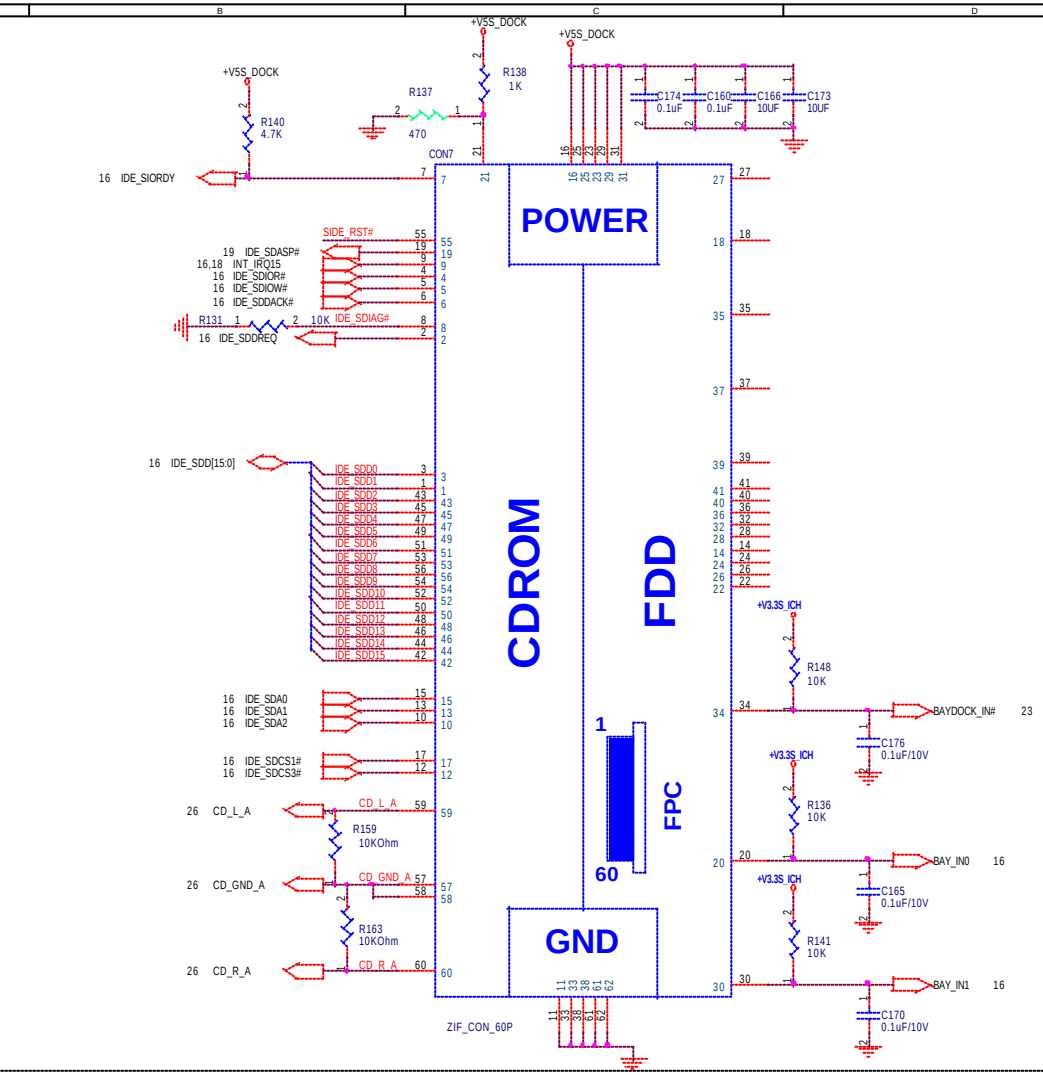
To LED Board

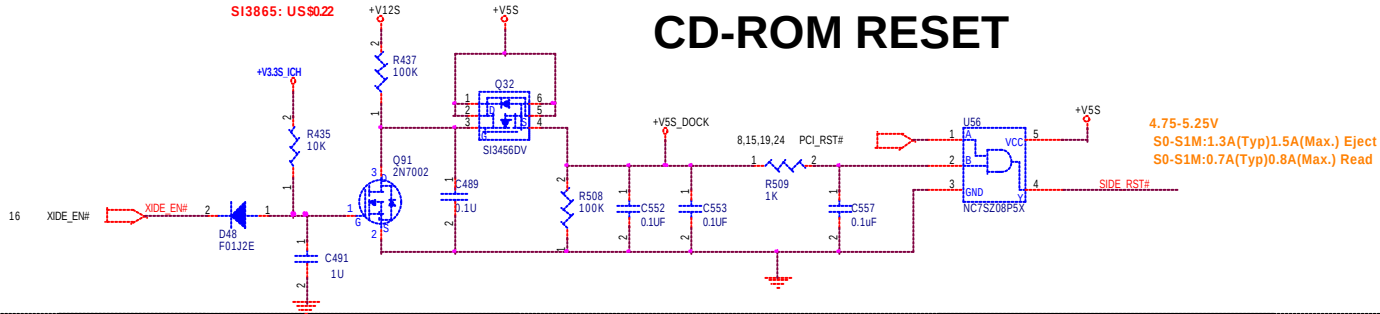
HDD RESET

Due to ringing, PCI_RST# must be buffered.



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: IDE & CDROM CONN.	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 19 OF		LIBRARY DATE :	

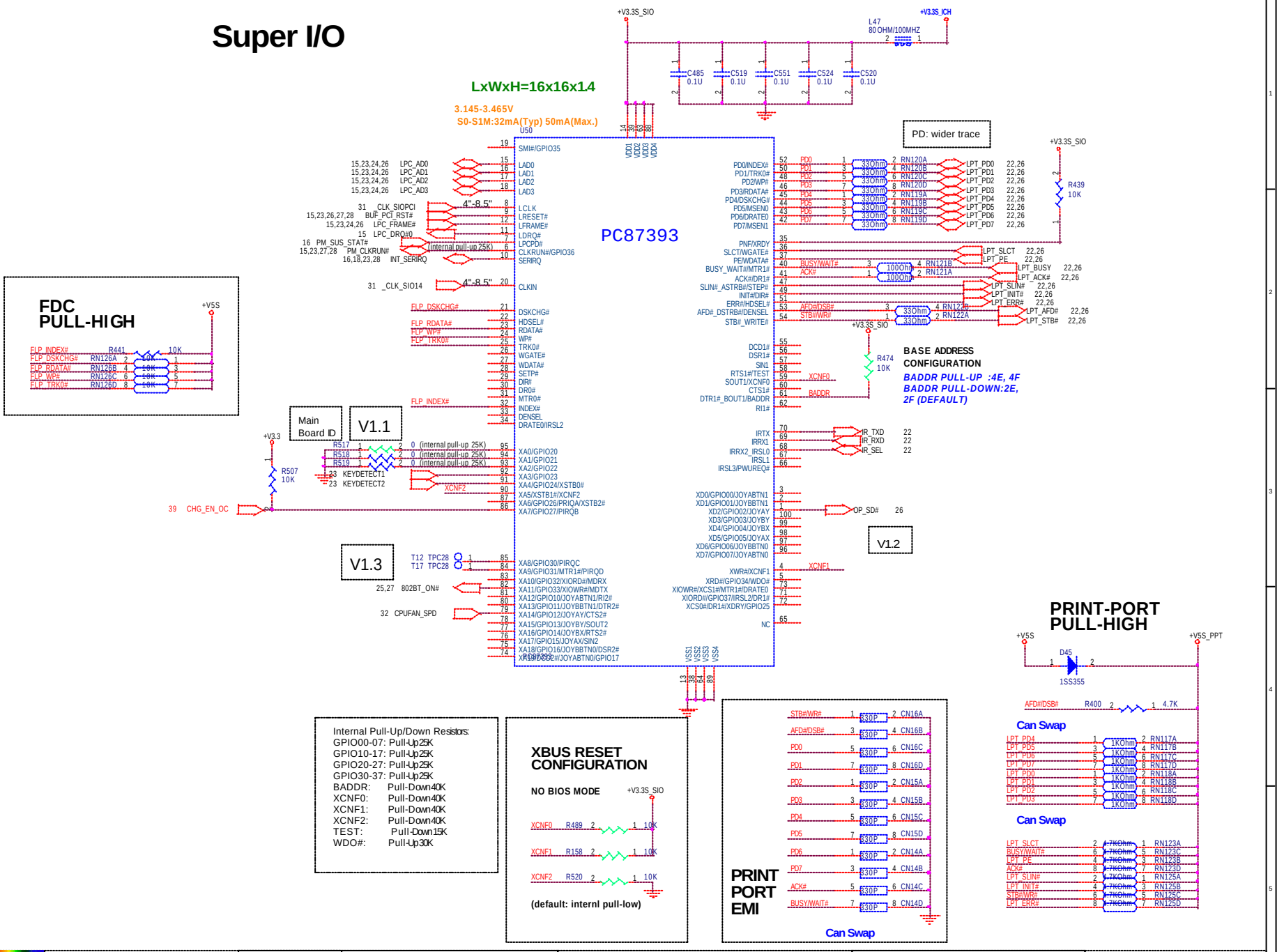




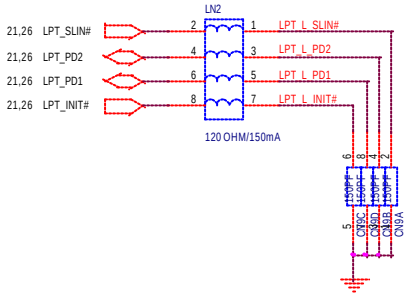
CD-ROM RESET

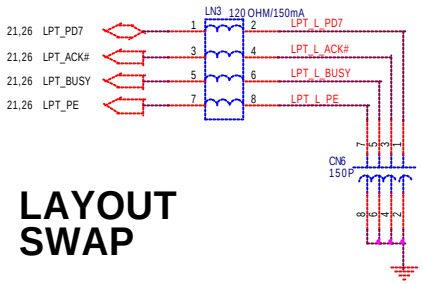
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: CDROM	SCHEMATIC FILE NAME :
		SHEET 20 OF		LIBRARY DATE :
				DESIGN ENGINEER :

Super I/O

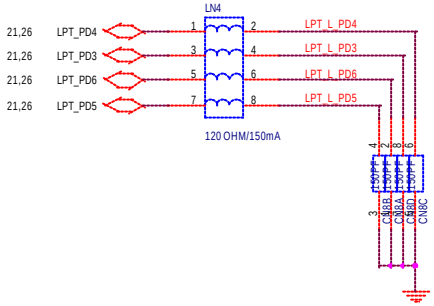


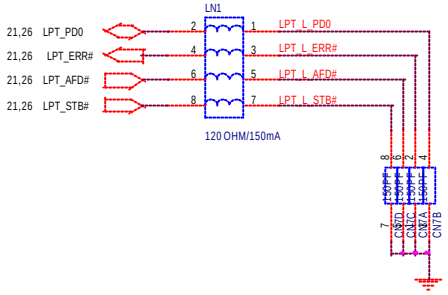
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: SUPER I/O - NS PC87393	SCHEMATIC FILE NAME :
		SHEET 21 OF		LIBRARY DATE :
				DESIGN ENGINEER :



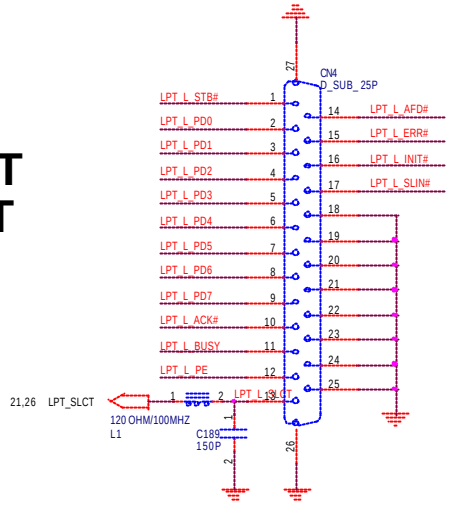


LAYOUT SWAP

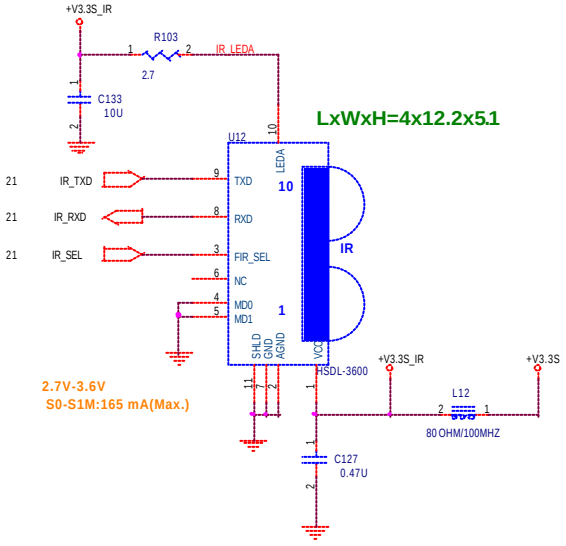




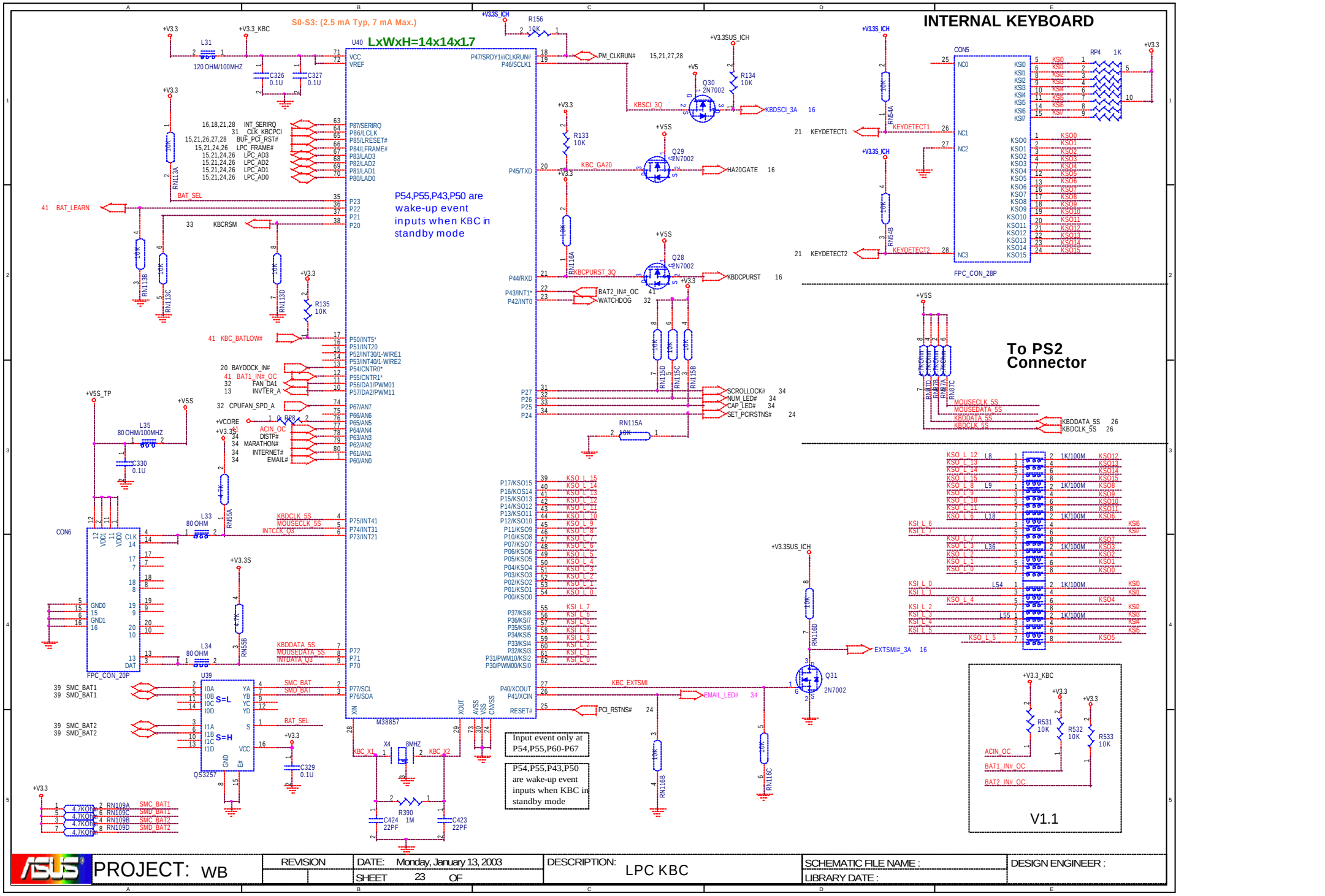
PRINT PORT



IR

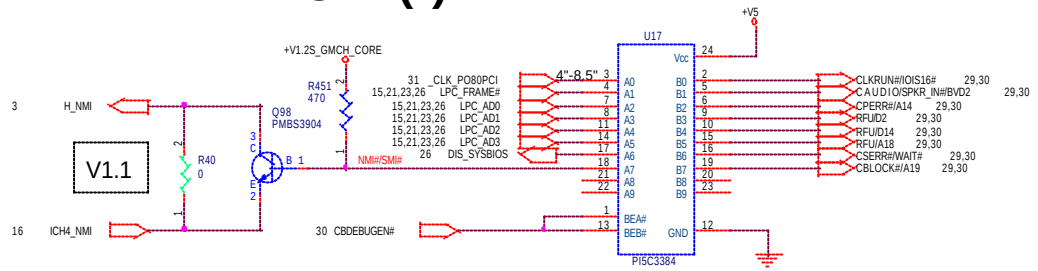


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: IR & LPT PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 22 OF		LIBRARY DATE :	

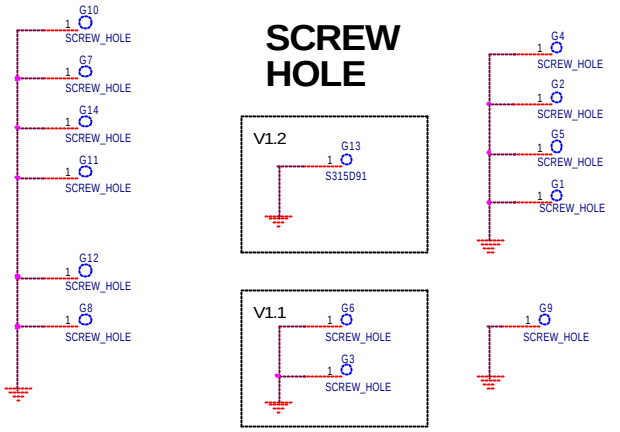


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: LPC KBC	SCHEMATIC FILE NAME :
		SHEET 23 OF		LIBRARY DATE :
				DESIGN ENGINEER :

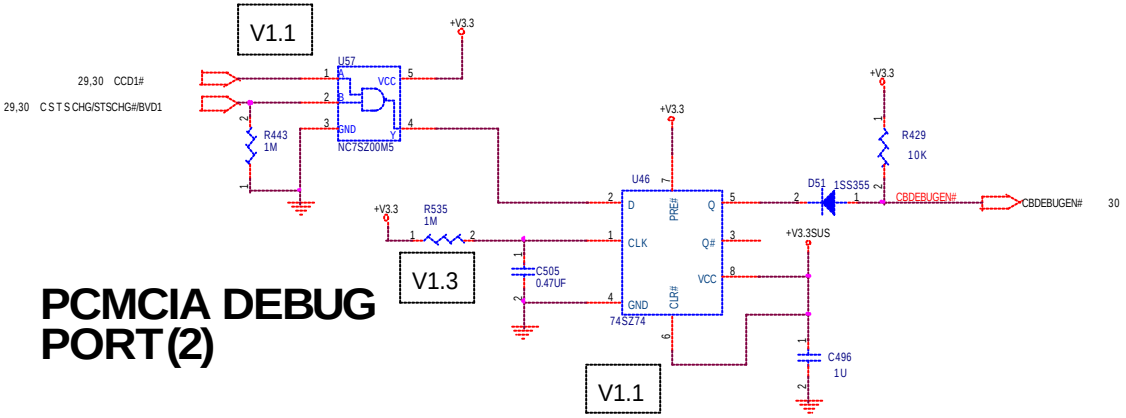
PCMCIA DEBUG PORT(1)



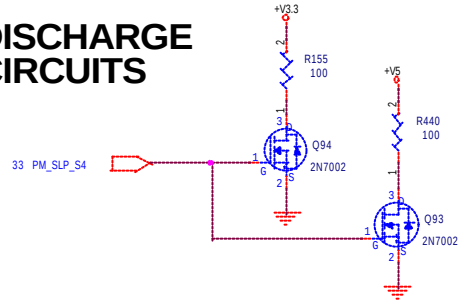
SCREW HOLE



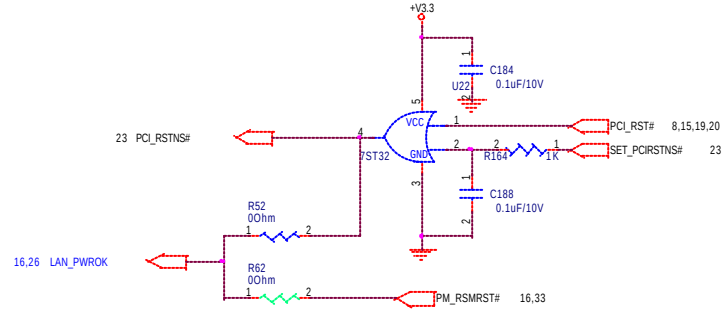
PCMCIA DEBUG PORT(2)



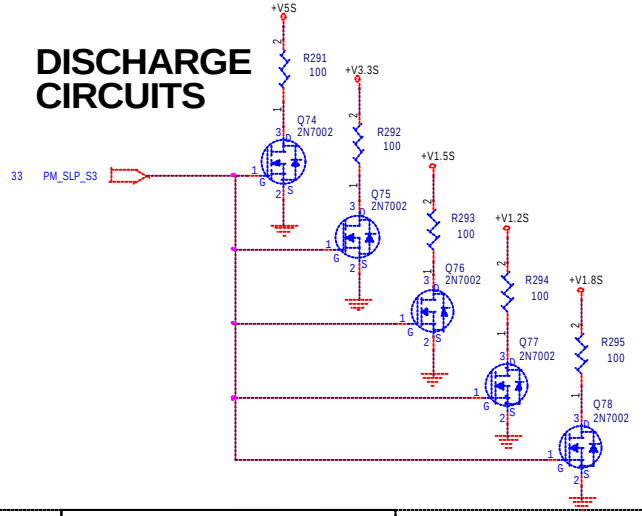
DISCHARGE CIRCUITS



PCI_RSTNS# Gen Circuit



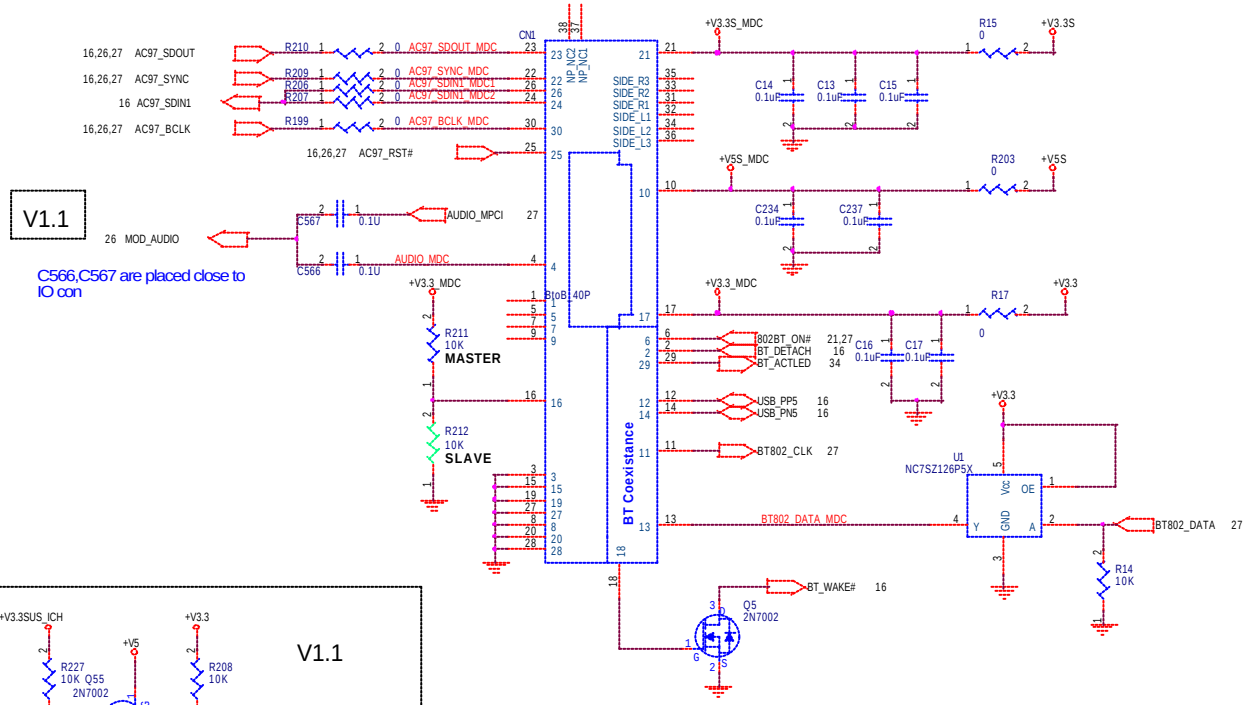
DISCHARGE CIRCUITS



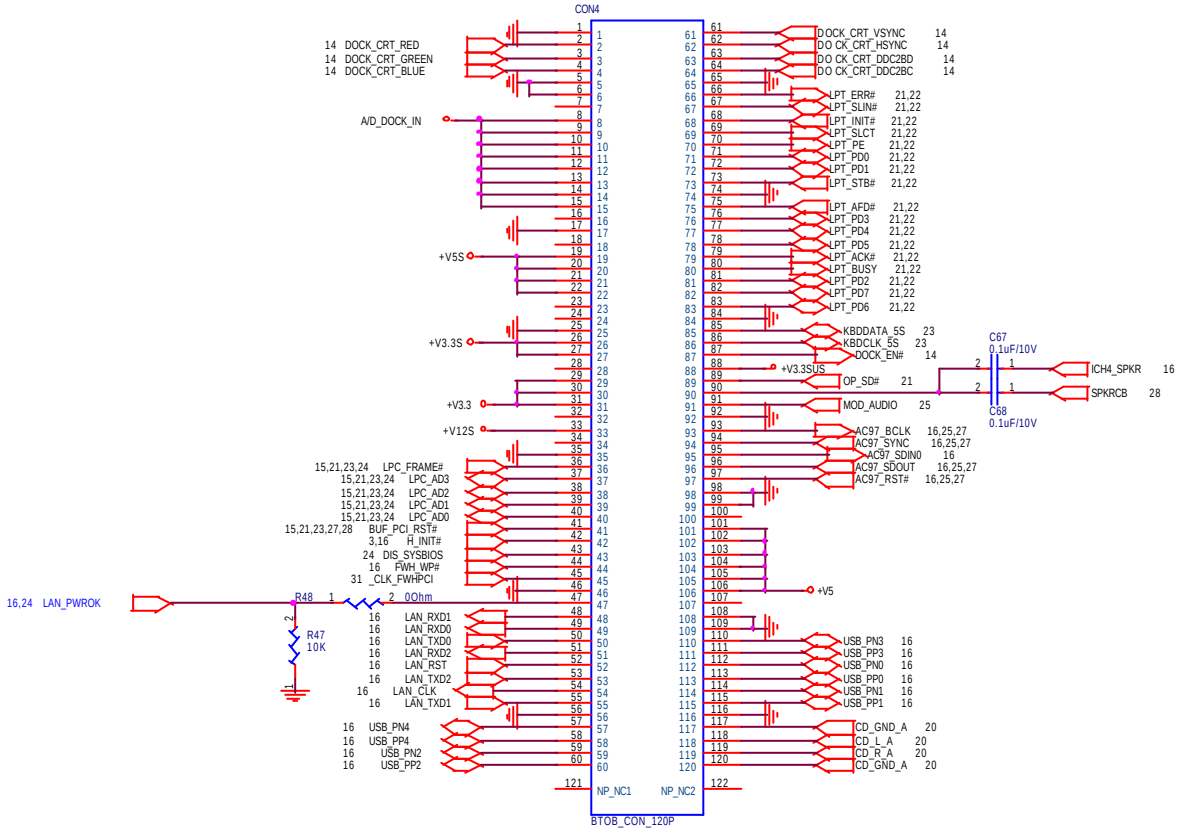
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: SM BUS & HOLES	SCHEMATIC FILE NAME :
		SHEET 24 OF		LIBRARY DATE :
				DESIGN ENGINEER :

AC97	AC97_SDIN0
MDC	AC97_SDIN1
MINIPCI	AC97_SDIN2

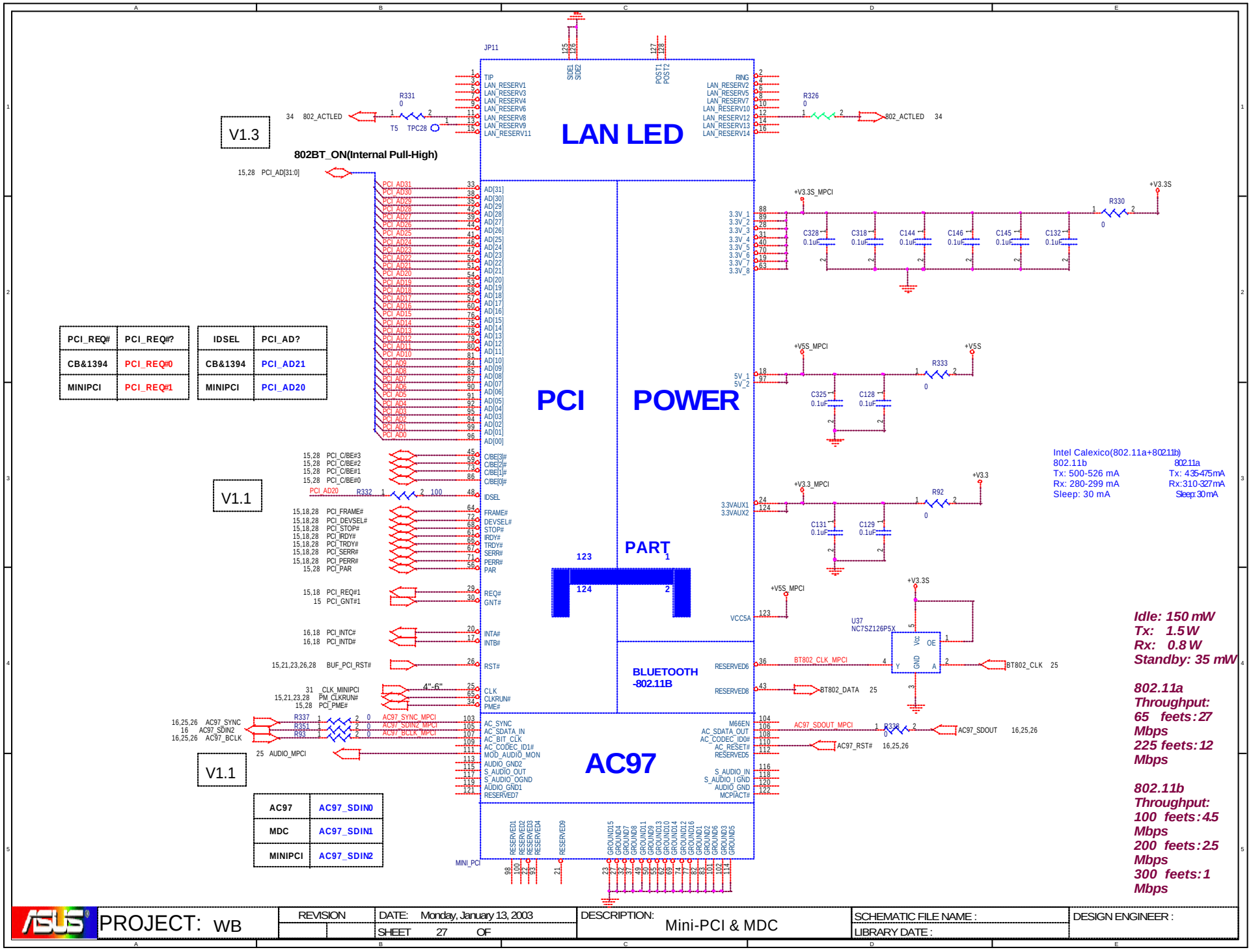
MDC

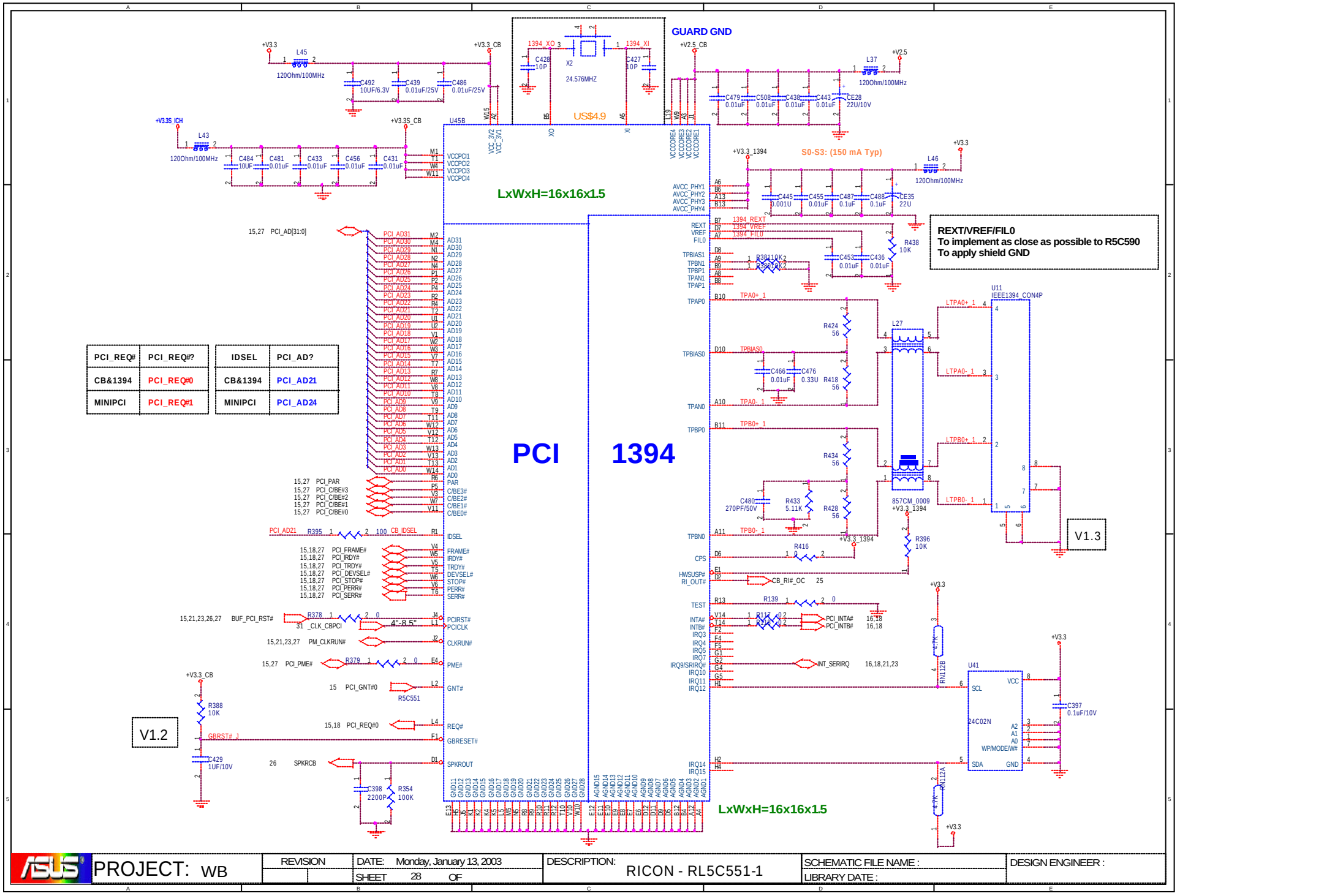


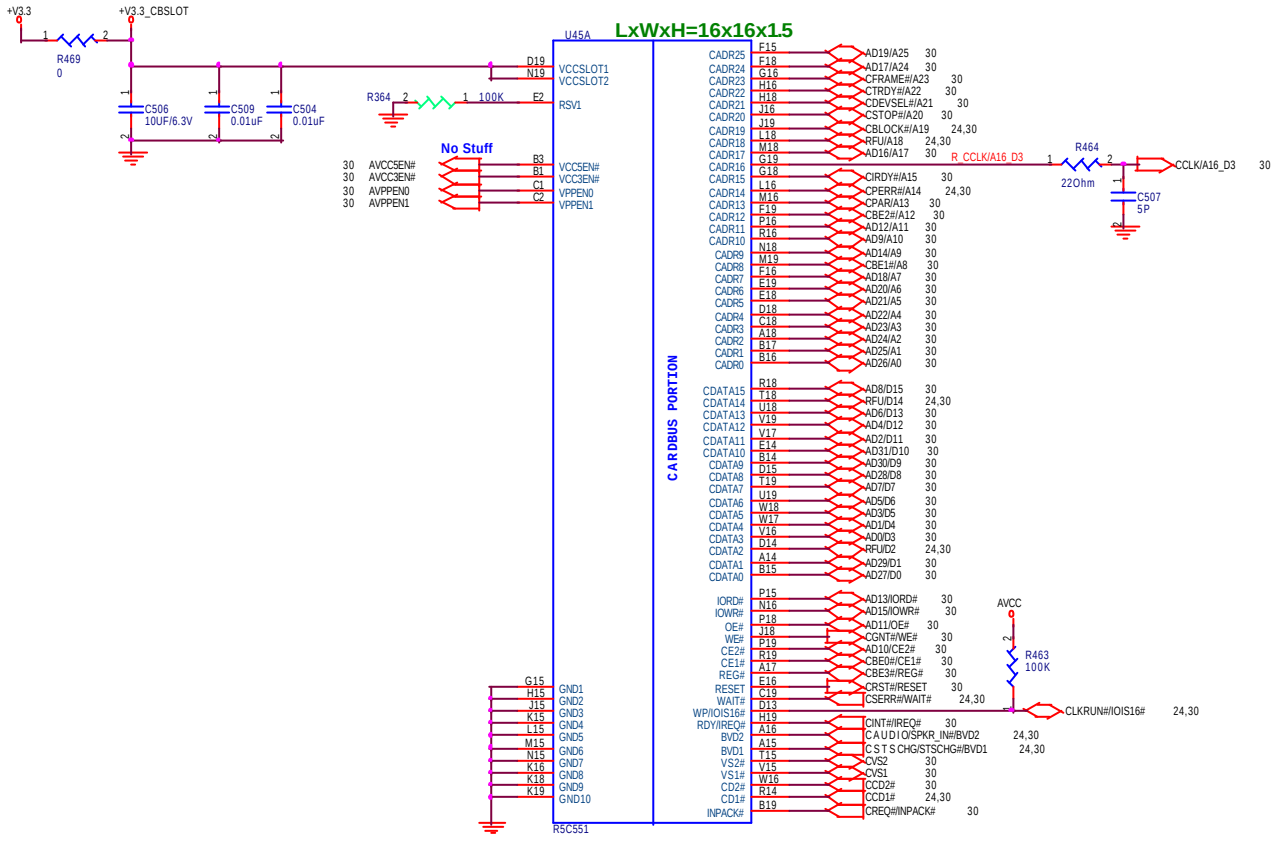
PROJECT: WB	REVISION	DESCRIPTION: MDC	SCHEMATIC FILE NAME :
	DATE: Monday, January 13, 2003		LIBRARY DATE :
	SHEET 25 OF		DESIGN ENGINEER :



PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: IO BOARD	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 26 OF		LIBRARY DATE :	

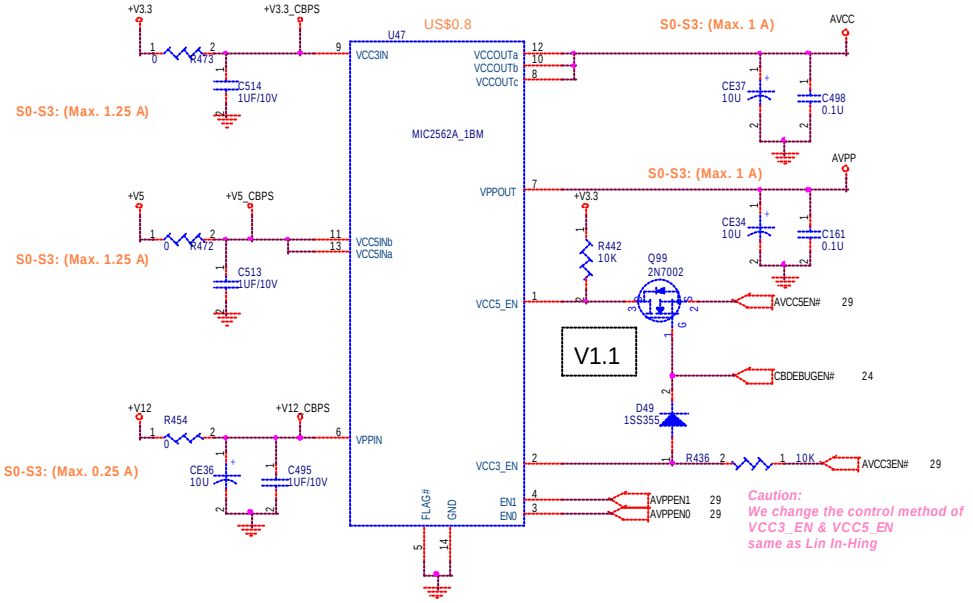

V1.3
802BT_ON(Internal Pull-High)
LAN LED
PCI
POWER
PART 1
BLUETOOTH -802.11B
AC97
V1.1
V1.1
PCI_REQ# | PCI_REQ#?
CB&1394 | PCI_REQ#0
MINIPCI | PCI_REQ#1
IDSEL | PCI_AD?
CB&1394 | PCI_AD21
MINIPCI | PCI_AD20
AC97 | AC97_SDIN0
MDC | AC97_SDIN1
MINIPCI | AC97_SDIN2
Intel Calexico(802.11a+802.11b)
802.11b
Tx: 500-526 mA
Rx: 280-299 mA
Sleep: 30 mA
802.11a
Tx: 435-475mA
Rx:310-327mA
Sleep: 30mA
Idle: 150 mW
Tx: 1.5W
Rx: 0.8 W
Standby: 35 mW
802.11a Throughput:
65 feets:27 Mbps
225 feets:12 Mbps
802.11b Throughput:
100 feets:4.5 Mbps
200 feets:2.5 Mbps
300 feets:1 Mbps
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 27 OF
DESCRIPTION: Mini-PCI & MDC
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :


PCI
1394
GUARD GND
LxWxH=16x16x1.5
LxWxH=16x16x1.5
S0-S3: (150 mA Typ)
REXT/VREF/FIL0
To implement as close as possible to R5C590
To apply shield GND
V1.3
V1.2
PCI_REQ# | PCI_REQ#? | IDSEL | PCI_AD?
CB&1394 | PCI_REQ#0 | CB&1394 | PCI_AD21
MINIPCI | PCI_REQ#1 | MINIPCI | PCI_AD24
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 28 OF
DESCRIPTION: RICON - RL5C551-1
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :

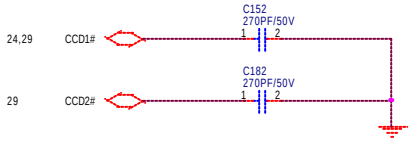


PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 29 OF	RICON - RL5C551-2	LIBRARY DATE :	

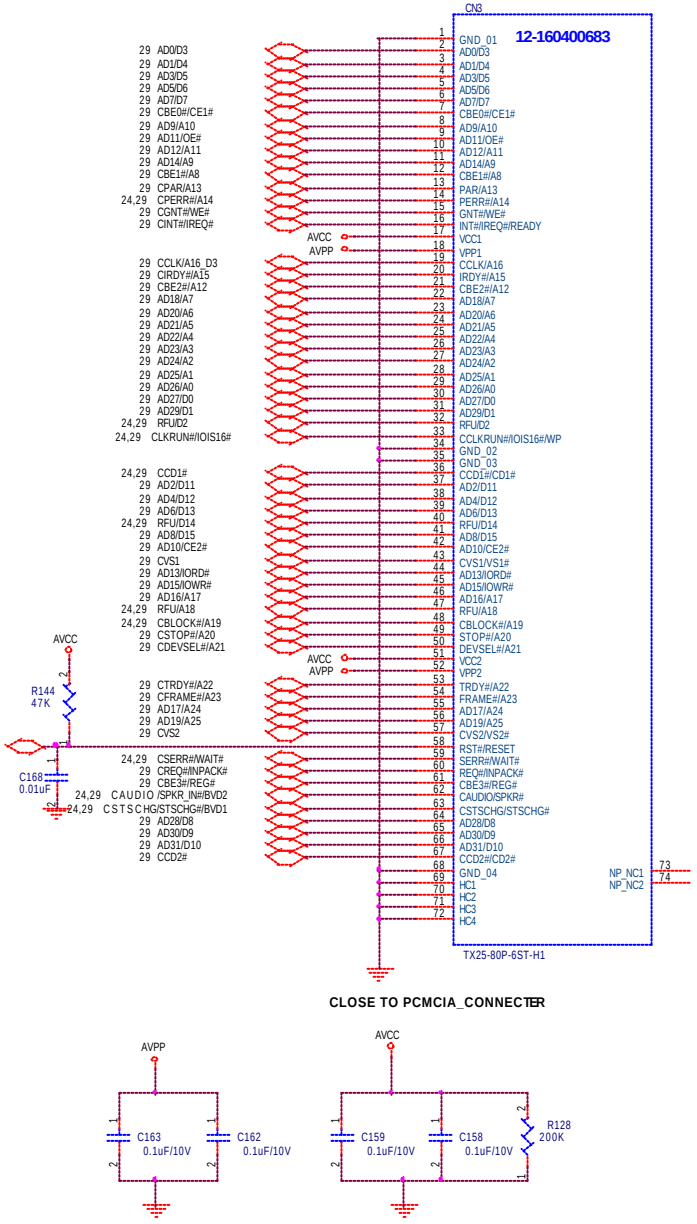
CB POWER SWITCH



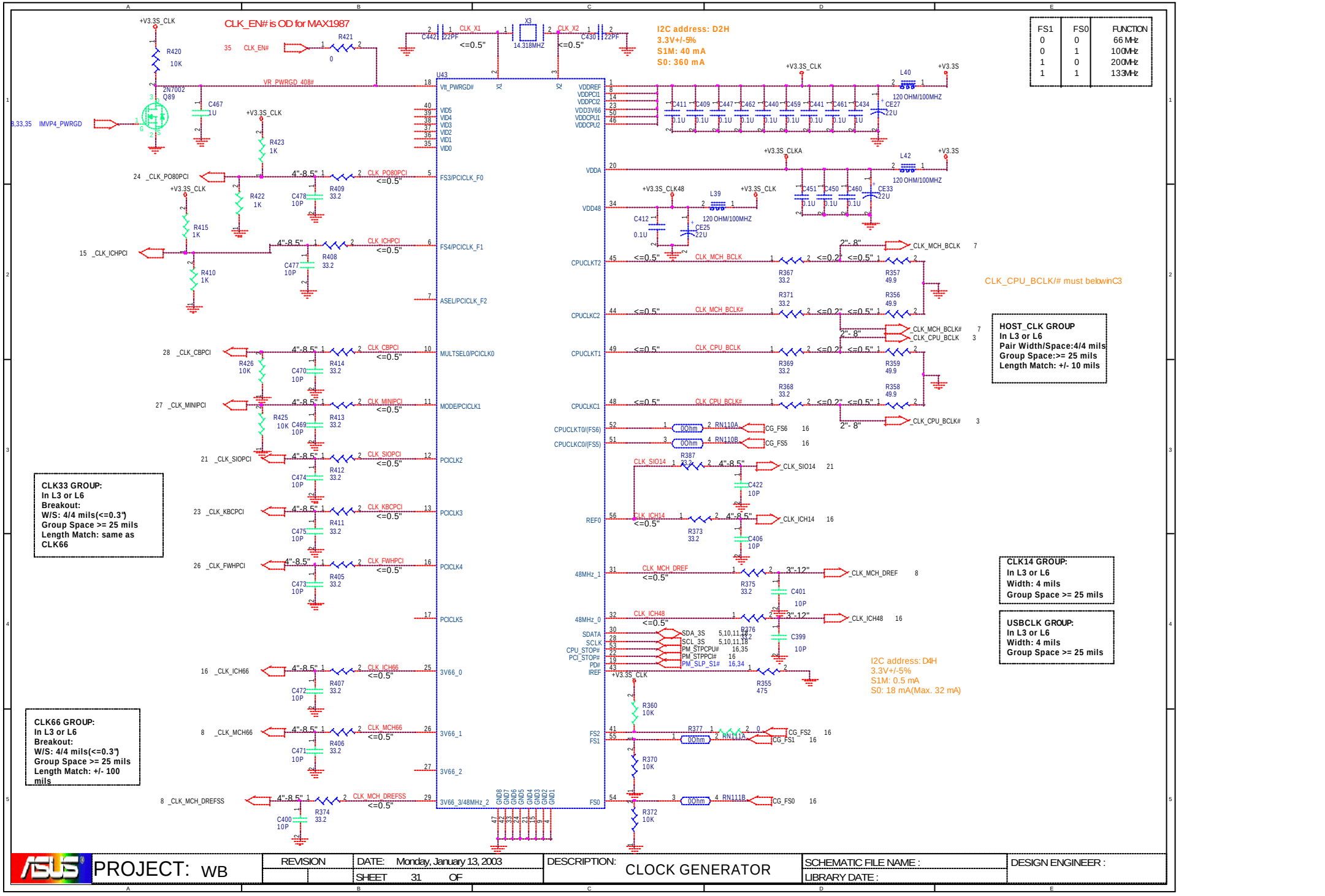
CB DE-BOUNCE



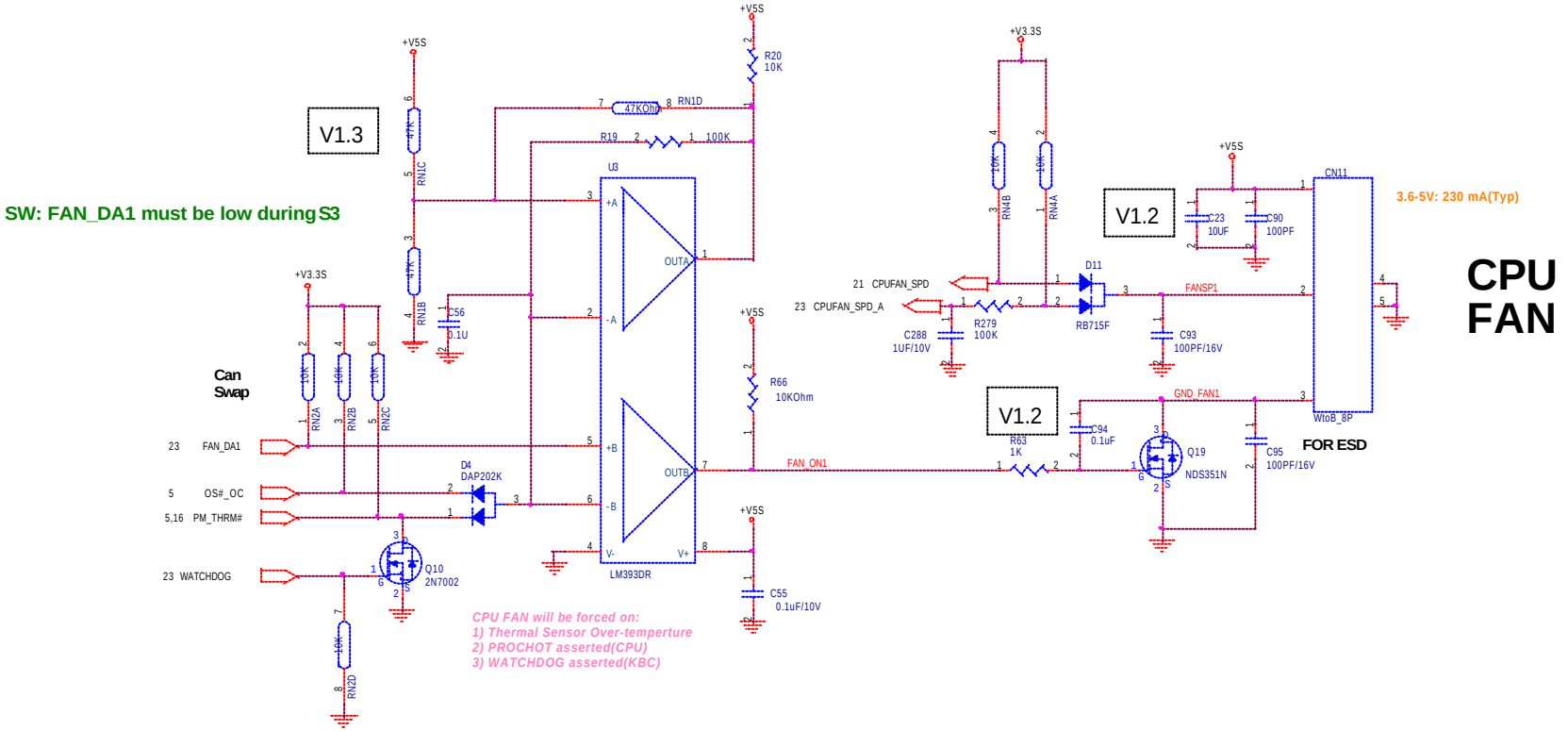
CB SOCKET



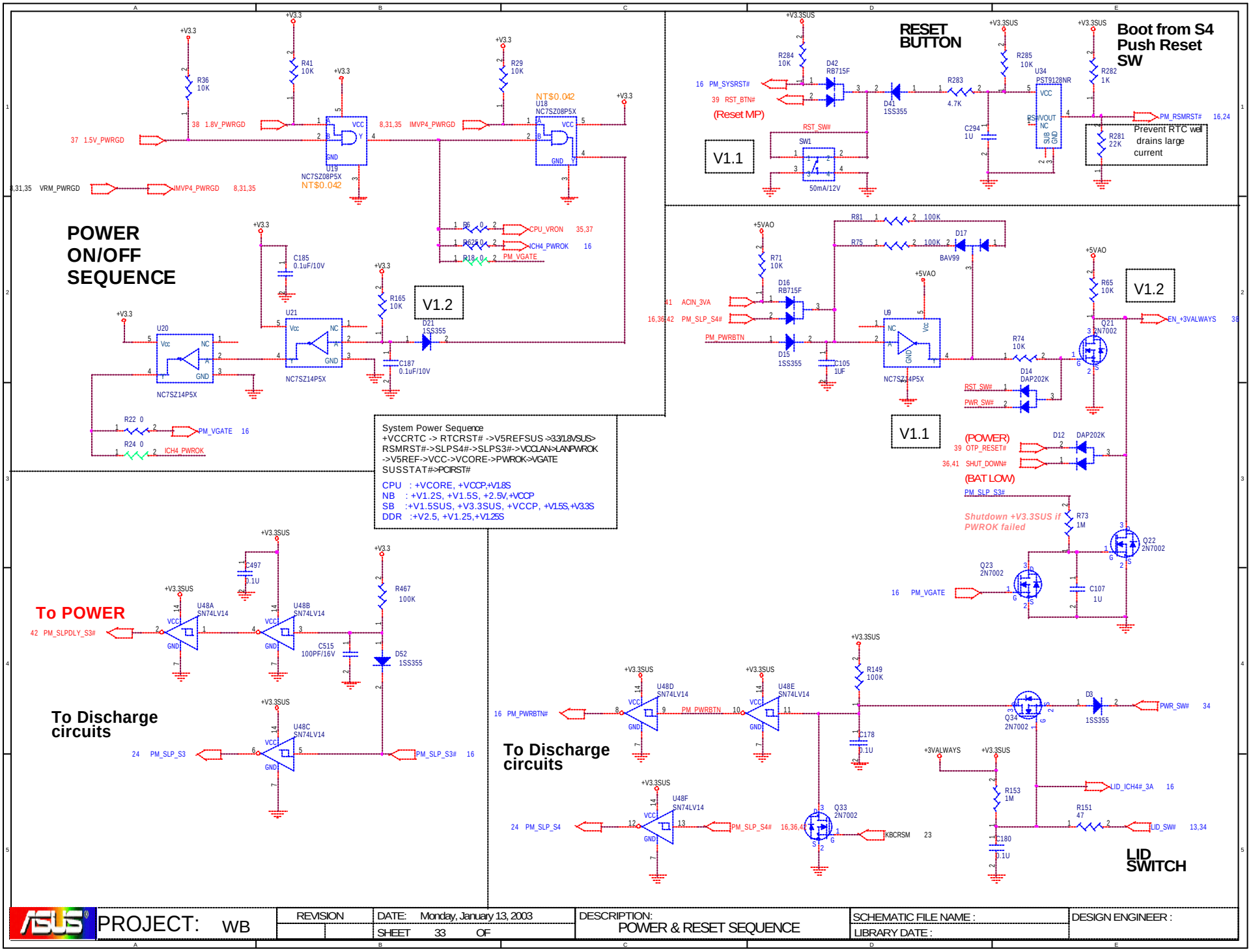
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: CB SOCKET & PWR	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 30 OF		LIBRARY DATE :	


CLK_EN# is OD for MAX1987
I2C address: D2H
3.3V+/-5%
S1M: 40 mA
S0: 360 mA
FS1 FS0 FUNCTION
0 0 66 MHz
0 1 100MHz
1 0 200MHz
1 1 133MHz
CLK33 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3')
Group Space >= 25 mils
Length Match: same as CLK66
CLK66 GROUP:
In L3 or L6
Breakout:
W/S: 4/4 mils(<=0.3')
Group Space >= 25 mils
Length Match: +/- 100 mils
HOST_CLK GROUP
In L3 or L6
Pair Width/Space:4/4 mils
Group Space:>= 25 mils
Length Match: +/- 10 mils
CLK_CPU_BCLK/# must belowinC3
CLK14 GROUP:
In L3 or L6
Width: 4 mils
Group Space >= 25 mils
USBCLK GROUP:
In L3 or L6
Width: 4 mils
Group Space >= 25 mils
I2C address: D4H
3.3V+/-5%
S1M: 0.5 mA
S0: 18 mA(Max. 32 mA)
U43
14.318MHZ
VR_PWRGD_408#
IMVP4_PWRGD
CLK_CPO80PCI
CLK_ICHPCI
CLK_CBPCI
CLK_MINIPCI
CLK_SIOPCI
CLK_KBCPCI
CLK_FWHPCI
CLK_ICH66
CLK_MCH66
CLK_MCH_DREFSS
CLK_MCH_BCLK
CLK_MCH_BCLK#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_DREF
CLK_ICH48
CLK_ICH14
SDA_3S
SCL_3S
PM_STPCPU#
PM_STPPCI#
PM_SLP_S1#
CG_FS6
CG_FS5
CG_FS2
CG_FS1
CG_FS0
PROJECT: WB
REVISION
DATE: Monday, January 13, 2003
SHEET 31 OF
DESCRIPTION: CLOCK GENERATOR
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :

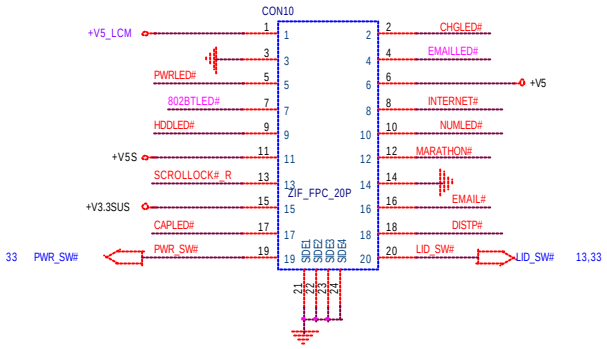
Fan Speed Control

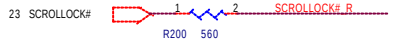


PROJECT: WB	REVISION	DESCRIPTION: FAN	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	DATE: Monday, January 13, 2003		LIBRARY DATE :	
	SHEET 32 OF			

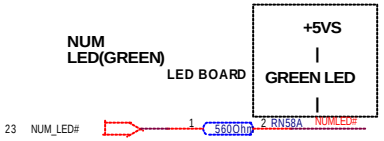


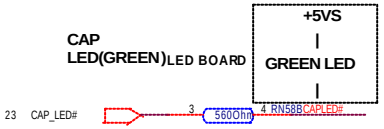
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: POWER & RESET SEQUENCE	SCHEMATIC FILE NAME :
		SHEET 33 OF		LIBRARY DATE :
				DESIGN ENGINEER :

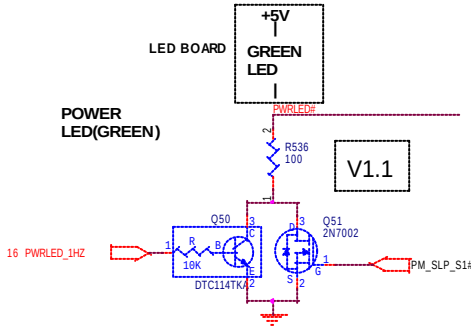


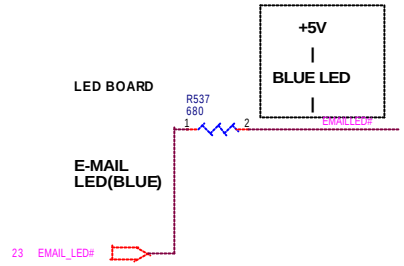


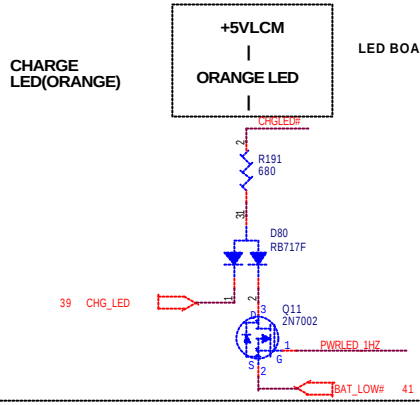
LED

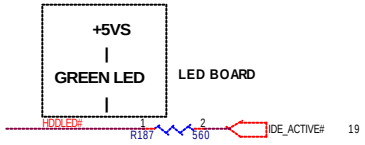


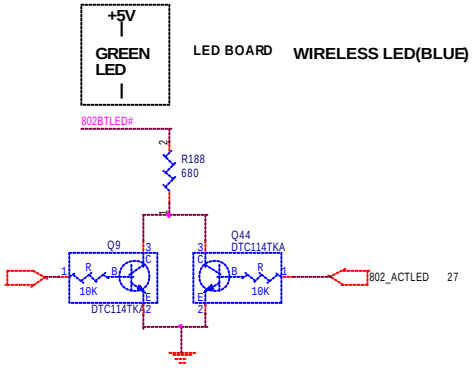




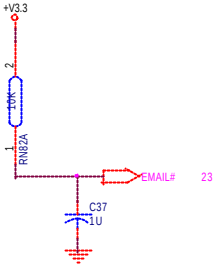


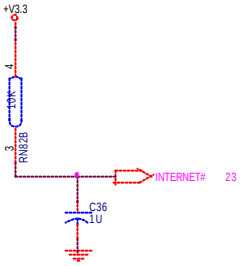


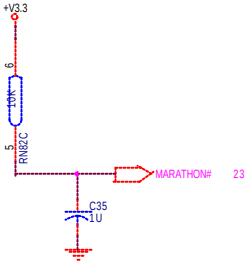


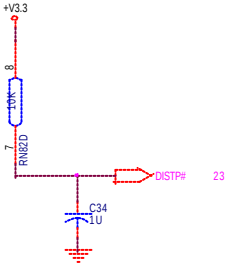


INSTANT KEY

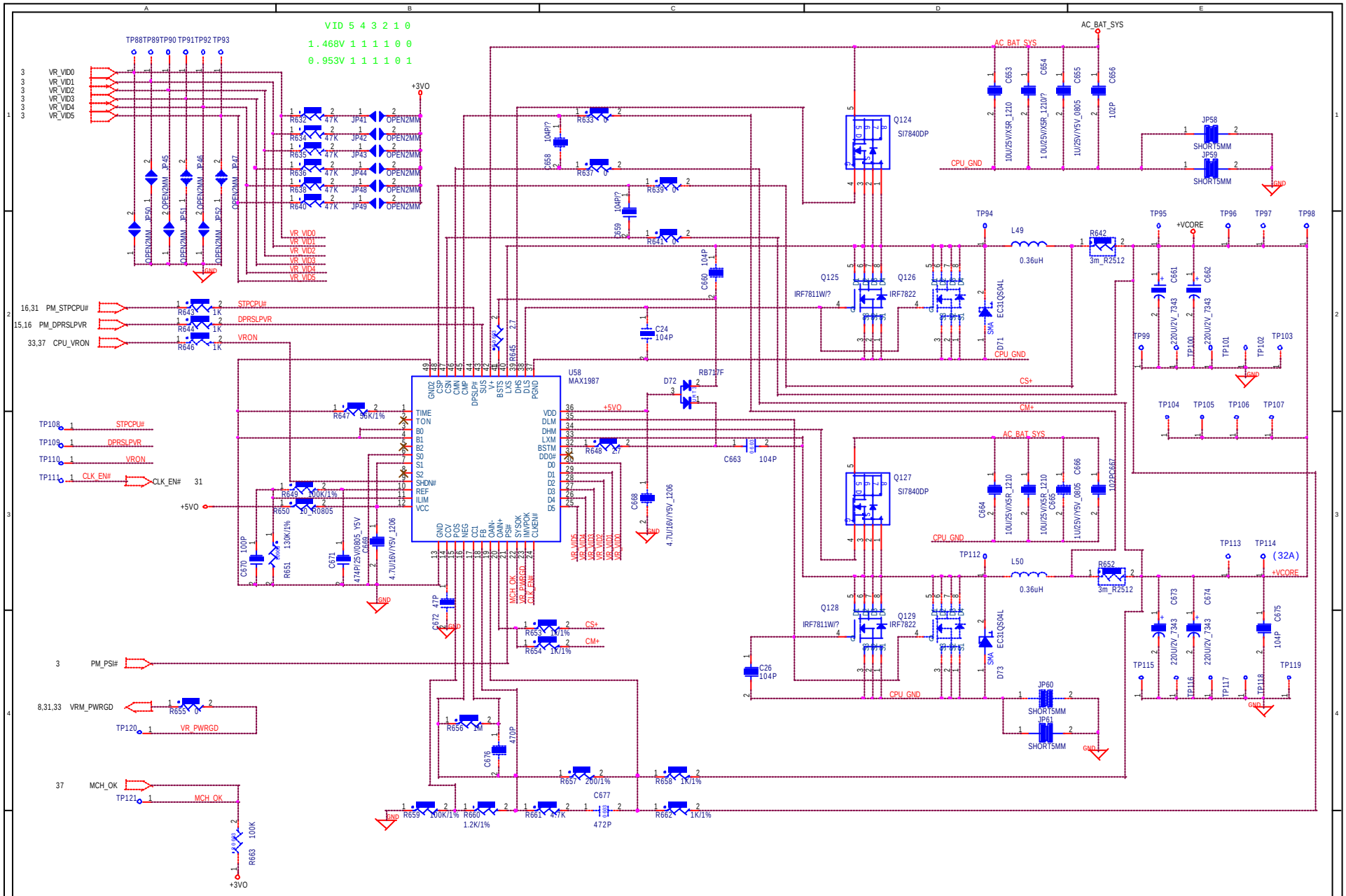




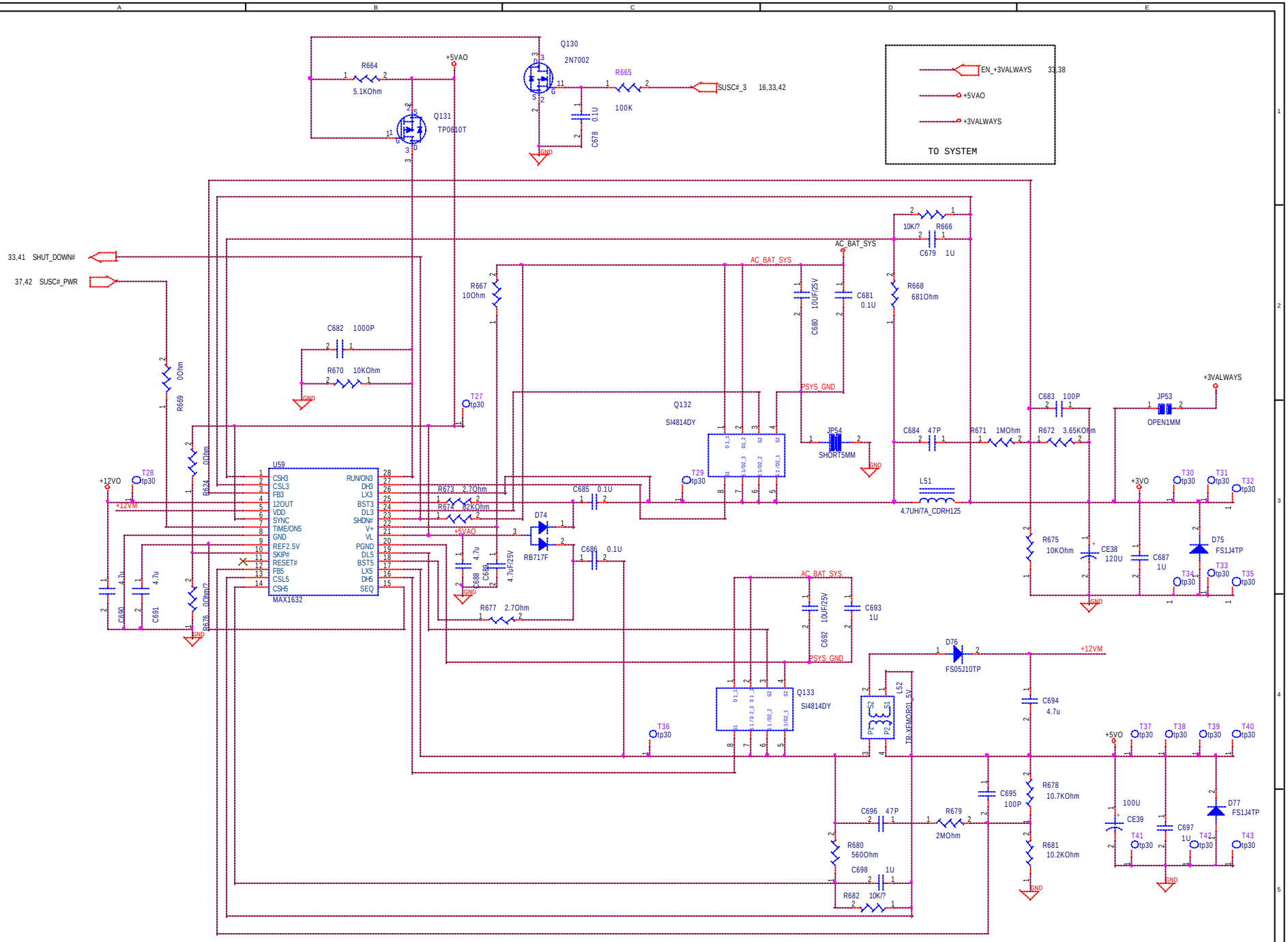




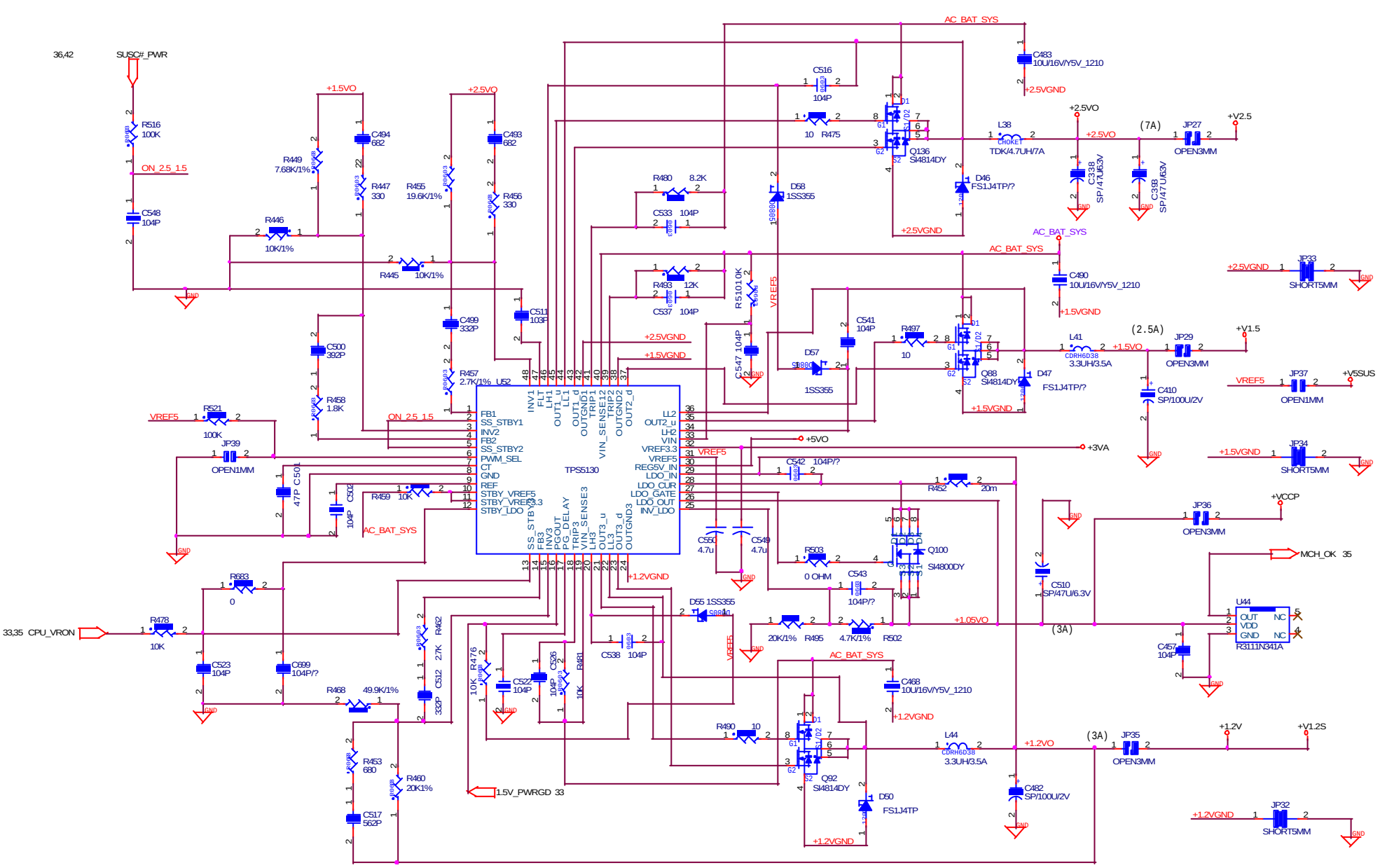
PROJECT: WB	REVISION	DATE: Monday, January 13, 2003	DESCRIPTION: LED BOARD	SCHEMATIC FILE NAME :
		SHEET 34 OF		LIBRARY DATE :
				DESIGN ENGINEER :



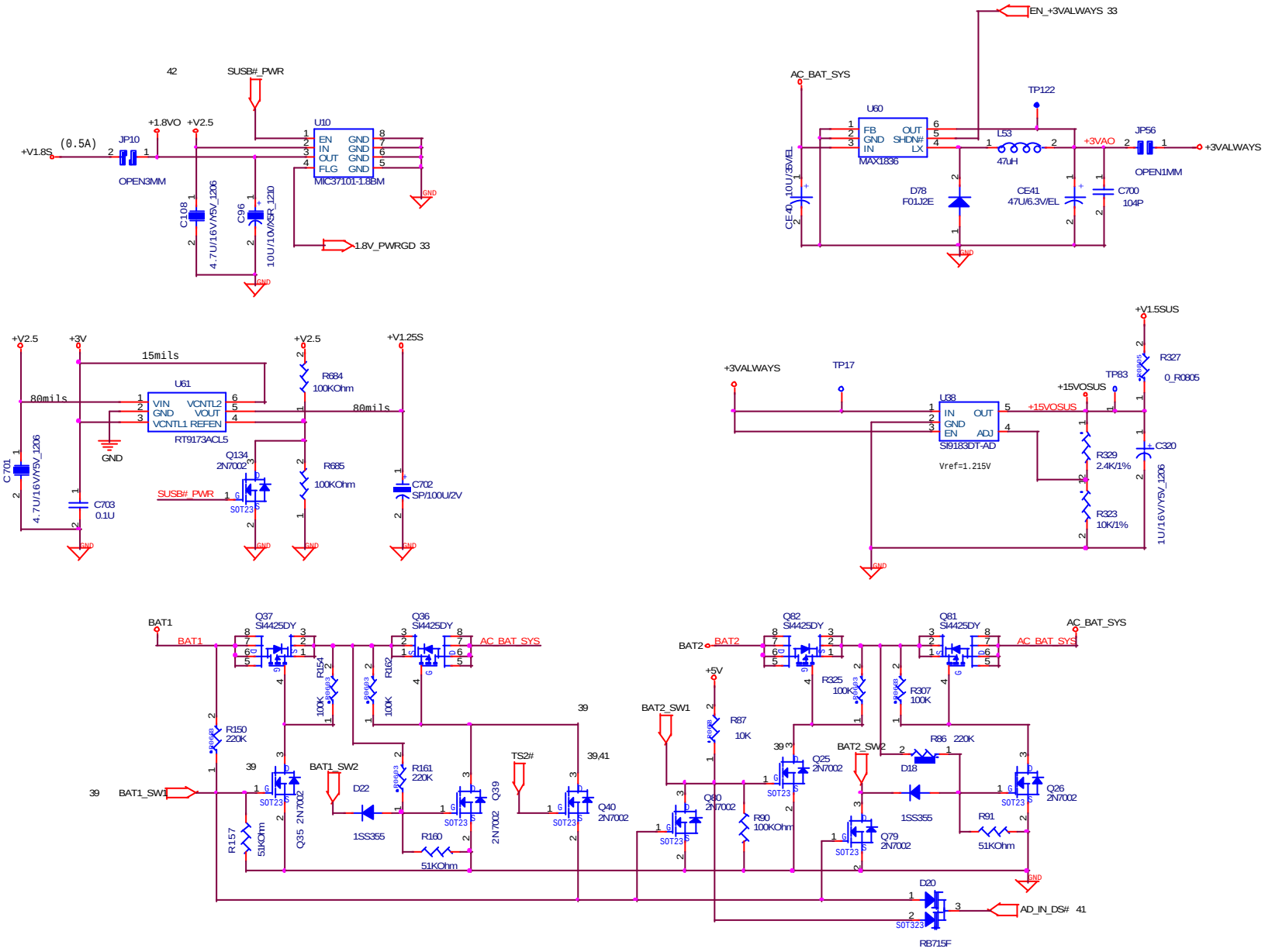
PROJECT: WB	REVISION 1.1	DATE: Monday, January 13, 2003	DESCRIPTION: Vcore
		SHEET 35 OF 42	SCHEMATIC FILE NAME :
			LIBRARY DATE :
			DESIGN ENGINEER :



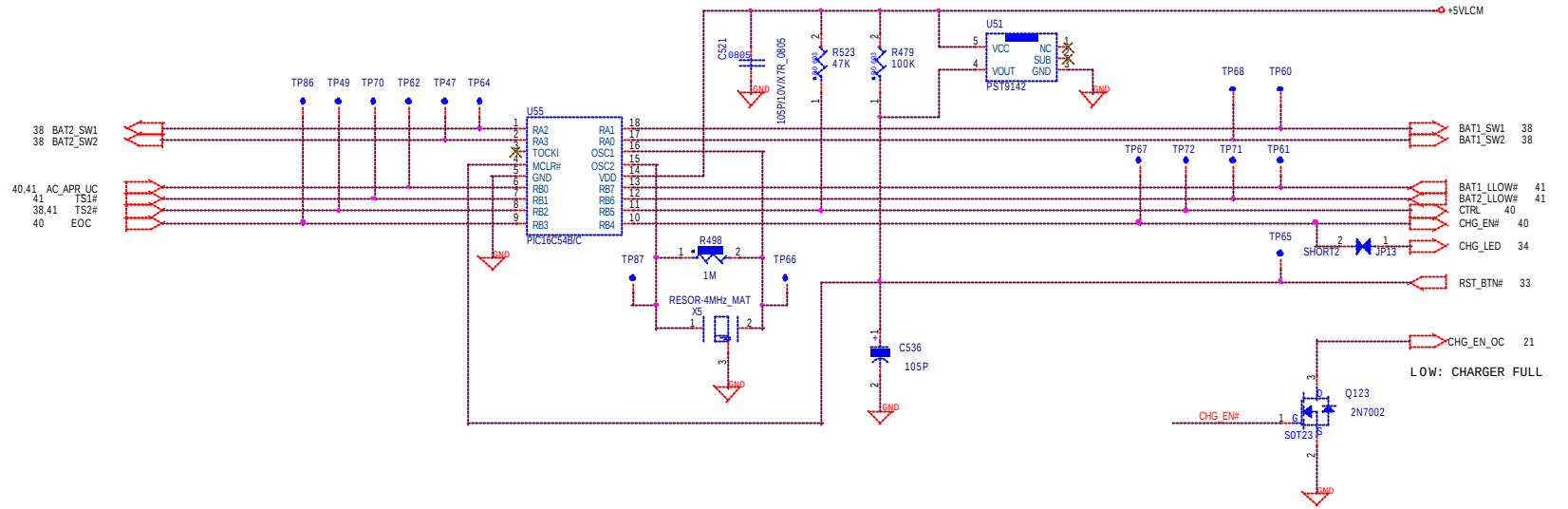
PROJECT: WB	REVISION 1.0	DATE: Monday, January 13, 2003	DESCRIPTION: SYSTEM	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 36 OF 42		LIBRARY DATE :	

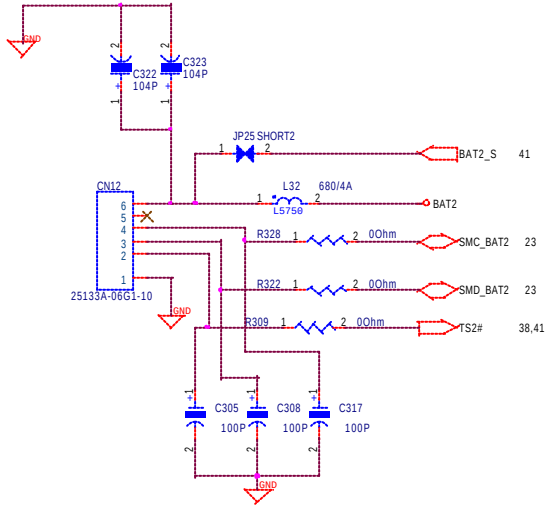


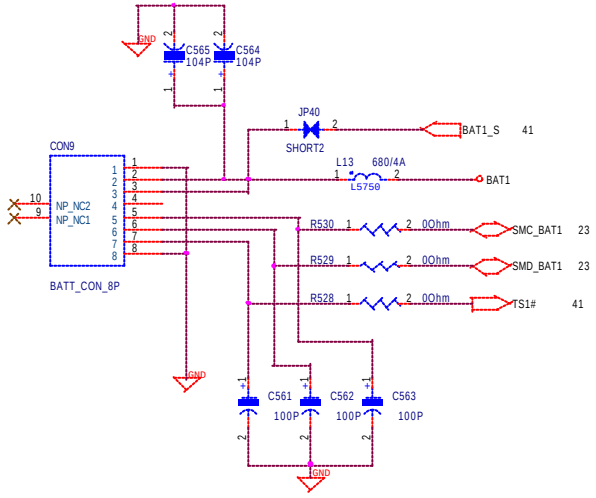
PROJECT: WB	REVISION 1.0	DATE: Monday, January 13, 2003	DESCRIPTION: 2.5V_1.5V_1.2V_1.05V	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 37 OF 42		LIBRARY DATE :	

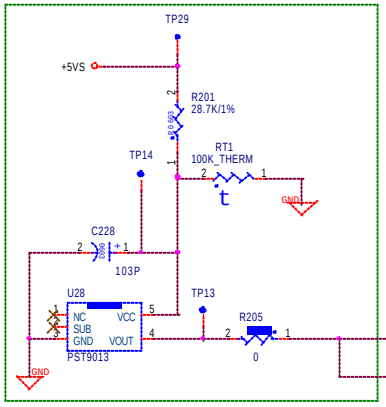


PROJECT: WB	REVISION 1.0	DATE: Monday, January 13, 2003	DESCRIPTION: 1.25V 1.8V 1.5SUS DISCHG	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 38 OF 42		LIBRARY DATE :	



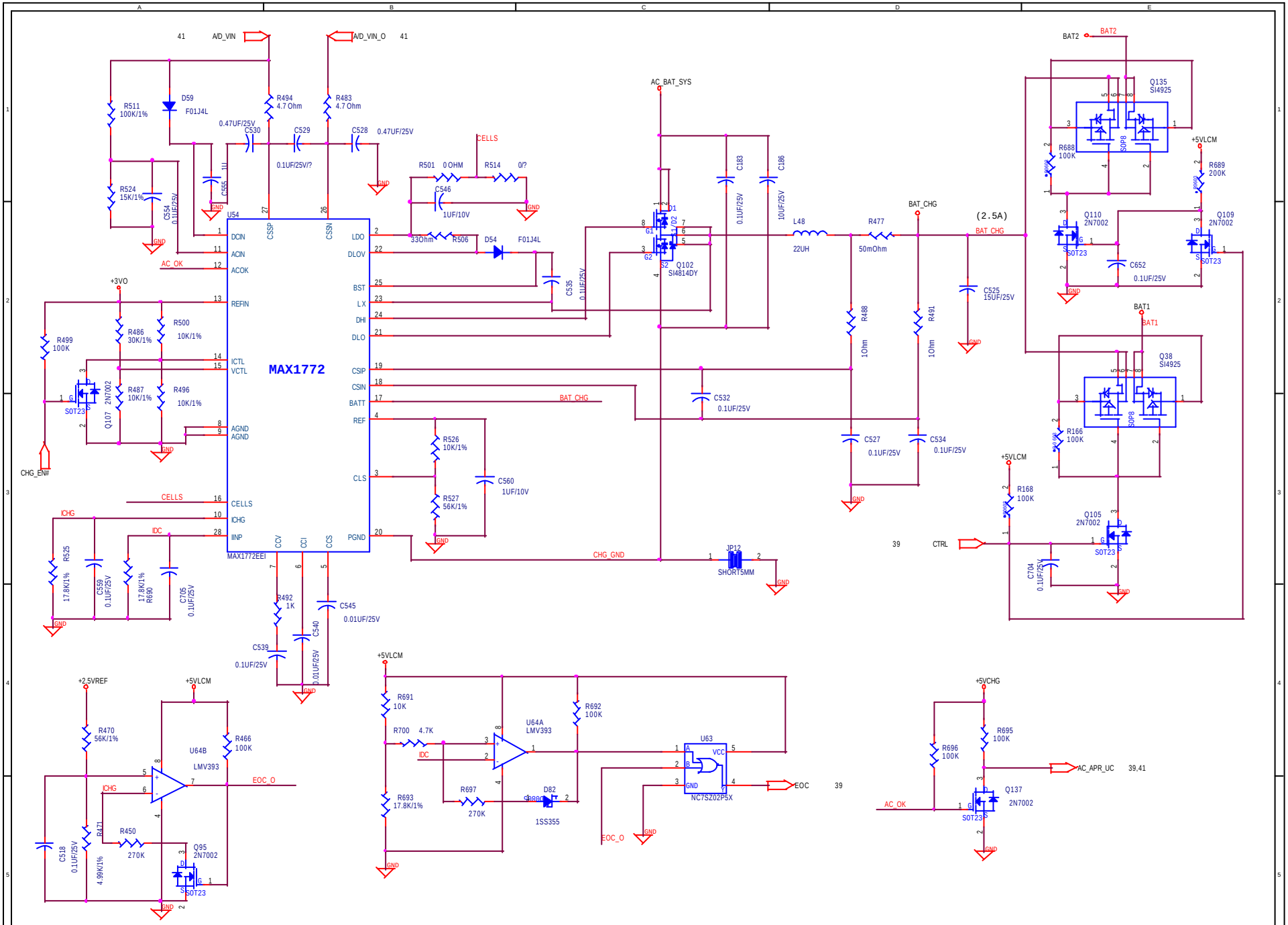




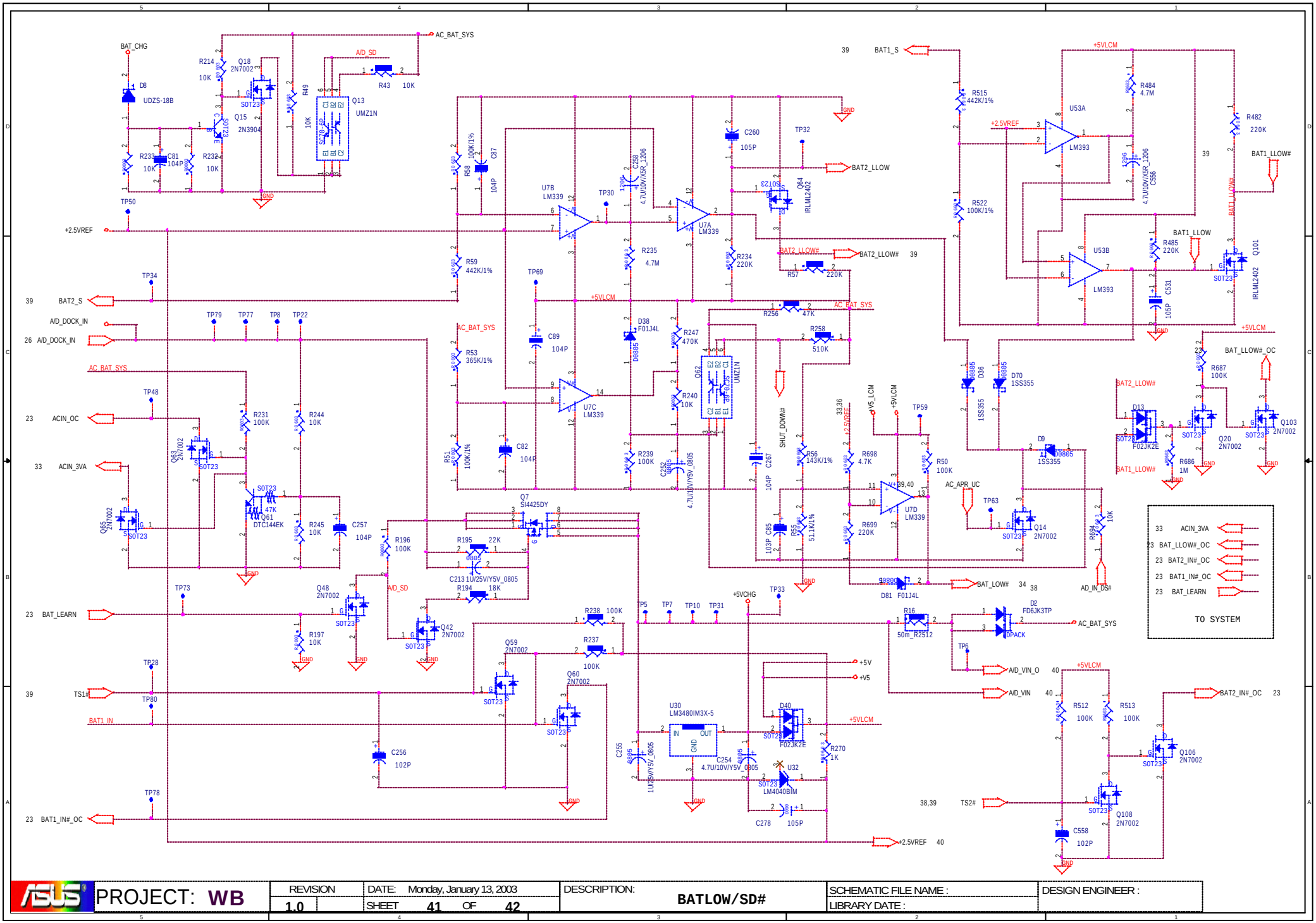


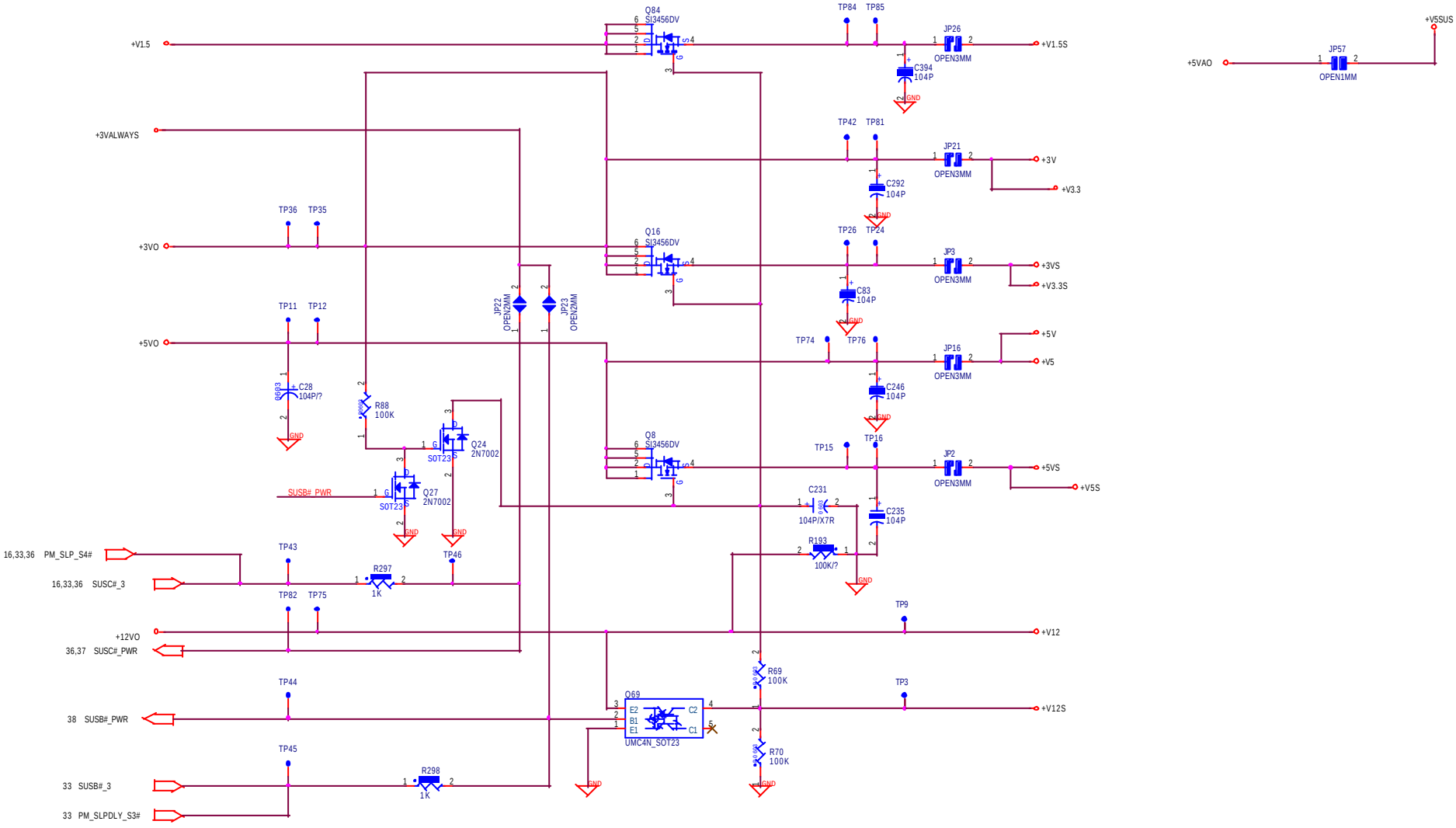
80 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU

PROJECT: WB	REVISION 1.0	DATE: Monday, January 13, 2003	DESCRIPTION: PIC16C54	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 39 OF 42		LIBRARY DATE :	



PROJECT: WB	REVISION 1.2	DATE: Monday, January 13, 2003	DESCRIPTION: CHARGER	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 40 OF 42		LIBRARY DATE :	


BAT_CHG
AC_BAT_SYS
A/D_SD
BAT1_S
+5VLCM
+2.5VREF
BAT2_LLOW
BAT2_LLOW#
BAT1_LLOW
BAT1_LLOW#
BAT_LLOW#_OC
+5VCHG
+5V
+V5
BAT_LOW#
AD_IN_DS#
AC_APR_UC
SHUT_DOWN#
A/D_DOCK_IN
ACIN_OC
ACIN_3VA
BAT_LEARN
BAT1_IN
BAT1_IN#_OC
BAT2_S
BAT2_IN#_OC
TS1#
TS2#
A/D_VIN_O
A/D_VIN
AC_BAT_SYS
TO SYSTEM
33 ACIN_3VA
23 BAT_LLOW#_OC
23 BAT2_IN#_OC
23 BAT1_IN#_OC
23 BAT_LEARN
PROJECT: WB
REVISION 1.0
DATE: Monday, January 13, 2003
SHEET 41 OF 42
DESCRIPTION: BATLOW/SD#
SCHEMATIC FILE NAME :
LIBRARY DATE :
DESIGN ENGINEER :



PROJECT: WB	REVISION 1.0	DATE: Monday, January 13, 2003	DESCRIPTION: LOAD SWITCH	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET 42 OF 42		LIBRARY DATE :	