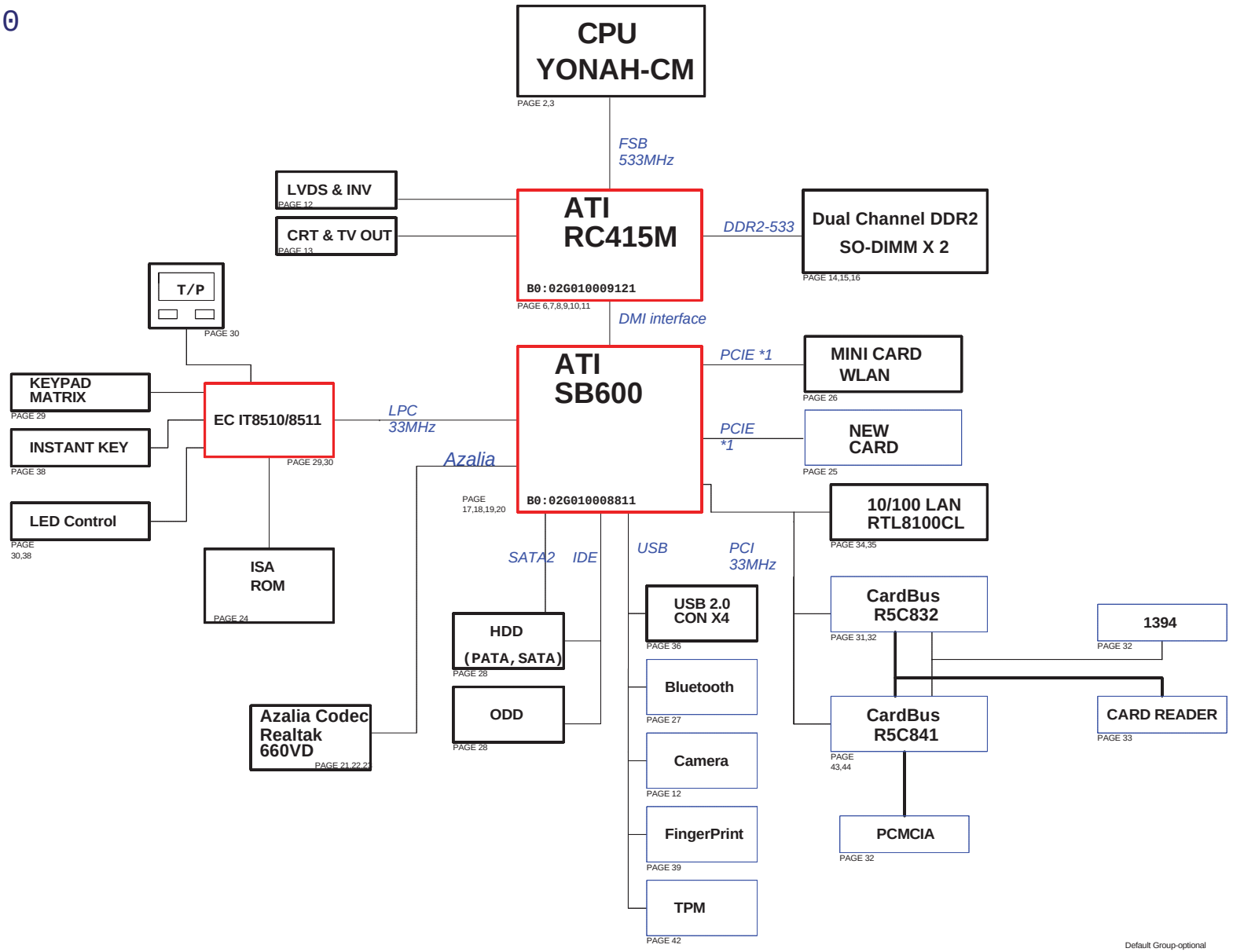
T12R Block Diagram

V2.0



Default Group-optional

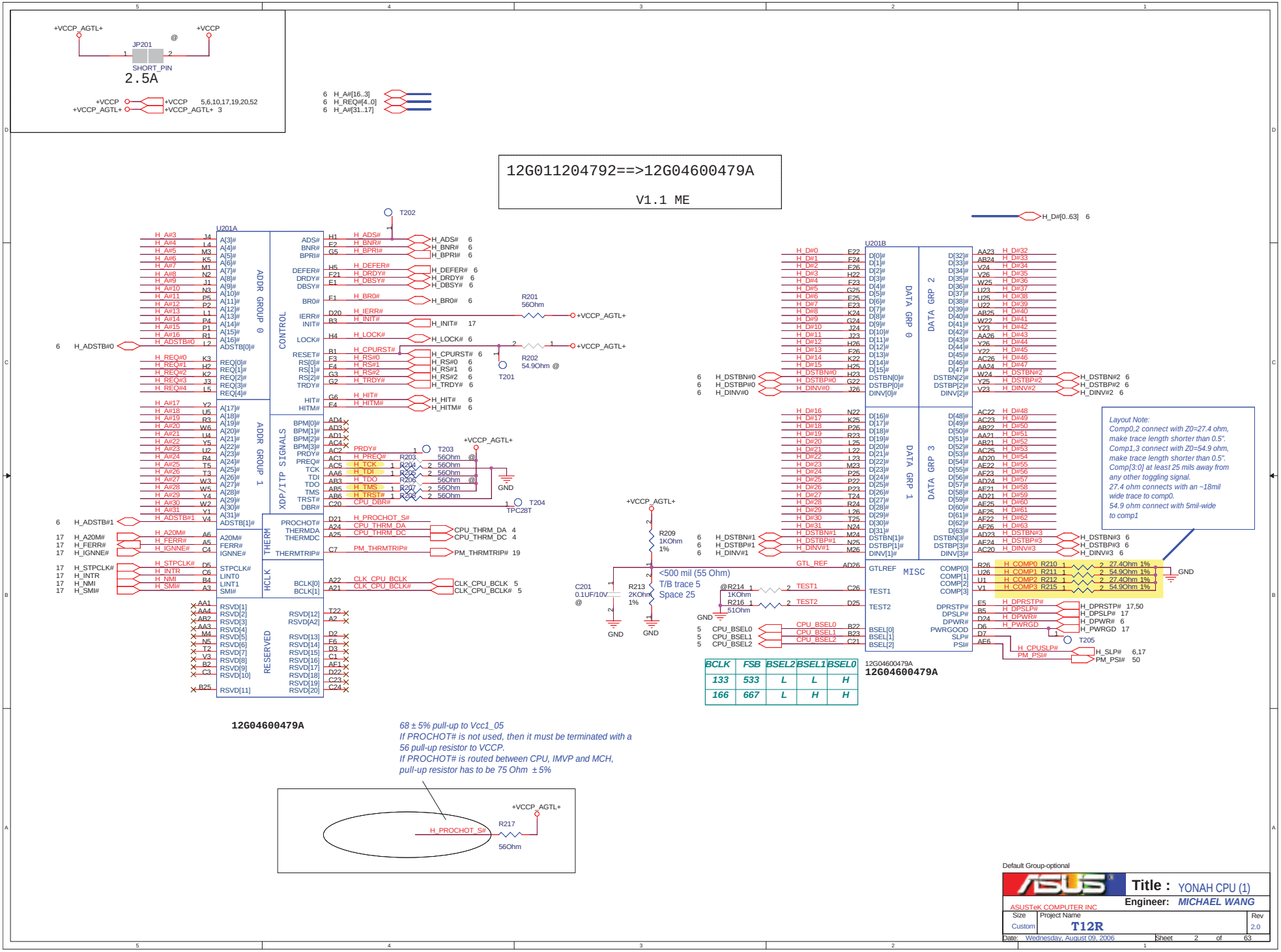
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 1 of 63



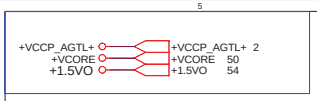
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

68 ± 5% pull-up to Vcc1_05
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%

Layout Note:
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
Comp[3:0] at least 25 mils away from any other toggling signal.
27.4 ohm connects with an ~18mil wide trace to comp0.
54.9 ohm connect with 5mil-wide to comp1

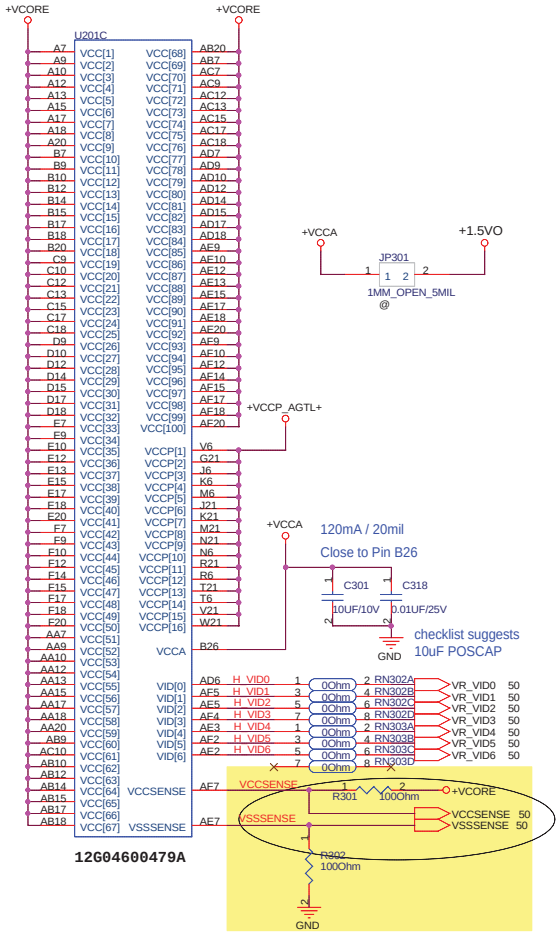
Default Group-optional

ASUSTeK COMPUTER INC	Title : YONAH CPU (1)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 2 of 63	

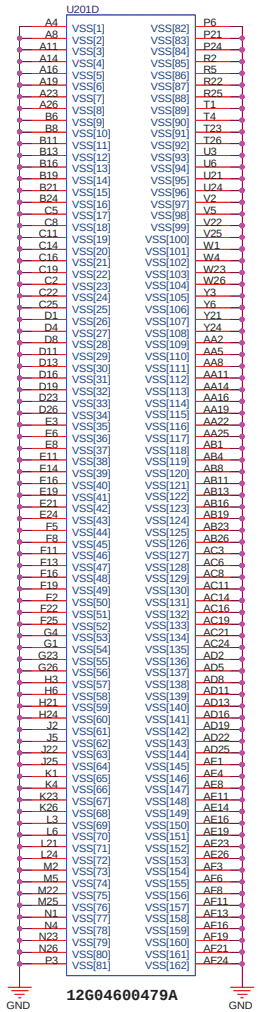


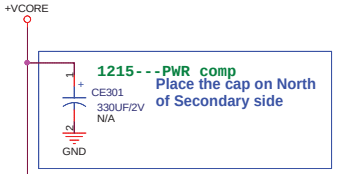
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

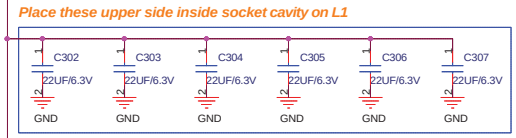


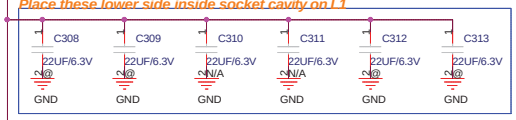
Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

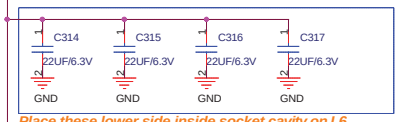


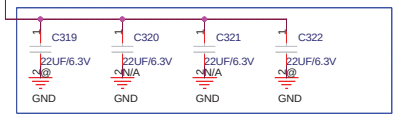


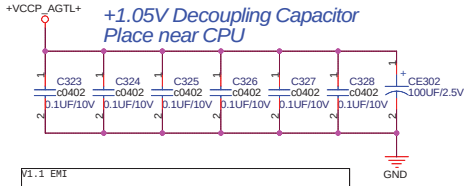
Vcc Core Decoupling Caps
Primary side => Bottom side
Secondary side => Top side

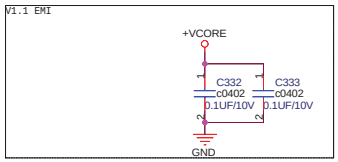












Default Group-optional

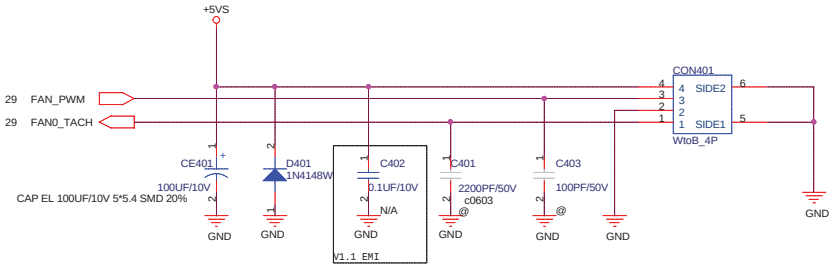
ASUSTeK COMPUTER INC	Title : Yonah CPU (2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 3 of 63	

+5VS +5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS +3VS 5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

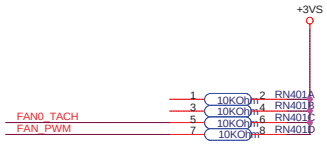
Fan Speed Control

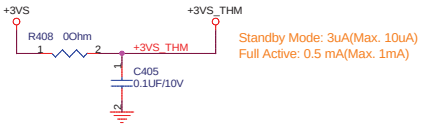
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



COULD BE CLOSED TO EC



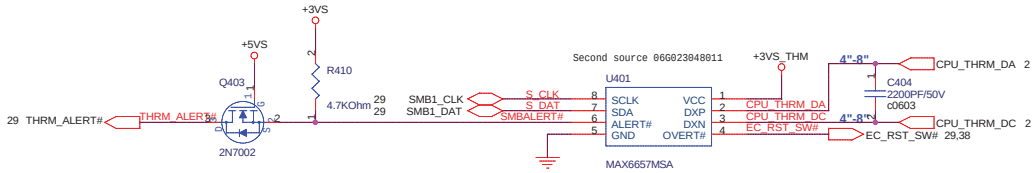


Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

Route H_THERMDA and H_THERMDC on the same layer

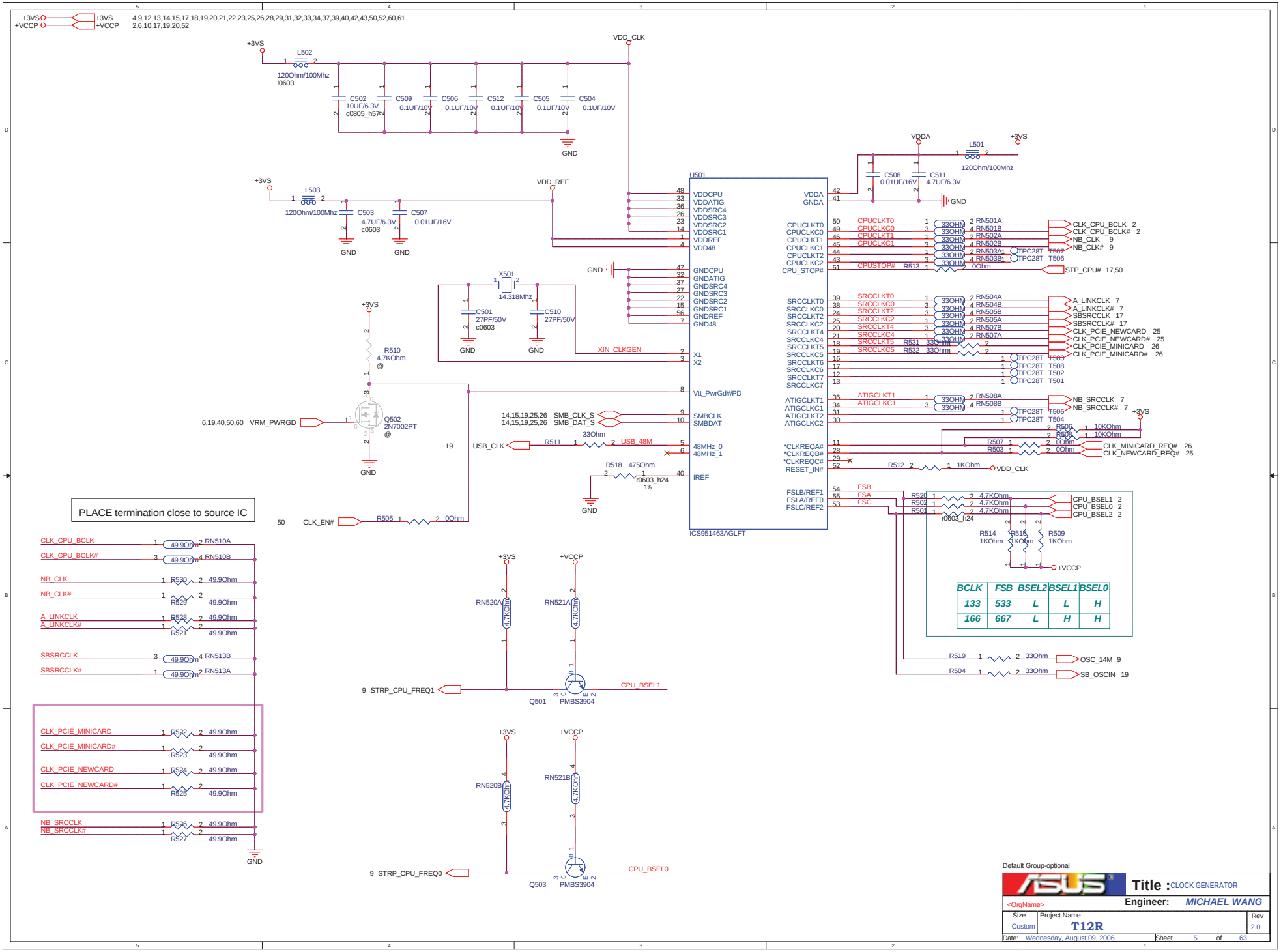
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

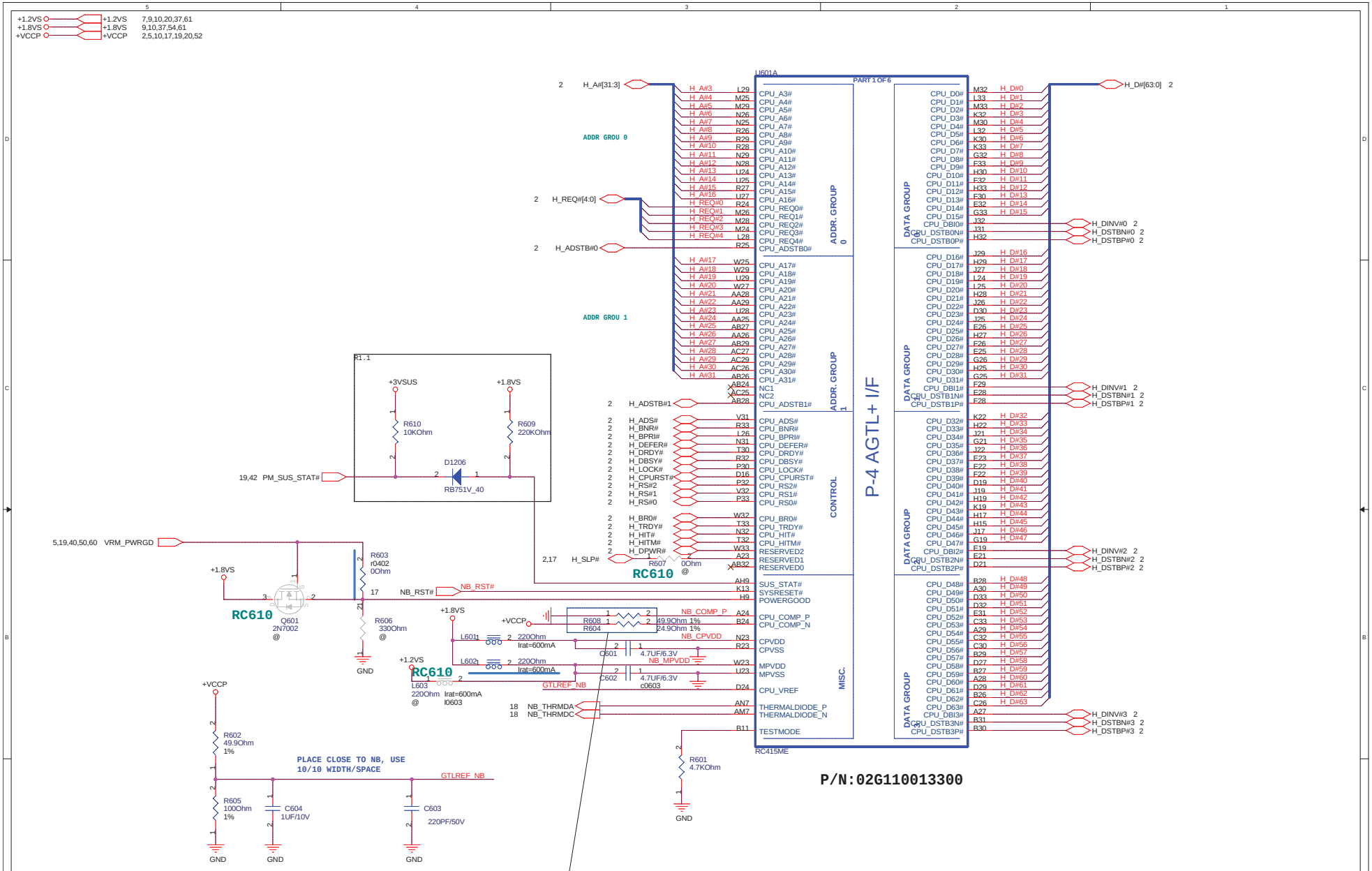
Avoid BPSB,Power



Default Group-optional

Title : THER-SENSOR,FAN
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: T12R | Rev: 2.0
Date: Wednesday, August 09, 2006 | Sheet 4 of 63





RC610/RC515	RC610	RC415
R0608	53.6(10G21*********)	49.9(10G21249R914030)
R0604	21 (10G21*********)	24.9(10G21224R914040)

Default Group-optional

ASUSTeK COMPUTER INC. NB1

Title : NBRC415M(HOST)

Engineer:

Size	Project Name	Rev
Custom	T12R	2.0

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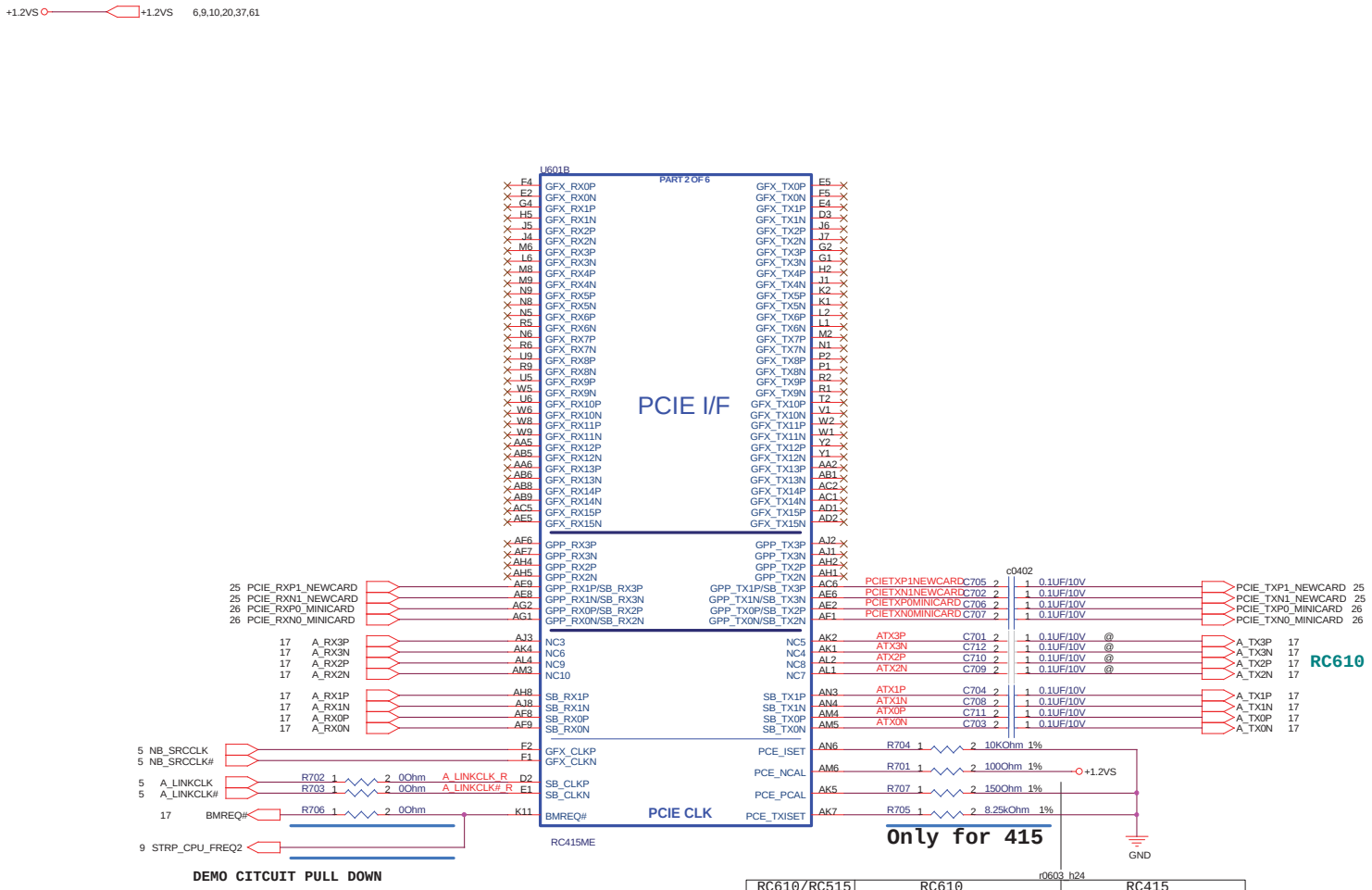


RC610/RC515	RC610	RC415
R0704	1.47K(10G21**********)	10K(10G213100213030)
R0701	2K (10G21**********)	100(10G213100013010)
R0707	562 (10G21**********)	150(10G213150013030)

Default Group-optional

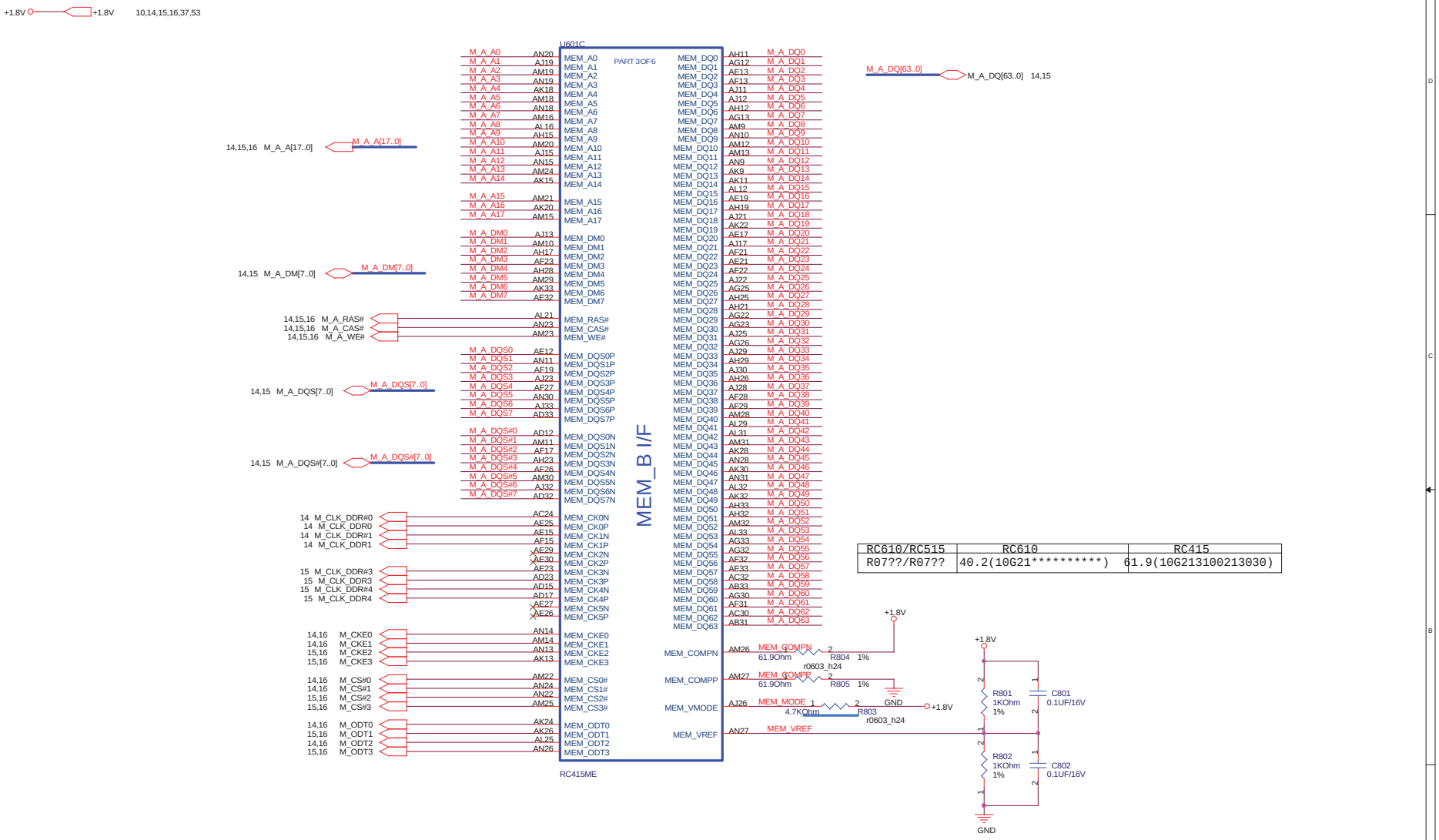
ASUSTeK COMPUTER INC. NB1

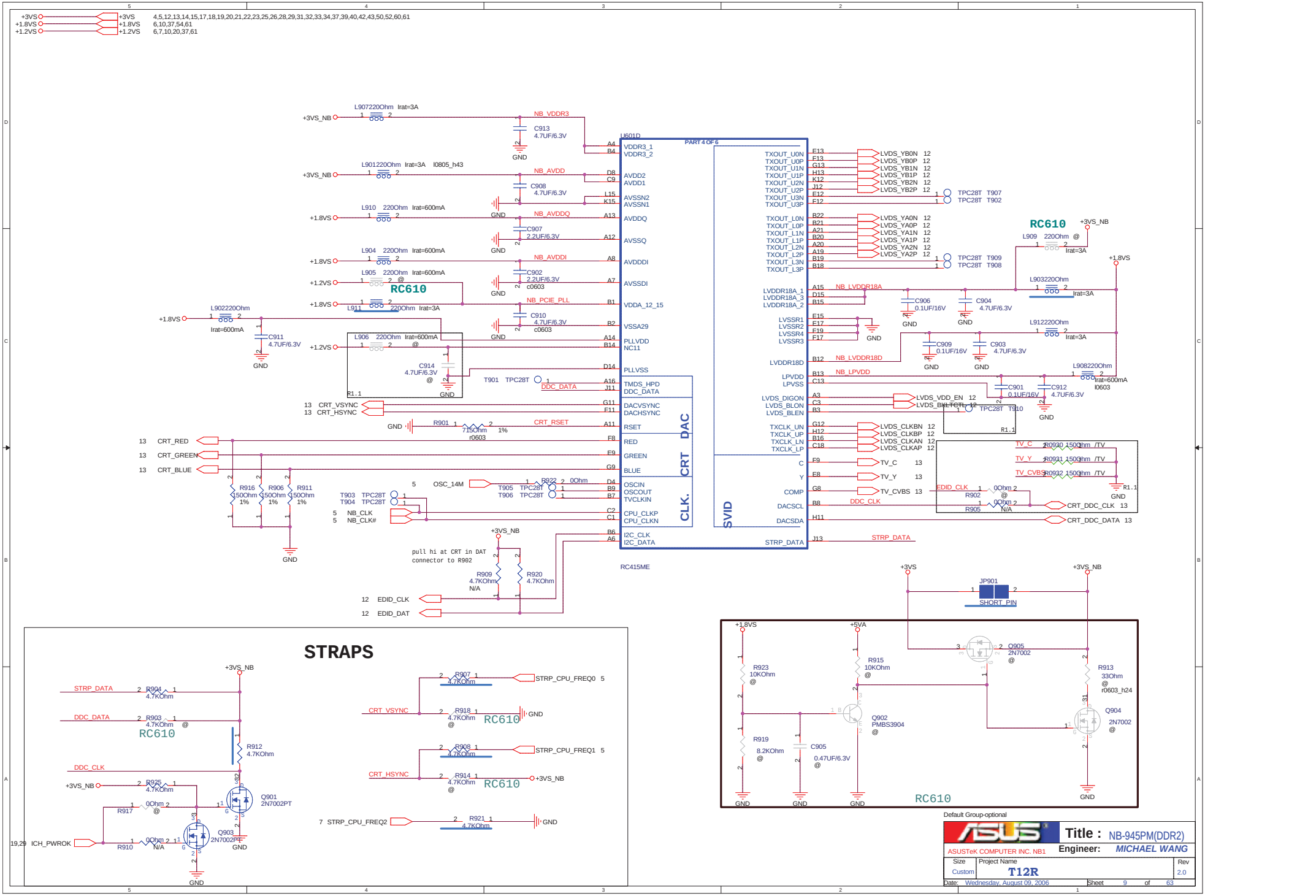
Title : NB-945PM(DMI & CFG)

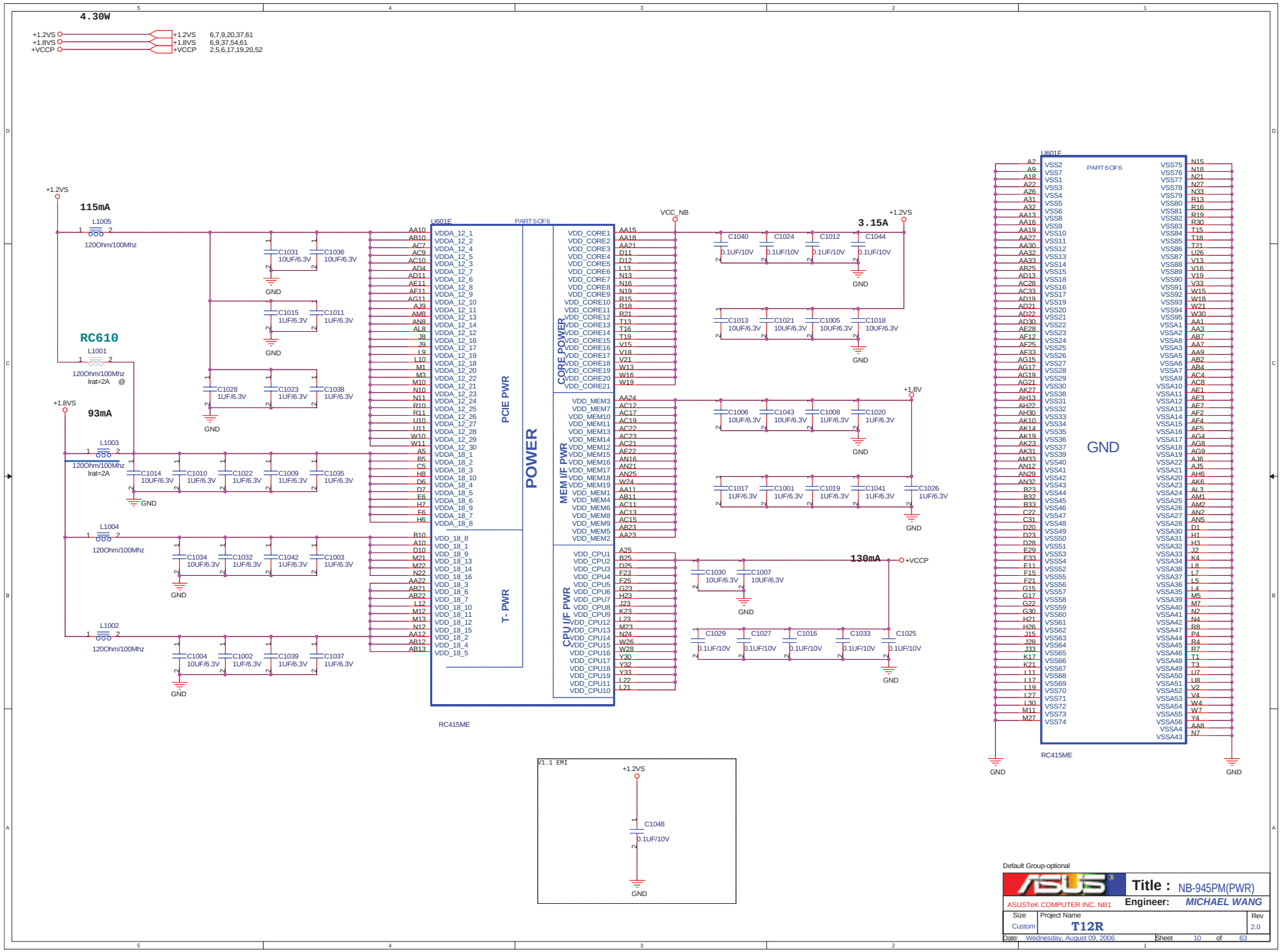
Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 7 of 63







Default Group-optional

Title : HISTORY

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

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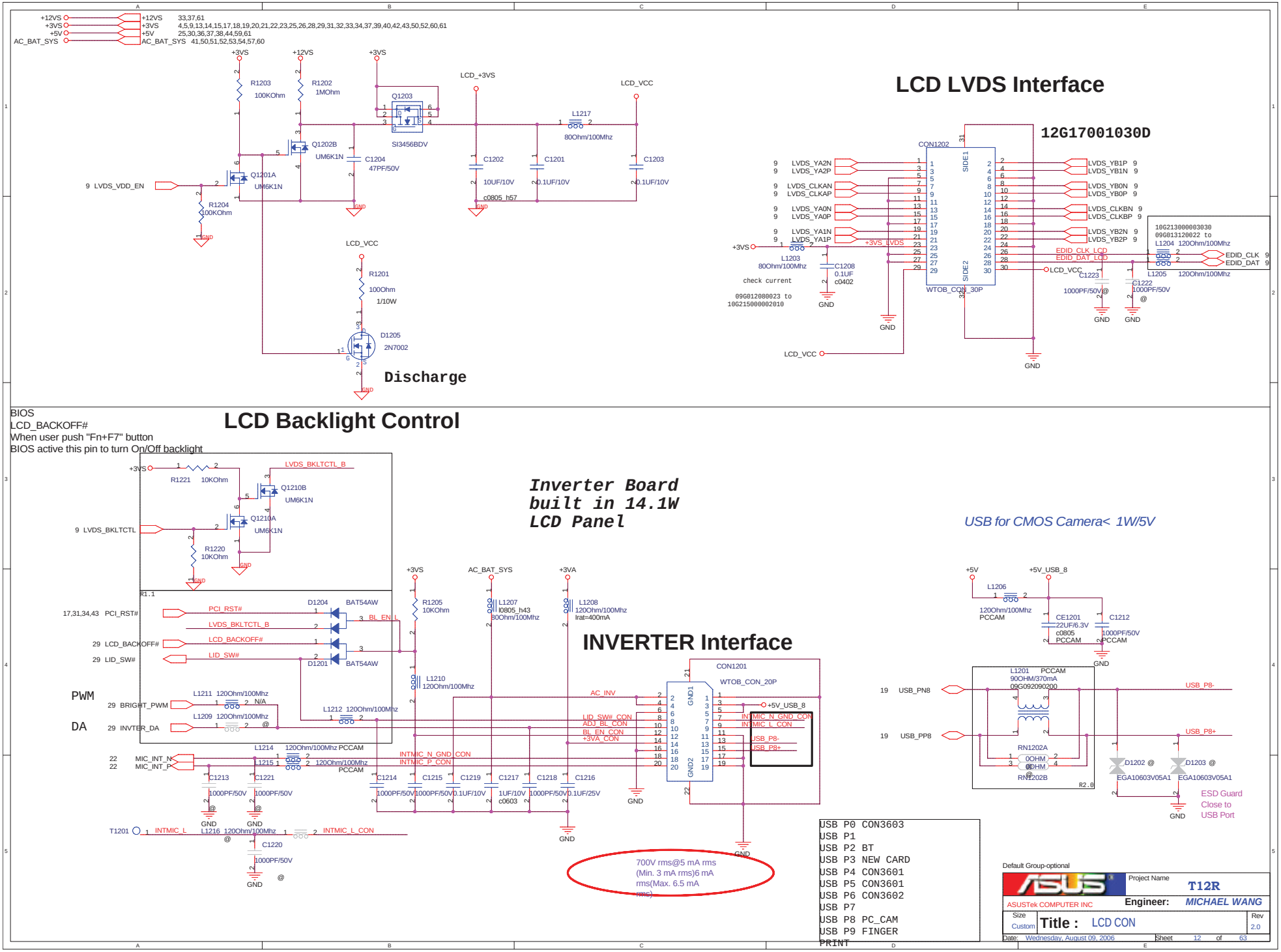
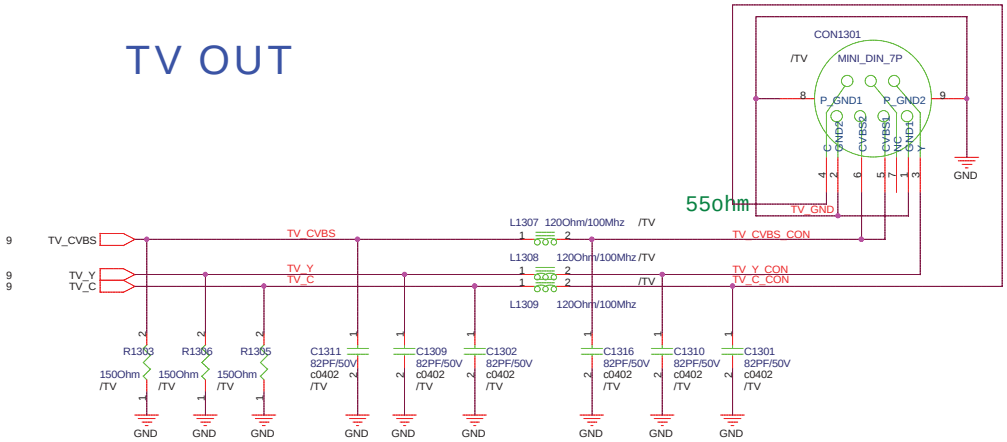
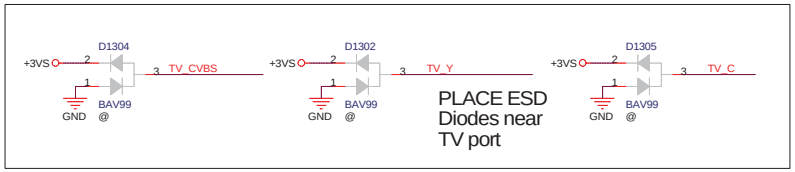


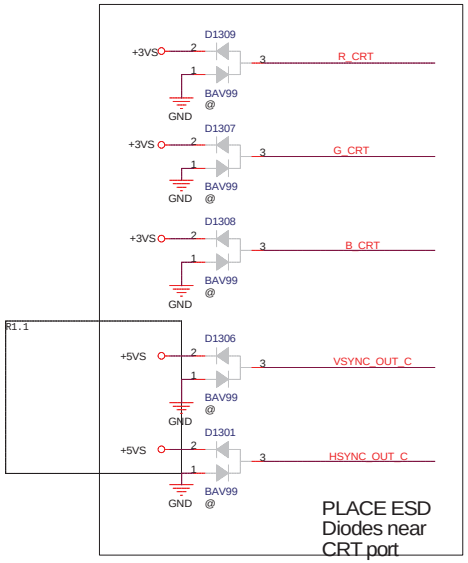
+5VS
+3VS
+5VS 4,20,22,23,28,29,30,37,38,50,61
+3VS 4,5,9,12,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

12G141011076

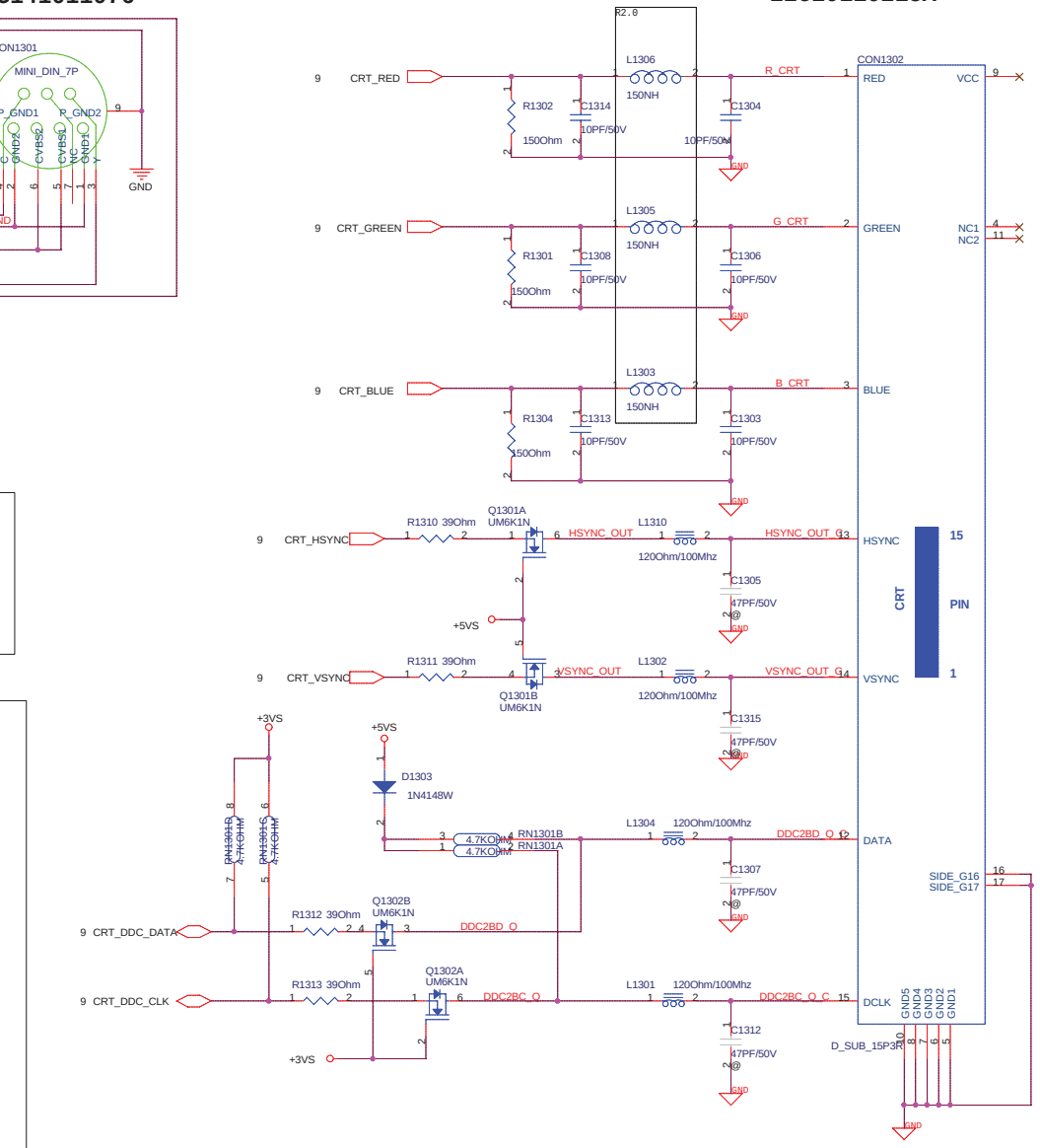
TV OUT





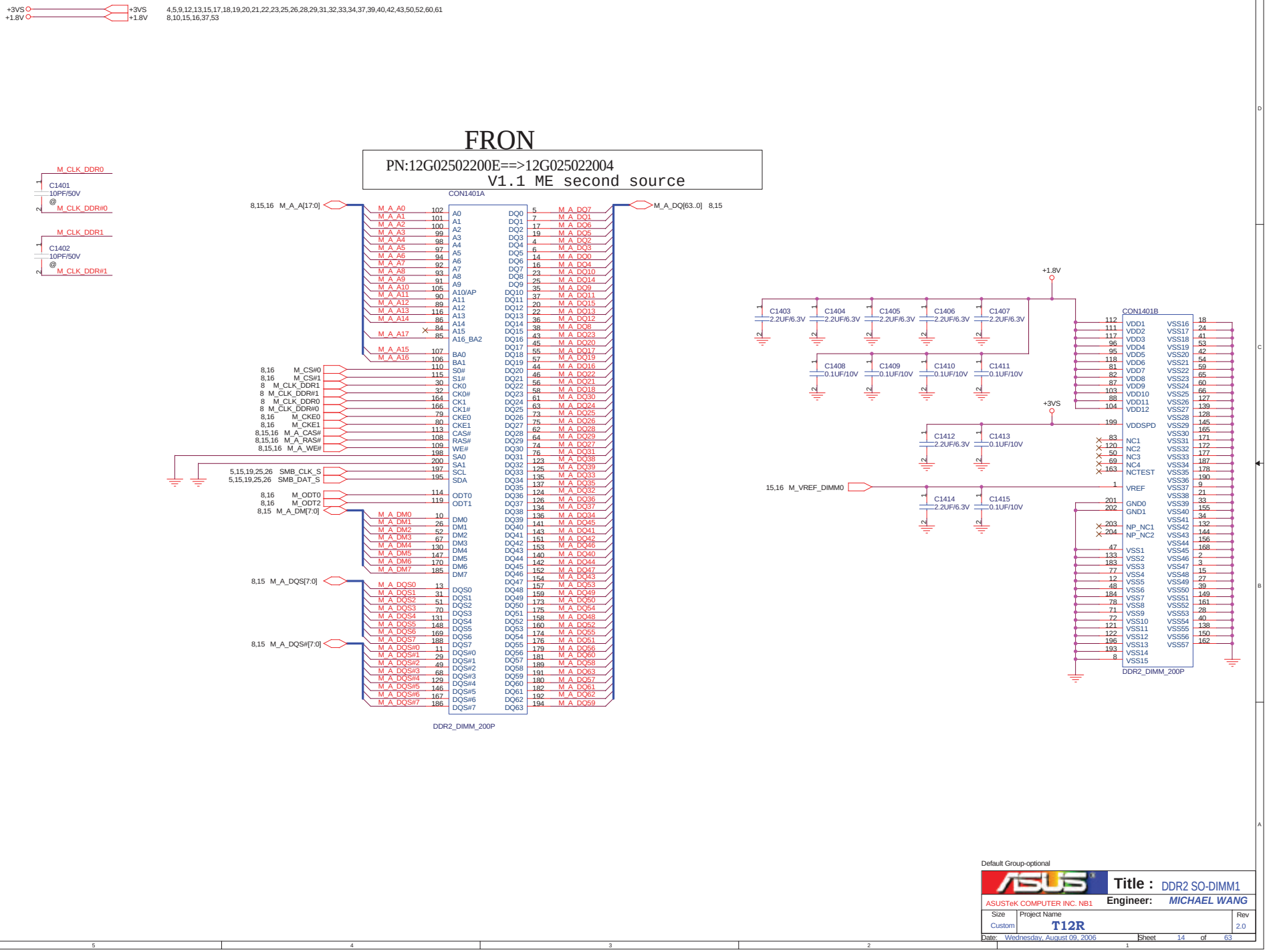


12G101102152
=>12G10110215A



Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 13 of 63	



+3VS
+1.8V
+3VS
+1.8V
4,5,9,12,13,14,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,14,16,37,53

M_CLK_DDR4
C1501
10PF/50V
@
M_CLK_DDR#4

M_CLK_DDR3
C1502
10PF/50V
@
M_CLK_DDR#3

PN:12G025C22000=>12G025C22004
V2.0 ME

CON1501A

8,14,16 M_A_A[17:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A17 M_A_A15 M_A_A16

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2 BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE# SA0 SA1 SCL SDA ODT0 ODT1 DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7 DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7 DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_A_DQ7 M_A_DQ3 M_A_DQ4 M_A_DQ0 M_A_DQ2 M_A_DQ1 M_A_DQ6 M_A_DQ5 M_A_DQ10 M_A_DQ14 M_A_DQ9 M_A_DQ11 M_A_DQ15 M_A_DQ13 M_A_DQ12 M_A_DQ8 M_A_DQ23 M_A_DQ20 M_A_DQ17 M_A_DQ19 M_A_DQ16 M_A_DQ22 M_A_DQ21 M_A_DQ18 M_A_DQ30 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ28 M_A_DQ29 M_A_DQ27 M_A_DQ31 M_A_DQ38 M_A_DQ39 M_A_DQ33 M_A_DQ35 M_A_DQ32 M_A_DQ36 M_A_DQ37 M_A_DQ34 M_A_DQ45 M_A_DQ41 M_A_DQ42 M_A_DQ46 M_A_DQ40 M_A_DQ44 M_A_DQ47 M_A_DQ43 M_A_DQ53 M_A_DQ49 M_A_DQ50 M_A_DQ54 M_A_DQ48 M_A_DQ52 M_A_DQ55 M_A_DQ51 M_A_DQ56 M_A_DQ60 M_A_DQ58 M_A_DQ63 M_A_DQ57 M_A_DQ61 M_A_DQ59 M_A_DQ62

M_A_DQ[63..0] 8,14

DDR_DIMM_200P

+3VS
R1501
10KOhm

8,16 M_CS#2
8,16 M_CS#3
8 M_CLK_DDR3
8 M_CLK_DDR#3
8 M_CLK_DDR4
8 M_CLK_DDR#4
8,16 M_CKE2
8,16 M_CKE3
8,14,16 M_A_CAS#
8,14,16 M_A_RAS#
8,14,16 M_A_WE#

5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S

8,16 M_ODT1
8,16 M_ODT3
8,14 M_A_DM[7:0]
M_A_DM0 M_A_DM1 M_A_DM2 M_A_DM3 M_A_DM4 M_A_DM5 M_A_DM6 M_A_DM7

8,14 M_A_DQS[7:0]
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

8,14 M_A_DQS#[7:0]
M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7

+1.8V

C1503 2.2UF/6.3V
C1504 2.2UF/6.3V
C1505 2.2UF/6.3V
C1506 2.2UF/6.3V
C1507 2.2UF/6.3V
C1508 0.1UF/10V
C1509 0.1UF/10V
C1510 0.1UF/10V
C1511 0.1UF/10V
C1512 2.2UF/6.3V
C1513 0.1UF/10V
C1514 2.2UF/6.3V
C1515 0.1UF/10V

+3VS

14,16 M_VREF_DIMM1

CON1501B

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDDSPD NC1 NC2 NC3 NC4 NCTEST VREF GND0 GND1 NP_NC1 NP_NC2 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

DDR_DIMM_200P

Default Group-optional

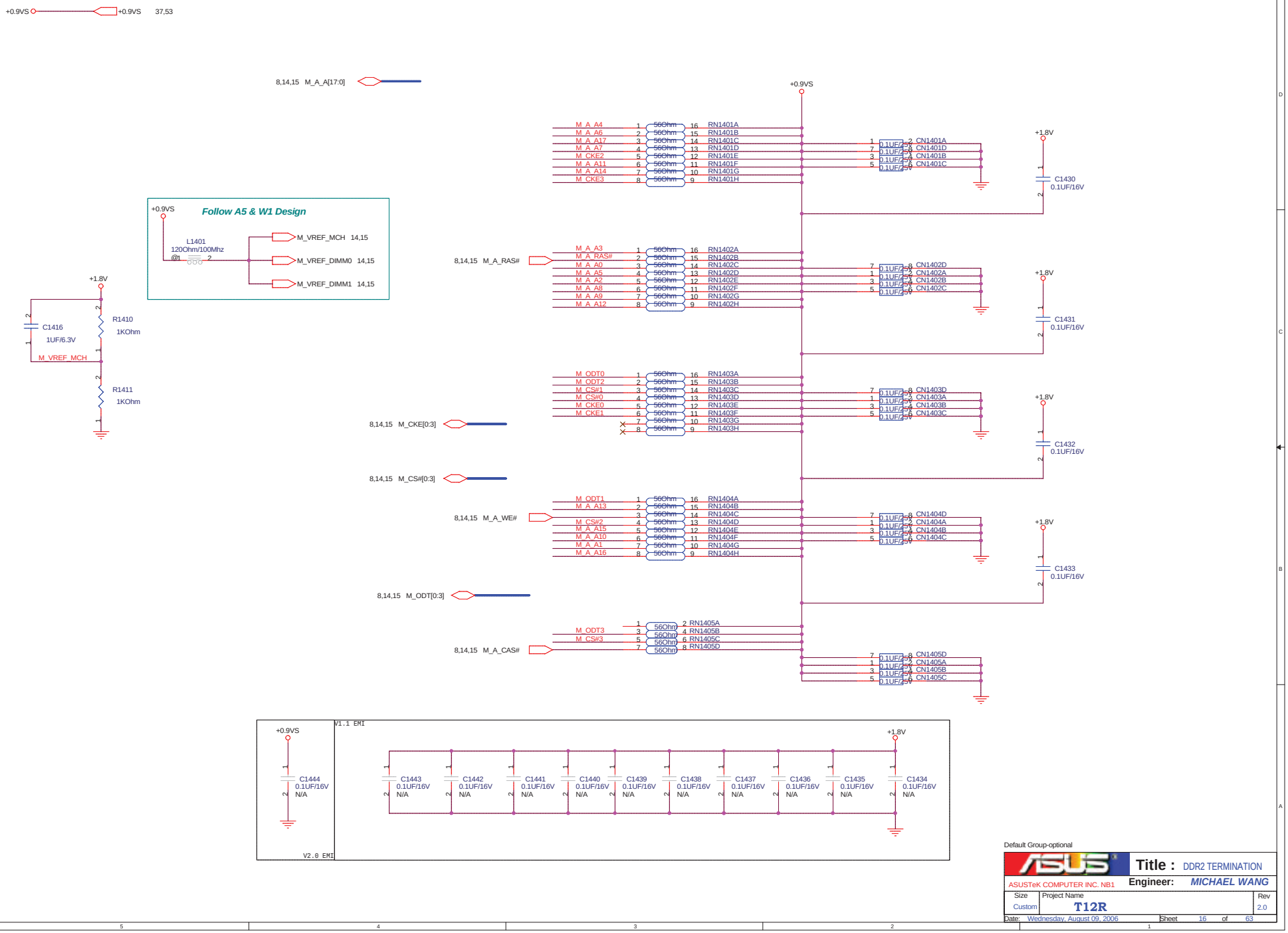
ASUSTeK COMPUTER INC. NB1

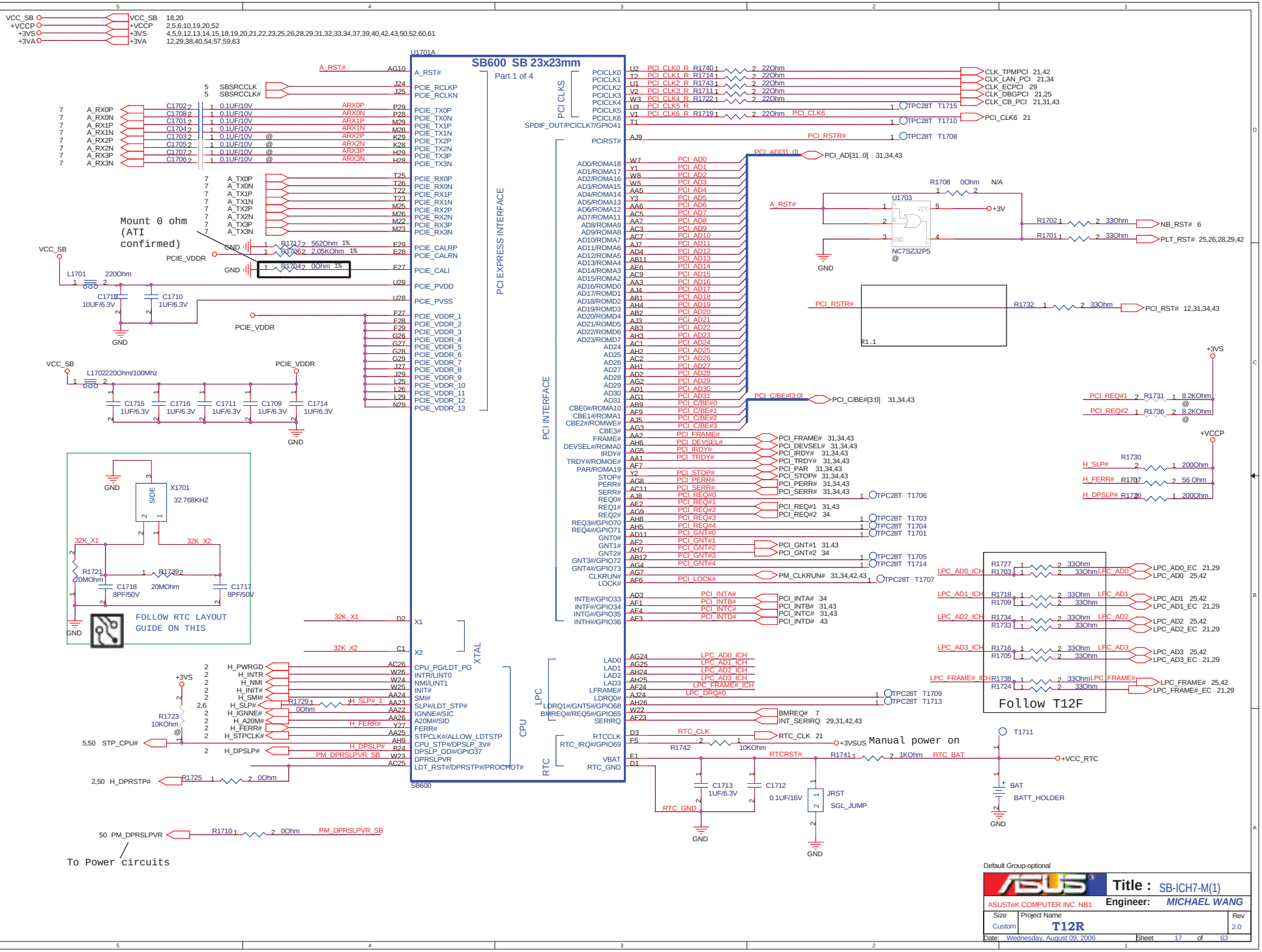
Title : DDR2 SO-DIMM1

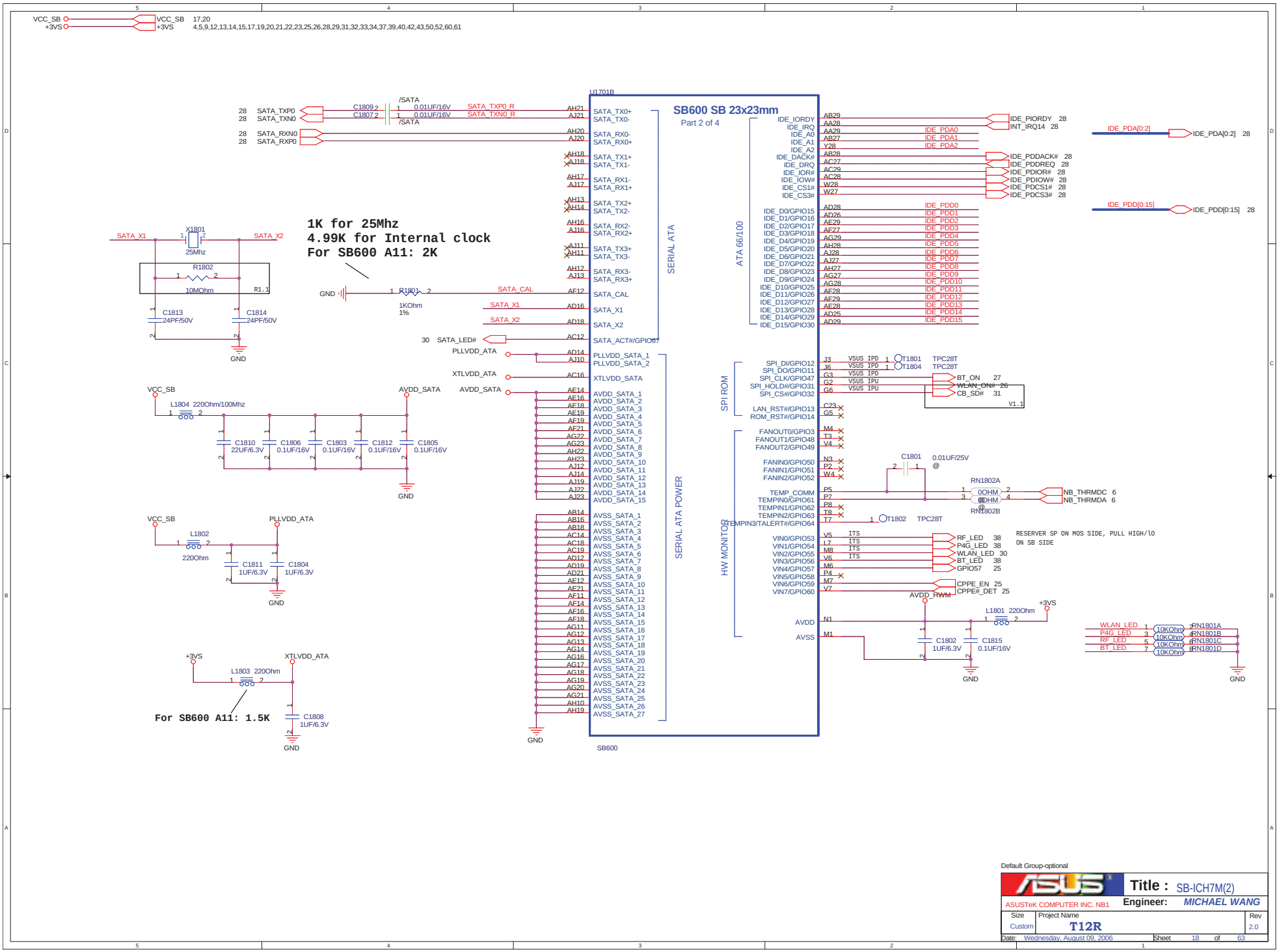
Engineer: MICHAEL WANG

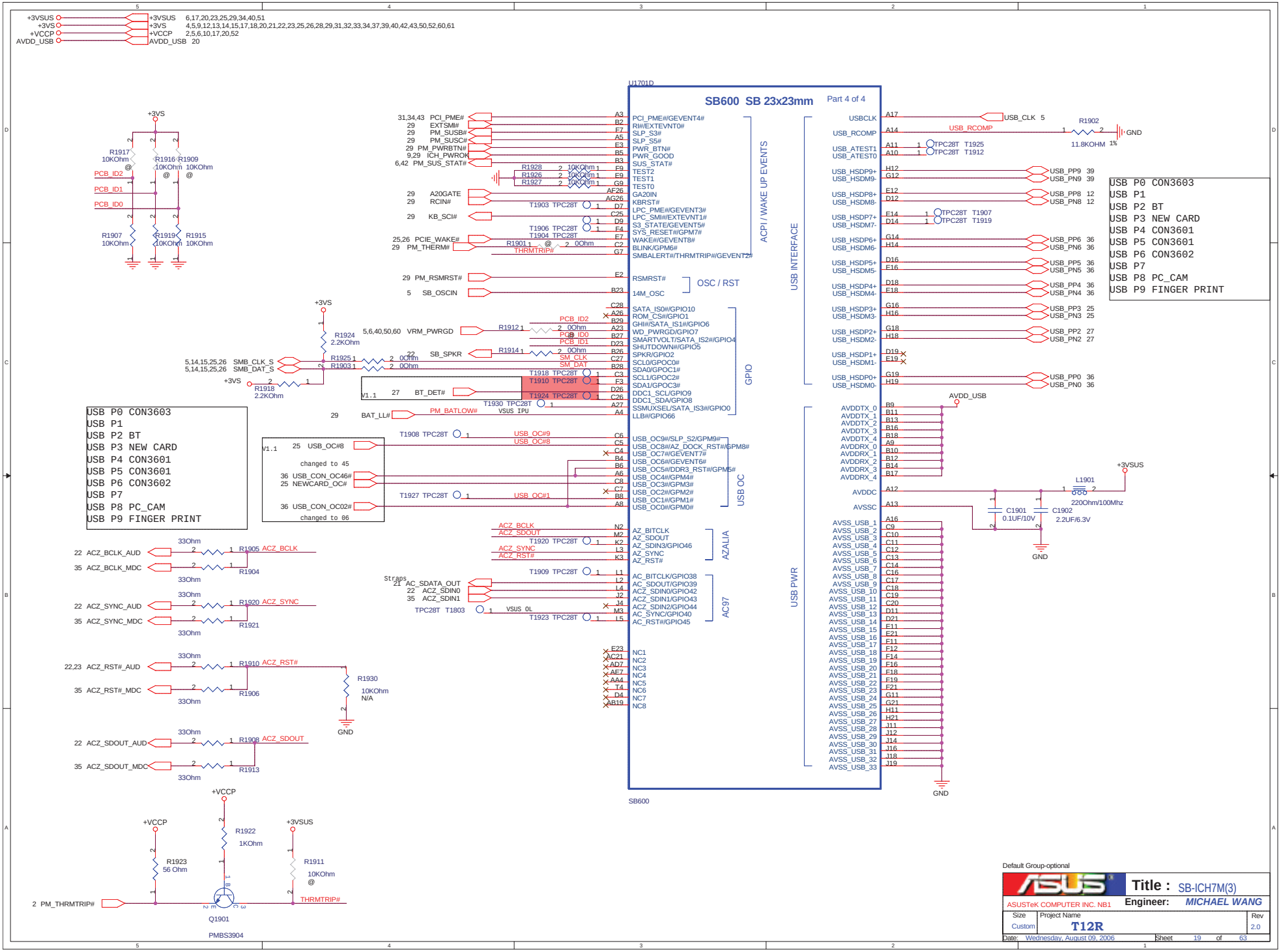
Size	Project Name	Rev
Custom	T12R	2.0

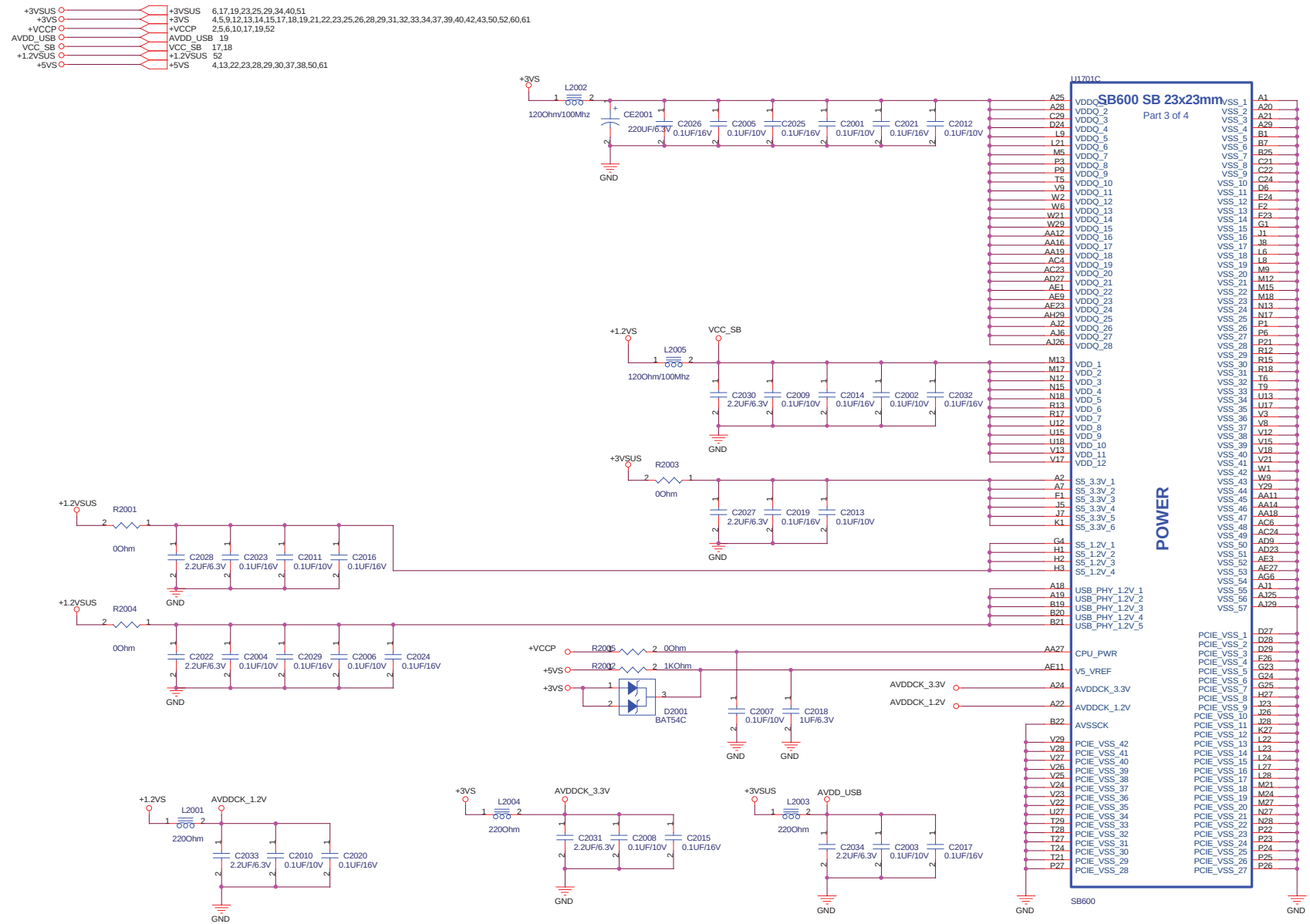
Date: Wednesday, August 09, 2006 Sheet 15 of 63





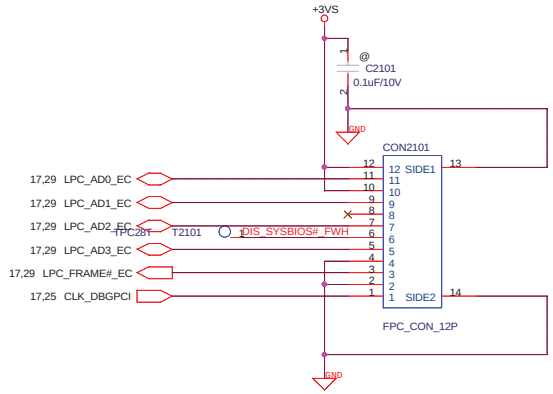






Default Group-optional

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(PWR)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 20 of 63	



19 AC_SDATA_OUT — R2101 2.2KOhm — +3VS

Ignore Debug Straps (Default)

17 RTC_CLK — TPC28T T2102

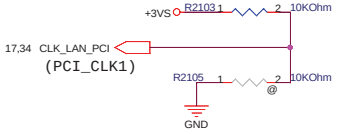
RTC_CLK has 15K internal pull up (Default): Uses Internal RTC

17,31,43 CLK_CB_PCI — R2106 10KOhm — GND

PCI_CLK4(CLK_CB_PCI) Pull-Low uses external 48Mhz(Default)

17 PCI_CLK6 — R2102 10KOhm — GND

PCI_CLK6 Pull-Low uses Intel P4(Default)



PCI_CLK0	PCI_CLK1	(ROM Type)	
H	H	PCI ROM	
H	L	SPI ROM	
L	H	LPC ROM	(Default)
L	L	FWH ROM	

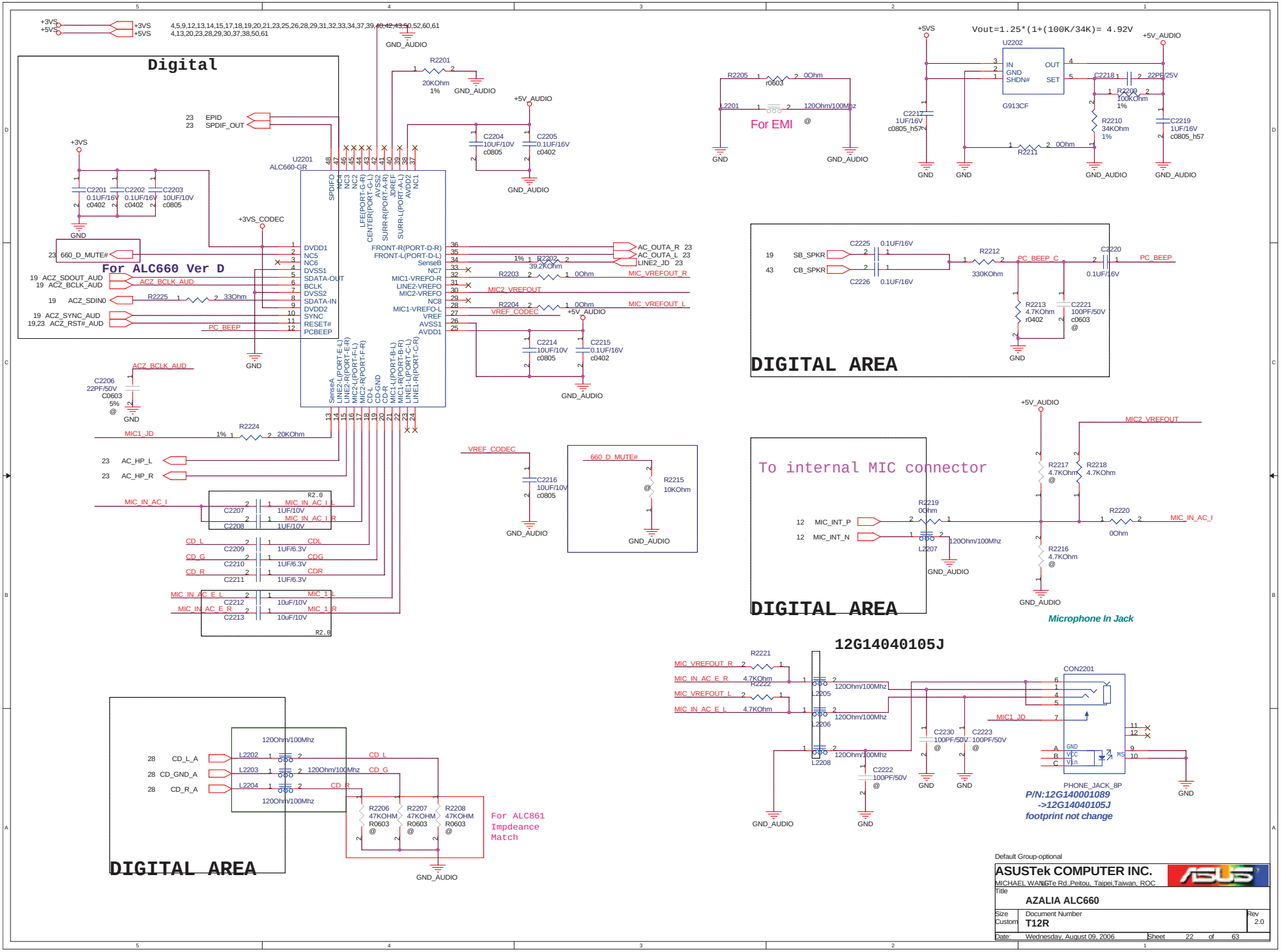
Default Group-optional

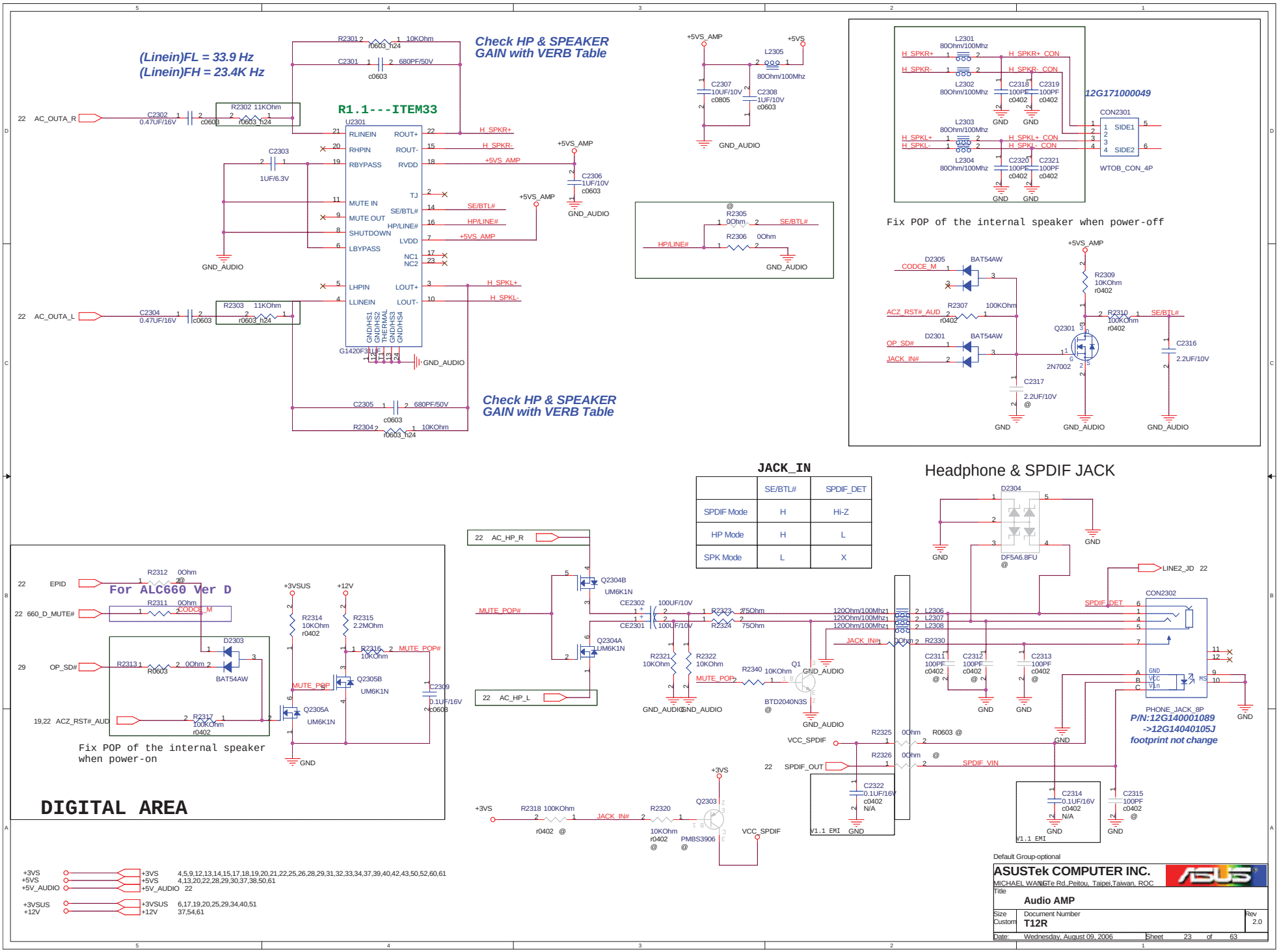
Title : BLOCK DIAGRAM

<OrgName> Engineer:

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 21 of 63



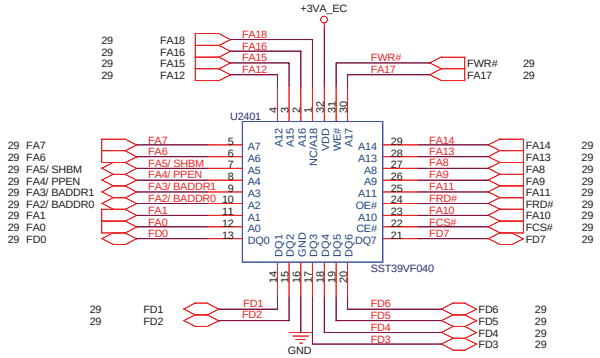


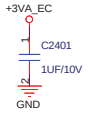
	SE/BTL#	SPDIF_DET
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X

+3VA_EC +3VA_EC 26,29

ISA ROM

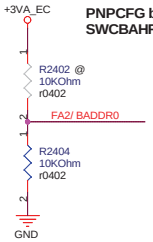
0.01A



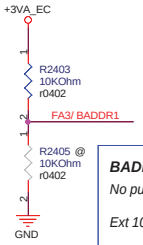


EC Hardware Strap

Strap value sampled after VSTBY power up reset

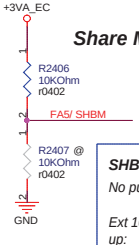


PNPCFG base address set by SWCBAHR/SWCBALR



BADDR[1:0]

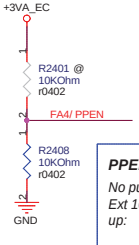
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*



Share Memory

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

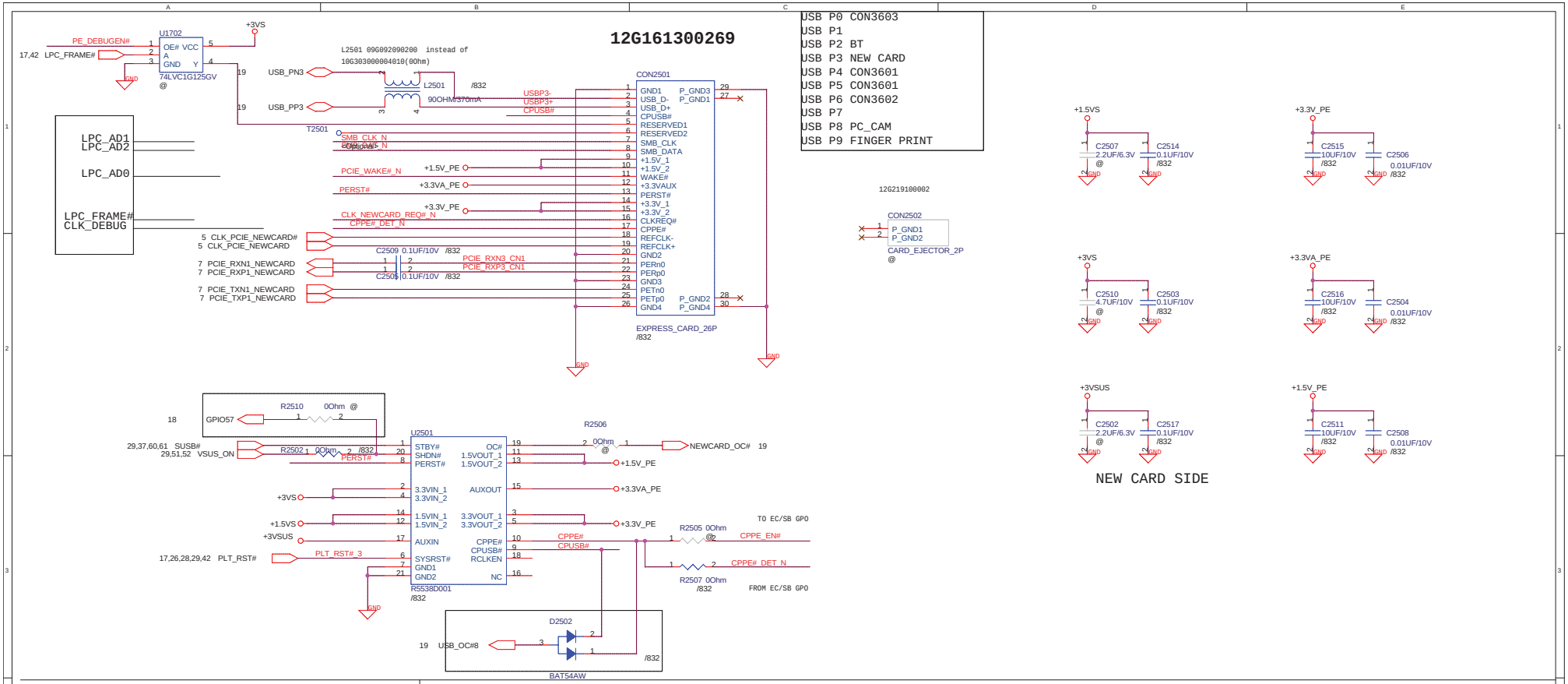


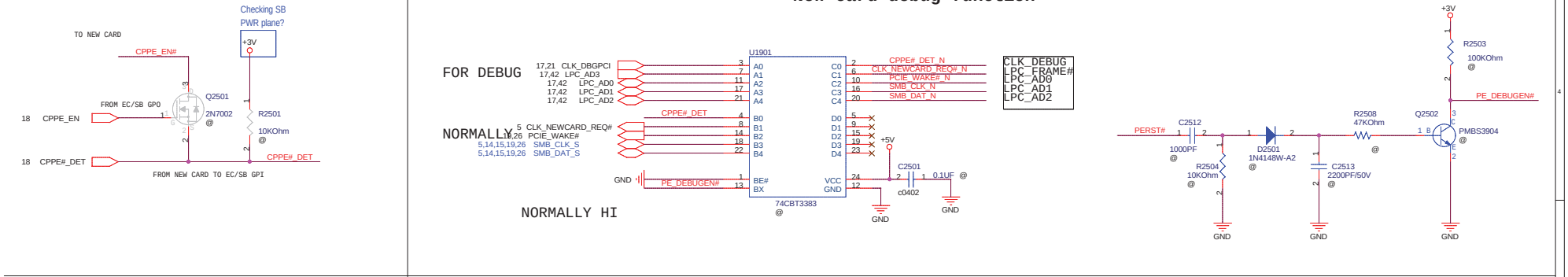
PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

Default Group-optional

ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 24 of 63	





Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	Engineer: MICHAEL WANG
Size: Custom	Title : New Card	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 25 of 63	

+3V 17,25,27,31,35,37,42,43,44,61
+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.5VS 25,37,54
+3VA_EC 24,29

12G030000526

CLKREQ#(output) CLOCK REQUEST could be pull low

CON2602

19,25 PCIE_WAKE#	1	WAKE#	3.3V_1	2	
27 CH_DATA	3	Reserved1	GND7	4	
27 CH_CLK	5	Reserved2	1.5V_1	6	
5 CLK_MINICARD_REQ#	7	CLKREQ#	UIM_PWR	8	
	9	GND1	UIM_DATA	10	
5 CLK_PCIE_MINICARD#	11	REFCLK-	UIM_CLK	12	
5 CLK_PCIE_MINICARD	13	REFCLK+	UIM_RESET	14	
	15	GND2	UIM_VPP	16	
	17	Reserved/UIM_C8	GND8	18	
	19	Reserved/UIM_C4W_DISABLE#		20	WIRELESS_LAN_ON/OFF#
	21	GND3	PERST#	22	PLT_RST# 17,25,28,29,42
7 PCIE_RXN0_MINICARD	23	PERn0	+3.3Vaux	24	
7 PCIE_RXP0_MINICARD	25	PERp0	GND9	26	
	27	GND4	1.5V_2	28	
	29	GND5	SMB_CLK	30	R2603 1 2 0Ohm @ SMB_CLK_S 5,14,15,19,25
7 PCIE_TXN0_MINICARD	31	PETn0	SMB_DATA	32	R2601 1 2 0Ohm @ SMB_DAT_S 5,14,15,19,25
7 PCIE_TXP0_MINICARD	33	PETp0	GND10	34	
	35	GND6	USB_D-	36	
	37	Reserved3	USB_D+	38	
	39	Reserved4	GND11	40	
	41	Reserved5	LED_WWAN#	42	
	43	Reserved6	LED_WLAN#	44	WL_LED# 1 T260 IPC28t
	45	Reserved7	LED_WPAN#	46	
	47	Reserved8	1.5V_3	48	
	49	Reserved9	GND12	50	
	51	Reserved10	3.3V_2	52	
	53	GND13	NP_NC2	56	
	54	GND14	NP_NC1	55	

MINI_CARD_LATCH_52P

GND GND

+3VS

C2602 0.1UF/10V GND — C2605 0.1UF/10V GND — C2606 10UF/6.3V GND

3.003V~3.597V
Max= 750 mA

+1.5VS

C2608 0.1UF/10V GND — C2601 0.1UF/10V GND — C2603 10UF/6.3V GND

1.425V~1.575V
Max= 375 mA

+3V

C2607 0.1UF/10V GND — C2604 1UF/6.3V GND

3.003V~3.597V
Max= 250 mA

CON2601

MINI_PCI_LATCH_5P

MINI PCI-E LATCH 5P

GND

12G162210052

+3VA_EC

PULL HIGH ON SB SIDE AND IT INTERNAL PULL HIGH

INTERNAL PU

R2602 47KOhm @

18 WLAN_ON#

Q2601 2N7002

WIRELESS_LAN_ON/OFF#

GND

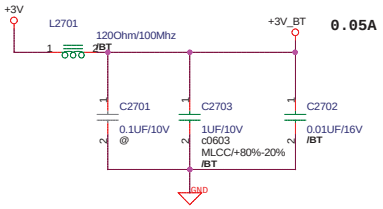
Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : MINI PCI	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 26 of 63	

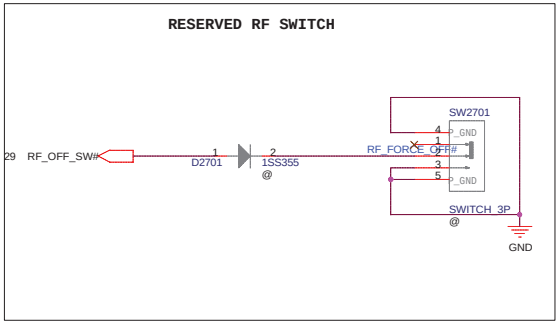
+3V +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

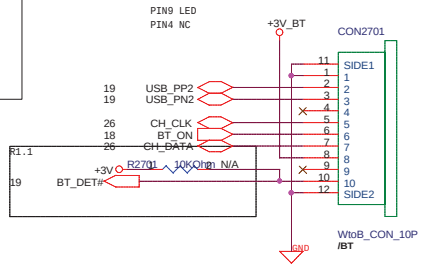
Bluetooth Module CN



RESERVED RF SWITCH



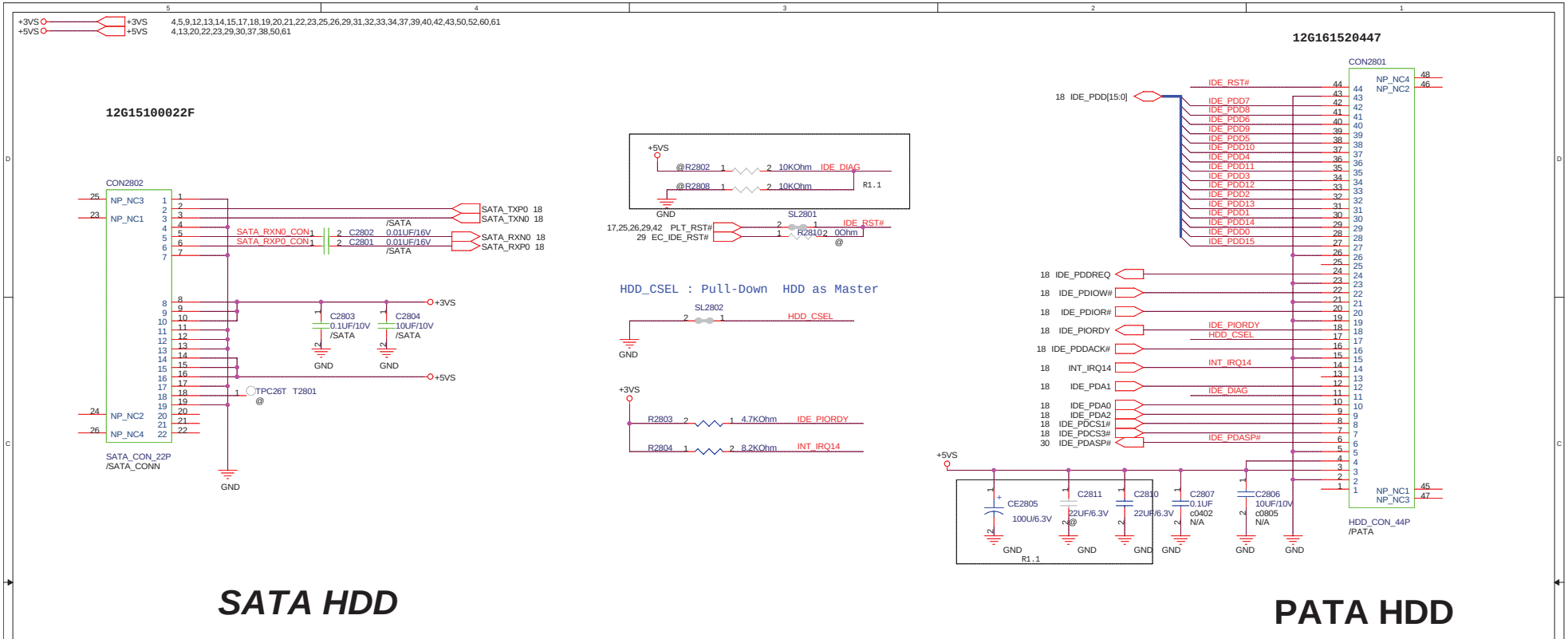
12G17101010L



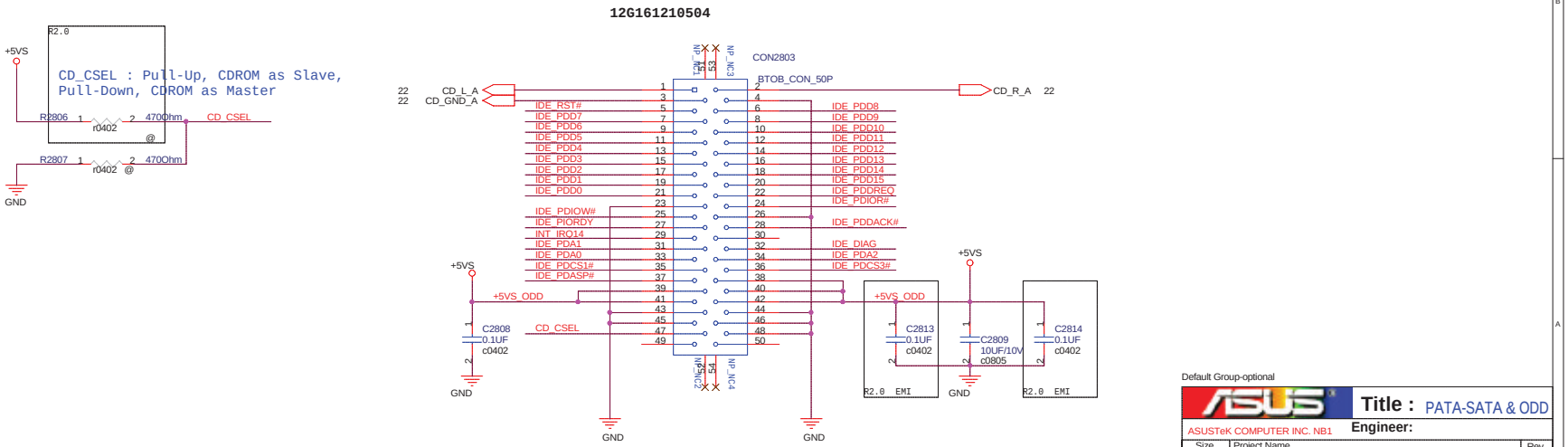

```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
```

Default Group-optional

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 27 of 63	



CD-ROM



Default Group-optional

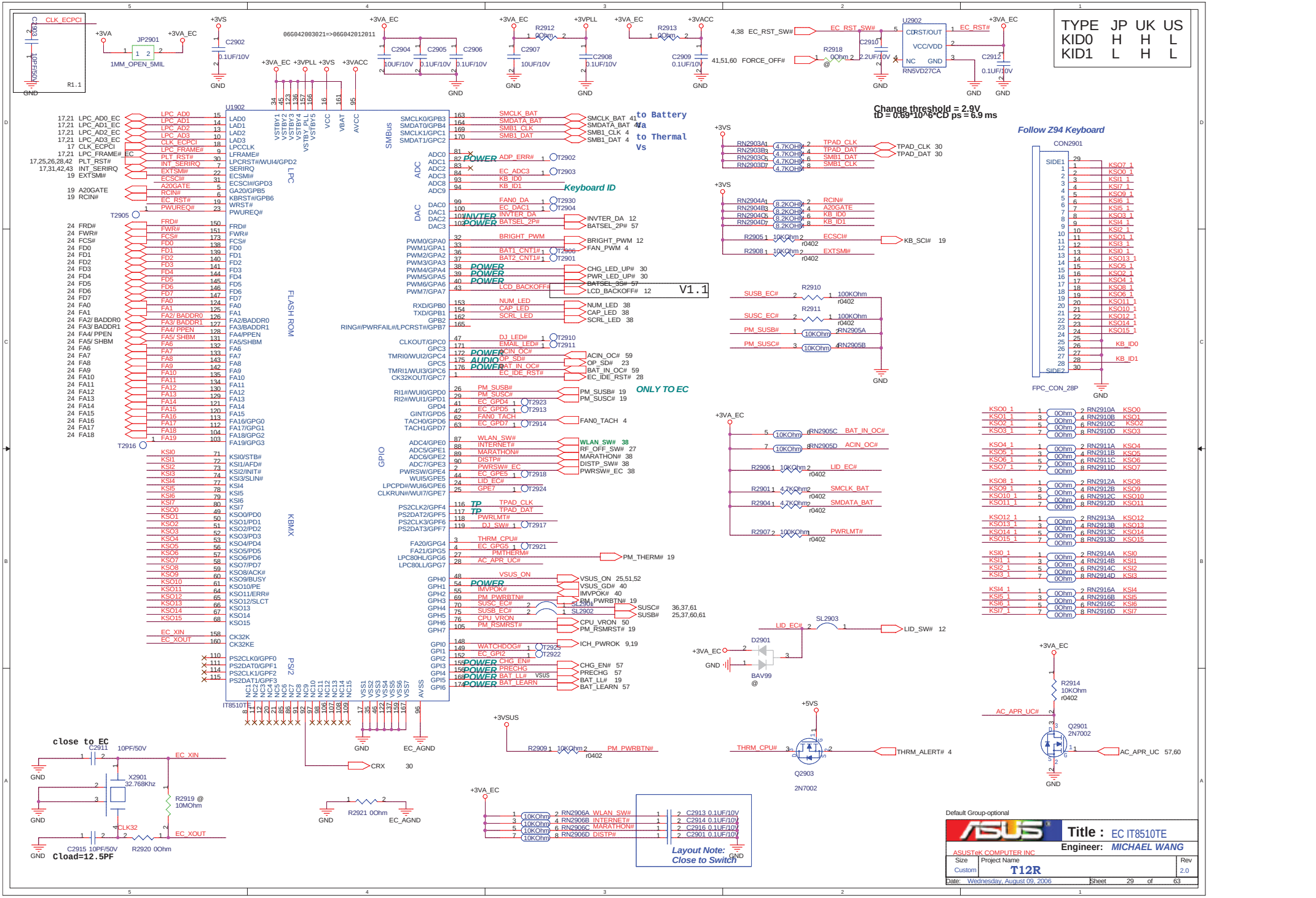
ASUSTeK COMPUTER INC. NB1

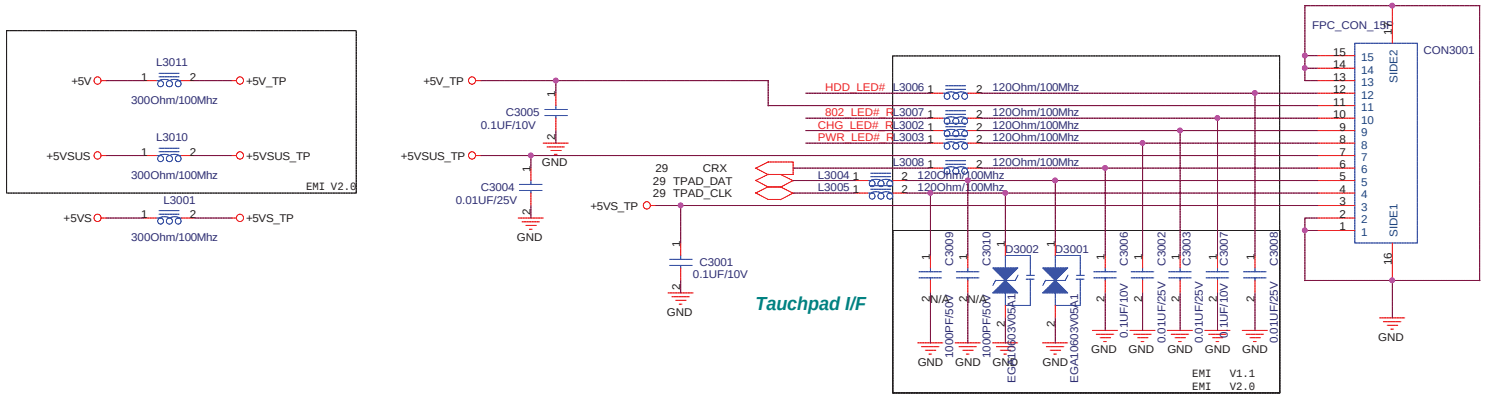
Title : PATA-SATA & ODD

Engineer:

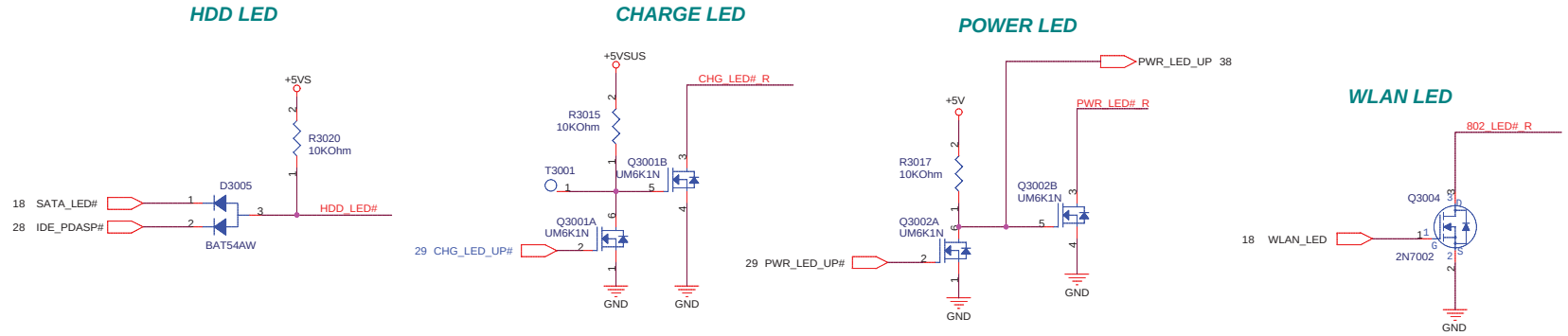
Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 28 of 63



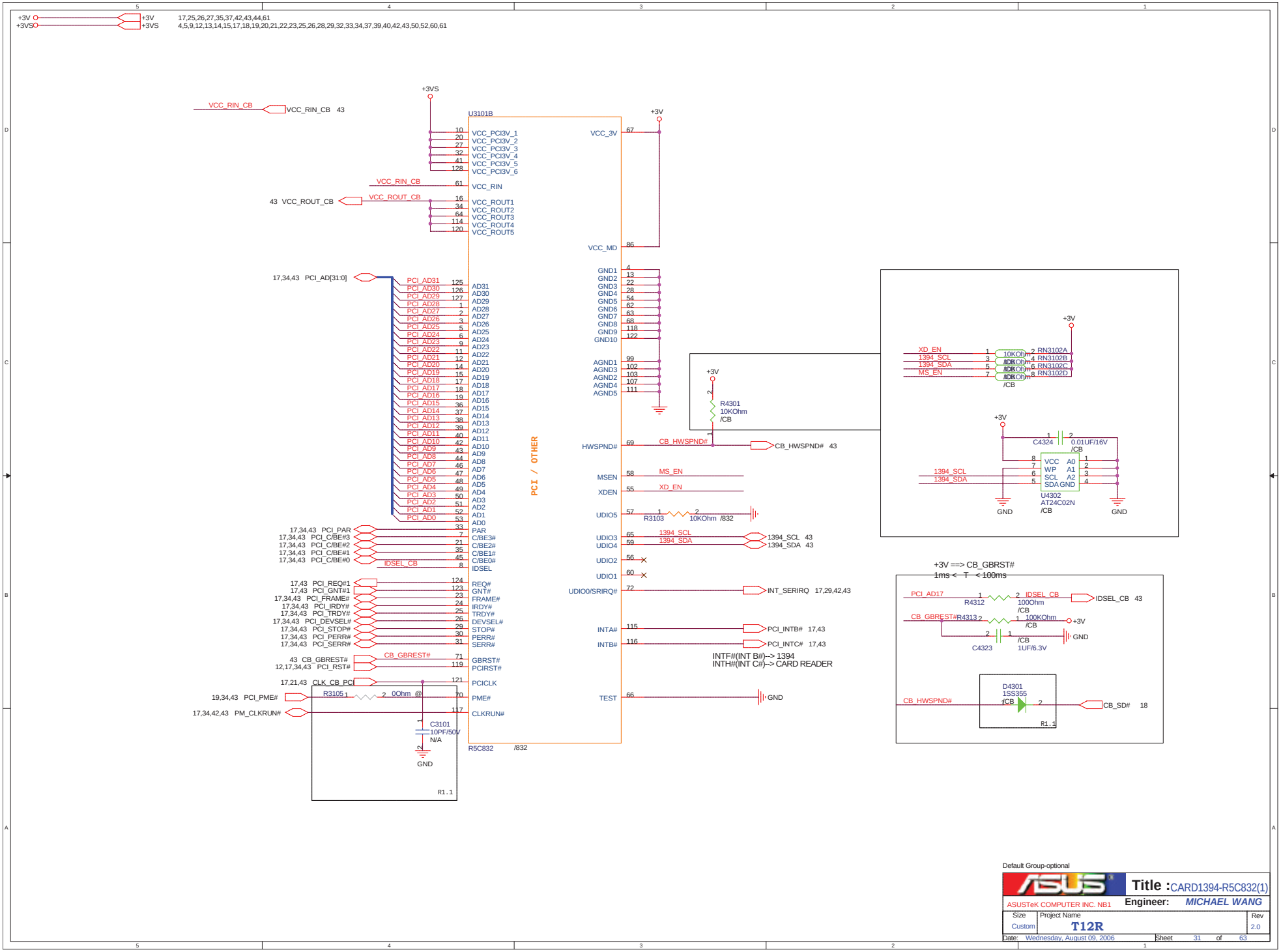


Touchpad



Default Group-optional

ASUSTeK COMPUTER INC	Title : EC IT8510TE(2/2)	
	Engineer: MICHAEL WANG	
Size: A3	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 30 of 63	



Default Group-optional

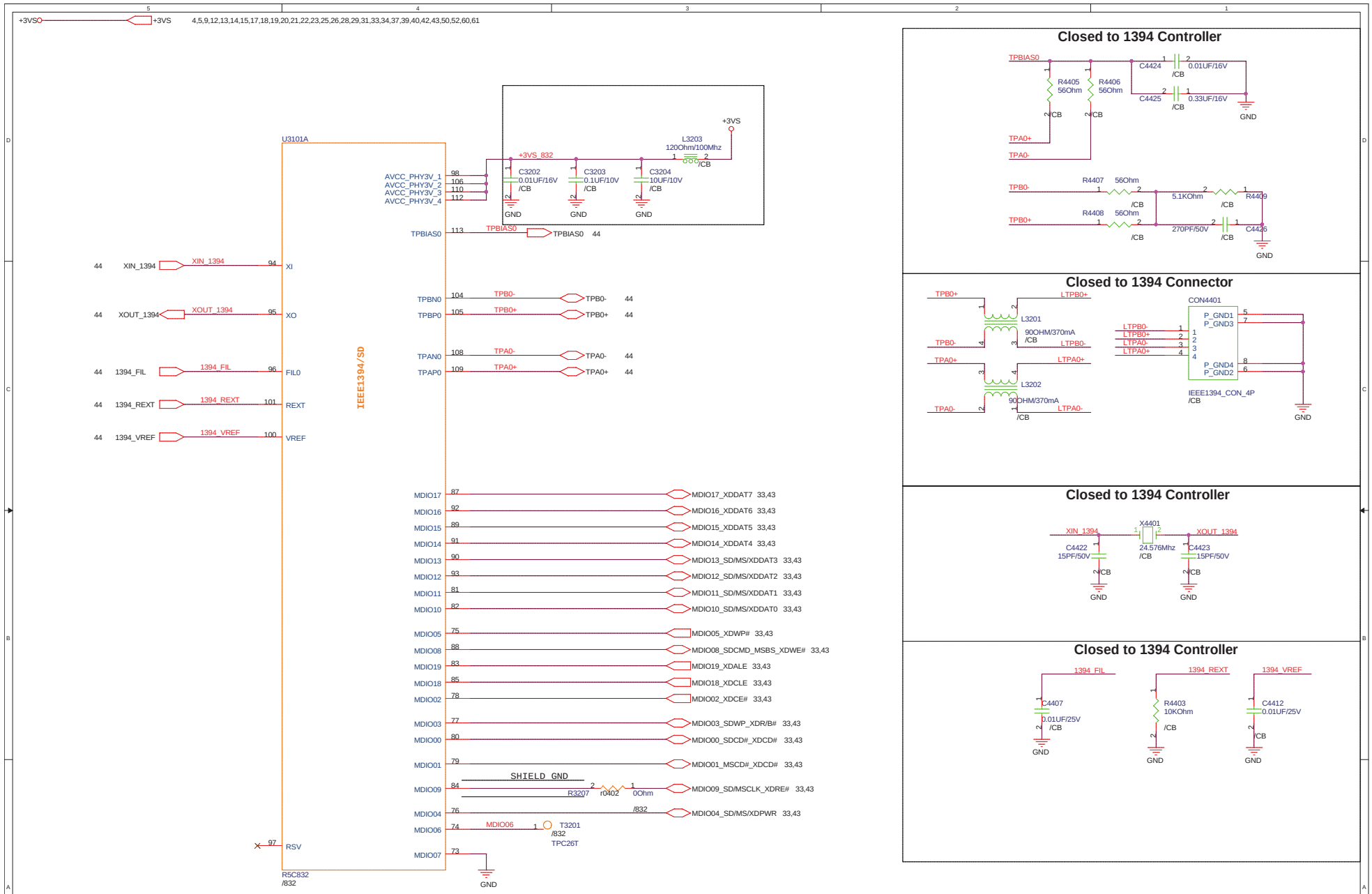
ASUSTeK COMPUTER INC. NB1

Title : CARD1394-R5C832(1)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 31 of 63



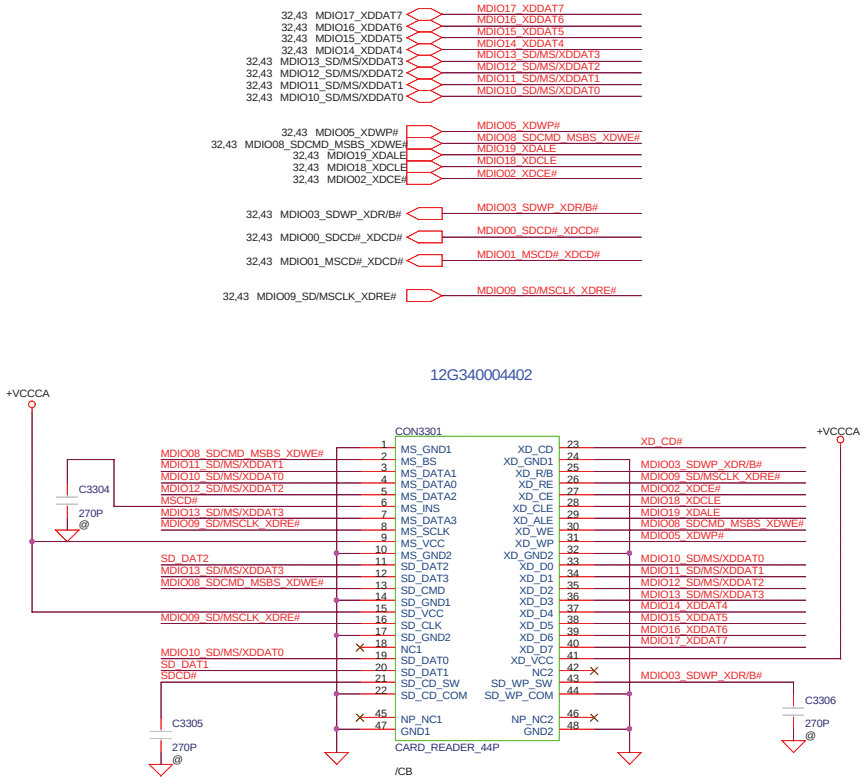
Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

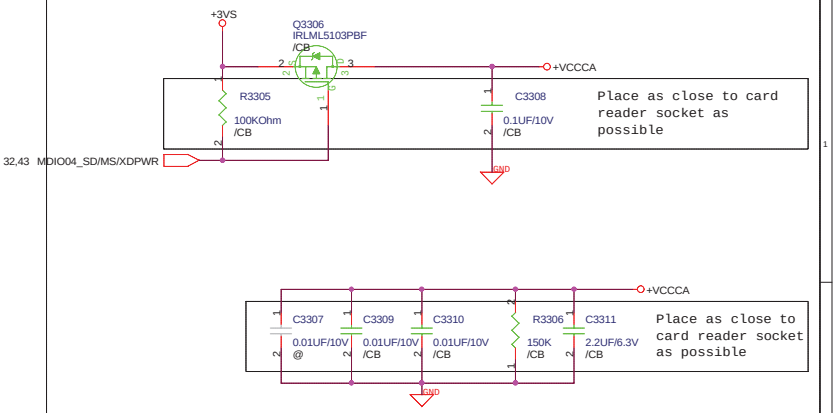
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

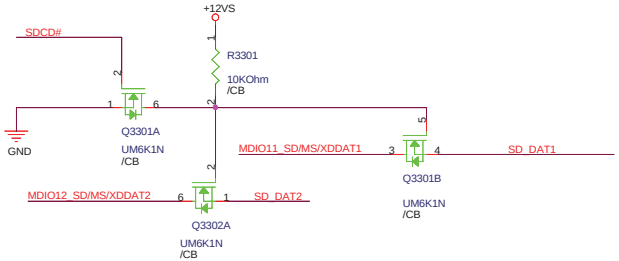
SD/MMC/MS/MS-PRO Card Reader Socket

12G340004402

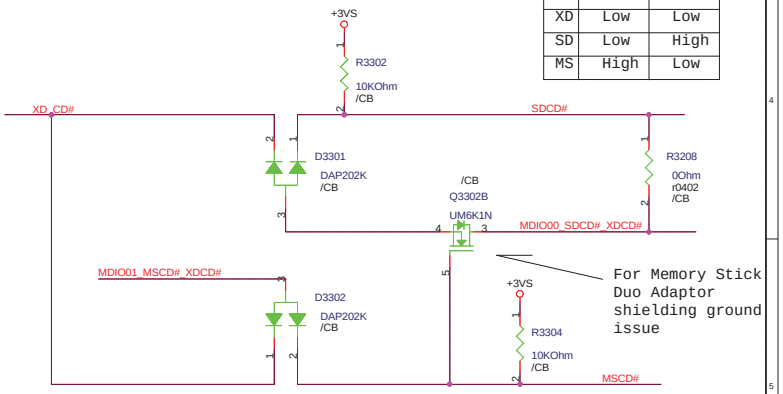




To coorect the problem when MS Duo adaptor is in use.



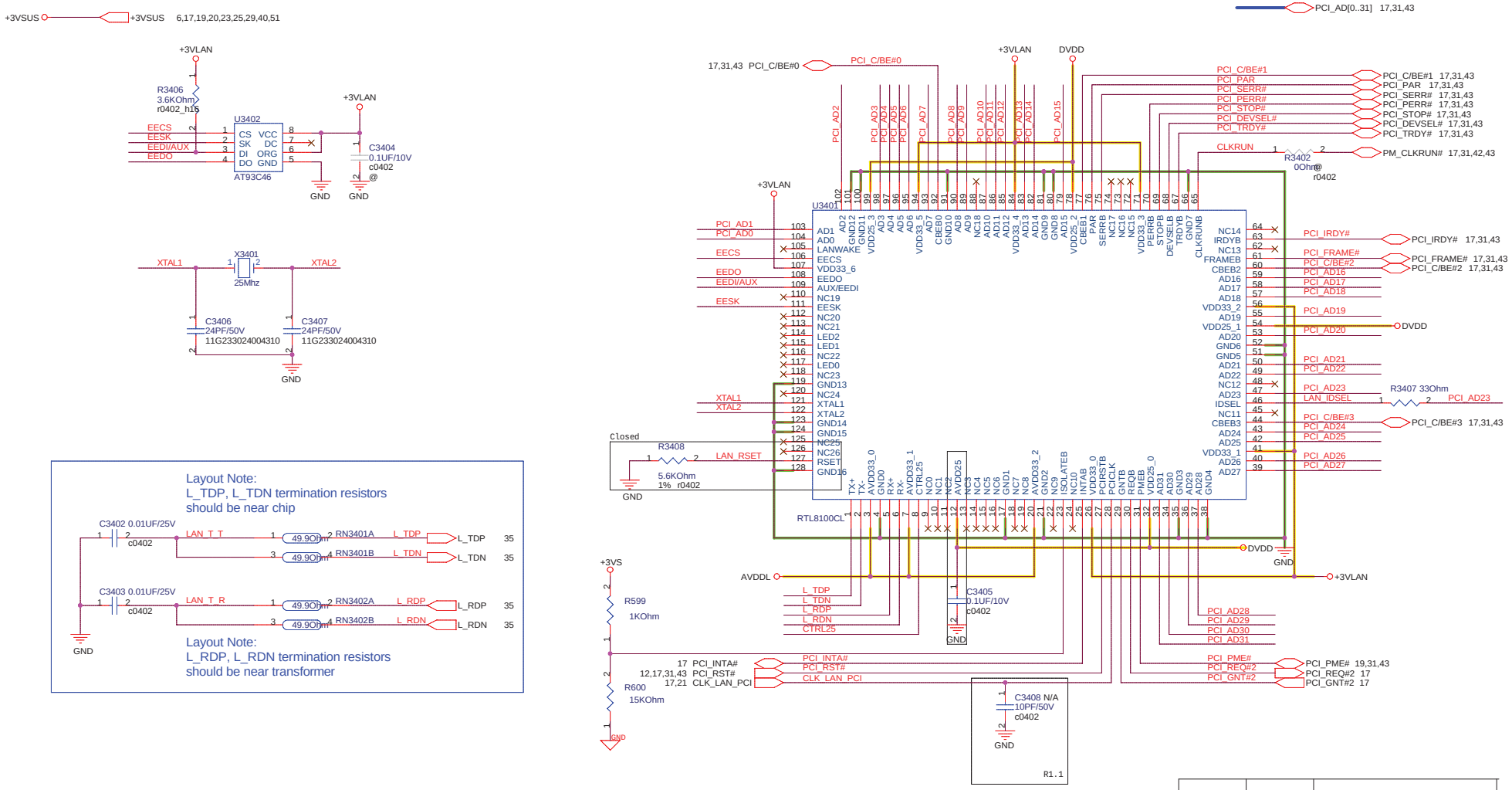
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



Default Group-optional

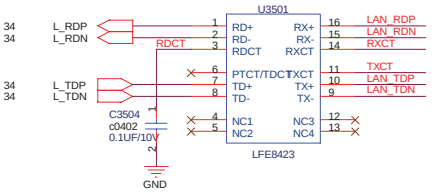
ASUSTek COMPUTER INC
Project Name: T12R
Engineer: MICHAEL WANG
Size: Custom
Title : CardReader
Rev: 2.0
Date: Wednesday, August 09, 2006
Sheet 33 of 63

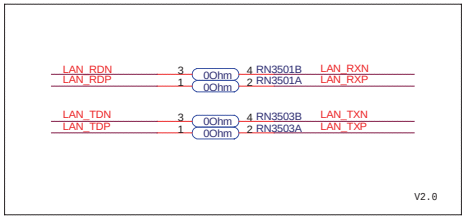
+12VS +3VS +12VS +3VS 12,37,61 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61



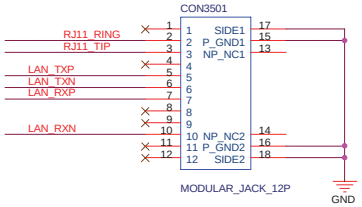
+3V +3V 17,25,26,27,31,37,42,43,44,61

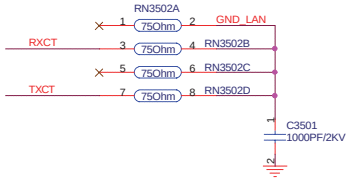
LAN PORT





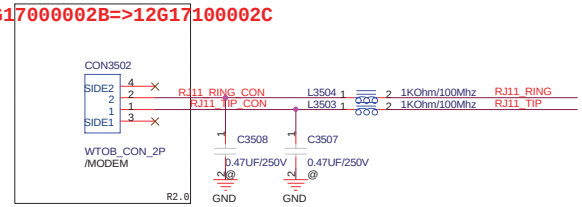
12G142111120





MDC CONNECTOR

12G17000002B=>12G17100002C



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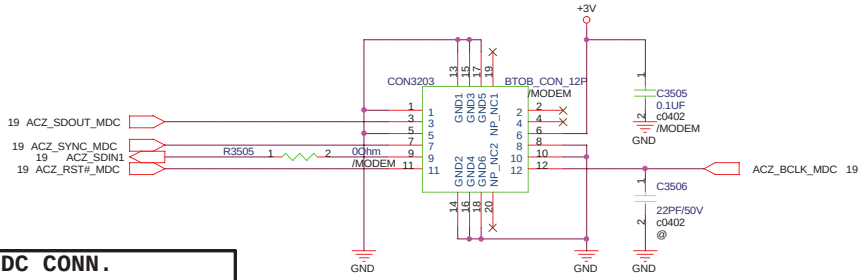
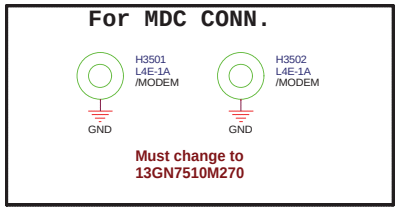
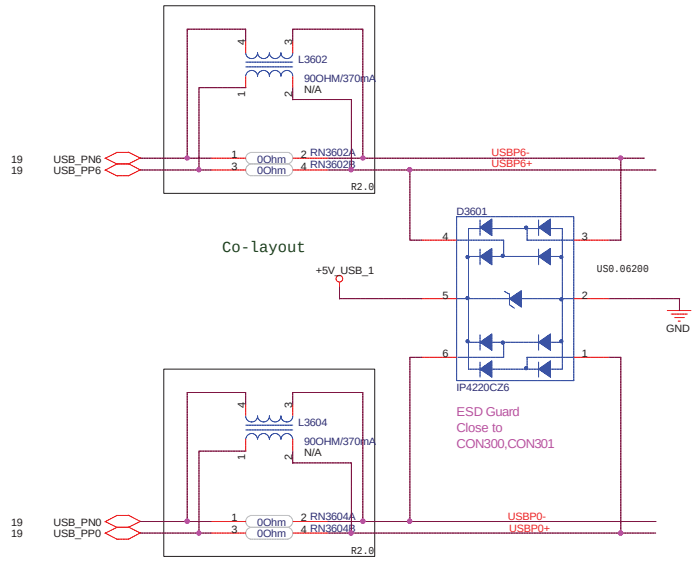
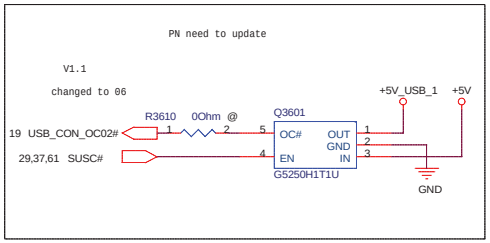


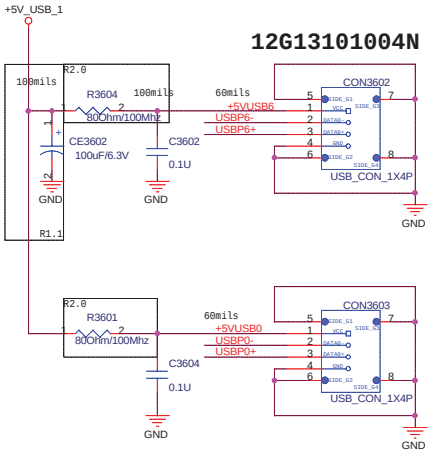


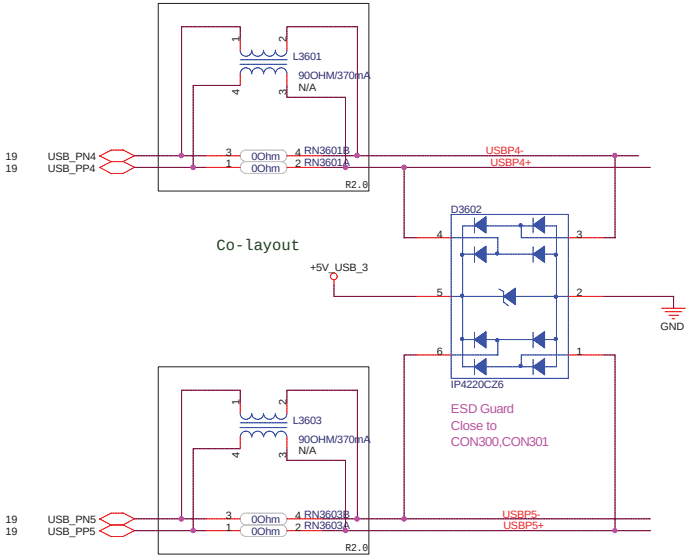
Default Group-optional

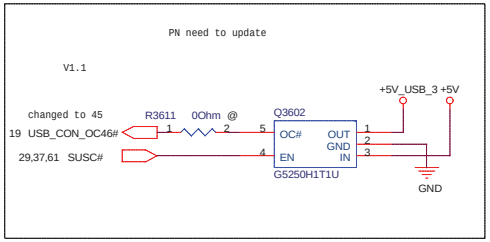
ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 35 of 63	

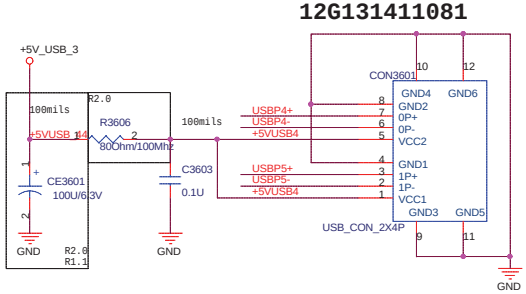






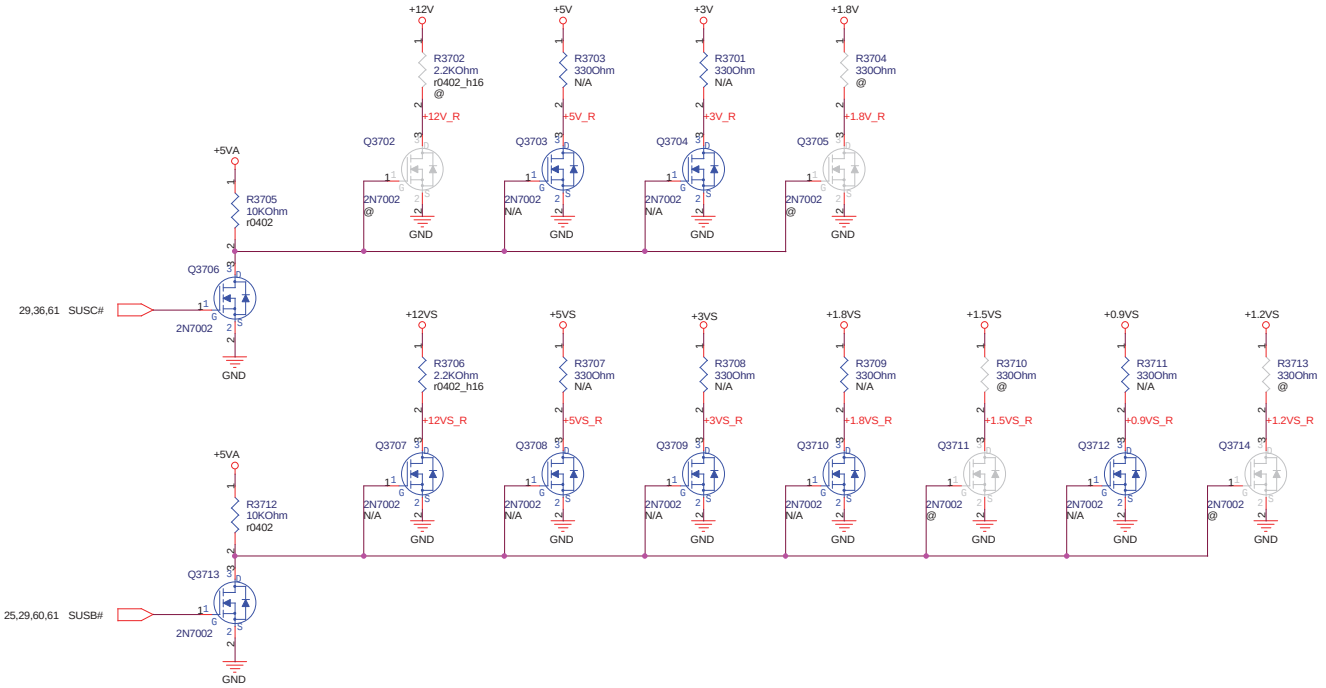






Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 36 of 63	

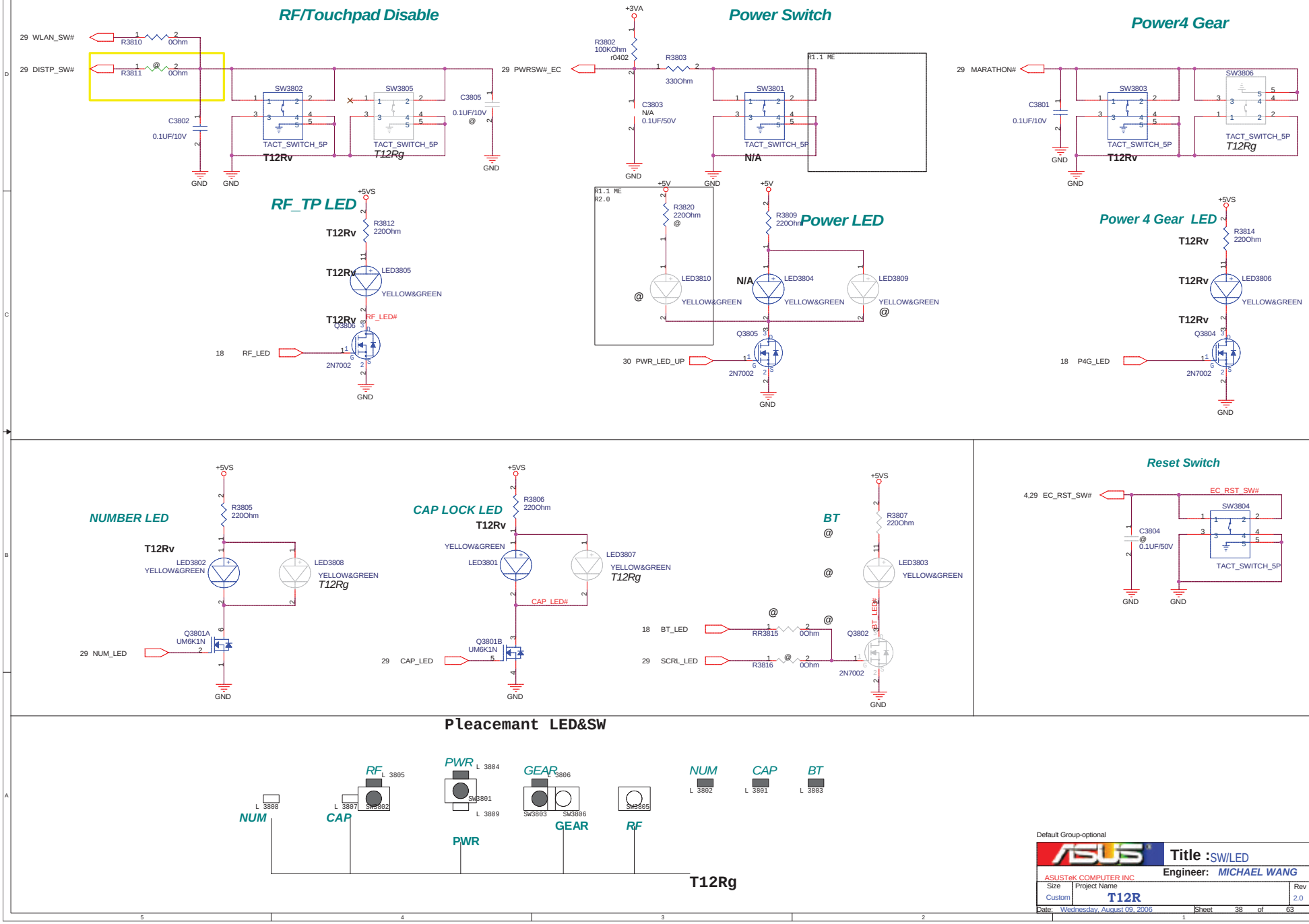


Check all power plan

Default Group-optional

ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 37 of 63	

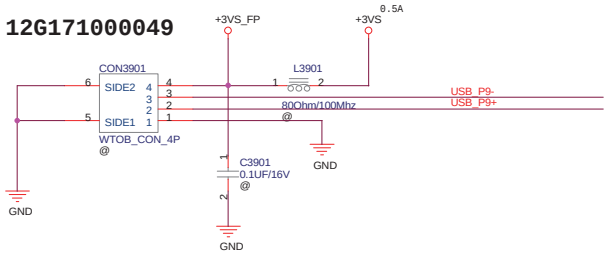
Main Board SW & LED

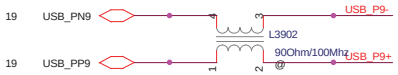


+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT





Default Group-optional

ASUSTeK COMPUTER INC

Title : FINGER PRINT

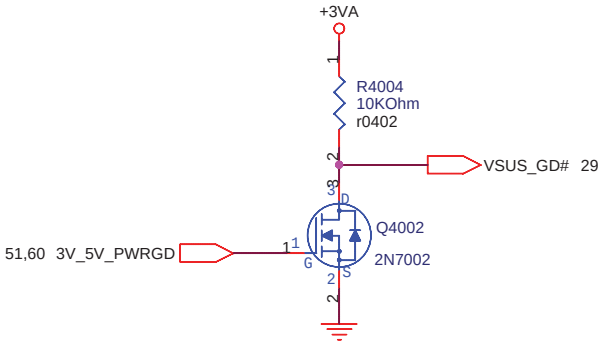
Engineer: MICHAEL WANG

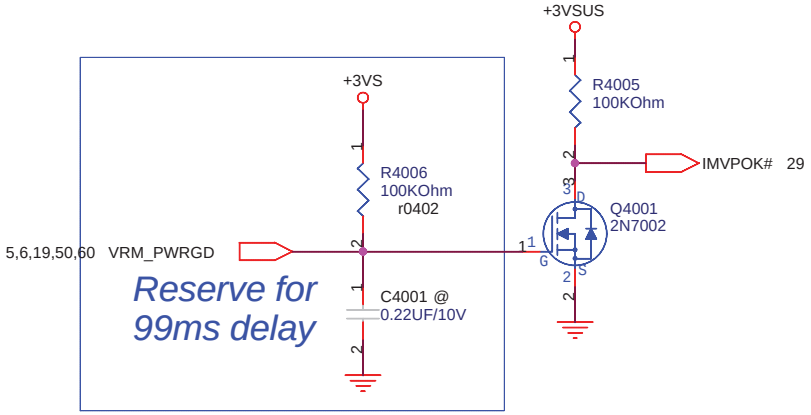
Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 39 of 63

+3VA
+3VS
+3VSUS

+3VA 12,29,38,54,57,59,63
+3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,42,43,50,52,60,61
+3VSUS 6,17,19,20,23,25,29,34,51





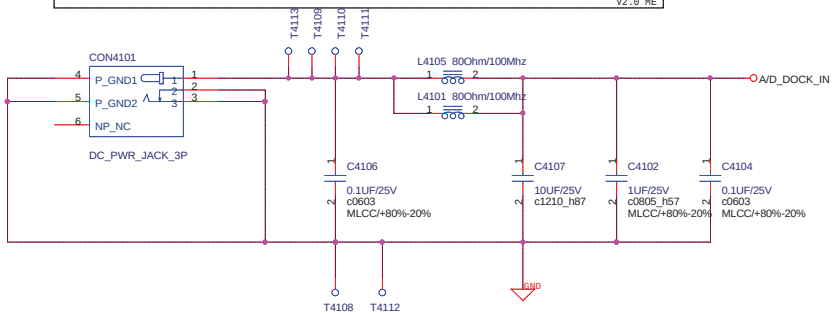
Default Group-optional

ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: MICHAEL WANG	
Size: A4	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 40 of 63	

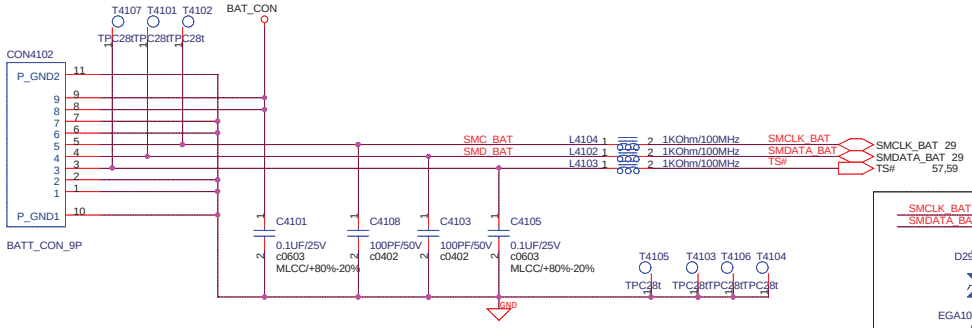
A/D_DOCK_IN
BAT_CON
AC_BAT_SYS

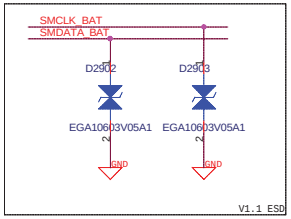
12G145002034=>12G14530103E

V2.0 ME

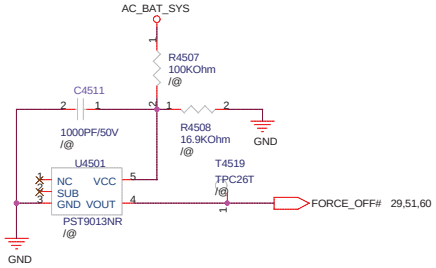


12G200010090G





Without Battery & Pull out Adapter
RESERVED



Default Group-optional

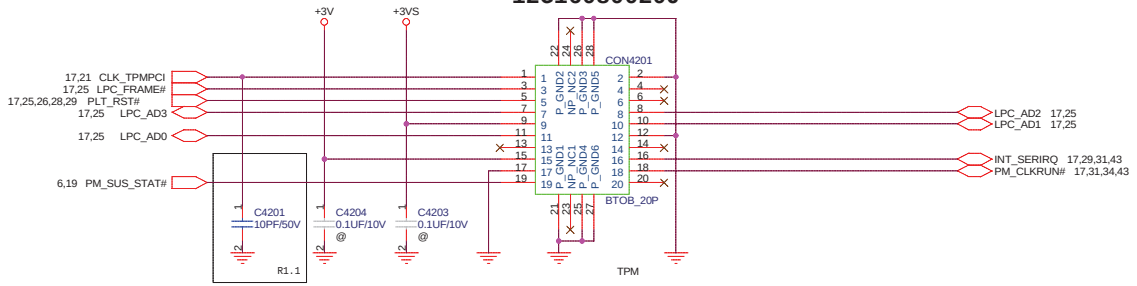
ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : DC IN	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 41 of 63	

+3VS +3VS 4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

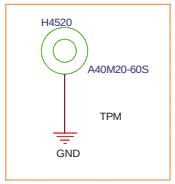
+3V +3V 17,25,26,27,31,35,37,43,44,61

TPM Module CON
RESERVED

12G16080020J



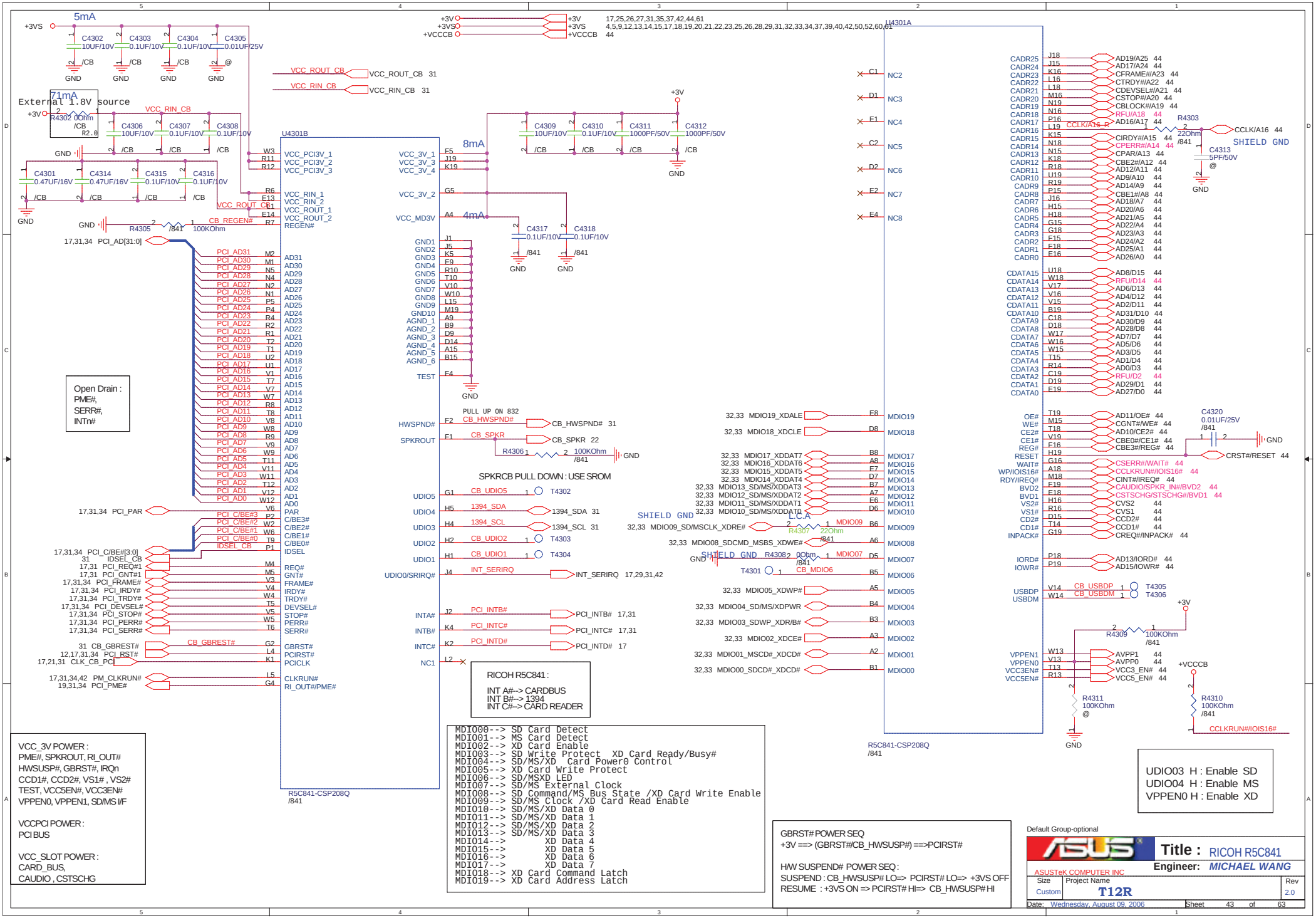
I

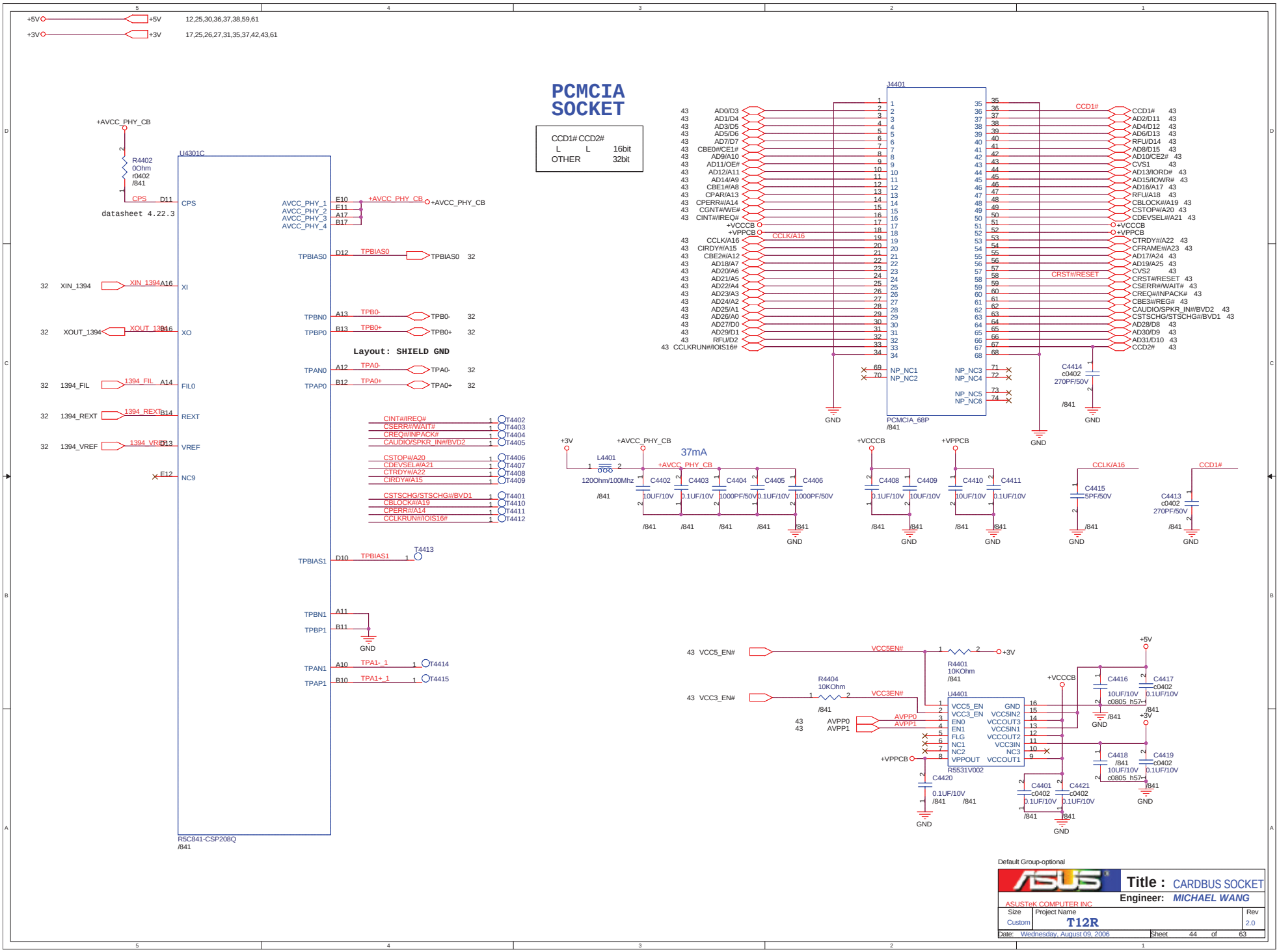


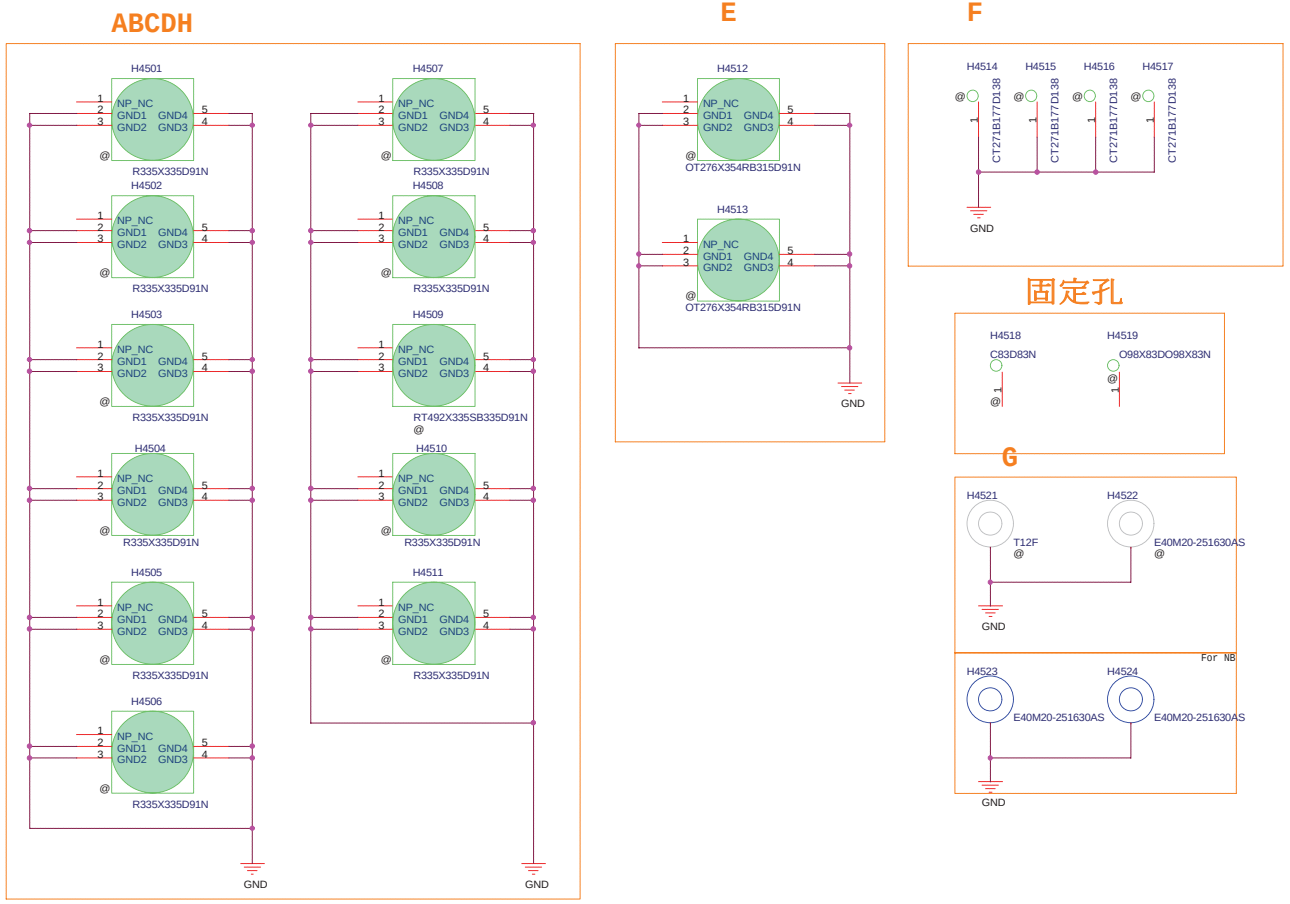
For TPM CONN.

Default Group-optional

ASUSTek COMPUTER INC	Project Name: T12R	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 42 of 63	







Default Group-optional

ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 45 of 63	

Default Group-optional

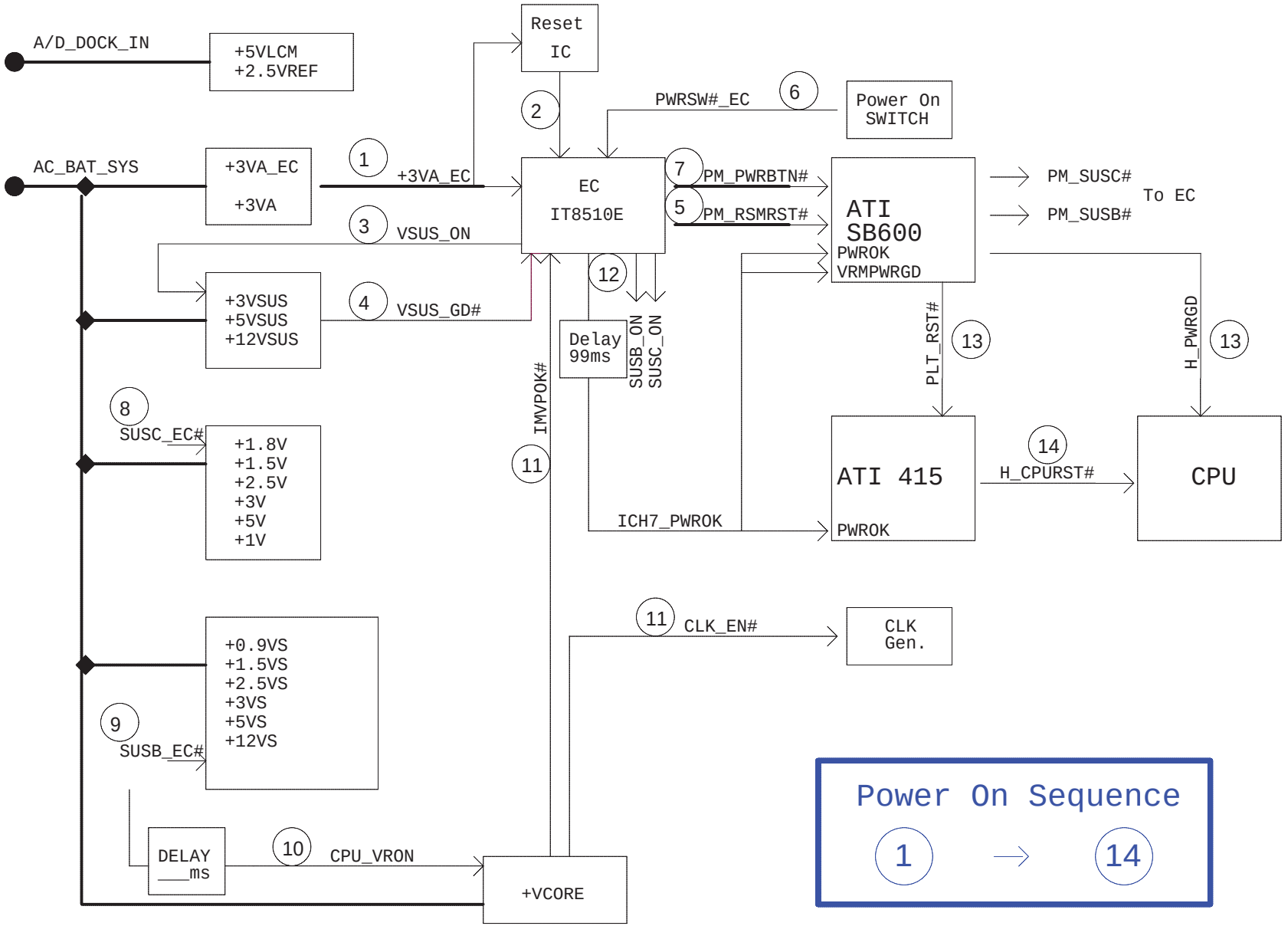
Title : HISTORY

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 46 of 63



Default Group-optional

Title : FLOWCHART

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 47 of 63

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

Default Group-optional

Title : GPIO Setting

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

Date: Wednesday, August 09, 2006 Sheet 48 of 63

T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9.All PCI clock added 6.8 pF to decrease skew.
10.PWM connected to EC and back-light connected to NB
11.D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12.page 19, added BT_DET# to detect BT.
13.Page 19, adjust USB OC ping to correspond USB port
14.Page 25, modification NEW CARD debug circuit to correspond new debug card
15.page 28, we used correctly capacity for customer request.
16.page 36, we used LDO with over current protect IC
17.page 41, DC in connector add 2nd source.
ME modify
1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加螺絲鎖付記號

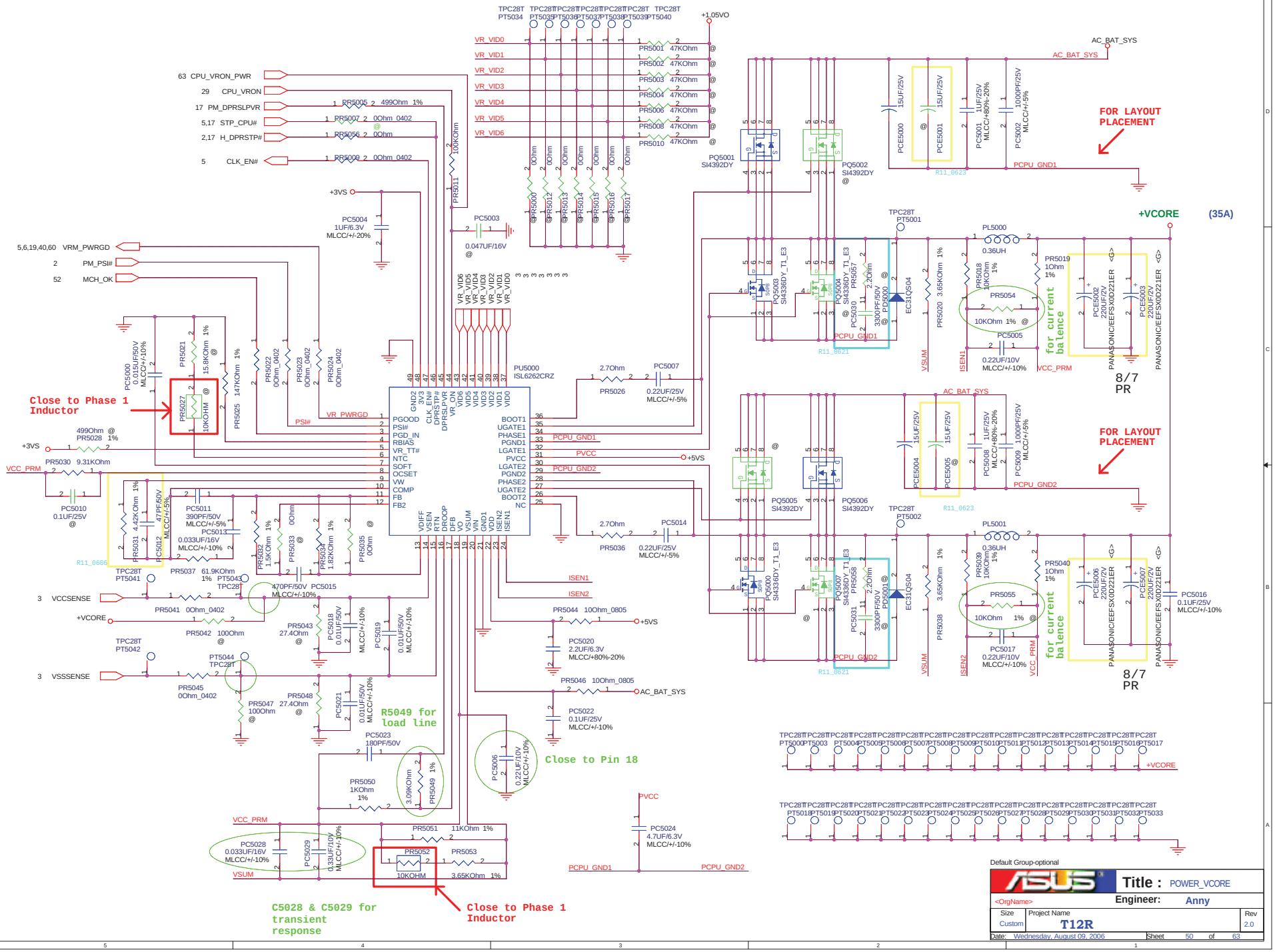
6.DDR2 added 2nd source
  P/N :12G025022004
  DDR2 DIMM 200P,1.8V,H:4mm,STD
  FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.連版圖修改

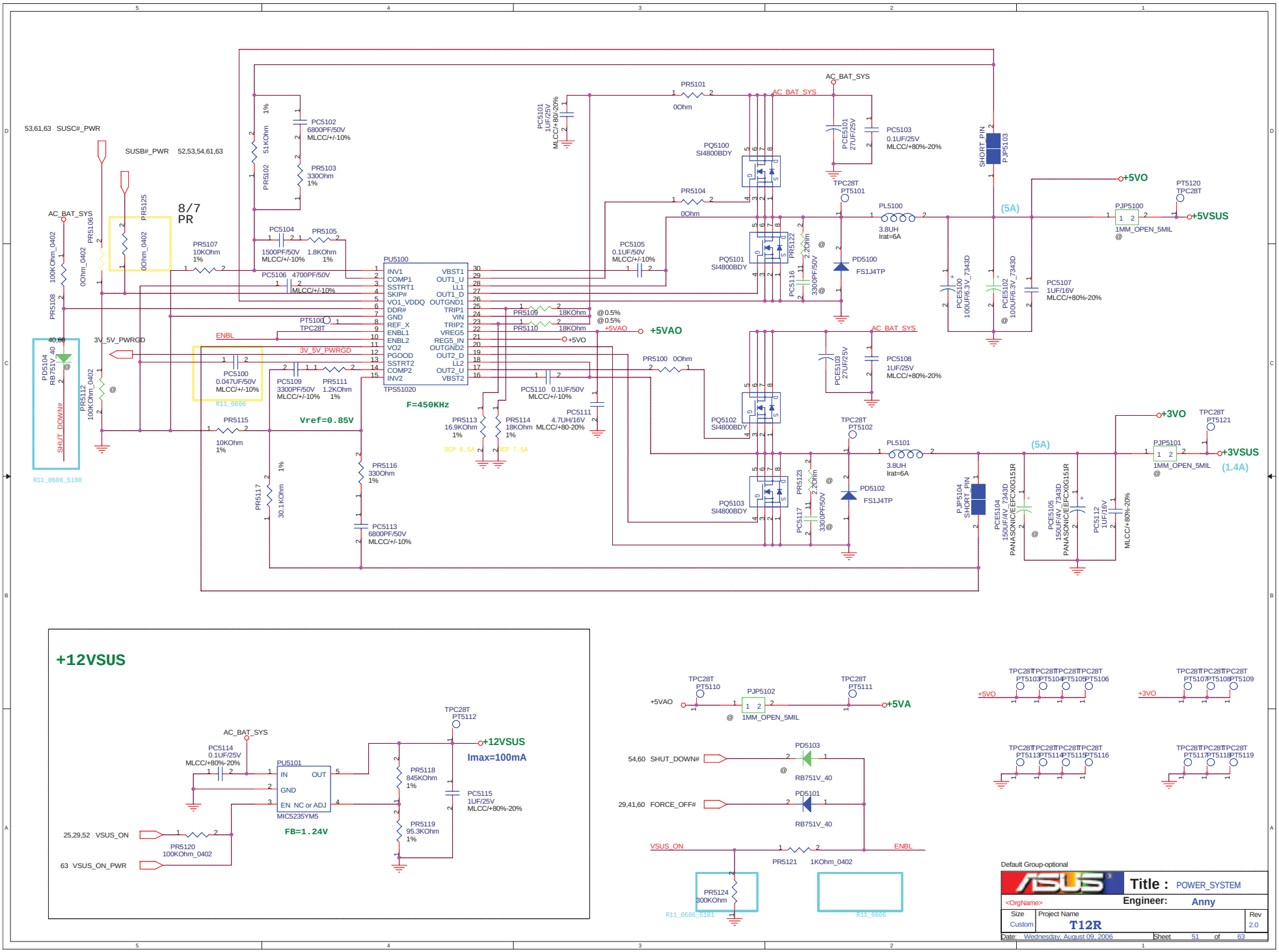
T12R V2.0 Modify History

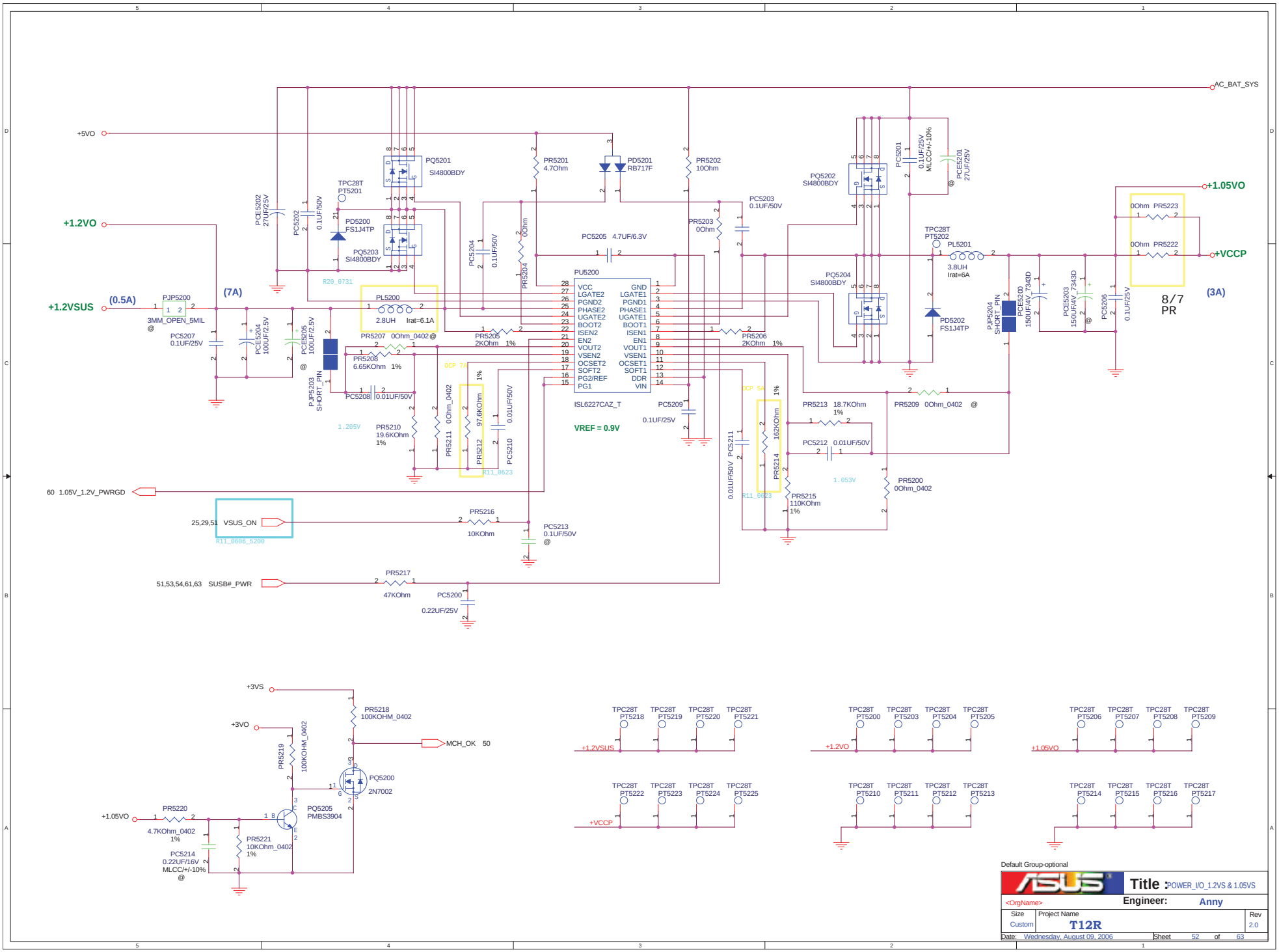
1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 10U with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006~3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

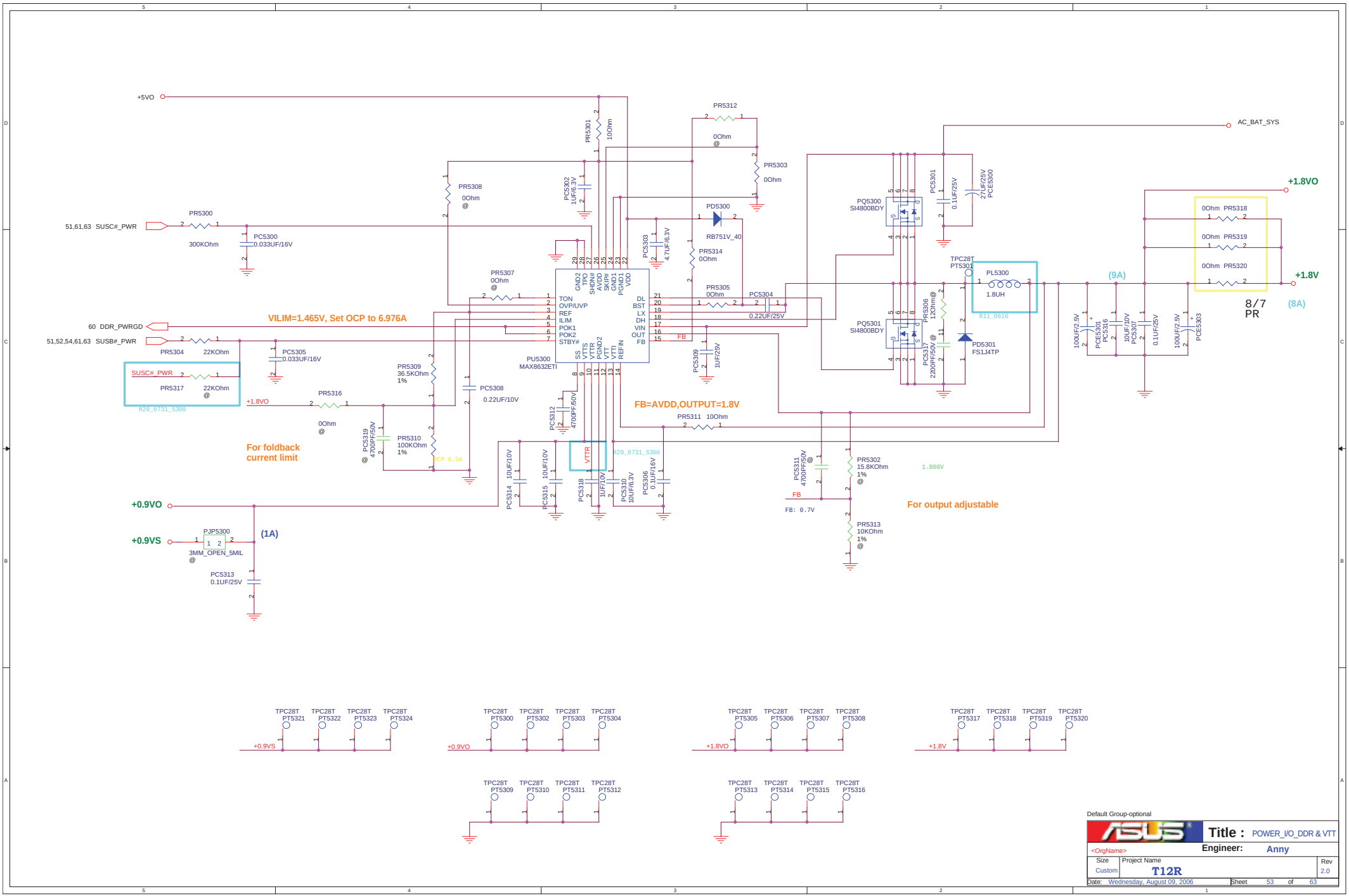
Default Group-optional

ASUS	Title : HISTORY	
<OrgName>	Engineer:	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 49 of 63	

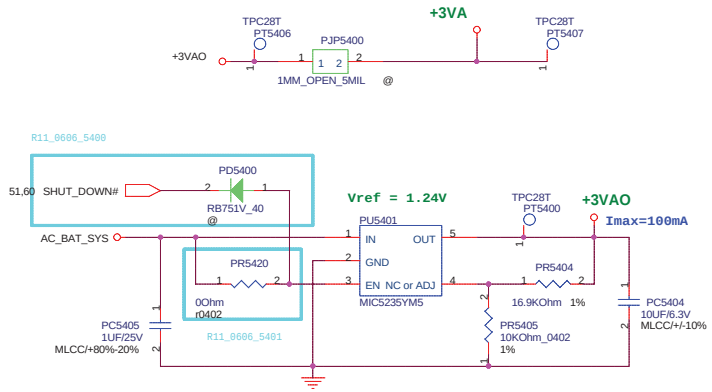




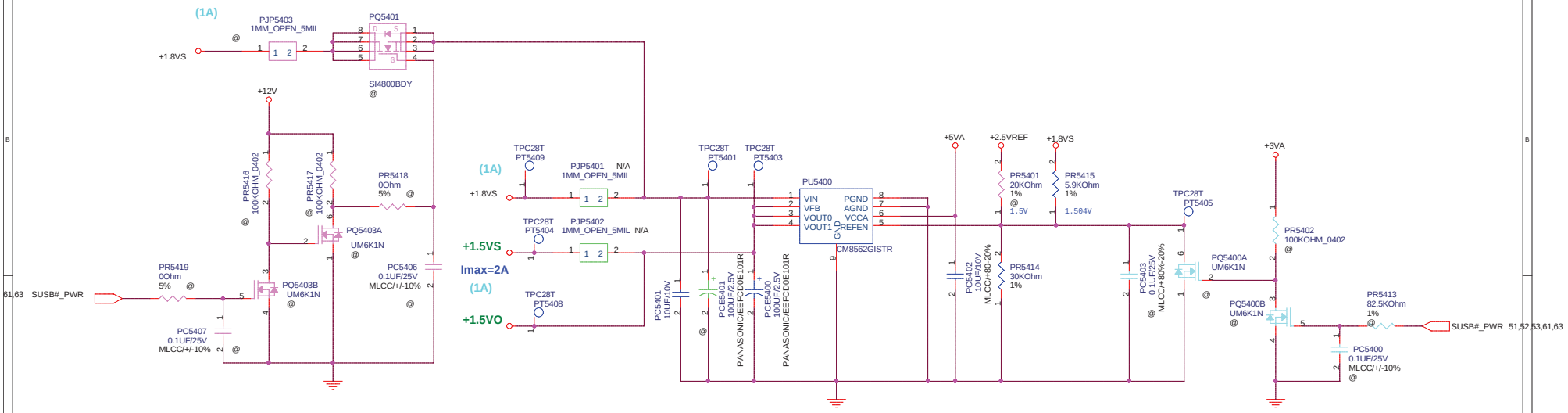




+3VA0

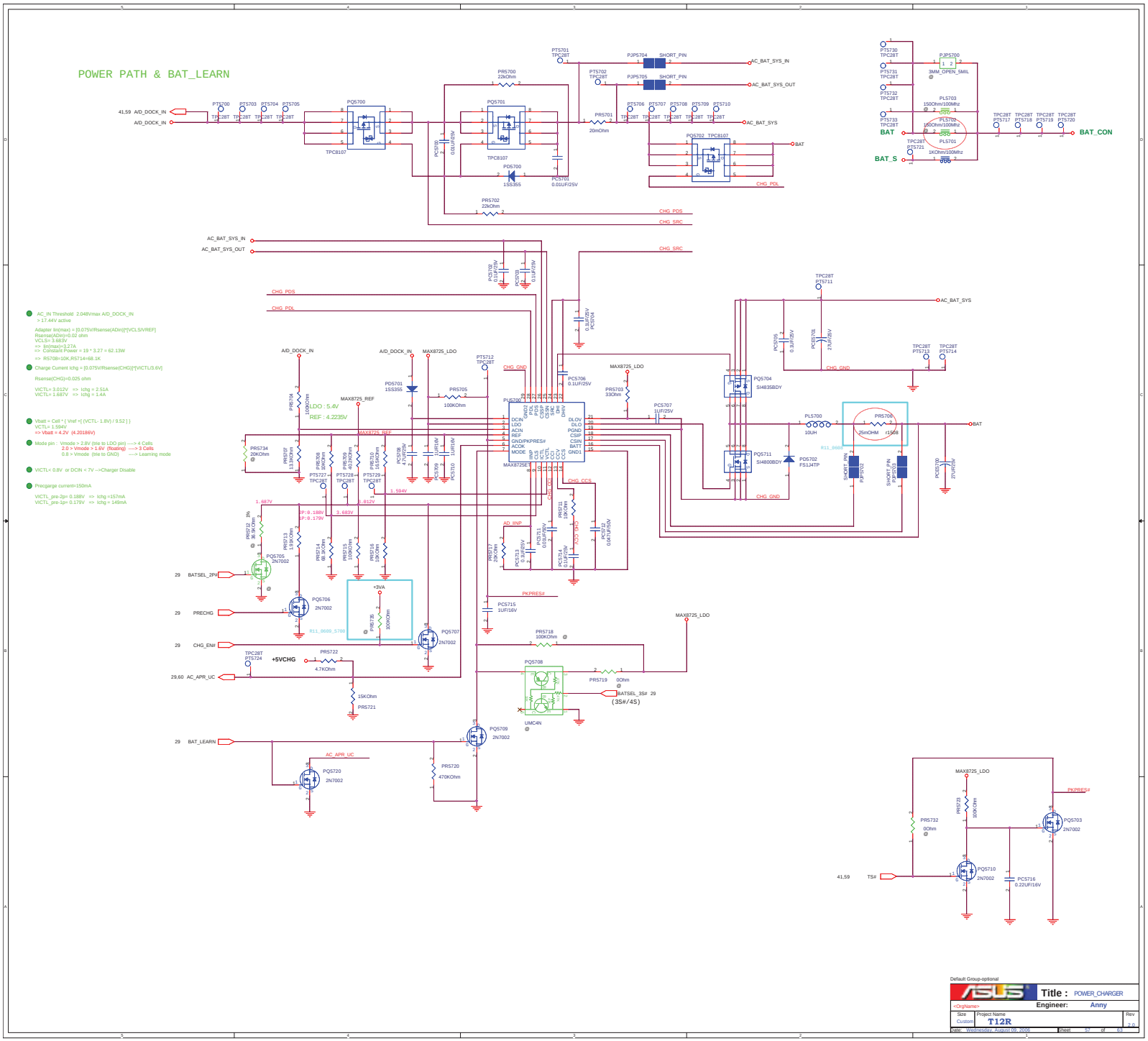


+2.5VS

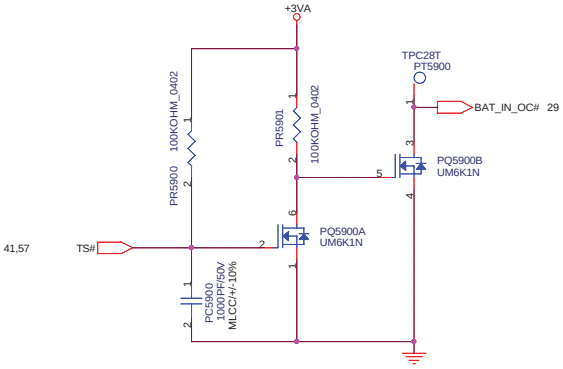


Default Group-optional

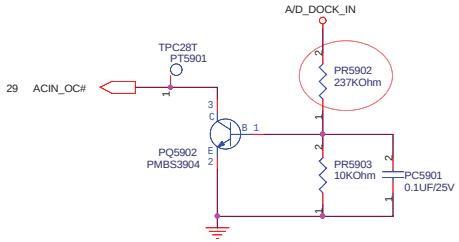
ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 54 of 63	



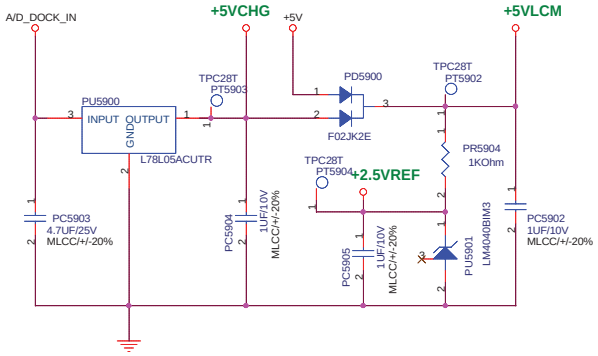
BATTERY IN DETECT



ADAPTER IN DETECT

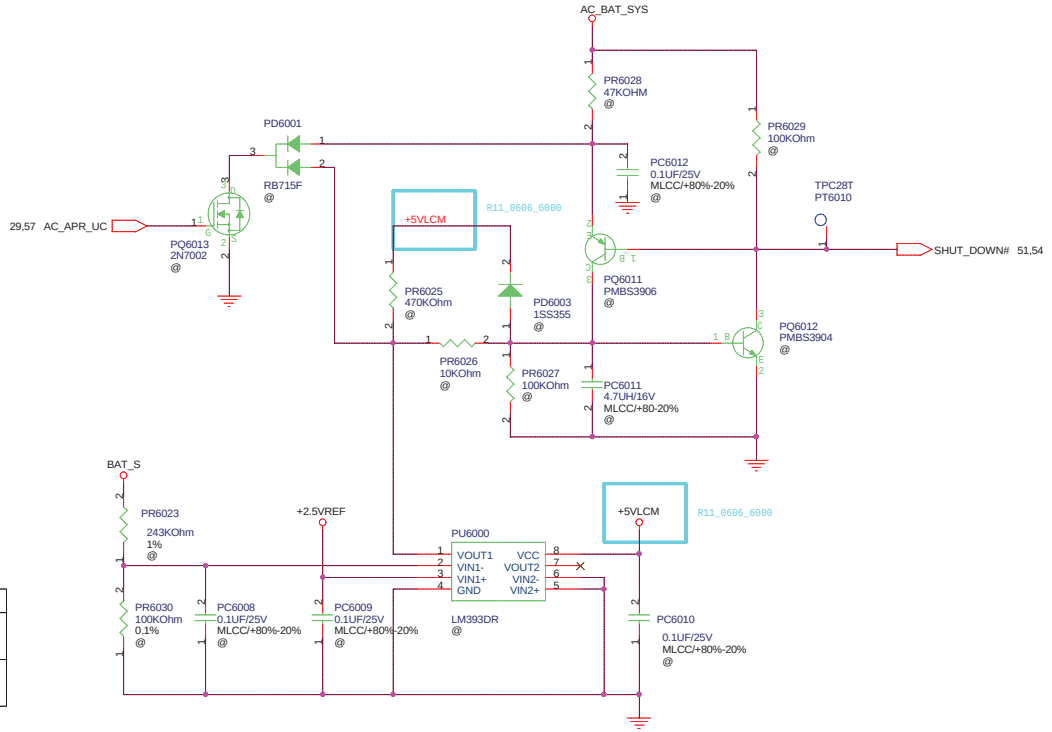


+5VLCM, +5VCHG & +2.5VREF



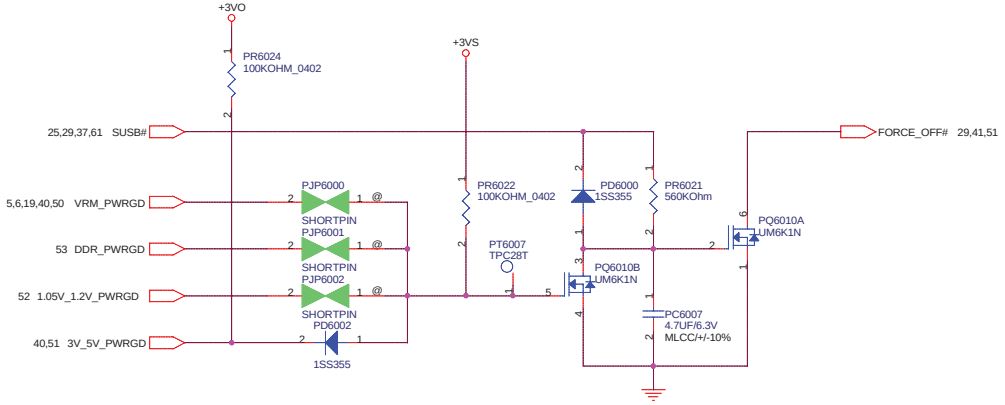
Default Group-optional

<OrgName>	Title : POWER_DETECT	
	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 59 of 63	



	8.575V	11.625V
R6023	243KOhm 10G213243313030 1%	365KOhm 10G213365313010 1%
R6024	100KOhm 10G213100323010 0.1%	100KOhm 10G213100323010 0.1%

POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD

TPC28T PT6004 1 DDR_PWRGD

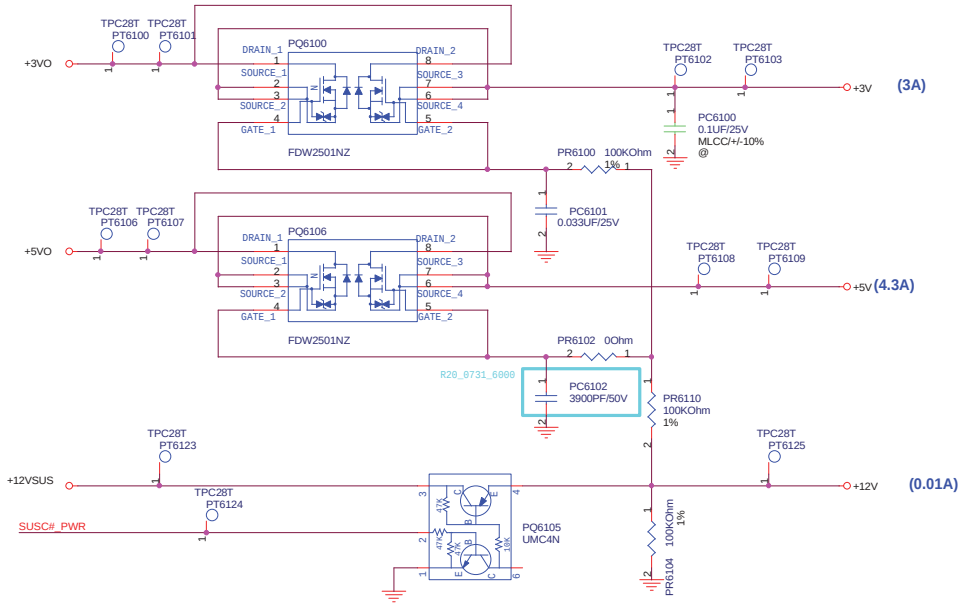
TPC28T PT6005 1 3V_5V_PWRGD

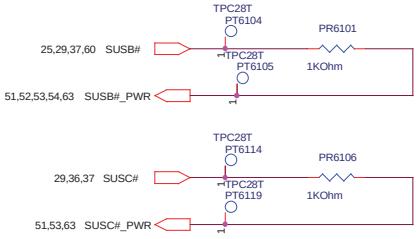
TPC28T PT6006 1 1.05V_1.2V_PWRGD

Default Group-optional

<OrgName>	Title : POWER_PROTECT	
	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 60 of 63	

SUSC#_PWR POWER





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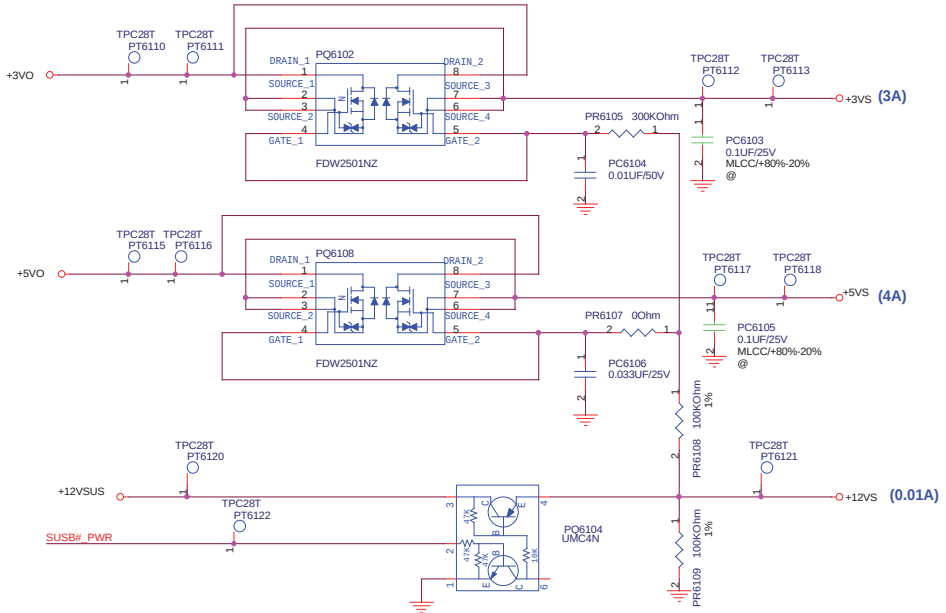
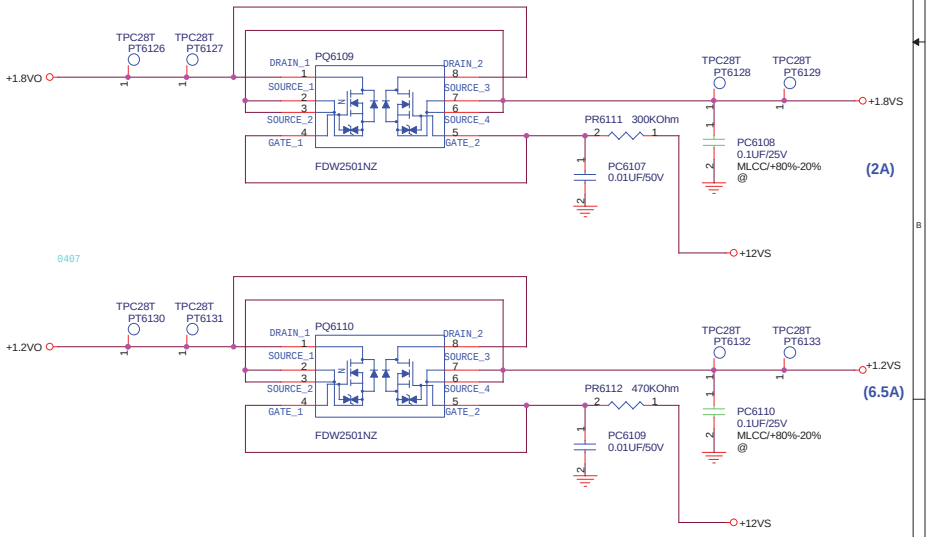
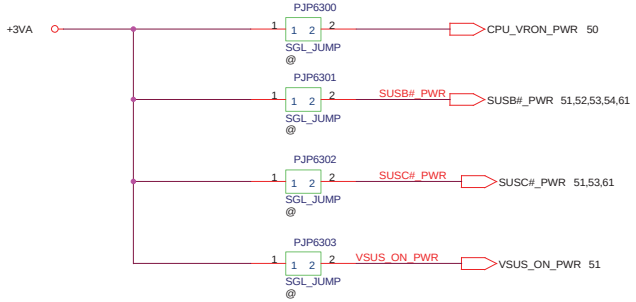




Default Group-optional

ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 61 of 63	

FOR POWER TEST



Default Group-optional

<OrgName>	Title : POWER_SIGNAL	
	Engineer: Anny	
Size: Custom	Project Name: T12R	Rev: 2.0
Date: Wednesday, August 09, 2006	Sheet 63 of 63	

R1.1

Item	Before	After	Reason	Owner	Date
R11_0606_5100		Add PD5104	for shutdown application		2006.06.06
R11_0606	PC5100: 0.01uF	PC5100 change to 0.047uF	for EE timing request		2006.06.06
R20_0606_5101		add PR5124	Pull ground to avoid vsus_on is float.		2006.06.06
R11_0606_5200	VSUS_ON_PWR	VSUS_ON			2006.06.06
R11_0609_5700		Add PR5735 to +3VA on CHG_EN# pin	To avoid CHG_EN# pin floating in initial		2006.06.06

R2.0

Item	Before	After	Reason	Owner	Date
R20_0731_6000	0.047uF	3900pF	for EE timing request		2006.07.31
R20_0731_5300	None	VTTR	For DDR Vref		2006.07.31

R2.0

Item	Before	After	Reason	Owner	Date

Default Group-optional

<OrgName>

Title : POWER_PIC

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

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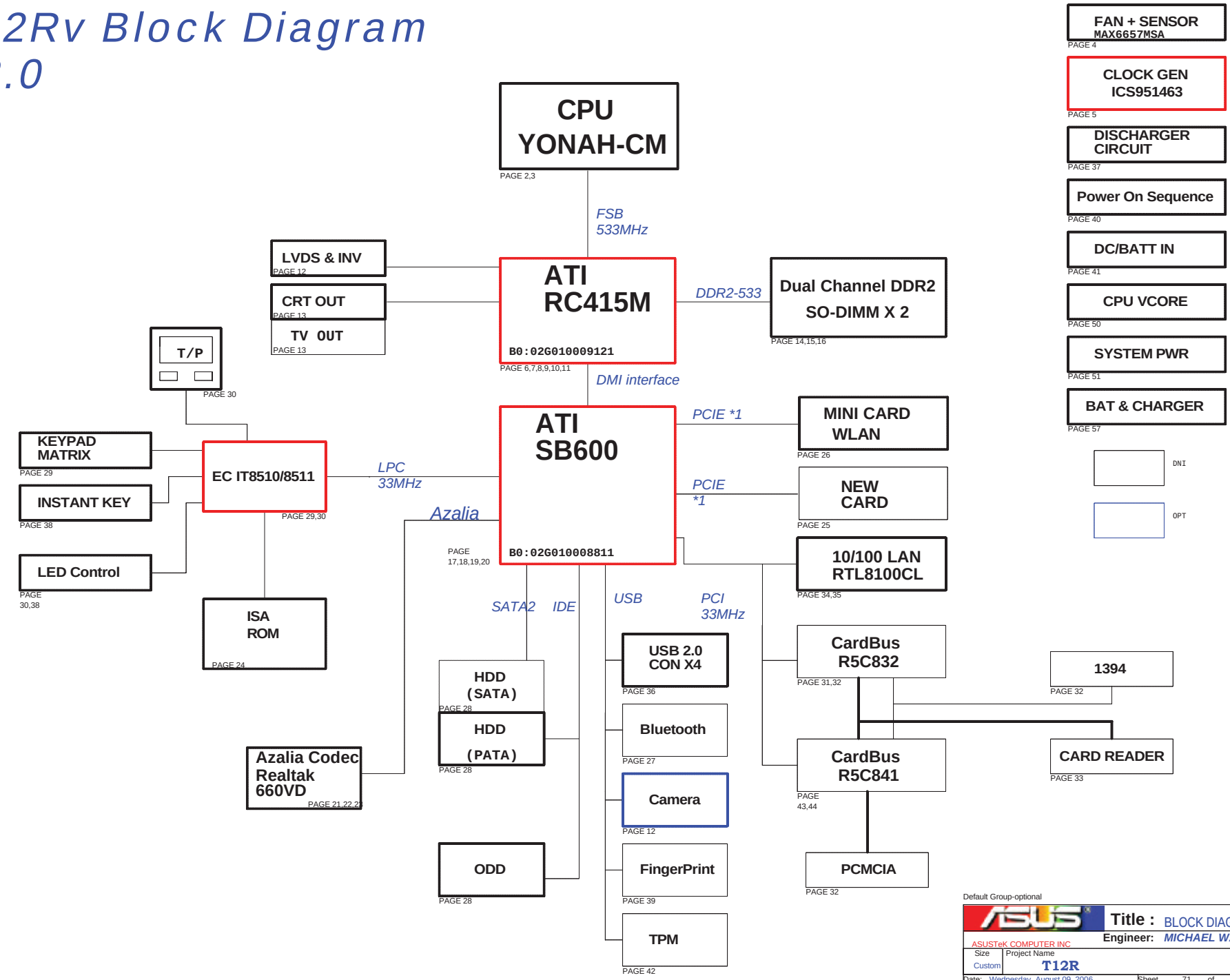
T12Rv Block Diagram V2.0



Default Group-optional

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	T12R	2.0

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T12Rg Block Diagram V1.1