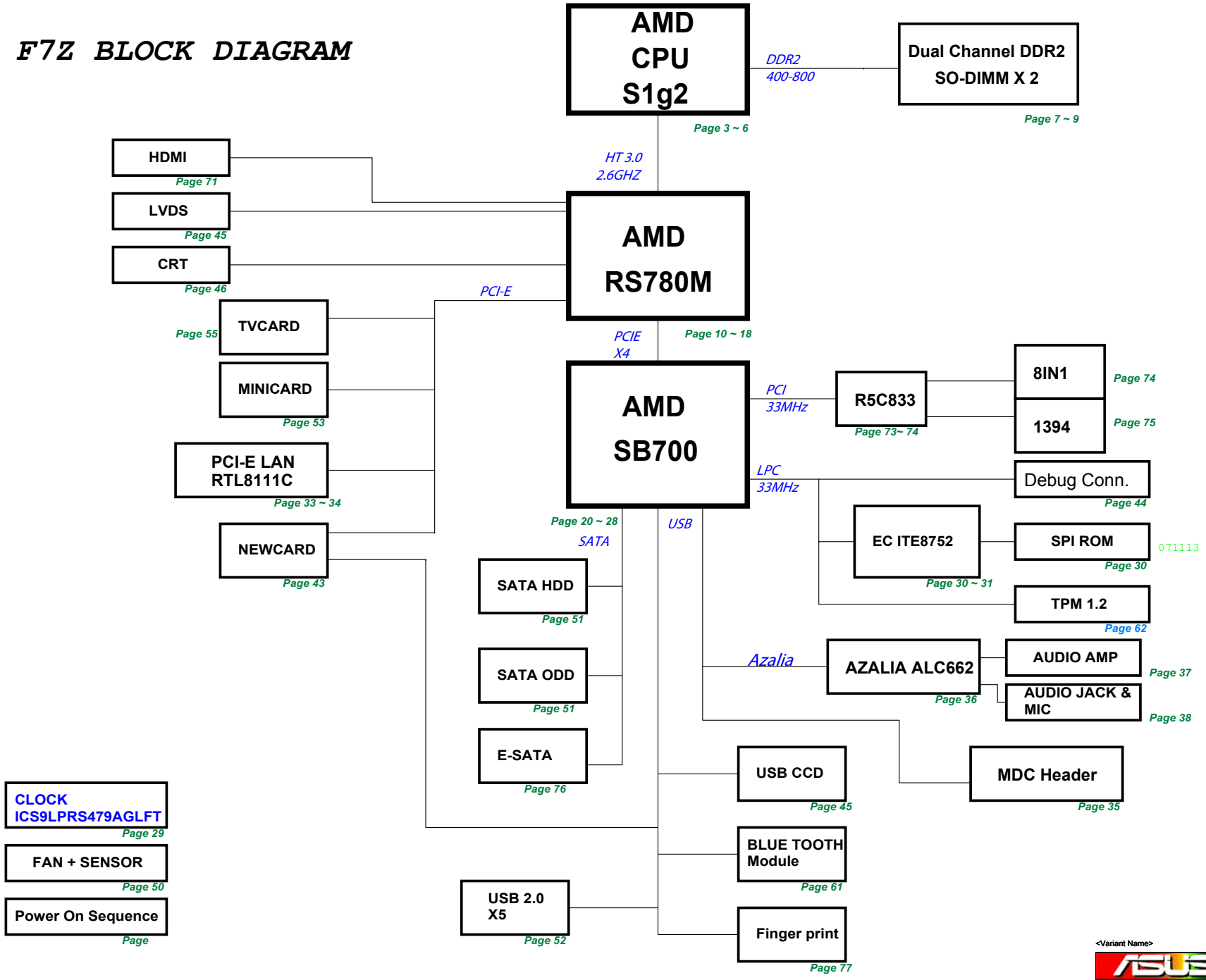
F7Z BLOCK DIAGRAM



<Variant Name>

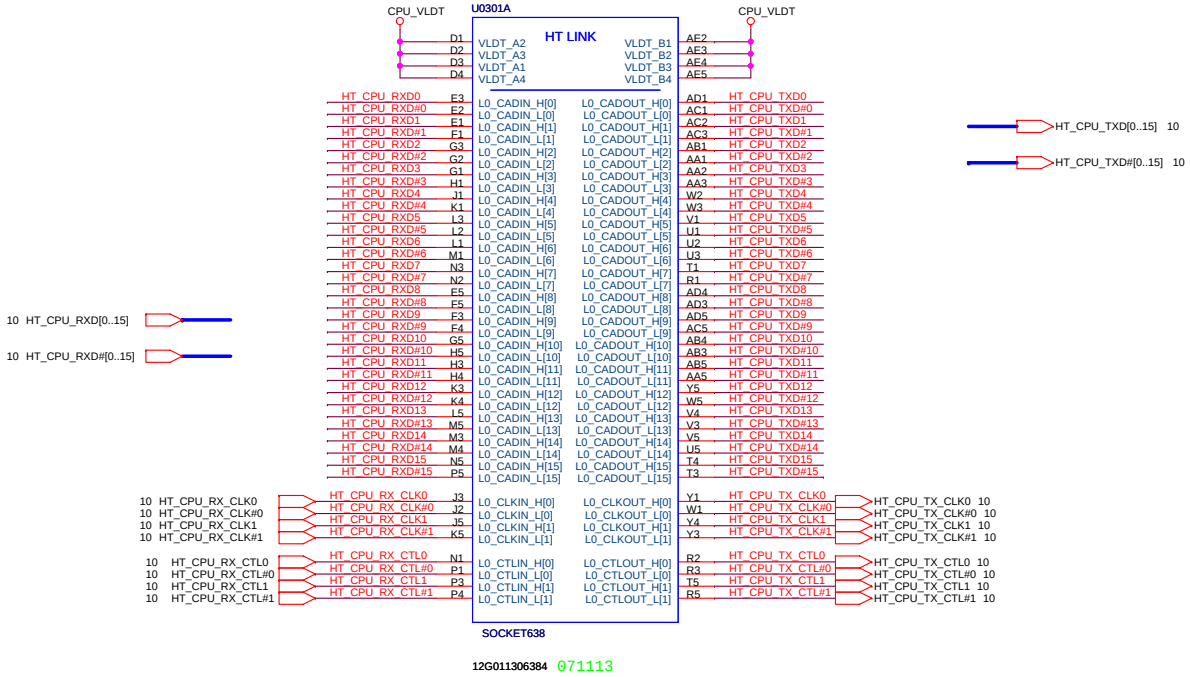
ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer:

Size	Project Name	Rev
Custom	F7Z	2.0

Date: Monday, May 19, 2008 Sheet 1 of 94



10 HT_CPU_RXD[0..15]

10 HT_CPU_RXD#[0..15]

HT_CPU_TXD[0..15] 10

HT_CPU_TXD#[0..15] 10

10 HT_CPU_RX_CLK0
10 HT_CPU_RX_CLK#0
10 HT_CPU_RX_CLK1
10 HT_CPU_RX_CLK#1

10 HT_CPU_RX_CTL0
10 HT_CPU_RX_CTL#0
10 HT_CPU_RX_CTL1
10 HT_CPU_RX_CTL#1

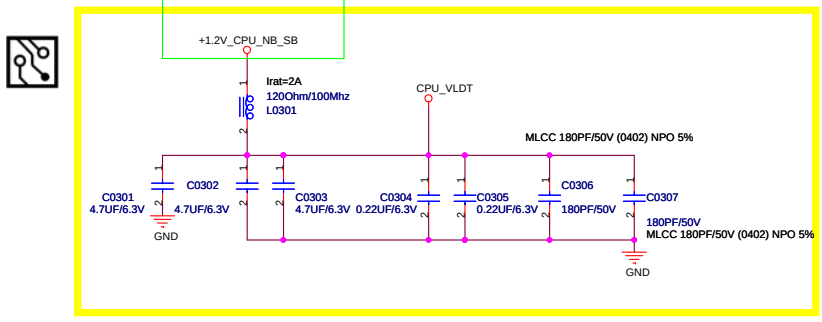
HT_CPU_TX_CLK0 10
HT_CPU_TX_CLK#0 10
HT_CPU_TX_CLK1 10
HT_CPU_TX_CLK#1 10

HT_CPU_TX_CTL0 10
HT_CPU_TX_CTL#0 10
HT_CPU_TX_CTL1 10
HT_CPU_TX_CTL#1 10

12G011306384 071113

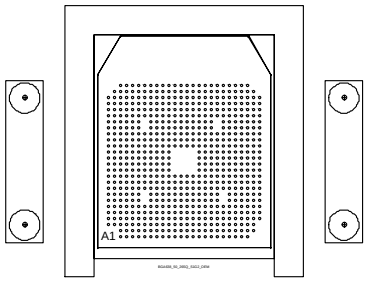
Do not cross plane.

071219 Recover



Place close to socket

*** If VLDT is connected only on one side, one 4.7uF cap should be added to the island side**



ASUSTeK.Computer.INC

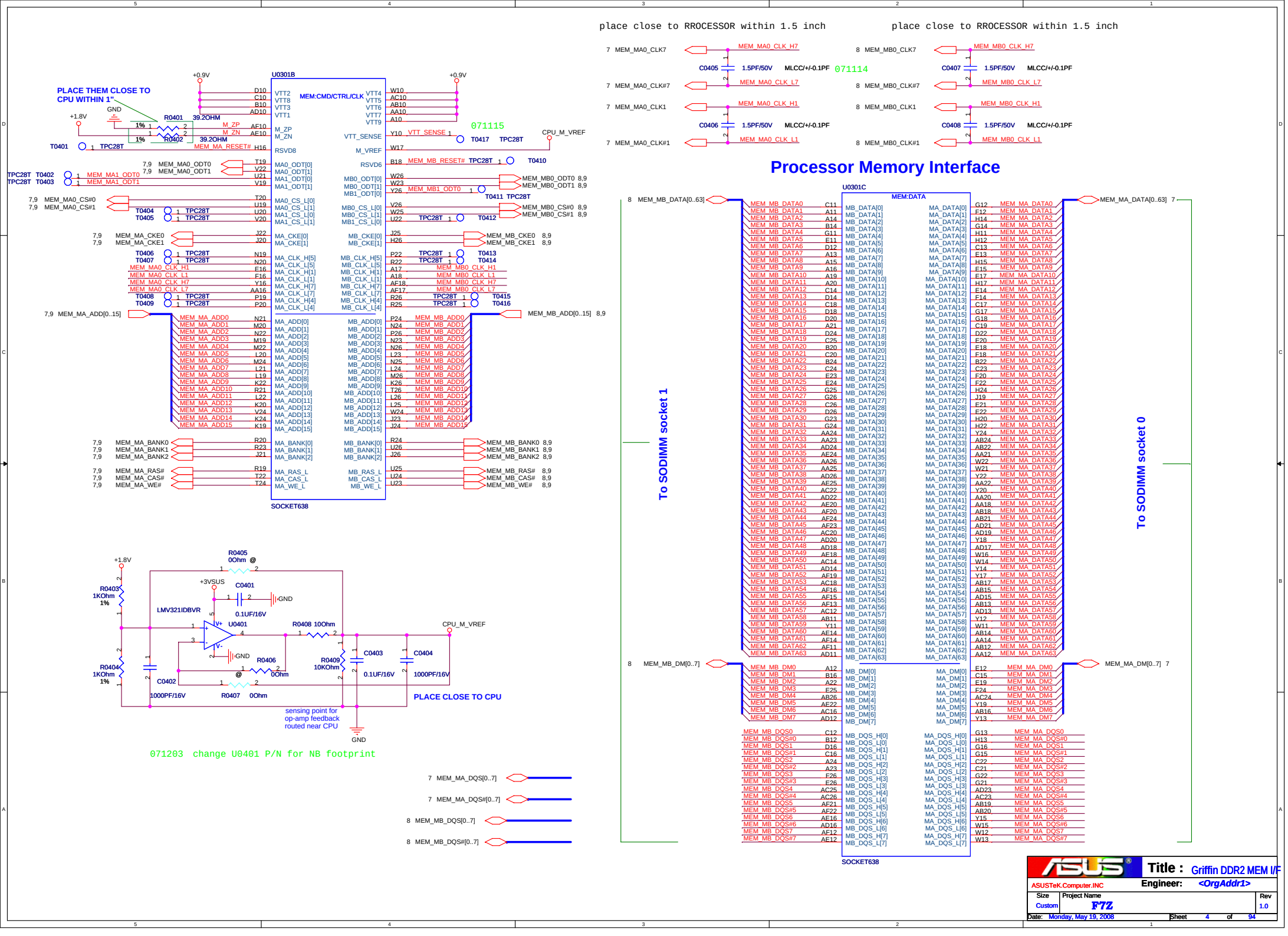
Title : Griffin HT I/F

Engineer: <OrgAddr1>

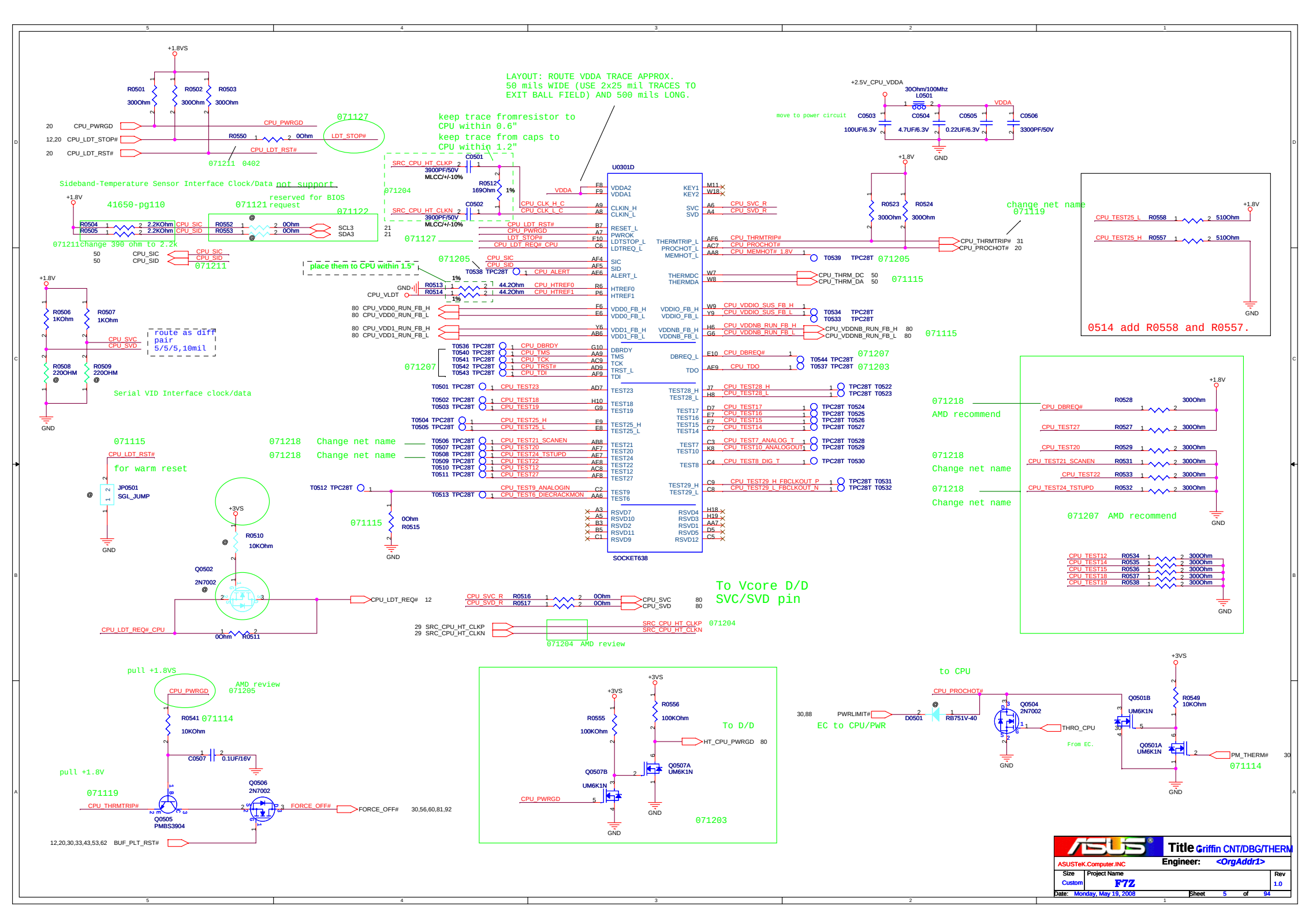
Size	Project Name	Rev
Custom	F7Z	1.0

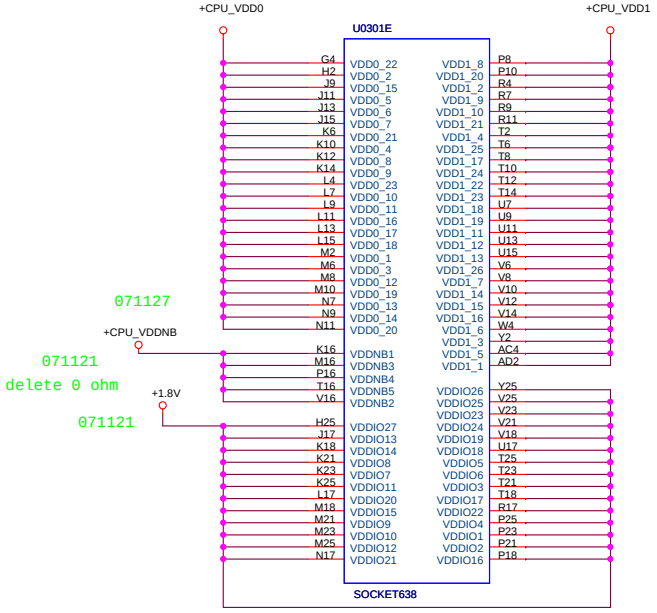
Date: Monday, May 19, 2008 Sheet 3 of 94

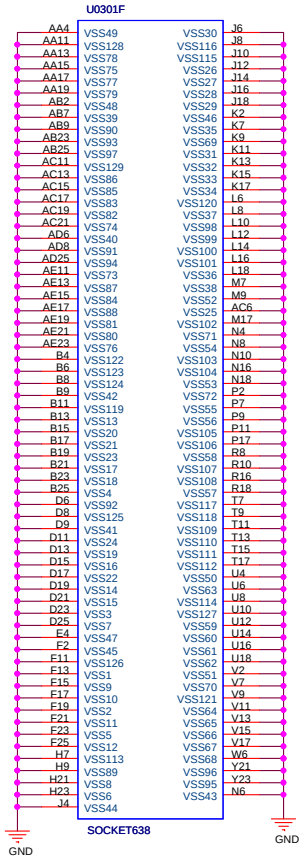
Processor Memory Interface



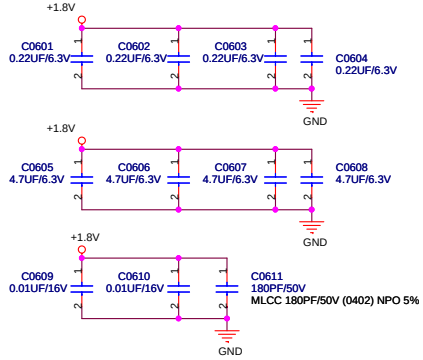
Title :	Griffin DDR2 MEM I/F		
ASUSTeK.Computer.INC	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 4 of 94		


LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
keep trace fromresistor to
CPU within 0.6"
keep trace from caps to
CPU within 1.2"
place them to CPU within 1.5"
U0301D
SOCKET638
Sideband-Temperature Sensor Interface Clock/Data not support
41650-pg110
reserved for BIOS request
change 390 ohm to 2.2k
route as diff pair 5/5/5,10mil
Serial VID Interface clock/data
for warm reset
Change net name
AMD recommend
To Vcore D/D
SVC/SVD pin
AMD review
pull +1.8VS
pull +1.8V
to CPU
EC to CPU/PWR
From EC.
0514 add R0558 and R0557.
Title Griffin CNT/DBG/THERM
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Project Name F7Z
Date: Monday, May 19, 2008
Sheet 5 of 94

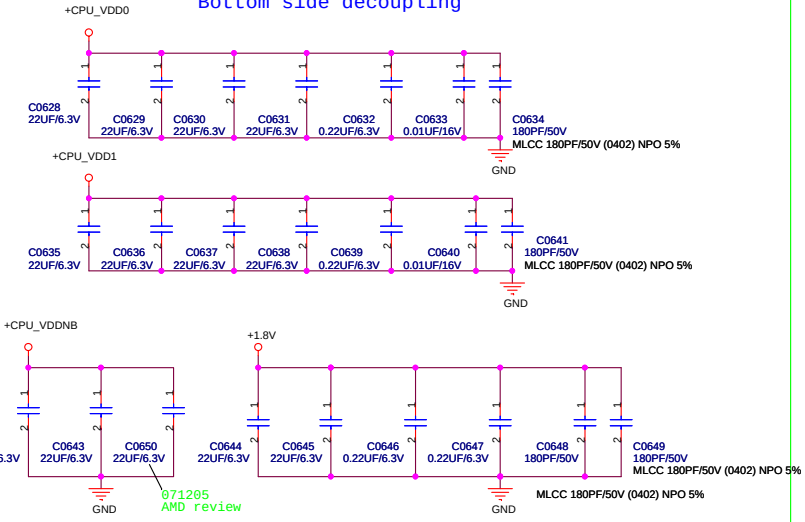




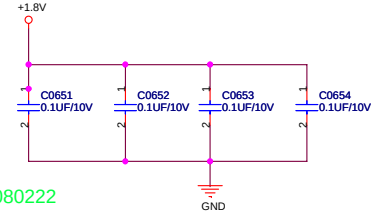
Decoupling between Processor and DIMMs, Place close to Porcessor as possible



Bottom side decoupling

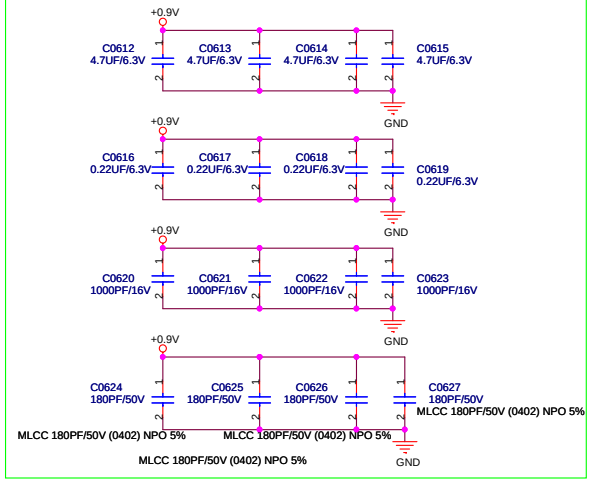


add MLCC 0.1UF/10V (0402) X7R 10% for EMI between +1.8v to GND moat.



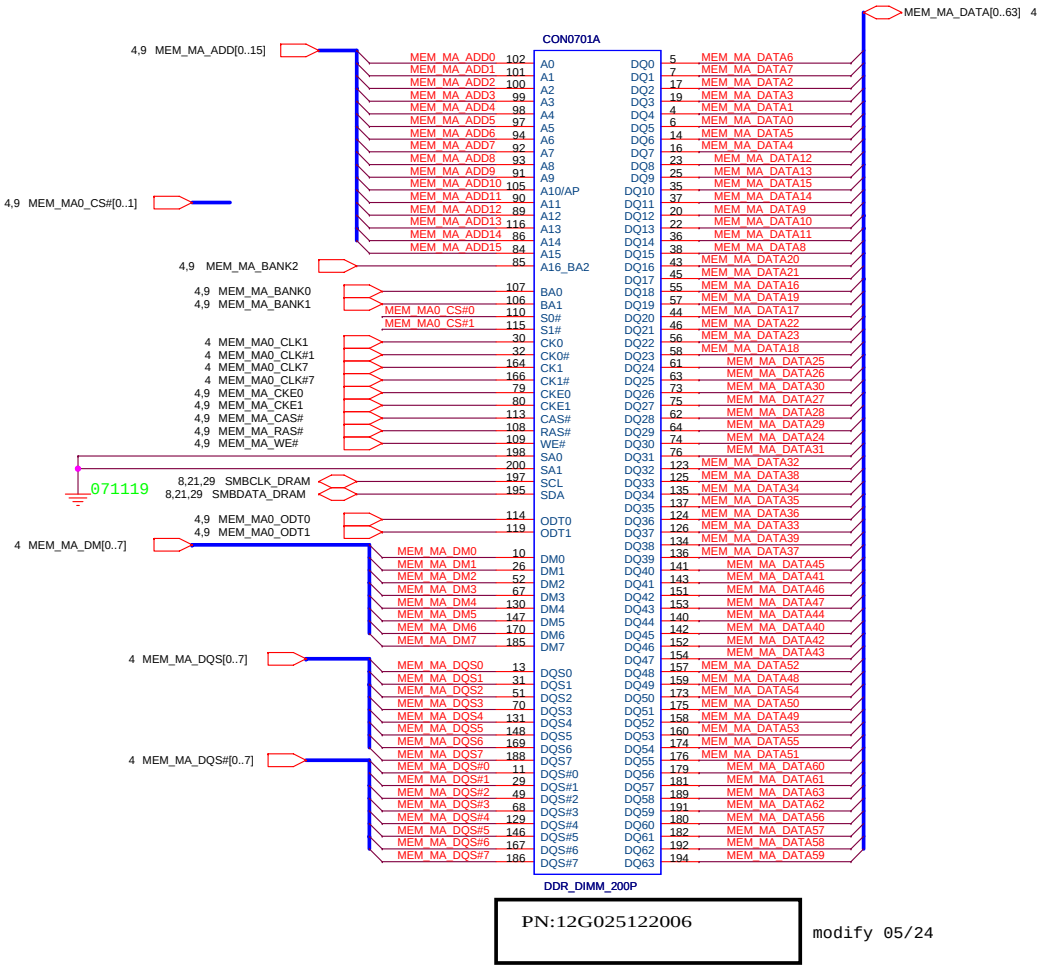
080222

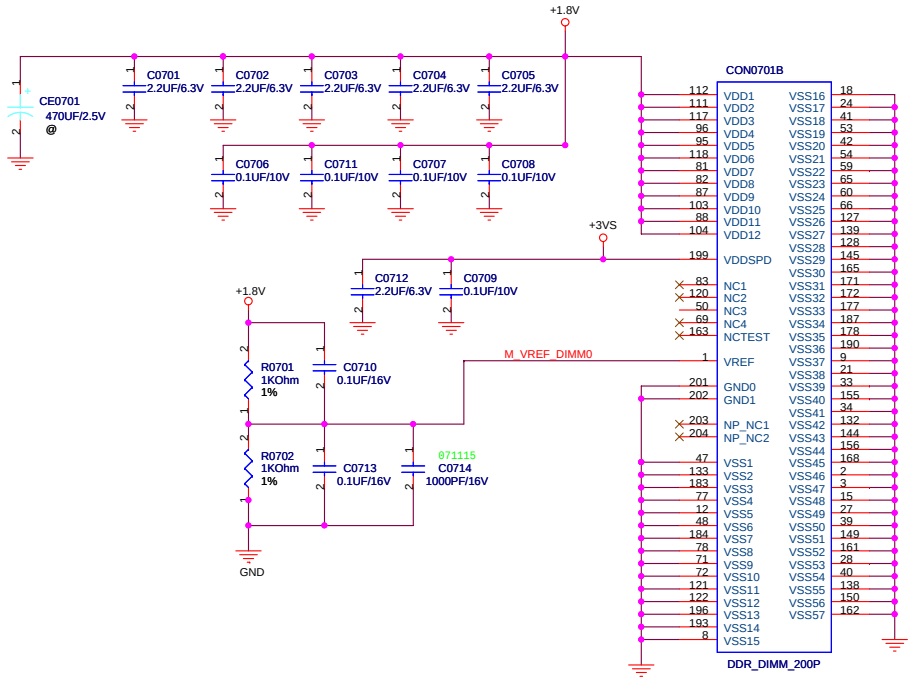
place close to socket



ASUSTeK.Computer.INC	Title : Griffin Power	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 6 of 94	

080220
SWAP





PN:12G025122006

modify 05/24

<Variant Name>

Title : DDR2 SO-DIMM0

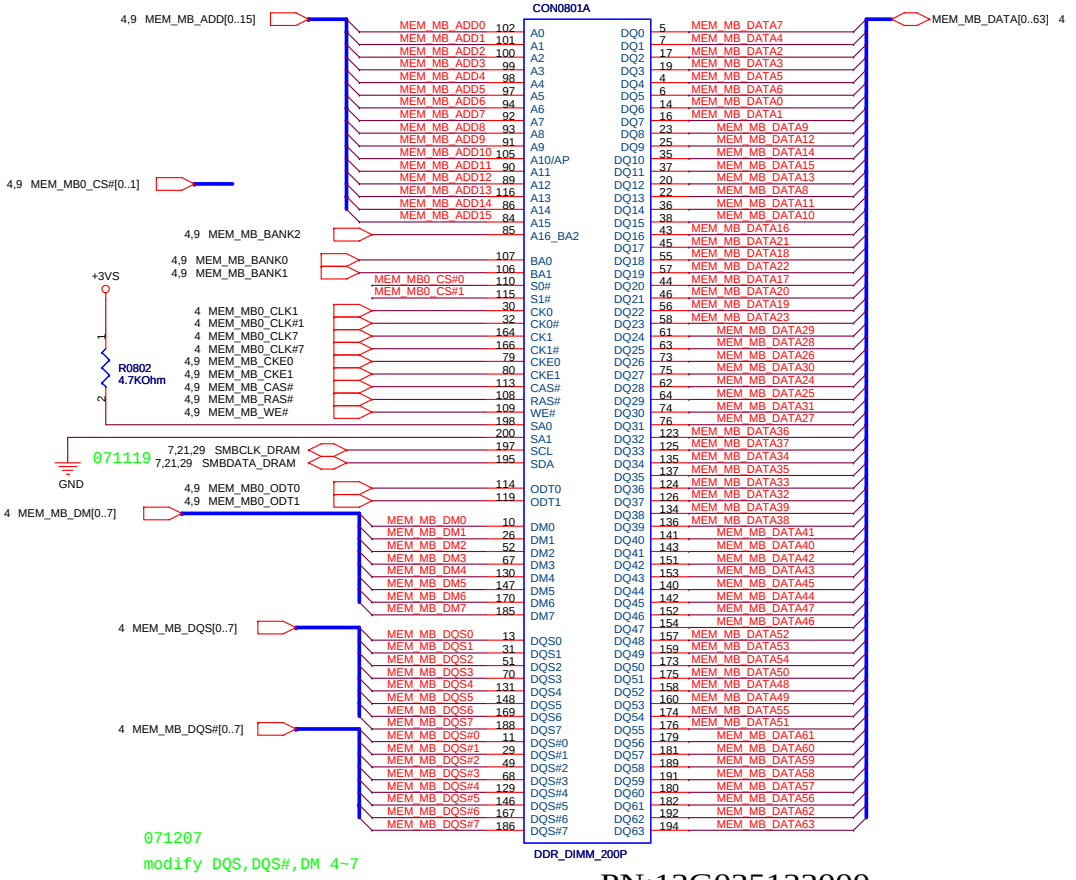
ASUSTeK COMPUTER INC

Engineer:

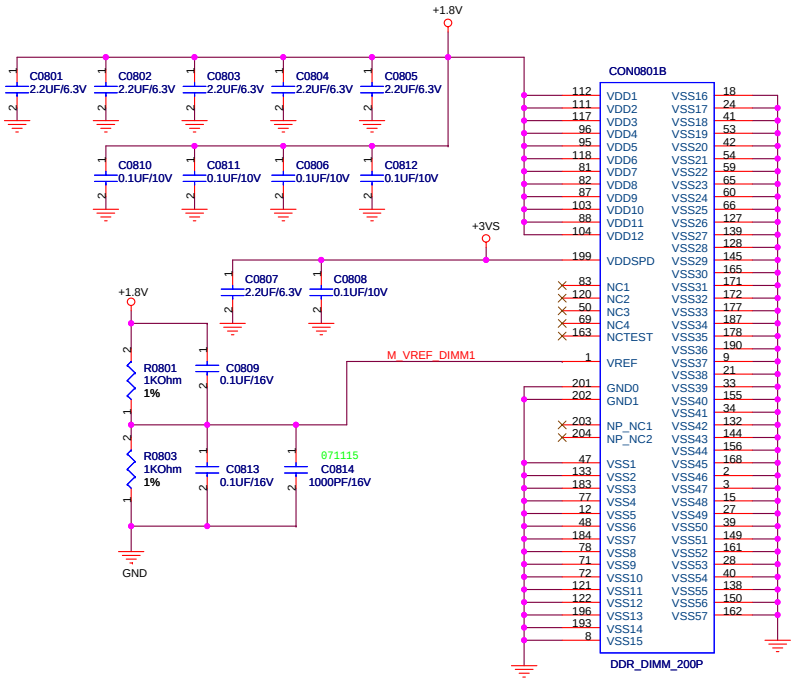
Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 7 of 94

080221
SWAP



PN:12G025122000



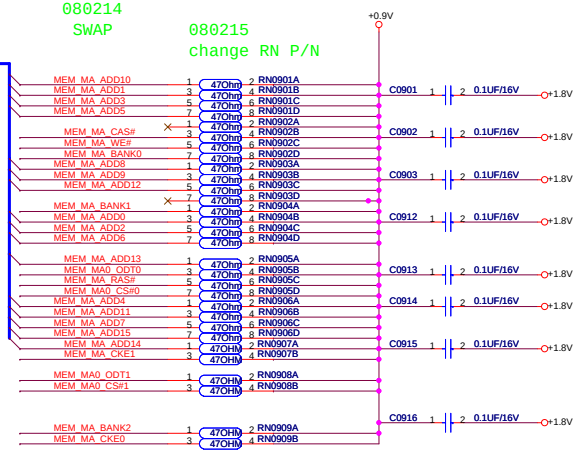
ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1		
	Engineer:		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 8 of 94		

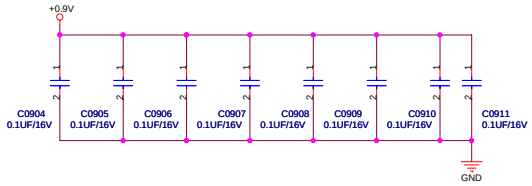
080214
SWAP

080215
change RN P/N

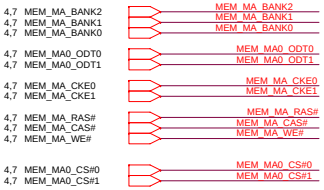
4,7 MEM_MA_ADD[0..15]

Del Bank2 to Bus





071207

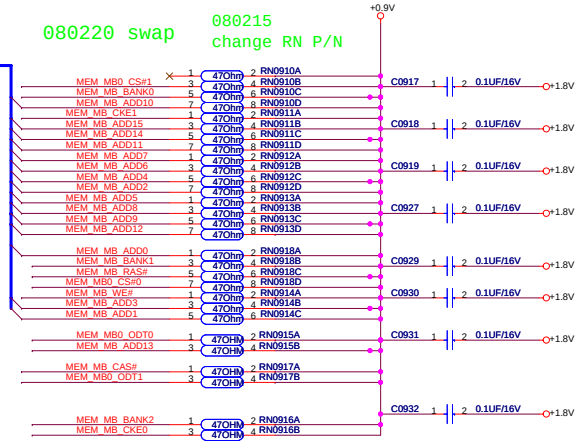


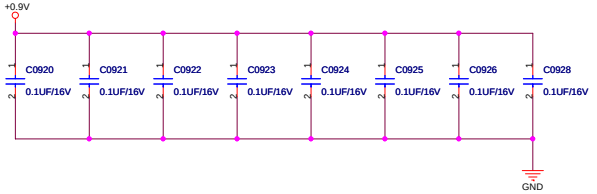
071121

080220 swap

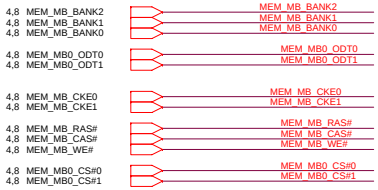
080215
change RN P/N

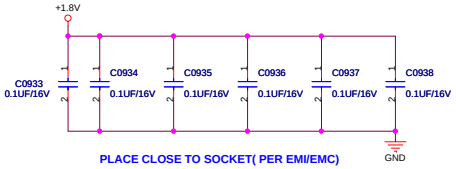
4,8 MEM_MB_ADD[0..15]





071211





PLACE CLOSE TO SOCKET(PER EMI/EMC)

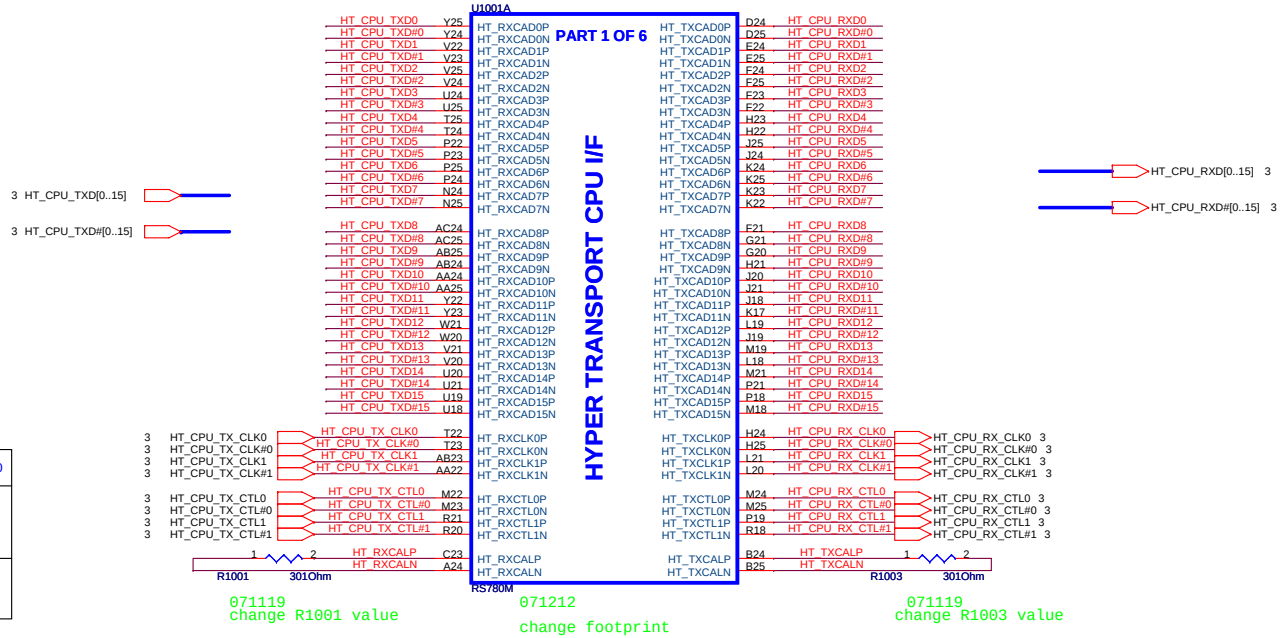
ASUSTeK COMPUTER INC

Title : DDR2_TERMINATIONS

Engineer:

Size	Project Name	Rev
Custom	P7Z	1.0

Date: Monday, May 19, 2008 Sheet 9 of 94



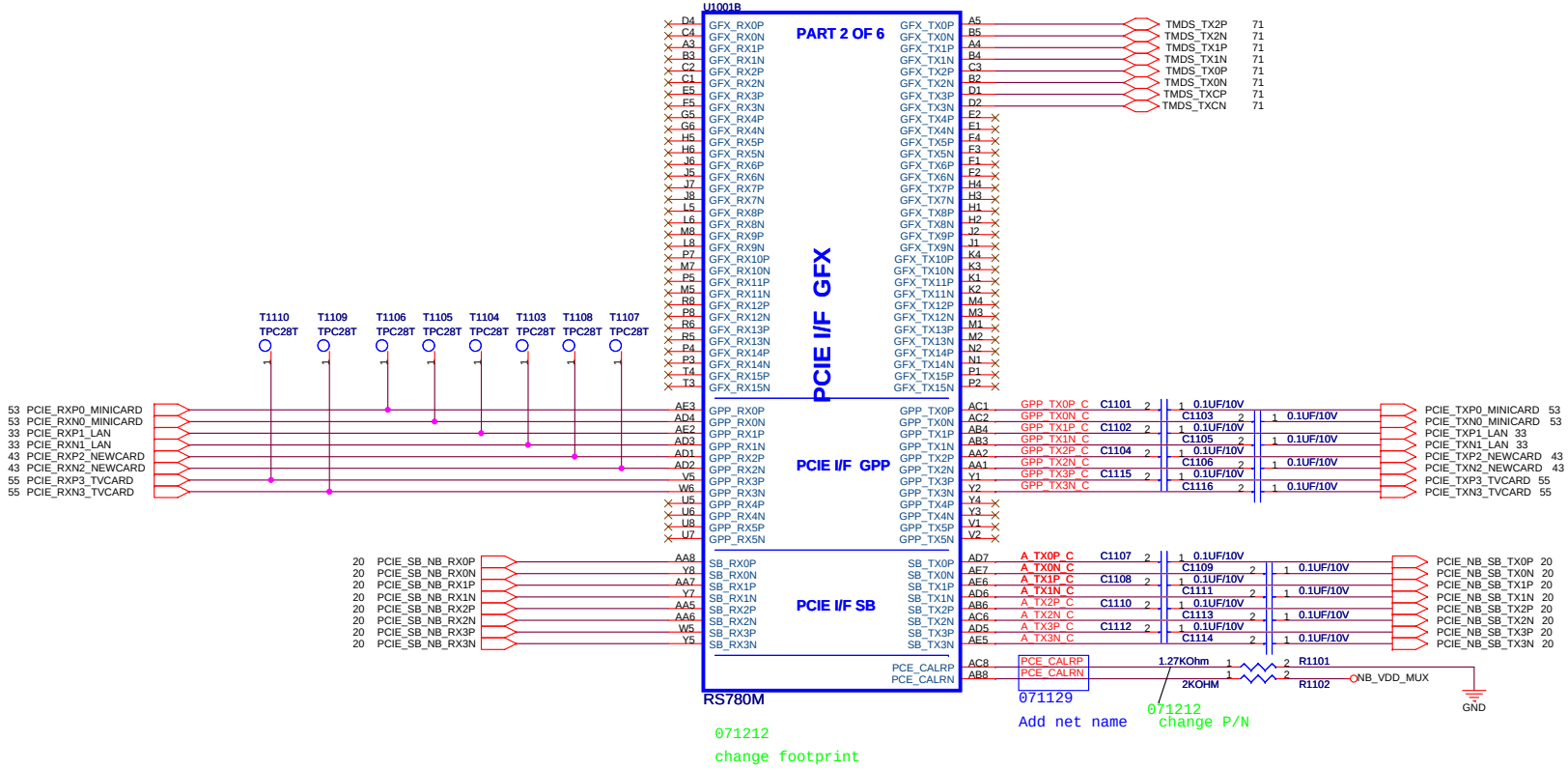
Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

071119
change R1001 value

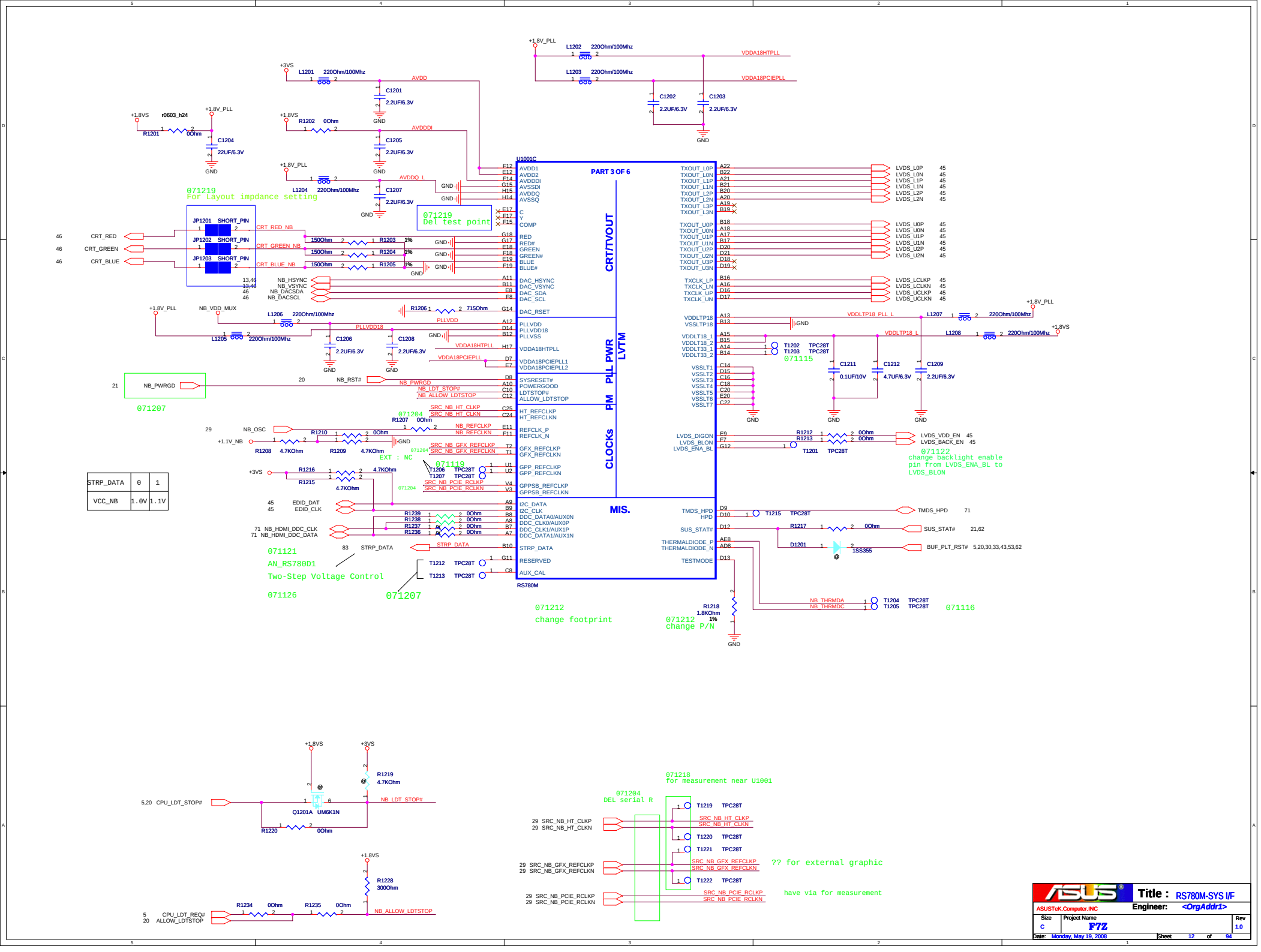
071212
change footprint

071119
change R1003 value

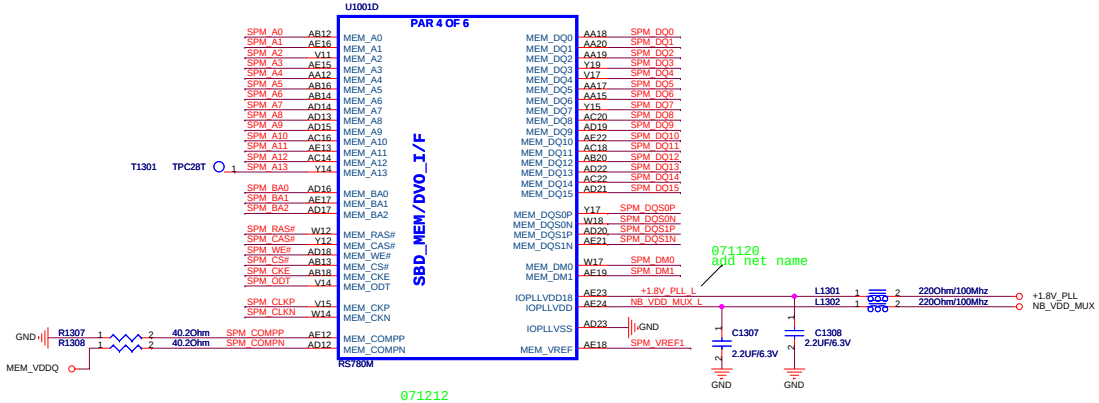
ASUSTeK.COMPUTER.INC	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 10 of 94	



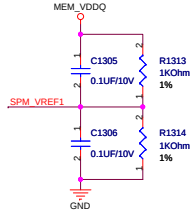
ASUSTeK.Computer.INC	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 11 of 94		

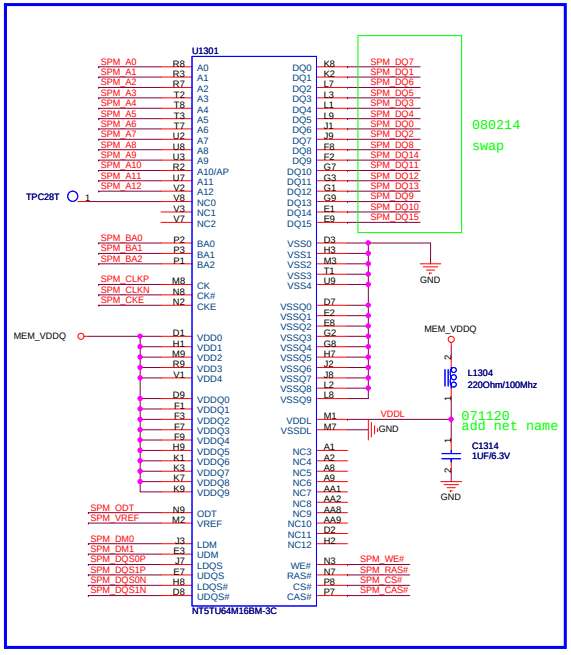

U1001C
PART 3 OF 6
RS780M
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.
071219
For Layout impdance setting
071219
Del test point
071207
071121
AN_RS780D1
Two-Step Voltage Control
071126
071212
change footprint
071212
change P/N
071204
EXT : NC
071118
071115
071122
change backlight enable pin from LVDS_ENA_BL to LVDS_BLON
071116
071218
for measurement near U1001
071204
DEL serial R
?? for external graphic
have via for measurement
STRP_DATA | 0 | 1
VCC_NB | 1.0V | 1.1V
Title : RS780M-SYS I/F
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 12 of 94

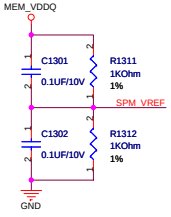
071113



071212
change footprint







071212 Change to Naya Pin 92

071218

AMD Qualified

16Mx16 Hynix HY5PS561621AFP-25 asus P/N: 03G15123621 4

32Mx16 Qimonda HYB18T512161B2F-25 asus P/N :03G15133F211

64Mx16 Samsung K4N16164QQ-HC25 asus P/N -

F5Z Use

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

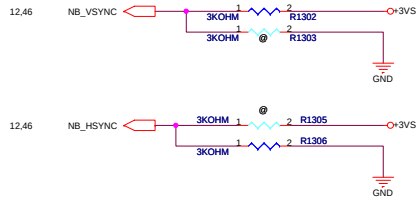
Enables the Test Debug Bus using PCIE bus:
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

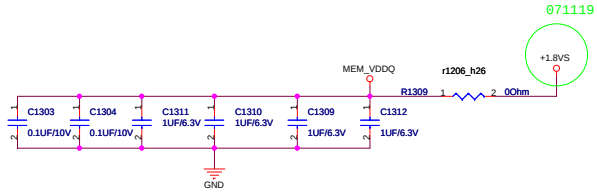
RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

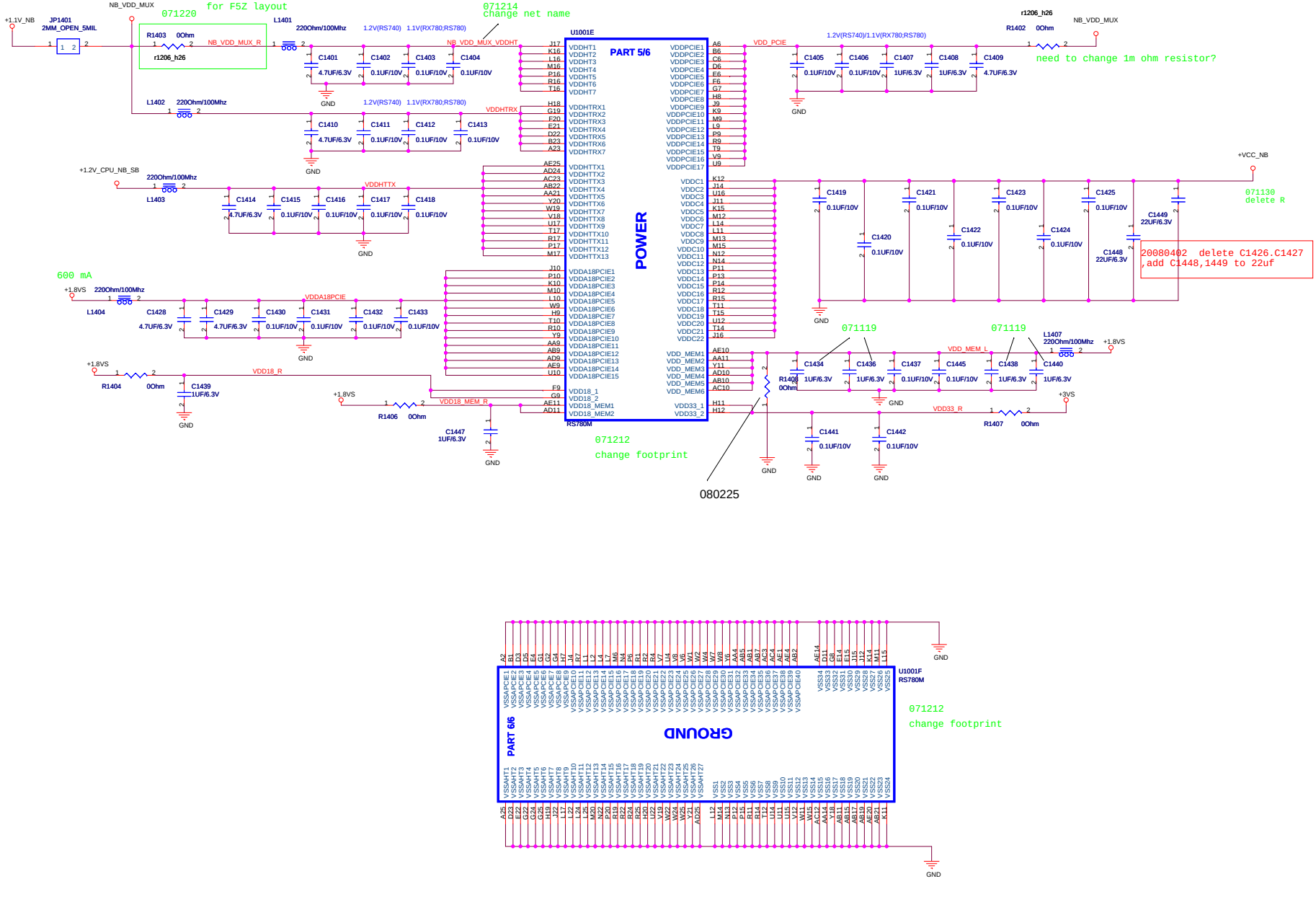
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

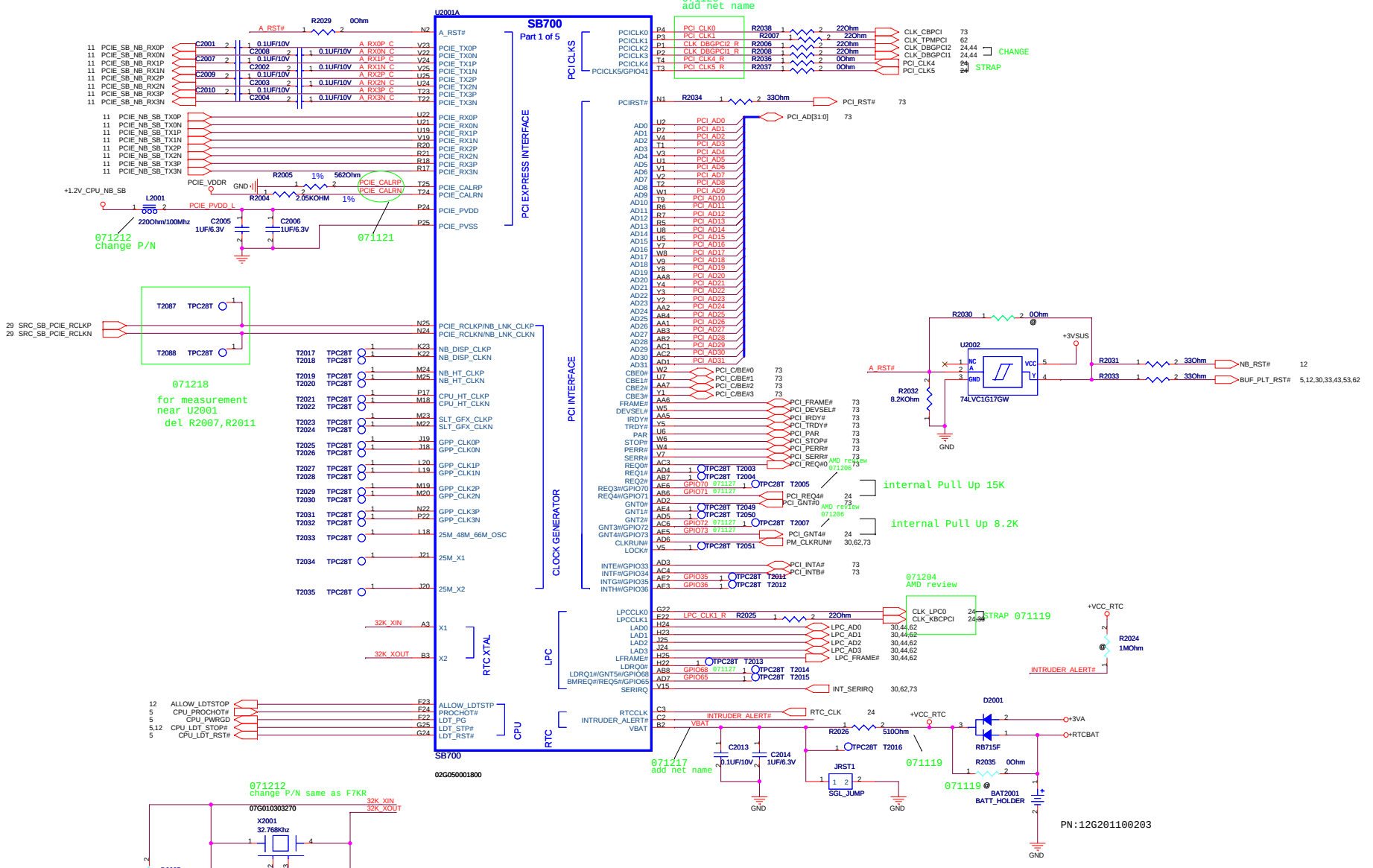


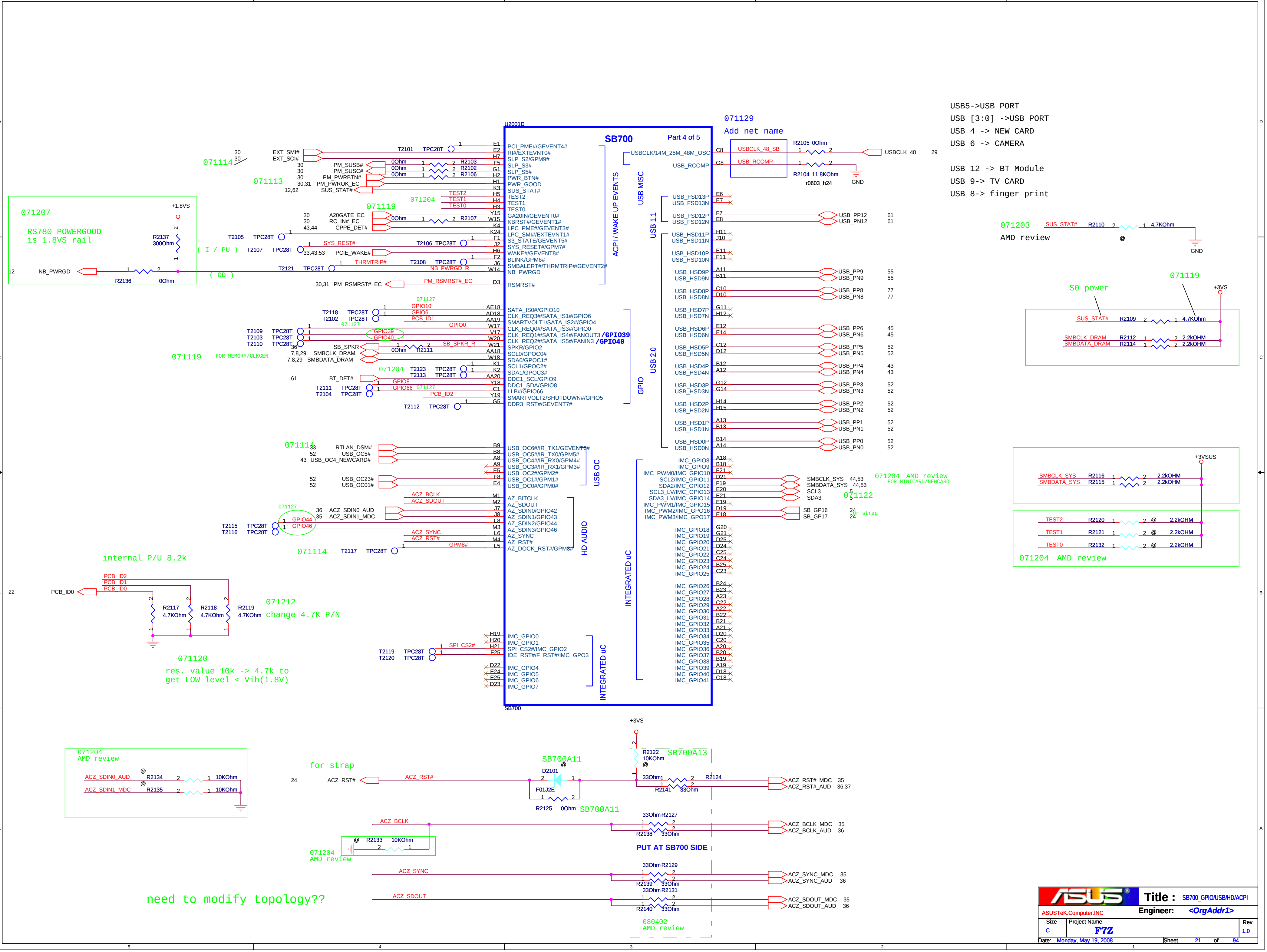


ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 13 of 94		

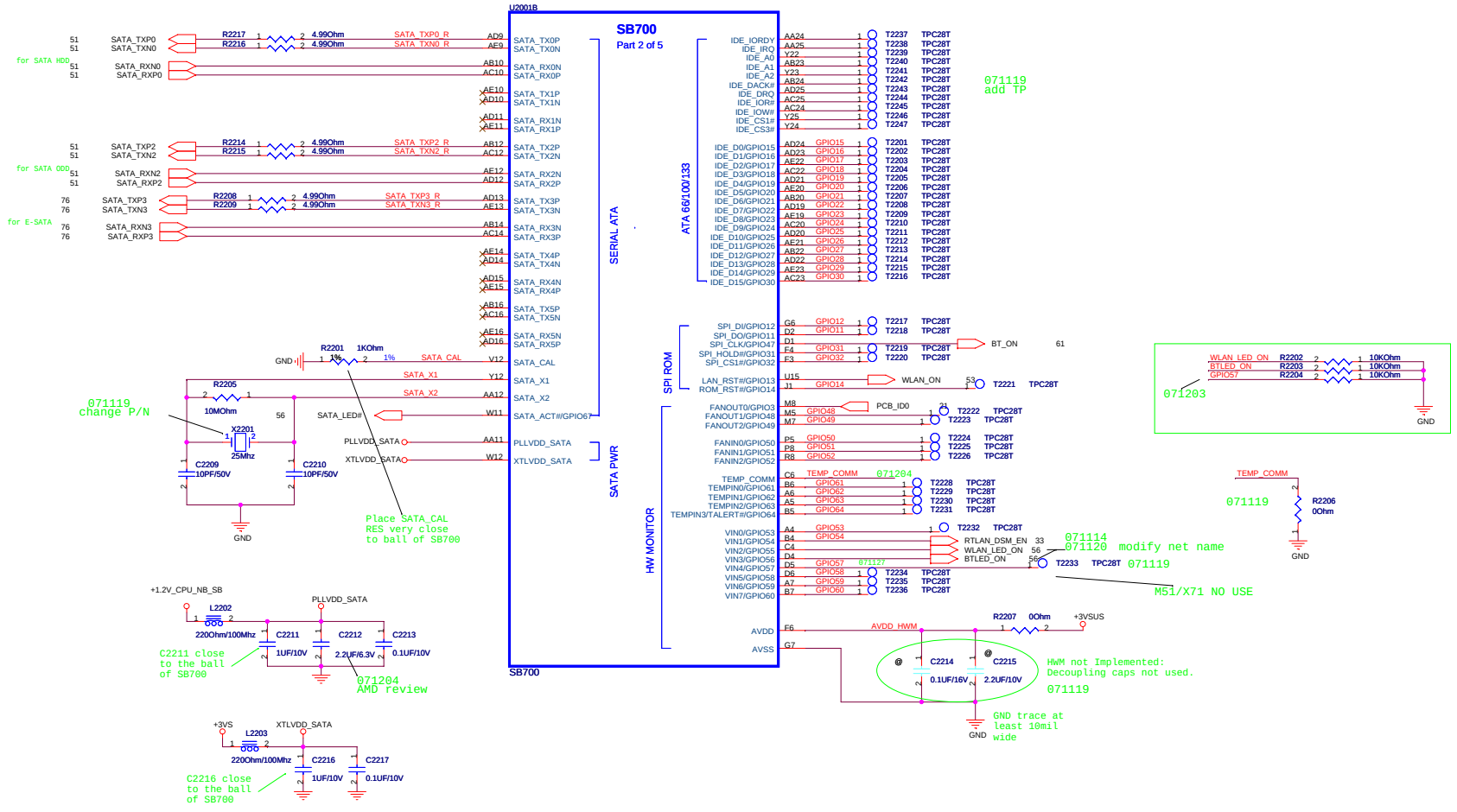


ASUSTeK.COMPUTER.INC	Title : RS780M-POWER		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 14 of 94		

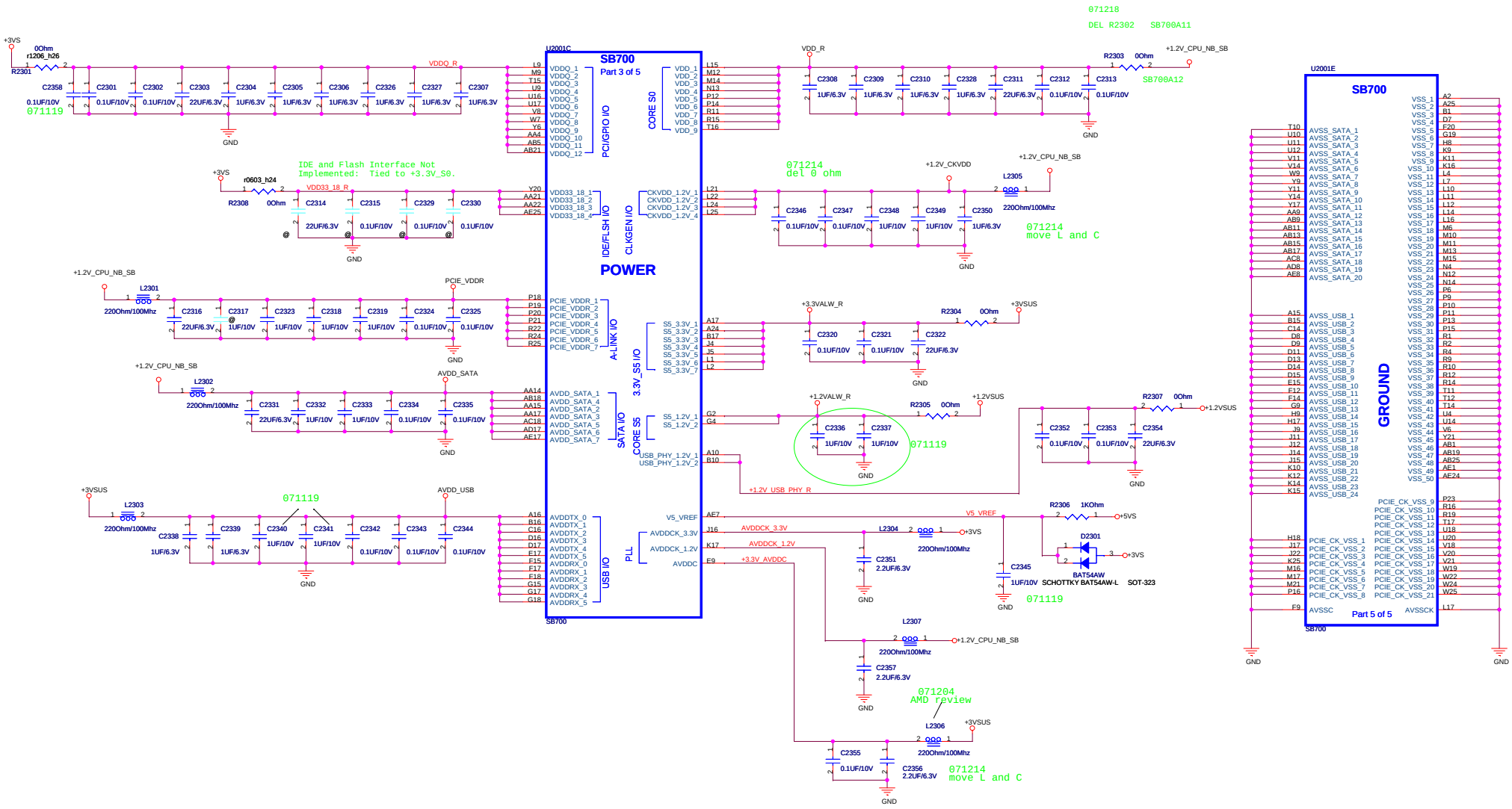

071120
add net name
SB700
Part 1 of 5
U2001A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
071212
change P/N
071121
071218
for measurement
near U2001
del R2007,R2011
internal Pull Up 15K
internal Pull Up 8.2K
071204
AMD review
STRAP 071119
071217
add net name
071119
071212
change P/N same as F7KR
07G010303270
X2001
32.768Khz
071119
follow check list DNI
PN:12G201100203
Title : SB700_CPU/PCIE/LPC/CLK
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 20 of 94



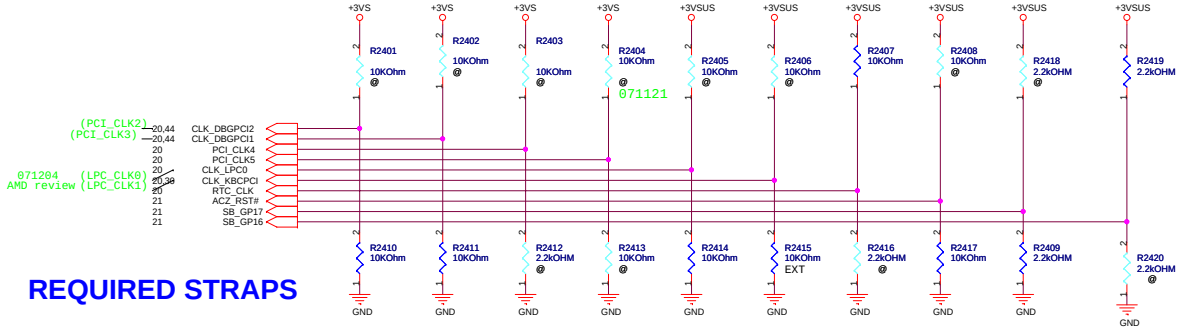
SB700
Part 4 of 5
U2001D
071129
Add net name
USB5->USB PORT
USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 6 -> CAMERA
USB 12 -> BT Module
USB 9-> TV CARD
USB 8-> finger print
071203
AMD review
071207
RS780 POWERGOOD
is 1.8VS rail
(I / PU)
(OD)
071114
071113
071119
071204
071127
FOR MEMORY/CLKGEN
S0 power
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
071204 AMD review
FOR MINICARD/NEWCARD
071122
for strap
internal P/U 8.2k
071212
change 4.7K P/N
071120
res. value 10k -> 4.7k to
get LOW level < Vih(1.8V)
SB700A11
SB700A13
PUT AT SB700 SIDE
080402
AMD review
need to modify topology??
ASUSTeK.Computer.INC
Title : SB700_GPIO/USB/HD/ACPI
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 21 of 94



ASUSTeK.COMPUTER.INC	Title : SB700_PATA/SATA		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 22 of 94		


071218
DEL R2302 SB700A11
SB700
Part 3 of 5
U2001C
POWER
PCI/GPIO I/O
CORE S0
IDE/FL-SH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
IDE and Flash Interface Not Implemented: Tied to +3.3V_S0.
071214 del 0 ohm
071214 move L and C
071119
071204 AMD review
SB700A12
GROUND
Part 5 of 5
U2001E
Title : SB700_POWER
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 23 of 94

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

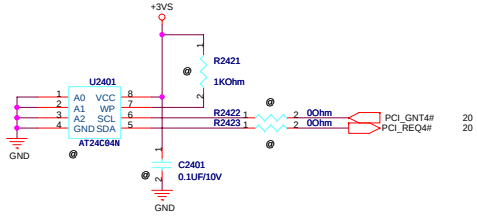


REQUIRED STRAPS

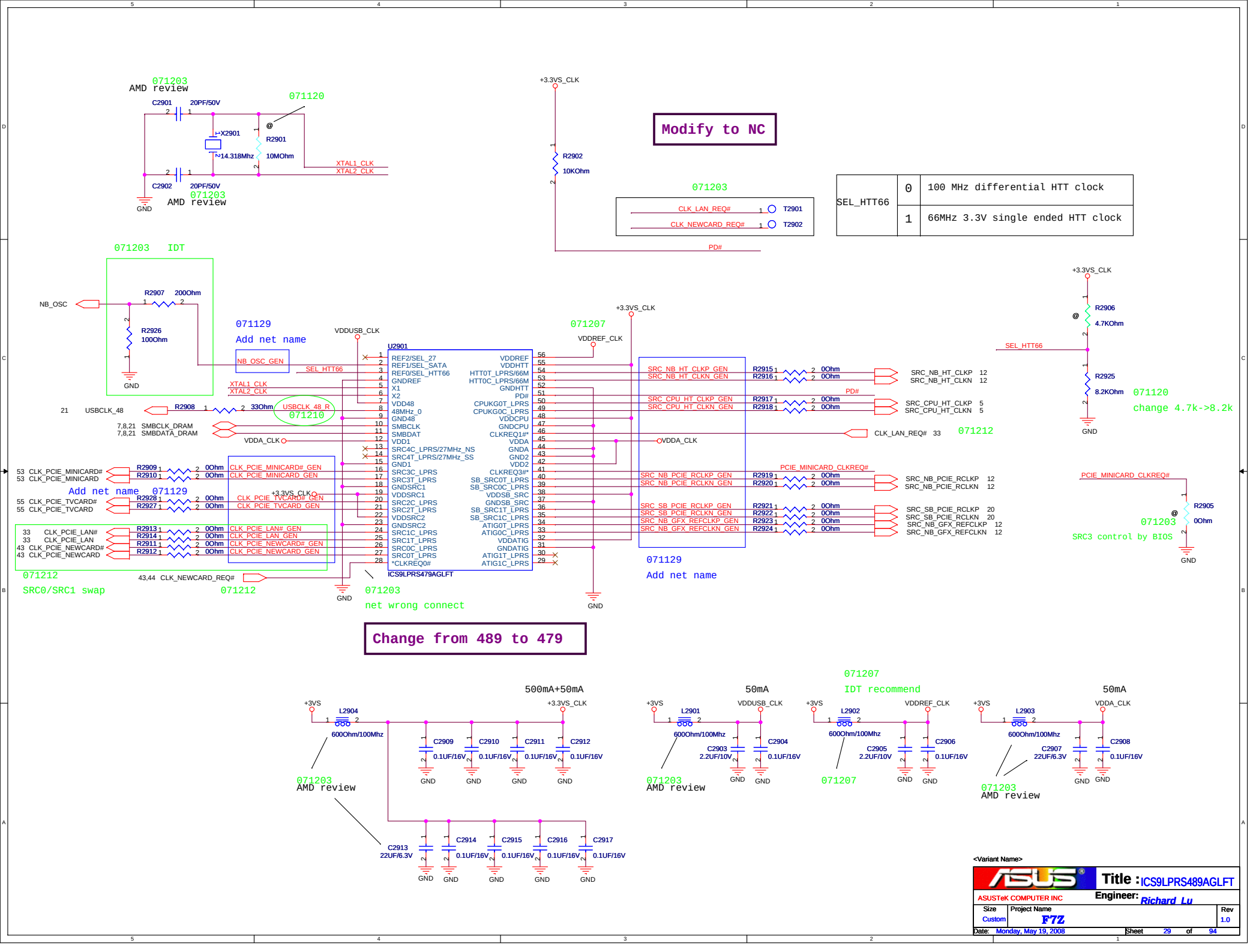
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

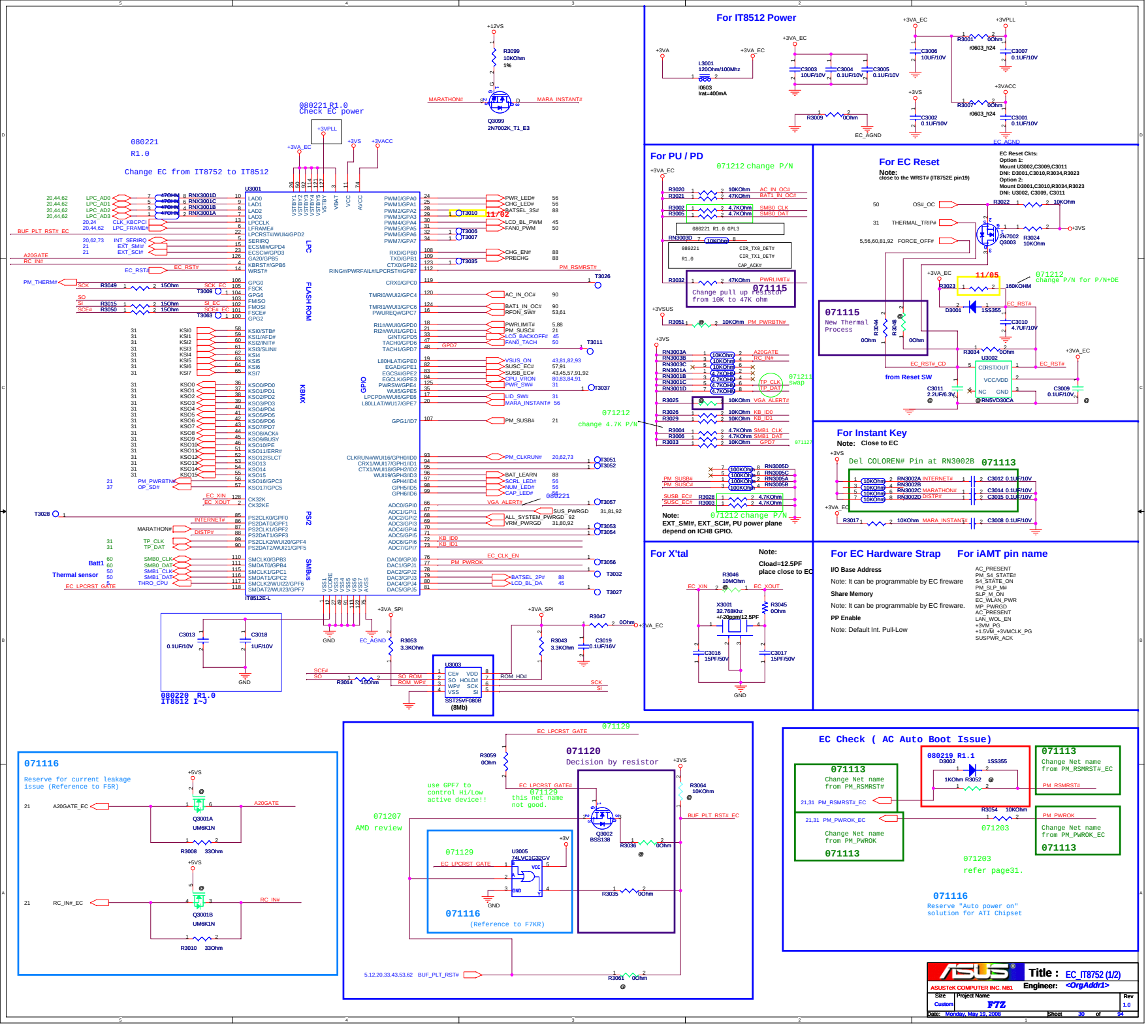
WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

071206
AMD review



ASUSTeK.Computer.INC	Title : SB700_STRAP	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 24 of 94	


071203
AMD review
C2901
20PF/50V
071120
X2901
14.318Mhz
R2901
10MOhm
@
XTAL1_CLK
XTAL2_CLK
C2902
20PF/50V
071203
AMD review
GND
+3.3VS_CLK
R2902
10KOhm
Modify to NC
071203
CLK_LAN_REQ#
CLK_NEWCARD_REQ#
T2901
T2902
PD#
SEL_HTT66
0
100 MHz differential HTT clock
1
66MHz 3.3V single ended HTT clock
071203 IDT
NB_OSC
R2907 200Ohm
R2926 100Ohm
071129
Add net name
NB_OSC_GEN
VDDUSB_CLK
U2901
REF2/SEL_27
REF1/SEL_SATA
REF0/SEL_HTT66
GNDREF
X1
X2
VDD48
48MHz_0
GND48
SMBCLK
SMBDAT
VDD1
SRC4C_LPRS/27MHz_NS
SRC4T_LPRS/27MHz_SS
GND1
SRC3C_LPRS
SRC3T_LPRS
GNDSRC1
VDDSRC1
SRC2C_LPRS
SRC2T_LPRS
VDDSRC2
GNDSRC2
SRC1C_LPRS
SRC1T_LPRS
SRC0C_LPRS
SRC0T_LPRS
*CLKREQ0#
VDDREF
VDDHTT
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDHTT
PD#
CPUKG0T_LPRS
CPUKG0C_LPRS
VDDCPU
GNDCPU
CLKREQ1#*
VDDA
GNDA
GND2
VDD2
CLKREQ3#*
SB_SRC0T_LPRS
SB_SRC0C_LPRS
VDDSB_SRC
GNDSB_SRC
SB_SRC1T_LPRS
SB_SRC1C_LPRS
ATIG0T_LPRS
ATIG0C_LPRS
VDDATIG
GNDATIG
ATIG1T_LPRS
ATIG1C_LPRS
ICS9LPRS479AGLFT
071207
VDDREF_CLK
+3.3VS_CLK
XTAL1_CLK
XTAL2_CLK
21 USBCLK_48
R2908 33Ohm
USBCLK_48_R
071210
7,8,21 SMBCLK_DRAM
7,8,21 SMBDATA_DRAM
VDDA_CLK
53 CLK_PCIE_MINICARD#
53 CLK_PCIE_MINICARD
R2909 0Ohm CLK_PCIE_MINICARD#_GEN
R2910 0Ohm CLK_PCIE_MINICARD_GEN
Add net name 071129
55 CLK_PCIE_TVCARD#
55 CLK_PCIE_TVCARD
R2928 0Ohm CLK_PCIE_TVCARD#_GEN
R2927 0Ohm CLK_PCIE_TVCARD_GEN
33 CLK_PCIE_LAN#
33 CLK_PCIE_LAN
43 CLK_PCIE_NEWCARD#
43 CLK_PCIE_NEWCARD
R2913 0Ohm CLK_PCIE_LAN#_GEN
R2914 0Ohm CLK_PCIE_LAN_GEN
R2911 0Ohm CLK_PCIE_NEWCARD#_GEN
R2912 0Ohm CLK_PCIE_NEWCARD_GEN
071212
SRC0/SRC1 swap
43,44 CLK_NEWCARD_REQ#
071212
071203
net wrong connect
SRC_NB_HT_CLKP_GEN
SRC_NB_HT_CLKN_GEN
R2915 0Ohm
R2916 0Ohm
SRC_NB_HT_CLKP 12
SRC_NB_HT_CLKN 12
SRC_CPU_HT_CLKP_GEN
SRC_CPU_HT_CLKN_GEN
R2917 0Ohm
R2918 0Ohm
SRC_CPU_HT_CLKP 5
SRC_CPU_HT_CLKN 5
CLK_LAN_REQ# 33
071212
PCIE_MINICARD_CLKREQ#
SRC_NB_PCIE_RCLKP_GEN
SRC_NB_PCIE_RCLKN_GEN
R2919 0Ohm
R2920 0Ohm
SRC_NB_PCIE_RCLKP 12
SRC_NB_PCIE_RCLKN 12
SRC_SB_PCIE_RCLKP_GEN
SRC_SB_PCIE_RCLKN_GEN
SRC_NB_GFX_REFCLKP_GEN
SRC_NB_GFX_REFCLKN_GEN
R2921 0Ohm
R2922 0Ohm
R2923 0Ohm
R2924 0Ohm
SRC_SB_PCIE_RCLKP 20
SRC_SB_PCIE_RCLKN 20
SRC_NB_GFX_REFCLKP 12
SRC_NB_GFX_REFCLKN 12
071129
Add net name
+3.3VS_CLK
R2906
@
4.7KOhm
SEL_HTT66
R2925
8.2KOhm
071120
change 4.7k->8.2k
PCIE_MINICARD_CLKREQ#
R2905
@
0Ohm
071203
SRC3 control by BIOS
Change from 489 to 479
500mA+50mA
+3VS
+3.3VS_CLK
L2904
600Ohm/100Mhz
C2909
C2910
C2911
C2912
0.1UF/16V
071203
AMD review
C2913
22UF/6.3V
C2914
C2915
C2916
C2917
50mA
VDDUSB_CLK
L2901
C2903
2.2UF/10V
C2904
071203
AMD review
071207
IDT recommend
VDDREF_CLK
L2902
C2905
2.2UF/10V
C2906
071207
50mA
VDDA_CLK
L2903
C2907
22UF/6.3V
C2908
071203
AMD review
GND
<Variant Name>
ASUSTeK COMPUTER INC
Title : ICS9LPRS489AGLFT
Engineer: Richard_Lu
Size Custom
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 29 of 94

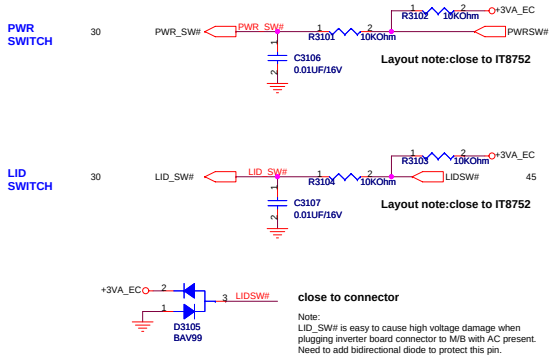

080221 R1.0
Check EC power
080221
R1.0
Change EC from IT8752 to IT8512
U3001
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
IT8512E-L
080220 R1.0
IT8512 1~J
For IT8512 Power
For PU / PD
071212 change P/N
For EC Reset
EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011
Note:
close to the WRST# (IT8752E pin19)
071115
Change pull up resistor from 10K to 47K ohm
071115
New Thermal Process
from Reset SW
For Instant Key
Note: Close to EC
Del COLOREN# Pin at RN3002B 071113
For X'tal
Note:
Cload=12.5PF
place close to EC
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.
For EC Hardware Strap
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
For iAMT pin name
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
071116
Reserve for current leakage issue (Reference to FSR)
Q3001A
UM6K1N
Q3001B
UM6K1N
071129
071120
Decision by resistor
use GPF7 to control Hi/low active device!!
071129 this net name not good.
071207
AMD review
071129
(Reference to F7KR)
EC Check (AC Auto Boot Issue)
080219 R1.1
071113
Change Net name from PM_RSMRST#
Change Net name from PM_PWROK
Change Net name from PM_RSMRST#_EC
Change Net name from PM_PWROK_EC
071203
refer page31.
071116
Reserve "Auto power on" solution for ATI Chipset
Title : EC_IT8752 (1/2)
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Size: Custom
Project Name: F7Z
Rev: 1.0
Date: Monday, May 19, 2008
Sheet 30 of 94

For Battery

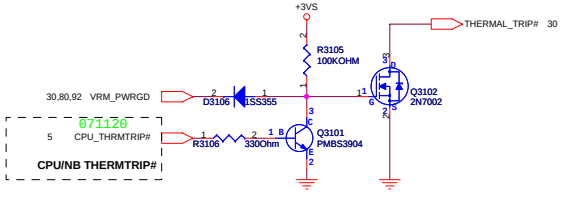
Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

In Page 60

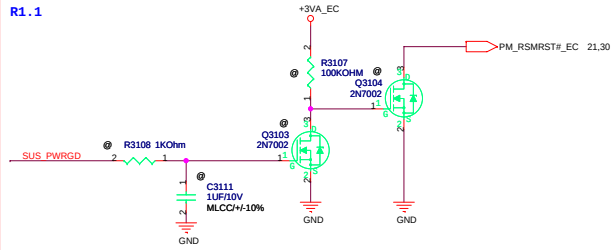
For Switch



For Thermal Control Method



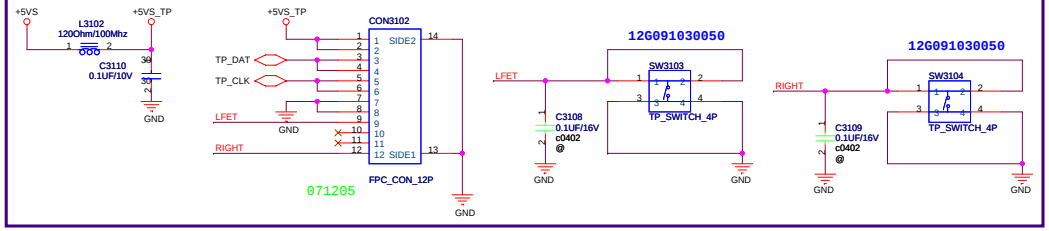
R1.1



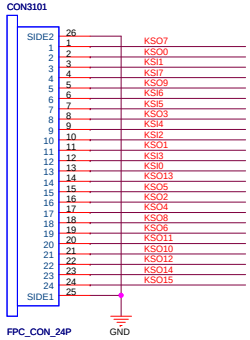
080219 Q3103 & Q3104 pin2 and pin3 Reverse

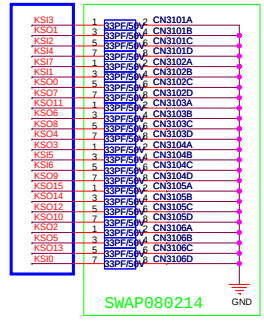
080219 Reserve for SB700 interface

Touch-Pad (F7se)



Keyboard Connector (F7se)





ASUSTeK COMPUTER INC. NB1	Title : EC_IT8511 (2/2)		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 31 of 94		

ALL Follow Design IP

071119 Add net name

close to IC 200 mil

071113

Add net name

close to pin1 with in 200 mil
please change:09G02X473522 4.7uH/20%
close to L3301 with in 200 mil

60 mil

071212
change P/N

071130
Add L3304

071130
Add R3318

40mil

40 mil

071212
change P/N

40mil

CONNECT TO 3.3V ENABLE
;0V TO DISABLE SWIRTCHING REGULATOR

close to pin63 within 200 mil

close to pin64

Add DSM function

Reserved DSM Function

Change to 2N7002

071120 Reserved

Pin.33 is Clkreq# pin similar to Clkrun function in the PCI interface. If this function not implemented, make this pin floating or connect to the ground.

071121 close to LAN CHIP

071129
Correct net name

To Transformer

To SB

From SB

From Clock Gen.

From SB

071217 Base on Design IP

25MHz Crystal

<Variant Name>

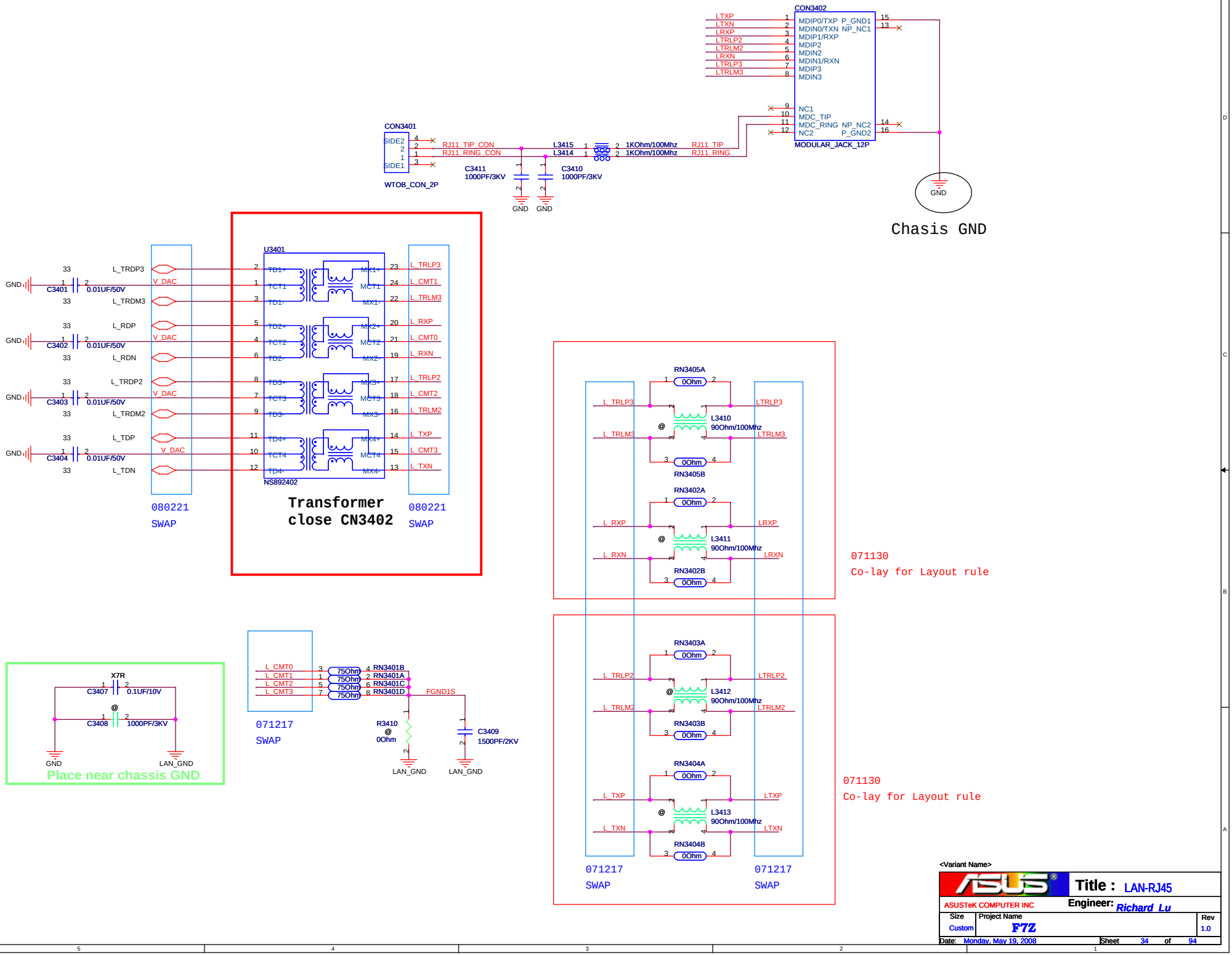
Title : LAN-RTL8111C

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

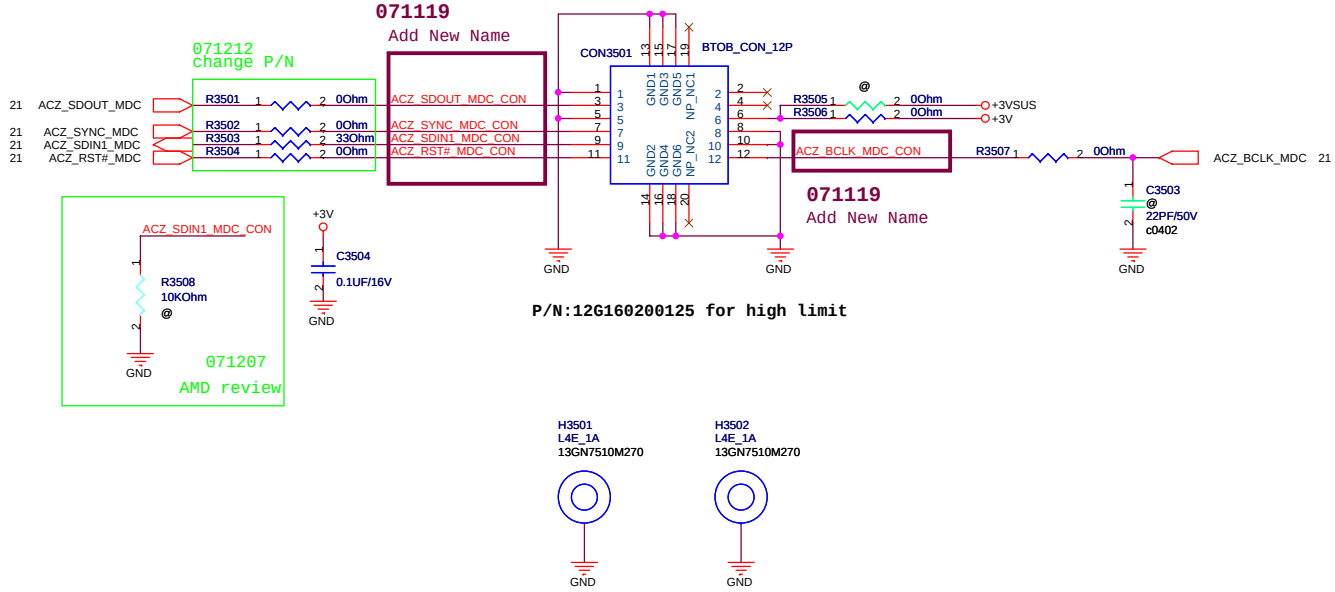
Date: Monday, May 19, 2008 Sheet 33 of 94



<variant_name>

ASUSTeK COMPUTER INC	Title : LAN-RJ45	
	Engineer: Richard Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 34 of 94	

MDC



<Variant Name>

Title : LAN-MDC

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 35 of 94

AUDIO POWER

ALC663		
	Mount	R3614,R3674,R3675,RX3612,RX3613,R3618,R3613,R3612,C3629,C3608
	NO Mount	R3672,R3673,R3631,R3632,R3608

CODEC:ALC662 / ALC663

Digital

Mount R3614 For ALC663 ;
Mount R3617 For ALC662

Need to Check

FROM ICH

Mout For ALC663

For ALC663
Need to Check

Mout C3629 For ALC663

Reserved For ALC663;
NC For ALC662

Mout R3674 and R3676 For ALC663 ;
Mount R3673 and R3672 For ALC662;

07116

Unuse in F5Z

Unuse in F5Z

Cap-less with pop-noise, RX3612, R3X613 mount 0 Ohm, mount R3777,R3778 no mount CE3751,CE3752,R3758,R3759, R3756, R3757

Isolate the voltage level

071207
AMD review

080519

Vout=1.25*(1+(100K/34.8K))=4.84V
Vdrop about 150mV@100mA
2nd source:GMT G923 470T1UF SOT23-5
(P/N:06G007342012)

FOR NORMAL FUNCTION .

Mount RX3613 and RX3612 For ALC663;
Mount R3632 and R3631 For ALC632;

TO HP

TO INTERNAL MIC

TO EXTERNAL MIC

TO SPK AMP

THE VALUE DEPEND ON C3635/C3636 TO MEET THE RECOMMENDATION VALUE(0.47UF).

07116

Del Audio DJ Function

DETECTION

EXT MIC DETECT.

Mount R3618 For ALC663 ;
Mount R3608 For ALC662;

FOR HP DETECT.

For ALC663 Cap-less detect pin

PC BEEP

Reserve for Cardbus controllor that has PCMCIA function.

IF NO PCMCIA,DNI IT.

FROM ICH

For EMI

<Variant Name>

ASUSTeK COMPUTER INC

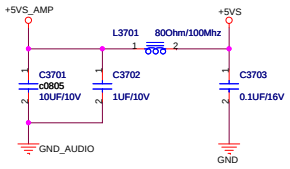
Title : CODEC-ALC662

Engineer: Richard Lu

Size	Project Name	Rev
C	F7Z	1.0

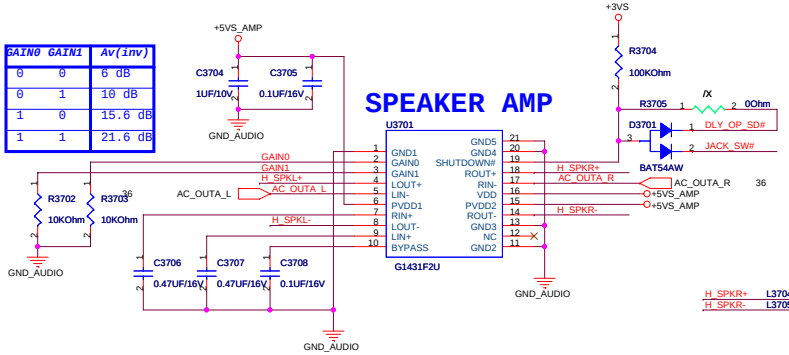
Date: Monday, May 19, 2008 Sheet 36 of 94

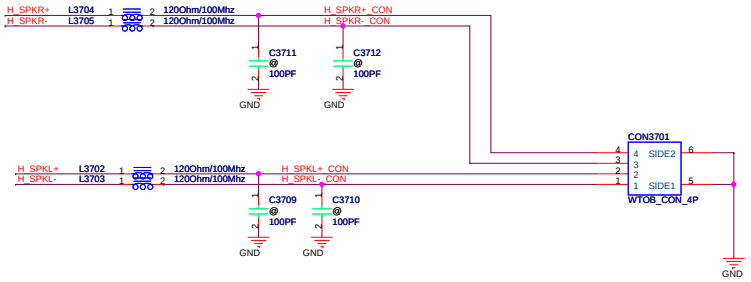
AMP POWER



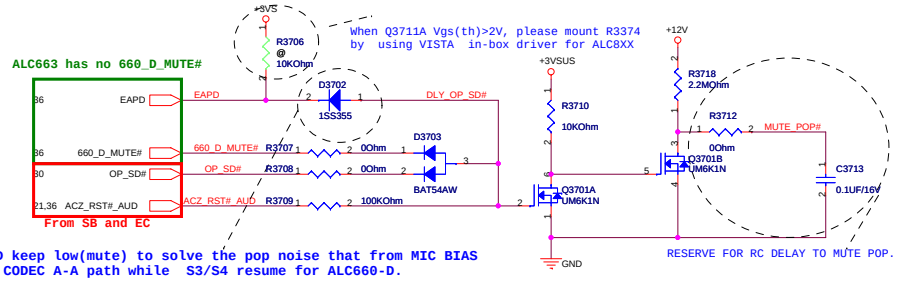
SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



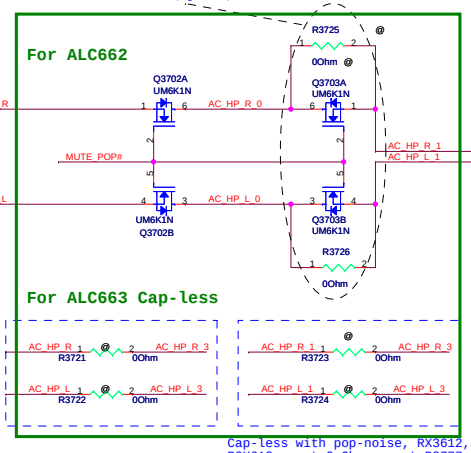


MUTE CONTROL



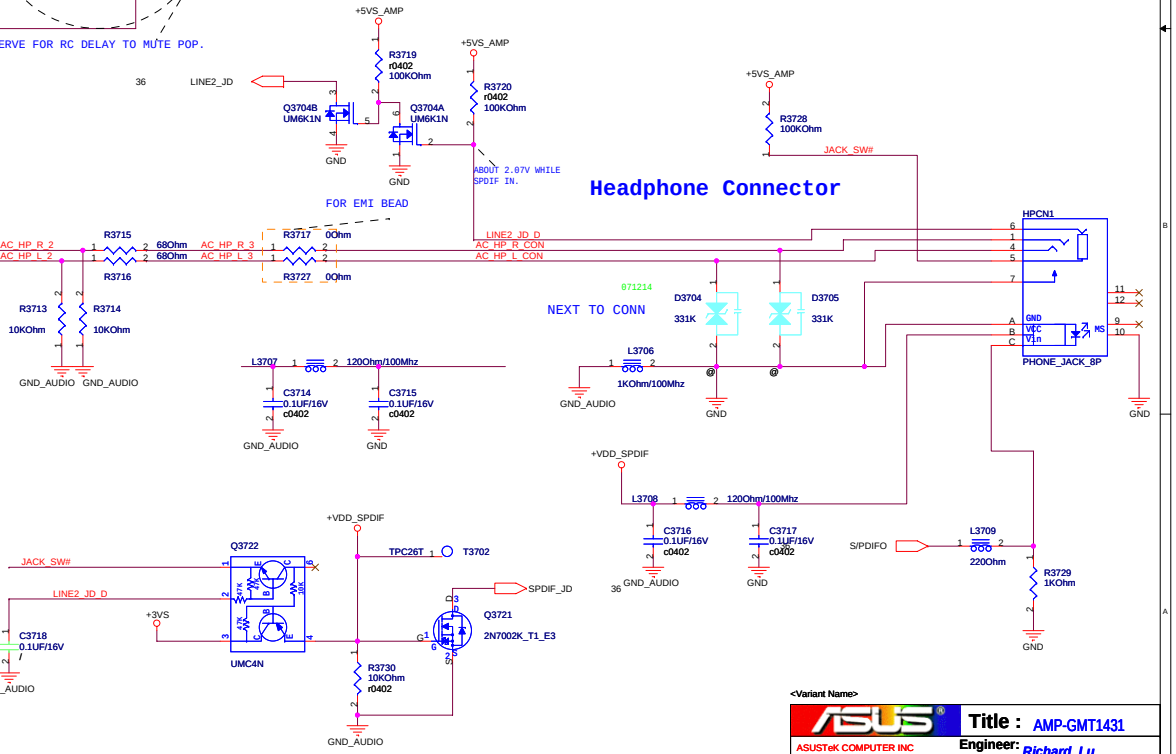
TYPE	LINE_OUT	S/PDIF_OUT	NC
LINE2_JD_D	L	H	H
JACK_SW#	L	L	H

EAPD keep low(mute) to solve the pop noise that from MIC BIAS via CODEC A-A path while S3/S4 resume for ALC660-D.
Base on pop noise by each model.if your model do not care the A-A path pop-nose, you can not mount D3711,Q3755,but mount R3764 and R3765



For ALC663 Cap-less,mount R3775,R3776,RX3612,RX3613

Cap-less with pop-noise, RX3612, R3X613 mount O Ohm, mount R3777,R3778. no mount CE3751,CE3752,R3758,R3759, R3756, R3757



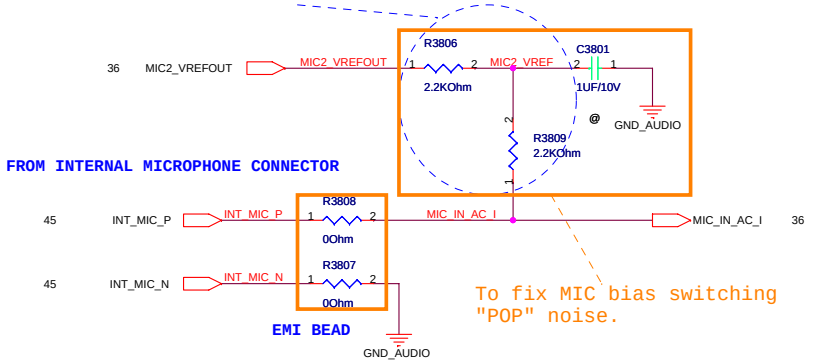
<Variant Name>

ASUSTeK COMPUTER INC	Title : AMP-GMT1431	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 37 of 94	

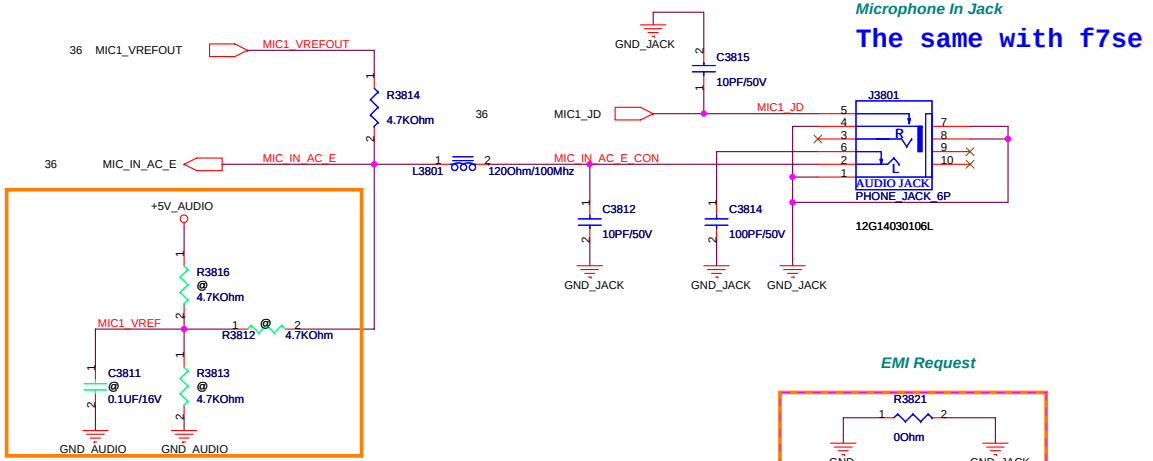
071116 Change form F5R to Design IP

INTERNAL MICROPHONE

If EAPD available(fix MIC bias switching "POP" noise):
Replace R3801,R3802 by one 4.7K ohm resistor.
DNI C3801.



EXTERNAL MICROPHONE

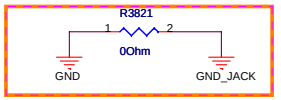


Microphone In Jack

The same with f7se

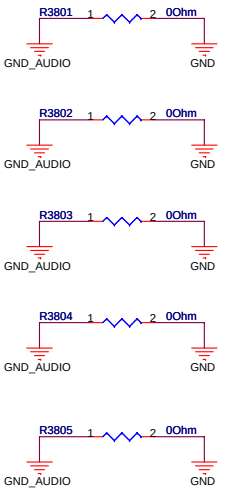
Reserved the external MIC bias(T filter).

EMI Request



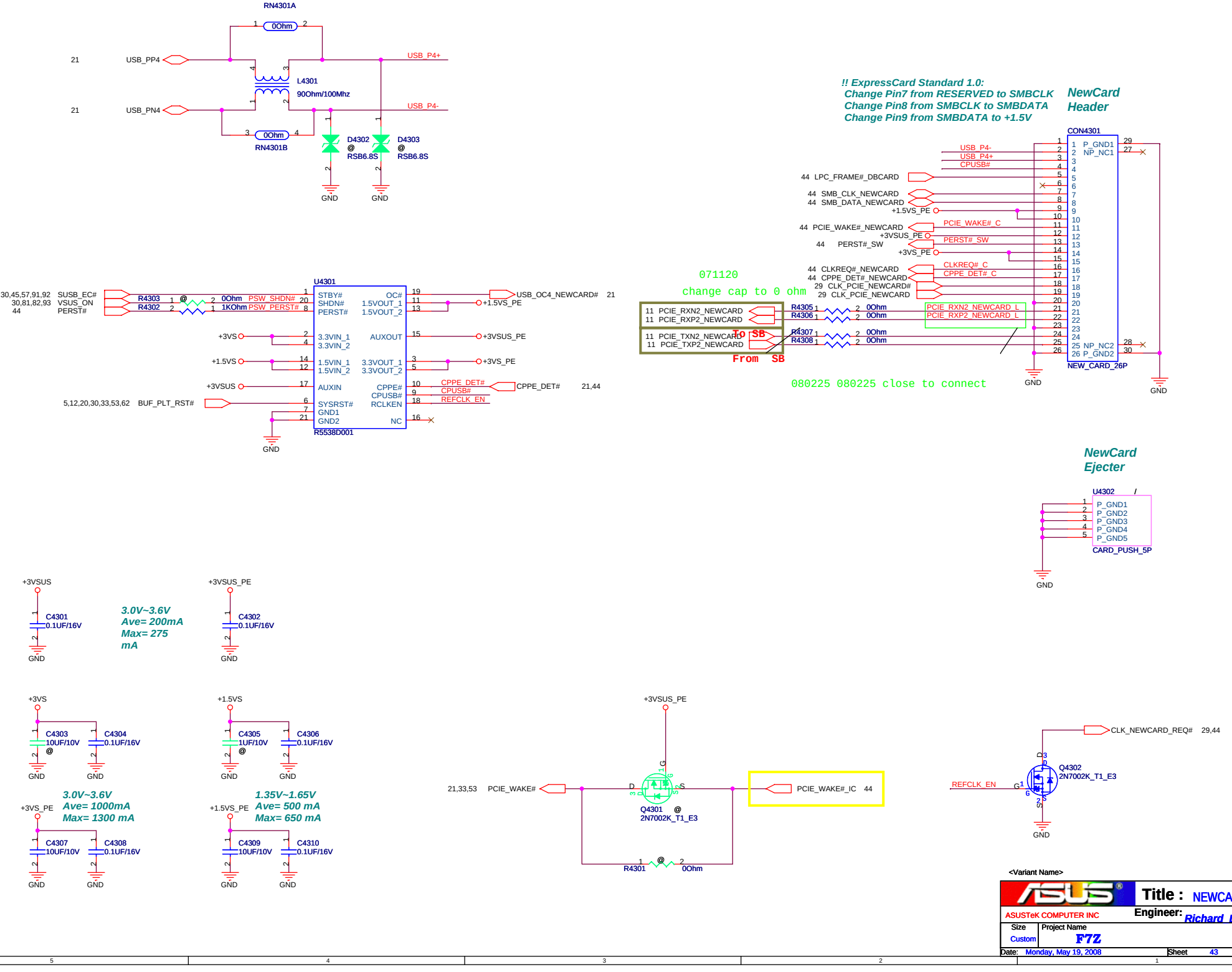
F7Z

071212
change 0 ohm P/N



<Variant Name>

ASUSTeK COMPUTER INC	Title : MIC-IN Jack	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 38 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

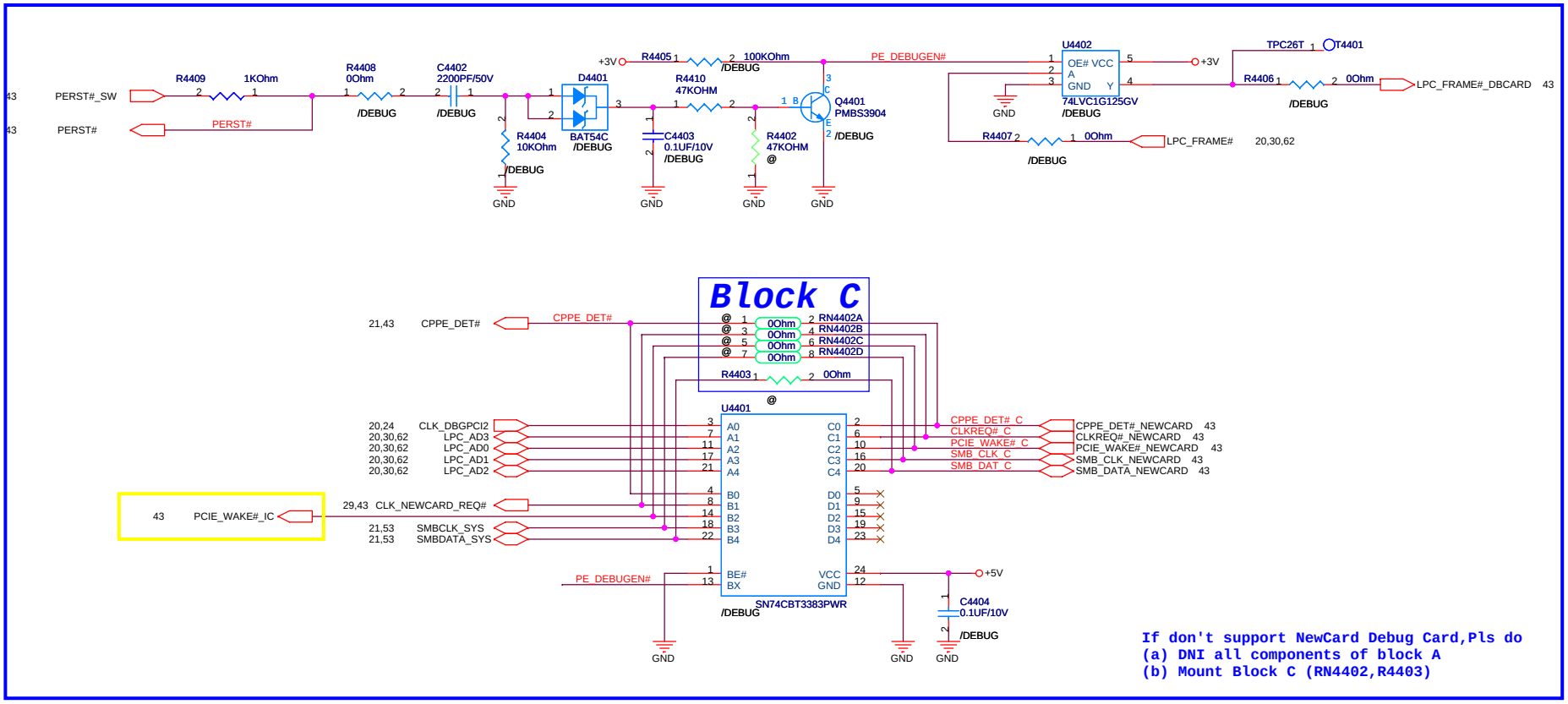
Title : NEWCARD

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

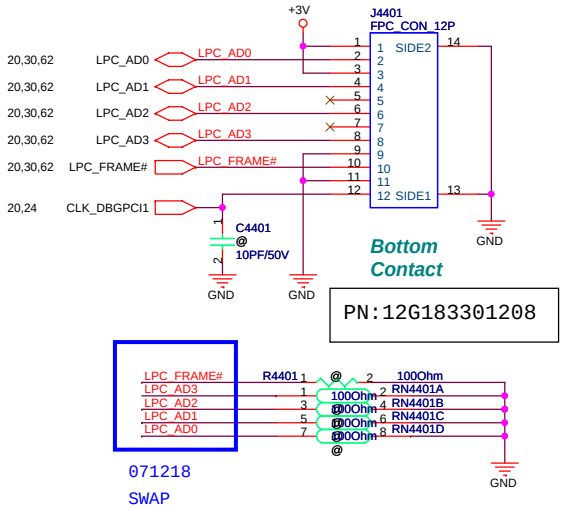
Date: Monday, May 19, 2008 Sheet 43 of 94

Block A



For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.

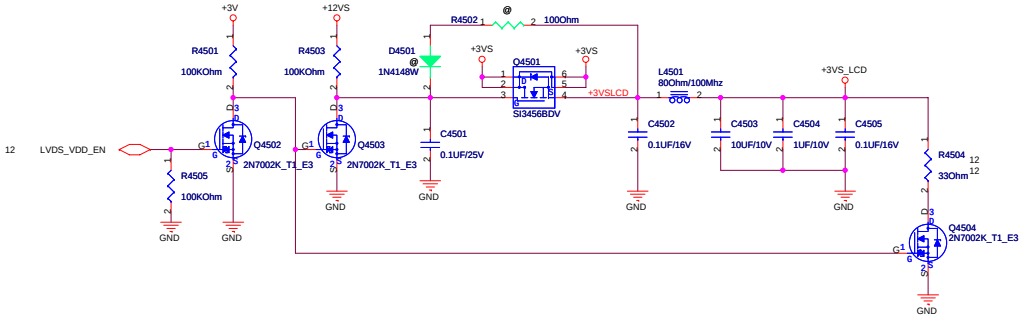


<Variant Name>

ASUSTeK COMPUTER INC	Title : DEBUG	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 44 of 94	

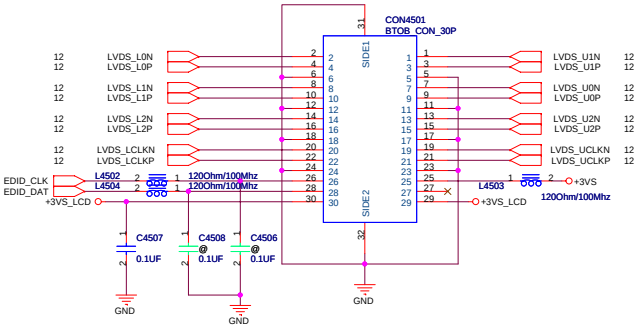
LCD Backlight Control

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

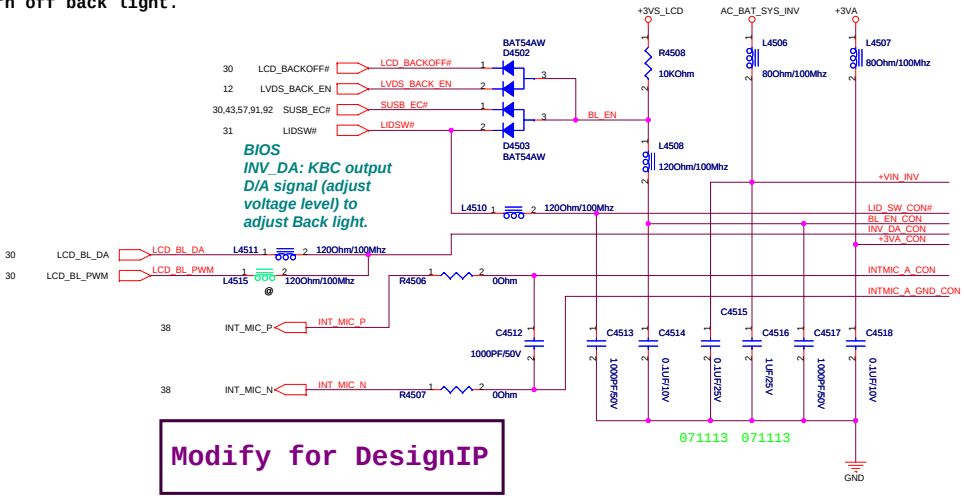
LCD LVDS Interface



INVERTER Interface

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

connect to JP8805
071203



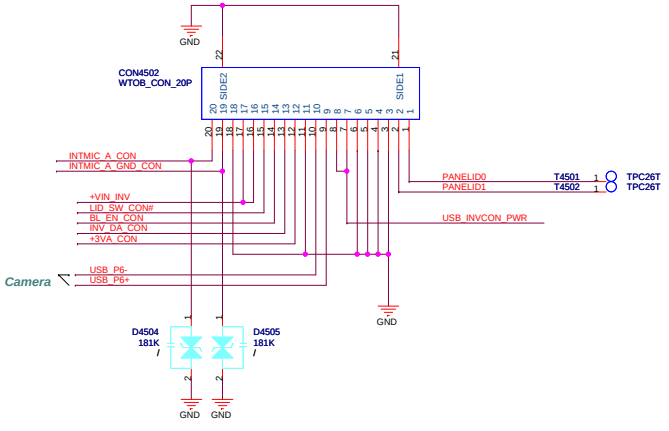
BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

071113 071113

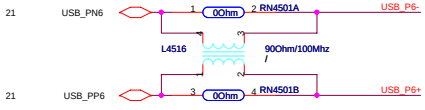
Modify for DesignIP

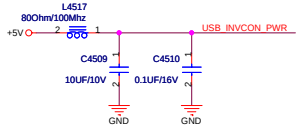
INVERTER
Interface/Speaker CONN.

Delete LID_SW SCH



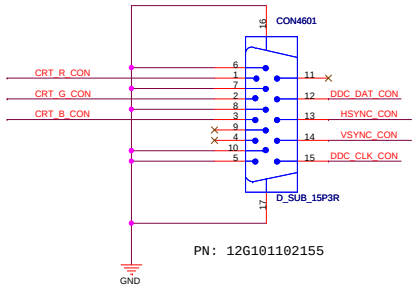
EMI REQUEST





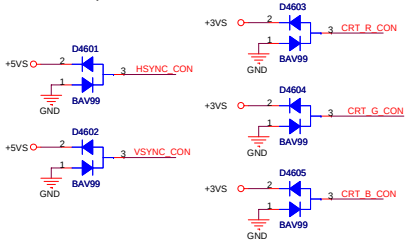
<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Richard_Lu	
Size: C	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 45 of 94	



PN: 12G101102155

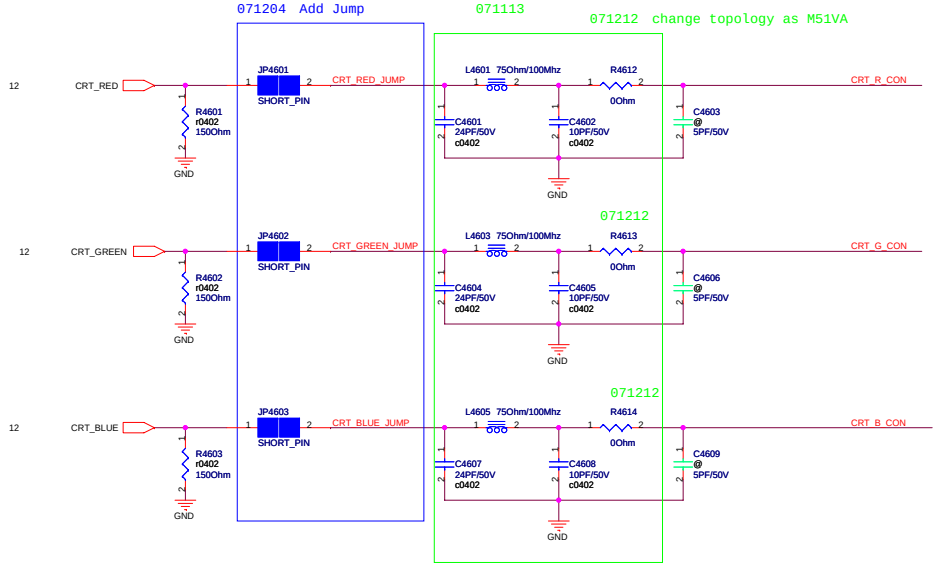
PLACE ESD Diodes near VGA port

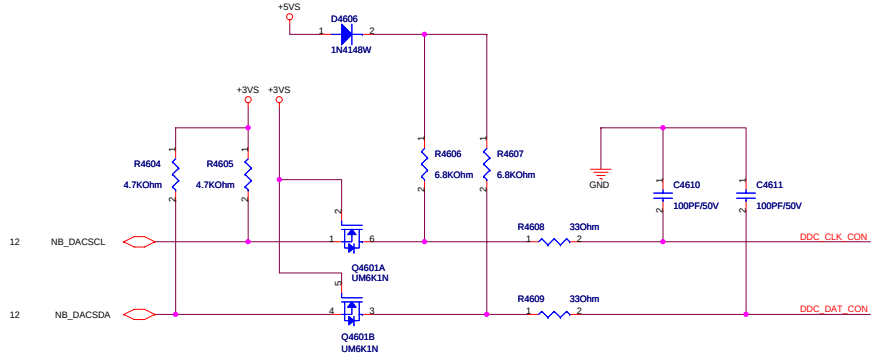


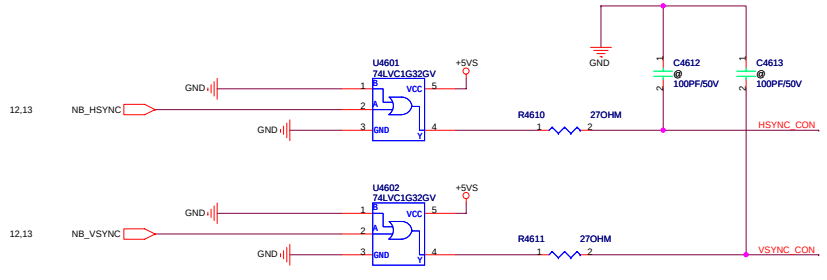
071204 Add Jump

071113

071212 change topology as M51VA







<Variant Name>

ASUSTeK COMPUTER INC

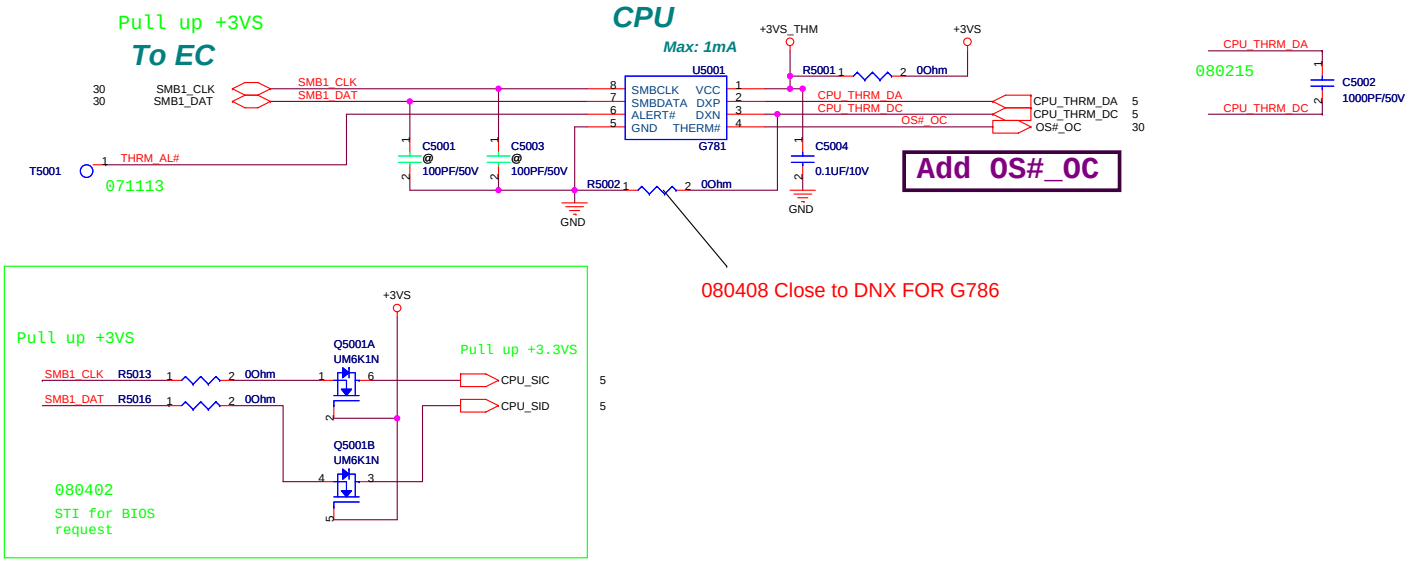
Title : CRT

Engineer: Richard Lu

Size	Project Name	Rev
C	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 46 of 94

Thermal Sensor

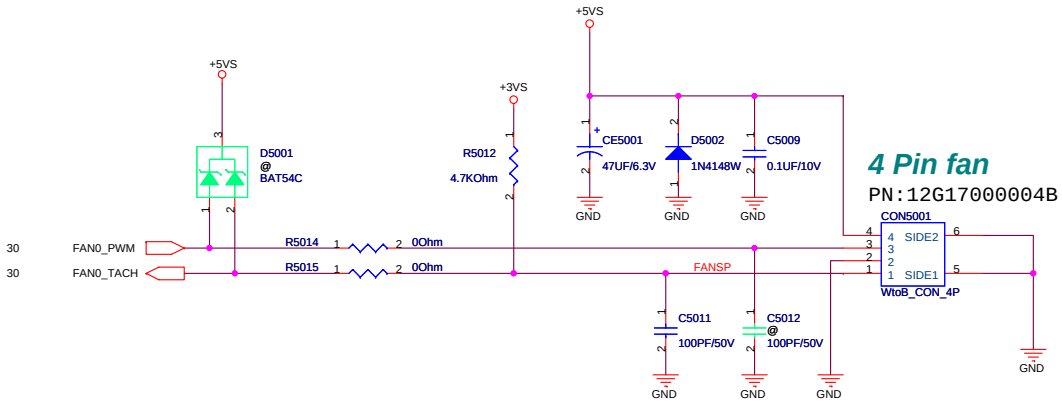


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



<Variant Name>

ASUSTeK COMPUTER INC

Title : THER SENSOR & FAN

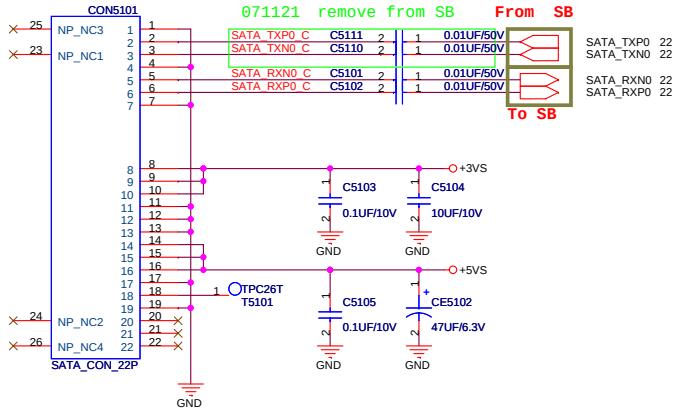
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

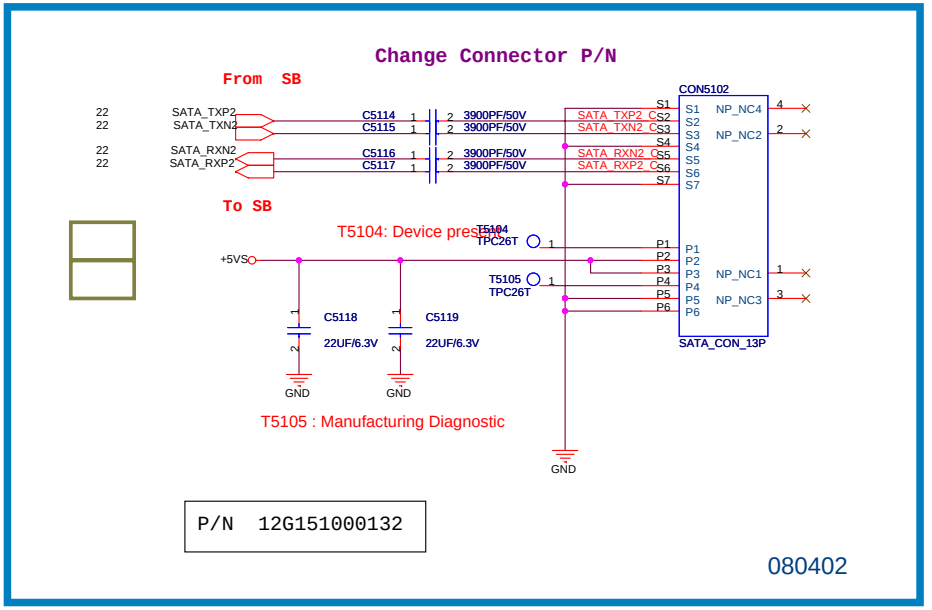
Date: Monday, May 19, 2008 Sheet 50 of 94

SATA HDD

071212
change 0.01UF P/N



ODD



<Variant Name>

ASUSTeK COMPUTER INC

Title : HDD & CD-ROM

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 51 of 94

071119 change common choke and R P/N

Change all MOS with ESD part

RN5201A
RN5201B
RN5202A
RN5202B
RN5203A
RN5203B
RN5204A
RN5204B
RN5205A
RN5205B
0Ohm

L5201 90Ohm/100Mhz 09G092090107
L5202 90Ohm/100Mhz 09G092090107
L5203 90Ohm/100Mhz 09G092090107
L5204 90Ohm/100Mhz 09G092090107
L5205 90Ohm/100Mhz 09G092090107
L5209 80Ohm/100Mhz
L5210 80Ohm/100Mhz
L5208 80Ohm/100Mhz

USB_PP3 USB_PN3 USB_LP3+ USB_LP3-
USB_PP2 USB_PN2 USB_LP2+ USB_LP2-
USB_PP1 USB_PN1 USB_LP1+ USB_LP1-
USB_PP0 USB_PN0 USB_LP0+ USB_LP0-
USB_PP5 USB_PN5 USB_LP5+ USB_LP5-

D5201 EGA10603V05A1
D5202 EGA10603V05A1
D5204 EGA10603V05A1
D5203 EGA10603V05A1
D5206 EGA10603V05A1
D5205 EGA10603V05A1
D5208 EGA10603V05A1
D5207 EGA10603V05A1
D5210 EGA10603V05A1
D5209 EGA10603V05A1

071119

swap 080214
swap 080214
swap
080213

Q5201 2N7002K_T1_E3 USB_OC23# USB_OC23#
Q5202 2N7002K_T1_E3 USB_OC01# USB_OC01#
Q5204 2N7002K_T1_E3 USB_OC5# USB_OC5#

F5202 2A/8V
F5203 2A/8V
F5204 0.75A/13.2V

R5215 4.7KOhm
R5210 8.2KOhm
R5214 4.7KOhm
R5211 8.2KOhm
R5213 4.7KOhm
R5212 8.2KOhm

CE5203 47UF/6.3V
C5204 0.1UF/10V
CE5204 47UF/6.3V
C5205 0.1UF/10V
CE5205 47UF/6.3V
C5206 0.1UF/10V
CE5206 47UF/6.3V
C5207 0.1UF/10V
CE5208 47UF/6.3V
C5209 0.1UF/10V

USBCN1 USBCN2 USBCN0
USB_CON_2X4P
USB_CON_1X4P

+5V GND

<Variant Name>

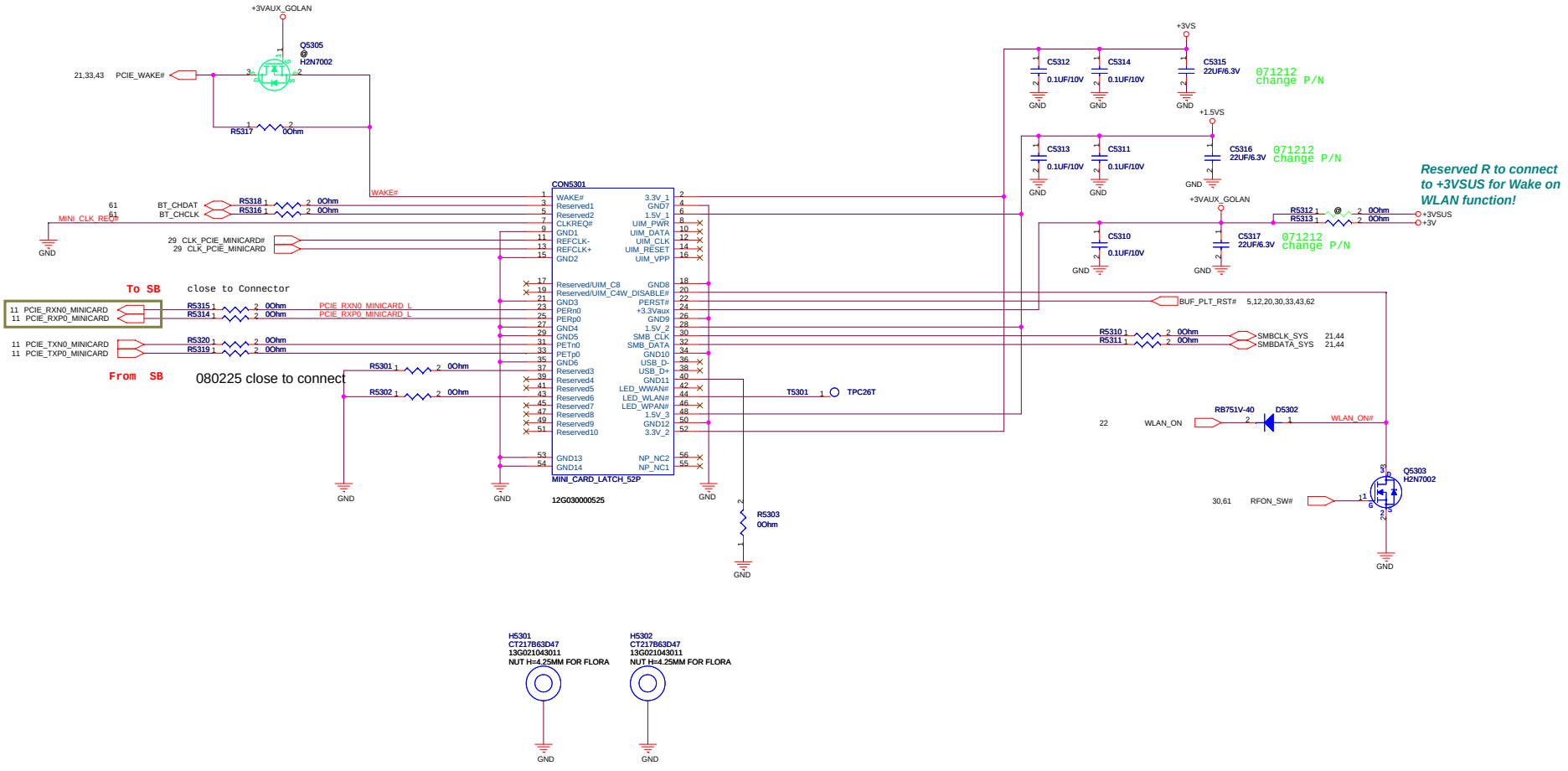
ASUSTeK COMPUTER INC

Title : USB CONN

Engineer: Richard Lu

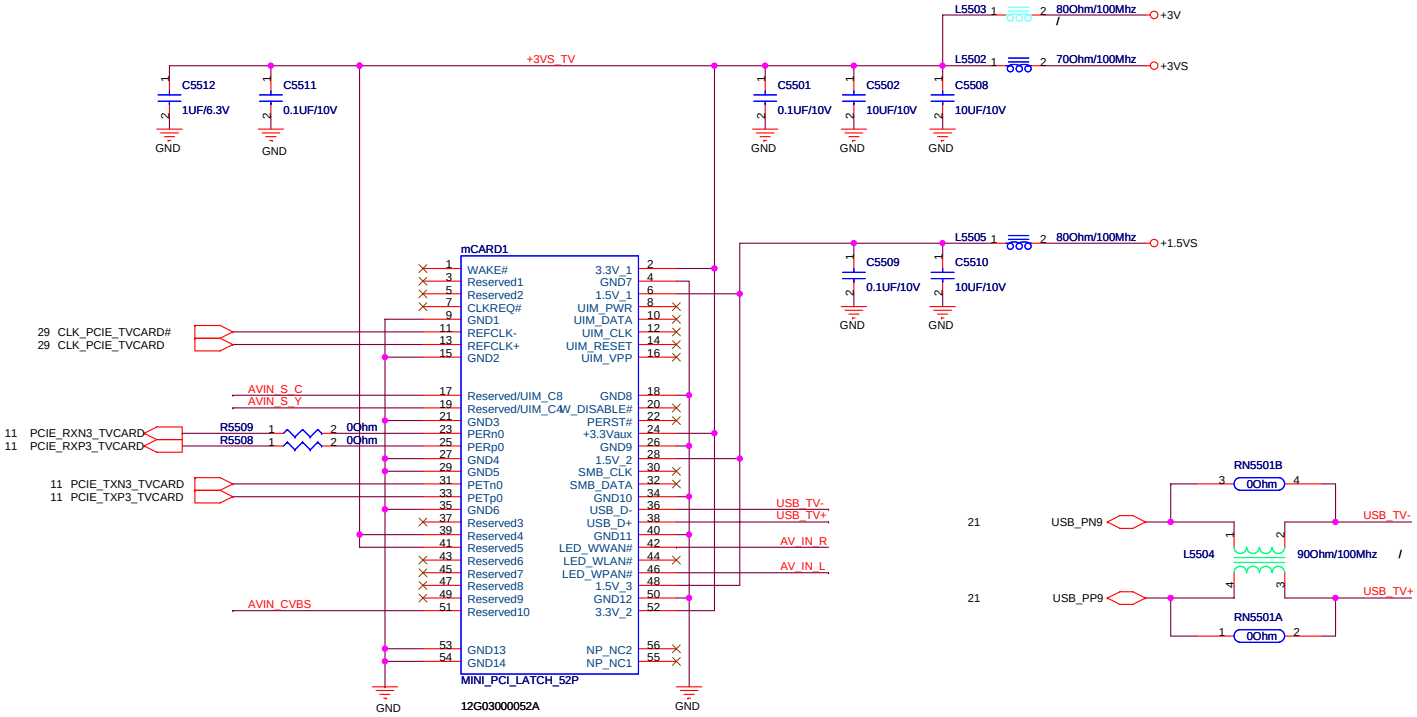
Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 52 of 94



<Variant Name>

ASUSTeK COMPUTER INC	Title : MINICARD	
	Engineer: Richard Lu	
Size: C	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 53 of 94	

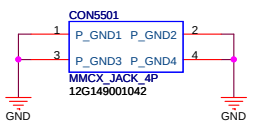


H = 5.2mm

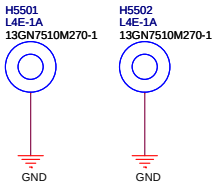
FOR TV TUNER

(UWB OPTION)

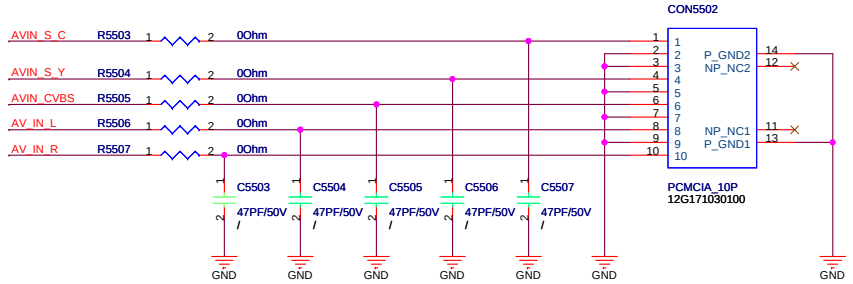
TV Conn.



ME P/N : 14G152075000



H = 3.0mm



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

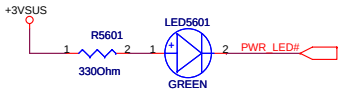
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

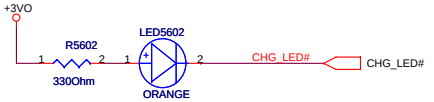
Date: Monday, May 19, 2008 Sheet 55 of 94

LED

For POWER LED

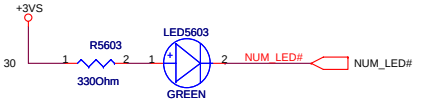


BATTERY LED



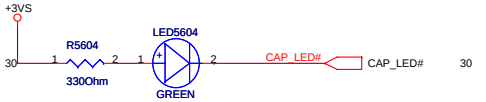
Num Lock

071122



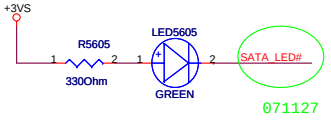
Cap Lock

071122



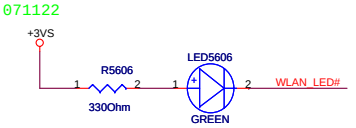
SATA/IDE LED

071122



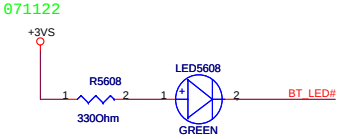
WireLess LED

071122



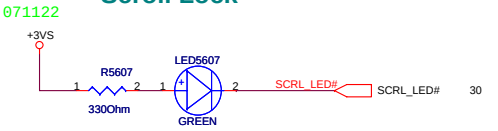
BT LED

071122



Scroll Lock

071122



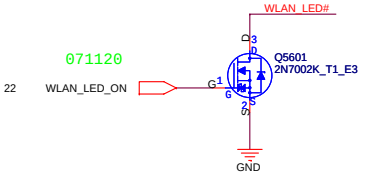
Change all LED for 5mA

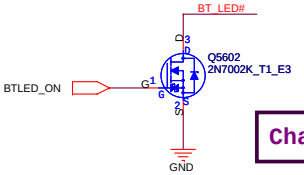
delete D5601

071127

From SB GPIO

071120





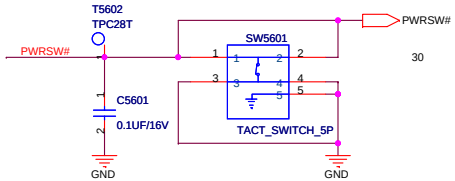
Change all MOS with ESD part

F5Z SWITCH CIRCUIT

Move SW from P32 to P56

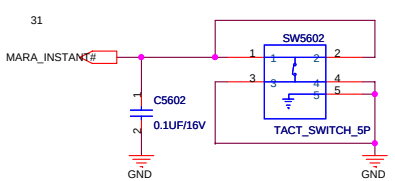
Add SHUT Down SCH

Power SW.

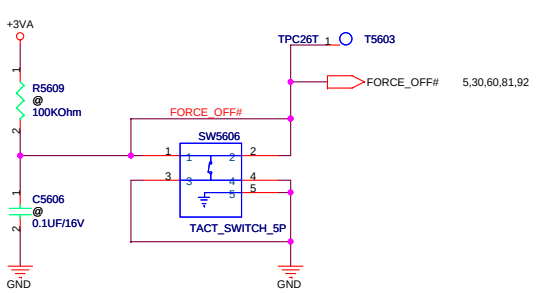


P/N: 12G091030050

Marathon SW.

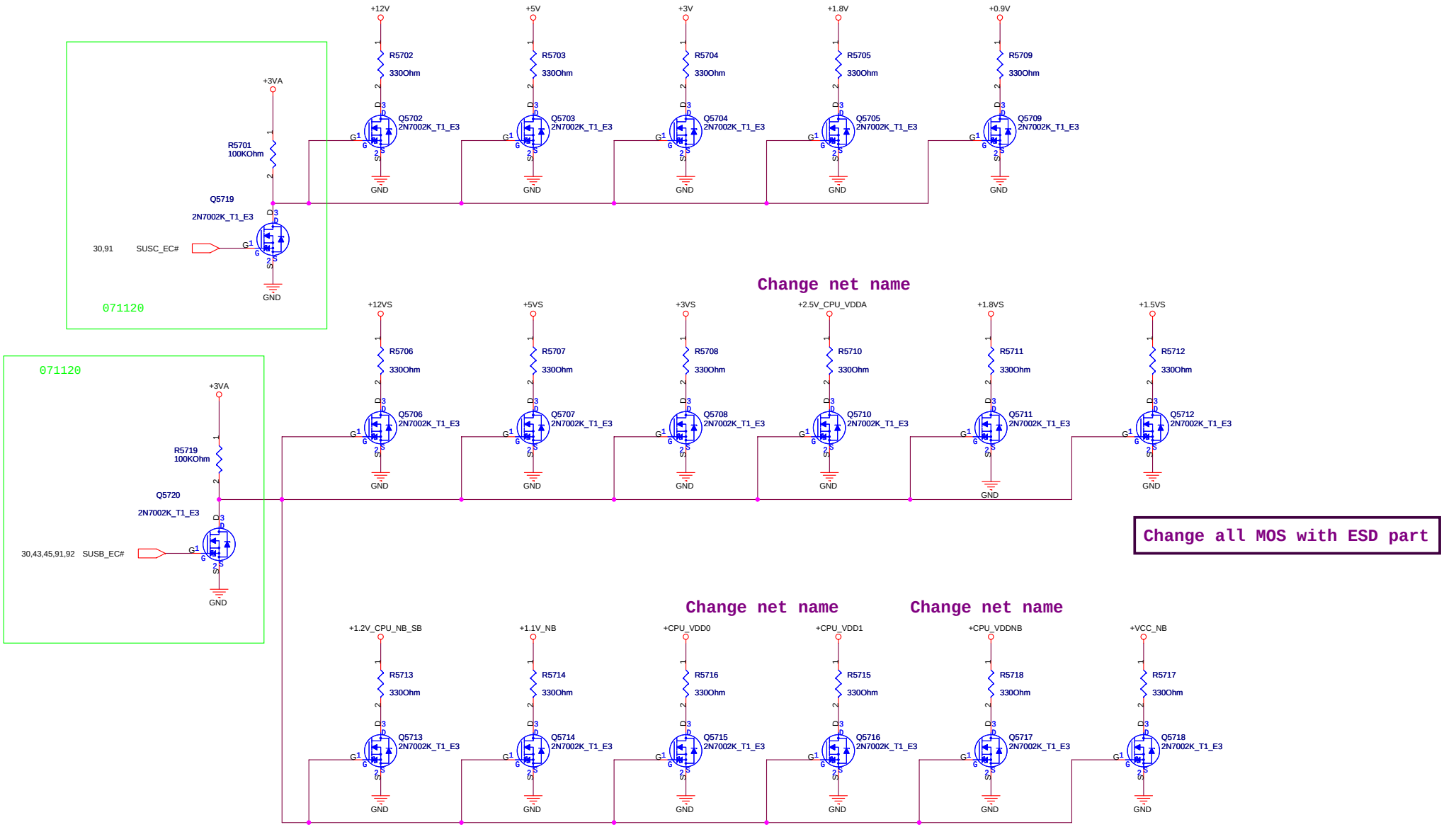


SHUT_DOWN#



<Variant Name>

ASUSTeK COMPUTER INC	Title : LED/PWR SWICH	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 56 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

Title : DISCHARGE CKT

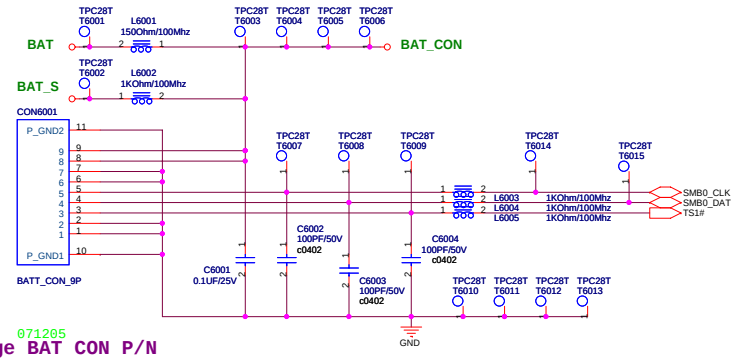
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 57 of 94

071120 cahnge PL->L,PT->T,PC->C

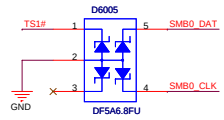
BATTERY



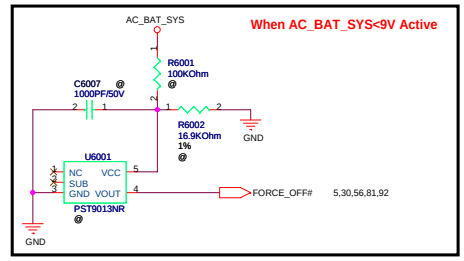
071205
Change BAT CON P/N

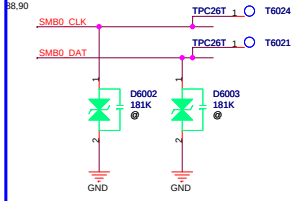
Reference To M51

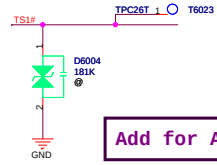
071203 change footprint



Without Battery & Pull out Adapter

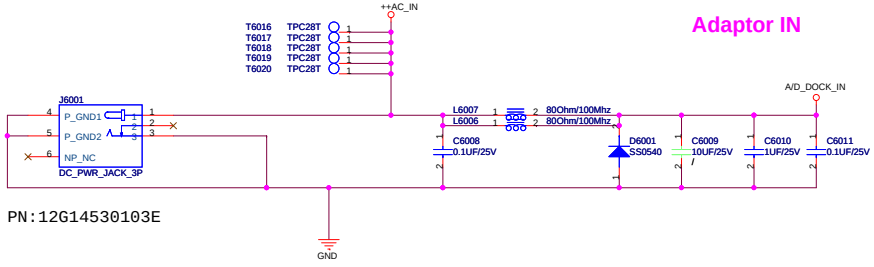






Add for AC Adapter protect

DC JACK-IN



PN:12G14530103E

071218
Delete GND_DC , Bead
,and Test Point

<Variant Name>

ASUSTeK COMPUTER INC

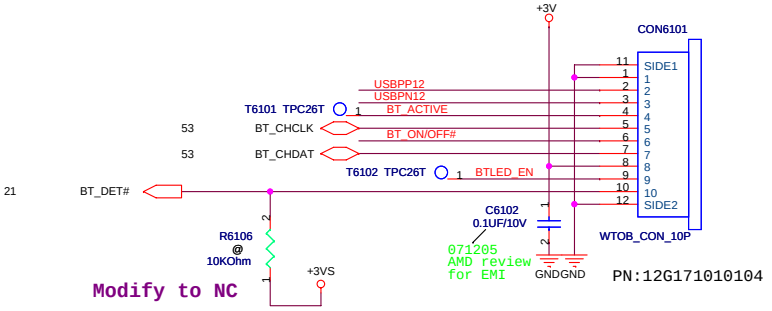
Title : DC_Jack & BAT Con

Engineer: Richard_Lu

Size	Project Name	Rev
C	F7Z	1.0

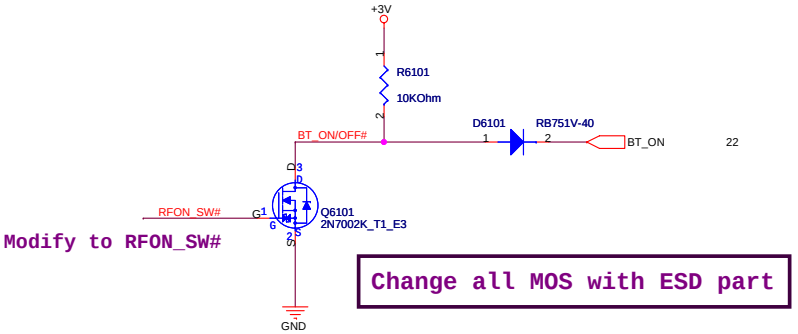
Date: Monday, May 19, 2008 Sheet 60 of 94

For Bluetooth



PN:12G171010104

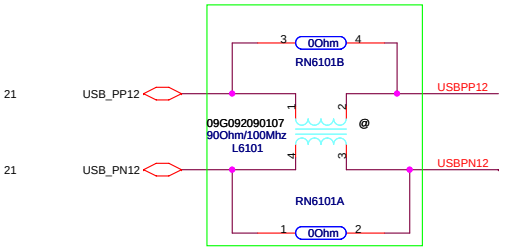
Modify to NC



Modify to RFON_SW#

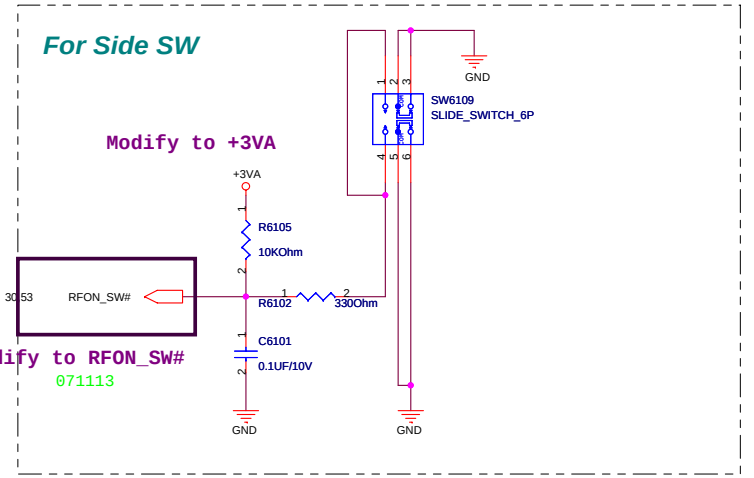
Change all MOS with ESD part

RN swap
071214



071120 change common choke and R P/N

For Side SW



Modify to +3VA

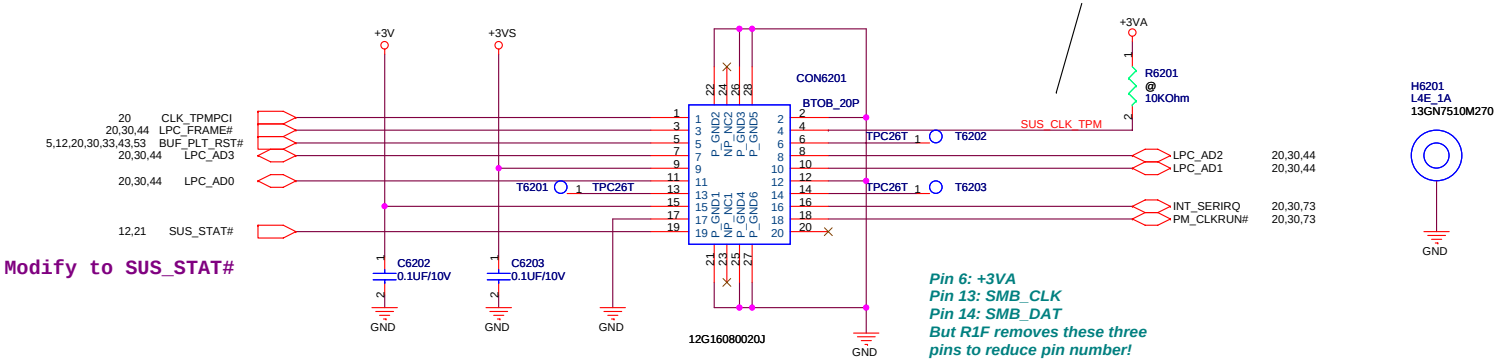
Modify to RFON_SW#
071113

<Variant Name>

ASUSTeK COMPUTER INC	Title : BT & Slide SW	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 61 of 94	

For TPM Module

071120
TPM module has internal crystal



H6201
L4E_1A
13GN7510M270
GND

Modify to SUS_STAT#

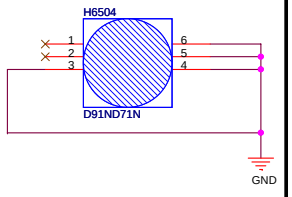
Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

SN:12G16080020J

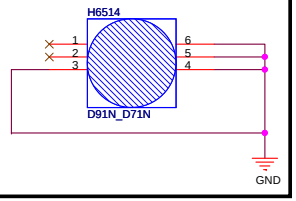
<Variant Name>

ASUSTeK COMPUTER INC	Title : TPM	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 62 of 94	

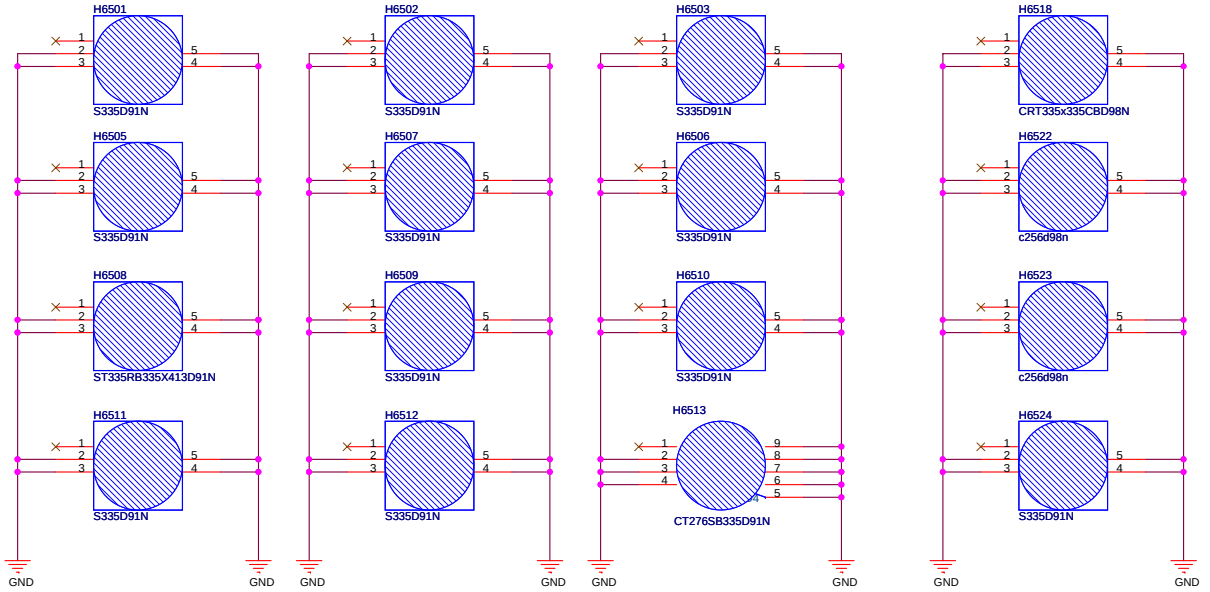
FOR LEFT UNDER



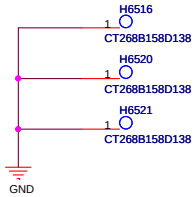
FOR RIGHT UP



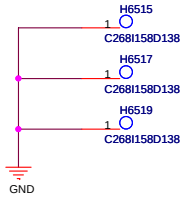
FOR SCREW HOLE

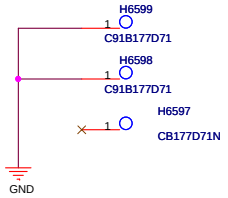


FOR CPU



FOR VGA





<Variant Name>

ASUSTeK COMPUTER INC

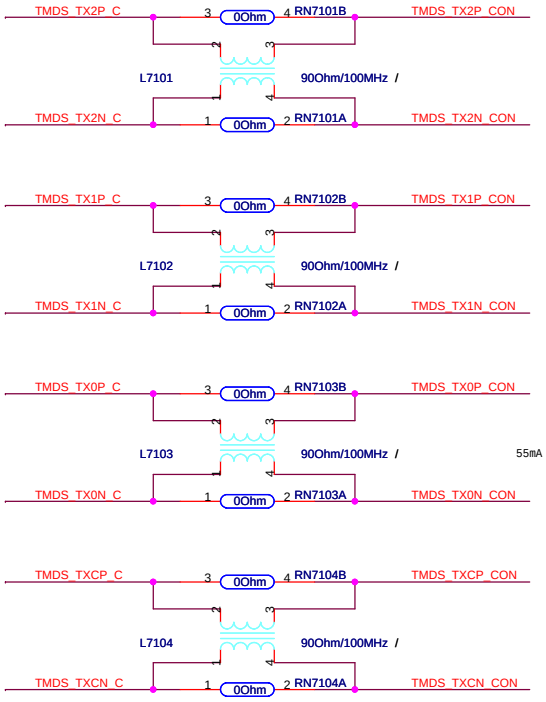
Title : Screw Hole

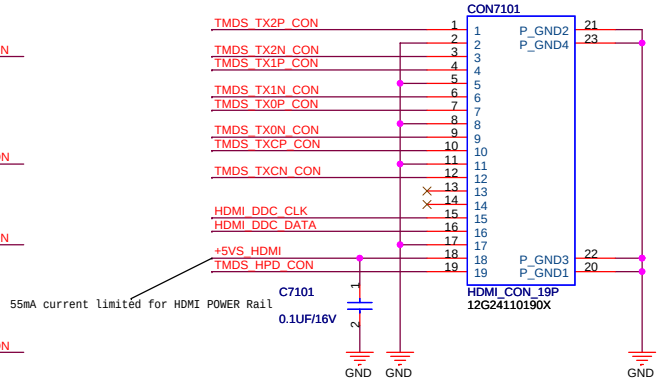
Engineer: <OrgAddr1>

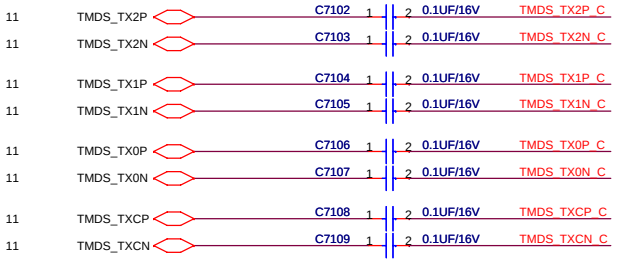
Size	Project Name	Rev
Custom	F7Z	1.0

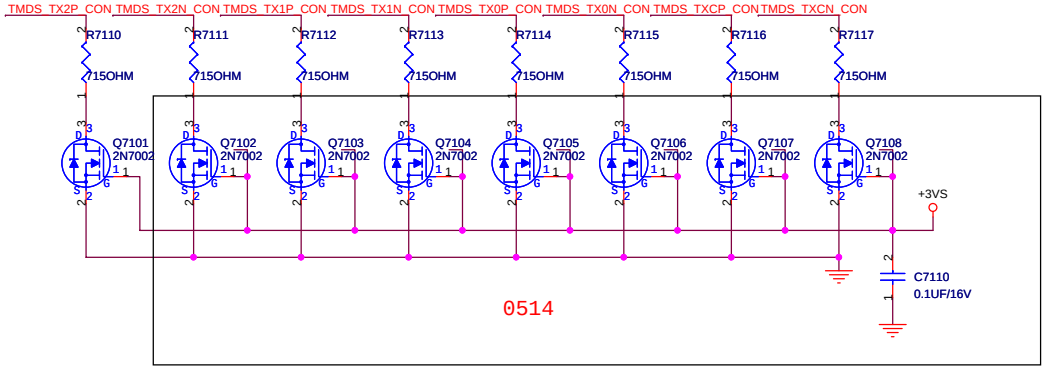
Date: Monday, May 19, 2008 Sheet 65 of 94

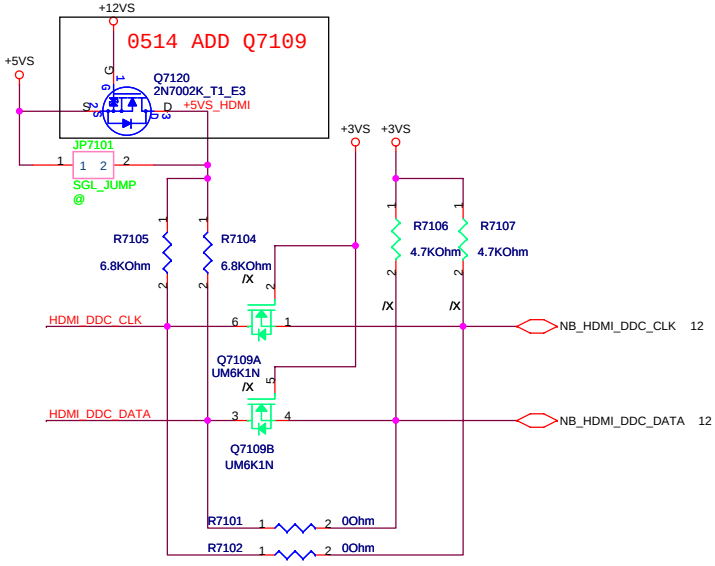
HDMI

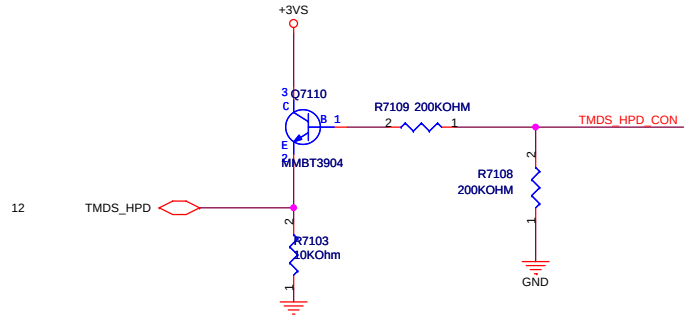












<Variant Name>

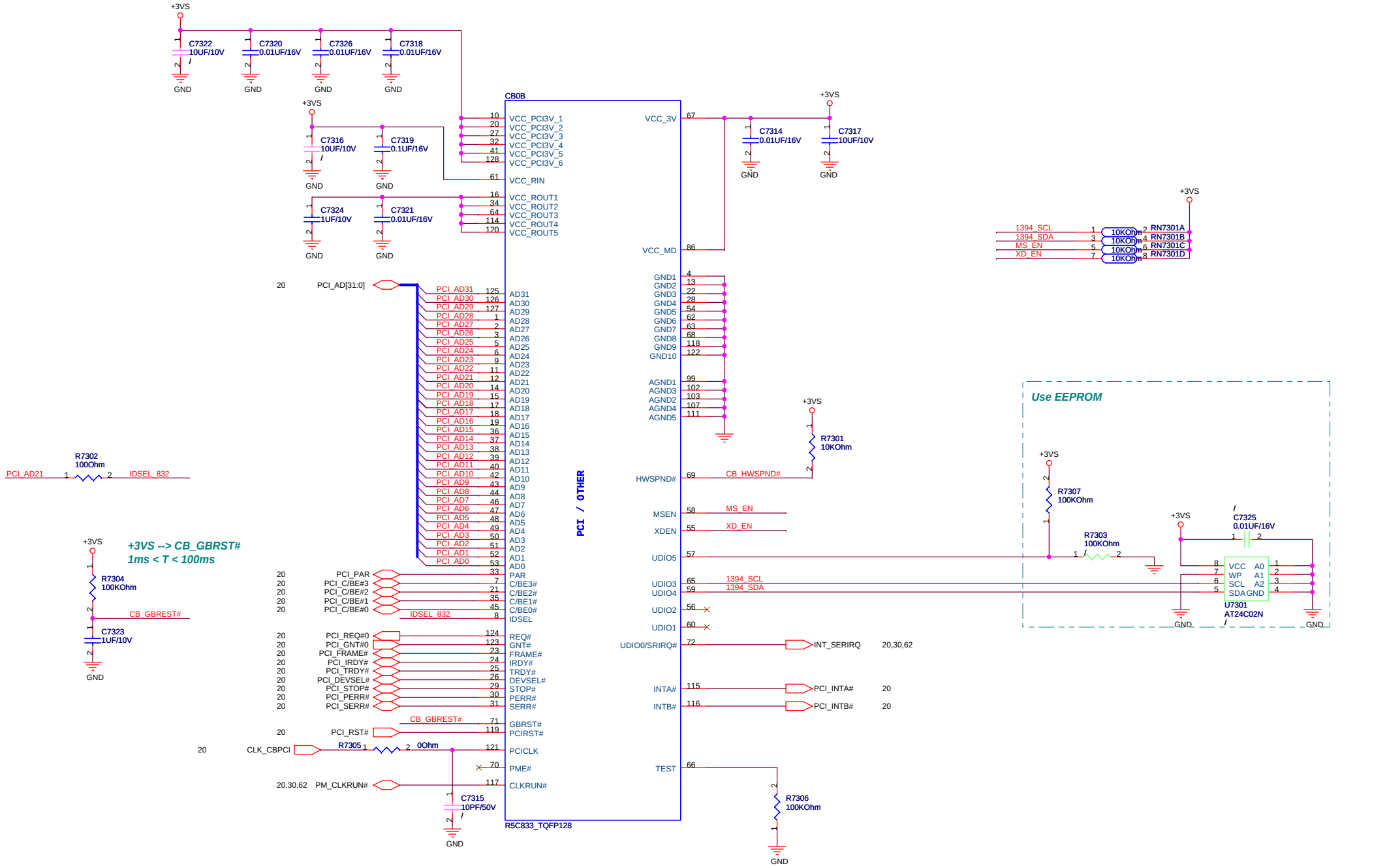
ASUSTeK COMPUTER INC

Title : HDMI CON

Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 71 of 94



<Variant Name>

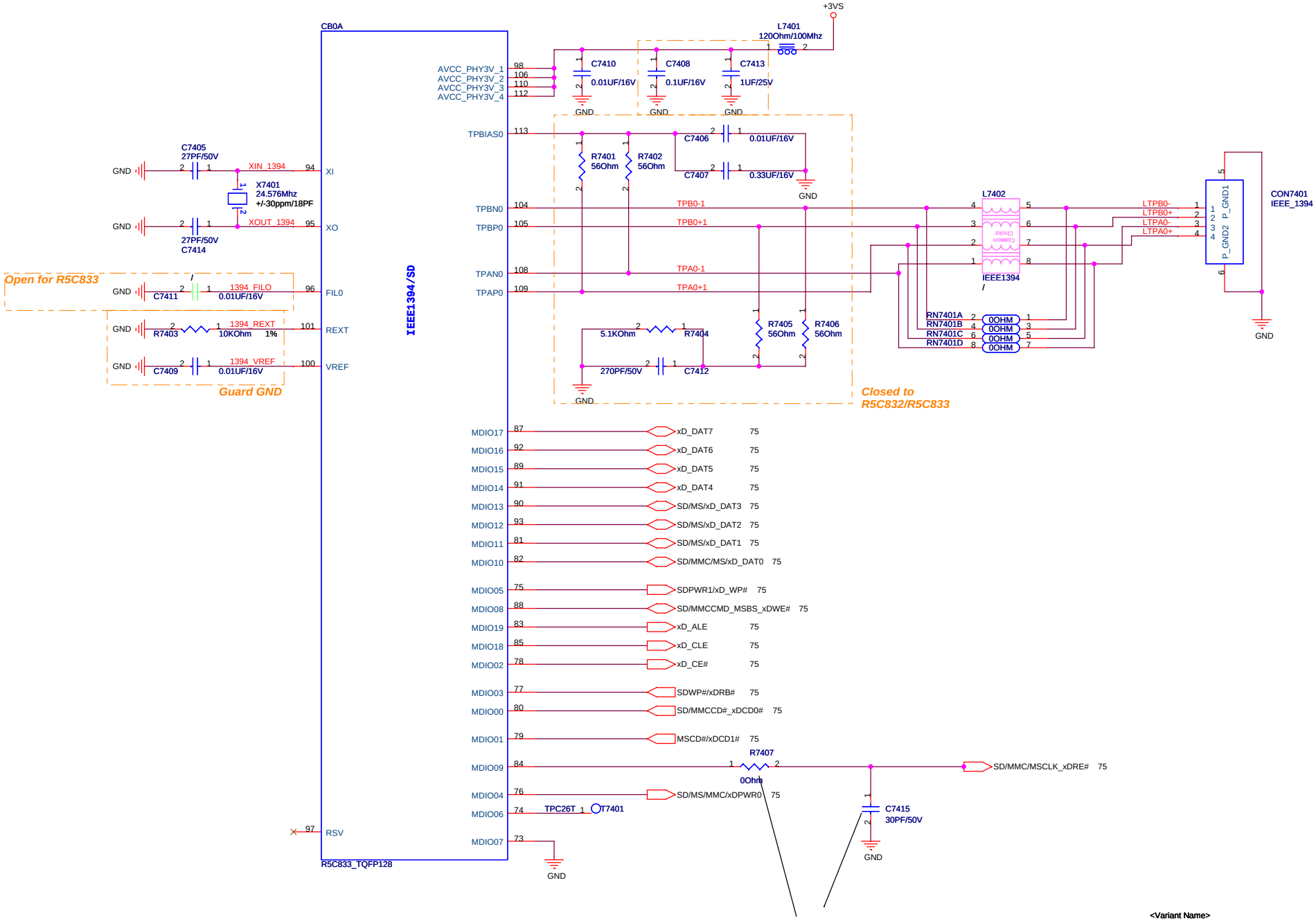
ASUSTeK COMPUTER INC

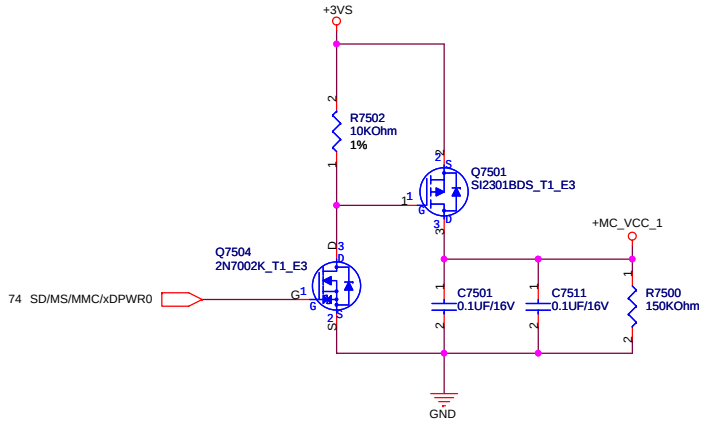
Title : *

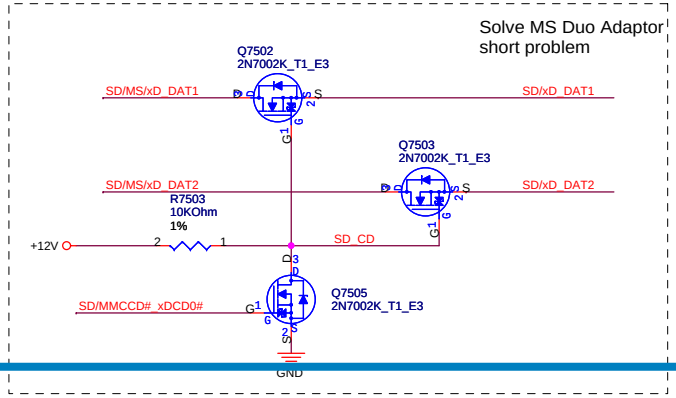
Engineer:

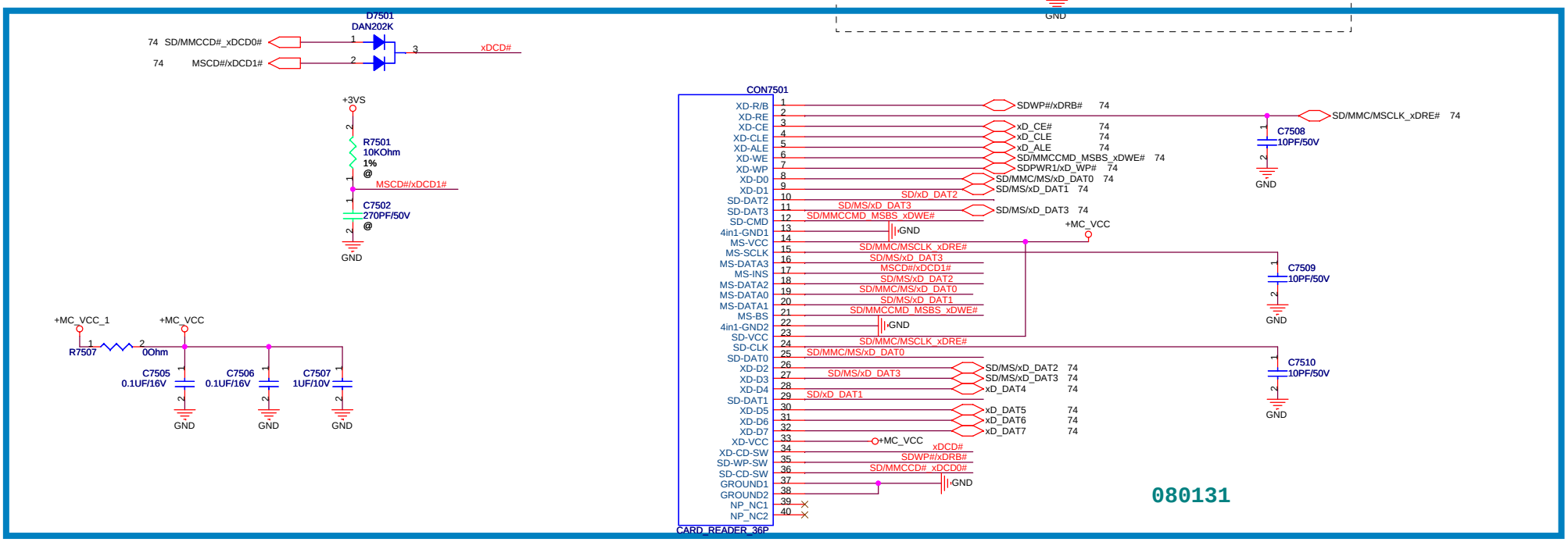
Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 73 of 94


CB0A
IEEE1394/SD
R5C833_TQFP128
+3VS
L7401
120Ohm/100Mhz
C7410
0.01UF/16V
C7408
0.1UF/16V
C7413
1UF/25V
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
TPBIAS0
C7406
0.01UF/16V
C7407
0.33UF/16V
R7401
56Ohm
R7402
56Ohm
C7405
27PF/50V
XIN_1394
XI
X7401
24.576Mhz
+/-30ppm/18PF
XOUT_1394
XO
C7414
27PF/50V
Open for R5C833
C7411
1394_FIL0
0.01UF/16V
FIL0
R7403
1394_REXT
10KOhm
1%
REXT
C7409
1394_VREF
0.01UF/16V
VREF
Guard GND
TPBN0
TPBP0
TPAN0
TPAP0
TPB0-1
TPB0+1
TPA0-1
TPA0+1
L7402
IEEE1394
RN7401A
RN7401B
RN7401C
RN7401D
0OHM
LTPB0-
LTPB0+
LTPA0-
LTPA0+
CON7401
IEEE_1394
P_GND1
P_GND2
R7405
56Ohm
R7406
56Ohm
5.1KOhm
R7404
270PF/50V
C7412
Closed to
R5C832/R5C833
MDIO17 xD_DAT7 75
MDIO16 xD_DAT6 75
MDIO15 xD_DAT5 75
MDIO14 xD_DAT4 75
MDIO13 SD/MS/xD_DAT3 75
MDIO12 SD/MS/xD_DAT2 75
MDIO11 SD/MS/xD_DAT1 75
MDIO10 SD/MMC/MS/xD_DAT0 75
MDIO05 SDPWR1/xD_WP# 75
MDIO08 SD/MMCCMD_MSBS_xDWE# 75
MDIO19 xD_ALE 75
MDIO18 xD_CLE 75
MDIO02 xD_CE# 75
MDIO03 SDWP#/xDRB# 75
MDIO00 SD/MMCCD#_xDCD0# 75
MDIO01 MSCD#/xDCD1# 75
MDIO09
MDIO04 SD/MS/MMC/xDPWR0 75
MDIO06
MDIO07
R7407
0Ohm
SD/MMC/MSCLK_xDRE# 75
C7415
30PF/50V
TPC26T
T7401
RSV
GND
080408 Add r7407 and c7415 for EMI
<Variant Name>
Title : *
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 74 of 94







<variant_name>

ASUSTeK COMPUTER INC

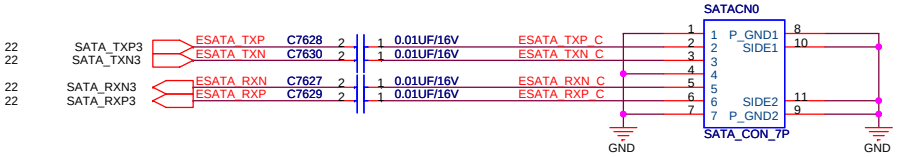
Title : *

Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 75 of 94

eSATA Connector



<Variant Name>

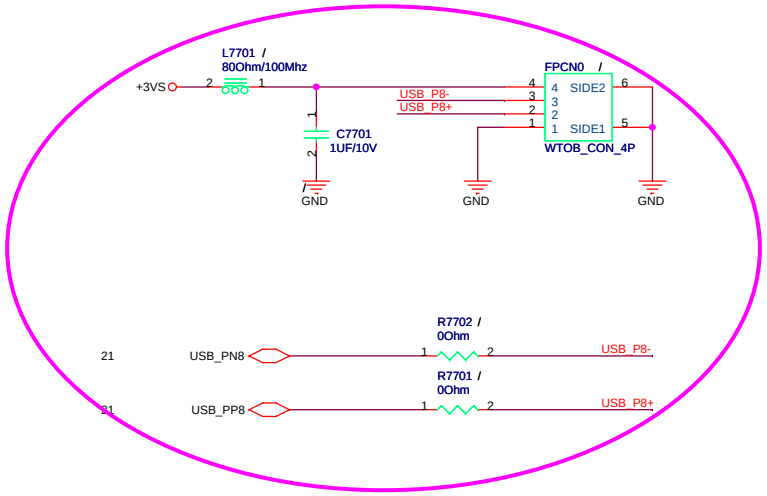
Title : *

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 76 of 94



<Variant Name>

ASUSTeK COMPUTER INC

Title : *

Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 77 of 94

080131 Change cardreader connect to 12G340003601.change CDROM connect to 12G151000132 .
080215 1.change thermal sensor to G781,change C5002 to 1000pf
2.fix stuff TMP module can not boot

080217 change C3711/C3712/C3709/C3710 connect to GND
change D7101 to 2 Pin
080219 Remove R3052 and R3108,move D3103 to R3052(N connect to EC side)
change Q9101/Q9107 to 07G005161020(07G005357011)

080221 change ec to 8512 Page82 Page83

080222 add C0651/C0652/C0653/C0654

080225 add R1408/R4307/R4308/R5319/R5320

080408 Add r7407 and c7415 for EMI

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F7Z	1.0

Date: Monday, May 19, 2008 Sheet 78 of 94

ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V Pre_metal	X	X

VFIXEN VID Codes

SVC	SVD	Output	Pre_metal
0	0	1.4	1.1
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8

Design Current : 4A
Maximum current : 4.4A
OCP point Typ : 4.6A
+CPU_VDDNB +CPU_VDDNB_O

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 21.6A
+CPU_VDD0

Design Current : 14.4A
Maximum current : 18A
OCP point Typ.: 21.6A
+CPU_VDD1

U8000 ISL6265HRTZ-T

close to CPU socket

Parallel

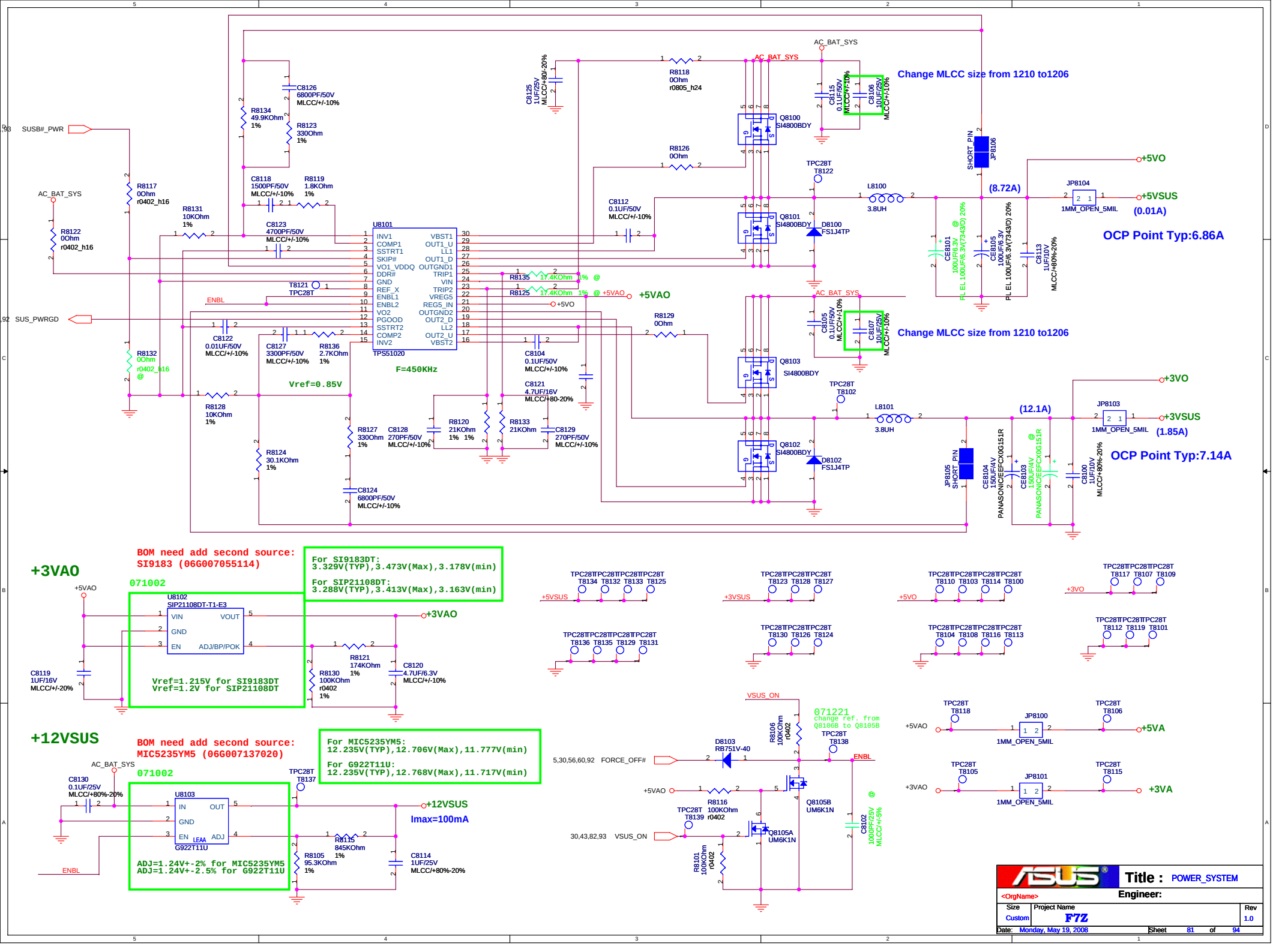
Parallel

Change Footprint For Net_IN

+3VSUS

SVC	SVD	Output
R8076	R8077	1.4
R8076	R8074	1.2
R8075	R8077	1.0
R8075	R8074	0.8

Title : POWER_VCORE
<OrgName>
Engineer:
Size: Custom
Project Name: F7Z
Rev: 1.0
Date: Monday, May 19, 2008
Sheet 80 of 94


SUSB#_PWR
SUS_PWRGD
AC_BAT_SYS
ENBL
U8101
TPS51020
F=450KHz
Vref=0.85V
Change MLCC size from 1210 to1206
Change MLCC size from 1210 to1206
+5VAO
+5VO
+5VSUS
(0.01A)
(8.72A)
OCP Point Typ:6.86A
+3VO
+3VSUS
(1.85A)
(12.1A)
OCP Point Typ:7.14A
+3VA0
BOM need add second source:
SI9183 (06G007055114)
071002
For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)
For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)
U8102
SIP21108DT-T1-E3
Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)
071002
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
U8103
G922T11U
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U
Imax=100mA
071221
change ref. from Q8106B to Q8105B
FORCE_OFF#
VSUS_ON
Q8105B UM6K1N
Q8105A UM6K1N
D8103 RB751V-40
Title : POWER_SYSTEM
Engineer:
Project Name F7Z
Rev 1.0
Date: Monday, May 19, 2008
Sheet 81 of 94

* Rocset = Ioc * DRC / 10uA

+1.2VO: ROCSET = R8213 ; R8215 = R8213=10KOhm; OCP>7.5A

+1.8VO: ROCSET = R8212 ; R8212 =R8211 =4.7KOhm ; OCP>14A

* VREF = 0.6V+-1%

+1.2VO = VREF * (R8206 + R8214) / R8214 =1.2V+-2%

+1.8VO = VREF * (R8207 + R8210) / R8207=1.806V+-2.38% (1.764~1.849)

* Fsw = 1 / K / Rfset ; K = 1.5 * 10e-10

+1.2VO: Rfset =R8204; Fsw=366KHz

+1.8VO: Rfset =R8202; Fsw=300KHz

* Pin 29 connect to GND with 5 Via independent, isolate Pin17 and Pin18

08/02/26change

08/04/14change

FSW2:366Khz

FSW1:300Khz

for jitter

U8200 ISL6228HRTZ_T

U8201 RT9173CPSP

+1.2VO (5.6A)

+1.2VSUS (0.31A)

+1.8VO (13.35A)

+1.8V (11.6A)

+0.9VO (3.25A)

+2.5VREF

VTT_PWRGD

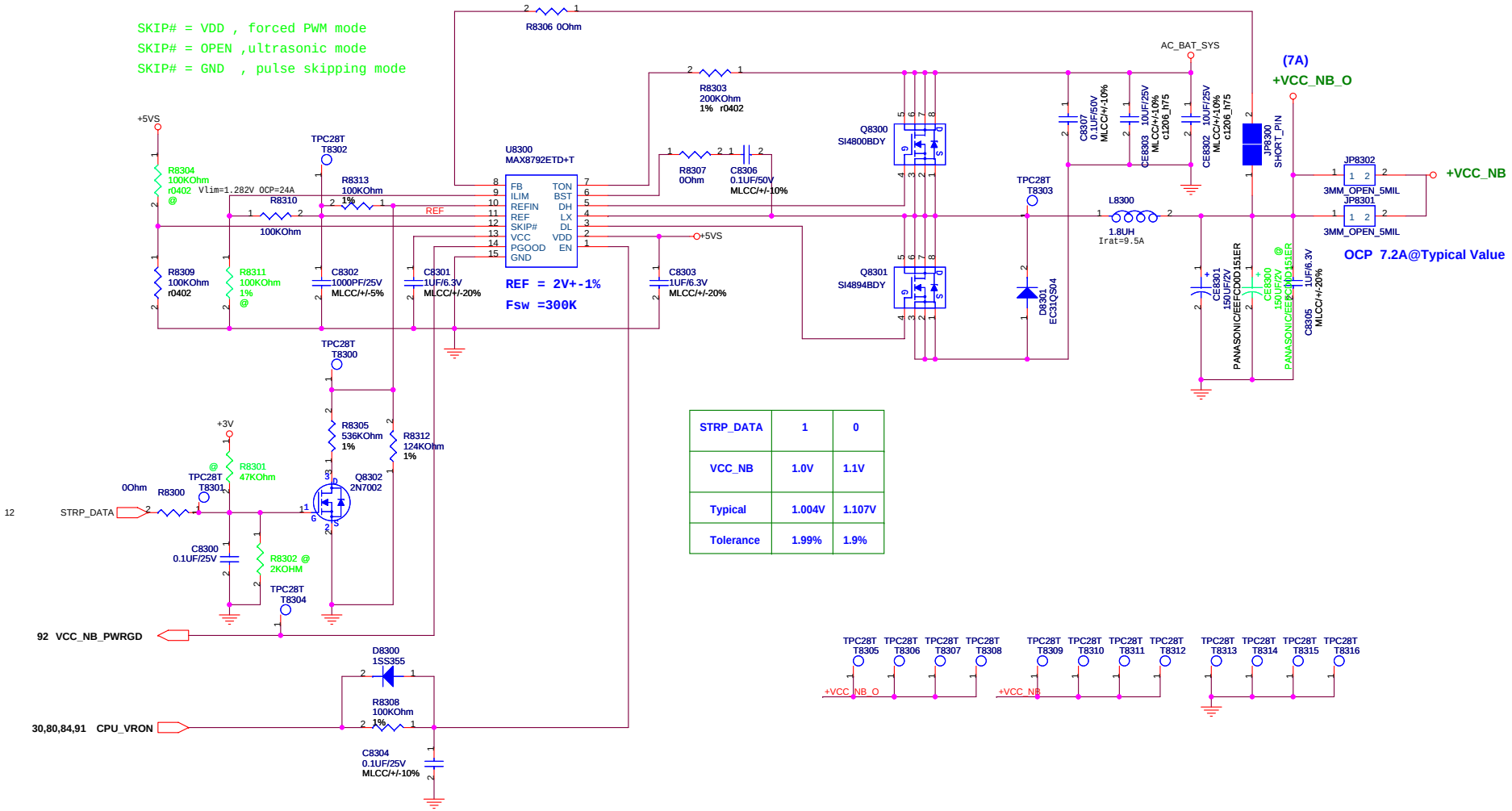
<OrgName>

Engineer:

Title : POWER_I/O_1.2VO & 1.8VO&0.9VO

Size: Custom | Project Name: F7Z | Rev: 1.0

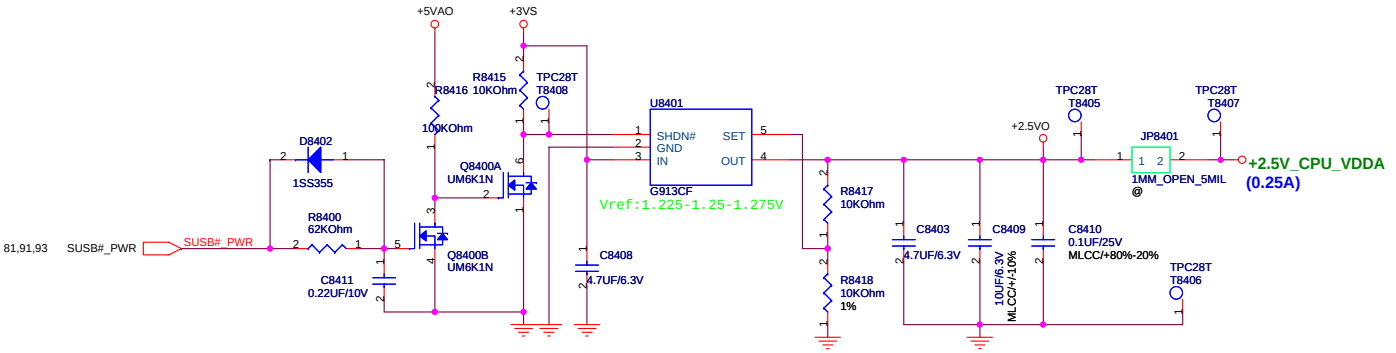
Date: Monday, May 19, 2008 | Sheet 82 of 94



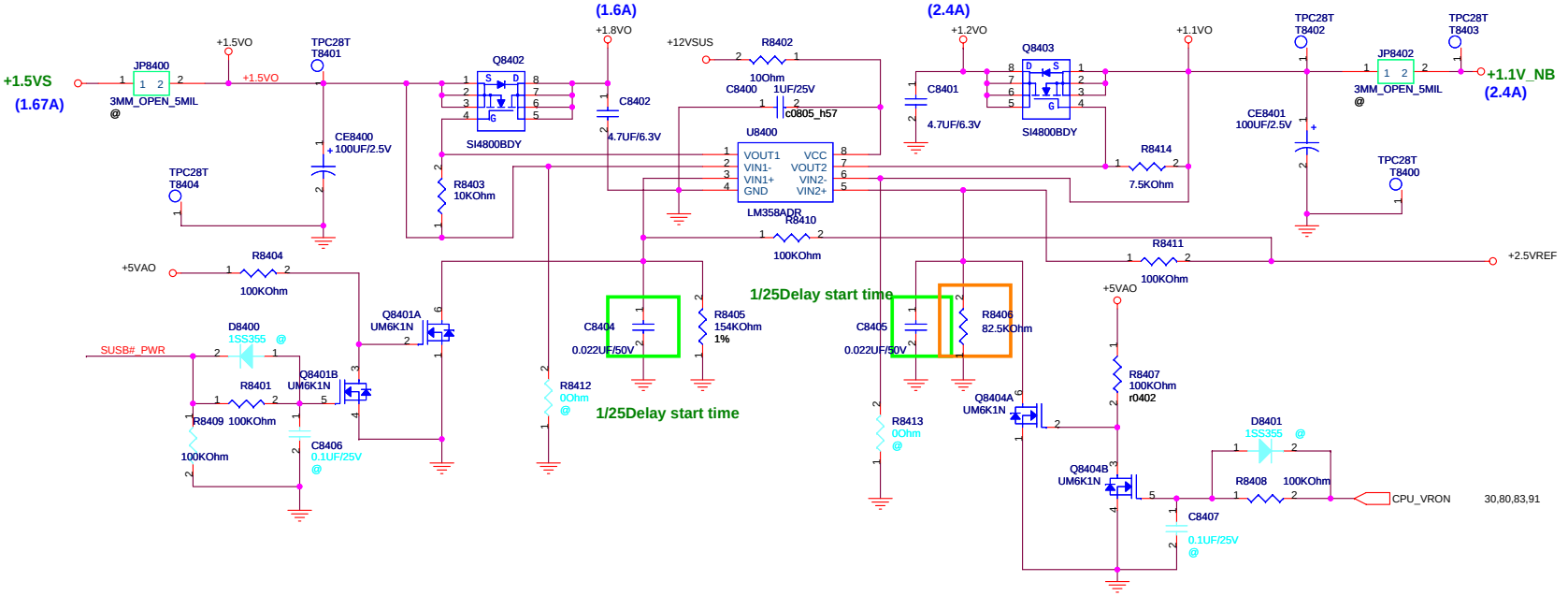
STRP_DATA	1	0
VCC_NB	1.0V	1.1V
Typical	1.004V	1.107V
Tolerance	1.99%	1.9%

Title : POWER_I/O_VCC_NB		
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 83 of 94	

+2.5V_CPU_VDDA

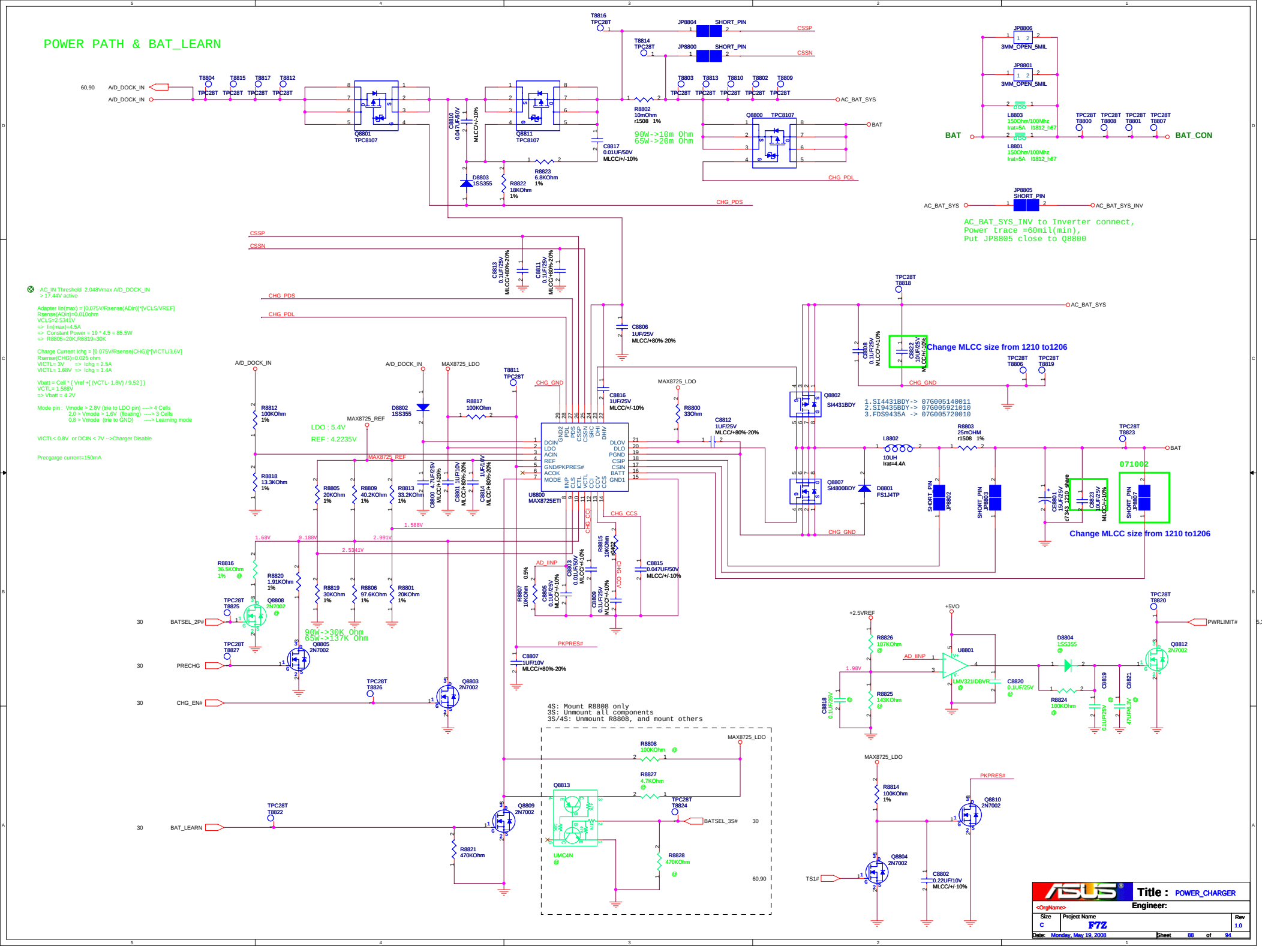


+1.5VS & +1.1V_NB

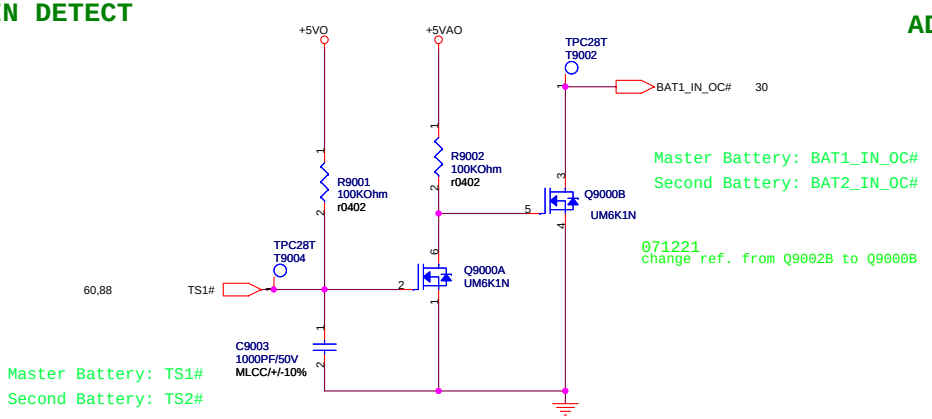


Title : POWER_+2.5VS&+1.5VS & +1.1VS		
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 84 of 94	

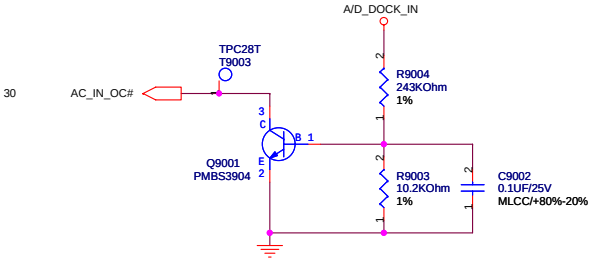
POWER PATH & BAT_LEARN



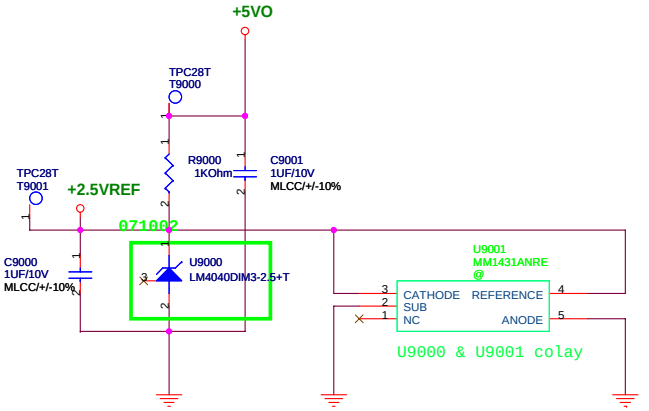
BATTERY IN DETECT



ADAPTER IN DETECT



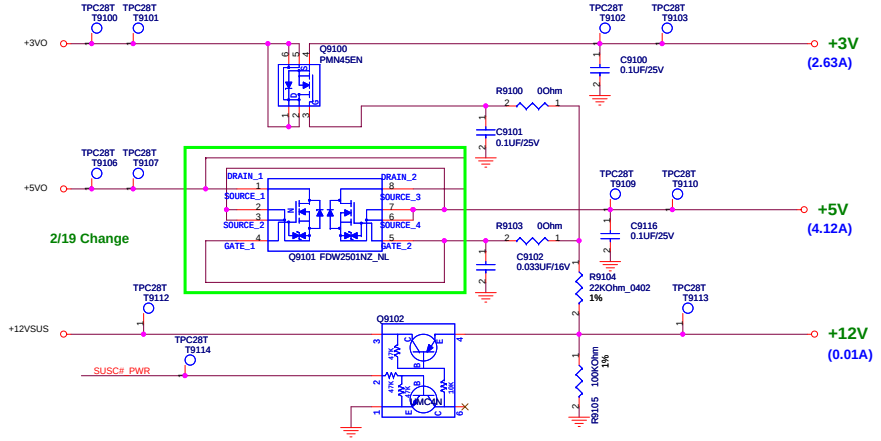
+2.5VREF

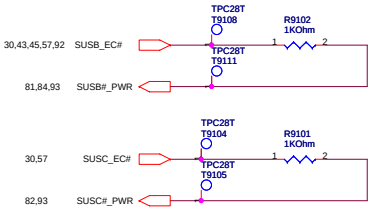


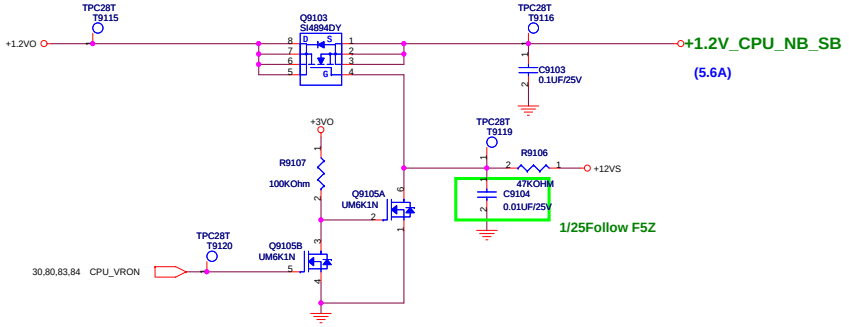
U9000 Main source change to 06G006002414(tolerence:1%).
Add second source 06G006002610 (tolerence:1%),
06G006002412 (tolerence:0.2%) and
06G006002020(tolerence:0.2%)

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 90 of 94	

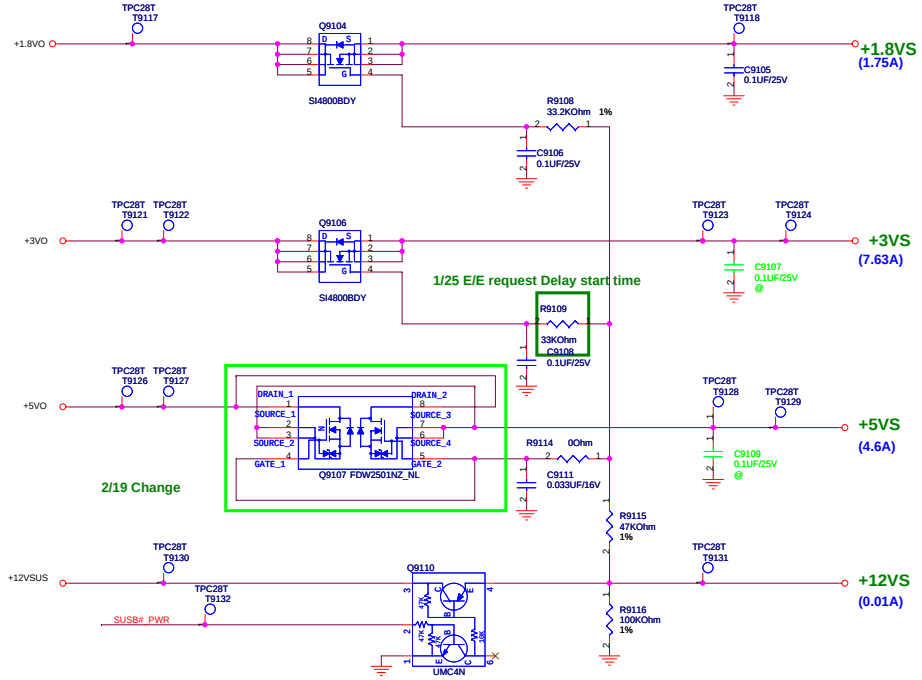
SUSC#_PWR POWER





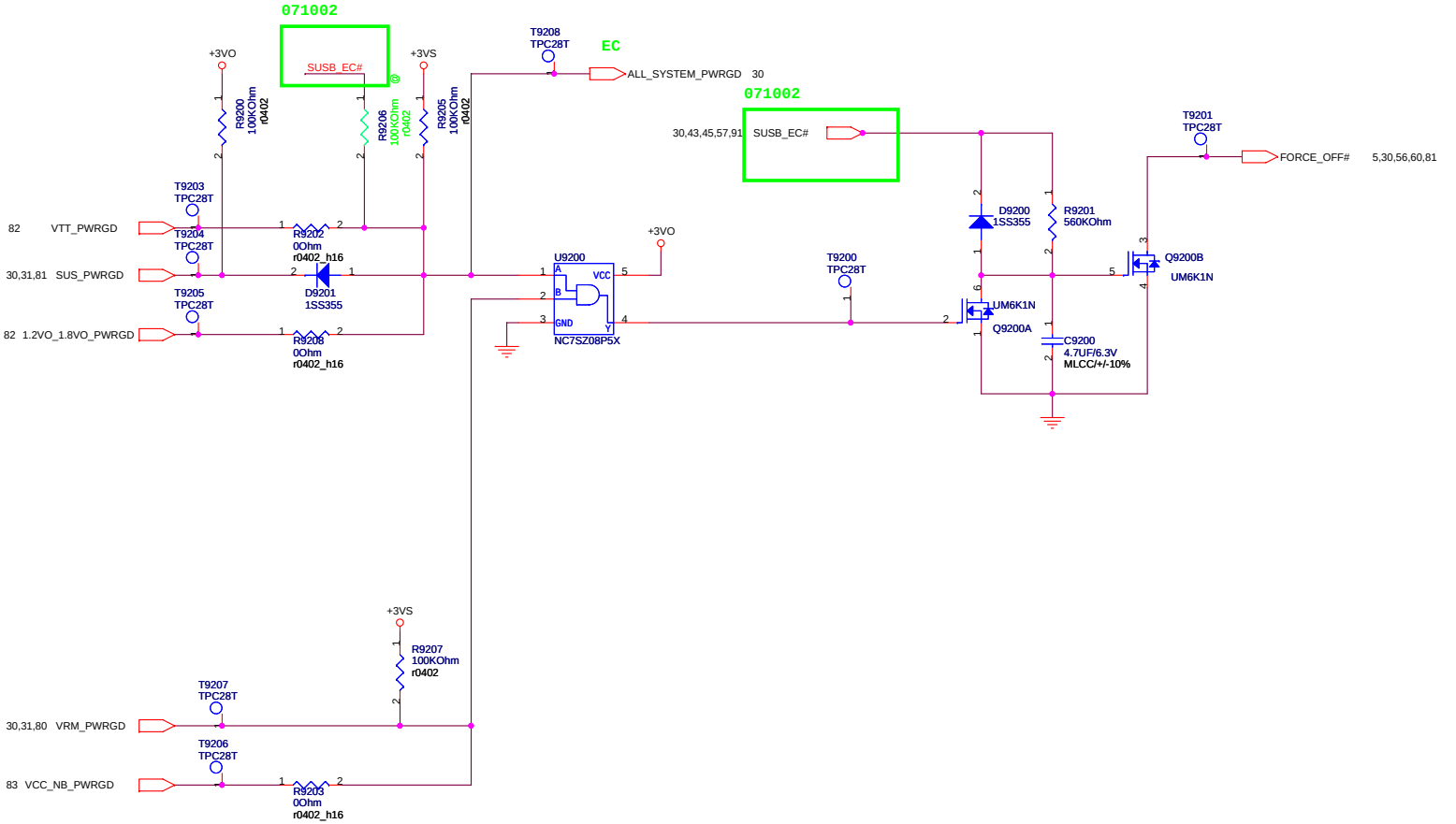


SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 91 of 94	

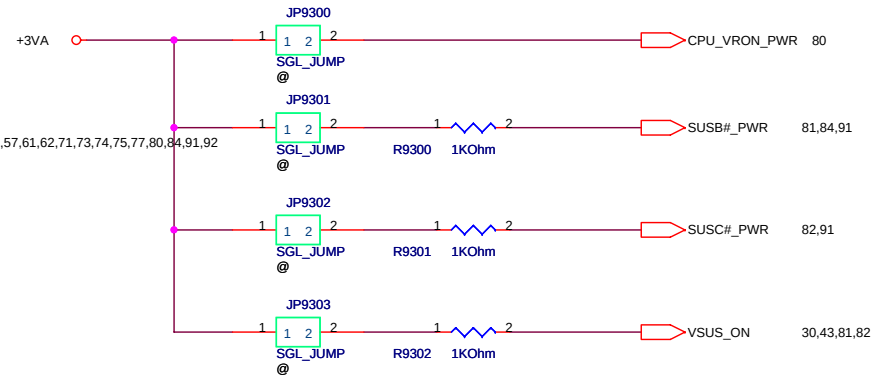
POWER GOOD DETECTER



ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: F7Z	Rev: 1.0
Date: Monday, May 19, 2008	Sheet 92 of 94	

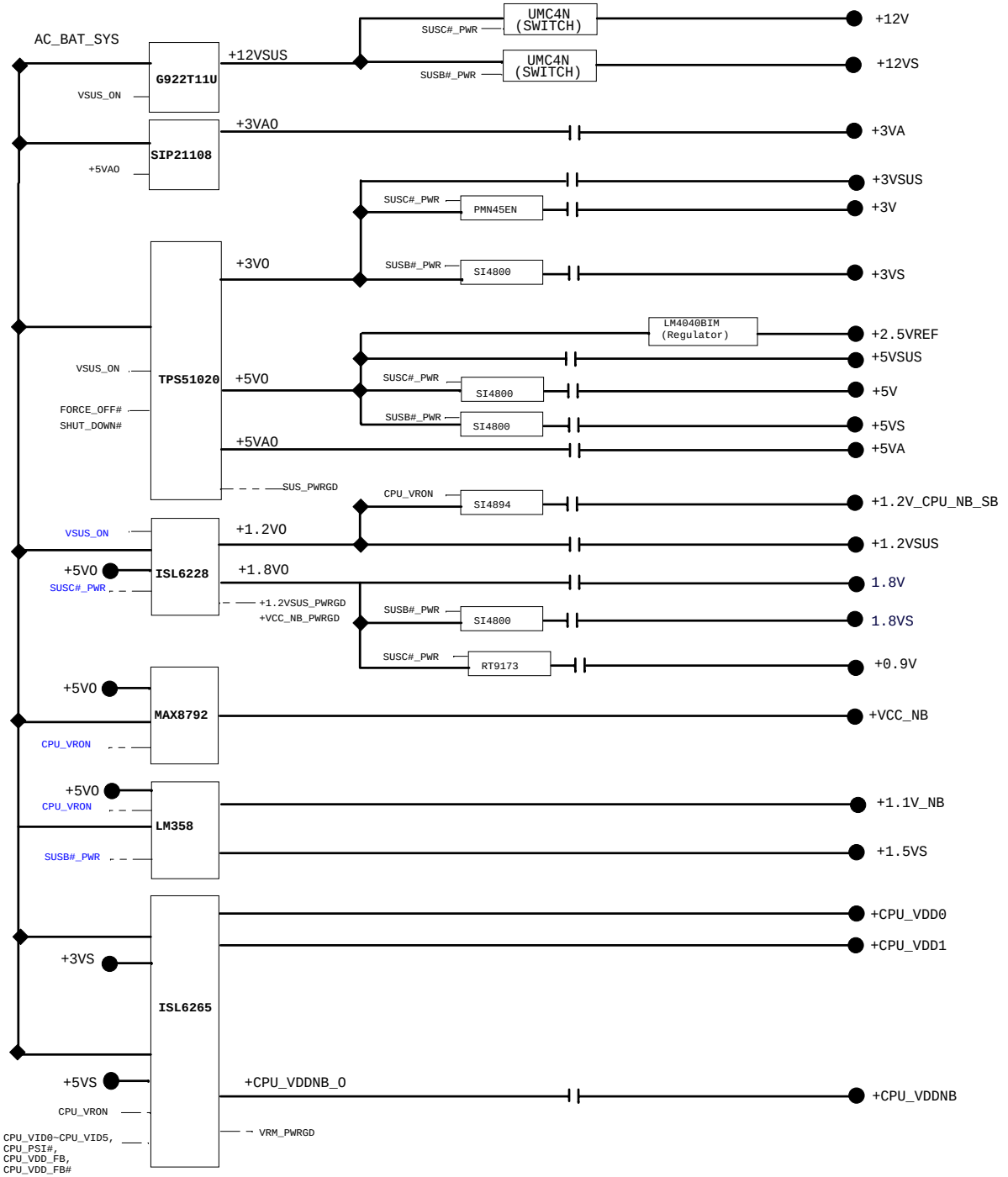
AC_BAT_SYS	AC_BAT_SYS	60,80,81,82,83,88
BAT	BAT	60,88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	82,84,88,90
+3VA	+3VA	20,30,45,56,57,61,62,81
+5VAO	+5VAO	81,84,90
+5VO	+5VO	81,82,88,90,91
+5VSUS	+5VSUS	81
+5V	+5V	44,45,52,57,91
+5VS	+5VS	23,30,31,36,37,46,50,51,57,71,80,83,91
+3VO	+3VO	56,81,91,92
+3VSUS	+3VSUS	4,20,21,22,23,24,30,33,35,37,43,53,56,80,81
+3V	+3V	30,35,44,45,53,55,57,61,62,83,91
+3VS	+3VS	5,7,8,12,13,14,21,22,23,24,29,30,31,33,36,37,43,45,46,50,51,53,55,56,57,61,62,71,73,74,75,77,80,84,91,92
+12VSUS	+12VSUS	81,84,91
+12V	+12V	37,57,75,91
+12VS	+12VS	30,45,57,71,91
+1.8VO	+1.8VO	82,84,91
+1.8V	+1.8V	4,5,6,7,8,9,57,82
+1.8VS	+1.8VS	5,12,13,14,21,57,91
+0.9V	+0.9V	4,6,9,57,82
+0.9VO	+0.9VO	82
+2.5V_CPU_VDDA	+2.5V_CPU_VDDA	5,57,84
+1.5VS	+1.5VS	43,53,55,57,84
+1.5VO	+1.5VO	84
+1.1VO	+1.1VO	84
+1.1V_NB	+1.1V_NB	12,14,57,84
+1.2VO	+1.2VO	82,84,91
+1.2VSUS	+1.2VSUS	23,82
+1.2V_CPU_NB_SB	+1.2V_CPU_NB_SB	3,14,20,22,23,57,91
+VCC_NB_O	+VCC_NB_O	83
+VCC_NB	+VCC_NB	14,57,83
+CPU_VDD0	+CPU_VDD0	6,57,80
+CPU_VDD1	+CPU_VDD1	6,57,80
+CPU_VDDNB_O	+CPU_VDDNB_O	80
+CPU_VDDNB	+CPU_VDDNB	6,57,80

FOR POWER TEST



Title : POWER_SIGNAL			
<OrgName>	Engineer:		
Size: B	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 93 of 94		

F7Z



Title : POWER_FLOWCHART			
<OrgName>	Engineer:		
Size: Custom	Project Name: F7Z		Rev: 1.0
Date: Monday, May 19, 2008	Sheet 94 of 94		