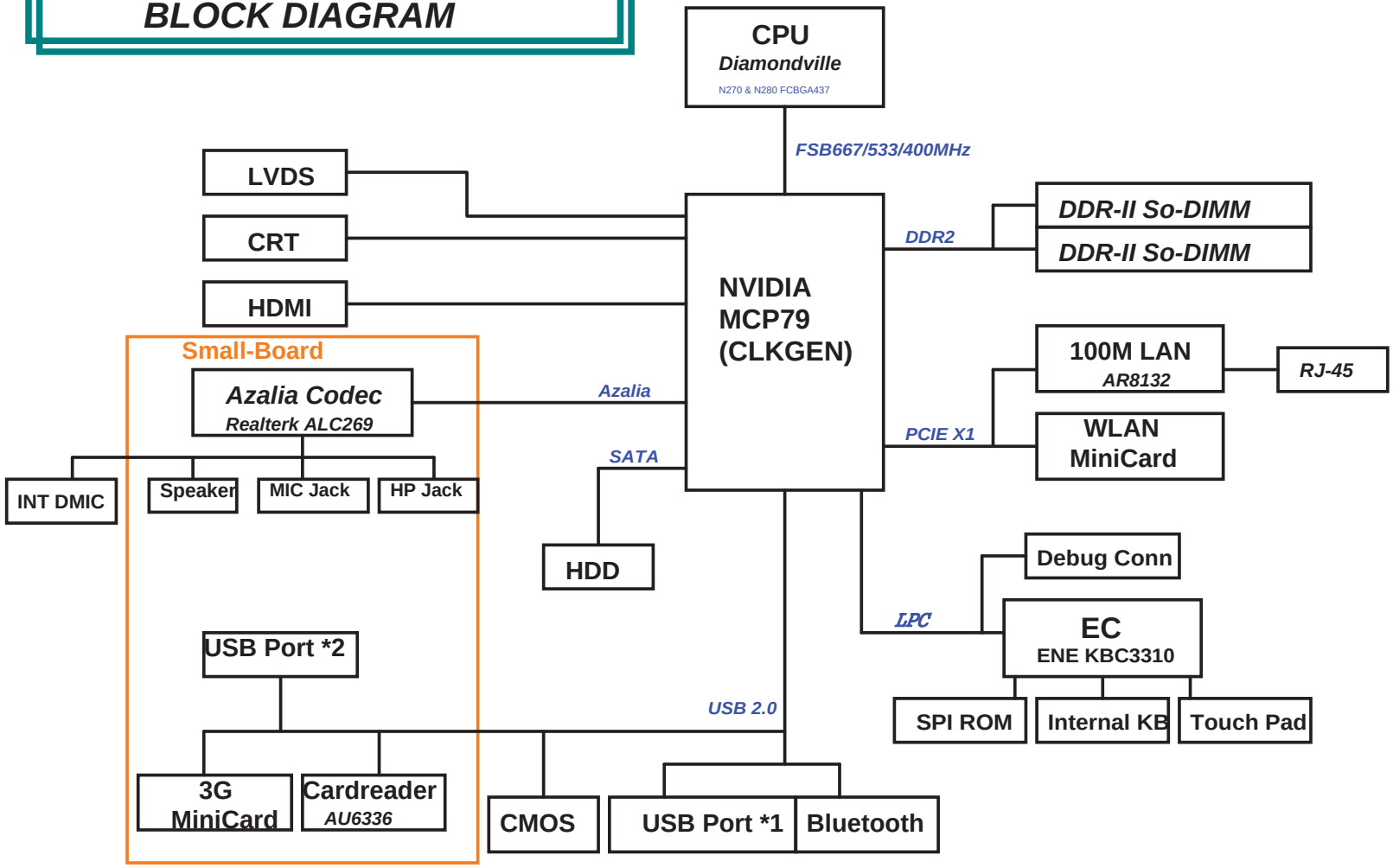
01_BLOCK DIAGRAM
02_MCP79 GPIO SETTING
03_NVIDIA_MCP79--CPU (1)
04_NVIDIA_MCP79--SATA&USB(9)
05_NVIDIA_MCP79--MISC(10)
06_NVIDIA_MCP79--HDCP&Other
07_NVIDIA_MCP79--STRAP
08_CPU-Diamondville (1)
09_CPU-Diamondville (2)
10_CPU-Diamondville (3)
11_NVIDIA_MCP79--DDR2 BUS (2)
12_NVIDIA_MCP79--MEM CONTROL(3)
13_NVIDIA_MCP79--POWER(4)
14_NVIDIA_MCP79--GND(5)
15_NVIDIA_MCP79--PCIE(6)
16_NVIDIA_MCP79--LAN(7)
17_NVIDIA_MCP79--LPC(8)
18_DDR2 SODIMM
19_DDR2_Termination
20_HDMI
21_CRT
22_LCD Conn_LID
23_3.5G
24_Mini WIFI
25_Bluetooth_BT253
26_FAN_THERMAL SENSOR
27_LAN_Atheros AR8113/AR8132
28_RJ45
29_Small brd Conn
30_EMI
31_USB Port&SATA HDD
32_EC_ENE KB3310
33_SPI ROM_Debug Conn
34_Reset Map
35_KB_Touch Pad
36_CMOS&DMIC
37_Discharge
38_PWR Jack
39_Screw Hole
40_Power Flow
41_Charger_Support JEITA
42_Power System
43_Power_1.05VSUS & VCCP
44_Power_VCORE_RT8152 Solution
45_Power_+1.8V & VTTDDR
46_Power_+1.5VS
47_Power_VDD_CORE
48_Power_Load Switch
49_Power Latch
50_BLANK
51_HISTORY
52_EC Pin Define
53_Power Sequence_DC
54_Power Sequence_AC
55_Power Sequence Description

1201I: Diamondville+MCP79 BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : Block Diagram

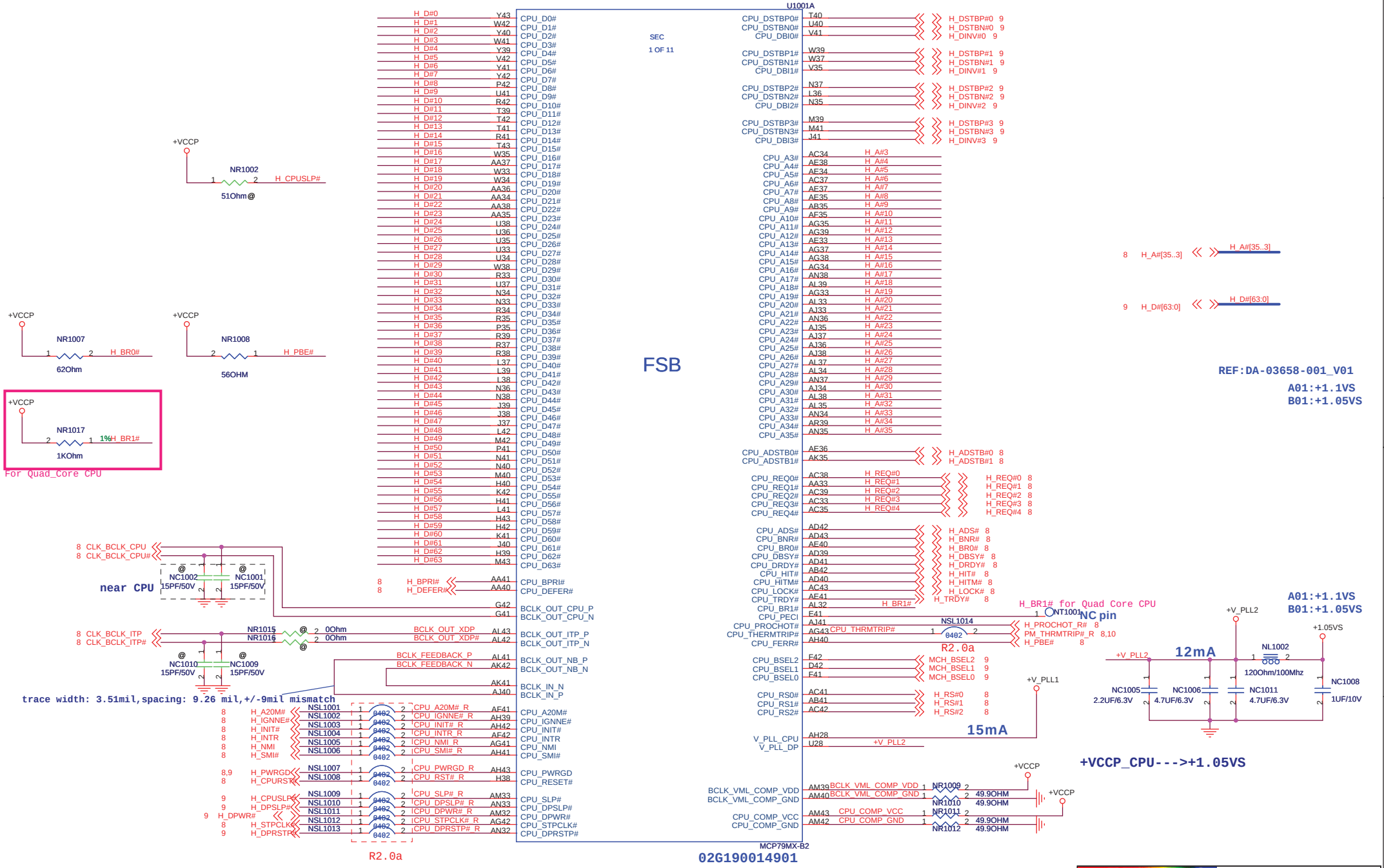
Engineer: N/A

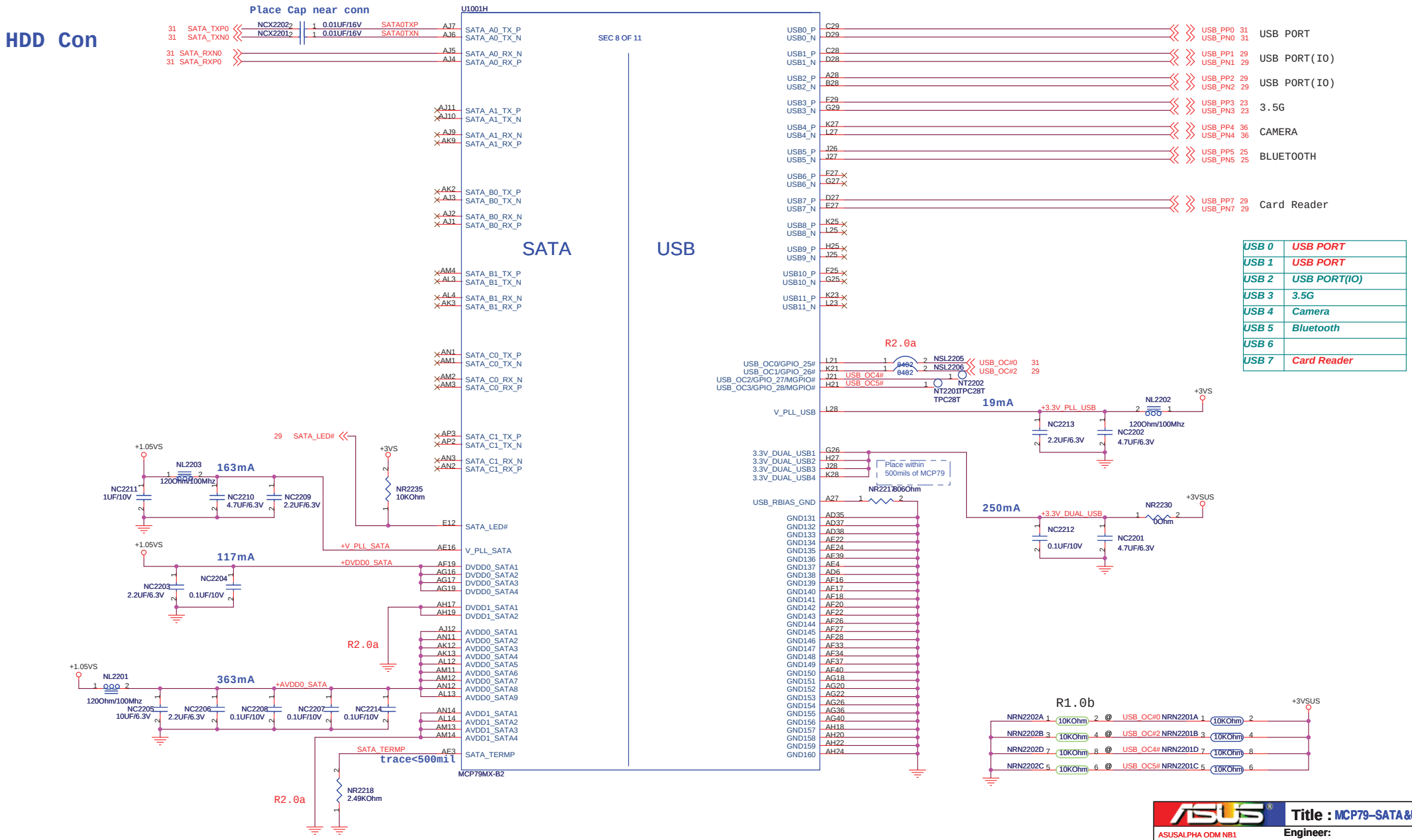
Size	Project Name	Rev
Custom	1201I	1.0

Date: Monday, July 20, 2009 Sheet 1 of 54

MCP79 GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIOSUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIOSUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N45	GPIOSUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIOSUS3/ USBCC	+VCCP_OV0	I/O CMOS3.3	Sus	VIX-unknown	OFF	output
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	CARD_READER_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F34	GPIO2	SIMCARD_IN#	I/O CMOS3.3	Core	OFF	OFF	iutput
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output


U1001A
FSB
SEC
1 OF 11
MCP79MX-B2
02G190014901
REF:DA-03658-001_V01
A01:+1.1VS
B01:+1.05VS
+VCCP_CPU--->+1.05VS
NR1002
51Ohm@
NR1007
62Ohm
NR1008
56OHM
NR1017
1KOhm
For Quad_Core CPU
near CPU
trace width: 3.51mil,spacing: 9.26 mil,+/-9mil mismatch
R2.0a
NC pin
12mA
15mA
NL1002
120Ohm/100Mhz
NC1005
2.2UF/6.3V
NC1006
4.7UF/6.3V
NC1011
4.7UF/6.3V
NC1008
1UF/10V
NC1002
15PF/50V
NC1001
15PF/50V
NC1010
15PF/50V
NC1009
15PF/50V
NR1015
NR1016
0Ohm
NR1009
NR1010
NR1011
NR1012
49.9OHM
NSL1014
0402
H_A#[35..3]
H_D#[63:0]
H_BR1# for Quad Core CPU
ASUSTeK COMPUTER INC. NB1
Engineer:
Title : MCP79 – CPU (1)
Size
Custom
Project Name
1201I
Rev
2.0g
Date: Friday, August 28, 2009
Sheet 3 of 54



USB 0	USB PORT
USB 1	USB PORT
USB 2	USB PORT(IO)
USB 3	3.5G
USB 4	Camera
USB 5	Bluetooth
USB 6	
USB 7	Card Reader

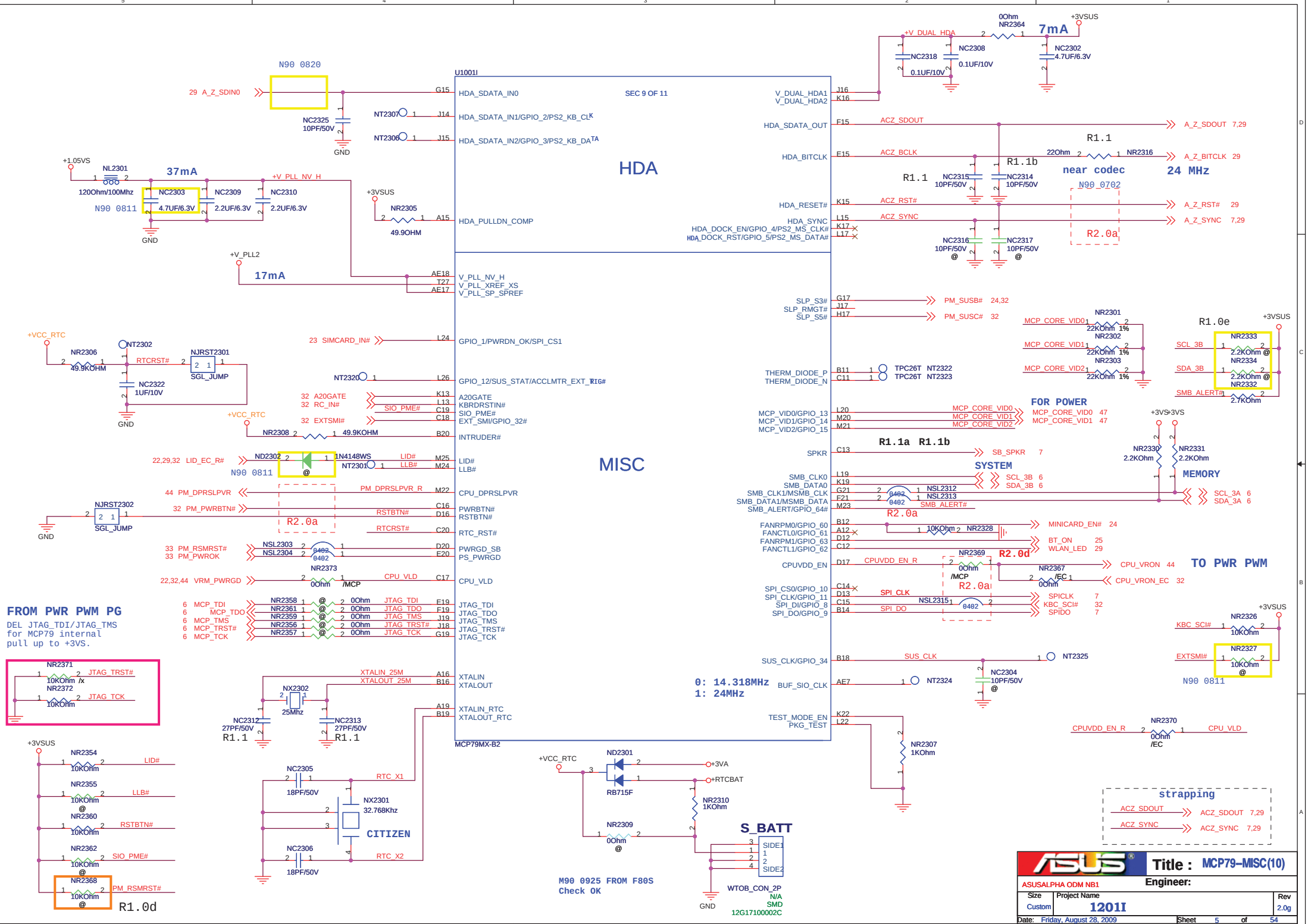
ASUSALPHA ODM NB1

Engineer:

Title : MCP79–SATA&USB(9)

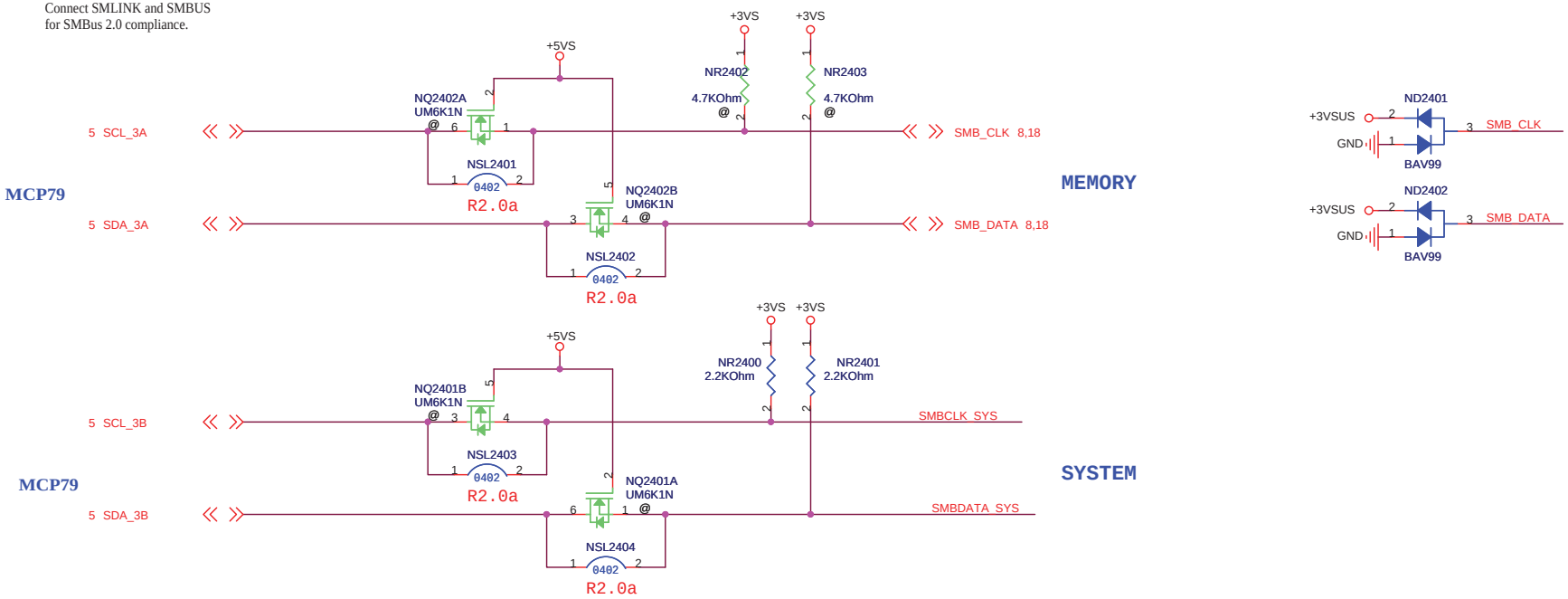
Size	Project Name	Rev
Custom	1201I	2.0g

Date: Friday, August 28, 2009 Sheet 4 of 54

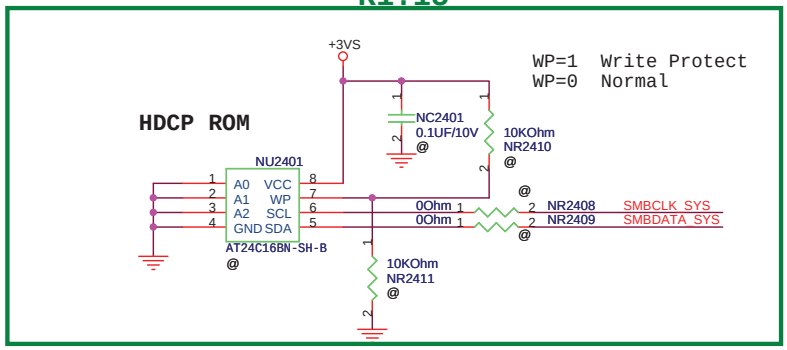


ASUSALPHA ODM NB1	Title : MCP79-MISC(10)		
	Engineer:		
Size: Custom	Project Name: 1201I		Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 5 of 54		

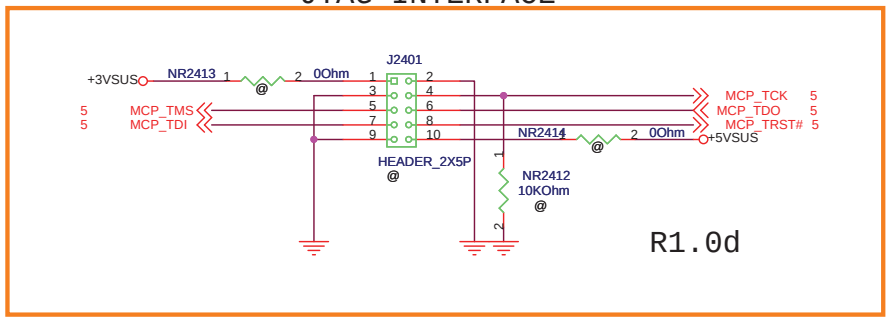
Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



R1.15



JTAG INTERFACE



ASUSTeK COMPUTER INC	Title : HDCP and Other	
	Engineer:	
Size B	Project Name 1201I	Rev 2.0g
Date: Friday, August 28, 2009	Sheet 6 of 54	

HDA_SYNC STRAP (BUF_SIO_CLK)	
0	14.318MHz (default)
1	24MHz

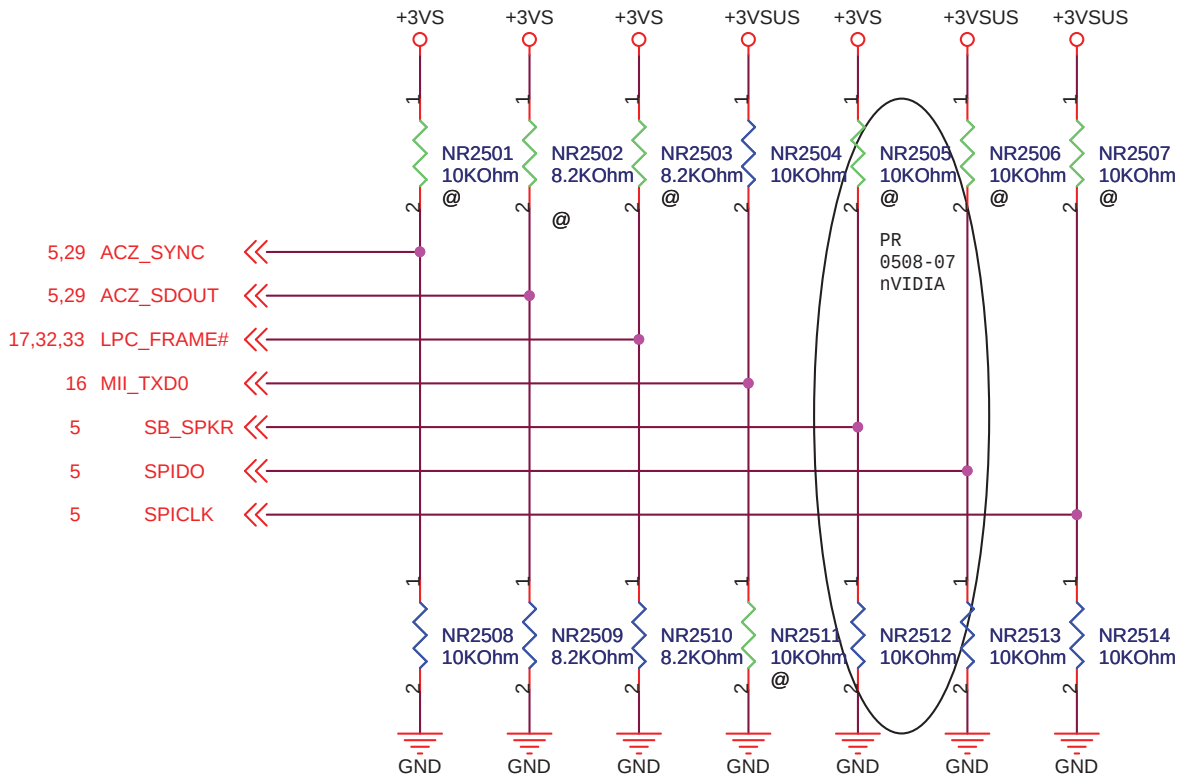
RGMII_TXD0	
0	MII
1	RGMII

SPKR	
0	User mode boot Init table
1	Safe mode boot Init table

Base on EC

HDA_SDOUT	LPC_FRAME	FUNCTION
0	0	LPC BIOS
0	1	PCI BIOS
1	0	SPI BIOS

SPI_DO	SPI_CLK	FUNCTION
0	0	31MHz
0	1	42MHz
1	0	25MHz
1	1	1MHz



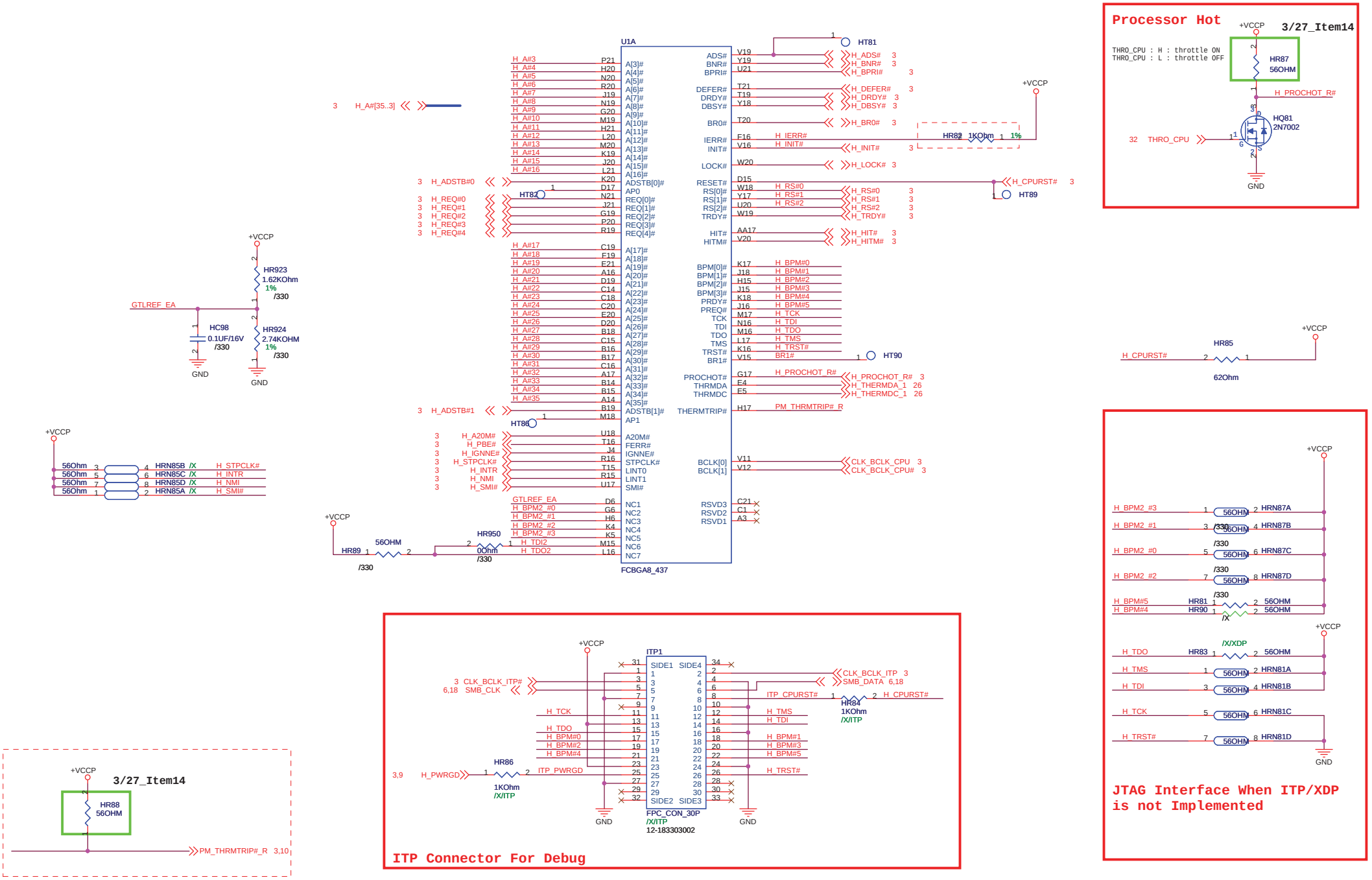
ASUSTeK COMPUTER INC. NB1

Title : MCP79 STRAP

Engineer:

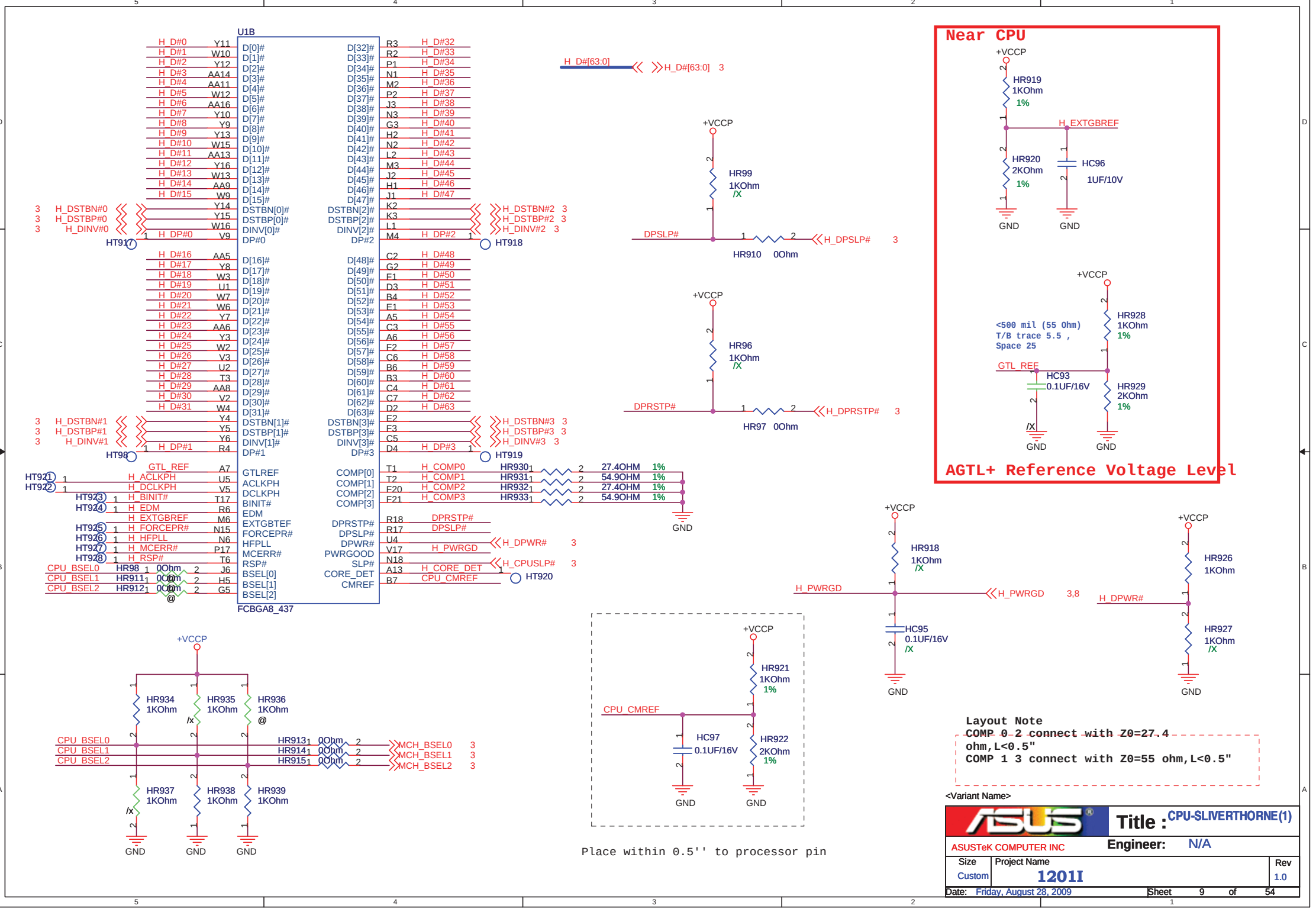
Size	Project Name	Rev
A	1201I	2.0g

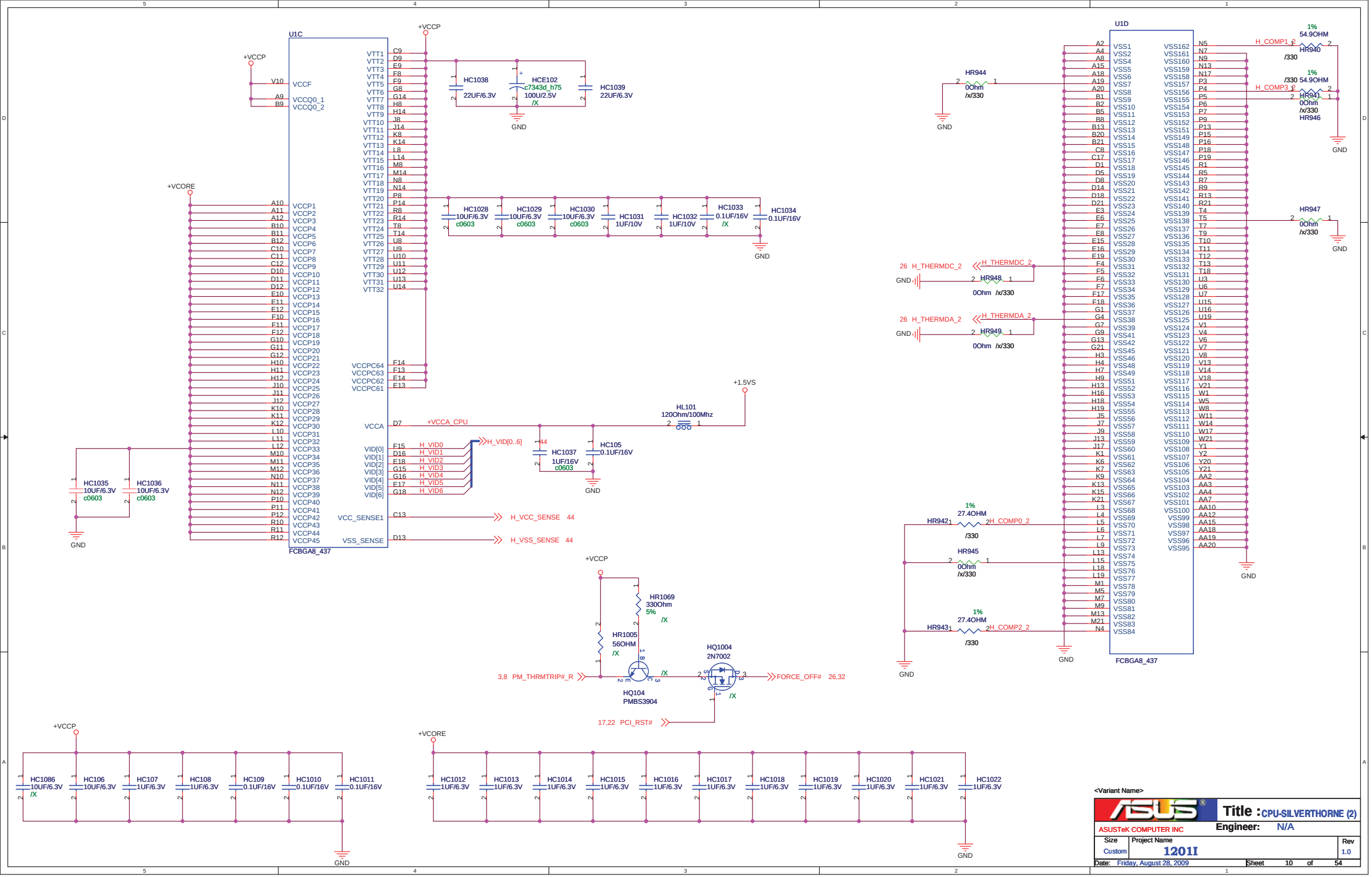
Date: Friday, August 28, 2009 Sheet 7 of 54

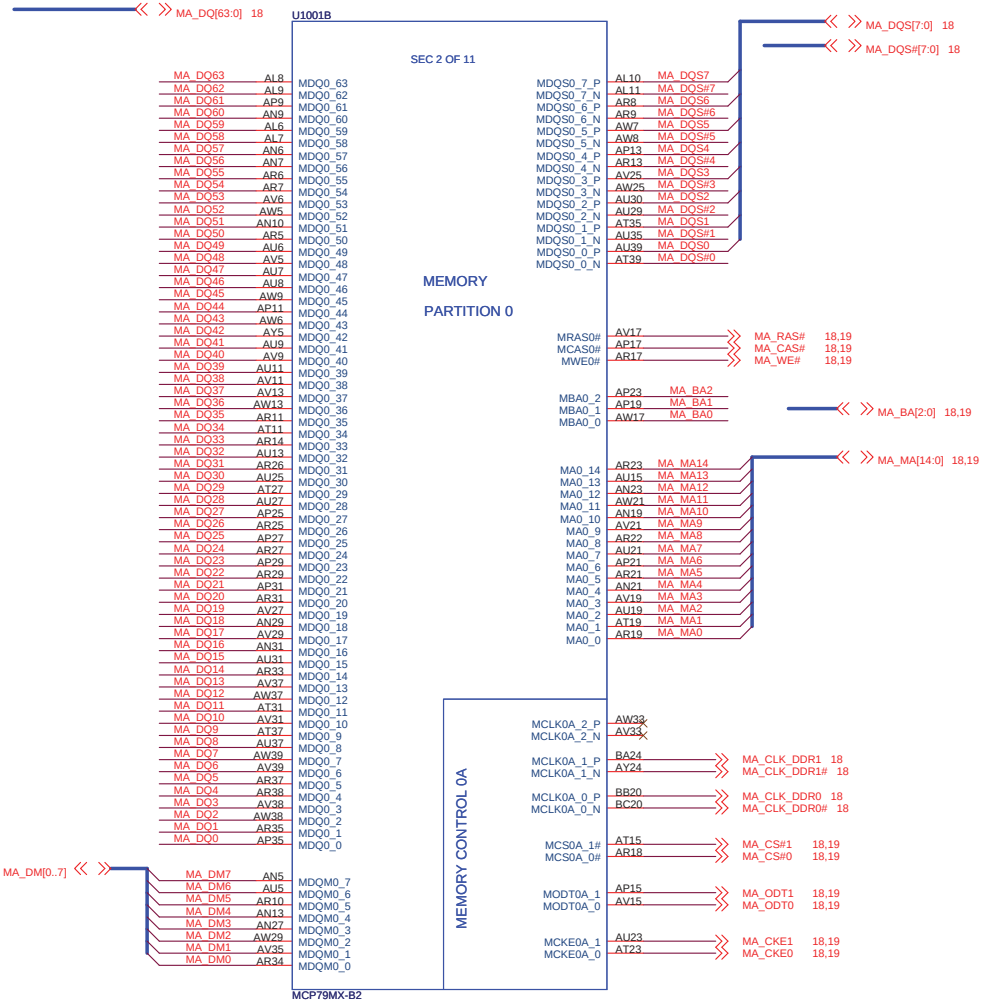


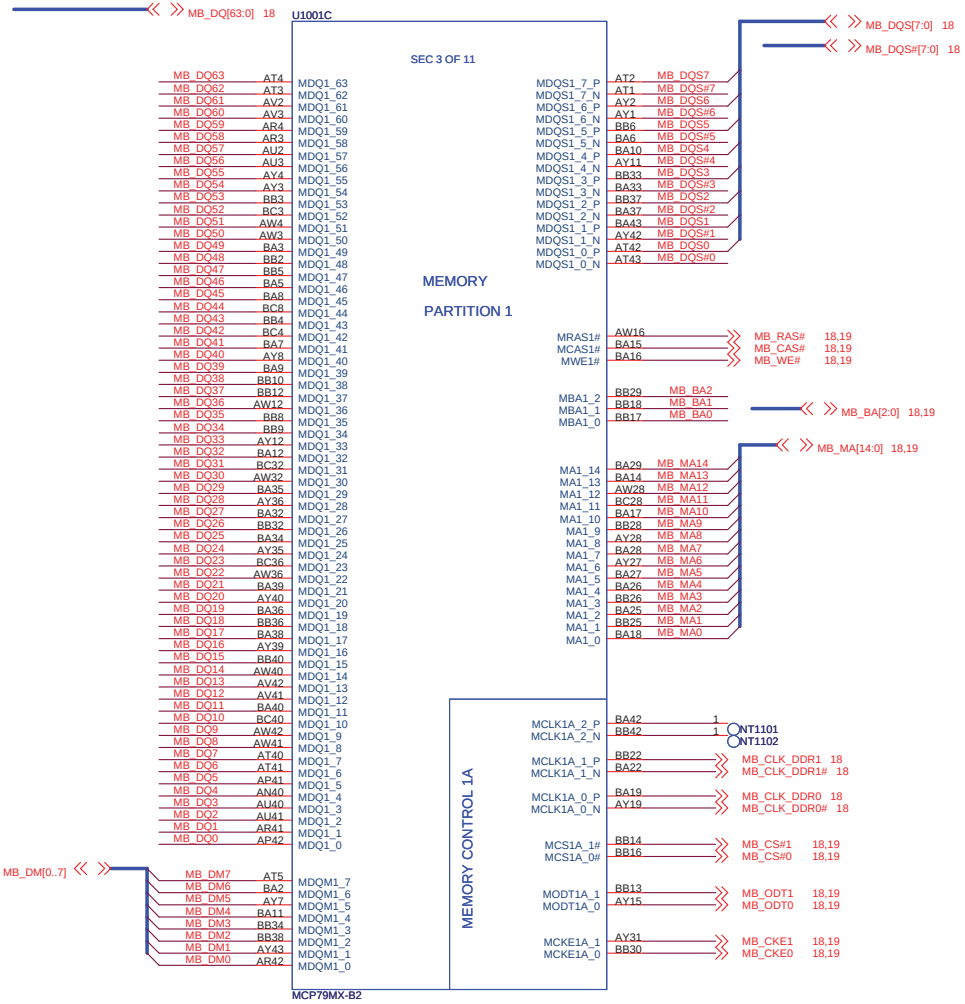
<Variant Name>

ASUSTeK COMPUTER INC	Title : CPU-SLIVERTHORNE(1)	Engineer: N/A
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Thursday, September 03, 2009	Sheet 8 of 54	

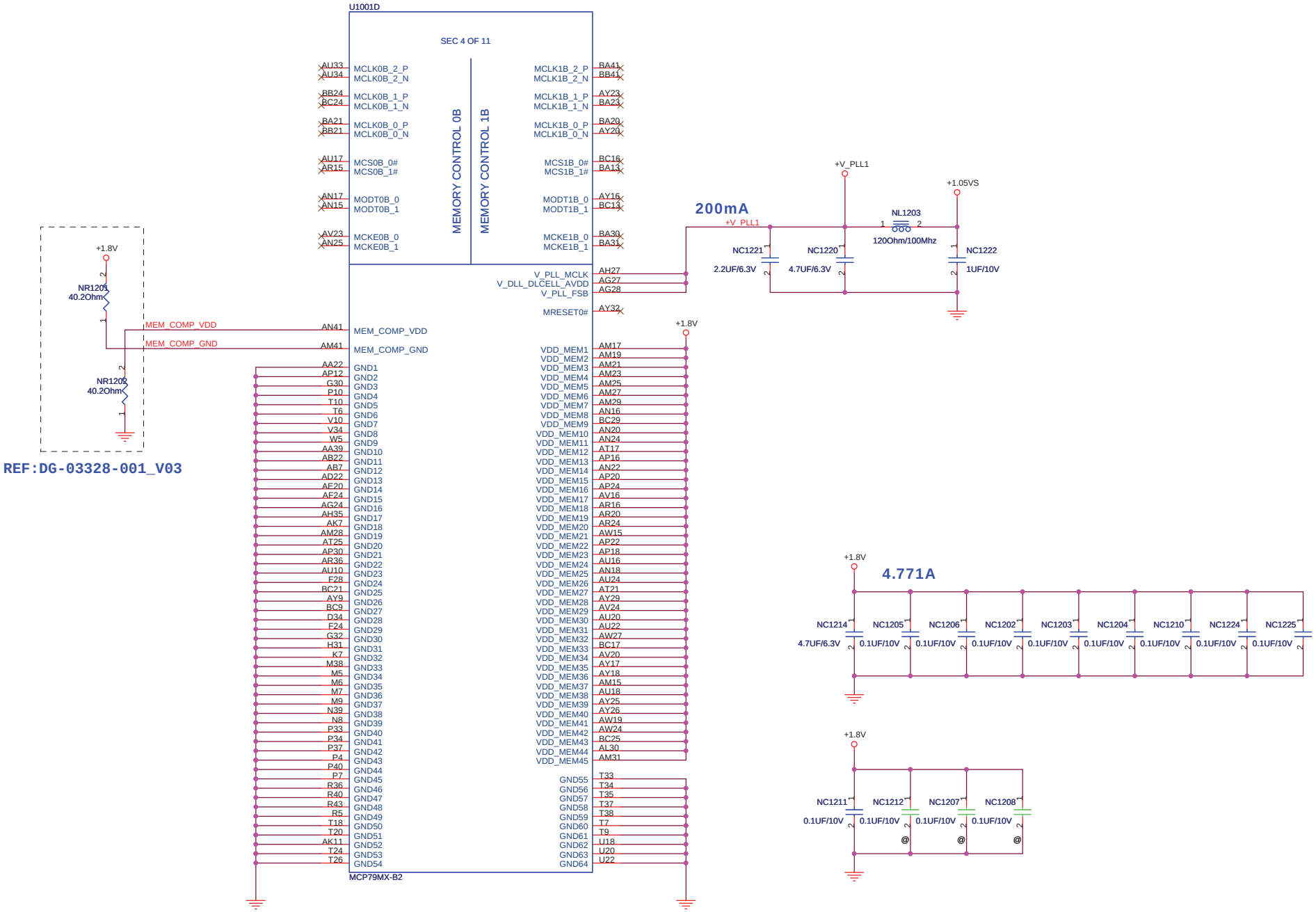

U1B
FCBGA8_437
H_D#[63:0]
H_D#[63:0] 3
H_DSTBN#0 3
H_DSTBP#0 3
H_DINV#0 3
H_DSTBN#1 3
H_DSTBP#1 3
H_DINV#1 3
H_DSTBN#2 3
H_DSTBP#2 3
H_DINV#2 3
H_DSTBN#3 3
H_DSTBP#3 3
H_DINV#3 3
HT917
HT918
HT919
HT920
HT921
HT922
HT923
HT924
HT925
HT926
HT927
HT928
GTL_REF
H_ACLKPH
H_DCLKPH
H_BINIT#
H_EDM
H_EXTGBREF
H_FORCEPR#
H_HFPLL
H_MCERR#
H_RSP#
CPU_BSEL0 HR98 0Ohm
CPU_BSEL1 HR911 0Ohm
CPU_BSEL2 HR912 0Ohm
H_COMP0 HR930 27.4OHM 1%
H_COMP1 HR931 54.9OHM 1%
H_COMP2 HR932 27.4OHM 1%
H_COMP3 HR933 54.9OHM 1%
DPRSTP#
DPSLP#
H_DPWR# 3
H_PWRGD
H_CPUSLP# 3
H_CORE_DET
CPU_CMREF
GND
+VCCP
HR99 1KOhm /X
DPSLP#
HR910 0Ohm
H_DPSLP# 3
HR96 1KOhm /X
DPRSTP#
HR97 0Ohm
H_DPRSTP# 3
Near CPU
HR919 1KOhm 1%
H_EXTGBREF
HR920 2KOhm 1%
HC96 1UF/10V
<500 mil (55 Ohm)
T/B trace 5.5 ,
Space 25
GTL_REF
HC93 0.1UF/16V
HR928 1KOhm 1%
HR929 2KOhm 1%
AGTL+ Reference Voltage Level
HR918 1KOhm /X
H_PWRGD
H_PWRGD 3,8
HC95 0.1UF/16V /X
HR926 1KOhm
H_DPWR#
HR927 1KOhm /X
HR934 1KOhm
HR935 1KOhm /x
HR936 1KOhm @
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
HR913 0Ohm
HR914 0Ohm
HR915 0Ohm
MCH_BSEL0 3
MCH_BSEL1 3
MCH_BSEL2 3
HR937 1KOhm /x
HR938 1KOhm
HR939 1KOhm
HR921 1KOhm 1%
CPU_CMREF
HC97 0.1UF/16V
HR922 2KOhm 1%
Place within 0.5'' to processor pin
Layout Note
COMP 0 2 connect with Z0=27.4 ohm,L<0.5"
COMP 1 3 connect with Z0=55 ohm,L<0.5"
<Variant Name>
Title : CPU-SLIVERTHORNE(1)
ASUSTeK COMPUTER INC
Engineer: N/A
Size Custom
Project Name 1201I
Rev 1.0
Date: Friday, August 28, 2009
Sheet 9 of 54


U1C
FCBGA8_437
U1D
FCBGA8_437
+VCCP
+VCORE
+1.5VS
GND
HC1038 22UF/6.3V
HCE102 c7343d_h75 100U/2.5V /X
HC1039 22UF/6.3V
HC1028 10UF/6.3V c0603
HC1029 10UF/6.3V c0603
HC1030 10UF/6.3V c0603
HC1031 1UF/10V
HC1032 1UF/10V
HC1033 0.1UF/16V /X
HC1034 0.1UF/16V
HC1035 10UF/6.3V c0603
HC1036 10UF/6.3V c0603
HL101 120Ohm/100Mhz
+VCCA_CPU
HC1037 1UF/16V c0603
HC105 0.1UF/16V
H_VID[0..6]
H_VCC_SENSE 44
H_VSS_SENSE 44
HR944 0Ohm /x/330
HR940 1% 54.9OHM /330
HR941 1% 54.9OHM /330
HR946 0Ohm /x/330
HR947 0Ohm /x/330
H_COMP1_2
H_COMP3_2
26 H_THERMDC_2
H_THERMDC_2
HR948 0Ohm /x/330
26 H_THERMDA_2
H_THERMDA_2
HR949 0Ohm /x/330
HR942 1% 27.4OHM /330
H_COMP0_2
HR945 0Ohm /x/330
HR943 1% 27.4OHM /330
H_COMP2_2
HR1069 330Ohm 5% /X
HR1005 56OHM /X
HQ104 PMBS3904
HQ1004 2N7002
3,8 PM_THRMTRIP#_R
FORCE_OFF# 26,32
17,22 PCI_RST#
HC1086 10UF/6.3V /X
HC106 10UF/6.3V
HC107 1UF/6.3V
HC108 1UF/6.3V
HC109 0.1UF/16V
HC1010 0.1UF/16V
HC1011 0.1UF/16V
HC1012 1UF/6.3V
HC1013 1UF/6.3V
HC1014 1UF/6.3V
HC1015 1UF/6.3V
HC1016 1UF/6.3V
HC1017 1UF/6.3V
HC1018 1UF/6.3V
HC1019 1UF/6.3V
HC1020 1UF/6.3V
HC1021 1UF/6.3V
HC1022 1UF/6.3V
<Variant Name>
Title : CPU-SILVERTHORNE (2)
ASUSTeK COMPUTER INC
Engineer: N/A
Size Custom
Project Name 1201I
Rev 1.0
Date: Friday, August 28, 2009
Sheet 10 of 54

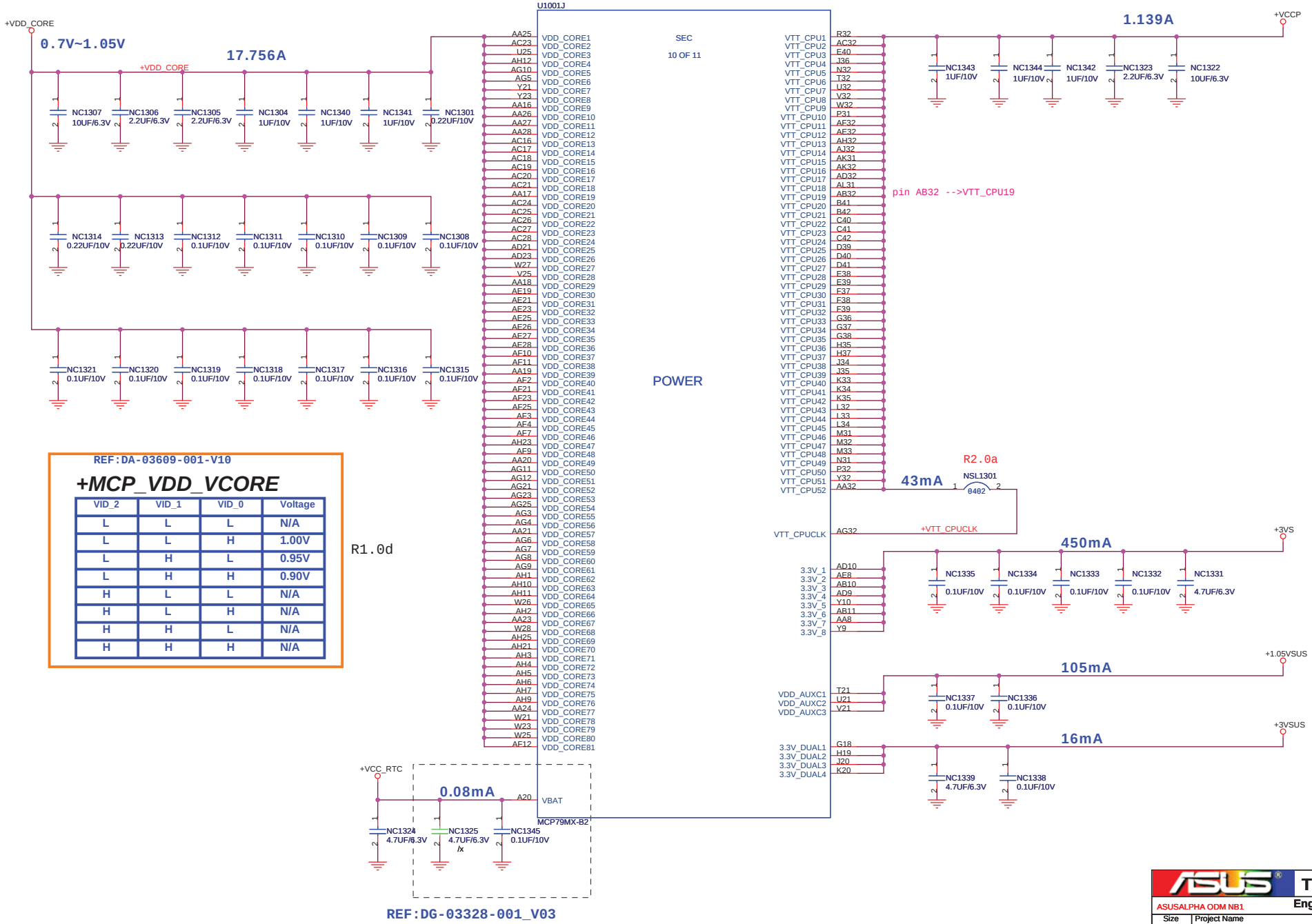




ASUSTeK COMPUTER INC. NB1	Title : MCP79-DDR2 BUS(2)		
	Engineer:		
Size: Custom	Project Name: 1201I		Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 11 of 54		



ASUSALPHA ODM NB1	Title : MCP79-MEM CNTL(3)	Engineer:
Size A3	Project Name 1201I	Rev 2.0g
Date: Tuesday, August 04, 2009	Sheet 12 of 54	



VID_2	VID_1	VID_0	Voltage
L	L	L	N/A
L	L	H	1.00V
L	H	L	0.95V
L	H	H	0.90V
H	L	L	N/A
H	L	H	N/A
H	H	L	N/A
H	H	H	N/A

ASUS

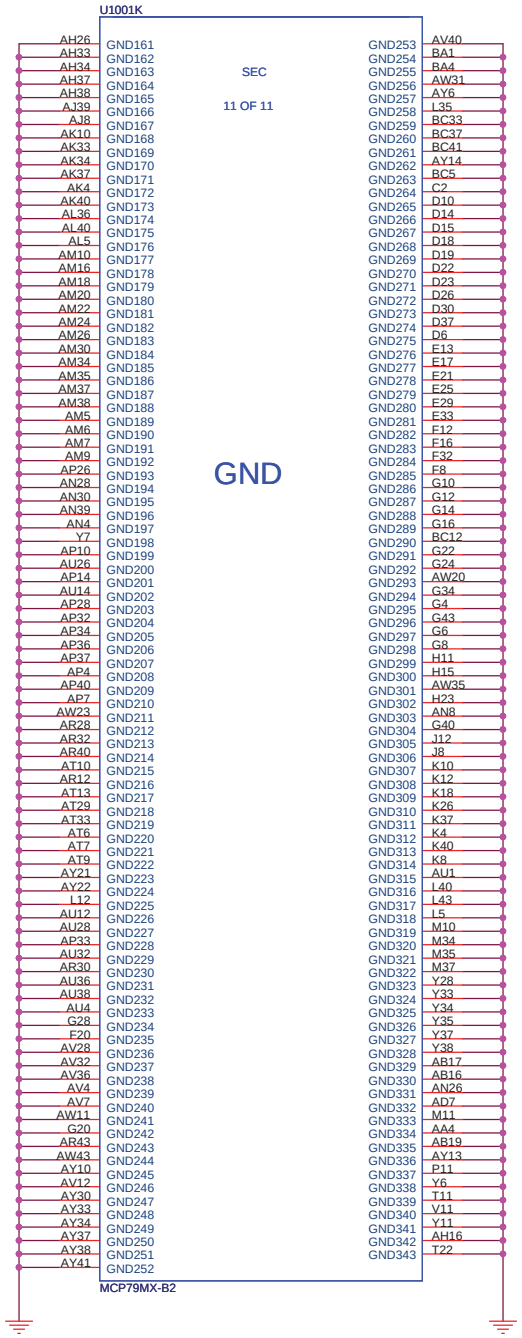
Title : MCP79–POWER(4)

ASUSALPHA ODM NB1

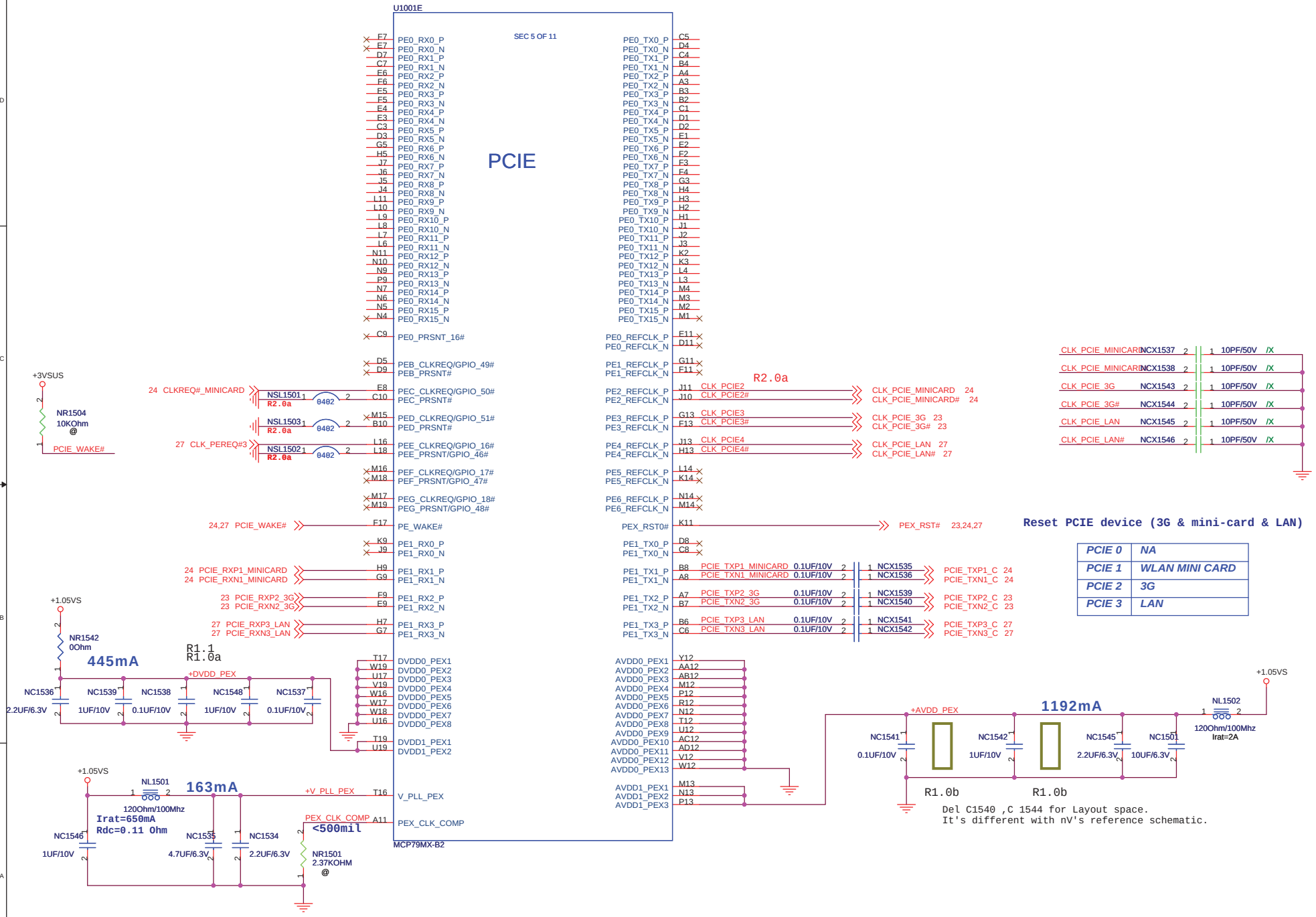
Engineer:

Size	Project Name	Rev
Custom	1201I	2.0g

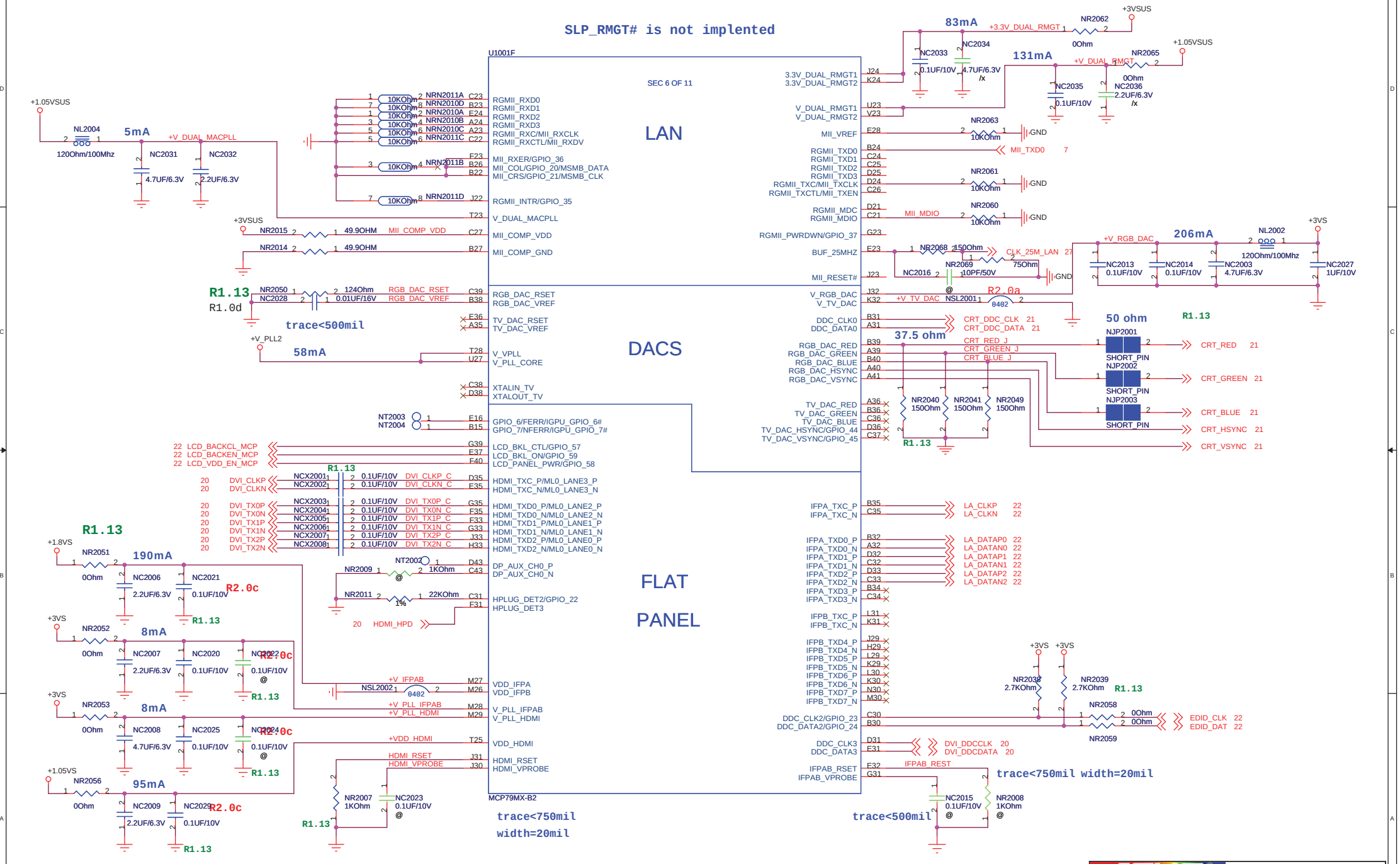
Date: Monday, August 24, 2009 Sheet 13 of 54



ASUSALPHA ODM NB1	Title : MCP79–GND(5)	Engineer:
Size A3	Project Name 1201I	Rev 2.0g
Date: Monday, July 20, 2009	Sheet 14 of 54	

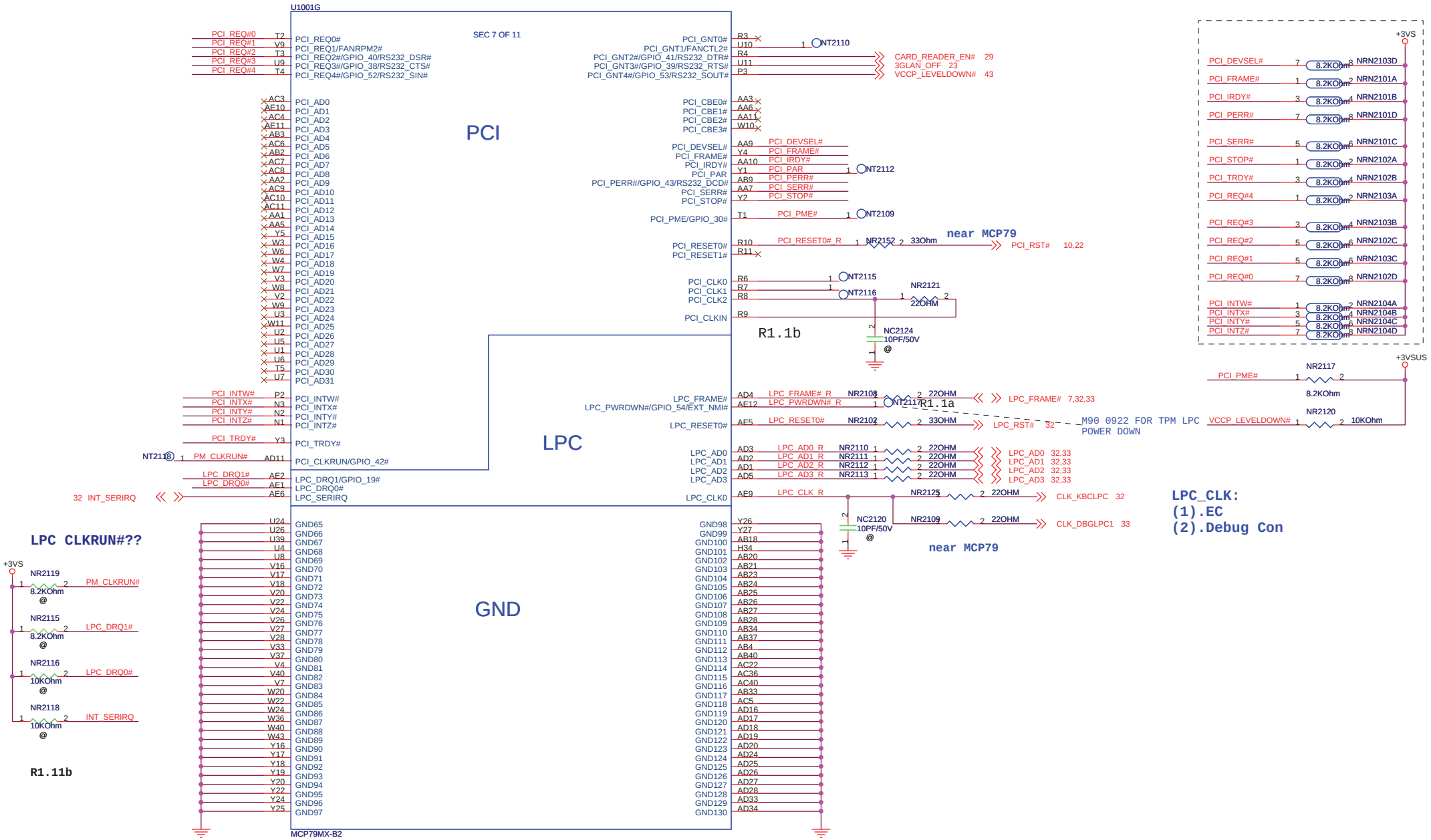


ASUS	Title : MCP79--PCI-E(6)
ASUSALPHA ODM NB1	Engineer:
Size: Custom	Project Name: 1201I
Rev: 2.0g	
Date: Friday, August 28, 2009	Sheet 15 of 54

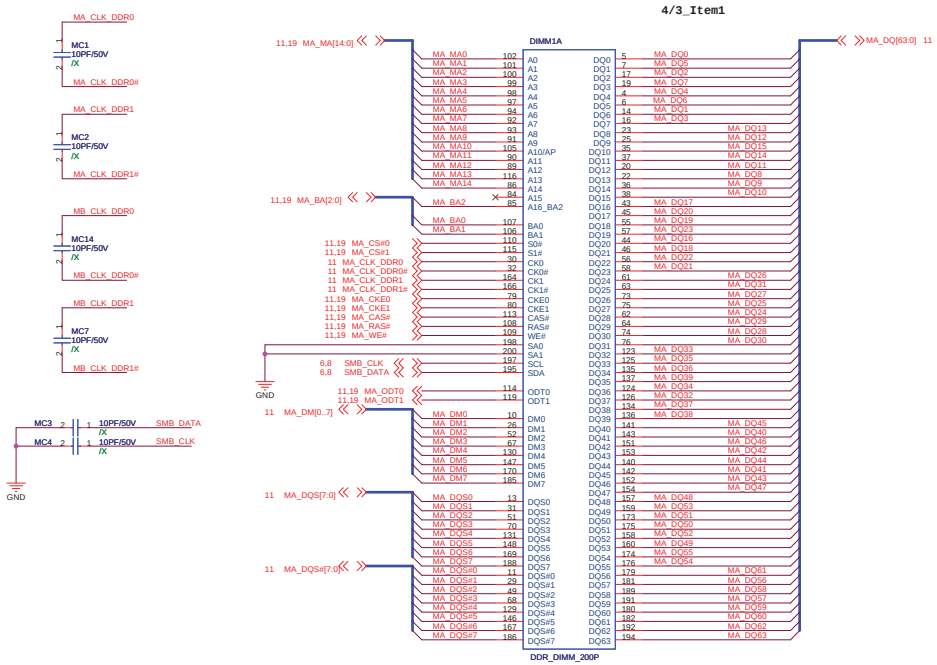


*.DO NOT SUPPORT HYBRID SLI:
Change C2013,C2019,C2021,C2022,C2029
From 0.1uF/10V to 0 ohm to GND.

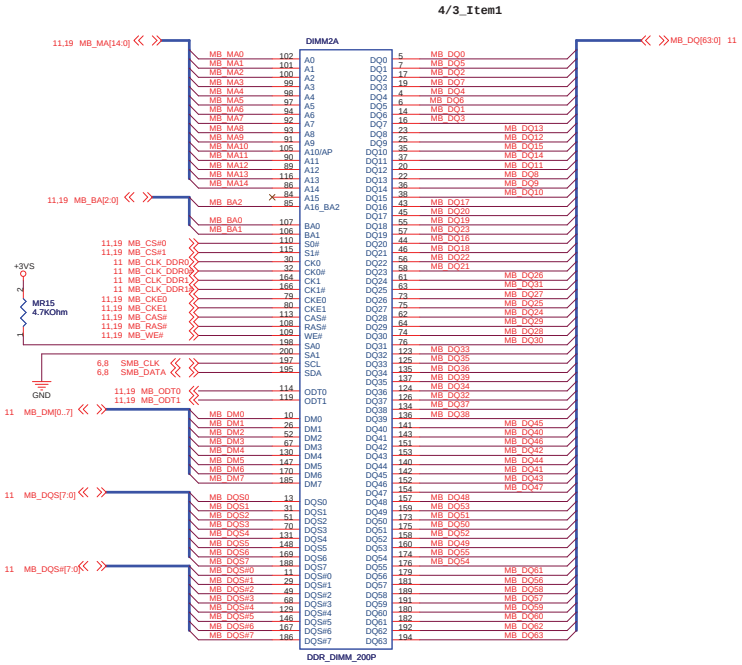
ASUS	Title : MCP79--LAN (7)	
ASUSALPHA ODM NB1	Engineer:	
Size A3	Project Name 1201I	Rev 2.0g
Date: Wednesday, September 02, 2009	Sheet 16 of 54	



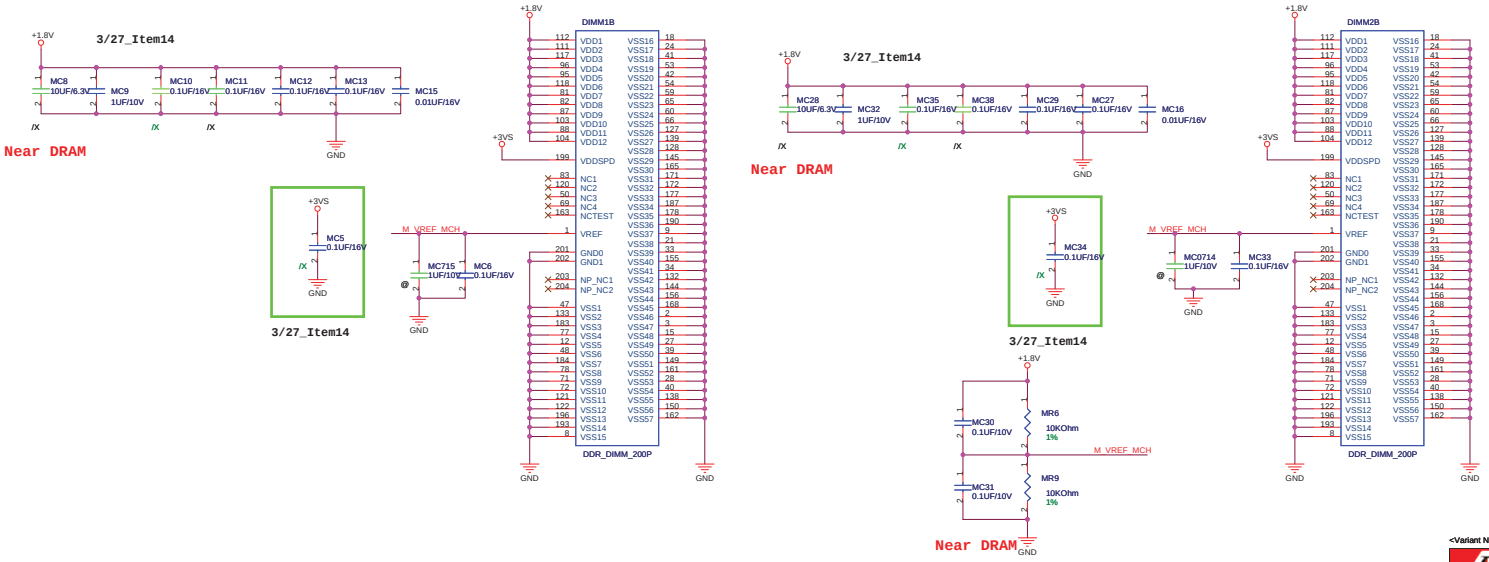
ASUSALPHA ODM NB1	Title : MCP79--LPC (8)	Engineer:
Size A3	Project Name 1201I	Rev 2.0g
Date: Friday, August 28, 2009	Sheet 17 of 54	



DDR10. slot Symbol use 12G02533200E
STD TYPE



DDR10. slot Symbol use 12G02533200D
REV TYPE

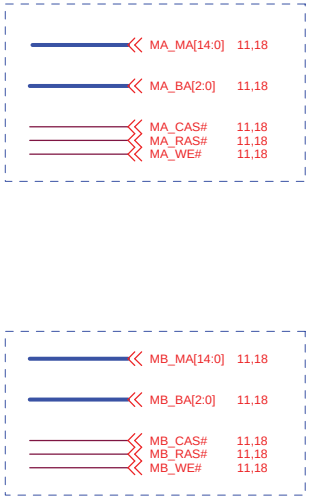


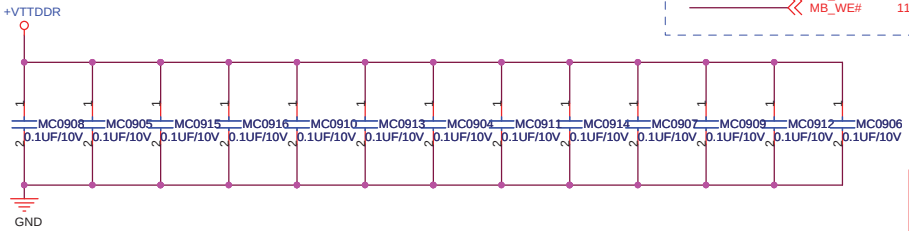
+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve STR_EN# and SUSC#

HAS TO BE SWAPED

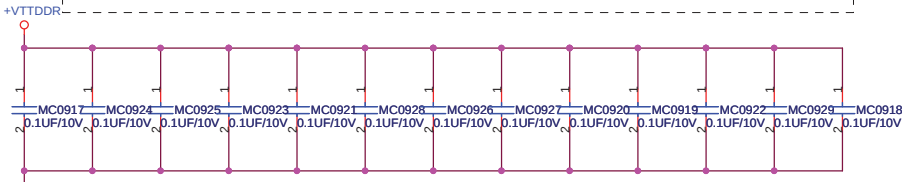
M_A_A14 is reserved signal and keep R0901 separately

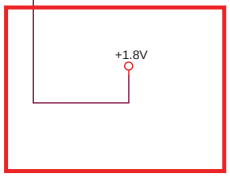
Don't include this page into DesignIP because of swapping





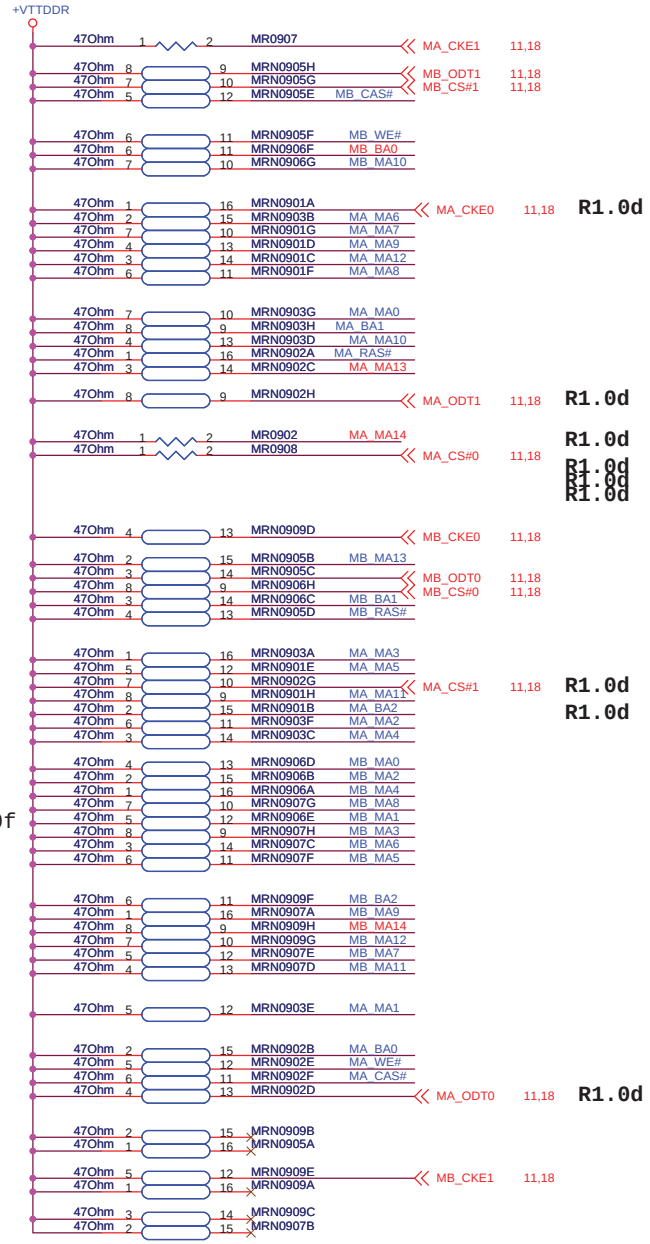
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



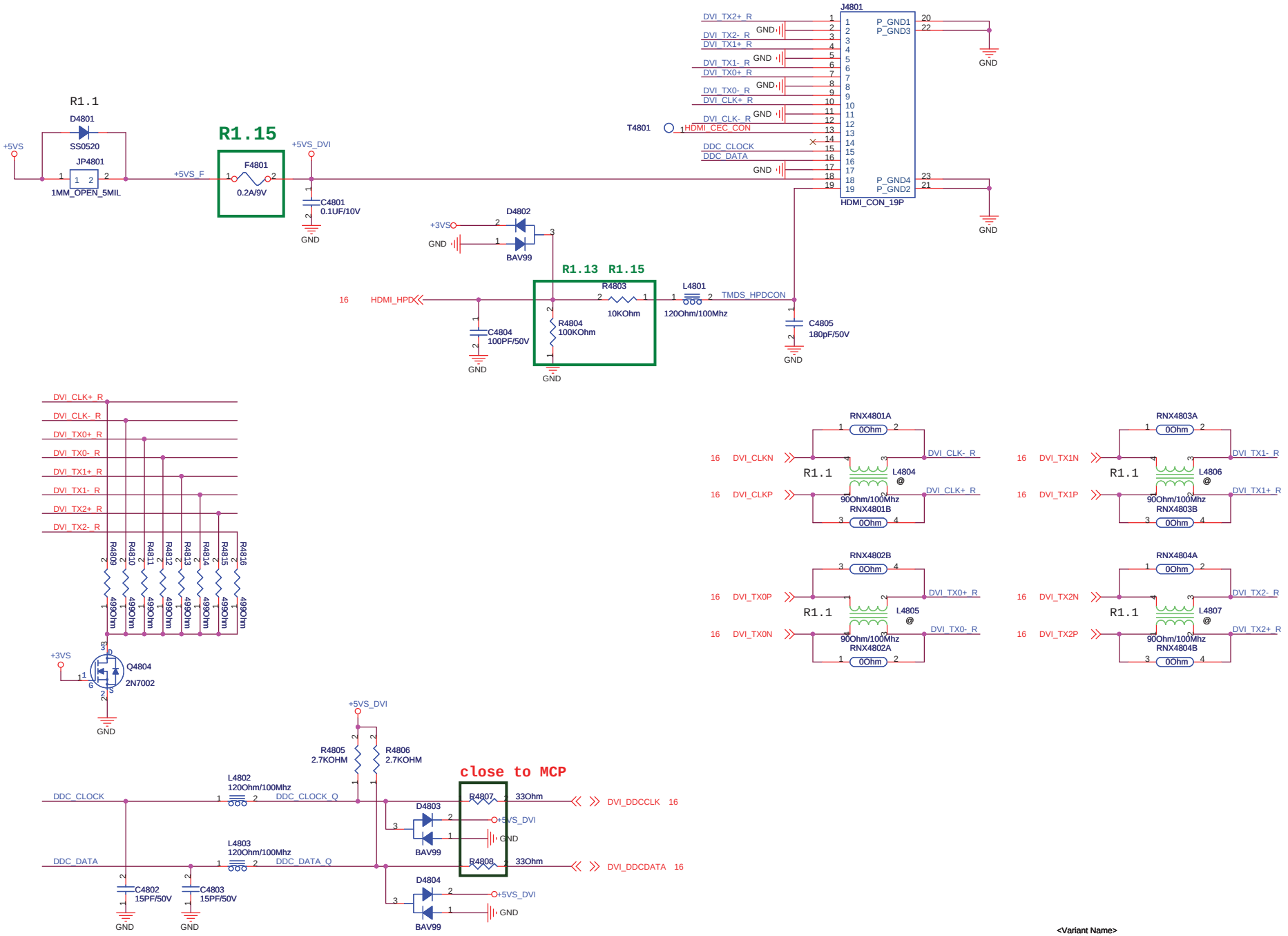


16X0.1UF to GND

16X0.1UF to 1.8V

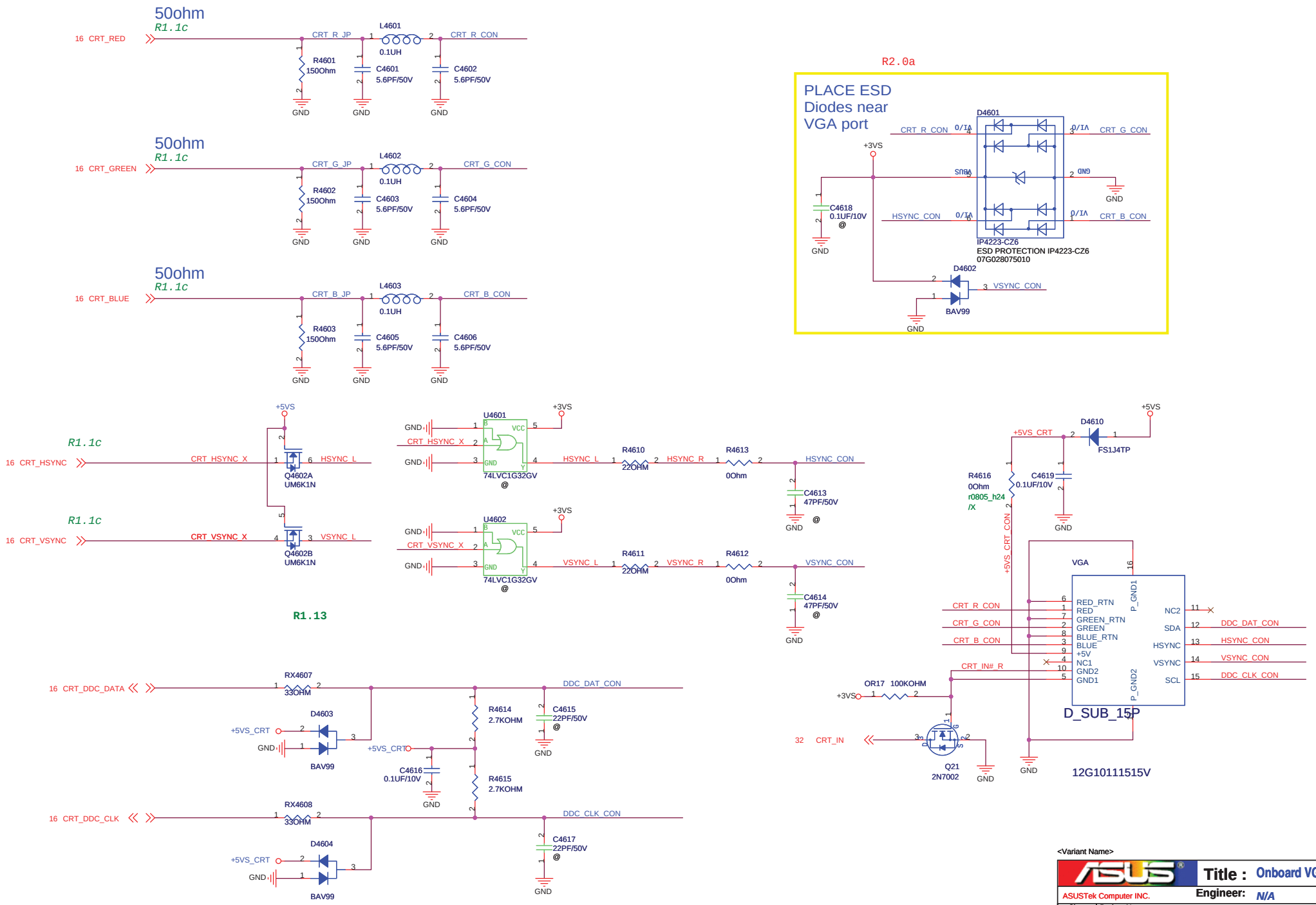


ASUSTeK COMPUTER INC	Title : DDR2 TERM	
	Engineer:	
Size: Custom	Project Name: 1201I	Rev: 2.0g
Date: Friday, August 28, 2009	Sheet 19 of 54	



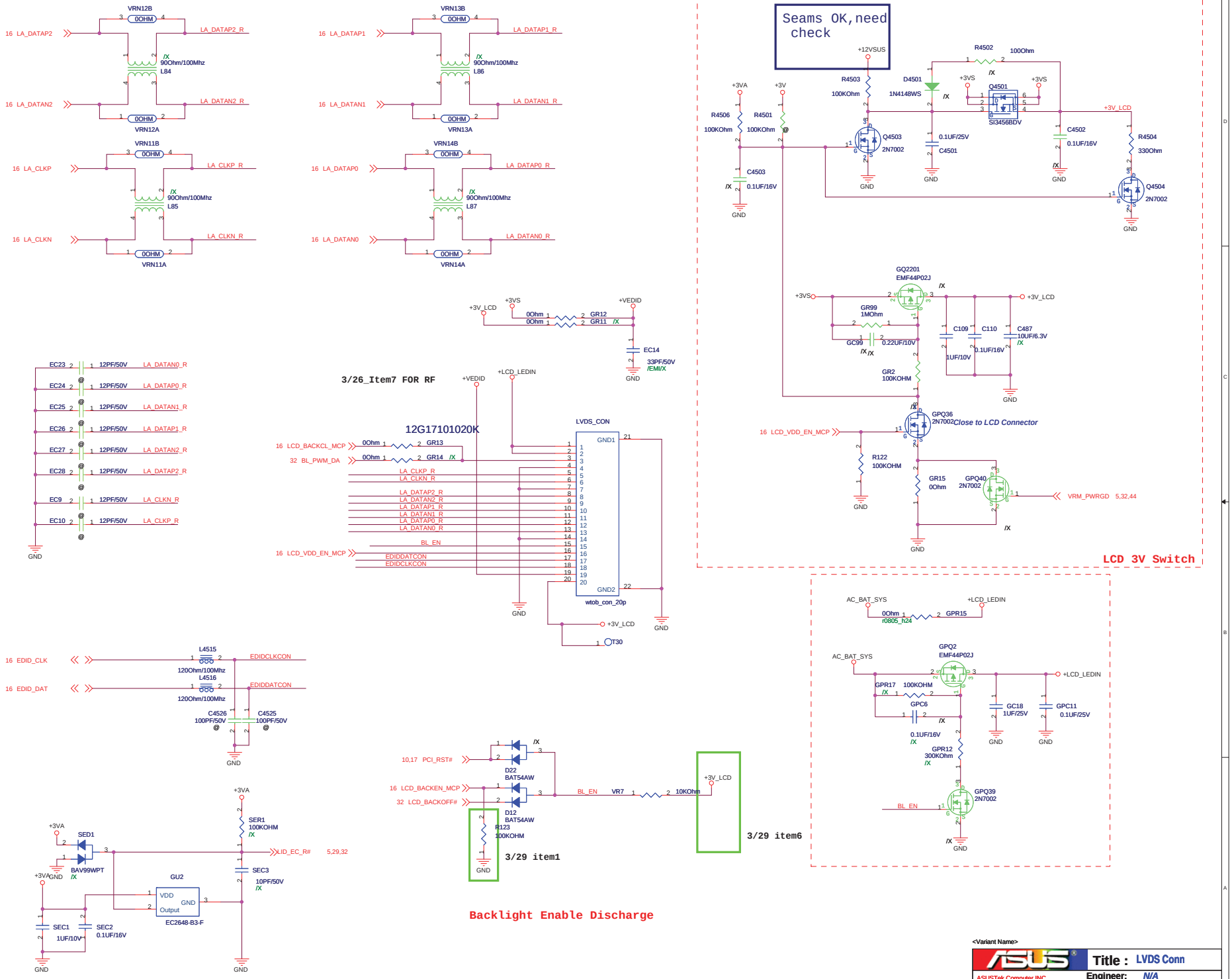
<Variant Name>

ASUSTek COMPUTER INC	Title : CH7317_SDVO_CRT	Engineer: N/A
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 20 of 54	



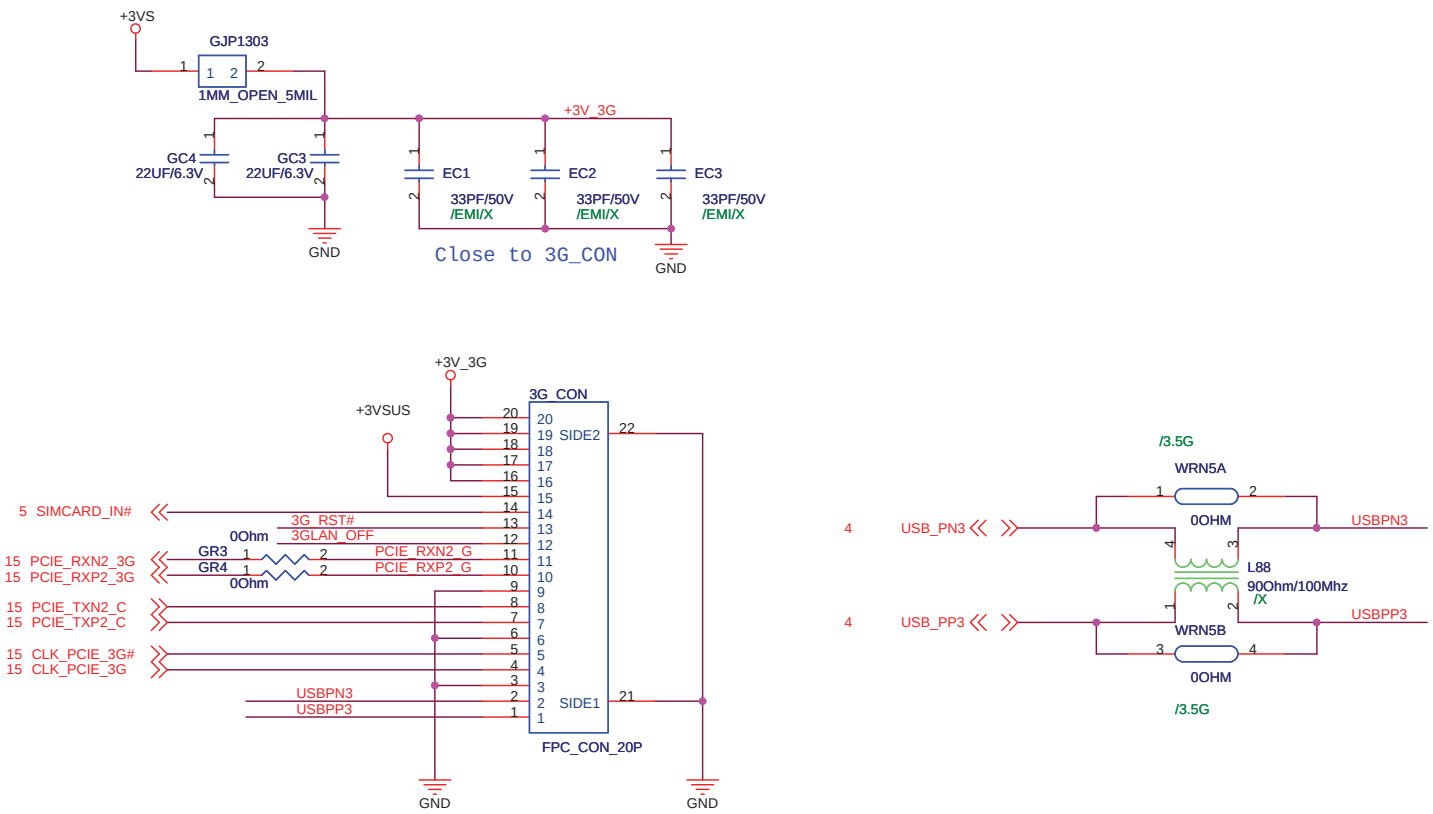
<Variant Name>

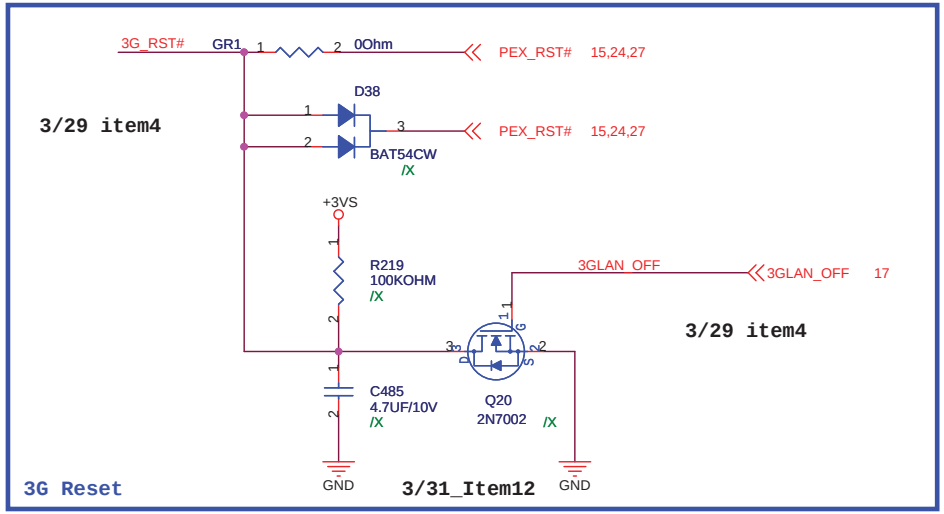
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 21 of 54	



<Variant Name>

ASUS	Title : LVDS Conn	
ASUSTek Computer INC.	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 22 of 54	





<Variant Name>

3.5G Module & External Antenna

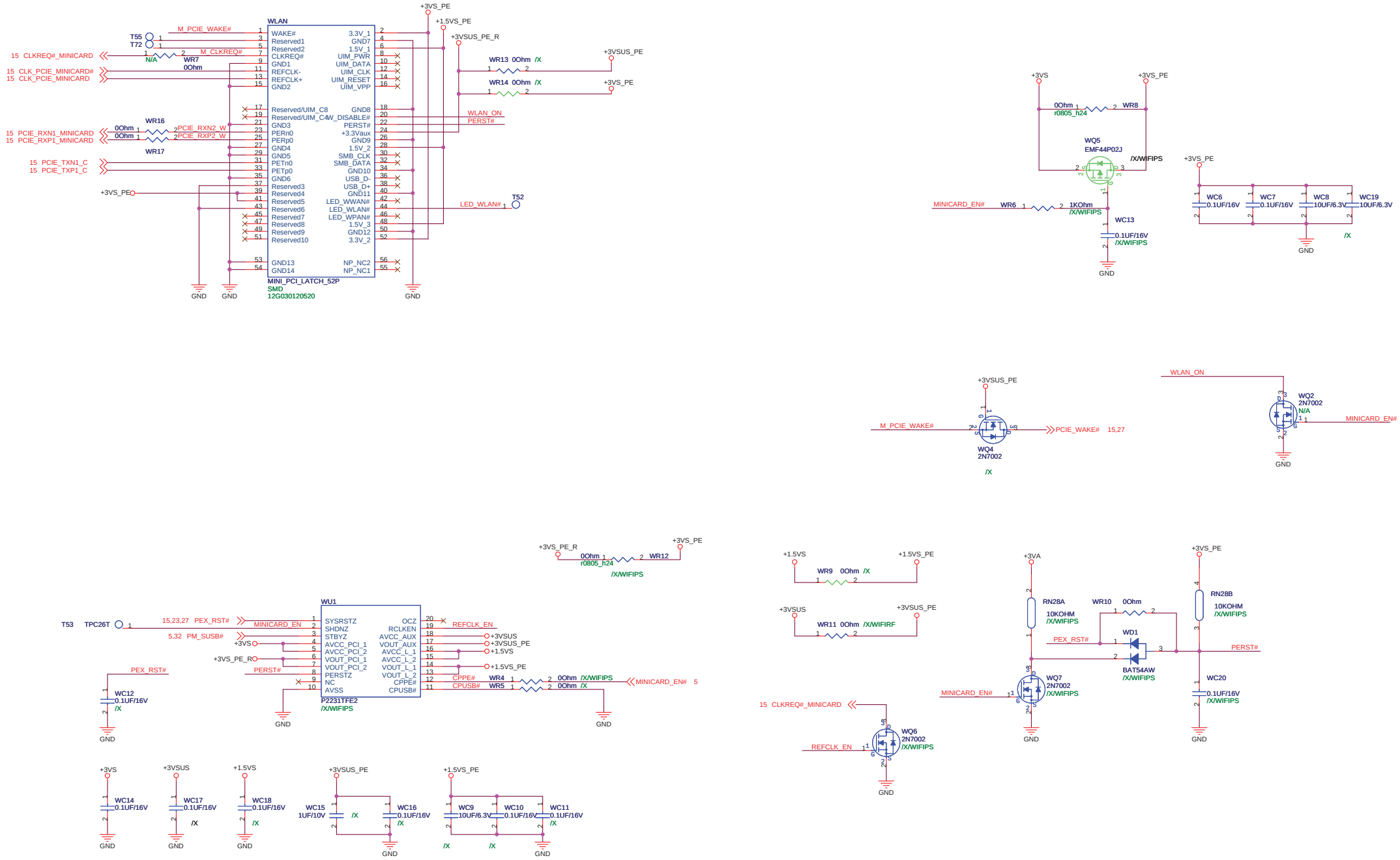
ASUSTek Computer INC.

Title :

Engineer: N/A

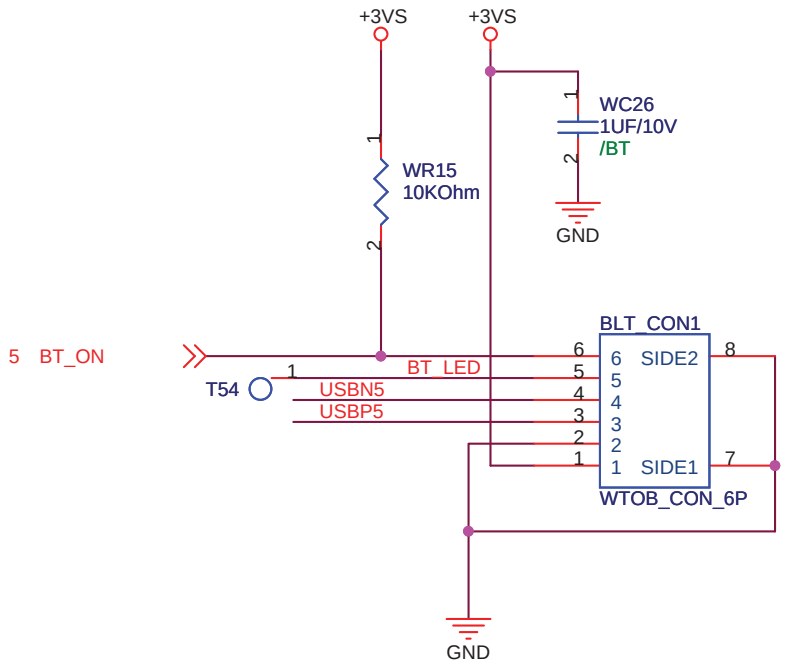
Size	Project Name	Rev
Custom	1201I	1.0

Date: Friday, August 28, 2009 Sheet 23 of 54

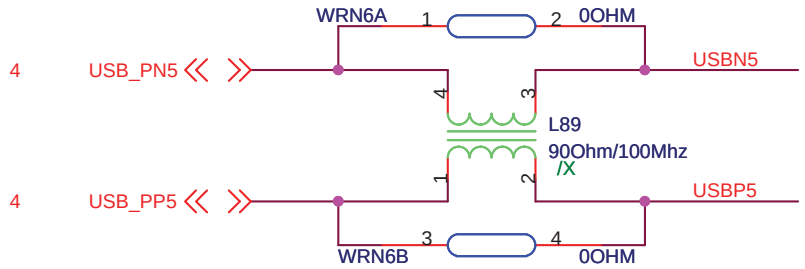


<Variant Name>

ASUSTek Computer INC.	Title : Mini WIFI	
	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Friday, August 28, 2009	Sheet 24 of 54	

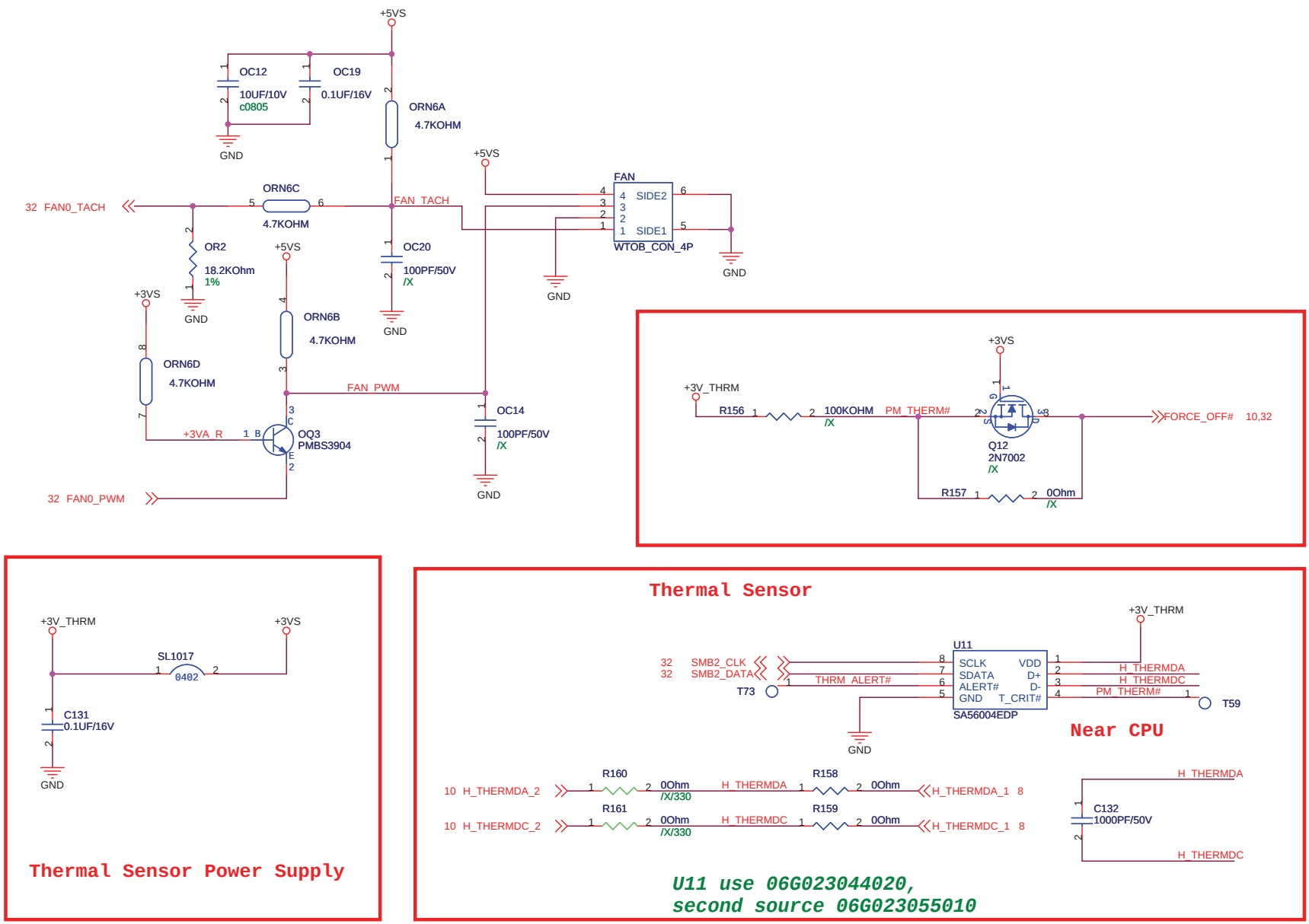


BT Conn



<Variant Name>

ASUS	Title : Bluetooth	
ASUSTek Computer INC.	Engineer: N/A	
Size A	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 25 of 54	

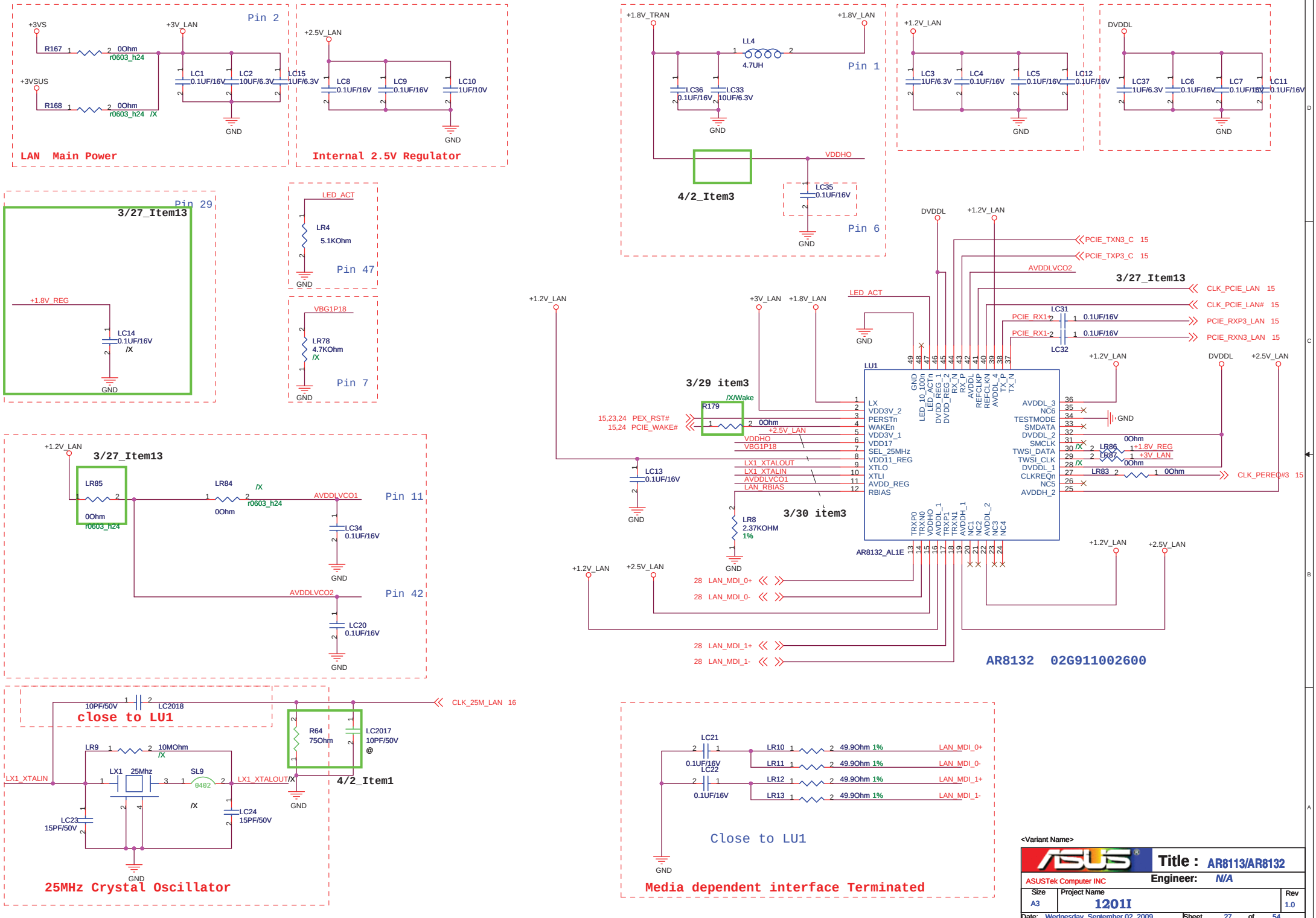


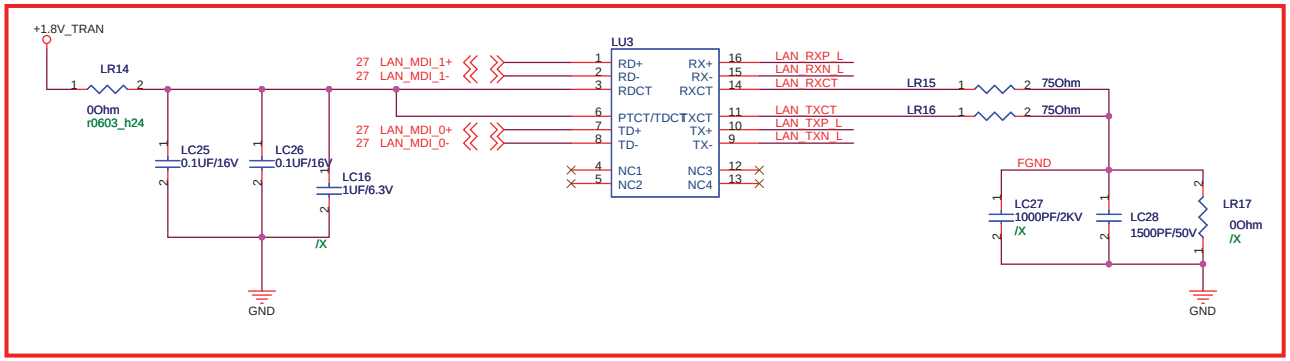
Thermal Sensor Power Supply

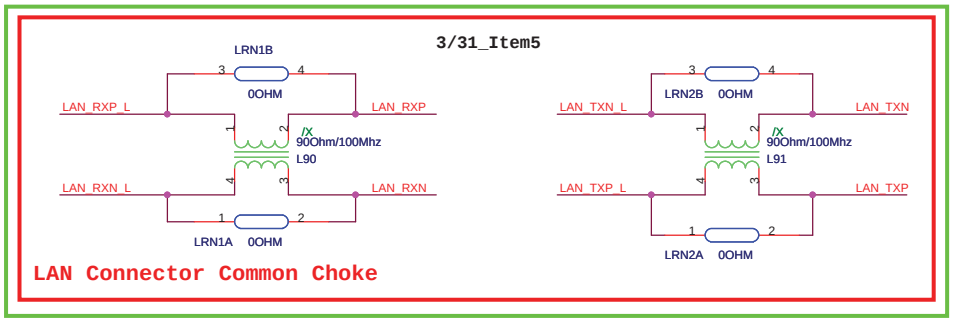
U11 use 06G023044020,
second source 06G023055010

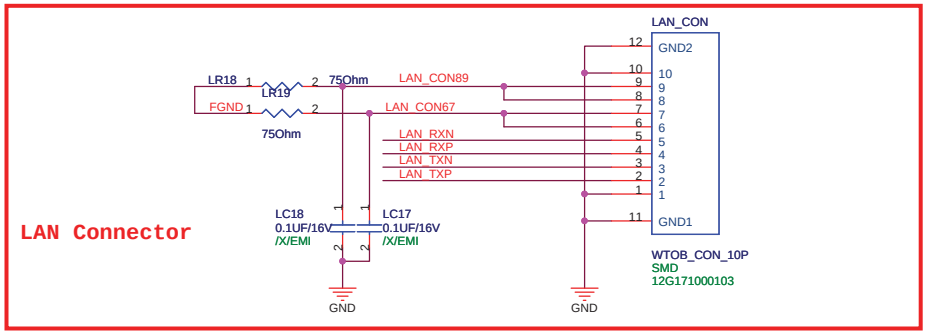
<Variant Name>

ASUSTek Computer INC.	Title : FAN_THERMAL SENSOR	
	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Wednesday, September 02, 2009	Sheet 26 of 54	


LAN Main Power
Pin 2
+3VS
+3V_LAN
R167 0Ohm r0603_h24
+3VSUS
R168 0Ohm r0603_h24 /X
LC1 0.1UF/16V
LC2 10UF/6.3V
LC15 1UF/6.3V
GND
Internal 2.5V Regulator
+2.5V_LAN
LC8 0.1UF/16V
LC9 0.1UF/16V
LC10 1UF/10V
Pin 1
+1.8V_TRAN
+1.8V_LAN
LL4 4.7UH
LC36 0.1UF/16V
LC33 10UF/6.3V
4/2_Item3
VDDHO
LC35 0.1UF/16V
Pin 6
+1.2V_LAN
LC3 1UF/6.3V
LC4 0.1UF/16V
LC5 0.1UF/16V
LC12 0.1UF/16V
DVDDL
LC37 1UF/6.3V
LC6 0.1UF/16V
LC7 0.1UF/16V
LC11 0.1UF/16V
Pin 29
3/27_Item13
+1.8V_REG
LC14 0.1UF/16V /X
LED_ACT
LR4 5.1KOhm
Pin 47
VBG1P18
LR78 4.7KOhm /X
Pin 7
3/29 item3
/X/Wake
R179
15,23,24 PEX_RST#
15,24 PCIE_WAKE#
0Ohm
LC13 0.1UF/16V
LR8 2.37KOHM 1%
3/30 item3
LU1
AR8132_AL1E
PCIE_TXN3_C 15
PCIE_TXP3_C 15
AVDDLVCO2
CLK_PCIE_LAN 15
CLK_PCIE_LAN# 15
PCIE_RX1+
PCIE_RX1-
LC31 0.1UF/16V
LC32 0.1UF/16V
PCIE_RXP3_LAN 15
PCIE_RXN3_LAN 15
LR86 0Ohm
LR87 0Ohm
LR83 0Ohm
CLK_PEREQ#3 15
28 LAN_MDI_0+
28 LAN_MDI_0-
28 LAN_MDI_1+
28 LAN_MDI_1-
AR8132 02G911002600
+1.2V_LAN
3/27_Item13
LR85 0Ohm r0603_h24
LR84 0Ohm r0603_h24 /X
AVDDLVCO1
Pin 11
LC34 0.1UF/16V
AVDDLVCO2
Pin 42
LC20 0.1UF/16V
CLK_25M_LAN 16
10PF/50V
LC2018
close to LU1
R64 75Ohm
LC2017 10PF/50V @
4/2_Item1
LR9 10MOhm /X
LX1_XTALIN
LX1 25Mhz
SL9 0402
LX1_XTALOUT/X
LC23 15PF/50V
LC24 15PF/50V
25MHz Crystal Oscillator
LC21 0.1UF/16V
LC22 0.1UF/16V
LR10 49.9Ohm 1%
LR11 49.9Ohm 1%
LR12 49.9Ohm 1%
LR13 49.9Ohm 1%
LAN_MDI_0+
LAN_MDI_0-
LAN_MDI_1+
LAN_MDI_1-
Close to LU1
Media dependent interface Terminated
<Variant Name>
Title : AR8113/AR8132
ASUSTek Computer INC
Engineer: N/A
Size A3
Project Name 1201I
Rev 1.0
Date: Wednesday, September 02, 2009
Sheet 27 of 54

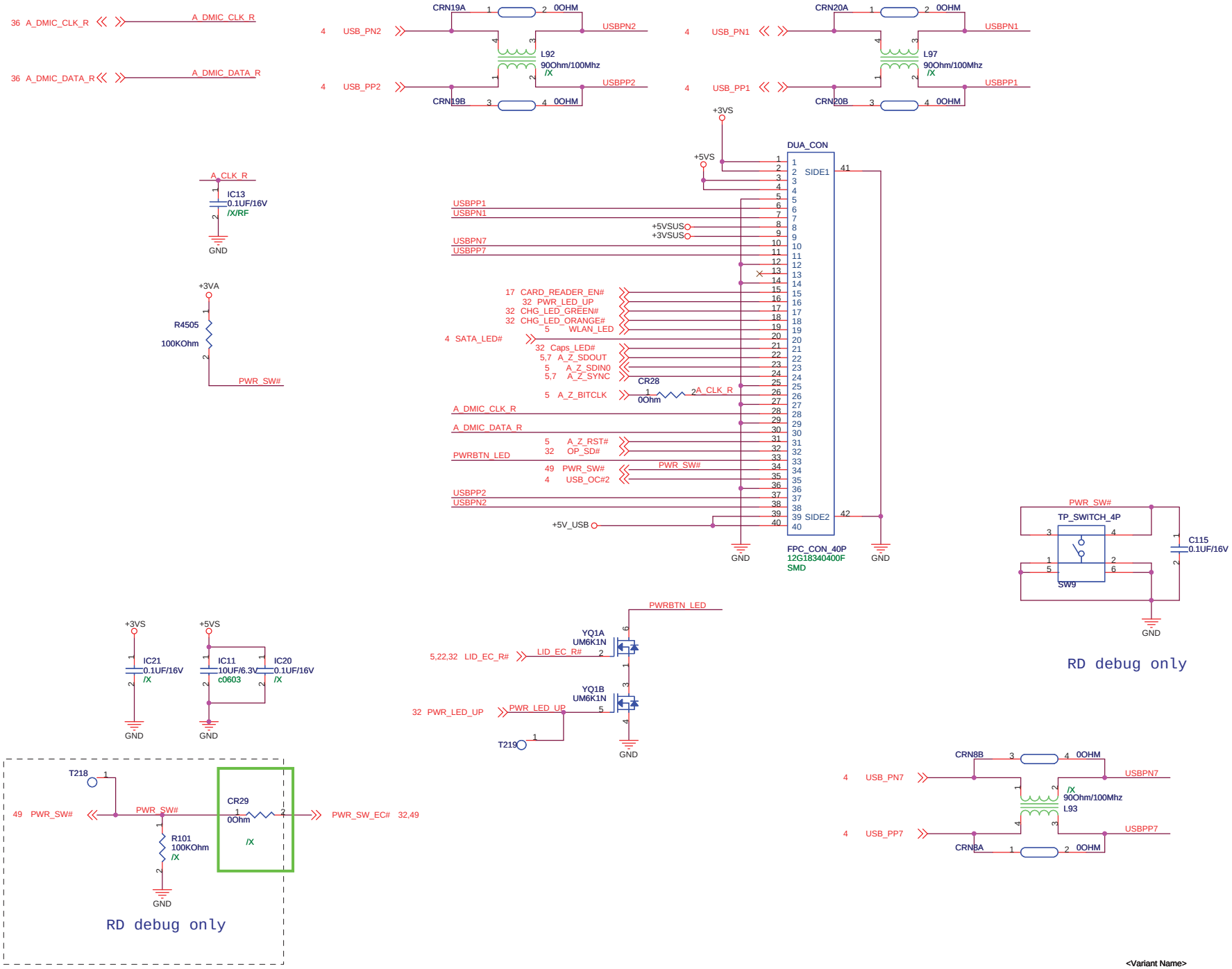






<Variant Name>

ASUSTek Computer INC.	Title : RJ45	
	Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 28 of 54	

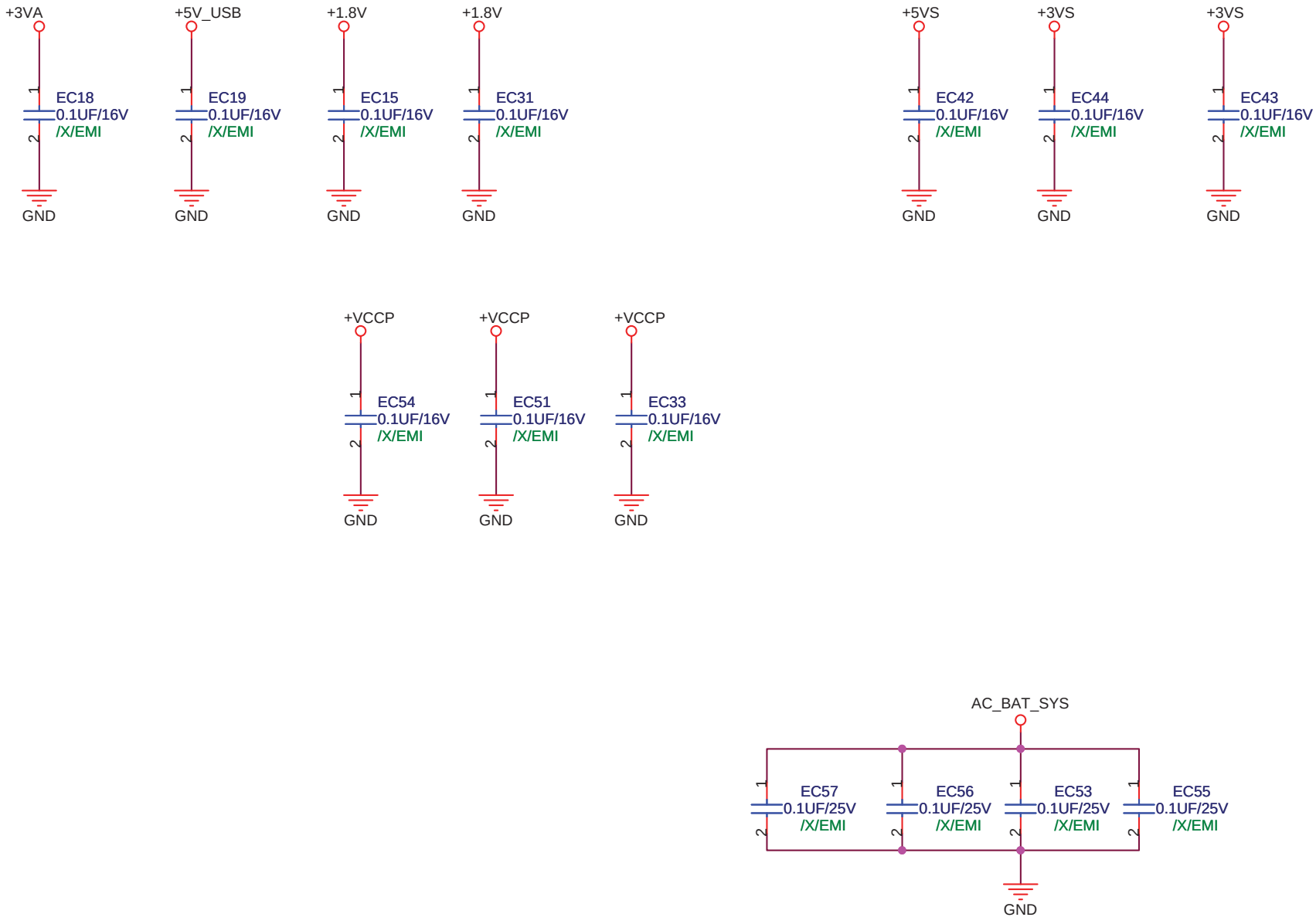


3/26 item11

3/25 item3

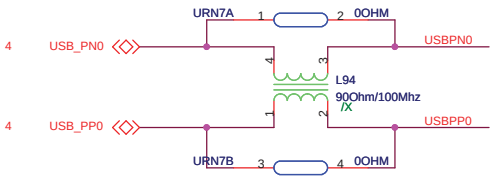
<Variant Name>

ASUS	Title : Flash Conn	
ASUSTek Computer INC.	Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 29 of 54	

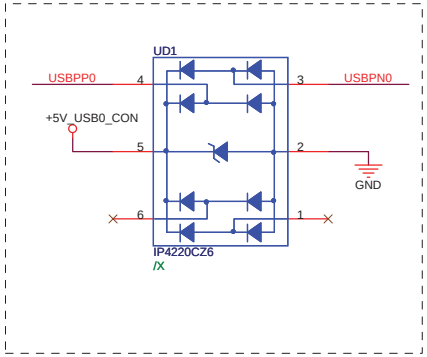


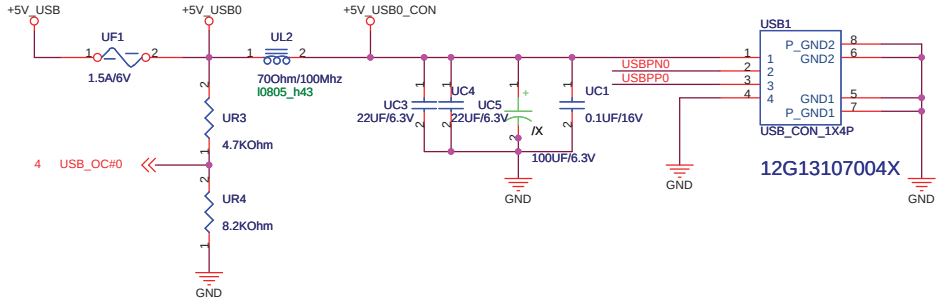
<Variant Name>

ASUSTek Computer INC.	Title : EMI	
	Engineer: N/A	
Size: A	Project Name: 1201I	Rev: 1.0
Date: Friday, August 07, 2009	Sheet 30 of 54	

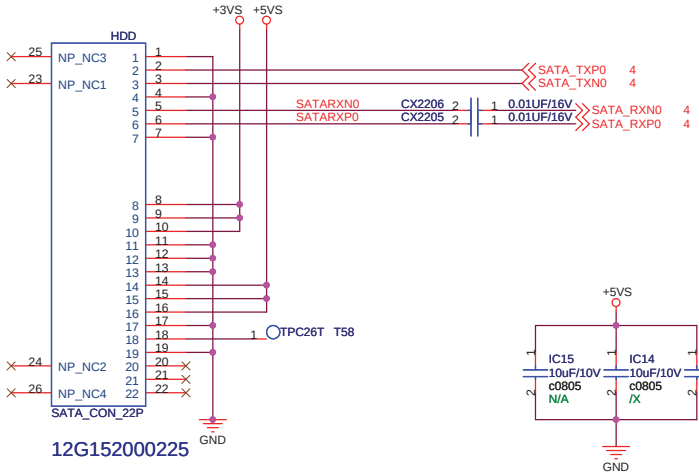


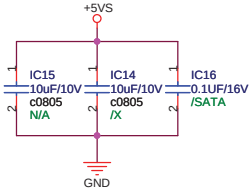
USB_PORT1

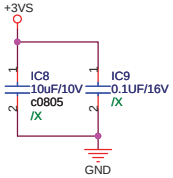




SATA HDD Connector

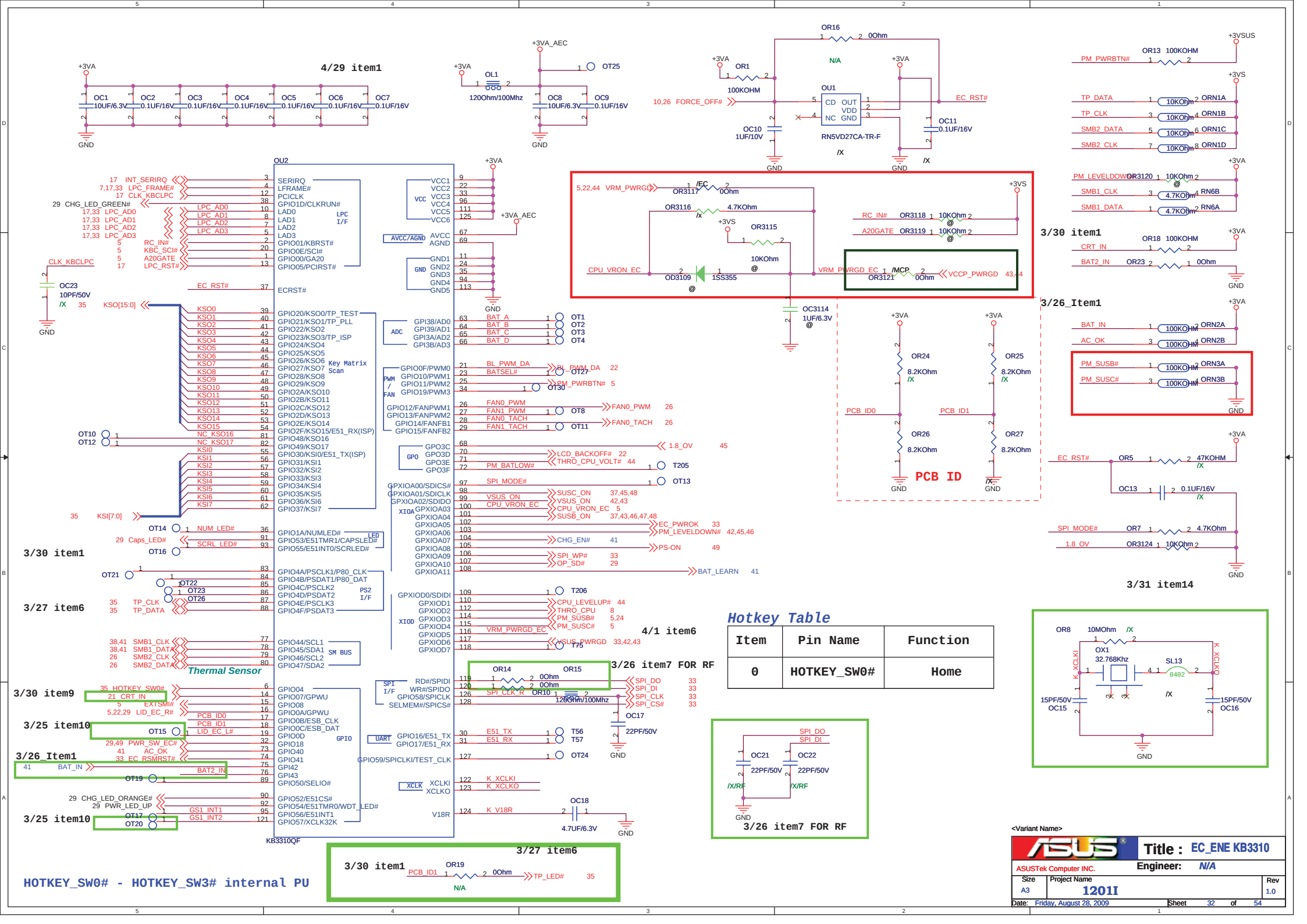




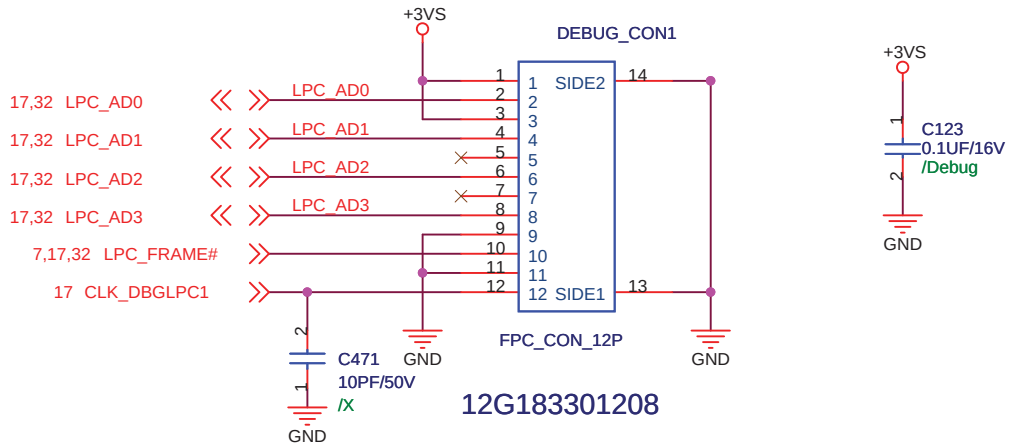


<Variant Name>

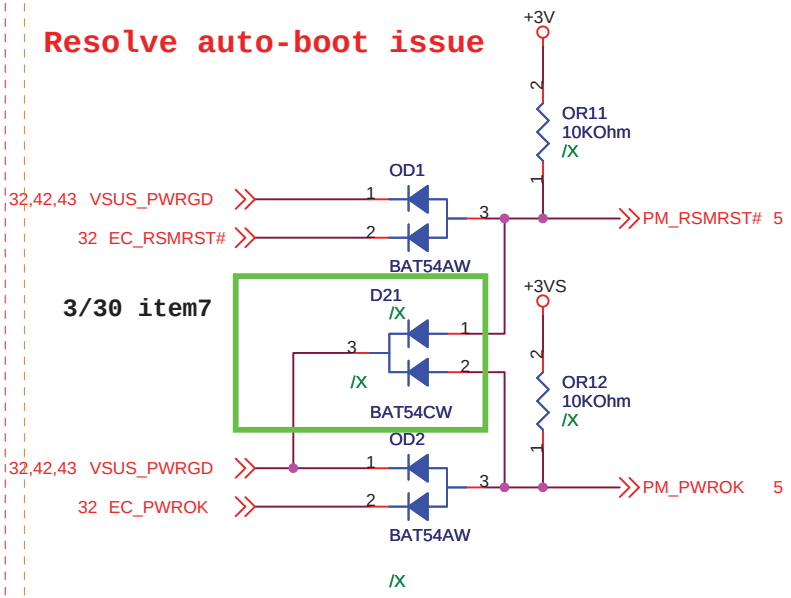
ASUSTek Computer INC.	Title : USB Port	
	Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 31 of 54	


4/29 item1
OC1 10UF/6.3V
OC2 0.1UF/16V
OC3 0.1UF/16V
OC4 0.1UF/16V
OC5 0.1UF/16V
OC6 0.1UF/16V
OC7 0.1UF/16V
OL1 120Ohm/100Mhz
OC8 10UF/6.3V
OC9 0.1UF/16V
OT25
OR16 0Ohm
N/A
OR1 100KOHM
OU1
CD OUT
VDD
NC GND
RN5VD27CA-TR-F
OC10 1UF/10V
OC11 0.1UF/16V
10,26 FORCE_OFF#
EC_RST#
OR13 100KOHM
PM_PWRBTN#
TP_DATA
TP_CLK
SMB2_DATA
SMB2_CLK
10KOhm
ORN1A
ORN1B
ORN1C
ORN1D
PM_LEVELDOWN
OR3120 10KOhm
SMB1_CLK
SMB1_DATA
4.7KOhm
RN6B
RN6A
3/30 item1
CRT_IN
BAT2_IN
OR18 100KOHM
OR23 0Ohm
OU2
KB3310QF
INT_SERIRQ
LPC_FRAME#
CLK_KBCLPC
CHG_LED_GREEN#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
RC_IN#
KBC_SCI#
A20GATE
LPC_RST#
LPC I/F
EC_RST#
ECRST#
KSO[15:0]
KSI[7:0]
Key Matrix Scan
NC_KSO16
NC_KSO17
NUM_LED#
Caps_LED#
SCRL_LED#
LED
3/30 item1
TP_CLK
TP_DATA
PS2 I/F
3/27 item6
SMB1_CLK
SMB1_DATA
SMB2_CLK
SMB2_DATA
SM BUS
Thermal Sensor
HOTKEY_SW0#
CRT_IN
EXTSMI#
LID_EC_R#
PCB_ID0
PCB_ID1
LID_EC_L#
PWR_SW_EC#
AC_OK
EC_RSMRST#
BAT_IN
BAT2_IN
GPIO
3/30 item9
3/25 item10
3/26_Item1
CHG_LED_ORANGE#
PWR_LED_UP
GS1_INT1
GS1_INT2
3/25 item10
VCC
AVCC/AGND
GND
ADC
PWM / FAN
GPO
XIOA
XIOD
SPI I/F
UART
XCLK
BAT_A
BAT_B
BAT_C
BAT_D
BL_PWM_DA
BATSEL#
PM_PWRBTN#
FAN0_PWM
FAN1_PWM
FAN0_TACH
FAN1_TACH
1.8_OV
LCD_BACKOFF#
THRO_CPU_VOLT#
PM_BATLOW#
SPI_MODE#
SUSC_ON
VSUS_ON
CPU_VRON_EC
SUSB_ON
EC_PWROK
PM_LEVELDOWN#
CHG_EN#
PS-ON
SPI_WP#
OP_SD#
BAT_LEARN
CPU_LEVELUP#
THRO_CPU
PM_SUSB#
PM_SUSC#
VRM_PWRGD_EC
VSUS_PWRGD
4/1 item6
3/26 item7 FOR RF
OR14 0Ohm
OR15 0Ohm
OR10 120Ohm/100Mhz
SPI_DO
SPI_DI
SPI_CLK_R
SPI_CLK
SPI_CS#
OC17 22PF/50V
E51_TX
E51_RX
GPIO59/SPICLKI/TEST_CLK
K_XCLKI
K_XCLKO
V18R
K_V18R
OC18 4.7UF/6.3V
5,22,44 VRM_PWRGD
OR3117 /EC 0Ohm
OR3116 4.7KOhm
OR3115 10KOhm
CPU_VRON_EC
OD3109 1SS355
RC_IN#
A20GATE
OR3118 10KOhm
OR3119 10KOhm
VRM_PWRGD_EC
OR3121 /MCP 0Ohm
VCCP_PWRGD
OC3114 1UF/6.3V
3/26_Item1
BAT_IN
AC_OK
PM_SUSB#
PM_SUSC#
ORN2A
ORN2B
ORN3A
ORN3B
OR24 8.2KOhm
OR25 8.2KOhm
OR26 8.2KOhm
OR27 8.2KOhm
PCB_ID0
PCB_ID1
PCB ID
EC_RST#
OR5 47KOHM
OC13 0.1UF/16V
SPI_MODE#
OR7 4.7KOhm
1.8_OV
OR3124 10KOhm
3/31 item14
Hotkey Table
Item | Pin Name | Function
0 | HOTKEY_SW0# | Home
OR8 10MOhm
OX1 32.768Khz
SL13 0402
K_XCLKI
K_XCLKO
15PF/50V OC15
15PF/50V OC16
OC21 22PF/50V
OC22 22PF/50V
3/26 item7 FOR RF
3/30 item1
OR19 0Ohm
PCB_ID1
TP_LED#
N/A
3/27 item6
HOTKEY_SW0# - HOTKEY_SW3# internal PU
Variant Name
ASUS
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1201I
Rev 1.0
Date: Friday, August 28, 2009
Sheet 32 of 54

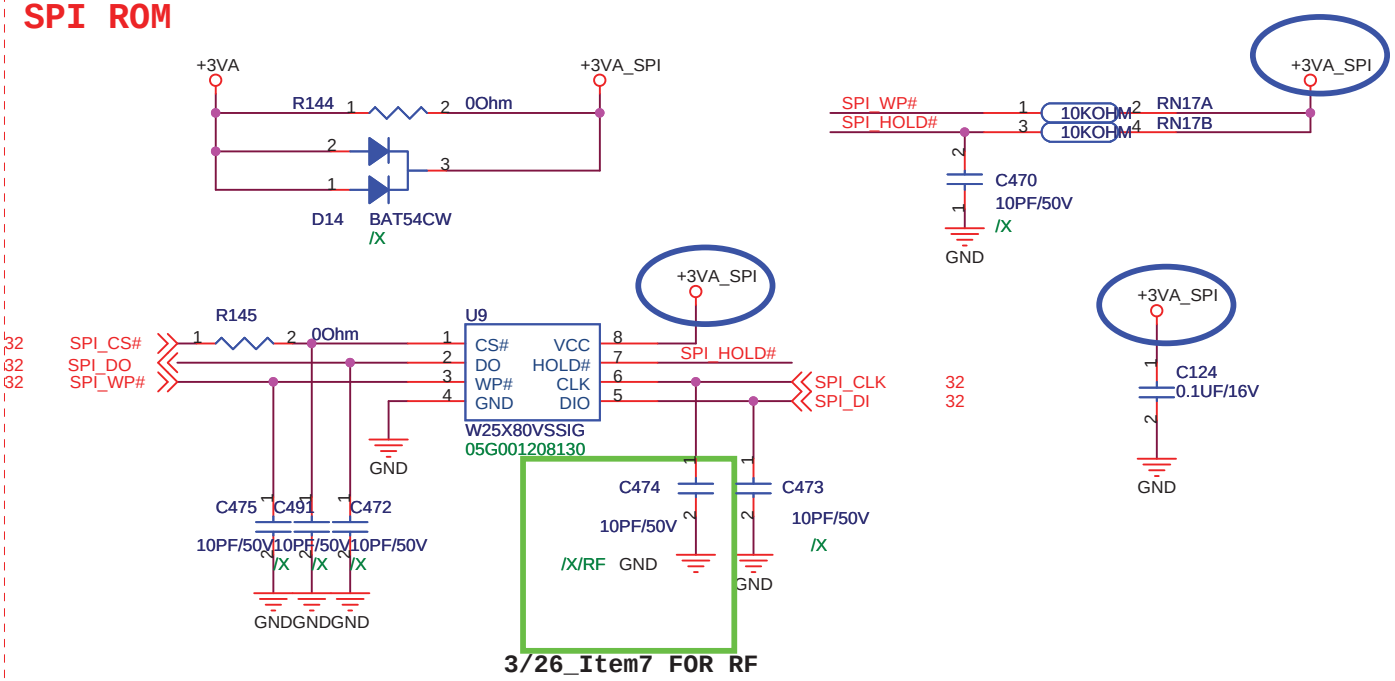
For Debug



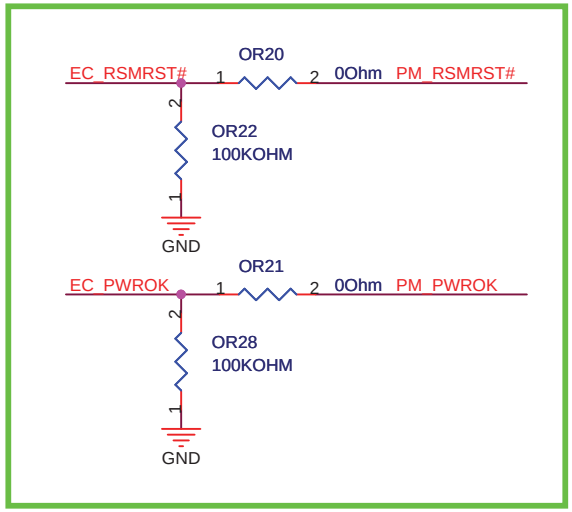
Resolve auto-boot issue



SPI ROM

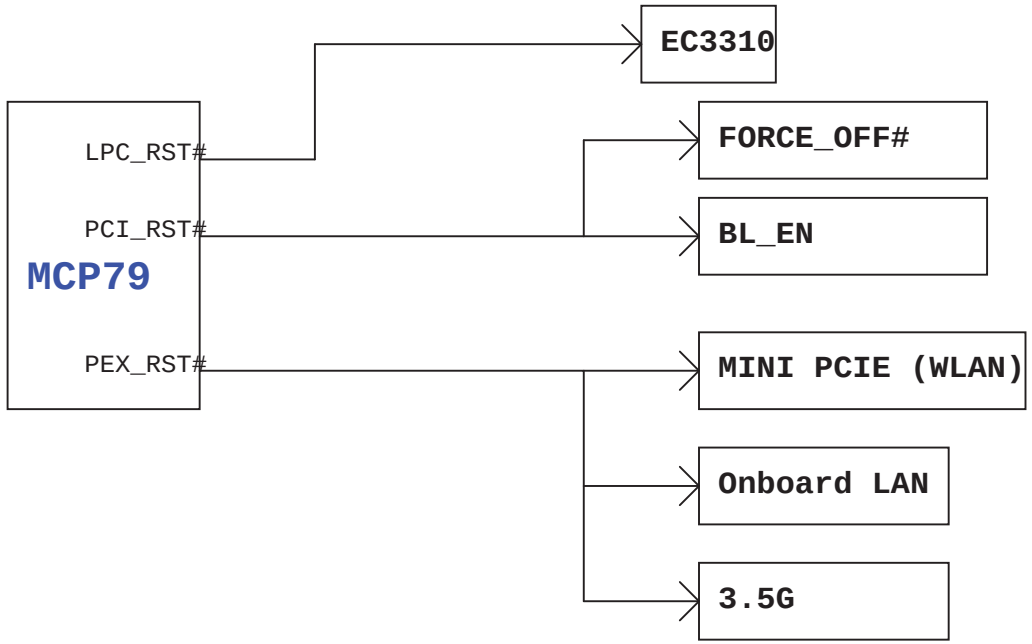


3/30 item7



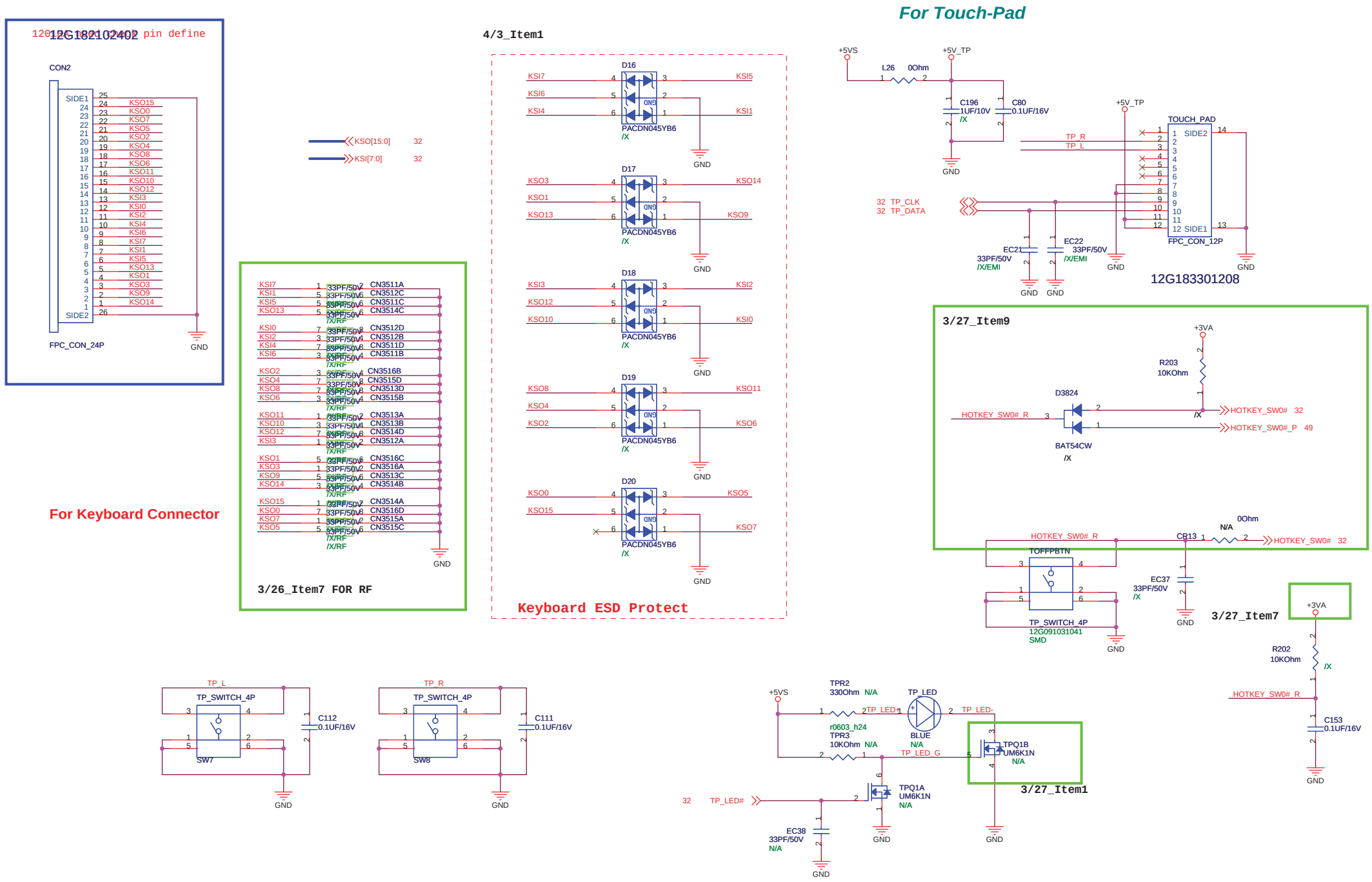
<Variant Name>

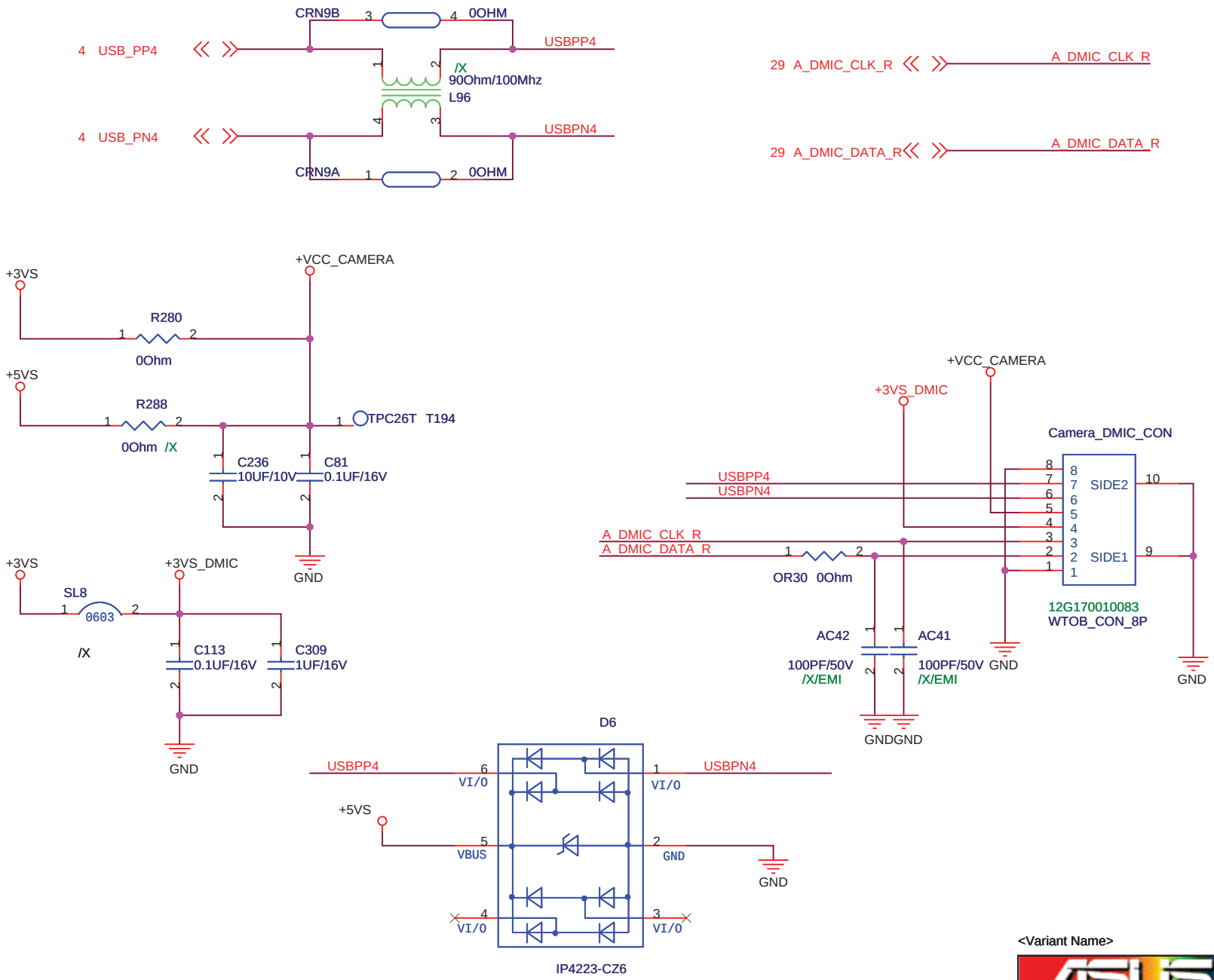
ASUS	Title : SPI ROM/ Debug	
ASUSTek Computer INC.	Engineer: N/A	
Size A4	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 33 of 54	



<Variant Name>

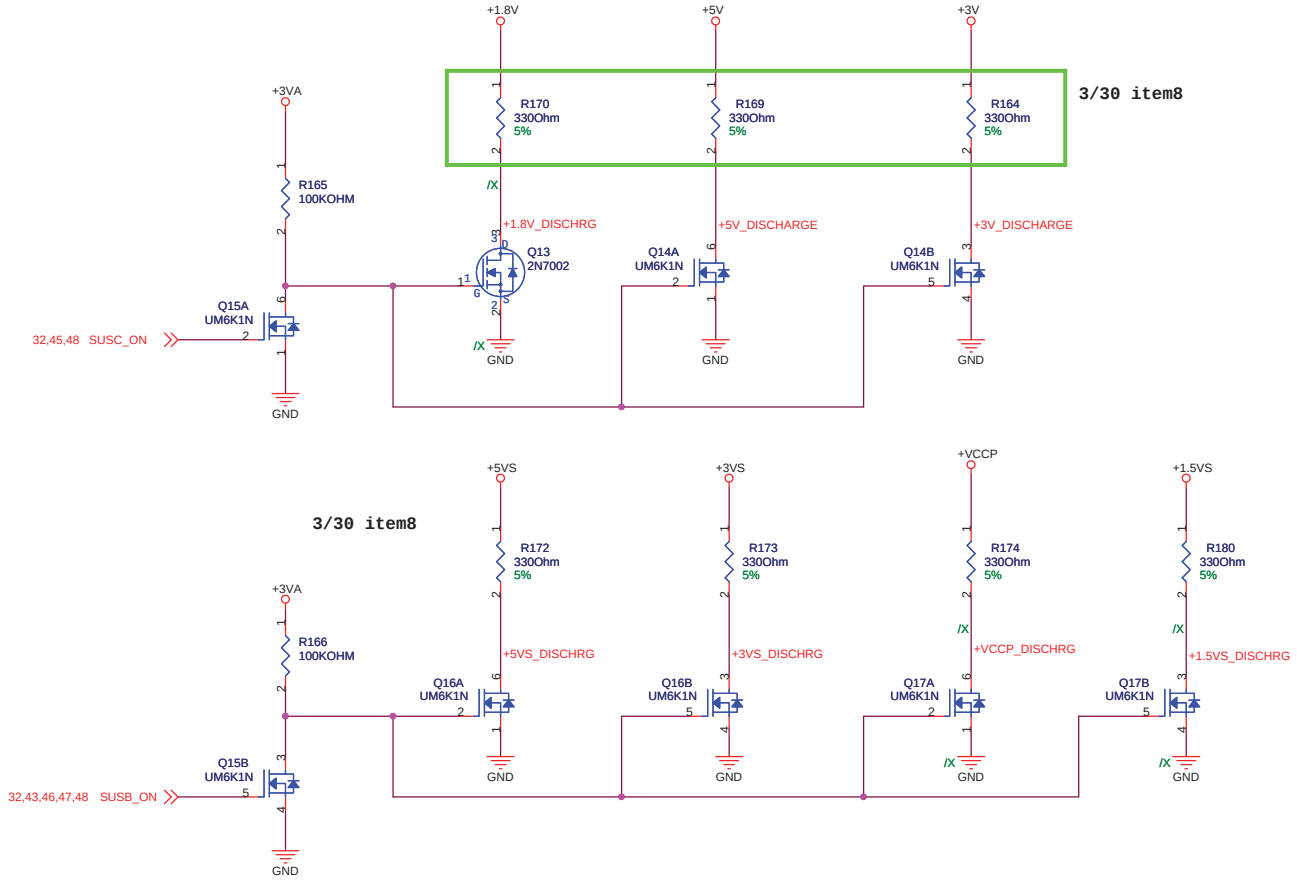
ASUSTeK COMPUTER INC	Title : Reset Map	
	Engineer: N/A	
Size A4	Project Name 1201I	Rev 1.0
Date: Monday, July 20, 2009	Sheet 34 of 54	


For Touch-Pad
12G182102402
CON2
FPC_CON_24P
GND
4/3_Item1
KSO[15:0] 32
KSI[7:0] 32
D16
D17
D18
D19
D20
PACDN045YB6
/X
3/26_Item7 FOR RF
33PF/50V
/X/RF
For Keyboard Connector
Keyboard ESD Protect
+5VS
+5V_TP
L26 0Ohm
C196 1UF/10V /X
C80 0.1UF/16V
TOUCH_PAD
FPC_CON_12P
TP_R
TP_L
32 TP_CLK
32 TP_DATA
EC21 33PF/50V /X/EMI
EC22 33PF/50V /X/EMI
12G183301208
3/27_Item9
+3VA
R203 10KOhm
D3824
BAT54CW
HOTKEY_SW0# R
HOTKEY_SW0# 32
HOTKEY_SW0#_P 49
CB13 0Ohm N/A
TOFFPBTN
TP_SWITCH_4P
12G091031041
SMD
EC37 33PF/50V /X
3/27_Item7
R202 10KOhm
C153 0.1UF/16V
TP_L
TP_R
C112 0.1UF/16V
C111 0.1UF/16V
SW7
SW8
TPR2 330Ohm N/A
TP_LED
BLUE N/A
TPR3 10KOhm N/A
r0603_h24
TPQ1B UM6K1N N/A
TPQ1A UM6K1N N/A
TP_LED+
TP_LED-
TP_LED_G
32 TP_LED#
EC38 33PF/50V N/A
3/27_Item1
ASUSTek Computer INC.
Title : KB_Touch Pad
Engineer: N/A
Size A3
Project Name 1201I
Rev 1.0
Date: Friday, August 28, 2009
Sheet 35 of 54



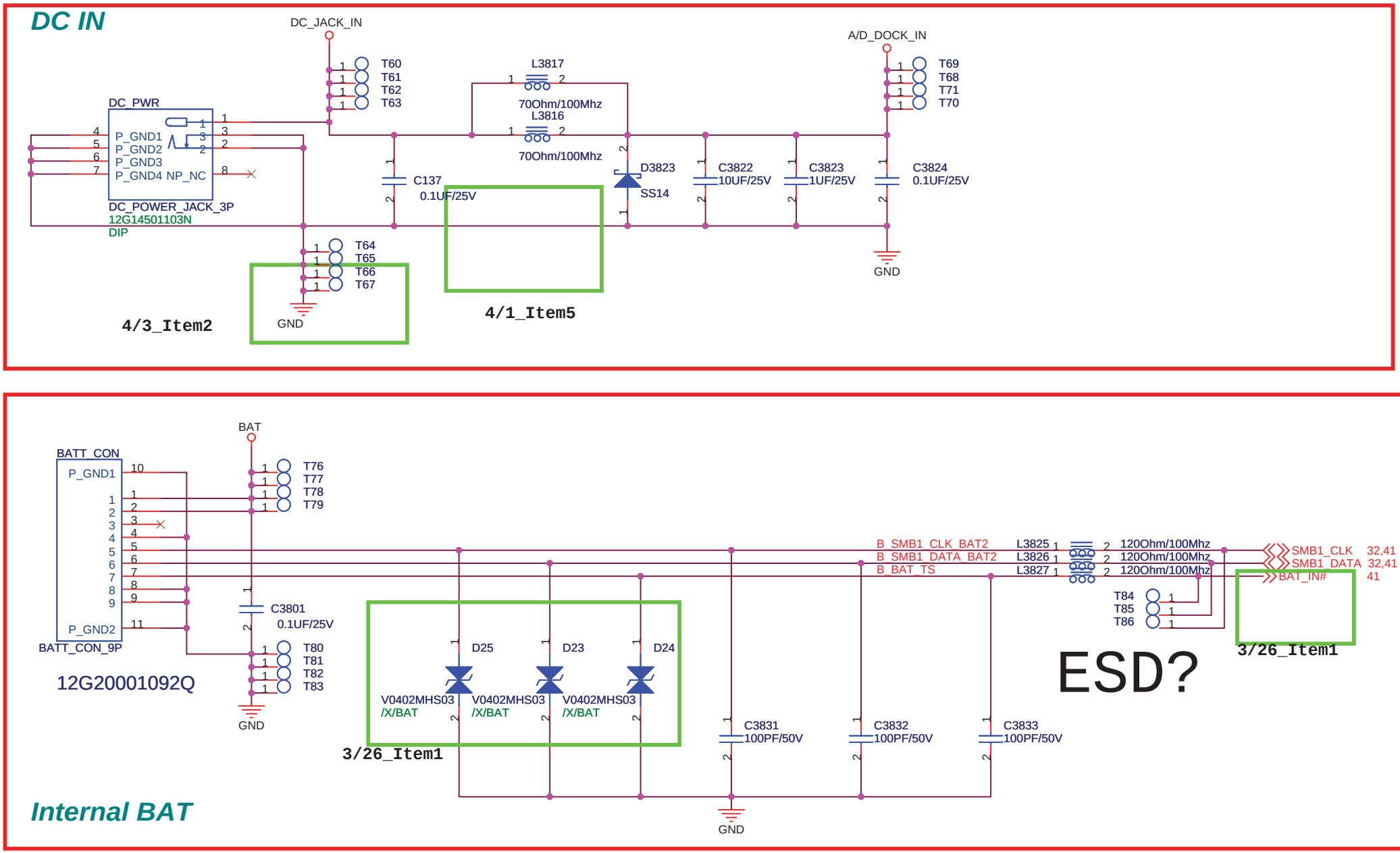
<Variant Name>

ASUS	Title : CMOS	
ASUSTek Computer INC.	Engineer: N/A	
Size A4	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 36 of 54	



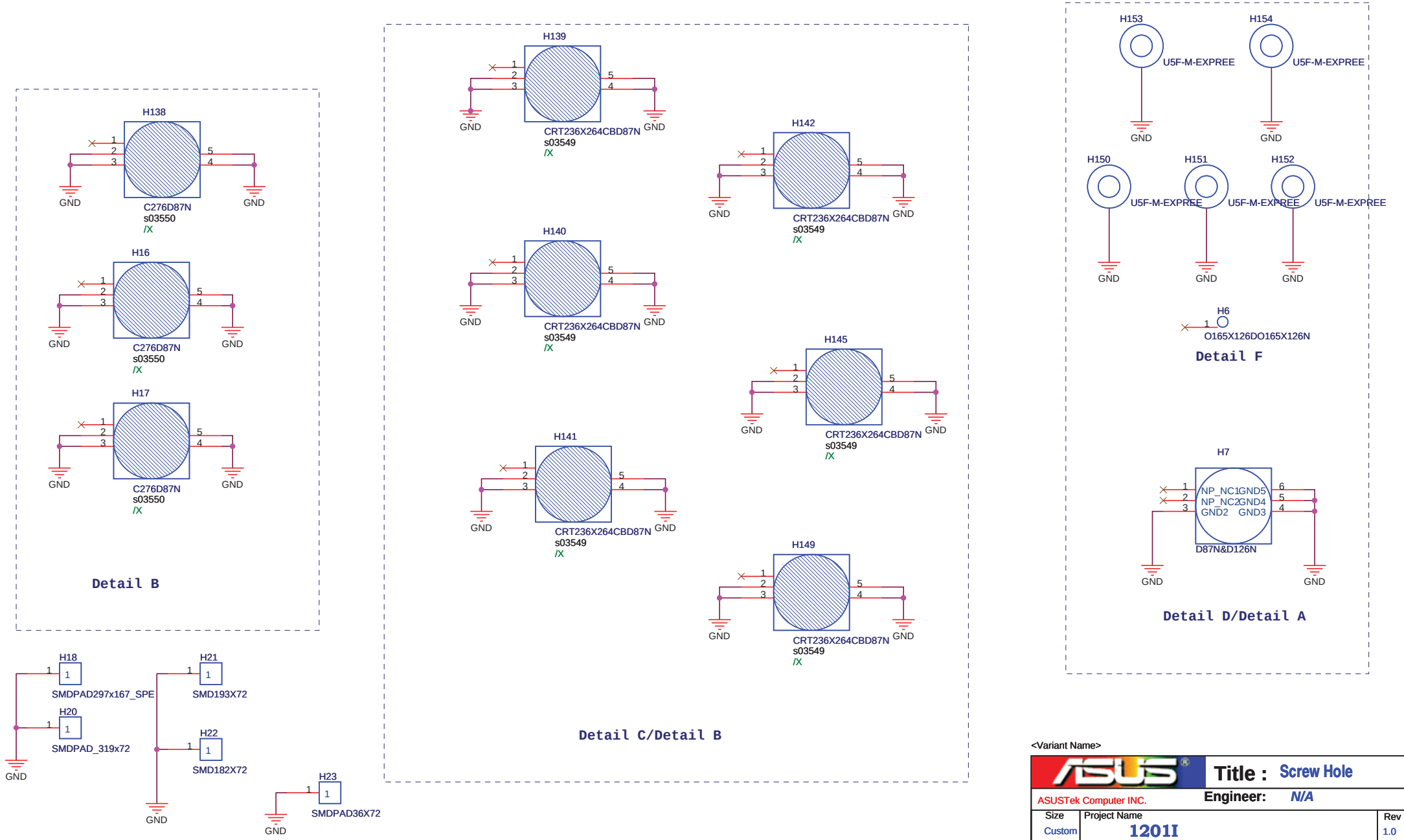
<Variant Name>

ASUSTek Computer INC.	Title : Discharge	
	Engineer: N/A	
Size A3	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 37 of 54	



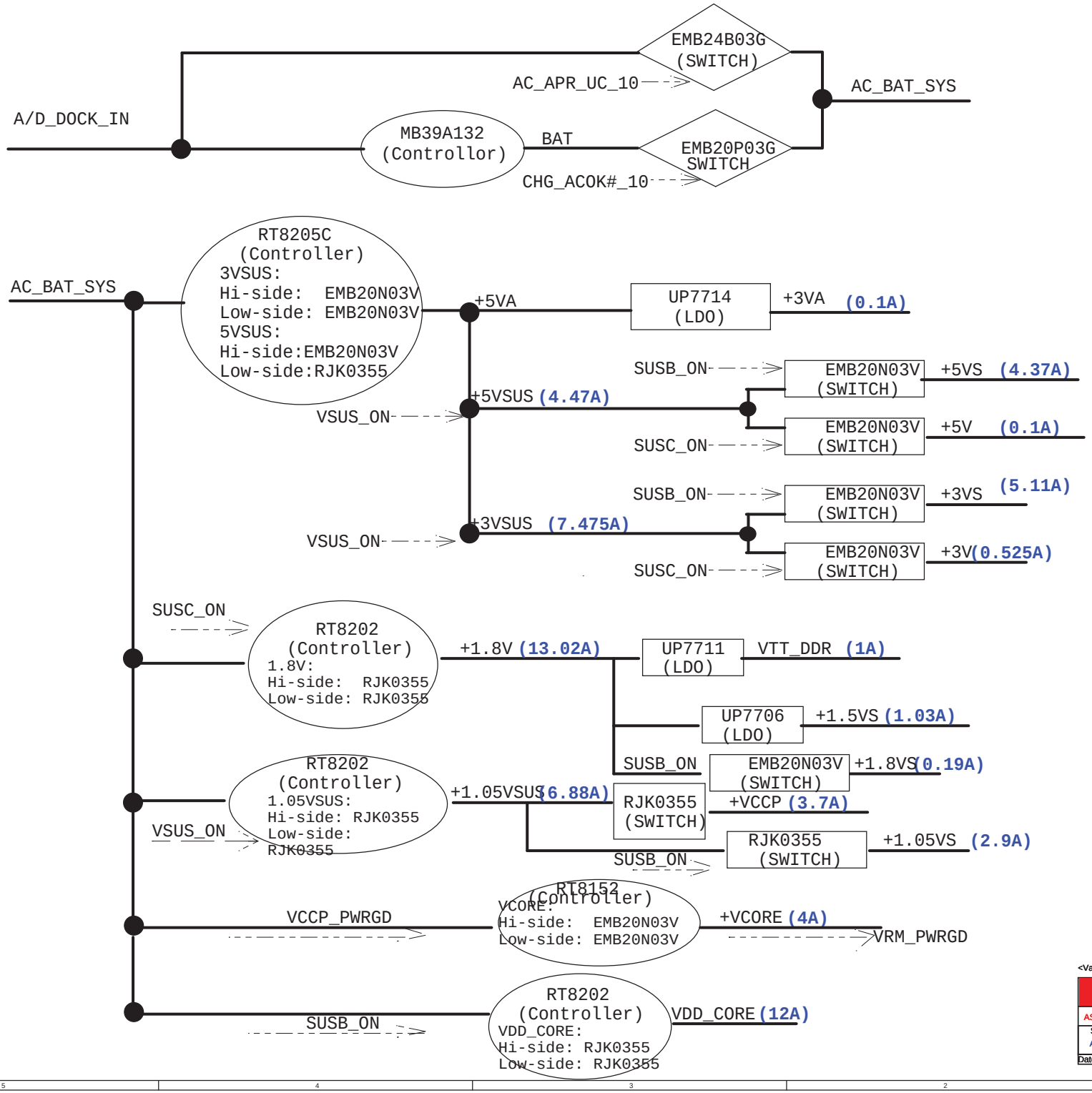
<Variant Name>

ASUS	Title : PWR Jack	
ASUSTek Computer INC.	Engineer: N/A	
Size A4	Project Name 1201I	Rev 1.0
Date: Friday, August 28, 2009	Sheet 38 of 54	



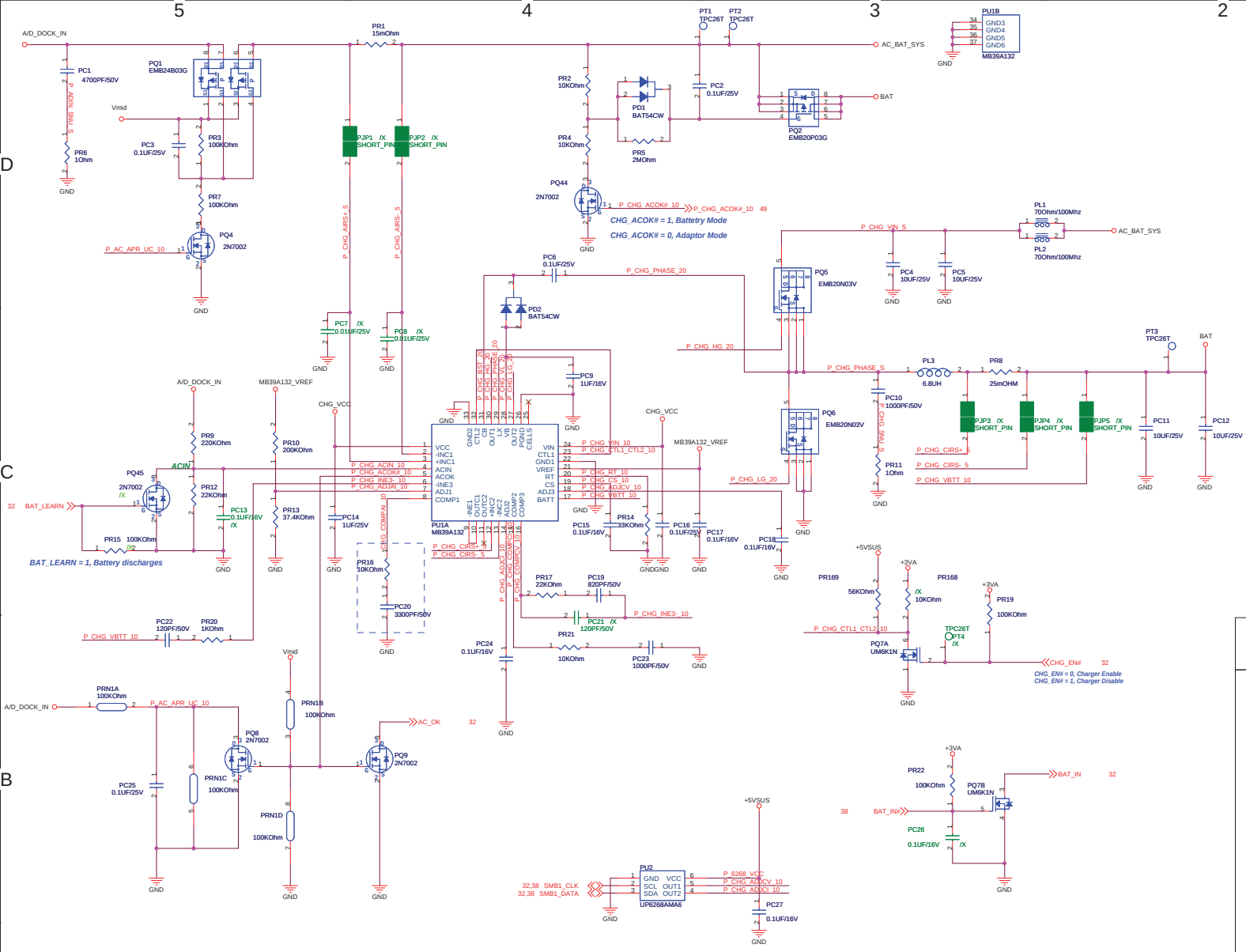
<Variant Name>

ASUS	Title : Screw Hole	
ASUSTek Computer INC.	Engineer: N/A	
Size: Custom	Project Name: 1201I	Rev: 1.0
Date: Thursday, September 03, 2009	Sheet 39 of 54	



<Variant Name>

ASUS	Title : Power Flow	
ASUSTek Computer INC.	Engineer: Jerry Liu	
Size A3	Project Name 1201i	Rev 1.2
Date: Wednesday, August 26, 2009	Sheet 40 of 54	



Power stage

1. I/P Current:

I in = Vo*Io/(0.8 * Vin) =1.64A

2. Ripple Current:

I ripple =0.875A
I spec=2A ⊙1 pcs

3. Inductor Spec:

I sat=8 A
I dc =4.5A
DCR=60mohm

4. MOSFET Spec:

H-side MOSFET:EMB20N03V

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

L-side MOSFET: EMB20N03V

Rds(ON)= 22 mohm (Vgs=4.5 V)
I cont = 6.5 A (T =25)
I peak = 40 A (Pause ≦10 us)

Controller

1. Voltage & Current:

+12.6V@2.5A

2. Frequency:

PR122=33KOHM,
Fosc=17000/RT(Kohm)=515KHz

3. OCP:

4. POR:

POR Hysteresis =0.1V
V on =7.5V

5. Enable Voltage:

V = 2.9 V

6. Soft start time:

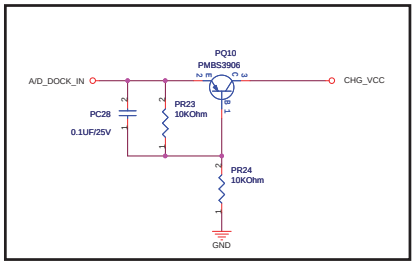
Tss=23ms

7. Phase selection:

N/A

8.Inrush Current:

C total =20uF
I inrush= 0.01A



Battery Charging Current :

Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

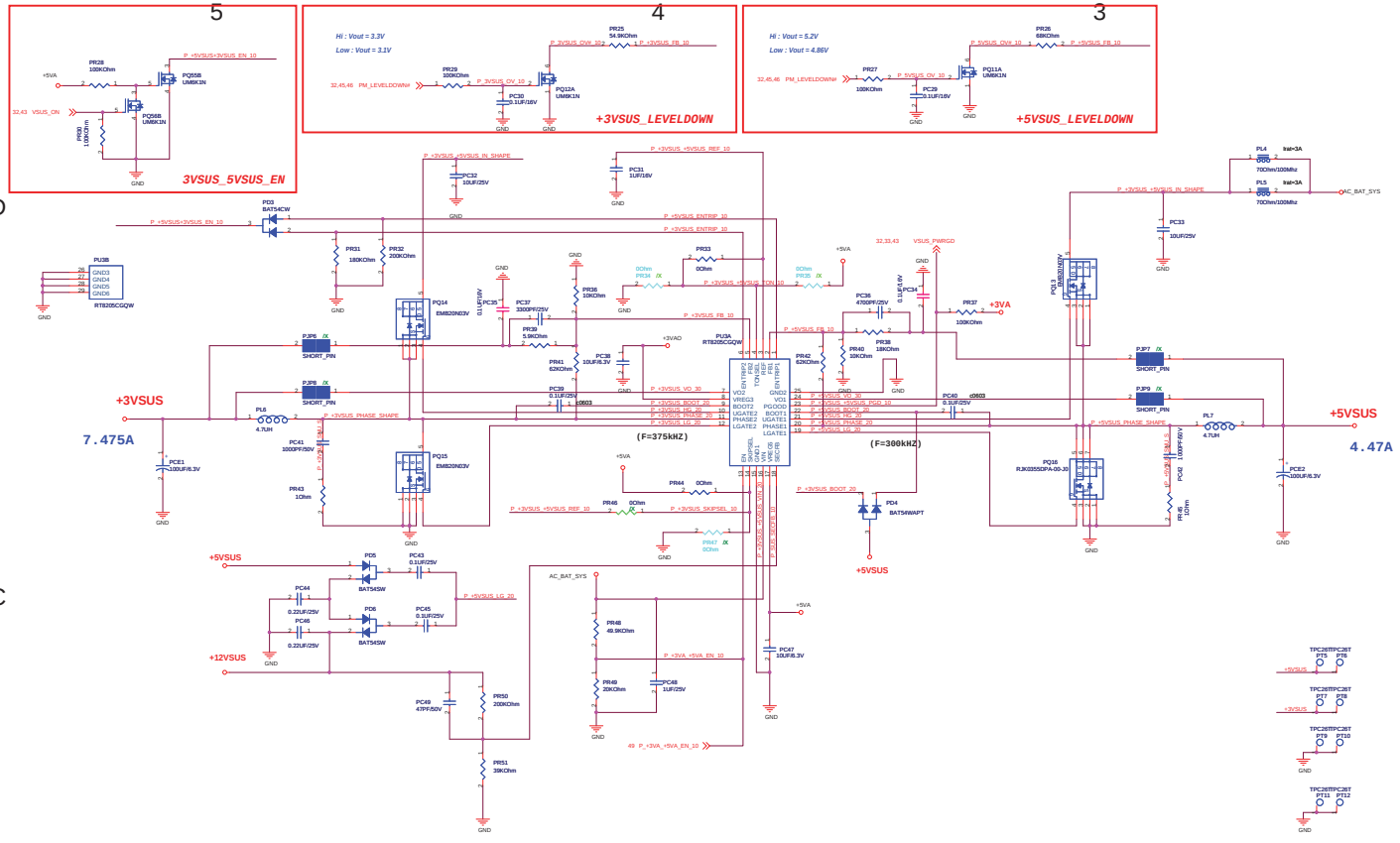
CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

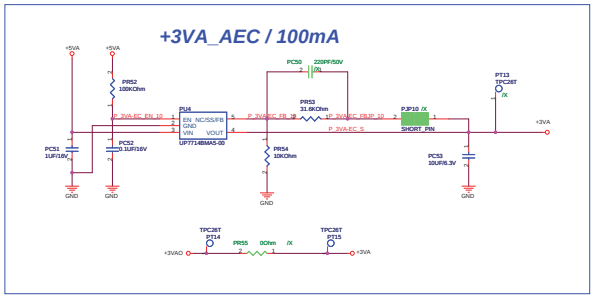
VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.23 * CS (uF)*

ASUS	Title : Charger	
ASUSTek Computer INC	Engineer: Joy_Zhou	
Size A2	Project Name 12011	Rev <RevCode>
Date: Friday, August 28, 2009	Sheet 41 of 54	





Power stage	+3VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =8A	
2. Ripple Current:	
I rip =2.13A	
I spec=2.5A ⊙1 pcs	
3. Dynamic:	
I peak=4.43A	
ESR / 1 pcs =18 mohm	
〉V =79.74mV	
4. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
5. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm (Vgs=4.5 V)	
I cont = 6.5 A (T =25)	
I peak = 40 A (Pause ≦10 us)	
L-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm (Vgs=4.5 V)	
I cont = 6.5 A (T =25)	
I peak = 40 A (Pause ≦10 us)	

Power stage	+5VSUS
1. I/P Current:	
I in = Vo*Io/(0.8 * Vin) =5A	
2. Ripple Current:	
I rip =2.84A	
I spec=2.5A ⊙1 pcs	
3. Dynamic:	
I peak=3.99A	
ESR / 1 pcs =18 mohm	
〉V =71.82mV	
4. Inductor Spec:	
I sat=10 A	
I dc =5.5 A	
DCR=37 mohm	
5. MOSFET Spec:	
H-side MOSFET: EMB20N03V	
Rds(ON)= 22 mohm (Vgs=4.5 V)	
I cont = 6.5 A (T =25)	
I peak = 40 A (Pause ≦10 us)	
L-side MOSFET: RJK0355DPA-00-J0 WPAK	
Rds(ON)= 11.8 mohm (Vgs=4.5 V)	
I cont = 30 A (T =25)	
I peak = 120 A (Pause ≦10 us)	

Controller	+3VSUS	Controller	+5VSUS
1. Voltage & Current:	6. OVP:	1. Voltage & Current:	6. OVP:
+3VSUS=3.3V@4.43A	V ovp=115%Vout	+5VSUS=5V@5.751A	V ovp=115%Vout
2. Frequency:	7. Enable Voltage:	2. Frequency:	7. Enable Voltage:
fosc=375KHz	V rising = 1V	fosc=300KHz	V rising = 1V
3. OCP:	V falling = 0.4 V	3. OCP:	V falling = 0.4 V
Set PR33=180Kohm	8. Soft start time:	Set PR82=200Kohm	8. Soft start time:
Iocp=8.18A	Tss=2ms	Iocp=17A	Tss=2ms
4. POR:	9. Phase selection:	4. POR:	9. Phase selection:
V on =4.35-4.5 V	/X	V on =4.35-4.5 V	/X
V off =3.9-4.25 V	10.Inrush Current:	V off =3.9-4.25 V	10.Inrush Current:
5. UVP:	C total = 110 uF	5. UVP:	C total = 110 uF
V uvp= 70% Vout	I inrush= 0.165 A	V uvp= 70% Vout	I inrush= 0.275 A

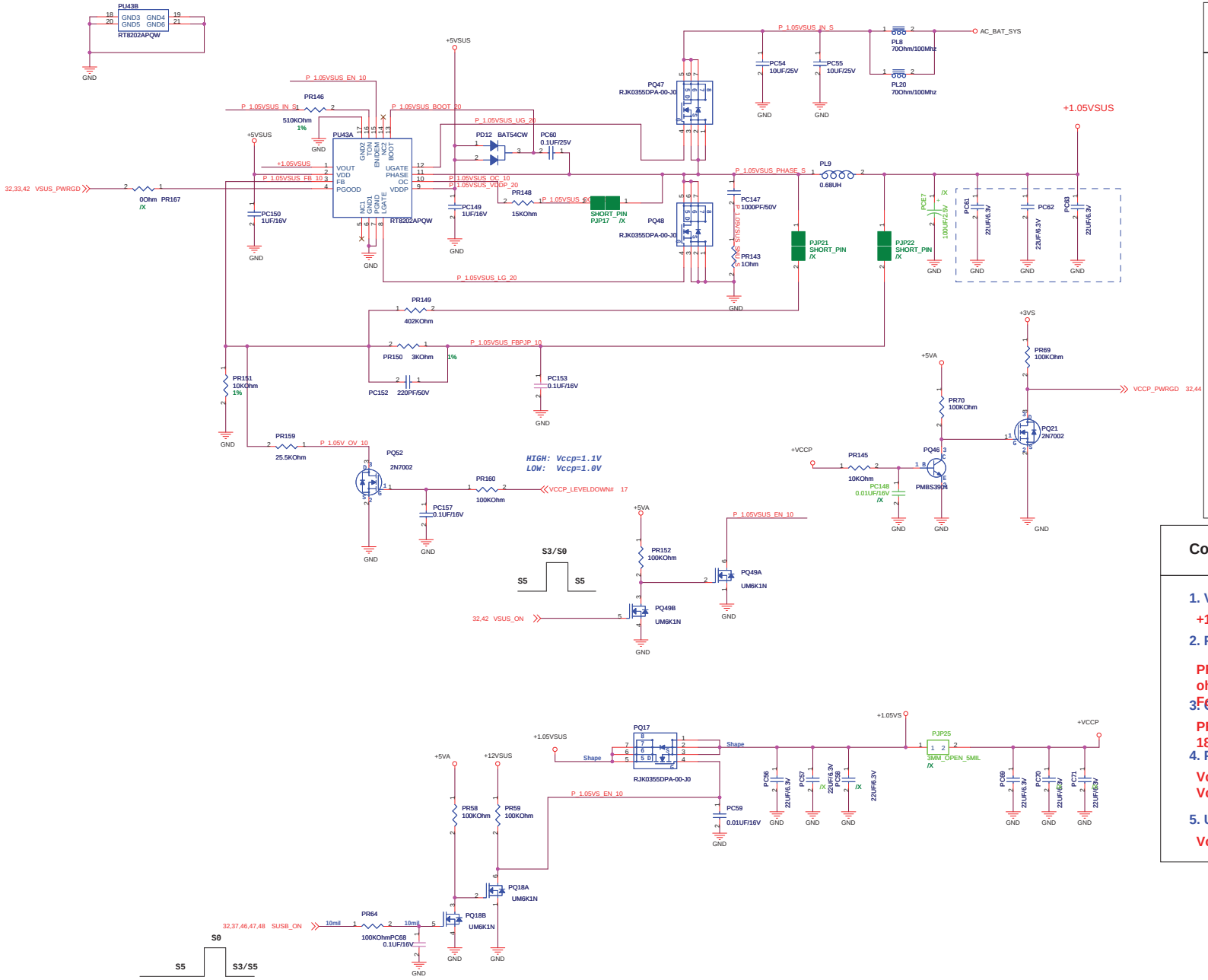
ASUSTeK Computer INC

Title : Power_+5SUS&+3VSUS&+12VSUS

Engineer: Joy_Zhou

Size: A1 | Project Name: 12011 | Rev: <RevCode>

Date: Friday, August 28, 2009 | Sheet 42 of 54



Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =1.7A

2. Ripple Current:

   I rip =2.72A
   I spec=2.5A
   ⊙2pcs

3. Dynamic:

   I peak=2.5A
   ESR / 1 pcs =18 mohm
   〉V =45mV

4. Inductor Spec:

   I SAC=25.5A
   IDC =15.5 A
   DCR=5mohm

5. MOSFET Spec:

   H-side MOSFET:RJK0355DPA-00-J0

   Rds(ON)= 16.5mOhm (Vgs=4.5 V)
   I cont = 30 A (T =25)
   I peak =120 A (Pause ≦10 us)

   L-side MOSFET: RJK0355DPA-00-J0

   Rds(ON)= 16.5mOhm (Vgs=4.5 V)
   I cont =30 A (T =25)
   I peak =120 A (Pause ≦10 us)

Controller

1. Voltage & Current:

   +1.05V@6.88A

2. Frequency:

   PR146=510K ohm
   Fosc=480KHz

3. OCP:

   PR148=15K ohm -> 18A

4. POR:

   Vccrth =3.7~4.1V
   Vcchys=0.2V

5. UVP:

   Vout*70%

6. OVP:

   Vout*115%

7. Enable Voltage:

   V = 2.9V

8. Soft start time:

   Tss=1.2 ms

9. Phase selection:

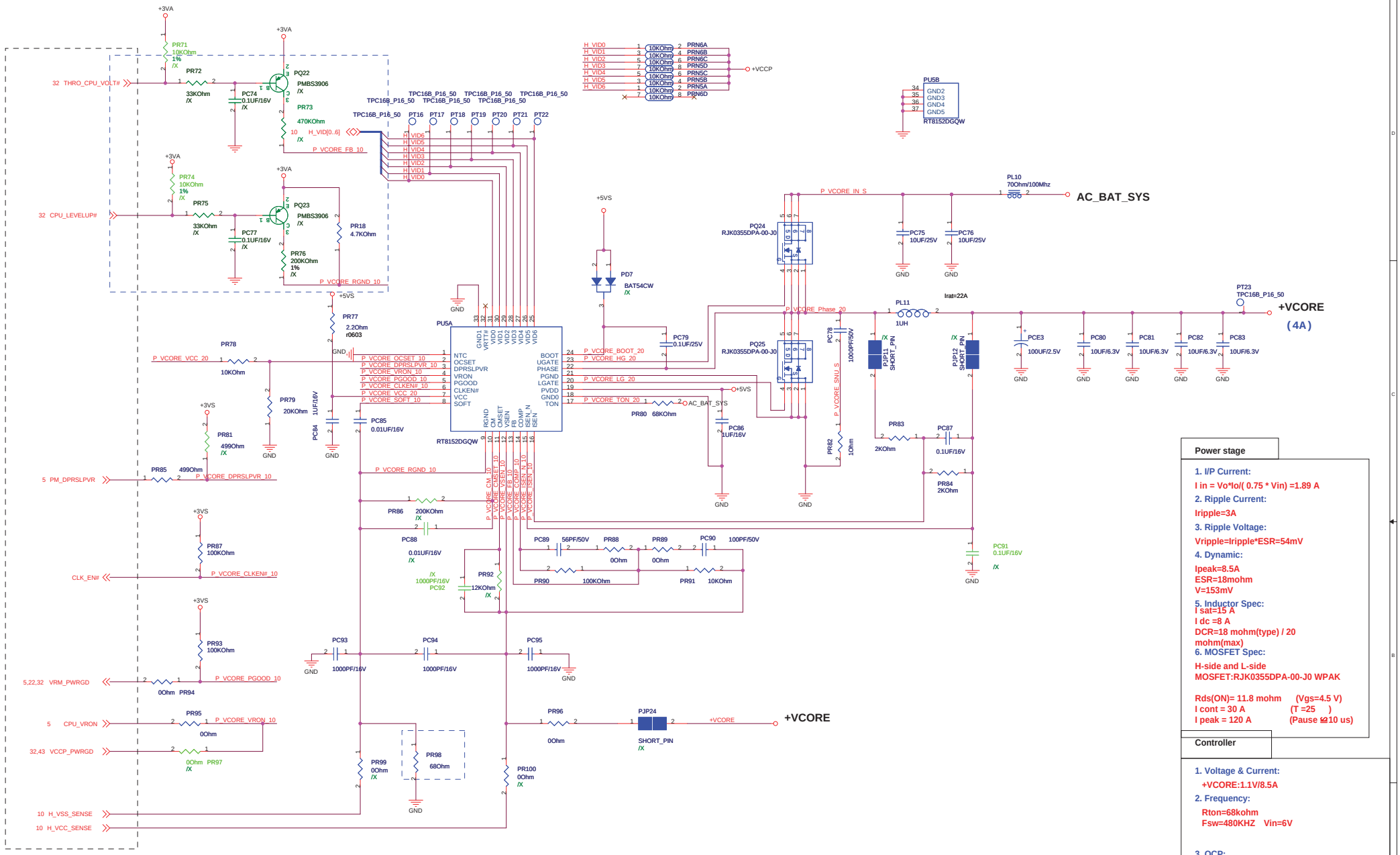
   /X

10. Inrush Current:

   C total = 100 uF
   I inrush= 0.15 A

<Variant Name>

ASUS	Title : POWER_1.05v
ASUSTeK COMPUTER INC. NB	Engineer: Joy_zhou
Size A2	Project Name 12011
Rev 1.0	
Date: Friday, August 28, 2009	Sheet 43 of 54



THRO_CPU_VOLT#	CPU_LEVELUP#	Voltage	Status
L	H	VID-50mV	Power Saving
H	H	VID	Normal
H	L	VID+50mV	Performance

Power stage

1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =1.89 A
2. Ripple Current:
Iripple=3A
3. Ripple Voltage:
Vripple=Iripple*ESR=54mV
4. Dynamic:
Ipeak=8.5A
ESR=18mohm
V=153mV
5. Inductor Spec:
I sat=15 A
I dc =8 A
DCR=18 mohm(type) / 20 mohm(max)
6. MOSFET Spec:
H-side and L-side
MOSFET:RJK0355DPA-00-J0 WPAK

Rds(ON)= 11.8 mohm (Vgs=4.5 V)
I cont = 30 A (T =25)
I peak = 120 A (Pause ≦10 us)

Controller

1. Voltage & Current:
+VCORE:1.1V/8.5A
2. Frequency:
Rton=68kohm
Fsw=480KHZ Vin=6V

3. OCP:
DCR*Imax*PR235/(PR232+PR235)=83.3mV
Imax=16.6A
4. On time:
Ton=265~580ns
5.LoadLine:
Rcs=PR84/(PR83+PR84)*Rdcr
=5mohm

<Variant Name>

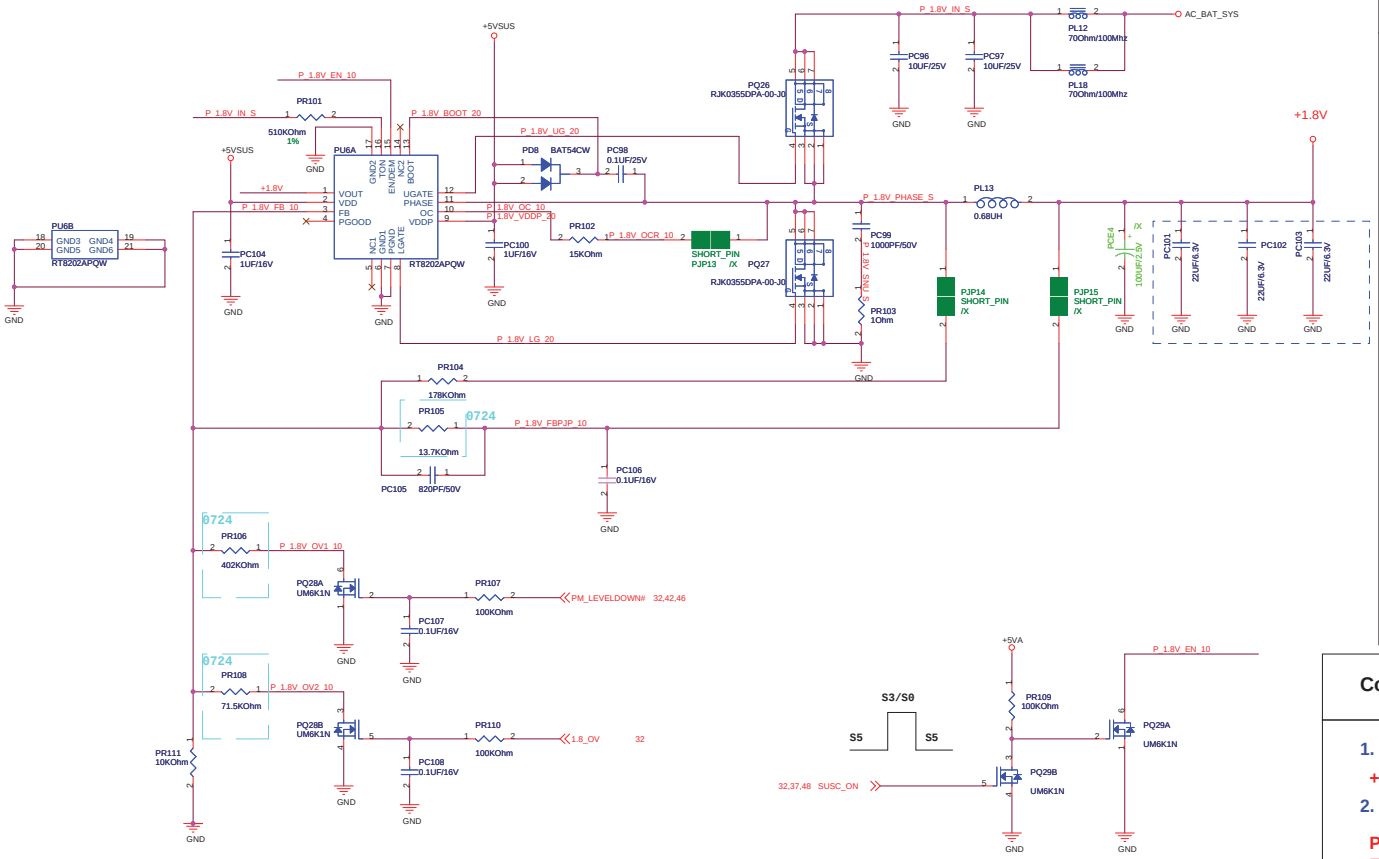
ASUSTeK COMPUTER INC. NB

Title : POWER_VCORE_RT8152

Engineer: Joy_zhou

Size	Project Name	Rev
C	1201i	1.0

Date: Friday, August 28, 2009 Sheet 44 of 54



PM_LEVELDOWN#	1.8_OV	Voltage	Status
L	L	1.778V	Power Saving
H	L	1.803V	Normal
H	H	1.931V	Performance

Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =1.7A

2. Ripple Current:

   I rip =2.72A
   I spec=2.5A

3. Dynamic:

   I peak=6.8A
   ESR / 1 pcs =18 mohm
   〉V =122.4mV

4. Inductor Spec:

   I SAC=25.5A
   IDC =15.5 A
   DCR=5mohm

5. MOSFET Spec:

   H-side MOSFET:RJK0355DPA-00-J0

   Rds(ON)= 16.5 mohm (Vgs=4.5 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

   L-side MOSFET: RJK0355DPA-00-J0

   Rds(ON)= 16.5 mohm (Vgs=4.5 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

Controller

1. Voltage & Current:

   +1.8V@6.8A

2. Frequency:

   PR101=510Kohm
   Fosc=480KHz

3. OCP:

   PR102=15K ohm -> 18A

4. POR:

   Vccrth =3.7~4.1V
   Vcchys=0.2V

5. UVP:

   Vout*70%

6. OVP:

   Vout*115%

7. Enable Voltage:

   V = 2.9V

8. Soft start time:

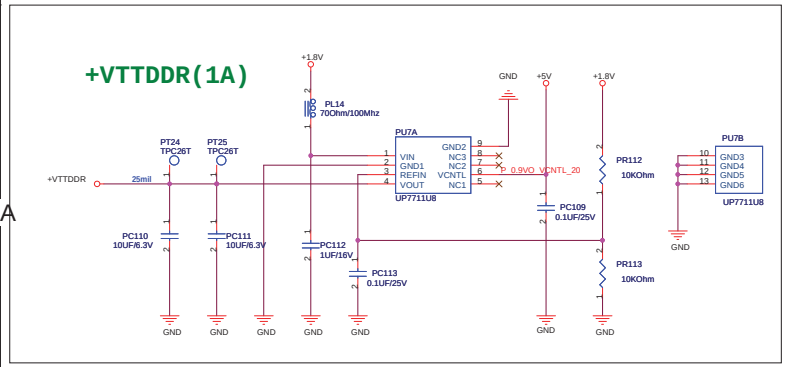
   Tss=1.2 ms

9. Phase selection:

   /X

10. Inrush Current:

   C total = 100 uF
   I inrush= 0.15 A



0.9VS@1 A

1. Dropout Voltage:

   〉V = 0.3V (Io = 2 A)

2. Current Limit:

   I limit = 4 A

3. Continue Current:

   I cont = 3 A

4. Power Dissipation:

   Rthjc = 52 /W
   Pd = 1.9 W

5. EN Voltage:

   V en = 1.4V
   V sd = 0.8 V

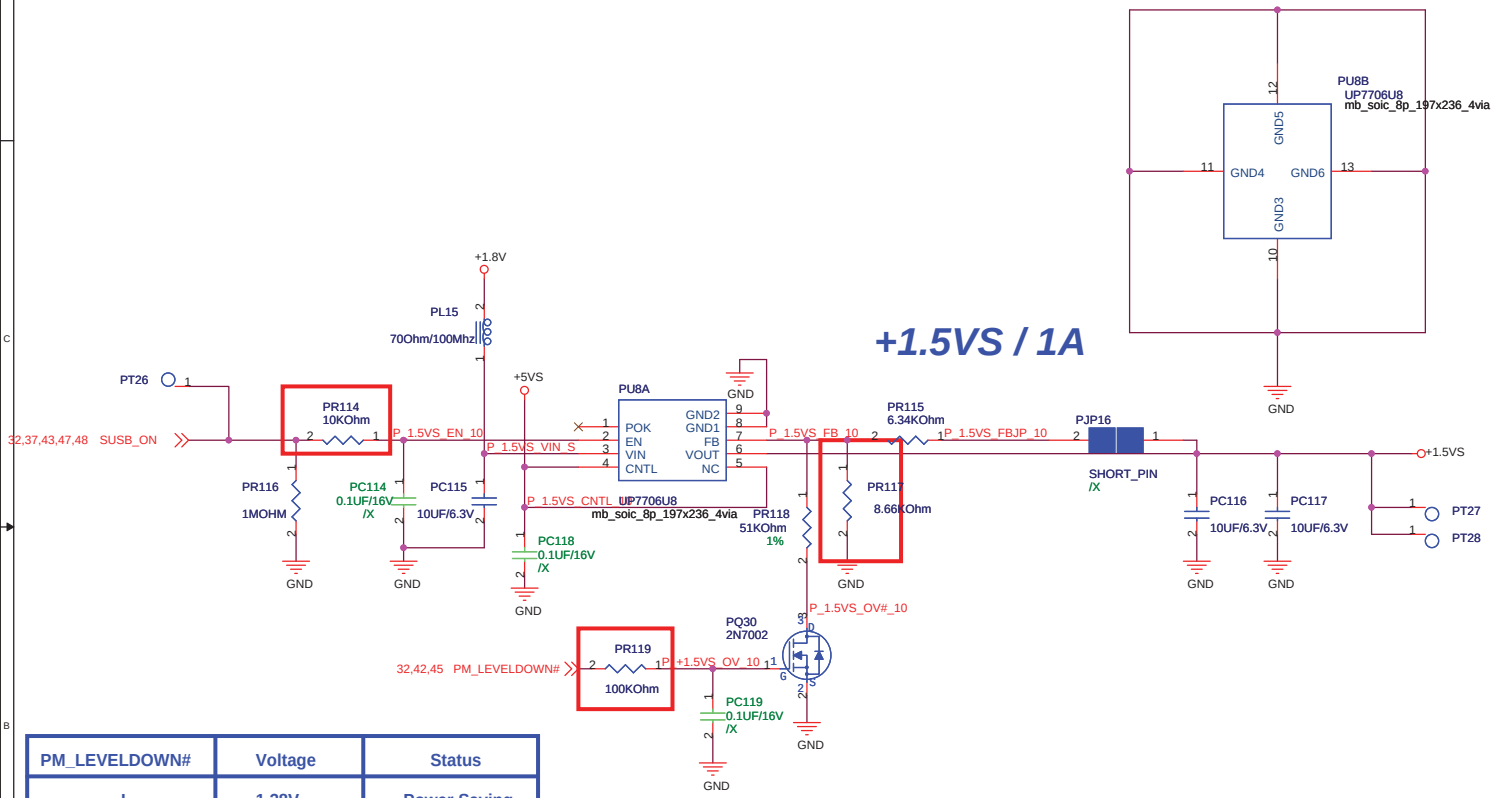
6. Supply Voltage:

   Vcc = 5 V

7. Inrush current:

   T ss = 5 ms
   C total = 10 uF
   I inrush = 3 mA

ASUS	Title : +1.8V&VTTDDR		
ASUSTek Computer INC	Engineer: Joy_Zhou		
Size A2	Project Name 12011		Rev <RevCode>
Date: Friday, August 28, 2009	Sheet 45 of 54		

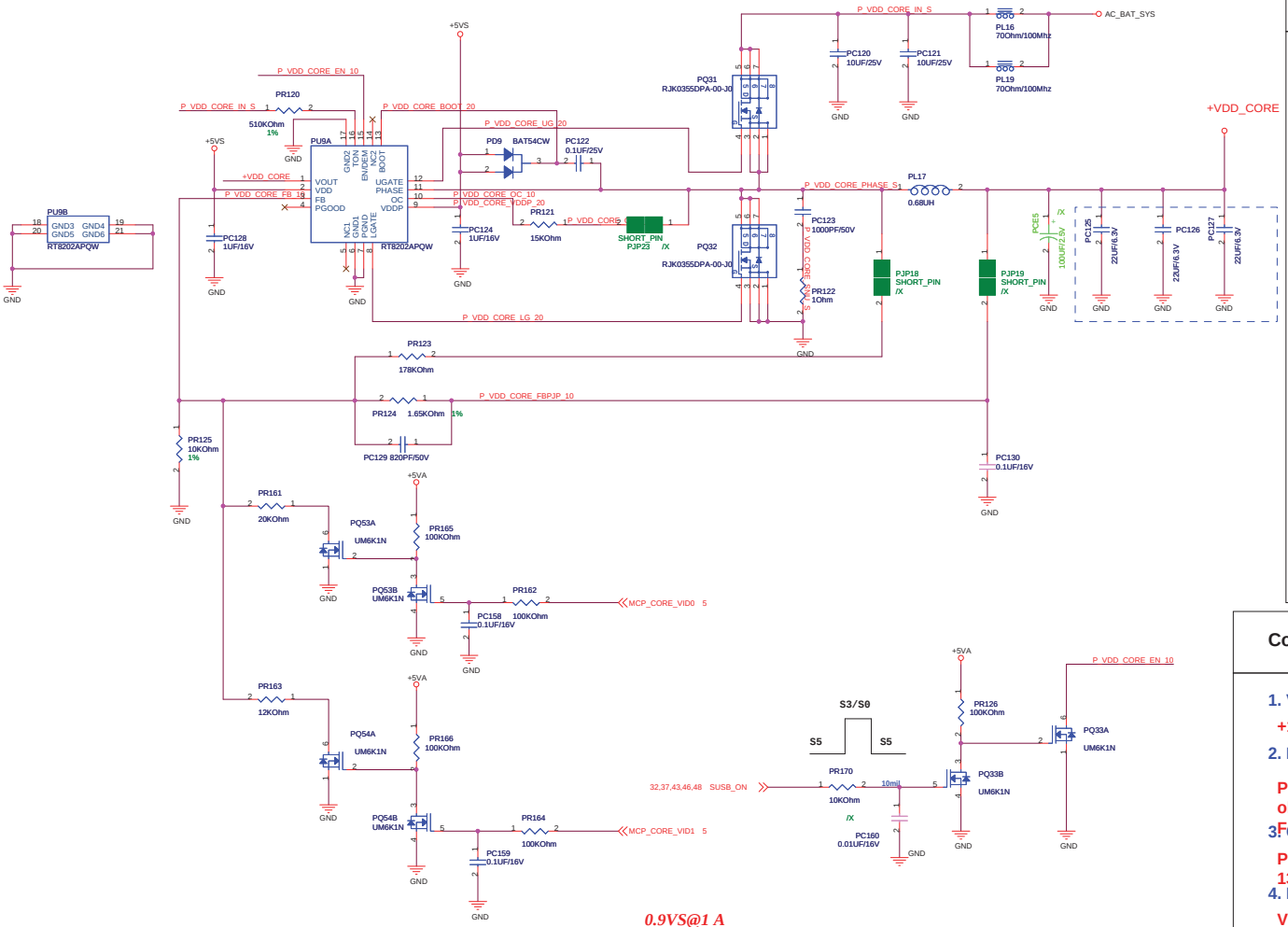


PM_LEVELDOWN#	Voltage	Status
L	1.38V	Power Saving
H	1.48V	Normal

1. Dropout Voltage:
   〉 V= 300 mV (Io=2 A)
2. Current Limit:
   I limit= 2.8 A
3. Continue Current:
   I cont= 1A
4. Pd:
   R thjc =5 C/W
   Pd =1.9W
5. EN Voltage:
   V rising = 1.4 V
   V falling = 0.4 V
6. Supply Voltage:
   Vcc=5V
7. Inrush current:
   Tss = 4 ms
   C total = 20 uF
   I inrush= 7.5mA

<Variant Name>

ASUS	Title : +1.5VS	
ASUSTek Computer INC.	Engineer: Joy_Zhou	
Size A3	Project Name 1201i	Rev 1.2
Date: Friday, August 28, 2009	Sheet 46 of 54	



Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =1.7A

2. Ripple Current:

   I rip =2.72A
   I spec=2.5A

3. Dynamic:

   I peak=6.8A
   ESR / 1 pcs =18 mohm
   〉V =122.4mV

4. Inductor Spec:

   I SAC=25.5A
   IDC =15.5 A
   DCR=5mohm

5. MOSFET Spec:

   H-side MOSFET: RJK0355DPA-00-J0

   Rds(ON)= 16.5 mohm (Vgs=4.5 V)
   I cont = 30 A (T =25)
   I peak = 120 A (Pause ≦10 us)

   L-side MOSFET: RJK0355DPA-00-J0

   Rds(ON)= 16.5 mohm (Vgs=4.5 V)
   I cont = 30A (T =25)
   I peak = 120 A (Pause ≦10 us)

Controller

1. Voltage & Current:

   +1.8V@6.8A

2. Frequency:

   PR120=510K ohm
   Fosc=480KHz

3. OCP:

   PR121=18K ohm -> 13.6A

4. POR:

   Vccrth =3.7~4.1V
   Vcchys=0.2V

5. UVP:

   Vout*70%

6. OVP:

   Vout*115%

7. Enable Voltage:

   V = 2.9V

8. Soft start time:

   Tss=1.2 ms

9. Phase selection:

   /X

10. Inrush Current:

   C total = 100 uF
   I inrush= 0.15 A

0.9VS@1 A

1. Dropout Voltage:

   〉V = 0.3V (Io = 2 A)

2. Current Limit:

   I limit = 4 A

3. Continue Current:

   I cont = 3 A

4. Power Dissipation:

   Rthjc = 52 /W
   Pd = 1.9 W

5. EN Voltage:

   V en = 1.4V
   V sd = 0.8 V

6. Supply Voltage:

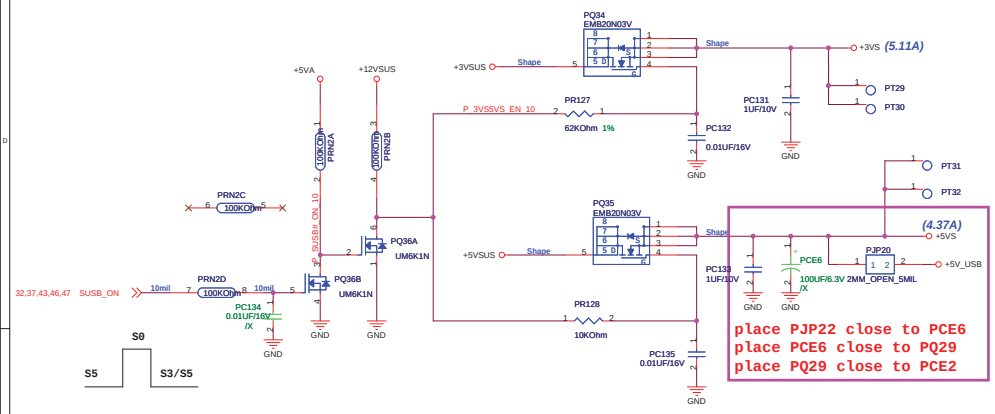
   Vcc = 5 V

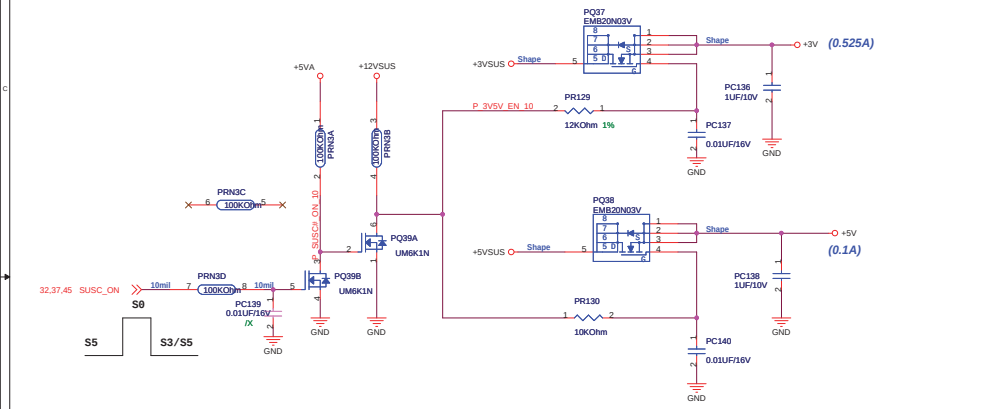
7. Inrush current:

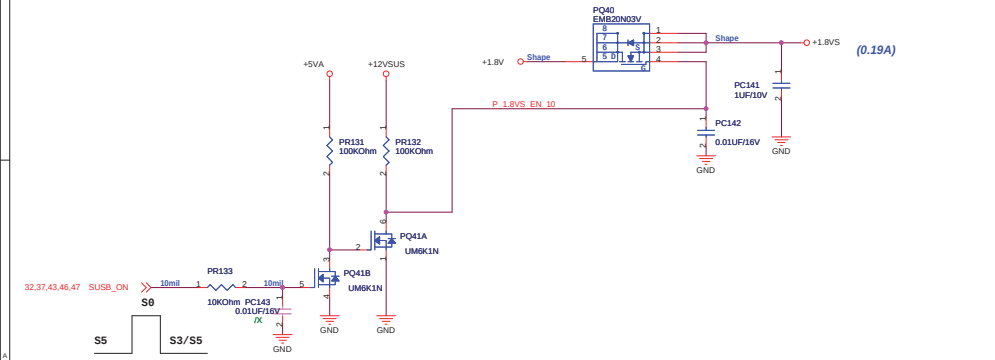
   T ss = 5 ms
   C total = 10 uF
   I inrush = 3 mA

VID2	VID1	VID0	Voltage	Status
L	L	L	0.88V	N/A
L	L	H	1V	Normal
L	H	L	0.95V	Performance
L	H	H	0.9V	Power Saving

ASUS	Title : +1.8V&VTTDDR	
ASUSTek Computer INC	Engineer: Joy_Zhou	
Size A2	Project Name 1201i	Rev <RevCode>
Date: Friday, August 28, 2009	Sheet 47 of 54	



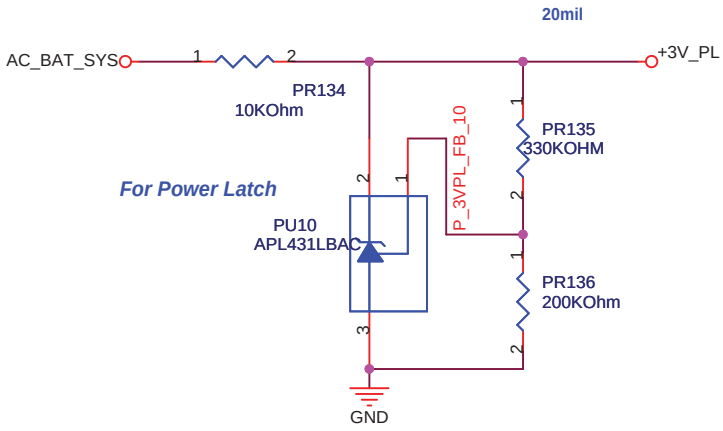


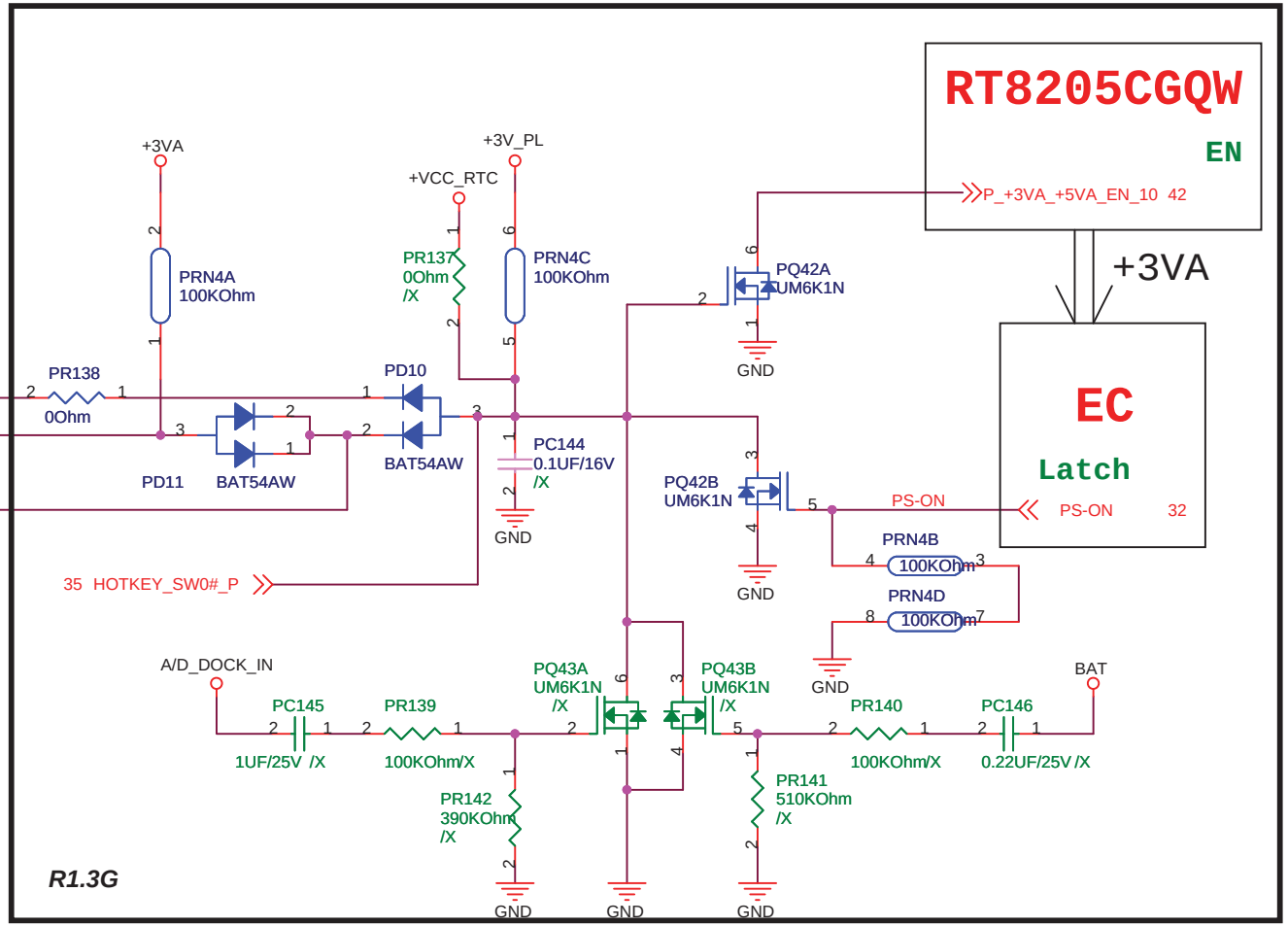


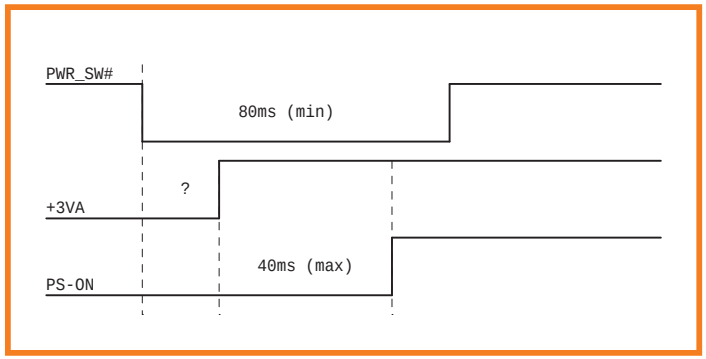
<Variant Name>

ASUS	Title :	Power_Load Switch
ASUSTek Computer INC.	Engineer:	Joy_Zhou
Size: A2	Project Name: 12011	Rev: 1.2
Date: Friday, August 28, 2009	Sheet 48 of 54	

+3V_P L







<Variant Name>

ASUS	Title : Power Latch	
ASUSTek Computer INC.	Engineer: Jerry Liu	
Size A4	Project Name 1201i	Rev 1.0
Date: Friday, August 28, 2009	Sheet 49 of 54	

Title : HISTORY			
<OrgName>	Engineer: <OrgAddr1>		
Size A3	Project Name 1201HA		Rev 1.0
Date: Friday, August 21, 2009	Sheet 50 of 54		

DATE 0706

1. P40,Delete some EMI CAP,add RF CAP EC58
2. P23,3G_RST# PU POWER change from +3VS to +3V_3G
3. P15,SCH_GPIO_0 PD R93 change from 10k to 1K
4. P16,+5VS_REF ADD serial R109
5. P22,+3V_LCD ADD GR15/PQ40
6. P23,+3V_3G GR21/GR22 change to 0805
7. P35,L26 change to 0 OHM
7. P7,CLK_PCIE_3G/CLK_PCIE_3G# add reserved CAP C476/C477

DATE 0707

1. P13,SDVO BUS/PCIE add net name before capacitor
2. P22,LVDS CON change part number to 12G17101020K
3. P40, add EMI CAP EC52/EC54
3. P29, add power switch for debug

DATE 0708

1.Delete test point T27/T28

2.ADD D6/OR30

3.Add net name for PCIE BUS

ASUS	Title : HISTORY	
<OrgName>	Engineer: <OrgAddr1>	
Size A3	Project Name 1201HA	Rev 1.0
Date: Monday, July 20, 2009	Sheet 51 of 54	

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	LPC_RST#	I	
14	GPIO07	CRT_IN	I	100K pull high to +3VA
15	GPIO08	EXT_SMI#	O	
16	GPIO0A	LID_EC_R#	I	Internal pull high
17	GPIO0B/ESB_CLK	PCB_ID0	I	8.2K pull down to GND
18	GPIO0C/ESB_DAT	PCB_ID1	I	8.2K pull down to GND
19	GPIO0D	LID_EC_L#(no use)	I	Internal pull high
20	GPIO0E/SCI#	KBC_SCI#	O	10K pull high to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#(no use)	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	100K pull high to +3VSUS
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM(no use)	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH(no use)	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX(no use)	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX(no use)	I	RS232 debug port
32	GPIO18	PWR_SW_EC#	I	100K pull high to +3VA
34	GPIO19/PWM3	PS-ON	O	latch power, 200K pull down to GND
36	GPIO1A/NUMLED	NUM_LED#(no use)	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#(no use)	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A(no use)	I	
64	GPI39/AD1	BAT_B(no use)	I	
65	GPIO3A/AD2	BAT_C(no use)	I	
66	GPIO3B/AD3	BAT_D(no use)	I	
68	GPO3C/DA0	CHG_EN#	O	100K pull high to +3VA

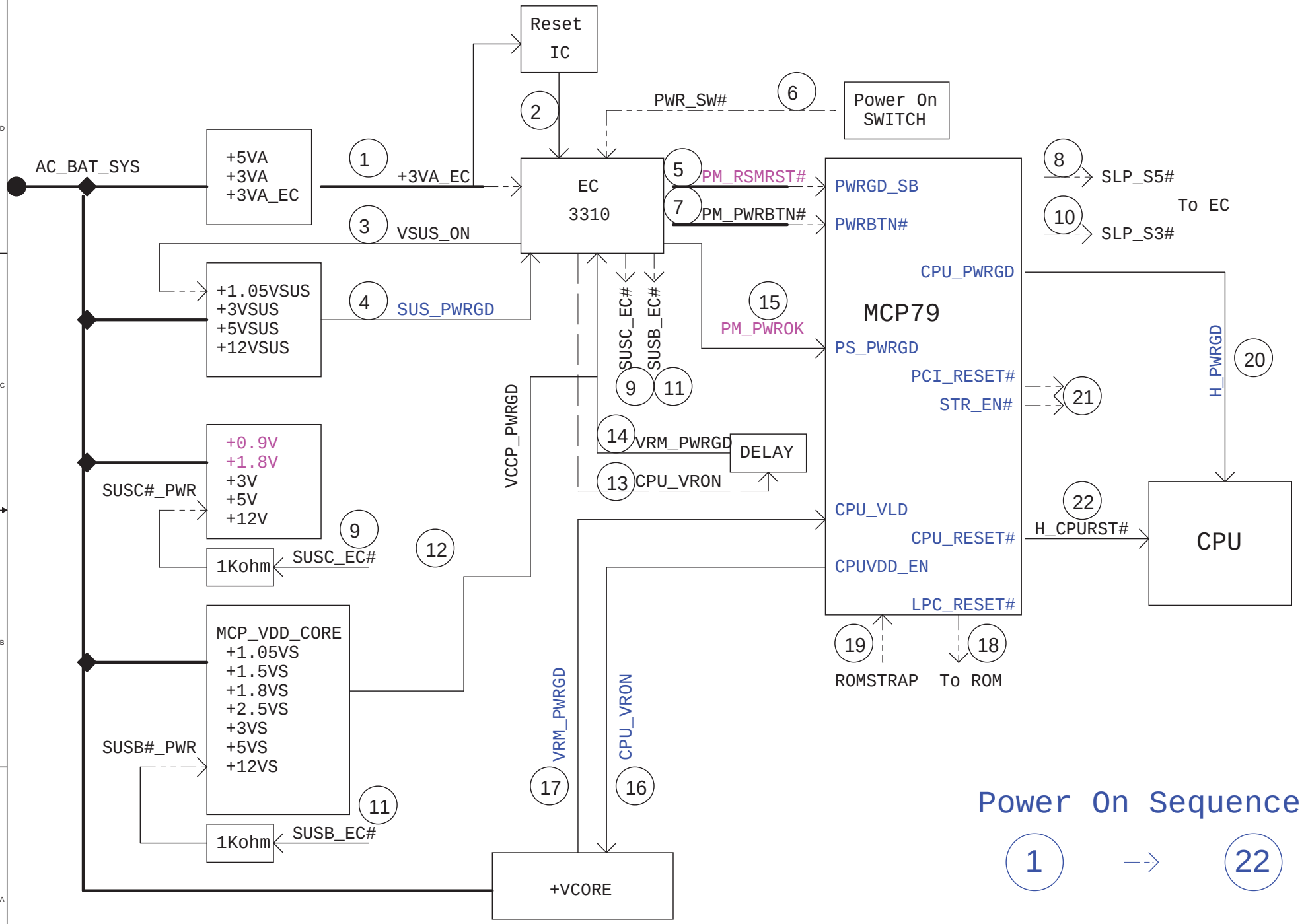
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	Default High
72	GPO3F/DA3	BAT_LL#(NO USE)	O	Battery Low Low
73	GPIO40	AC_OK	I	100K pull high to +3VA
74	GPIO41	EC_RSMRST#	O	100K pull down to GND
75	GPI42	BAT_IN	I	100K pull high to +3VA
76	GPI43	BAT2_IN(no use)	I	Batt1 (Small/Internal): 1 present, 0 absent (to GND)
77	GPIO44/SCL1	SMB1_CLK	I/OD	4.7K pull high to +3VA
78	GPIO45/SDA1	SMB1_DATA	I/OD	4.7K pull high to +3VA
79	GPIO46/SCL2	SMB2_CLK	I/OD	10K pull high to +3VS
80	GPIO47/SDA2	SMB2_DATA	I/OD	10K pull high to +3VS
81	GPIO48/KSO16	KB_ID0(no use)	I	for KB type detection
82	GPIO49/KSO17	KB_ID1(no use)	I	for KB type detection
83	GPIO4A/PSCLK1	1.8_OV	O	10K pull down to GND; default low
84	GPIO4B/PSDAT1	NC	I	
85	GPIO4C/PSCLK2	NC	O	
86	GPIO4D/PSDAT2	NC	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3VS
88	GPIO4F/PSDAT3	TP_DATA	I/OD	10K pull high to +3VS
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_ORANGE#	O	Orange charger LED
91	GPIO53/CAPLED	CAPS_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRL_LED#(no use)	O	
95	GPIO56	GS1_INT1(no use)	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON_EC	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	CNT1_CHG#(no use)	O	
103	GPXOA06	PM_LEVELDOWN#	O	Default High
104	GPXOA07	CNT2_CHG#(no use)	O	
105	GPXOA08	CNT2_CHG#(no use)	O	
106	GPXOA09	SPI_WP#	O	10K pull high to +3VA
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	100K pull down to GND
109	GPXID0/SDIDI	EC_PWROK	O	100K pull down to GND
110	GPXID1	CPU_LEVELUP#	O	Default High
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SUSB#	I	100K pull down to GND
115	GPXID4	PM_SUSC#	I	100K pull down to GND
116	GPXID5	VRM_PWRGD_EC	I	100K Pull high to +3VS
117	GPXID6	VSUS_PWRGD	I	100K Pull high to +3VA
118	GPXID7	NC	O	
121	GPIO57	GS1_INT2(no use)	I	Internal pull high
126	GPIO58/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_KBCLPC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA
67	AVCC	+3VA_AEC	P	
69	AGND	GND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_DO	I	
120	WR#/SPIDO	SPI_DI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	K_V18R	P	Reserved 4.7uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

<Variant Name>

ASUSTek Computer INC.	Title : EC Pin Define		
	Engineer: N/A		
Size A3	Project Name 1201HA		Rev 1.0
Date: Wednesday, August 12, 2009	Sheet 52 of 54		



ASUS	Title : PowerOn sequence		
ASUSTeK COMPUTER INC	Engineer: MIRO TSAI		
Size: Custom	Project Name: 1201I		Rev: 2.0g
Date: Wednesday, July 29, 2009	Sheet 53 of 54		

S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for AC_OK until adaptor power is good, then

2.At least 5mS after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.

3.At least 20mS after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)

4.EC asserts RSTWARN.

5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

6.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

7.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

8.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

10.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

11.Waiting for RSTRDY# until deasserted by SCH.

12.RESET# can be deasserted at lease 100uS after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

1.Waiting for BAT_IN until battery power is good, then

2.Waiting for PWR_SW# until user is pressed.

3.EC asserts VSUS_ON to enable VSUS power.

4.At least 20mS after VSUS power is stable.

5.EC asserts RSTWARN.

6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.

7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.

8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.

9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.

10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.

12.Waiting for RSTRDY# until deasserted by SCH.

13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).

2.At least 20mS after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.

3.Waiting for SLPRDY# until has been asserted.

4.EC asserts RSTWARN to SCH to begin internal sequence.

5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.

6.EC asserts RESET# after detecting RSTRDY# asserted.

7.EC deasserts ICH_PWROK.

8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

9.EC asserts PM_RSMRST#.

10.EC deasserts SUSC_ON to turn off the other power planes.

11.EC deasserts VSUS_ON if in battery mode.

12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.

2.For external wake event (PWR_SW#, keyboard wake up), then

3.EC asserts PM_PWRBTN# at least 50mS to wake SCH, and waiting for SLPRDY# until SCH deasserted.

4.EC asserts SUSB_ON to enable SUSB power.

5.CPU_VRON is deasserted at least 100mS after SUSB power is stable.

6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.

7.At least 5mS after receiving CPUPWR_GD, ICH_PWROK is asserted.

8.Deasserts RSTWARN after ICH_PWROK is asserted.

9.RESET# can be deasserted 100uS after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# for 1200mS to SCH after asserts RSTWARN.

4.EC deasserts RSTWARN.

5.EC deasserts RESET# after at least 100uS delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.

2.EC asserts RSTWARN to SCH.

3.EC asserts RESET# to SCH after asserts RSTWARN.

4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.

5.EC asserts PM_RSMRST# after CPU_VRON power is off.

6.EC disables SUSC_ON power for 3~5 seconds.

7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.