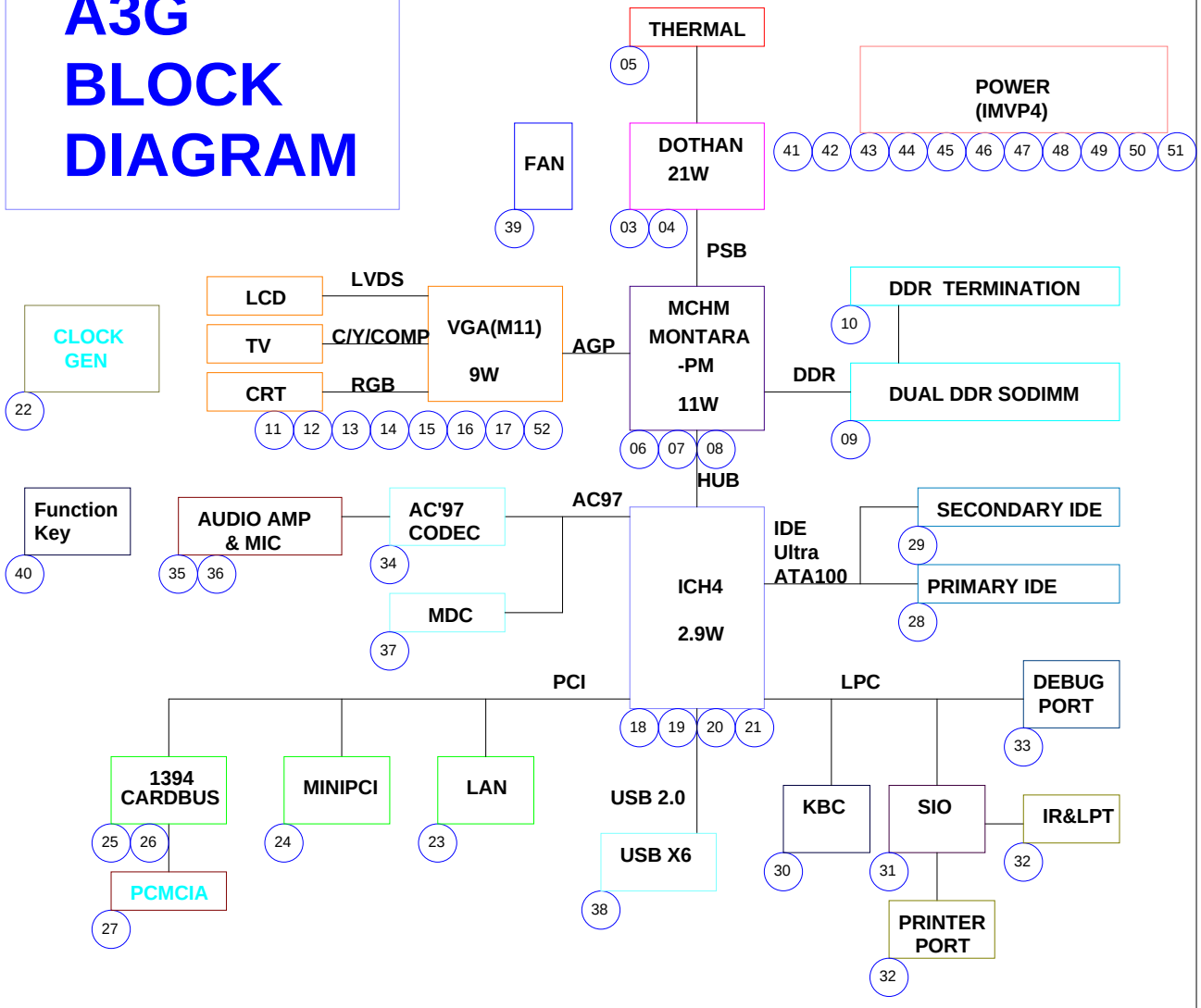
A3G BLOCK DIAGRAM



FILE LIST

01

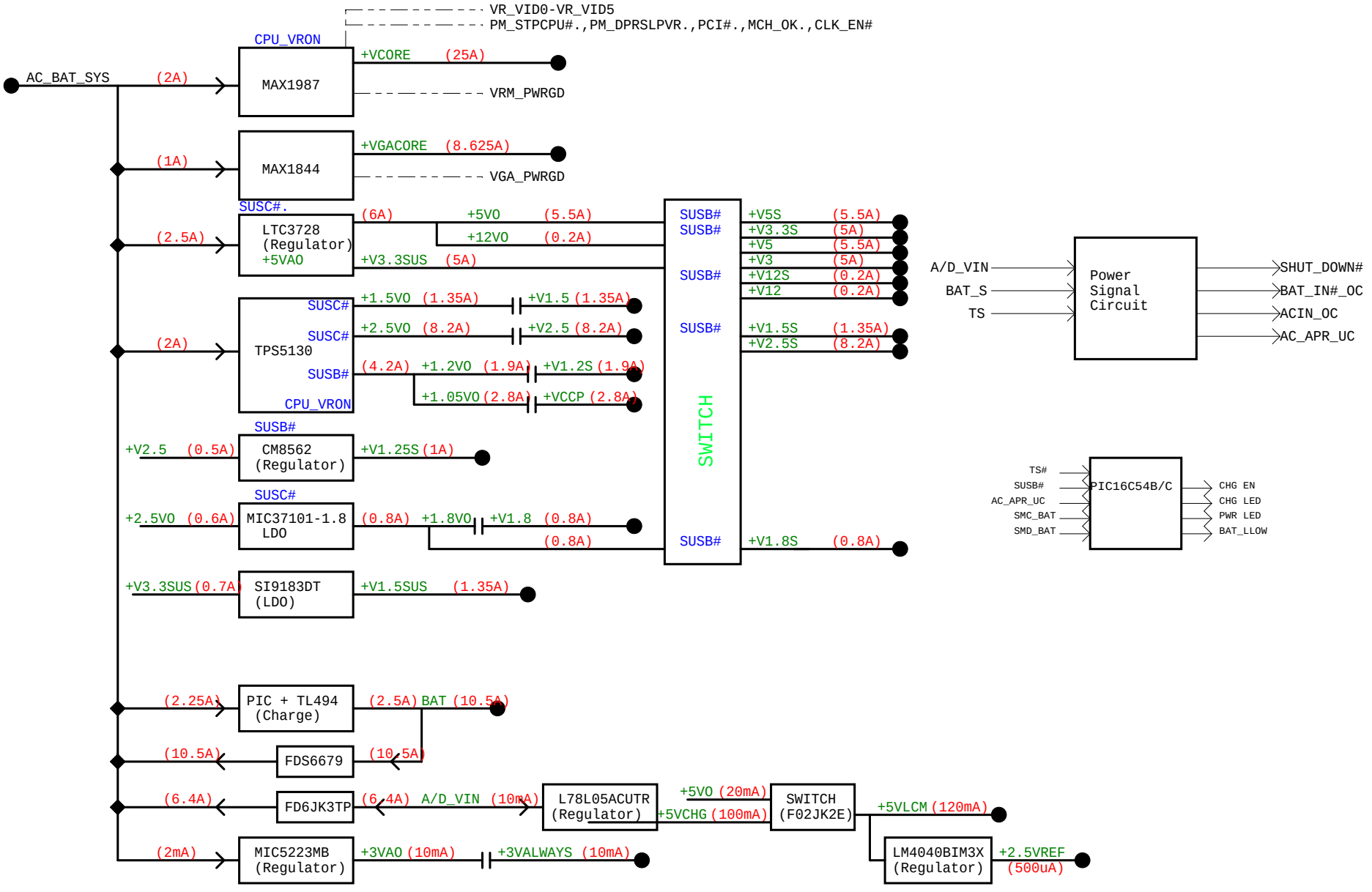
ASUSTECH CO.,LTD.

Title : BLOCK DIAGRAM

Engineer: HD_NB TEAM

Size	Project Name	Rev
C	A3G	1.2

Date: Thursday, August 19, 2004 Sheet 1 of 53



Title :	POWER DIAGRAM
ASUSTECH CO.,LTD.	Engineer: EDDY ZHAO
Size: C	Project Name: A3G
Rev: 1.2	
Date: Thursday, August 19, 2004	Sheet 2 of 57

CPU Pin A1 need to be enlarged(M)

WIDTH: 5 mils
SPACE >= 1:2
GROUP SPACE >=1:5
Breakout Length:<=200 mil
LENGTH: 1" - 6.5"(OPT: 4"+/-0.5")
(#0011)

WIDTH:4mils
SPACE >= 1:2
STROBE SPACE >=1:3
GROUP SPACE >=1:5

LENGTH: 0.5" - 6.5"
(#0012)

WIDTH:4mils
SPACE >= 1:3
GROUP SPACE >=1:5

LENGTH: 0.5" - 5.5"
(#0012)

Here IERR# is not routed as a test point or to any optional system receiver

RESET# Signal Routing with NO ITP700FLEX Connector

CPU PLL CIRCUITS

Close to Pin VCCA[3..1] of CPU

TOPOLOGY 2A:
Open Drain (OD) Signal
R-CPU-ICH Y-FORK
CPU-ICH: 0.5" - 12"
R - CPU <= 3"
(#0013)

TOPOLOGY 1B:
Open Drain (OD) Signal
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)

TOPOLOGY 2B:
CMOS Signals
MCH-CPU-ICH4
MCH-CPU:0.5"-6.5"
CPU-ICH4:0.5"-12"
(#0013)

TOPOLOGY 1C:
Open Drain (OD) Signal
CPU-R-LSC-ICH
CPU-R: 0.5" - 12"
R - LSC<= 3"
LSC-ICH:0.5"-12"

TOPOLOGY 2C:
CMOS Signals:
LINT0/INTR,LINT1/NMI,A20M#,
IGNNE#,SLP#,SMI#,and STPCLK#
CPU-ICH:0.5" - 12"

TOPOLOGY 3:
CMOS Signals
CPU-ICH-R-LSC-FWH
CPU-ICH:0.5" - 12"
R - LSC <= 3"
LSC-FWH:0.5"-6"(#0013)

TOPOLOGY 1B:
Open Drain (OD) Signal
CPU-ICH-R
CPU-ICH: 0.5" - 12"
ICH-R <= 3"
(#0013)

H_GTLREF0
LENGTH <=0.5"
WIDTH = 5 mils
SPACE >= 25 mils
X BPSB(#0004)

Close to Pin AD26 of CPU

CPU_COMP2 :
Analog
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)

CPU_COMP0 :
Analog
Length <= 0.5"
Width = 20 mils(L1/L4)
Space>= 25 mils
X BPSB(#0001)

CPU_COMP3 :
Analog
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)

CPU_COMP1 :
Analog
Length <= 0.5"
Width = 5 mils
Space>= 25 mils
X BPSB(#0001)

Pin AD1,AC2 of BANIAS

CPU DEBUG PORT

Close to Pin A8 of CPU

Close to Pin A12 of CPU
Width= 5 mils
Length <= 2"

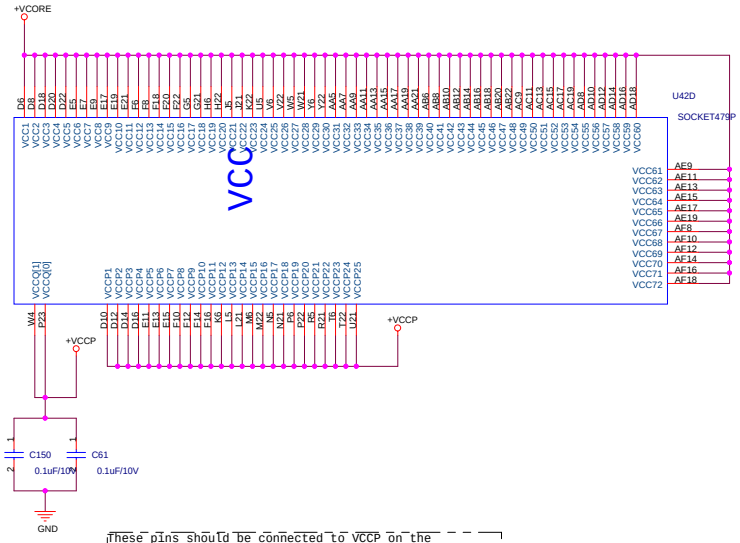
CPU JTAG

Project Name	Rev
A3G	1.2

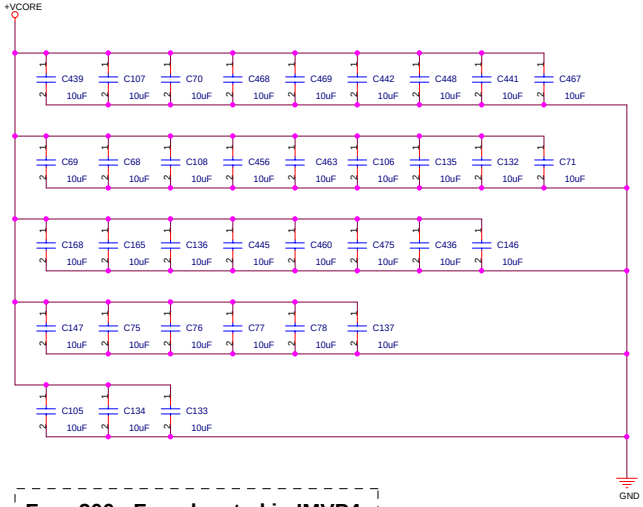
Title : CPU-DOTHAN(HOST)
ASUSTECH CO.,LTD.
Engineer: EDDY ZHAO
Size: C
Date: Thursday, August 19, 2004
Sheet 3 of 57

Target VCC (Std Voltage) :
HFM: 1.308V
LFM: 0.956V
Target Deeper Sleep Vcc = 0.745 V

TDP:
21W (Std Voltage)
10W (Low Voltage)
5W (Ultra Low Voltage)



These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.

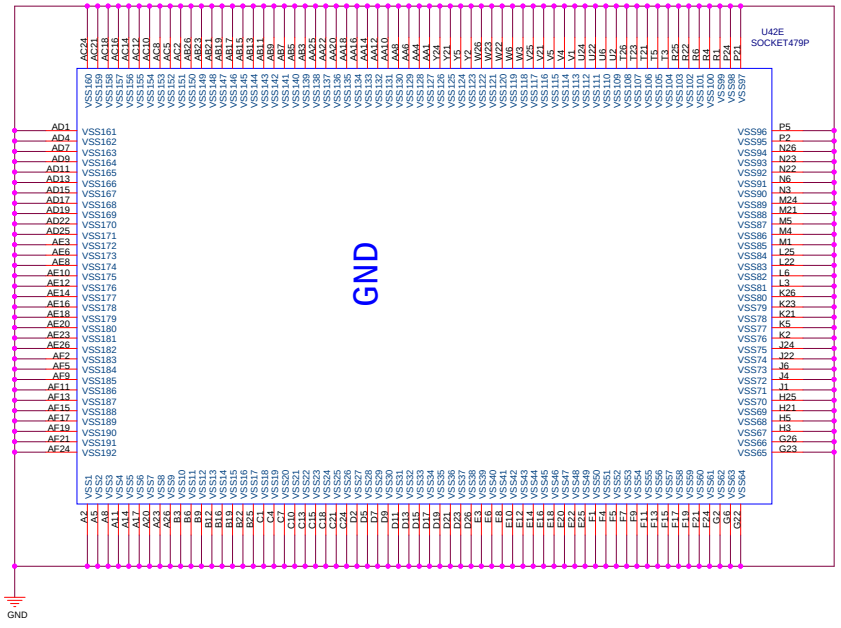


Four 200 uF are located in IMVP4

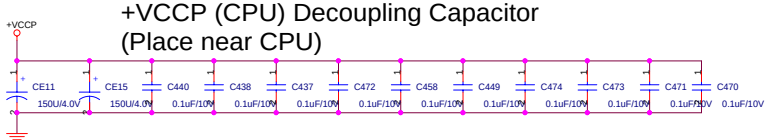
Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling



+VCCP (CPU) Decoupling Capacitor (Place near CPU)



Two 150-UF POSCAPs with an ESR of 36 mOhm(typ) should be used for bulk decoupling. One capacitor should be placed next to the processor socket and one capacitor in close proximity to the MCH package.

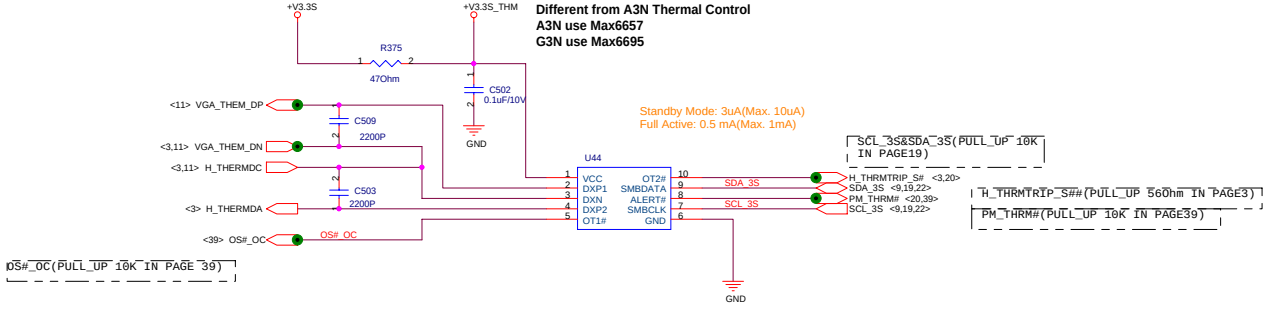
Ten 0.1-UF X7R capacitors in a 0603 form factor should be placed on the secondary side of the motherboard under the processor socket cavity next to the VCCP pins of the processor. Five capacitors should be spread out near the Data signal side and five capacitors near the Address signal side of the processor socket's pin-map.

ASUSTECH CO.,LTD.
Title : CPU-DOTHAN(PWR)
Engineer: EDDY ZHAO
Size: C | Project Name: A3G | Rev: 1.2
Date: Thursday, August 19, 2004 | Sheet 4 of 57

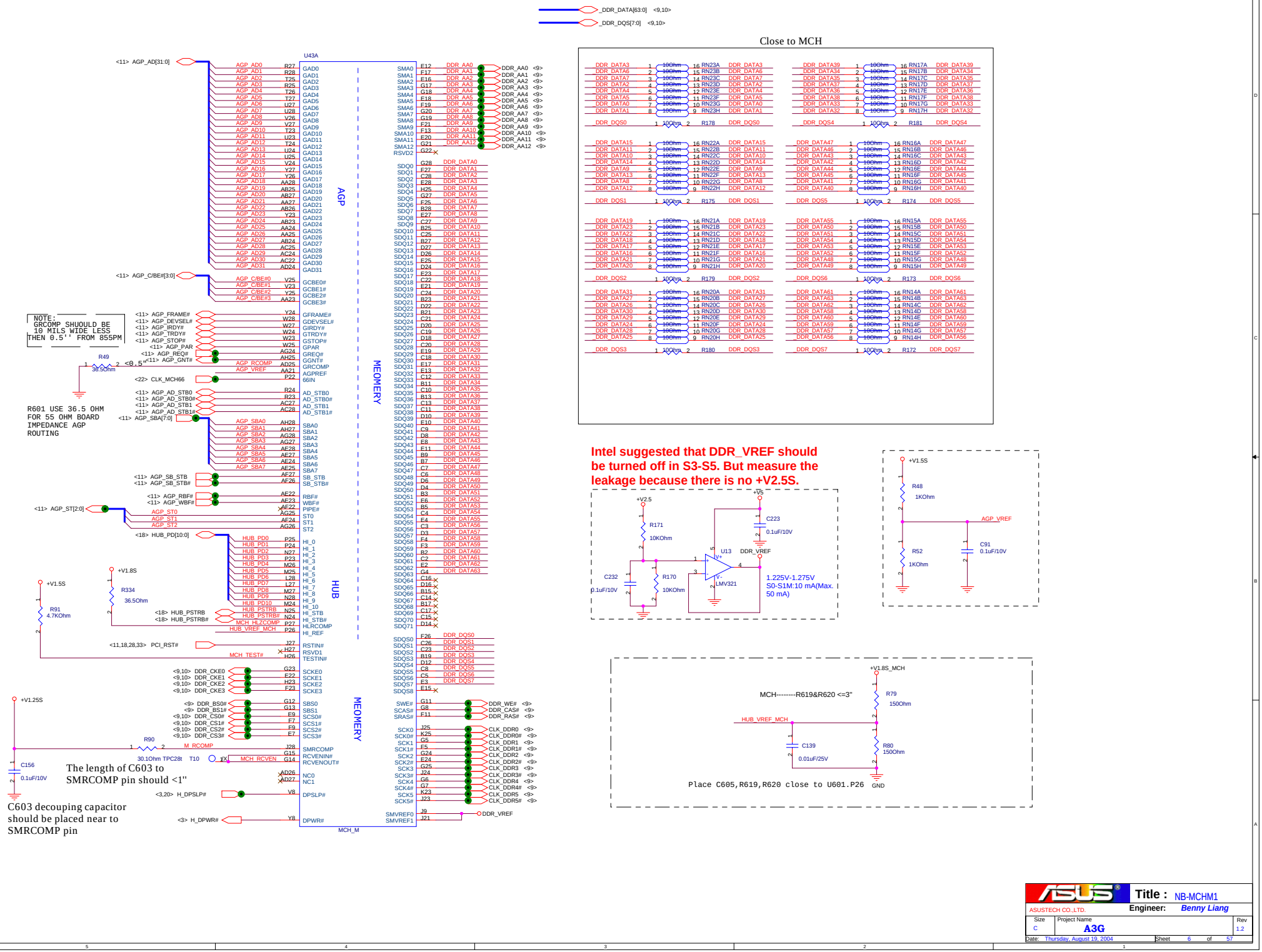
Route H_THERMDA and H_THERMDC on the same layer
Route VGA_THEM_DP and VGA_THEM_DN on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

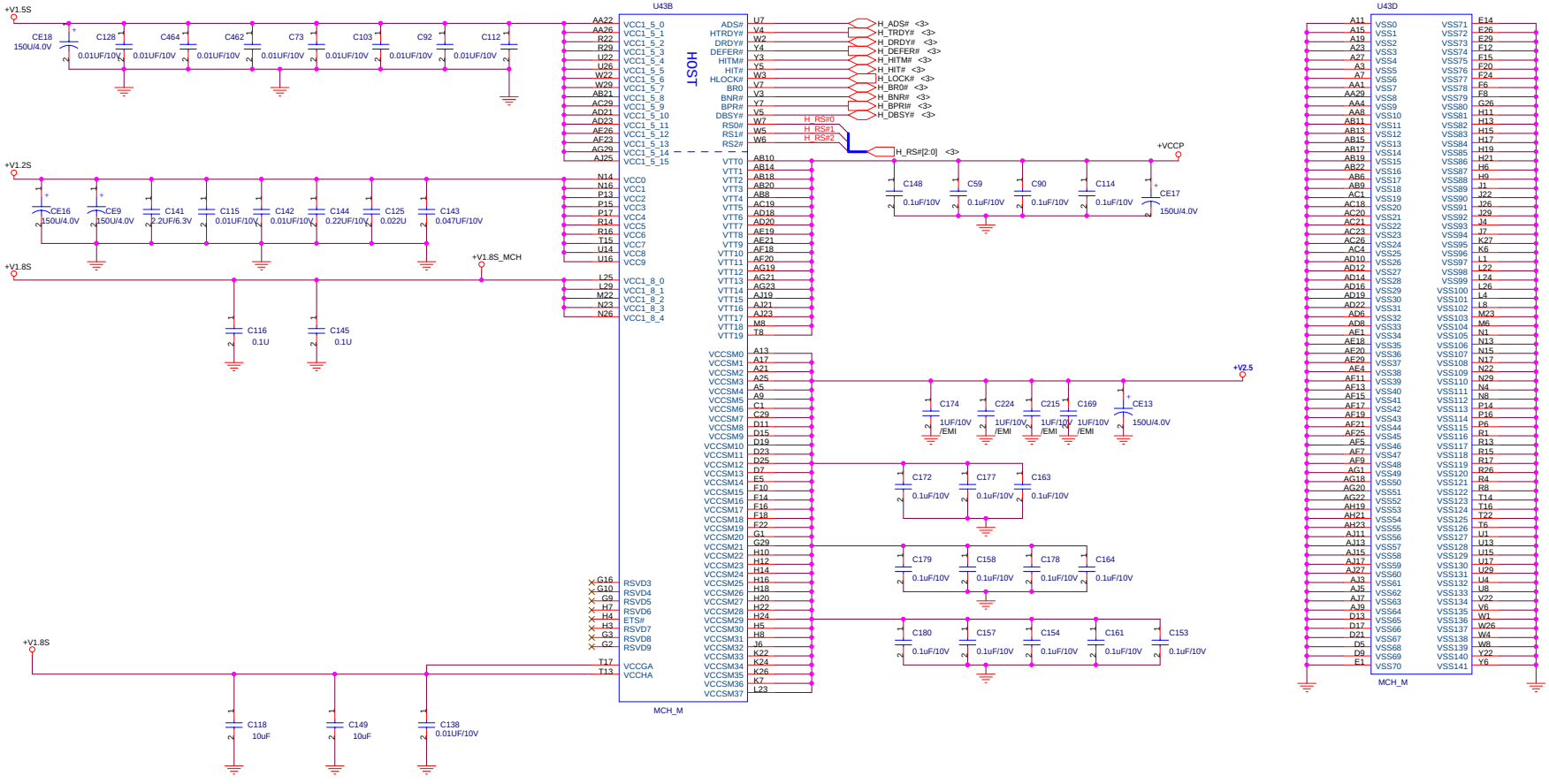


ASUSTECH CO.,LTD.	Title : THERMAL	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 5 of 57	

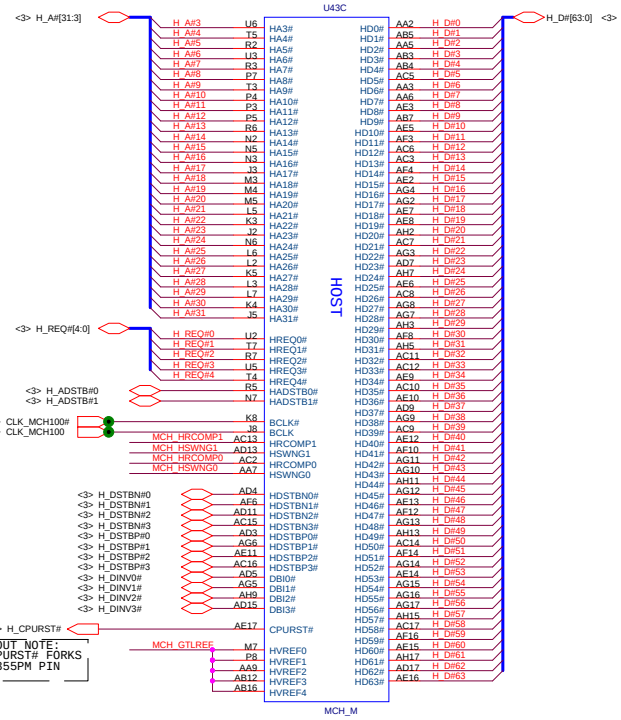


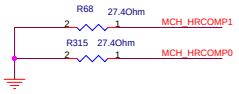
ASUSTEK COMPUTER INC.	Title : NB-MCHM1		
	Engineer: Benny Liang		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 6 of 57		

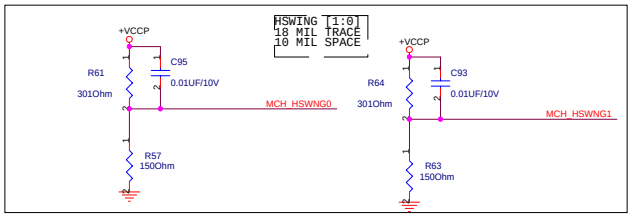
All decoupling capacitances should Be
placed near to the associated pins.



ASUSTEK CO.,LTD.	Title : NB-MCHM2	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 7 of 57	

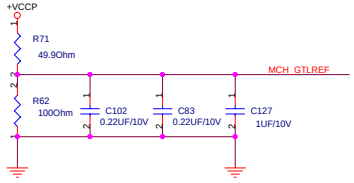






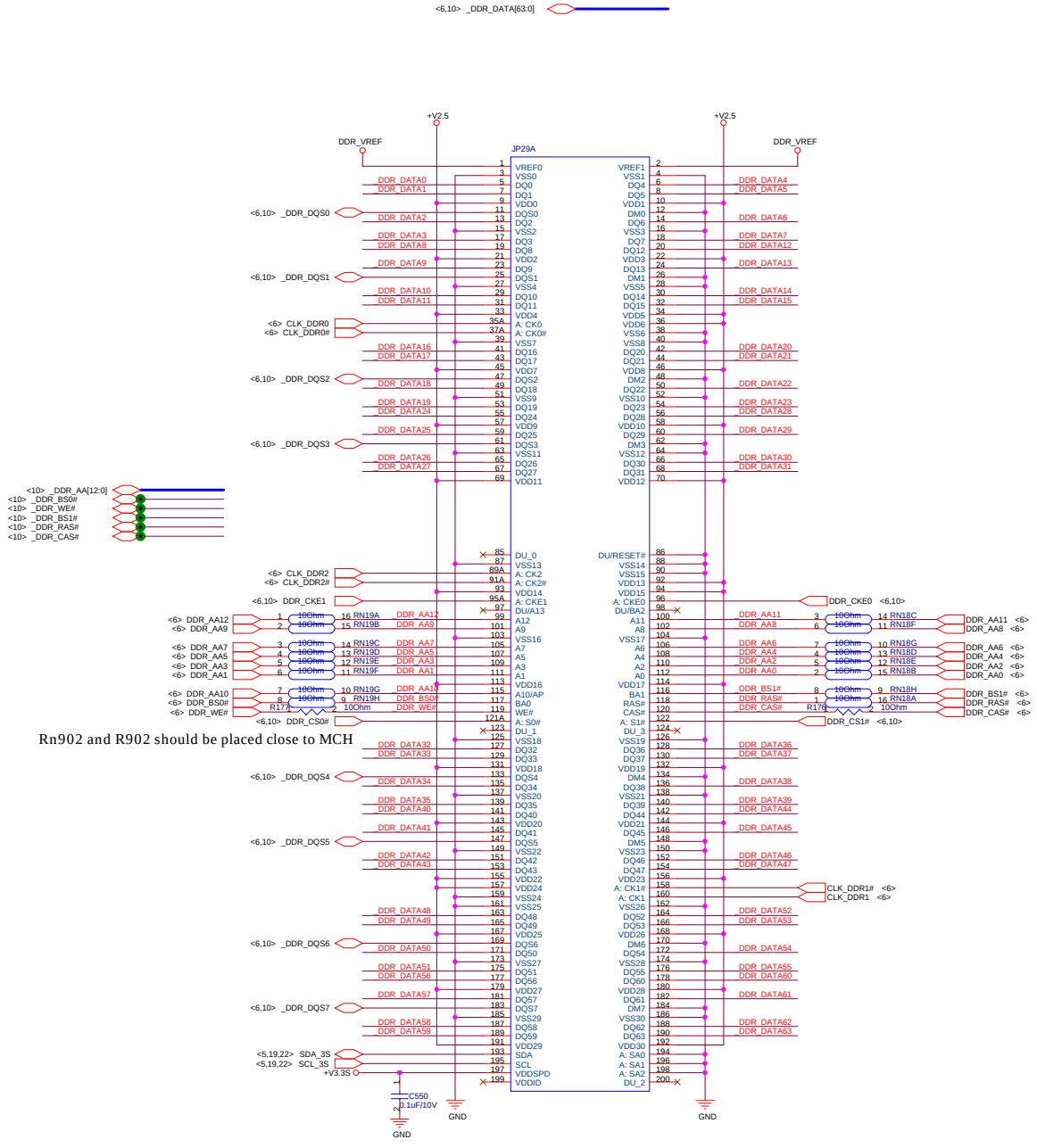
C801 should be placed closer to de HSWNG0 than R805 and R807

C802 should be placed closer to de HSWNG1 than R806 and R808



Place R809 close to HVREF4 and R810 close to HVREF1

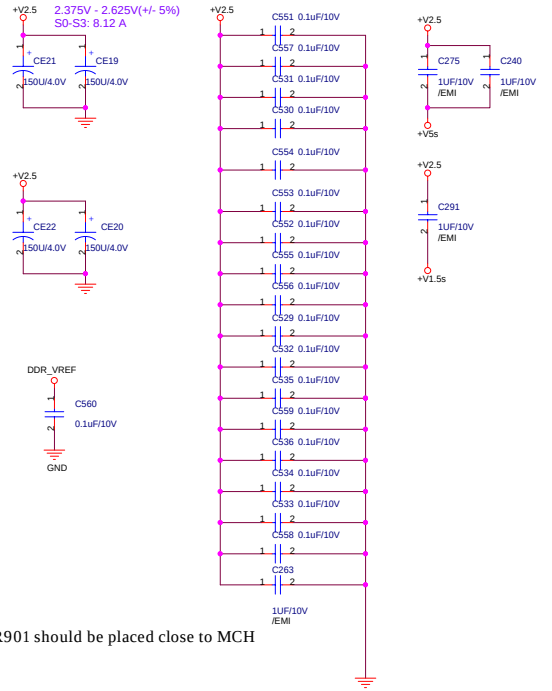
ASUSTECH CO.,LTD.	Title : NB-MCHM3	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 8 of 57	



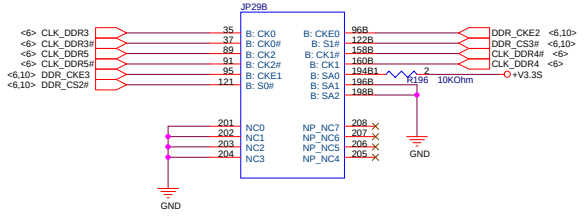
Rn902 and R902 should be placed close to MCH

All decoupling capacitances should Be placed near to the associated pins.

FOR +V2.5 DECOUPLING

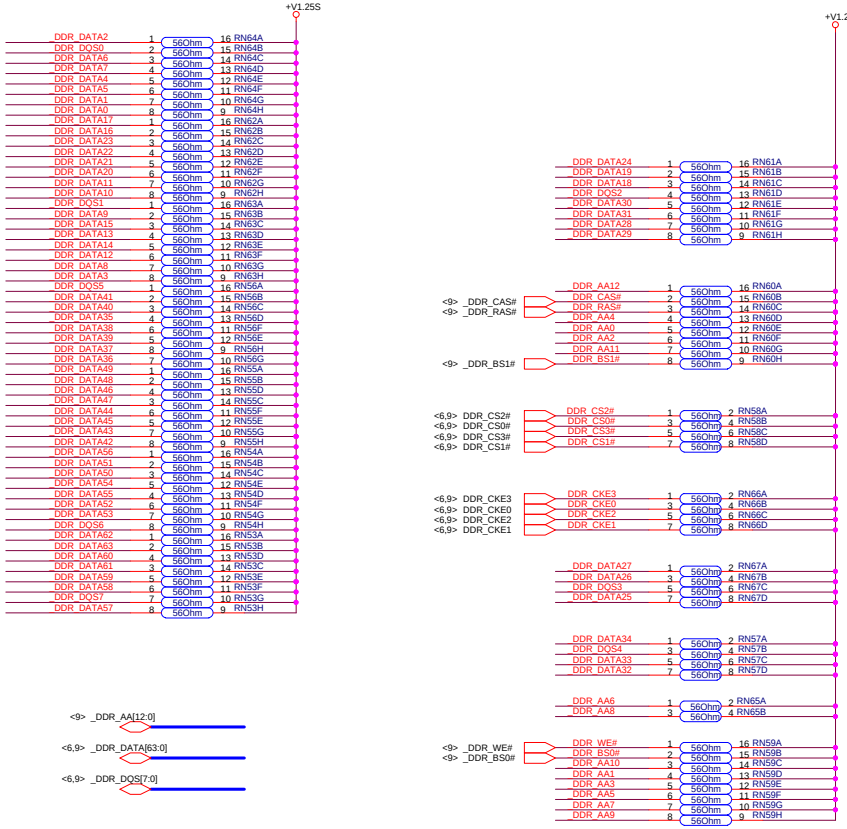


Rn901 and R901 should be placed close to MCH



ASUSTEK CO.,LTD.	Title : DUAL_DDR	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 9 of 57	

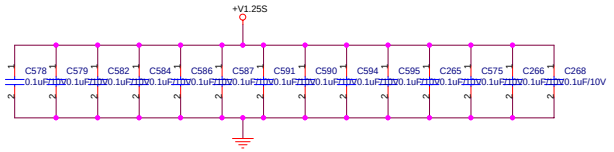
All termination registers should Be placed near to the associated pins of SO-DIMM1

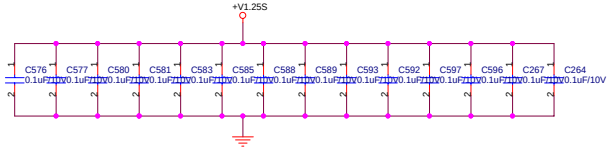


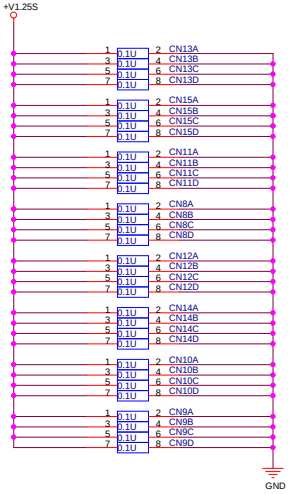
FOR +V1.25S DECOUPLING

Place one cap between every 2 pullup resistors to +V1.25S

All decoupling capacitances should Be placed near to the associated pins.

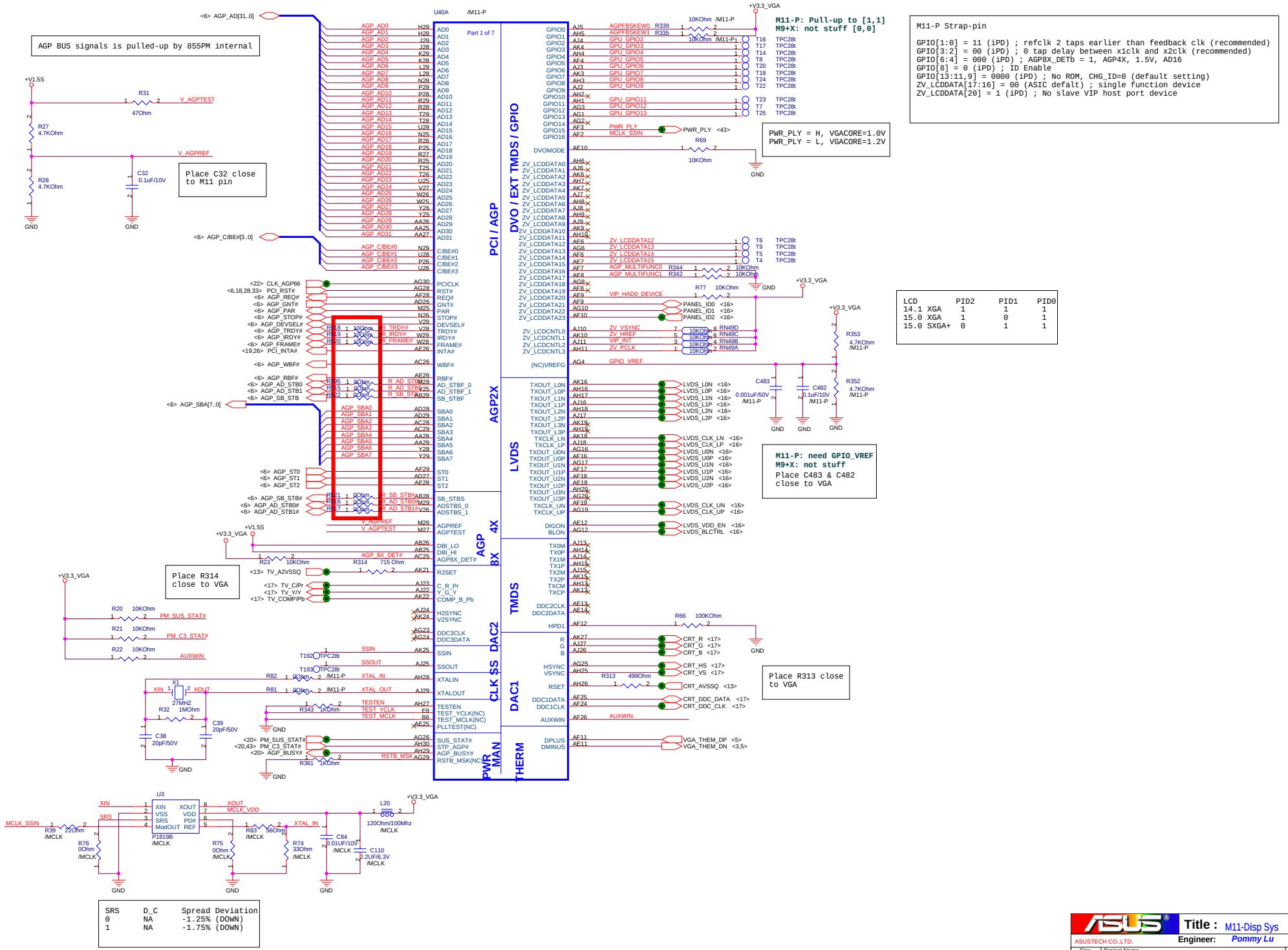


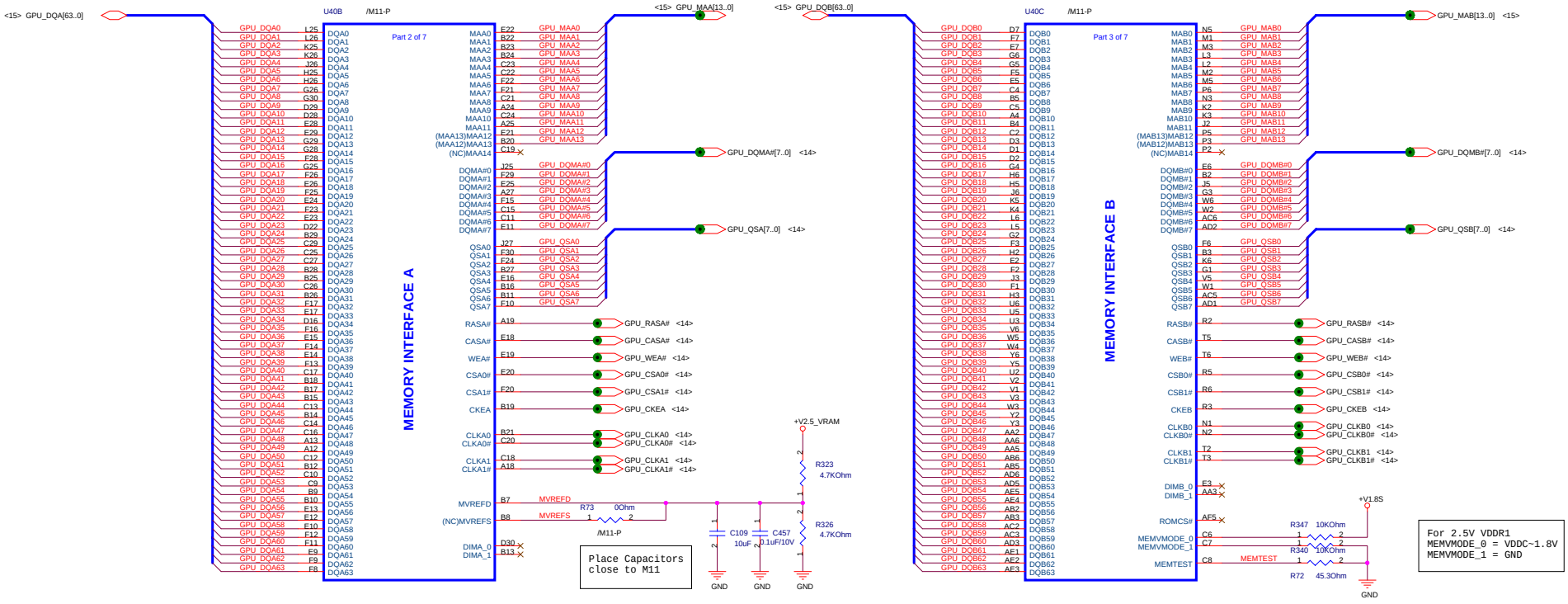




These chip capacitors should be placed equationally near the termination resistors

ASUSTEK CO.,LTD.	Title : DDR_TERMINATION	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 10 of 57	


AGP BUS signals is pulled-up by 855PM internal
Place C32 close to M11 pin
Place R314 close to VGA
M11-P: Pull-up to [1,1]
M9+X: not stuff [0,0]
PWR_PLY = H, VGACORE=1.0V
PWR_PLY = L, VGACORE=1.2V
M11-P Strap-pin
GPIO[1:0] = 11 (iPD) ; refclk 2 taps earlier than feedback clk (recommended)
GPIO[3:2] = 00 (iPD) ; 0 tap delay between x1clk and x2clk (recommended)
GPIO[6:4] = 000 (iPD) ; AGP8X_DETb = 1, AGP4X, 1.5V, AD16
GPIO[8] = 0 (iPD) ; ID Enable
GPIO[13:11,9] = 0000 (iPD) ; No ROM, CHG_ID=0 (default setting)
ZV_LCDDATA[17:16] = 00 (ASIC defalt) ; single function device
ZV_LCDDATA[20] = 1 (iPD) ; No slave VIP host port device
LCD PID2 PID1 PID0
14.1 XGA 1 1 1
15.0 XGA 1 0 1
15.0 SXGA+ 0 1 1
M11-P: need GPIO_VREF
M9+X: not stuff
Place C483 & C482 close to VGA
Place R313 close to VGA
SRS D_C Spread Deviation
0 NA -1.25% (DOWN)
1 NA -1.75% (DOWN)
Title : M11-Disp Sys
Engineer: Pommy Lu
ASUSTECH CO.,LTD.
Project Name A3G
Date: Thursday, August 19, 2004



ASUSTEK CO.,LTD.	Title : M11-Mem IF	
	Engineer: Pommy Lu	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 12 of 57	

place Decoupling Capacitors close to M11

Memory I/O Power

S0-S3: 530mA

+V2.5_VRAM

VDDR

CE14 22U/10V; C98 10uF; C113 10uF; C74 0.1uF/10V; C481 0.1uF/10V; C119 0.1uF/10V; C111 0.01UF/10V; C121 0.01UF/10V; C479 0.01UF/10V

R84 0Ohm /M11-P

LVDS I/O Power

S0-S3: 100mA

+V2.5S

L18 /M11-P 120Ohm/100Mhz

LVDS_LVDDR_25

C72 10uF; C82 0.1uF/10V

LVDS Digital Logic Power

S0-S3: 30mA

+V1.8S

L19 120Ohm/100Mhz

LVDS_LVDDR_18

C96 10uF; C62 0.1uF/10V

LVDS/TMDS PLL Power

S0-S3: 6mA

+V1.8S

L57 120Ohm/100Mhz

LVDS_LPVDD

C446 10uF; C447 0.1uF/10V

TMDS I/O Power

S0-S3: 30mA

+V1.8S

L58 120Ohm/100Mhz

TMDS_TXVDDR

C451 10uF; C452 0.1uF/10V

Memory Clock Power

S0-S3: 530mA

+V2.5_VRAM

L16 220Ohm/100Mhz

MEMCLK_VDDRH

C86 10uF; CE6 22U/10V; C33 10uF; C45 1UF/10V; C130 0.01UF/10V

S0-S3: 120mA

+V2.5S

L56 120Ohm/100Mhz

TV_A2VDD

C434 10uF; C435 0.1uF/10V

S0-S3: 66mA

+V1.8S

L11 120Ohm/100Mhz

TV_A2VDDQ

C52 10uF; C53 0.1uF/10V

L10 120Ohm/100Mhz

TV_A2VSSQ <11>

S0-S3: 66mA

+V1.8S

L54 120Ohm/100Mhz

CRT_AVDD

C432 10uF; C431 0.1uF/10V

L53 120Ohm/100Mhz

CRT_AVSSQ <11>

DAC Digital Power

S0-S3: 7mA

+V1.8S

L13 120Ohm/100Mhz

CRT_VDDDI

C63 10uF; C64 0.1uF/10V

L17 120Ohm/100Mhz

CRT_VSSDI

PLL Power

S0-S3: 21mA

+V1.8S

L8 120Ohm/100Mhz

PLL_PVDD

C54 10uF; C47 10uF; C46 0.1uF/10V

L9 120Ohm/100Mhz

PLL_PVSS

U40D /M11-P Part 4 of 7

I/O POWER

VDDR_1 VDDR_2(CLKBFB) VDDR_3 VDDR_4 VDDR_5 VDDR_6 VDDR_7 VDDR_8 VDDR_9 VDDR_10 VDDR_11 VDDR_12 VDDR_13 VDDR_14 VDDR_15 VDDR_16 VDDR_17 VDDR_18 VDDR_19 VDDR_20 VDDR_21 VDDR_22 VDDR_23 VDDR_24 VDDR_25 VDDR_26 VDDR_27 VDDR_28 VDDR_29 VDDR_30 VDDR_31 VDDR_32 VDDR_33 VDDR_34 VDDR_35 VDDR_36 VDDR_37 VDDR_38 VDDR_39 VDDR_40 VDDR_41 VDDR_42 VDDR_43 VDDR_44 VDDR_45 VDDR_46 VDDR_47 VDDR_48 VDDR_49 VDDR_50 VDDR_51 VDDR_52 VDDR_53 VDDR_54 VDDR_55 VDDR_56(CLKAFB) VDDR_57

R65 /M11-P 0Ohm

LVDS_LVDDR_25 LVDS_LVDDR_18 LVDS_LPVDD TMDS_TXVDDR MEMCLK_VDDRH TV_A2VDD TV_A2VDDQ CRT_AVDD CRT_VDDDI PLL_PVDD

LVDDR_25(LVDDR18_25)_1 LVDDR_25(LVDDR18_25)_2 LVDDR_18_1 LVDDR_18_2 LPVDD TPVDD TXVDDR_1 TXVDDR_2 VDDRH0 VDDRH1 A2VDD_1 A2VDD_2 A2VDDQ AVDD VDD1DI VDD2DI PVDD MPVDD

VDDC_63 VDDC_64 VDDC_65 VDDC_66 VDDC_67 (VDDC18)VDD15_1 (VDDC18)VDD15_2 (VDDC18)VDD15_3 (VDDC18)VDD15_4 (VDDC18)VDD15_5 (VDDC18)VDD15_6 (VDDC18)VDD15_7 (VDDC18)VDD15_8 VDDR3_1 VDDR3_2 VDDR3_3 VDDR3_4 VDDR3_5 VDDR3_6 VDDR3_7 VDDR3_8 VDDR4_1 VDDR4_2 VDDR4_3 VDDR4_4 VDDR4_5 VDDP_1 VDDP_2 VDDP_3 VDDP_4 VDDP_5 VDDP_6 VDDP_7 VDDP_8 VDDP_9 VDDP_10 VDDP_11 VDDP_12 VDDP_13 VDDP_14 VDDP_15 VDDP_16 VDDP_17 VDDP_18 VDDP_19 VDDP_20 VDDP_21 AVSSQ

LVSSR_1 LVSSR_2 LVSSR_3 LVSSR_4 LPVSS TPVSS TXVSSR_1 TXVSSR_2 TXVSSR_3 VSSRH0 VSSRH1 A2VSSN_1 A2VSSN_2 A2VSSQ AVSSN VSS1DI VSS2DI PVSS MPVSS

CRT_AVSSQ TV_A2VSSQ CRT_VSSDI PLL_PVSS MEMPLL_MPVSS

Memory PLL Power

+V1.8S

L59 120Ohm/100Mhz

L60 120Ohm/100Mhz

C129 10uF; C465 0.1uF/10V

S0-S3: 6mA

MEMPLL_MPVDD MEMPLL_MPVSS

C43 1UF/10V /EMI; C40 1UF/10V /EMI

+V3.3_VGA R386 /LEAK 0OHM; R389 /X_LEAK 0OHM +V3.3S +V3.3

S0-S3 MAX: 8.625A

+VGACORE

C94 C122 C55 C89 C97 C123 C67 CE10 C81 C100 C101 C124 C66 C85 C60

Power Between core and I/O

S0-S3: 160mA

R15 /M11-P 0OHM +V1.5S

R16 /M9+X 0OHM +V1.8S

I/O Power

S0-S3: 2mA

C117 C120 C104 CE2 22U/10V

C126 C56 C25 C80 C277 CE3 22U/10V

VDO Power

S0-S3: 2mA

R70 0Ohm +V3.3_VGA

AGP I/O Power

S0-S3: 90mA

+V1.5S

C36 C35 C37 C51 C30 C31 CE4 22U/10V

C22 C9 C14 C428 1UF/10V /EMI

U40F /M11-P Part 6 of 7

M10-P (708 BGA) M9+X (708 BGA) CENTER ARRAY

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 VDDC_23 VDDC_24 VDDC_25 VDDC_26 VDDC_27 VDDC_28 VDDC_29 VDDC_30 VDDC_31 VDDC_32 VDDC_33 VDDC_34 VDDC_35 VDDC_36

VSS_101 VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124

VDDCI_1 VDDCI_2 VDDCI_3 VDDCI_4

L12 60 Ohm/100MHz

C49 2.2UF/6.3V; C50 2.2UF/6.3V; C87 0.1uF/10V; C88 10uF; C99 0.01UF/10V

MASK OFF CENTER BALL ARRAY WITH M9+X (684BGA)

U40G /M11-P Part 7 of 7

M9+X (708 BGA) INNER ROWS

VDDC_37 VDDC_38 VDDC_39 VDDC_40 VDDC_41 VDDC_42 VDDC_43 VDDC_44 VDDC_45 VDDC_46 VDDC_47 VDDC_48 VDDC_49 VDDC_50 VDDC_51 VDDC_52 VDDC_53 VDDC_54 VDDC_55 VDDC_56 VDDC_57 VDDC_58 VDDC_59 VDDC_60 VDDC_61 VDDC_62

VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138

U40E /M11-P Part 5 of 7

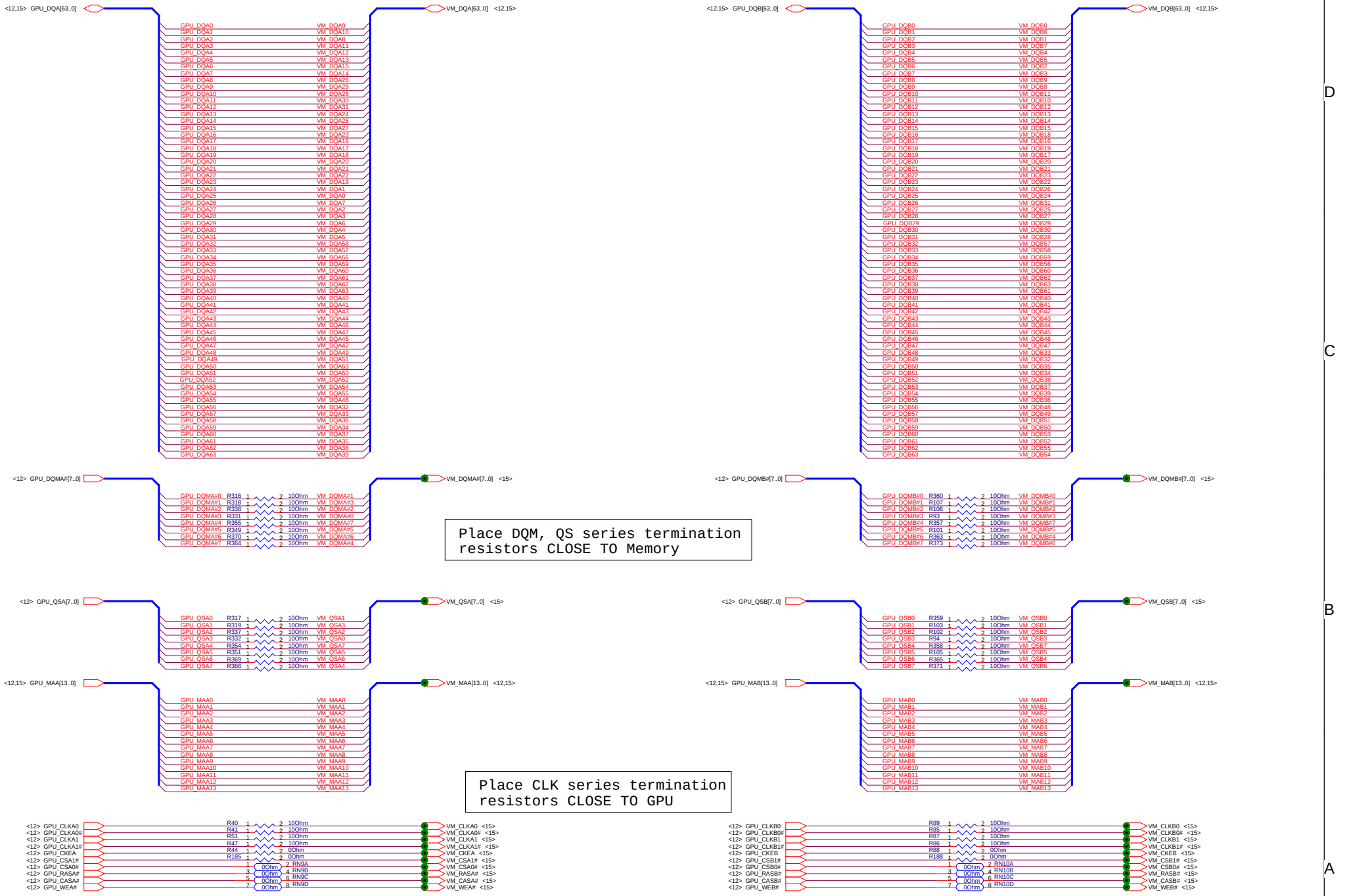
CORE GND

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50

VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100

GND

ASUSTeK COMPUTER INC.	Title : M11-PWR/GND		
	Engineer: Pommy Lu		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 13 of 57		



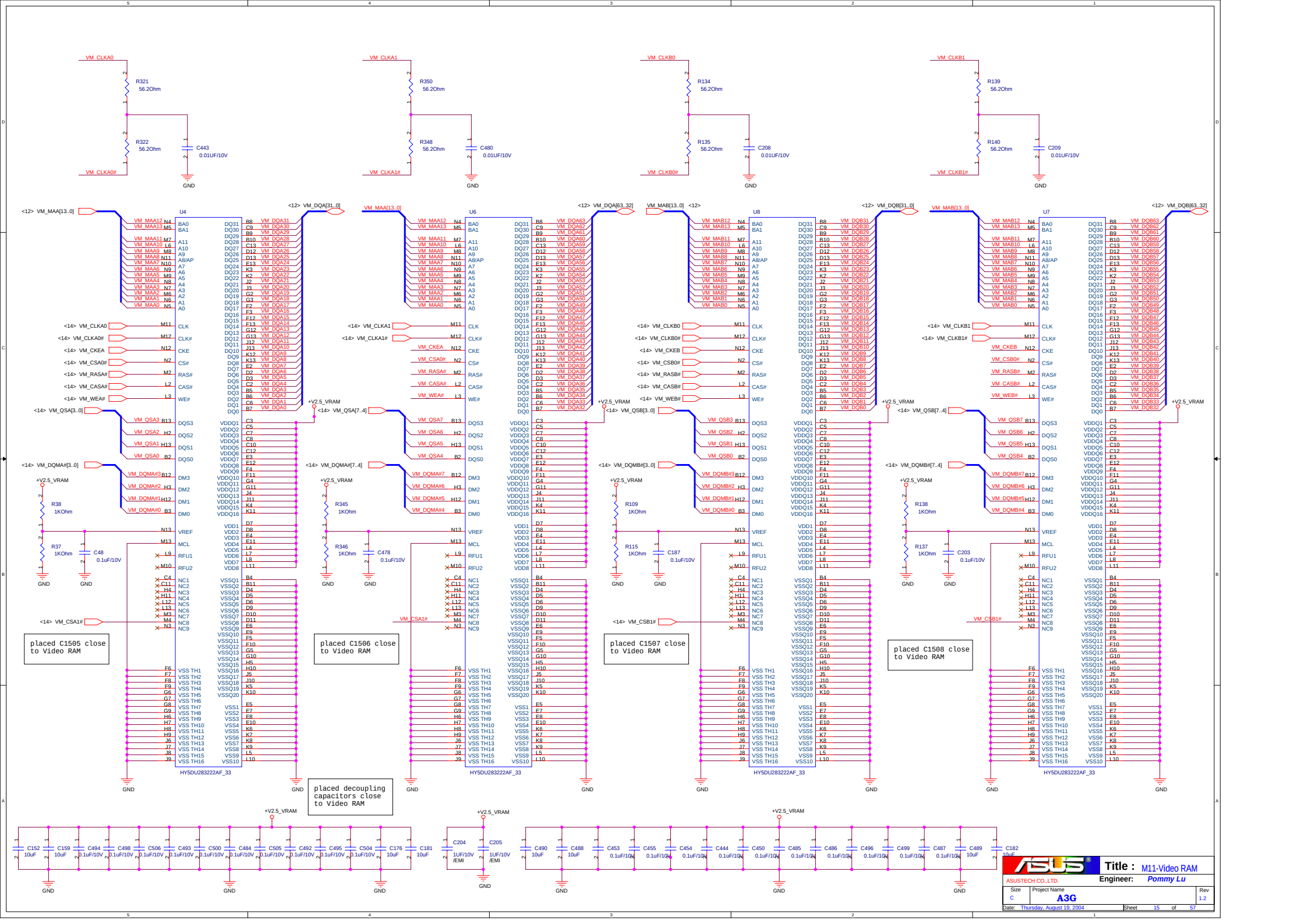
ASUSTECH CO.,LTD.

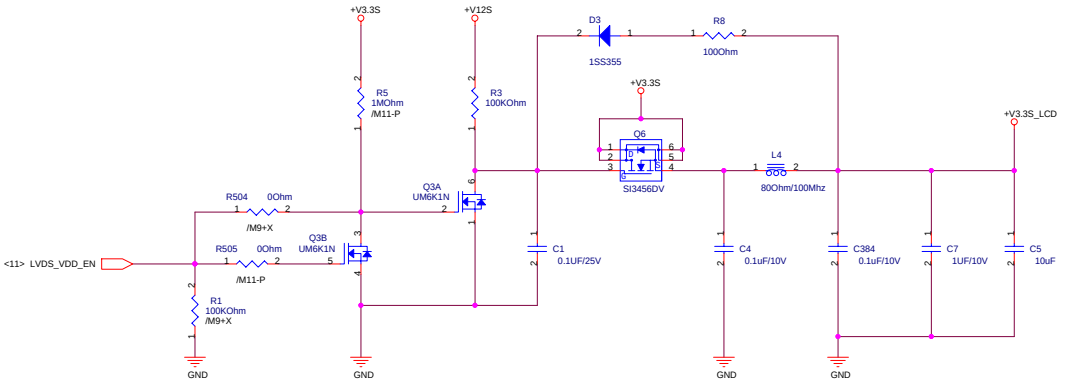
Title : VRAM DAMPING

Engineer: Pommy Lu

Size	Project Name	Rev
C	A3G	1.2

Date: Thursday, August 19, 2004 Sheet 14 of 57

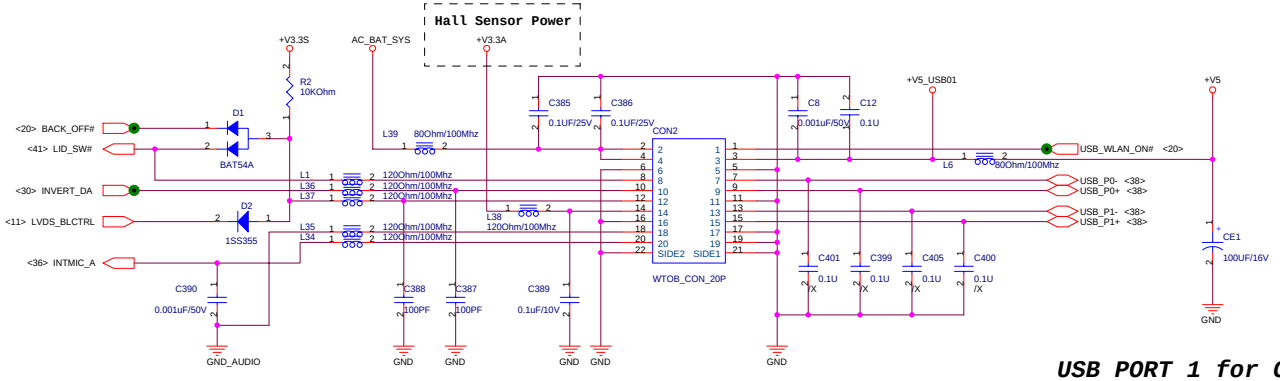

VM_CLKA0
R321 56.2Ohm
R322 56.2Ohm
C443 0.01UF/10V
VM_CLKA0#
GND
VM_CLKA1
R350 56.2Ohm
R348 56.2Ohm
C480 0.01UF/10V
VM_CLKA1#
VM_CLKB0
R134 56.2Ohm
R135 56.2Ohm
C208 0.01UF/10V
VM_CLKB0#
VM_CLKB1
R139 56.2Ohm
R140 56.2Ohm
C209 0.01UF/10V
VM_CLKB1#
U4
U6
U8
U7
HY5DU283222AF_33
+V2.5_VRAM
R38 1KOhm
R37 1KOhm
C48 0.1uF/10V
R345 1KOhm
R346 1KOhm
C478 0.1uF/10V
R109 1KOhm
R115 1KOhm
C187 0.1uF/10V
R138 1KOhm
R137 1KOhm
C203 0.1uF/10V
placed C1505 close to Video RAM
placed C1506 close to Video RAM
placed C1507 close to Video RAM
placed C1508 close to Video RAM
placed decoupling capacitors close to Video RAM
C152 10uF
C159 10uF
C494 0.1uF/10V
C498 0.1uF/10V
C506 0.1uF/10V
C493 0.1uF/10V
C500 0.1uF/10V
C484 0.1uF/10V
C505 0.1uF/10V
C492 0.1uF/10V
C495 0.1uF/10V
C504 0.1uF/10V
C176 10uF
C181 10uF
C204 1UF/10V /EMI
C205 1UF/10V /EMI
C490 10uF
C488 10uF
C453 0.1uF/10V
C455 0.1uF/10V
C454 0.1uF/10V
C444 0.1uF/10V
C450 0.1uF/10V
C485 0.1uF/10V
C486 0.1uF/10V
C496 0.1uF/10V
C499 0.1uF/10V
C487 0.1uF/10V
C489 10uF
C182 10uF
ASUSTeK COMPUTER INC.
Title : M11-Video RAM
Engineer: Pommy Lu
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 15 of 57



M11-P: Internal PD, not stuff R1
M9+X: stuff R1

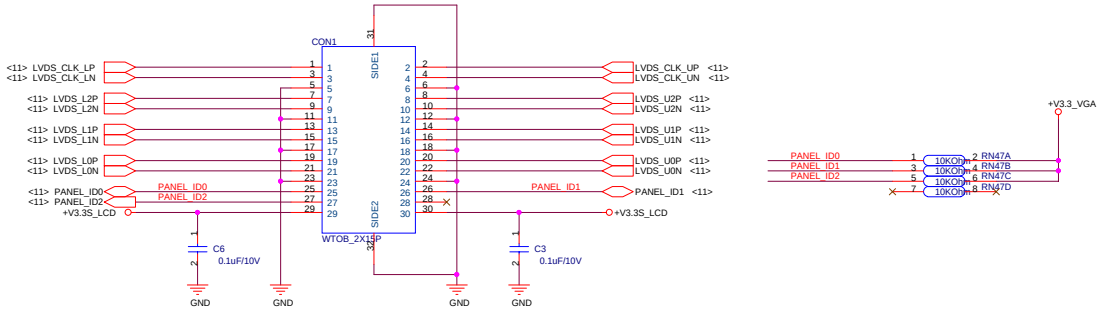
placed BEAD close to CON1

Backlgnt: Level Control



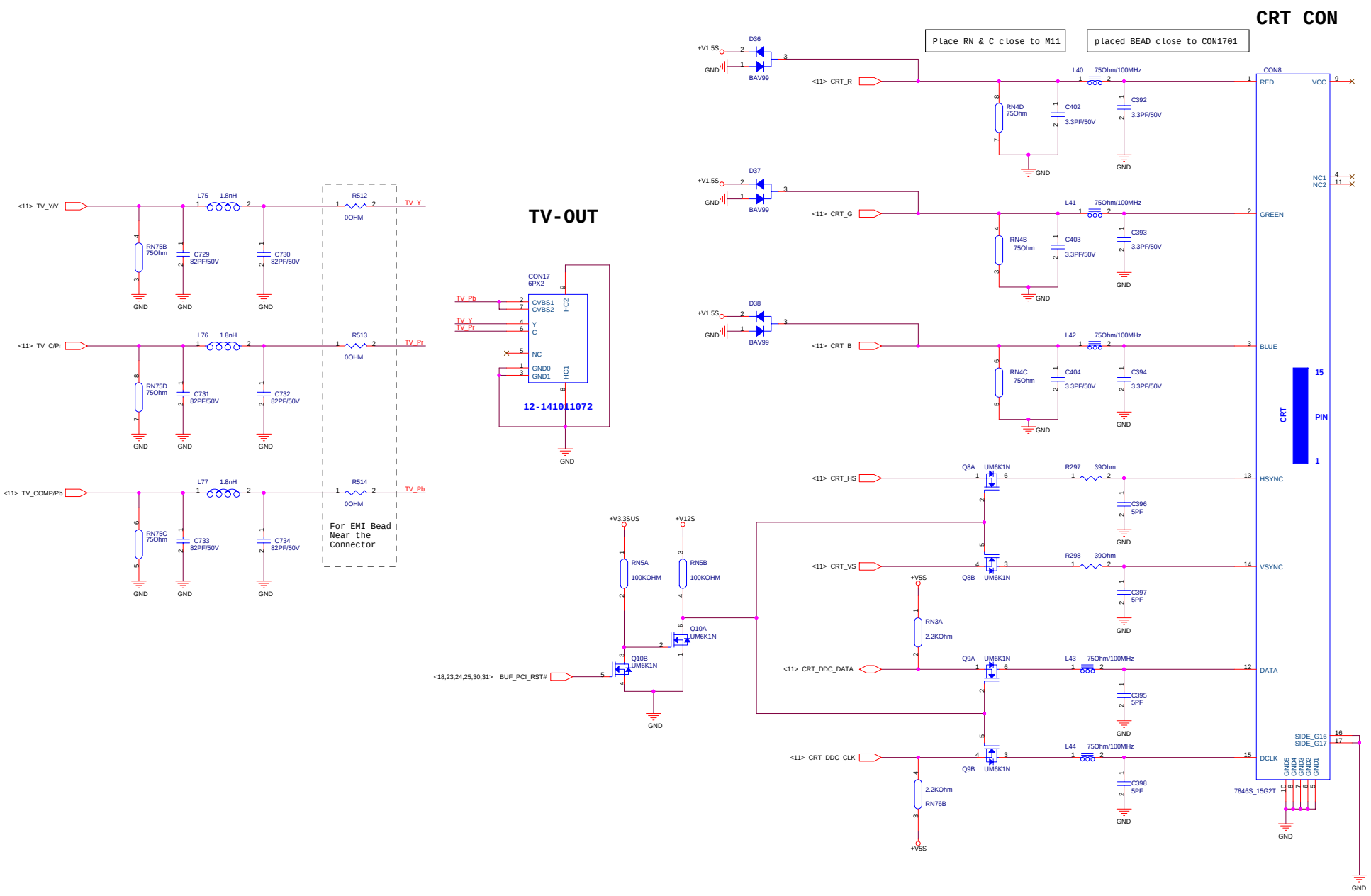
placed BEAD close to CON1603

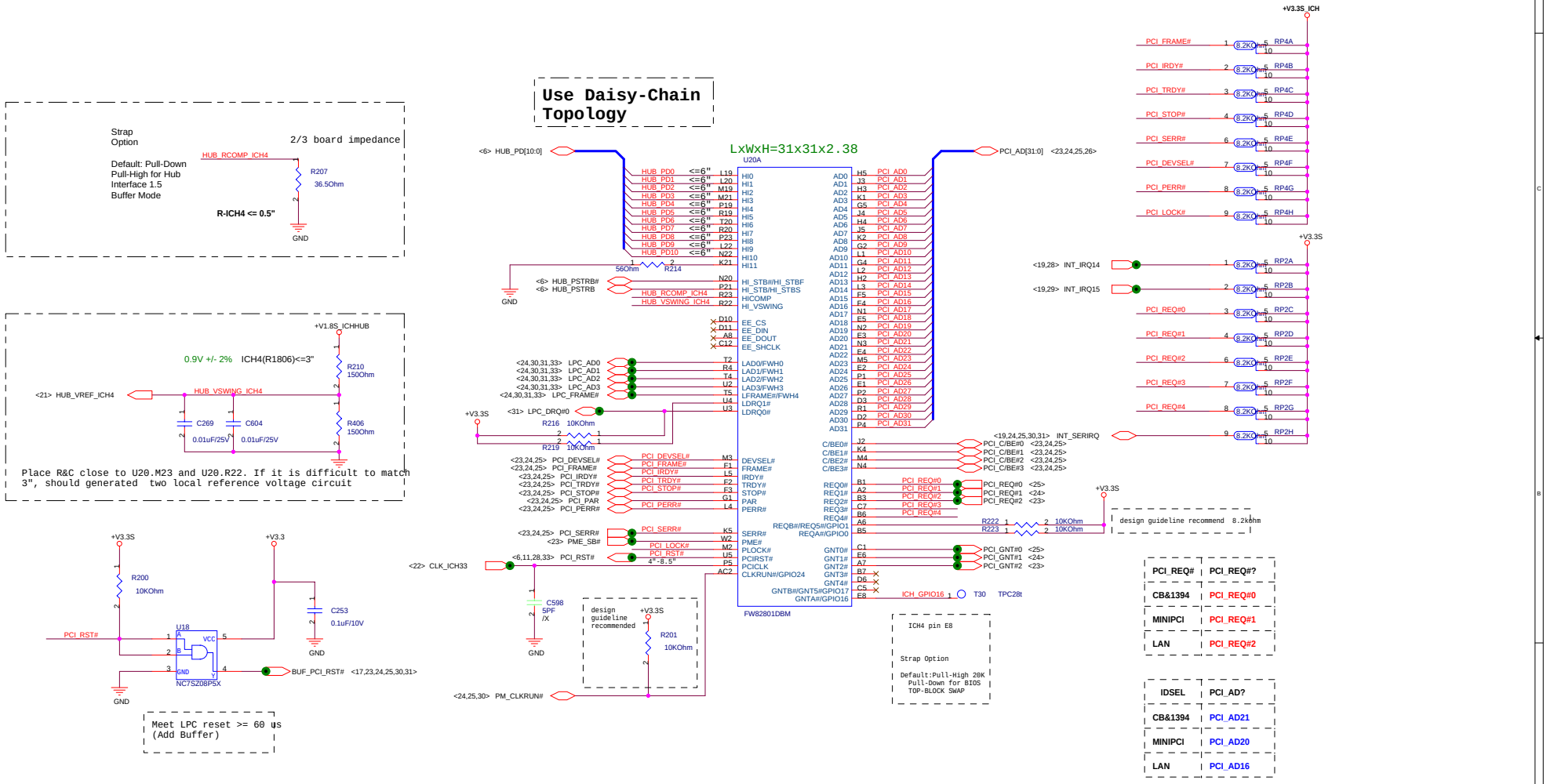
USB PORT 1 for CAMERA
USB PORT 0 for WLAN

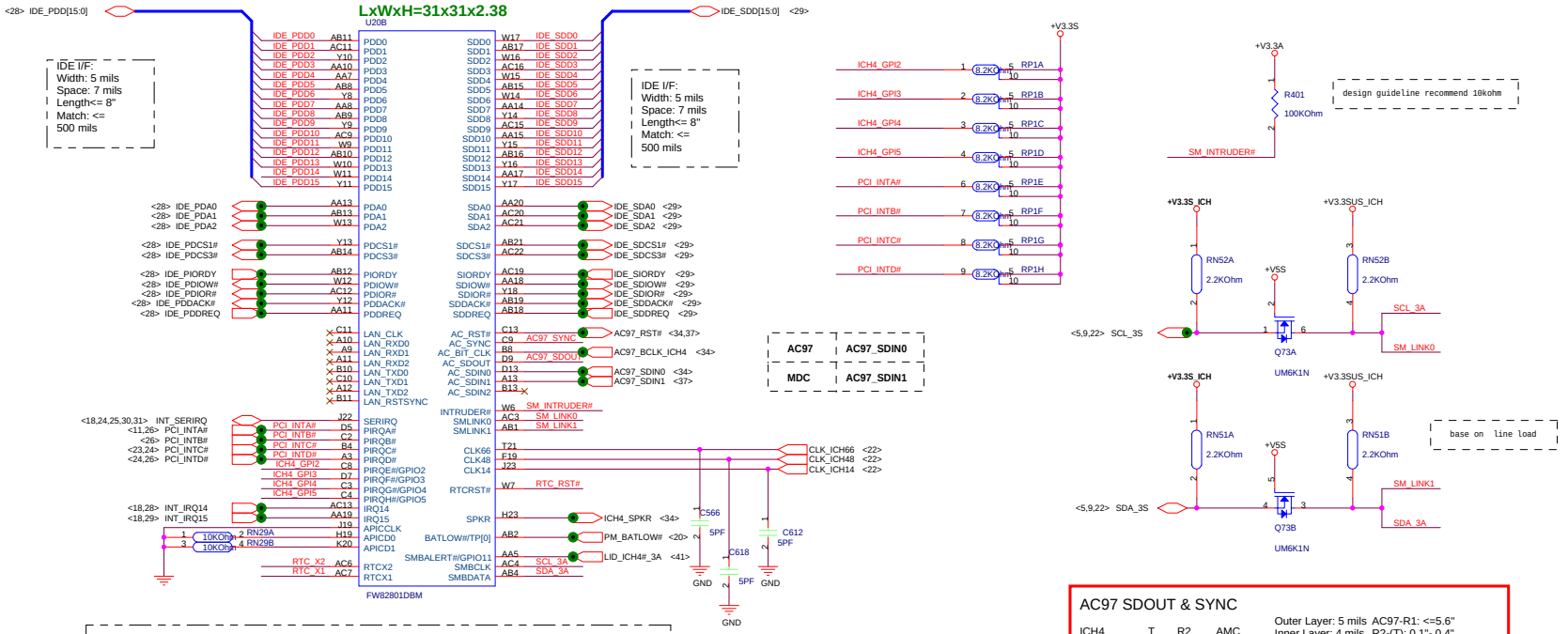


LCD CON

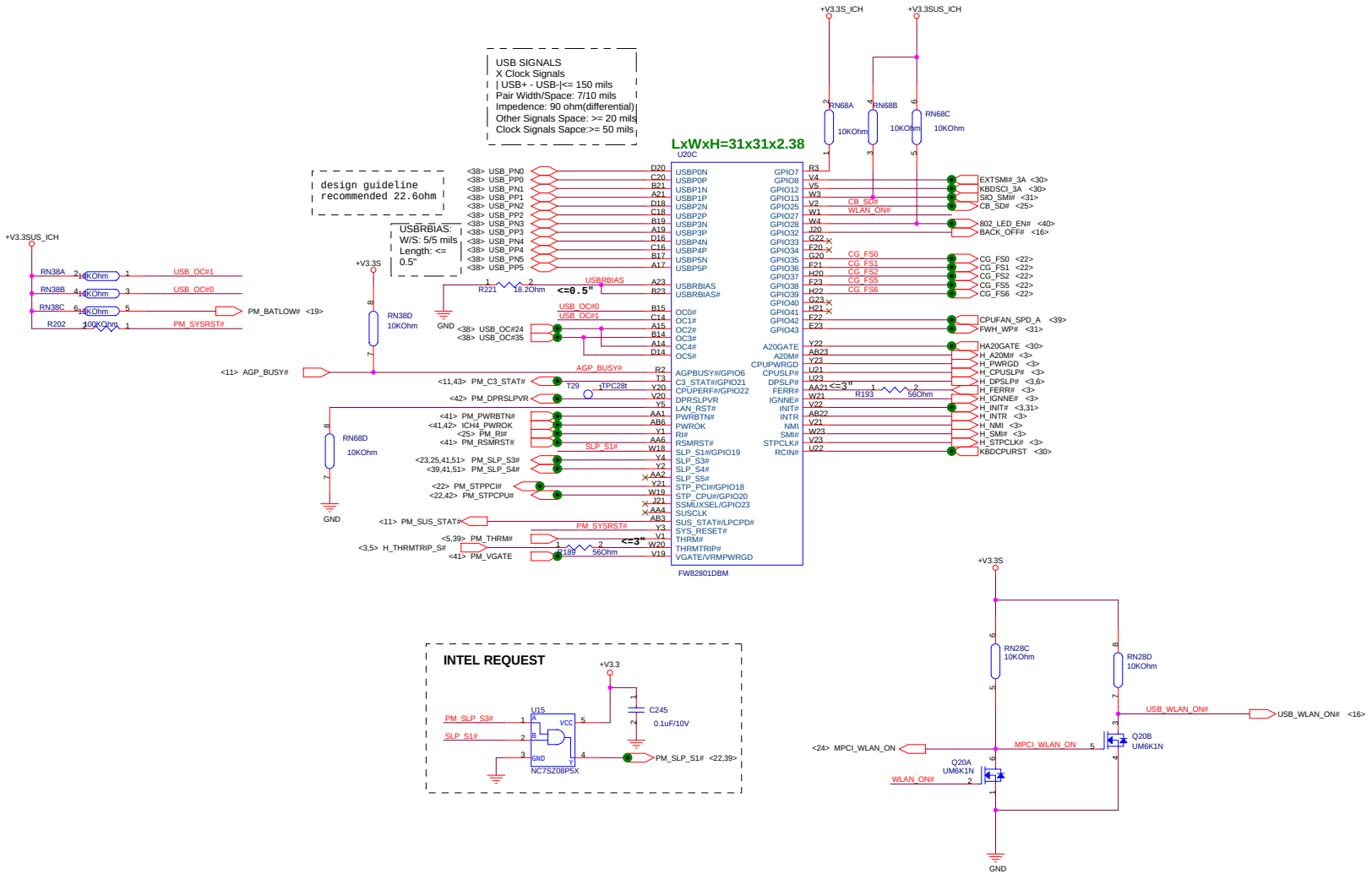
ASUSTECH CO.,LTD.	Title : BL&LCD CON	
	Engineer: Pommy Lu	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 16 of 57	

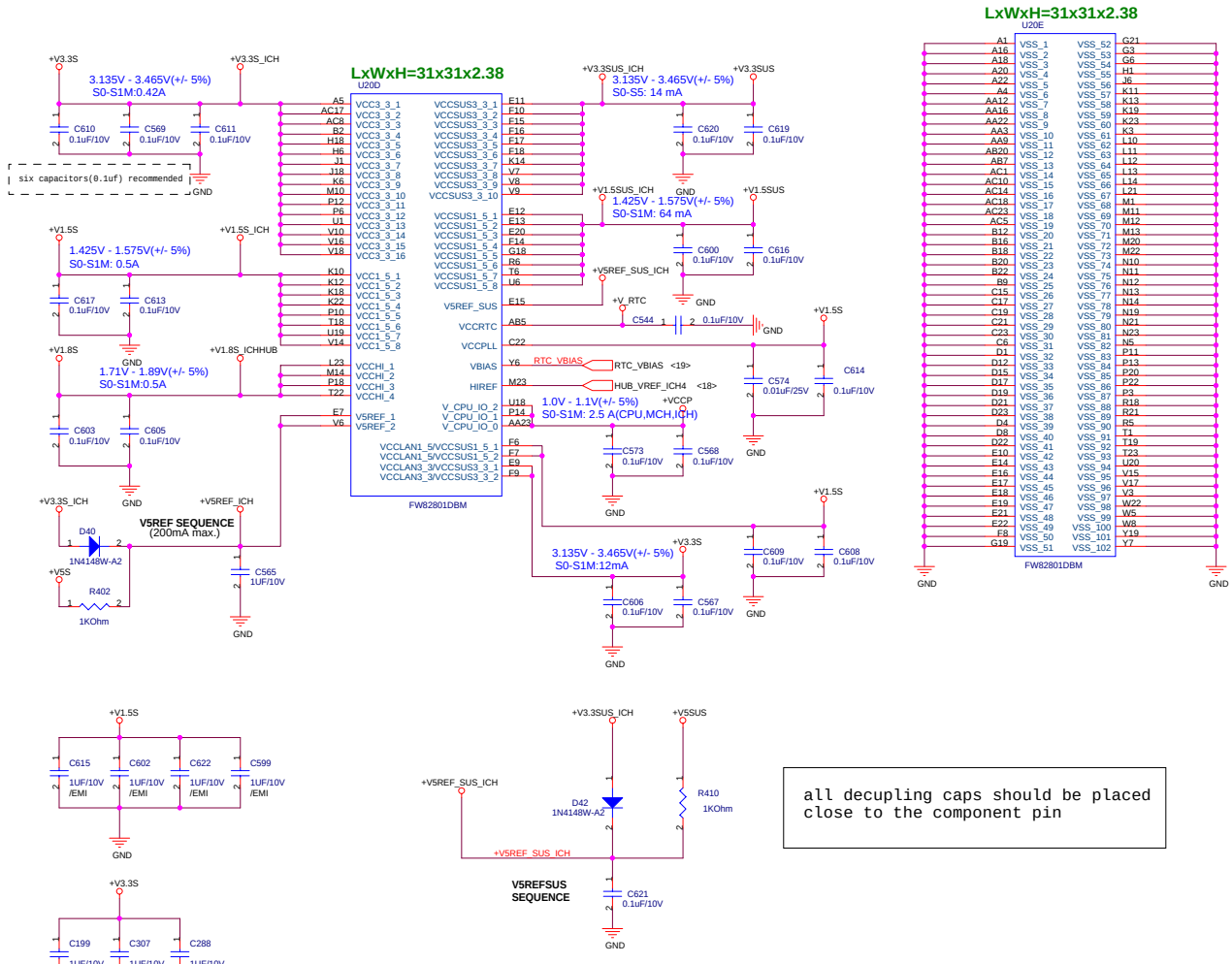

CRT CON
TV-OUT
Place RN & C close to M11
placed BEAD close to CON1701
For EMI Bead Near the Connector
12-141011072
CON8
CON17 6PX2
CRT
15 PIN 1
Title : TV-OUT & CRT CON
ASUSTEK CO.,LTD.
Engineer: Pommy Lu
Project Name A3G
Size C
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 17 of 57


Use Daisy-Chain Topology
LxWxH=31x31x2.38
U20A
FW82801DBM
Strap Option
2/3 board impedance
Default: Pull-Down
Pull-High for Hub Interface 1.5 Buffer Mode
R-ICH4 <= 0.5"
HUB_RCOMP_ICH4
R207
36.5Ohm
GND
+V1.8S_ICHHUB
0.9V +/- 2%
ICH4(R1806)<=3"
<21> HUB_VREF_ICH4
HUB_VSWING_ICH4
R210
150Ohm
R406
150Ohm
C269
0.01uF/25V
C604
0.01uF/25V
Place R&C close to U20.M23 and U20.R22. If it is difficult to match 3", should generated two local reference voltage circuit
<6> HUB_PD[10:0]
HUB_PD0 <=6" L19
HUB_PD1 <=6" L20
HUB_PD2 <=6" M19
HUB_PD3 <=6" M21
HUB_PD4 <=6" P19
HUB_PD5 <=6" R19
HUB_PD6 <=6" T20
HUB_PD7 <=6" R20
HUB_PD8 <=6" P23
HUB_PD9 <=6" L22
HUB_PD10 <=6" N22
R214
56Ohm
<6> HUB_PSTRB#
<6> HUB_PSTRB
HUB_RCOMP_ICH4
HUB_VSWING_ICH4
HI0 HI1 HI2 HI3 HI4 HI5 HI6 HI7 HI8 HI9 HI10 HI11
HI_STB#/HI_STBF
HI_STB/HI_STBS
HICOMP
HI_VSWING
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK
<24,30,31,33> LPC_AD0
<24,30,31,33> LPC_AD1
<24,30,31,33> LPC_AD2
<24,30,31,33> LPC_AD3
<24,30,31,33> LPC_FRAME#
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LFRAME#/FWH4
LDRQ1#
LDRQ0#
+V3.3S
<31> LPC_DRQ#0
R216 10KOhm
R219 10KOhm
<23,24,25> PCI_DEVSEL#
<23,24,25> PCI_FRAME#
<23,24,25> PCI_IRDY#
<23,24,25> PCI_TRDY#
<23,24,25> PCI_STOP#
<23,24,25> PCI_PAR
<23,24,25> PCI_PERR#
DEVSEL# FRAME# IRDY# TRDY# STOP# PAR PERR#
<23,24,25> PCI_SERR#
<23> PME_SB#
PCI_LOCK#
PCI_RST#
SERR# PME# PLOCK# PCIRST# PCICLK CLKRUN#/GPIO24
<6,11,28,33> PCI_RST#
4"-8.5"
<22> CLK_ICH33
C598
5PF
/X
design guideline recommended
R201
10KOhm
<24,25,30> PM_CLKRUN#
REQB#/REQ5#/GPIO1
REQA#/GPIO0
GNTB#/GNT5#/GPIO17
GNTA#/GPIO16
ICH_GPIO16
T30
TPC28t
ICH4 pin E8
Strap Option
Default:Pull-High 20K
Pull-Down for BIOS
TOP-BLOCK SWAP
PCI_AD[31:0] <23,24,25,26>
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
PCI_AD0 PCI_AD1 PCI_AD2 PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 PCI_AD20 PCI_AD21 PCI_AD22 PCI_AD23 PCI_AD24 PCI_AD25 PCI_AD26 PCI_AD27 PCI_AD28 PCI_AD29 PCI_AD30 PCI_AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C/BE#0 <23,24,25>
PCI_C/BE#1 <23,24,25>
PCI_C/BE#2 <23,24,25>
PCI_C/BE#3 <23,24,25>
REQ0# REQ1# REQ2# REQ3# REQ4#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_REQ#0 <25>
PCI_REQ#1 <24>
PCI_REQ#2 <23>
R222 10KOhm
R223 10KOhm
+V3.3S
design guideline recommend 8.2kohm
GNT0# GNT1# GNT2# GNT3# GNT4#
PCI_GNT#0 <25>
PCI_GNT#1 <24>
PCI_GNT#2 <23>
<19,24,25,30,31> INT_SERIRQ
+V3.3S_ICH
PCI_FRAME# PCI_IRDY# PCI_TRDY# PCI_STOP# PCI_SERR# PCI_DEVSEL# PCI_PERR# PCI_LOCK#
8.2KOhm
RP4A RP4B RP4C RP4D RP4E RP4F RP4G RP4H
+V3.3S
<19,28> INT_IRQ14
<19,29> INT_IRQ15
PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 PCI_REQ#3 PCI_REQ#4
RP2A RP2B RP2C RP2D RP2E RP2F RP2G RP2H
PCI_REQ# | PCI_REQ#?
CB&1394 | PCI_REQ#0
MINIPCI | PCI_REQ#1
LAN | PCI_REQ#2
IDSEL | PCI_AD?
CB&1394 | PCI_AD21
MINIPCI | PCI_AD20
LAN | PCI_AD16
+V3.3S
+V3.3
R200
10KOhm
C253
0.1uF/10V
PCI_RST#
U18
NC7SZ08P5X
BUF_PCI_RST# <17,23,24,25,30,31>
Meet LPC reset >= 60 us
(Add Buffer)
ASUSTeK COMPUTER INC.
Title : ICH4-M(HUB_PCI)
Engineer: charlie_xie
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 18 of 57

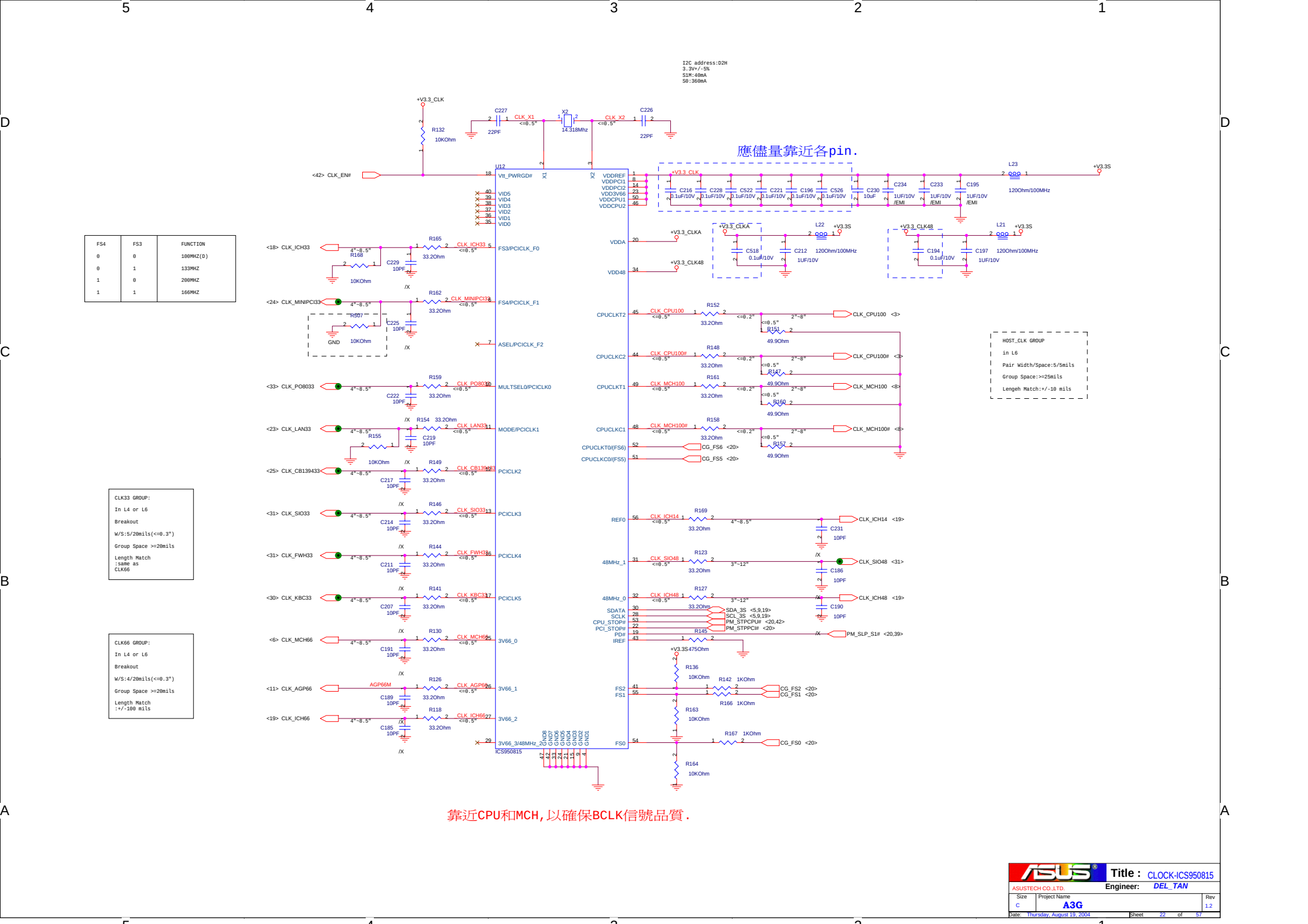


ASUSTEK COMP.	Title : ICH4-M(IDE_AC97)		
ASUSTEK CO.,LTD.	Engineer: charlie_xie		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 19 of 57		


USB SIGNALS
X Clock Signals
| USB+ - USB-|<= 150 mils
Pair Width/Space: 7/10 mils
Impedence: 90 ohm(differential)
Other Signals Space: >= 20 mils
Clock Signals Sapce:>= 50 mils
LxWxH=31x31x2.38
U20C
FW82801DBM
design guideline
recommended 22.6ohm
USBRBIAS:
W/S: 5/5 mils
Length: <= 0.5"
INTEL REQUEST
U15
NC7SZ08P5X
+V3.3S_ICH
+V3.3SUS_ICH
+V3.3S
+V3.3
GND
RN38A
RN38B
RN38C
RN38D
RN68A
RN68B
RN68C
RN68D
RN28C
RN28D
R202
R221
R193
R189
C245
0.1uF/10V
Q20A
Q20B
UM6K1N
USB_OC#1
USB_OC#0
PM_BATLOW# <19>
PM_SYSRST#
AGP_BUSY#
PM_C3_STAT#
PM_DPRSLPVR
PM_PWRBTN#
ICH4_PWROK
PM_RI#
PM_RSMRST#
PM_SLP_S3#
PM_SLP_S4#
PM_STPPCI#
PM_STPCPU#
PM_SUS_STAT#
PM_THRM#
H_THRMTRIP_S#
PM_VGATE
SLP_S1#
PM_SLP_S1# <22,39>
CB_SD#
WLAN_ON#
CG_FS0
CG_FS1
CG_FS2
CG_FS5
CG_FS6
MPCI_WLAN_ON
USB_WLAN_ON#
USB_WLAN_ON# <16>
<24> MPCI_WLAN_ON
EXTSMI#_3A <30>
KBDSCI_3A <30>
SIO_SMI# <31>
CB_SD# <25>
802_LED_EN# <40>
BACK_OFF# <16>
CPUFAN_SPD_A <39>
FWH_WP# <31>
HA20GATE <30>
H_A20M# <3>
H_PWRGD <3>
H_CPUSLP# <3>
H_DPSLP# <3,6>
H_FERR# <3>
H_IGNNE# <3>
H_INIT# <3,31>
H_INTR <3>
H_NMI <3>
H_SMI# <3>
H_STPCLK# <3>
KBDCPURST <30>
Title : ICH4-M(USB_PM)
ASUSTECH CO.,LTD.
Engineer: charlie_xie
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 20 of 57



Title :	ICH4-M(POWER)
ASUSTECH CO.,LTD.	Engineer: charlie_xie
Size: C	Project Name: A3G
Rev: 1.2	
Date: Thursday, August 19, 2004	Sheet 21 of 57


I2C address:D2H
3.3V+/-5%
S1M:40mA
S0:360mA
應儘量靠近各pin.
靠近CPU和MCH,以確保BCLK信號品質.
FS4 FS3 FUNCTION
0 0 100MHZ(D)
0 1 133MHZ
1 0 200MHZ
1 1 166MHZ
CLK33 GROUP:
In L4 or L6
Breakout
W/S:5/20mils(<=0.3")
Group Space >=20mils
Length Match :same as CLK66
CLK66 GROUP:
In L4 or L6
Breakout
W/S:4/20mils(<=0.3")
Group Space >=20mils
Length Match :+/-100 mils
HOST_CLK GROUP
in L6
Pair Width/Space:5/5mils
Group Space:>=25mils
Lengeh Match:+/-10 mils
U12
ICS950815
Title : CLOCK-ICS950815
ASUSTECH CO.,LTD.
Engineer: DEL_TAN
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
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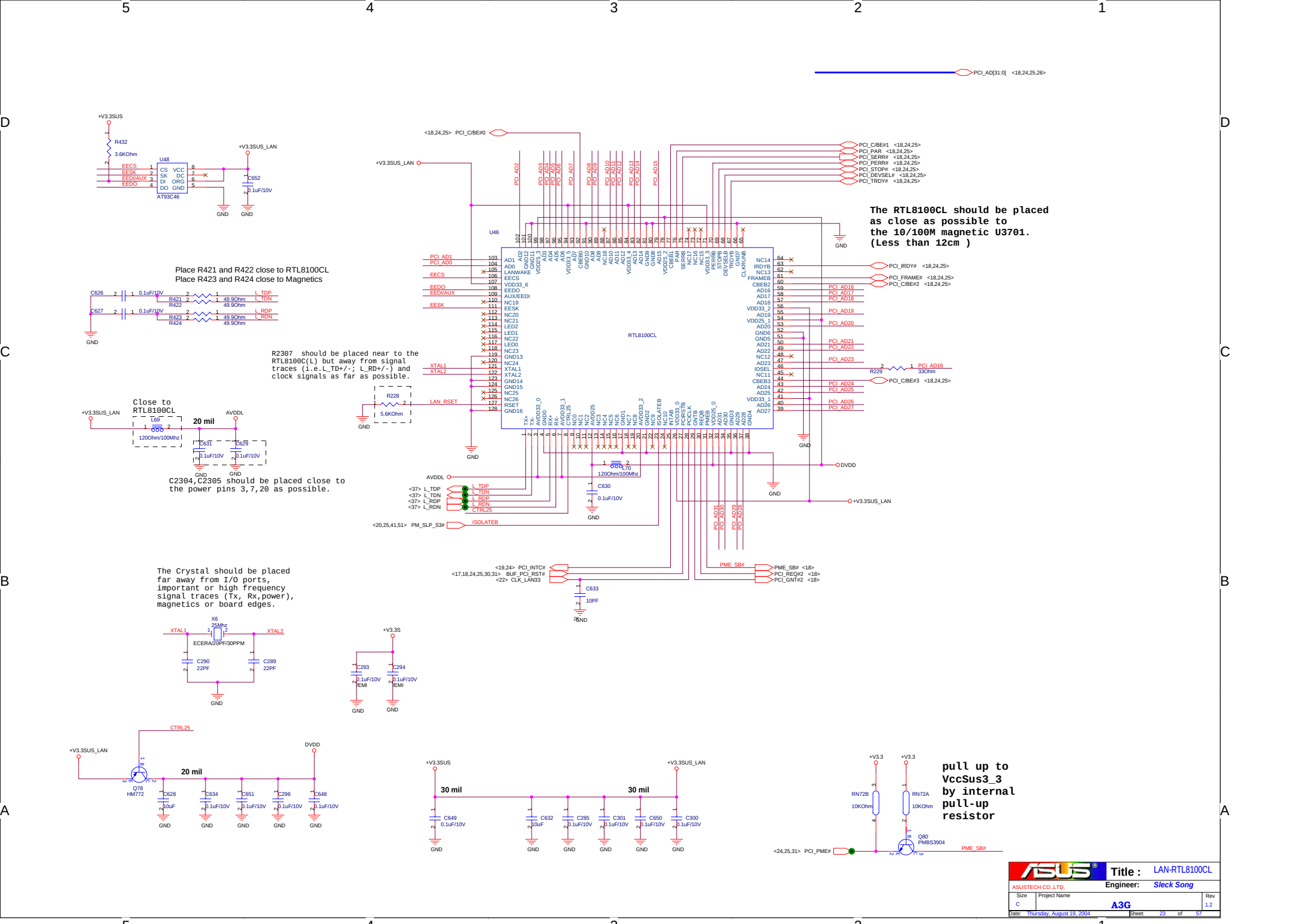
PCI_AD[31:0] <18,24,25,26>
+V3.3SUS
R432
3.6KOhm
U48
EECS
EESK
EEDI/AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46
+V3.3SUS_LAN
C652
0.1uF/10V
GND
<18,24,25> PCI_C/BE#0
+V3.3SUS_LAN
PCI_C/BE#1 <18,24,25>
PCI_PAR <18,24,25>
PCI_SERR# <18,24,25>
PCI_PERR# <18,24,25>
PCI_STOP# <18,24,25>
PCI_DEVSEL# <18,24,25>
PCI_TRDY# <18,24,25>
The RTL8100CL should be placed as close as possible to the 10/100M magnetic U3701. (Less than 12cm)
U46
RTL8100CL
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
LAN_RSET
PCI_IRDY# <18,24,25>
PCI_FRAME# <18,24,25>
PCI_C/BE#2 <18,24,25>
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
PCI_C/BE#3 <18,24,25>
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
R229
33Ohm
Place R421 and R422 close to RTL8100CL
Place R423 and R424 close to Magnetics
C626
C627
0.1uF/10V
R421
R422
R423
R424
49.9Ohm
L_TDP
L_TDN
L_RDP
L_RDN
GND
R2307 should be placed near to the RTL8100C(L) but away from signal traces (i.e.L_TD+/-; L_RD+/-) and clock signals as far as possible.
R228
5.6KOhm
Close to RTL8100CL
+V3.3SUS_LAN
L69
120Ohm/100Mhz
20 mil
AVDDL
C631
C629
0.1uF/10V
C2304,C2305 should be placed close to the power pins 3,7,20 as possible.
DVDD
L70
120Ohm/100Mhz
C630
0.1uF/10V
<37> L_TDP
<37> L_TDN
<37> L_RDP
<37> L_RDN
CTRL25
ISOLATEB
<20,25,41,51> PM_SLP_S3#
<19,24> PCI_INTC#
<17,18,24,25,30,31> BUF_PCI_RST#
<22> CLK_LAN33
C633
10PF
PME_SB# <18>
PCI_REQ#2 <18>
PCI_GNT#2 <18>
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
X6
25Mhz
ECERA/20PF/30PPM
C290
22PF
C289
22PF
+V3.3S
C293
C294
0.1uF/10V
/EMI
CTRL25
+V3.3SUS_LAN
20 mil
Q78
HM772
C628
10uF
C634
C651
C296
C648
0.1uF/10V
DVDD
+V3.3SUS
30 mil
C649
C632
C285
C301
C650
C300
+V3.3
RN72B
RN72A
10KOhm
Q80
PMBS3904
<24,25,31> PCI_PME#
pull up to VccSus3_3 by internal pull-up resistor
Title : LAN-RTL8100CL
ASUSTECH CO.,LTD.
Engineer: Sleck Song
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
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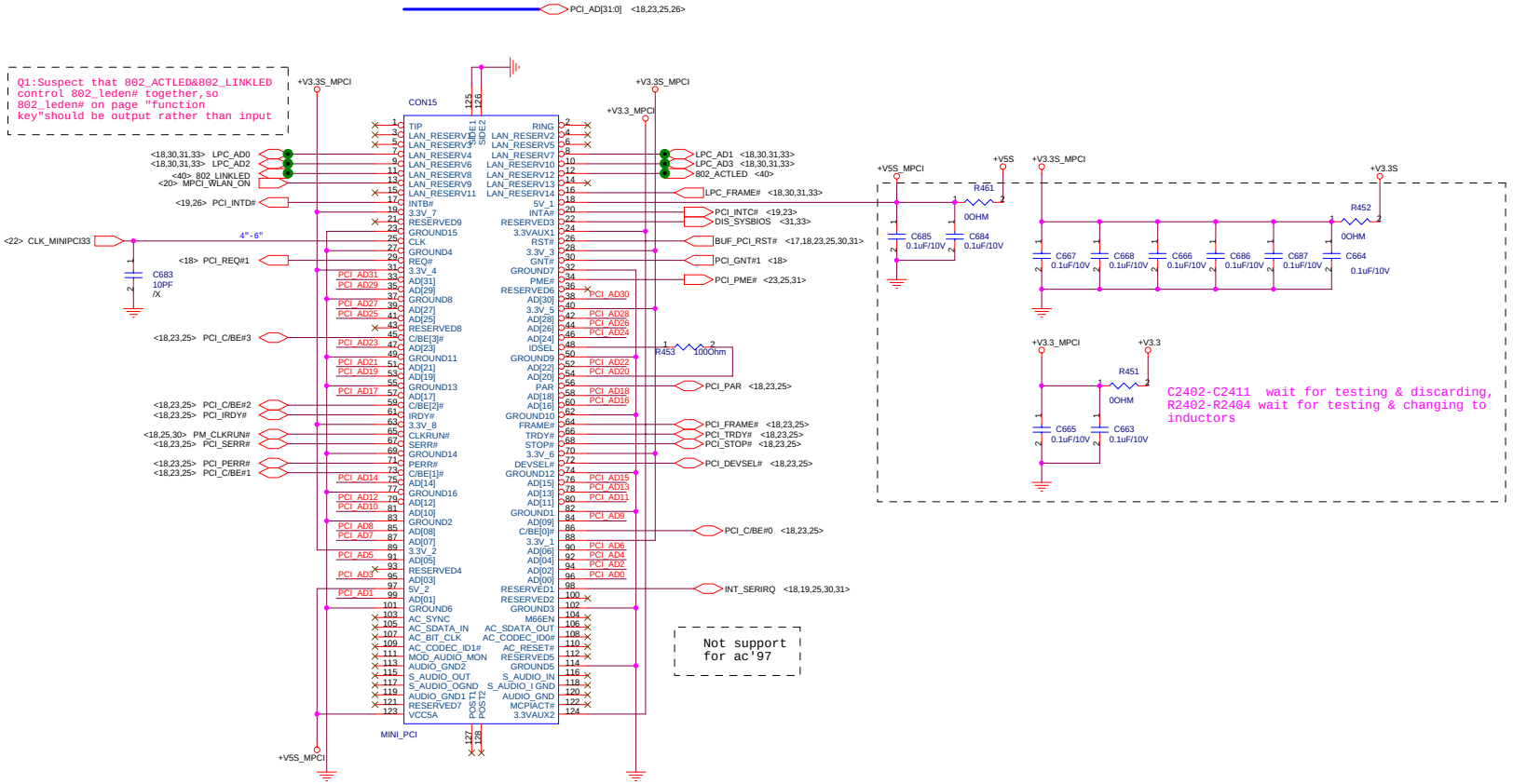
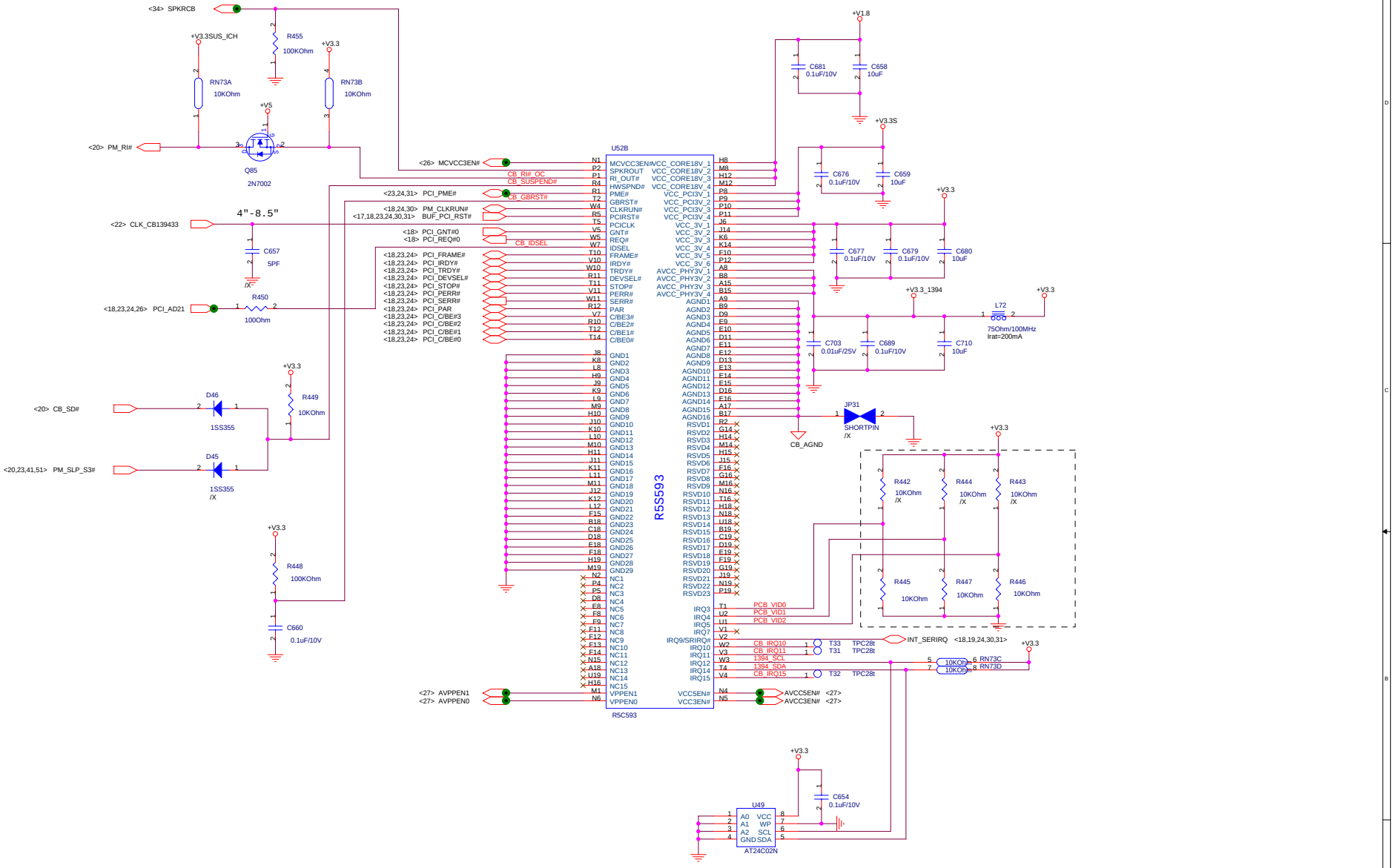


ASUSTECH CO.,LTD.	Title : MINIPCI	
	Engineer: Jully Ma	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 24 of 57	

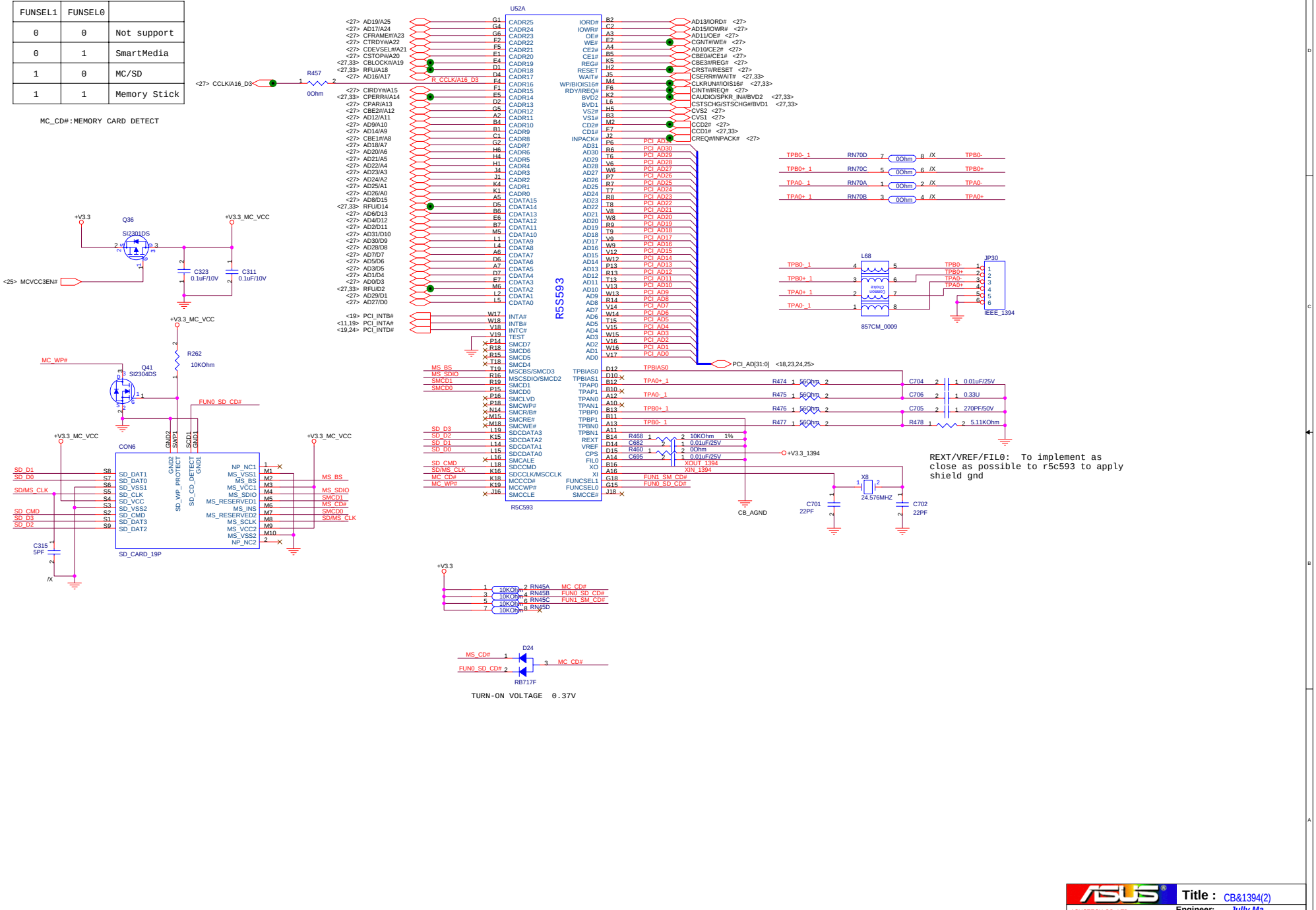


ASUSTEK CO.,LTD.	Title : CB&1394(1)	
	Engineer: Jully Ma	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 25 of 57	

Memory Card Detect

FUNSEL1	FUNSEL0	
0	0	Not support
0	1	SmartMedia
1	0	MC/SD
1	1	Memory Stick

MC_CD#:MEMORY CARD DETECT

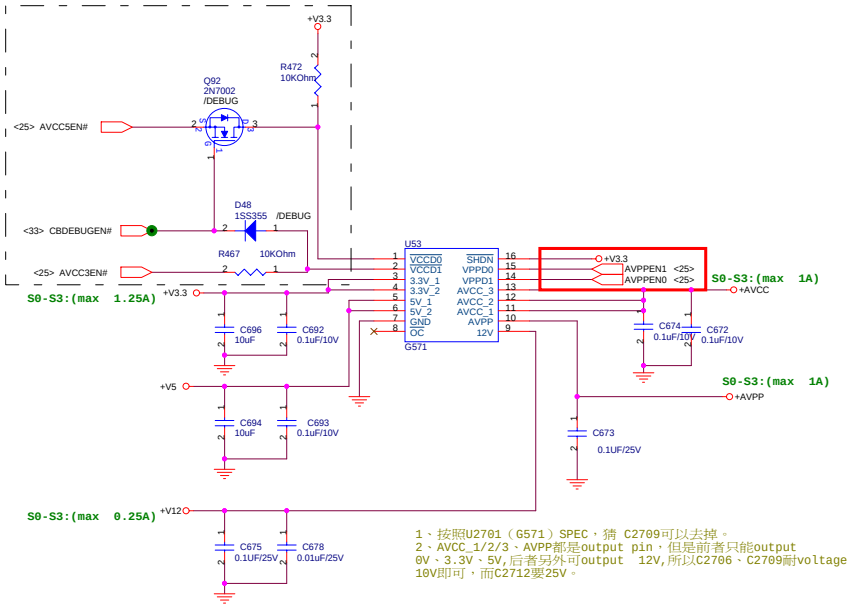


TURN-ON VOLTAGE 0.37V

REXT/VREF/FIL0: To implement as close as possible to r5c593 to apply shield gnd

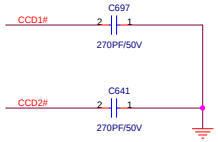
ASUSTEK CO.,LTD.	Title : CB&1394(2)		
	Engineer: Jully Ma		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 26 of 57		

CB POWER SWITCH

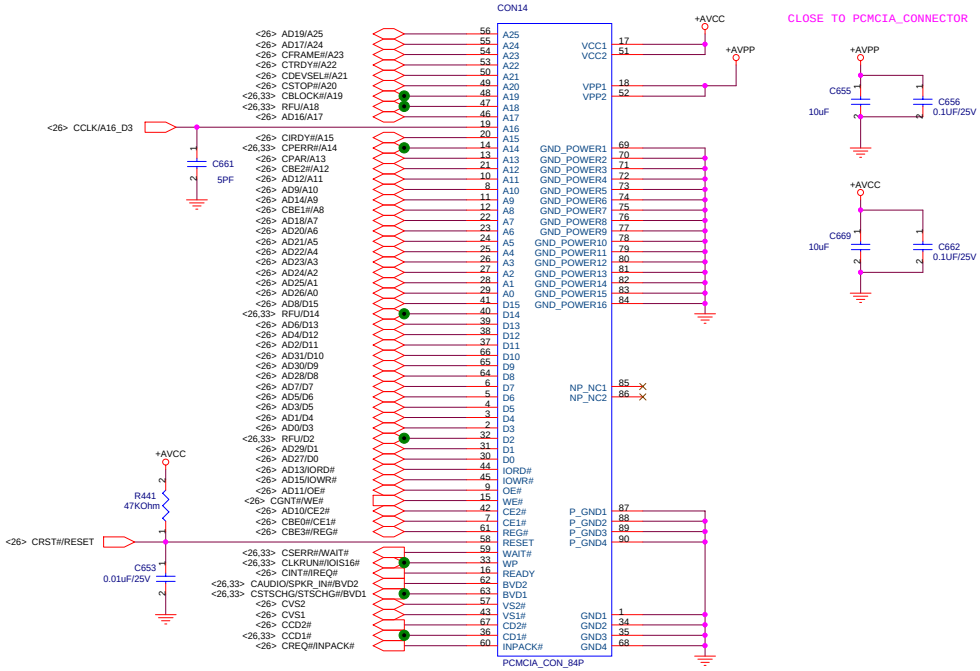


1、按照U2701（G571）SPEC，猜 C2709可以去掉。
2、AVCC_1/2/3、AVPP都是output pin，但是前者只能output 0V、3.3V、5V,后者另外可output 12V,所以C2706、C2709耐voltage 10V即可，而C2712要25V。

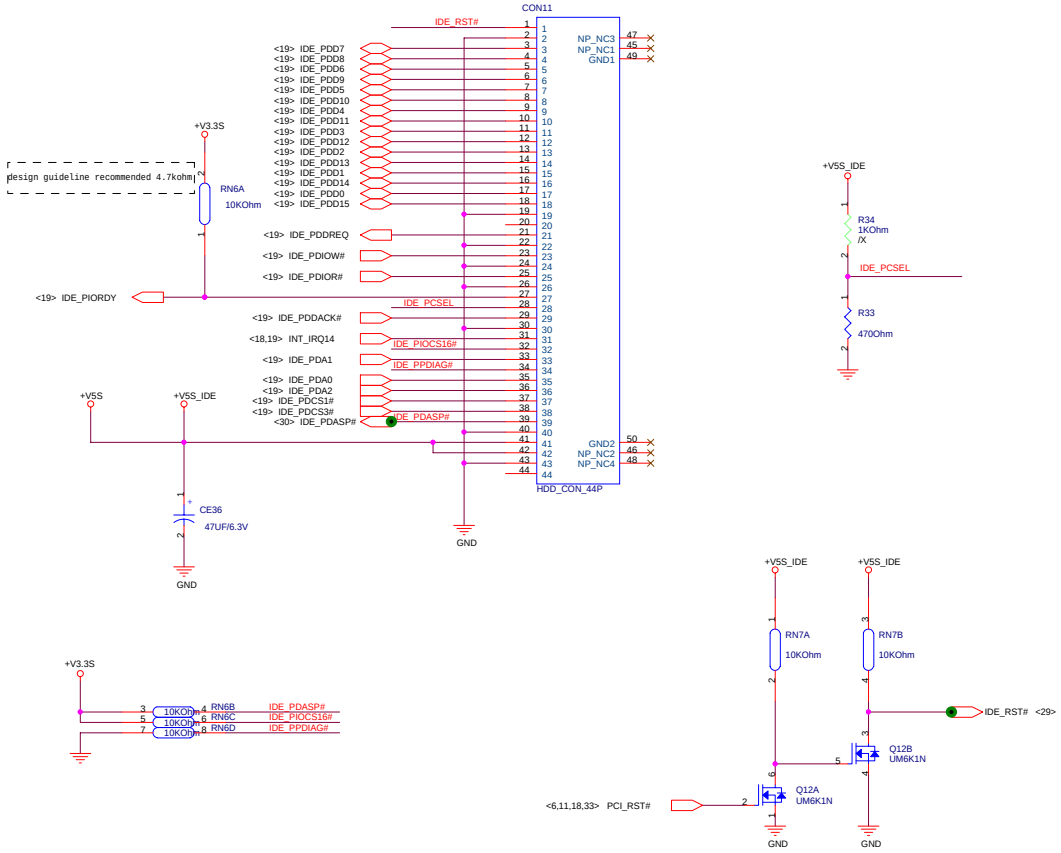
CB DE-BOUNCE



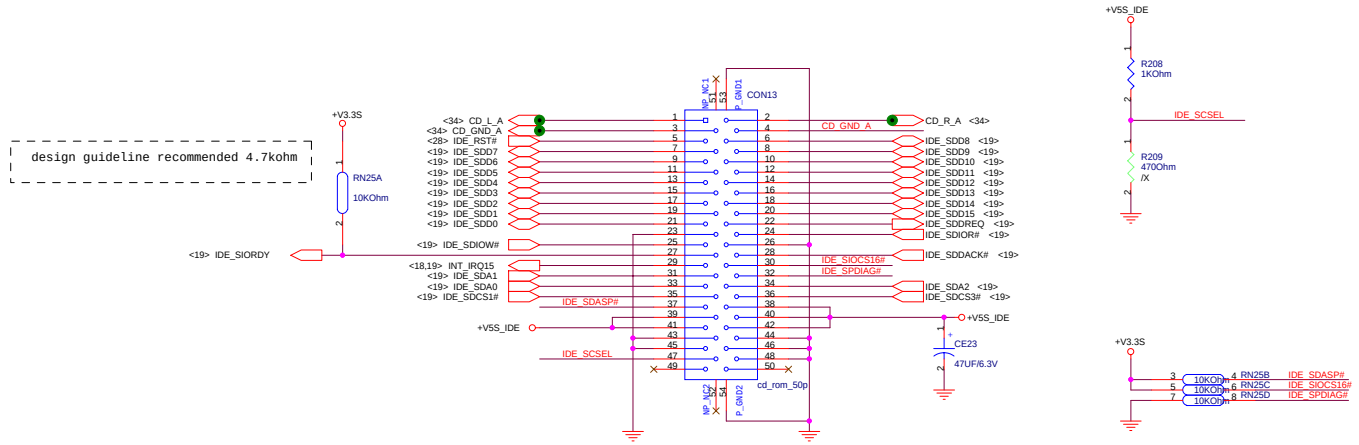
CB SOCKET



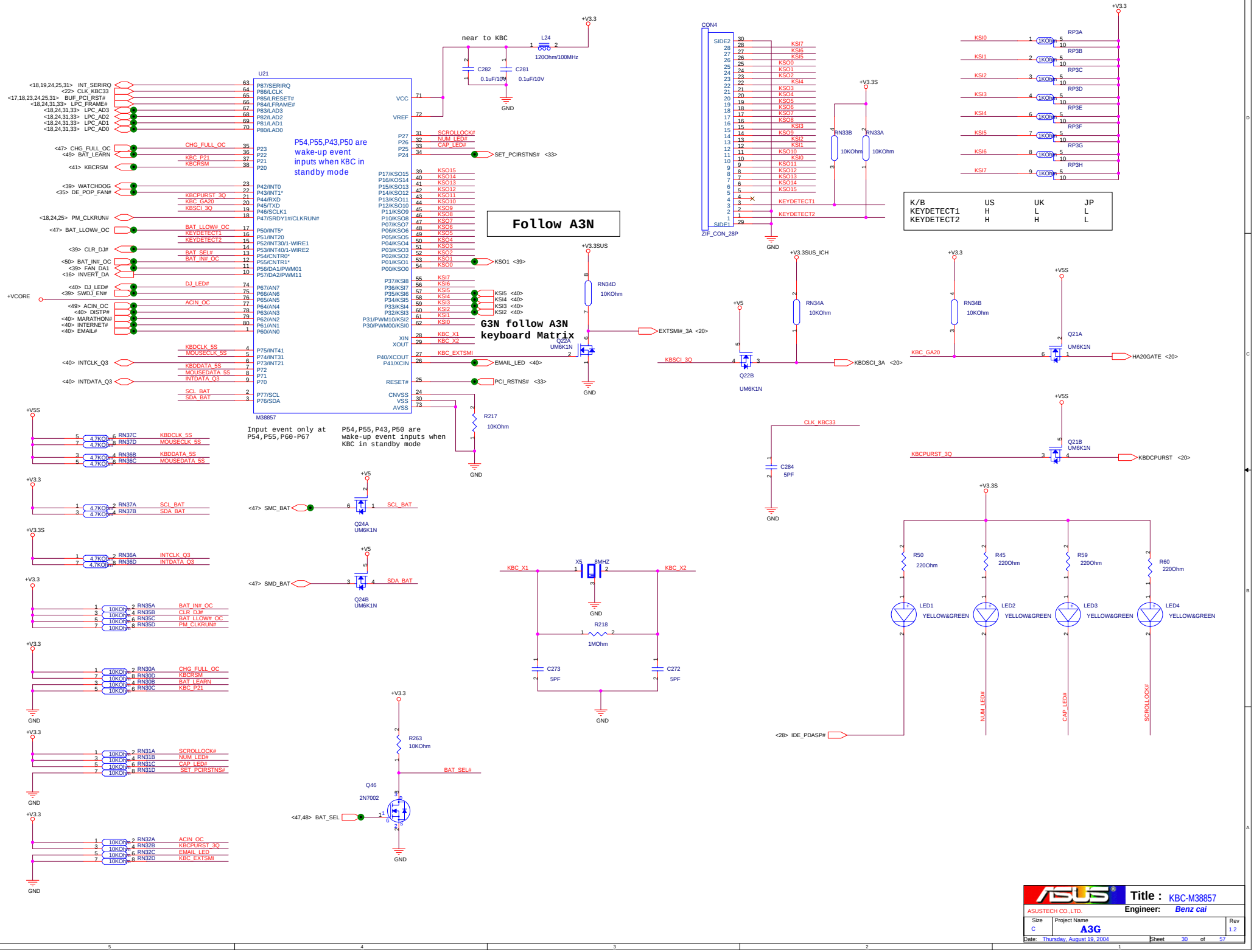
ASUSTEK CO.,LTD.	Title : PCMCIA SOCKET	
	Engineer: Jully_ma	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 27 of 57	



ASUSTECH CO.,LTD.	Title : IDE(HDD)	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 28 of 57	



ASUSTECH CO.,LTD.	Title : IDE(ODD)	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 29 of 57	


U21
M38857
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
Follow A3N
G3N follow A3N keyboard Matrix
Input event only at P54,P55,P60-P67
P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode
near to KBC
L24
120Ohm/100MHz
C282
0.1uF/10V
C281
0.1uF/10V
CON4
ZIF_CON_28P
K/B US UK JP
KEYDETECT1 H L L
KEYDETECT2 H H L
RP3A
RP3B
RP3C
RP3D
RP3E
RP3F
RP3G
RP3H
RN33B
RN33A
RN34D
RN34A
RN34B
Q22A
Q22B
Q21A
Q21B
Q24A
Q24B
UM6K1N
Q46
2N7002
X5
8MHZ
R218
1MOhm
R263
10KOhm
R217
10KOhm
C284
5PF
C273
5PF
C272
5PF
R50
R45
R59
R60
220Ohm
LED1
LED2
LED3
LED4
YELLOW&GREEN
ASUSTECH CO.,LTD.
Title : KBC-M38857
Engineer: Benz cai
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
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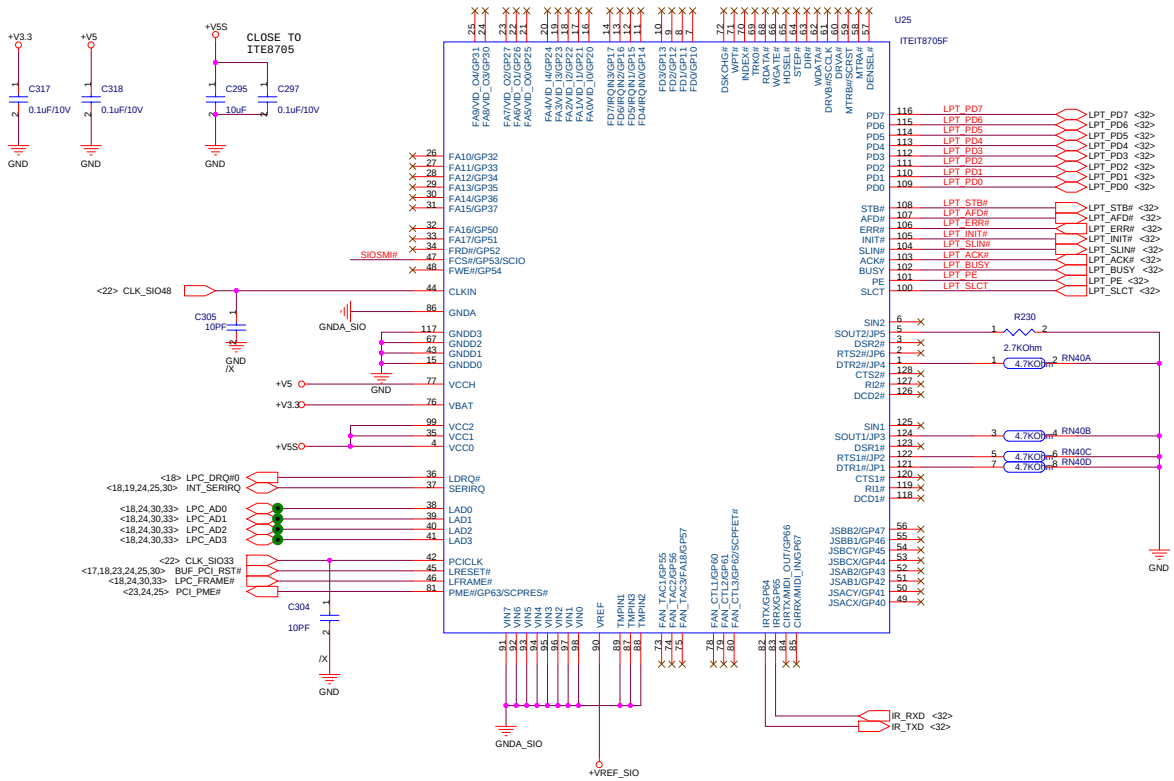
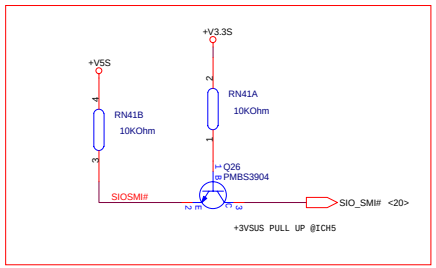
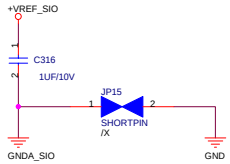
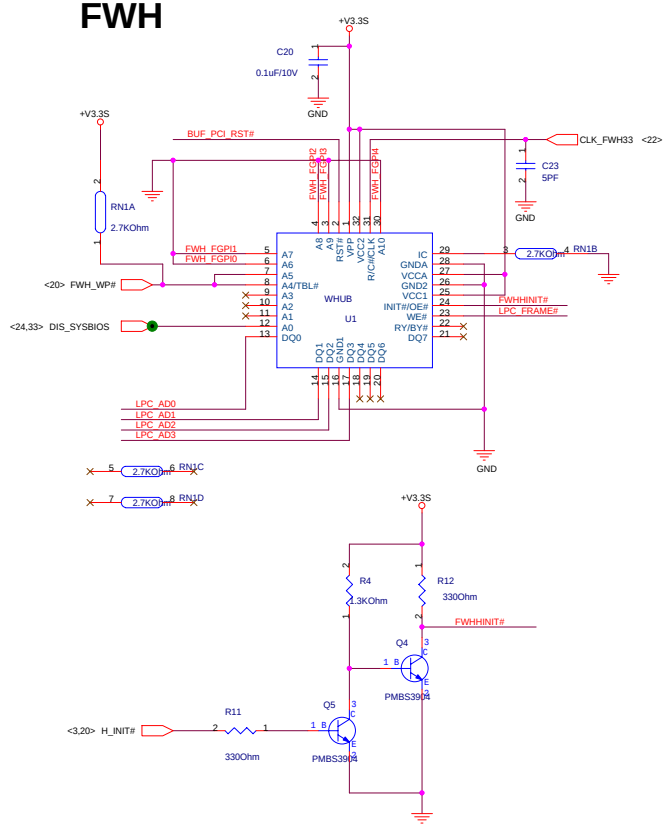
Super I/O





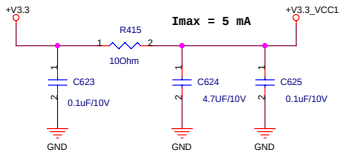


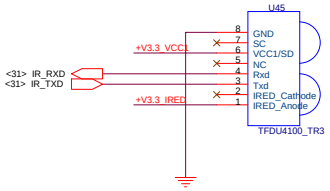
FWH

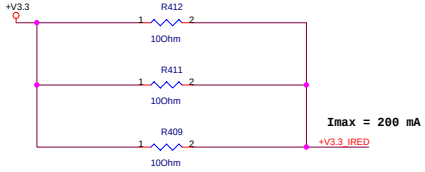


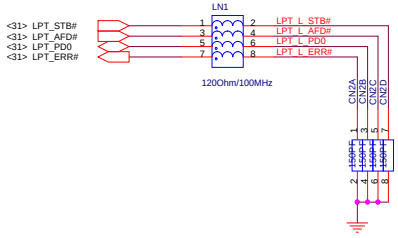
ASUSTEK CO.,LTD.	Title :	Superl/O&FWH	
	Engineer:	Lassie_Bao	
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 31 of 57		

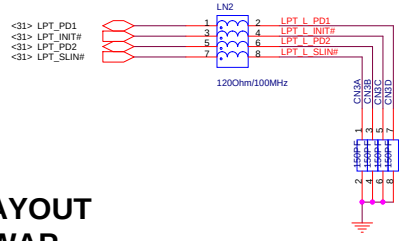
IR

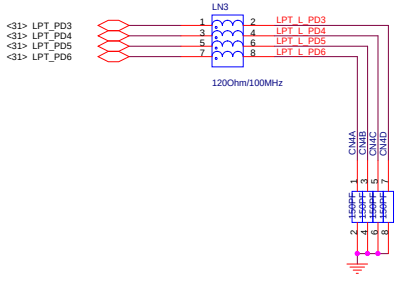


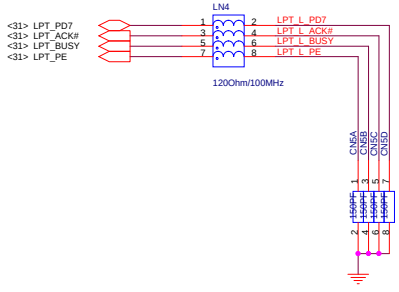




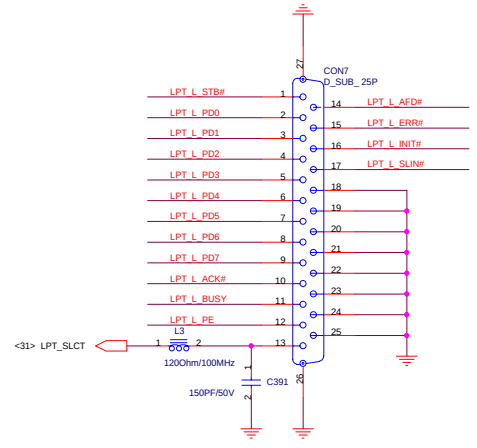








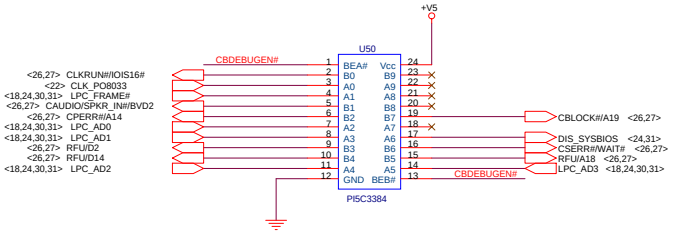
LAYOUT SWAP

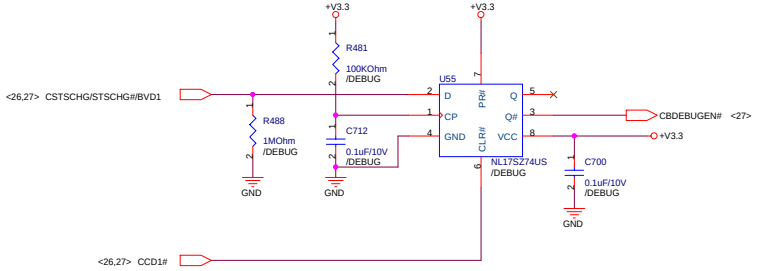


PRINT PORT

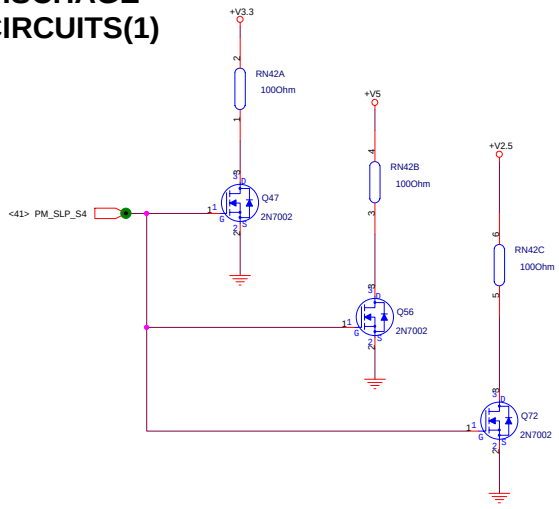
ASUSTEK CO.,LTD.	Title : IR&LPT PORT	
	Engineer: Lassie_Bao	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 32 of 57	

PCMCIA DEBUG CARD

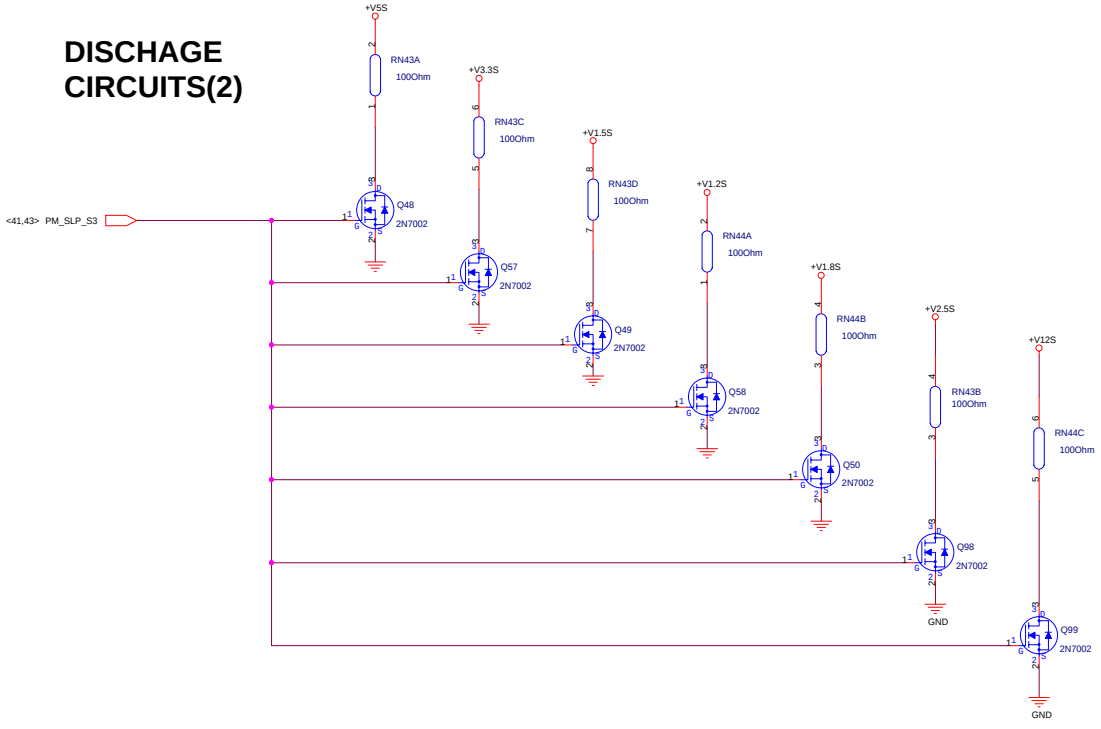




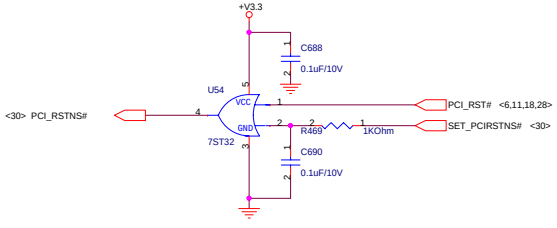
DISCHAGE CIRCUITS(1)



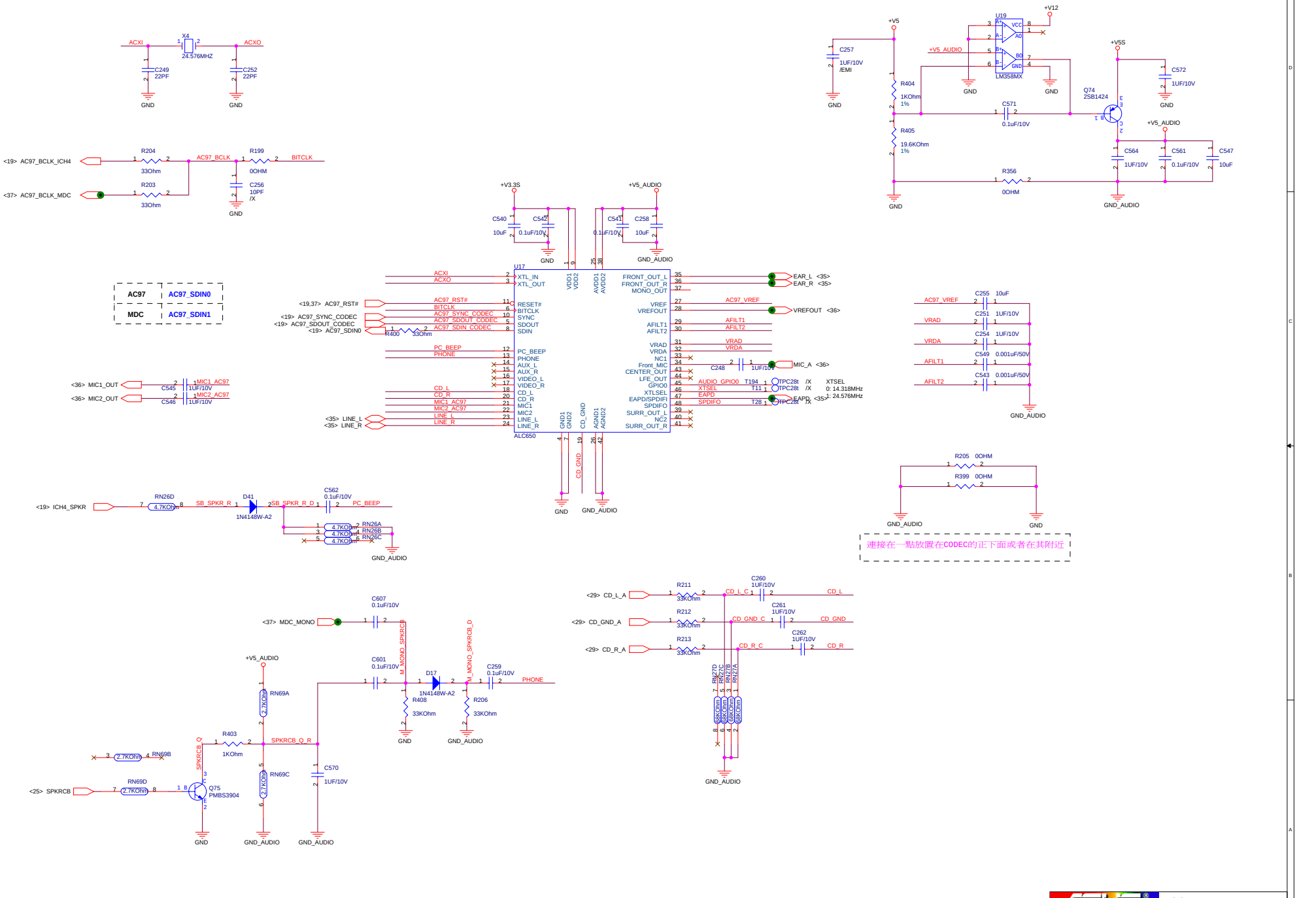
DISCHAGE CIRCUITS(2)



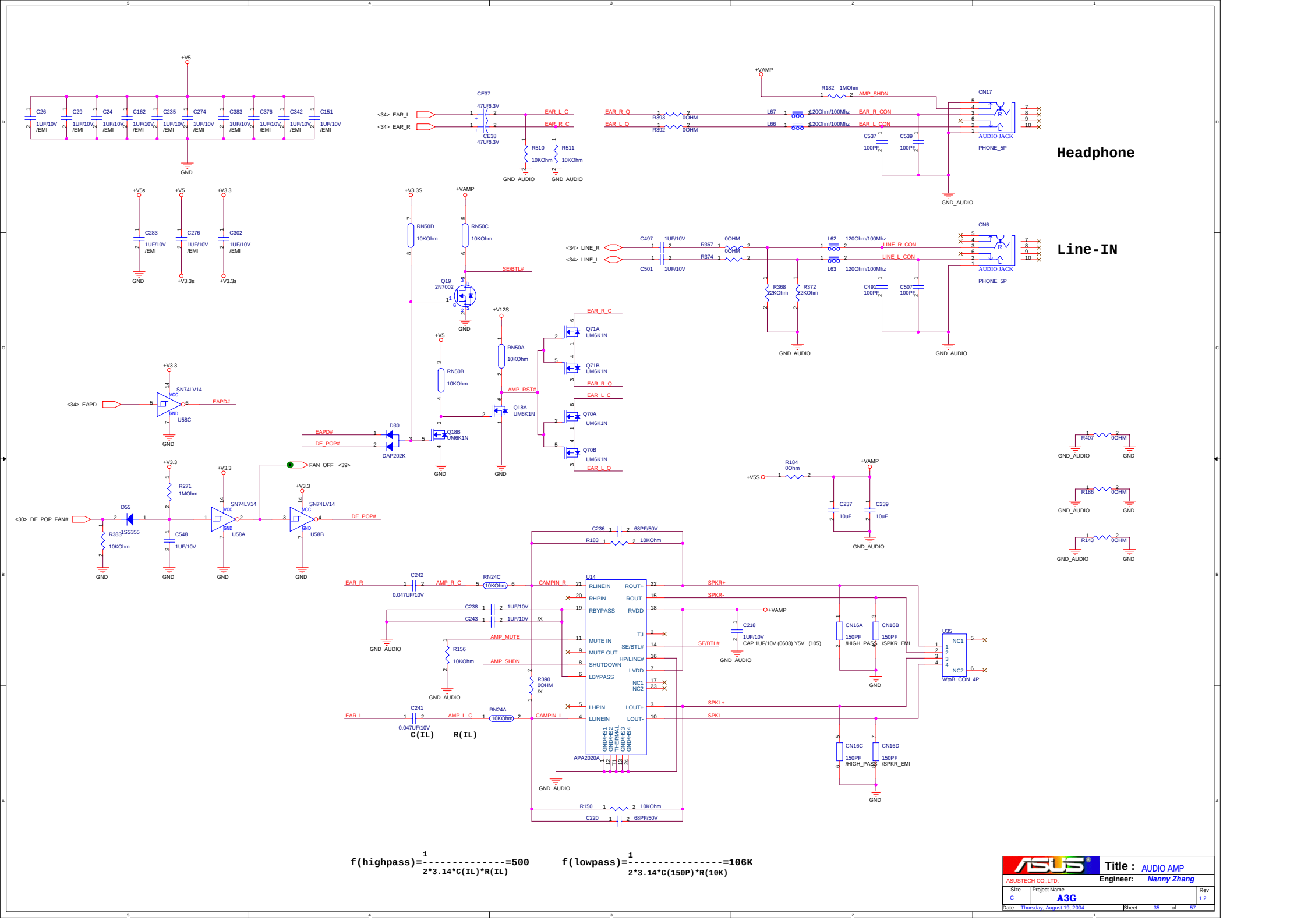
PCI_RSTNS# Gen Circuit



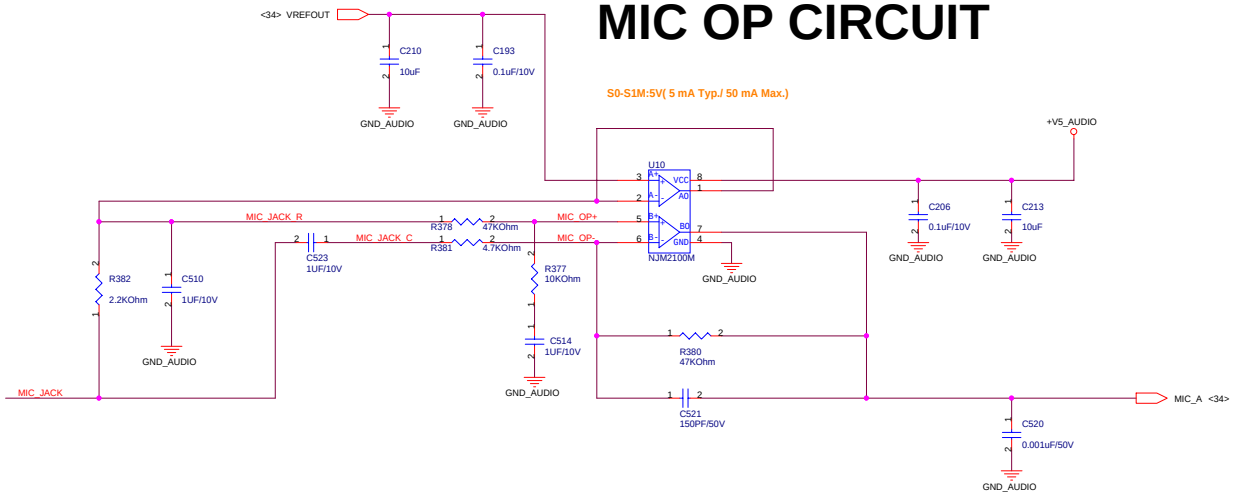
ASUSTEK CO.,LTD.	Title : DEBUG PORT	
	Engineer: Lassie_Bao	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 33 of 57	



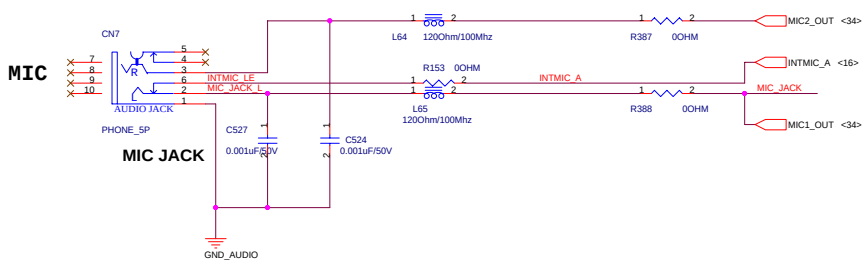
ASUSTEK CO.,LTD.	Title : CODEC-ALC650		
	Engineer: Nanny Zhang		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 34 of 57		


Headphone
Line-IN
C(IL) R(IL)
f(highpass)=1/(2*3.14*C(IL)*R(IL))=500
f(lowpass)=1/(2*3.14*C(150P)*R(10K))=106K
Title : AUDIO AMP
ASUSTECH CO.,LTD.
Engineer: Nanny Zhang
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 35 of 57

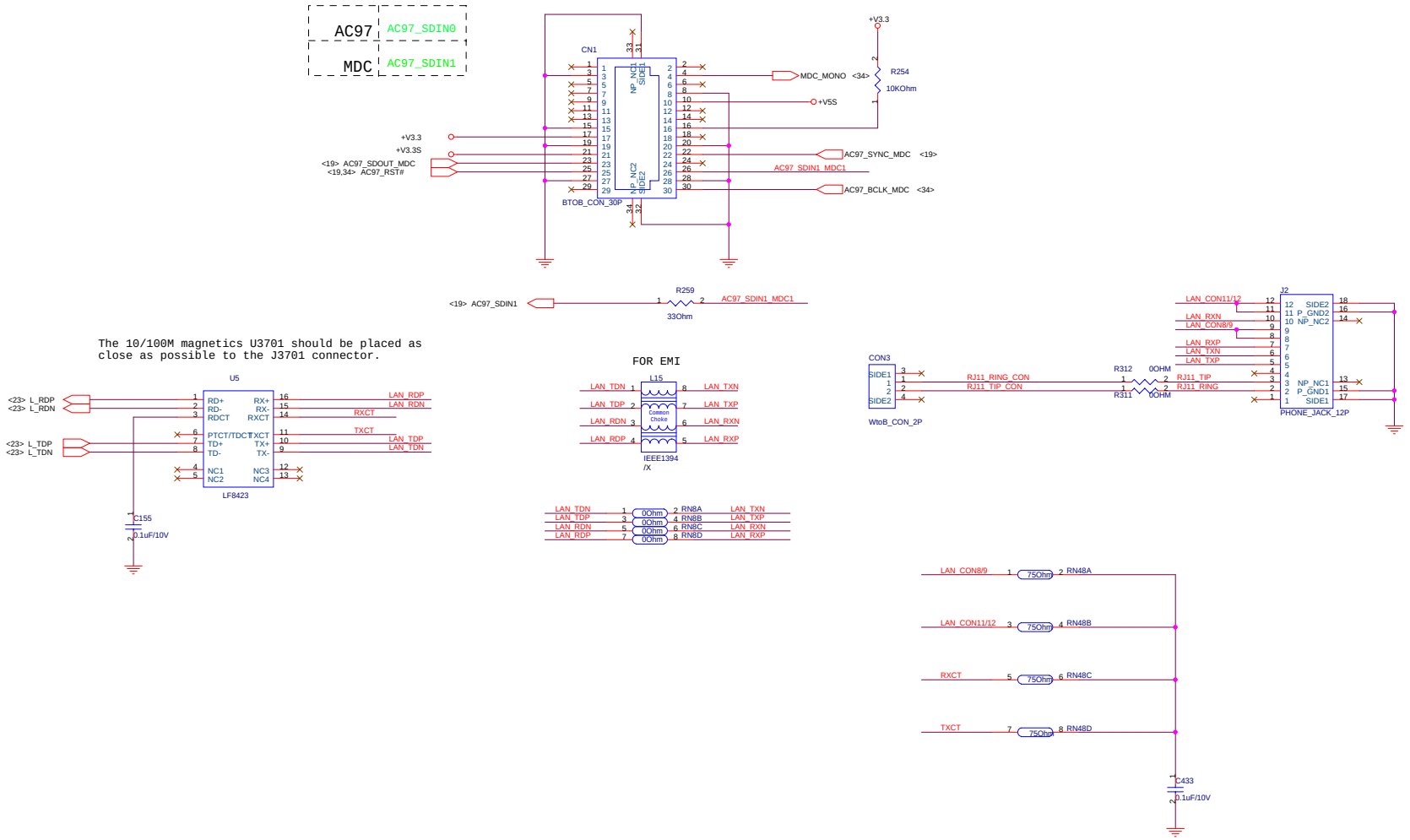
MIC OP CIRCUIT



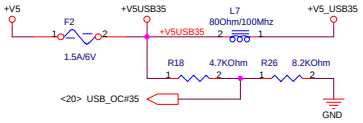
MIC JACK

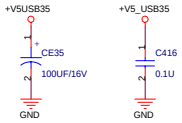


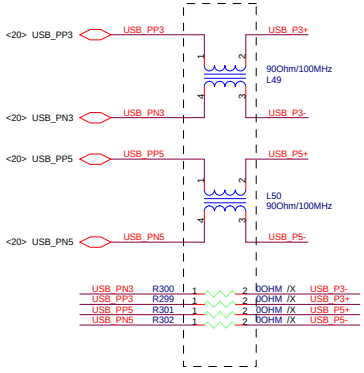
ASUSTECH CO.,LTD.	Title : MIC	
	Engineer: Nanny Zhang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 36 of 57	



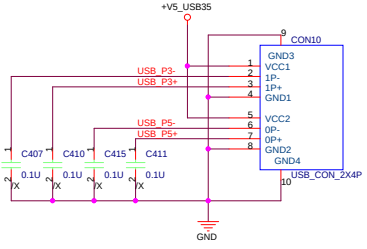
Title :	MDC&RJ45&RJ11
ASUSTECH CO.,LTD.	Engineer: Sleck Song
Size: C	Project Name: A3G
Rev: 1.2	
Date: Thursday, August 19, 2004	Sheet 37 of 57





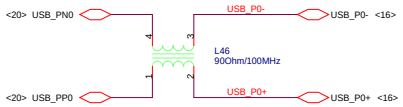


C & L Co-Lay

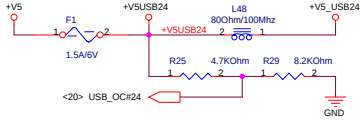


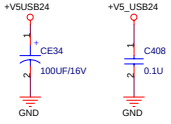
USB PORT 3 & PORT 5

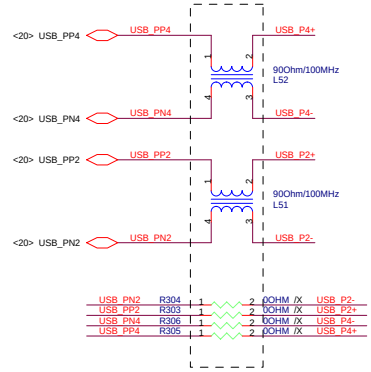
USB PORT 0 for WLAN



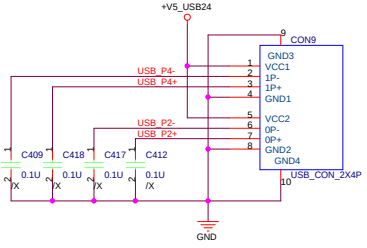
choke位置的原因,Port 0 正負與其他Port相反 (03/17)





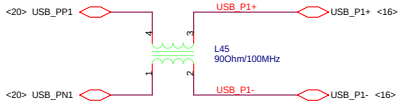


C & L Co-Lay



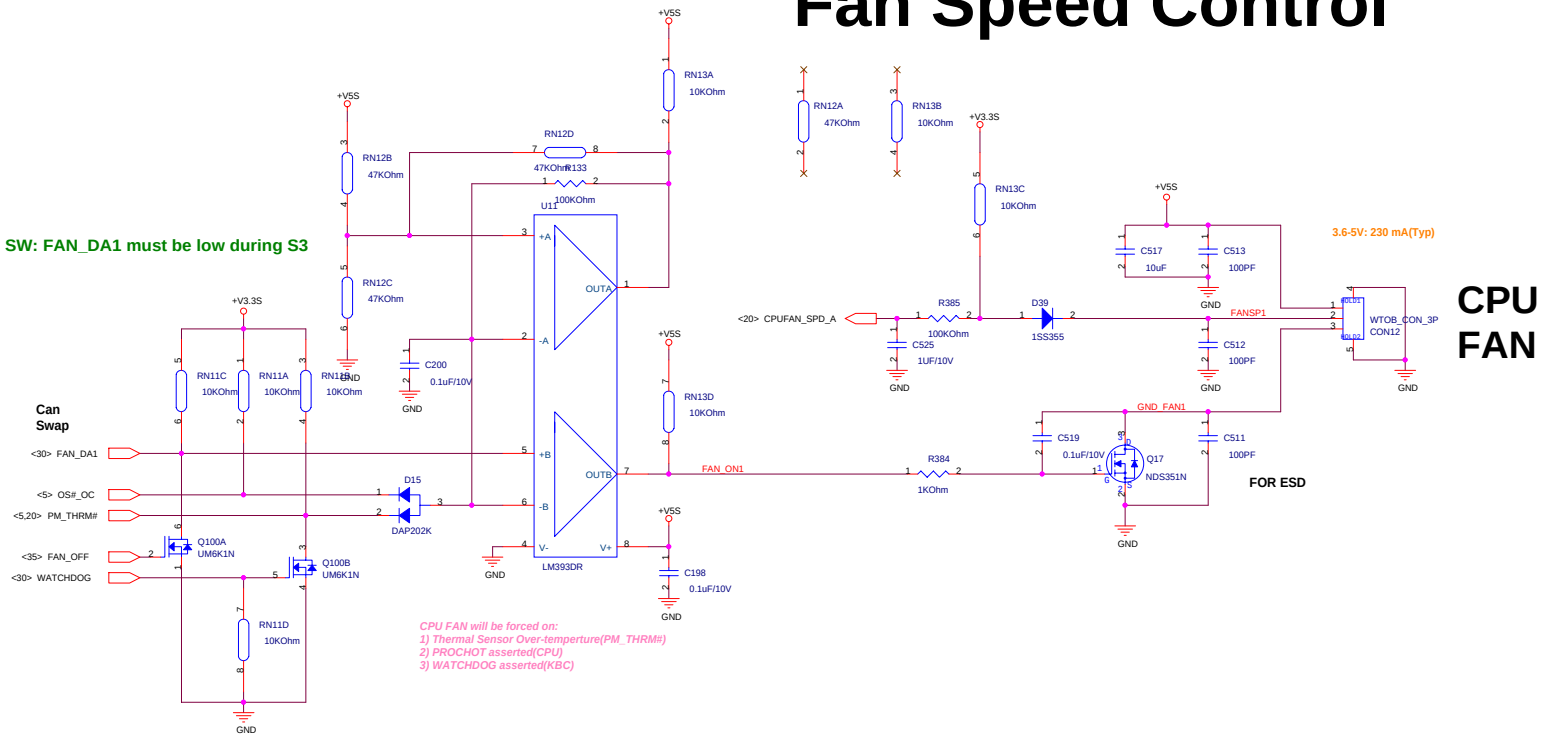
USB PORT 2 & PORT 4

USB PORT 1 for CAMERA



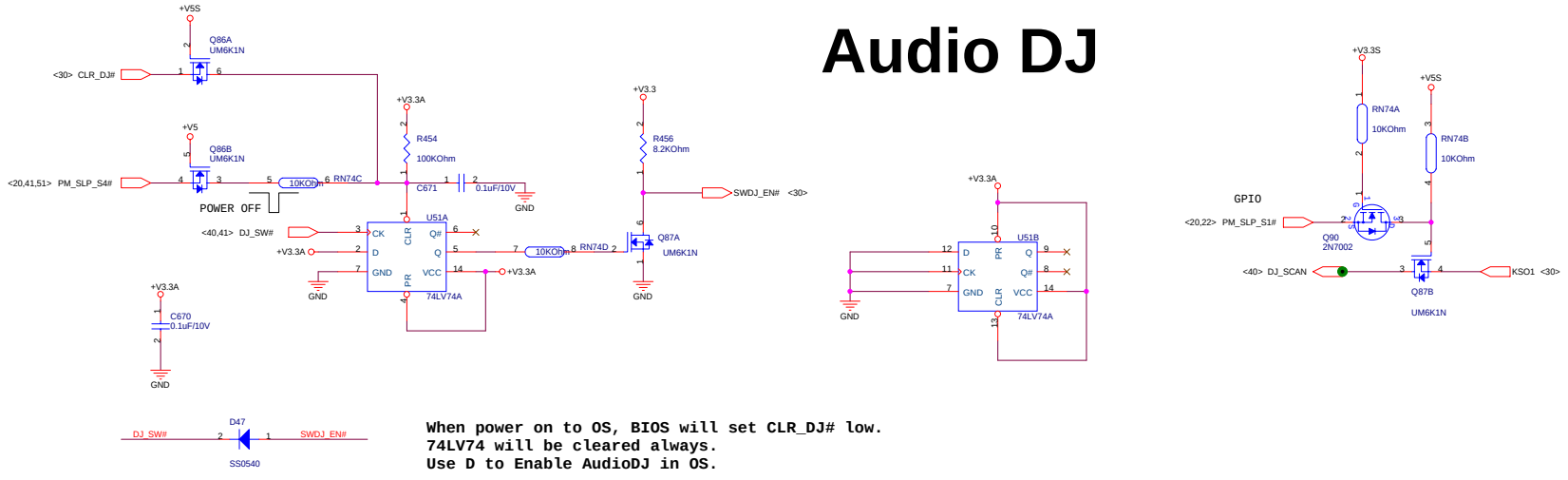
ASUSTEK CO.,LTD.	Title : USBPORT	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 38 of 57	

Fan Speed Control



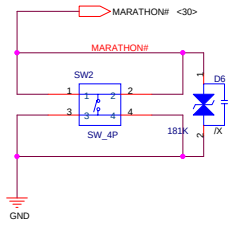
CPU FAN

Audio DJ



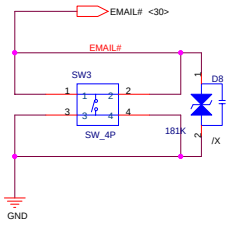
When power on to OS, BIOS will set CLR_DJ# low.
74LV74 will be cleared always.
Use D to Enable AudioDJ in OS.

ASUSTECH CO.,LTD.	Title : FAN&Audio DJ	
	Engineer: BENZ CAI	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 39 of 57	



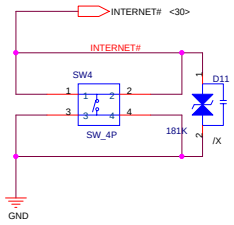
Power4 Gear

FOLLOW A3N



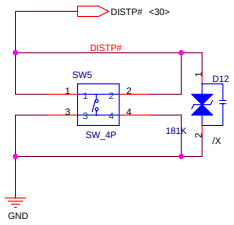
E-Mail

FOLLOW A3N



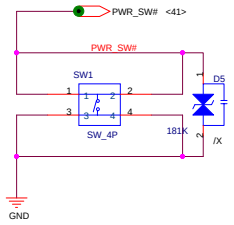
Internet

FOLLOW A3N



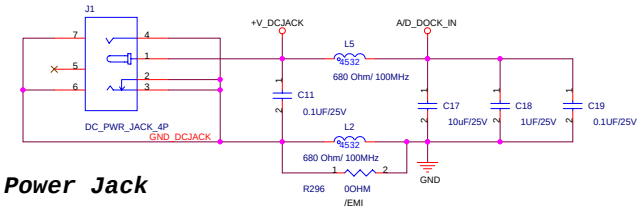
Touchpad Disable

FOLLOW A3N

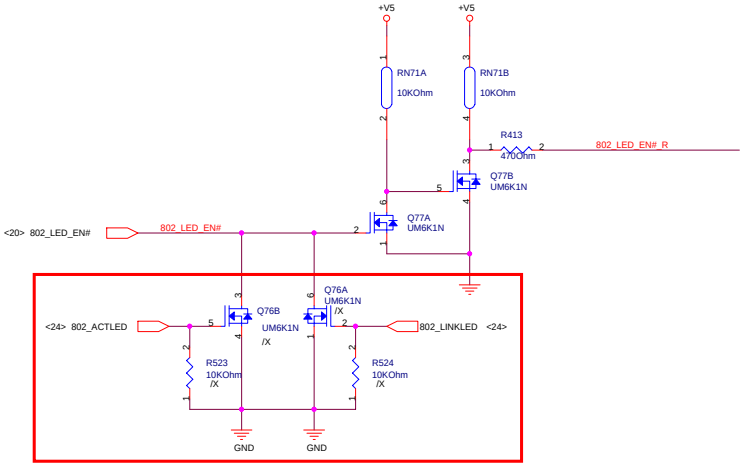


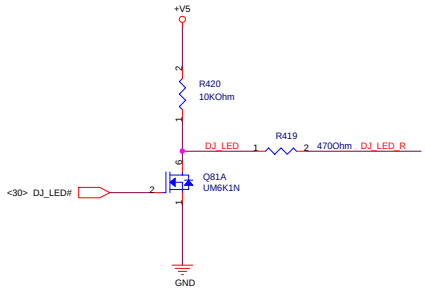
Power Switch

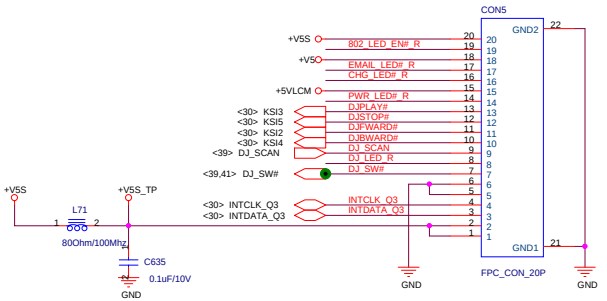
FOLLOW A3N

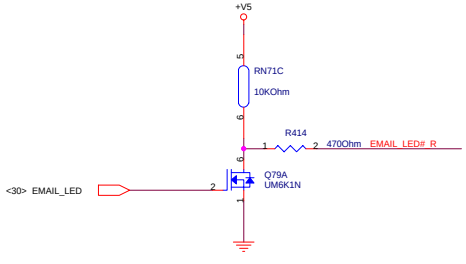


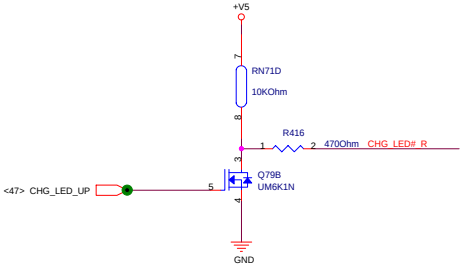
DC Power Jack

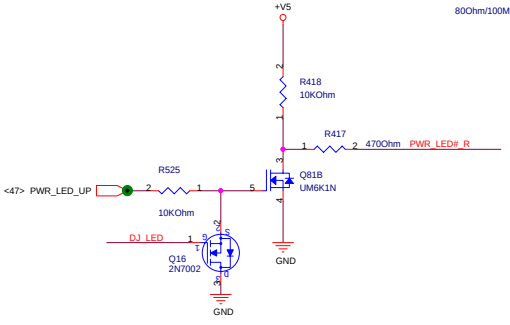












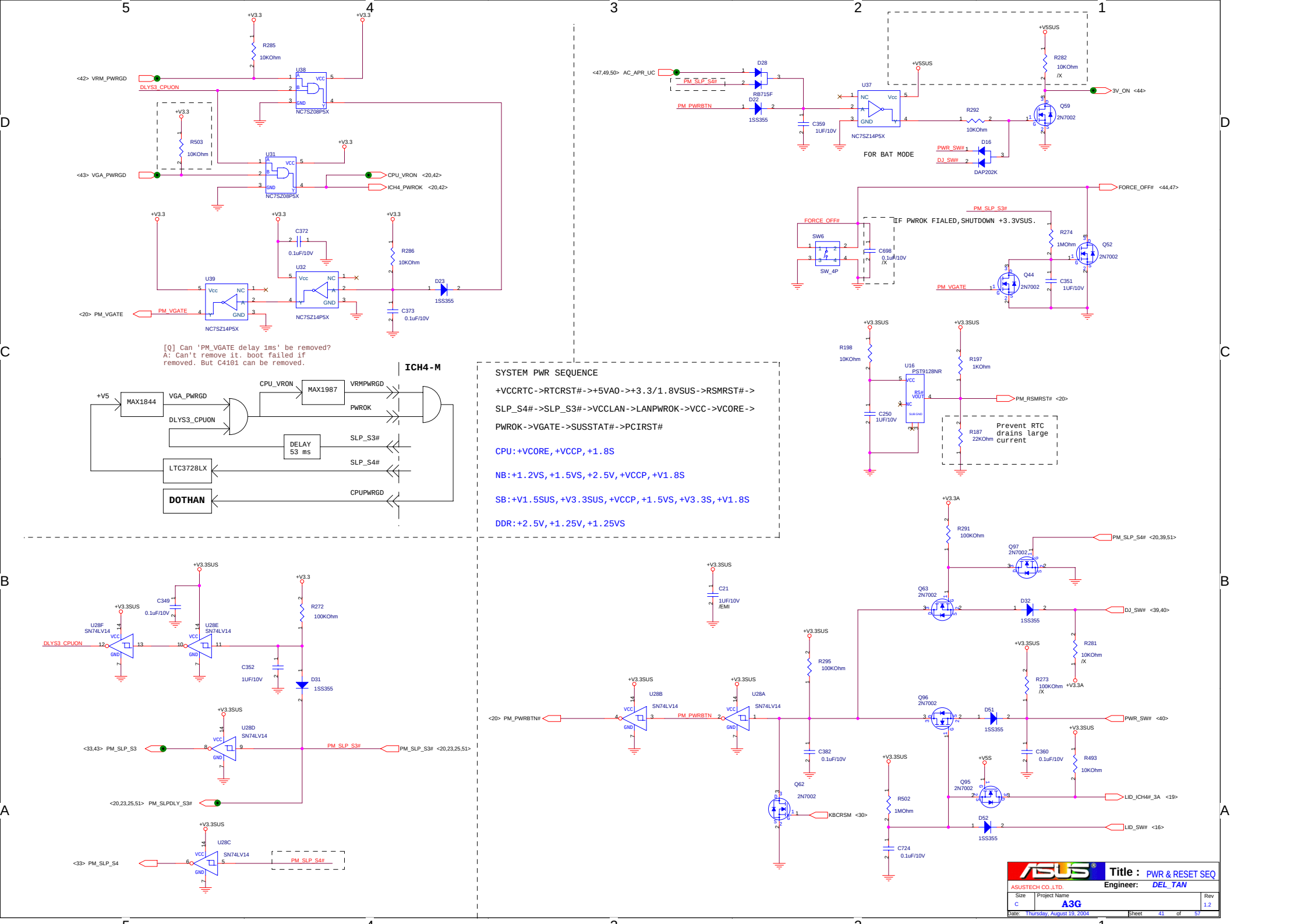
ASUSTEK CO.,LTD.

Title : FUNCTION KEY

Engineer: BENZ CAI

Size	Project Name	Rev
C	A3G	1.2

Date: Thursday, August 19, 2004 Sheet 40 of 57


R285
10KOhm
U38
NC7SZ08P5X
<42> VRM_PWRGD
DLYS3_CPUON
R503
10KOhm
U31
NC7SZ08P5X
<43> VGA_PWRGD
CPU_VRON <20,42>
ICH4_PWROK <20,42>
C372
0.1uF/10V
U32
NC7SZ14P5X
R286
10KOhm
D23
1SS355
C373
0.1uF/10V
U39
NC7SZ14P5X
<20> PM_VGATE
PM_VGATE
[Q] Can 'PM_VGATE delay 1ms' be removed?
A: Can't remove it. boot failed if
removed. But C4101 can be removed.
ICH4-M
+V5
MAX1844
VGA_PWRGD
DLYS3_CPUON
CPU_VRON
MAX1987
VRMPWRGD
PWROK
DELAY
53 ms
SLP_S3#
SLP_S4#
LTC3728LX
DOTHAN
CPUPWRGD
SYSTEM PWR SEQUENCE
+VCCRTC->RTCRST#->+5VAO->+3.3/1.8VSUS->RSMRST#->
SLP_S4#->SLP_S3#->VCCLAN->LANPWROK->VCC->VCORE->
PWROK->VGATE->SUSSTAT#->PCIRST#
CPU:+VCORE,+VCCP,+1.8S
NB:+1.2VS,+1.5VS,+2.5V,+VCCP,+V1.8S
SB:+V1.5SUS,+V3.3SUS,+VCCP,+1.5VS,+V3.3S,+V1.8S
DDR:+2.5V,+1.25V,+1.25VS
<47,49,50> AC_APR_UC
PM_SLP_S4#
PM_PWRBTN
D28
RB715F
D22
1SS355
C359
1UF/10V
U37
NC7SZ14P5X
FOR BAT MODE
R282
10KOhm
/X
3V_ON <44>
R292
10KOhm
Q59
2N7002
PWR_SW#
DJ_SW#
D16
DAP202K
FORCE_OFF# <44,47>
IF PWROK FIALED,SHUTDOWN +3.3VSUS.
SW6
SW_4P
C698
0.1uF/10V
/X
R274
1MOhm
Q52
2N7002
Q44
2N7002
C351
1UF/10V
PM_VGATE
R198
10KOhm
U16
PST9128NR
R197
1KOhm
PM_RSMRST# <20>
C250
1UF/10V
R187
22KOhm
Prevent RTC
drains large
current
C349
0.1uF/10V
U28F
SN74LV14
U28E
SN74LV14
R272
100KOhm
C352
1UF/10V
D31
1SS355
U28D
SN74LV14
<33,43> PM_SLP_S3
PM_SLP_S3#
PM_SLP_S3# <20,23,25,51>
<20,23,25,51> PM_SLPDLY_S3#
U28C
SN74LV14
<33> PM_SLP_S4
PM_SLP_S4#
C21
1UF/10V
/EMI
U28B
SN74LV14
U28A
SN74LV14
<20> PM_PWRBTN#
PM_PWRBTN
R295
100KOhm
C382
0.1uF/10V
Q62
2N7002
KBCRSM <30>
R291
100KOhm
Q97
2N7002
PM_SLP_S4# <20,39,51>
Q63
2N7002
D32
1SS355
DJ_SW# <39,40>
R281
10KOhm
/X
R273
100KOhm
/X
Q96
2N7002
D51
1SS355
PWR_SW# <40>
C360
0.1uF/10V
R493
10KOhm
R502
1MOhm
C724
0.1uF/10V
Q95
2N7002
LID_ICH4#_3A <19>
D52
1SS355
LID_SW# <16>
Title : PWR & RESET SEQ
ASUSTECH CO.,LTD.
Engineer: DEL_TAN
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
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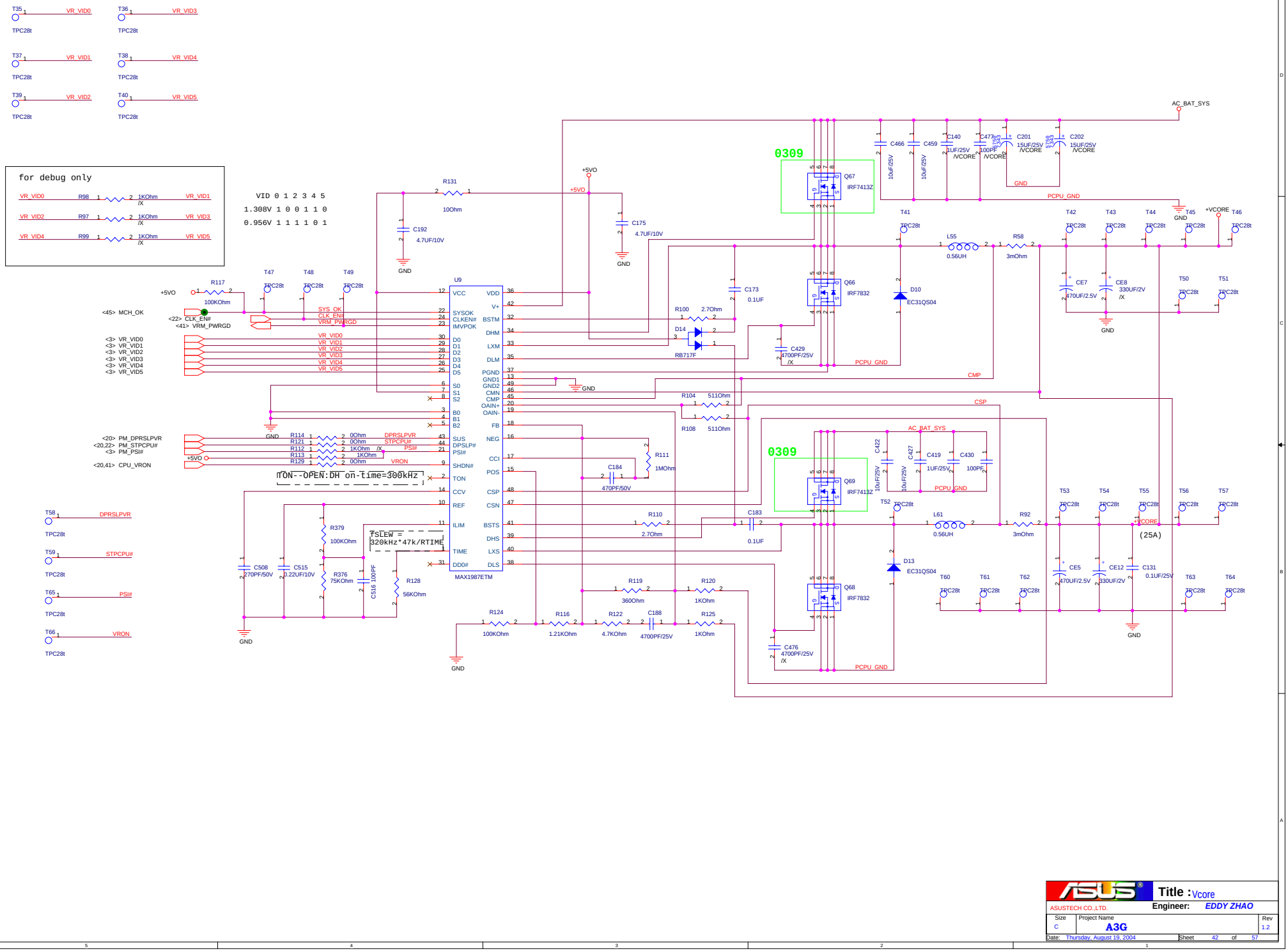
for debug only
VR_VID0 R98 1KOhm /X VR_VID1
VR_VID2 R97 1KOhm /X VR_VID3
VR_VID4 R99 1KOhm /X VR_VID5
VID 0 1 2 3 4 5
1.308V 1 0 0 1 1 0
0.956V 1 1 1 1 0 1
T35 VR_VID0
T36 VR_VID3
T37 VR_VID1
T38 VR_VID4
T39 VR_VID2
T40 VR_VID5
TPC28t
U9
MAX1987ETM
VCC VDD SYSOK CLKEN# IMVPOK D0 D1 D2 D3 D4 D5 S0 S1 S2 B0 B1 B2 SUS DPSLP# PSI# SHDN# TON CCV REF ILIM TIME DD0# VDD V+ BSTM DHM LXM DLM PGND GND1 GND2 CMN CMP OAIN+ OAIN- FB NEG CCI POS CSP CSN BSTS DHS LXS DLS
<45> MCH_OK
<22> CLK_EN#
<41> VRM_PWRGD
SYS_OK
CLK_EN#
VRM_PWRGD
<3> VR_VID0
<3> VR_VID1
<3> VR_VID2
<3> VR_VID3
<3> VR_VID4
<3> VR_VID5
<20> PM_DPRSLPVR
<20,22> PM_STPCPU#
<3> PM_PSI#
<20,41> CPU_VRON
DPRSLPVR
STPCPU#
PSI#
VRON
ON--OPEN:DH on-time=300kHz
fSLEW = 320kHz*47k/RTIME
0309
Q67 IRF7413Z
Q66 IRF7832
Q69 IRF7413Z
Q68 IRF7832
D10 EC31QS04
D13 EC31QS04
D14 RB717F
L55 0.56UH
L61 0.56UH
R58 3mOhm
R92 3mOhm
R131 10Ohm
R100 2.7Ohm
R104 511Ohm
R108 511Ohm
R110 2.7Ohm
R111 1MOhm
R117 100KOhm
R379 100KOhm
R376 75KOhm
R128 56KOhm
R124 100KOhm
R116 1.21KOhm
R122 4.7KOhm
R119 360Ohm
R120 1KOhm
R125 1KOhm
C192 4.7UF/10V
C175 4.7UF/10V
C173 0.1UF
C183 0.1UF
C184 470PF/50V
C188 4700PF/25V
C429 4700PF/25V /X
C476 4700PF/25V /X
C508 270PF/50V
C515 0.22UF/10V
C516 100PF
C466 10uF/25V
C459 10uF/25V
C140 1UF/25V /VCORE
C477 100PF /VCORE
C201 15UF/25V /VCORE
C202 15UF/25V /VCORE
C422 10uF/25V
C427 10uF/25V
C419 1UF/25V
C430 100PF
CE7 470UF/2.5V
CE8 330UF/2V /X
CE5 470UF/2.5V
CE12 330UF/2V
C131 0.1UF/25V
AC_BAT_SYS
+5VO
+VCORE
(25A)
PCPU_GND
CMP
CSP
GND
Title : Vcore
ASUSTECH CO.,LTD.
Engineer: EDDY ZHAO
Size C
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
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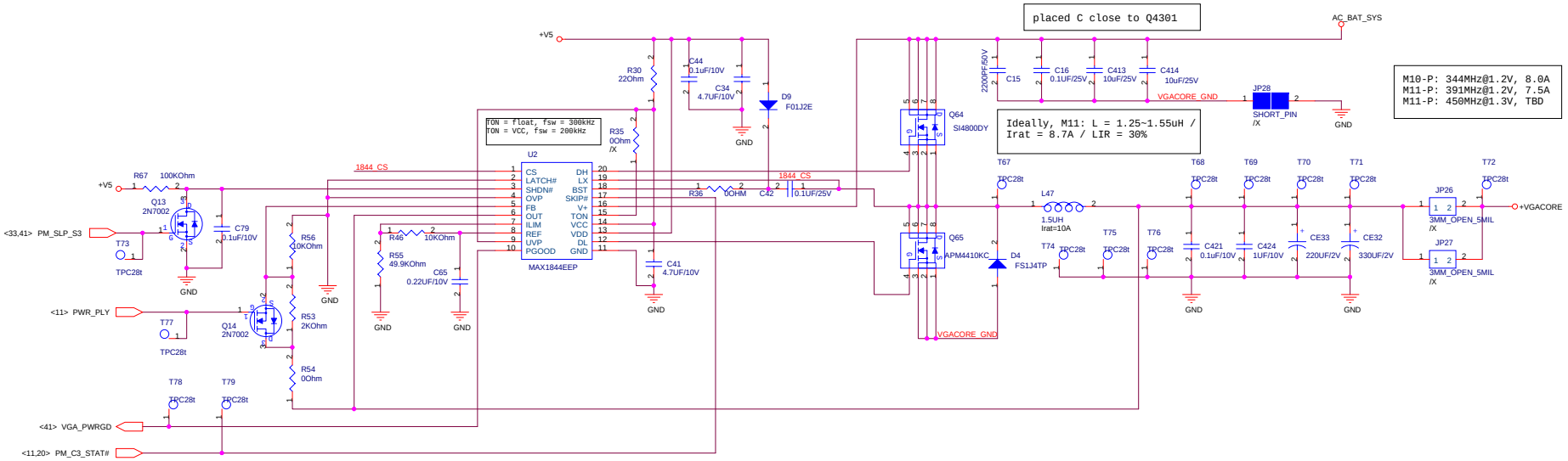

M9+X:	M10/M11:
R4306 = 8KOhm, 10-003418026-21 R4308 = R4309 = 2KOhm, 10-004412020 PWR_PLY=H, VGACORE=1.25V PWR_PLY=L, VGACORE=1.5V	R4306 = 10KOhm, 10-004401030 R4308 = 2KOhm, 10-004412020 R4309 = 0Ohm, 10-004400000 PWR_PLY = H, VGACORE=1.0V PWR_PLY = L, VGACORE=1.2V

ASUSTECH CO.,LTD.

Title : VGACORE

Engineer: Pommy Lu

Size	Project Name	Rev
C	A3G	1.2

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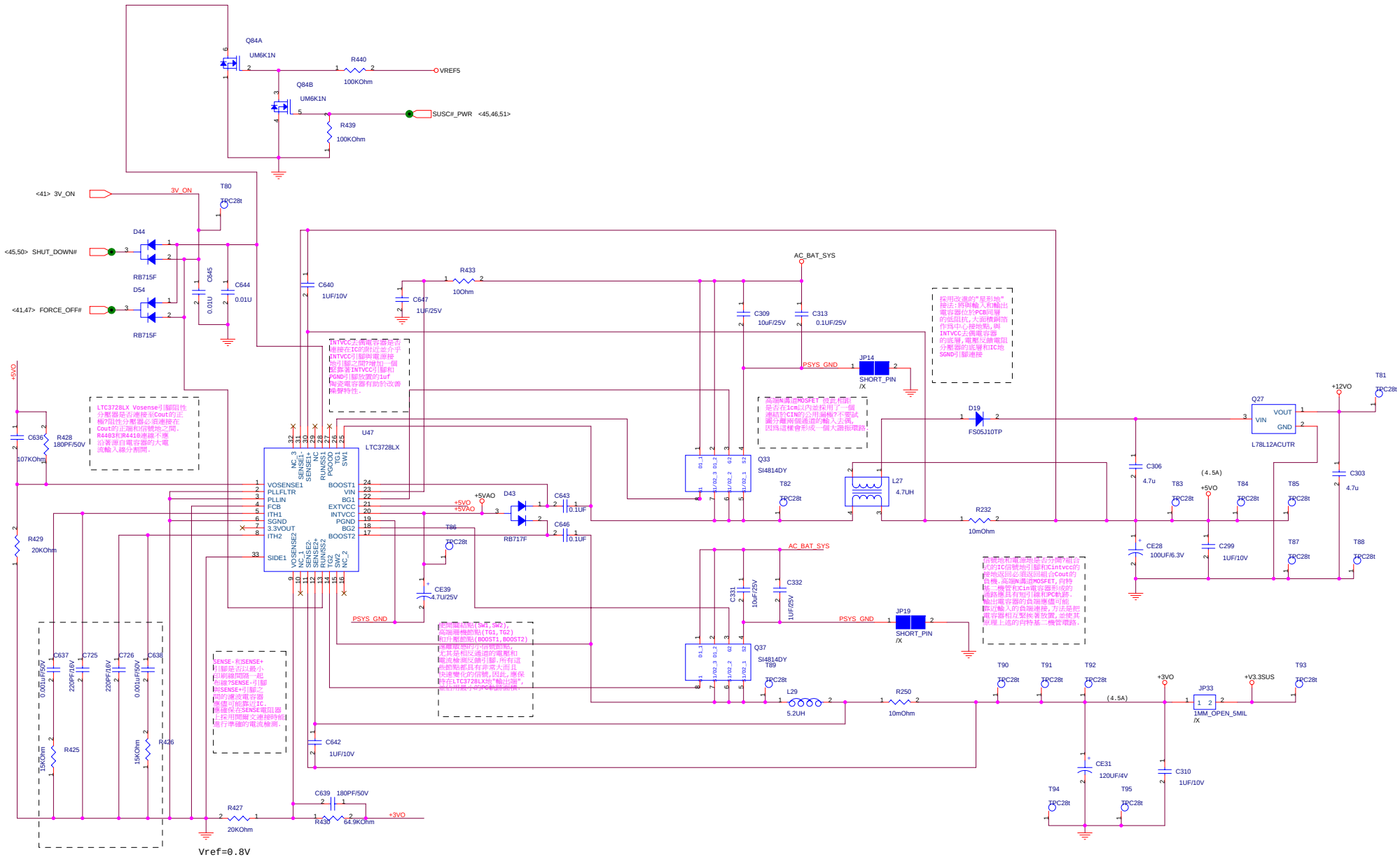
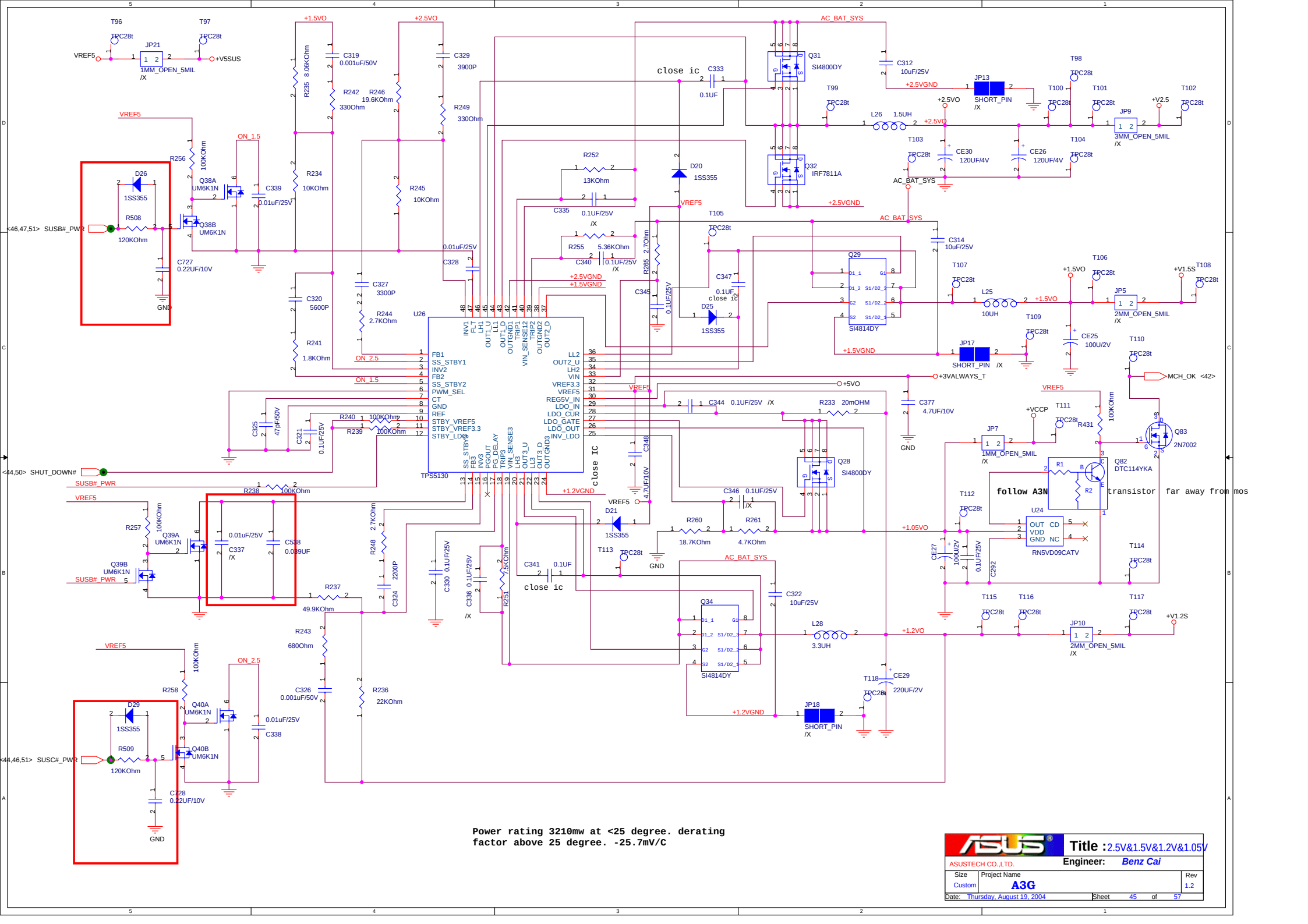
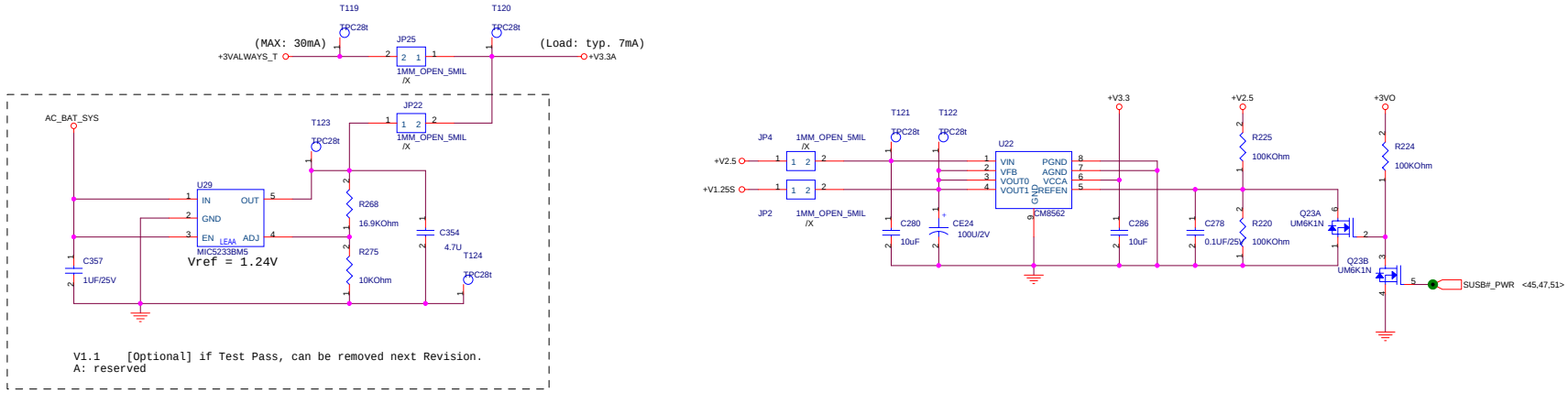
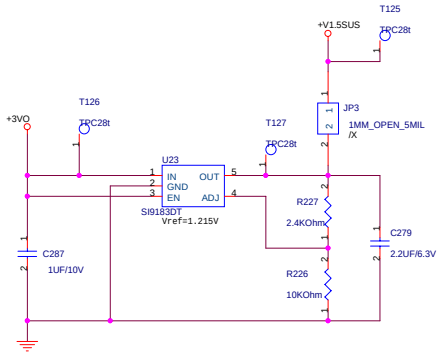
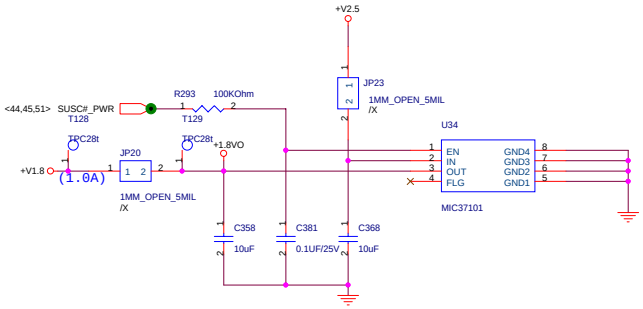


ASUSTEK CO.,LTD.	Title : SYSTEM		
	Engineer: NANNY ZHANG		
Size: C	Project Name: A3G		Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 44 of 57		

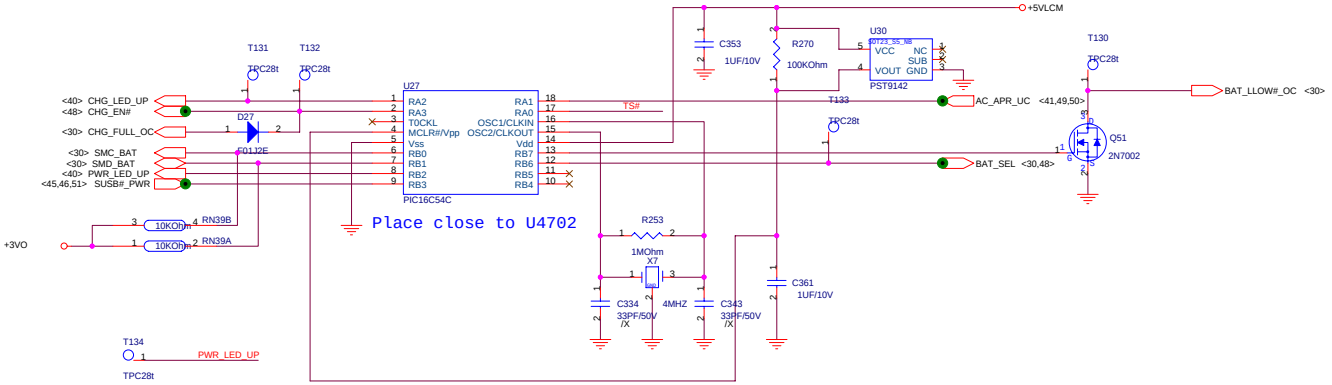

TPS5130
U26
close IC
close ic
follow A3N transistor far away from mos
Power rating 3210mw at <25 degree. derating factor above 25 degree. -25.7mV/C
Title : 2.5V&1.5V&1.2V&1.05V
ASUSTECH CO.,LTD.
Engineer: Benz Cai
Size Custom
Project Name A3G
Rev 1.2
Date: Thursday, August 19, 2004
Sheet 45 of 57

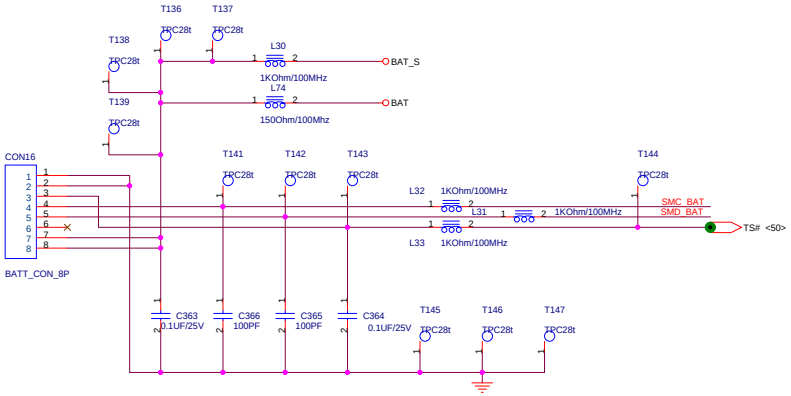


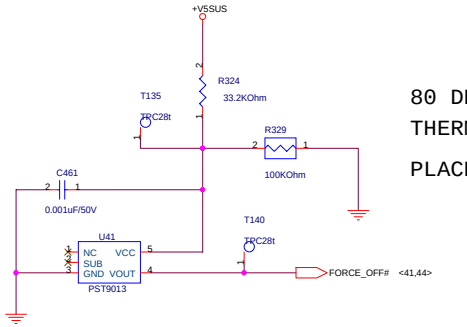




ASUSTECH CO.,LTD.	Title : 1.25V&1.8V	
	Engineer: Sleck Song	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 46 of 57	



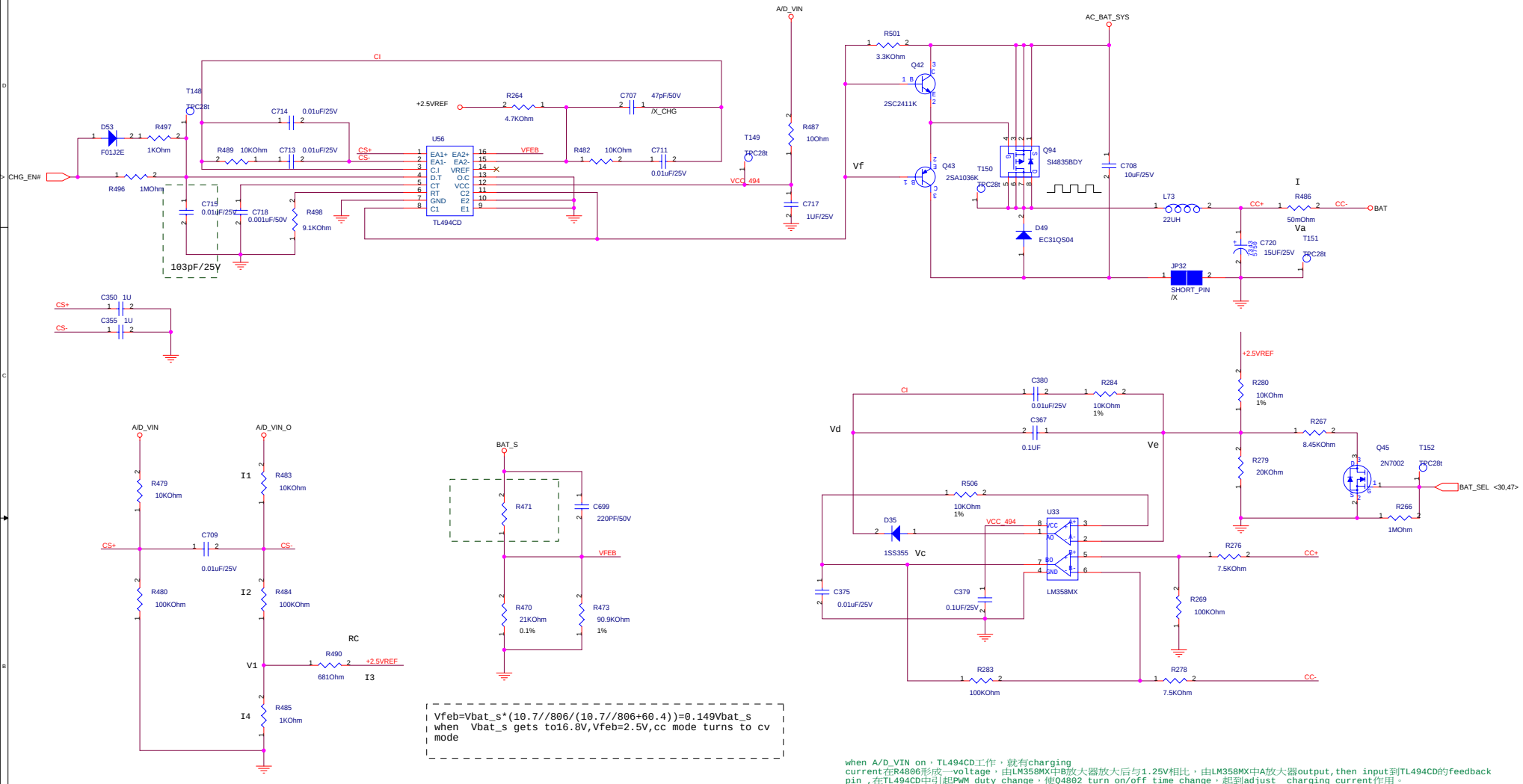




80 DEGREE C
THERMAL PROTECTION

PLACE UNDER CPU

ASUSTECH CO.,LTD.	Title : PIC16C54C	
	Engineer: DEL_TAN	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 47 of 57	



Vfeb=Vbat_s*(10.7//806/(10.7//806+60.4))=0.149Vbat_s
when Vbat_s gets to16.8V,Vfeb=2.5V,cc mode turns to cv mode

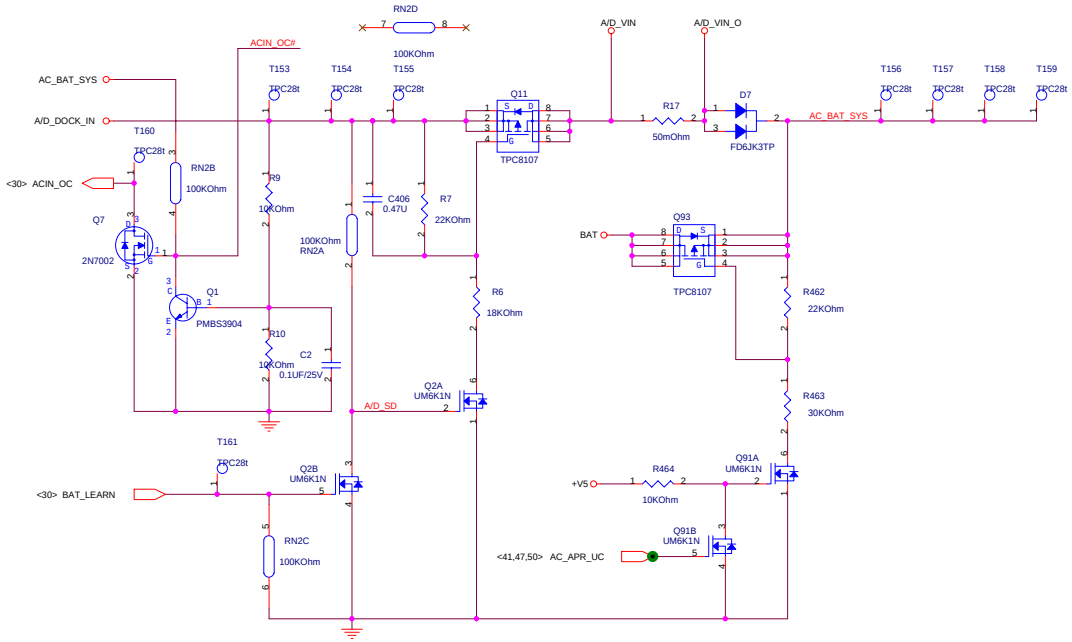
current sharing=3.1A

A/D_VIN=19V A/D_VIN_O=19V-3.1A*50mohm=18.845V
CS+=CS-=19V*100/(10+100)=17.272727V
I1=(18.845V-17.272727V)/10K=0.15723mA
V1=17.272727V-0.15723mA*100K=1.5497V
I4=1.5497V/1K=1.5497mA
I3=I4-I1=1.39247mA
RC=(2.5V-1.5497V)/1.39247mA=681 Ohm

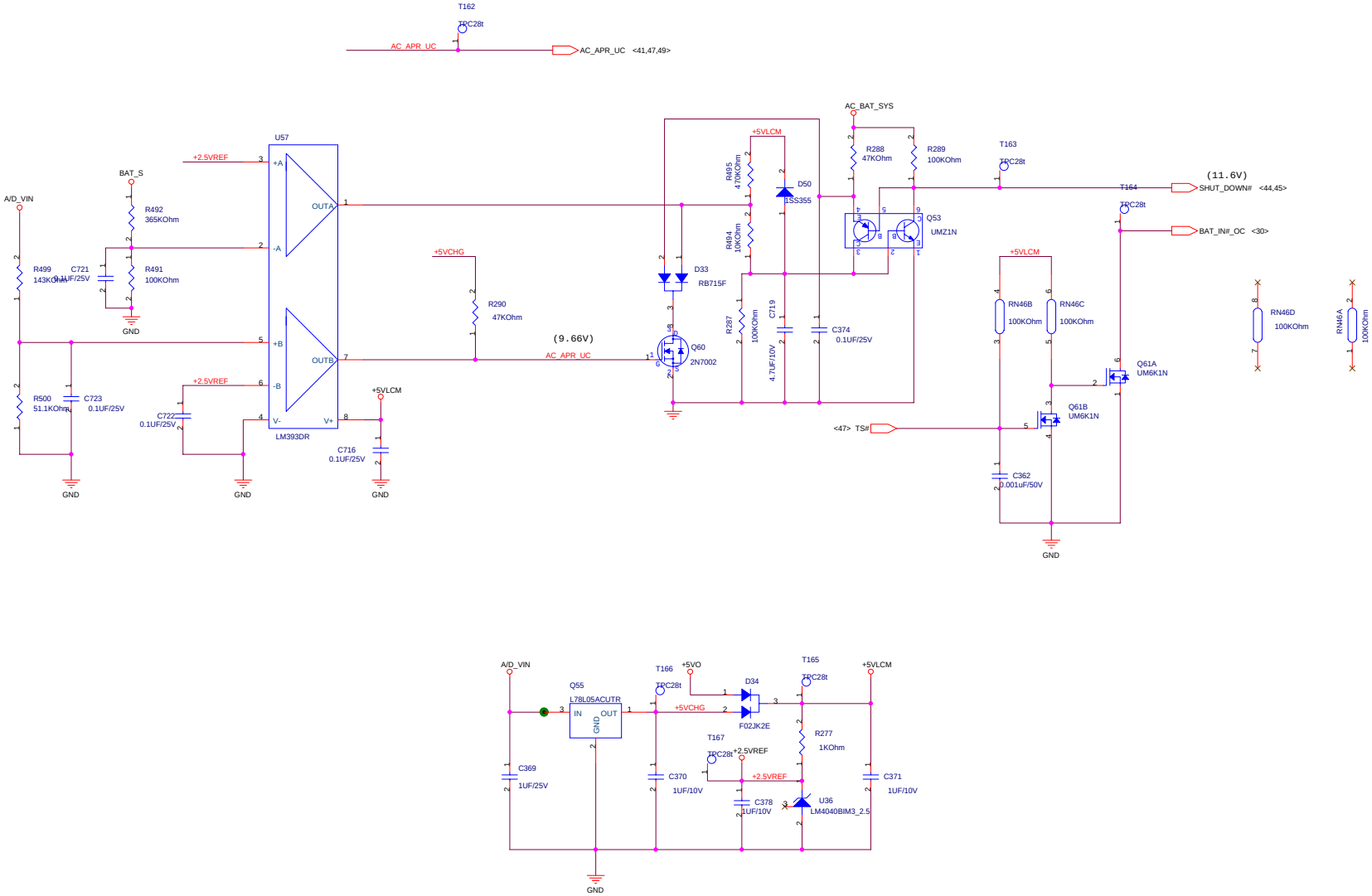
when A/D_VIN on，TL494CD工作，就有charging current在R4806形成一voltage，由LM358MX中B放大器放大后与1.25V相比，由LM358MX中A放大器output,then input到TL494CD的feedback pin ,在TL494CD中引起PWM duty change，使Q4802 turn on/off time change，起到adjust charging current作用。
例：I增大,致Va增大,致Vc增大,致Vc>Ve(=1.25V) ,致Vd增大,致PWM duty增大,致 Vf降低,致Q4802 turn on time降低,致I降低
由上起到cc模式控制。when平衡,Vc=1.25V,可算出I。I*20mOHM*24.9/25.9*(1+24.9/1)=1.25,so I=2.51A

Q1:How to get 3.1A?
Q2:CS+=CS-,Why or the purpose? and with EA1?

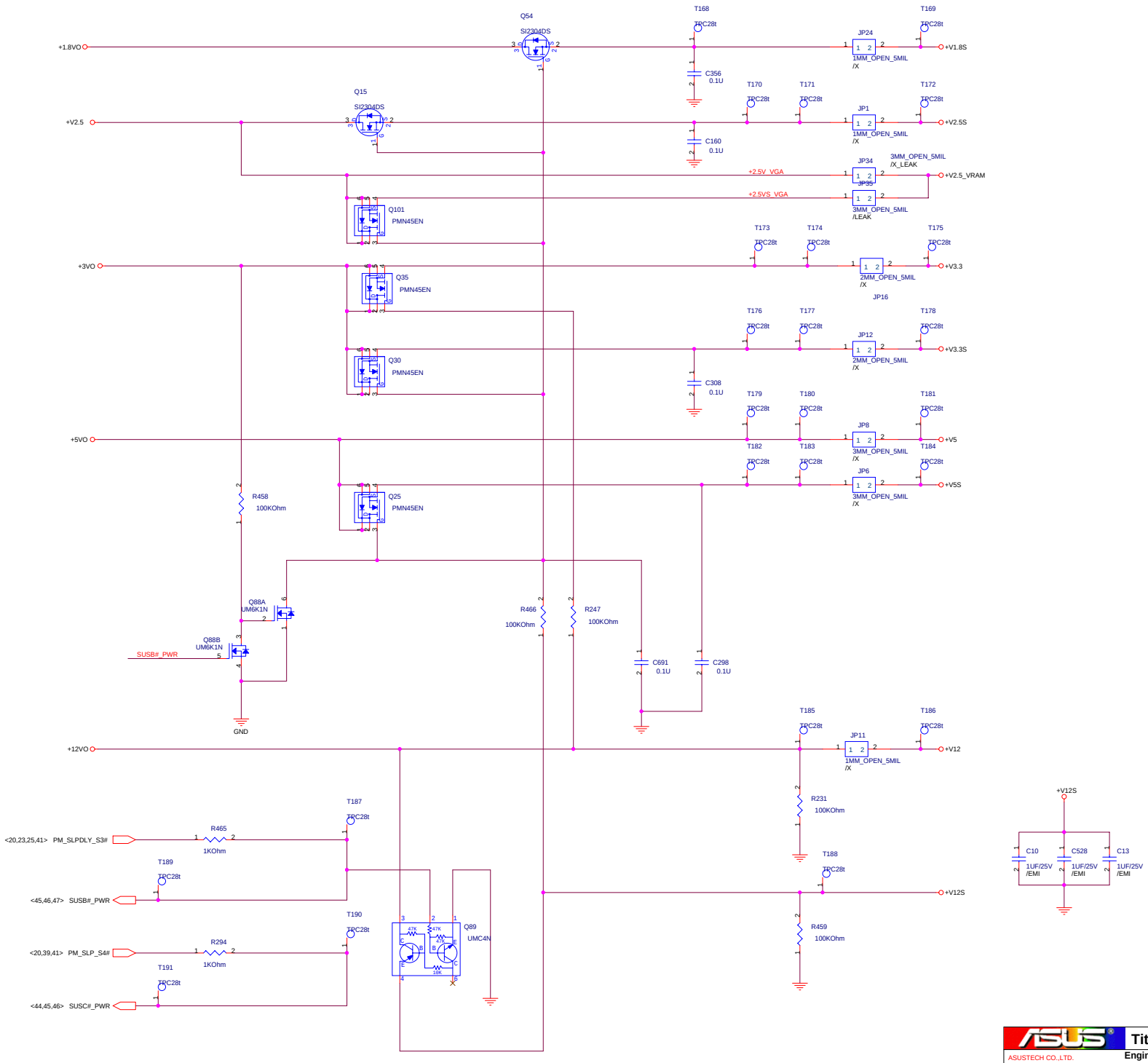
ASUSTEK CO.,LTD.
Title : CHARGER
Engineer: Jully_ma
Size: C
Project Name: A3G
Rev: 1.2
Date: Thursday, August 19, 2004
Sheet 48 of 57



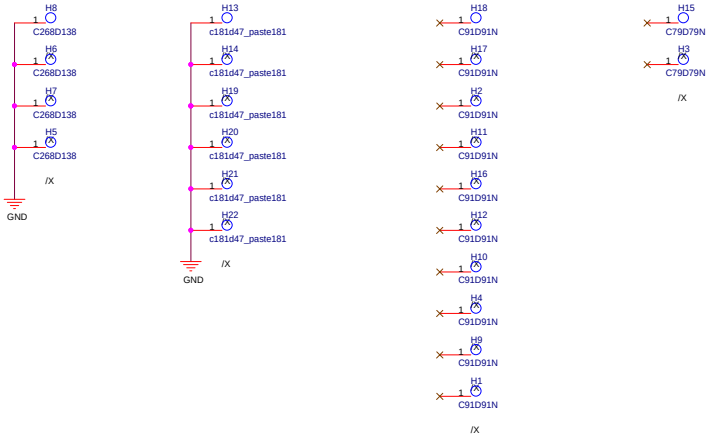
ASUSTECH CO.,LTD.	Title : AC_BAT_SYS	
	Engineer: charlie_xie	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 49 of 57	



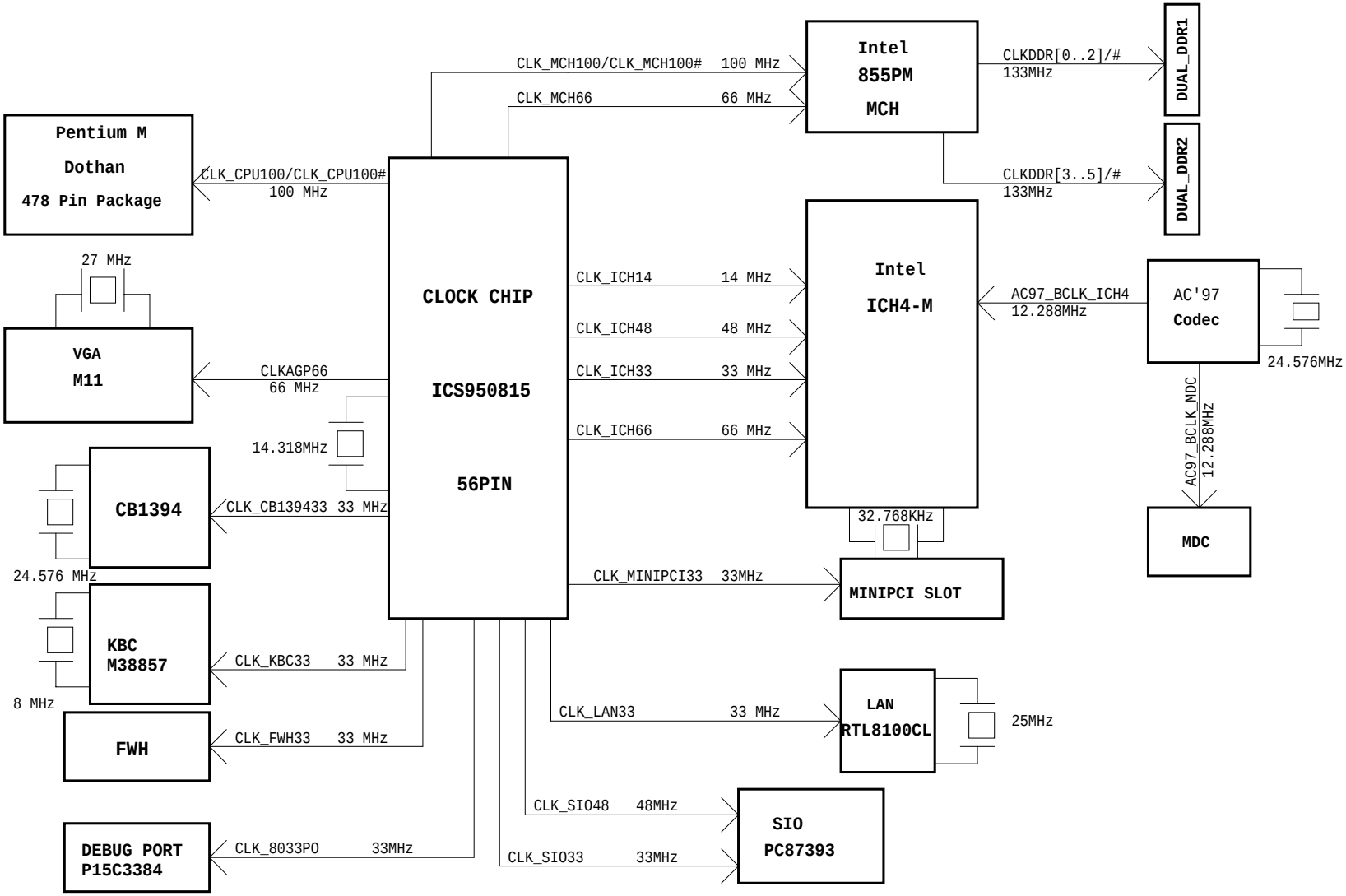
ASUSTECH CO.,LTD.	Title : BATLOW/SD#	
	Engineer: Lassie Bao	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 50 of 57	



ASUSTECH COMPUTER INC.	Title : LOAD SWITCH	
	Engineer: Benny Liang	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 51 of 57	

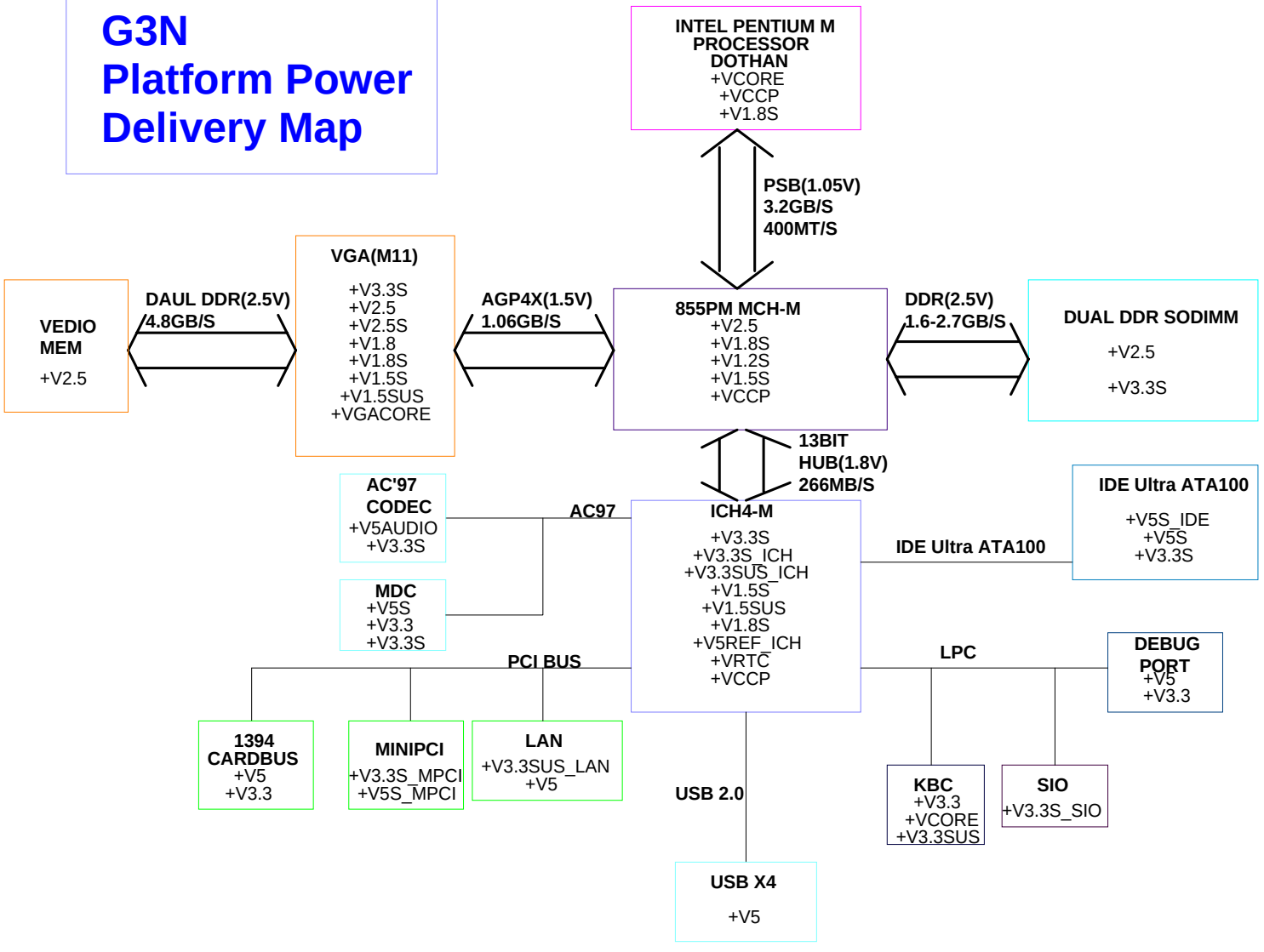


ASUSTECH CO.,LTD.	Title : SCREW_HOLES	
	Engineer: *Pommy Lu*	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 52 of 57	



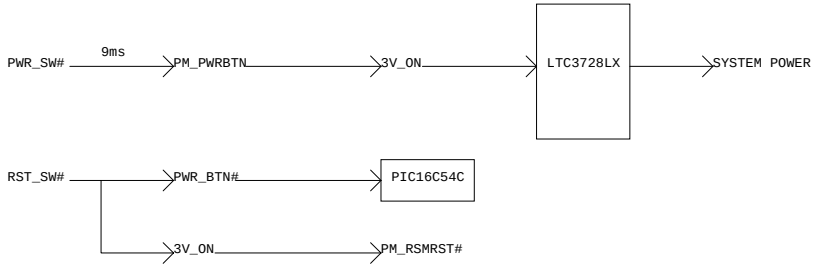
ASUSTECH CO.,LTD.	Title : Clock Map	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 53 of 57	

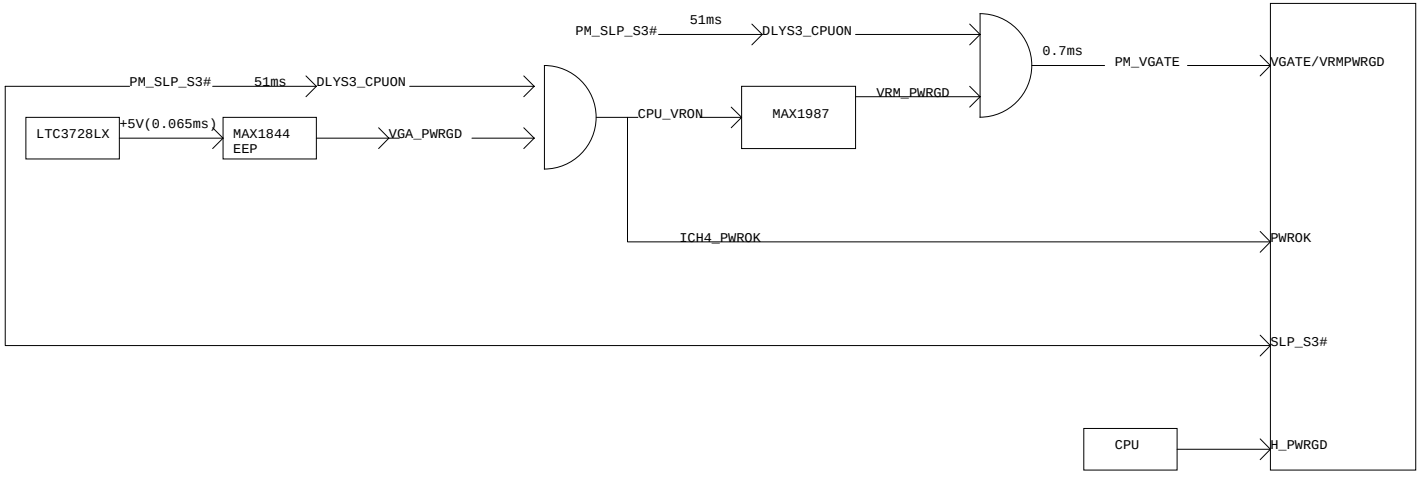
G3N Platform Power Delivery Map



ASUSTECH CO.,LTD.	Title : Power Delivery Map	
	Engineer: EDDY ZHAO	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 54 of 57	

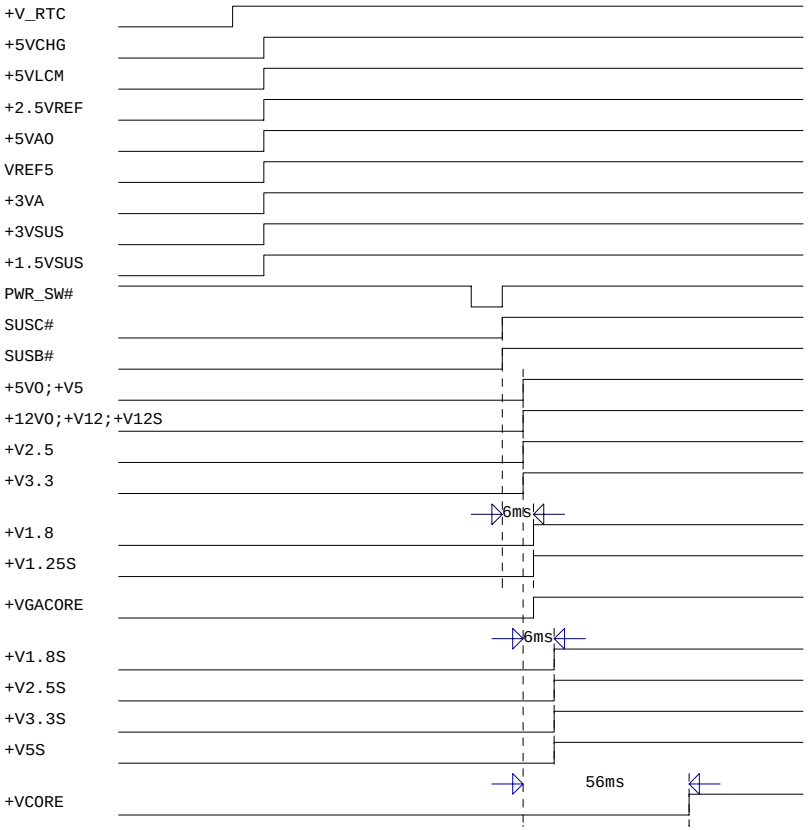
AC Mode:



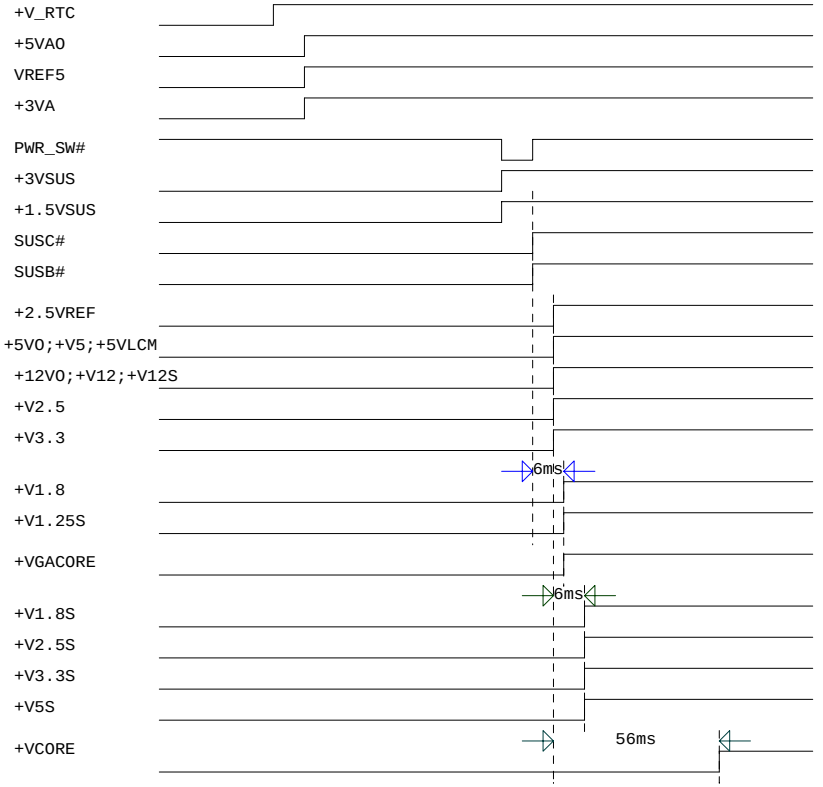


ASUSTECH CO.,LTD.	Title : Power Sequence(1)	
	Engineer: Lassie_Bao	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 55 of 57	

AC MODE



BAT MODE



ASUSTECH	Title : Power Sequence(2)	
	Engineer: DEL_TAN	
Size: C	Project Name: A3G	Rev: 1.2
Date: Thursday, August 19, 2004	Sheet 56 of 57	

REVISION HISTORY

SCHEME REV.	DATE	REVISION DESCRIPTION
0.1	2004/02/04	Preliminary based on A3N/M3N Add M11-P
0.2	2004/02/06	Fix DRC errors P51: Remove +1.5VO to +V1.5S switch P46: one of +V3.3A source is Optional, need be Identifed Add Power Jumpers
0.3	2004/02/10	Add 54_Clock Map and 55_Platform Power Delivery Map (Created by Eddy) Fix Power Sequence error Change some Circuit to optional Update parts status and part type
0.4	2004/03/18	Add audio codec to 6 channel output Add VGA compatible with M9+X Add comment on Comp. placement Remove TV-OUT function Merge USB CON of WLAN and Camera with Planel Power CON Remove series termination resistors of DQ and MA between VRAM and GPU Change part package Add WLAN RF en/disable Add Battery Selection Modify Audio Amplifier Circuit Modify Audio DJ & Function Key Add System Power Sequence Add Screw Holes
1.0	2004/04/12	Add two local Hublink Ref. Voltage cirtcuit Rename the parts reference Release for Sample Run

ASUSTECH CO.,LTD.

Title : Revision History

Engineer: Pommy Lu

Size	Project Name	Rev
C	A3G	1.2

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