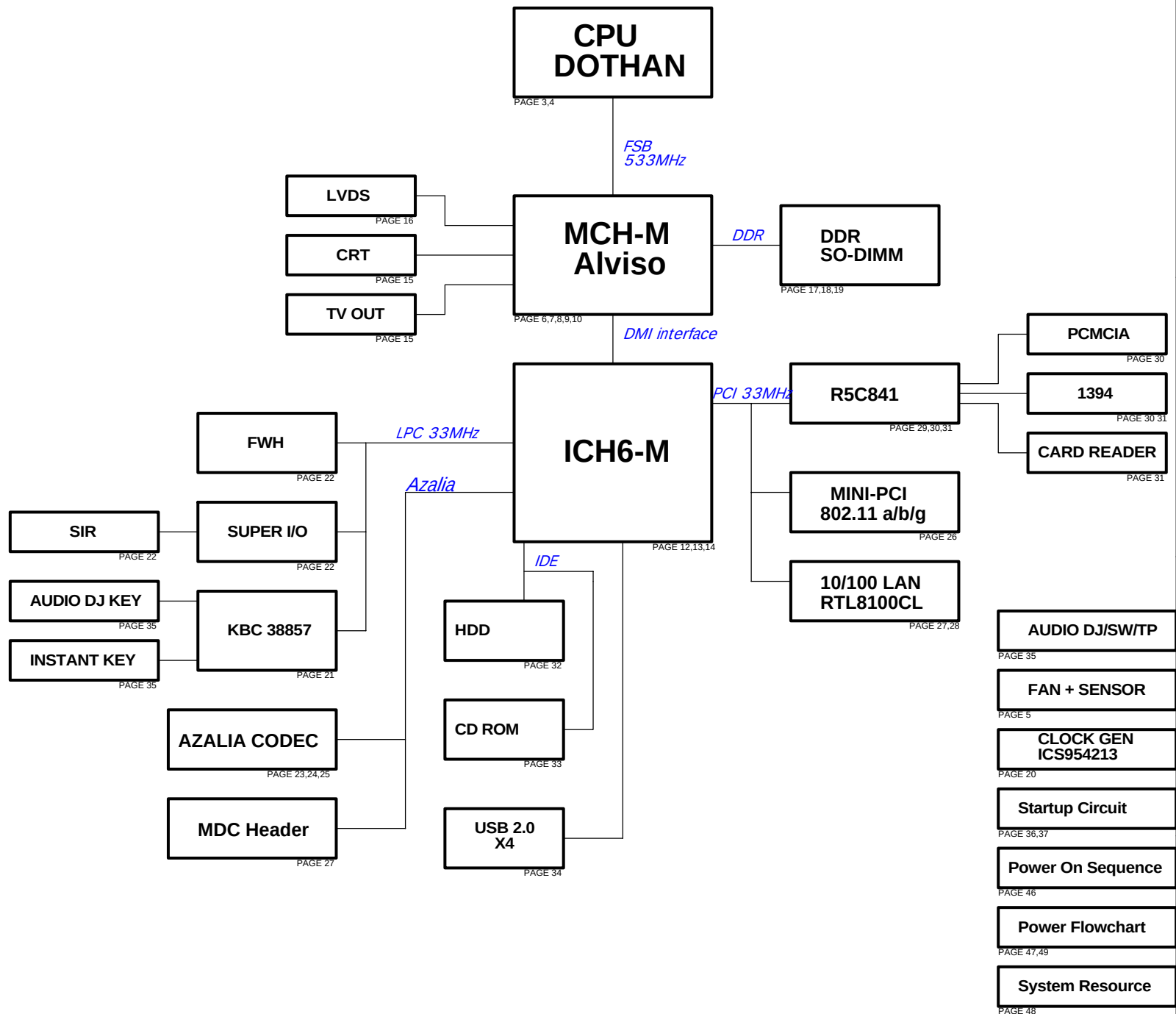


A3A CONTEXT

01_BLOCK DIAGRAM
02_REVISION LIST
03_DOYHAN CPU(1)
04_DOTHAN CPU(2)
05_THERMAL SENSOR,FAN
06_ALVISO GMCH(1)
07_ALVISO PCIE(2)
08_ALVISO DDR SLOT(3)
09_ALVISO POWER(4)
10_ALVISO GND(5)
11_GMCH STRAPPING/LVDS TRANS
12_ICH6M_SATA,LPC,IDE(1)
13_ICH6M_USB,PCI/E,PMIO(2)
14_ICH6M_PWR,GND(3)
15_CRT&TV OUT CONN
16_LVDS&INVERTER(CAMERA,WLAN)
17_DDR_SODIMM
18_DDR_DATA TERMINATION
19_DDR_ADDRESS TERMINATION
20_CLOCK GEN ICS954213
21_KBC M38857
22_FWH,SIO,SIR
23_AZALIA ALC880
24_AMPLIFIER 2 CHANNEL
25_MIC,LINE-IN JACK
26_MINI-PCI
27_LAN RTL8100CL
28_RJ11/45,MDC,PRN
29_PCI CARDBUS R5C841
30_PCI PCMCIA SOCKET A
31_PCI IEEE1394A,3IN1 CON
32_HDD CONNECTOR
33_Q/SW,CD-ROM CONNECTOR
34_USB CONNECTOR
35_DJ BOARD/SW/TP
36_STARTUP CIRCUIT(1)
37_STARTUP CIRCUIT(2)
38_VCORE
39_SYSTEM(3V,5V)
40_2.5V,1.5V,1.8V,1.05V
41_VCCA,DDR(1.25VS)
42_PIC/BAT CONN/PWOK/THERM PT
43_CHARGE
44_BATLOW/SD#
45_LOAD SWITCH
46_POWER ON SEQUENCE
47_POWER FLOW CHART
48_SYSTEM RESOURCE
49_HISTORY



REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSPLVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
+1.5VSUS	1.5V	270 mA
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH
TOP/BOT 18 mils

37.5 OHM WIDTH
TOP/BOT 11 mils
IN1/IN2 9.5 mils

50 OHM WIDTH
TOP/BOT 6 mils
IN1/IN2 5 mils

55 OHM WIDTH
TOP/BOT 5.5 mils
IN1/IN2 4.5 mils

75 OHM WIDTH
TOP/BOT 4 mils
IN1/IN3 3.5 mils

Differential

85 OHM WIDTH/SPACE
TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils

90 OHM WIDTH/SPACE
TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils

100 OHM WIDTH/SPACE
TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils

110 OHM WIDTH/SPACE
TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI PCI_REQ#3
10/100 PCI_REQ#2
CB&1394 PCI_REQ#1

IDSEL

MINIPCI PCI_AD19
10/100 PCI_AD16
CB&1394 PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

PAGE 38

SIGNAL	IN:	VR_VID[0...5] PM_DPRSPLVR STP_CPU# PM_PSI# CPU_VRON MCH_OK
	OUT:	DELAY_VR_PWRGD CLK_PWR_GD#
POWER	IN:	AC_BAT_SYS +5V0 +3V0
	OUT:	+VCORE

PAGE 39

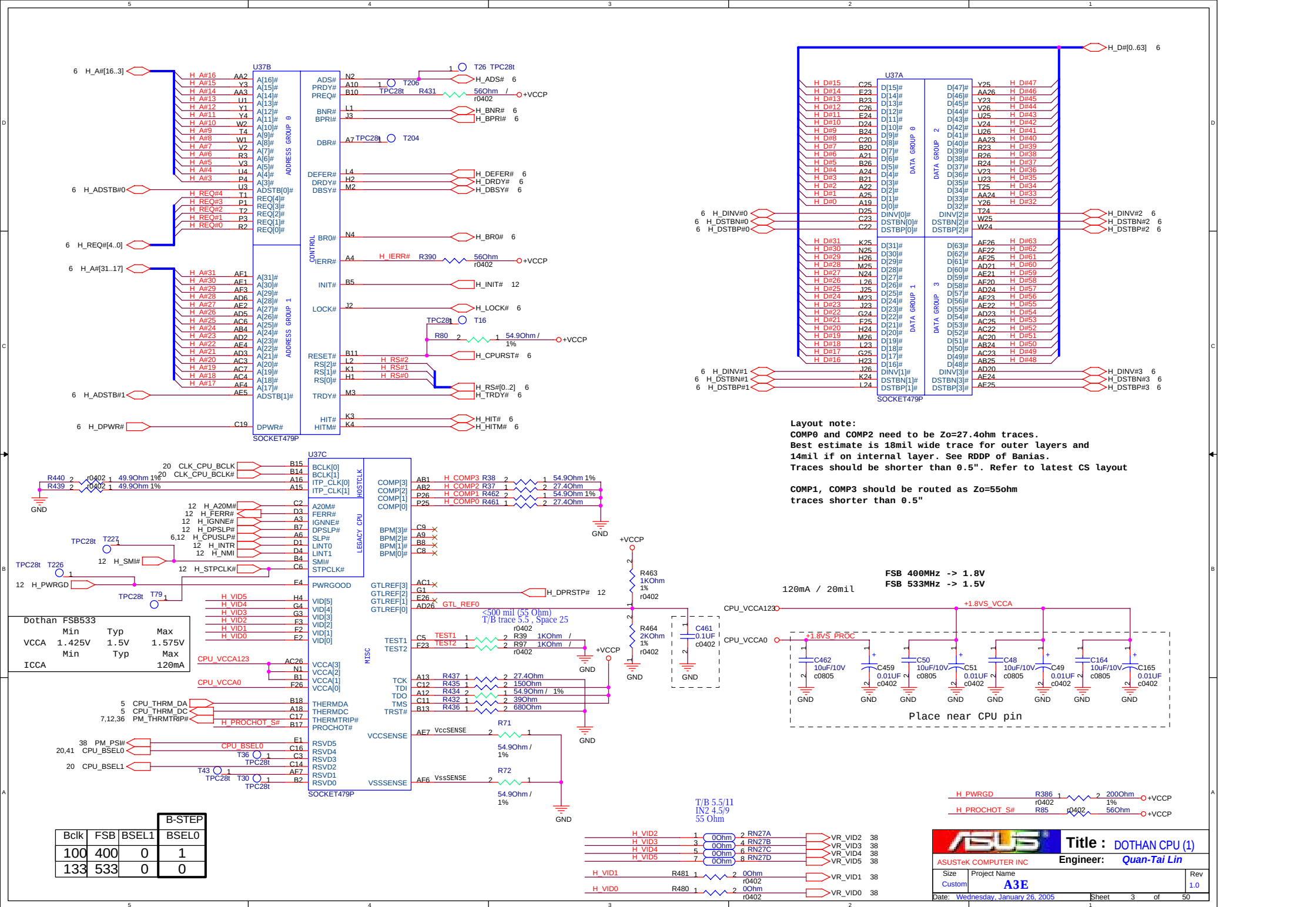
SIGNAL	IN:	SUSC#_PWR VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12V0 +3V0 +5V0

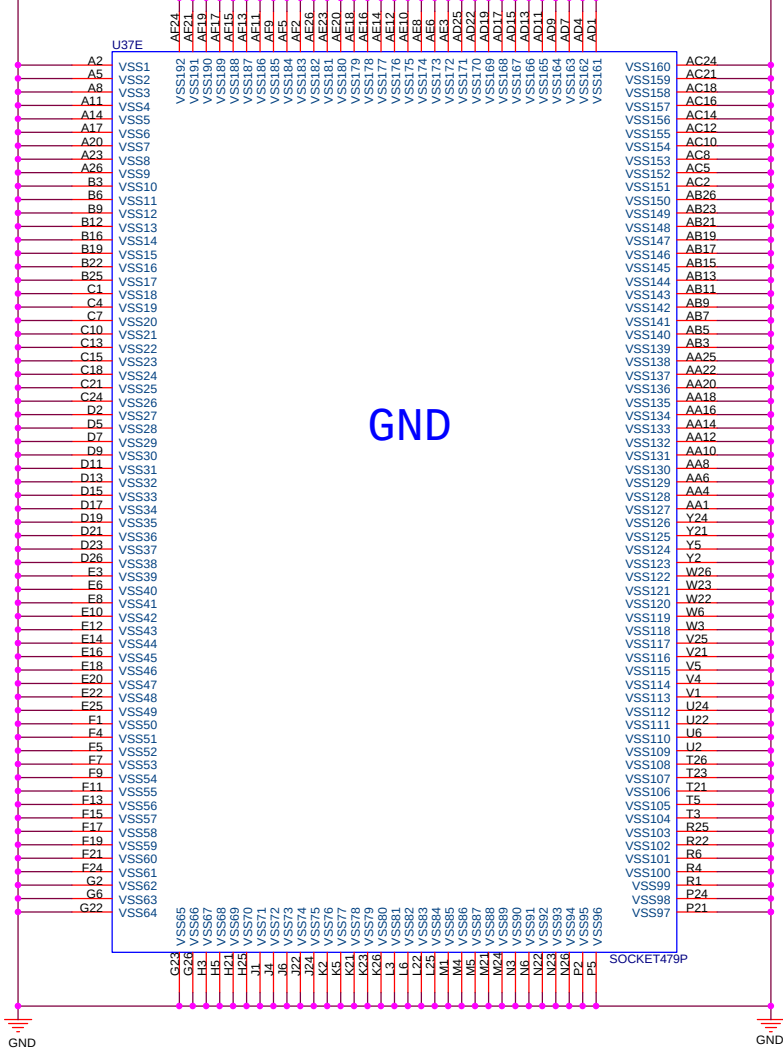
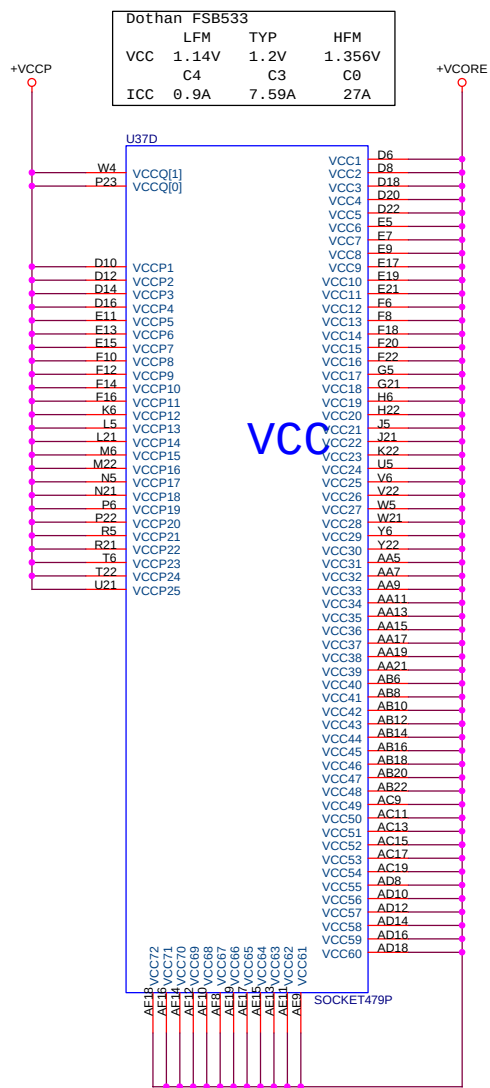
PAGE 40

SIGNAL	IN:	SUSB#_PWR SUSC#_PWR CPU_VRON
POWER	IN:	AC_BAT_SYS +5V0
	OUT:	+1.8V +1.5VS +2.5VS +VCC_GMCH_CORE +5VALWAYS +3VALWAYS +VCCP

PAGE 41

SIGNAL	IN:	SUSB#_PWR
POWER	IN:	+3V +1.8V
	OUT:	+0.9VS





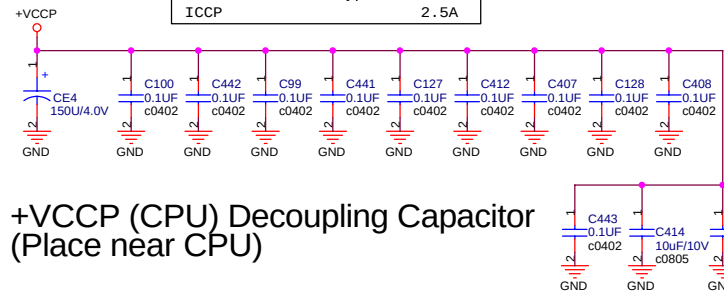
MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533

Min	Typ	Max
VCCP 0.997V	1.05V	1.102V
ICC		2.5A



When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

**P/N change to
06-010112010
for cost down**

CPU FAN will be forced on:

- 1) Thermal Sensor Over-temperature
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage south bridge. Add a MOS to transfer it to +3V level.

Route H_THERMDA and H_THERMDC on the same layer

```

=====OTHER SIGNALS
 12 mils
=====GND
 10 mils
=====H_THERMDA(10 mils)
 10 mils
=====H_THERMDC(10 mils)
 10 mils
=====GND
 12 mils
=====OTHER SIGNALS

```

Avoid BPSB,Power

CPU VCORE Decoupling Capacitor

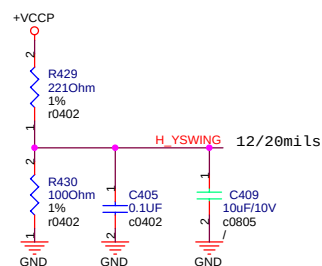
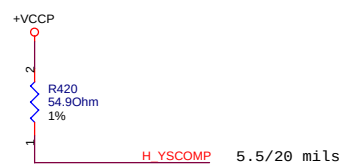
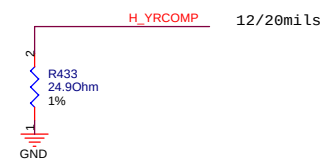
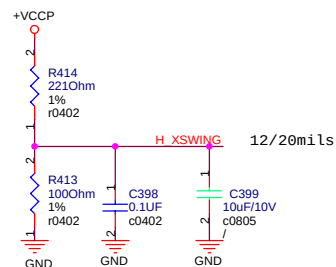
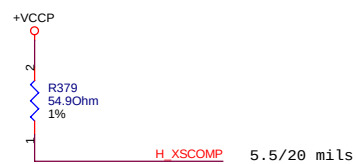
Mid Frequency
Decoupling (Place
around
Processor)

High Frequency
Decoupling (Place
underneath
Processor) using
10uF/6.3V X5R

+V CORE
Bulk
Decoupling

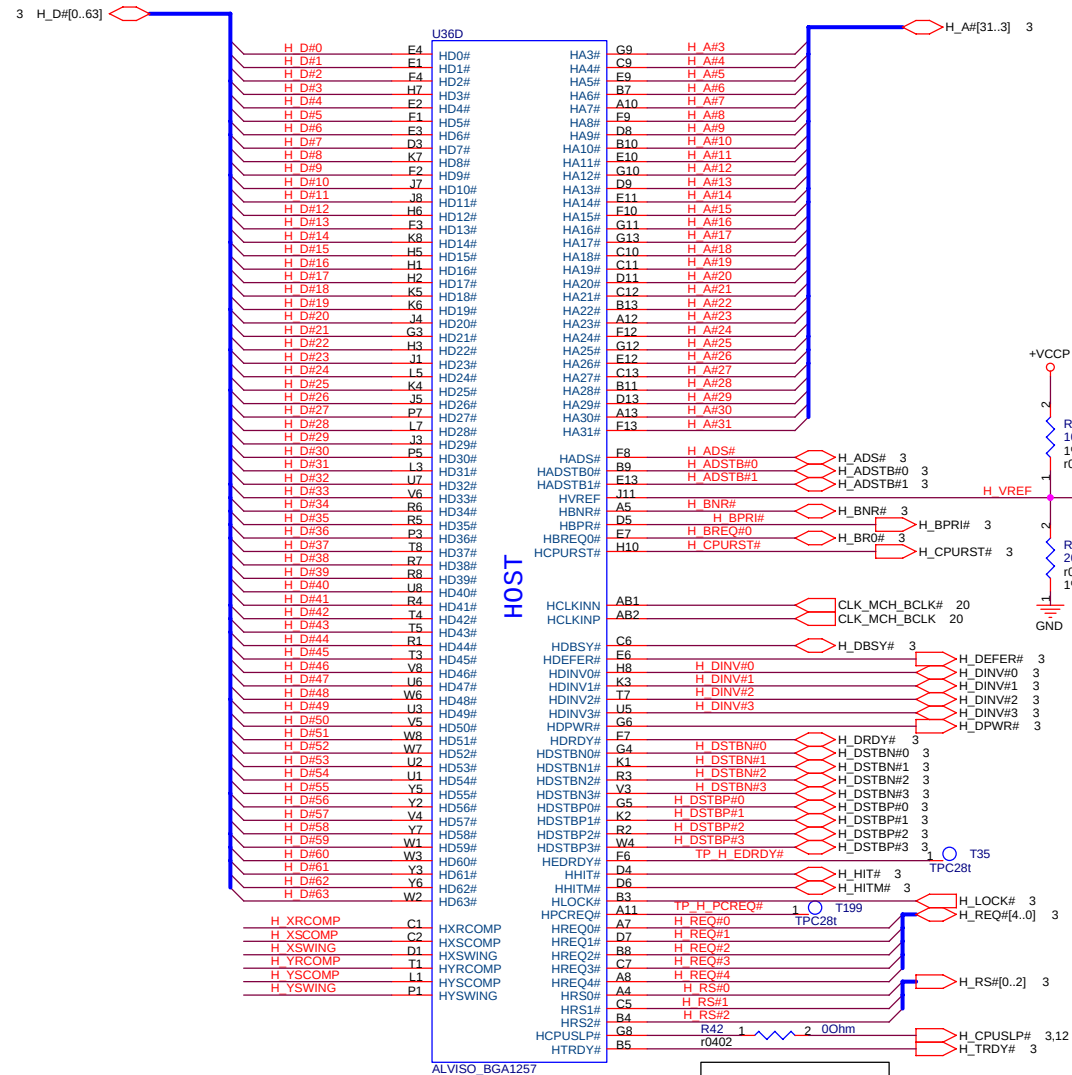
Four 200 uF are located in IMVP4

Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



In OrCAD circuit,ALVISO PM P/N :02-010002600

But we have to use ALVISO GM P/N : 02-010002610 in BOM list



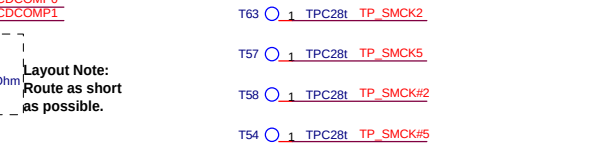
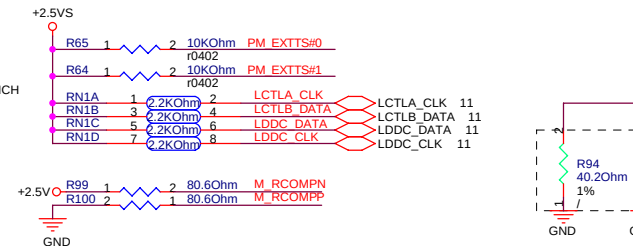
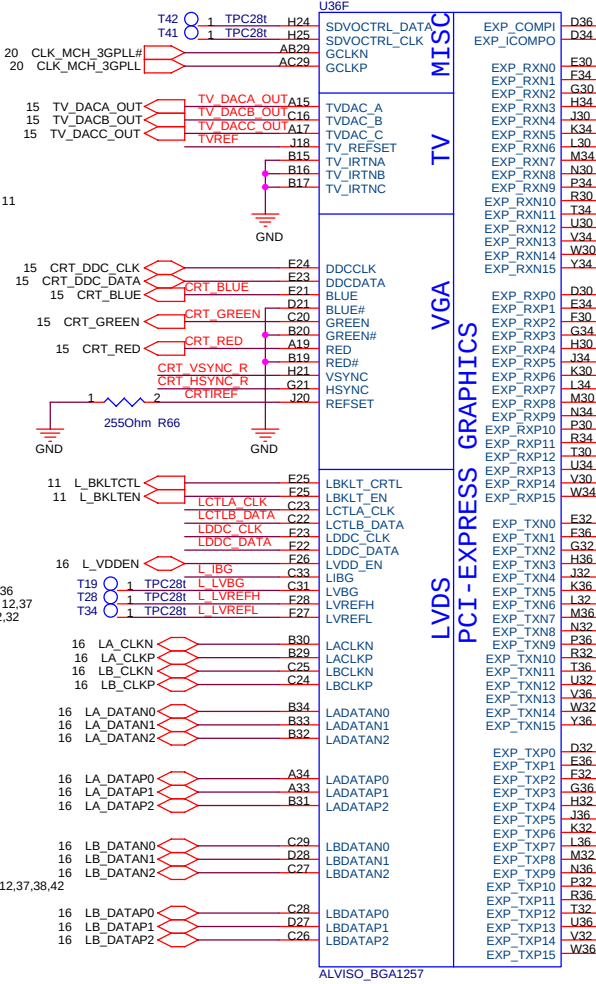
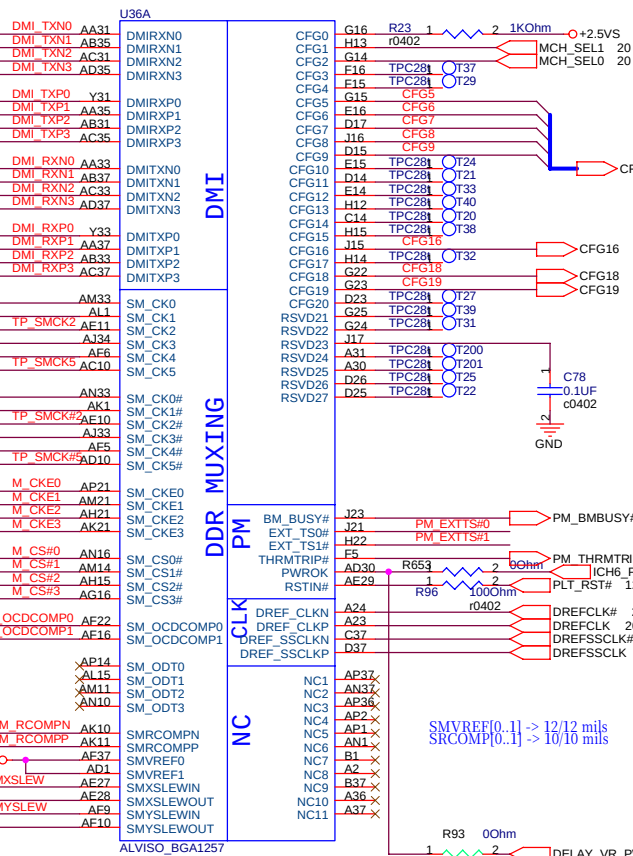
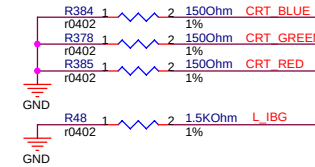
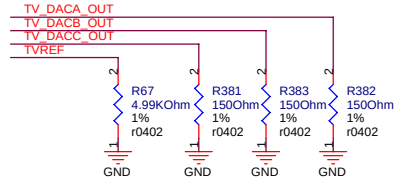
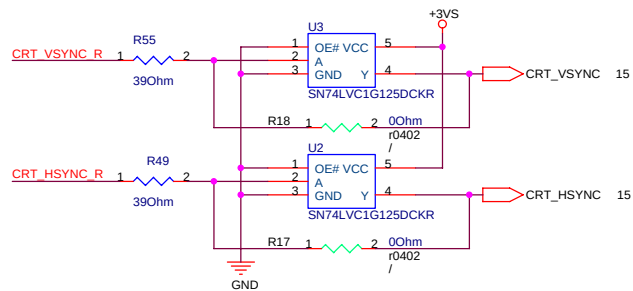
HOST

ALVISO_BGA1257

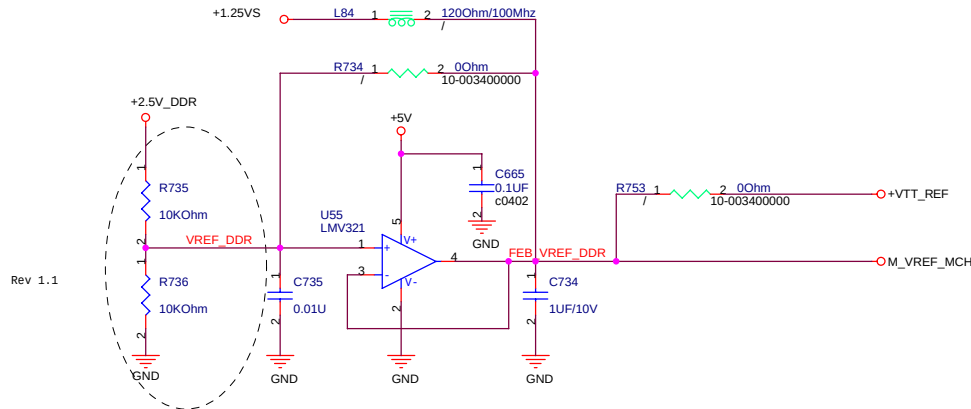
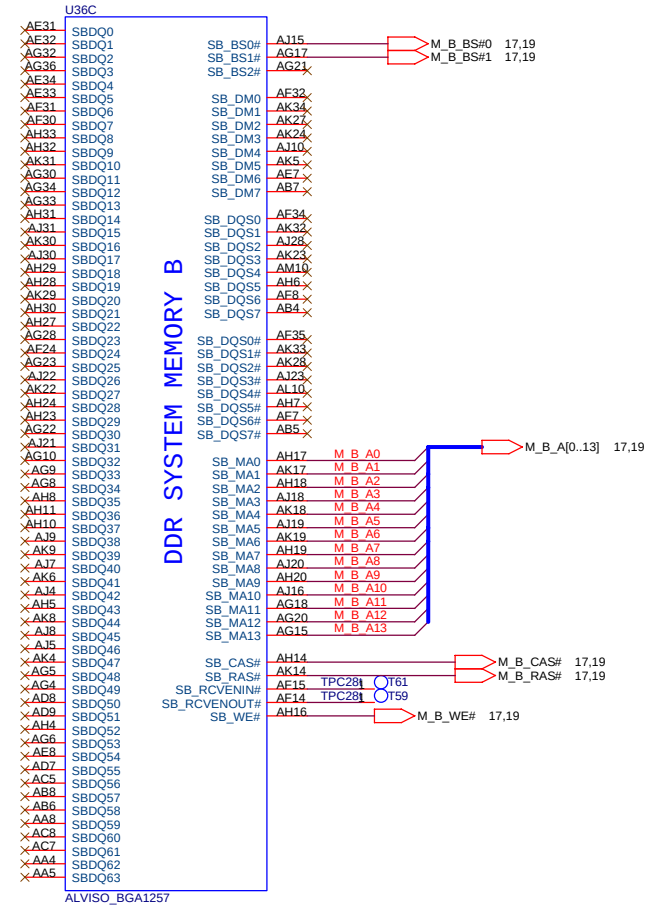
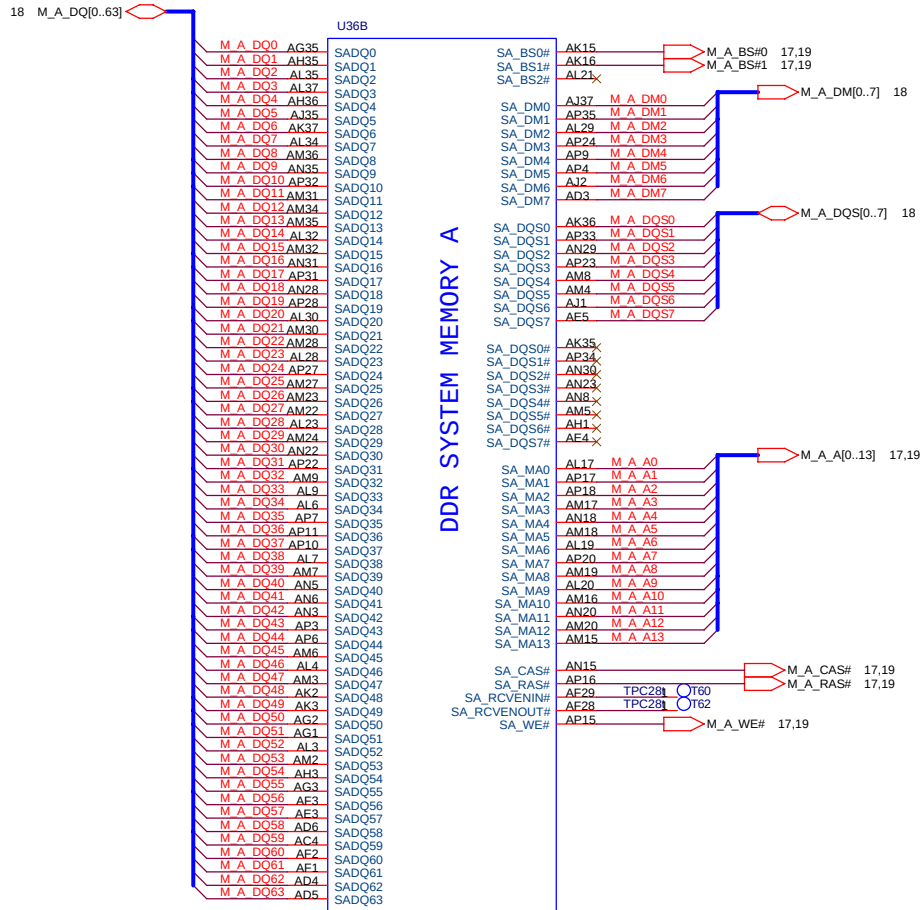
Dothan A : R282
NO STUFF

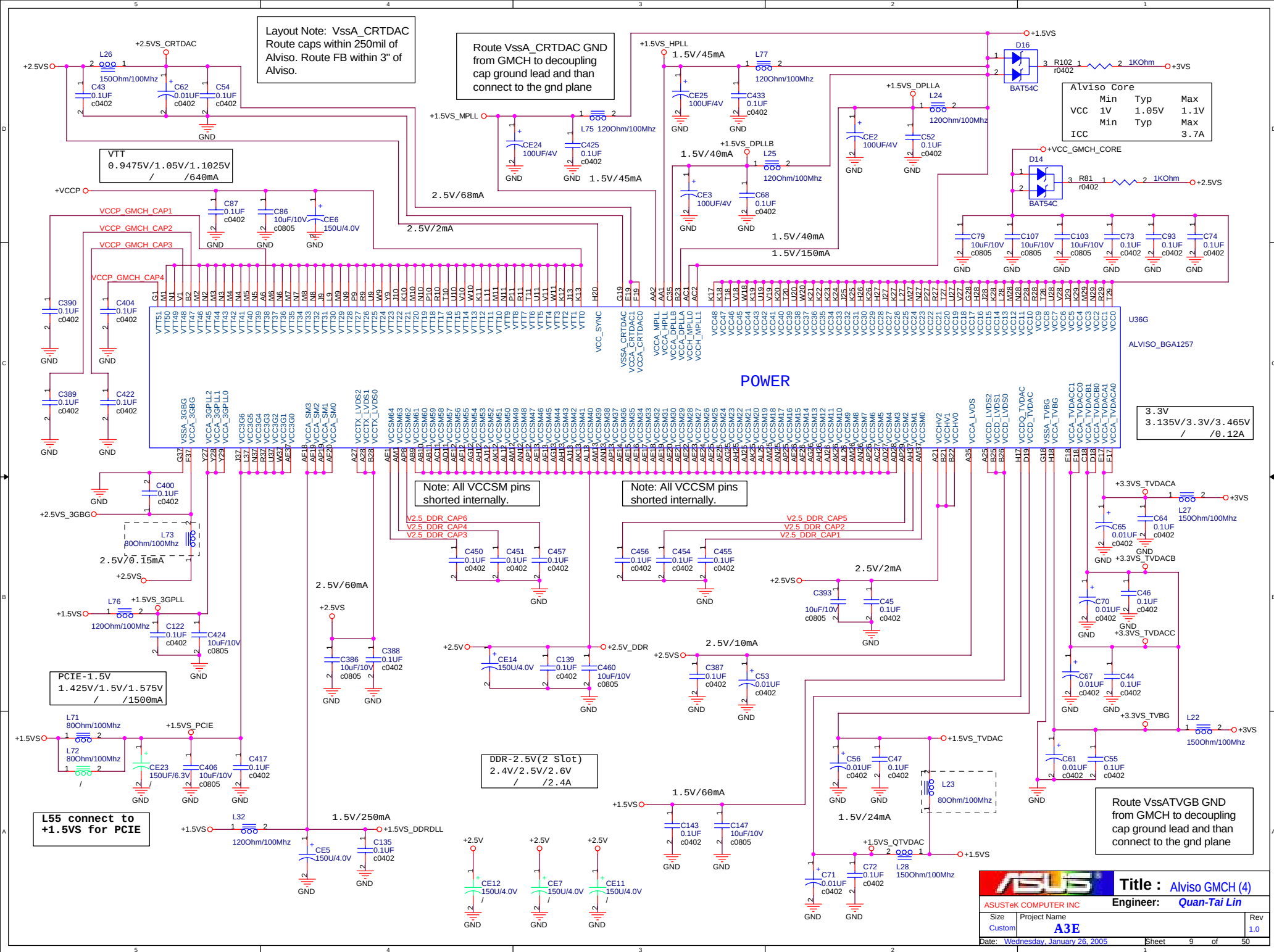


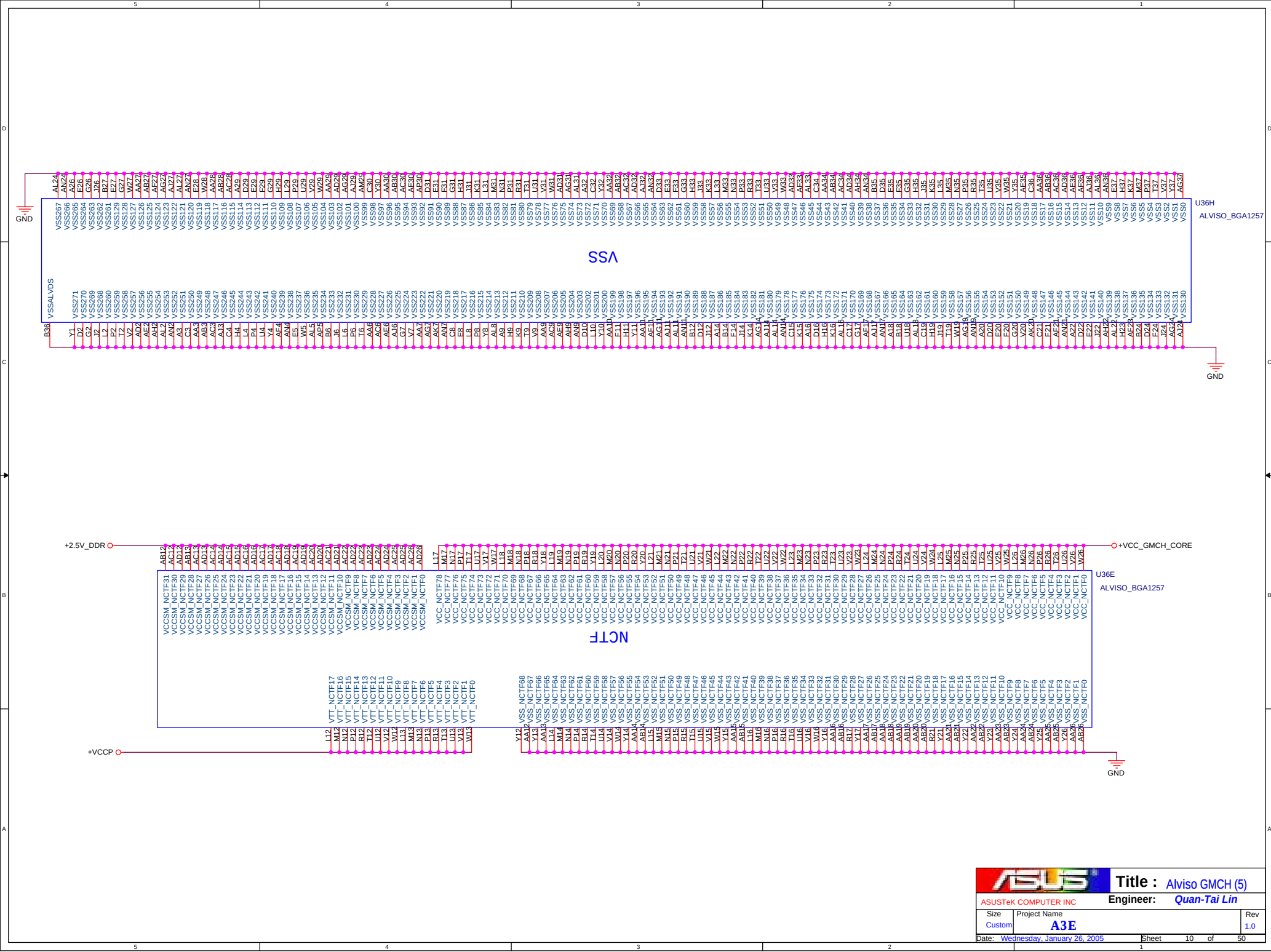
Near Alviso 0.5" → ← Near CRT Bead 0.5"



Layout Note:
Route as short
as possible.

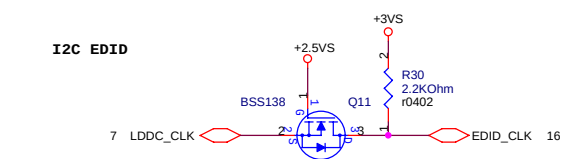
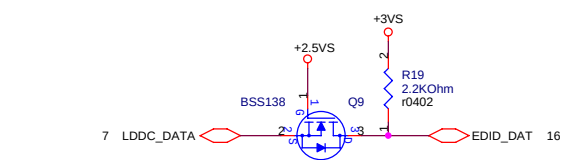
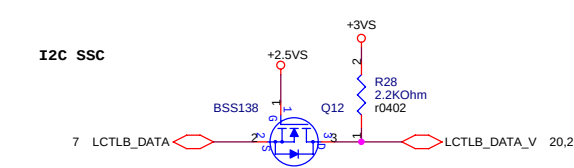
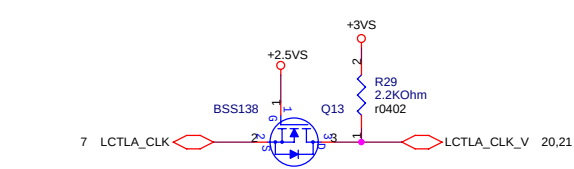
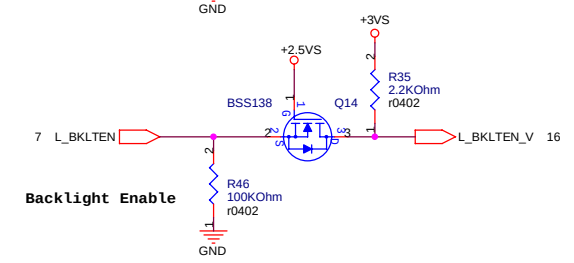
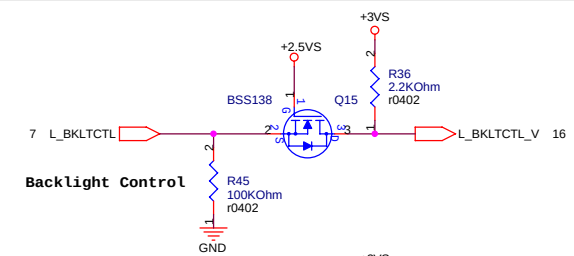
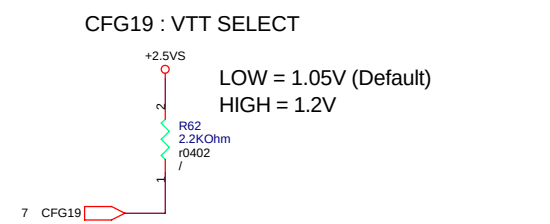
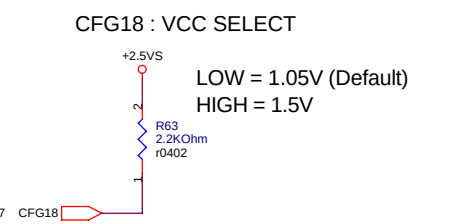
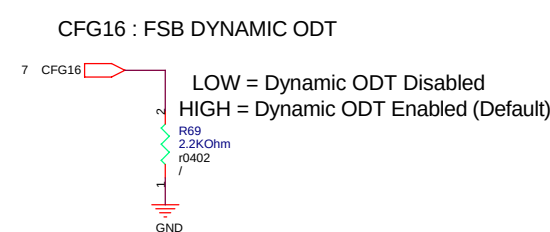
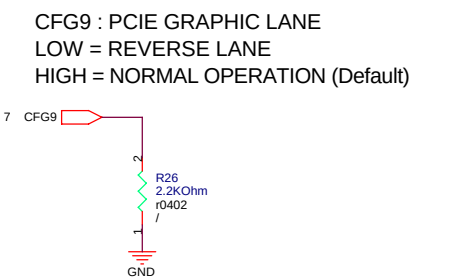
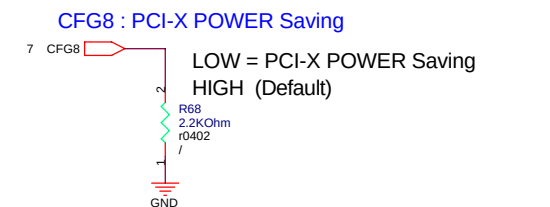
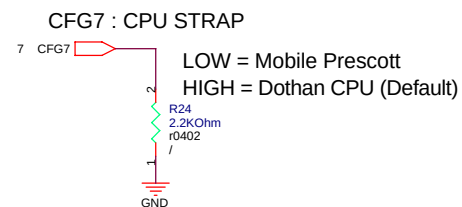
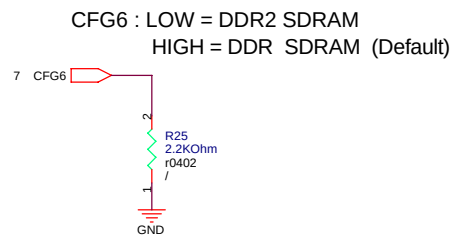
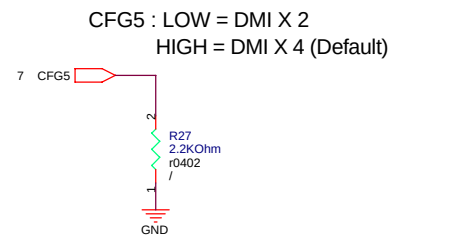


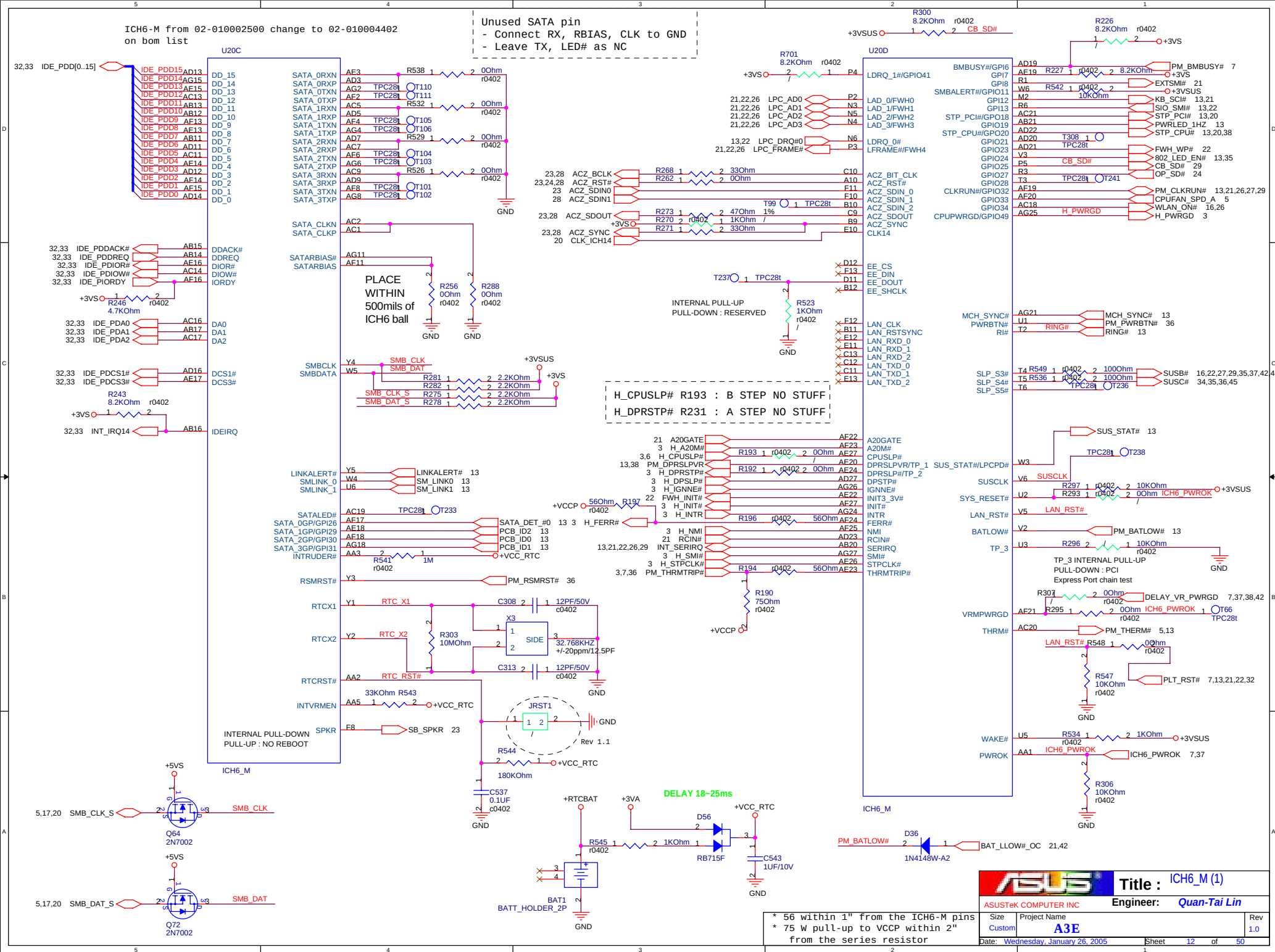


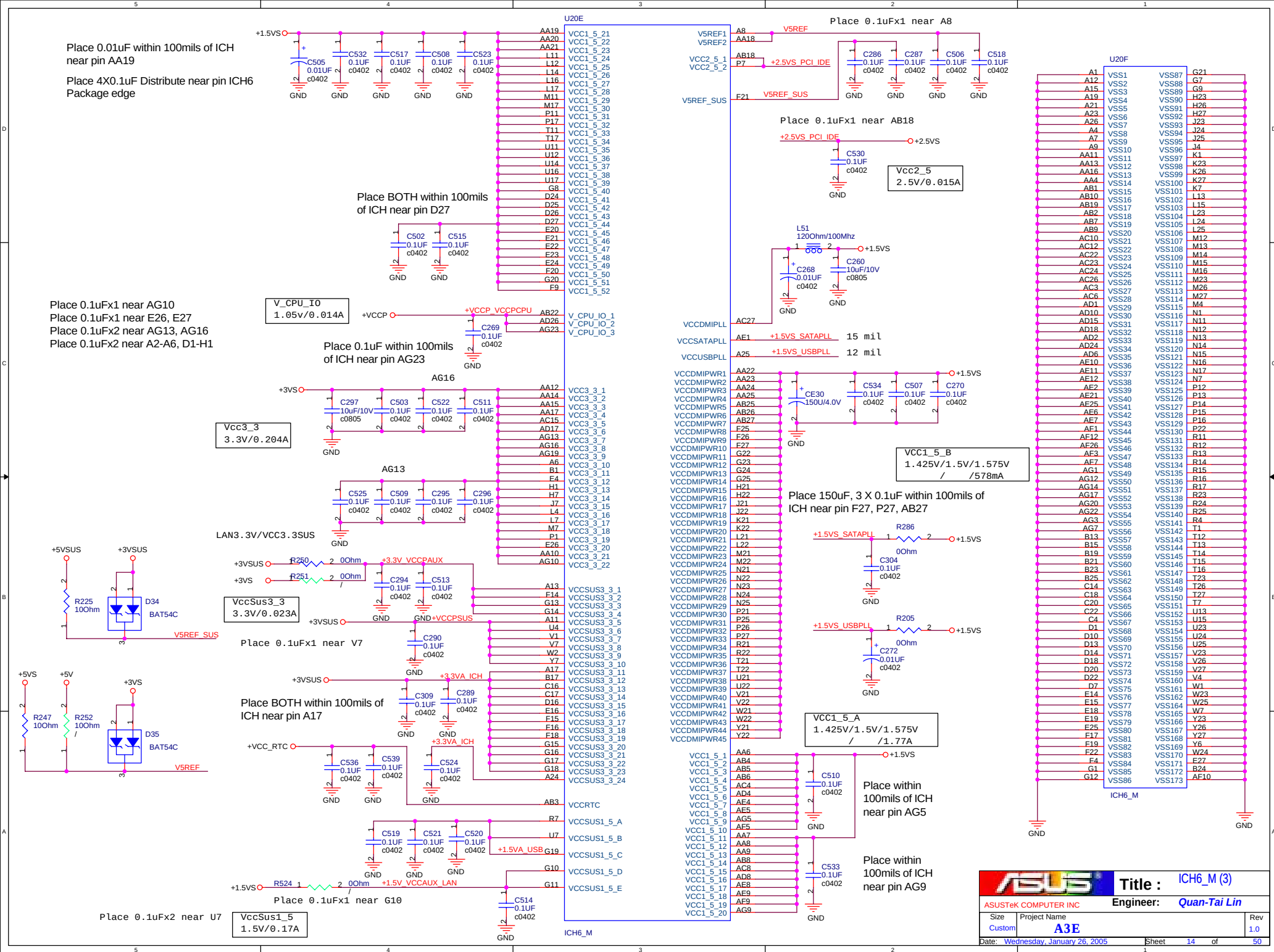


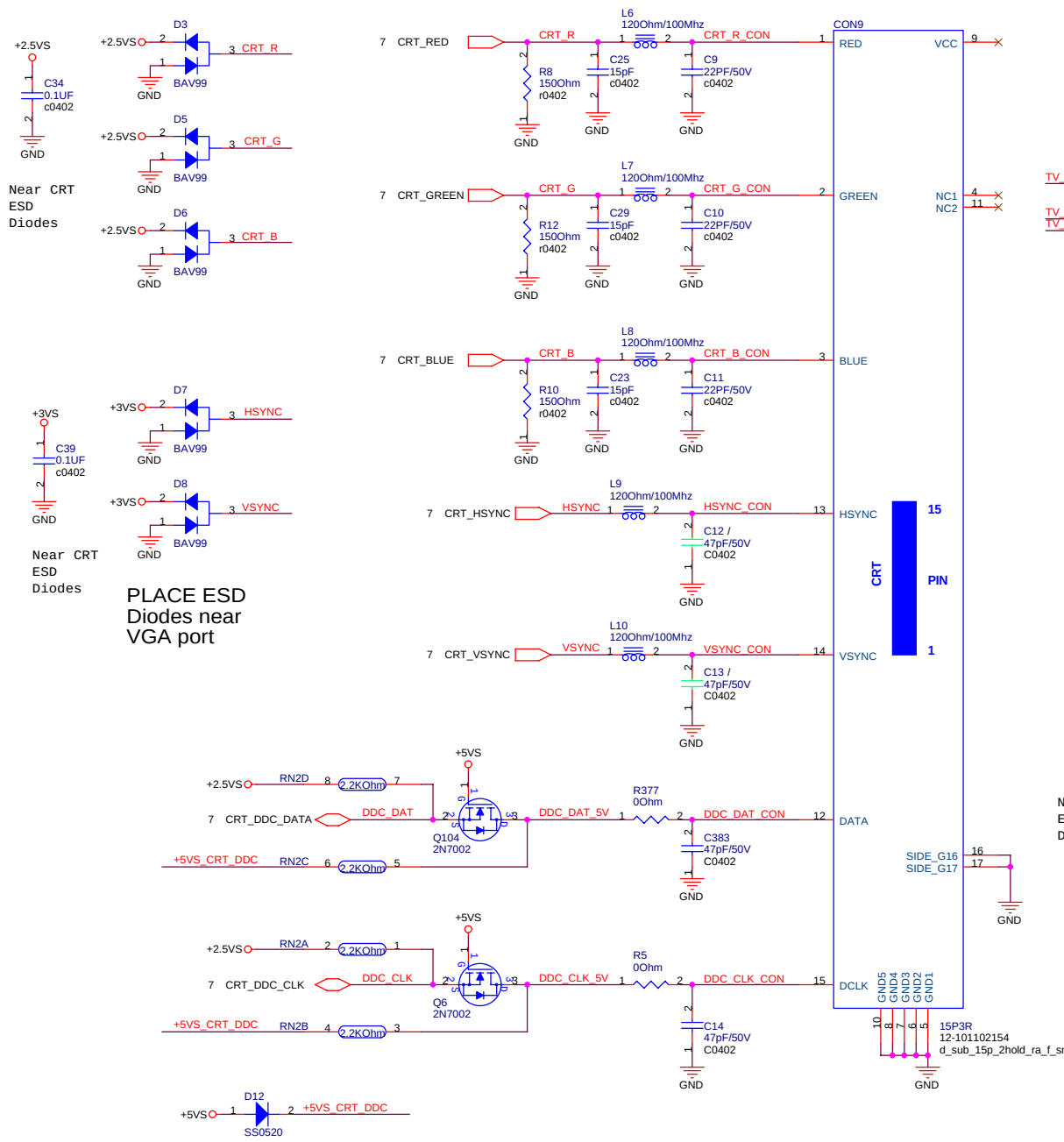
CFG[2:0] are HVC MOS (+2.5VS)
 CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
 CFG[19..18] have internal pulldown resistors./HVC MOS(+2.5VS)/
 SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
 LOW = No SDVO device present (Default)

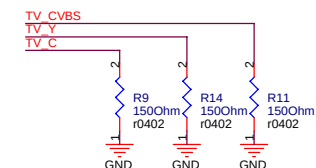
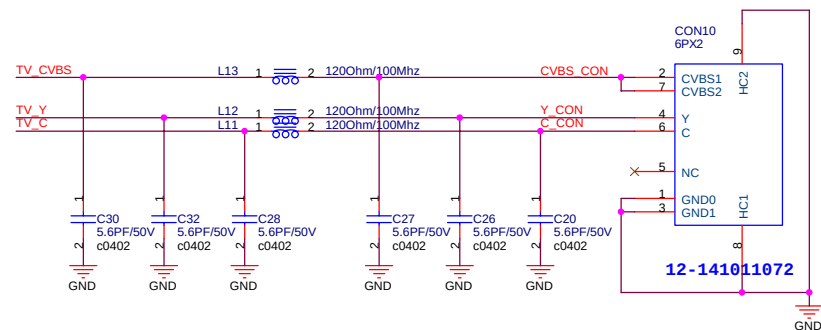






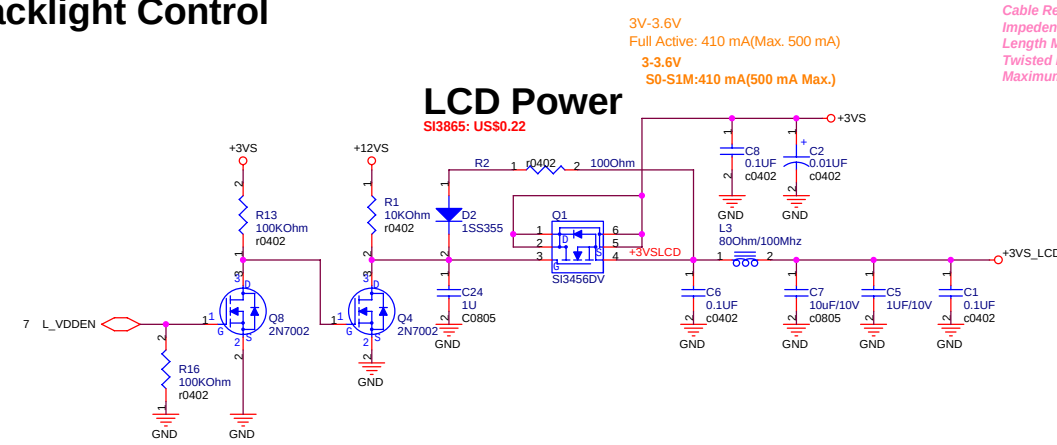


Note: CRT_Red, CRT Green, CRT Blue are ground reference.



PLACE ESD Diodes near TV port

LCD Backlight Control



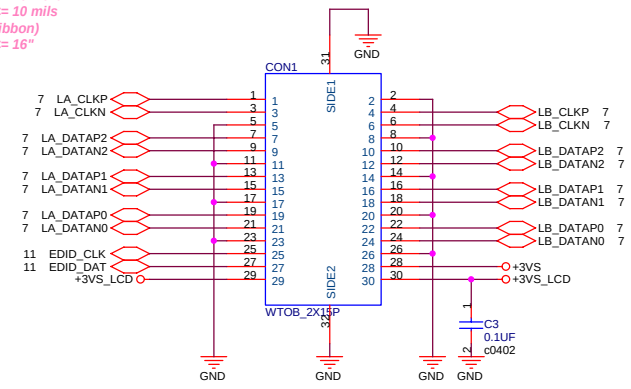
LCD Power

SI3865: US\$0.22

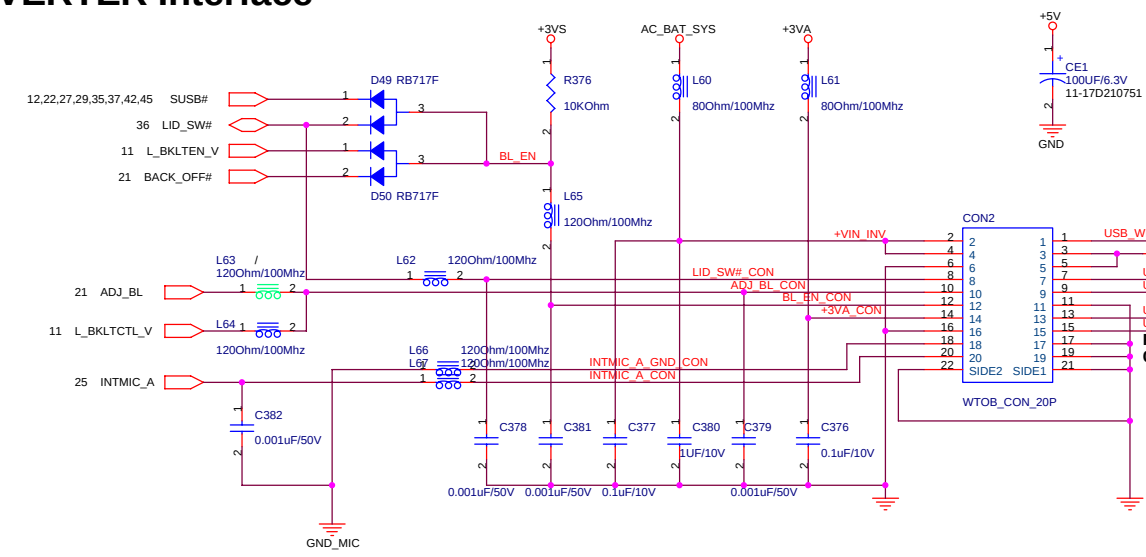
3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

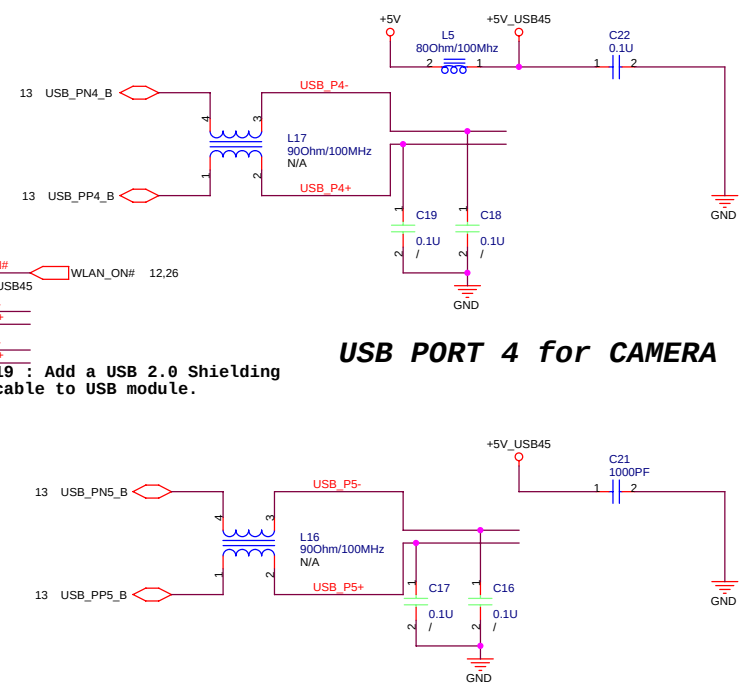


INVERTER Interface



BIOS
ADJ_BL: KBC
output D/A
signal (adjust
voltage level)
to adjust Back
light.

BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.



USB PORT 4 for CAMERA

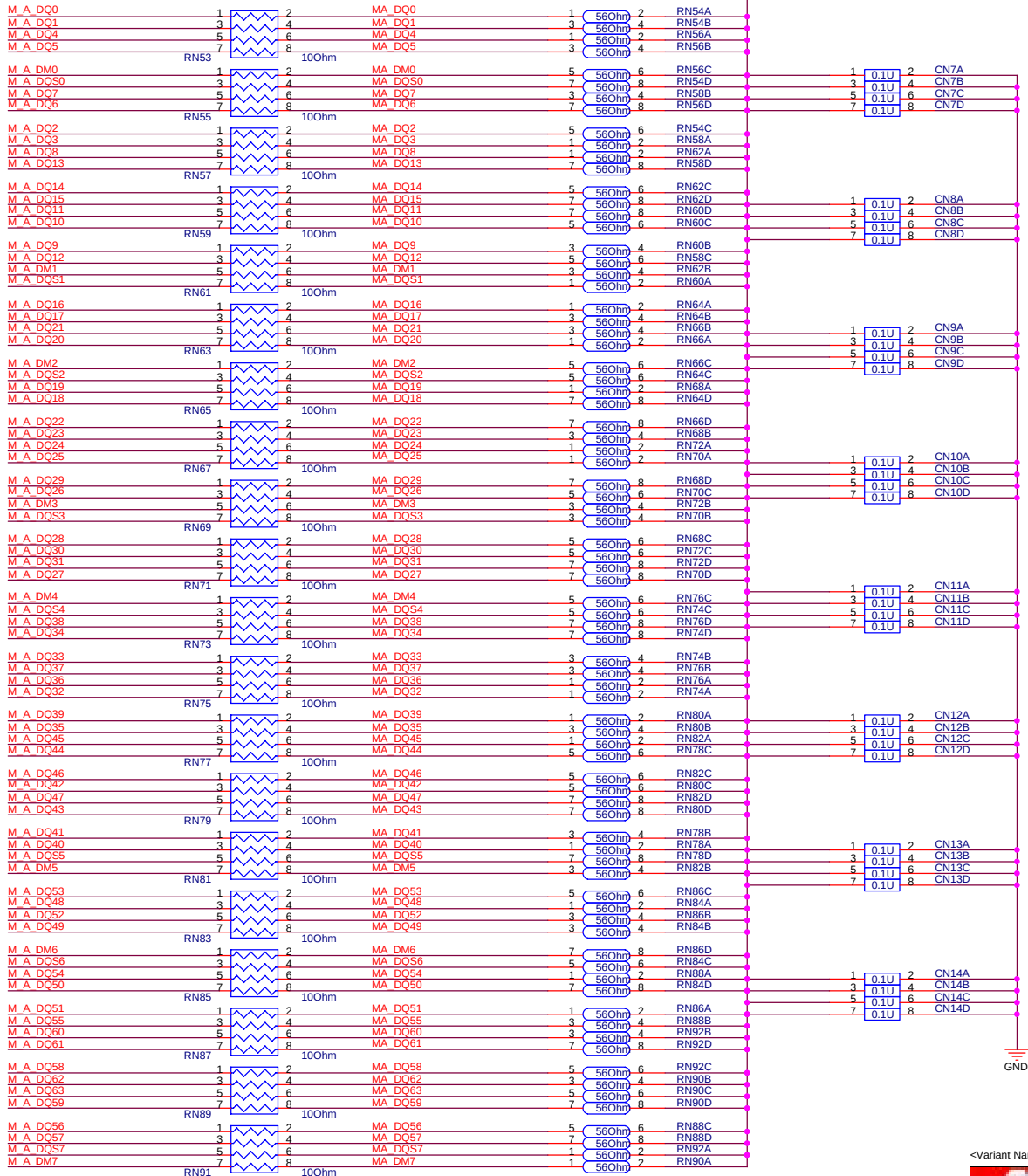
USB PORT 5 for WLAN

700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

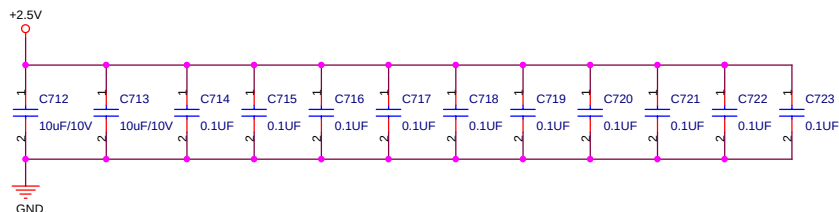
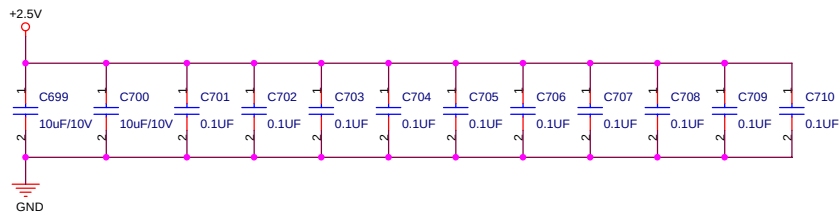
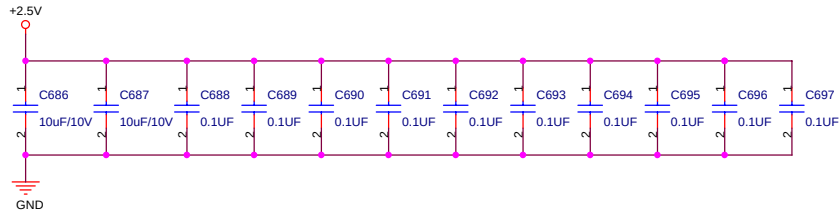
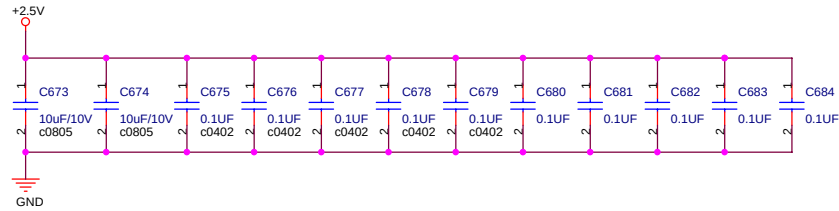
ASUS		Title : LVDS & INVERTER	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	1.0	
Date: Wednesday, January 26, 2005	Sheet	16	of 50

M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DM[0..7] 8

MA_DQ[0..63] 17
MA_DQS[0..7] 17
MA_DM[0..7] 17



<Variant Name>



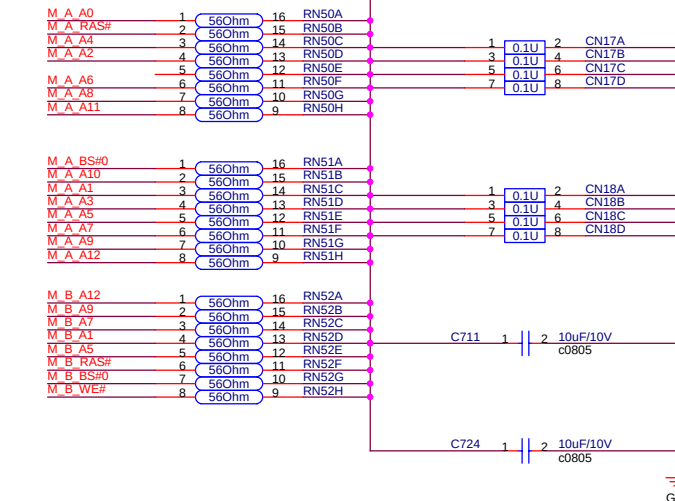
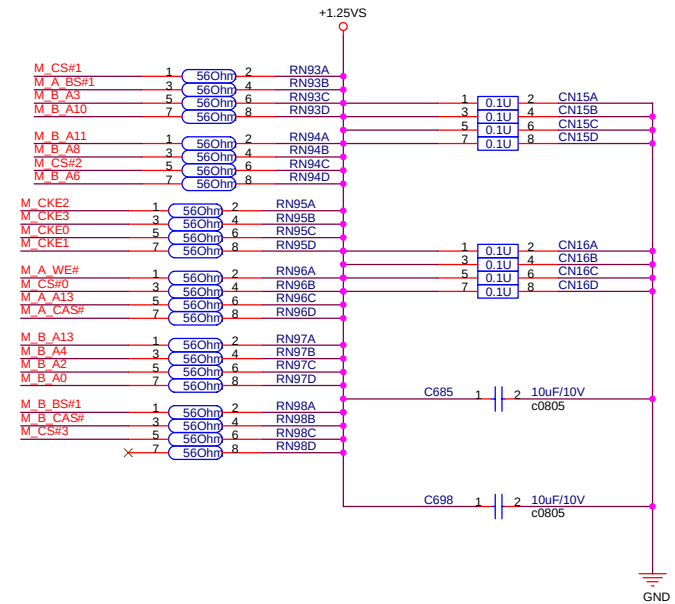
M_A_A[0..13] 8,17
M_B_A[0..13] 8,17
M_CKE[0..3] 7,17
M_CS#[0..3] 7,17

M_B_RAS# M_B_RAS# 8,17
M_B_CAS# M_B_CAS# 8,17
M_B_WE# M_B_WE# 8,17

M_A_RAS# M_A_RAS# 8,17
M_A_CAS# M_A_CAS# 8,17
M_A_WE# M_A_WE# 8,17

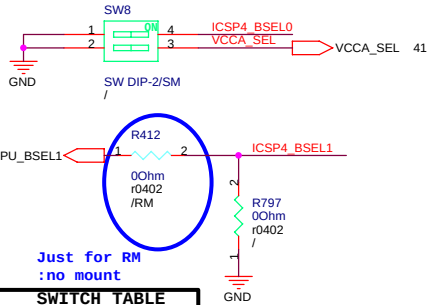
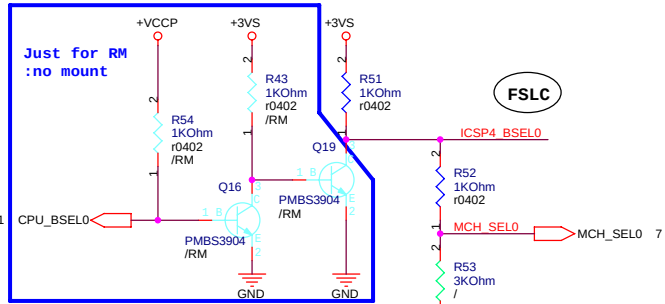
M_A_BS#0 M_A_BS#0 8,17
M_A_BS#1 M_A_BS#1 8,17

M_B_BS#0 M_B_BS#0 8,17
M_B_BS#1 M_B_BS#1 8,17

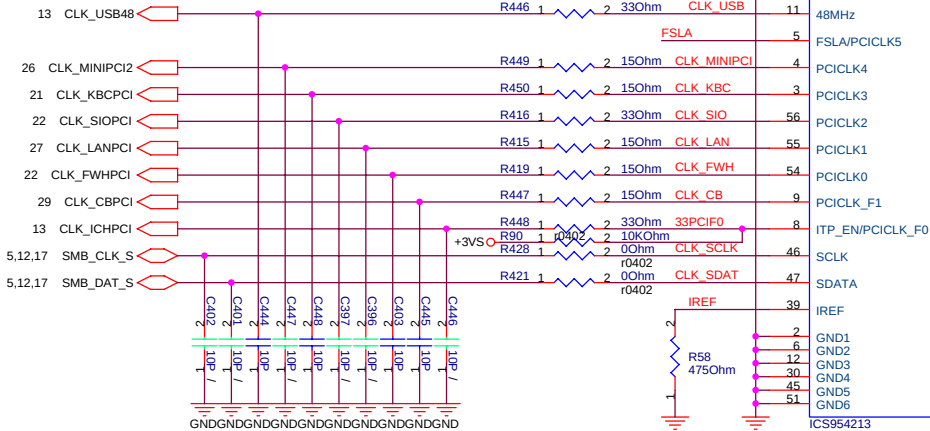


<Variant Name>

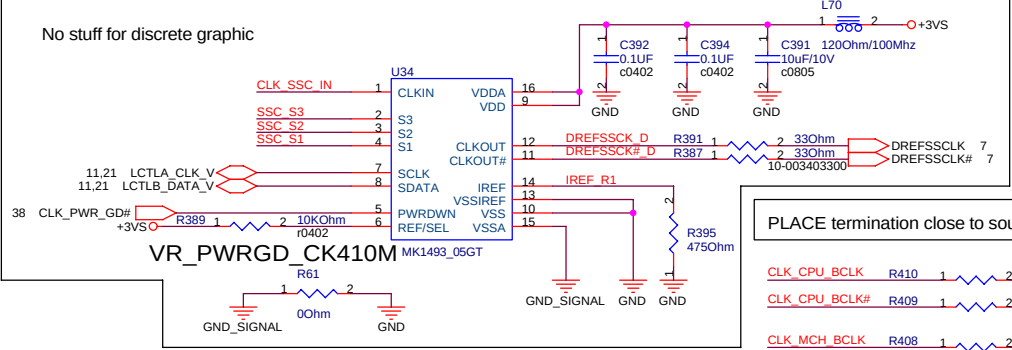
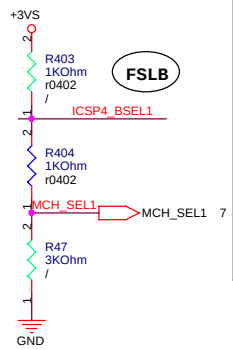
Bit	Bit	Bit	CPU	SRC	SATA	PC
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	200.00	100.00	100.00	33.33
0	0	1	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
0	1	1	133.33	100.00	100.00	33.33
1	0	0	333.33	100.00	100.00	33.33
1	0	1	133.33	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33



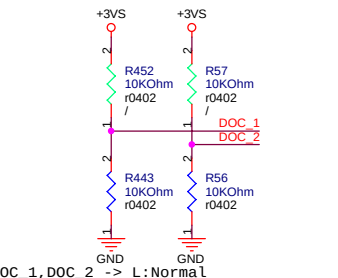
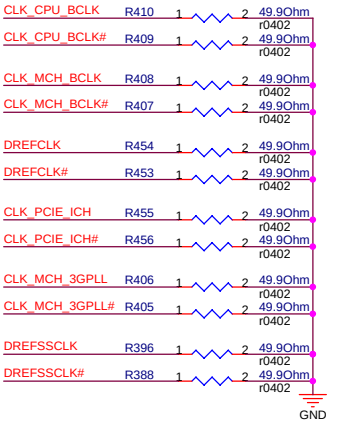
SWITCH TABLE	10r4	20r3
Dothan 533	4	3
Dothan 480	1	2
Celeron	1	2
Banias	1	2



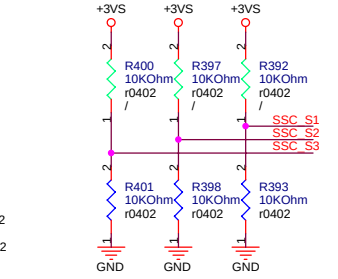
R441 10K pull up to +3VS for CPUCLK2_ITP
R442 10K pull down to GND for SRC5

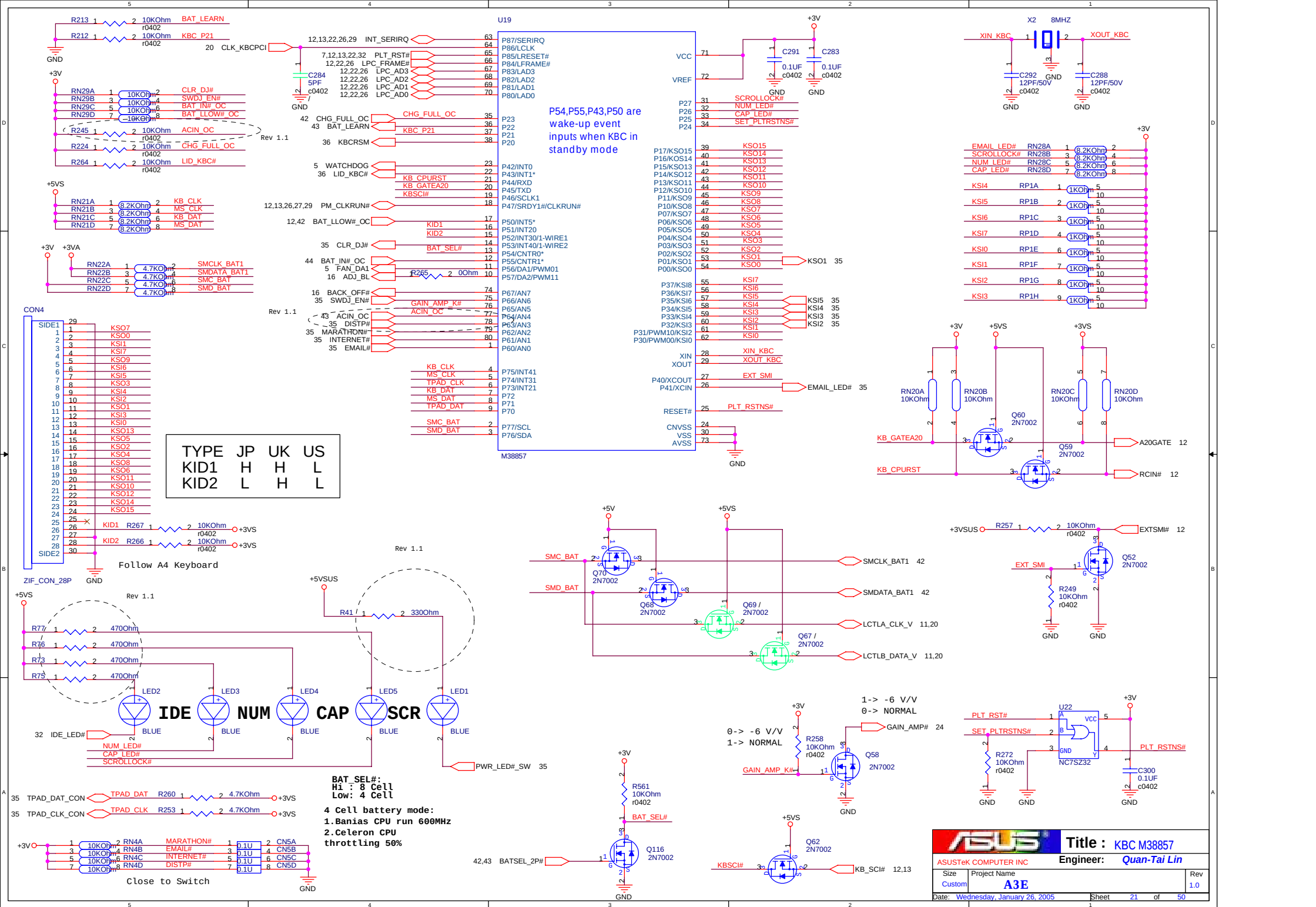


PLACE termination close to source IC

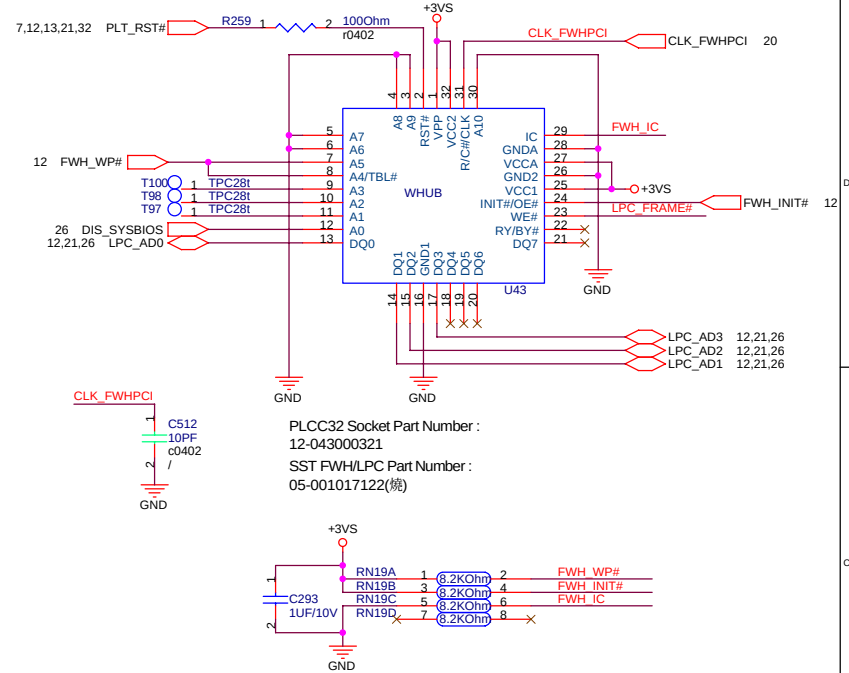
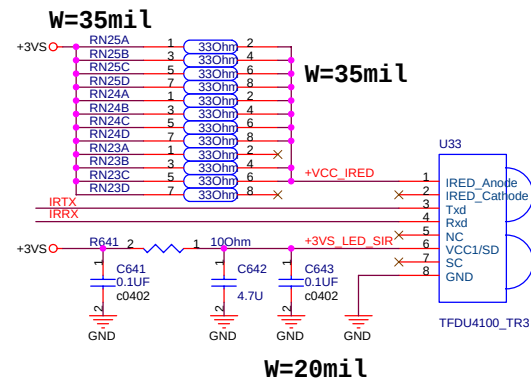
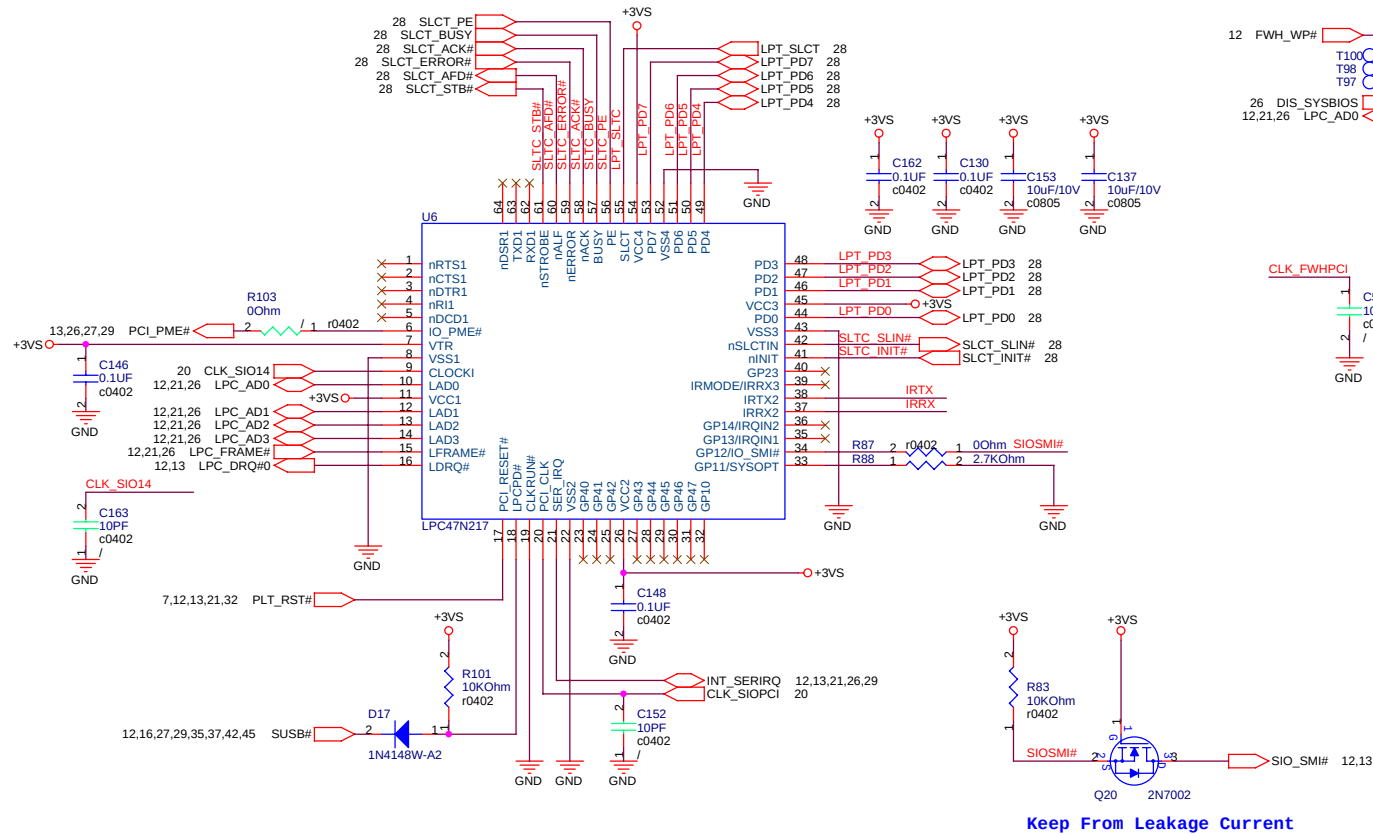


H:Freq will jump to a preprogrammed value in the I2C



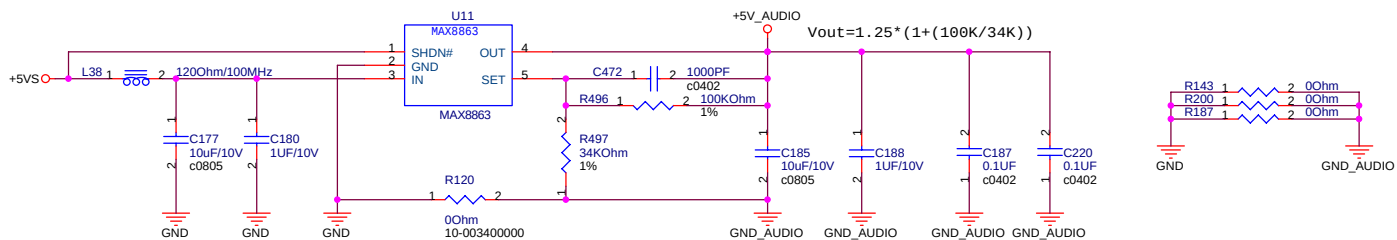
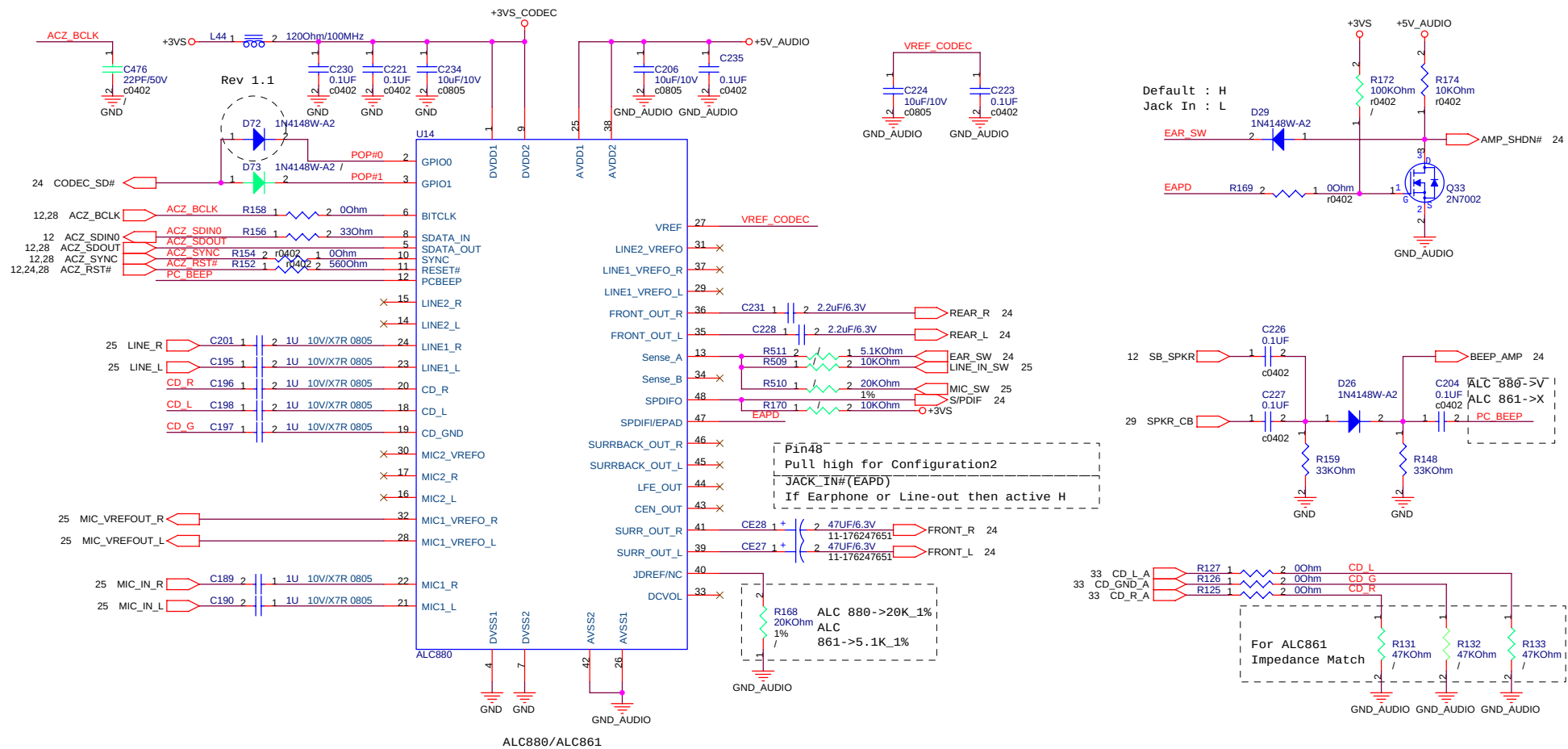


Super I/O

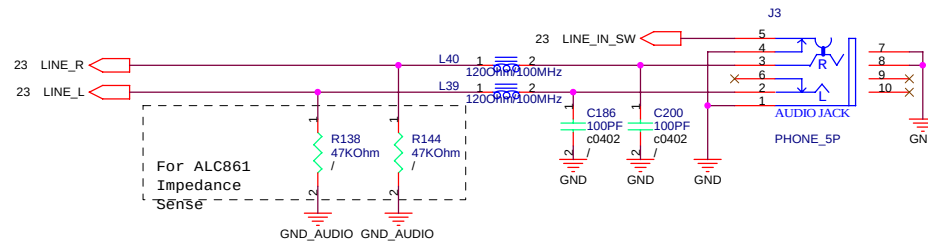
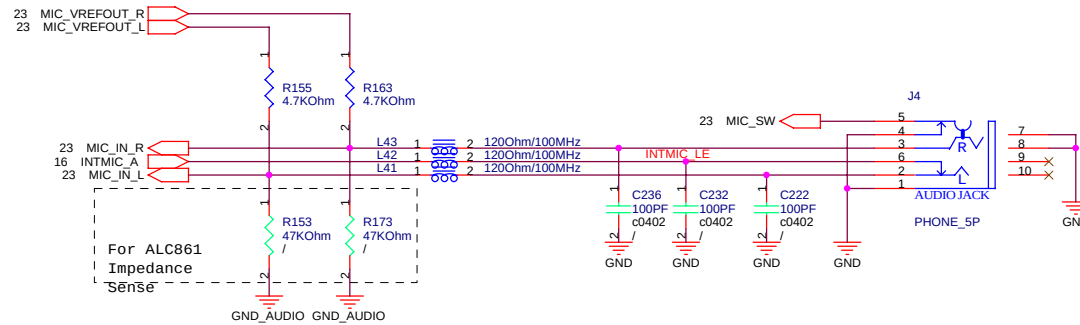
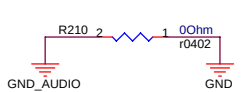
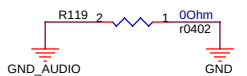
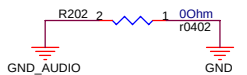
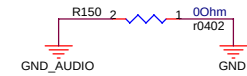
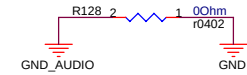
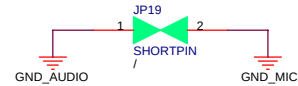


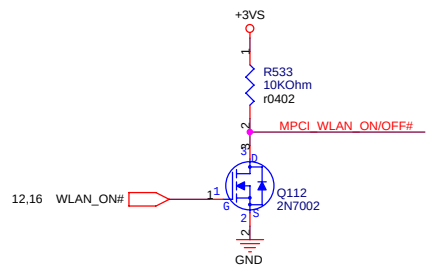
Keep From Leakage Current

ASUS		Title : FWH / SIO / SIR	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	1.0	
Date: Wednesday, January 26, 2005		Sheet	22 of 50

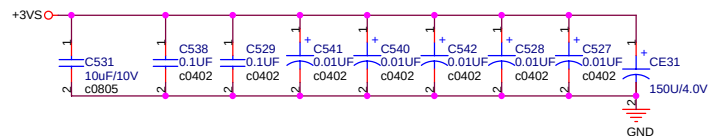
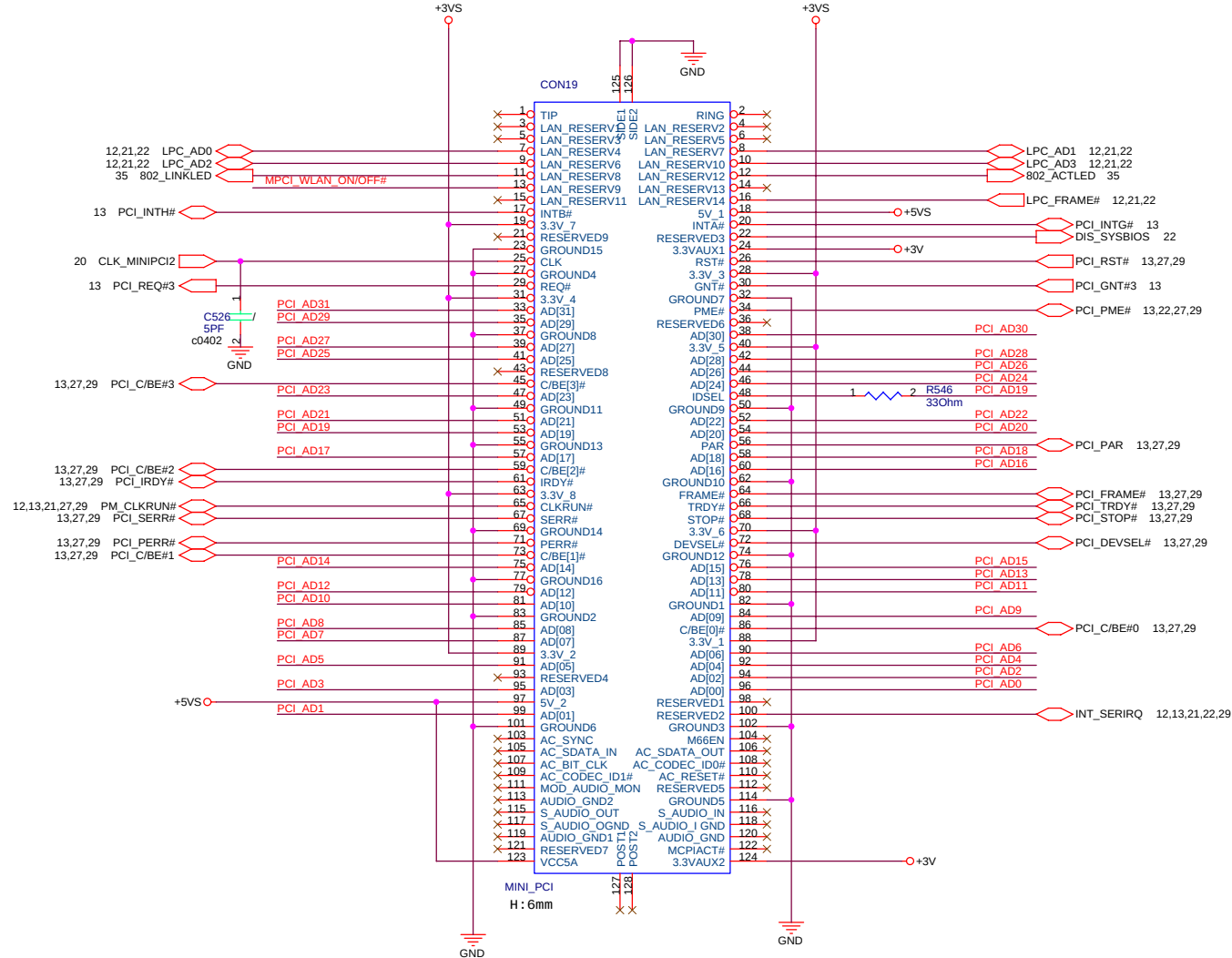


INTMIC_A:GND_AUDIO : W/P/X = 12/5/15mils



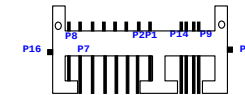
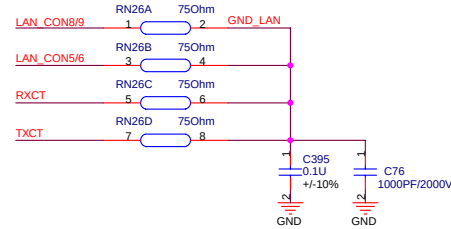
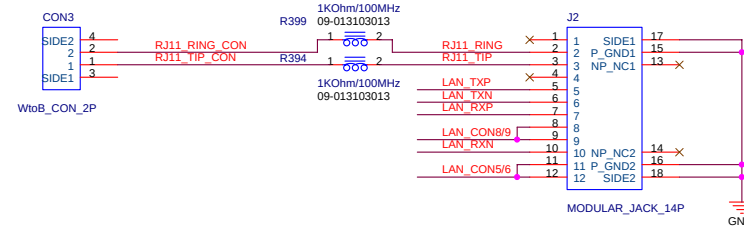
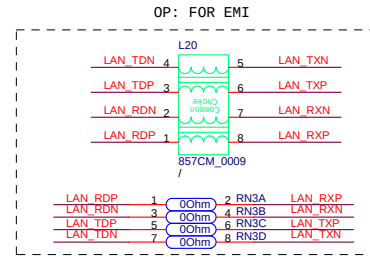
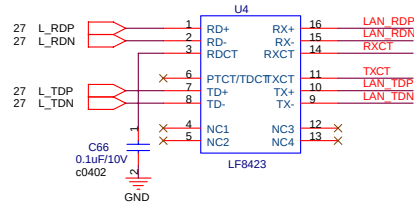


13,27,29 PCI_AD[0..31]



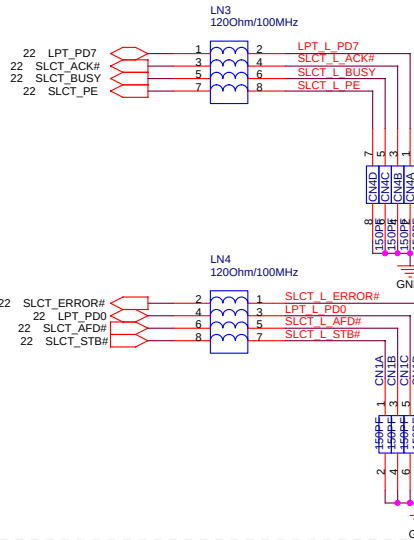
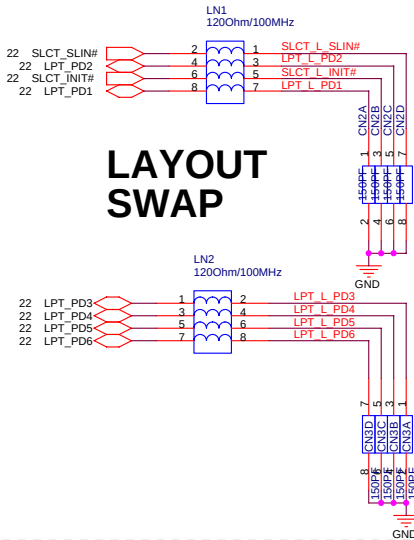


LAN PORT

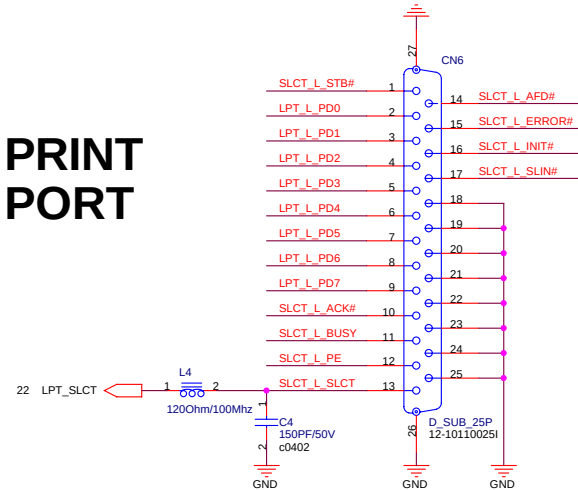


RJ 45 & RJ 11
BOTTOM VIEW

LAYOUT SWAP

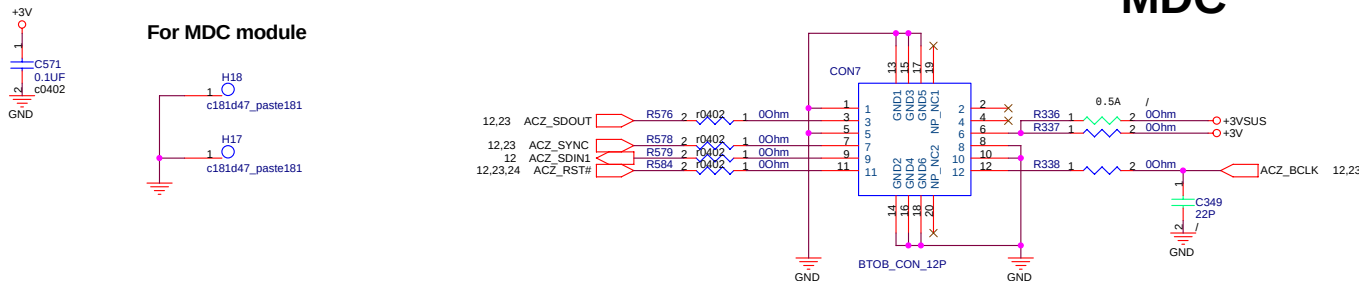


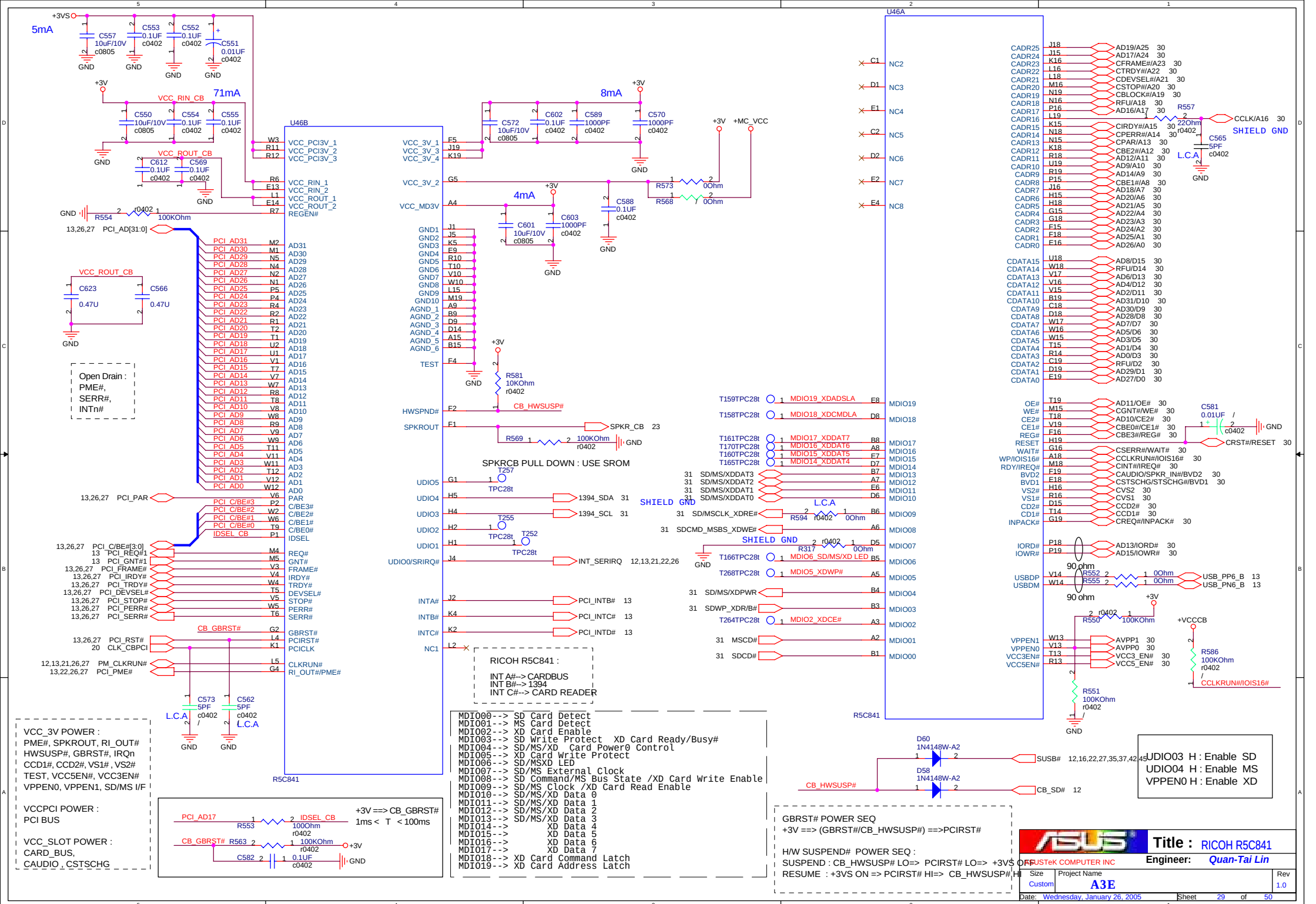
PRINT PORT

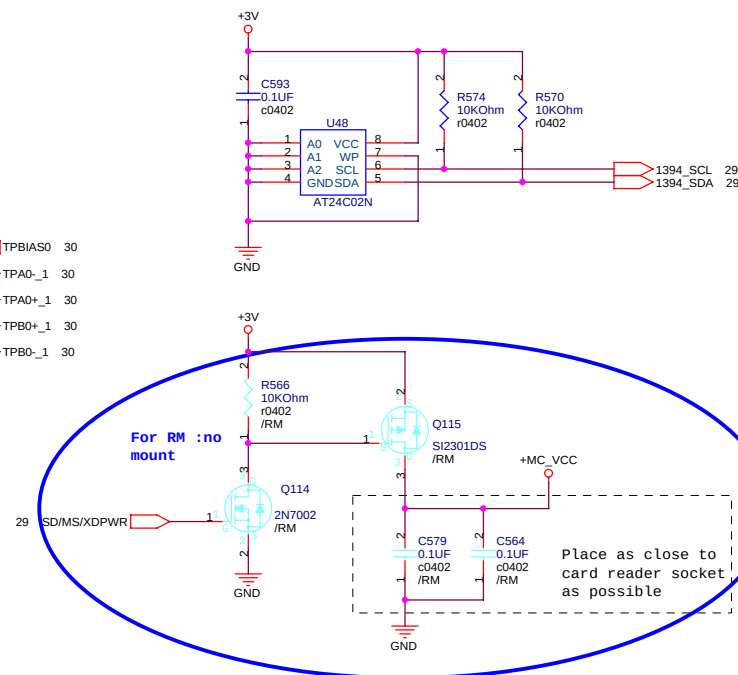


MDC

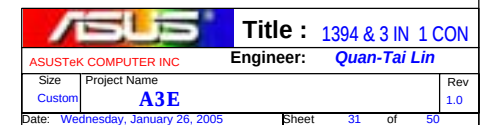
For MDC module

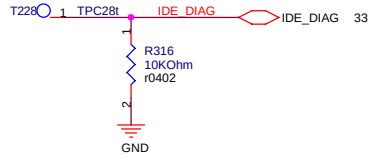




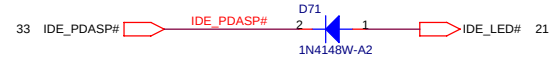
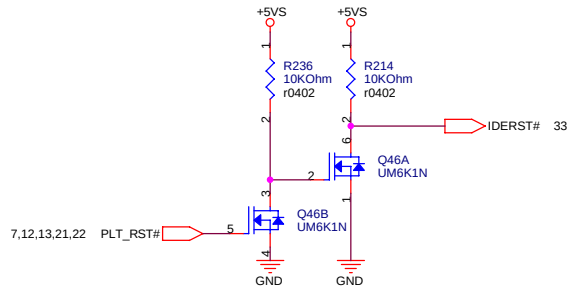
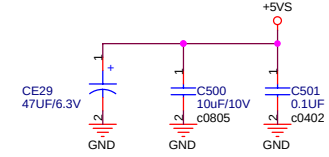
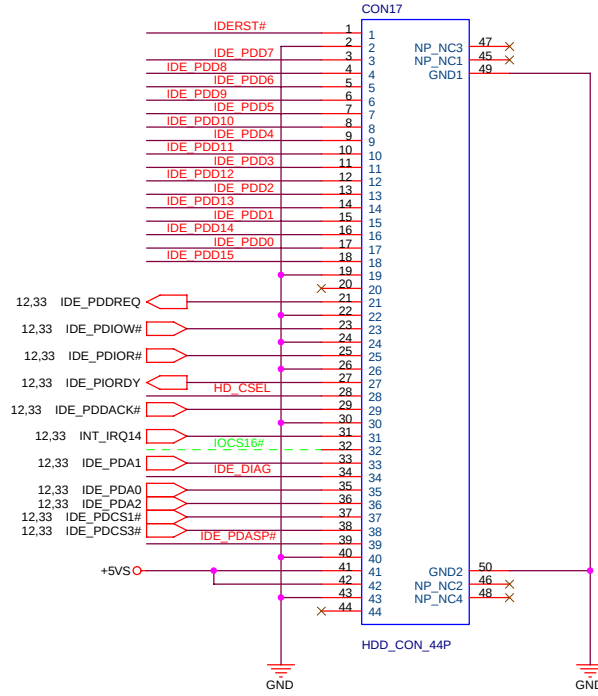
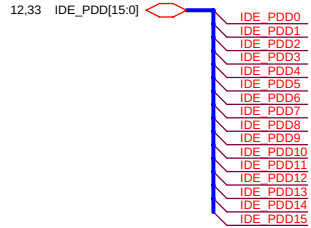


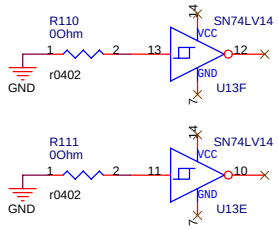
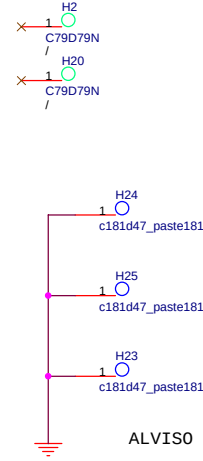
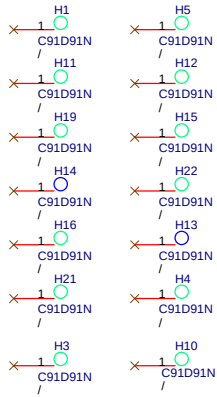
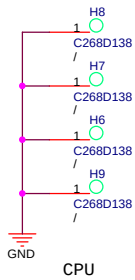
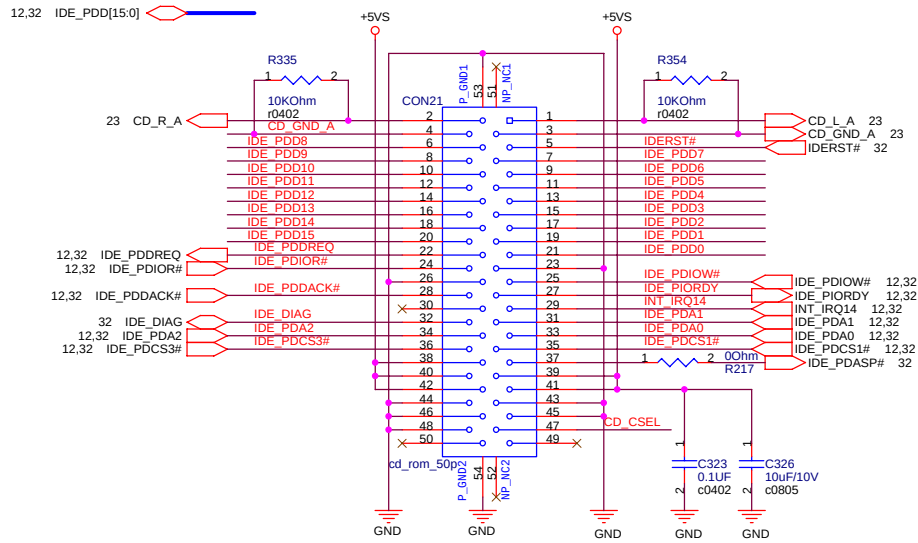
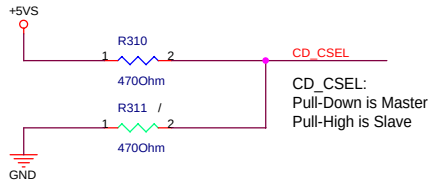
- Layout: SHIELD GND



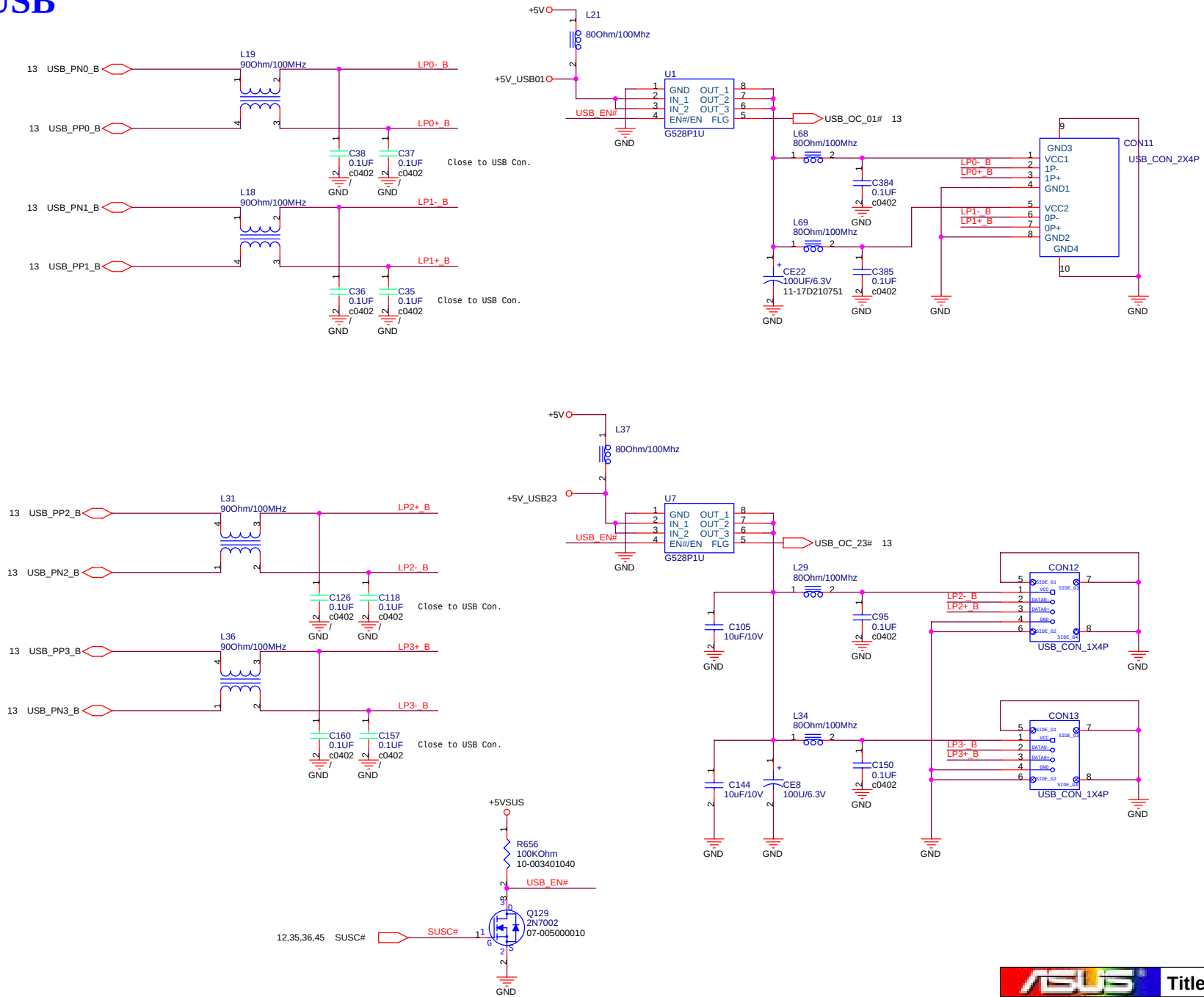


HD_CSEL : Pull-Down, HDD as Master





USB



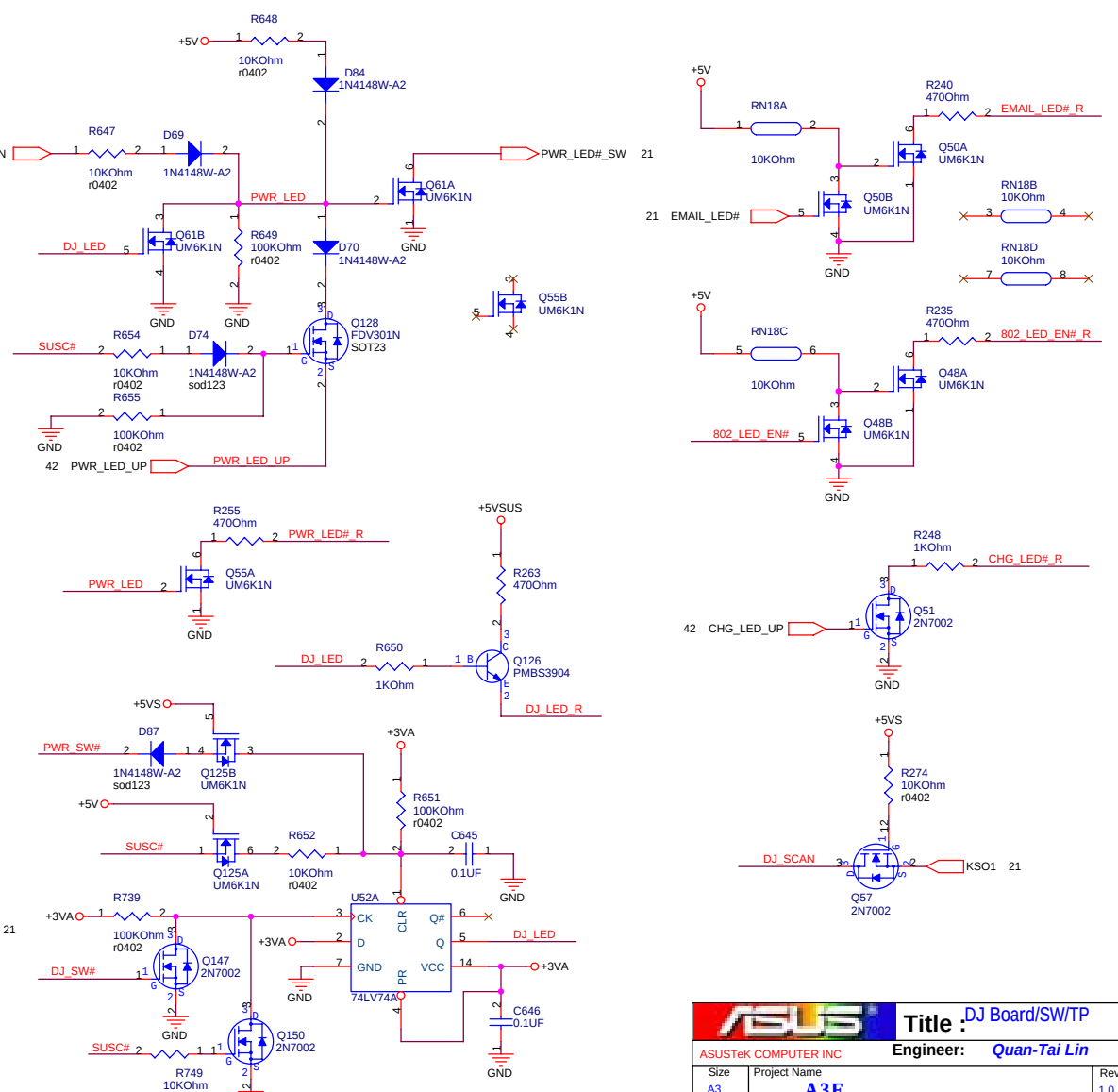
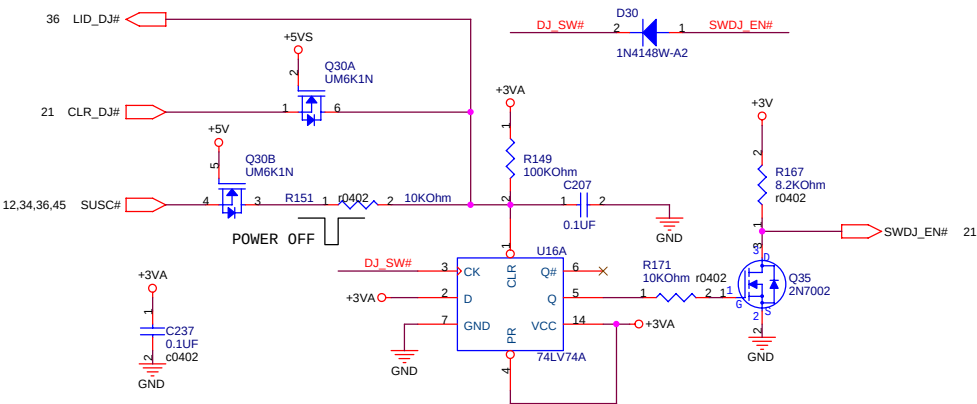
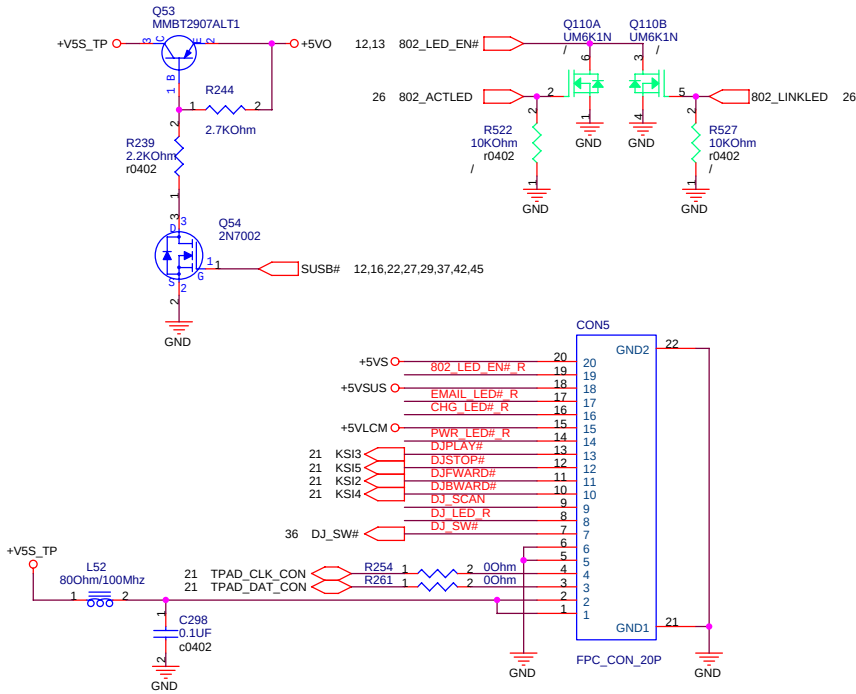
Power4 Gear

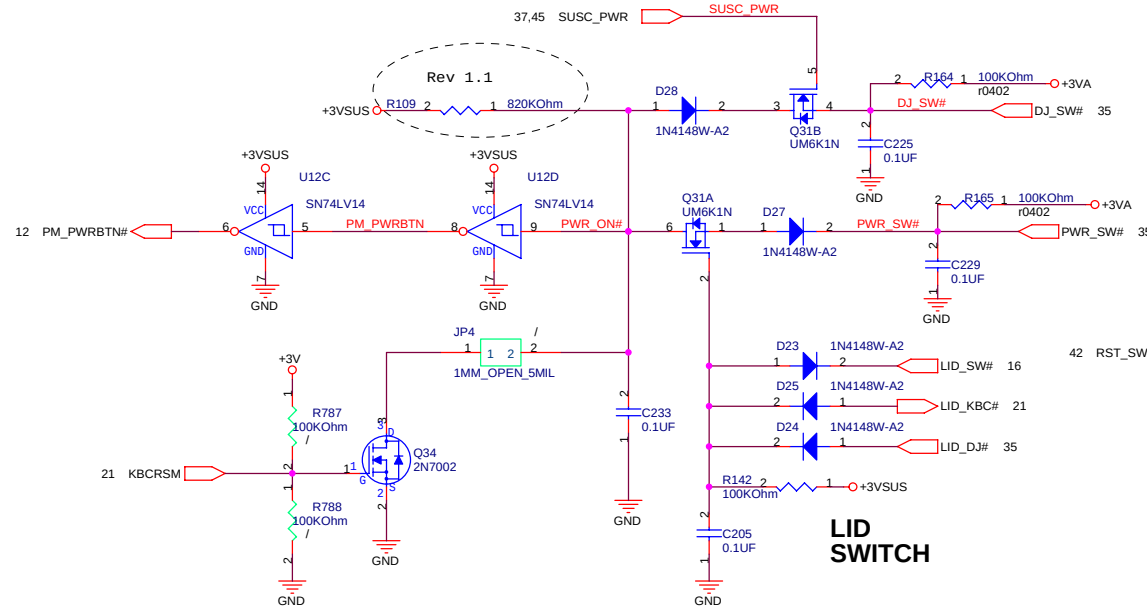
E-Mail

Internet

Touchpad Disable

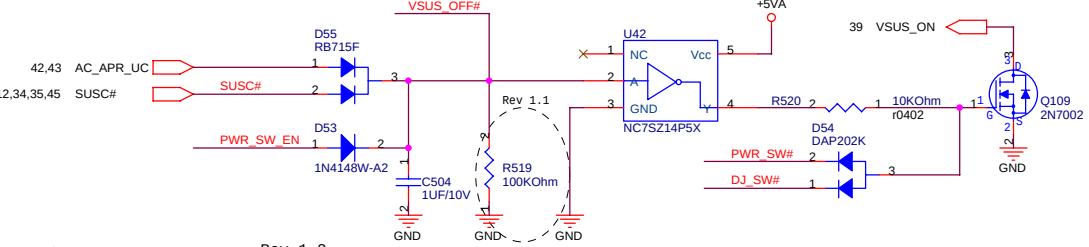
Power Switch





LID SWITCH

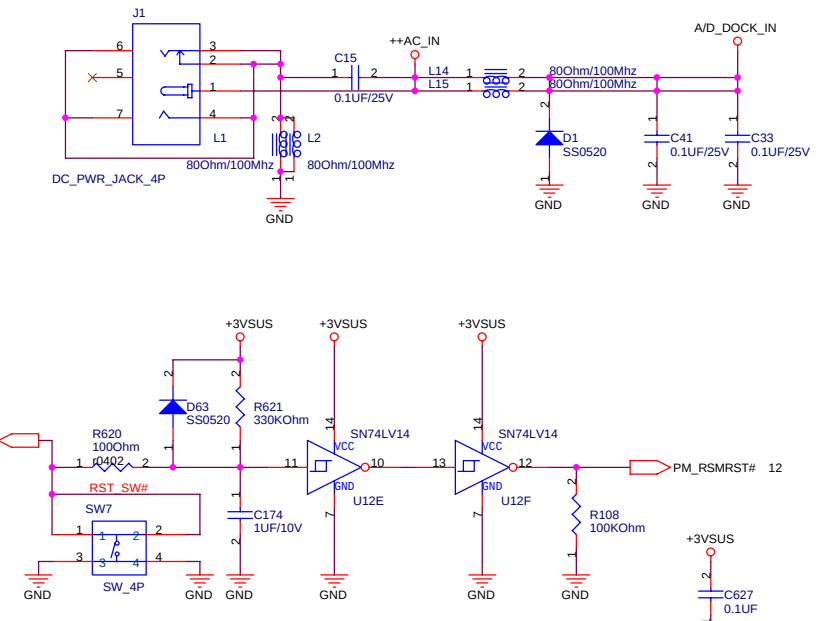
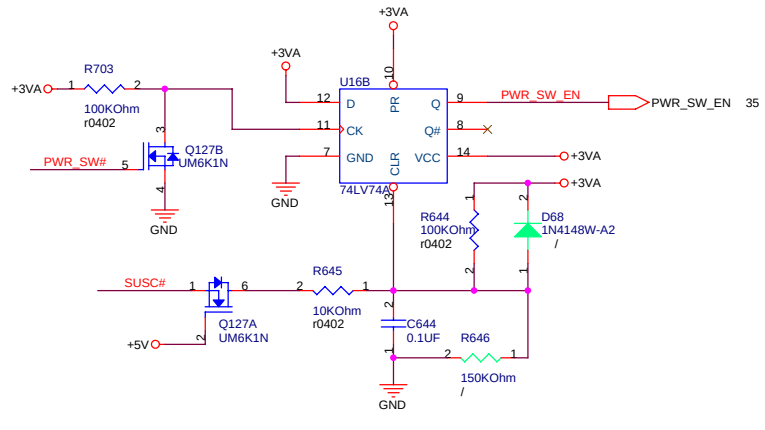
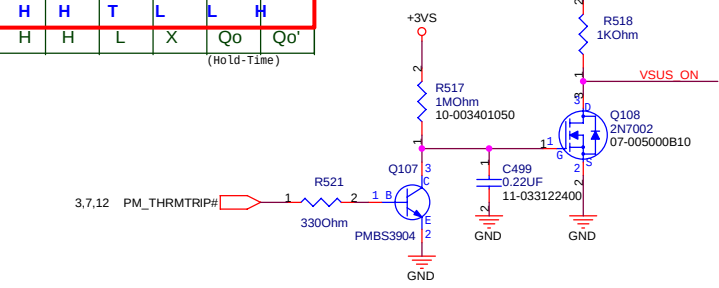
AC_APR_UC:IN=HIGH / OUT=LOW



74HC74 TRUTH TABLE Rev 1.2

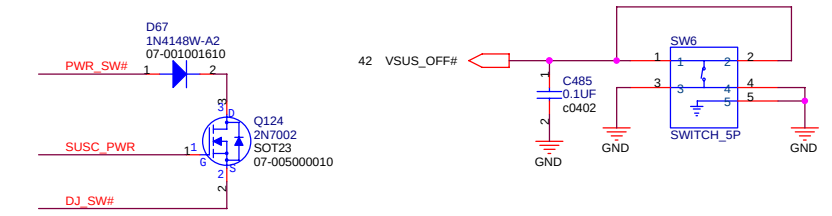
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Q ₀	Q ₀ '

(Hold-Time)

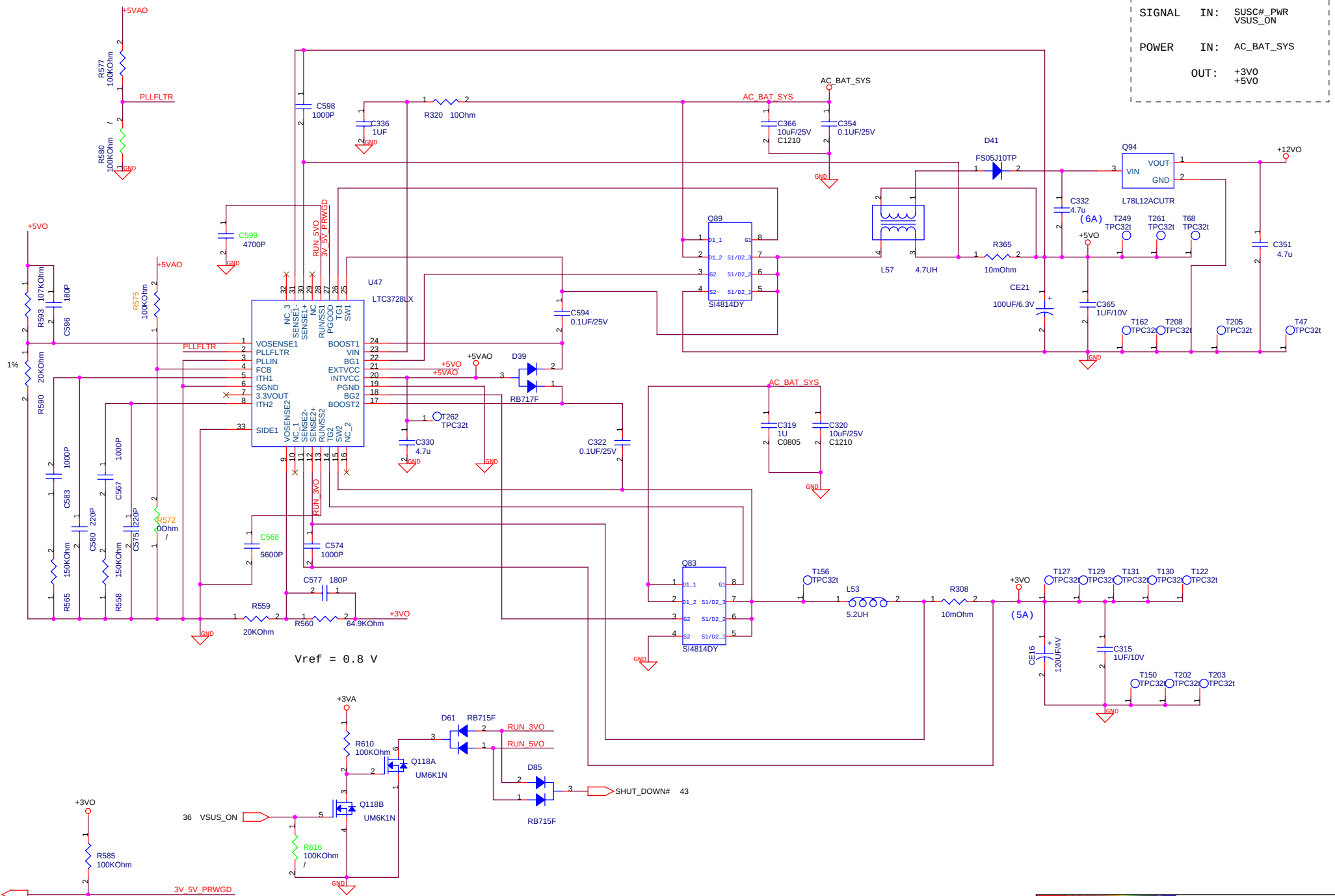


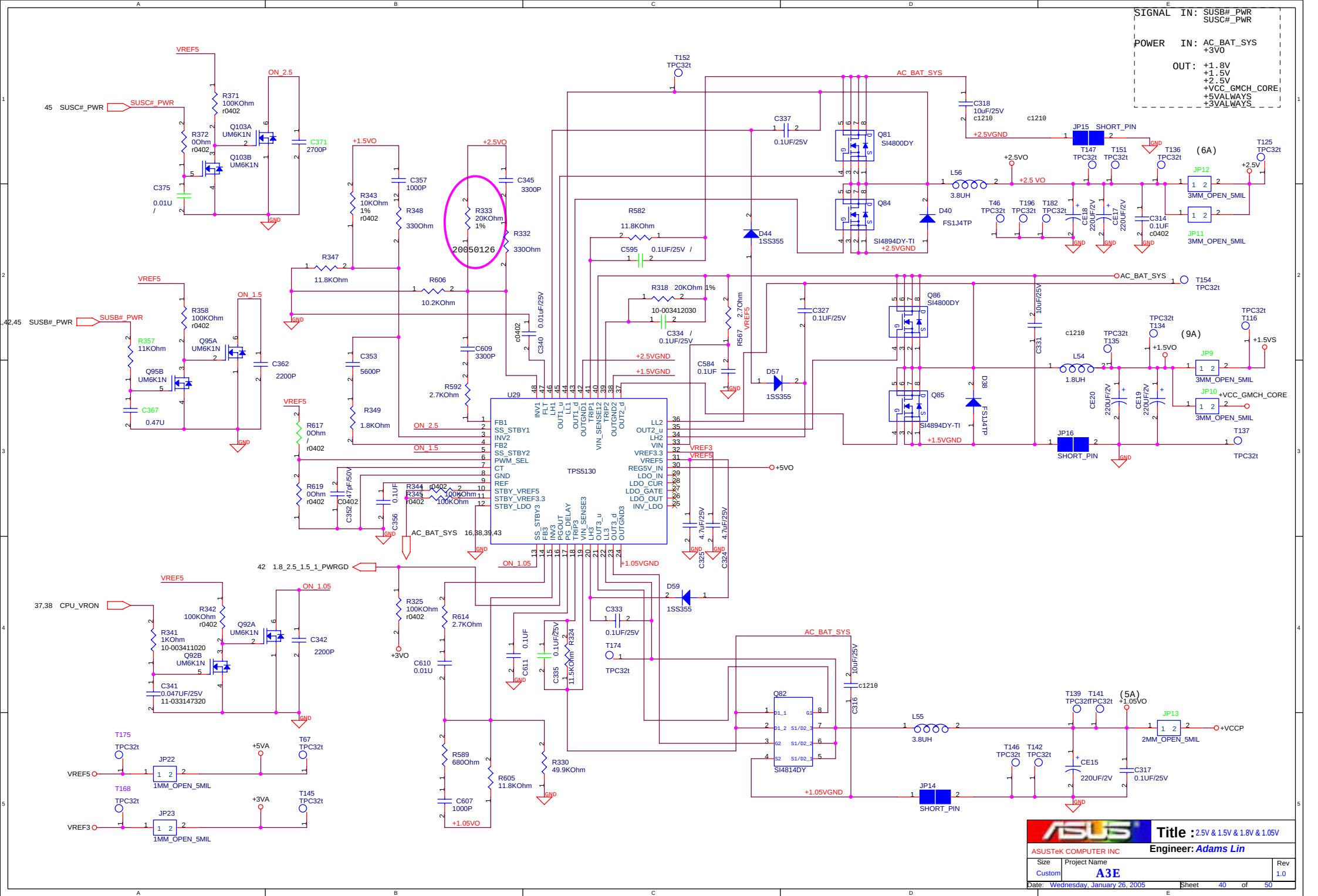
RESET BUTTON Boot from S4 Push Reset SW

RISE TIME: 40mV/uS
40 mS FORM 0 V TO 2.318 V
(SPEC: >10 mS) +3.3VA TO RSMRST#



System Power Sequence
+VCCRTC -> RTCRST# -> V5REFSUS -> 3.3/L5VSUS
RSMRST# -> SUSB# -> SUSB# -> VCCLAN -> LANPWOK
-> V5REF -> PWOK -> GMCH -> VCCP -> VCORE
SUSSTAT# -> PCIRST#
CPU : +VCORE, +VCCP, +1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS





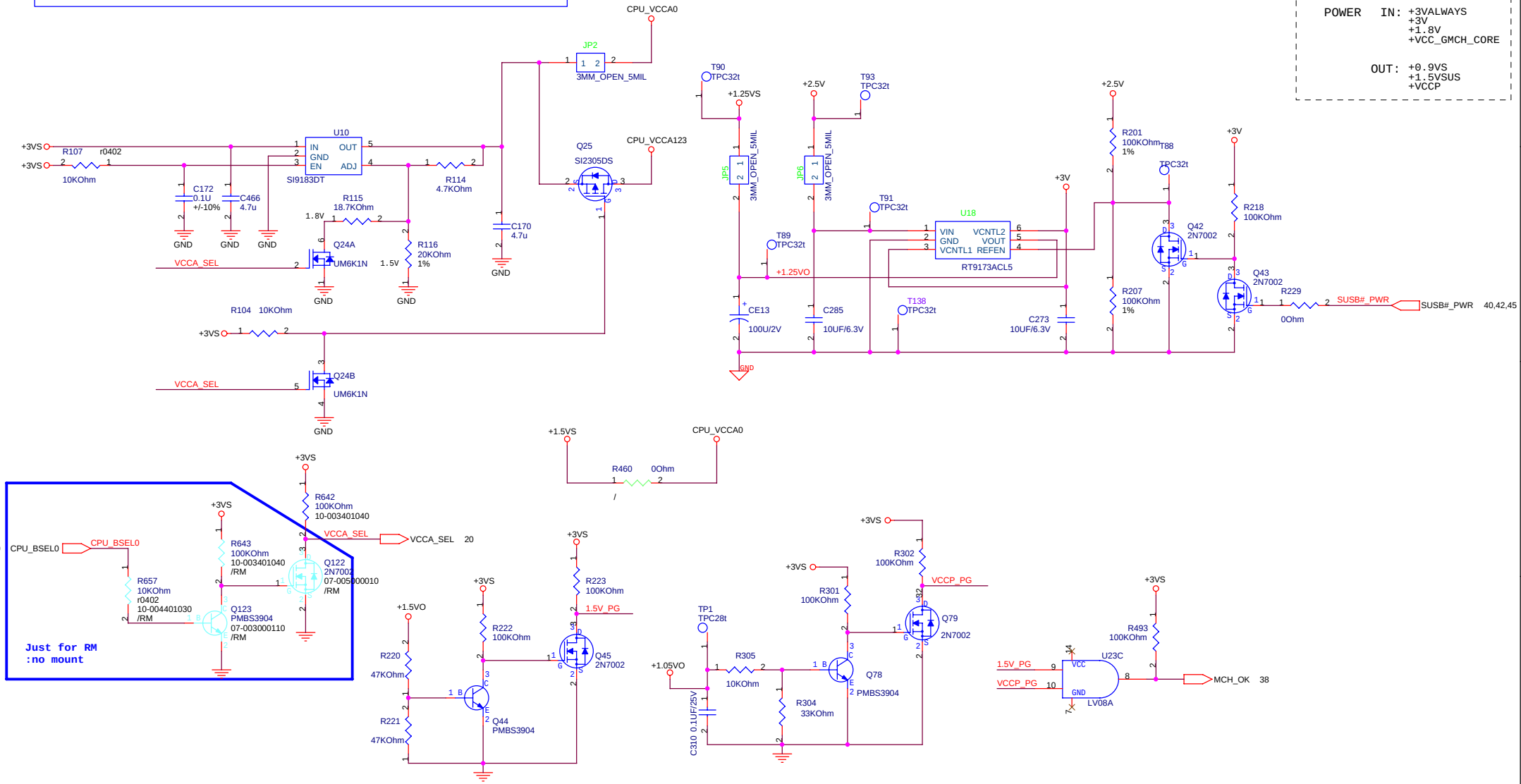
SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3V0
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS

For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V
 For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

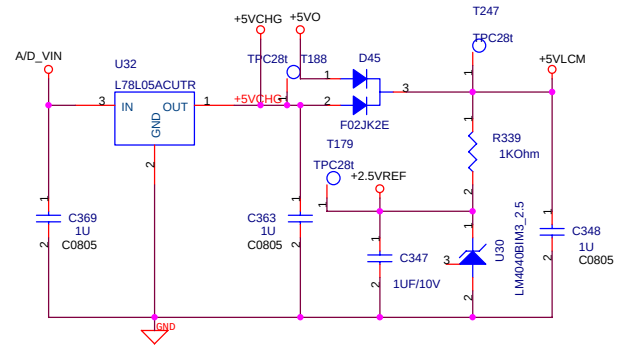
SIGNAL IN: SUSB#_PWR
 CPU_VRON

POWER IN: +3VALWAYS
 +3V
 +1.8V
 +VCC_GMCH_CORE

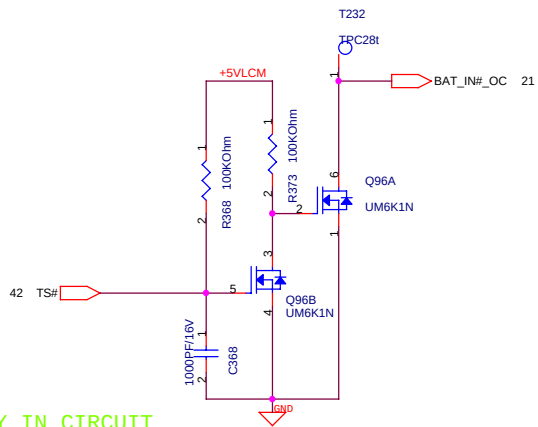
OUT: +0.9VS
 +1.5VSUS
 +VCCP



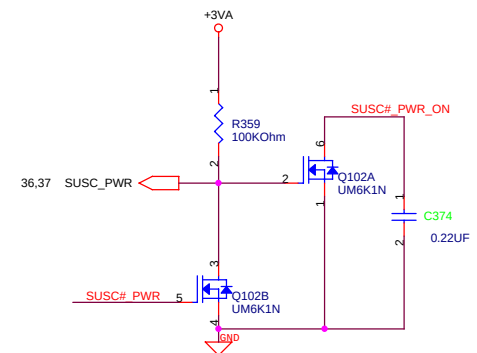
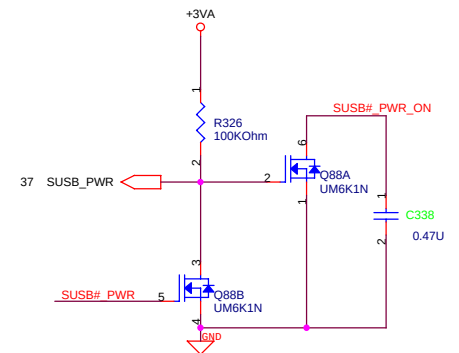
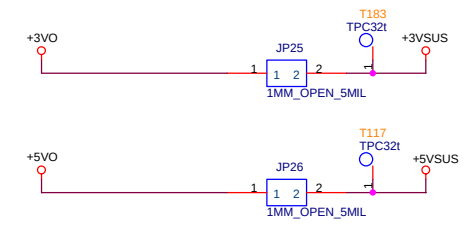
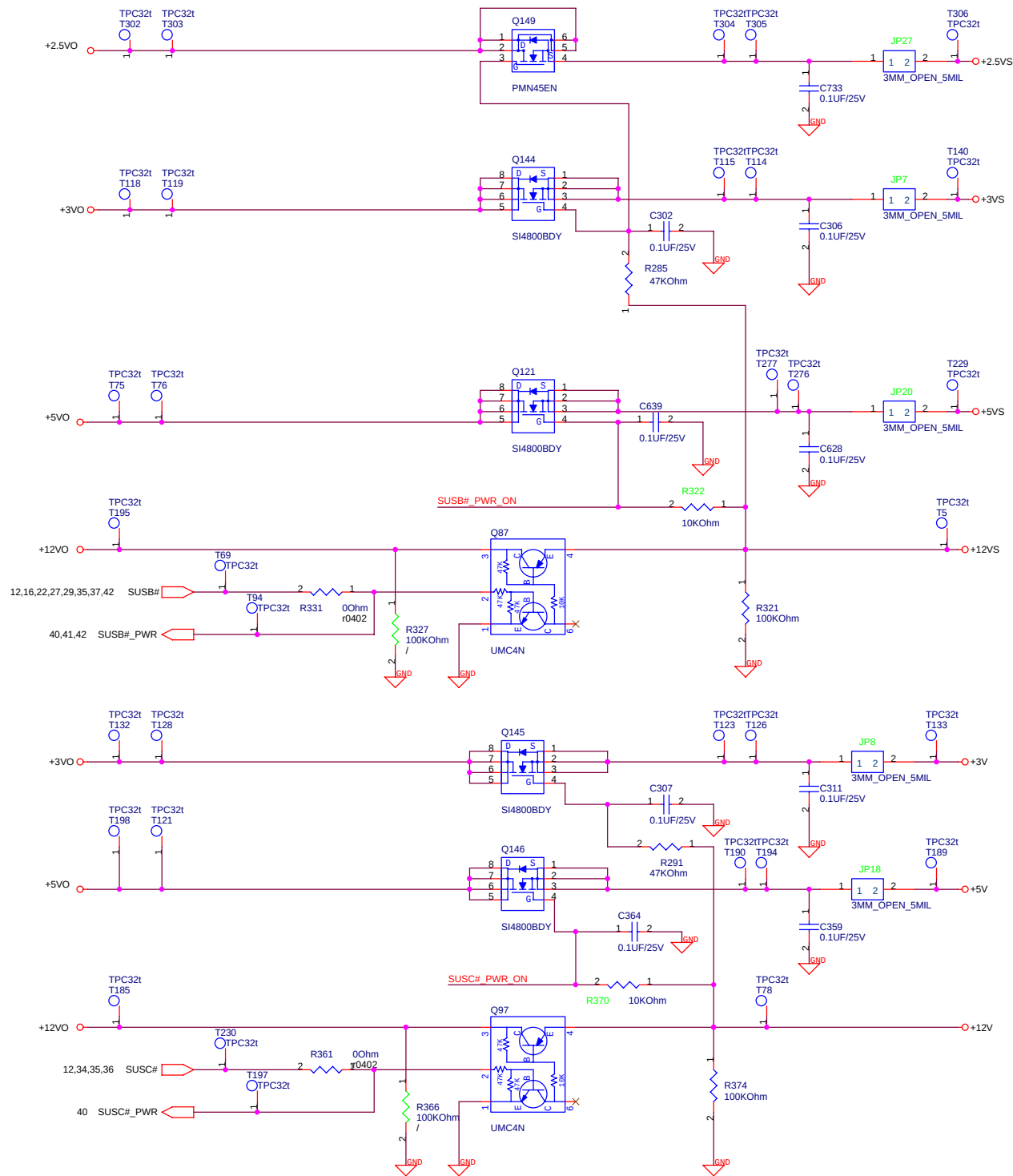


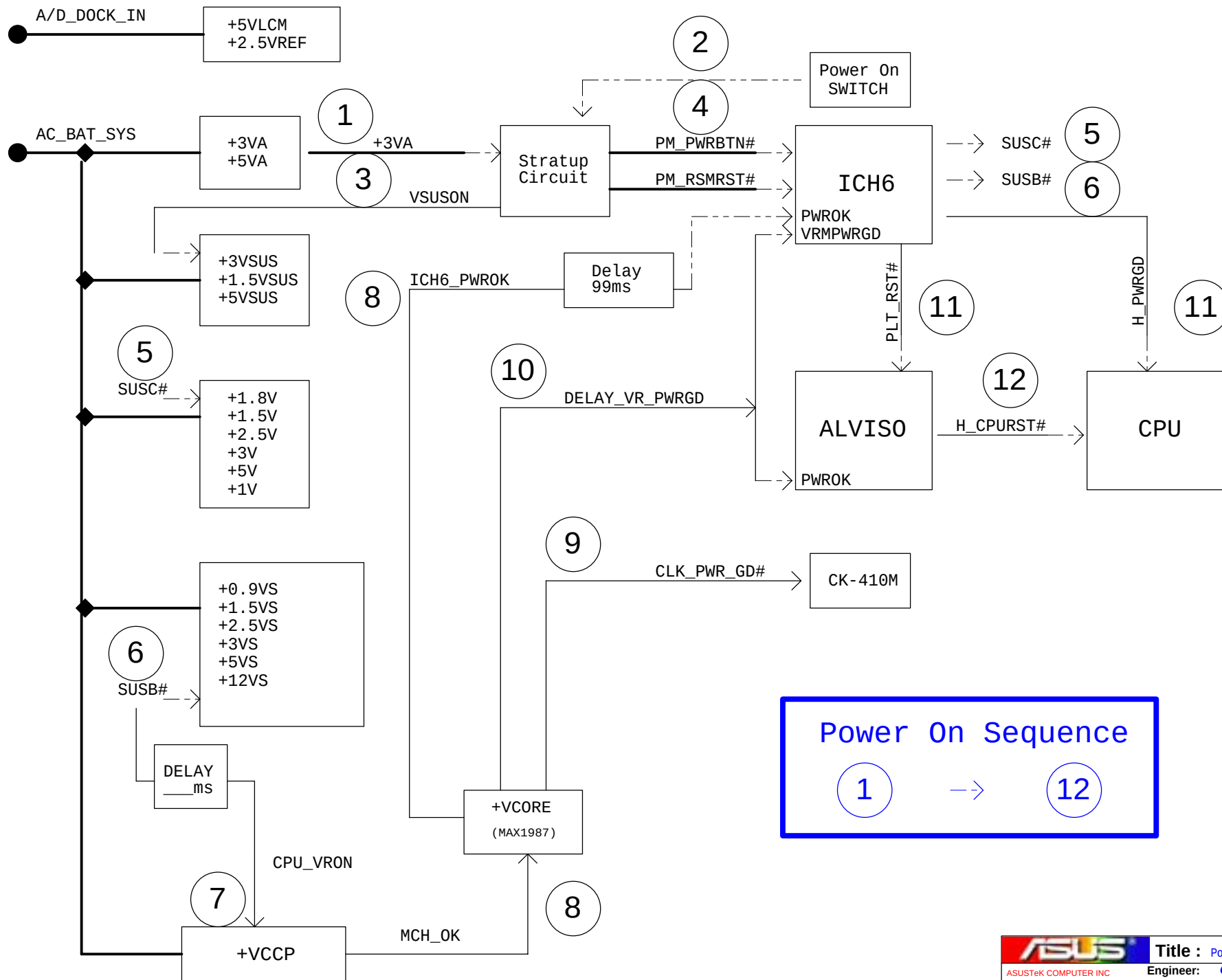


+5VCHG, +5VLCM, +2.5VREF



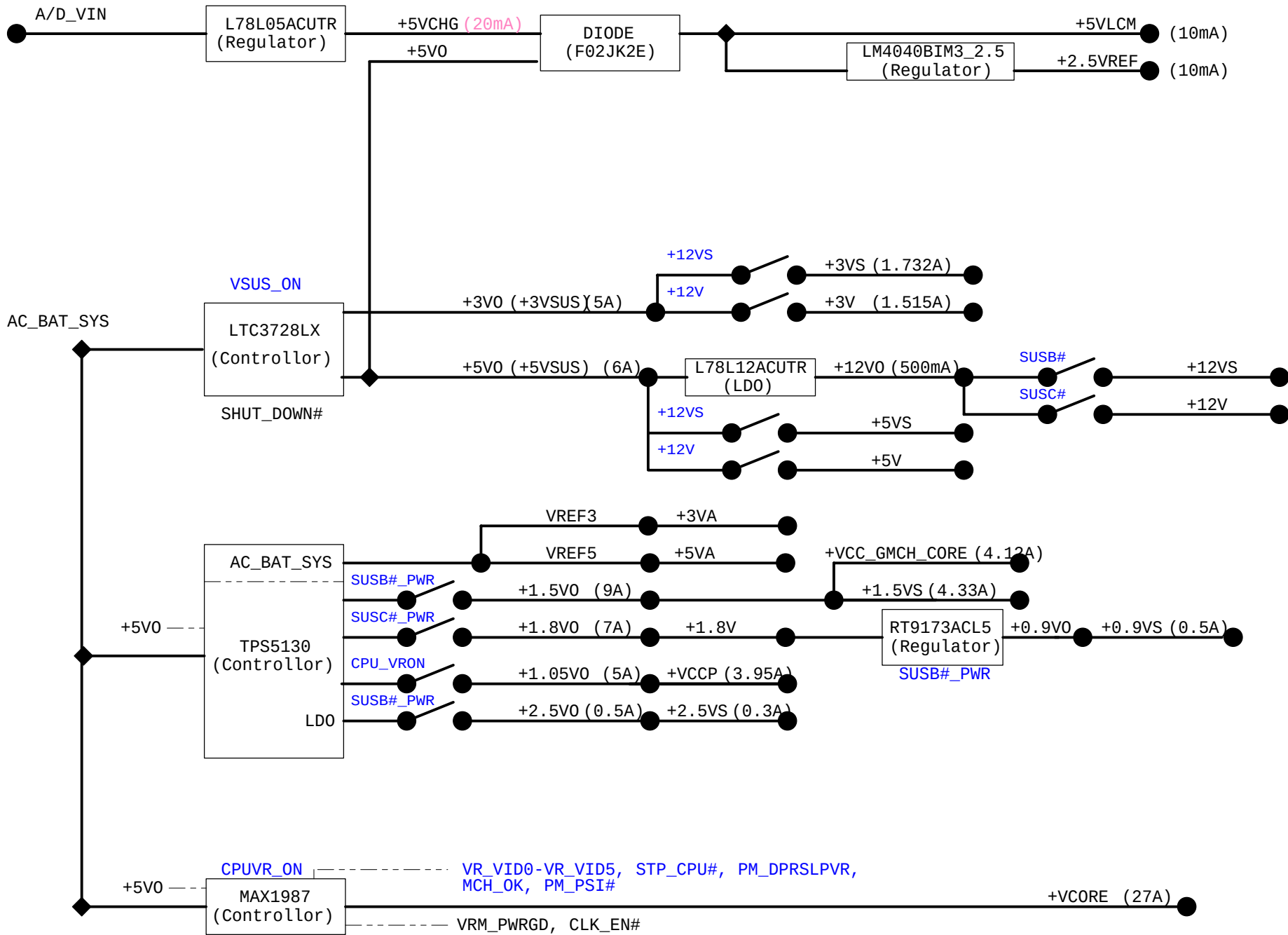
BATTERY IN CIRCUIT





Power On Sequence

1 → 12



PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSM1#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
2005/01/21-1140		JP28 for CMOS clear renames to JRST1 and no mount
2005/01/21-1140		U19.77 signal changes to ACIN_OC and R245 still mount
2005/01/21-1140		R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm
2005/01/21-1140		R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm
2005/01/26-0945		D72 mount

Rev.	Data	Description
For RM:		
2005/01/24-1035		Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

