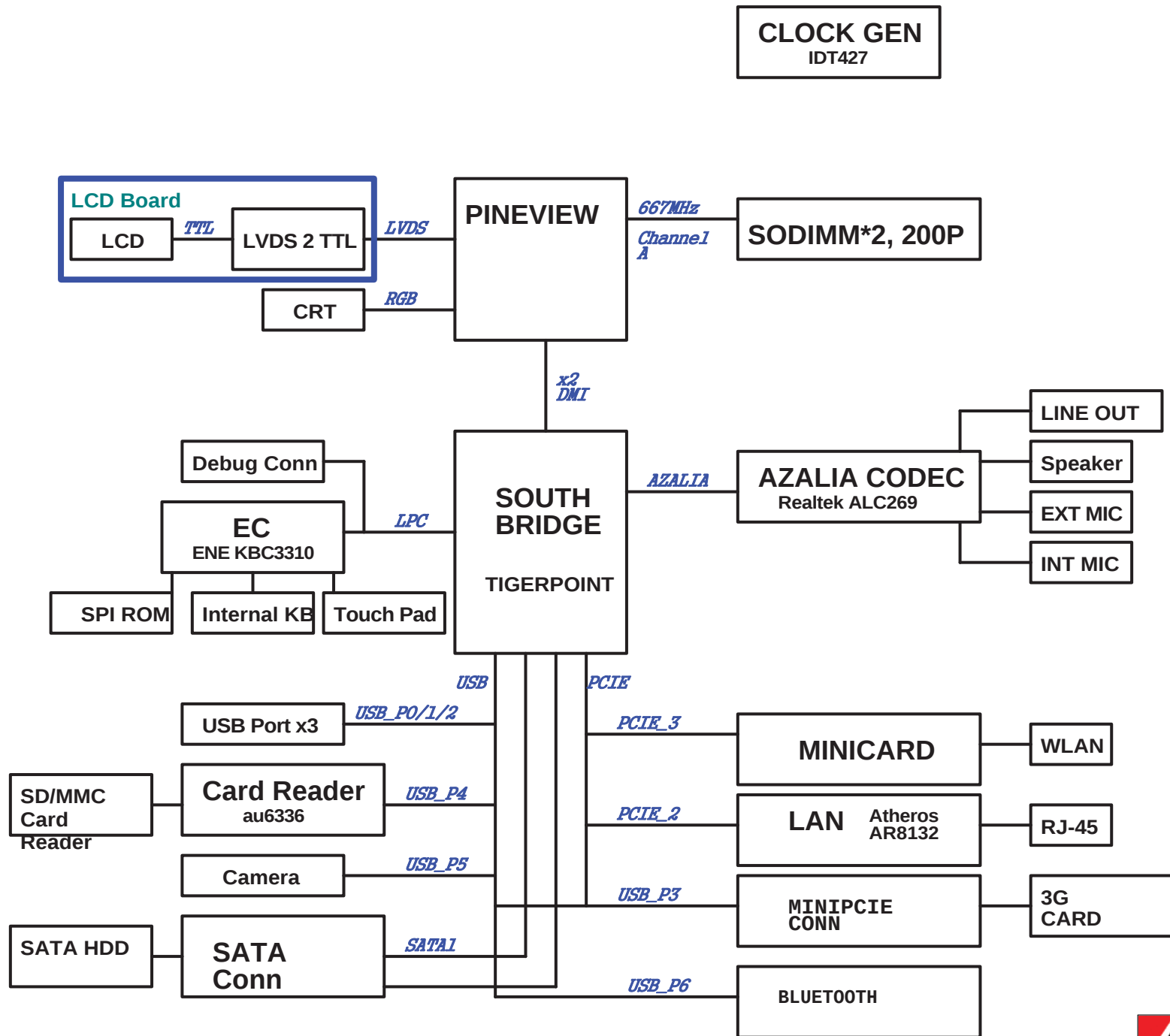
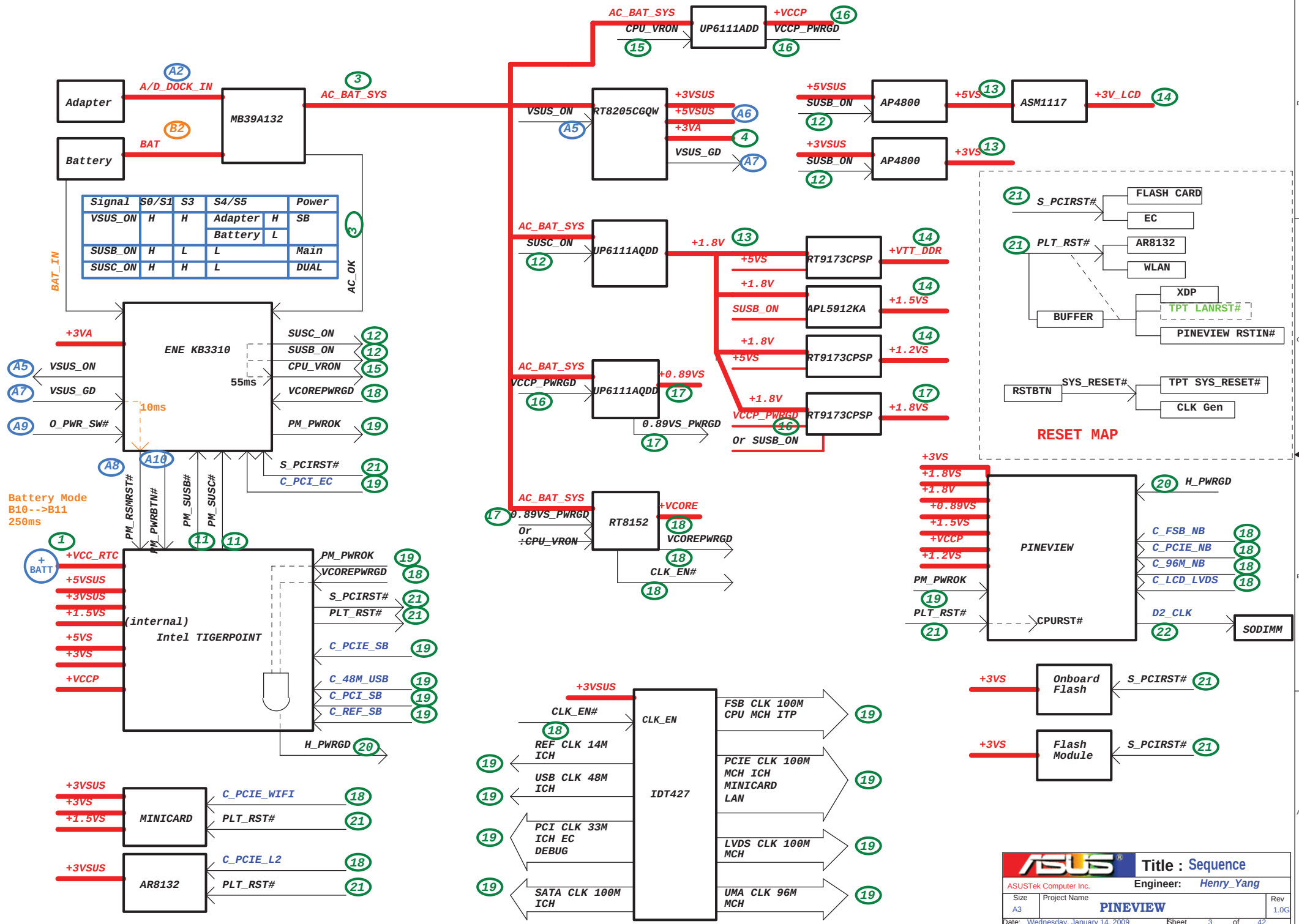


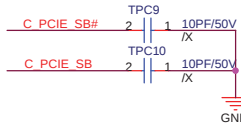
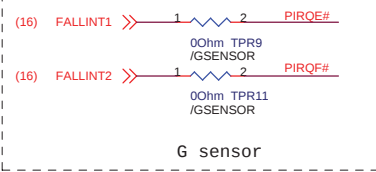
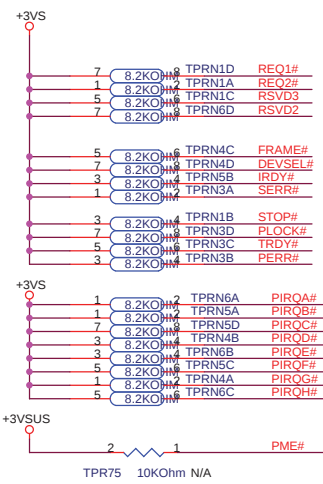


ICH7M GPIO DEFAULT&NOW
SETTING

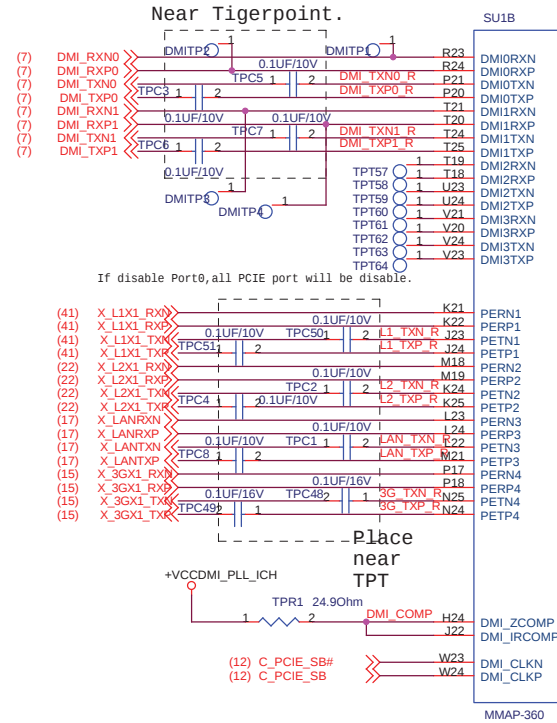
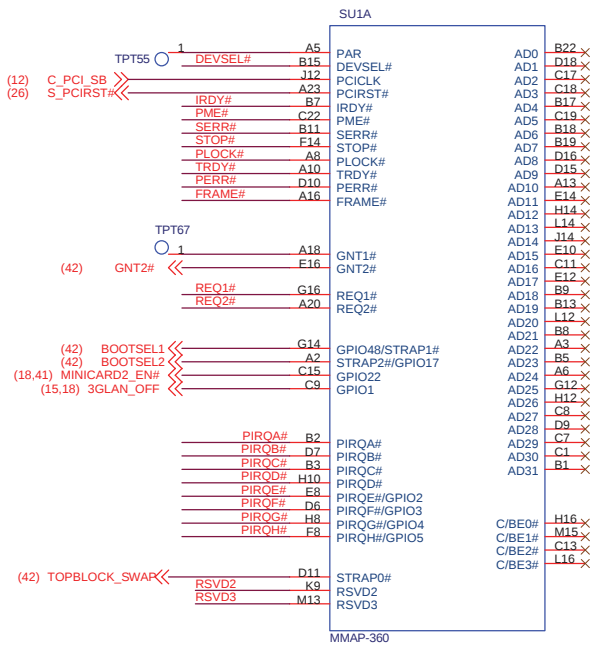
Pin	Pin Name	Type	Tolerance	Powe Well	Default	Now Setting
AB18	GPIO0/BM_BUSY#	I/O	3.3V	CORE	GPI	BM_BUSY#
C8	GPIO1/REQ5#	I/O	5V	CORE	GPI	REQ5#
G8	GPIO2/PIRQE#	I/OD	5V	CORE	GPI	PIRQE#
F7	GPIO3/PIRQF#	I/OD	5V	CORE	GPI	PIRQF#
F8	GPIO4/PIRQG#	I/OD	5V	CORE	GPI	PIRQG#
G7	GPIO5/PIRQH#	I/OD	5V	CORE	GPI	PIRQH#
AC21	GPIO6	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AC18	GPIO7	I/O	3.3V	CORE	GPI	GPO,WLAN_LED
E21	GPIO8	I/O	3.3V	Resume	GPI	GPI,EXTSMI#
E20	GPIO9	I/O	3.3V	Resume	GPI	GPI,No Function,10K Pull +3VS
A20	GPIO10	I/O	3.3V	Resume	GPI	GPO,WLAN_ON#
B23	GPIO11/SMBALERT#	I/O	3.3V	Resume	Native	SMBALERT#
F19	GPIO12	I/O	3.3V	Resume	GPI	GPI,KBC_SCI#
E19	GPIO13	I/O	3.3V	Resume	GPI	GPO,VCCP_DOWN
R4	GPIO14	I/O	3.3V	Resume	GPI	GPO,1.5VS_DOWN
E22	GPIO15	I/O	3.3V	Resume	GPI	GPI,No Function,10K Pull +3VSUS
AC22	GPIO16/DPRSLVR	I/O	3.3V	CORE	Native	DPRSLVR
D8	GPIO17/GNT5#	I/O	3.3V	CORE	GPO	BIOS_SEL1
AC20	GPIO18/STPPCI#	I/O	3.3V	CORE	GPO	STP_PCI#
AH18	GPIO19/SATA1GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AF21	GPIO20/STPCPU#	I/O	3.3V	CORE	GPO	STP_CPU#
AF19	GPIO21/SATA0GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
A13	GPIO22/REQ4#	I/O	3.3V	CORE	Native	REQ4#
AA5	GPIO23/LDRQ1#	I/O	3.3V	CORE	Native	LDRQ1#
R3	GPIO24	I/O	3.3V	Resume	GPO	GPO,MINICARD1_EN#
D20	GPIO25	I/O	3.3V	Resume	GPO	GPO,DUAL_DOWN

Pin	Pin Name	Type	Tolerance	Powe Well	Default	Now Setting
A21	GPIO26	I/O	3.3V	Resume	GPO	GPO,VCORE_DOWN
B21	GPIO27	I/O	3.3V	Resume	GPO	GPO,CARD_READER_EN#
E23	GPIO28	I/O	3.3V	Resume	GPO	GPO,MODEM_EN#
C3	GPIO29/OC5#	I/O	3.3V	Resume	Native	OC5#
A2	GPIO30/OC6#	I/O	3.3V	Resume	Native	OC6#
B3	GPIO31/OC7#	I/O	3.3V	Resume	Native	OC7#
AG18	GPIO32/CLKRUN#	I/O	3.3V	CORE	GPO	CLKRUN#
AC19	GPIO33/AZ_DOCK_EN#	I/O	3.3V	CORE	GPO	GPO,No Function,NC
U2	GPIO34/AZ_DOCK_RST#	I/O	3.3V	CORE	GPO	GPO,No Function,NC
AD21	GPIO35	I/O	3.3V	CORE	GPO	GPO,CAMERA_EN
AH19	GPIO36/SATA2GP	I/O	3.3V	CORE	GPI	GPI,No Function,10K Pull +3VS
AE19	GPIO37/SATA3GP	I/O	3.3V	CORE	GPI	GPI,PCB_ID0
AE20	GPIO38	I/O	3.3V	CORE	GPI	GPI,PCB_ID1
AD20	GPIO39	I/O	3.3V	CORE	GPI	GPI,PCB_ID2
NA	GPIO40	NA	NA	NA	NA	NA
NA	GPIO41	NA	NA	NA	NA	NA
NA	GPIO42	NA	NA	NA	NA	NA
NA	GPIO43	NA	NA	NA	NA	NA
NA	GPIO44	NA	NA	NA	NA	NA
NA	GPIO45	NA	NA	NA	NA	NA
NA	GPIO46	NA	NA	NA	NA	NA
NA	GPIO47	NA	NA	NA	NA	NA
A14	GPIO48/GNT4#	I/O	3.3V	CORE	Native	BIOS_SEL0
AG24	GPIO49/CPUPWRGD	I/O	V_CPU_IO	V_CPU_IO	Native	CPUPWRGD

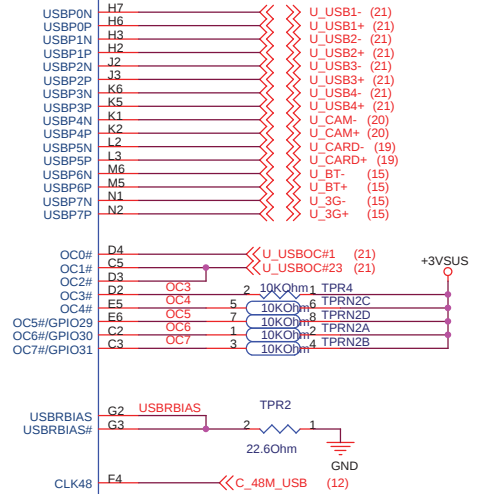




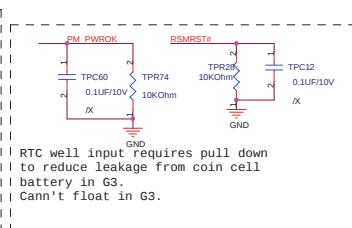
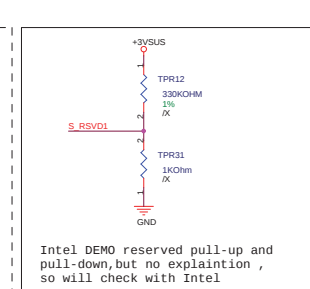
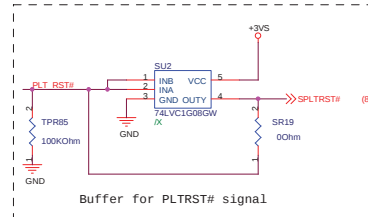
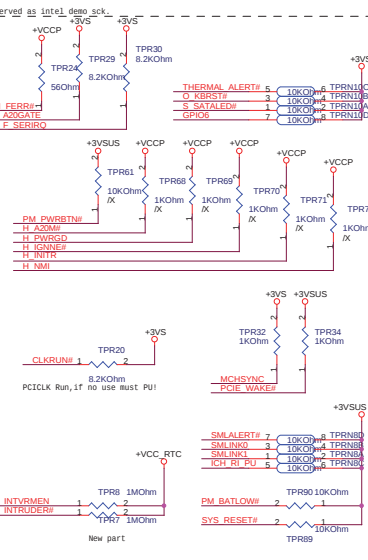
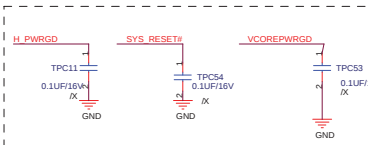
Remain
PCICLK

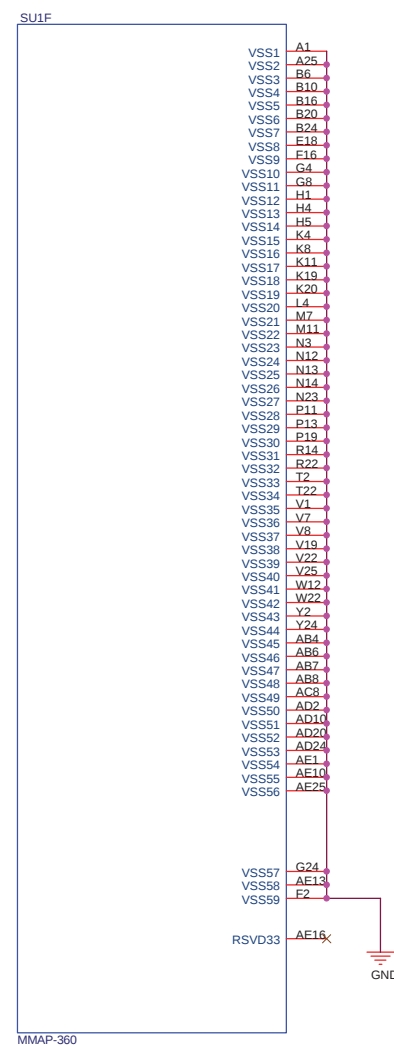
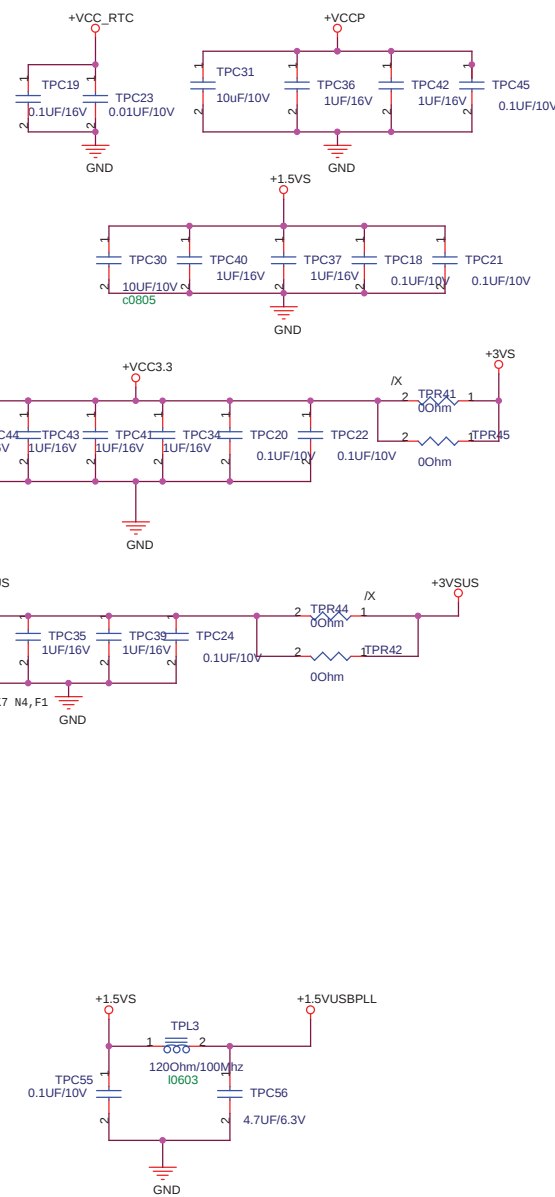
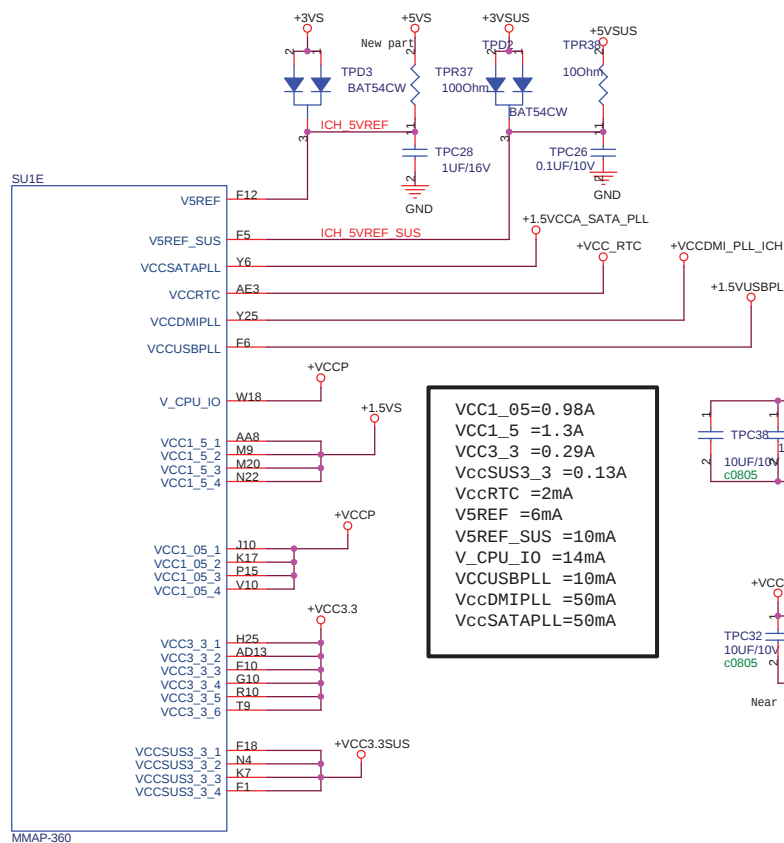


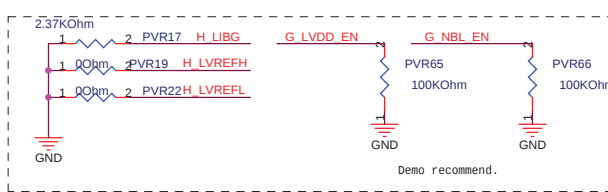
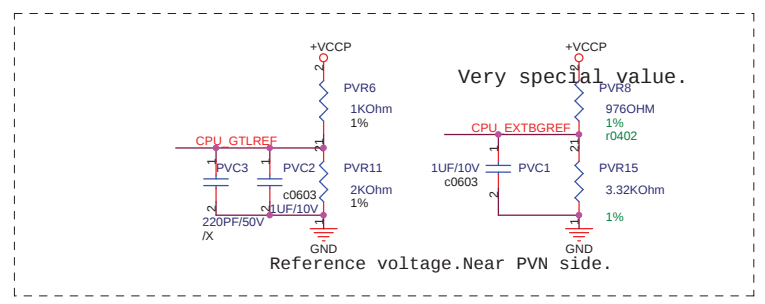
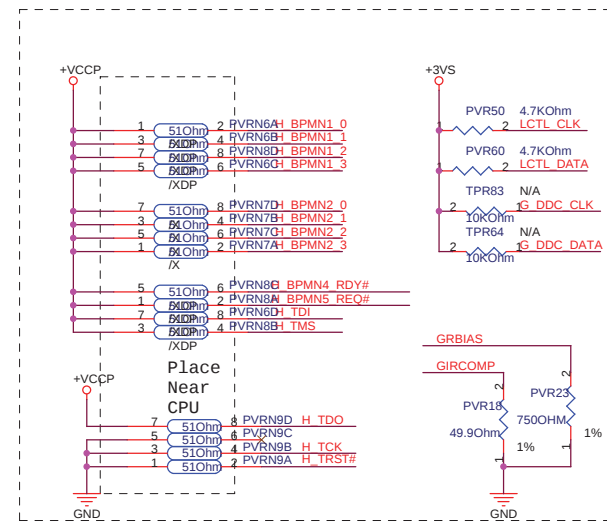
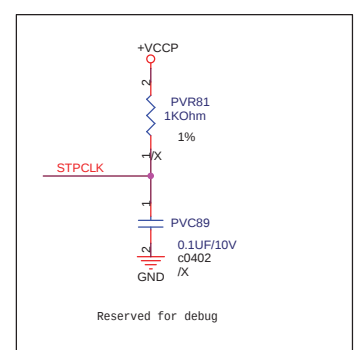
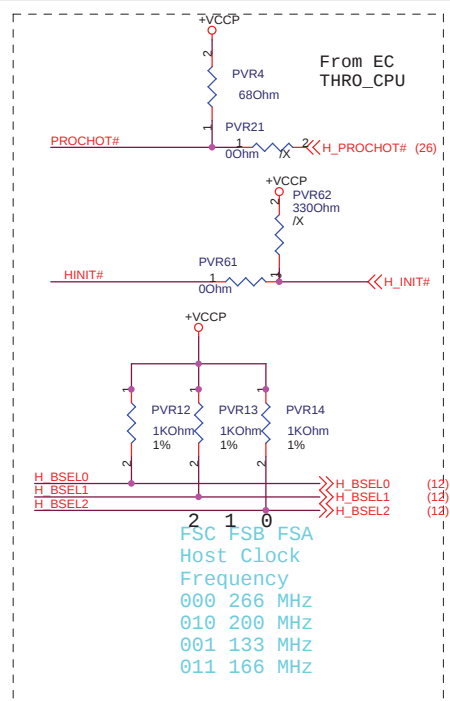
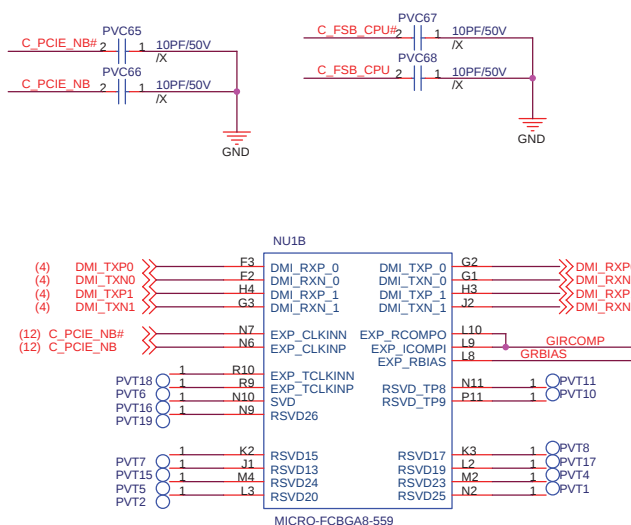
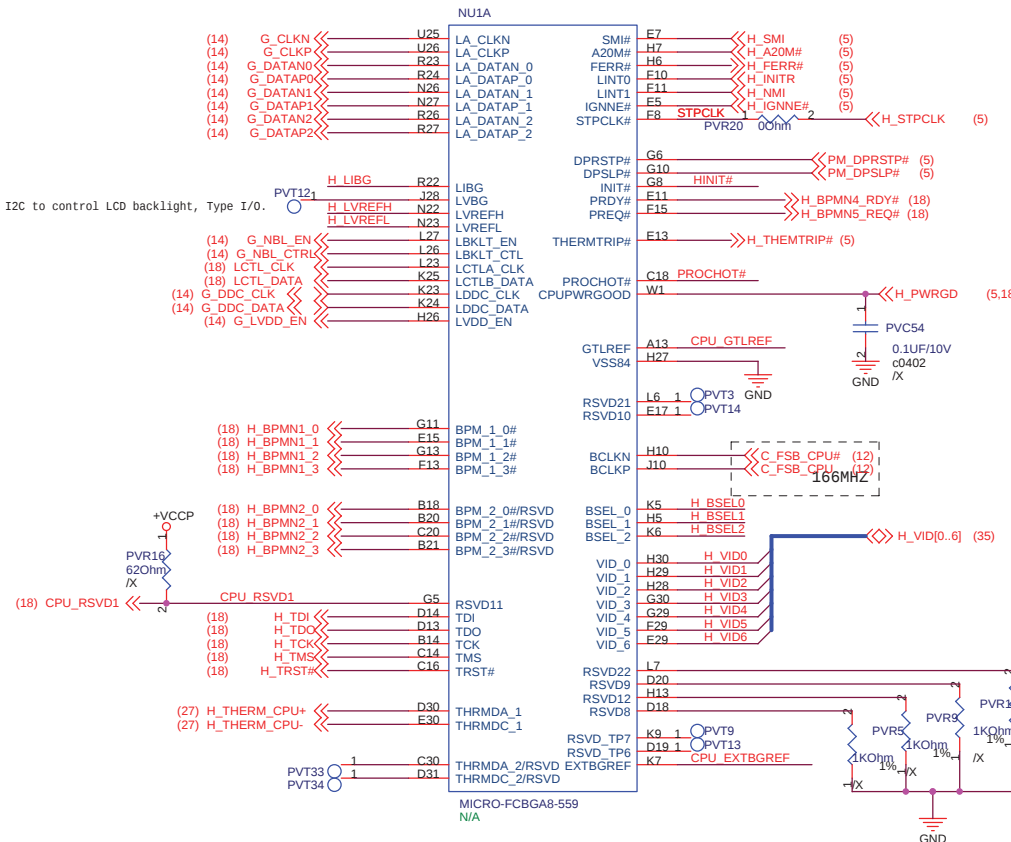
USB0	USB CONN
USB1	USB CONN
USB2	USB CONN
USB3	USB CONN
USB4	Camera
USB5	Card Reader
USB6	Blue tooth
USB7	3G



SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.







(10.11) D2_MAA[0..14] <<>

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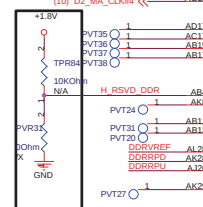
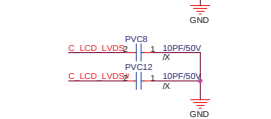
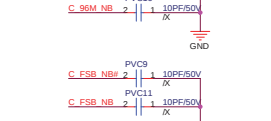
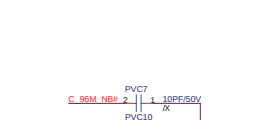
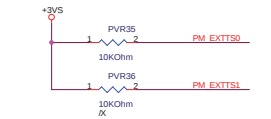
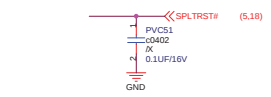
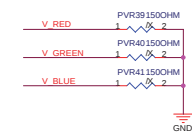
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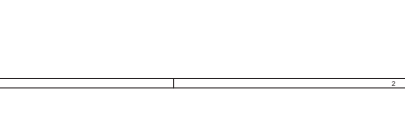
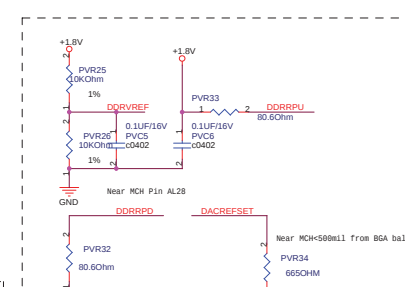
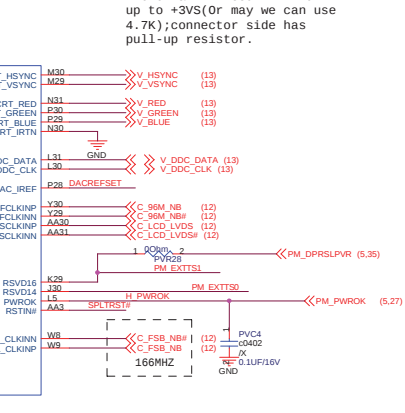
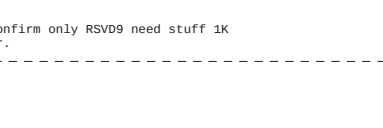
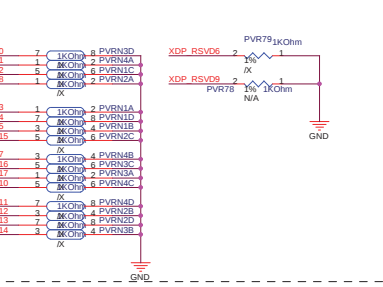
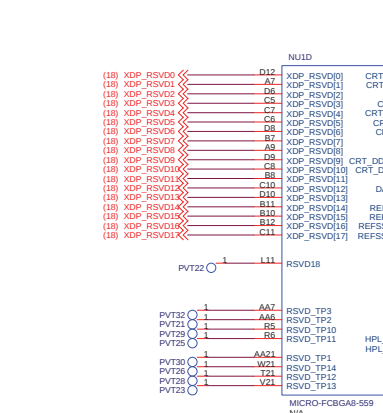
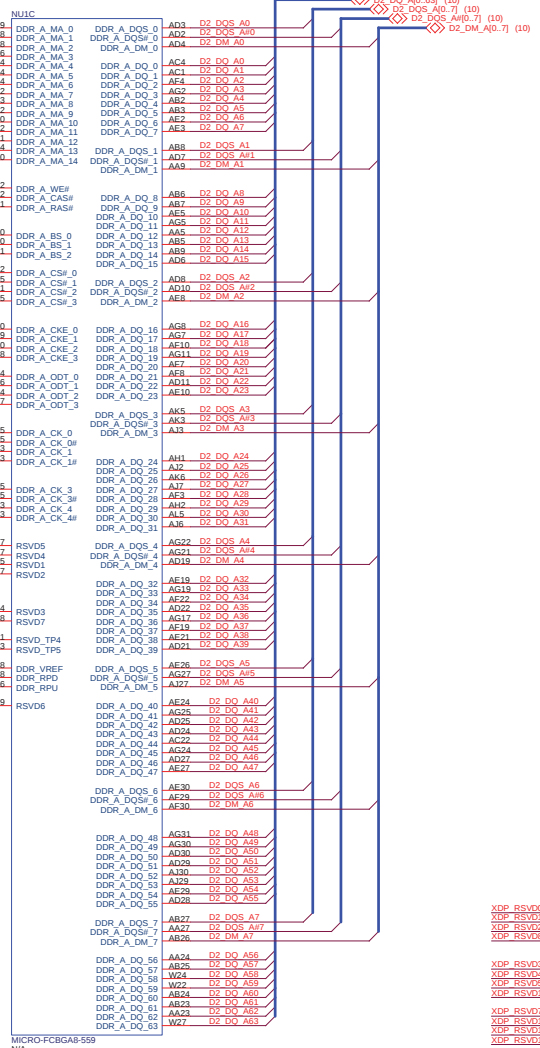
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DDC CLK&DATA need 2.2K Pull
up to +3VS(Or may we can use
4.7K);connector side has
pull-up resistor.



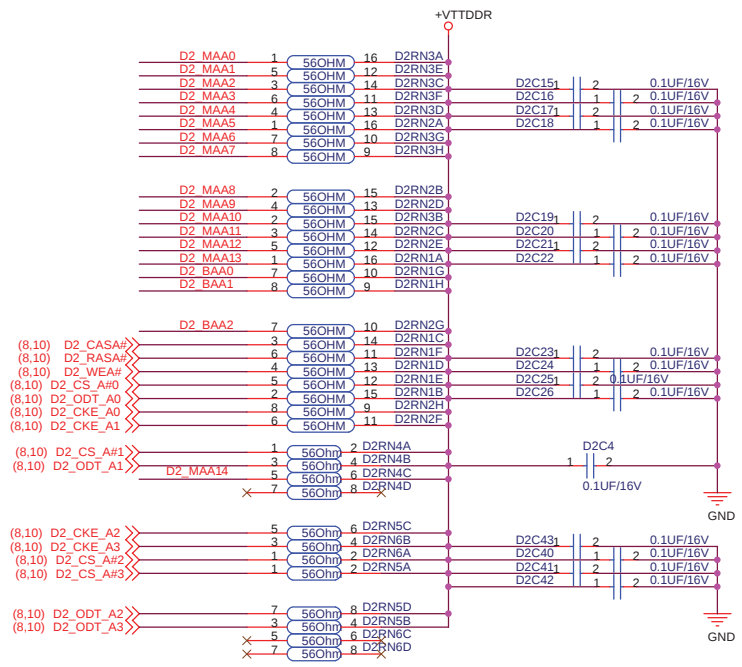
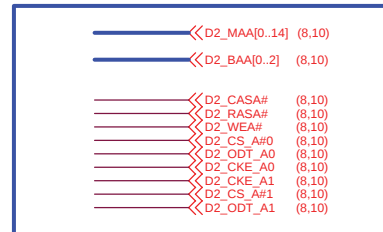
Pull up to 1.8V only for
A0 version ES sample,
later will be pulled down,
so later must N/A PVR31.

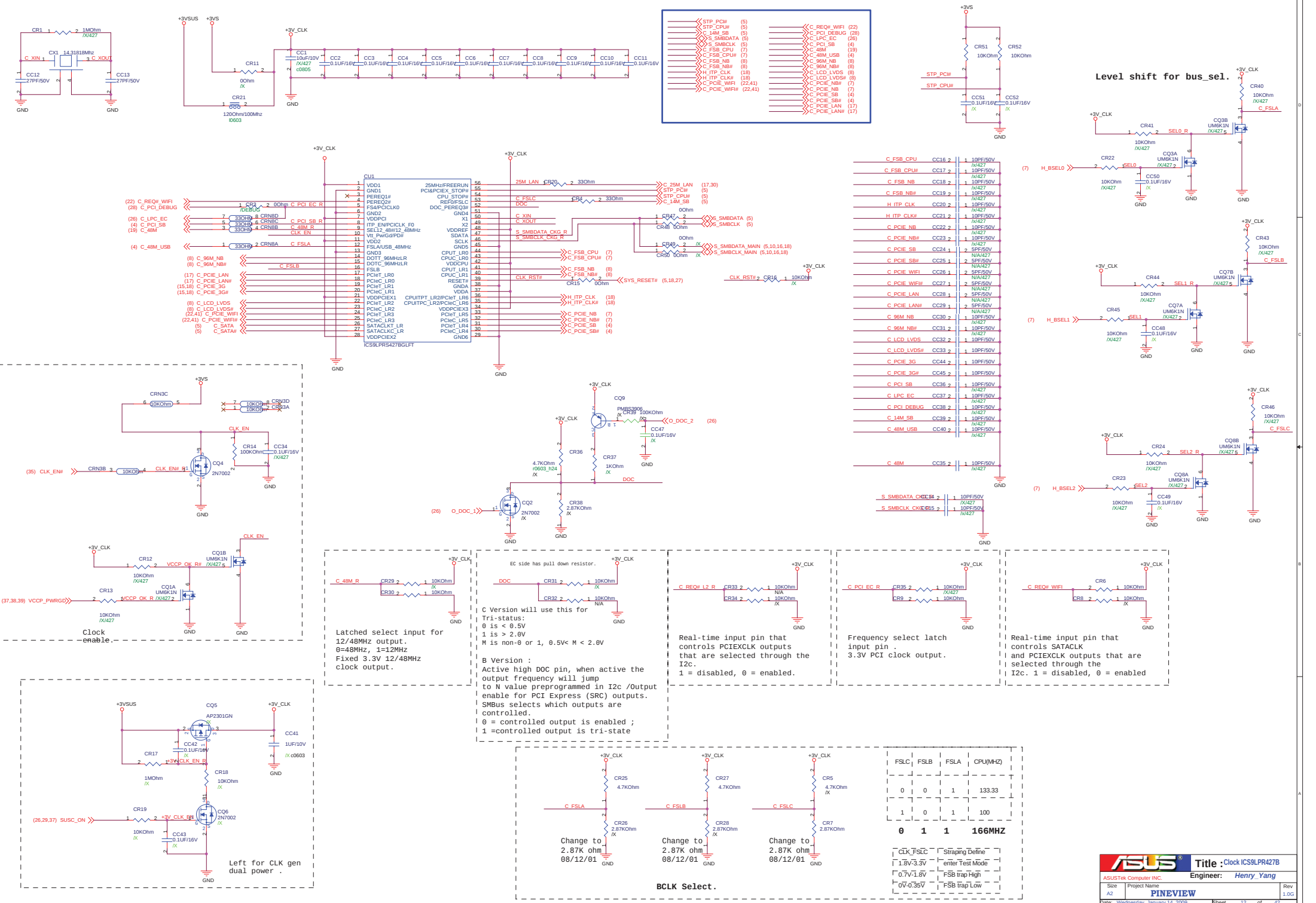


Intel confirm only RSDV9 need stuff 1K
resistor.



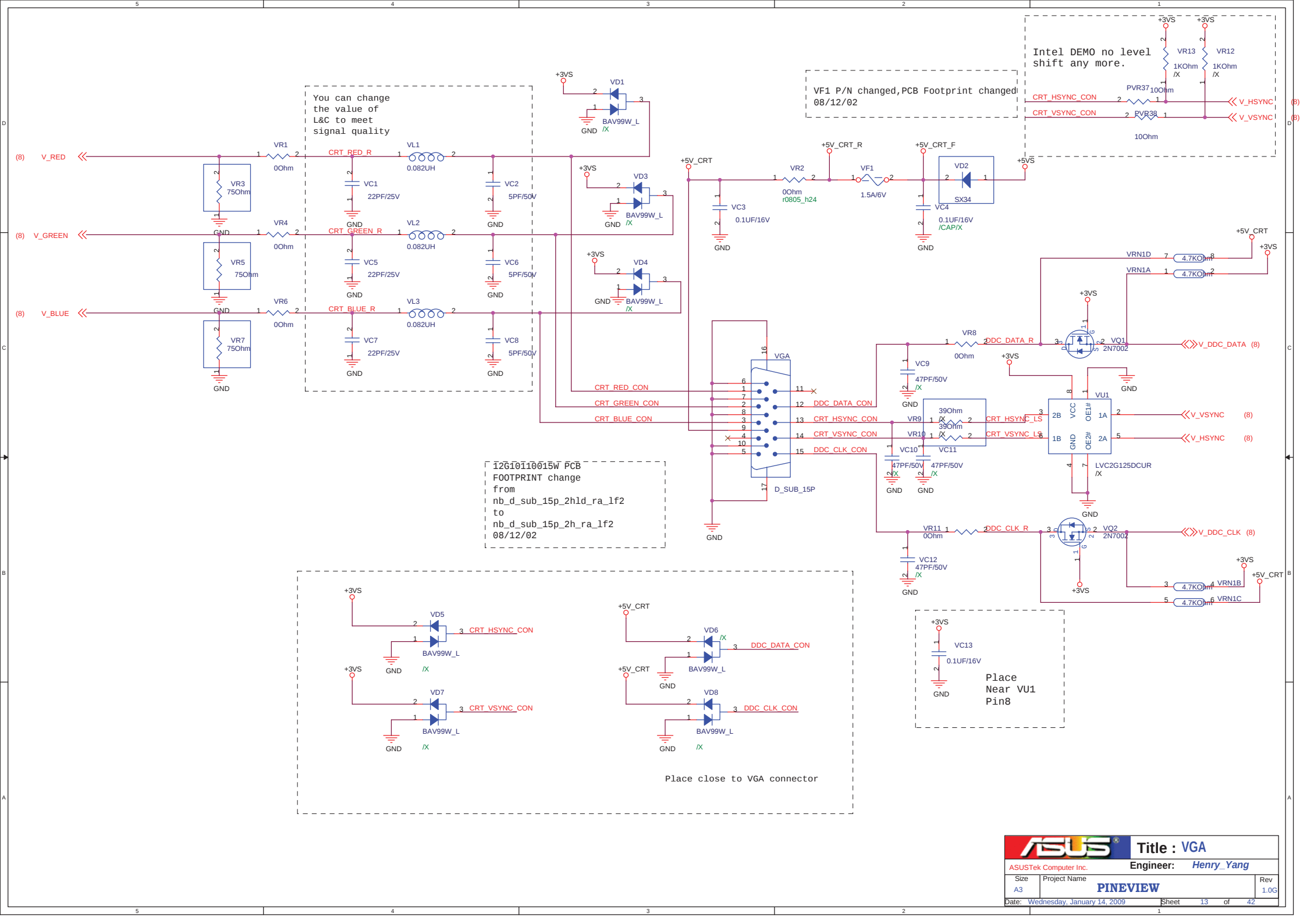






<< STP_PCW# (5)	<< C_REQ#_WIFI (22)
<< STP_CPU# (5)	<< C_PCI_DEBUG (28)
<< 14M_SB (5)	<< C_LPC_EC (30)
<< S_SMBDATA (5)	<< C_PCI_SB (4)
<< S_SMBCLK (5)	<< 48M (19)
<< FSB_CPU (7)	<< 48M_USB (6)
<< FSB_CPU# (7)	<< 48M_NB (6)
<< FSB_NB (8)	<< C_LCD_LVDS# (8)
<< FSB_NB# (8)	<< C_LCD_LVDS (8)
<< H_ITP_CLK (18)	<< C_PCIE_NB# (7)
<< H_ITP_CLK# (18)	<< C_PCIE_SB (4)
<< C_PCIE_WIF# (22,41)	<< C_PCIE_SB# (7)
<< C_PCIE_WIF# (22,41)	<< C_PCIE_LAN (17)
<< C_PCIE_WIF# (22,41)	<< C_PCIE_LAN# (17)

C_FSB_CPU#	CC16 2	1	10PF/50V	IX427
C_FSB_CPU#	CC17 2	1	10PF/50V	IX427
C_FSB_NB	CC18 2	1	10PF/50V	IX427
C_FSB_NB#	CC19 2	1	10PF/50V	IX427
H_ITP_CLK	CC20 2	1	10PF/50V	IX427
C_PCIE_NB#	CC21 2	1	10PF/50V	IX427
C_PCIE_NB	CC22 2	1	10PF/50V	IX427
C_PCIE_SB	CC24 1	2	5PF/50V	IX427
C_PCIE_SB#	CC25 1	2	5PF/50V	IX427
C_PCIE_WIF#	CC26 1	2	5PF/50V	IX427
C_PCIE_WIF#	CC27 1	2	5PF/50V	IX427
C_PCIE_LAN	CC28 1	2	5PF/50V	IX427
C_PCIE_LAN#	CC29 1	2	5PF/50V	IX427
C_96M_NB	CC30 2	1	10PF/50V	IX427
C_96M_NB#	CC31 2	1	10PF/50V	IX427
C_LCD_LVDS#	CC32 2	1	10PF/50V	IX427
C_PCIE_3G	CC44 2	1	10PF/50V	IX427
C_PCIE_3G#	CC45 2	1	10PF/50V	IX427
C_PCI_SB	CC36 2	1	10PF/50V	IX427
C_LPC_EC	CC37 2	1	10PF/50V	IX427
C_PCI_DEBUG	CC38 2	1	10PF/50V	IX427
C_14M_SB	CC39 2	1	10PF/50V	IX427
C_48M_USB	CC40 2	1	10PF/50V	IX427
S_SMBDATA_CHK#	CC41 2	1	10PF/50V	IX427
S_SMBCLK_CHK#	CC42 2	1	10PF/50V	IX427



You can change
the value of
L&C to meet
signal quality

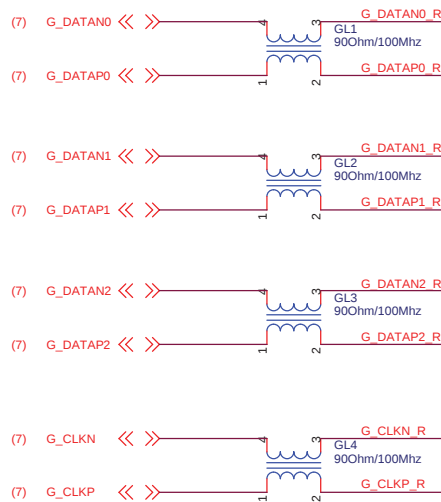
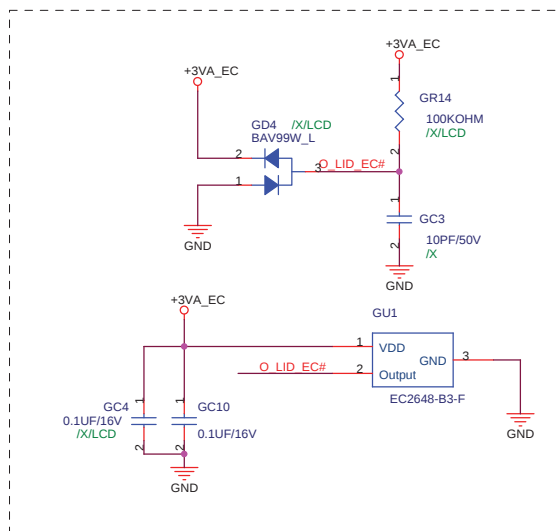
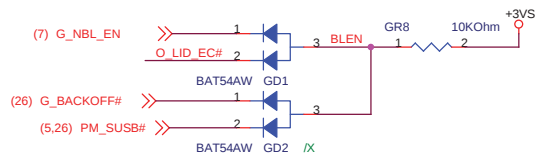
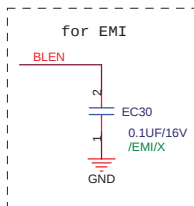
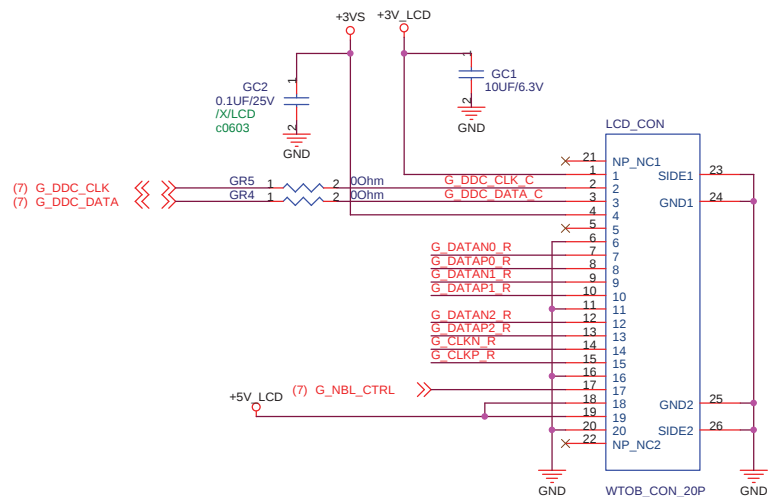
VF1 P/N changed,PCB Footprint changed
08/12/02

Intel DEMO no level
shift any more.

12G10110015W PCB
FOOTPRINT change
from
nb_d_sub_15p_2h1d_ra_1f2
to
nb_d_sub_15p_2h_ra_1f2
08/12/02

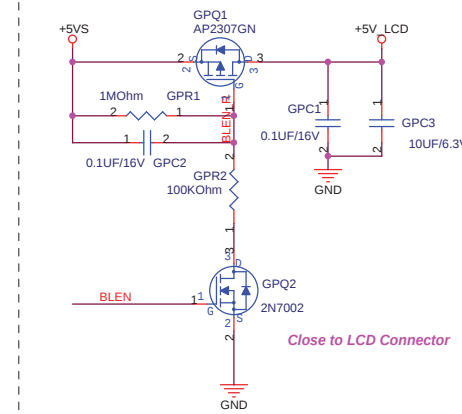
Place
Near VU1
Pin8

Place close to VGA connector

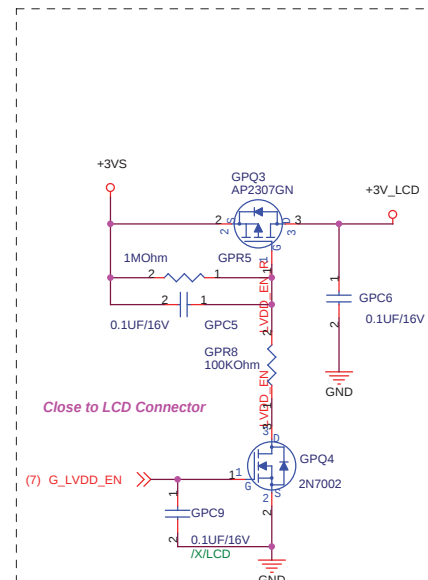


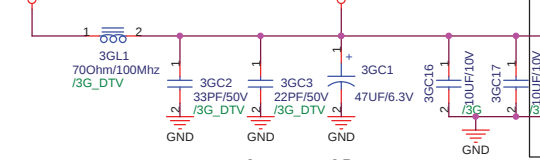
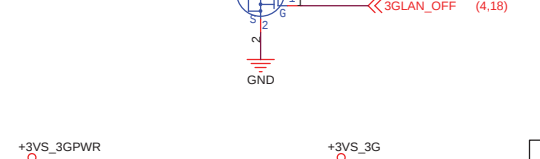
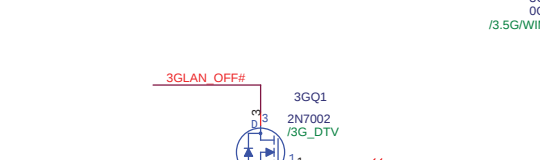
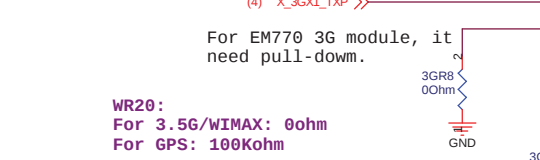
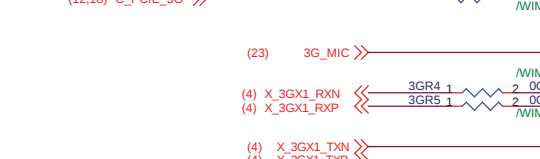
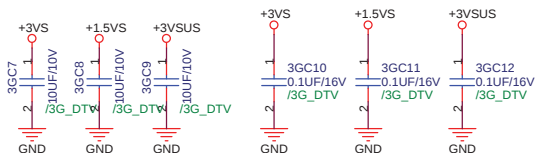
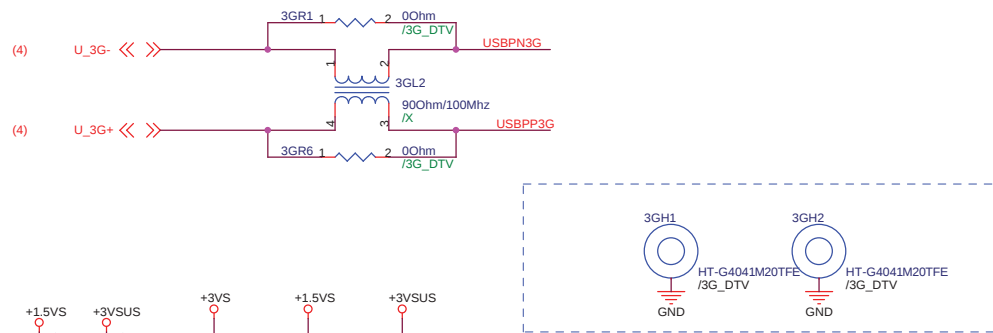
Add for RF request.

0.1 B Beta

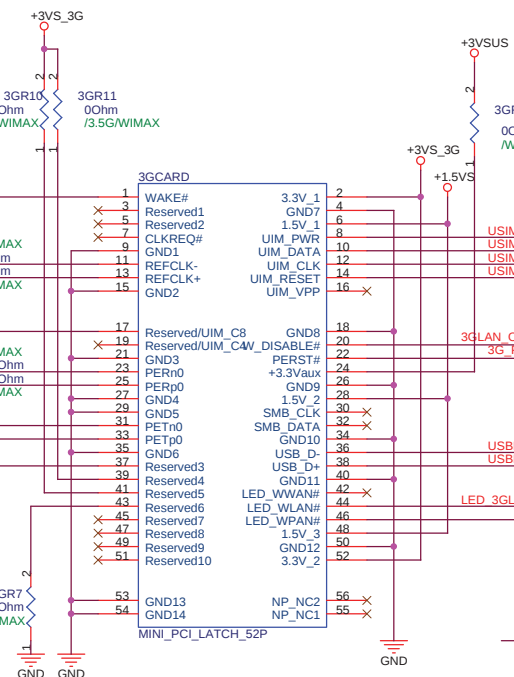


- (7) G_NBL_CTRL
- (7) G_CLKP
- (7) G_CLKN
- (7) G_DATAP2
- (7) G_DATAN2
- (7) G_DATA0
- (7) G_DATA1
- (7) G_DATA2
- (7) G_CLKN_R
- (7) G_CLKP_R
- (7) G_DDC_DATA
- (7) G_DDC_CLK
- (7) G_NBL_EN
- (26) G_BACKOFF#
- (26,27) O_LID_EC#

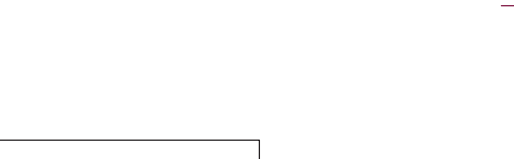




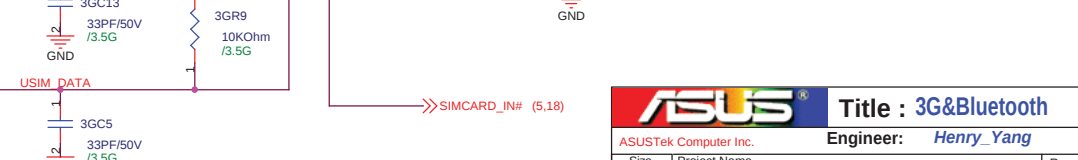
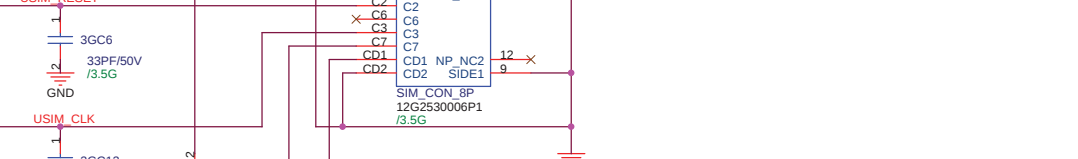
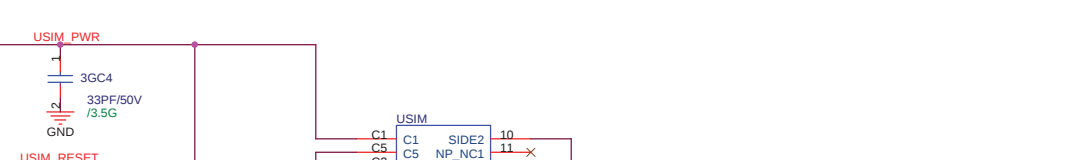
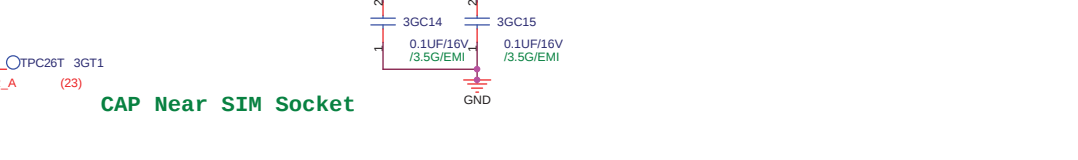
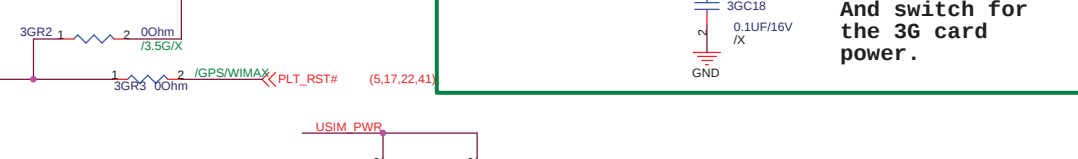
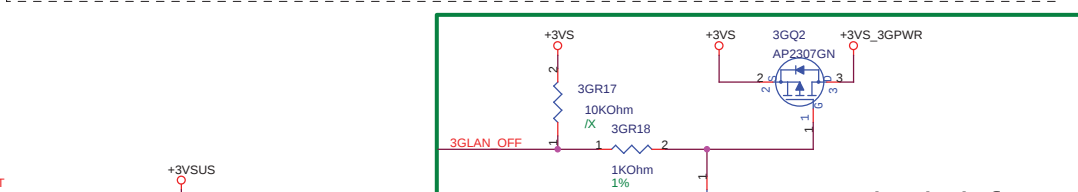
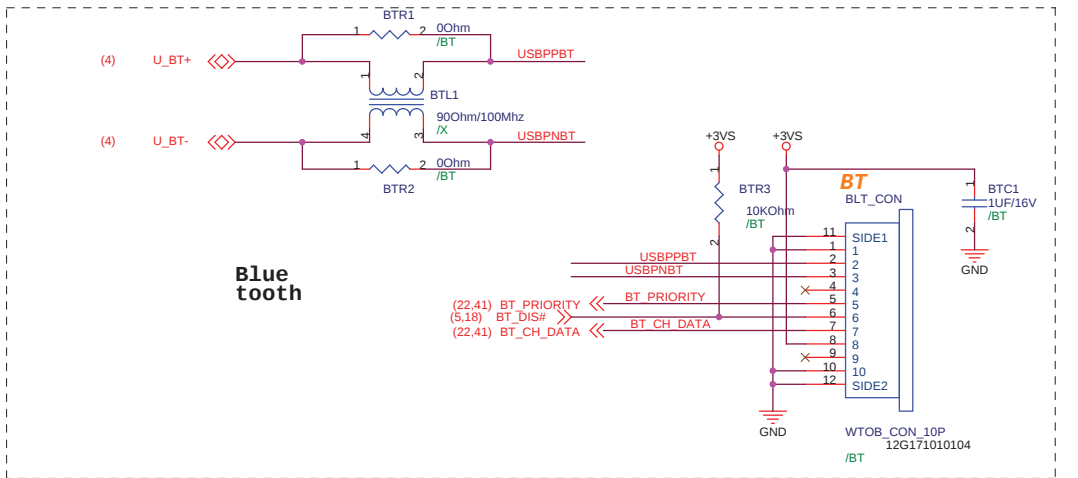
Power trace must be 30mils or more!!!



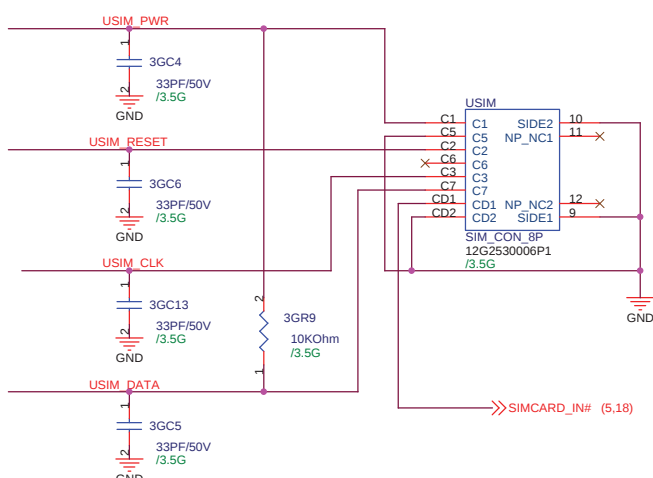
3G CARD use 12603010052L



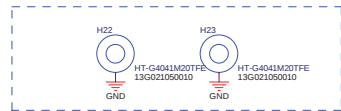
Add CAP for RF request



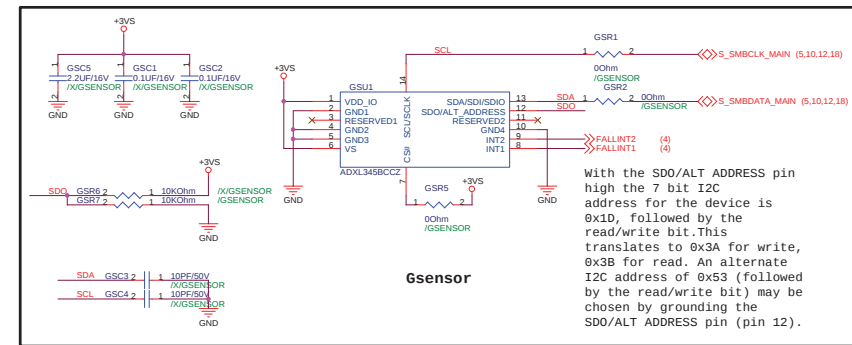
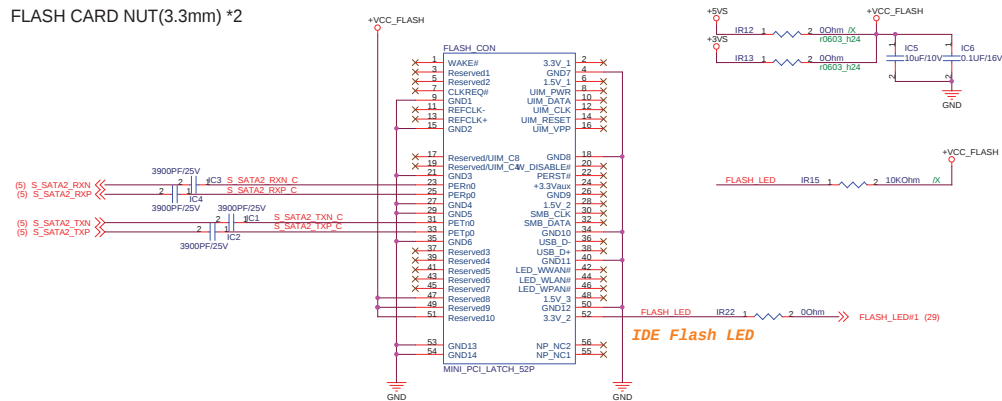
And switch for the 3G card power.



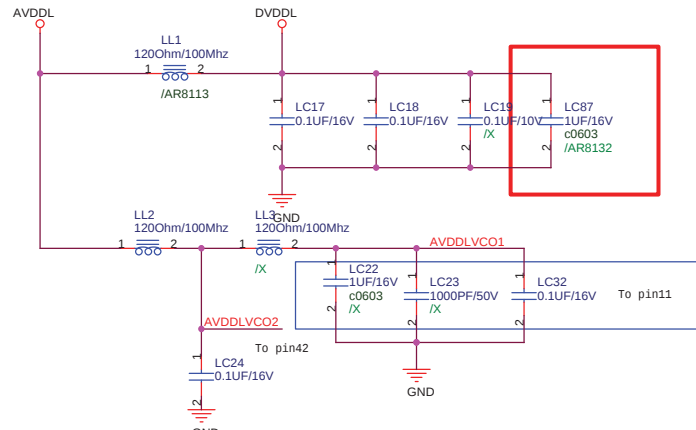
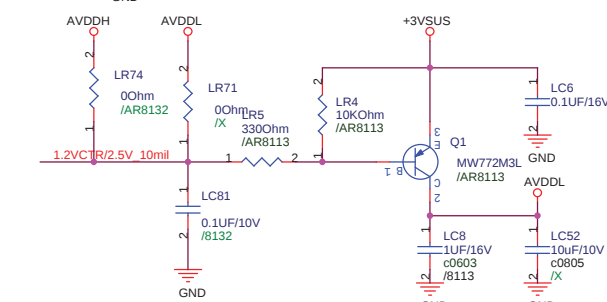
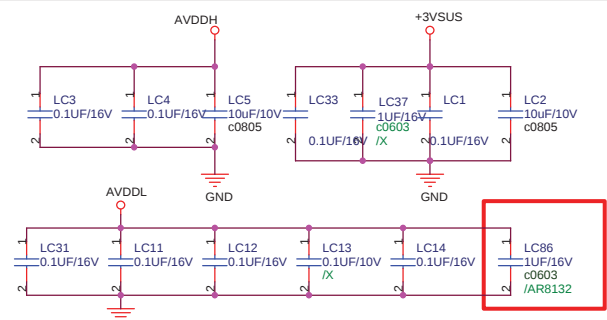
SATA HDD Connector



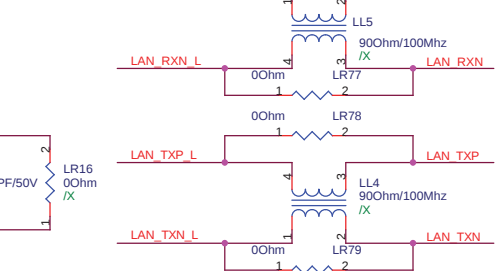
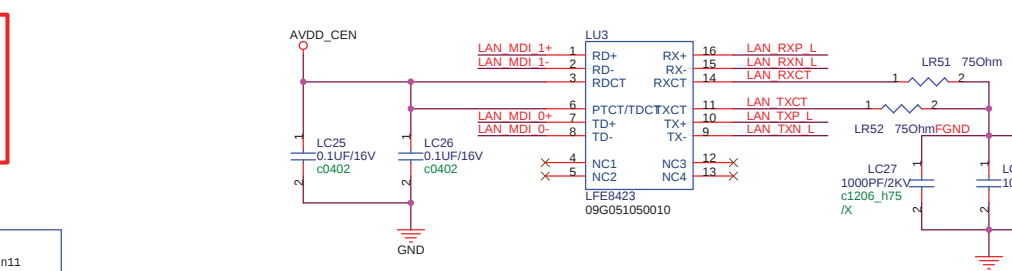
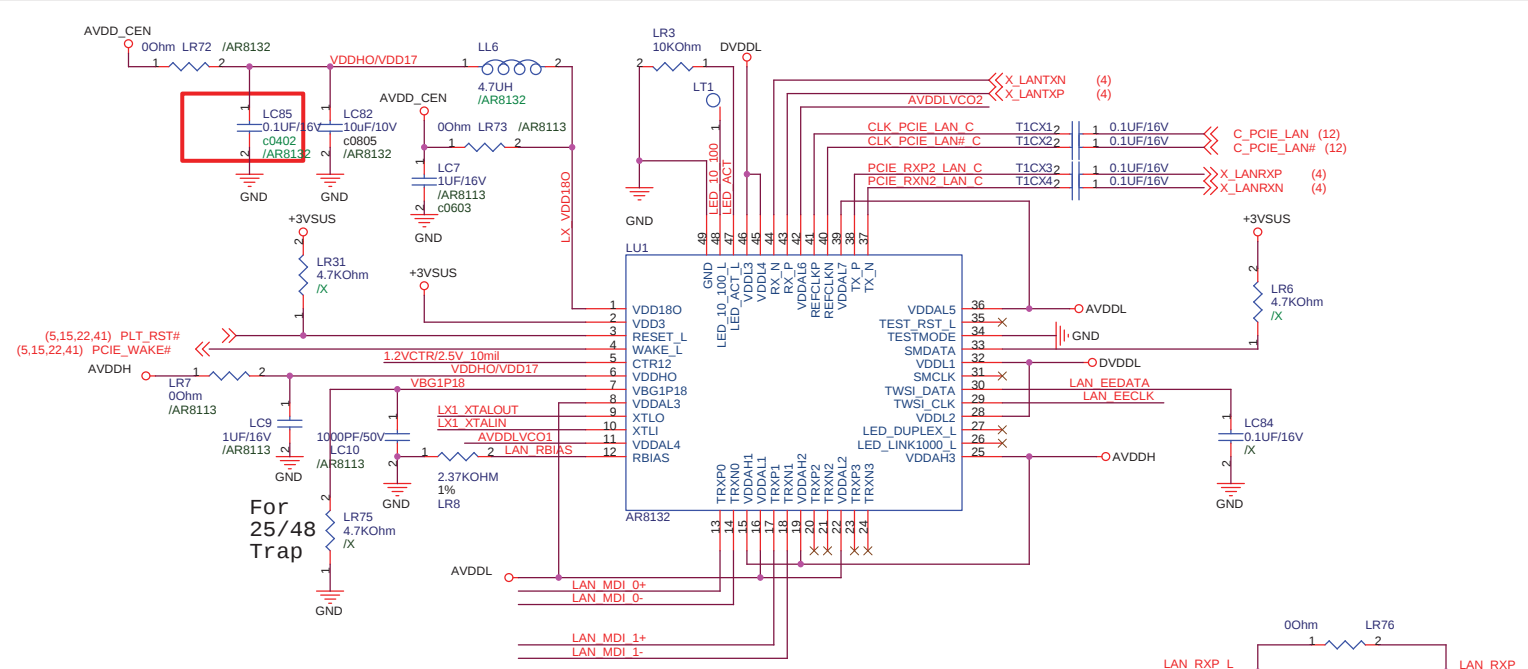
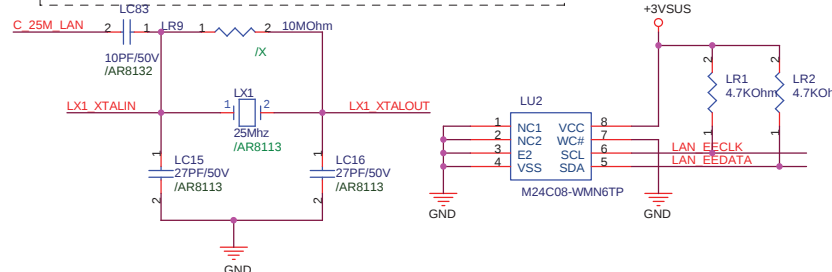
FLASH CARD NUT(3.3mm) *2



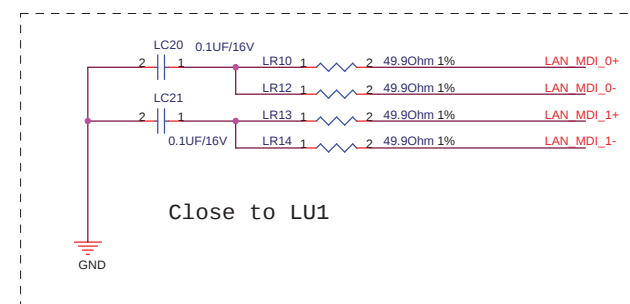
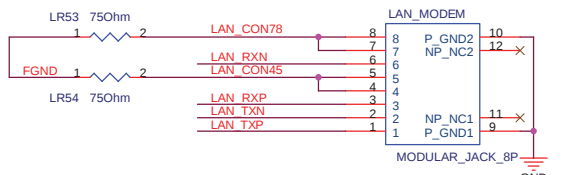
With the SDO/ALT ADDRESS pin high the 7 bit I2C address for the device is 0x1D, followed by the read/write bit. This translates to 0x3A for write, 0x3B for read. An alternate I2C address of 0x53 (followed by the read/write bit) may be chosen by grounding the SDO/ALT ADDRESS pin (pin 12).

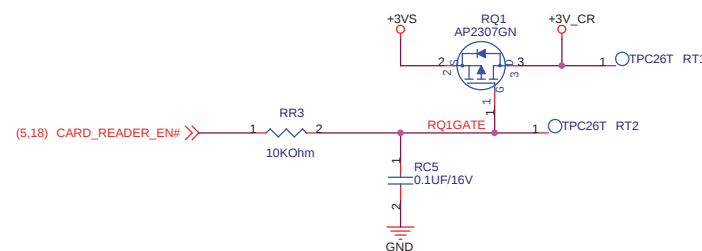
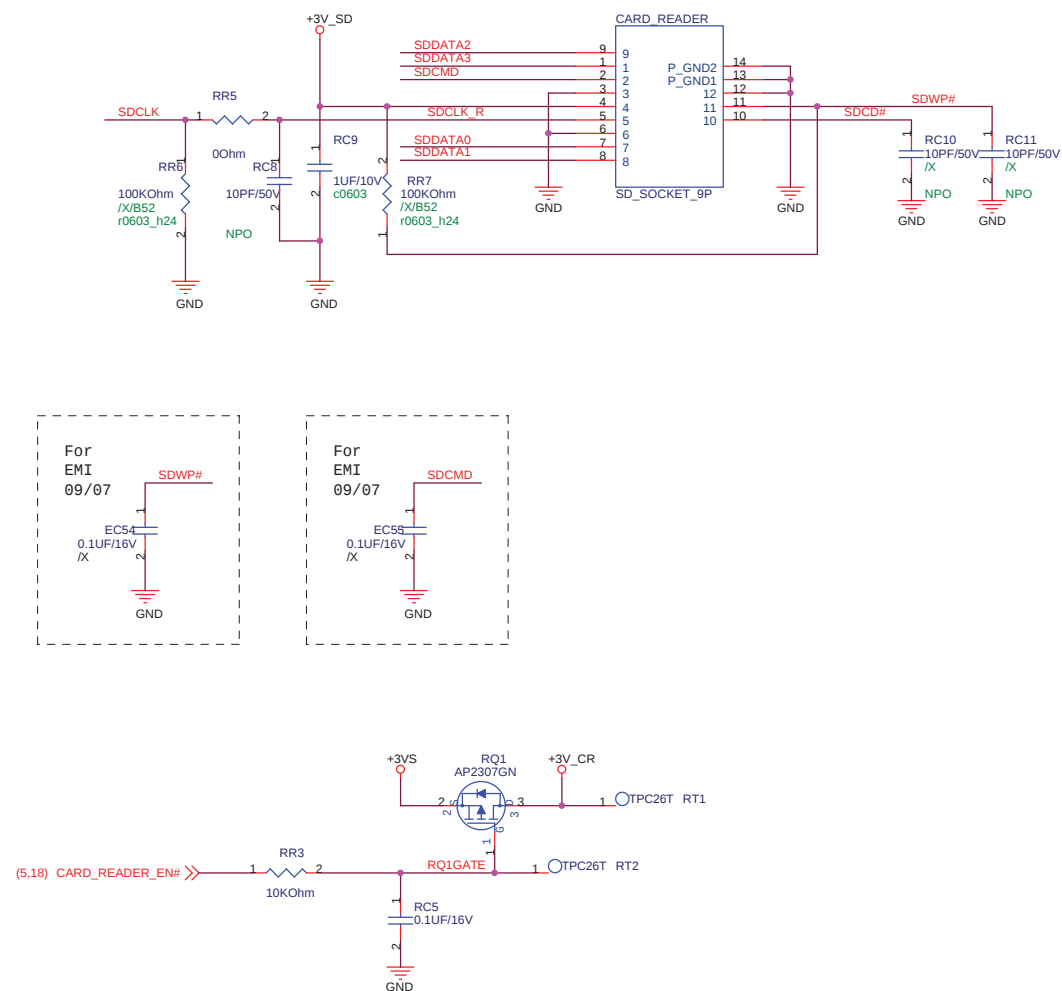


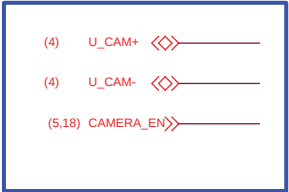
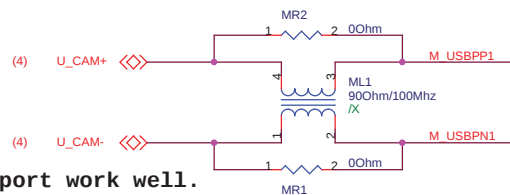
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept



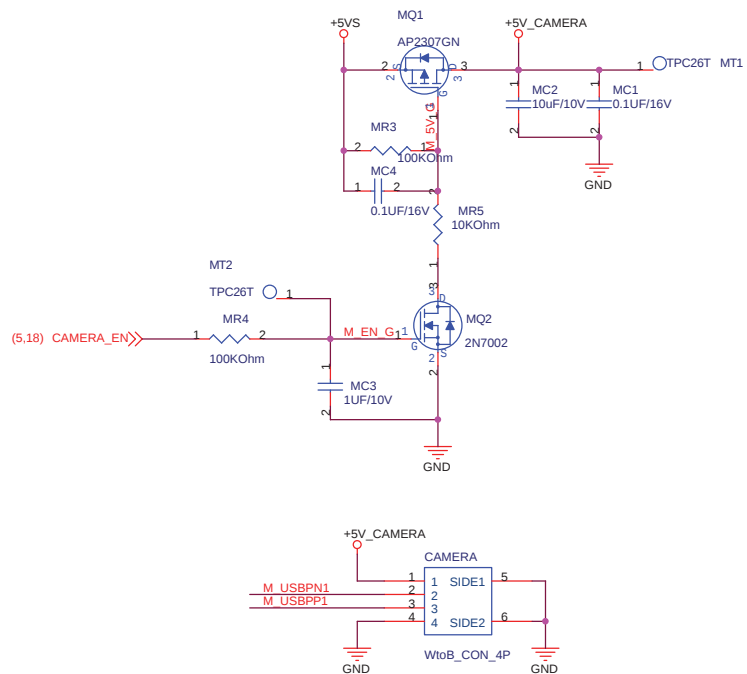
LAN connector: 12G148301086

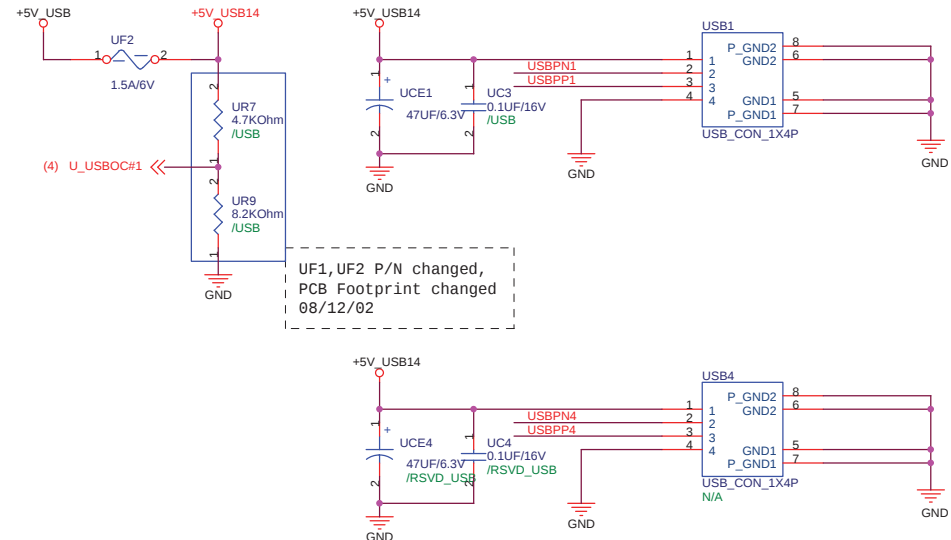
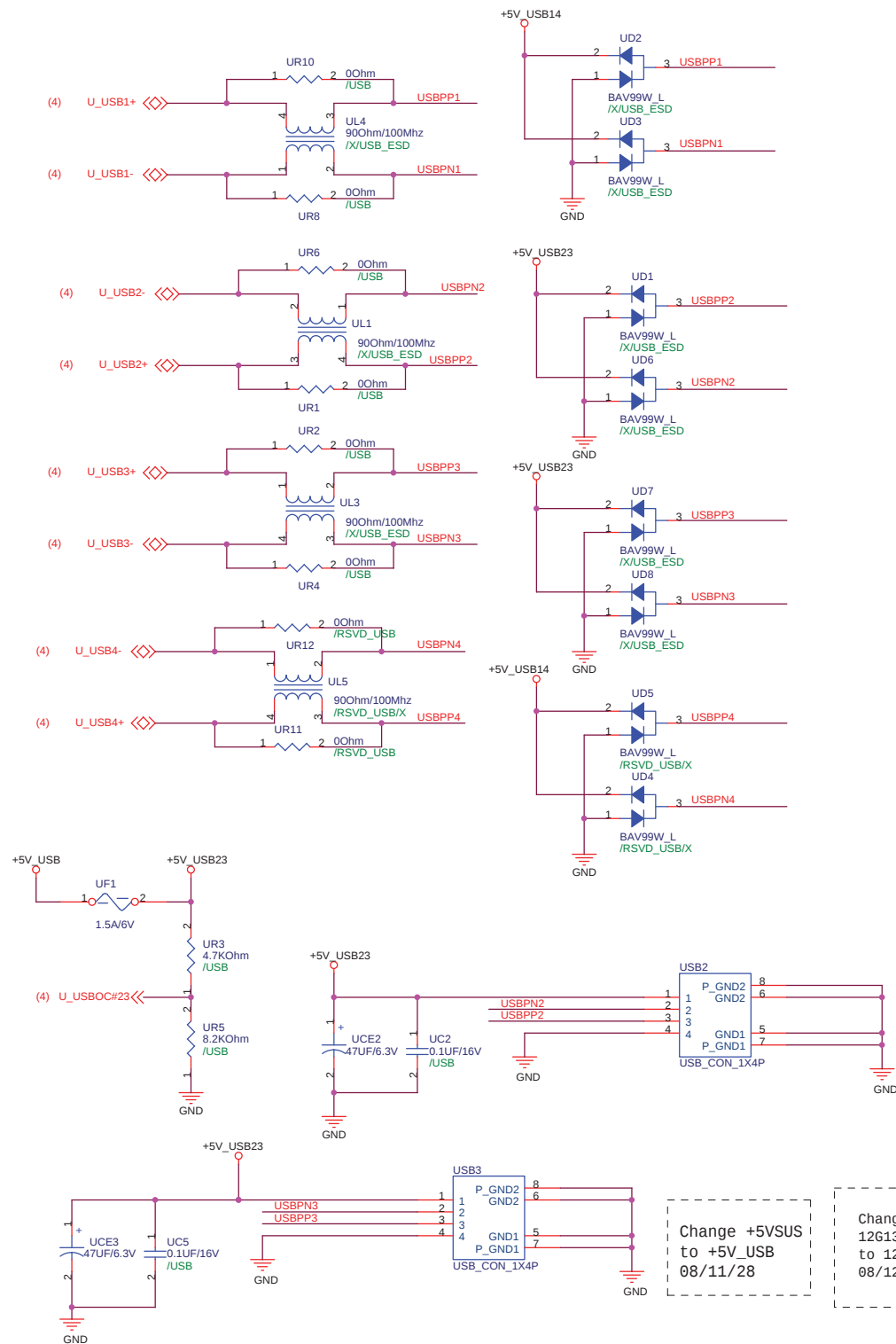






For check if the USB port work well.

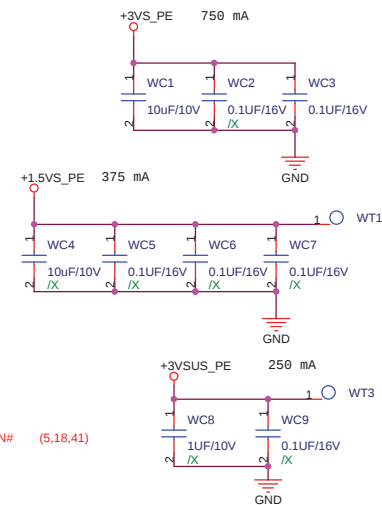
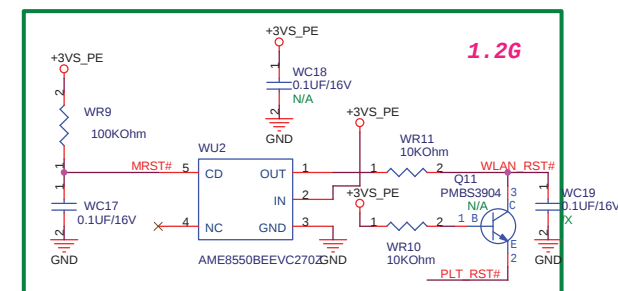
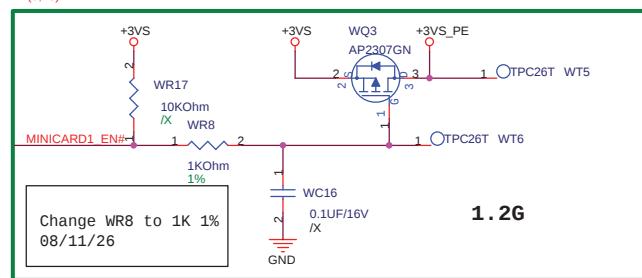


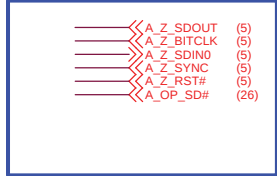


UF1,UF2 P/N changed,
PCB Footprint changed
08/12/02

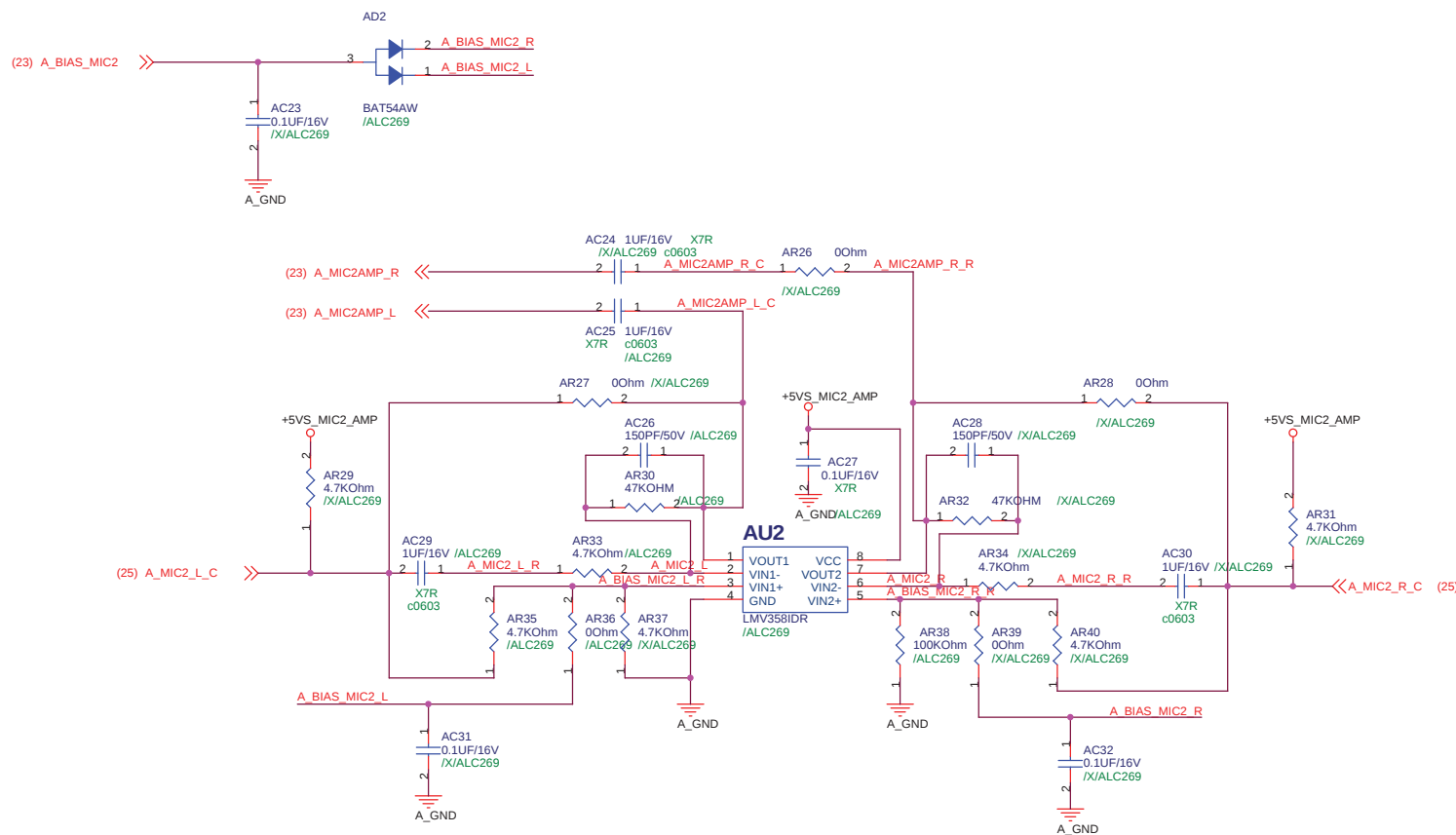
Change +5VSUS
to +5V_USB
08/11/28

Change USB CON P/N from
12G130011045
to 12G131030042
08/12/02



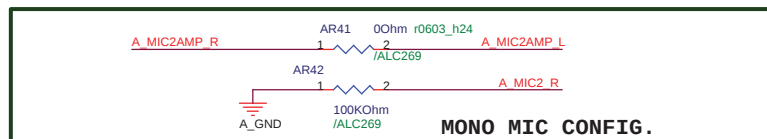


0.1ABeta

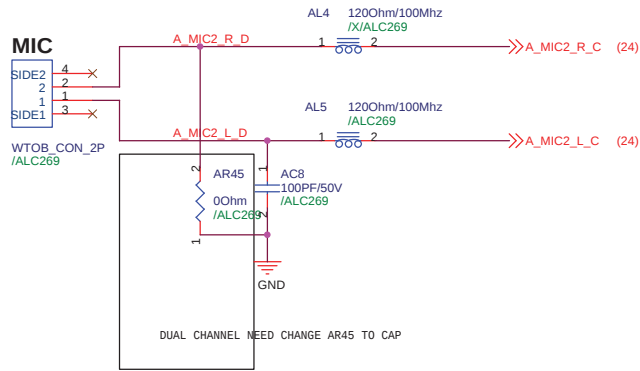


Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz



Internal MIC

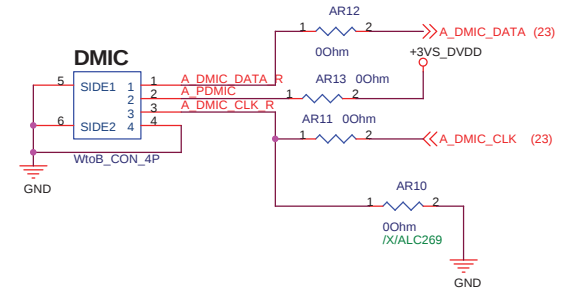
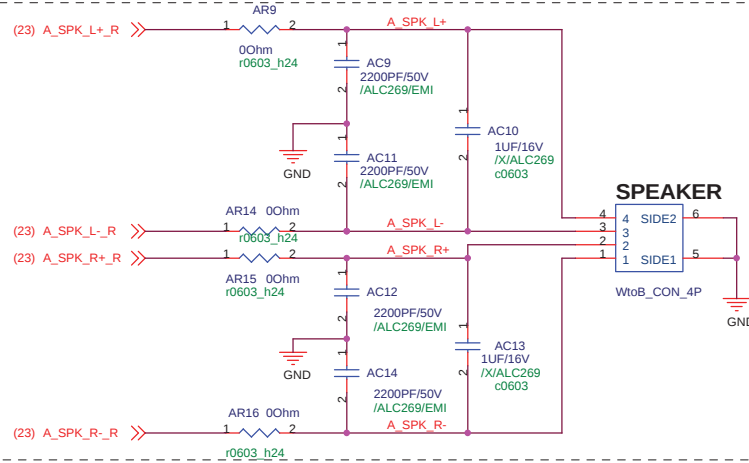


Change AR21,AR22 to 1K 1%
08/11/26

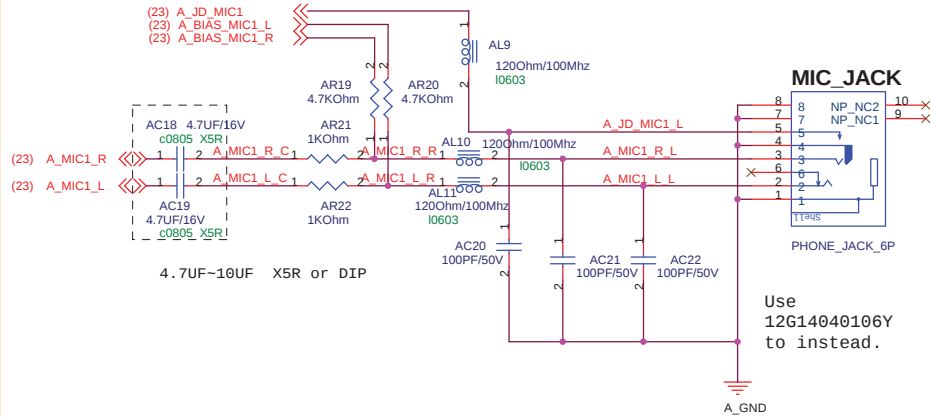
SPEAKER

Demodulation Filter
Placement near
Audio Codec

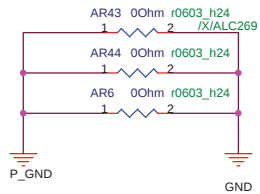
<<Attention>>
you can use LC filter(AR9,AR14,AR15,AR16
mount 8.2uH L ;and mount AC10,AC13) to
eliminate the EMI(please don't use
general beads,because they may influence
the THD+N quality) , AC9/AC11/AC12/AC14
are reserved for EMI fine-tune ; For EMI
issue, All L and C should near to codec



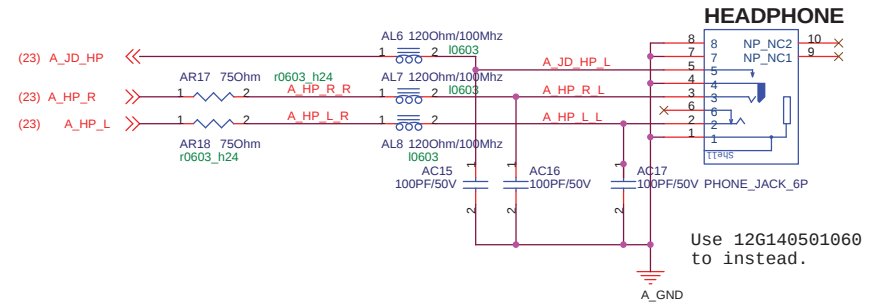
MIC JACK



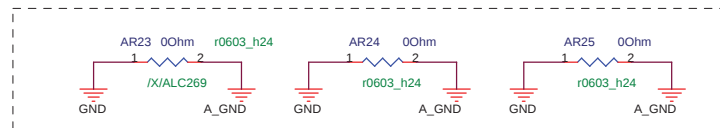
Use
12G14040106Y
to instead.



HEADPHONE

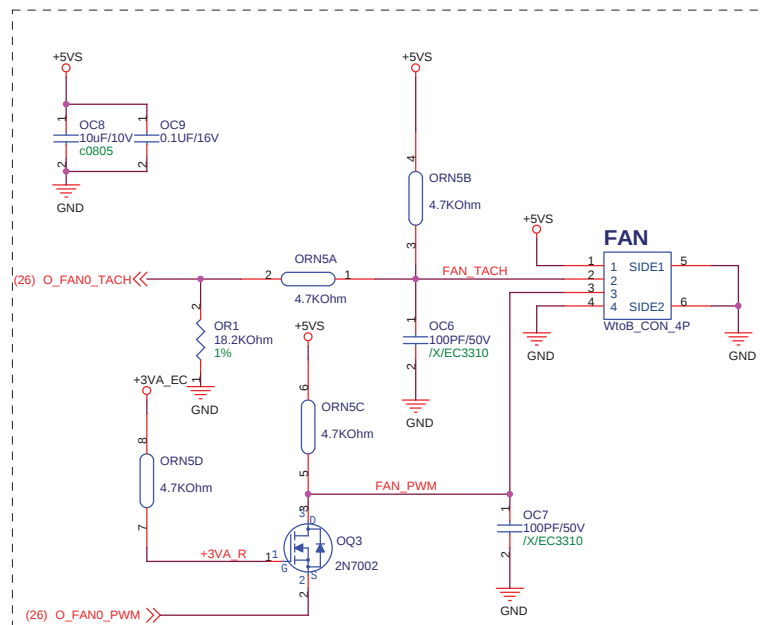
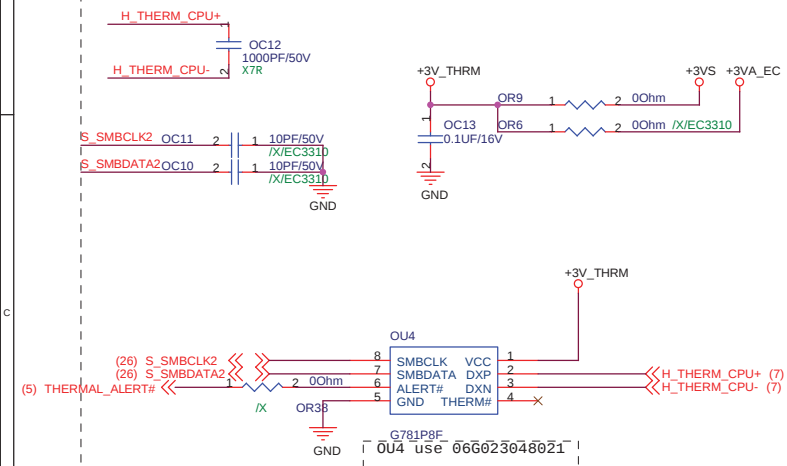


Use 12G140501060
to instead.



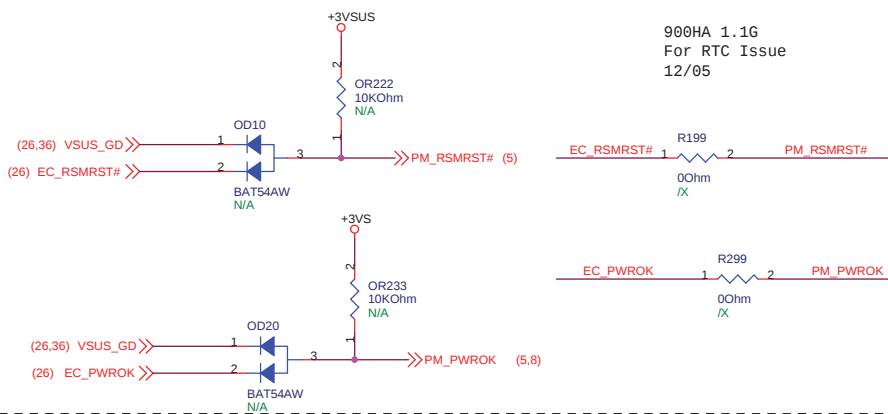
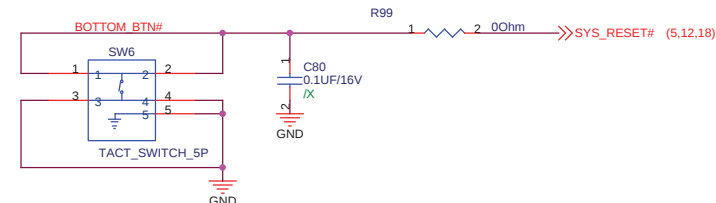
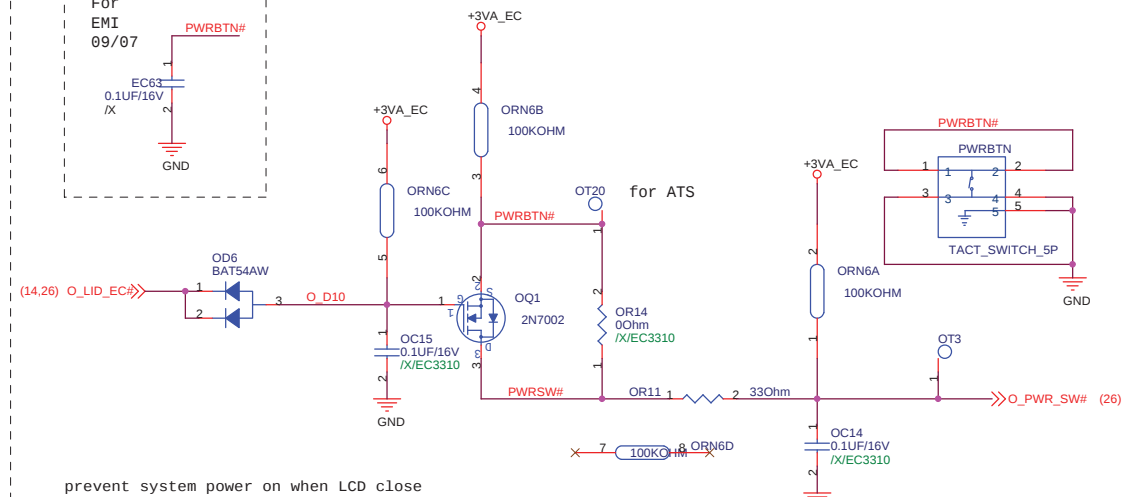
AR24, AR25 can use
0.1UF 11G233310432320
for EMI

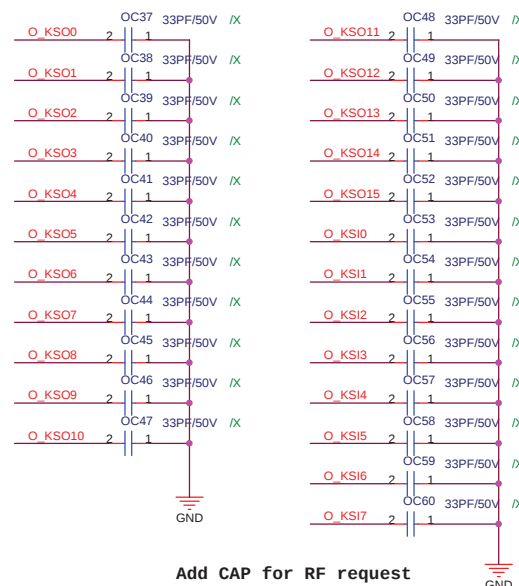
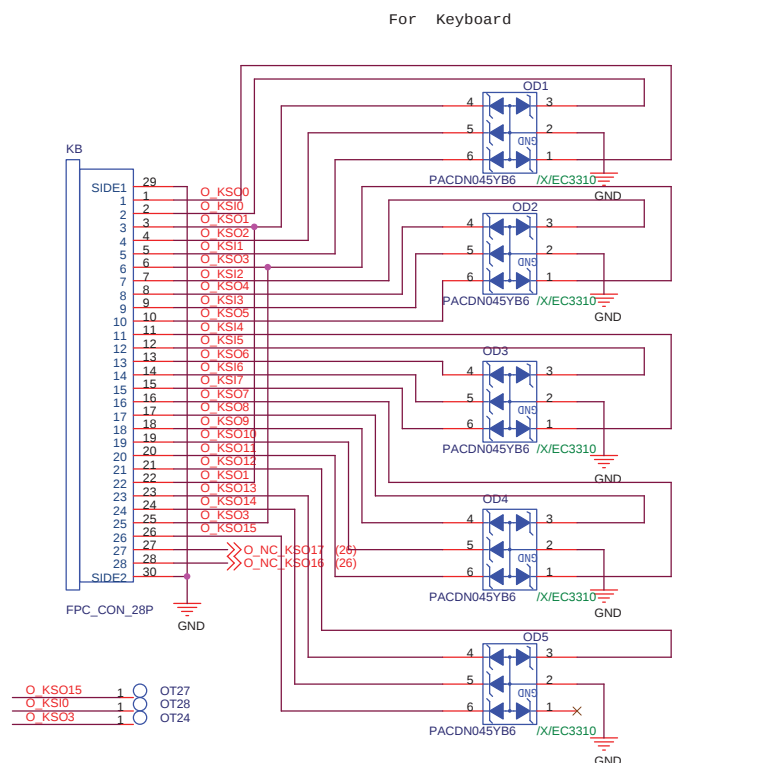
Remove Force_off
function
08/11/28



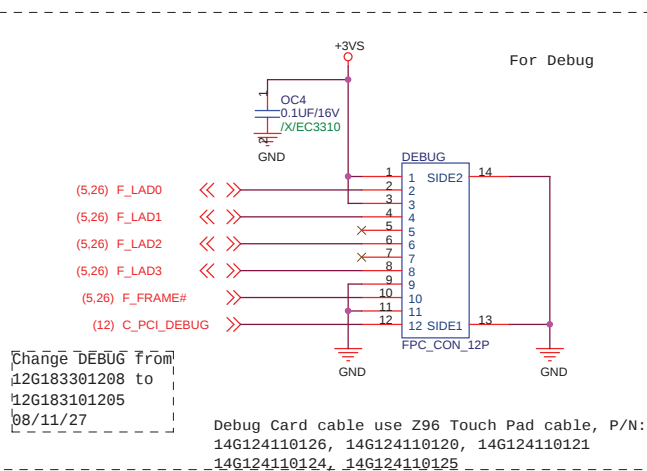
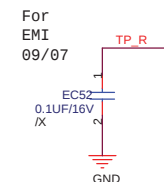
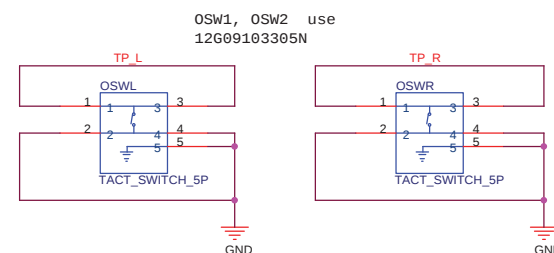
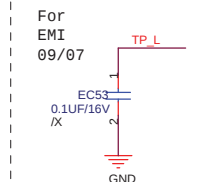
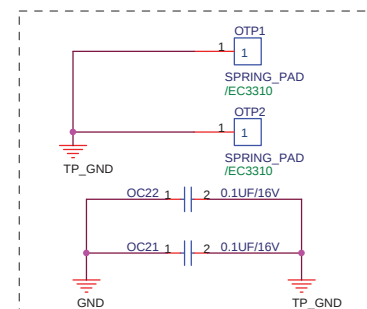
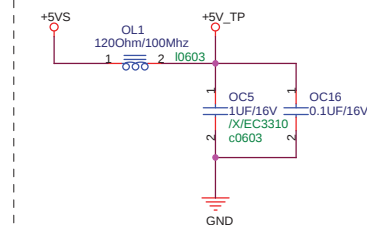
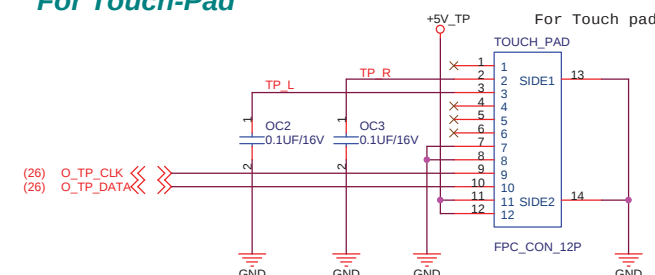
For
EMI
09/07

The diagram shows a circuit connection for EMI suppression. A capacitor, labeled EC63 with specifications 0.1uF/16V, is connected between the PWRBTN# signal line and the GND (ground) plane. The capacitor is represented by two parallel blue lines. The PWRBTN# line is shown in red, and the ground connection is also in red with a standard ground symbol.





Add CAP for RF request



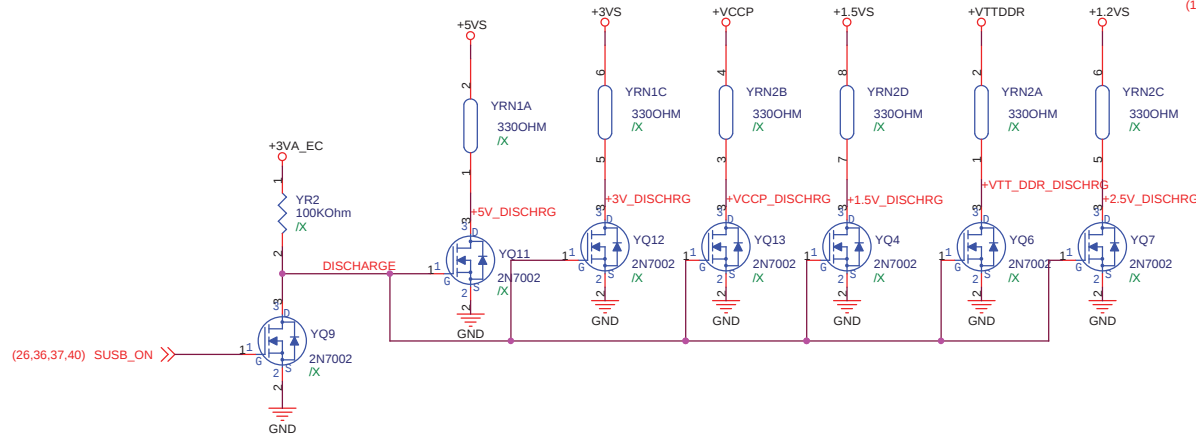
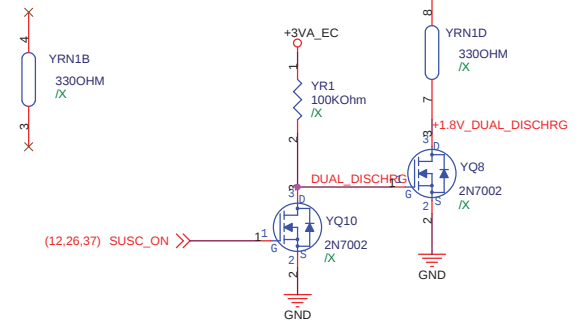
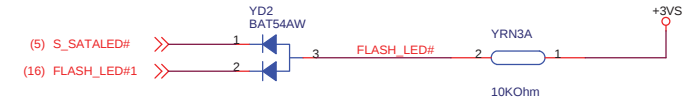
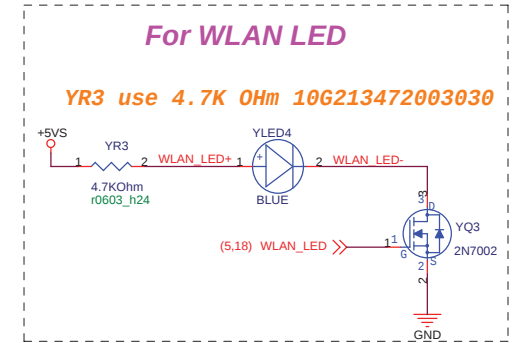
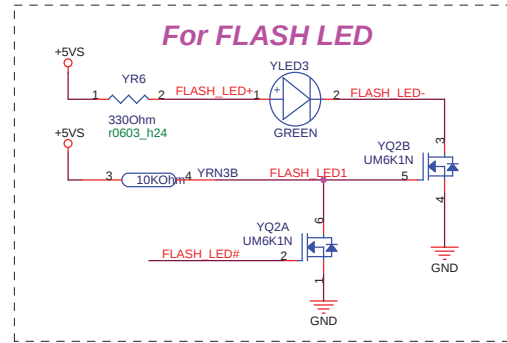
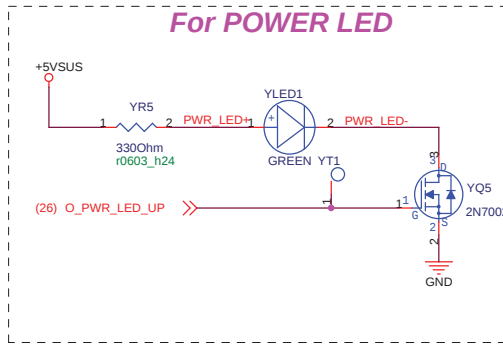
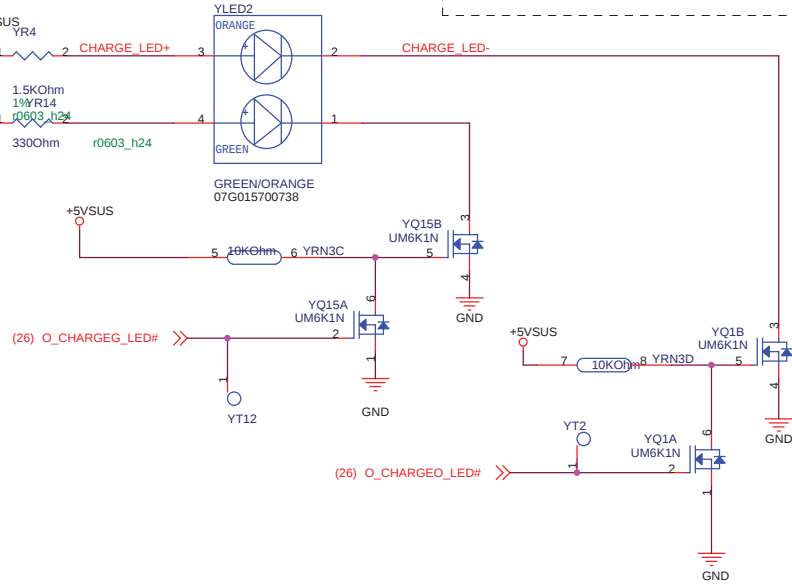
For CHARGE LED

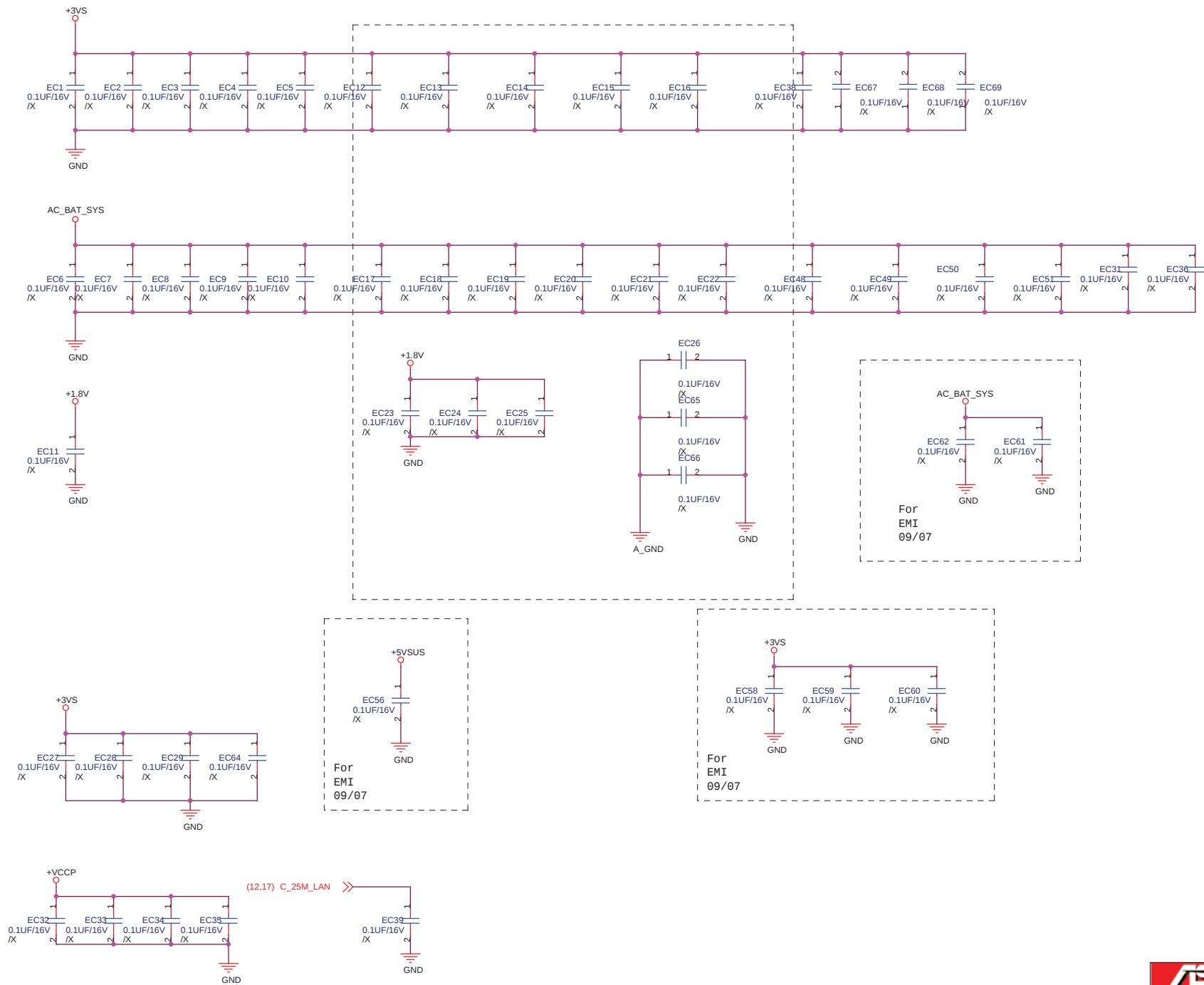
For POWER LED

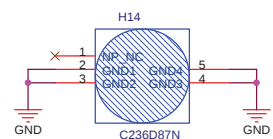
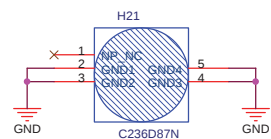
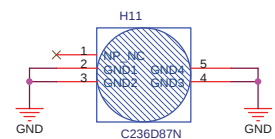
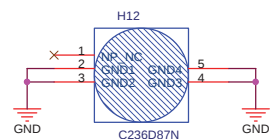
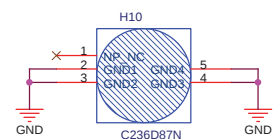
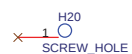
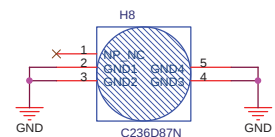
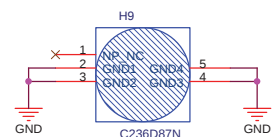
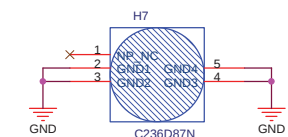
For FLASH LED

For WLAN LED

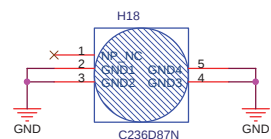
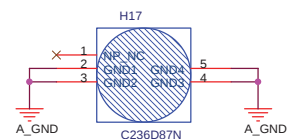
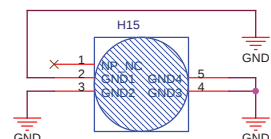
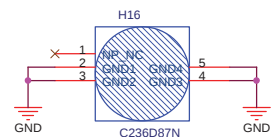
YR3 use 4.7K 0Hm 10G213472003030



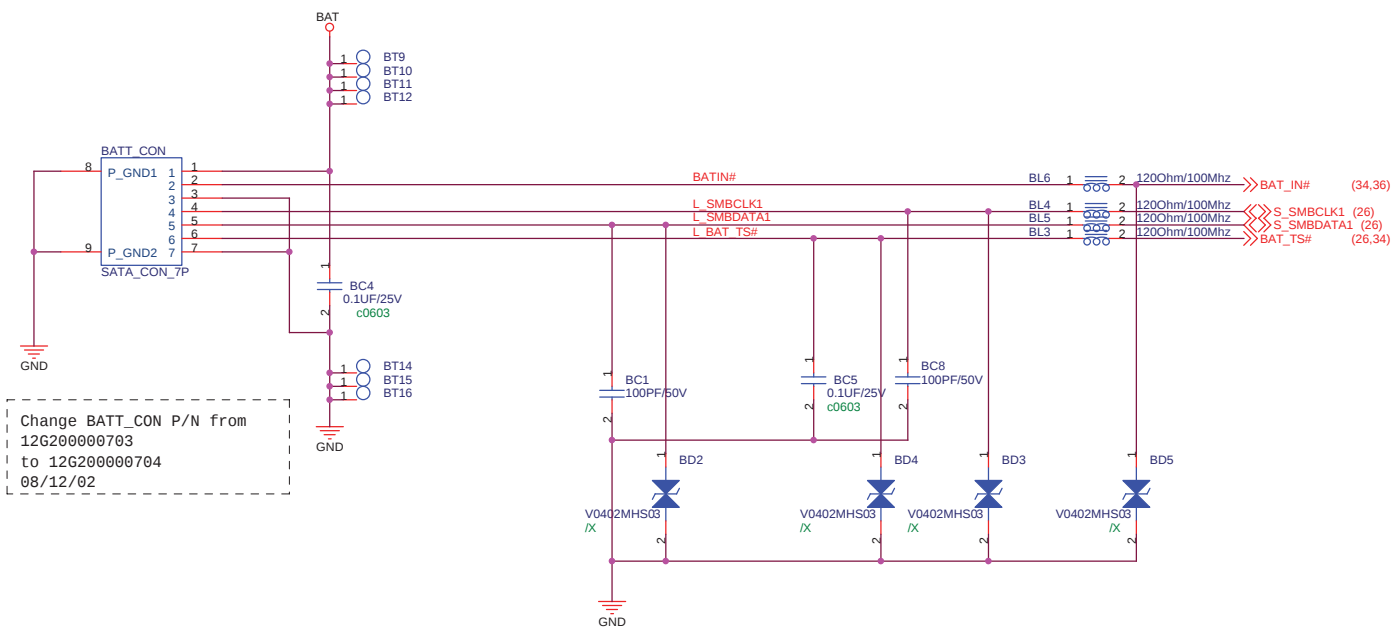
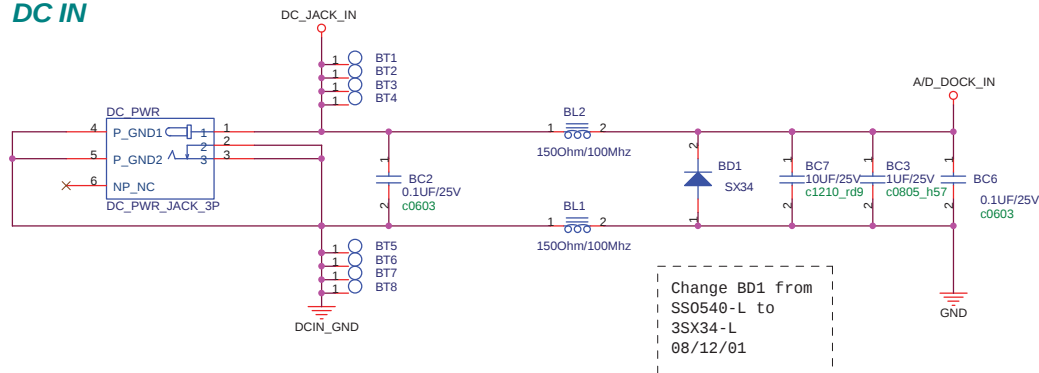


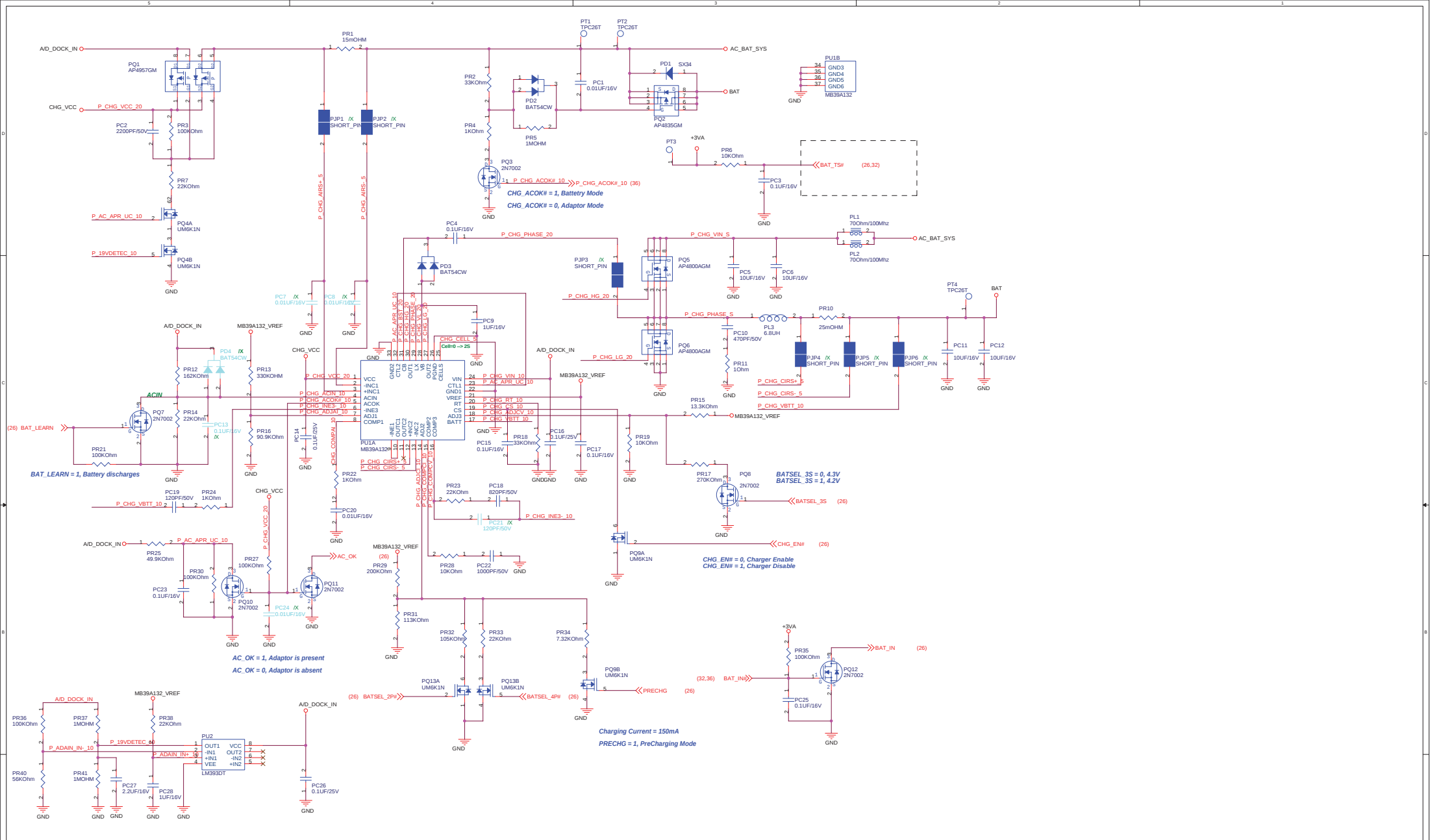


Due to 900PV cut a piece of PCB for bluetooth, so we has removed the H13.



DC IN





Battery Charging Voltage : Vadj3 > 4.1V ==> Vbat = 4.2V /cell 2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell Battery Charging Current : 4.4V > Vadj2 >= 0V ==> Ichg = (Vadj2-0.075)/(25*Rs) Input Adaptor Max. Current Limit : Ilimit_current = (Vadj1-0.075) / (25*Rs)	Pre-Charging Mode : Precharging current = 146mA Vadj2 = 166mV Adaptor Max. Current : PR13=330KOHM; PR16=90.9KOHM=> Ilimit = 2.679A ACIN Threshold = 1.25V Adaptor >10.45V, System Powered by Adaptor Adaptor <10.45V, System Powered by Battery	Prevent Input from 19V : Adaptor > 13.92V, PQ4B Turn-off Adaptor < 13.92V, PQ4B Turn-on Battery Cell Selection : CELLS:VREF,4-Cell; CELLS:OPEN,3-Cell; CELLS:GND,2-Cell;	VREF = 5.0V fosc(KHz) = 17000 / RT (KOhm) =515KHz Soft start: ts(s) = 0.23 * CS (uF) =23mS	Charging Current : <table><tr><th>4P#</th><th>2P#</th><th>Icharge</th></tr><tr><td>1</td><td>0</td><td>0.56A</td></tr><tr><td>0</td><td>1</td><td>1.6A</td></tr><tr><td>0</td><td>0</td><td>2.8A</td></tr></table>	4P#	2P#	Icharge	1	0	0.56A	0	1	1.6A	0	0	2.8A
4P#	2P#	Icharge														
1	0	0.56A														
0	1	1.6A														
0	0	2.8A														



ASUSTek Computer Inc.

Title : CHARGER

Engineer: Joy.ZHOU

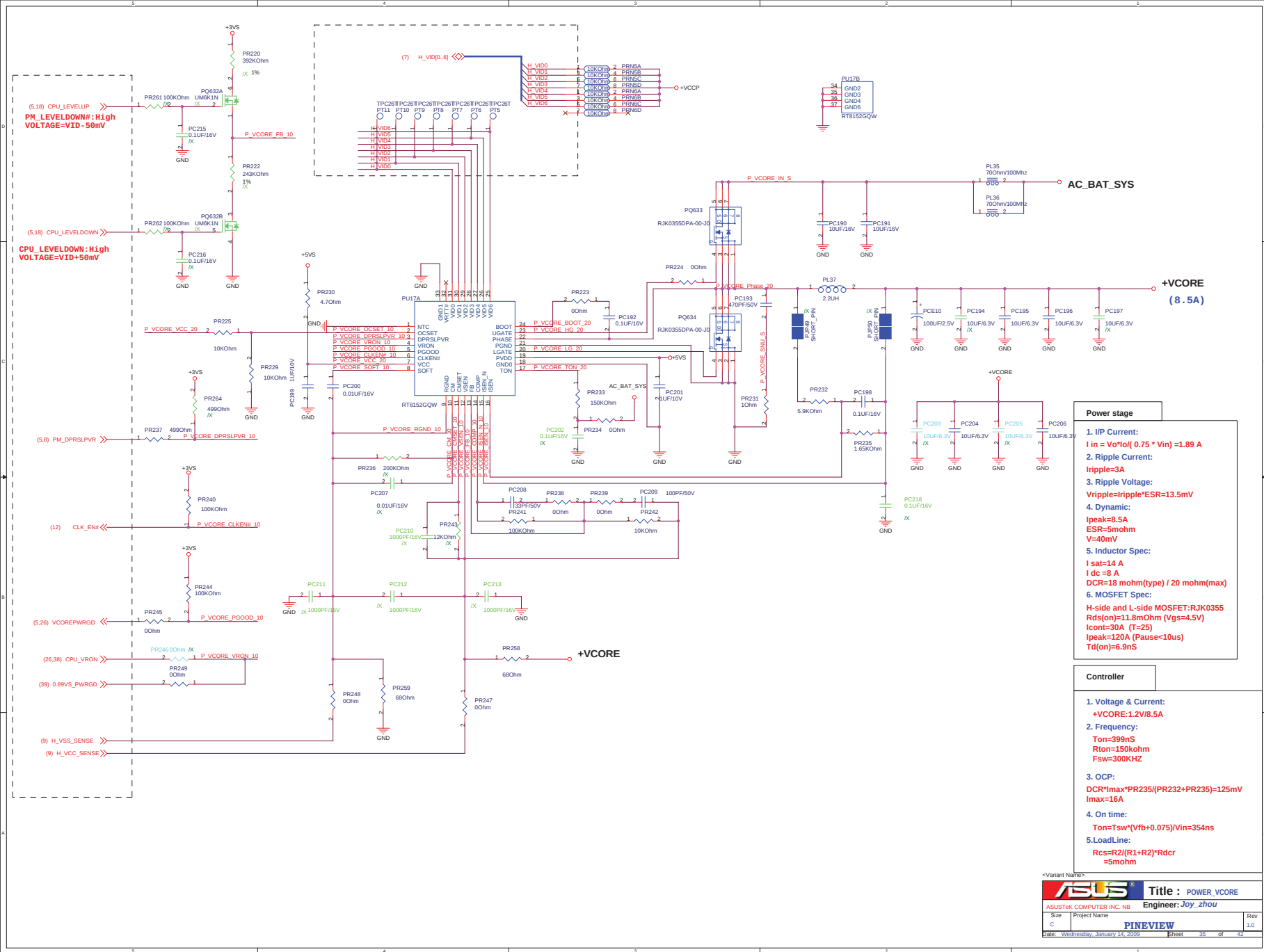
Size A2

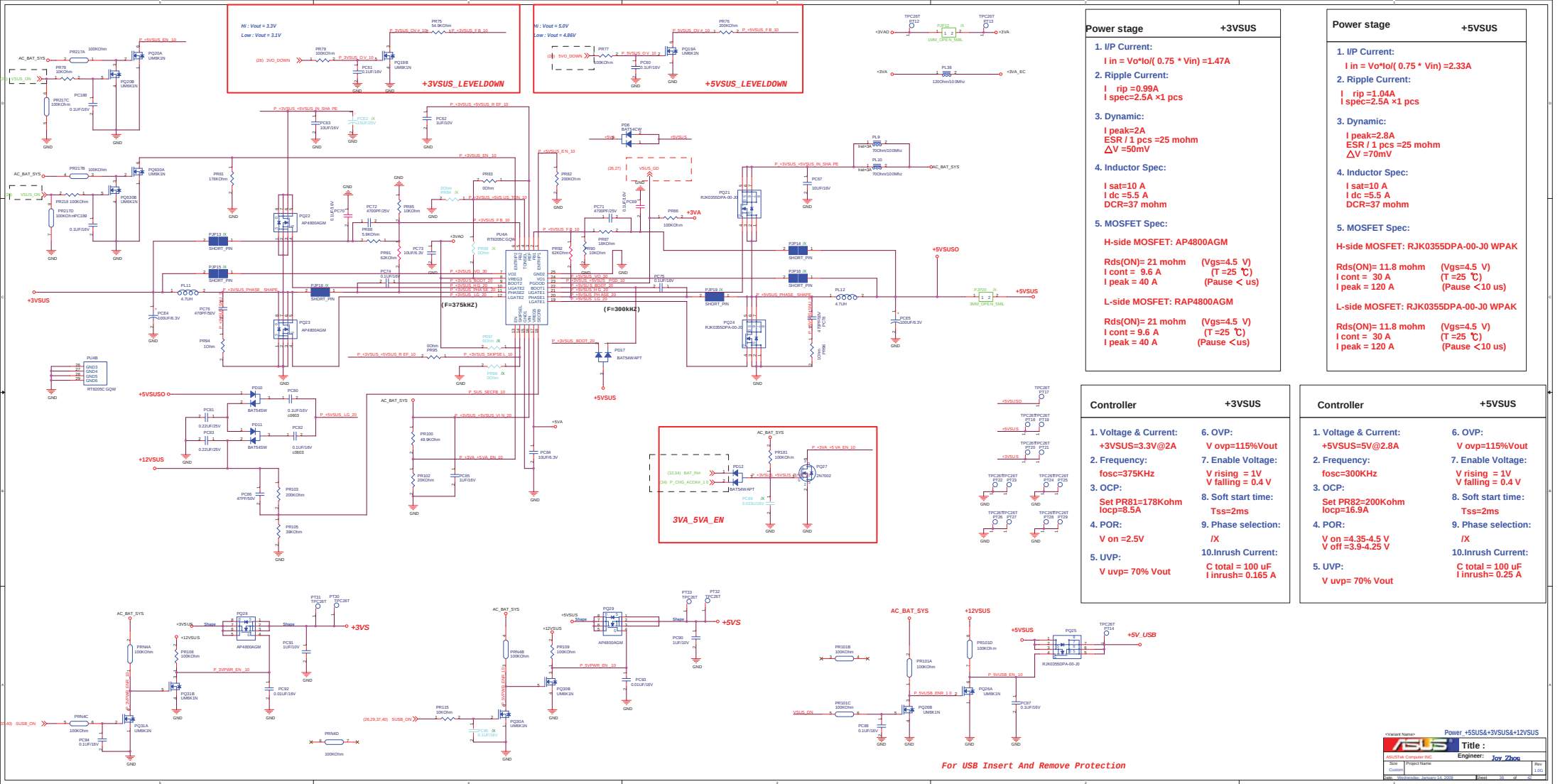
Project Name PINEVIEW

Rev 1.0C

Date: Wednesday, January 14, 2009

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Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.47A$
2. Ripple Current:	$I_{rip} = 0.99A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 2A$ $ESR / 1 \text{ pcs} \approx 25 \text{ mohm}$ $\Delta V = 50mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: AP4800AGM $R_{ds(ON)} = 21 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 9.6 A$ ($T = 25^\circ C$) $I_{peak} = 40 A$ (Pause < us) L-side MOSFET: RAP4800AGM $R_{ds(ON)} = 21 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 9.6 A$ ($T = 25^\circ C$) $I_{peak} = 40 A$ (Pause < us)

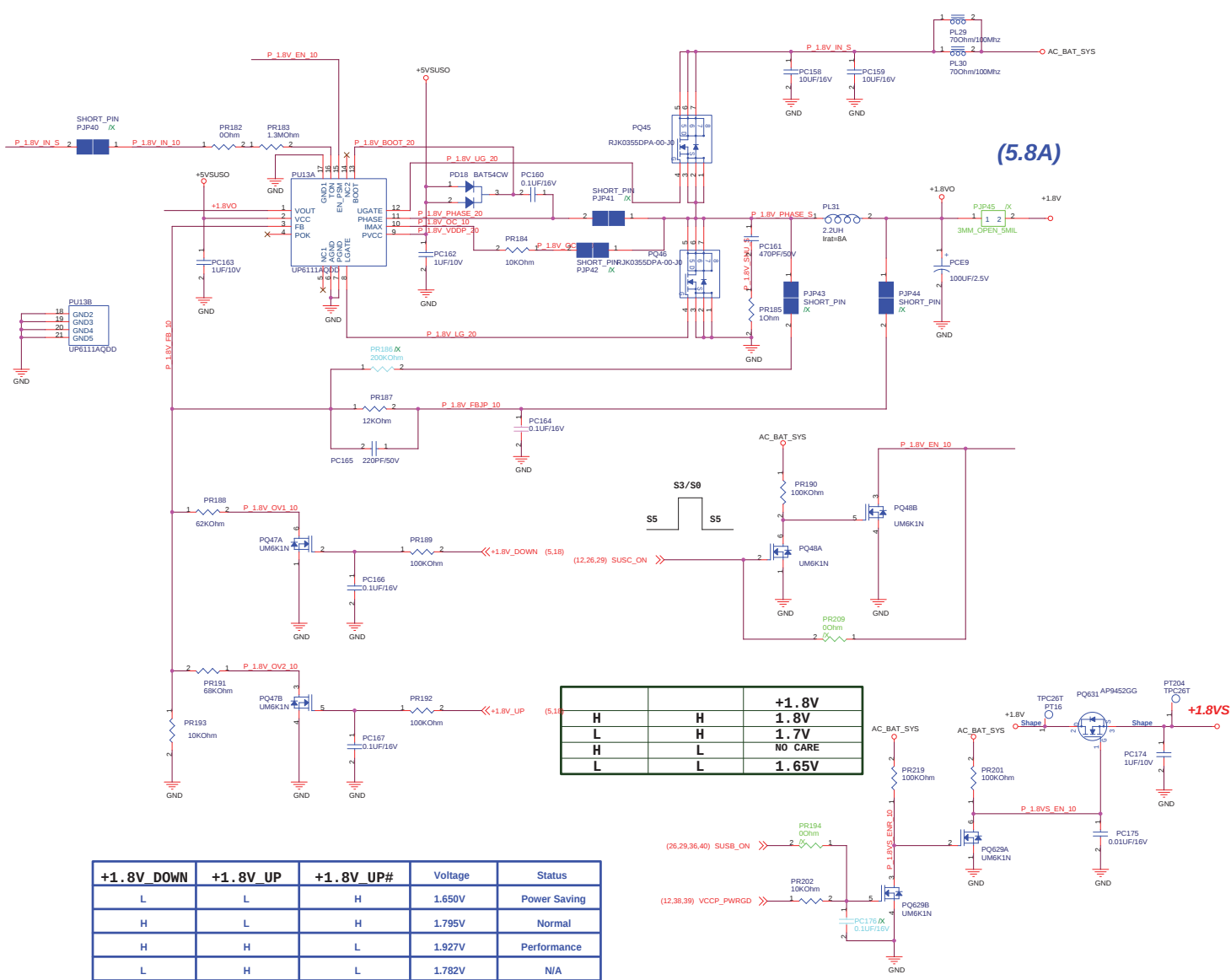
Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.33A$
2. Ripple Current:	$I_{rip} = 1.04A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 2.8A$ $ESR / 1 \text{ pcs} \approx 25 \text{ mohm}$ $\Delta V = 70mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 30 A$ ($T = 25^\circ C$) $I_{peak} = 120 A$ (Pause < 10 us) L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5 V$) $I_{cont} = 30 A$ ($T = 25^\circ C$) $I_{peak} = 120 A$ (Pause < 10 us)

Controller	+3VSUS
1. Voltage & Current:	+3VSUS=3.3V@2A
2. Frequency:	fosc=375KHz
3. OCP:	Set PR81=178Kohm locp=8.5A
4. POR:	V on =2.5V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4 V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 100 uF I inrush= 0.165 A

Controller	+5VSUS
1. Voltage & Current:	+5VSUS=5V@2.8A
2. Frequency:	fosc=300KHz
3. OCP:	Set PR82=200Kohm locp=16.9A
4. POR:	V on =4.35-4.5 V V off =3.9-4.25 V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4 V
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 100 uF I inrush= 0.25 A

For USB Insert And Remove Protection

Project Name: Power: +5VSUS+3VSUS+12VSUS	
ASUS	Title:
ASUSTek Computer Inc.	Engineer: Jay Zhou
Rev: 1	Project Name: Power: +5VSUS+3VSUS+12VSUS
Created: 2018-08-14	Rev: 1



Power stage

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.175A$

2. Ripple Current:
 $I_{rip} = 2.65A$
 $I_{spec} = 2.5A \times 2 \text{ pcs}$

3. Dynamic:
 $I_{peak} = 5.8A$
 $ESR / 1 \text{ pcs} = 18 \text{ mohm}$
 $\Delta V = 104.4mV$

4. Inductor Spec:
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18 \text{ mohm}$

5. MOSFET Spec:

H-side MOSFET: RJK0355DPA-00-J0 WPAK

 $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause < 10 us)

L-side MOSFET: RJK0355DPA-00-J0 WPAK

 $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^\circ C$)
 $I_{peak} = 120A$ (Pause < 10 us)

Controller

1. Voltage & Current:
+1.8V@5.8A

2. Frequency:
 $PR183 = 1.3M \text{ ohm}$
 $F_{osc} = 191KHz$

3. OCP:
 $PR184 = 10K \text{ ohm} \rightarrow 16.7A$

4. POR:
 $V_{ccrth} = 3.7\sim 4.1V$
 $V_{ccchys} = 0.2V$

5. UVP:
Vout*70%

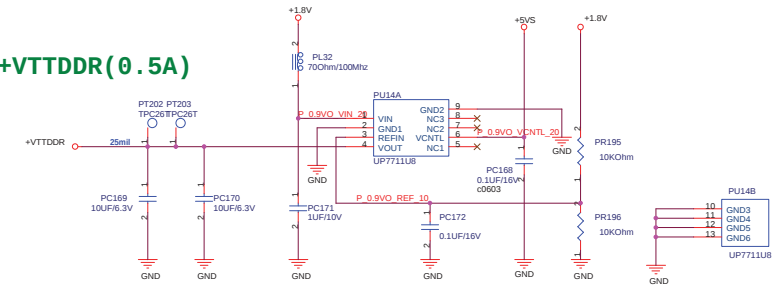
6. OVP:
Vout*115%

7. Enable Voltage:
V = 2.9V

8. Soft start time:
Tss=1.2 ms

9. Phase selection:
/X

10. Inrush Current:
C total = 100 uF
I inrush = 0.15 A



1.5VS @1.1 A

1. Dropout Voltage:
 $\Delta V = 0.3V$ ($I_o = 2A$)

2. Current Limit:
I limit = 4A

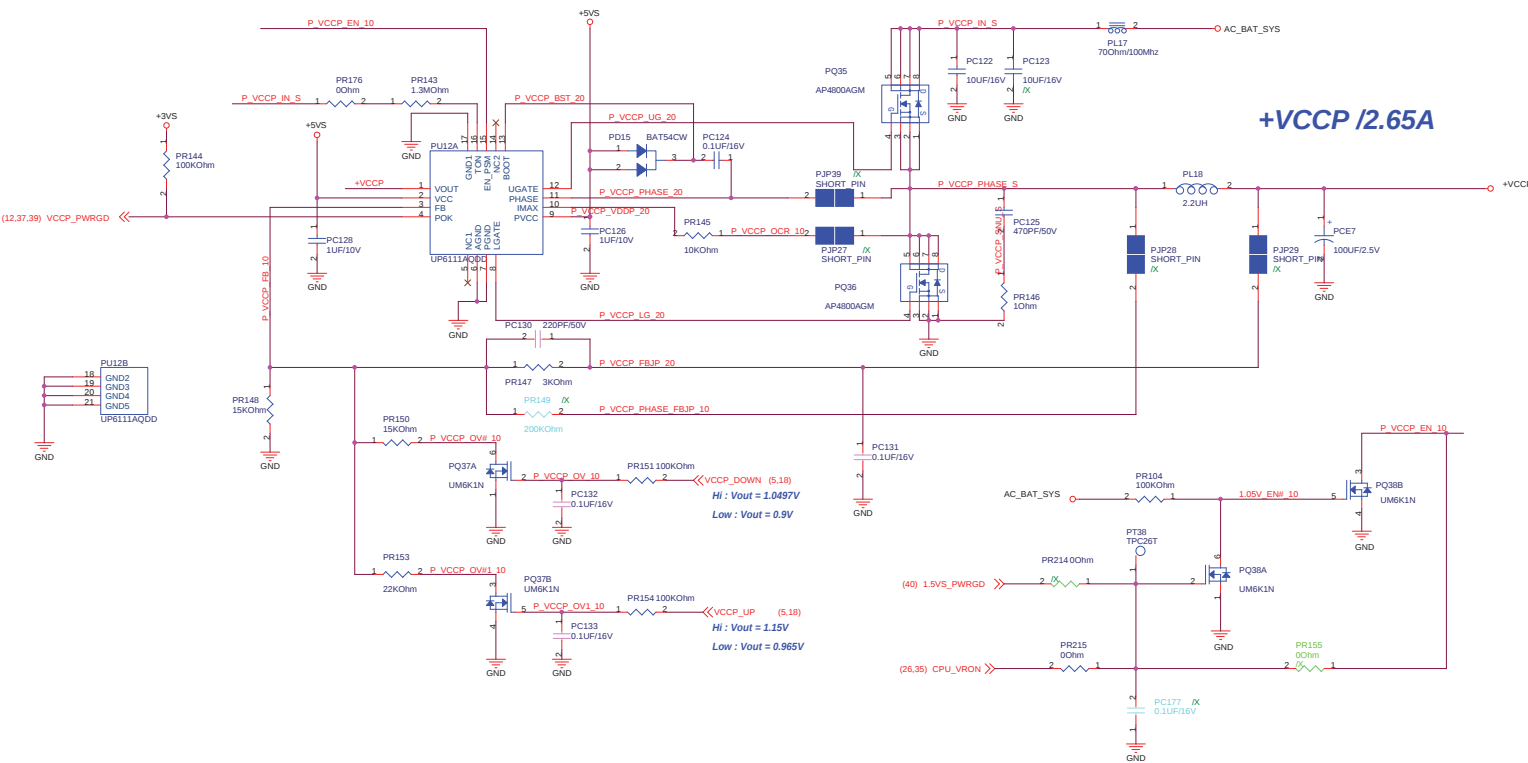
3. Continue Current:
I cont = 3A

4. Power Dissipation:
 $R_{thjc} = 52^\circ C/W$
 $P_d = 1.9W$

5. EN Voltage:
 $V_{en} = 1.4V$
 $V_{sd} = 0.8V$

6. Supply Voltage:
Vcc = 5V

7. Inrush current:
 $T_{ss} = 5ms$
C total = 10 uF
I inrush = 3 mA



+VCCP /2.65A

VCCP_DOWN	VCCP_UP	VCCP_UP#	Voltage	Status
L	L	H	0.9V	Power Saving
H	L	H	1.050V	Normal
H	H	L	1.152V	Performance
L	H	L	1.002V	N/A

Power stage

1. I/P Current:

$I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.58A$

2. Ripple Current:

$I_{rip} = 1A$

$I_{spec} = 2.5A \times 1 pcs$

3. Dynamic:

$I_{peak} = 2.65 A$

$ESR / 1 pcs = 18 mohm$

$\Delta V = 47.7mV$

4. Inductor Spec:

$I_{sat} = 14 A$

$I_{dc} = 8 A$

$DCR = 18 mohm$

5. MOSFET Spec:

H-side MOSFET: AP4800AGM

$R_{ds(ON)} = 21 mohm$

$I_{cont} = 9.6 A$

$I_{peak} = 40 A$

$(V_{gs} = 4.5 V)$

$(T = 25 ^\circ C)$

$(Pause < us)$

L-side MOSFET: RAP4800AGM

$R_{ds(ON)} = 21 mohm$

$I_{cont} = 9.6 A$

$I_{peak} = 40 A$

$(V_{gs} = 4.5 V)$

$(T = 25 ^\circ C)$

$(Pause < us)$

Controller

1. Voltage & Current:

$+1.05V @ 2.65A$

2. Frequency:

$PR143 = 1.3M ohm$

$F_{osc} = 191KHz$

3. OCP:

$PR145 = 10K ohm \rightarrow 9.5A$

4. POR:

$V_{certh} = 3.7 \sim 4.1V$

$V_{chys} = 0.2V$

5. UVP:

$V_{out} * 70\%$

6. OVP:

$V_{out} * 115\%$

7. Enable Voltage:

$V = 2.9V$

8. Soft start time:

$T_{ss} = 1.2 ms$

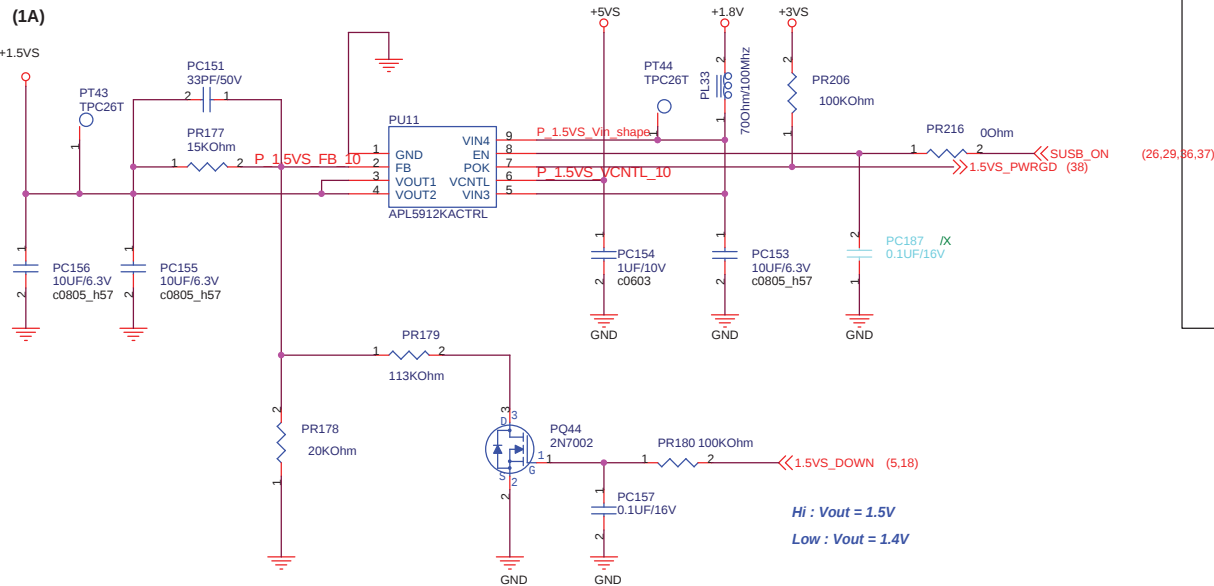
9. Phase selection:

$/X$

10. Inrush Current:

$C_{total} = 100 uF$

$I_{inrush} = 0.0875 A$



1.5VS @ 2 A

1. Dropout Voltage:

$$\Delta V = 0.2V \quad (I_o = 5A)$$

2. Current Limit:

$$I_{limit} = 7A$$

3. Continue Current:

$$I_{cont} = 6A$$

4. Power Dissipation:

$$R_{thjc} = 40^{\circ}C/W$$

$$P_d = 3W$$

5. EN Voltage:

$$V_{rising} = 0.4V$$

$$Hysteresis = 30mV$$

6. Supply Voltage:

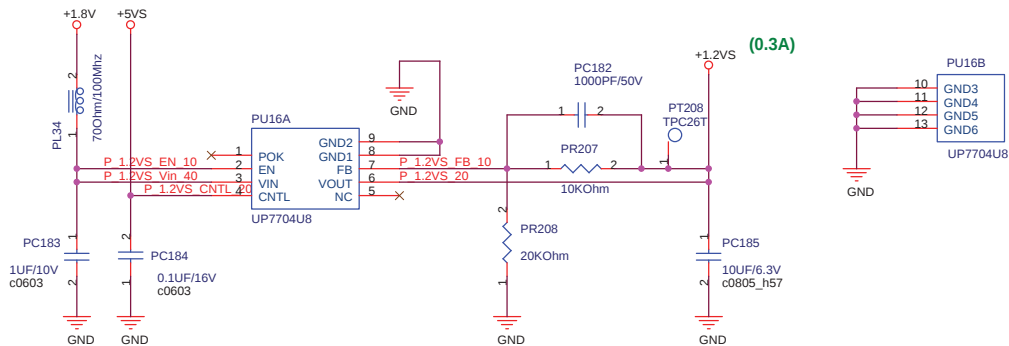
$$V_{cc} = 5V$$

7. Inrush current:

$$T_{ss} = 2ms$$

$$C_{total} = 20\mu F$$

$$I_{inrush} = 15mA$$



1.2VS @ 0.3A

1. Dropout Voltage:

$$\Delta V = 0.3V \quad (I_o = 1A)$$

2.OCP:

$$I_{ocp} = 1.5A$$

3. Short Circuit Current Limit:

$$I_{sc} = 300mA$$

4. Power Dissipation:

$$R_{thjc} = 75^{\circ}C/W$$

$$P_d = 1.33W$$

5. EN Voltage:

$$V_{en} = 1.6V$$

$$V_{sd} = 0.4V$$

6. Power OK Voltage:

$$V_{pokth} = 92\% \cdot V_{out}$$

$$V_{pokhys} = 8\%$$

7. Inrush current:

$$T_{ss} = 5ms$$

$$C_{total} = 10\mu F$$

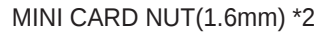
$$I_{inrush} = 2.4mA$$

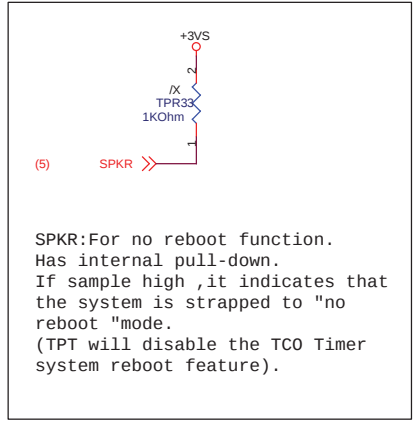
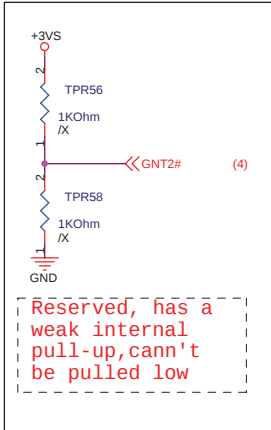
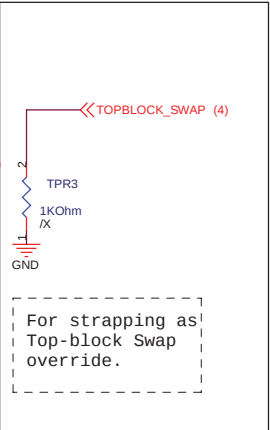
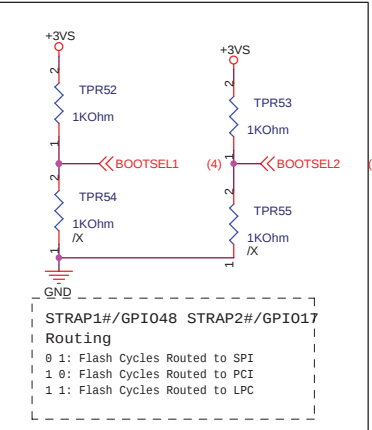
8. FB Voltage:

$$V_{FB} = 0.8V$$

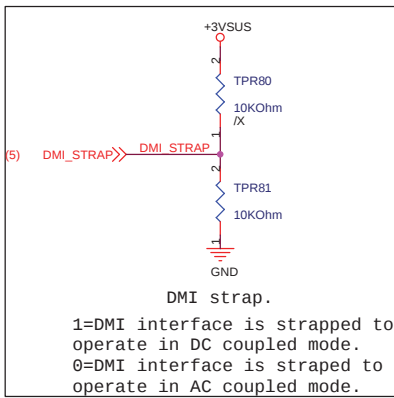
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MINICARD use 12G03010052Q

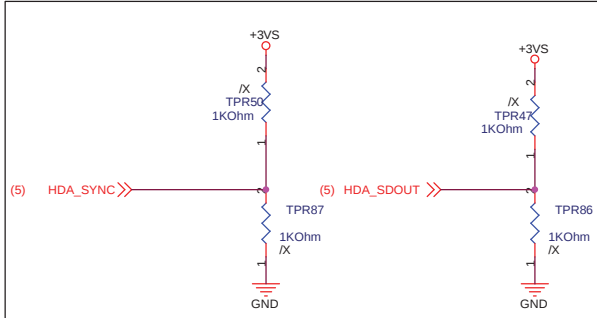




SPKR:For no reboot function.
Has internal pull-down.
If sample high ,it indicates that
the system is strapped to "no
reboot "mode.
(TPT will disable the TCO Timer
system reboot feature).



DMI strap.
1=DMI interface is strapped to
operate in DC coupled mode.
0=DMI interface is strapped to
operate in AC coupled mode.



Check EDS of TPT Section 10.1.30
for details.
HDA_SYNC(PCIE port
config bit 0):
Has weak internal
pull-down.

HDA_SDOUT(PCIE port config bit 1):
Has weak internal pull-down,if not
pulled
low at rising edge of PWROK,sets
bit 1 of RPC.PC.

From 1225.1900 change 3GC1 to 47u,modify screw to
13G021050010.

