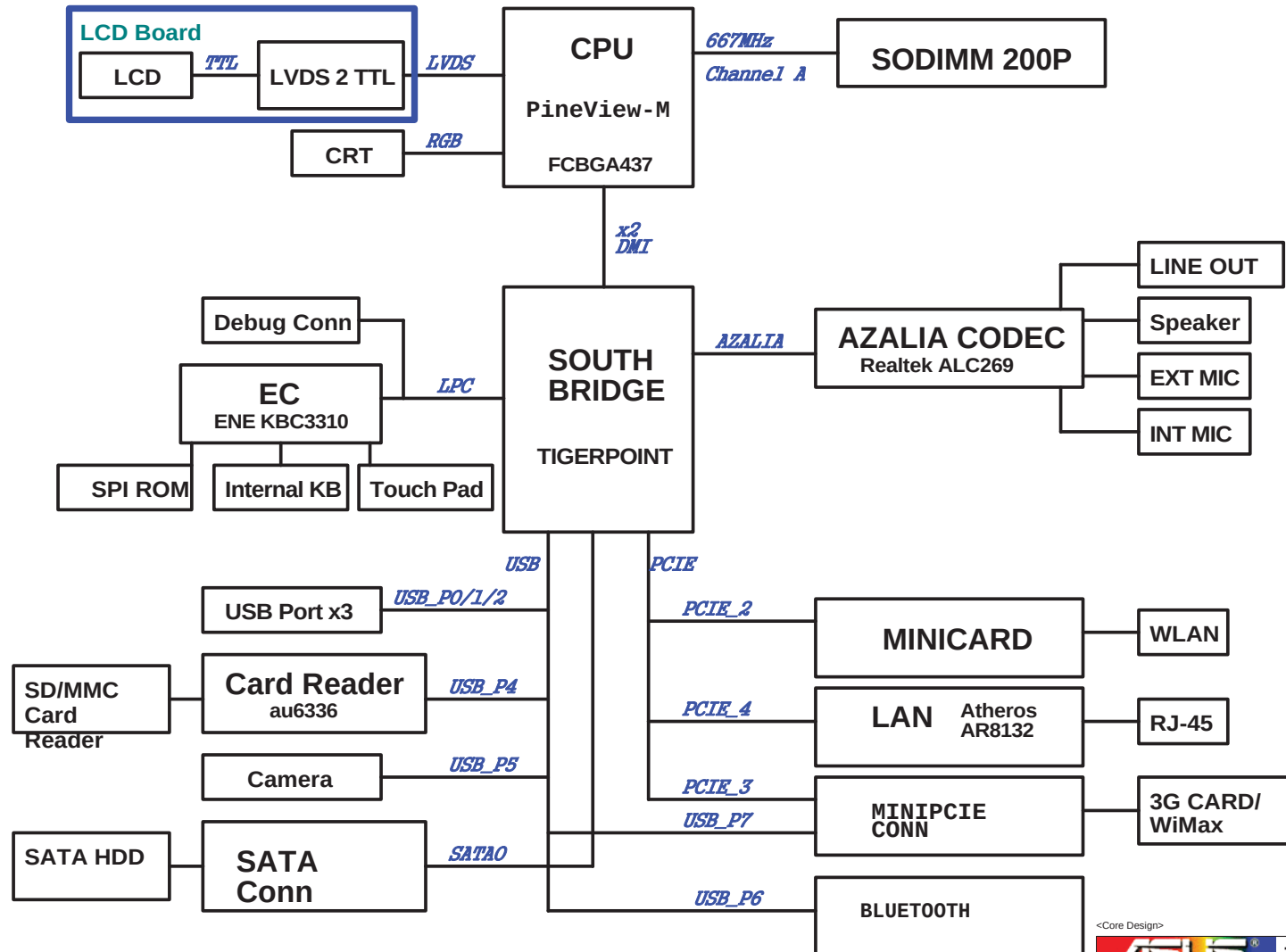


01_Block Diagram
02_Power Sequence
03_Clock Gen_ICS9LPRS427C
04.PineView-M_1 (LVDS_DMI_CPU)
05.PineView-M_2 (DDR2_XDP_CRT)
06.PineView-M_3 (PWR&GND)
07.XDP
08.Tigerpoint_DMI_USB
09.Tigerpoint_SYS
10.Tigerpoint_PWR
11.DDR2 SODIMM
12.DDR2-Termination
13.Onboard VGA
14.LCD Conn_LID
15.WIFI&SMART33SW
16.LAN_AR8132
17.WLAN
18.USIN&3G_CON
19.Bluetooth
20.HDD_CON
21.
22.
23.USB Port1
24.EC_ENE KB3310
25.KB_TP
26.Fan_debug
27.SPI_ROM
28.DUA_CON
29.PWR Jack
30_Discharge
31.
32.Srew Hole&EMI
33.Power Flow
34.Power_Charger
35.Vcore
36.Power_+1.8V&VTDDR&+1.8VS
37.Power_VCCP
38.Power_+0.89VS
39.Power_+1.5VS
40.Power Latch
41.Power System
42.power switch

1015P2

1.0G

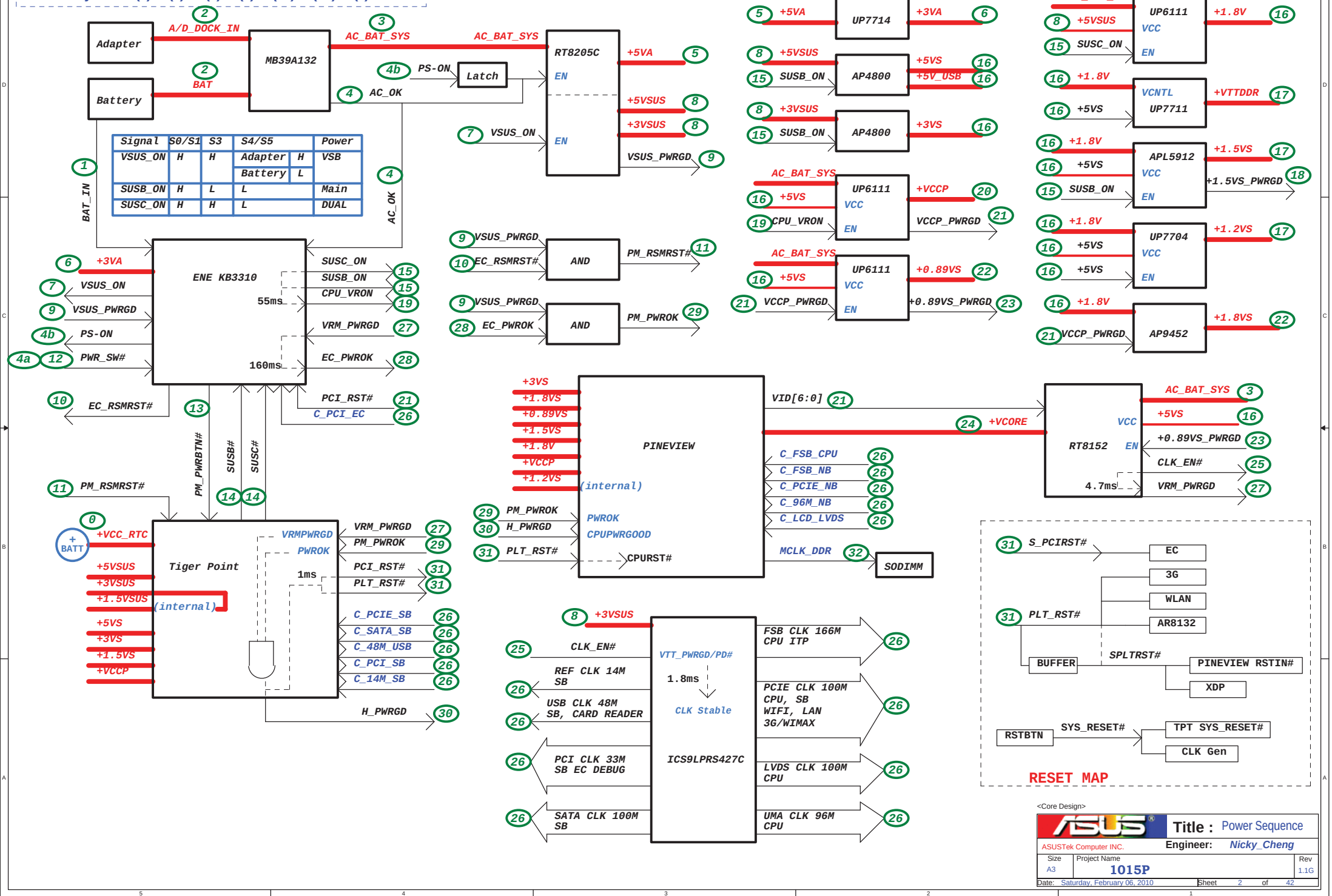
2010_0104

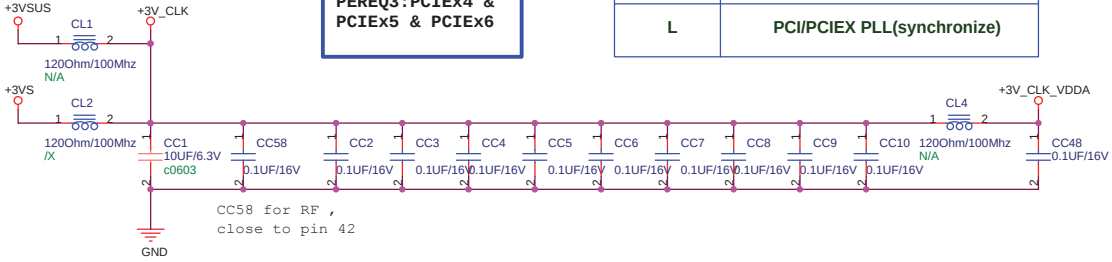
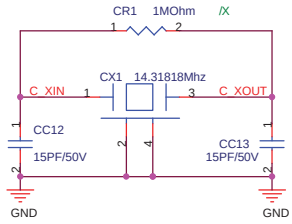


<Core Design>

ASUS		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size Custom	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 1 of 42	

For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
 For Battery Mode: (1) -> (2) -> (3) -> (4) -> (4a) -> (4b) -> (5) -> ...



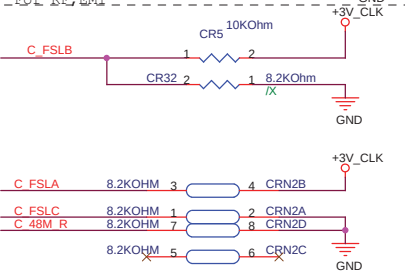
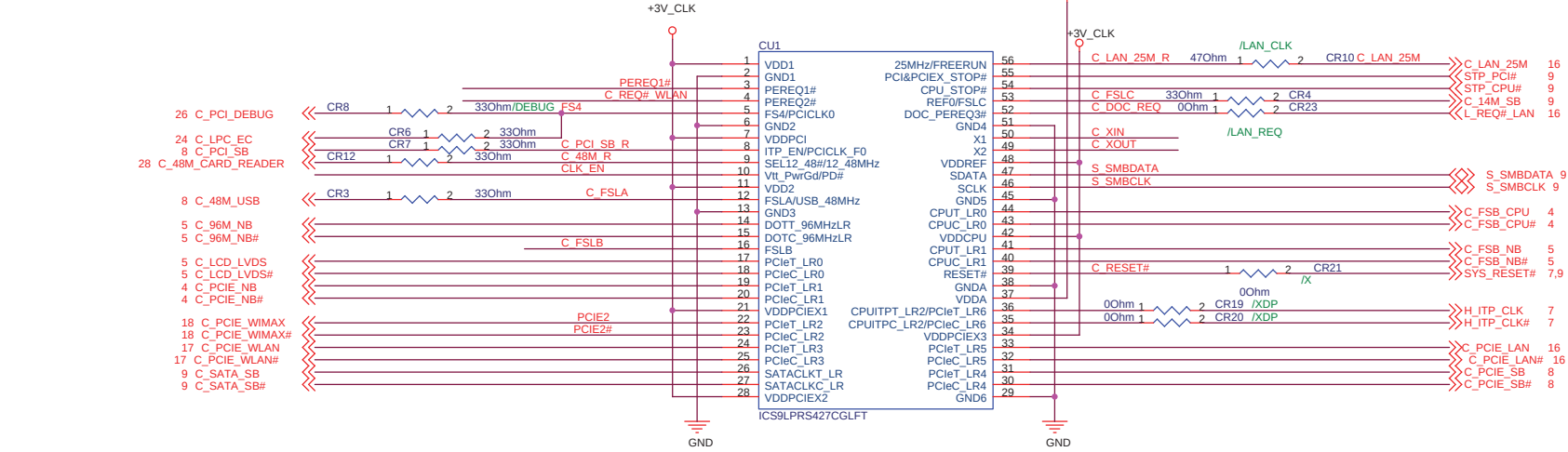


1:Disable
0:Enable

PEREQ1:PCIEx0 &
PCIEx1
PEREQ2:PCIEx2 &
PCIEx3 & SATA
PEREQ3:PCIEx4 &
PCIEx5 & PCIEx6

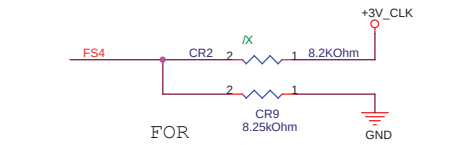
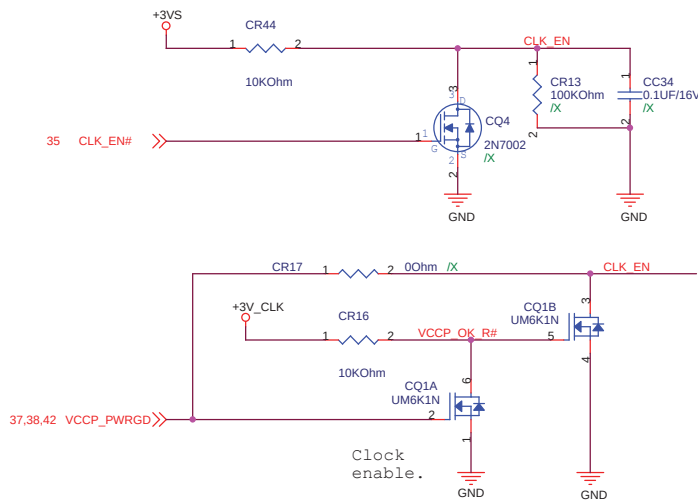
FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

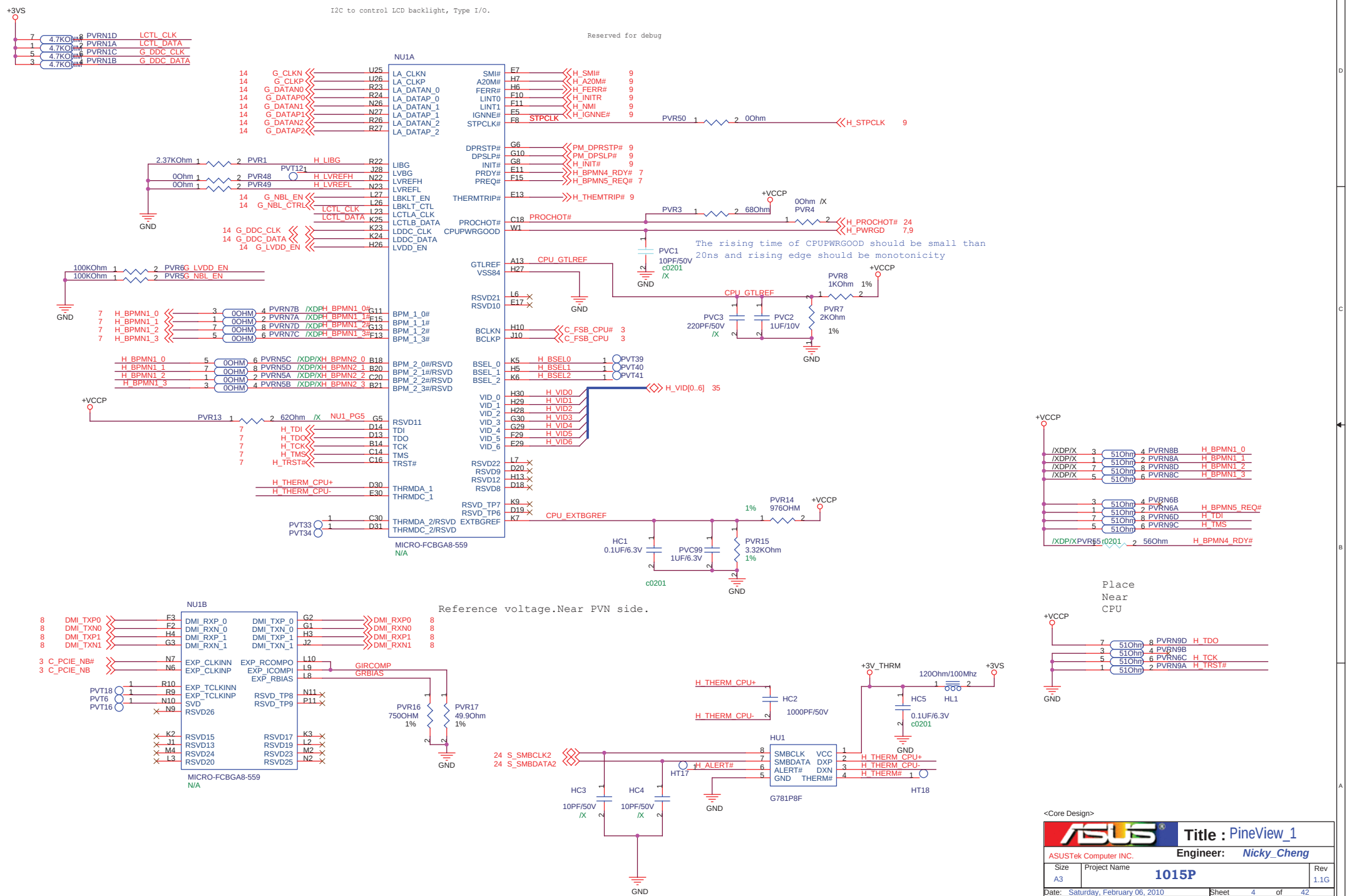
C_SATA_SB	CC50	1	10PF/50V
C_SATA_SB#	CC51	2	10PF/50V
PCIEX2	CC52	2	10PF/50V
PCIEX2#	CC53	2	10PF/50V
C_LCD_LVDS	CC54	2	10PF/50V
C_LCD_LVDS#	CC55	2	10PF/50V
STP_PCI#	EC7	2	10PF/50V
STP_CPU#	EC10	2	10PF/50V
C_PCI_SB_R	CC36	2	10PF/50V
FS4	CC37	2	10PF/50V
S_SMBDATA	EC14	2	10PF/50V
S_SMBCLK	EC15	2	10PF/50V
C_DOC_REQ	EC16	2	10PF/50V
C_FSLC	CC39	2	10PF/50V
C_FSLA	CC40	2	10PF/50V
C_48M_R	CC35	2	47PF/50V
C_LAN_25M_R	CC11	2	10PF/50V
C_PCIE_LAN	EC17	2	10PF/50V
C_PCIE_LAN#	EC18	2	10PF/50V
C_PCI_DEBUG	EC19	2	10PF/50V
C_LPC_EC	EC20	2	10PF/50V
C_14M_SB	EC21	2	10PF/50V



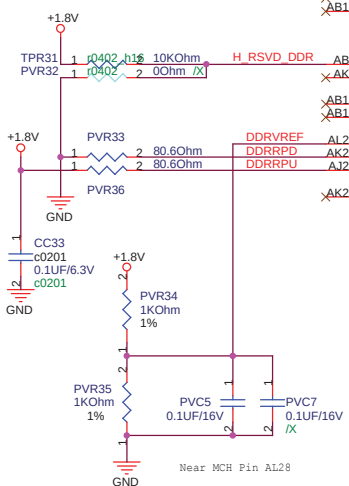
FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133

O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving

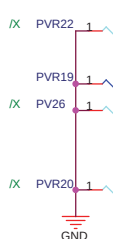




11.12 D2_MAA[14:0] <<>

11.12 D2_WEA# <<>
11.12 D2_CASA# <<>
11.12 D2_RASA# <<>11.12 D2_BAA0 <<>
11.12 D2_BAA1 <<>
11.12 D2_BAA2 <<>11.12 D2_CS_A#0 <<>
11.12 D2_CS_A#1 <<>11.12 D2_CKE_A0 <<>
11.12 D2_CKE_A1 <<>11.12 D2_ODT_A0 <<>
11.12 D2_ODT_A1 <<>11 D2_MA_CLK0 <<>
11 D2_MA_CLK#0 <<>
11 D2_MA_CLK1 <<>
11 D2_MA_CLK#1 <<>

NU1C

D2_MAA0 AH19
D2_MAA1 AJ18
D2_MAA2 AK18
D2_MAA3 AK16
D2_MAA4 AJ14
D2_MAA5 AK14
D2_MAA6 AK14
D2_MAA7 AJ12
D2_MAA8 AH13
D2_MAA9 AK12
D2_MAA10 AK20
D2_MAA11 AH12
D2_MAA12 AJ11
D2_MAA13 AJ24
D2_MAA14 AJ10DDR_A_WE#
DDR_A_CAS#
DDR_A_RAS#DDR_A_BS_0
DDR_A_BS_1
DDR_A_BS_2DDR_A_CS#_0
DDR_A_CS#_1
DDR_A_CS#_2
DDR_A_CS#_3DDR_A_CKE_0
DDR_A_CKE_1
DDR_A_CKE_2
DDR_A_CKE_3DDR_A_ODT_0
DDR_A_ODT_1
DDR_A_ODT_2
DDR_A_ODT_3DDR_A_CK_0
DDR_A_CK_0#
DDR_A_CK_1
DDR_A_CK_1#DDR_A_CK_3
DDR_A_CK_3#
DDR_A_CK_4
DDR_A_CK_4#RSVD5
RSVD4
RSVD1
RSVD2RSVD3
RSVD7
RSVD_TP4
RSVD_TP5RSVD6
DDR_VREF
DDR_RPD
DDR_RPUDDR_A_DQS_5
DDR_A_DQS#_5
DDR_A_DM_5DDR_A_DQ_40
DDR_A_DQ_41
DDR_A_DQ_42
DDR_A_DQ_43
DDR_A_DQ_44
DDR_A_DQ_45
DDR_A_DQ_46
DDR_A_DQ_47DDR_A_DQS_6
DDR_A_DQS#_6
DDR_A_DM_6DDR_A_DQ_48
DDR_A_DQ_49
DDR_A_DQ_50
DDR_A_DQ_51
DDR_A_DQ_52
DDR_A_DQ_53
DDR_A_DQ_54
DDR_A_DQ_55DDR_A_DQS_7
DDR_A_DQS#_7
DDR_A_DM_7DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58
DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62
DDR_A_DQ_63MICRO-FCBGA8-559
N/ADDR_A_DQS_0
DDR_A_DQS#_0
DDR_A_DM_0
DDR_A_DQ_0
DDR_A_DQ_1
DDR_A_DQ_2
DDR_A_DQ_3
DDR_A_DQ_4
DDR_A_DQ_5
DDR_A_DQ_6
DDR_A_DQ_7DDR_A_DQ_8
DDR_A_DQ_9
DDR_A_DQ_10
DDR_A_DQ_11
DDR_A_DQ_12
DDR_A_DQ_13
DDR_A_DQ_14
DDR_A_DQ_15DDR_A_DQS_2
DDR_A_DQS#_2
DDR_A_DM_2DDR_A_DQ_16
DDR_A_DQ_17
DDR_A_DQ_18
DDR_A_DQ_19
DDR_A_DQ_20
DDR_A_DQ_21
DDR_A_DQ_22
DDR_A_DQ_23DDR_A_DQS_3
DDR_A_DQS#_3
DDR_A_DM_3DDR_A_DQ_24
DDR_A_DQ_25
DDR_A_DQ_26
DDR_A_DQ_27
DDR_A_DQ_28
DDR_A_DQ_29
DDR_A_DQ_30
DDR_A_DQ_31DDR_A_DQS_4
DDR_A_DQS#_4
DDR_A_DM_4DDR_A_DQ_32
DDR_A_DQ_33
DDR_A_DQ_34
DDR_A_DQ_35
DDR_A_DQ_36
DDR_A_DQ_37
DDR_A_DQ_38
DDR_A_DQ_39DDR_A_DQS_5
DDR_A_DQS#_5
DDR_A_DM_5DDR_A_DQ_40
DDR_A_DQ_41
DDR_A_DQ_42
DDR_A_DQ_43
DDR_A_DQ_44
DDR_A_DQ_45
DDR_A_DQ_46
DDR_A_DQ_47DDR_A_DQS_6
DDR_A_DQS#_6
DDR_A_DM_6DDR_A_DQ_48
DDR_A_DQ_49
DDR_A_DQ_50
DDR_A_DQ_51
DDR_A_DQ_52
DDR_A_DQ_53
DDR_A_DQ_54
DDR_A_DQ_55DDR_A_DQS_7
DDR_A_DQS#_7
DDR_A_DM_7DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58
DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62
DDR_A_DQ_63DDR_A_DQS_8
DDR_A_DQS#_8
DDR_A_DM_8DDR_A_DQ_64
DDR_A_DQ_65
DDR_A_DQ_66
DDR_A_DQ_67
DDR_A_DQ_68
DDR_A_DQ_69
DDR_A_DQ_70
DDR_A_DQ_71DDR_A_DQS_9
DDR_A_DQS#_9
DDR_A_DM_9AD3 D2_DQS_A0
AD2 D2_DQS_A#0
AD4 D2_DM_A0
AC4 D2_DQ_A0
AC1 D2_DQ_A1
AF4 D2_DQ_A2
AG2 D2_DQ_A3
AB2 D2_DQ_A4
AB3 D2_DQ_A5
AE2 D2_DQ_A6
AE3 D2_DQ_A7AB8 D2_DQS_A1
AD7 D2_DQS_A#1
AA9 D2_DM_A1AB6 D2_DQ_A8
AB7 D2_DQ_A9
AE5 D2_DQ_A10
AG5 D2_DQ_A11
AA5 D2_DQ_A12
AB5 D2_DQ_A13
AB8 D2_DQ_A14
AD6 D2_DQ_A15AD8 D2_DQS_A2
AD10 D2_DQS_A#2
AE8 D2_DM_A2AG8 D2_DQ_A16
AG7 D2_DQ_A17
AF10 D2_DQ_A18
AG11 D2_DQ_A19
AE7 D2_DQ_A20
AF8 D2_DQ_A21
AD11 D2_DQ_A22
AE10 D2_DQ_A23AK5 D2_DQS_A3
AK3 D2_DQS_A#3
AJ3 D2_DM_A3AH1 D2_DQ_A24
AJ2 D2_DQ_A25
AK6 D2_DQ_A26
AJ7 D2_DQ_A27
AF3 D2_DQ_A28
AH2 D2_DQ_A29
AL5 D2_DQ_A30
AJ6 D2_DQ_A31AG22 D2_DQS_A4
AG21 D2_DQS_A#4
AD19 D2_DM_A4AE19 D2_DQ_A32
AG19 D2_DQ_A33
AF22 D2_DQ_A34
AD22 D2_DQ_A35
AG17 D2_DQ_A36
AF19 D2_DQ_A37
AE21 D2_DQ_A38
AD21 D2_DQ_A39AE26 D2_DQS_A5
AG27 D2_DQS_A#5
AJ27 D2_DM_A5AE24 D2_DQ_A40
AG25 D2_DQ_A41
AD25 D2_DQ_A42
AD24 D2_DQ_A43
AC22 D2_DQ_A44
AG24 D2_DQ_A45
AD27 D2_DQ_A46
AE27 D2_DQ_A47AE30 D2_DQS_A6
AF29 D2_DQS_A#6
AE30 D2_DM_A6AG31 D2_DQ_A48
AG30 D2_DQ_A49
AD30 D2_DQ_A50
AD29 D2_DQ_A51
AJ30 D2_DQ_A52
AJ29 D2_DQ_A53
AE29 D2_DQ_A54
AD28 D2_DQ_A55AB27 D2_DQS_A7
AA27 D2_DQS_A#7
AB26 D2_DM_A7AA24 D2_DQ_A56
AB25 D2_DQ_A57
W24 D2_DQ_A58
W22 D2_DQ_A59
AB24 D2_DQ_A60
AB23 D2_DQ_A61
AA23 D2_DQ_A62
W27 D2_DQ_A63DDR_A_DQ_56
DDR_A_DQ_57
DDR_A_DQ_58
DDR_A_DQ_59
DDR_A_DQ_60
DDR_A_DQ_61
DDR_A_DQ_62
DDR_A_DQ_63DDR_A_DQS_8
DDR_A_DQS#_8
DDR_A_DM_8DDR_A_DQ_64
DDR_A_DQ_65
DDR_A_DQ_66
DDR_A_DQ_67
DDR_A_DQ_68
DDR_A_DQ_69
DDR_A_DQ_70
DDR_A_DQ_71DDR_A_DQS_9
DDR_A_DQS#_9
DDR_A_DM_9DDR_A_DQ_72
DDR_A_DQ_73
DDR_A_DQ_74
DDR_A_DQ_75
DDR_A_DQ_76
DDR_A_DQ_77
DDR_A_DQ_78
DDR_A_DQ_79>>>D2_DQ_A[63:0] 11
>>>D2_DQS_A[7:0] 11
>>>D2_DQS_A#7[7:0] 11
>>>D2_DM_A[7:0] 11

NU1D

XDP_RSVD[0]
XDP_RSVD[1]
XDP_RSVD[2]
XDP_RSVD[3]
XDP_RSVD[4]
XDP_RSVD[5]
XDP_RSVD[6]
XDP_RSVD[7]
XDP_RSVD[8]
XDP_RSVD[9]
XDP_RSVD[10]
XDP_RSVD[11]
XDP_RSVD[12]
XDP_RSVD[13]
XDP_RSVD[14]
XDP_RSVD[15]
XDP_RSVD[16]
XDP_RSVD[17]
RSVD_TP3
RSVD_TP2
RSVD_TP10
RSVD_TP11
RSVD_TP1
RSVD_TP14
RSVD_TP12
RSVD_TP13MICRO-FCBGA8-559
N/ACRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTNCRT_DDC_DATA
CRT_DDC_CLK
DAC_IREFREFCLKINP
REFCLKINN
REFSSCLKINP
REFSSCLKINNC_96M_NB
C_96M_NB#
C_LCD_LVDS
C_LCD_LVDS#PM_DPRSPLPVR
PM_EXITS1
PM_EXITS0
PM_PWROK
PM_S_PCIRST#C_FSB_NB#
C_FSB_NBPVC9
PVC1010PF/50V
10PF/50VGND
GNDDDC CLK&DATA need 2.2K Pull
up to +3VS(Or may we can use
4.7K);connector side has
pull-up resistor.

CPU Sample SKU	ASUS P/N
ES1	01G013070000
ES2	01G0132000000
QS	01G0132000001
PRQ	01G0132000002

Intel confirm only RSVD9 need stuff 1K
resistor.

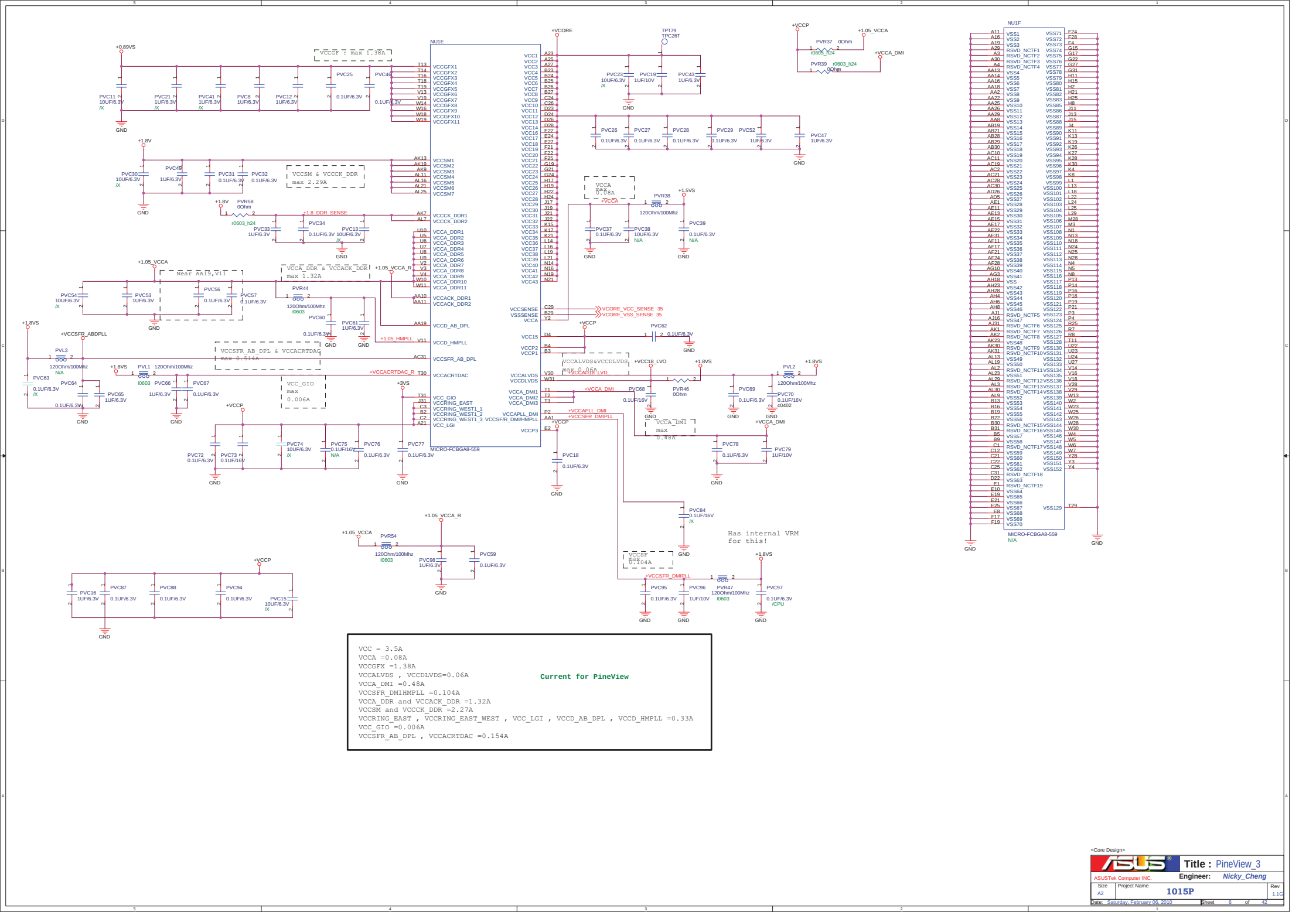
<Core Design>

Title : PineView_2

ASUSTek Computer INC. Engineer: Nicky Cheng

Size A3 Project Name 1015P Rev 1.0G

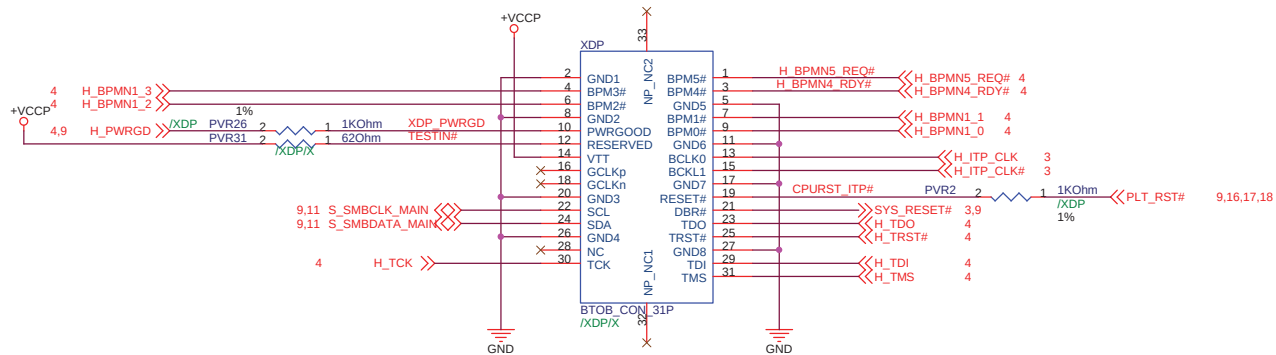
Date: Saturday, February 06, 2010 Sheet 5 of 42



VCC = 3.5A
VCCA = 0.08A
VCCGFX = 1.38A
VCCALVDS, VCCDLVDS = 0.06A
VCCA_DMI = 0.48A
VCCSFR_DMIHPLL = 0.104A
VCCA_DDR and VCCACK_DDR = 1.32A
VCCSM and VCCCK_DDR = 2.27A
VCCRING_EAST, VCCRING_EAST_WEST, VCC_LGI, VCCD_AB_DPL, VCCD_HMPLL = 0.33A
VCC_GIO = 0.006A
VCCSFR_AB_DPL, VCCACRTDAC = 0.154A

Current for PineView

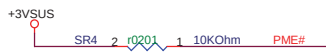
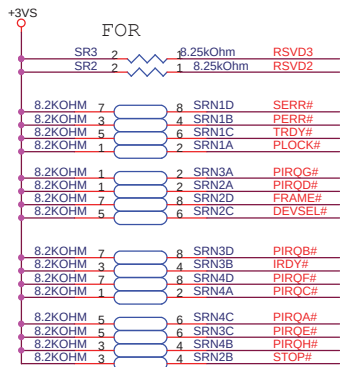
NU1F		
A11	VSS1	VSS71
A16	VSS2	VSS72
A19	VSS3	VSS73
A29	RSVD_NCTF1	VSS74
A3	RSVD_NCTF2	VSS75
A30	RSVD_NCTF3	VSS76
A4	RSVD_NCTF4	VSS77
AA14	VSS4	VSS78
AA16	VSS5	VSS79
AA18	VSS6	VSS80
AA2	VSS7	VSS81
AA22	VSS8	VSS82
AA25	VSS9	VSS83
AA26	VSS10	VSS84
AA29	VSS11	VSS85
AA3	VSS12	VSS86
AB19	VSS13	VSS87
AB21	VSS14	VSS88
AB29	VSS15	VSS89
AB30	VSS16	VSS90
AC10	VSS17	VSS91
AC11	VSS18	VSS92
AC19	VSS19	VSS93
AC2	VSS20	VSS94
AC21	VSS21	VSS95
AC28	VSS22	VSS96
AD26	VSS23	VSS97
AE1	VSS24	VSS98
AE11	VSS25	VSS99
AE15	VSS26	VSS100
AE17	VSS27	VSS101
AE22	VSS28	VSS102
AE31	VSS29	VSS103
AE33	VSS30	VSS104
AE34	VSS31	VSS105
AE37	VSS32	VSS106
AE4	VSS33	VSS107
AE41	VSS34	VSS108
AE47	VSS35	VSS109
AE54	VSS36	VSS110
AE58	VSS37	VSS111
AG10	VSS38	VSS112
AG19	VSS39	VSS113
AG3	VSS40	VSS114
AH23	VSS41	VSS115
AH28	VSS42	VSS116
AH29	VSS43	VSS117
AH4	VSS44	VSS118
AH6	VSS45	VSS119
AH8	VSS46	VSS120
AH9	RSVD_NCTF5	VSS121
AJ16	RSVD_NCTF6	VSS122
AJ2	RSVD_NCTF7	VSS123
AJ23	RSVD_NCTF8	VSS124
AK30	RSVD_NCTF9	VSS125
AK31	RSVD_NCTF10	VSS126
AL13	VSS47	VSS127
AL19	VSS48	VSS128
AL2	VSS49	VSS129
AL24	VSS50	VSS130
AL29	VSS51	VSS131
AL3	VSS52	VSS132
AL30	VSS53	VSS133
AL39	VSS54	VSS134
B13	VSS55	VSS135
B16	VSS56	VSS136
B19	VSS57	VSS137
B22	VSS58	VSS138
B30	VSS59	VSS139
B5	VSS60	VSS140
B9	VSS61	VSS141
C11	VSS62	VSS142
C12	VSS63	VSS143
C21	VSS64	VSS144
C22	VSS65	VSS145
C25	VSS66	VSS146
C31	VSS67	VSS147
D22	VSS68	VSS148
E1	VSS69	VSS149
E10	VSS70	VSS150
E19	VSS71	VSS151
E21	VSS72	VSS152
E25	VSS73	VSS153
E8	VSS74	VSS154
F17	VSS75	VSS155
F19	VSS76	VSS156



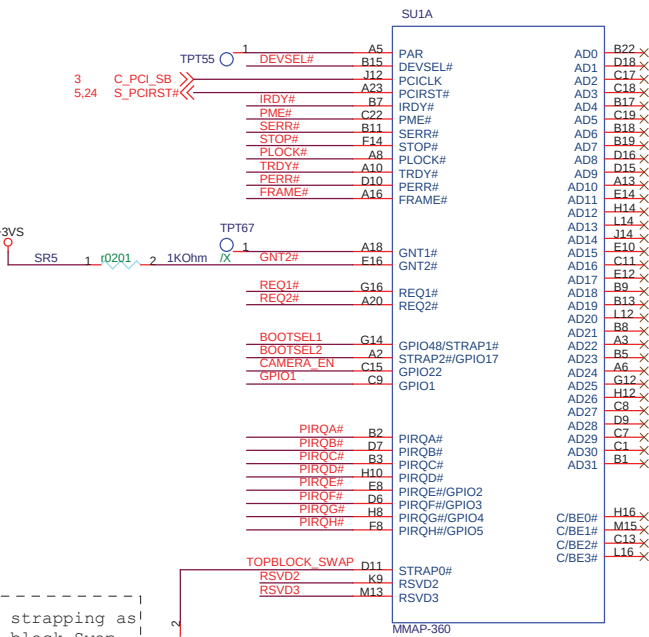
根據 Layout 訣竅叫 XDP Connector 叫確
12G161300311 (w/ 2 through holes)

<Core Design>

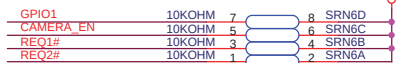
ASUS		Title : XDP	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 7 of 42	



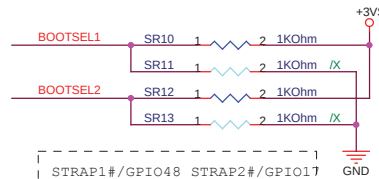
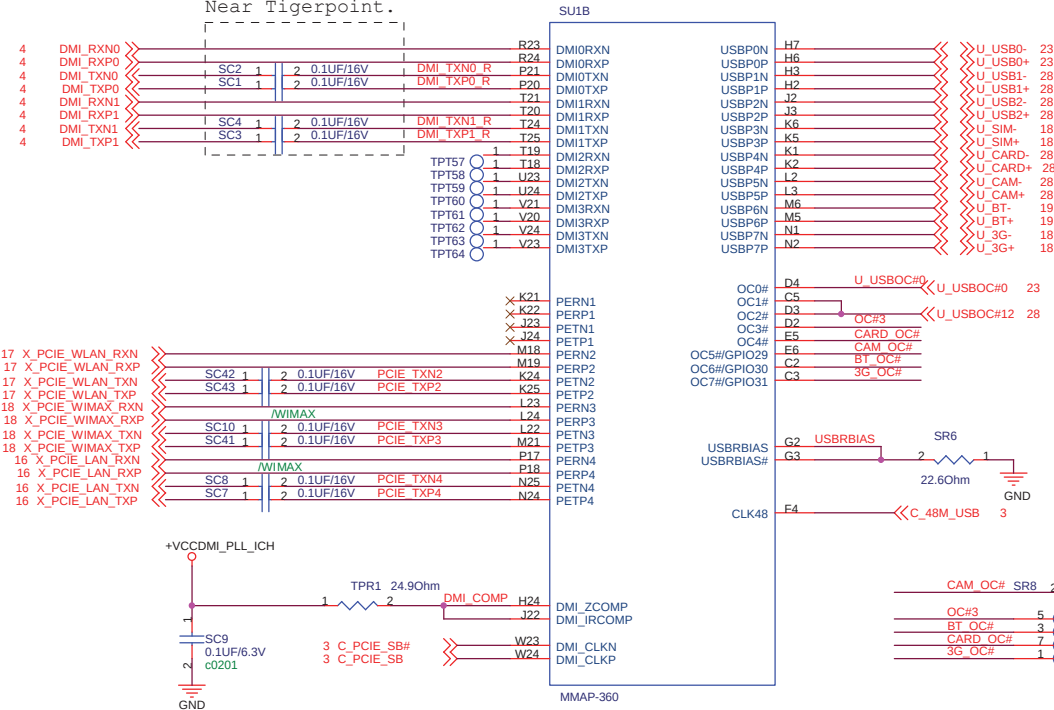
Remain
PCICLK



For strapping as
Top-block Swap
override.



Near Tigerpoint.

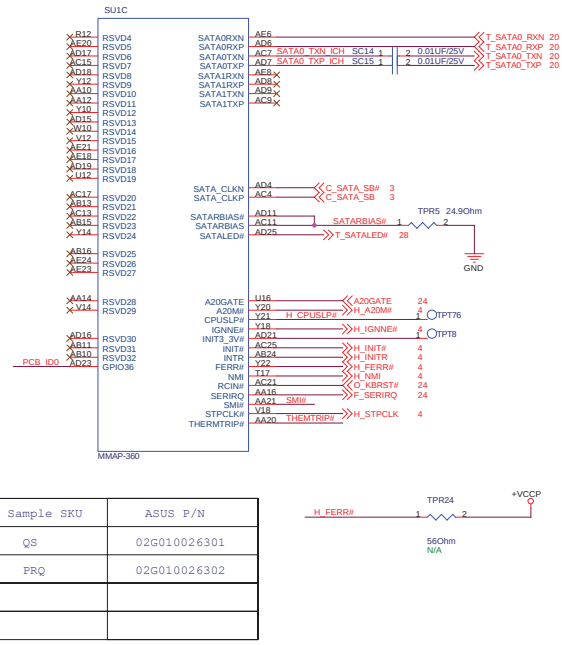


<Core Design>

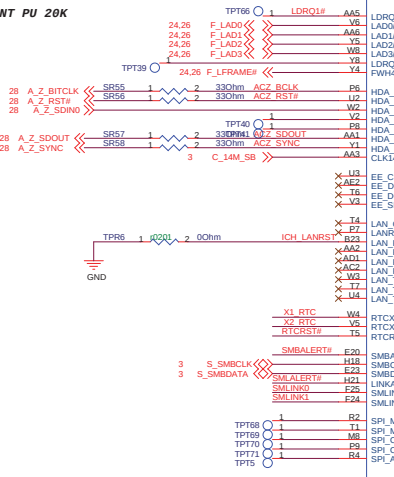
CLK 14MHZ has a 22ohm resistor near clk Gen.

LDRQ0/1 LPC DMA/master request, ICH7M has internal PU, but we need TPT datasheet

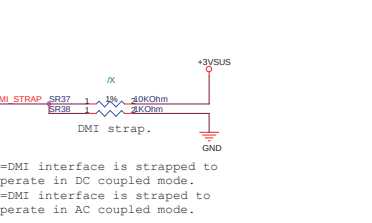
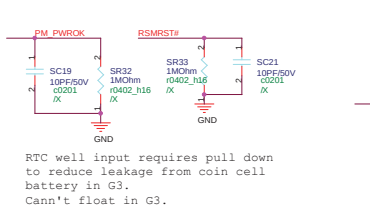
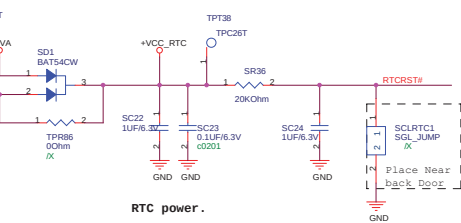
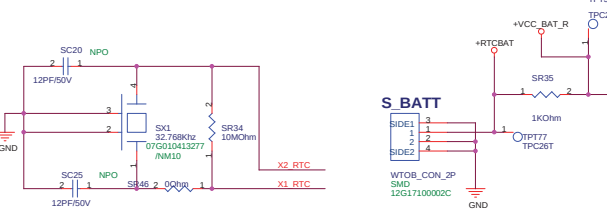
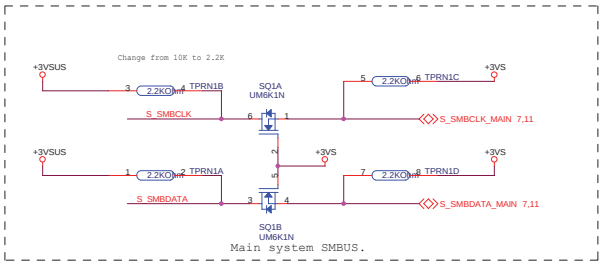
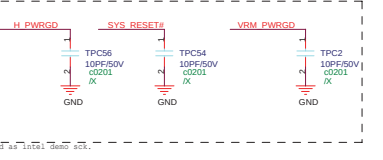
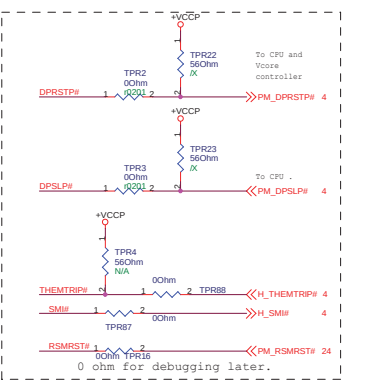
SATA RX, TX all need AC couple and place near Connector. And Traces to them should match length. ICH7M need pull down RX, if no use.



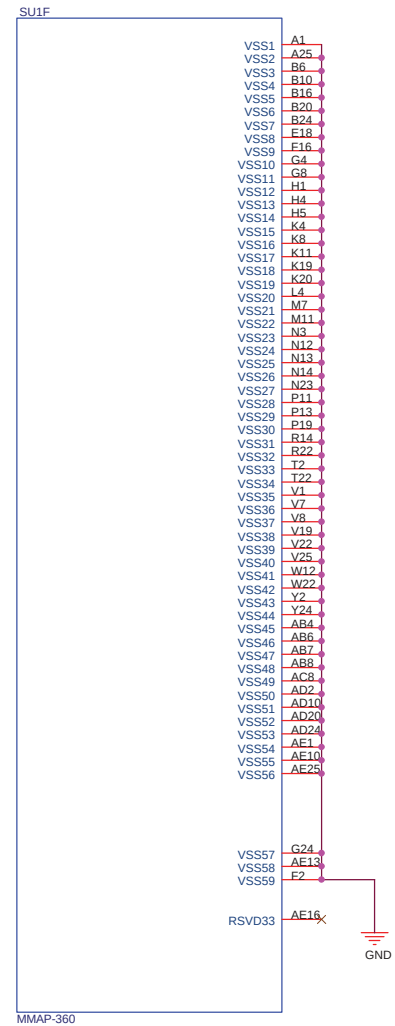
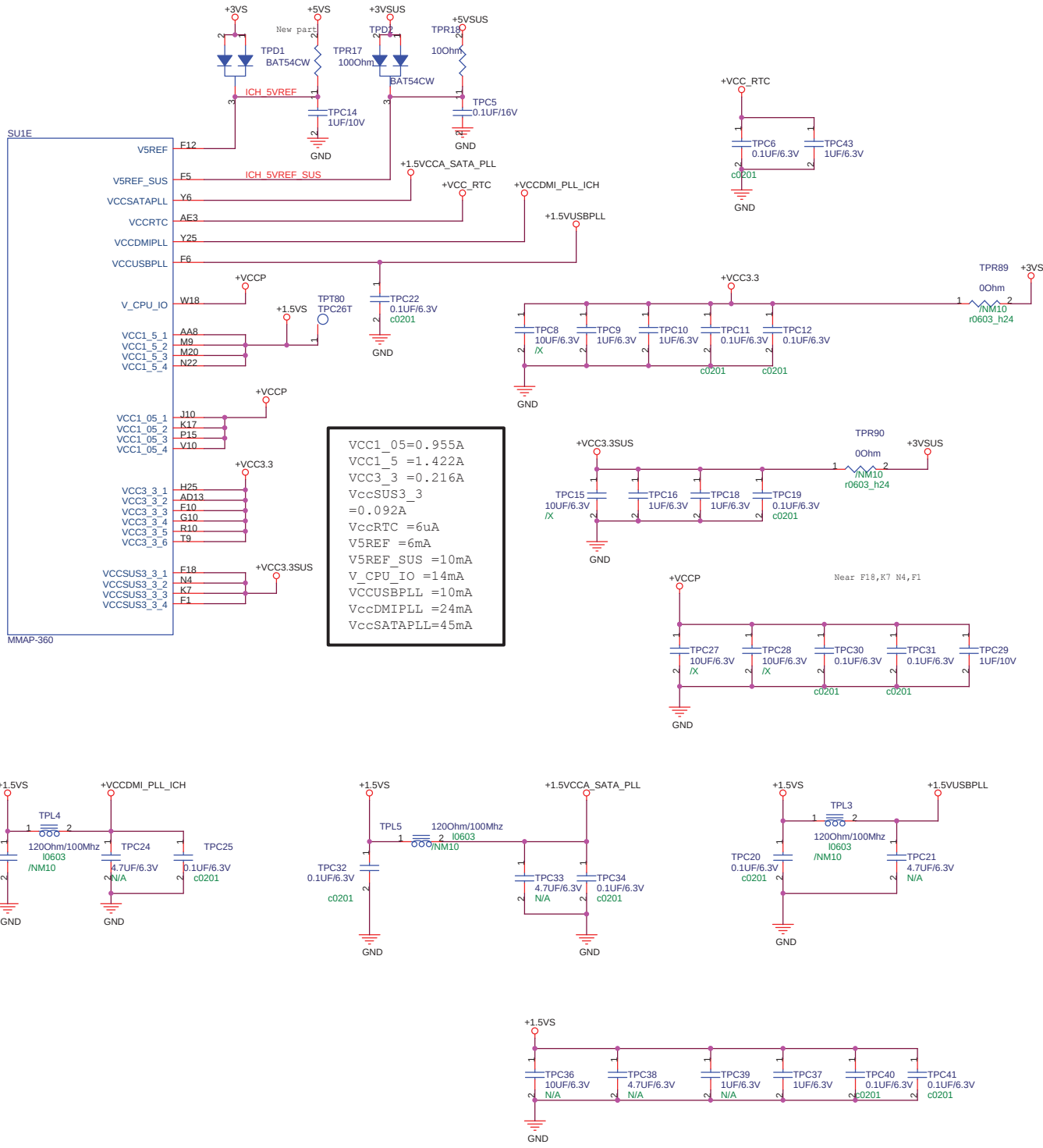
LAD[0:3] INT PU 20K

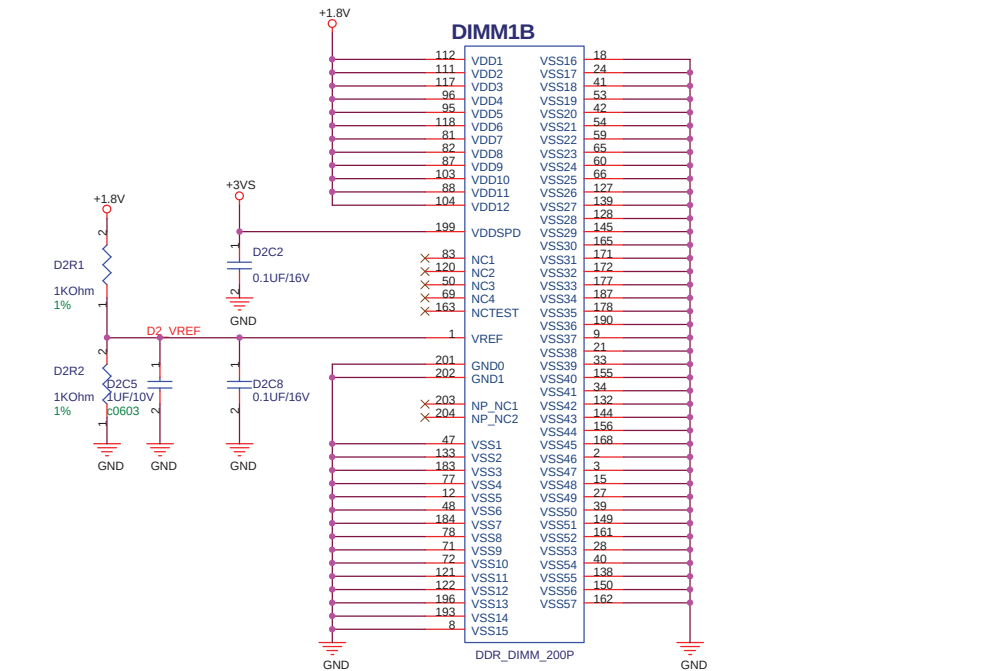
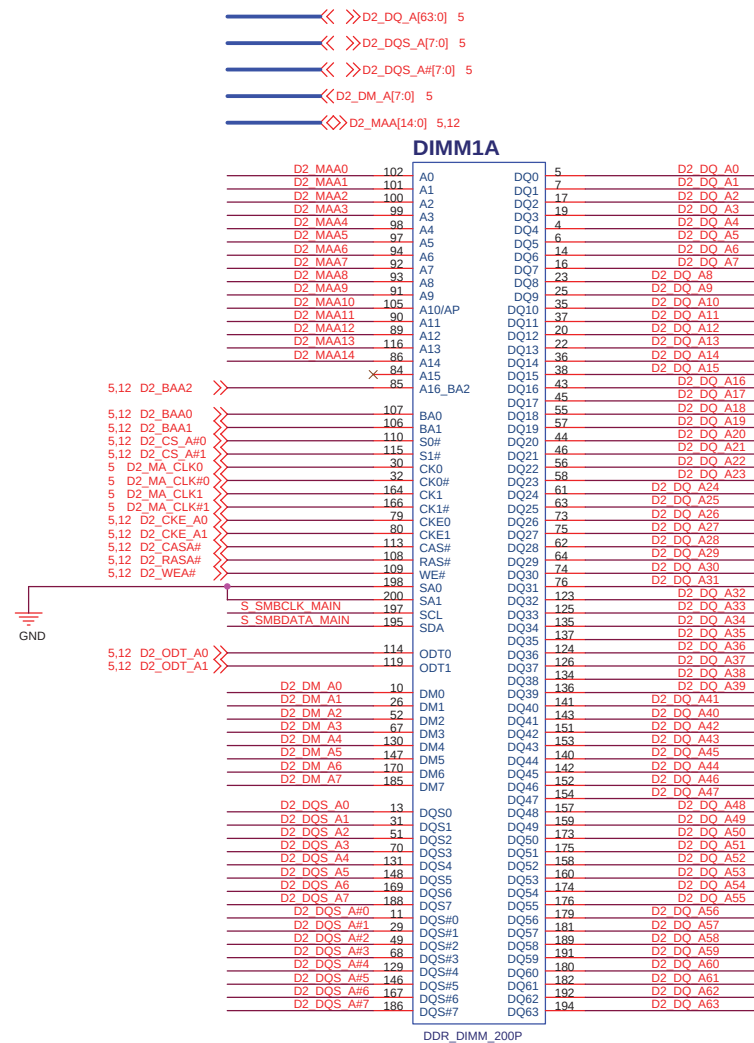


PCB ID

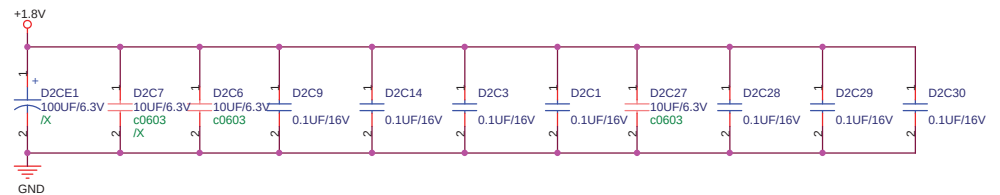
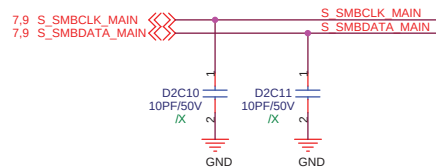


For Rechargeable solution: Mount TPR2
For NON-Rechargeable solution: Unmount TPR2

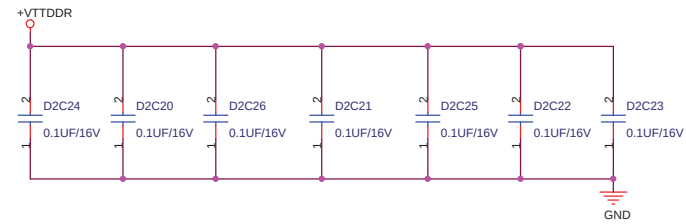
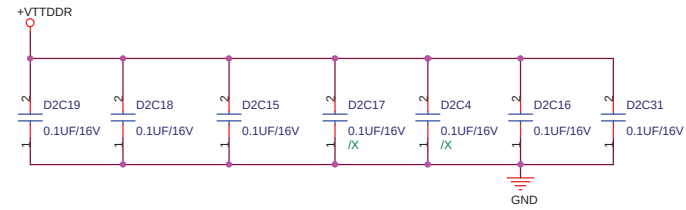
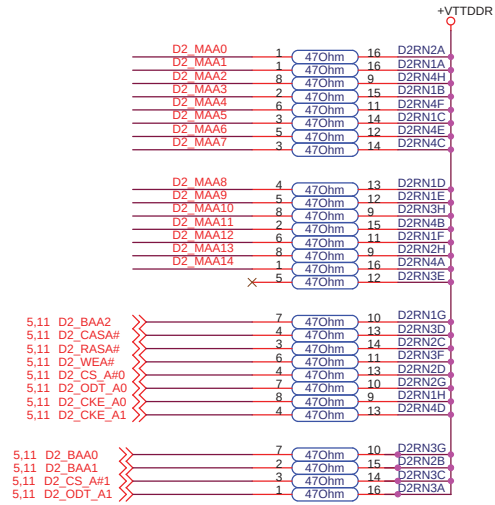




"根 Layout 訣賀叫c祇2nd source / 12G025C2200X PCB footprint
 , 磷 2nd DIMM 敷耗婉策ン玻ネ 疊- 2nd source PCB footprint
 敷main source size DIMM羅 T↑い "

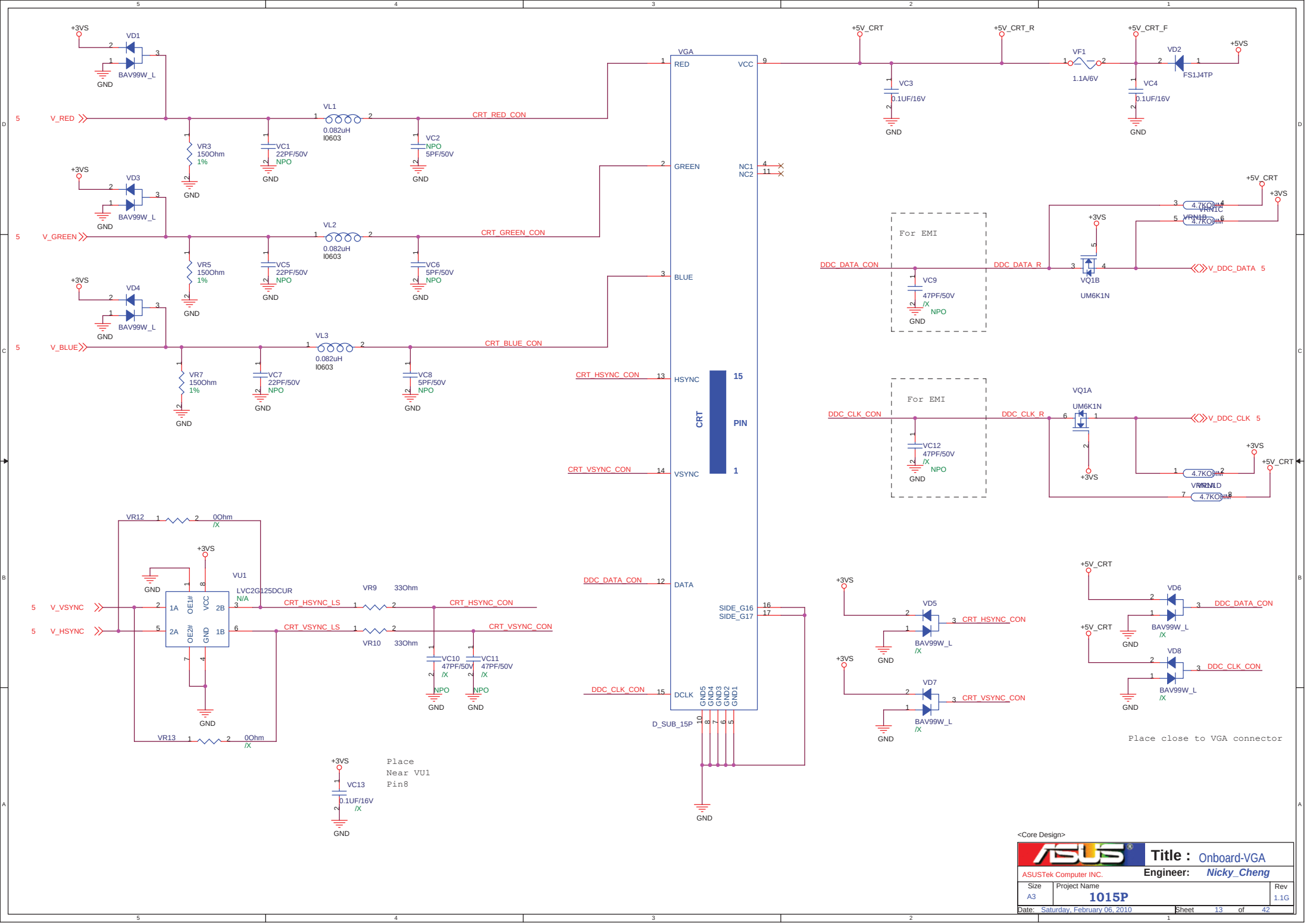


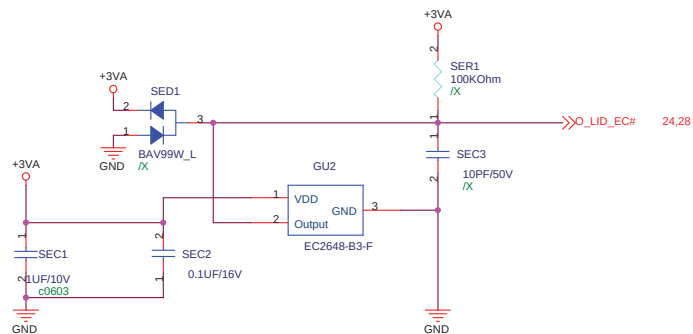
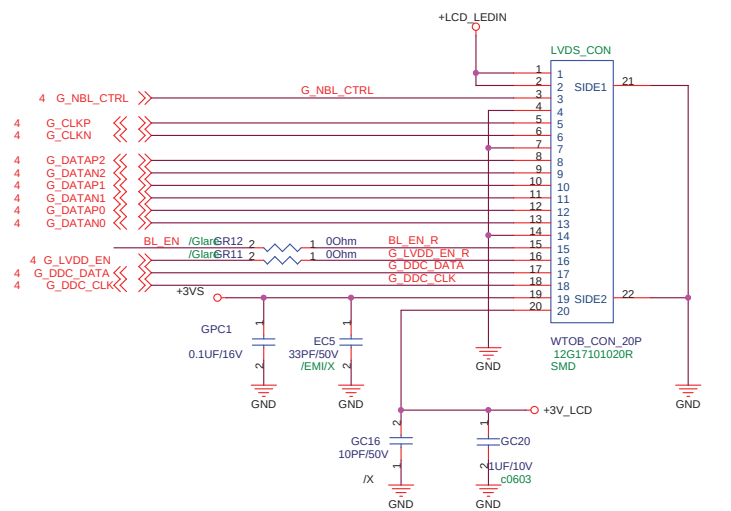
◇◇ D2_MAA[14:0] 5,11



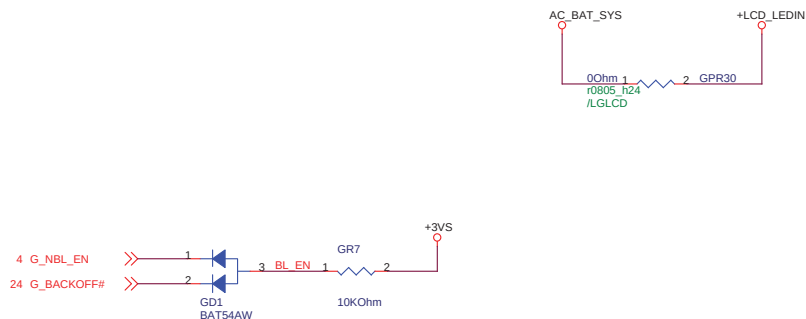
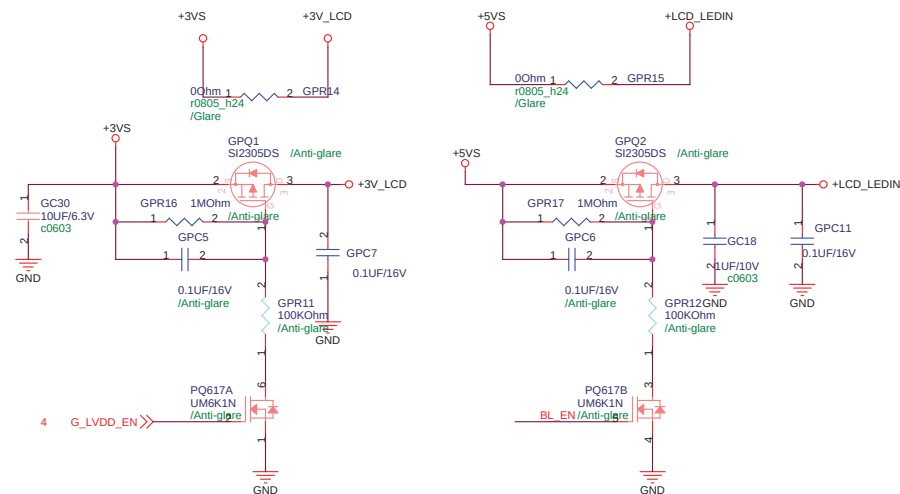
<Core Design>

ASUS		Title : DDR2-Termination	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.0G	
Date: Saturday, February 06, 2010		Sheet	12 of 42



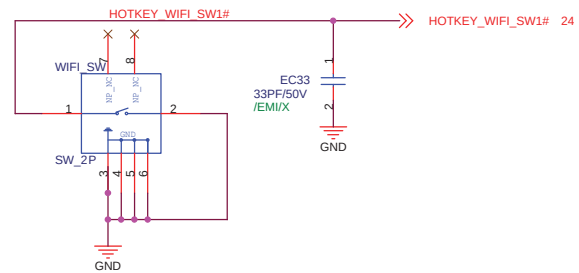
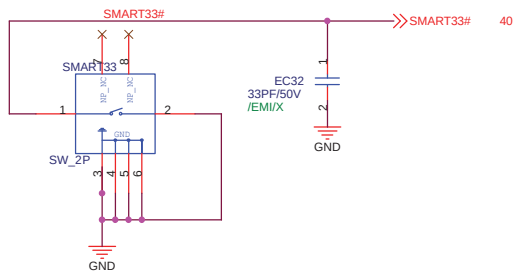


G_DDC_CLK	GC1	2	1	10PF/50V	/X
G_DDC_DATA	GC2	2	1	10PF/50V	/X
G_CLKP	GC3	2	1	10PF/50V	N/A
G_CLKN	GC4	2	1	10PF/50V	N/A
G_DATAP2	GC5	2	1	10PF/50V	N/A
G_DATAN2	GC6	2	1	10PF/50V	N/A
G_DATAP1	GC7	2	1	10PF/50V	N/A
G_DATAN1	GC8	2	1	10PF/50V	N/A
G_DATAP0	GC9	2	1	10PF/50V	N/A
G_DATAN0	GC10	2	1	10PF/50V	N/A
G_NBL_CTRL	GC12	2	1	10PF/50V	/X
BL_EN	EC11	2	1	10PF/50V	EMI/X
G_LVDD_EN	EC12	2	1	10PF/50V	EMI/X



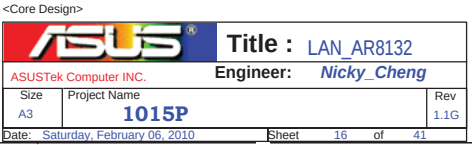
<Core Design>

		Title : LVDS Conn_LID	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size Custom	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010	Sheet	14	of 42

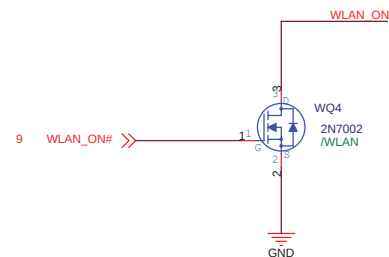
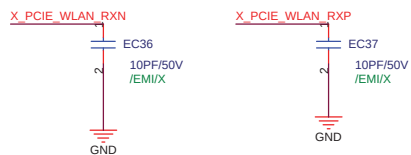
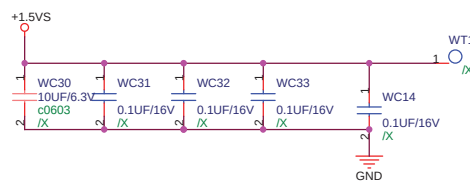
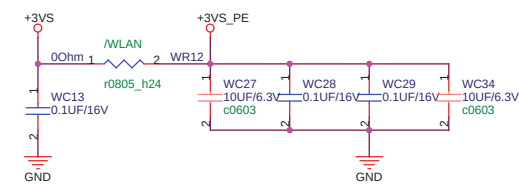
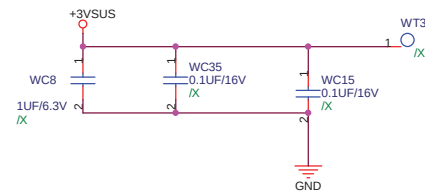
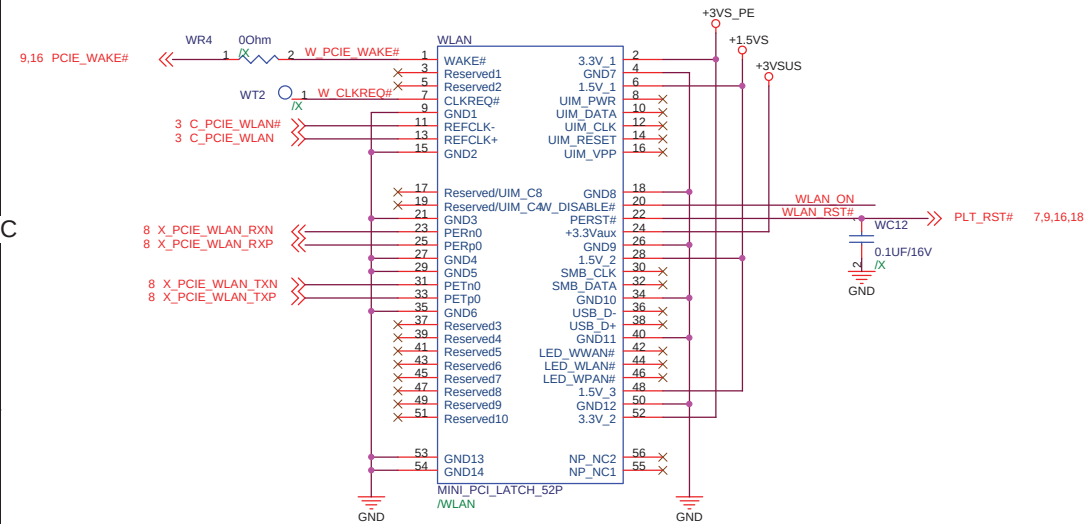


<Core Design>

		Title : <u>WIFI_SAMRT33</u>	
ASUSTek Computer INC.		Engineer: <u>Nicky_Cheng</u>	
Size A3	Project Name 1015P		Rev 1.1G
Date: <u>Saturday, February 06, 2010</u>		Sheet	<u>15</u> of <u>42</u>

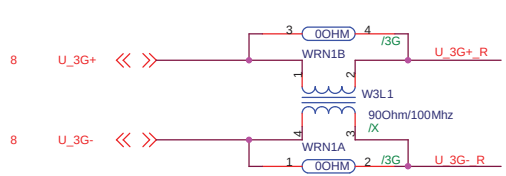


WIFI use PCIE 1.1 Spec
+3VS = 1.0A peak / 0.75A Normal
+1.5VS = 0.5A peak / 0.375A Normal
+3VSUS = 0.375A peak / 0.25A Normal

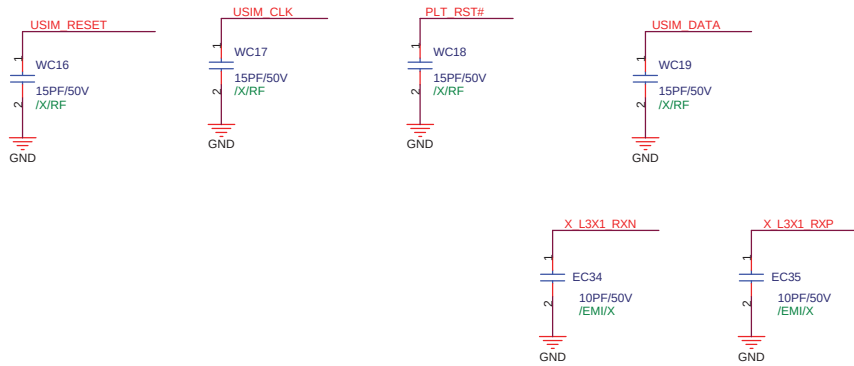
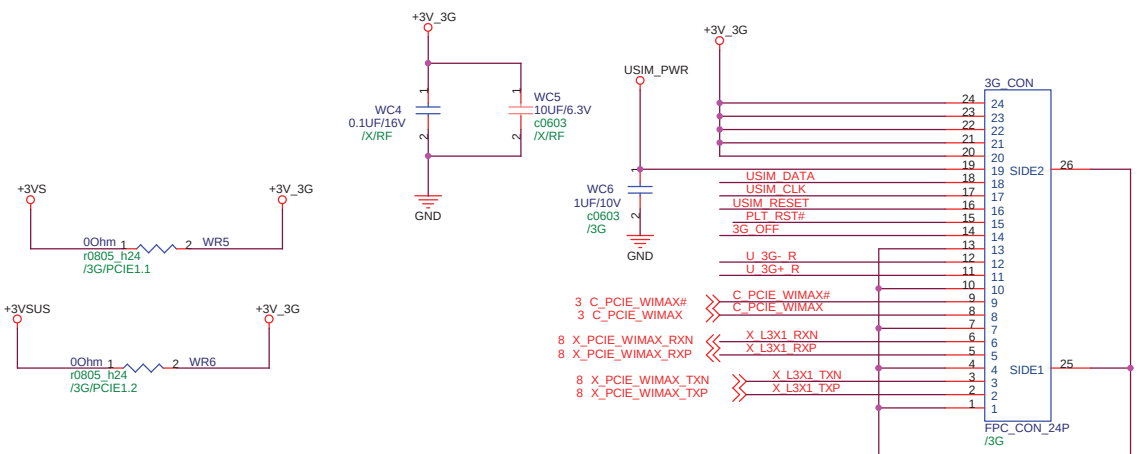
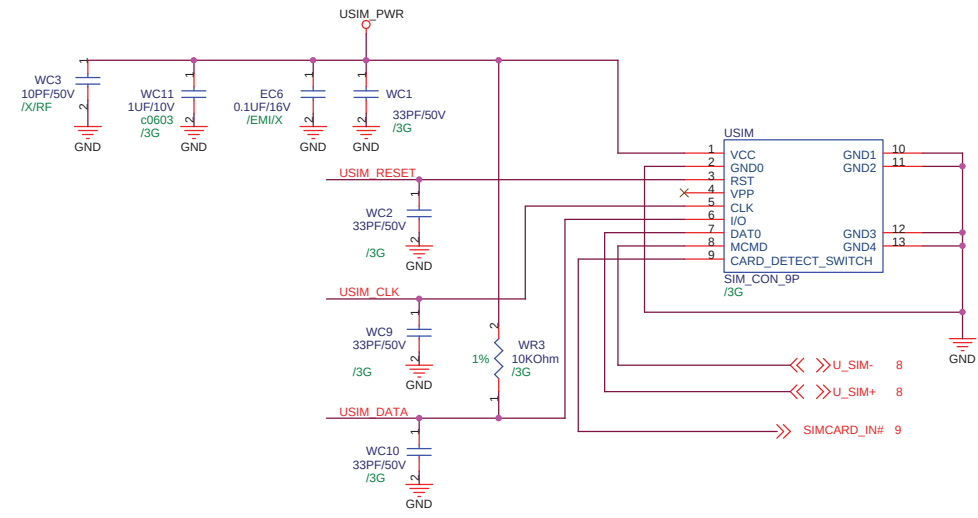


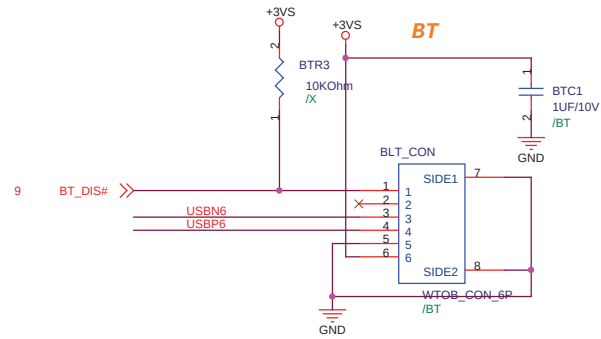
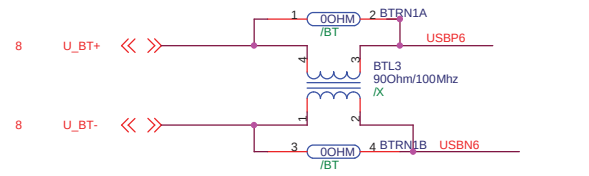
<Core Design>

ASUS®		Title : WLAN	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P		Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 17 of 42	

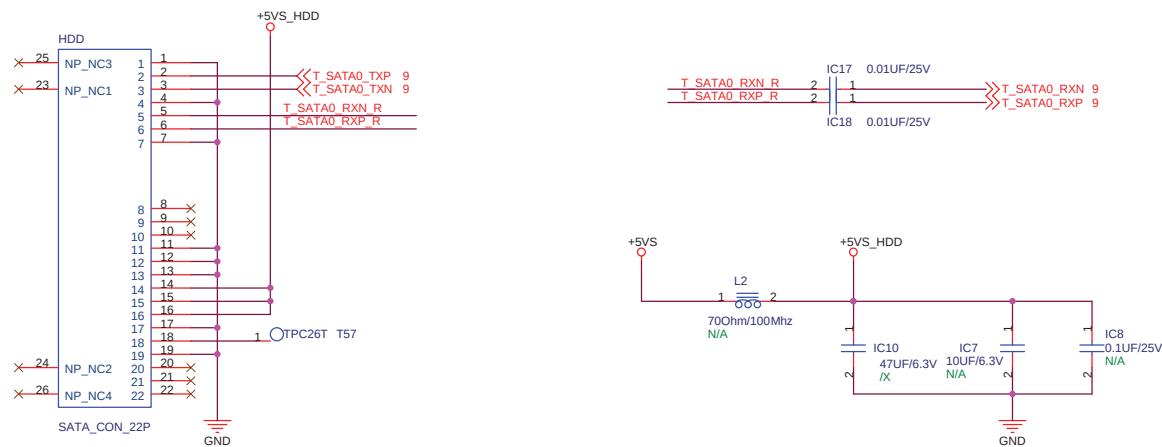


7,9,16,17 PLT_RST# >>>
9 3G_OFF >>>





SATA HDD Connector





<Core Design>



Title : USB3.0

ASUSTek Computer INC.

Engineer:

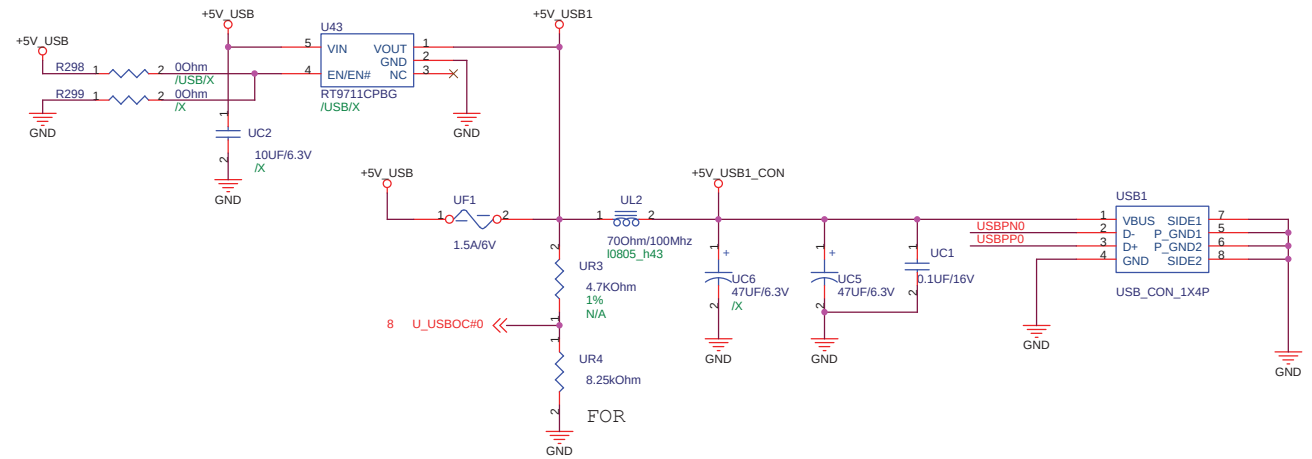
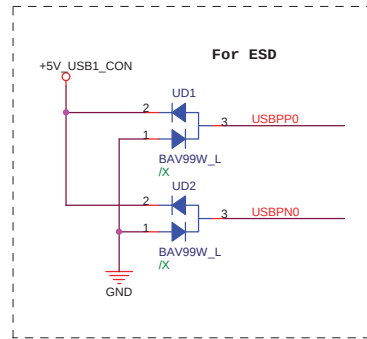
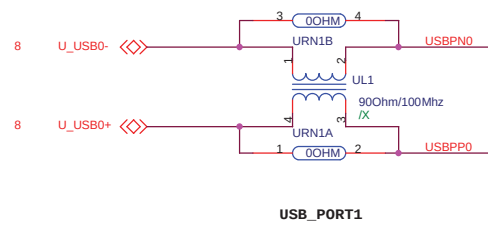
Size	Project Name	Rev
C	1015P	1.1G

Date: Saturday, February 06, 2010Sheet 21 of 42



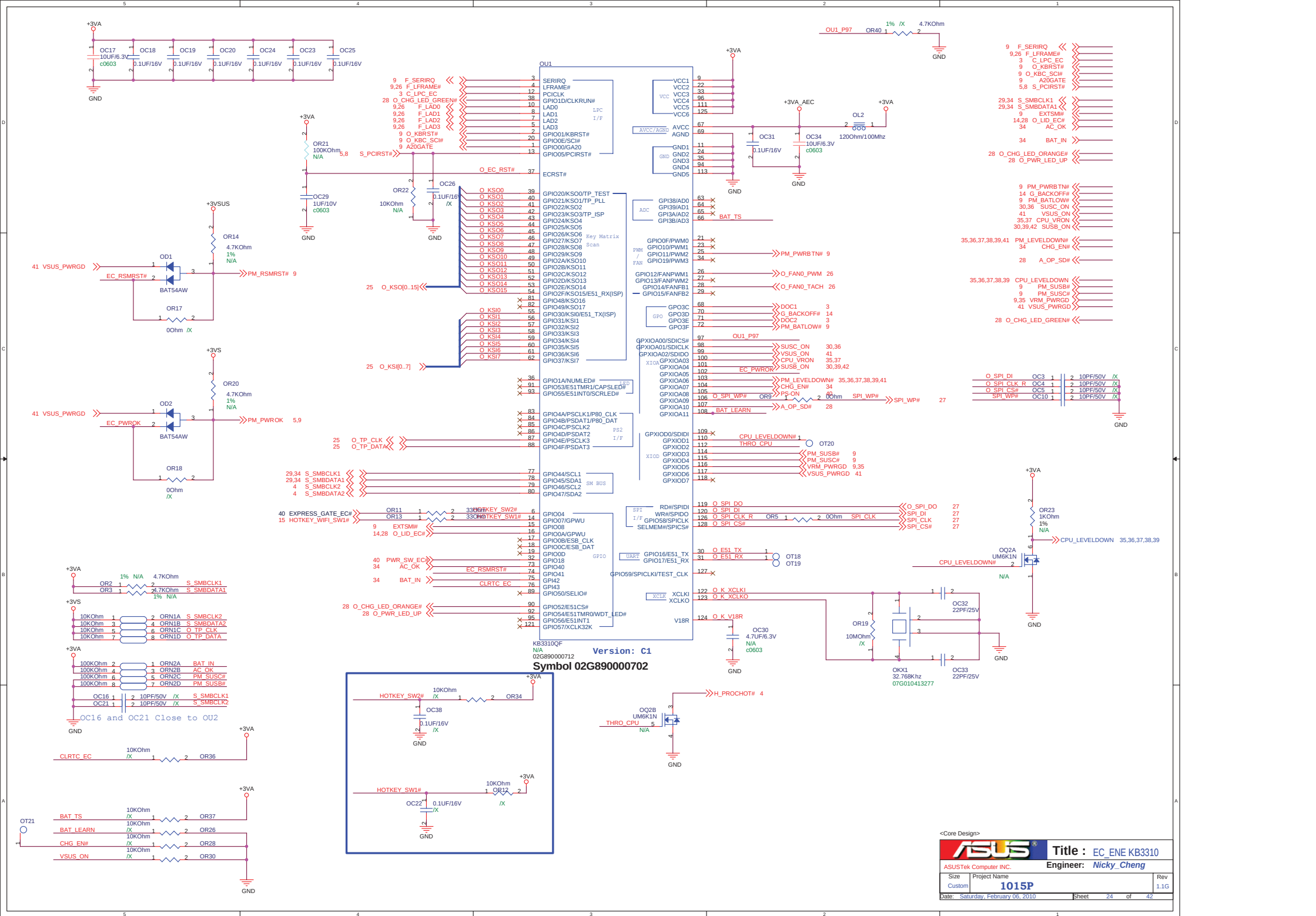
<Core Design>

		Title : USB 3.0	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P		Rev 1.1G
Date: Saturday, February 06, 2010		Sheet 22 of 42	

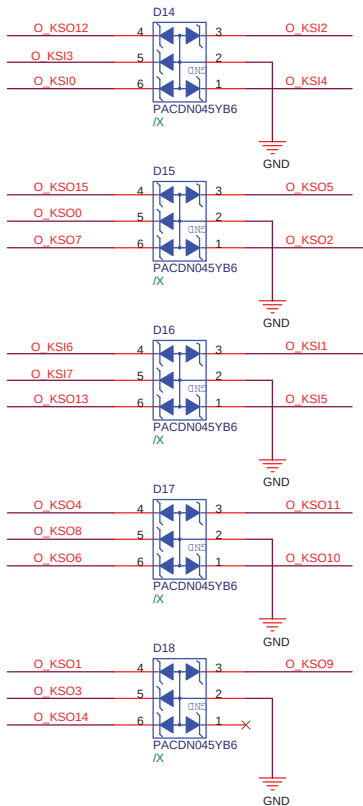
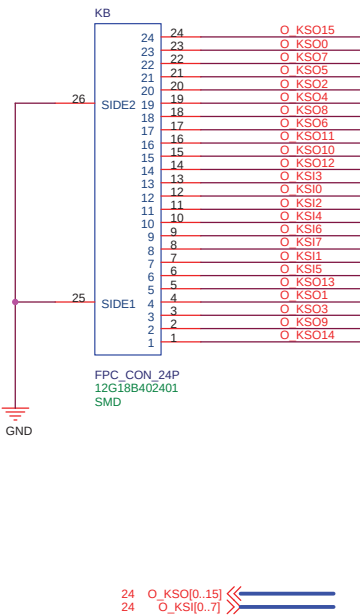


<Core Design>

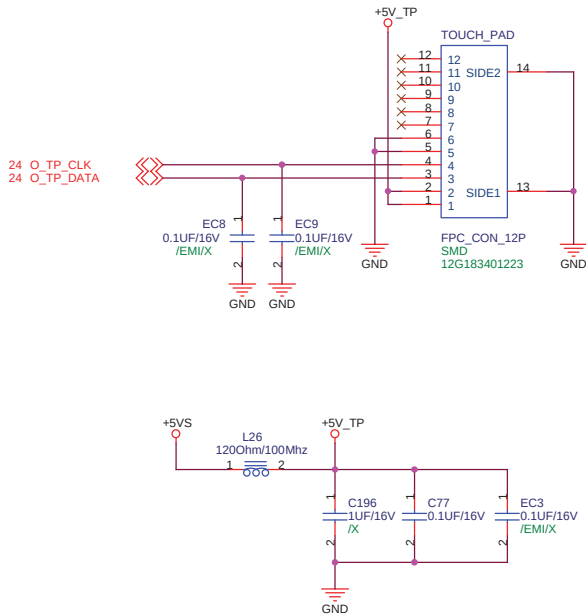
ASUS		Title : USB Port1	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A3	Project Name 1015P	Rev 1.1G	
Date: Saturday, February 06, 2010		Sheet 23 of 42	

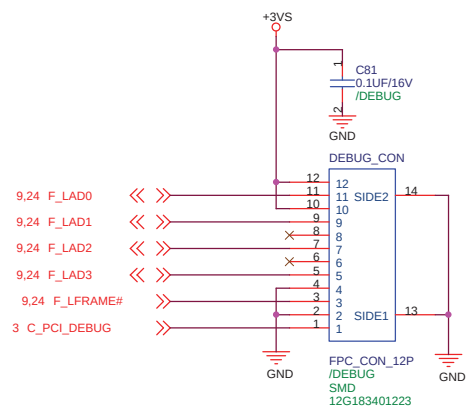
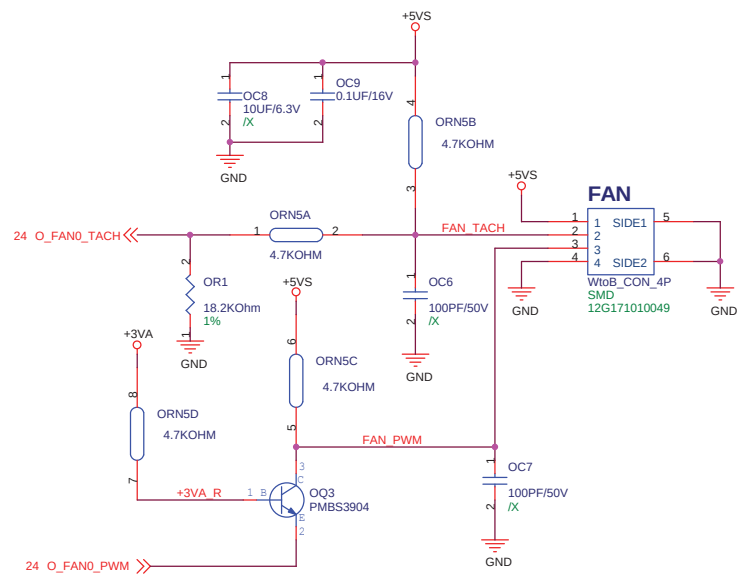


For Keyboard Connector



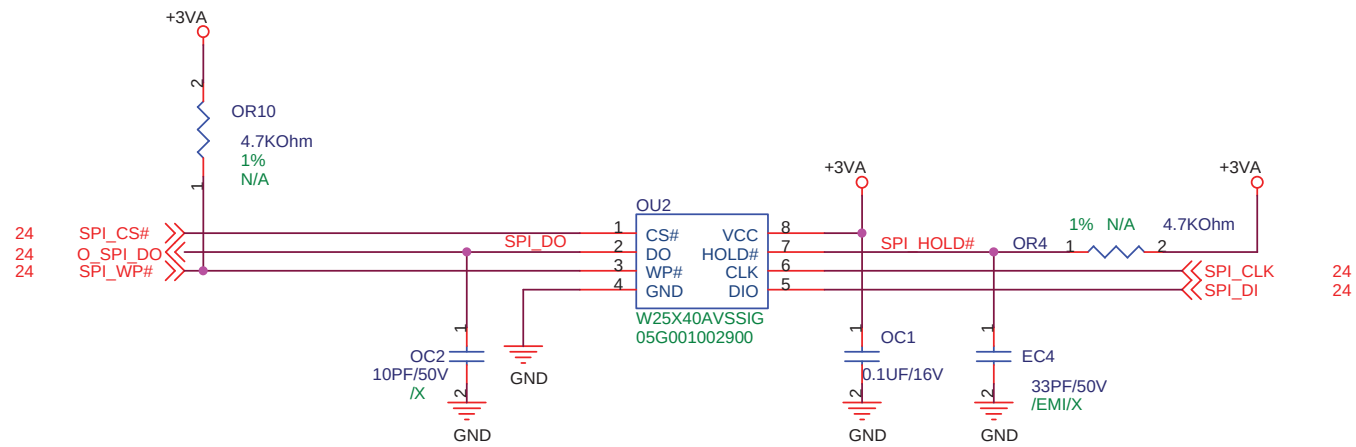
For Touch-Pad





<Core Design>

		Title : <u>Fan_Debug</u>	
ASUSTek Computer INC.		Engineer: <u>Nicky_Cheng</u>	
Size A3	Project Name 1015P		Rev 1.1G
Date: Saturday, February 06, 2010	Sheet	26 of 42	



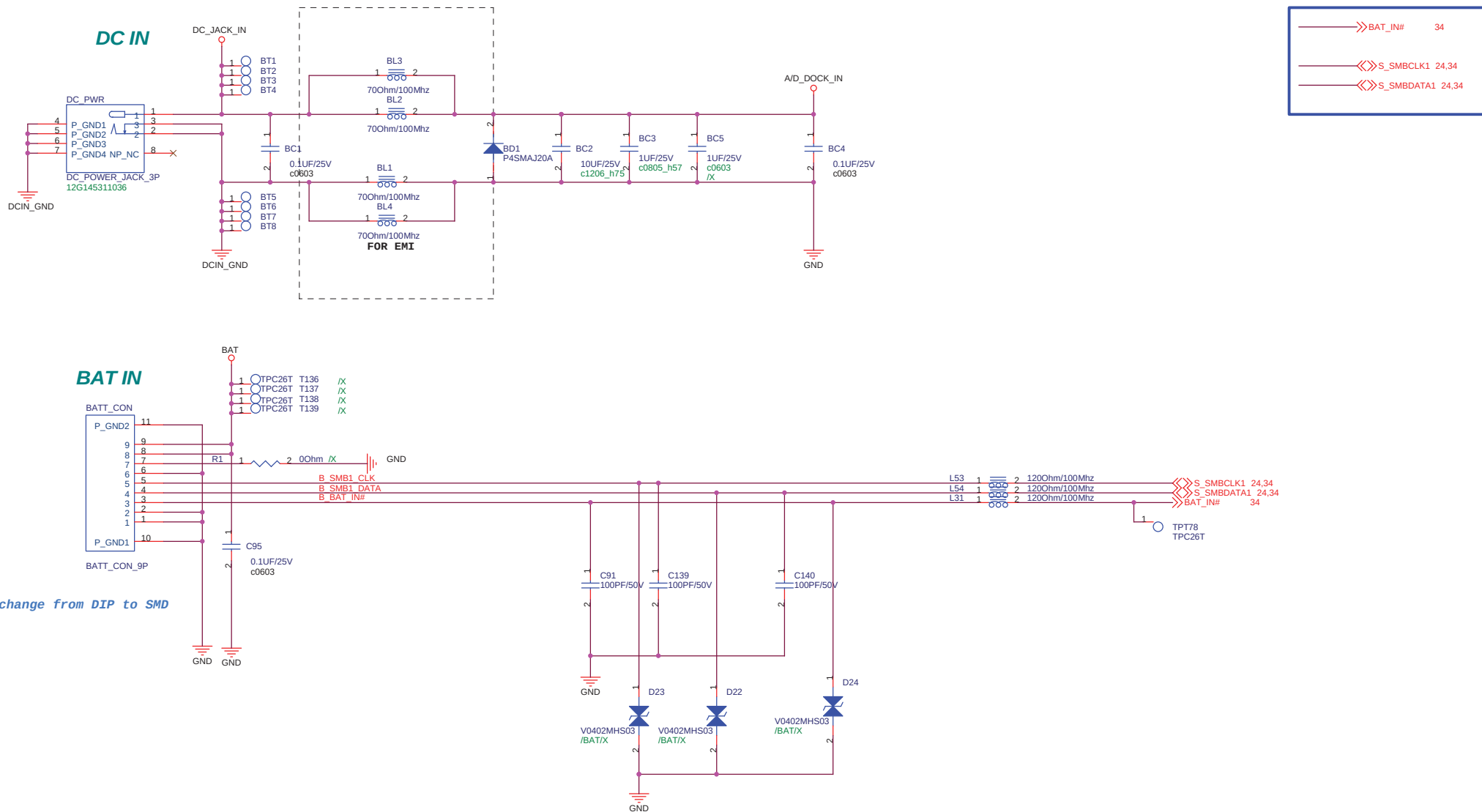
05G001002900;
05G00100F131;
05G00100F133

<Core Design>

ASUS®		Title : SPI_ROM	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size A4	Project Name 1015P		Rev 1.1G
Date: Saturday, February 06, 2010		Sheet	27 of 42

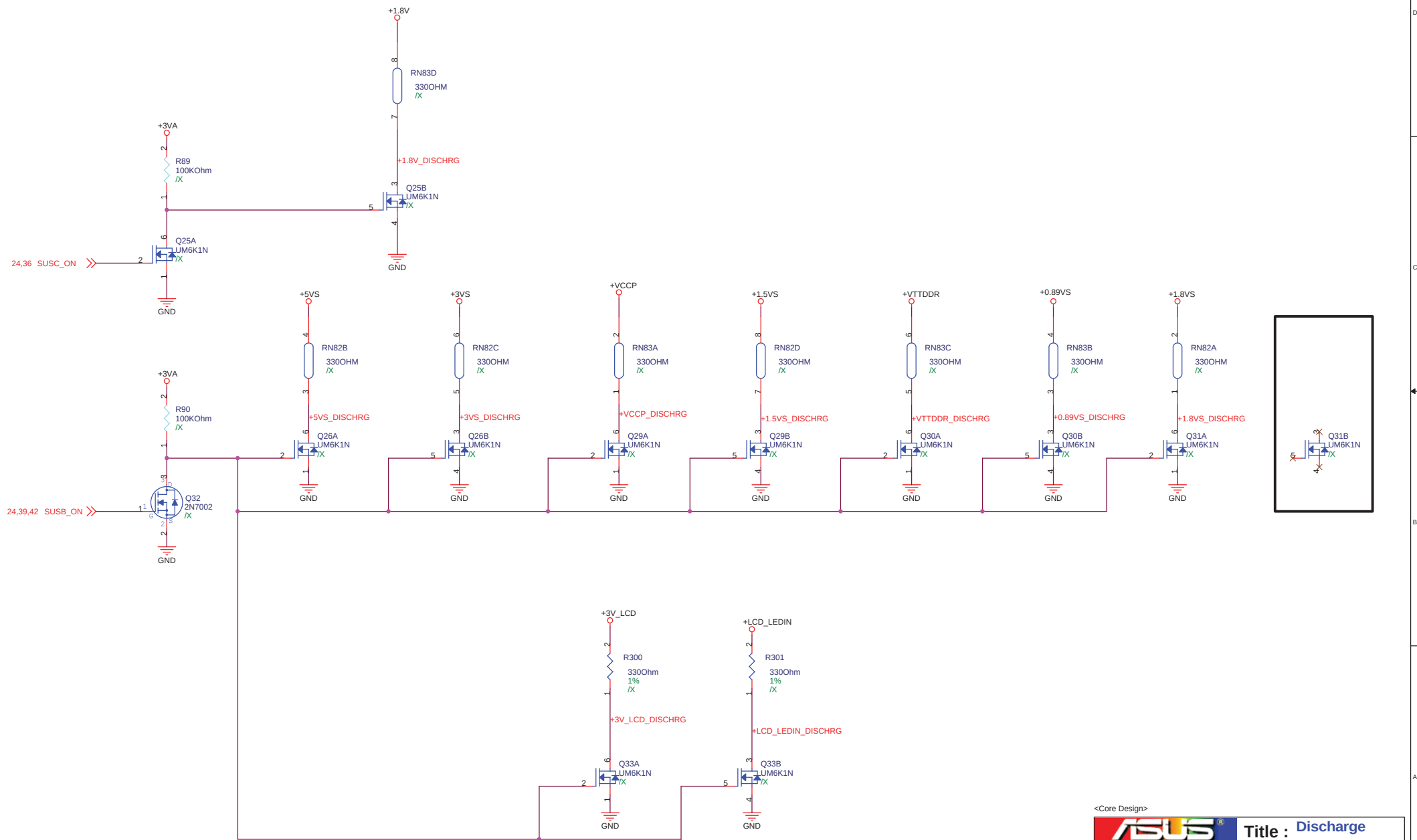


0.1B Beta



<Core Design>

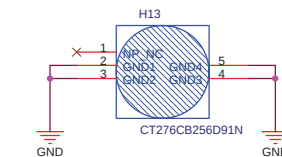
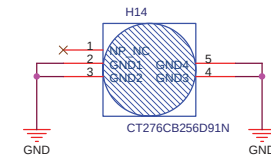
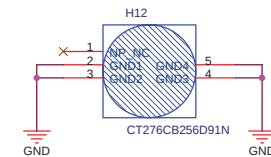
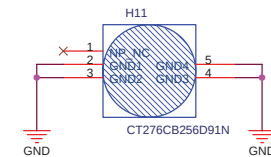
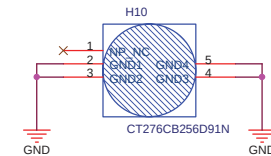
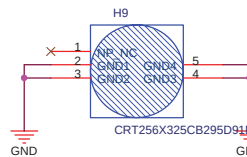
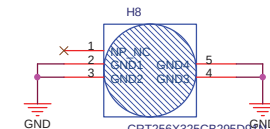
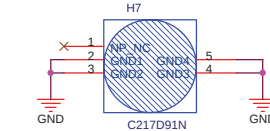
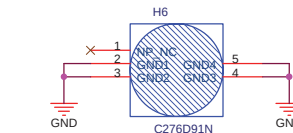
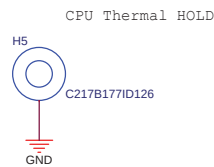
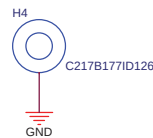
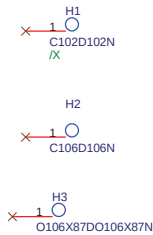
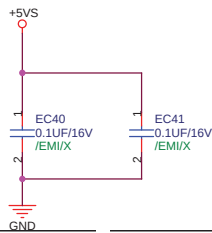
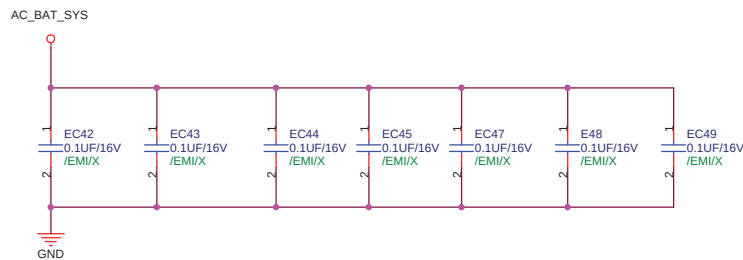
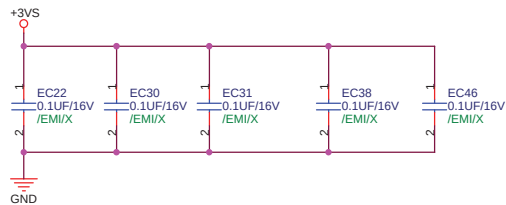
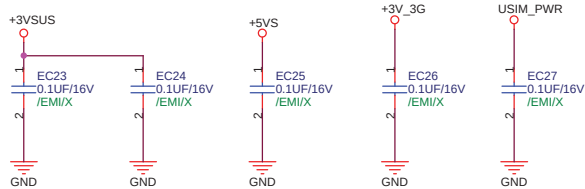
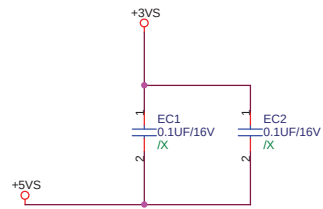
ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size	Project Name	Rev	
A3	1015P	1.1G	
Date: Saturday, February 06, 2010		Sheet	29 of 42





<Core Design>

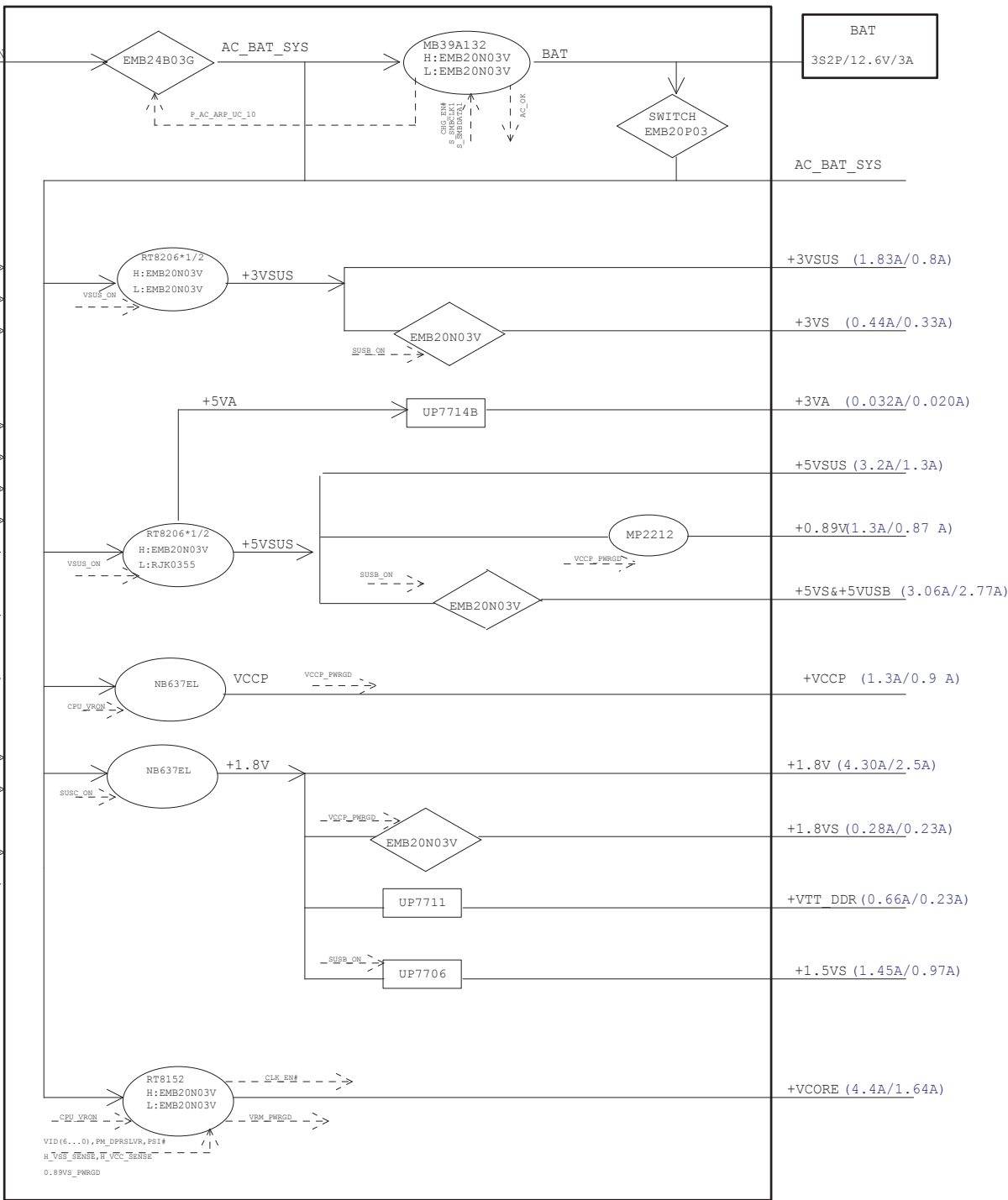
		Title : SD_CON	
ASUSTek Computer INC.		Engineer: Nicky_Cheng	
Size	Project Name		Rev
A3	1015P		1.1G
Date: Saturday, February 06, 2010		Sheet	31 of 42



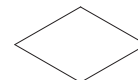
Adaptor
40W (19V/2.1A)

EC

CPU



Switching



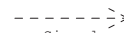
Switch



Linear



Current flow

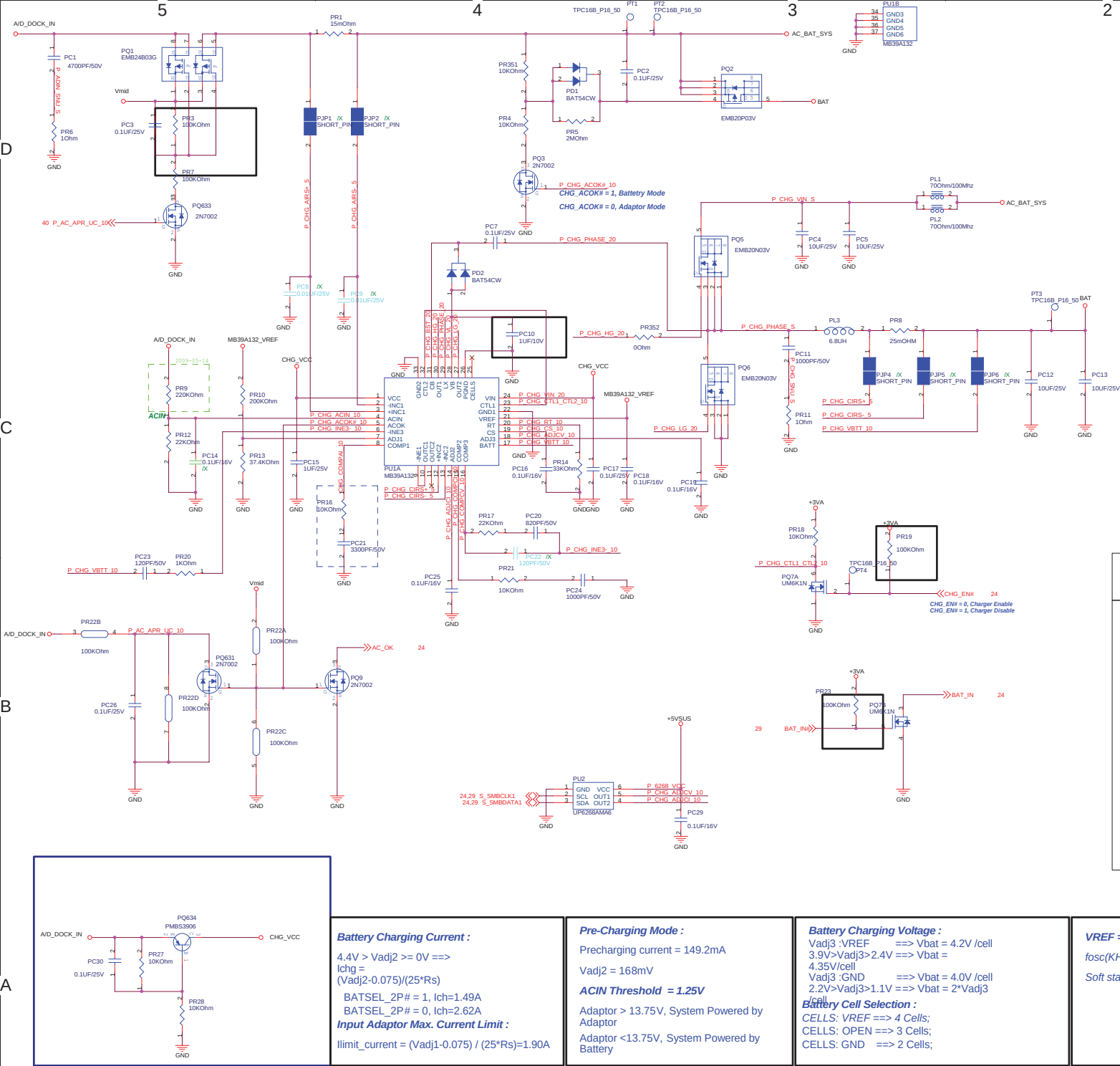


Signal



Device

STD version :1.02G(09/12/2)



Power stage

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$$

2. Ripple Current:

$$I_{rip} = 1.18A$$

$$I_{spec} = 2A$$

$$\phi 1 \text{ pcs}$$

3. Inductor Spec:

$$I_{sat} = 10A$$

$$I_{dc} = 5.5A$$

$$DCR = 37m\Omega$$

4. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ m}\Omega \quad (V_{gs} = 4.5 \text{ V})$$

$$I_{cont} = 6.5 \text{ A} \quad (T = 25^\circ \text{C})$$

$$I_{peak} = 40 \text{ A} \quad (\text{Pause} \geq 10 \text{ us})$$

L-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ m}\Omega \quad (V_{gs} = 4.5 \text{ V})$$

$$I_{cont} = 6.5 \text{ A} \quad (T = 25^\circ \text{C})$$

$$I_{peak} = 40 \text{ A} \quad (\text{Pause} \geq 10 \text{ us})$$

Controller

1. Voltage & Current:

$$+12.6V @ 2.5A$$

2. Frequency:

$$PR122 = 33K\Omega, \text{ Fosc} = 515KHz$$

3. OCP:

$$POR \text{ Hysteresis} = 0.1V$$

$$V_{on} = 7.5V$$

4. POR:

$$POR \text{ Hysteresis} = 0.1V$$

$$V_{on} = 7.5V$$

5. Enable Voltage:

$$V = 2.9 \text{ V}$$

6. Soft start time:

$$T_{ss} = 23ms$$

7. Phase selection:

$$N/A$$

8. Inrush Current:

$$C_{total} = 20\mu F$$

$$I_{inrush} = 0.01A$$

Battery Charging Current :

$$4.4V > V_{adj2} \geq 0V \Rightarrow$$

$$I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$$

$$BATSEL_2P\# = 1, I_{ch} = 1.49A$$

$$BATSEL_2P\# = 0, I_{ch} = 2.62A$$

Input Adaptor Max. Current Limit :

$$I_{limit_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$$

Pre-Charging Mode :

$$\text{Precharging current} = 149.2mA$$

$$V_{adj2} = 168mV$$

$$ACIN \text{ Threshold} = 1.25V$$

$$\text{Adaptor} > 13.75V, \text{ System Powered by Adaptor}$$

$$\text{Adaptor} < 13.75V, \text{ System Powered by Battery}$$

Battery Charging Voltage :

$$V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / \text{cell}$$

$$3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} =$$

$$4.35V / \text{cell}$$

$$V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / \text{cell}$$

$$2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3}$$

Battery Cell Selection :

$$CELLS : V_{REF} \Rightarrow 4 \text{ Cells;}$$

$$CELLS : OPEN \Rightarrow 3 \text{ Cells;}$$

$$CELLS : GND \Rightarrow 2 \text{ Cells;}$$

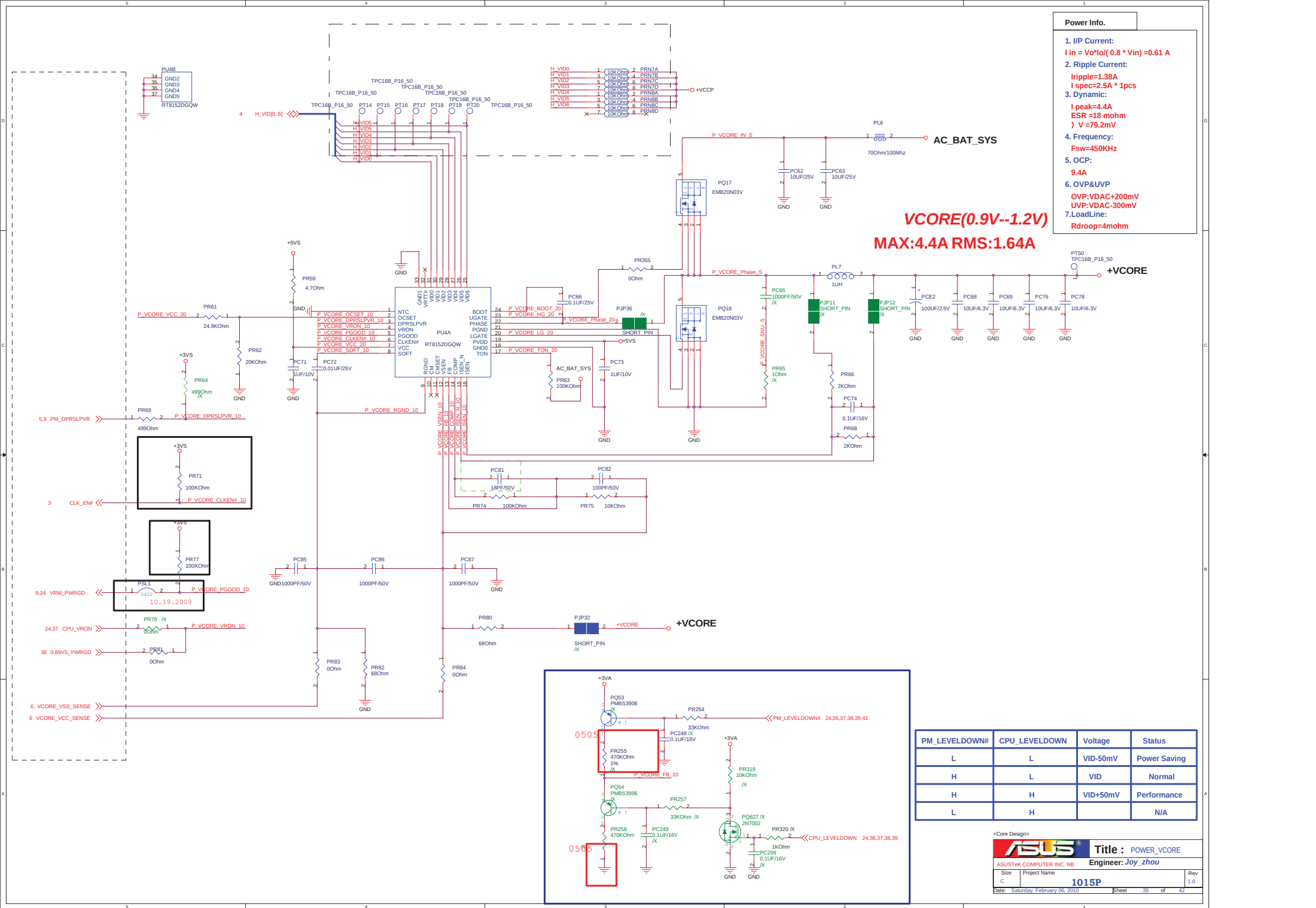
VREF = 5.0V

$$f_{osc}(KHz) = 17000 / RT (K\Omega)$$

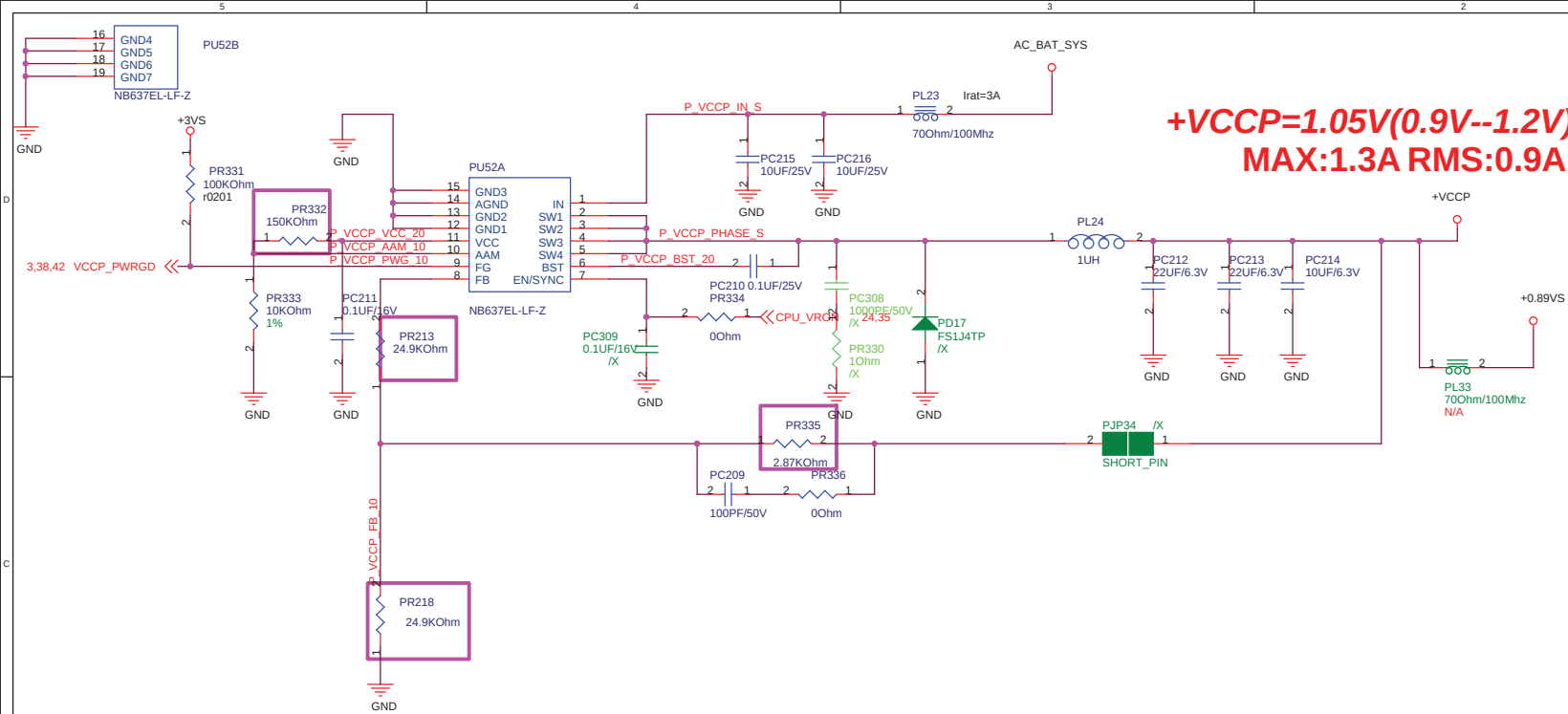
$$\text{Soft start: } t_{s(s)} = 0.13 \cdot CS (\mu F)$$

<Core Design>

ASUS		Title : Charger	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	<Rev Code>
A2	1008P		
Date: Saturday, February 05, 2010		Sheet 34 of 32	



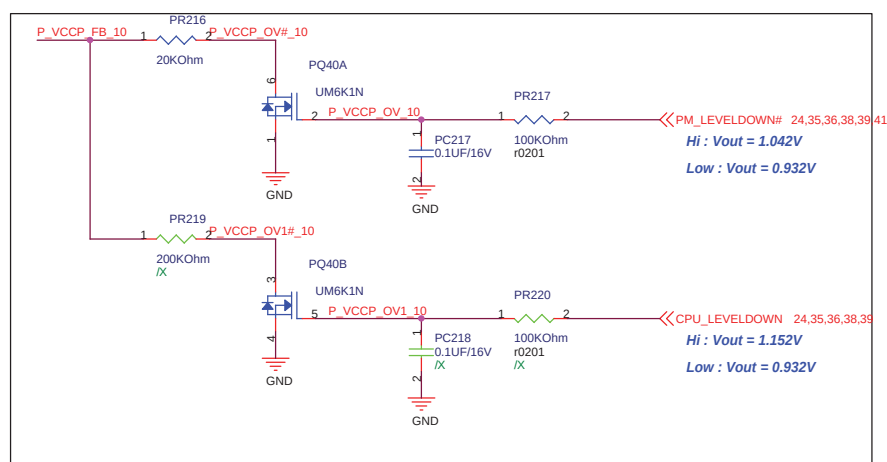


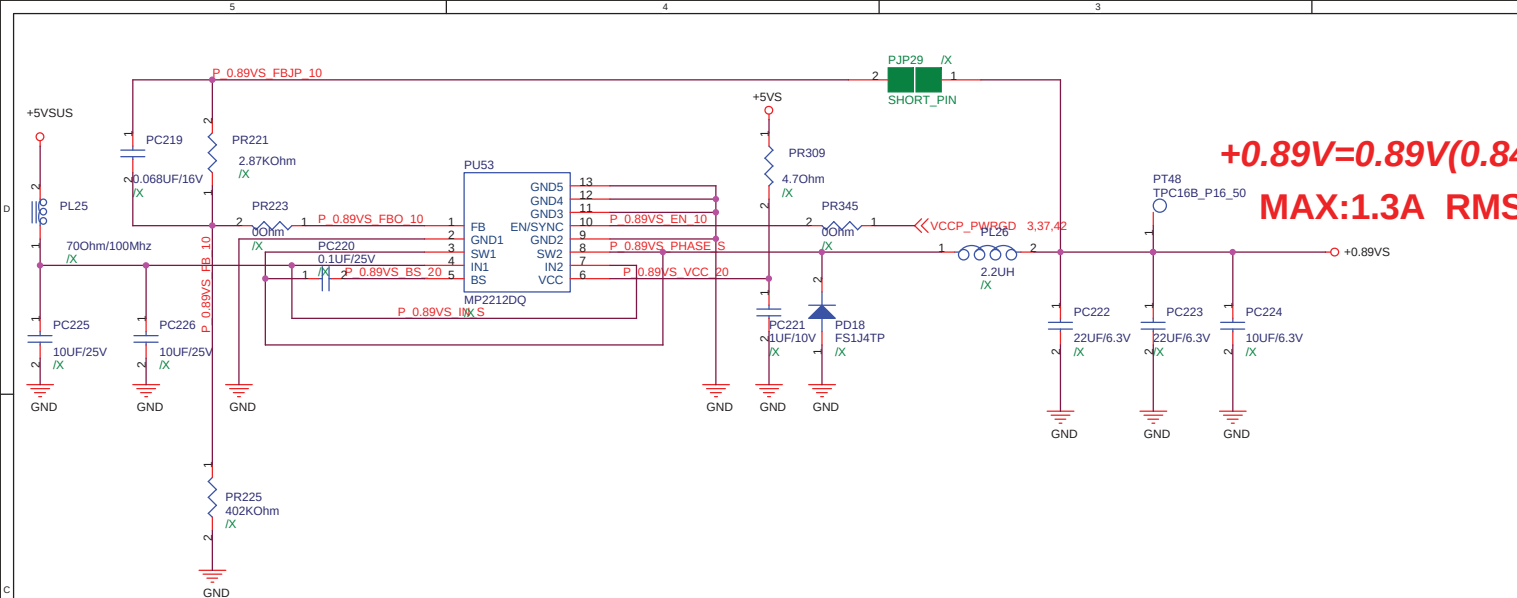


2009.11.27

CPU_VRON 24,35
 PM_LEVELDOWN# 24,35,36,38,39,41
 CPU_LEVELDOWN 24,35,36,38,39

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.932V	Power Saving
H	L	H	1.042V	Normal
H	H	L	1.127V	Performance
L	H	L		N/A





Power Info.

1. I/P Current:

$$I_{in} = V_o * I_o / (0.8 * V_{in}) = 0.36A$$

2. Ripple Current:

$$I_{rip} = 0.61A$$

$$I_{spec} = 2.5A * 1pc$$

3. Dynamic:

$$I_{peak} = 1.6A$$

$$ESR = 18 \text{ mohm}$$

$$V = 28.8mV$$

4. Frequency:

$$F_{osc} = 600KHz$$

5. Current Limit:

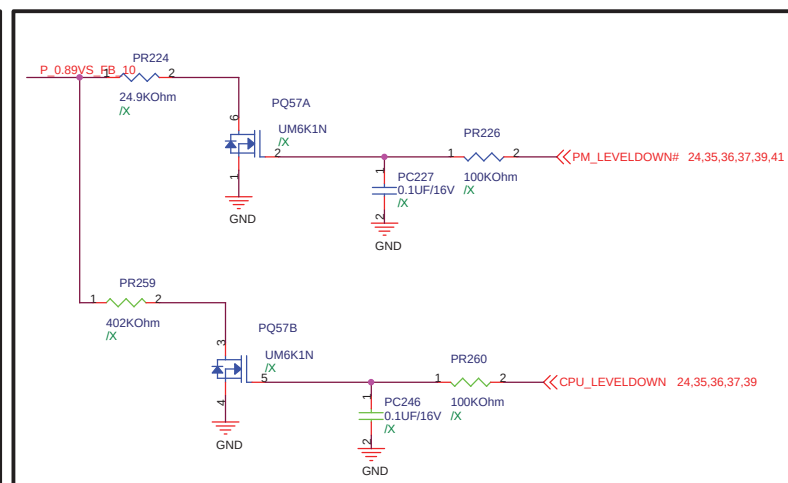
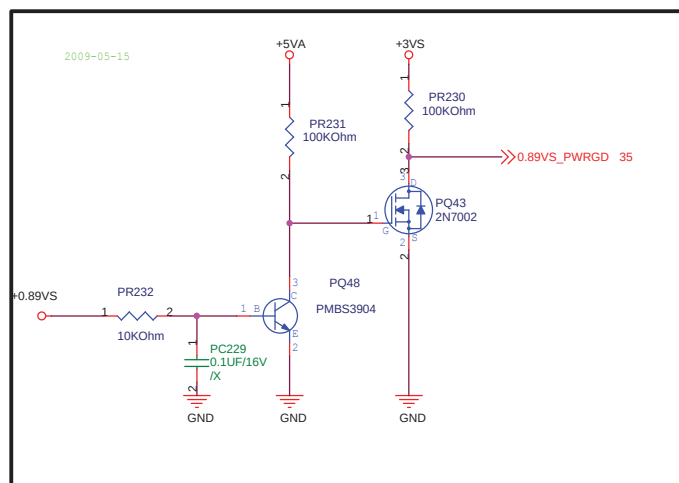
$$6A$$

2009.11.27

《VCCP_PWRGD 3.37.42

《PM_LEVELDOWN# 24,35,36,37,39,41

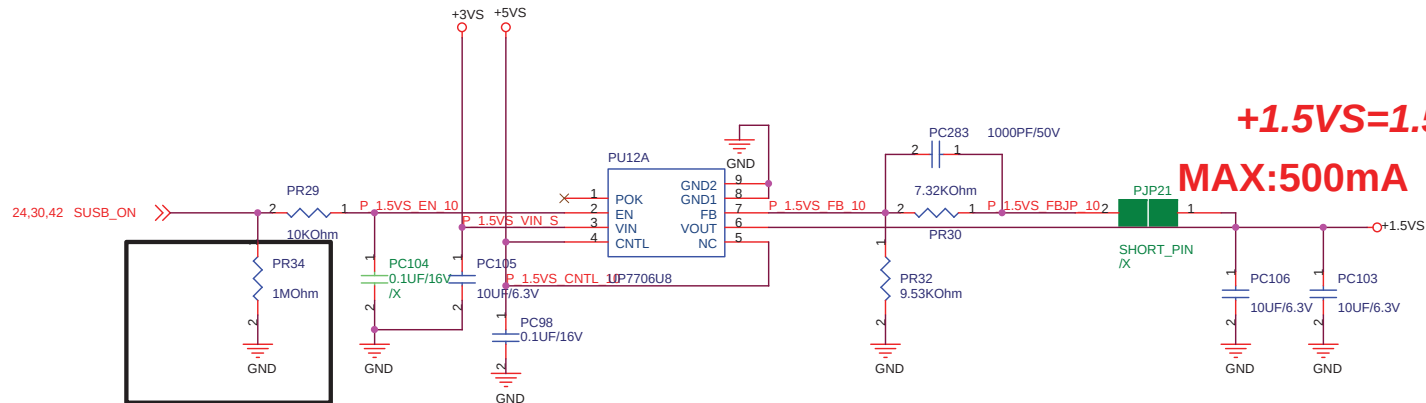
《CPU_LEVELDOWN 24,35,36,37,39



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	0.844V	Power Saving
H	L	0.897V	Normal
H	H	0.950V	Performance
L	H		N/A

<Core Design>

ASUS		Title : +1.5VS +2.5VS	
ASUSTek Computer INC		Engineer: Joy_Zhou	
Size	Project Name	Rev	
A3	1015P	1.0	
Date: Saturday, February 06, 2010	Sheet	38	of 42



+1.5VS=1.5V(1.44V--1.5V)
MAX:500mA RMS:350mA

1. Dropout Voltage:

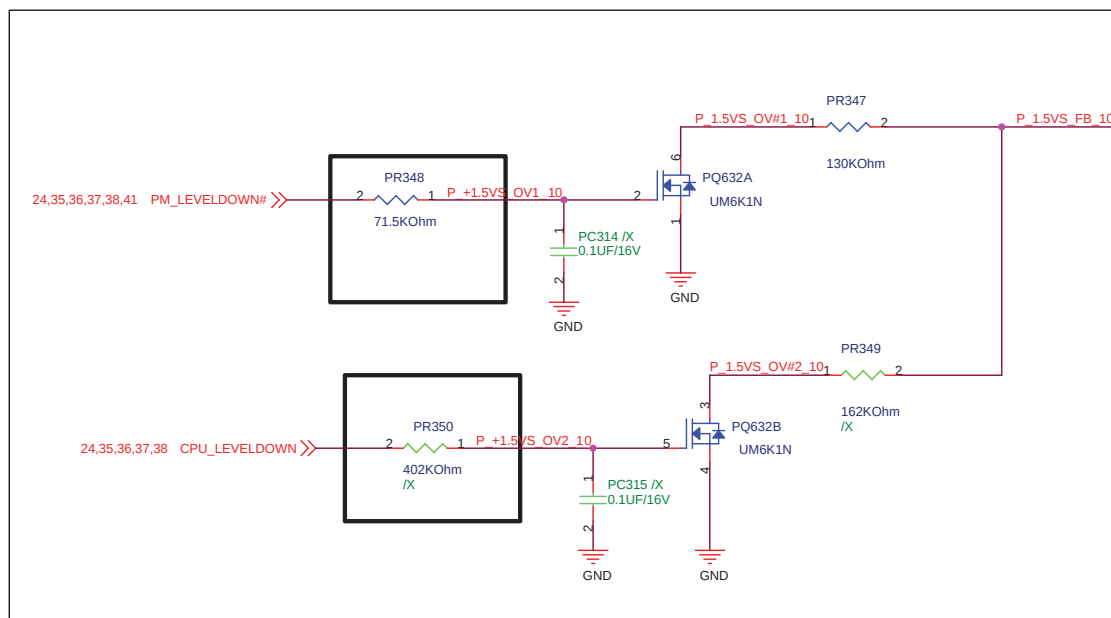
V= 300 mV (I_o=2A)

2. Current Limit:

I limit= 2.8A

3. Pd:

R thjc =5 C/W
Pd =1.9W

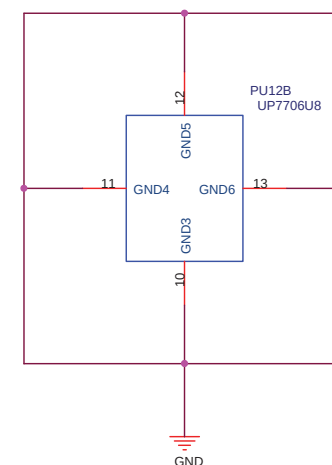


2009.11.27

24,30,42 SUSB_ON >>

24,35,36,37,38,41 PM_LEVELDOWN# >>

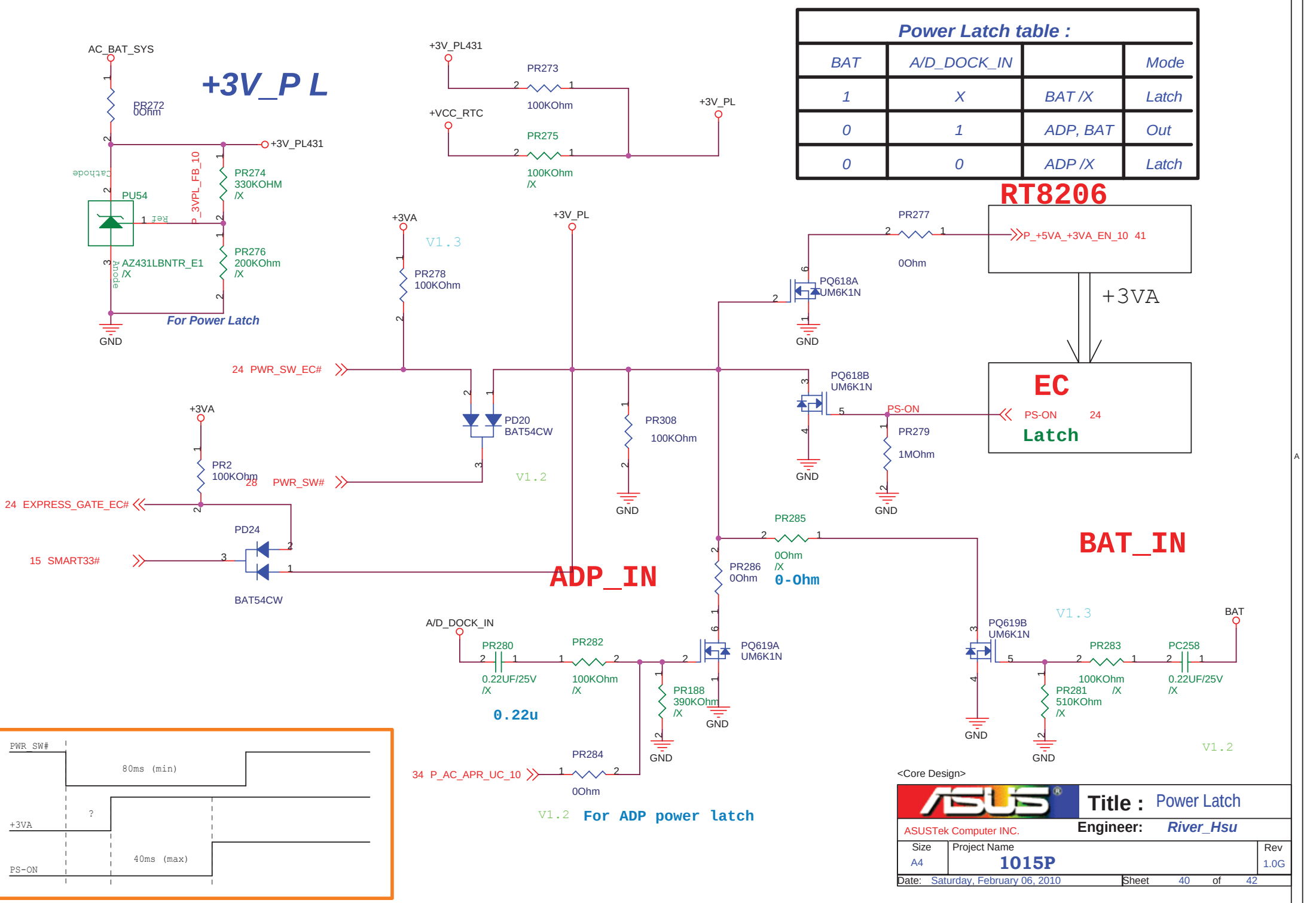
24,35,36,37,38 CPU_LEVELDOWN >>



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	1.41V	Power Saving
H	L	1.49V	Normal
H	H	1.51V	Performance
L	H	1.50V	

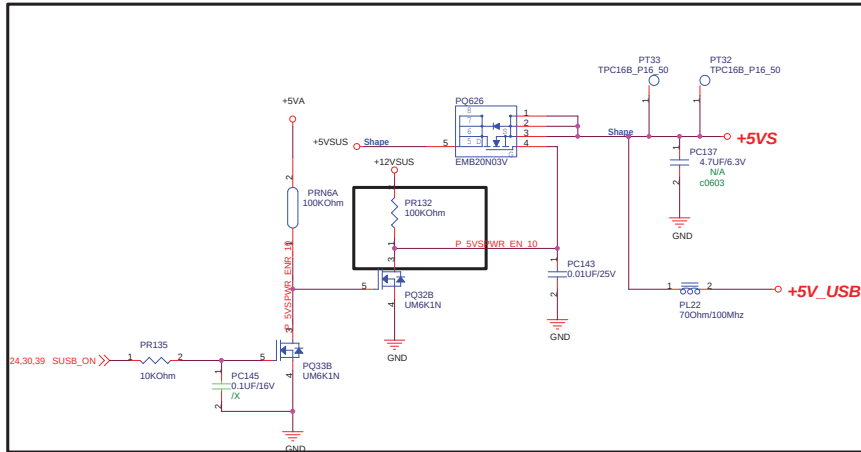
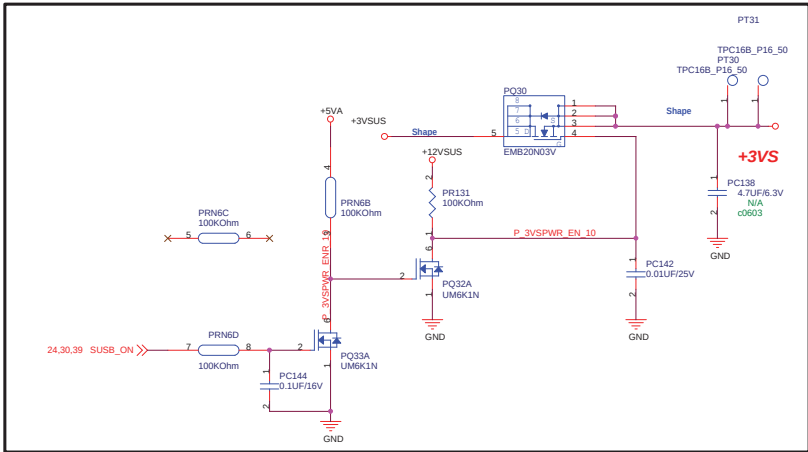
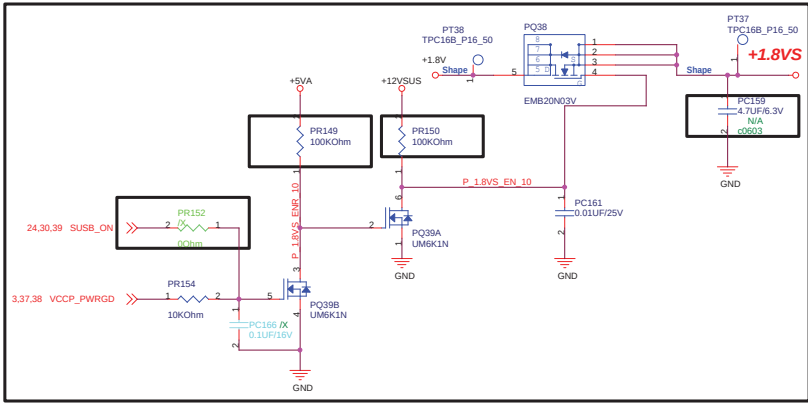
<Core Design>

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC		Engineer: Joy Zhou	
Size B	Project Name 1015P		Rev 1.0
Date: Saturday, February 06, 2010		Sheet 39	of 42



<Core Design>

ASUS		Title : Power Latch	
ASUSTek Computer INC.		Engineer: River_Hsu	
Size A4	Project Name 1015P		Rev 1.0G
Date: Saturday, February 06, 2010		Sheet 40 of 42	



2009.11.27

24,30,39 SUBS_ON

3,37,38 VCCP_PWRGD