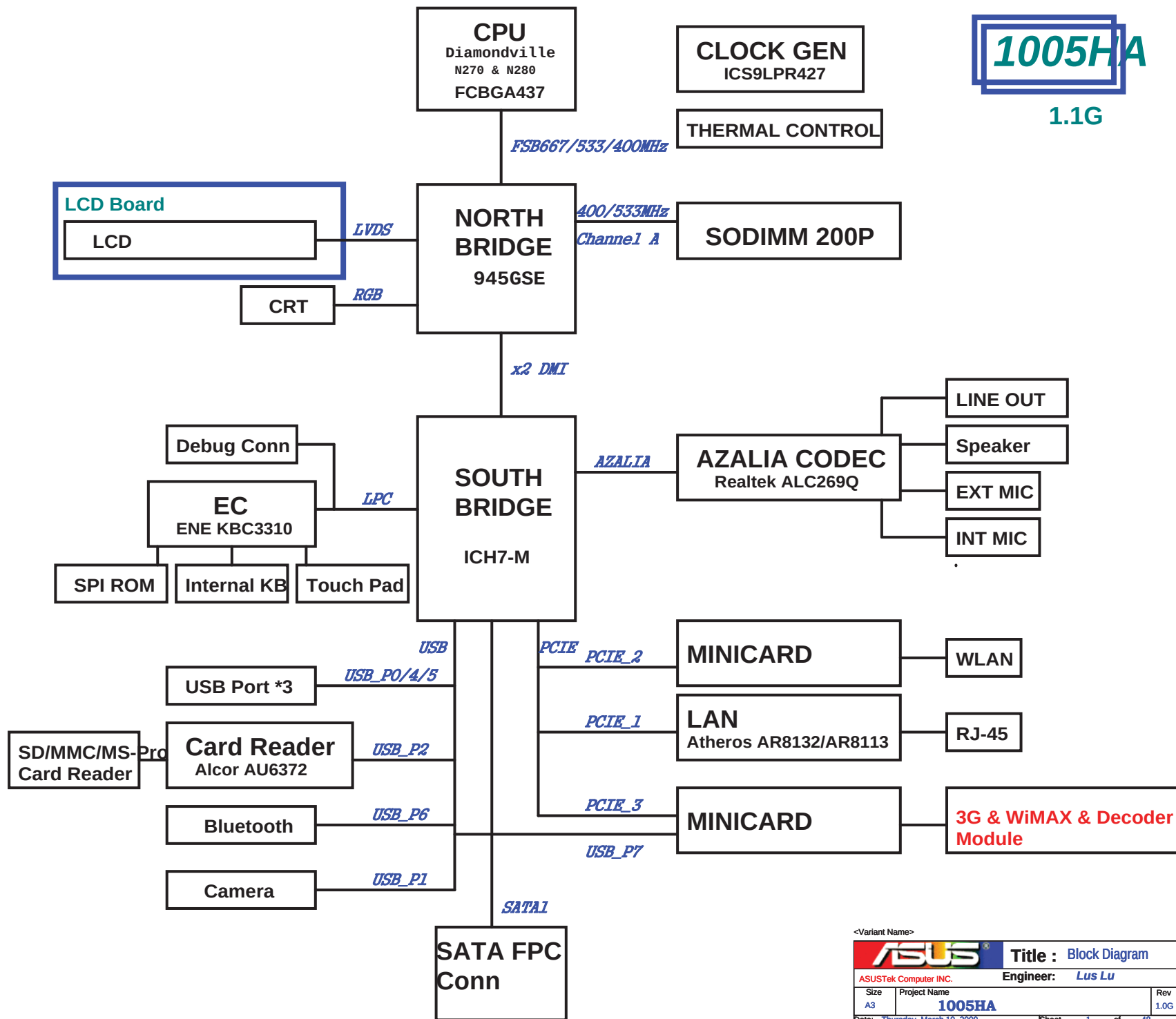


01_Block Diagram
02_System Setting
03_Power Sequence
04_Clock Gen_ICS9LPR434
05_Diamondville_BUS
06_Diamondville_PWR
07_NB-945GMS(HOST)
08_NB-945GMS(DMI)
09_NB-945GMS(GRAPHIC)
10_NB-945GMS(DDR2)
11_NB-945GMS(PWR)
12_NB-945GMS(PWR2)
13_NB-945GMS(GND)
14_SB-ICH7M(PWR)
15_SB-ICH7M(1)
16_SB-ICH7M(2)
17_SB-ICH7M(3)
18_DDR2 SODIMM
19_DDR2 Termination
20_Onboard VGA
21_LCD Conn_LID
22_Blank
23_Mini WIFI+ BT
24_LAN_Atheros AR8113
25_RJ45
26_Flash Conn
27_USB Port
28_Camera Conn
29_Card Reader_AU6372A51
30_Codec_ALC269
31_Audio_AMP_Jack
32_EC_ENE KB3310
33_EC
34_Switch_SPI ROM_Debug Conn
35_Thermal Sensor_FAN
36_KB_Touch Pad
37_LED_THERMTRIP
38_Discharge
39_PWR Jack
40_Srew Hole
41_EMI
42_POWER FLOW
43_Vcore
44_Power System
45_Power_+1.8V & VTTDDR
46_Power_VCCP
47_Power_+1.5VS & +2.5VS
48_Power_Charger
49_EC Pin Define
49_History



EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera

PCIE

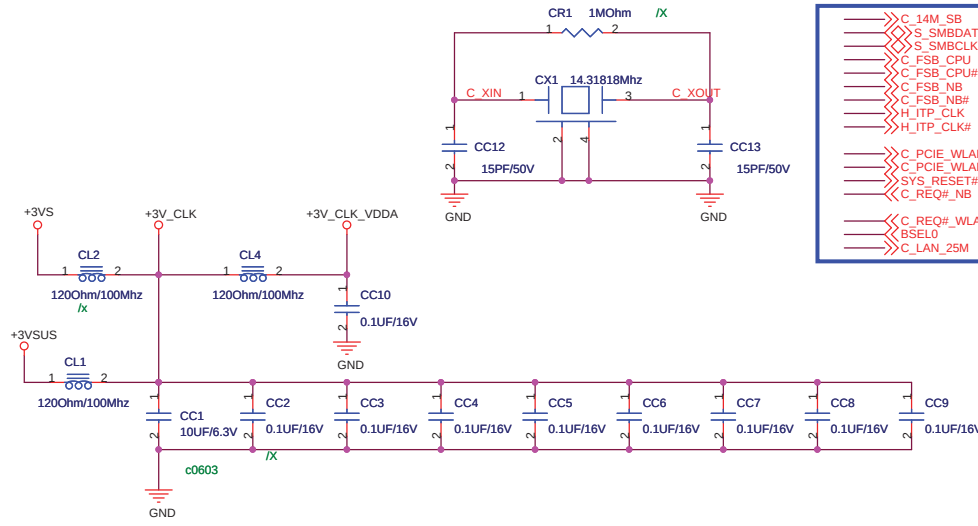
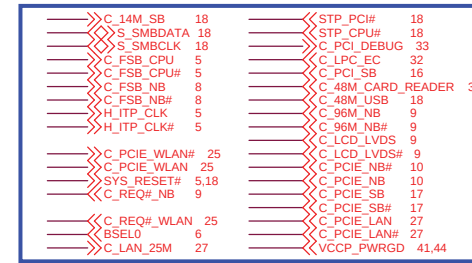
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Variant Name>

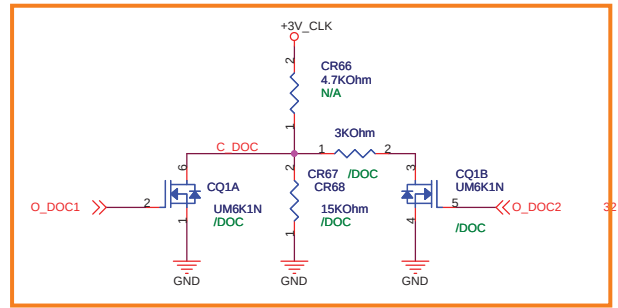
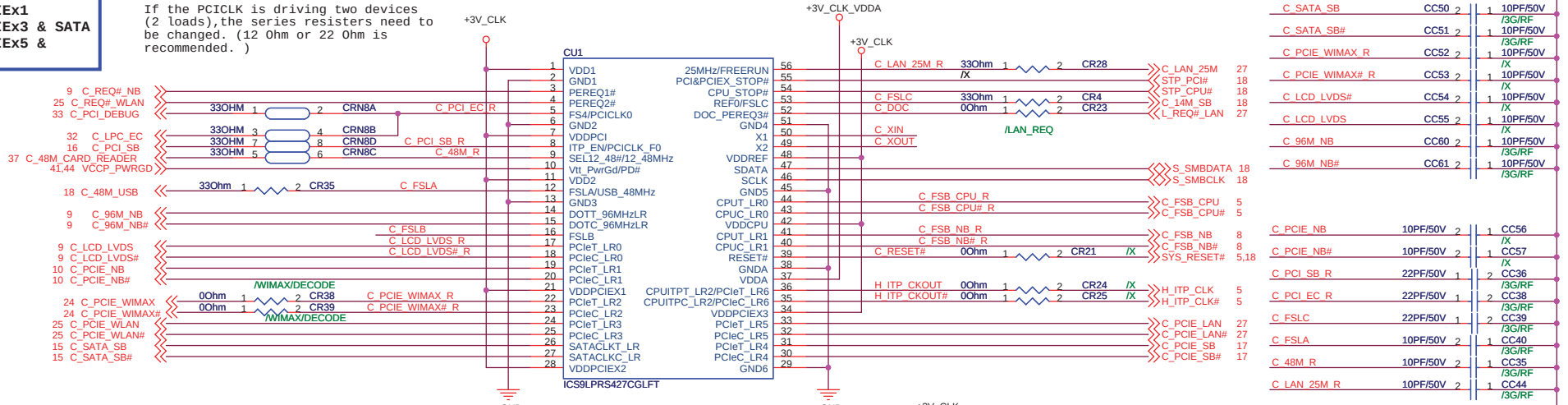
		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size A3	Project Name 1005HA		Rev 1.0G
Date: Thursday, March 19, 2009		Sheet 2	of 48



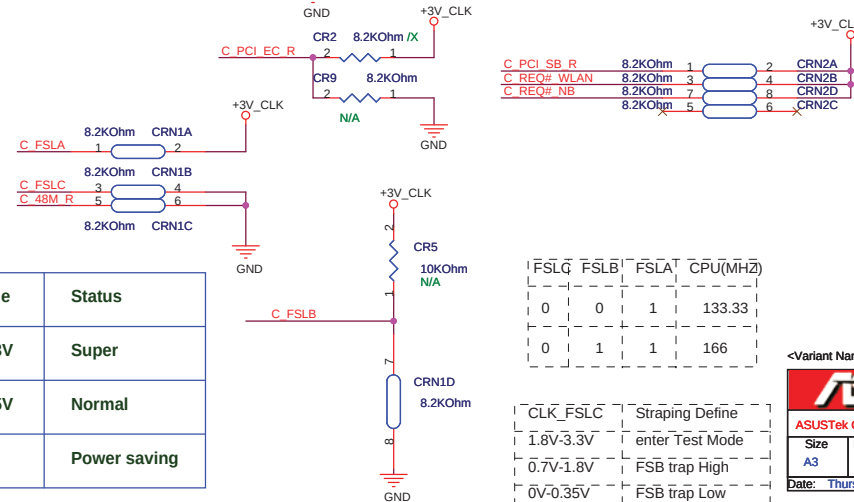
1:Disable
0:Enable

```
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 &
PCIEx6
```

If the PCICLK is driving two devices (2 loads), the series resistors need to be changed. (12 Ohm or 22 Ohm is recommended.)

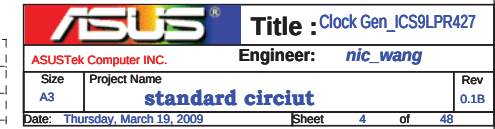


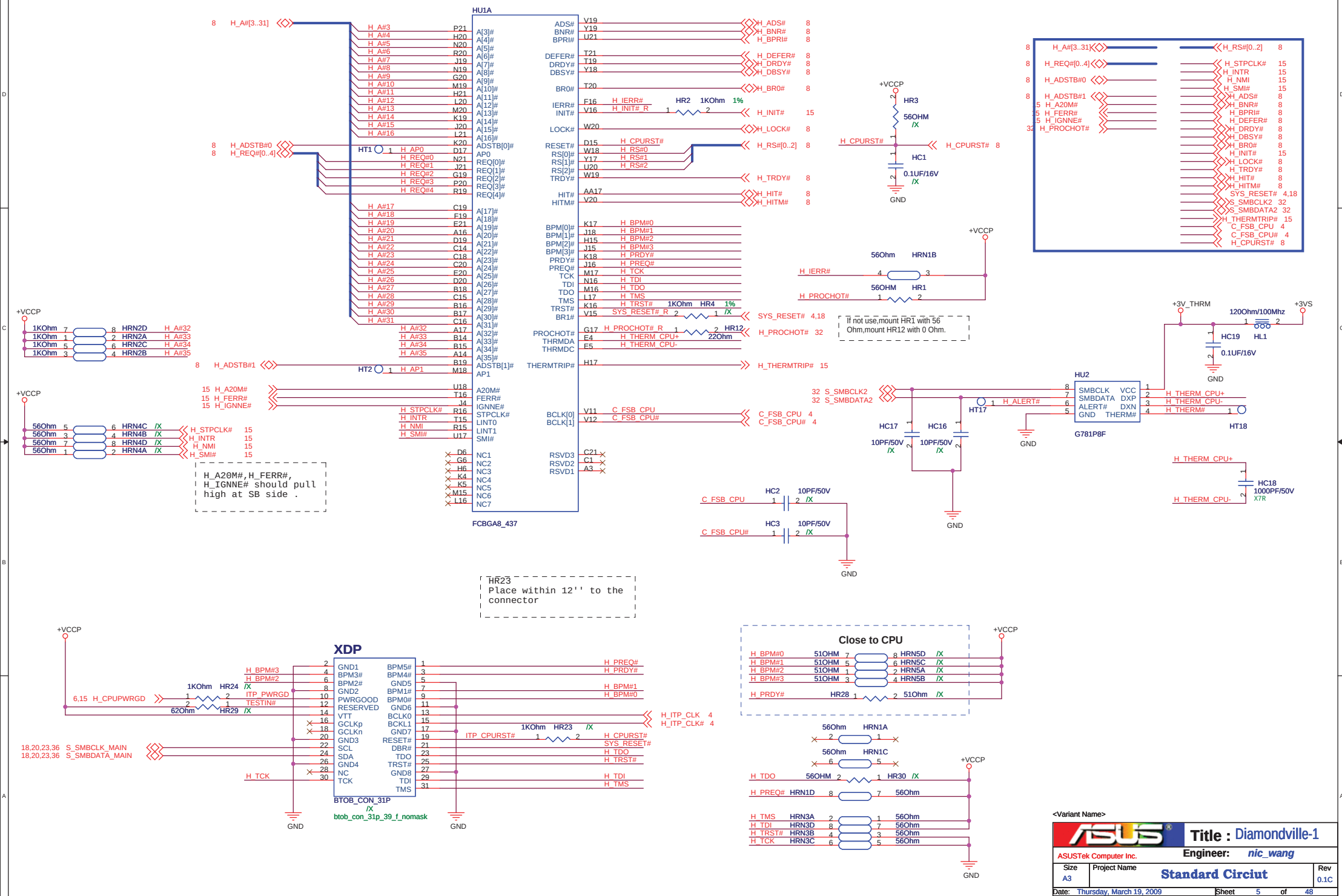
O_DOC1	O_DOC2	Voltage	Status
L	L	2.0-3.3V	Super
L	H	0.7-1.5V	Normal
H	*	0V	Power saving



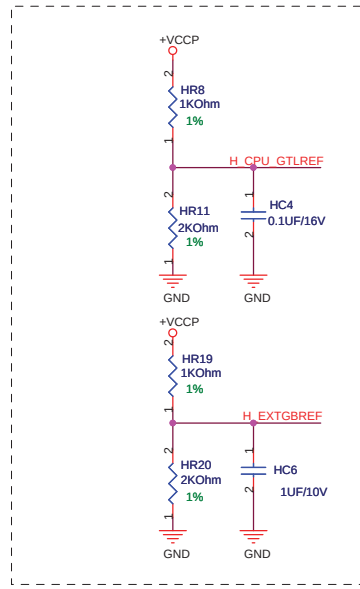
FSLQ	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
0	1	1	166

<Variant Name>

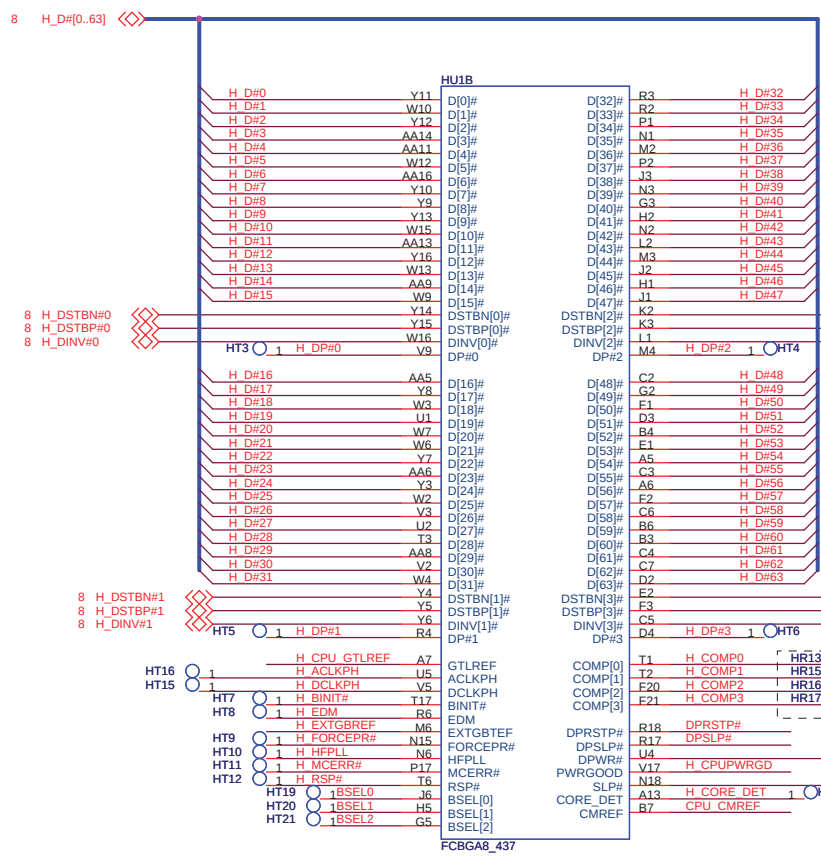




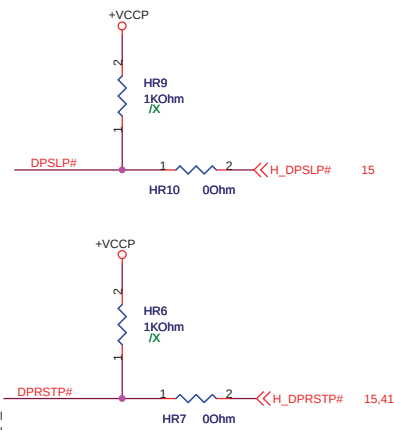
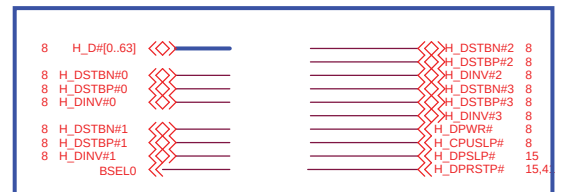
Place within 0.5'' to processor pin



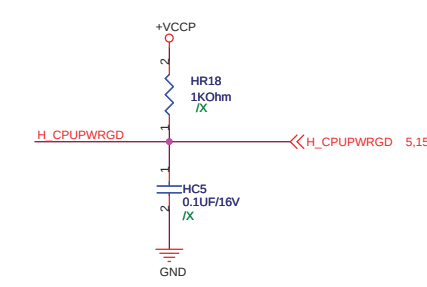
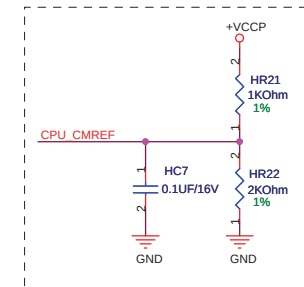
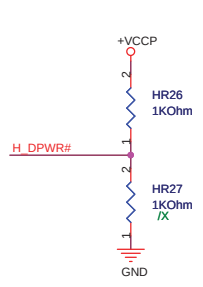
BSEL0	BSEL1	BSEL2	FSB
0	X	X	400
1	X	X	533

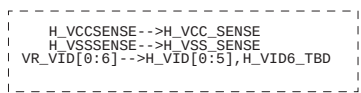


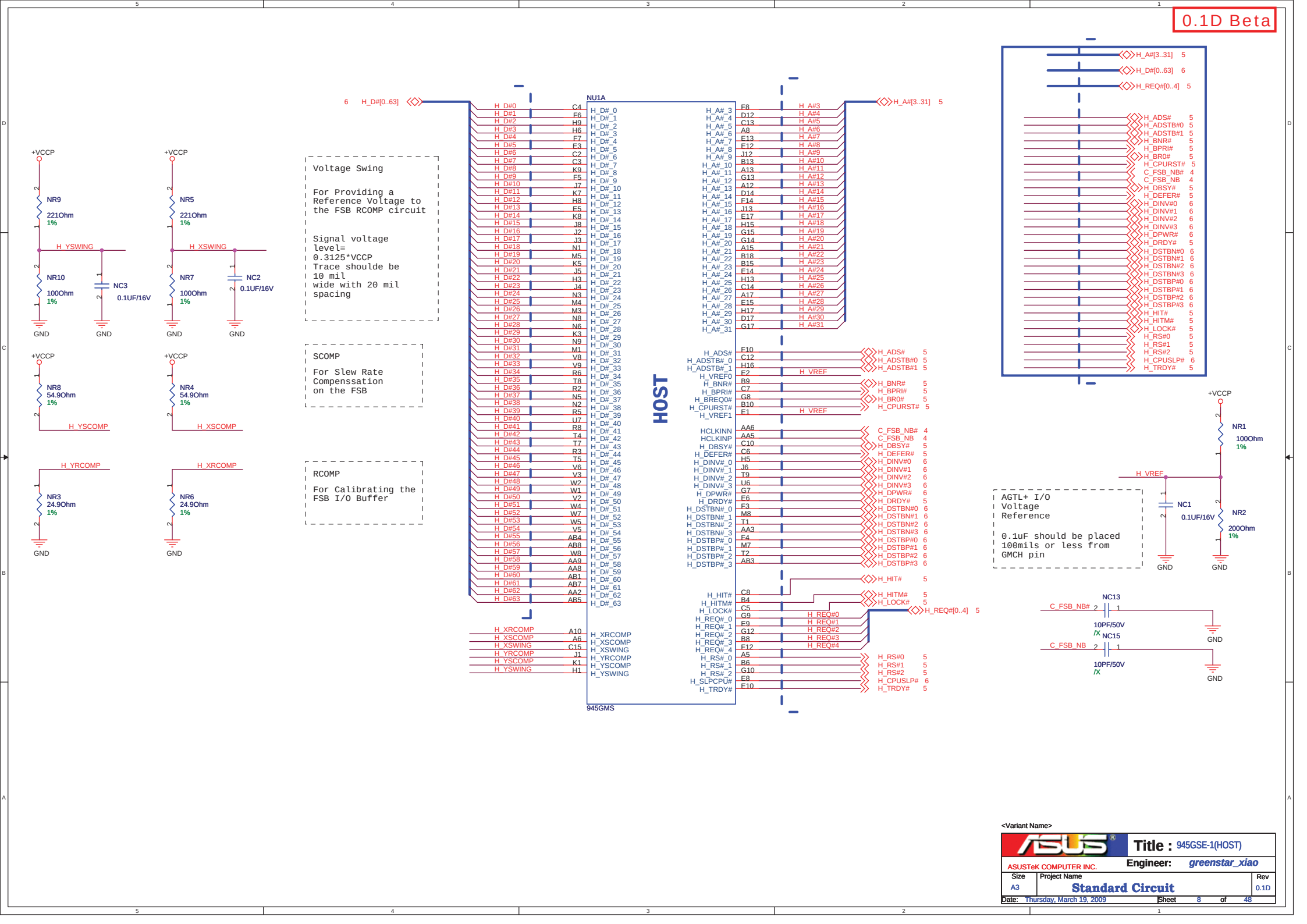
Place within 0.5'' to processor pin

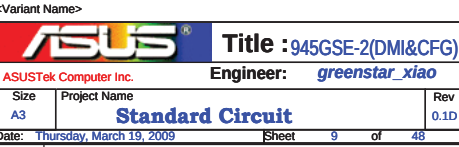


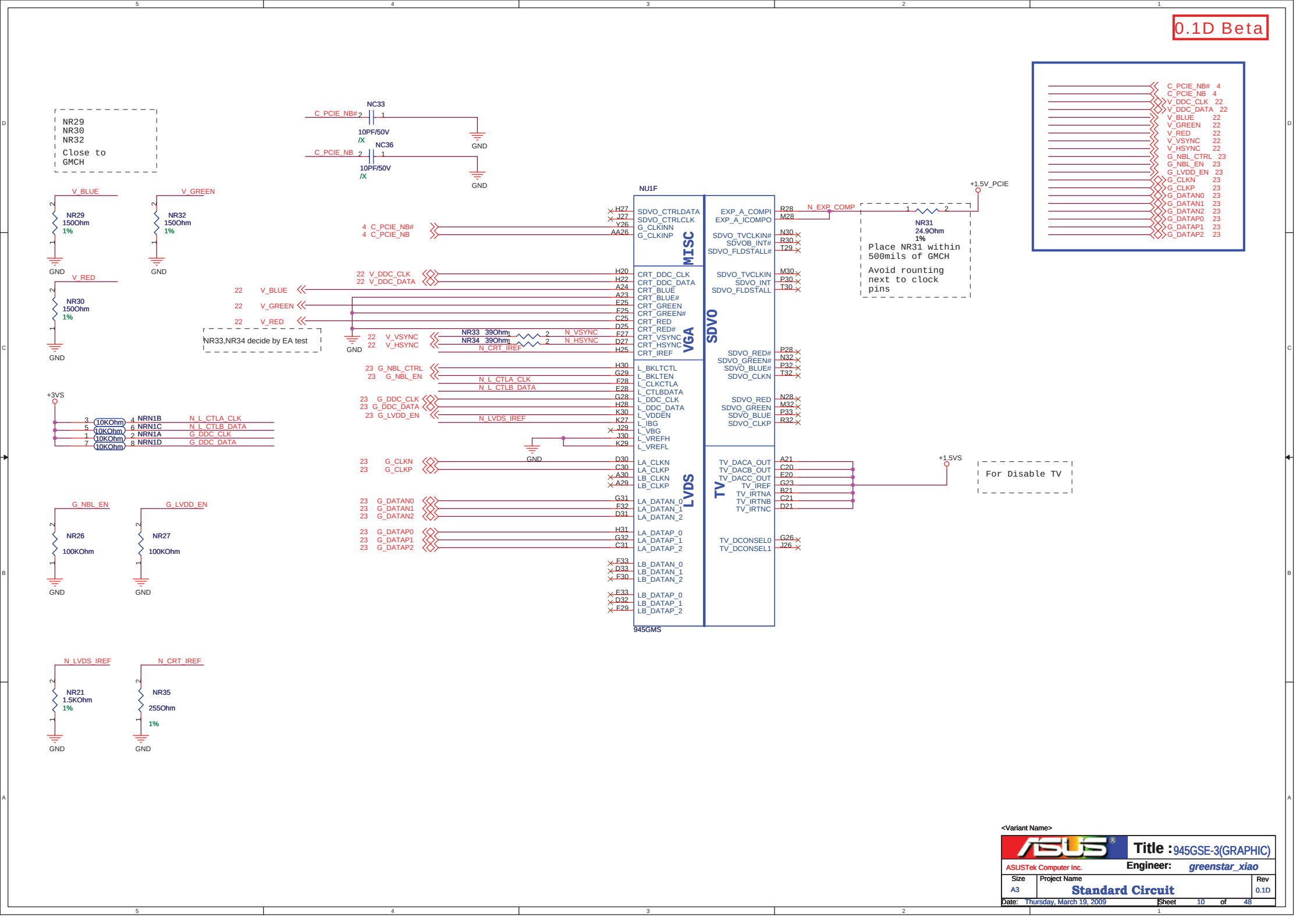
Place within 0.5'' to processor pin



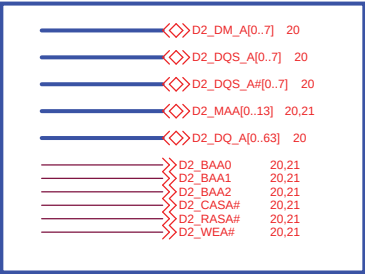
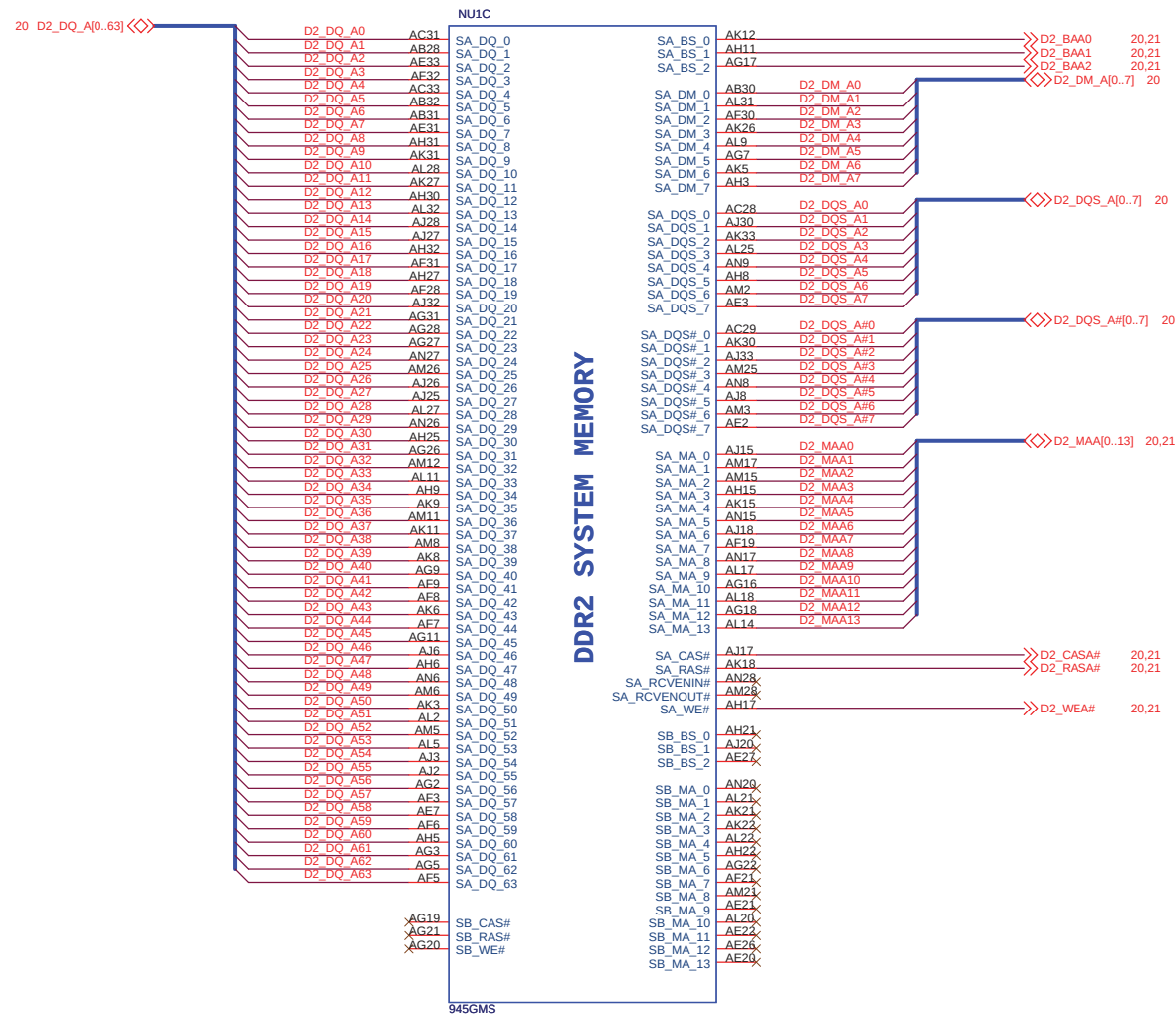




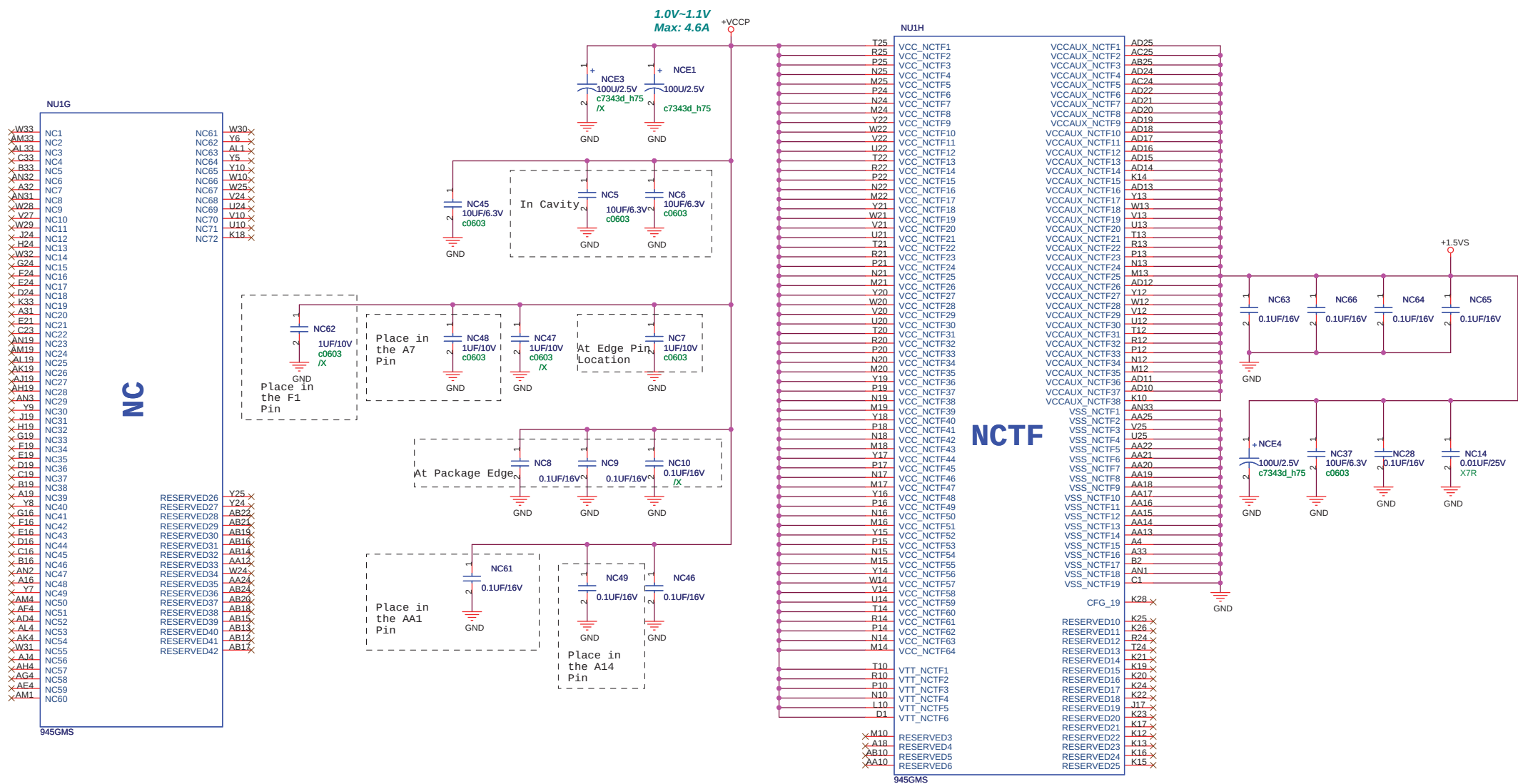




<Variant Name>



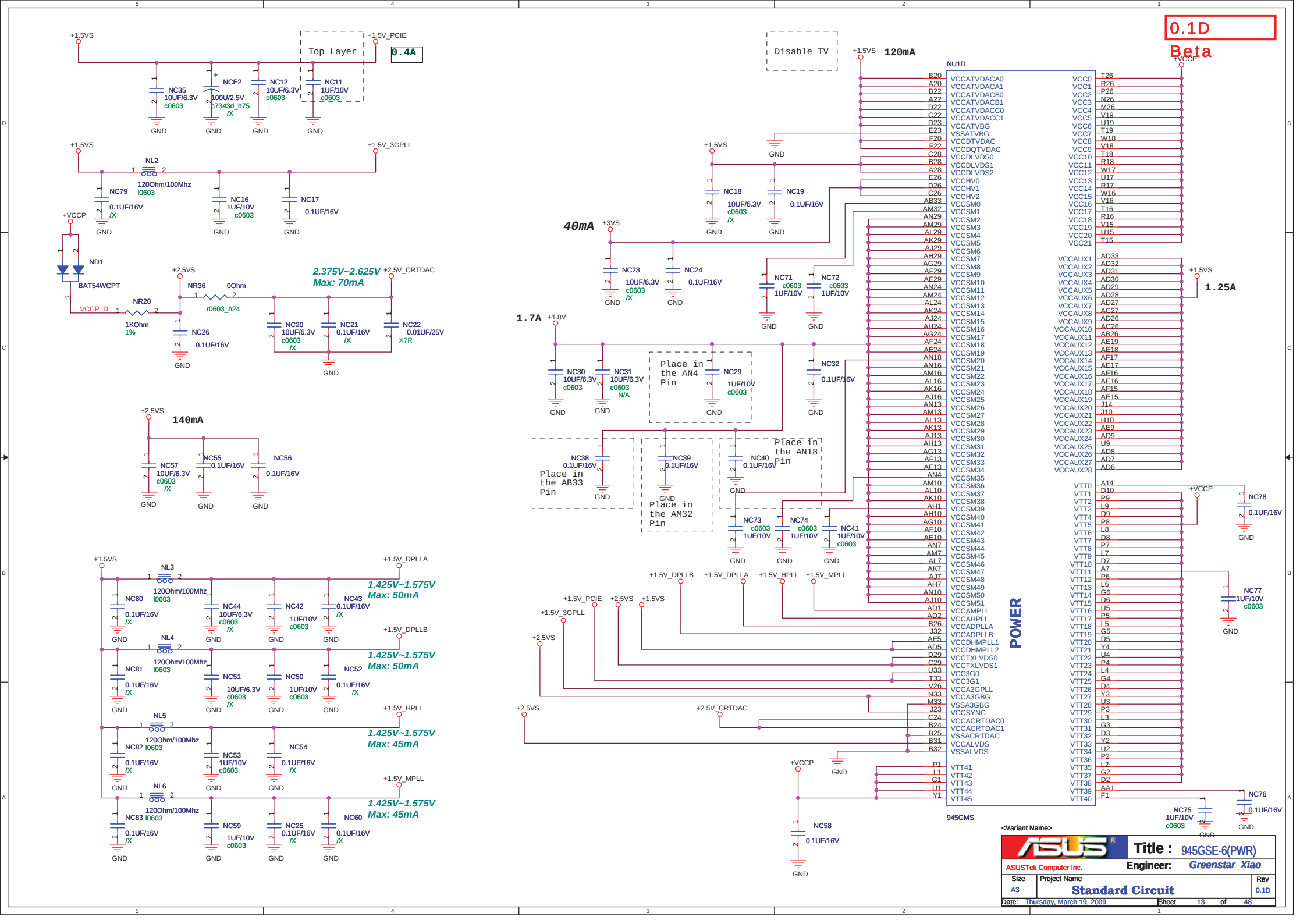
<Variant Name>

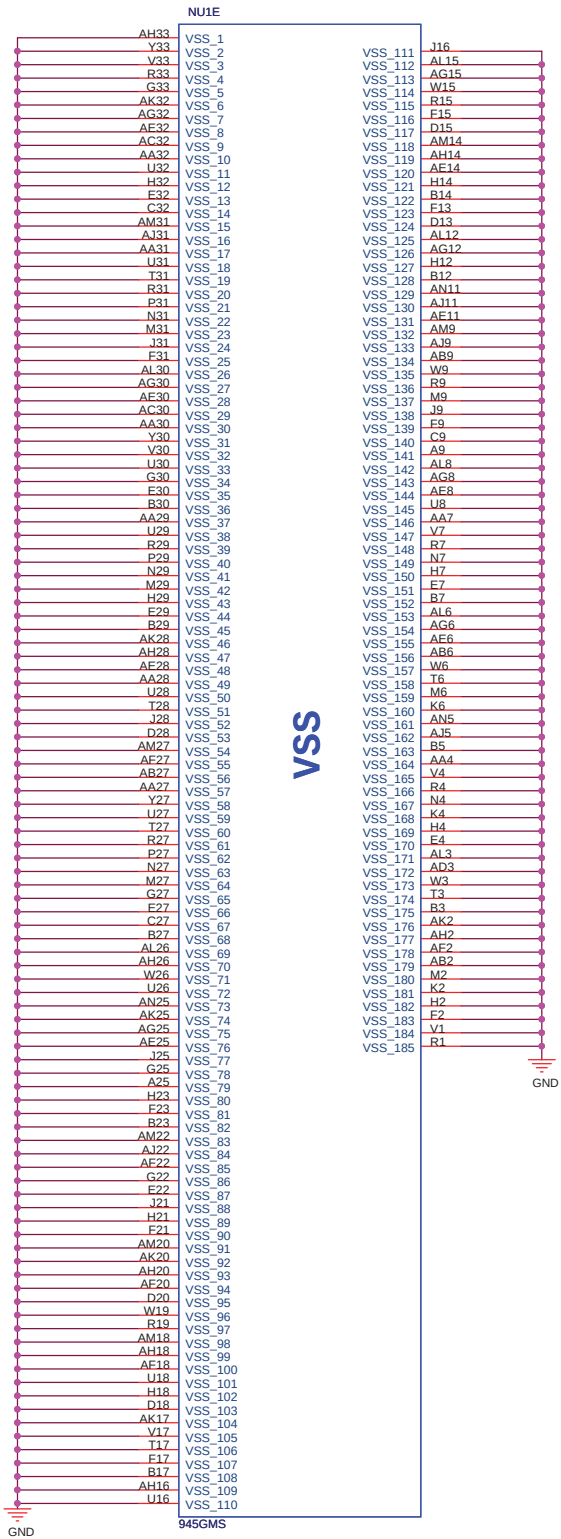


<Variant Name>

ASUSTek Computer Inc. Engineer: greenstar_xiao

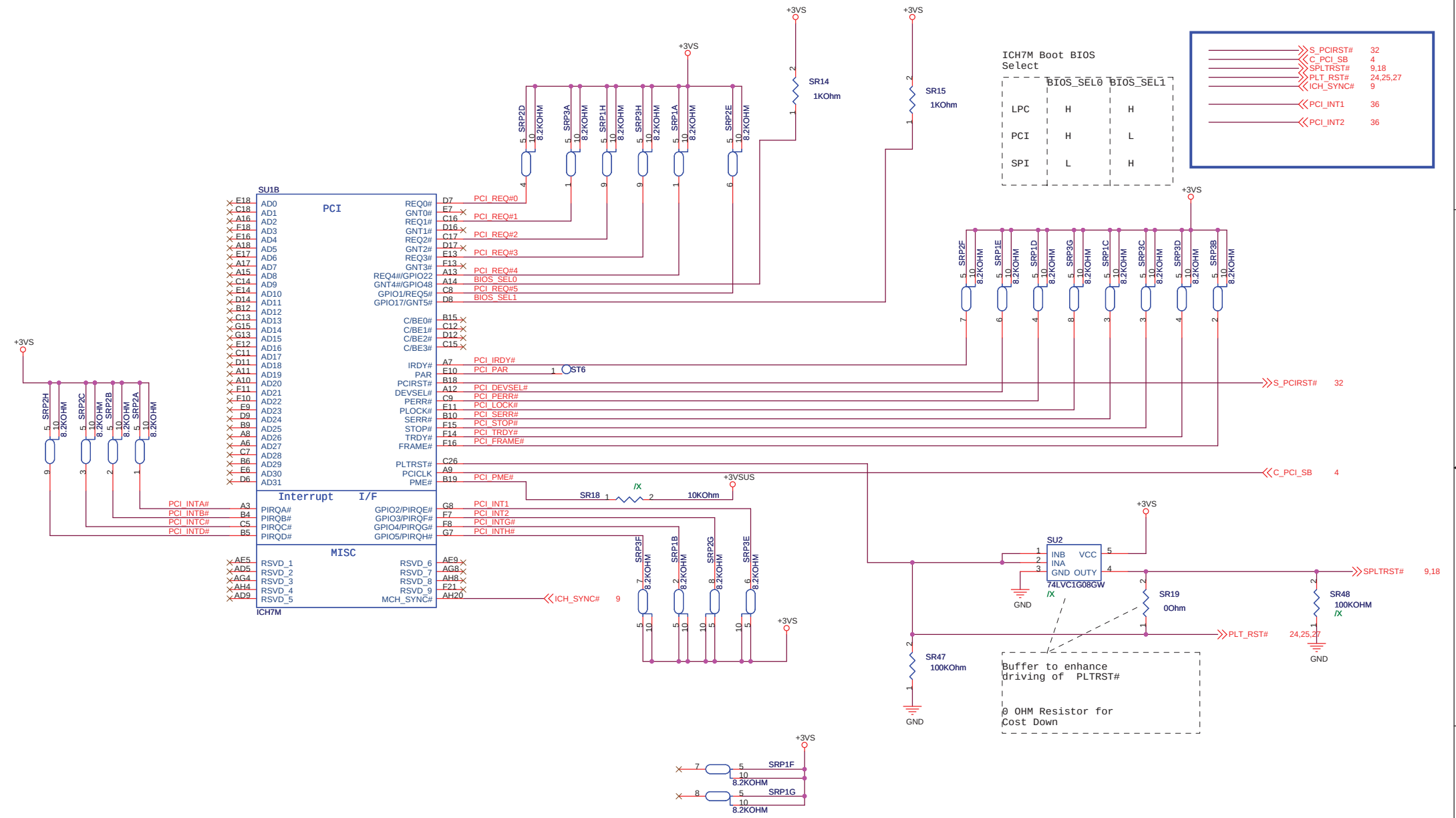
Size A3	Project Name Standard Circuit	Rev 0.1D
Date: <u>Thursday, March 19, 2009</u>		Sheet <u>12</u> of <u>48</u>

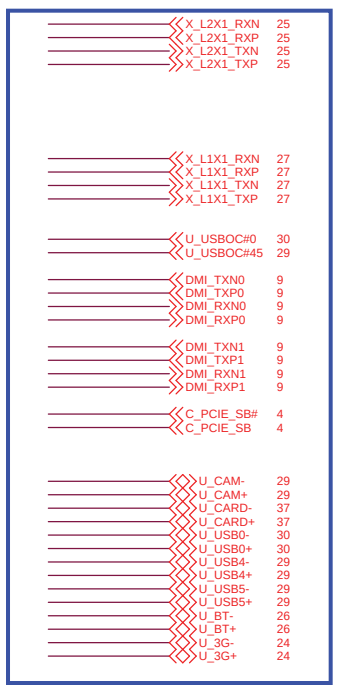
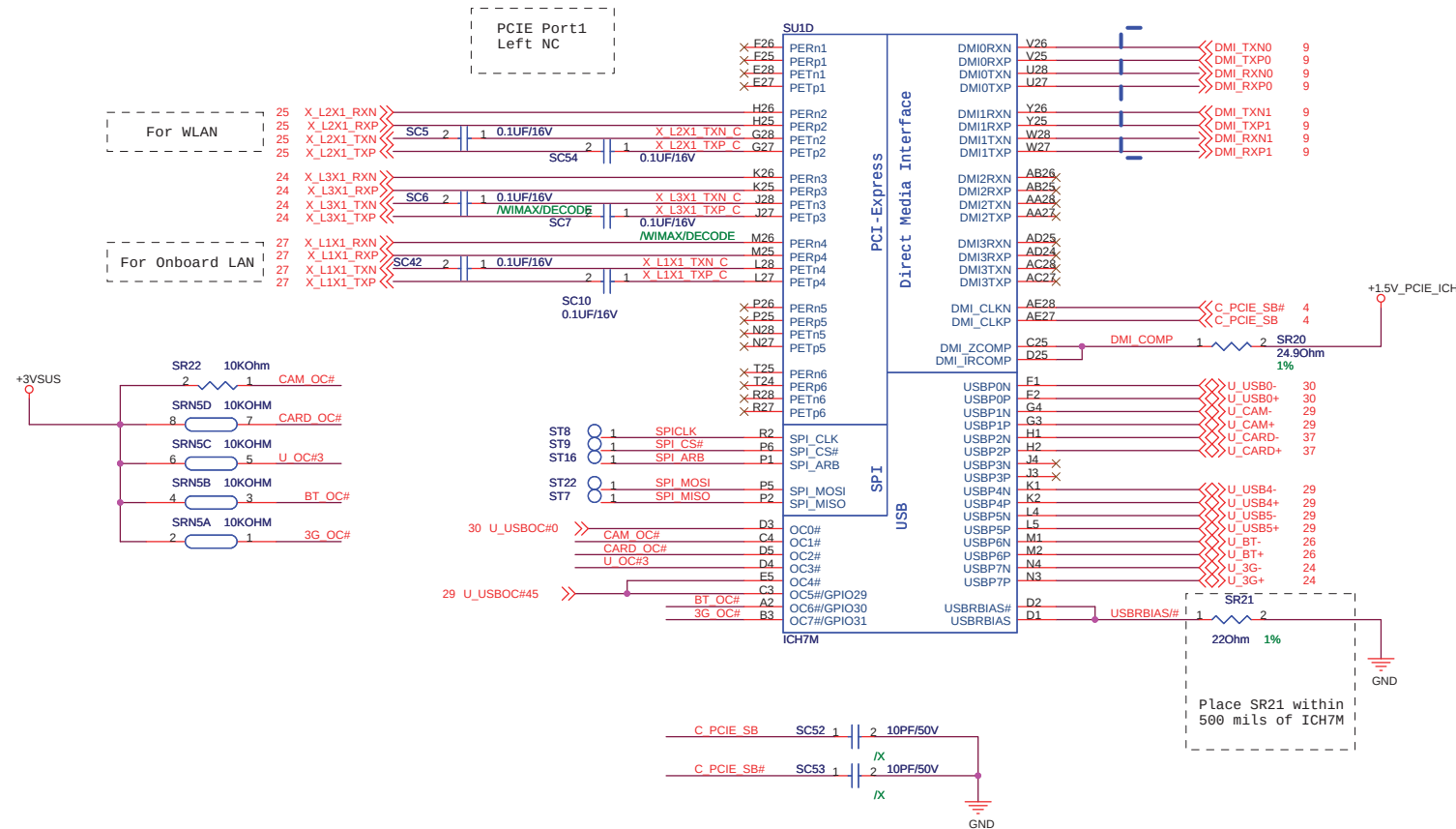




<Variant Name>

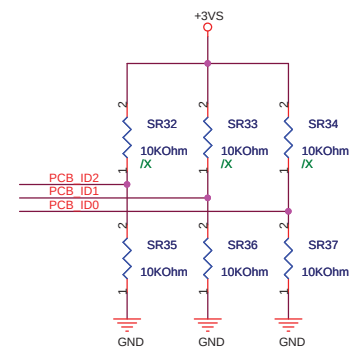
		Title : 945GSE-7(GND)	
ASUSTek Computer Inc.		Engineer: Greenstar_Xiao	
Size A3	Project Name Standard Circuit		Rev 0.1D
Date: Thursdav, March 19, 2009		Sheet 14	of 48



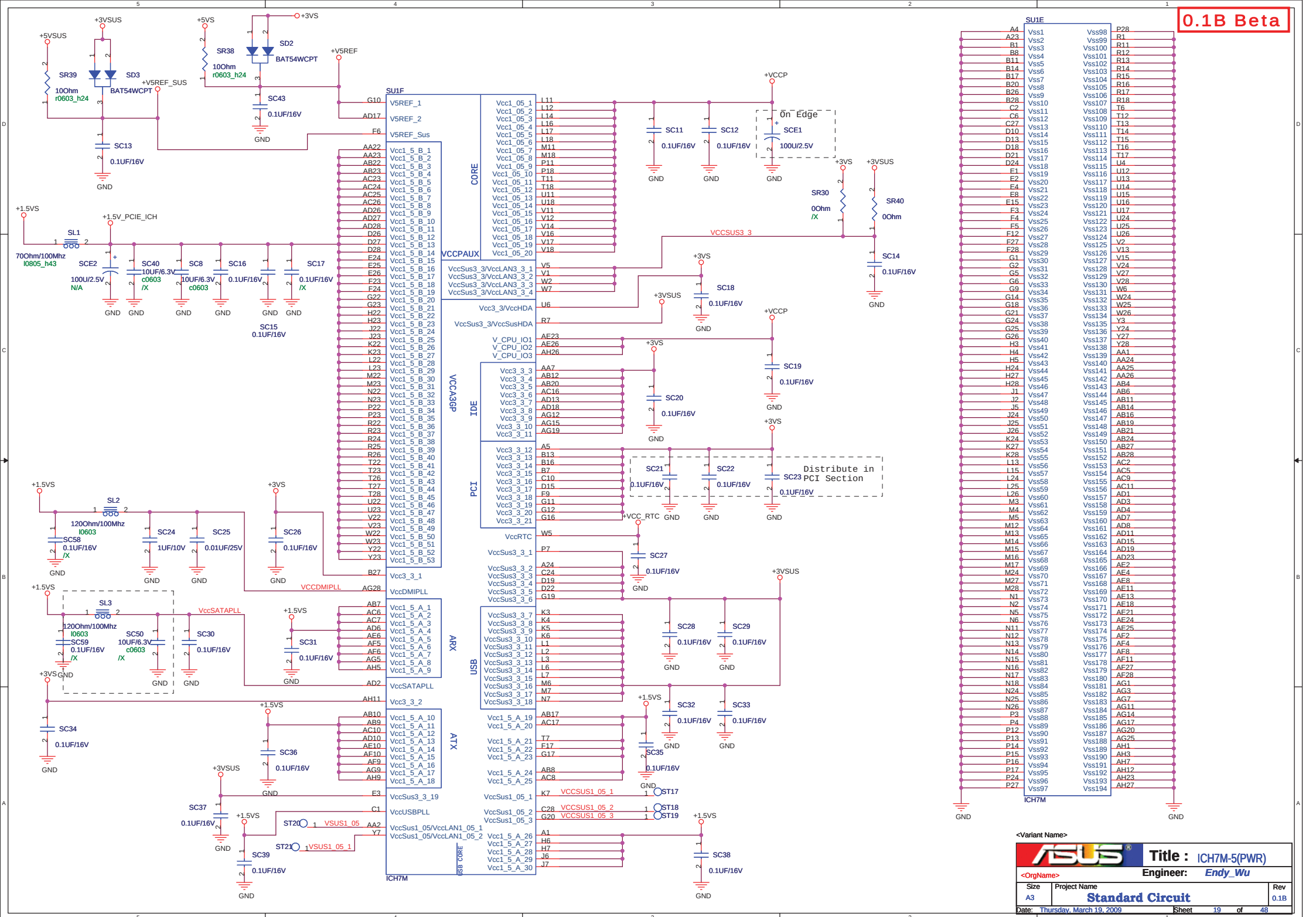


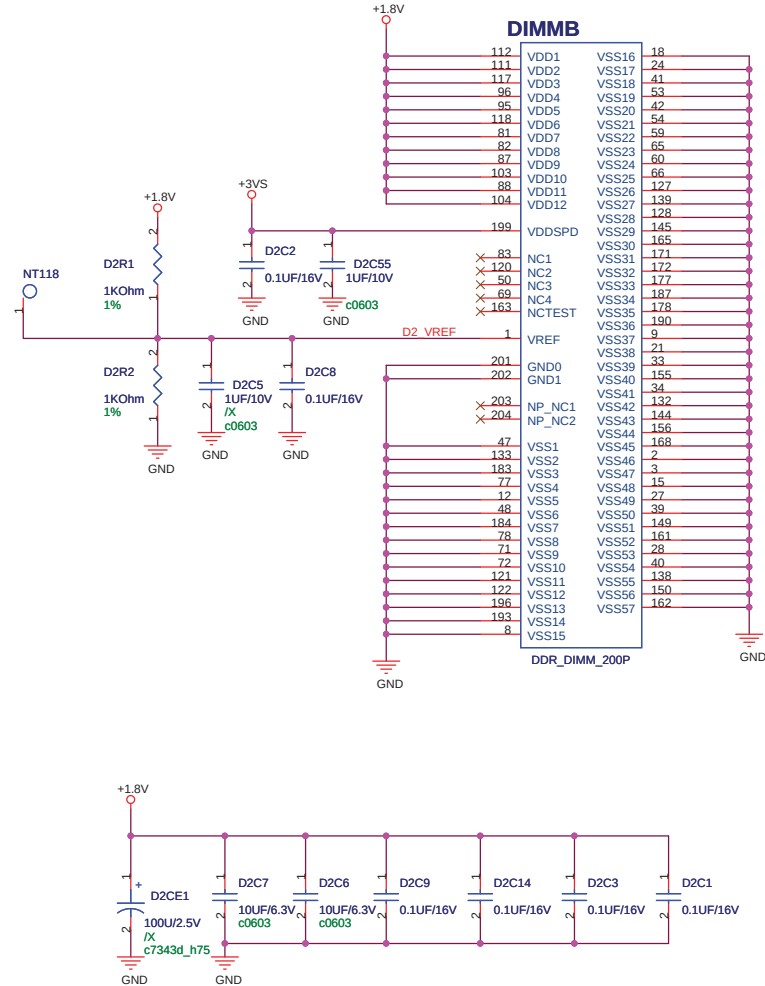
USB0	NC
USB1	Camera
USB2	Card Reader
USB3	USB CONN
USB4	USB CONN
USB5	USB CONN
USB6	Blue Tooth
USB7	3G Card

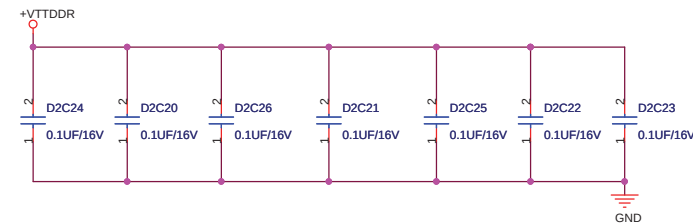
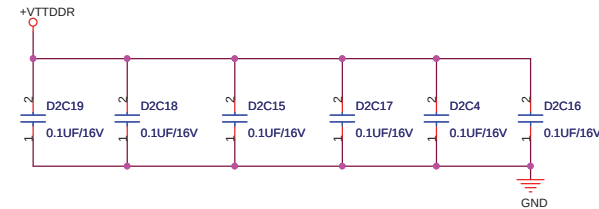
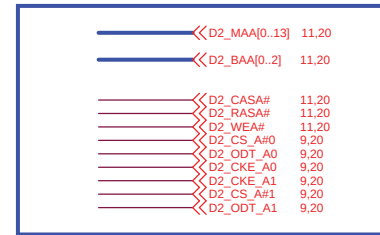
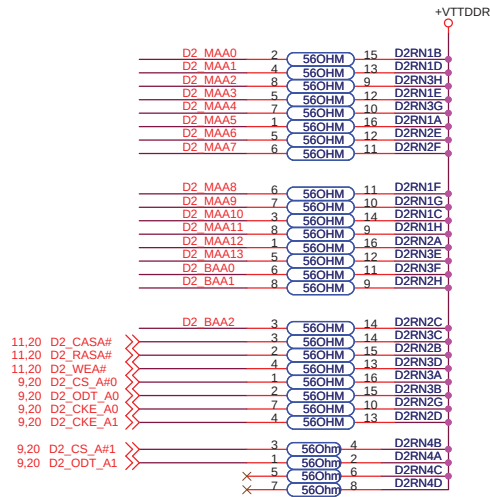
Place SR21 within 500 mils of ICH7M

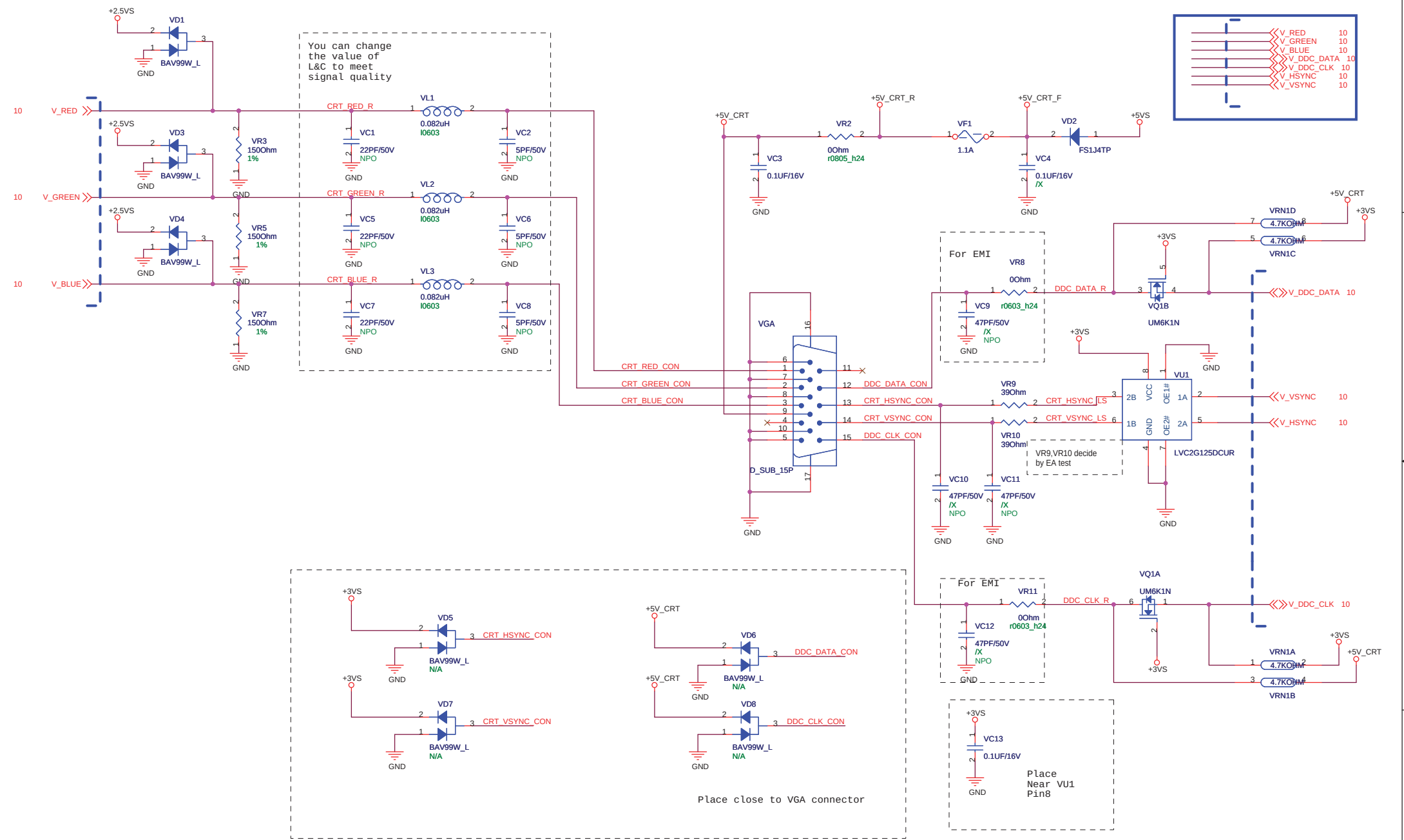


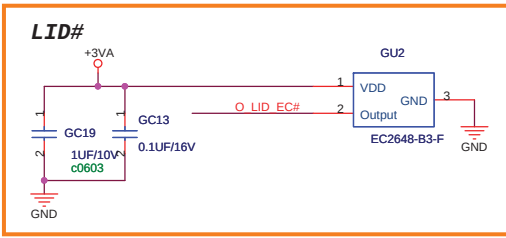
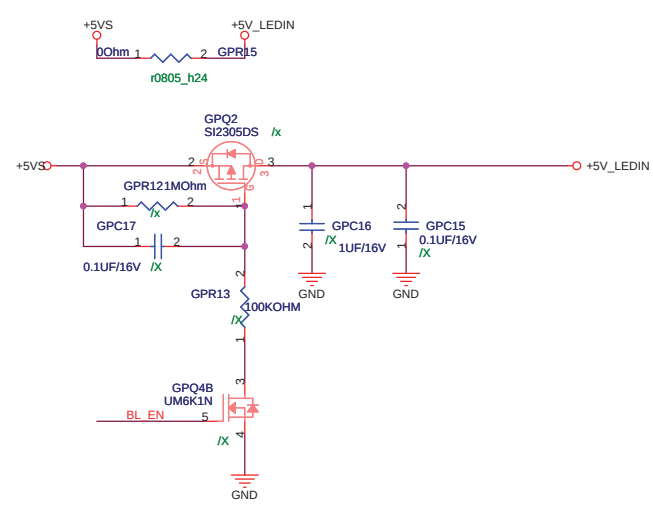
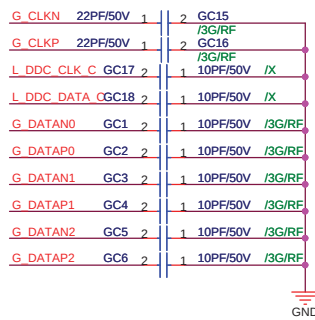
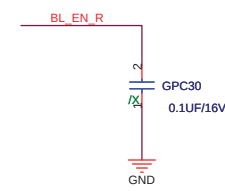
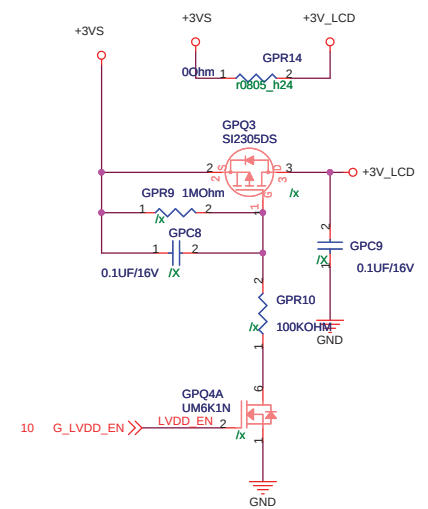
		Title : ICH7M-4(GPIO)	
<OrgName>		Engineer: <i>Endy_Wu</i>	
Size A3	Project Name Standard Circuit	Rev 0.10	
Date: Thursday, March 19, 2009		Sheet 18	of 48

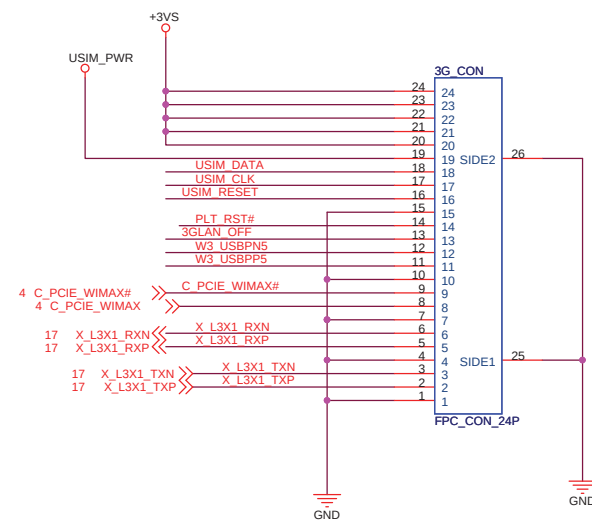
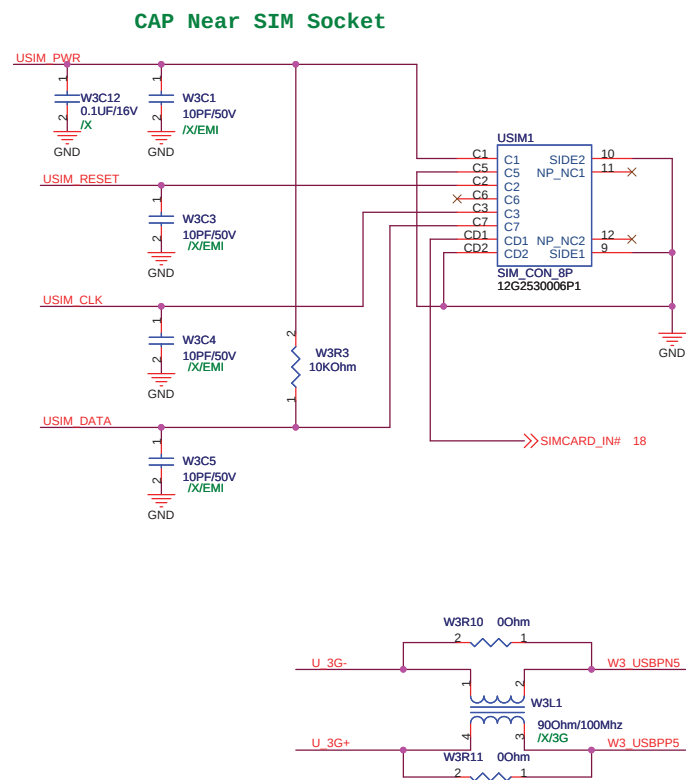






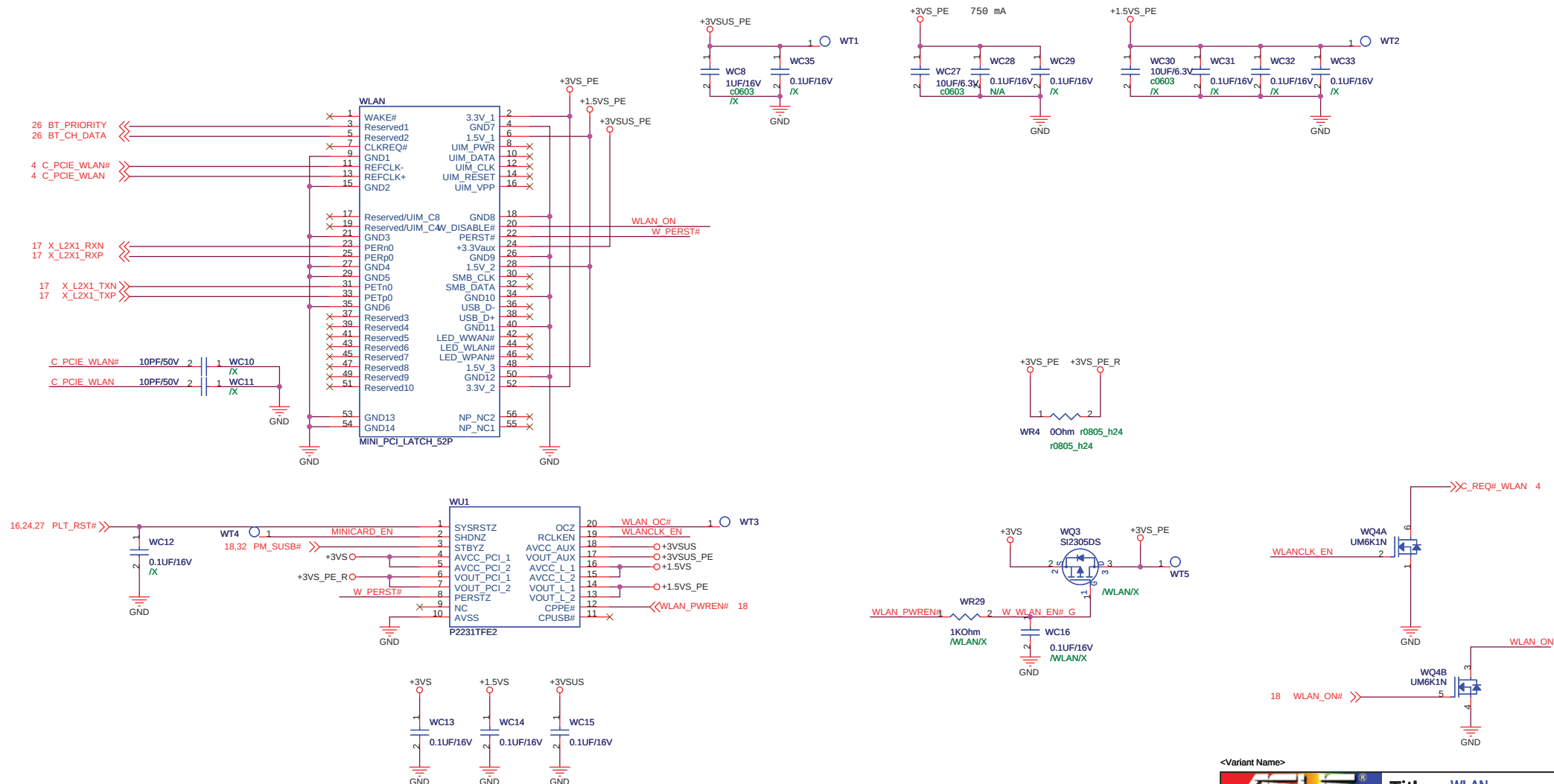






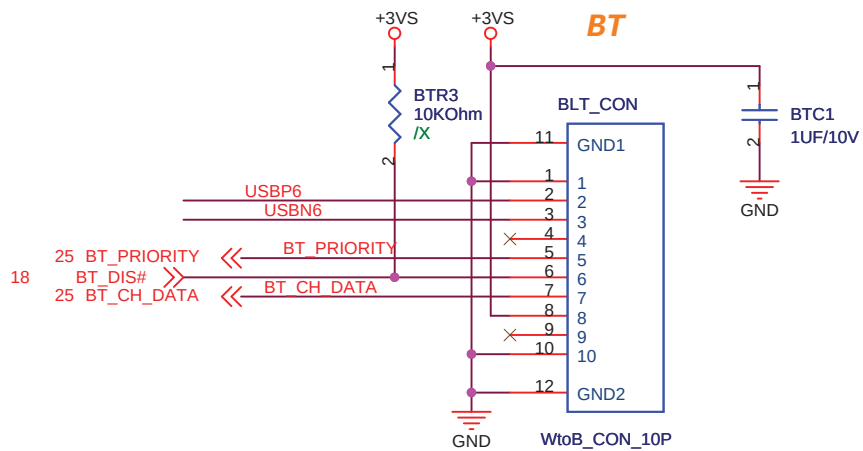
26 BT_PRIORITY <<=====
26 BT_CH_DATA <<=====
4 C_PCIE_WLAN# <<=====
4 C_PCIE_WLAN <<=====
17 X_L2X1_RXN <<=====
17 X_L2X1_RXP <<=====
17 X_L2X1_TXN <<=====
17 X_L2X1_TXP <<=====
16,24,27 PLT_RST# <<=====
18,32 PM_SUSB# <<=====
18 WLAN_PWREN# <<=====
4 C_REQ#_WLAN <<=====

18 WLAN_ON# >>=====

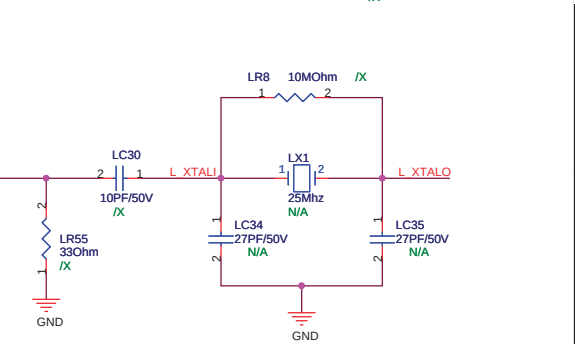
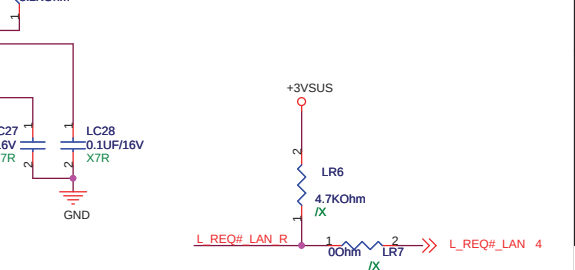
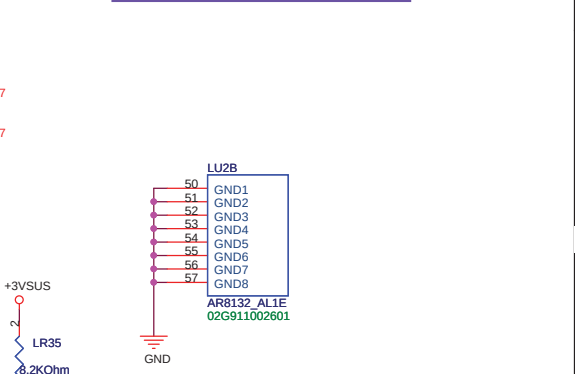
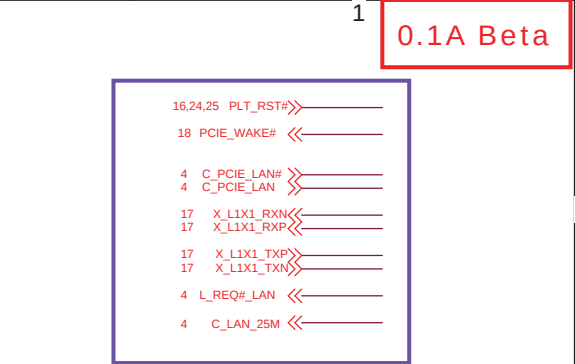
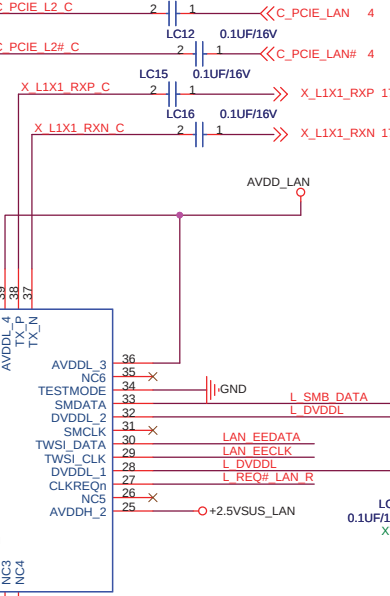
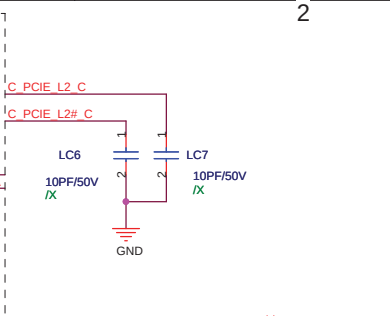
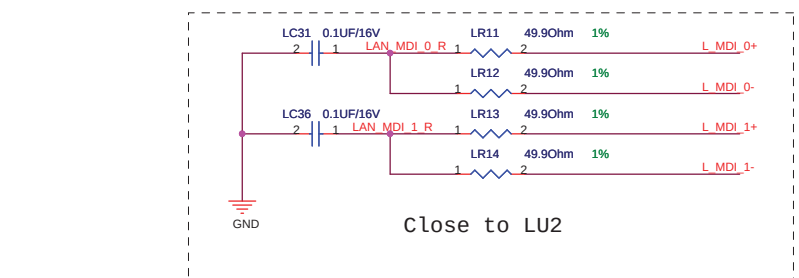
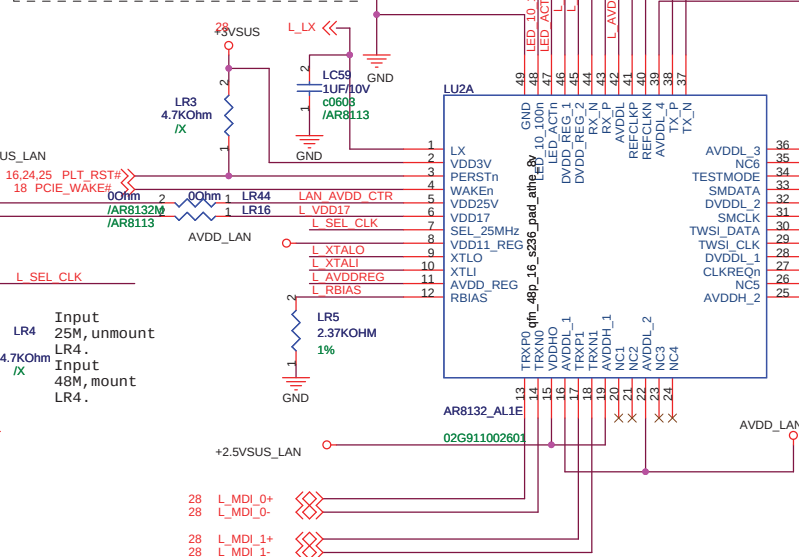
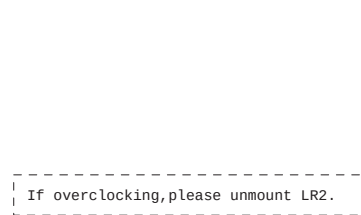
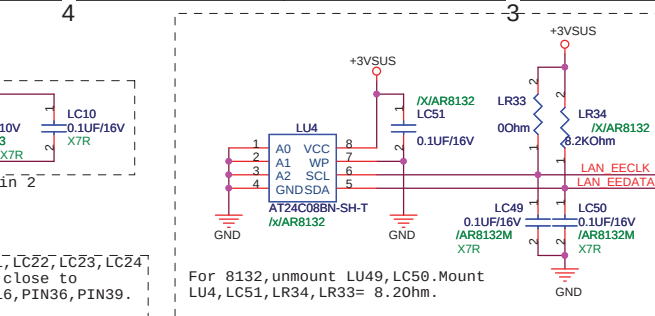
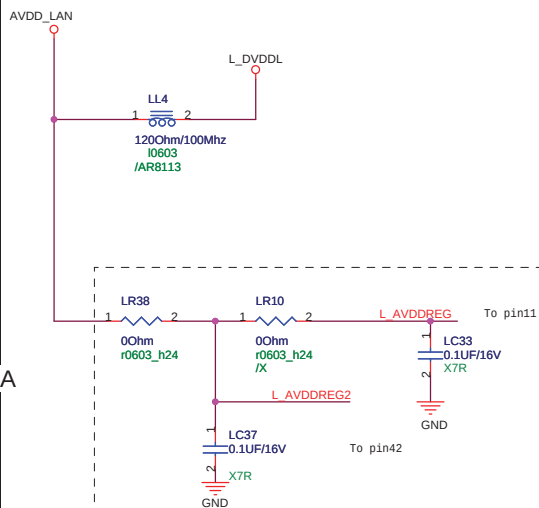
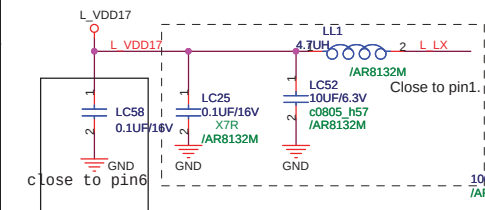
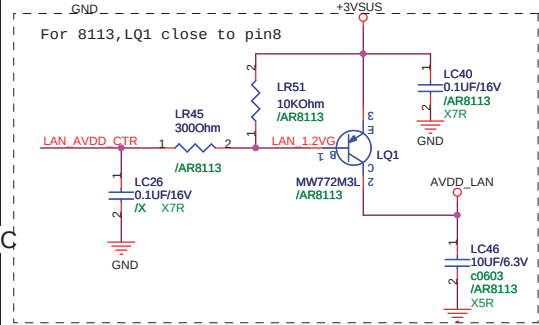
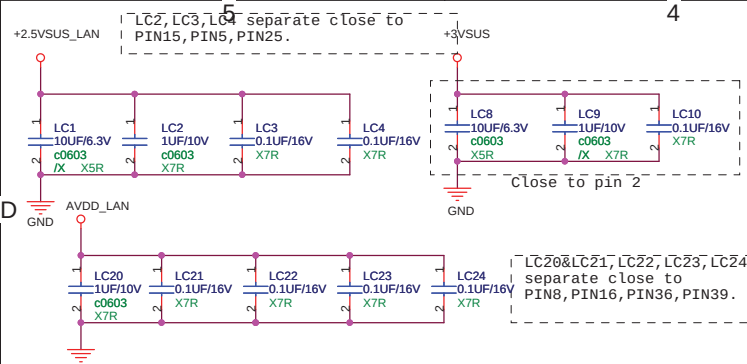


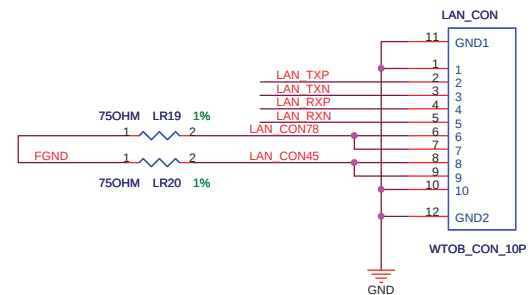
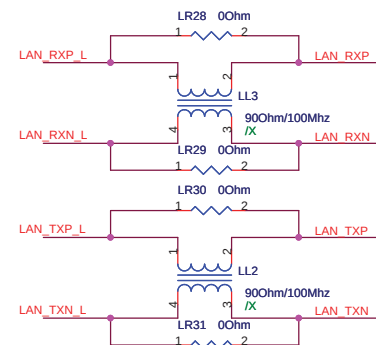
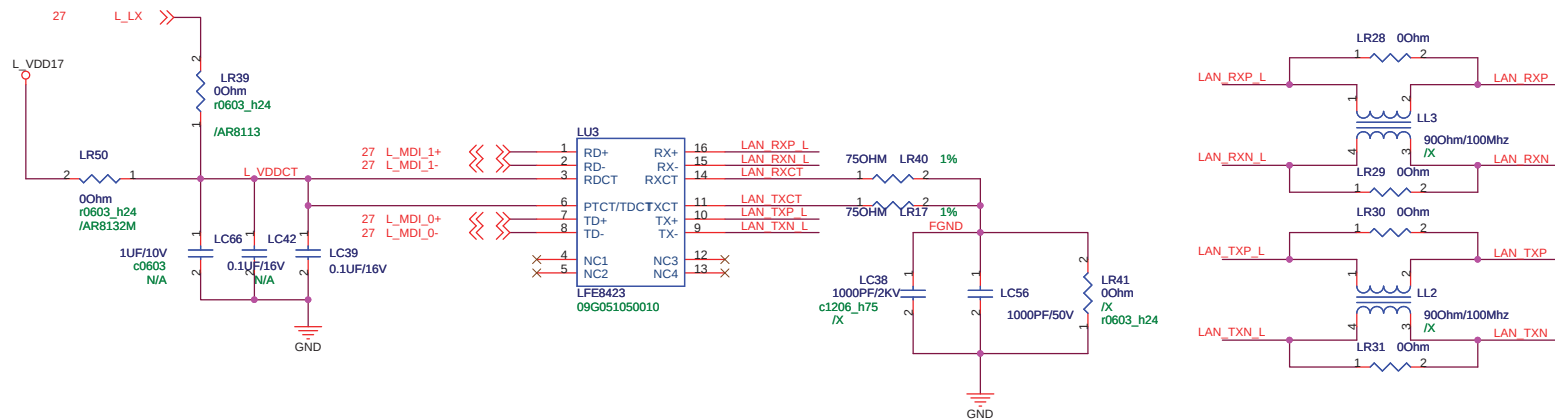
<Variant Name>

ASUS		Title : WLAN	
ASUSTek Computer INC.		Engineer: Joe1_Zhou	
Size	Project Name	Standard circuit	
A3			
Date: Thursday, March 19, 2009	Sheet	25	of 48



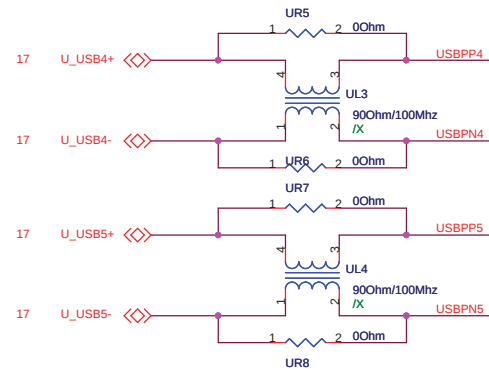
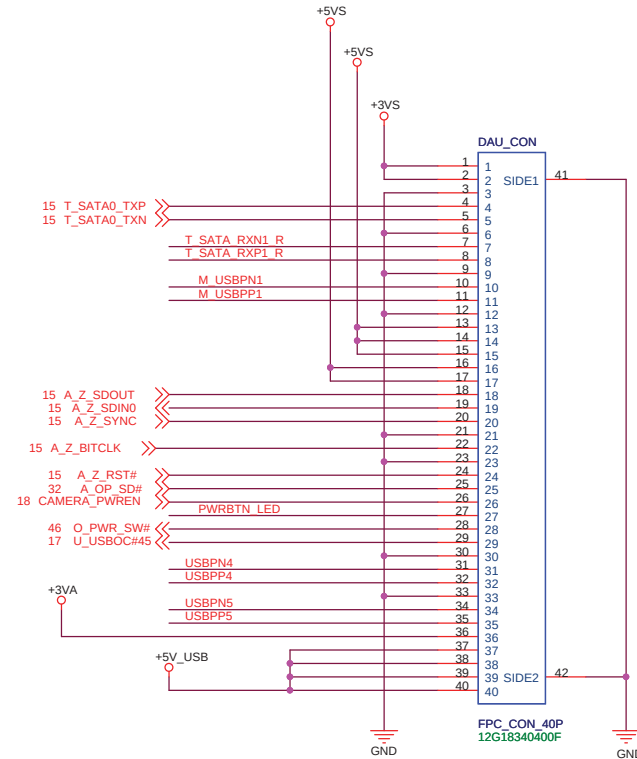
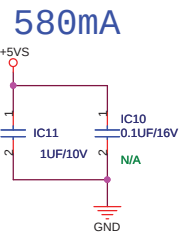
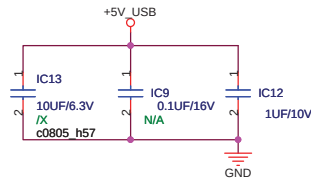
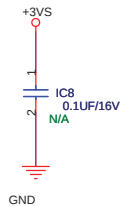
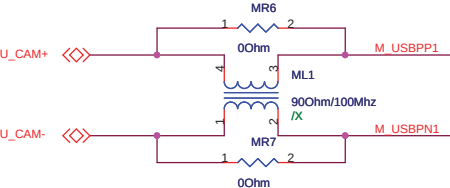
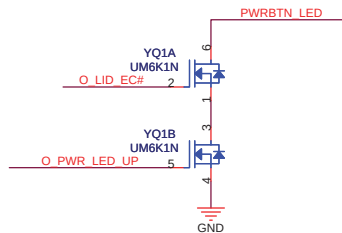
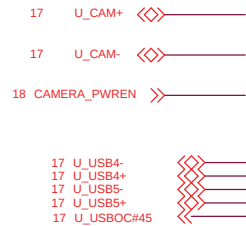
		Title : <u>BLUETOOTH</u>	
ASUSTek Computer INC.		Engineer: <u>JOE1_ZHOU</u>	
Size <u>A4</u>	Project Name <u>Standard Circiut</u>	Rev <u>0.1A</u>	
Date: <u>Thursday, March 19, 2009</u>		Sheet <u>26</u> of <u>48</u>	





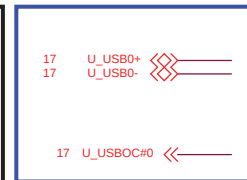
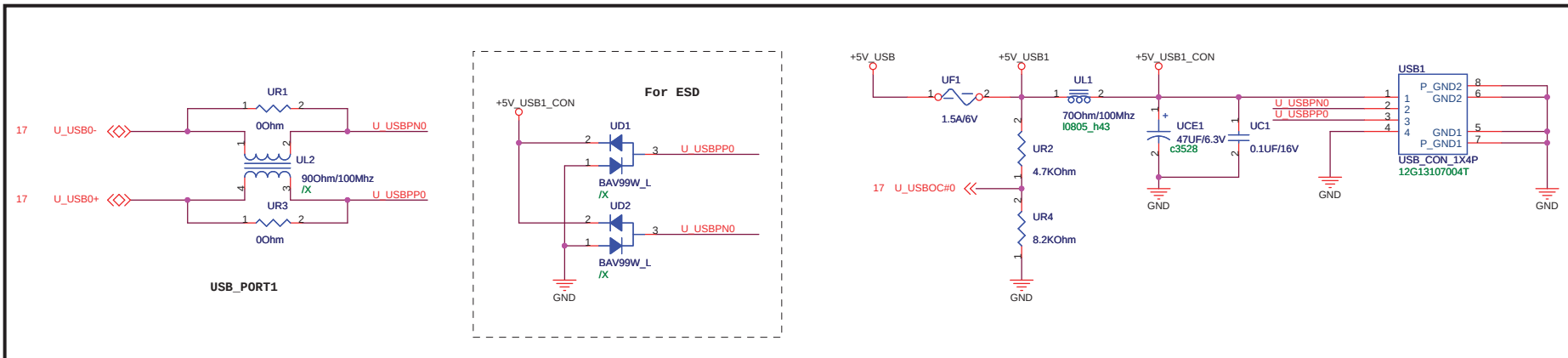
<Variant Name>

		Title : RJ45	
ASUSTek Computer INC.		Engineer: Hui-sheng_wu	
Size A3	Project Name Standard Circiut	Rev 0.1A	
Date: Thursday, March 19, 2009		Sheet 28	of 48



<Variant Name>

ASUS		Title : SATA HDD	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name		Rev
A3	1000HN		1.0
Date: Thursday, March 19, 2009		Sheet	29 of 48





<Variant Name>



ASUSTEK COMPUTER INC

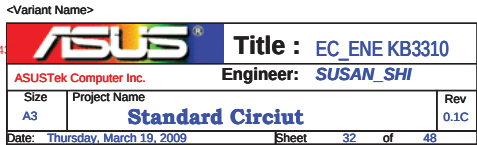
Title : Camera CONN

ASUSTEK COMPUTER INC

Engineer: KEN_JIN

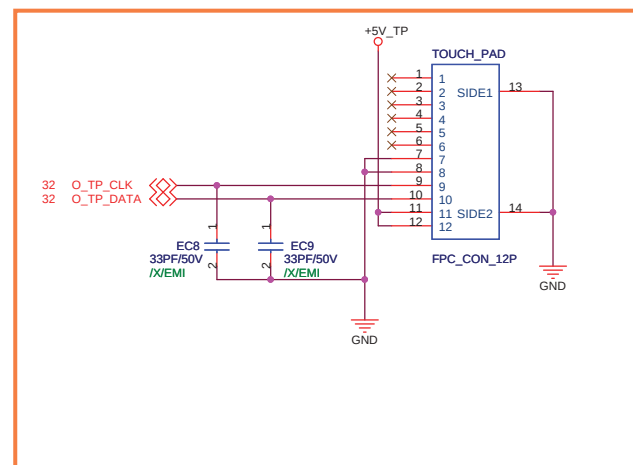
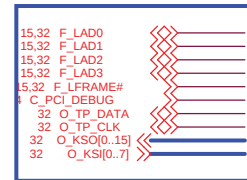
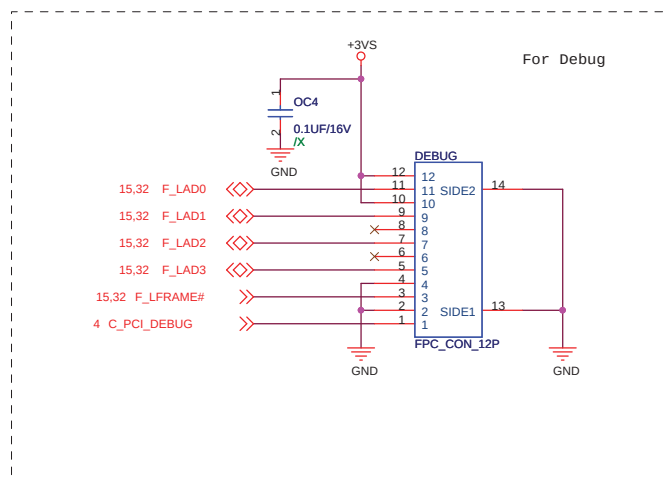
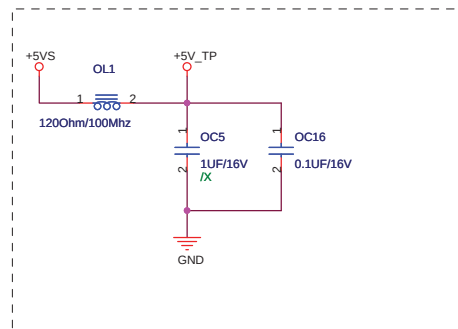
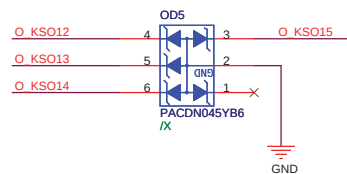
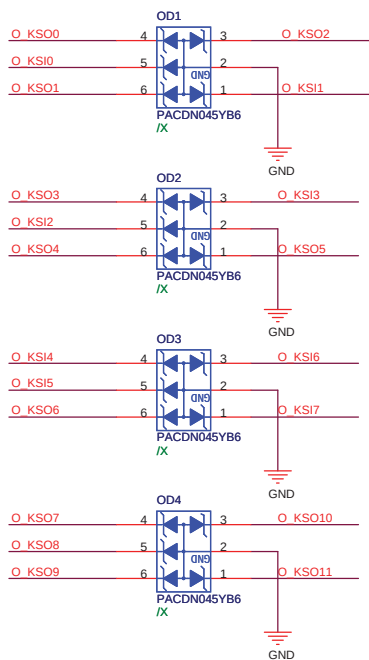
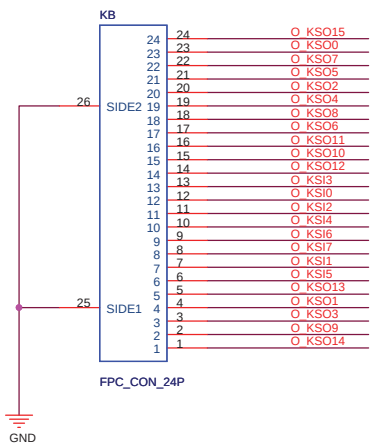
Size	Project Name	Rev
A3	Standard Circiut	0.1A

Date: Thursday, March 19, 2009Sheet 31 of 48



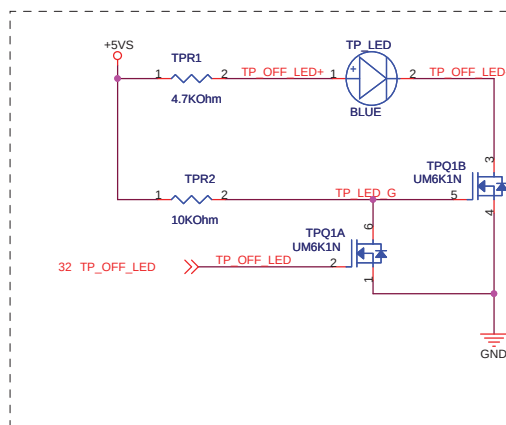
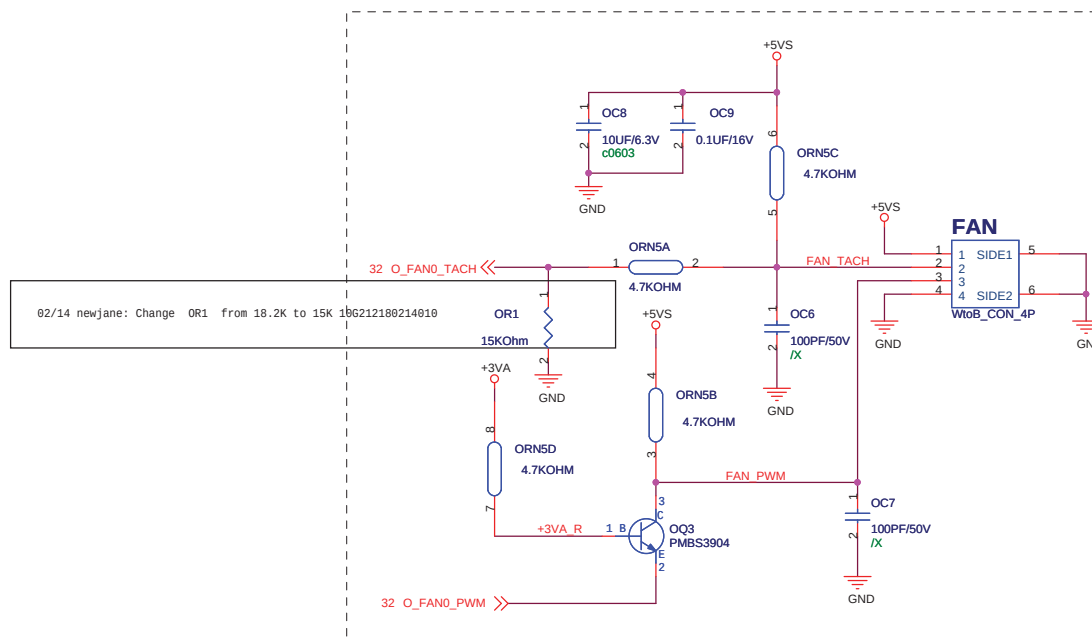
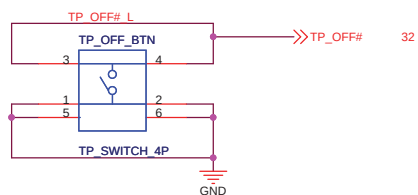
>>O_KSO[0..15] 32
<<O_KSI[0..7] 32

For Keyboard Connector



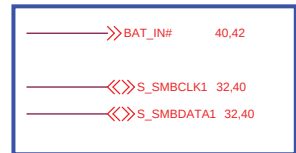
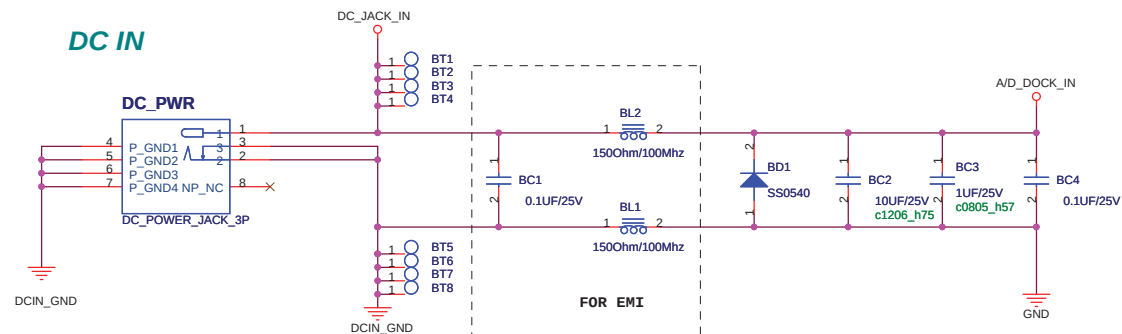
<Variant Name>

ASUS		Title : EC_ENE KB3310	
ASUSTek Computer Inc.		Engineer: SUSAN_SHI	
Size A3	Project Name	Standard Circuit	Rev 0.1C
Date: Thursday, March 19, 2009		Sheet 33 of 48	

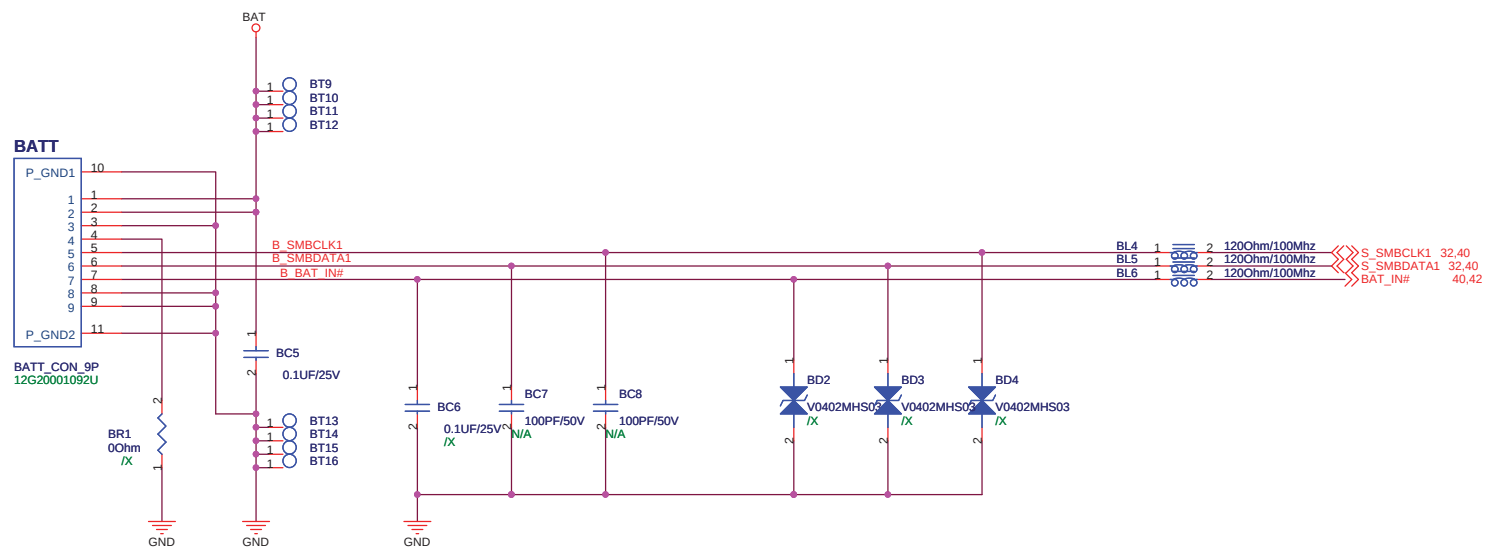


0.1B Beta

DC IN

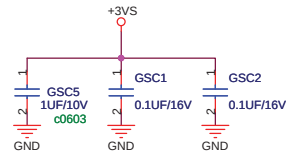
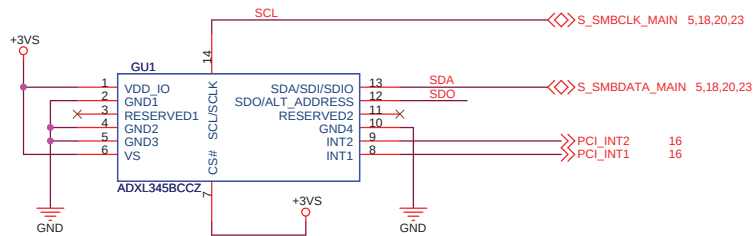
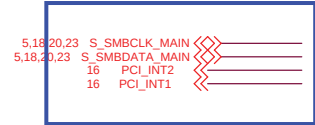


change from DIP to SMD



<Variant Name>

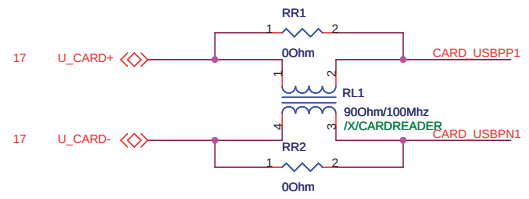
ASUS		Title : PWR Jack	
ASUSTEK COMPUTER INC		Engineer: KEN_JIN	
Size	Project Name	Rev	
A3	Standard Circuit	0.1B	
Date: Thursday, March 19, 2009		Sheet 35 of 48	



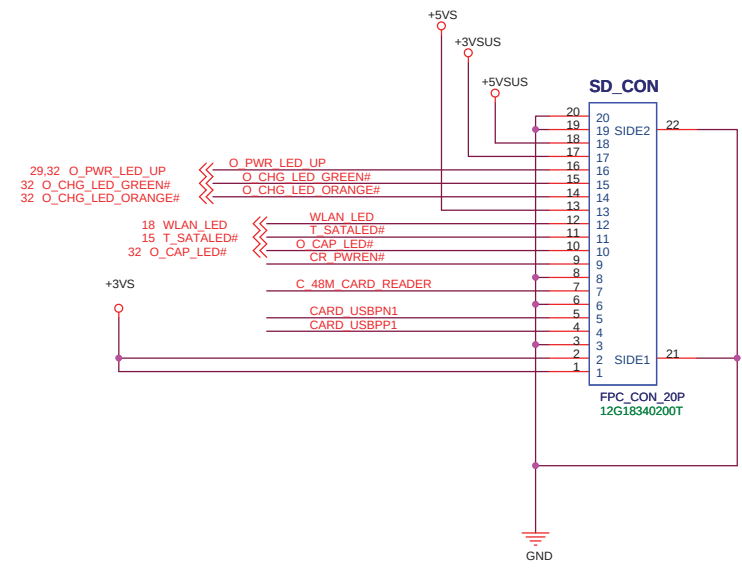
Install GSR6 being slave address "3A" for ADI/Freescale/ST G-sensors

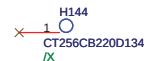
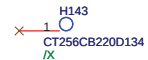
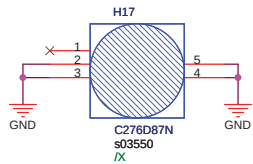
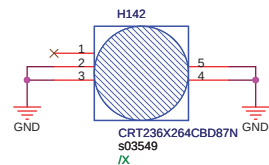
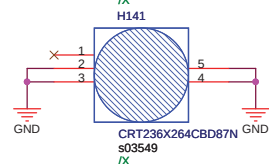
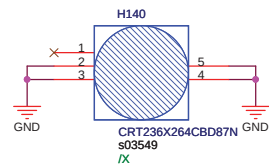
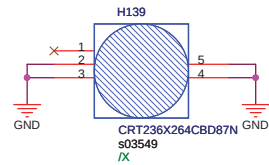
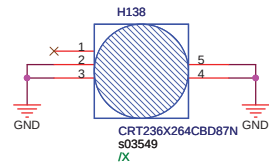
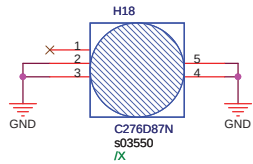


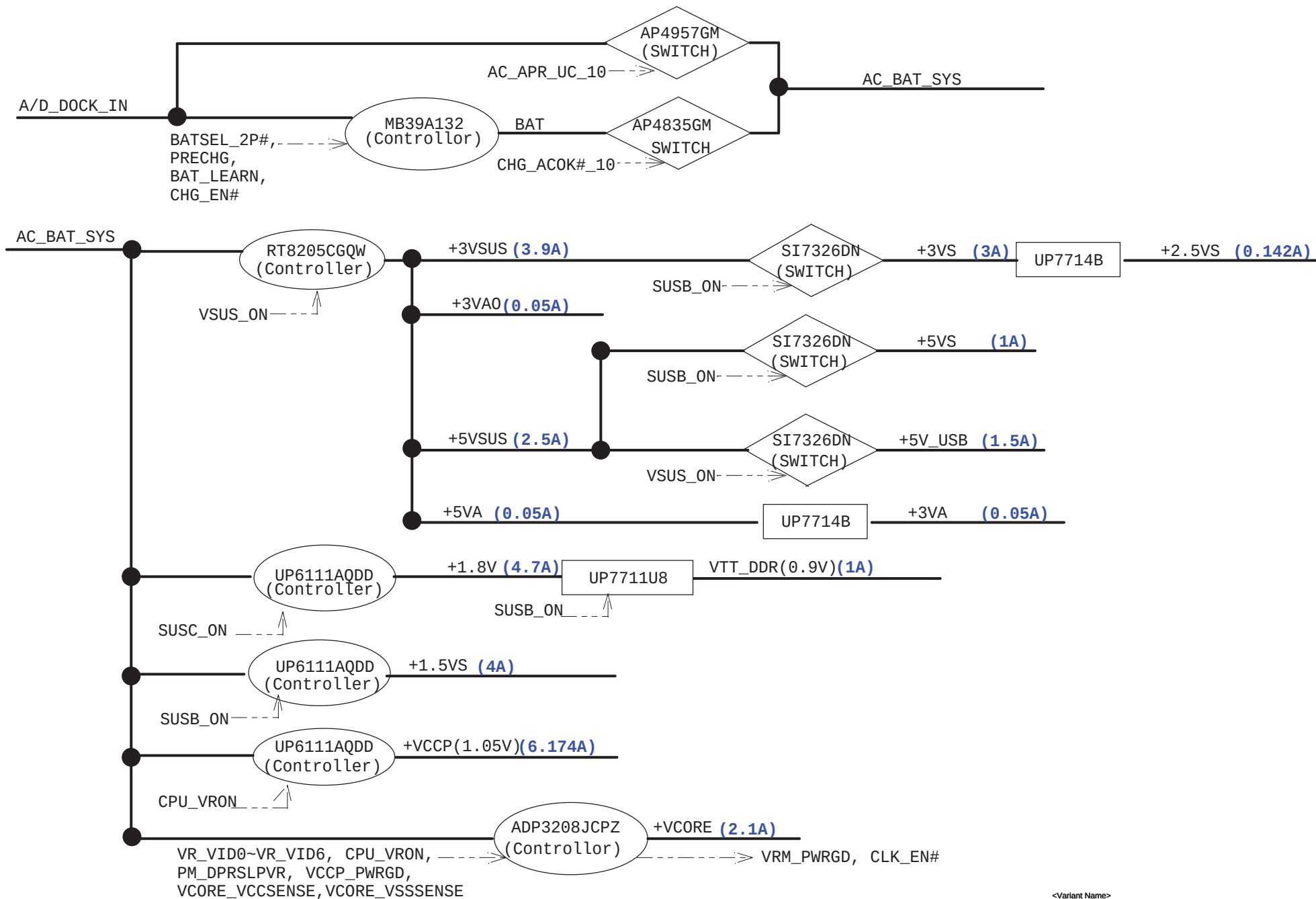
<Variant Name>

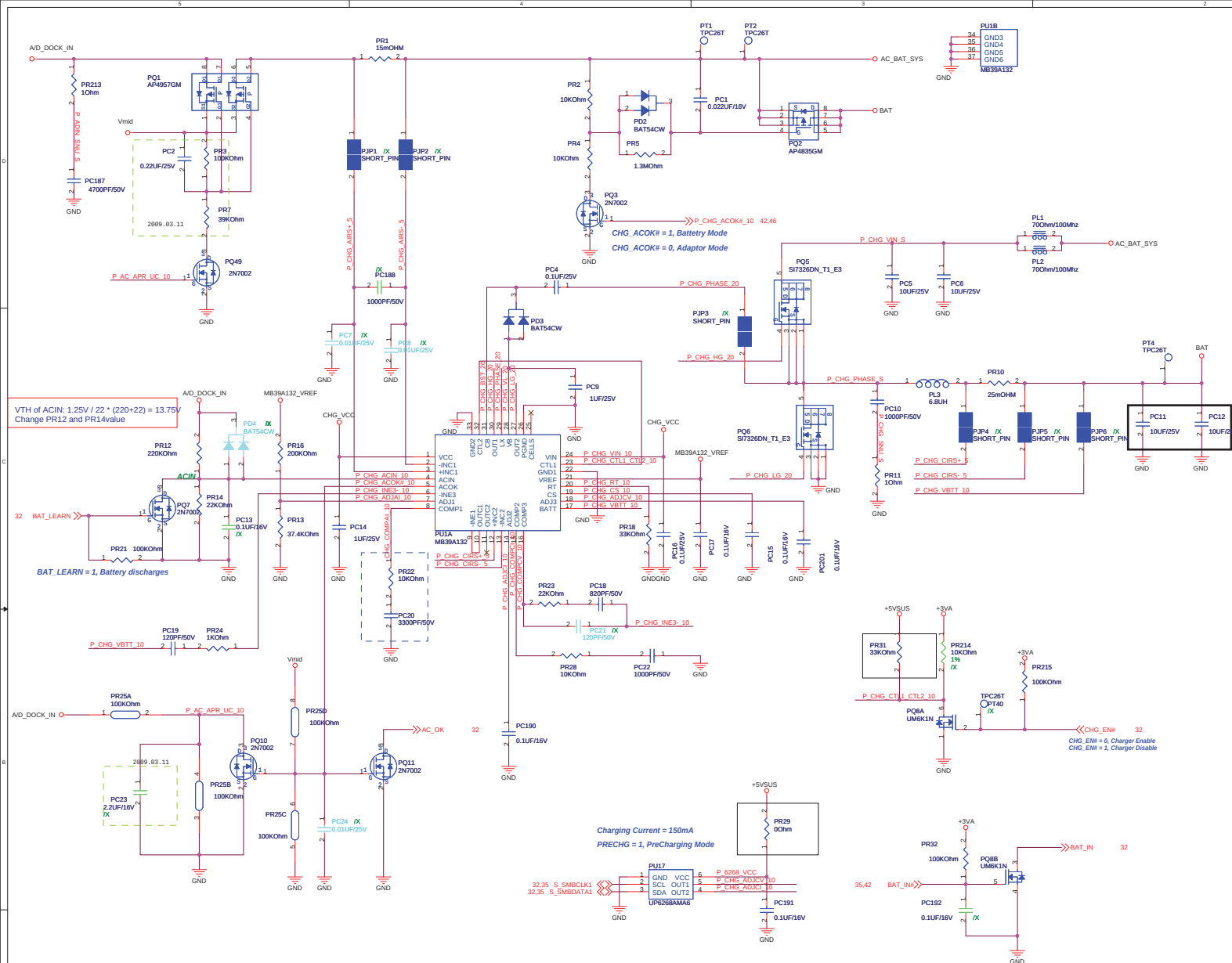


4 C_48M_CARD_READER >>>
17 U_CARD+ >>>
17 U_CARD- >>>
18 CR_PWREN# >>>









Power stage

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$$

2. Ripple Current:

$$I_{rip} = 1.18A$$
$$I_{spec} = 2A \text{ @ } 1 \text{ pcs}$$

3. Inductor Spec:

$$I_{sat} = 10A$$
$$I_{dc} = 5.5A$$
$$DCR = 37m\Omega$$

4. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ m}\Omega \quad (V_{gs} = 4.5V)$$
$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$
$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ m}\Omega \quad (V_{gs} = 4.5V)$$
$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$
$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

Controller

1. Voltage & Current:

$$+12.6V @ 2.5A$$

2. Frequency:

$$PR18 = 33K\Omega, F_{osc} = 515KHz$$

3. OCP:

N/A

4. POR:

$$POR \text{ Hysteresis} = 0.1V$$
$$V_{on} = 7.5V$$

5. Enable Voltage:

$$V = 2.9V$$

6. Soft start time:

$$T_{ss} = 23ms$$

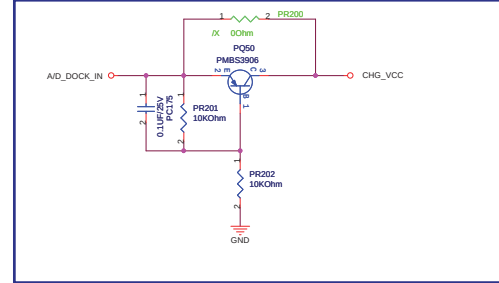
7. Phase selection:

N/A

8. Inrush Current:

$$C_{total} = 20\mu F$$
$$I_{inrush} = 0.01A$$

MODIFY FOR 19V ADAPTER



Battery Charging Current :

$$4.4V > V_{adj2} > 0V \Rightarrow$$
$$I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$$
$$BATSEL_2P\# = 1, I_{ch} = 1.49A$$
$$BATSEL_2P\# = 0, I_{ch} = 2.5A$$

Input Adaptor Max. Current Limit :

$$I_{limit_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$$

Pre-Charging Mode :

$$\text{Precharging current} = 149.2mA$$
$$V_{adj2} = 168mV$$

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor
Adaptor < 13.75V, System Powered by Battery

Battery Charging Voltage :

$$V_{adj3} : V_{REF} \Rightarrow V_{bat} = 4.2V / \text{cell}$$
$$3.9V > V_{adj3} > 2.4V \Rightarrow V_{bat} = 4.35V / \text{cell}$$
$$V_{adj3} : GND \Rightarrow V_{bat} = 4.0V / \text{cell}$$
$$2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 \cdot V_{adj3} / \text{cell}$$

Battery Cell Selection :

CELLS: VREF $\Rightarrow$ 4 Cells;
CELLS: OPEN $\Rightarrow$ 3 Cells;
CELLS: GND $\Rightarrow$ 2 Cells;

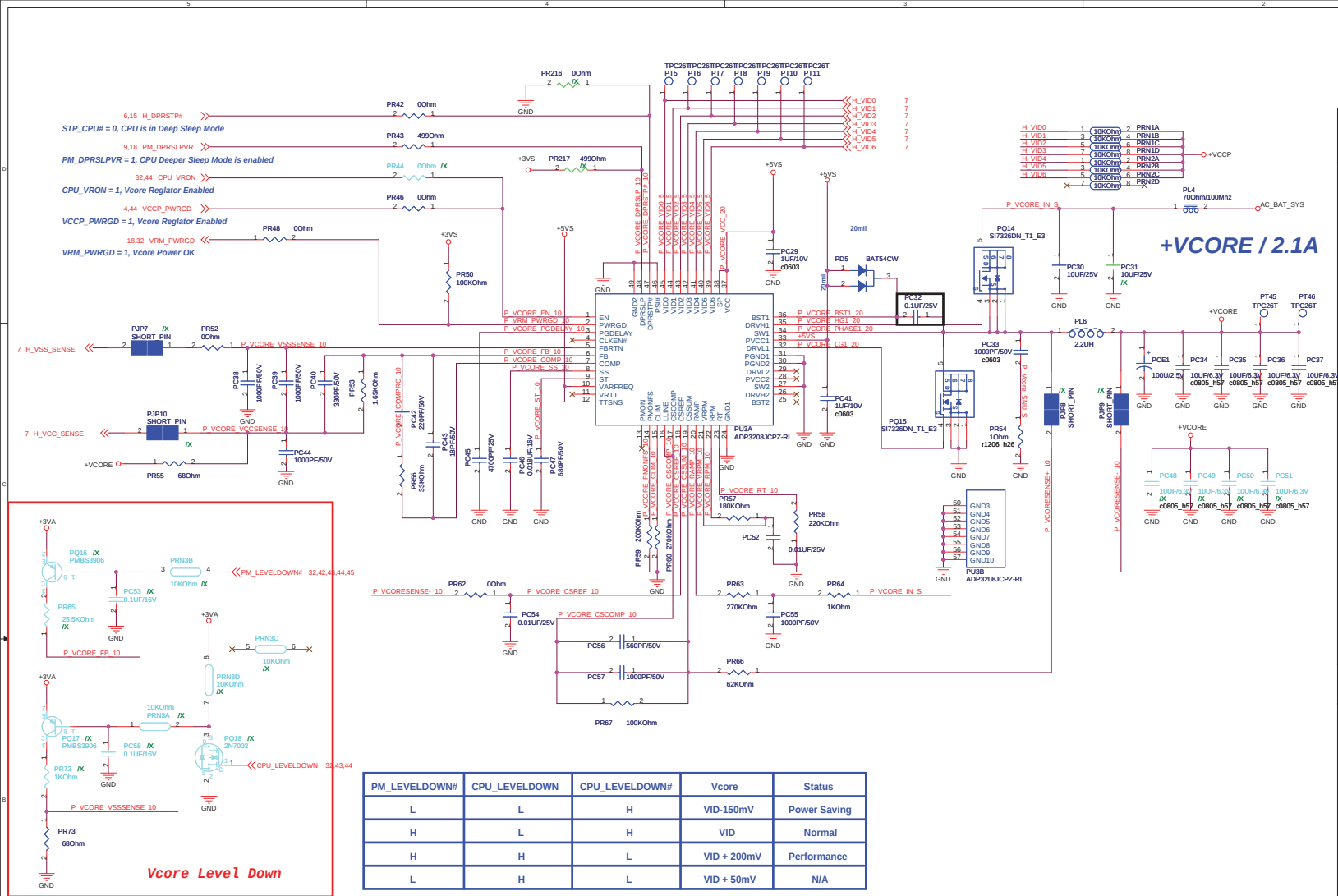
VREF = 5.0V

$$f_{osc}(KHz) = 17000 / R_T (K\Omega) = 515KHz$$

$$\text{Soft start: } t_s(s) = 0.13 \cdot C_S (\mu F)$$

<Variant Name>

ASUS		Title : Charger	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	1.00
A2	1005SHA		
Date: Thursday, March 10, 2016		Sheet 40 of 40	



Power Stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.32A$
- Ripple Current:**
 $I_{rip} = 0.6A$
 $I_{spec} = 2.5A$
- Dynamic:**
 $I_{peak} = 2.1A$
 $ESR / 1 \text{ pcs} = 18m\Omega$
 $V = 38mV$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18m\Omega$

- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3

$R_{ds(ON)} = 22m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)

L-side MOSFET: SI7326DN_T1_E3

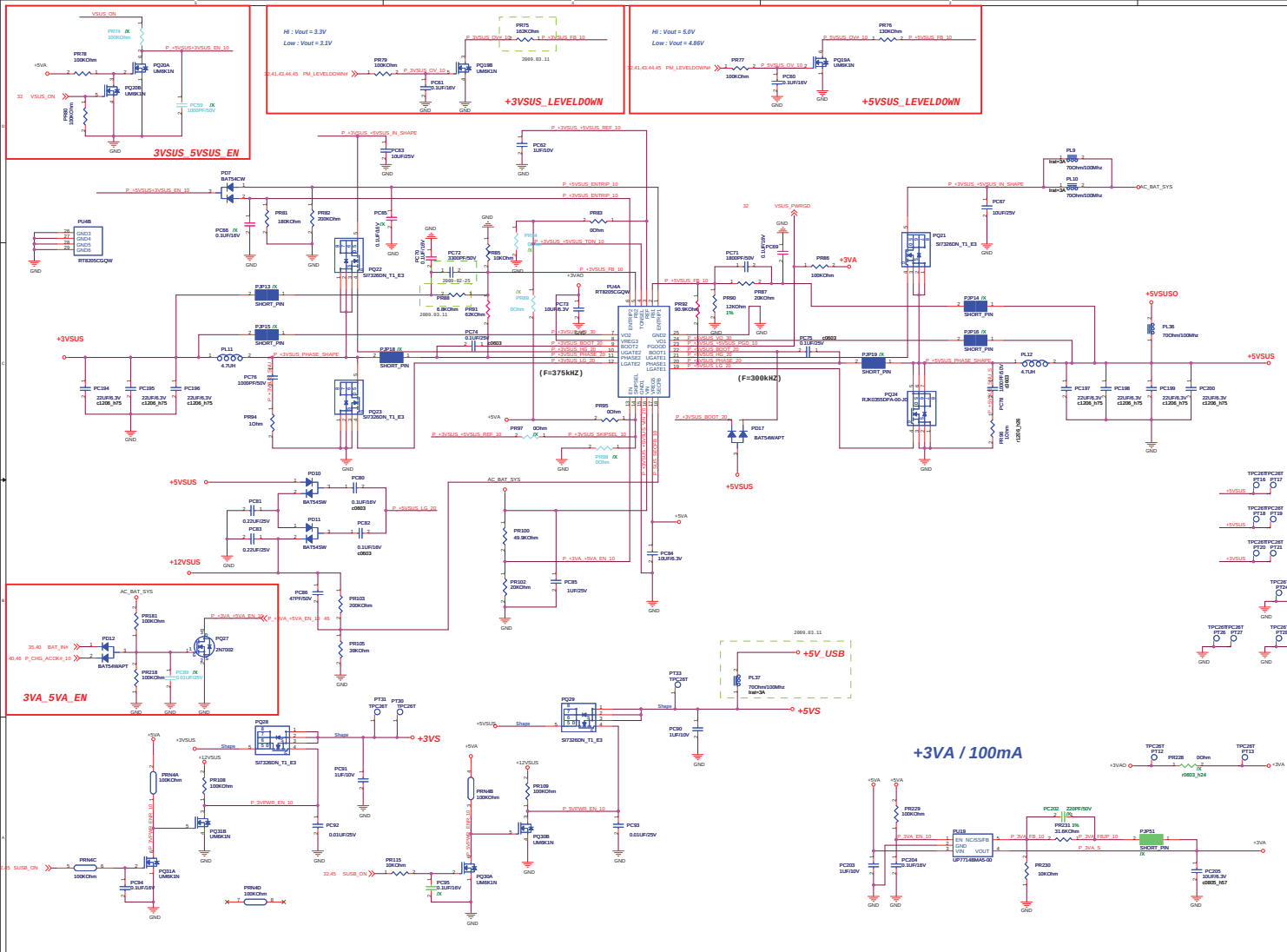
$R_{ds(ON)} = 22m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause $\leq 10\mu s$)

Controller

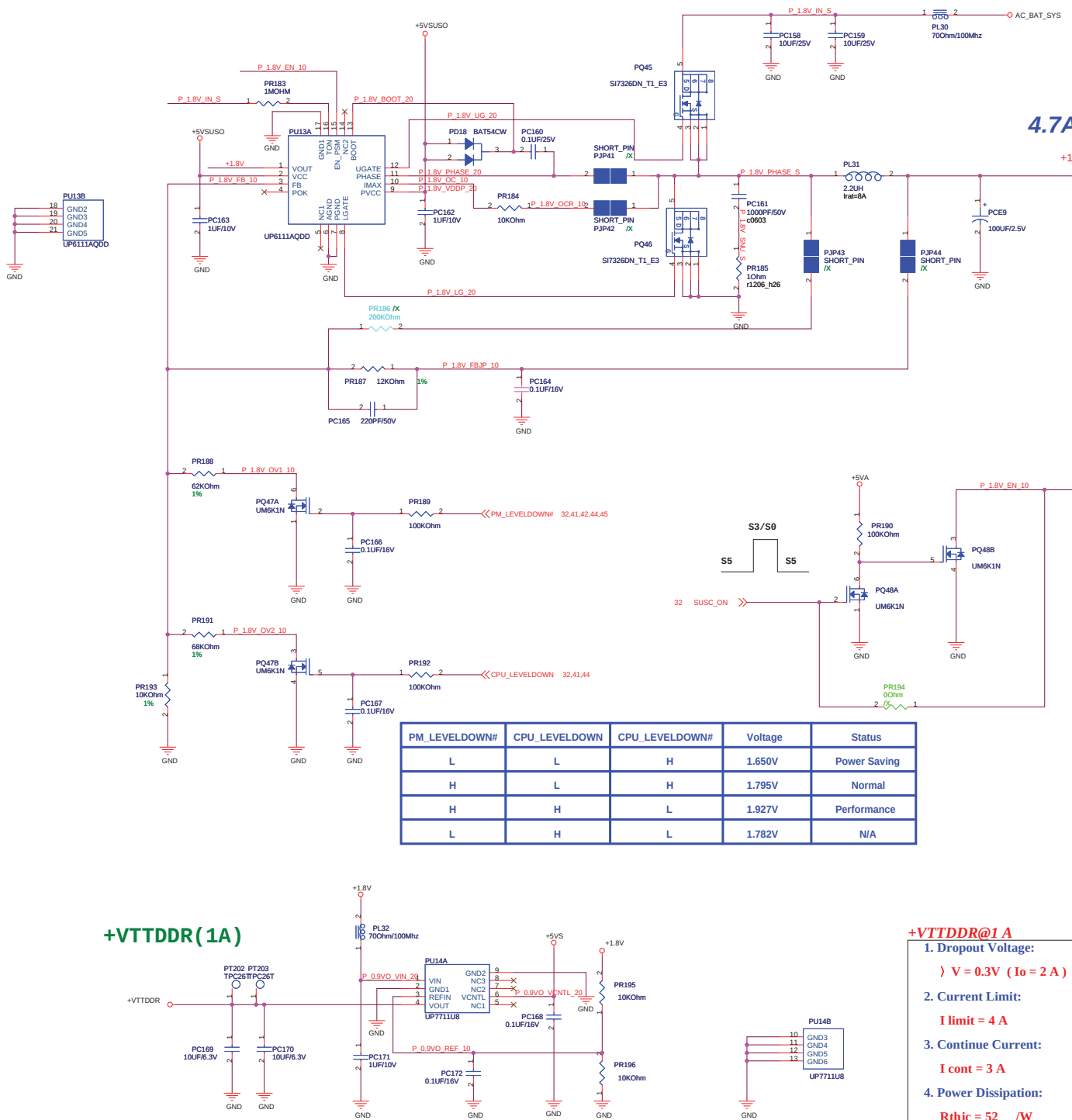
- Voltage & Current:**
 $V_{CORE} = 0.5-1.5V @ 2.1A$
- Frequency:**
Set PR58=220Kohm
Fosc=322KHz for RPM
Set PR57=180Kohm
Fosc=272KHz for CCM
- OCP:**
Set PR60=270KOHM
I_{ocp}=9.3A
- POR:**
POR Hysteresis =0.15V
V_{on} =4.4-4.5 V
V_{off} =4.0-4.2 V

- UVP:**
VID=300mV
- OVP:**
VID+200mV
- Soft start time:**
2.7ms
- Phase selection:**
SP=VCC
single phase
- Loadline:**
30mOhm

<Variant Name>



Power stage		+3VSUS	+5VSUS
1. I/P Current:		$I_{in} = V_o I_o / (0.8 * V_{in}) = 1.1A$	$I_{in} = V_o I_o / (0.8 * V_{in}) = 1.67A$
2. Ripple Current:		$I_{rip} = 1.36A$ $I_{spec} = 2.5A$ @1 pcs	$I_{rip} = 2.07A$ $I_{spec} = 2.5A$ @1 pcs
3. Dynamic:		$I_{peak} = 3A$ ESR / 1 pcs = 18 mohm V = 54mV	$I_{peak} = 3A$ ESR / 1 pcs = 18 mohm V = 54mV
4. Inductor Spec:		$I_{sat} = 10A$ $I_{dc} = 5.5A$ DCR = 37 mohm	$I_{sat} = 10A$ $I_{dc} = 5.5A$ DCR = 37 mohm
5. MOSFET Spec:		H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause $\geq 10\text{ us}$) L-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause $\geq 10\text{ us}$)	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22\text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause $\geq 10\text{ us}$) L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 10.7\text{ mohm}$ ($V_{gs} = 10V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause $\geq 10\text{ us}$)
Controller		+3VSUS	+5VSUS
1. Voltage & Current:		+3VSUS=3.3V@3A	+5VSUS=5V@2.5A
2. Frequency:		fosc=375KHz	fosc=300KHz
3. OCP:		Set PR81=180Kohm Iocp=8A	Set PR82=200Kohm Iocp=17A
4. POR:		V on =4.35-4.5 V V off =3.9-4.25 V	V on =4.35-4.5 V V off =3.9-4.25 V
5. UVP:		V uvp= 70% Vout	V uvp= 70% Vout
6. OVP:		V ovp=115%Vout	V ovp=115%Vout
7. Enable Voltage:		V rising = 1V V falling = 0.4 V	V rising = 1V V falling = 0.4 V
8. Soft start time:		Tss=2ms	Tss=2ms
9. Phase selection:		/X	/X
10. Inrush Current:		C total = 100 uF I inrush= 0.165 A	C total = 100 uF I inrush= 0.25 A
+3VA AEC/100mA		1. Dropout Voltage: V = 0.21V ($I_o = 0.3A$) 2. OCP: I ocp=480mA 3. Short Circuit Current Limit: I sc= 320mA 4. Power Dissipation: Rthjc =250 /W Pd =0.4W	5. EN Voltage: V en = 2V V d = 6. New OK Voltage: Vpkth = 92%*Vout Vpkhys = 8% 7. Inrush current: T ss = 400uS C total =10uF I inrush 8. Feedback: VFB = 0.8 V



Power stage

1. I/P Current:

$$I_{in} = V_o * I_o / (0.8 * V_{in}) = 1.175A$$

2. Ripple Current:

$$I_{rip} = 1.88A$$

$$I_{spec} = 2.5A \odot 1$$

3. Dynamic:

$$I_{peak} = 4.7A$$

$$ESR / 1 \text{ pcs} = 18 \text{ mohm}$$

$$V = 84.6mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 18 \text{ mohm}$$

5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

Controller

1. Voltage & Current:

$$+1.8V @ 5.8A$$

2. Frequency:

$$PR183 = 1M \text{ ohm}$$

$$F_{osc} = 250KHz$$

3. OCP:

$$PR184 = 10K \text{ ohm} \rightarrow 9A$$

4. POR:

$$V_{ccrth} = 3.7 \sim 4.1V$$

$$V_{cclys} = 0.2V$$

5. UVP:

$$V_{out} = 70\%$$

6. OVP:

$$V_{out} = 115\%$$

7. Enable Voltage:

$$V = 2.9V$$

8. Soft start time:

$$T_{ss} = 1.2 \text{ ms}$$

9. Phase selection:

$$IX$$

10. Inrush Current:

$$C_{total} = 100 \mu F$$

$$I_{inrush} = 0.15A$$

+VTTDDR@1A

1. Dropout Voltage:

$$V = 0.3V \quad (I_o = 2A)$$

2. Current Limit:

$$I_{limit} = 4A$$

3. Continue Current:

$$I_{cont} = 3A$$

4. Power Dissipation:

$$R_{thjc} = 52^\circ C/W$$

$$P_d = 1.9W$$

5. EN Voltage:

$$V_{en} = 1.4V$$

$$V_{sd} = 0.8V$$

6. Supply Voltage:

$$V_{cc} = 5V$$

7. Inrush current:

$$T_{ss} = 5 \text{ ms}$$

$$C_{total} = 10 \mu F$$

$$I_{inrush} = 1.8 \text{ mA}$$

<Variant Name>



Title : +1.8V & +VTTDDR

ASUSTek Computer INC.

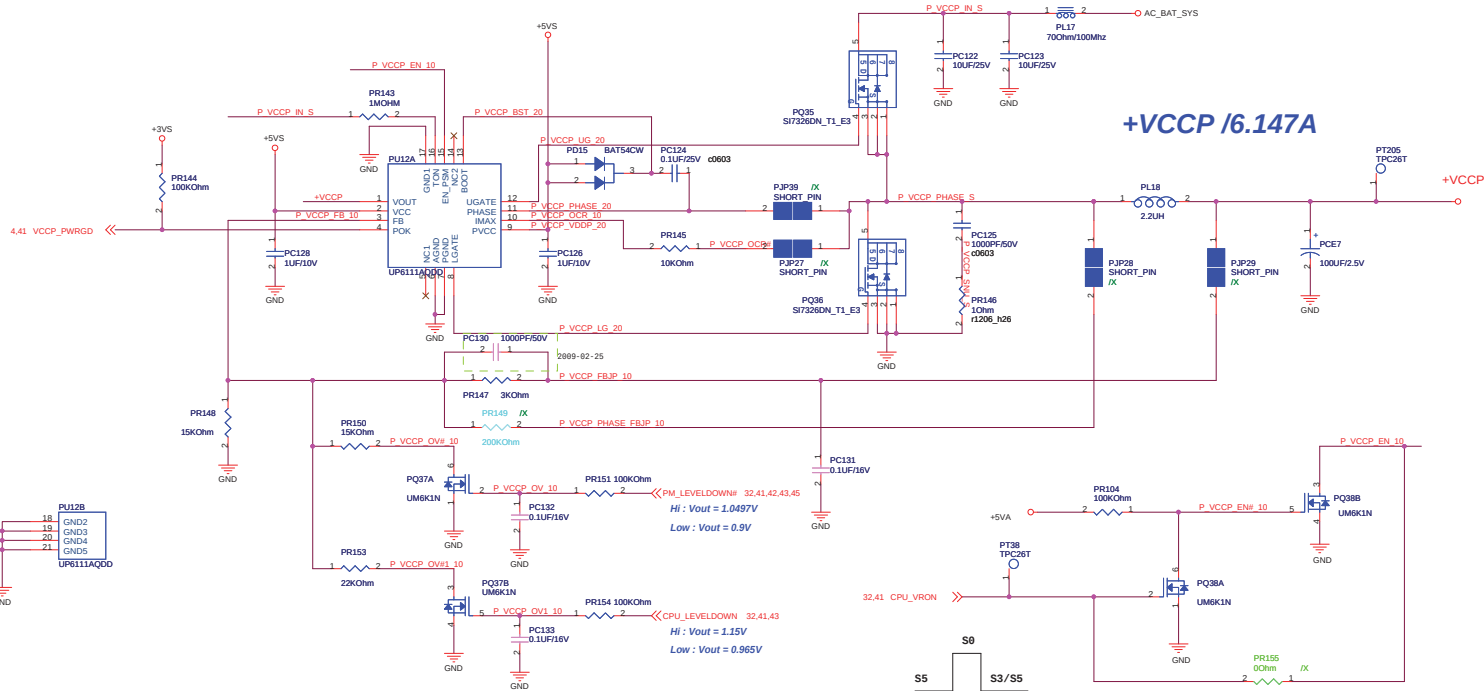
Engineer: Joy_Zhou

Size Project Name
c 1005HA

Date: Thursday, March 19, 2009

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Rev 1.06



Power stage

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.89A$$

2. Ripple Current:

$$I_{rip} = 1.93A$$

$$I_{spec} = 2.5A @ 1$$

3. Dynamic:

$$I_{peak} = 6.147A$$

$$ESR / 1 \text{ pcs} = 18 \text{ mohm}$$

$$V = 110mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 18 \text{ mohm}$$

5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

Controller

1. Voltage & Current:

$$+VCCP @ 6.147A$$

$$PR143 = 1.3M \text{ ohm}$$

$$F_{osc} = 188KHz$$

$$PR145 = 10K \text{ ohm} \rightarrow 9A$$

$$V_{ccrth} = 3.7 \sim 4.1V$$

$$V_{cchys} = 0.2V$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

$$V_{out} = 70\%$$

6. OVP:

$$V_{out} * 115\%$$

7. Enable Voltage:

$$V = 2.9V$$

8. Soft start time:

$$T_{ss} = 1.2 \text{ ms}$$

9. Phase selection:

$$IX$$

10. Inrush Current:

$$C_{total} = 100 \mu F$$

$$I_{inrush} = 0.0875A$$

$$I_{inrush} = 0.0875A$$

$$I_{inrush} = 0.0875A$$

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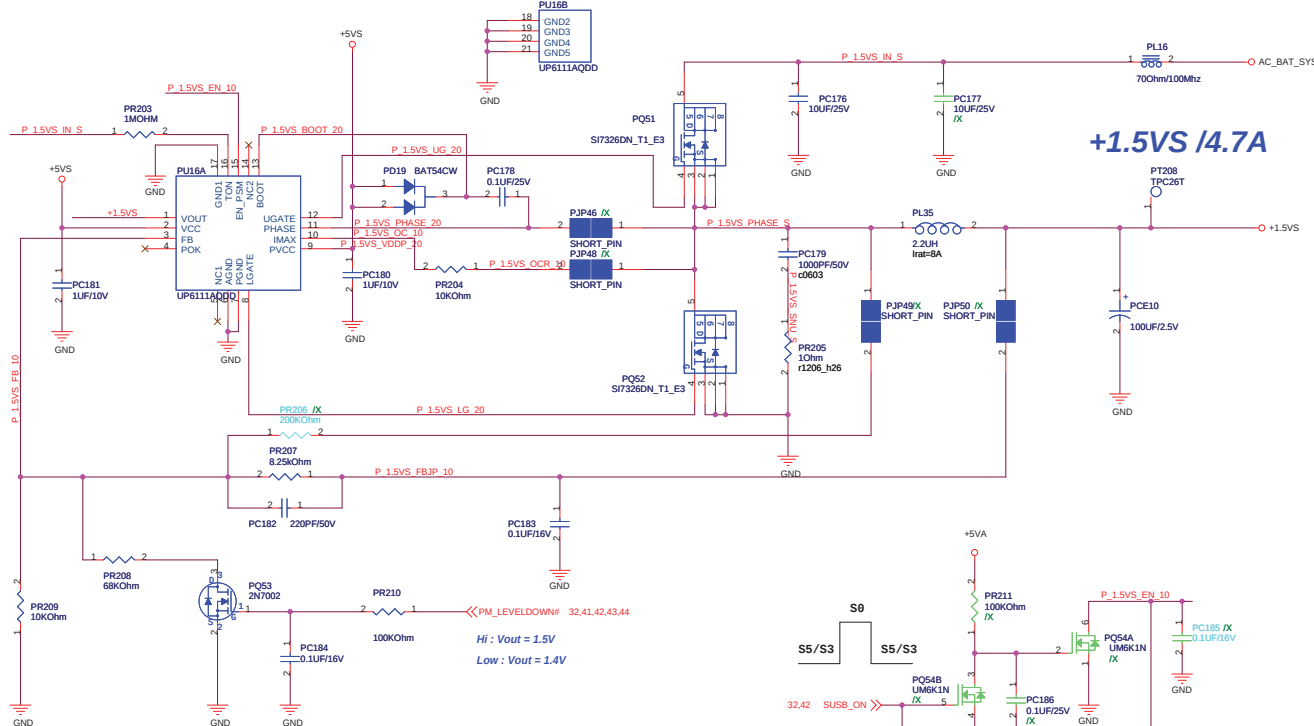
$$I_{inrush} = 0.0875A$$

$$I_{inrush} = 0.0875A$$

PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.9V	Power Saving
H	L	H	1.050V	Normal
H	H	L	1.152V	Performance
L	H	L	1.002V	N/A

<Variant Name>

ASUS		Title : VCCP	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	1.30
A2	1005HA		
Date: Thursday, March 19, 2009		Sheet 44 of 48	



+1.5VS / 4.7A

Power stage

1. I/P Current:

$$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.83A$$

2. Ripple Current:

$$I_{rip} = 1.5A$$

$$I_{spec} = 2.5A @ 1$$

3. Dynamic:

$$I_{peak} = 4.7A$$

$$ESR / 1 \text{ pcs} = 18 \text{ mohm}$$

$$V = 84.6mV$$

4. Inductor Spec:

$$I_{sat} = 14A$$

$$I_{dc} = 8A$$

$$DCR = 18 \text{ mohm}$$

5. MOSFET Spec:

H-side MOSFET: SI7326DN_T1_E3

$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

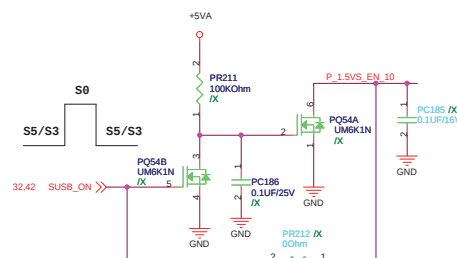
$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$

L-side MOSFET: SI7326DN_T1_E3

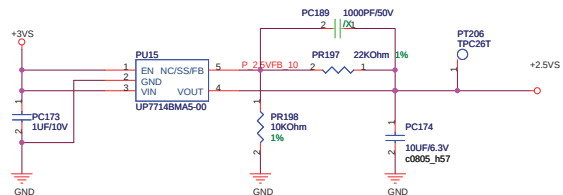
$$R_{ds(ON)} = 22 \text{ mohm} \quad (V_{gs} = 4.5V)$$

$$I_{cont} = 6.5A \quad (T = 25^\circ C)$$

$$I_{peak} = 40A \quad (\text{Pause} \geq 10 \mu s)$$



+2.5V / 142mA



Ver	Description	Date
1.0G	change UF1 to the same as 1005hn's	2009.0122.2027
	change lvds conn P/N to 12G170190201 change CPU P/N from 01G012290000 to 01G012520100 P4: 糠 CC50 ..CC57 盤箒臂 clock gen pin 狼 P23: 糠 GC21 P29: 奔IL2	2009.0203.1555
	update NB symbol 癸clock gen cm WIFI 场だ 酚1005HN 和 稂	2009.0205.1555
	P4: C_PCIE_LAN_R C_PCIE_LAN#_R H_ITP_CKOUT H_ITP_CKOUT# add 10pf for RF P23: cancel BL_EN, G_LVDD_EN, G_NBL_CTRL EMI cap	2009.0205.2120
	ADD LR55 02/14 newjane: Change PR227 to 5% 10G212105004031 02/14 newjane: Change OR1 from 18.2K to 18K 10G212100214010 02/14 newjane: Change HR1 from 68ohm to 56 ohm 02/14 newjane: Change SR1 from 20K 10G212200214110to 20K 10G212200214030 02/14 newjane: ChangeHC18 from 11G23211021115 to 11G232110214030 02/14 newjane: ChangeHC6 GC20 HC11 HC12 from 11G233310531360 to11G233210516320 02/14 newjane: /X LC41 02/14 newjane: SD RC1 RC7 RC12 from 11G232310431360to11G232110411320 02/14 xiao-jie SR4 PR227 from 10G212105004031 to 10G212100414030 02/14 xiao-jie aAR8 AR5 from 10G212200214110 to 10G212200214030 02/14 xiao-jie AR7 P/N toPR105 P/N	2009.0210.1513

