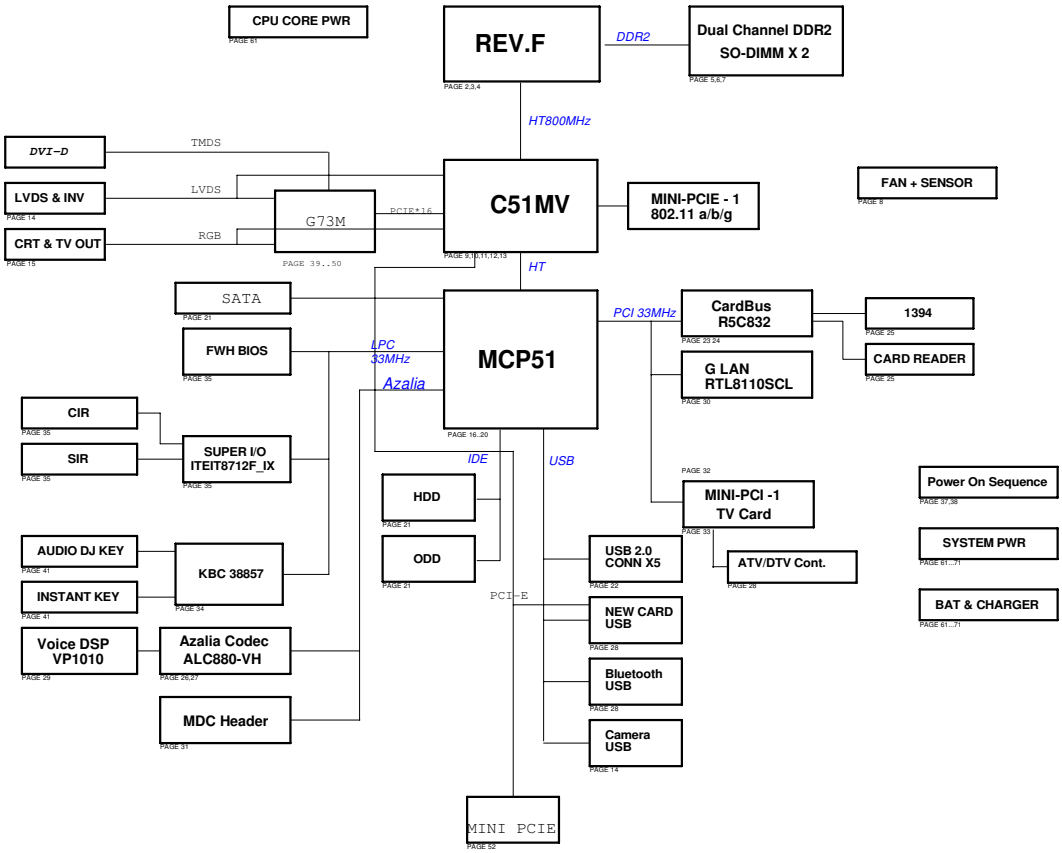
A7T/M BLOCK DIAGRAM



ASUSTeK

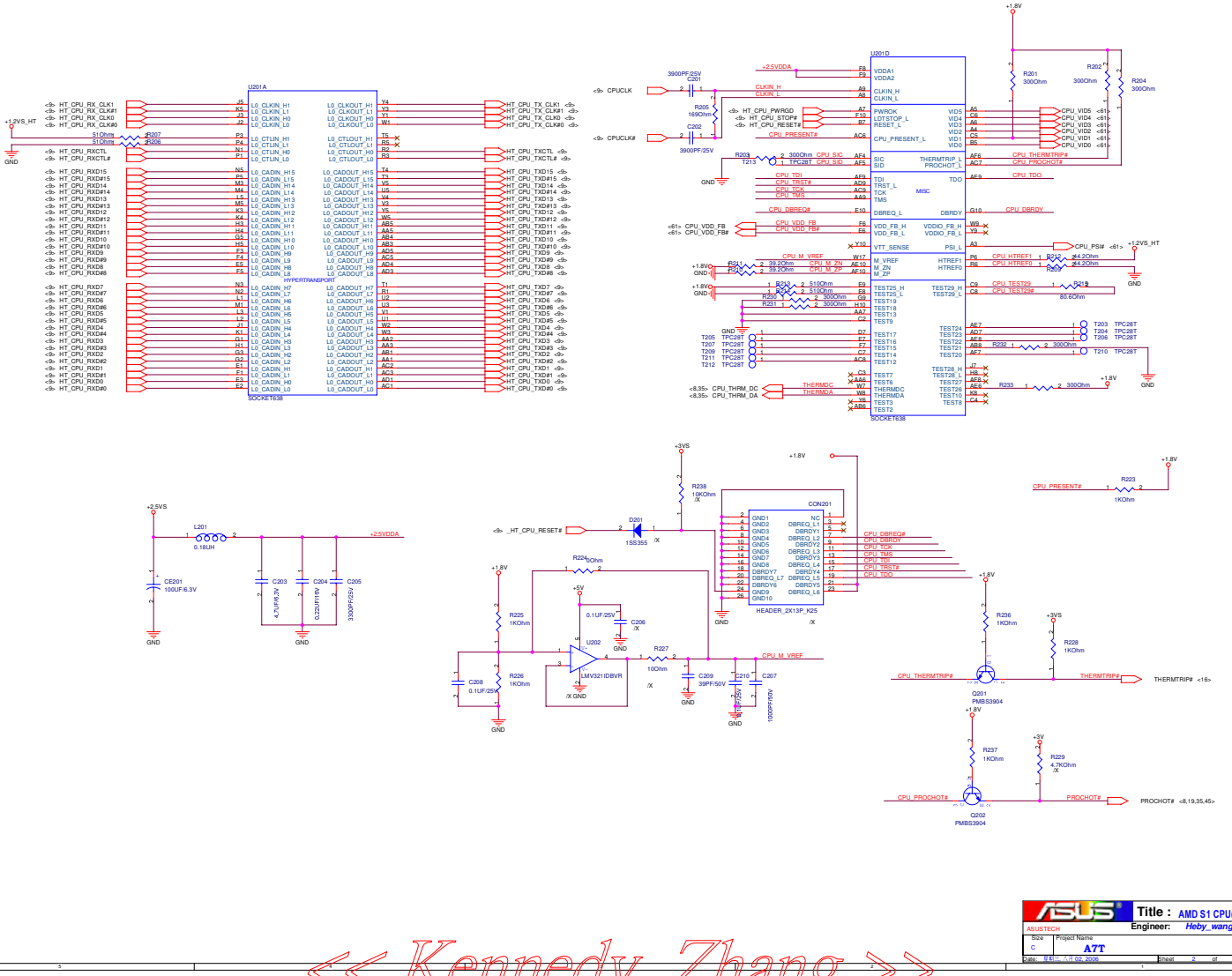
Title : BLOCK DIAGRAM

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

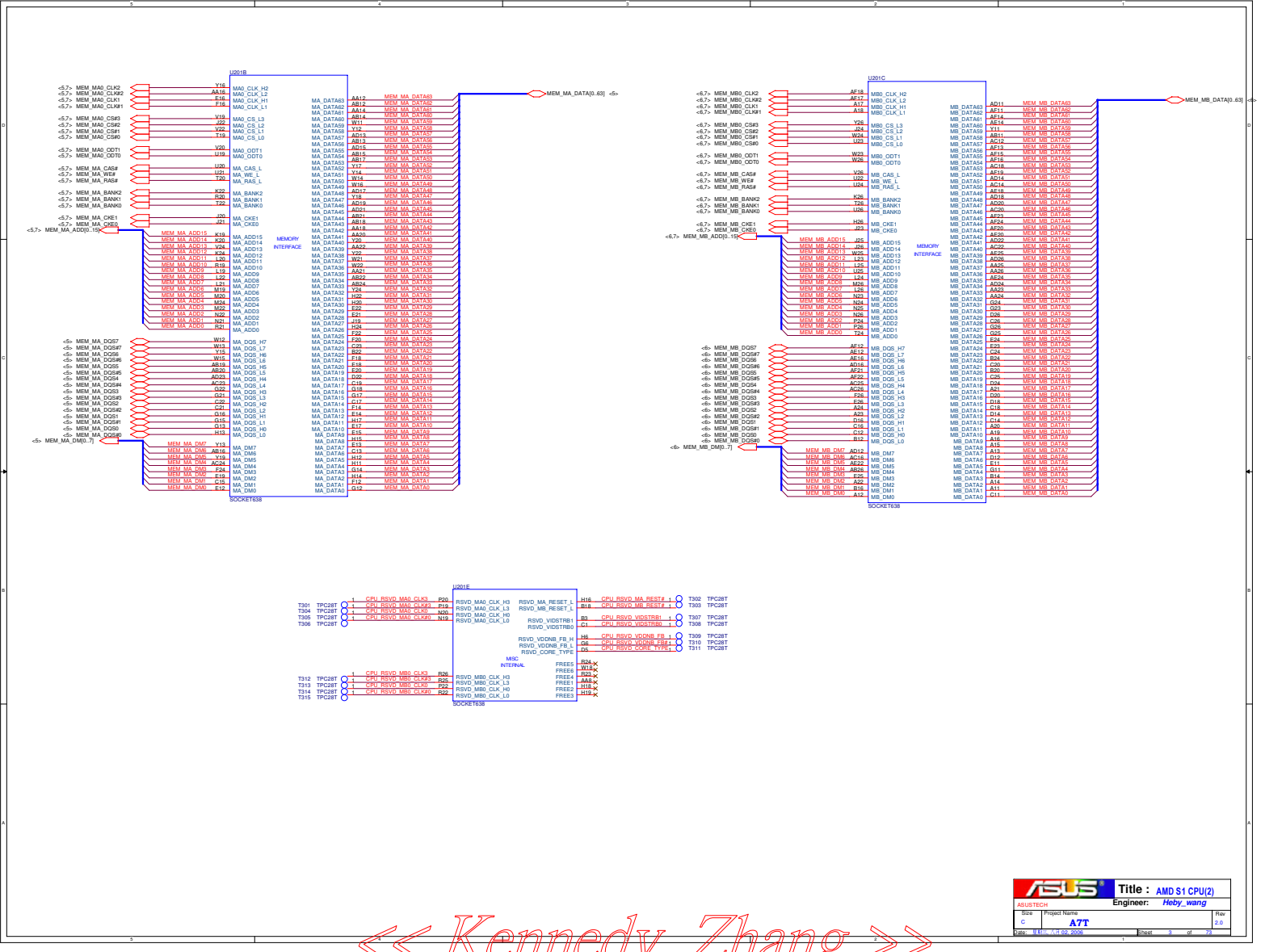
Date: 星期日, 四月 29, 2006 Sheet 1 of 73

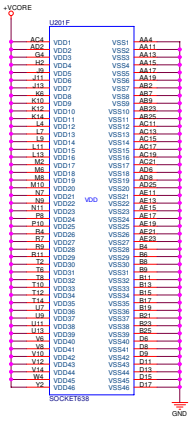
<< Kennedy_Zhang >>

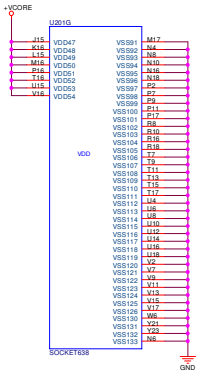


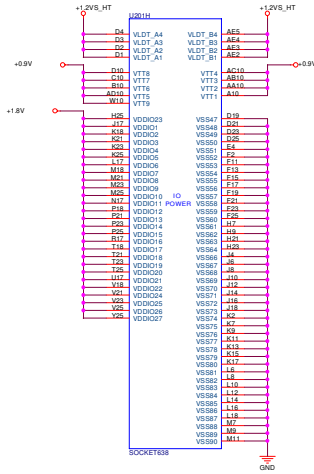
<< Kennedy_Zhang >>

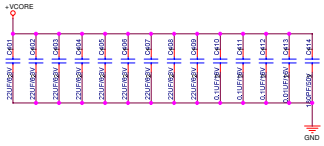
ASUSTECH	Title : AMD S1 CPU(1)		
	Engineer: Heby_wang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期一, 八月 02, 2006	Sheet 2 of 79		

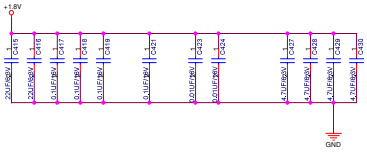


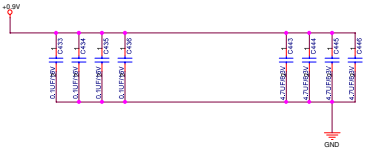


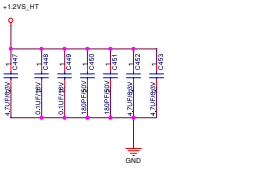






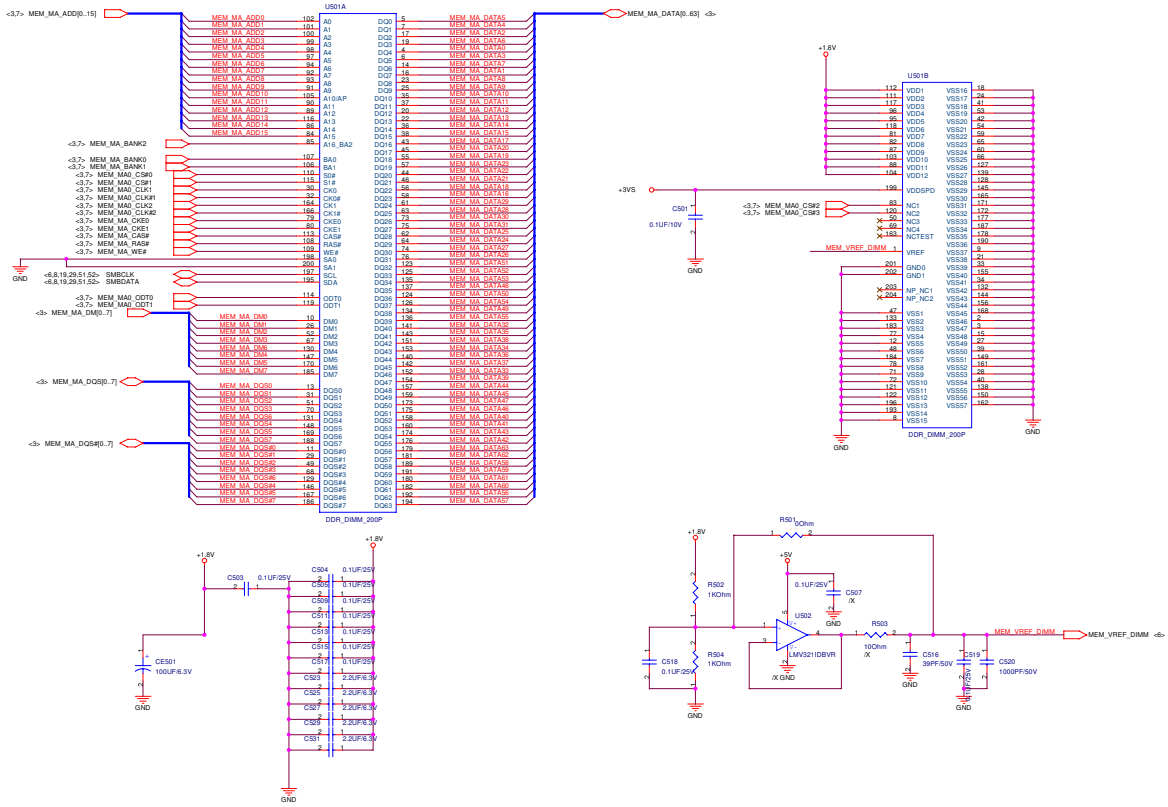






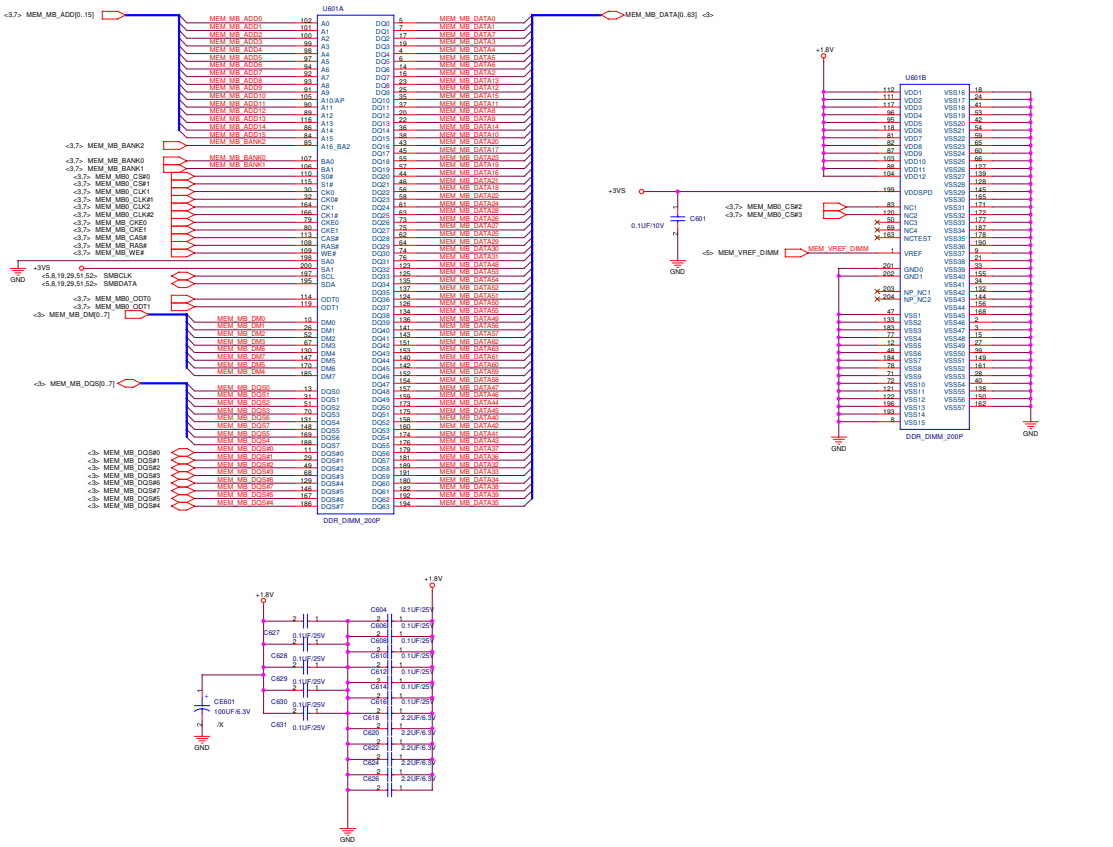
ASUSTECH	Title : AMD S1 CPU(3)	
	Engineer: Heby_wang	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期五, 四月 28, 2006	Sheet 4 of 79	

TOP



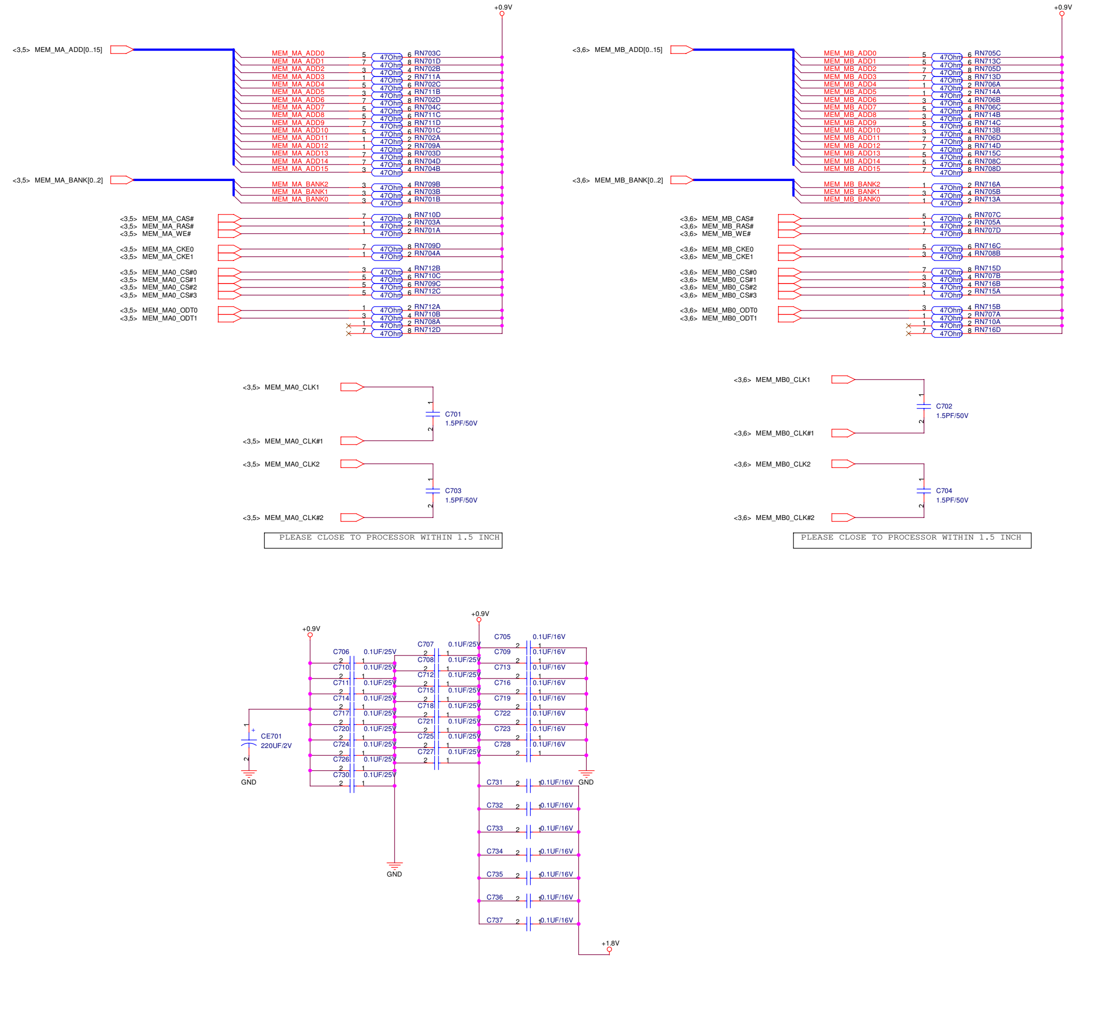
<< Kennedy_Zhang >>

BOTTOM



ASUSTECH	Title : DDR2_SO_DIMM(1)		
	Engineer: Heby_wang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期五, 四月 28, 2006	Sheet 6 of 79		

<< Kennedy_Zhang >>

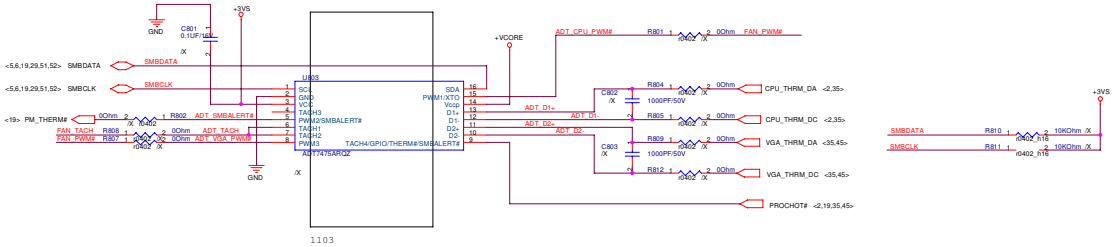


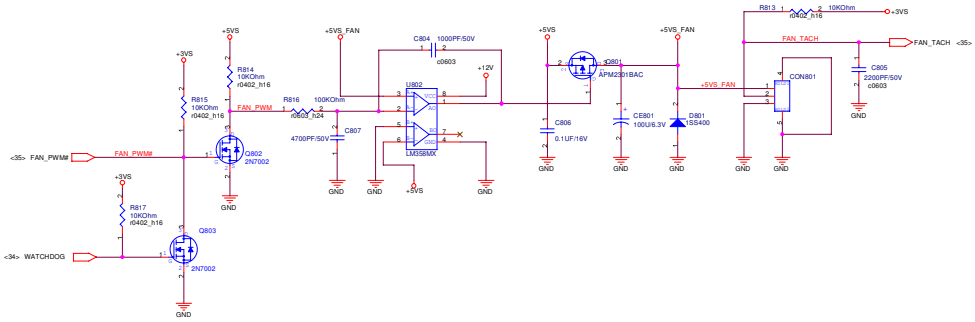
ASUSTECH

Title : DDR2TERMINATIONS

Engineer: Heby_wang

Size C | Project Name A7T | Rev 2.0





Pin 13 State	Pin 14 State	Address
0	Low (10 kΩ to GND)	0101100 (0x2C)
0	High (10 kΩ Pull-Up)	0101101 (0x2D)
1	Don't Care	0101110 (0x2E) (Default)

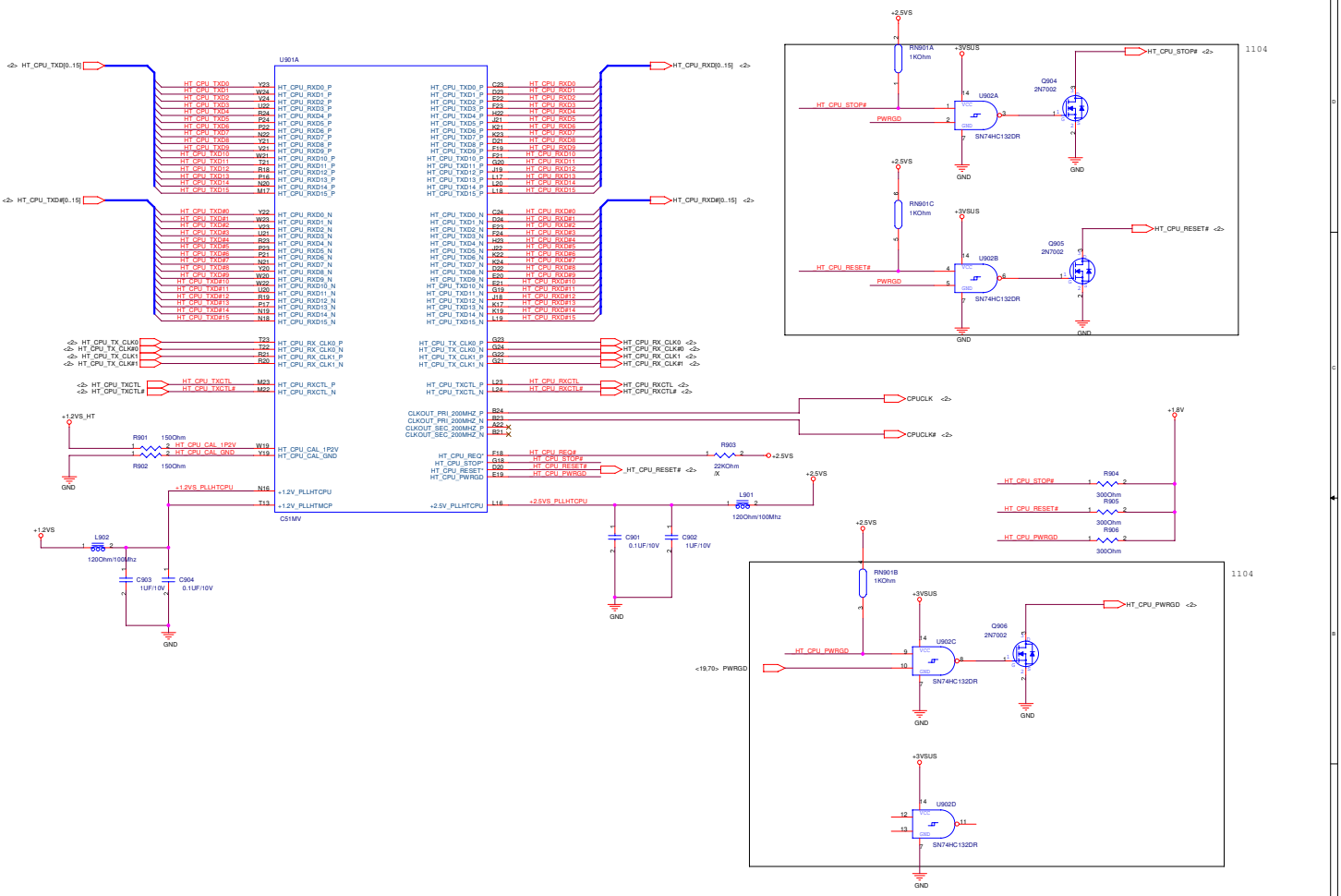
ASUSTECH

Title : THERMAL&FAN

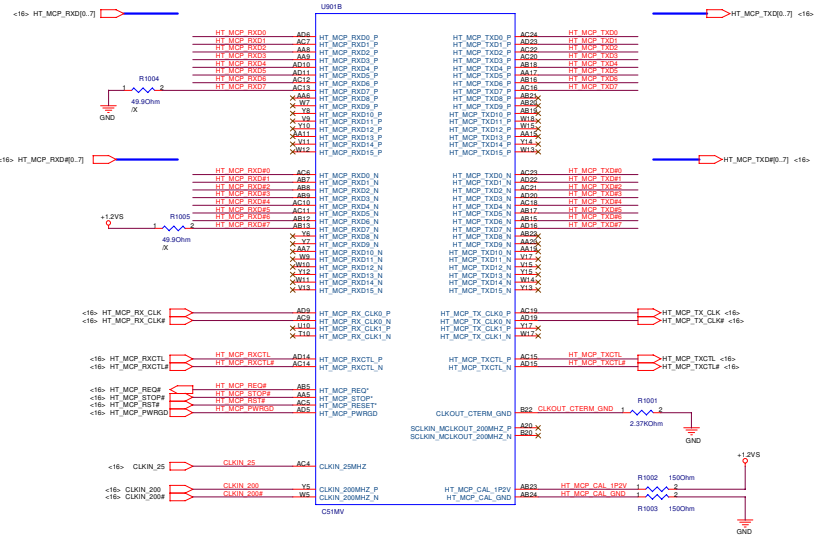
Engineer: Heby_wang

Size	Project Name	Rev
C	A7T	2.0

Date: Wednesday, July 02, 2008 Sheet 8 of 79

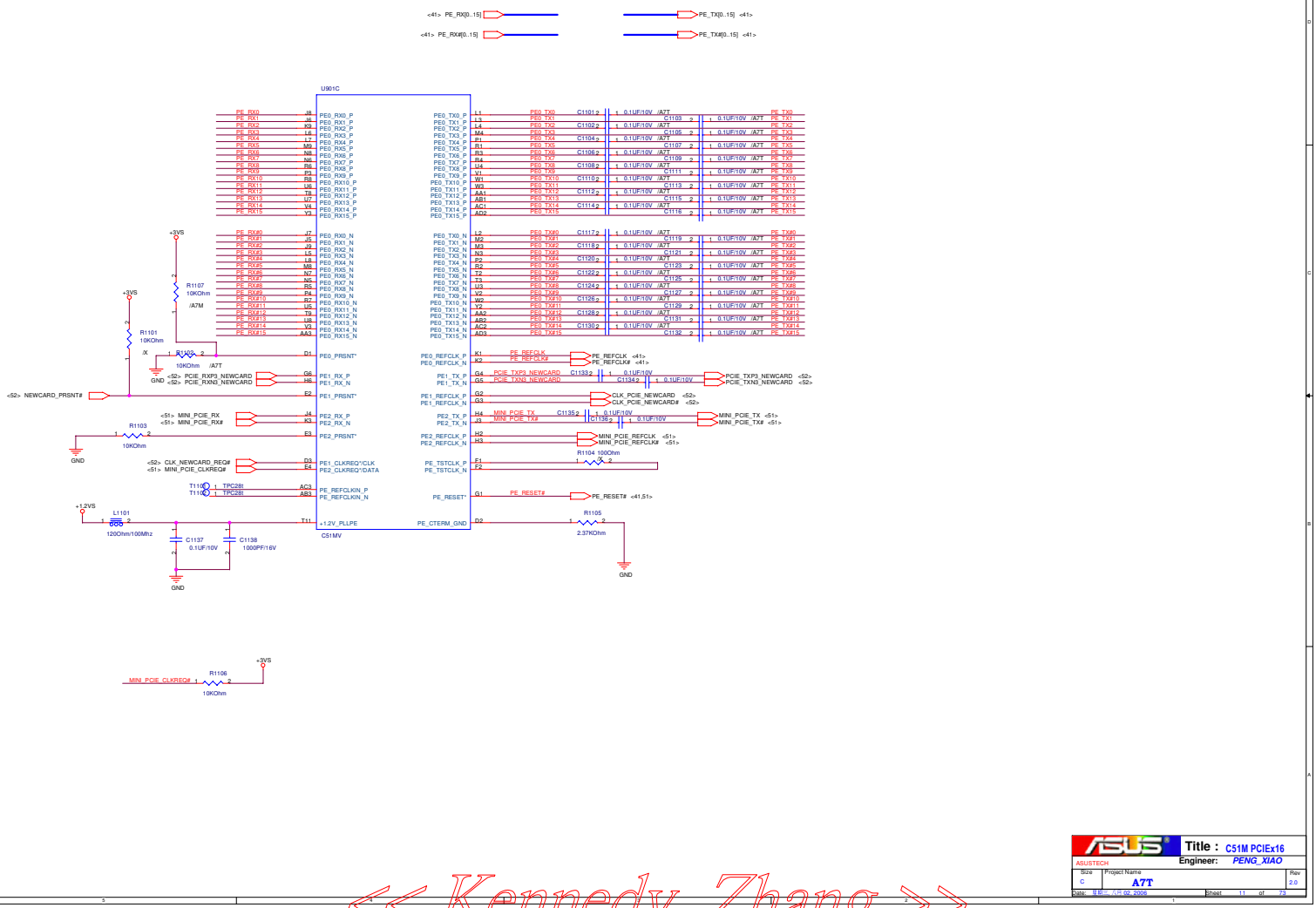


ASUSTeK	Title : C51M HT_CPU		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 9 of 29		

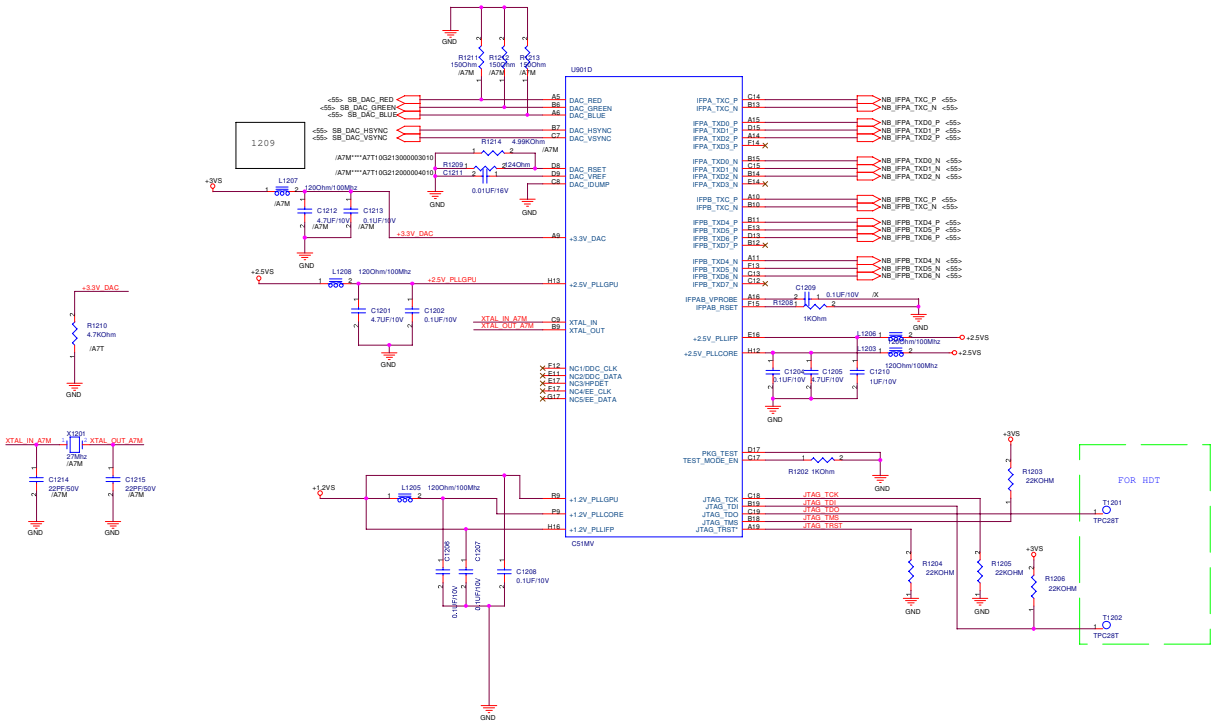


ASUSTeK	Title : C51 HT_MCP		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 10 of 73		

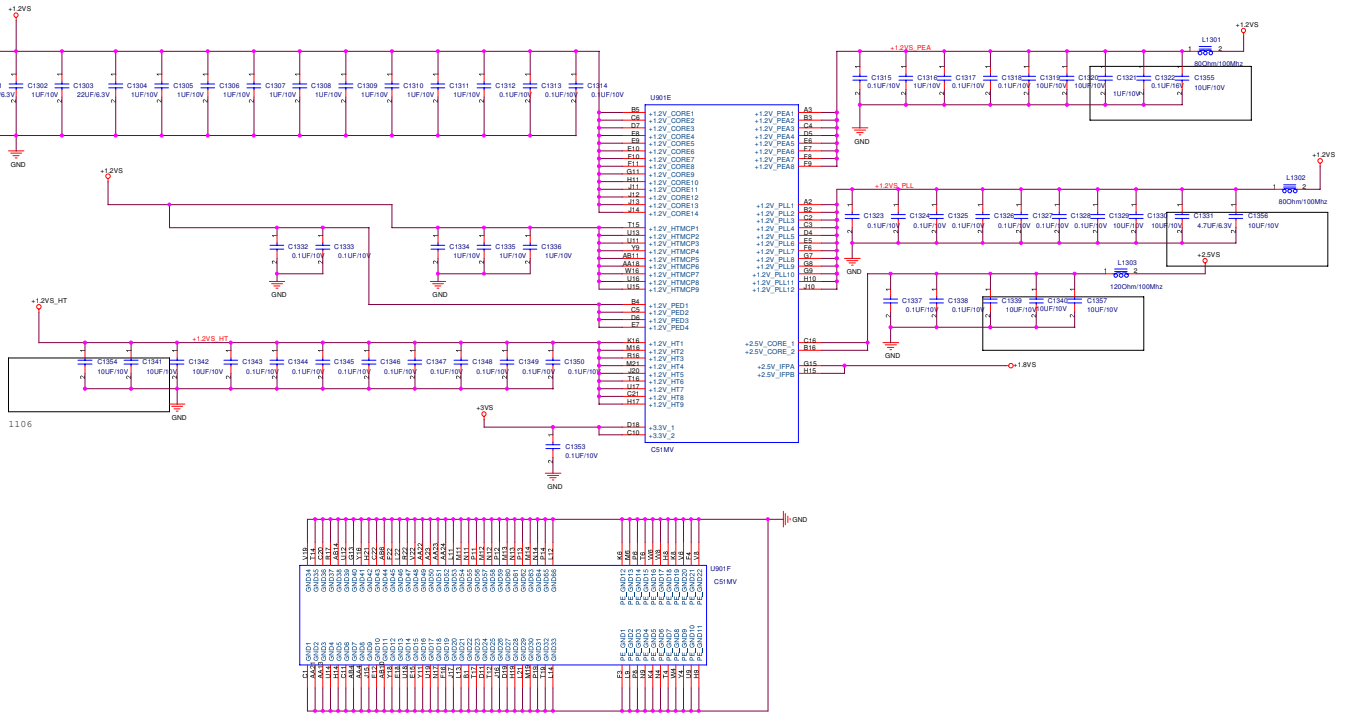
<< Kennedy_Zhang >>



ASUSTeK	Title : C51M PCIEx16		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 11 of 29		



ASUSTECH	Title : C51M RGB&TV OUT	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 12 of 29	



ASUSTeK	Title : C51M PWR&GND	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 13 of 73	

LCD Backlight Control

LCD Power

3-3.6V
S0-S1M:410 mA(500 mA Max.)

3V-3.6V
Full
Active:
410
mA(Max.
500 mA)

SI3865: US$0.22

LCD LVDS Interface

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 18"

INVERTER Interface

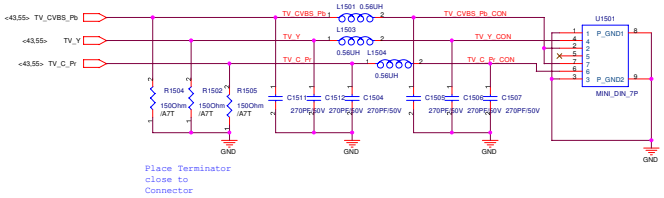
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

700Vrms@5 mArms
(Min. 3 mArms)6
mArms(Max. 6.5
mArms)

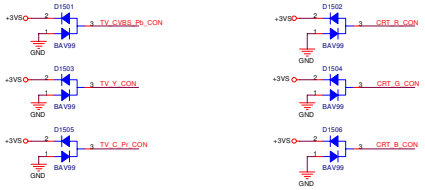
Title : LVDS CONNECTER			
ASUSTECK	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 14 of 29		

<< Kennedy_Zhang >>

TV OUT

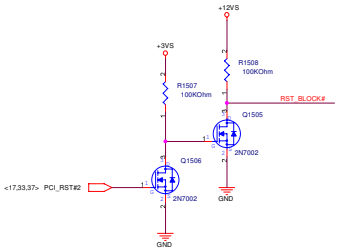


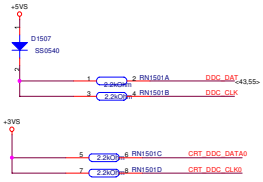
Place Terminator close to Connector



PLACE ESD Diodes near TV port

PLACE ESD Diodes near VGA port

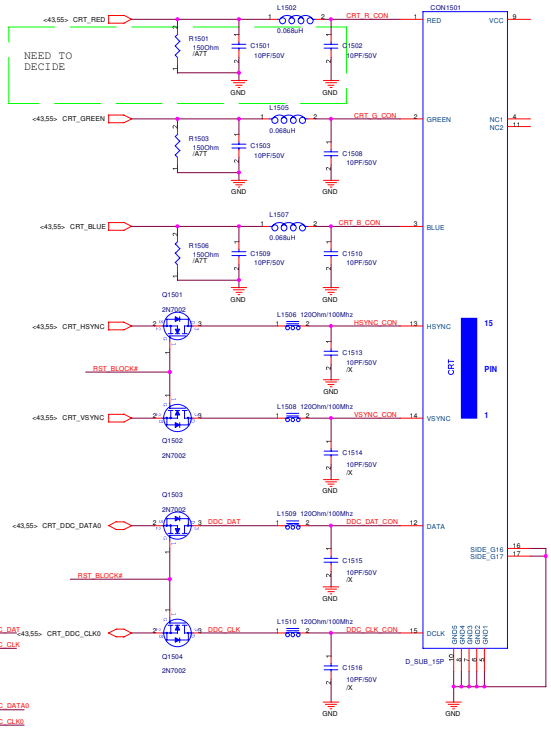




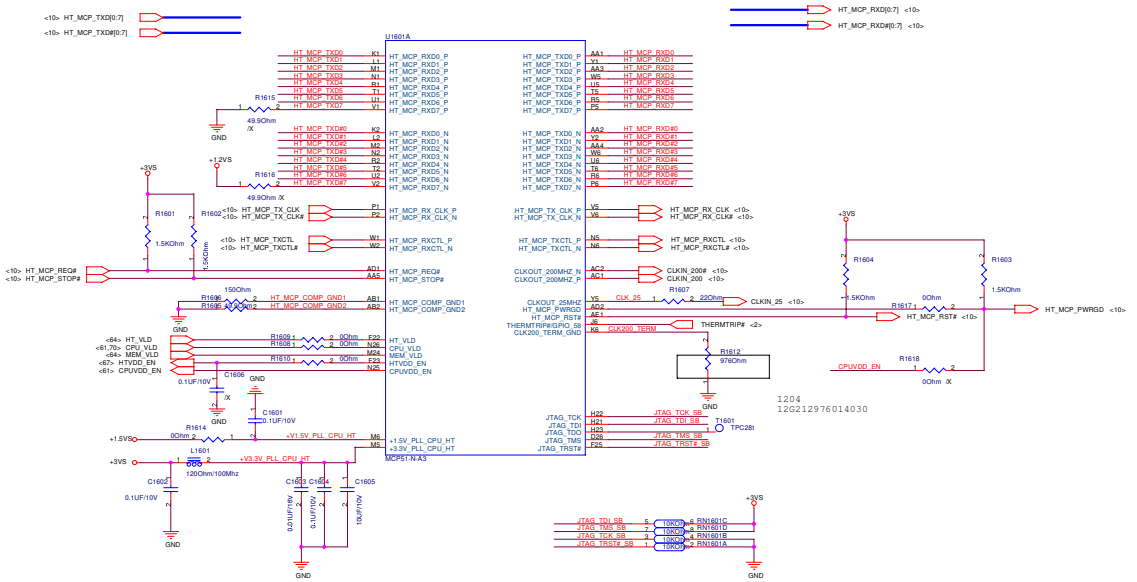
CRT OUT

1208

NEED TO DECIDE

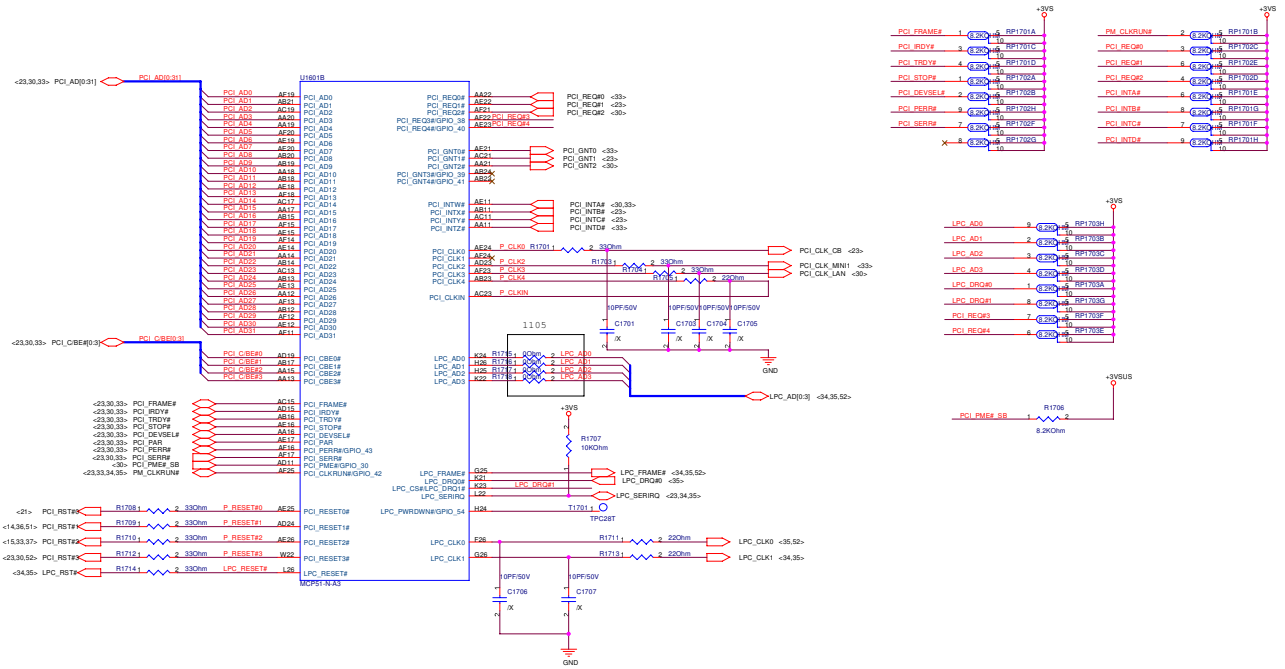


ASUSTECH
Title : CRT TV CONNECTER
Engineer: PENG_XIAO
Size: C
Project Name: A7T
Rev: 2.0
Date: 日 七月 04, 2006
Sheet 15 of 79

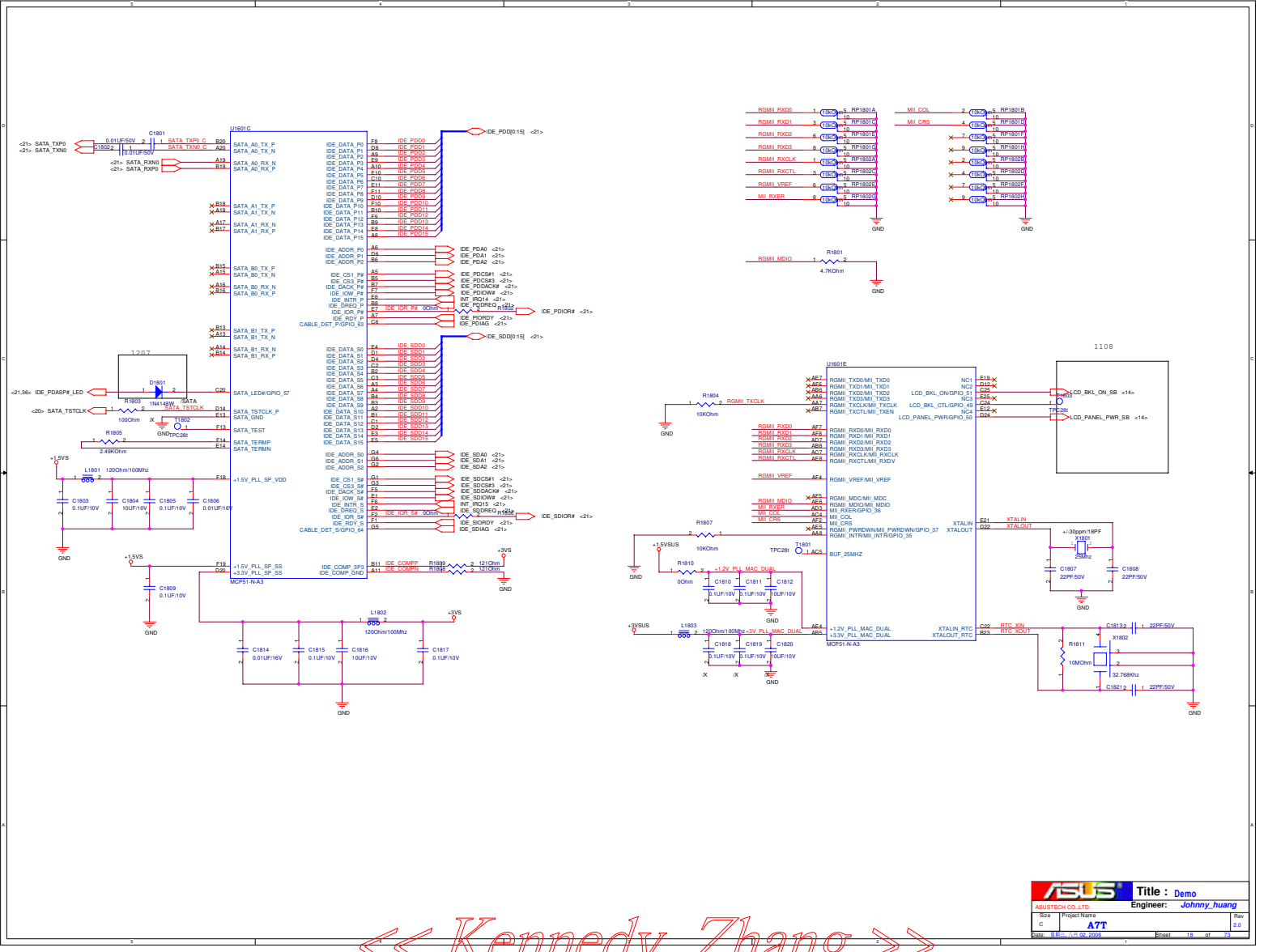


1204
12G212976014030

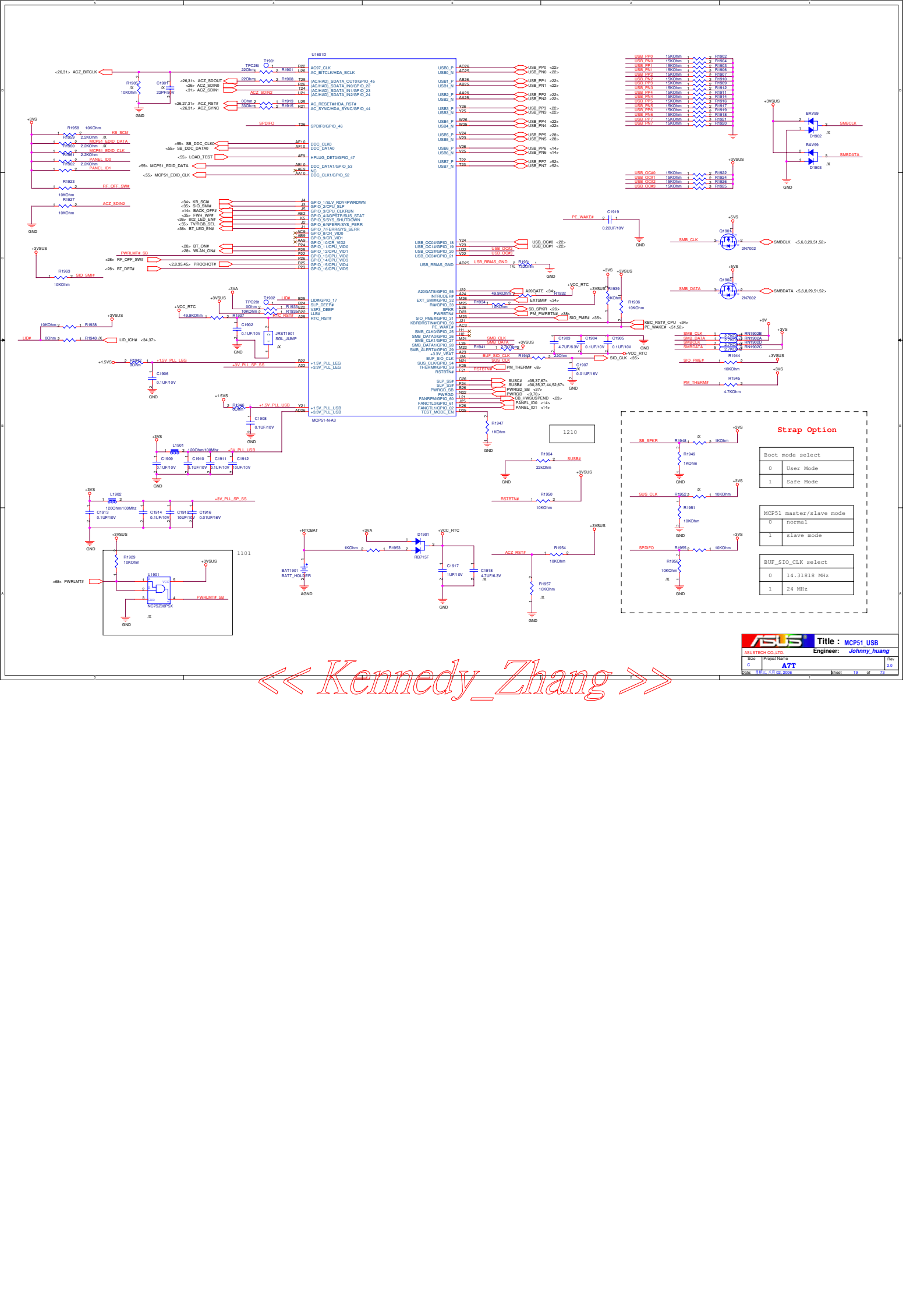
ASUSTECH CO.,LTD	Title : SB HT I/F		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 18 of 73		

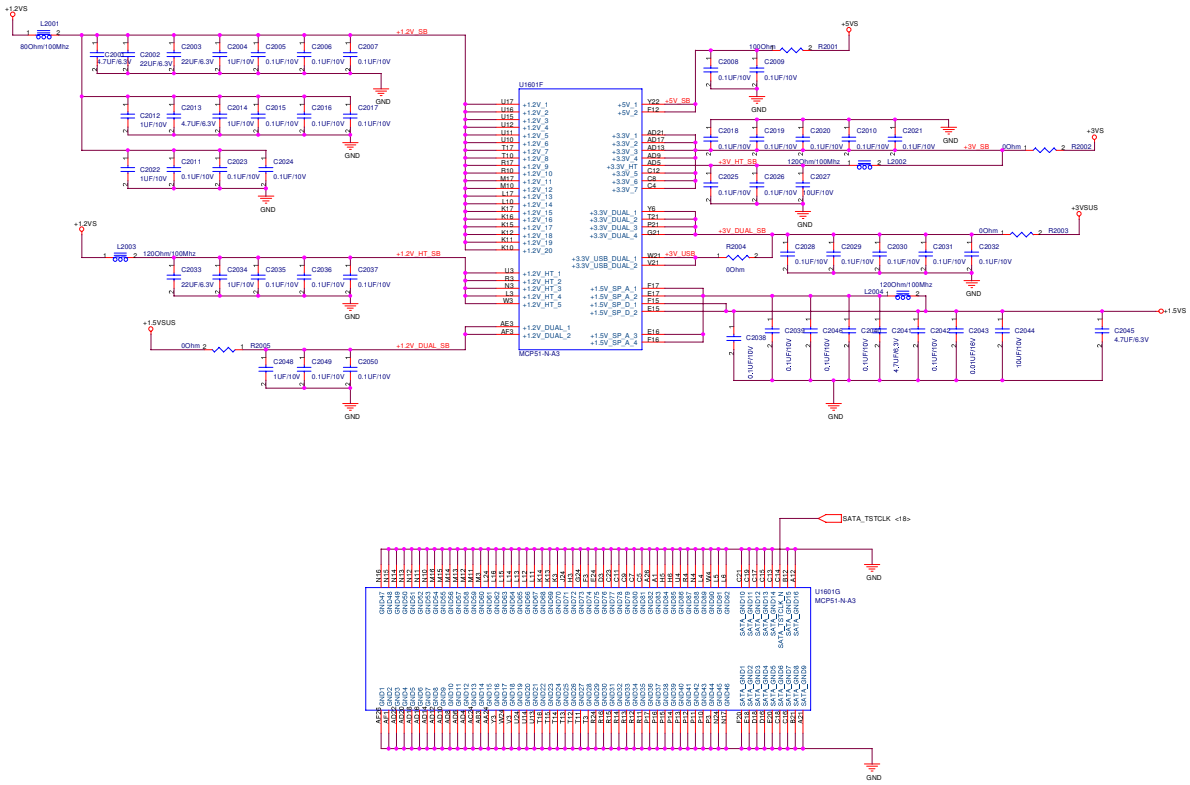


ASUSTECH CO.,LTD	Title : PCI I/F		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 17 of 73		



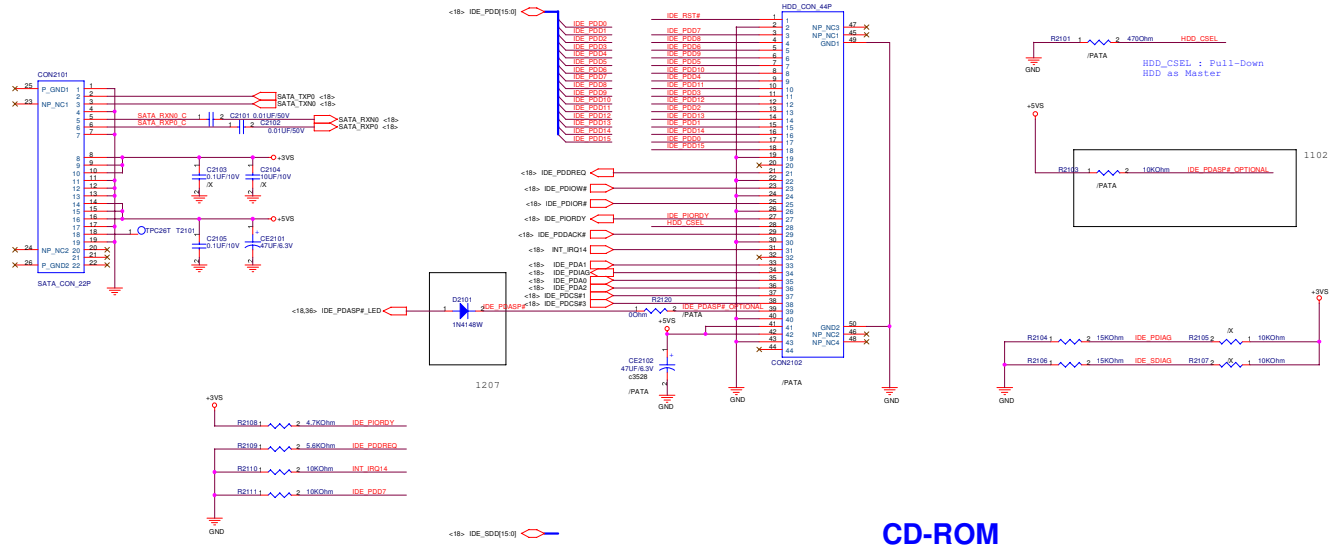
ASUSTeK COMPUTER INC.	Title : Demo		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 18 of 73		


U1601D
MCP51-N-A3
Strap Option
Boot mode select
0 User Mode
1 Safe Mode
MCP51 master/slave mode
0 normal
1 slave mode
BUF_SIO_CLK select
0 14.31818 MHz
1 24 MHz
Title : MCP51_USB
Engineer: Johnny_huang
ASUSTeK CO.,LTD
Size C
Project Name A7T
Rev 2.0
Date: 星期三, 八月 02, 2006
Sheet 19 of 73
<< Kennedy_Zhang >>

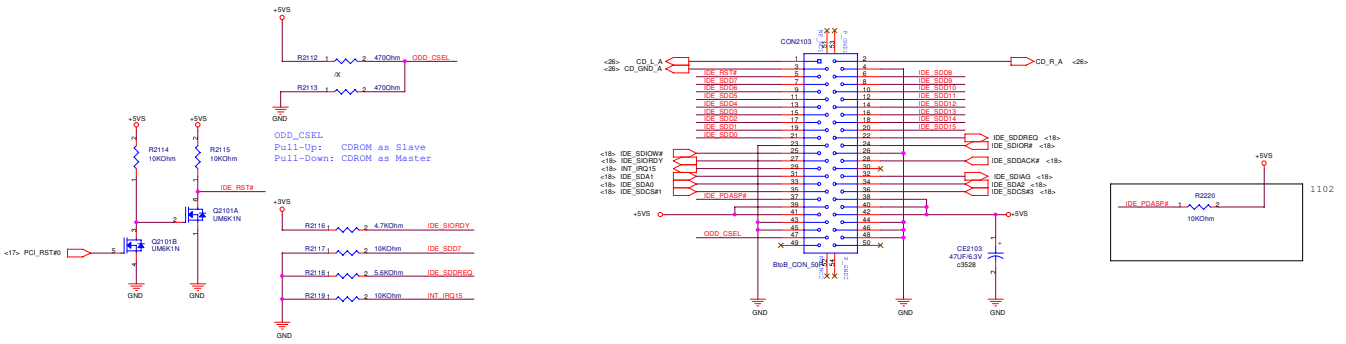


ASUSTECH CO.,LTD	Title : MCP51_PWR	
	Engineer: Johnny_huang	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 20 of 73	

HDD

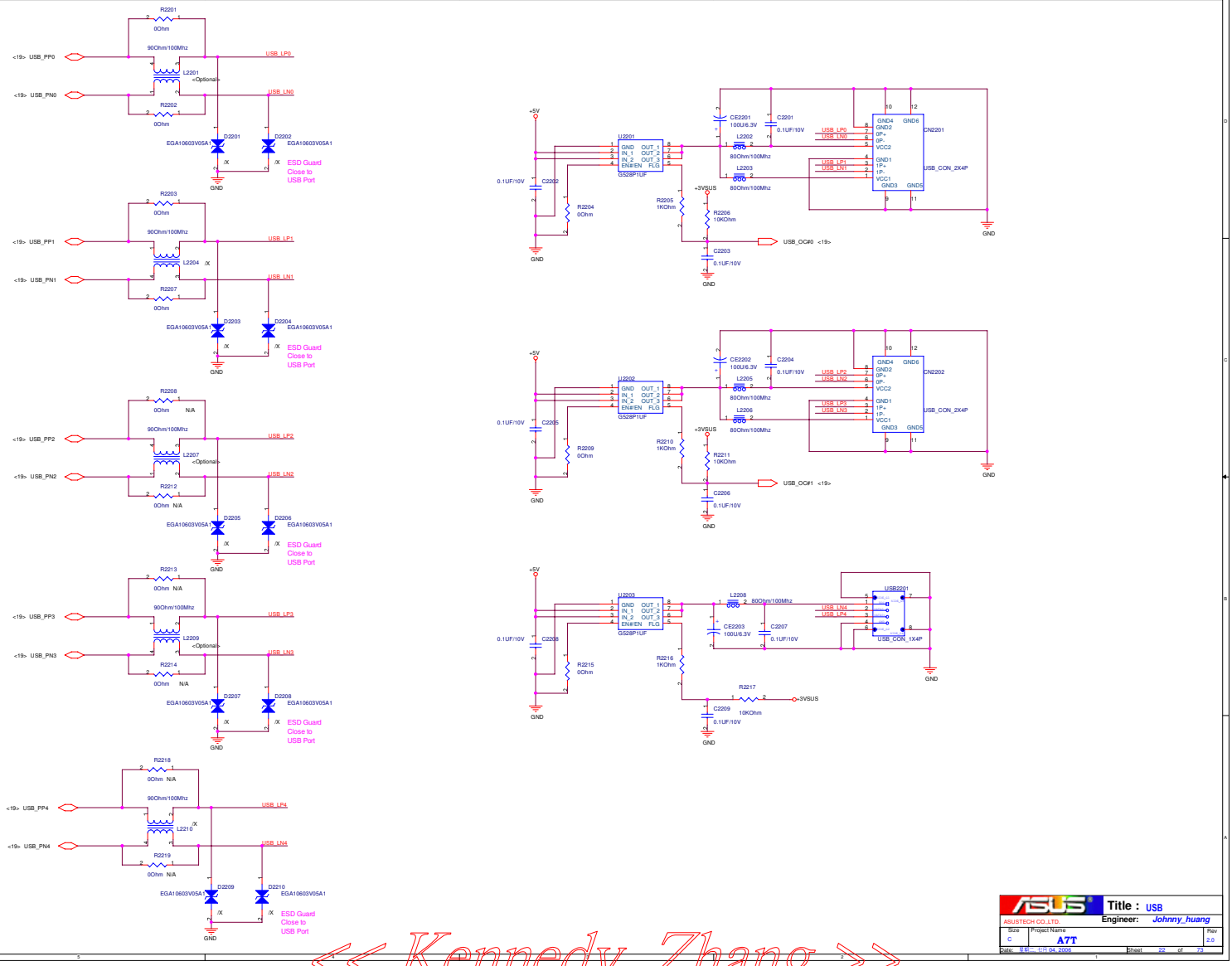


CD-ROM

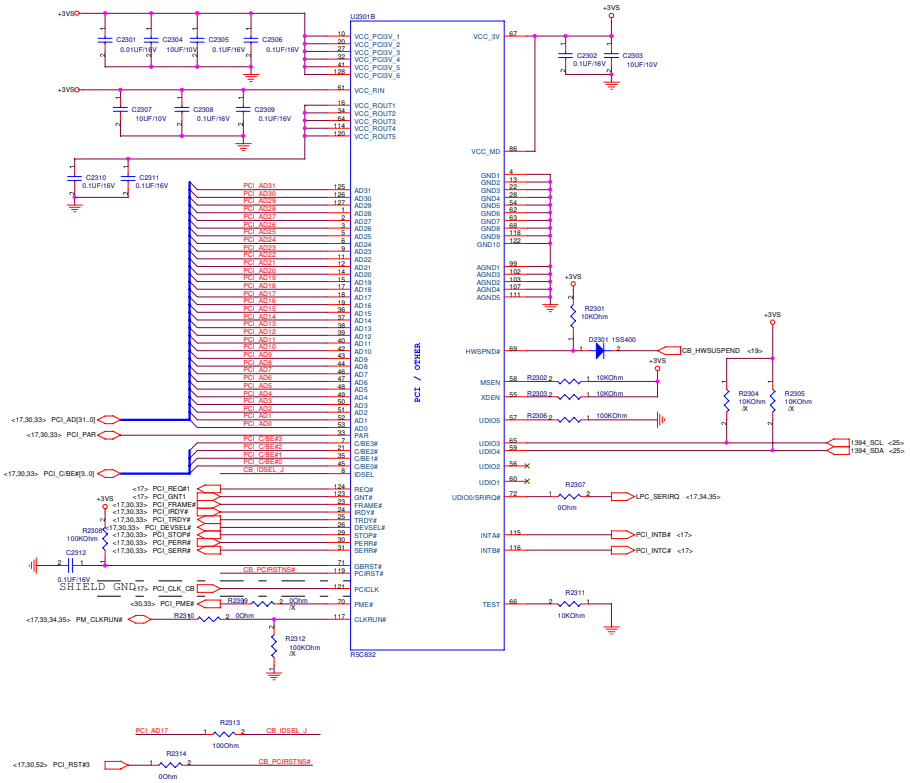


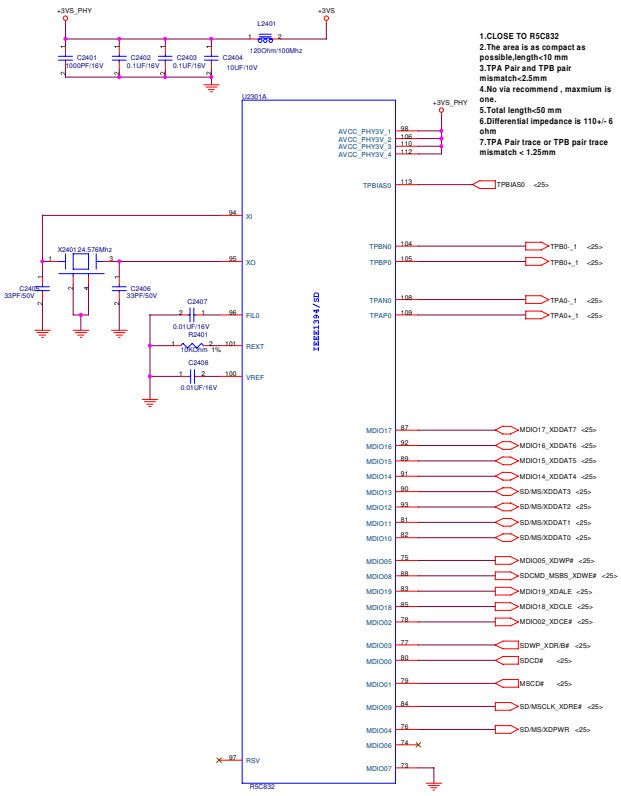
ASUSTeK COMPUTER INC.	Title : HDD&ODD		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 六月 02, 2006	Sheet 21 of 73		

<< Kennedy_Zhang >>

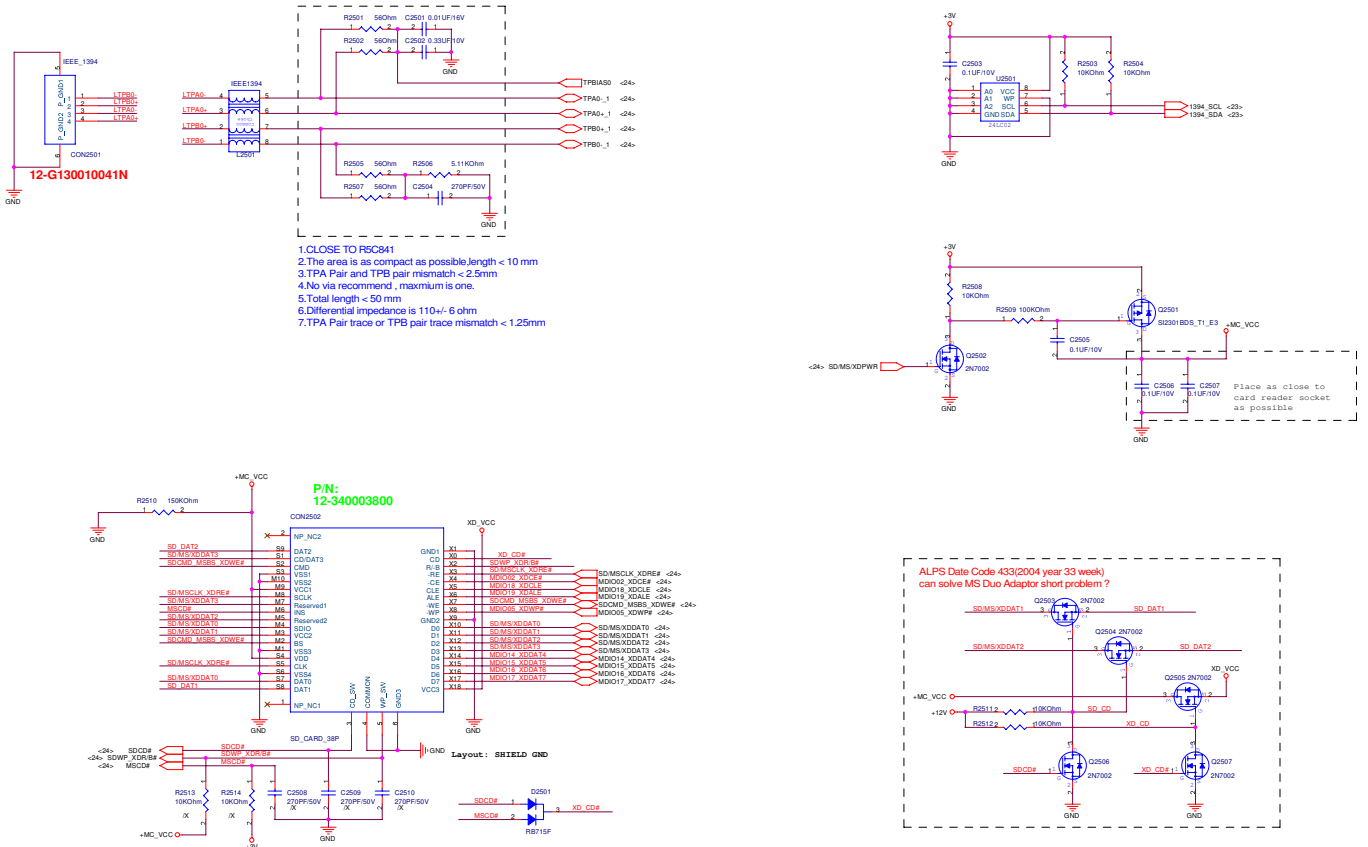


ASUSTECH COMPUTER INC.	Title : USB		
	Engineer: Johnny_huang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 十月 04, 2005	Sheet 22 of 73		





ASUSTEK	Title : R5C832_2	
	Engineer: echo_xing	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 24 of 73	



ASUSTEK

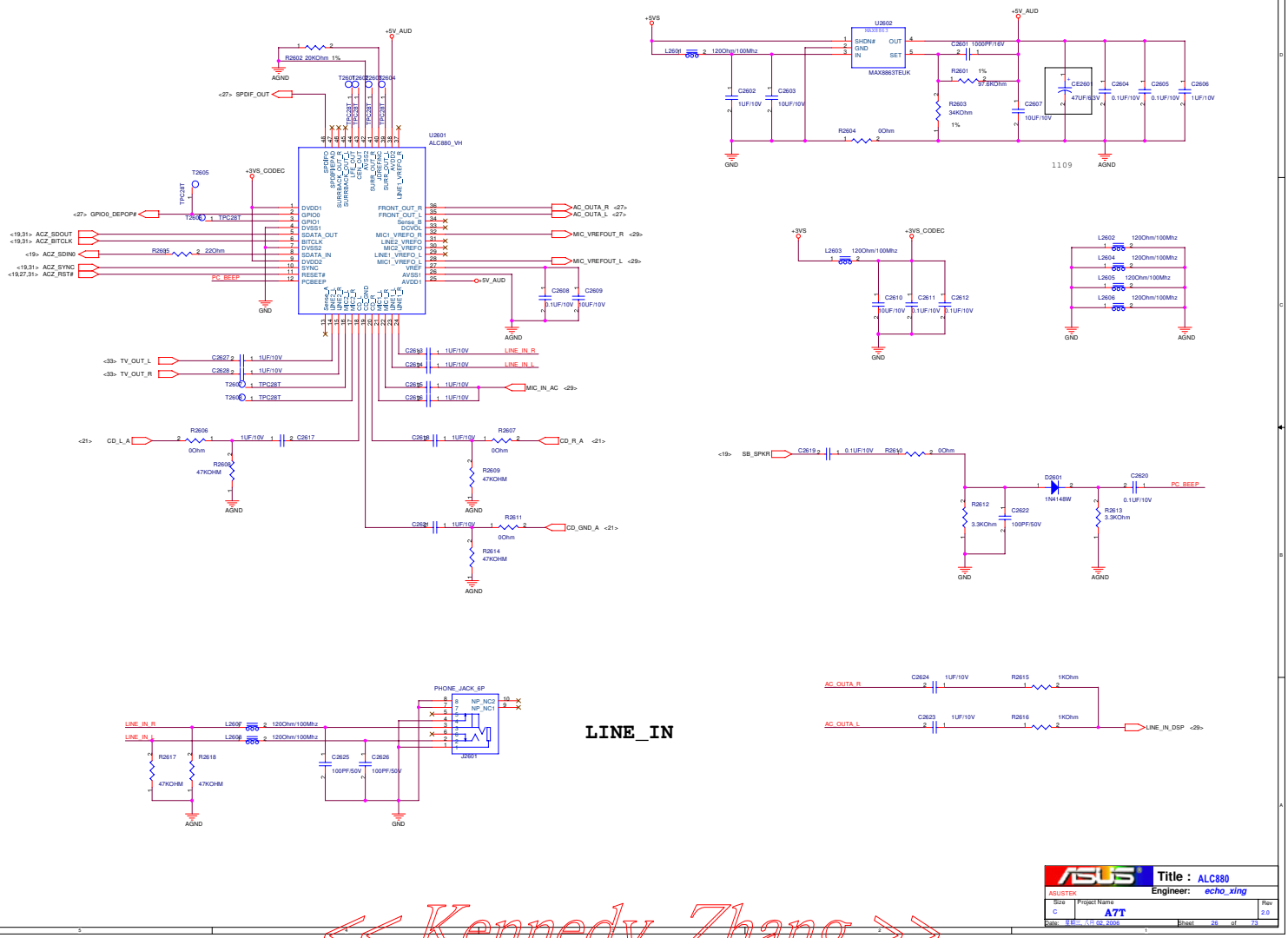
Title : 1394&IN 1 CON

Engineer: echo_xing

Size: C | Project Name: A7T | Rev: 2.0

Date: 星期二, 八月 15, 2006 | Sheet 25 of 73

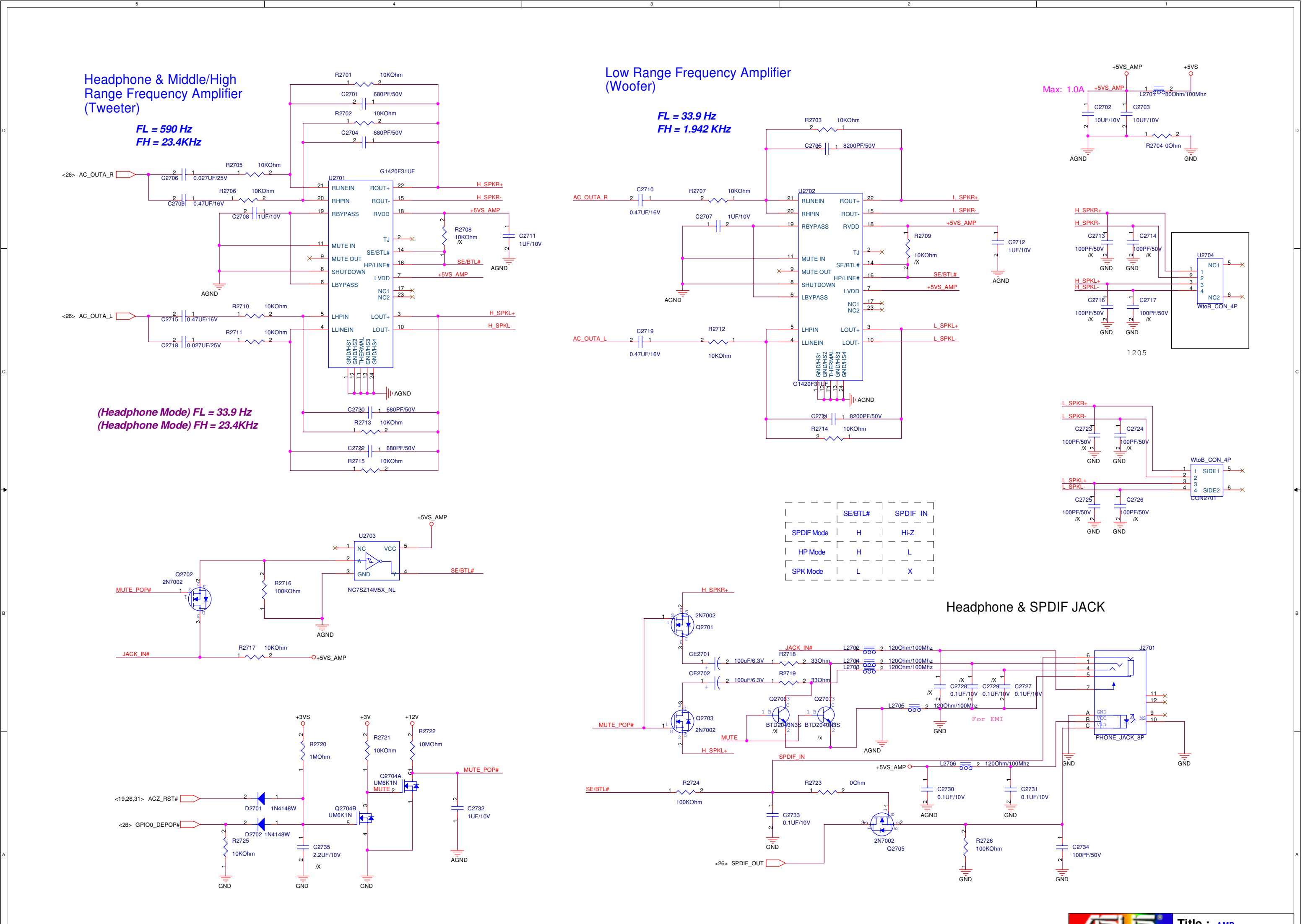
<< Kennedy_Zhang >>



LINE_IN

ASUSTEK	Title : ALC880		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 26 of 73		

<< Kennedy_Zhang >>



	SE/BTL#	SPDIF_IN
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X

ASUSTEK

Title : AMP

Engineer: echo_xing

Size: C

Project Name: A7T

Rev: 2.0

Date: 星期三, 八月 02, 2006

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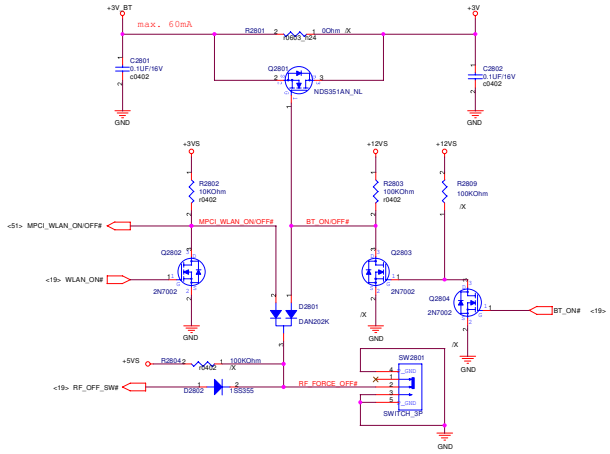
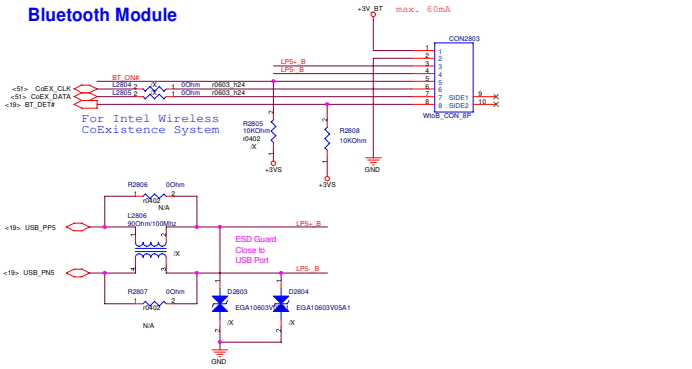
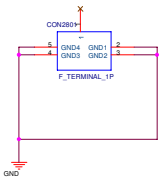
WLAN/BT ON/OFF Control



Bluetooth Module



ATV_DTV_FM Antenna



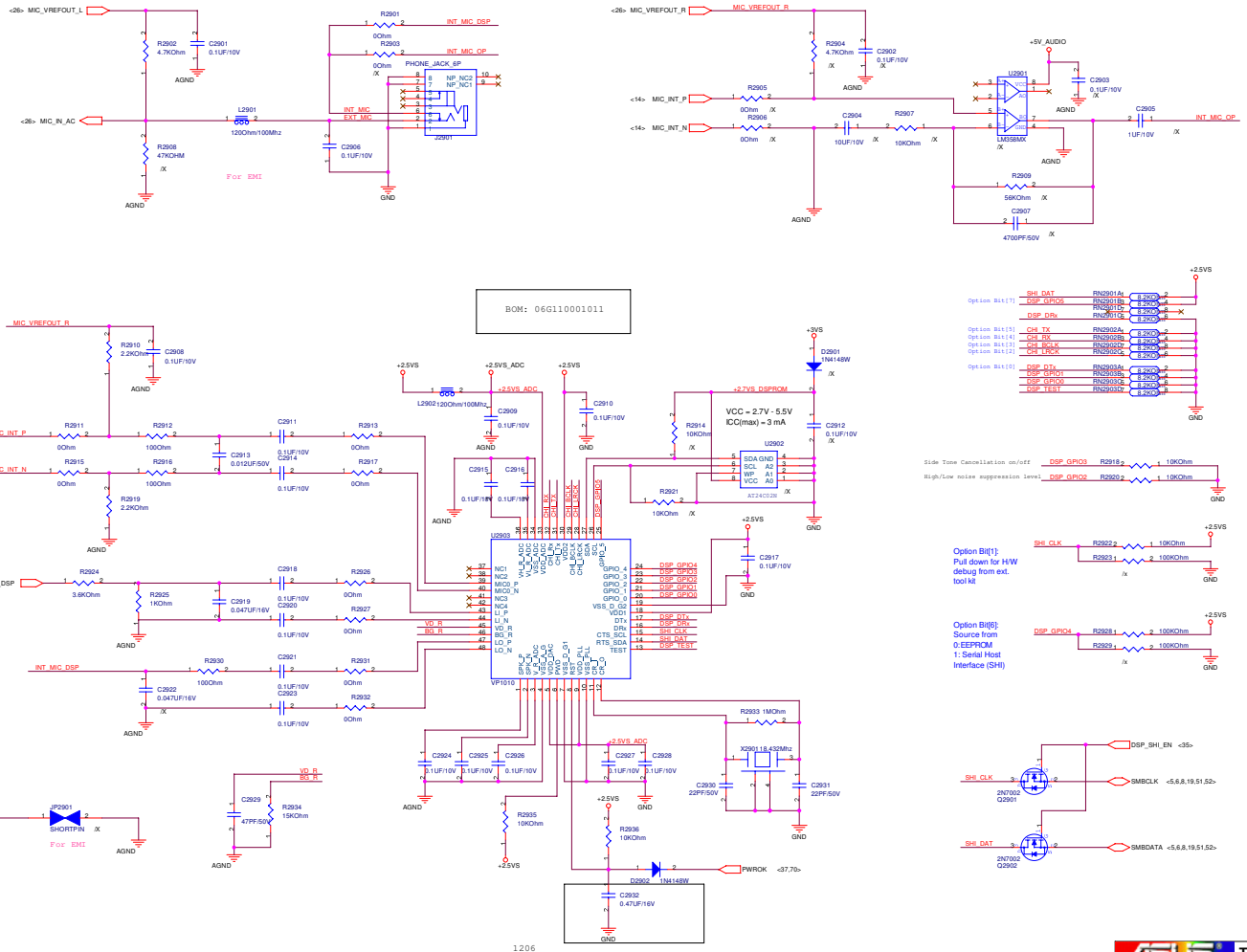
14G152075000

ASUSTeK	Title : BT/RF		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 28 of 73		

<< Kennedy_Zhang >>

FL = TBD
FH = TBD

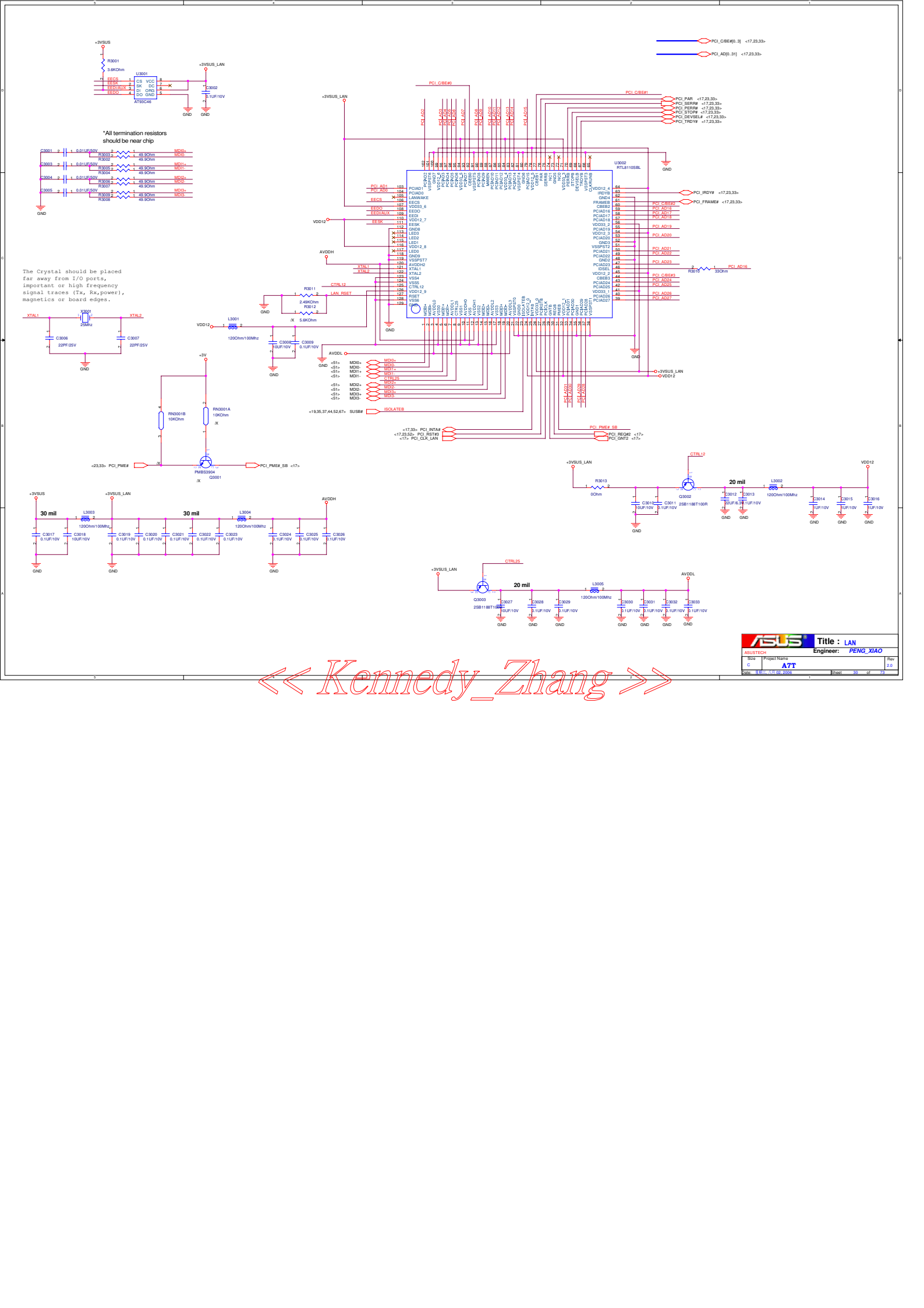
Internal MIC Pre-Amplifier

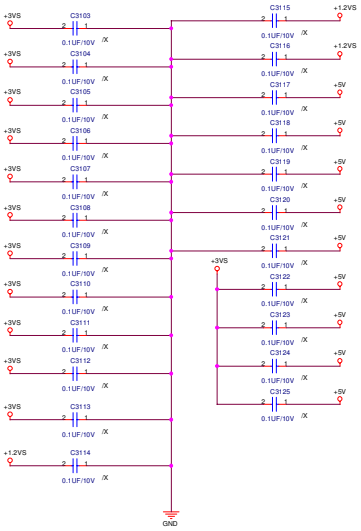


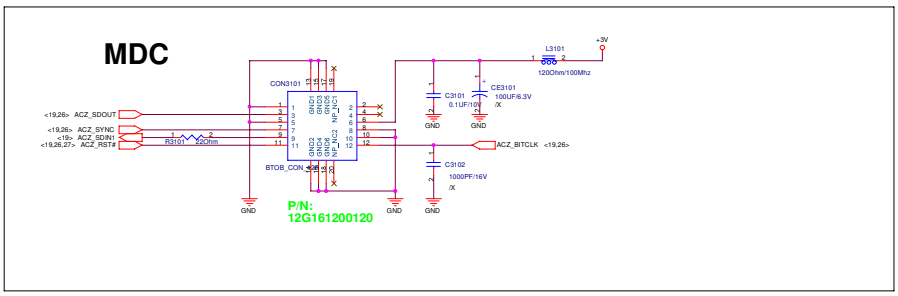
1206

ASUSTEK	Title : VOICE DSP		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 29 of 73		

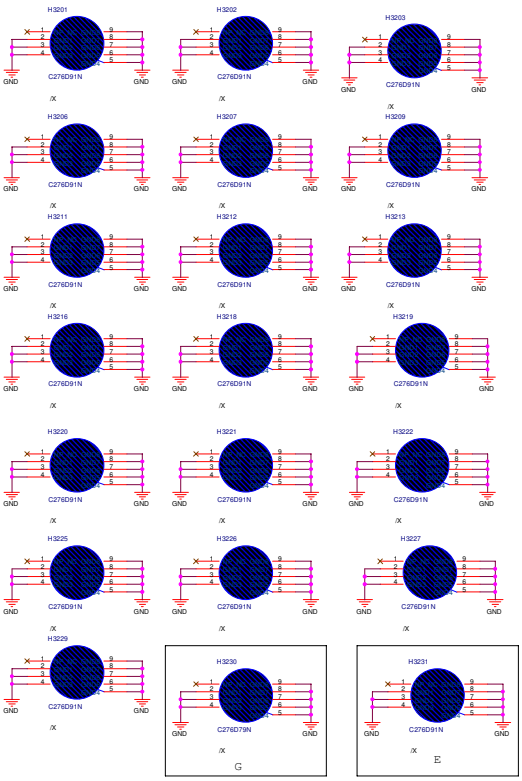
<< Kennedy_Zhang >>

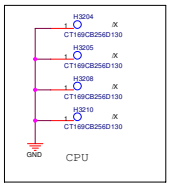

*All termination resistors should be near chip
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges.
U3002 RTL8110SBL
U3001 AT93C46
Q3001 PMBS3904
Q3002 2SB1188T100R
Q3003 2SB1188T100R
Title : LAN
Engineer: PENG_XIAO
ASUSTeK
Size C
Project Name A7T
Rev 2.0
Date: 星期三, 八月 02, 2006
Sheet 30 of 73
<< Kennedy_Zhang >>

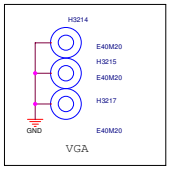


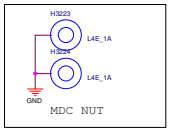


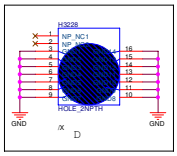
ASUSTeK	Title : MDC	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 31 of 73	











ASUSTEK

Title : Screw Hole

Engineer: echo_xing

Size	Project Name	Rev
C	A7T	2.0

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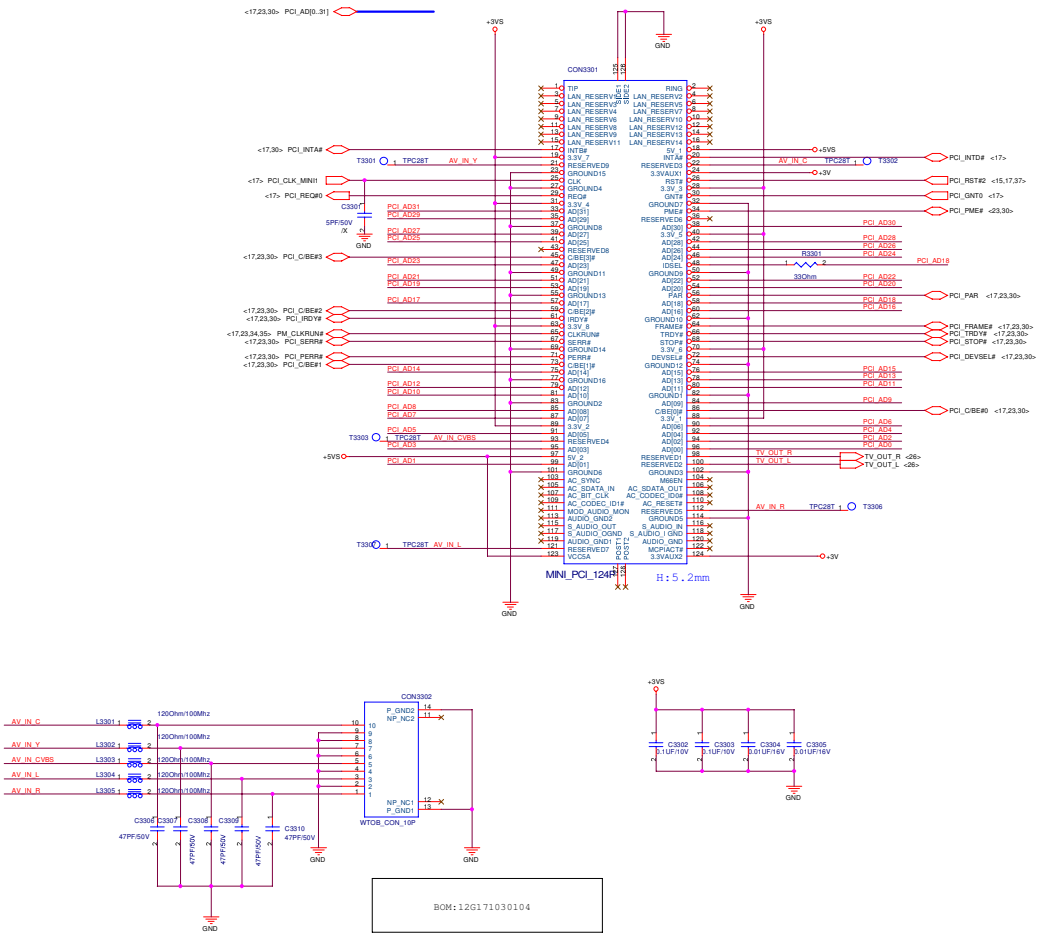
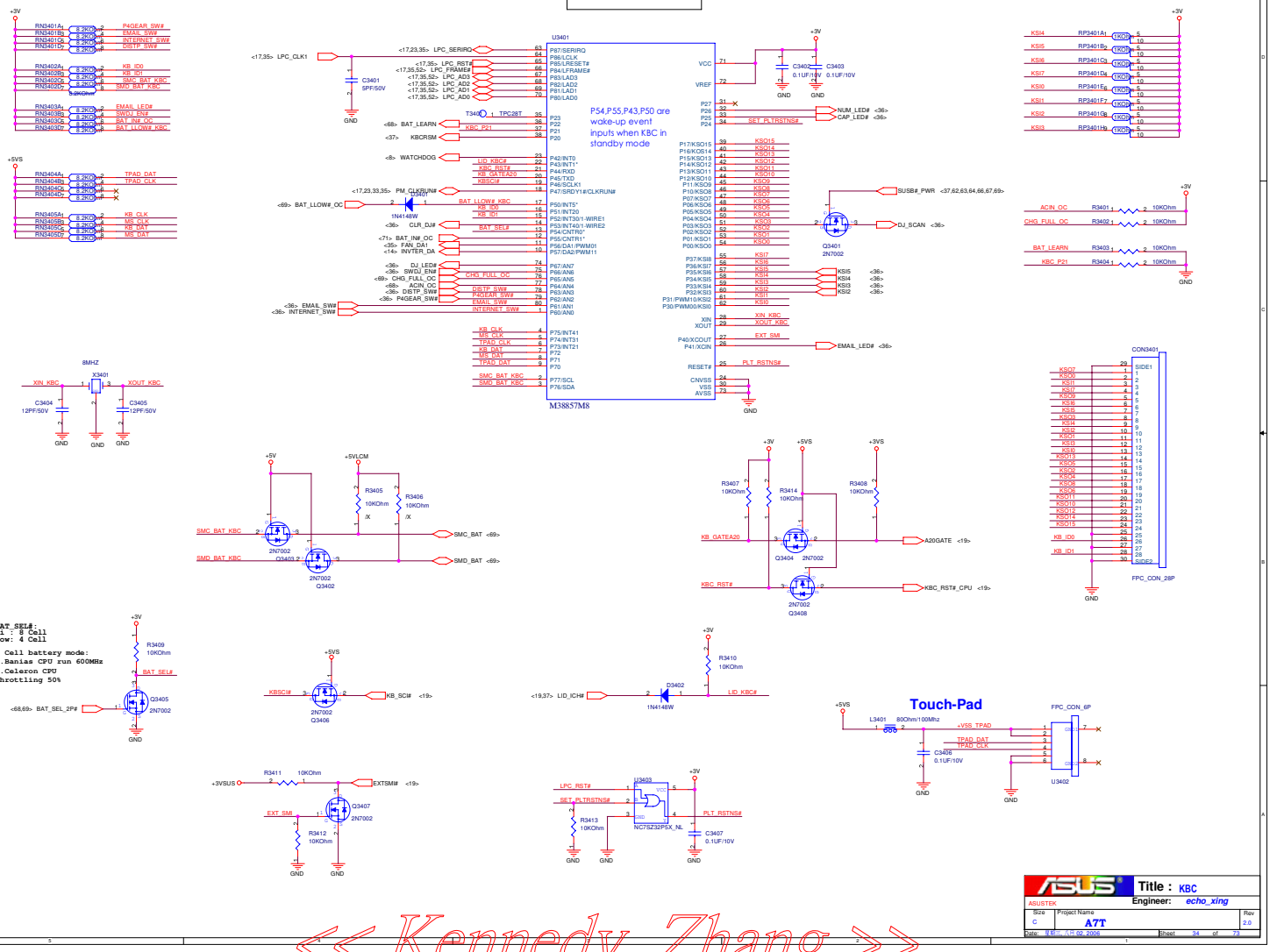
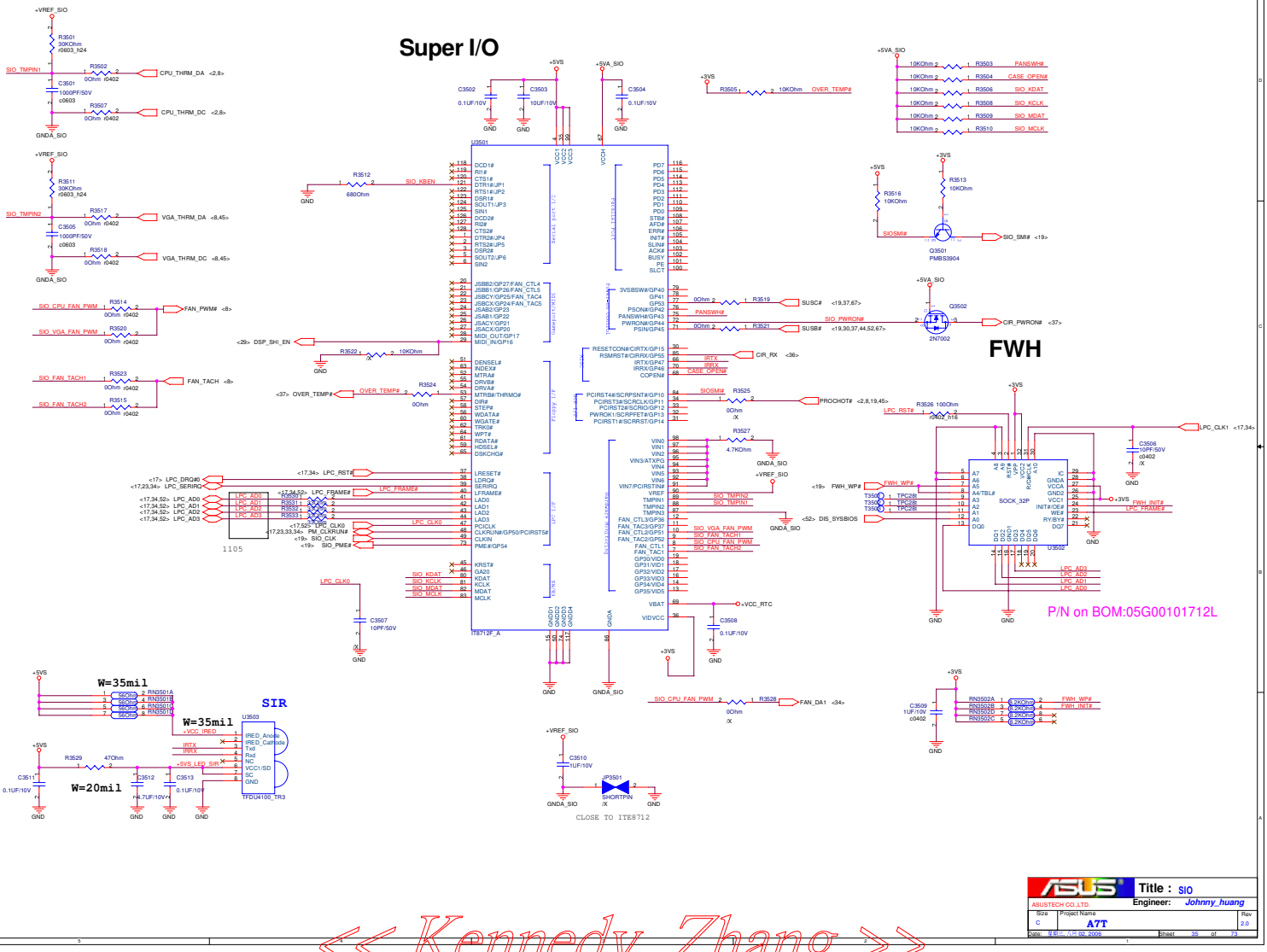
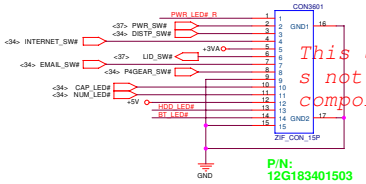


TYPE	JP	UK	US
KID0	L	L	H
KID1	L	H	H





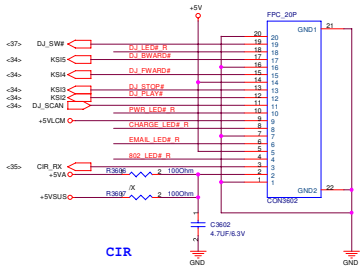
Launch Board Conn.



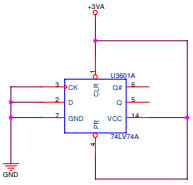
This JACK is not GREEN component

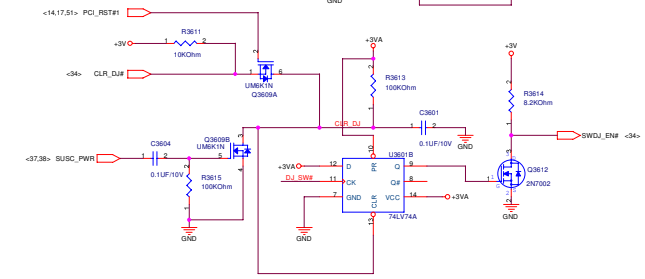
P/N:
12G183401503

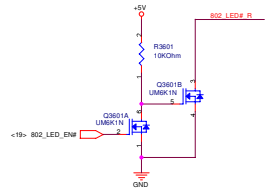
DJ Board Conn.

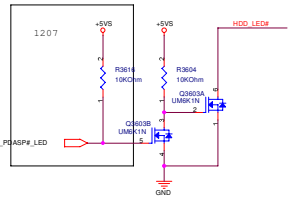


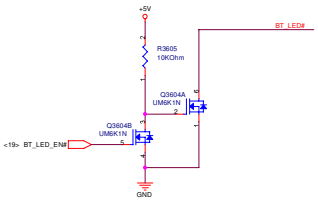
CIR

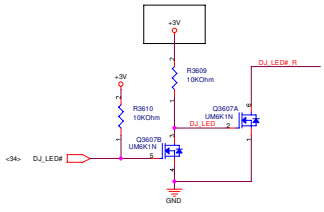


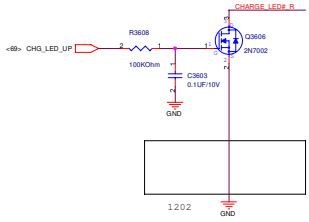


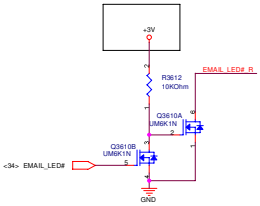


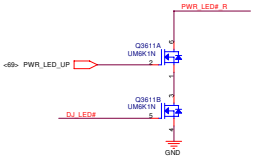












ASUSTEK	Title : FUNCTION KEY		
	Engineer: echo_xing		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 36 of 73		

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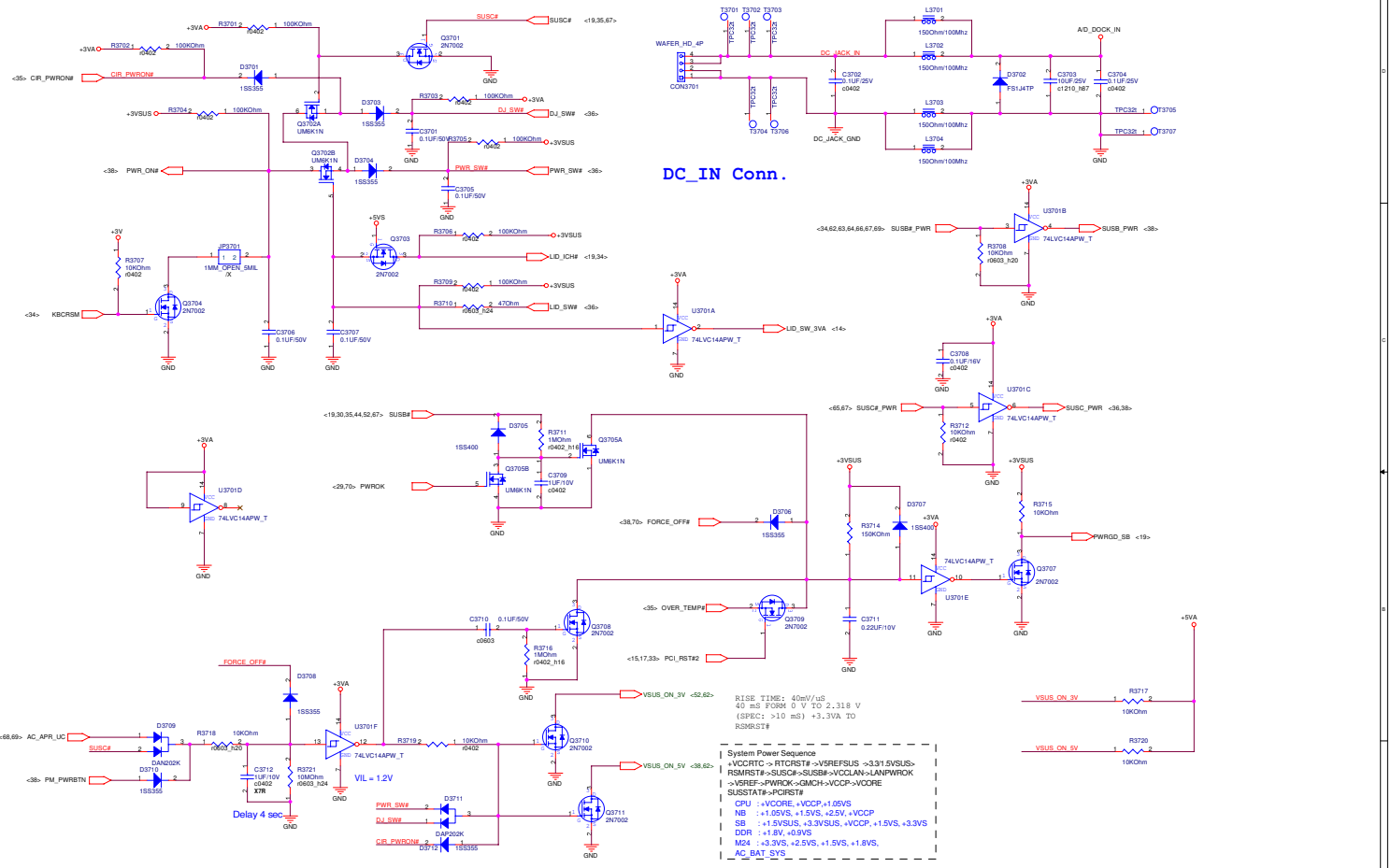
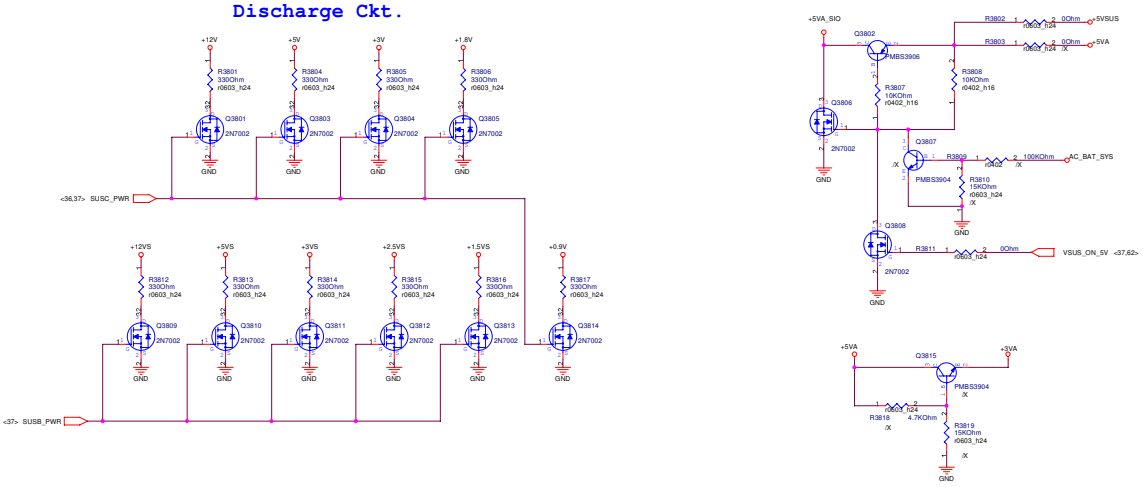


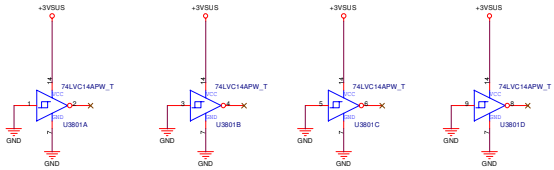
ASUSTeK	Title : POWER ON SEQ		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 37 of 73		

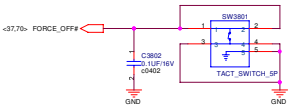
<< Kennedy_Zhang >>

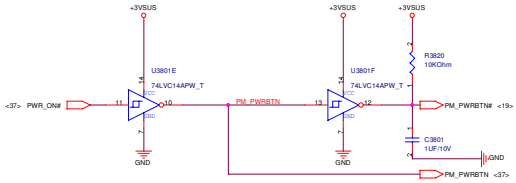
Discharge Ckt.



RESET SW.







ASUSTeK	Title : PWR ON SEQ		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 38 of 73		

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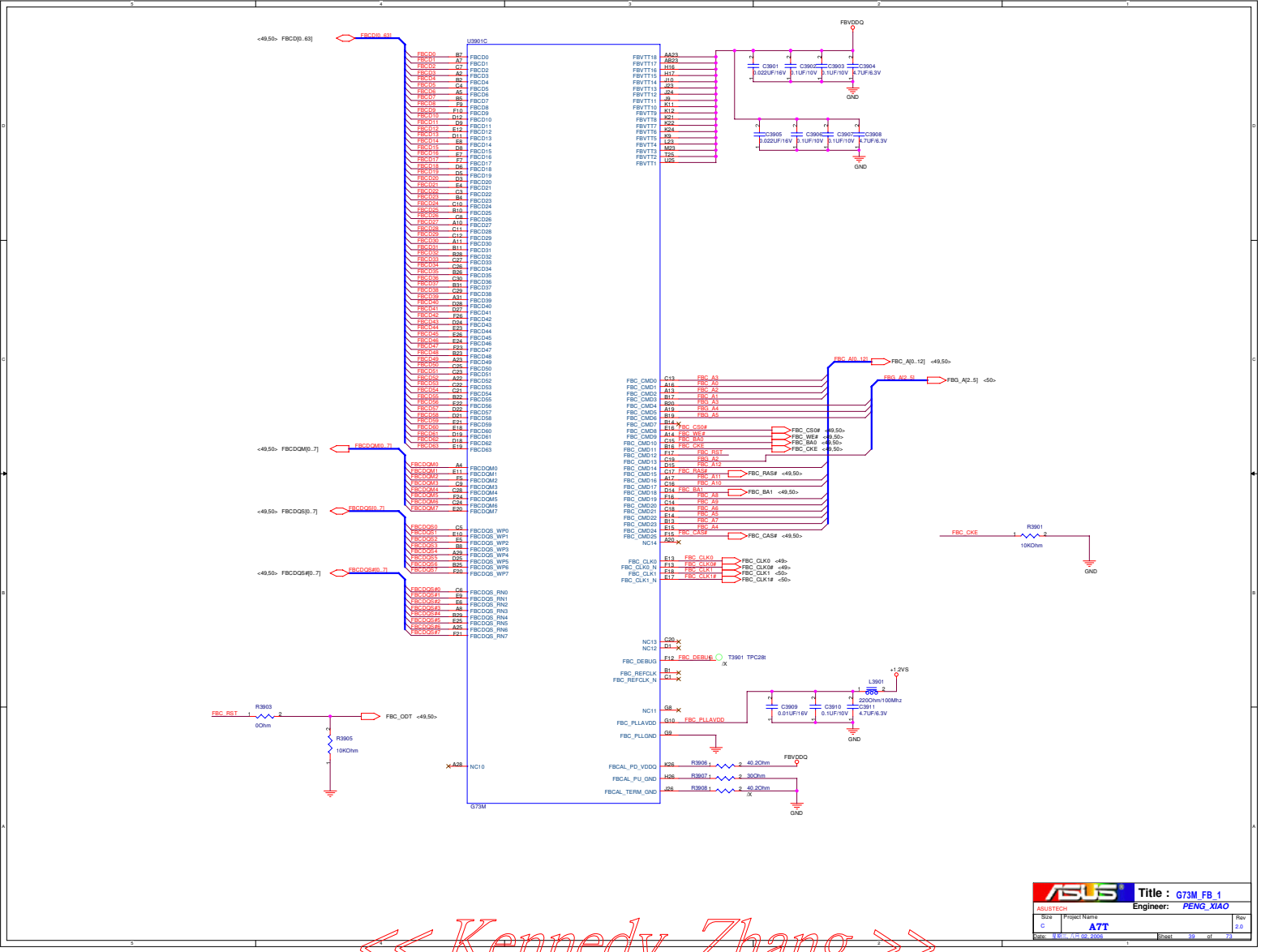
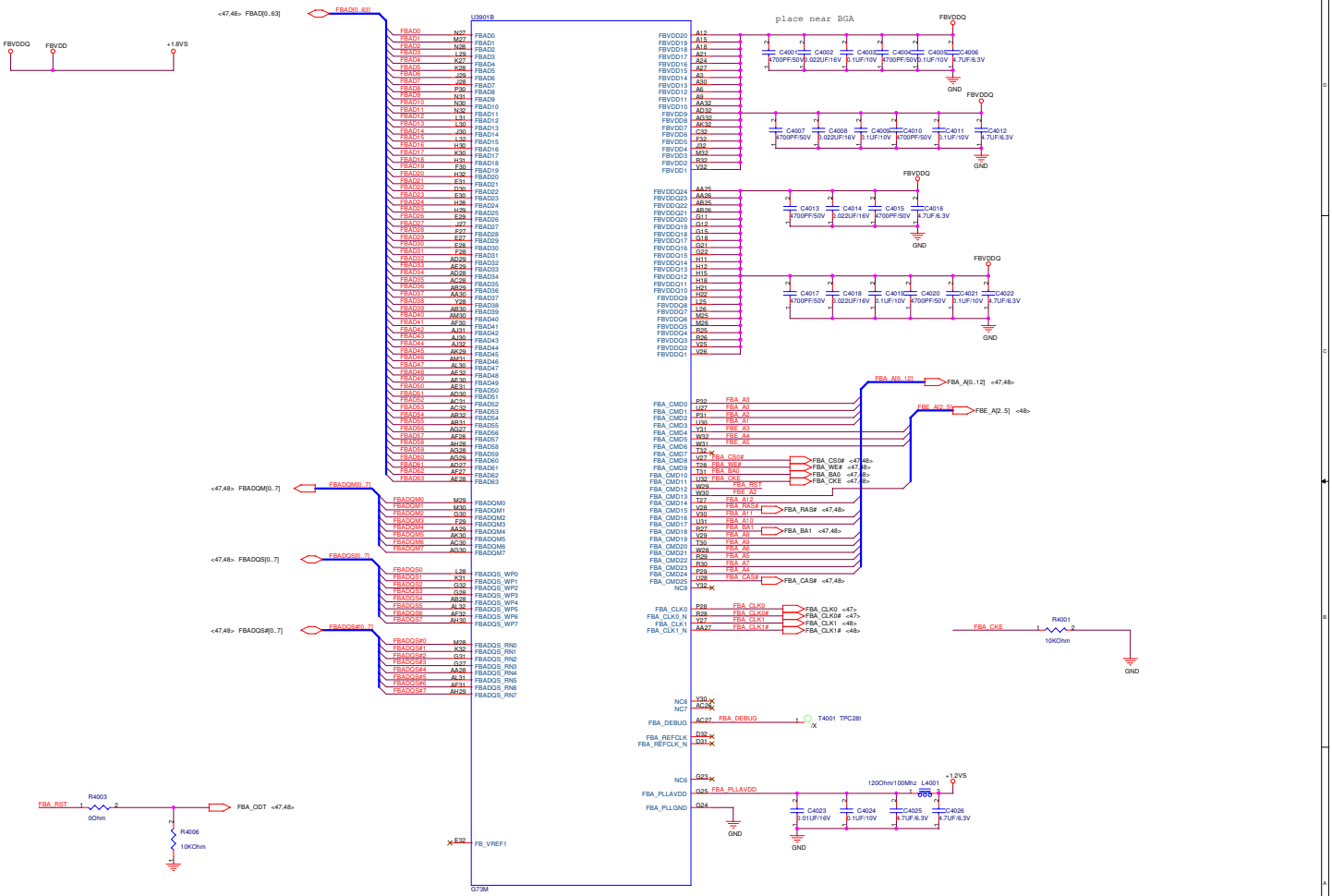
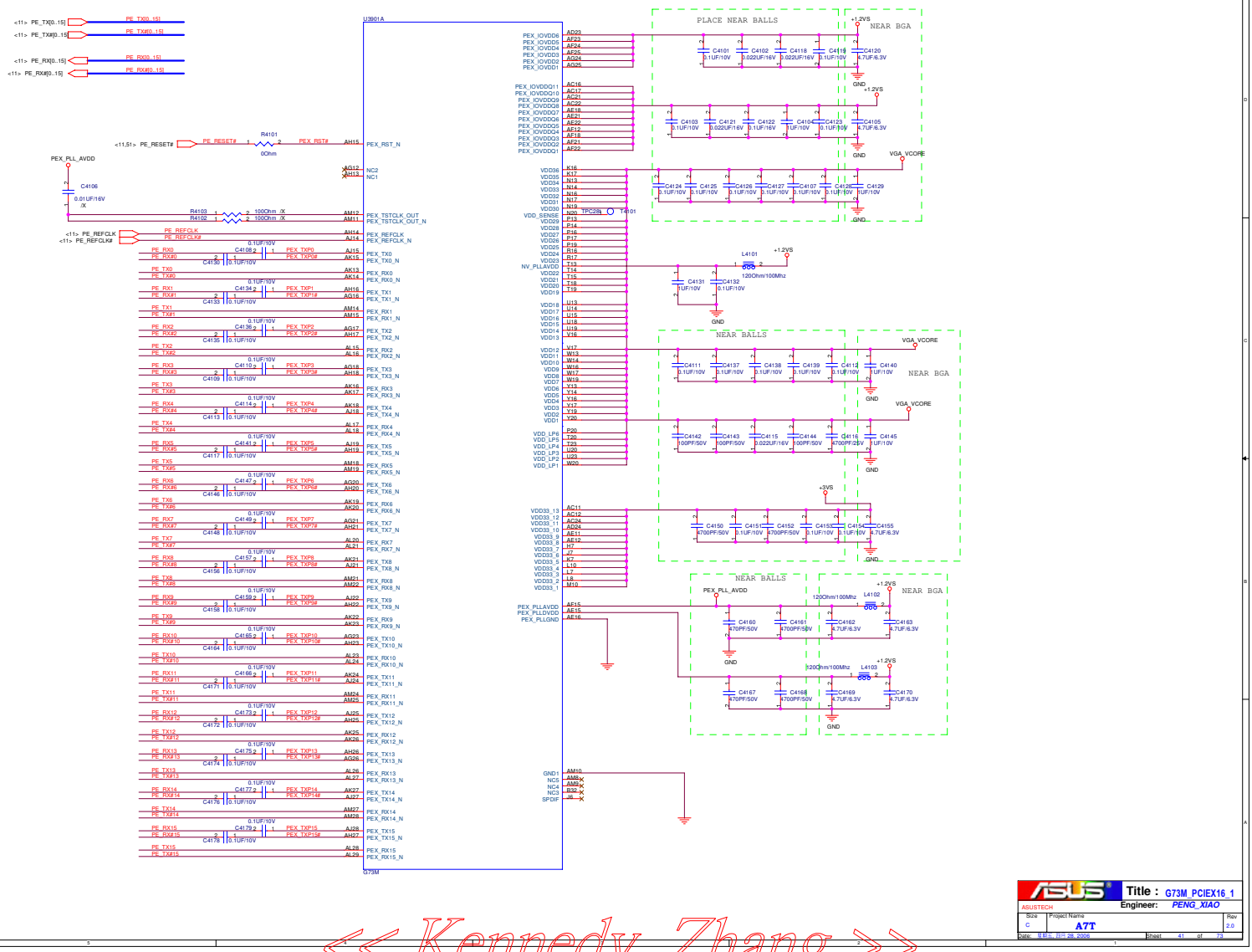


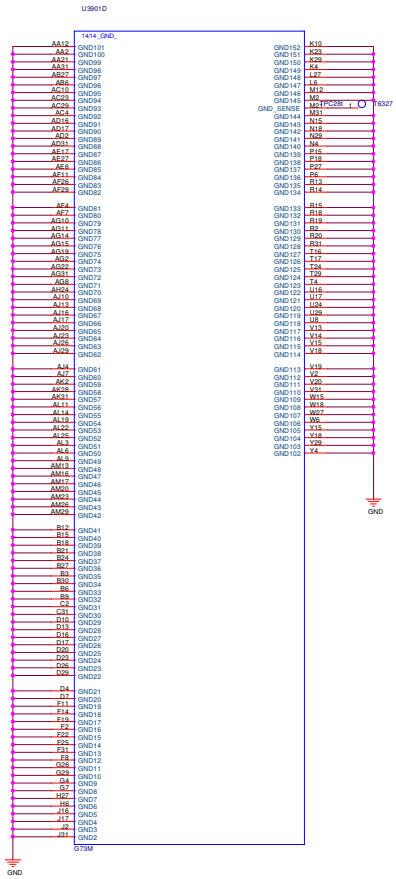


ASUSTeK	Title : G73M_FB_2		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 40 of 73		

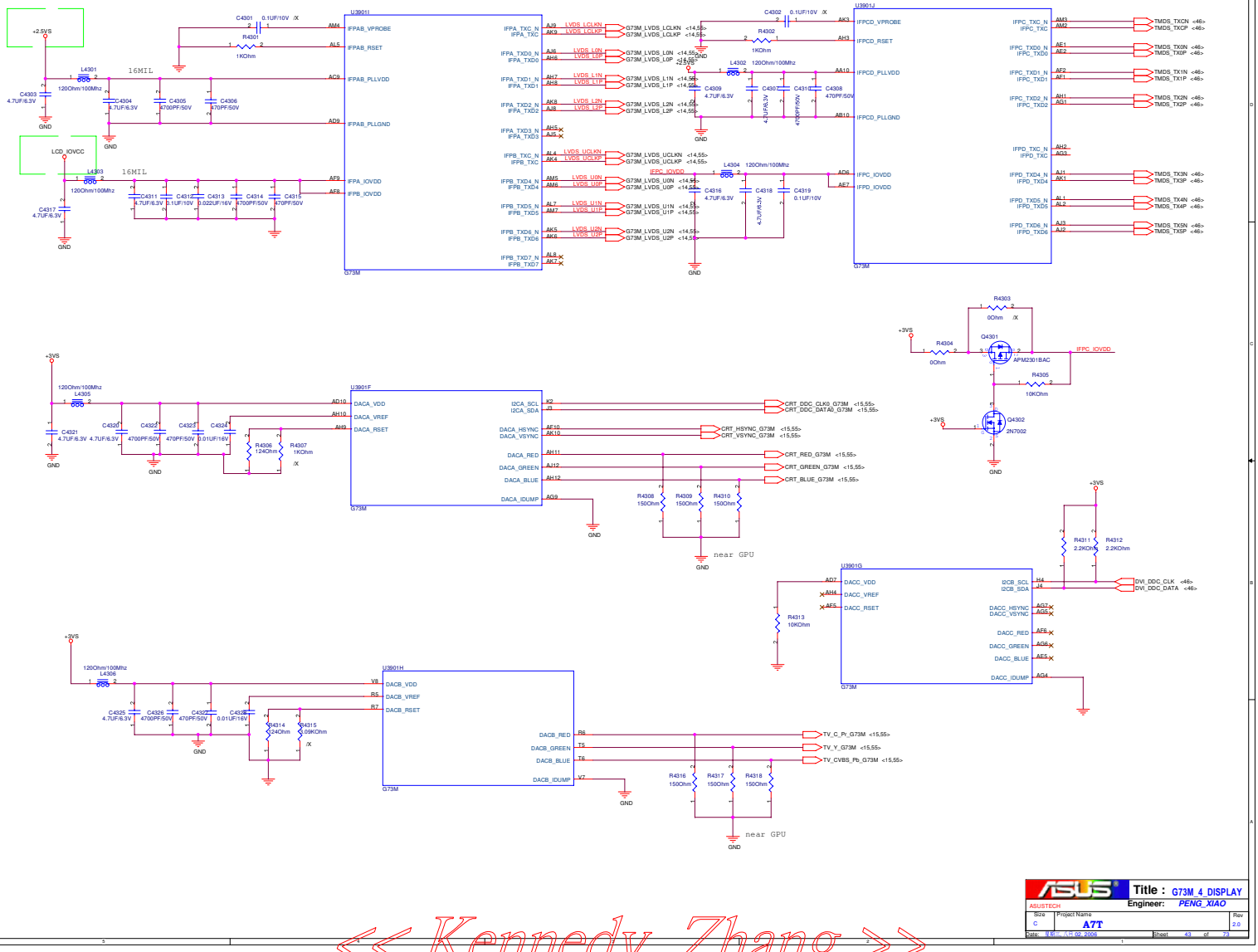
<< Kennedy_Zhang >>



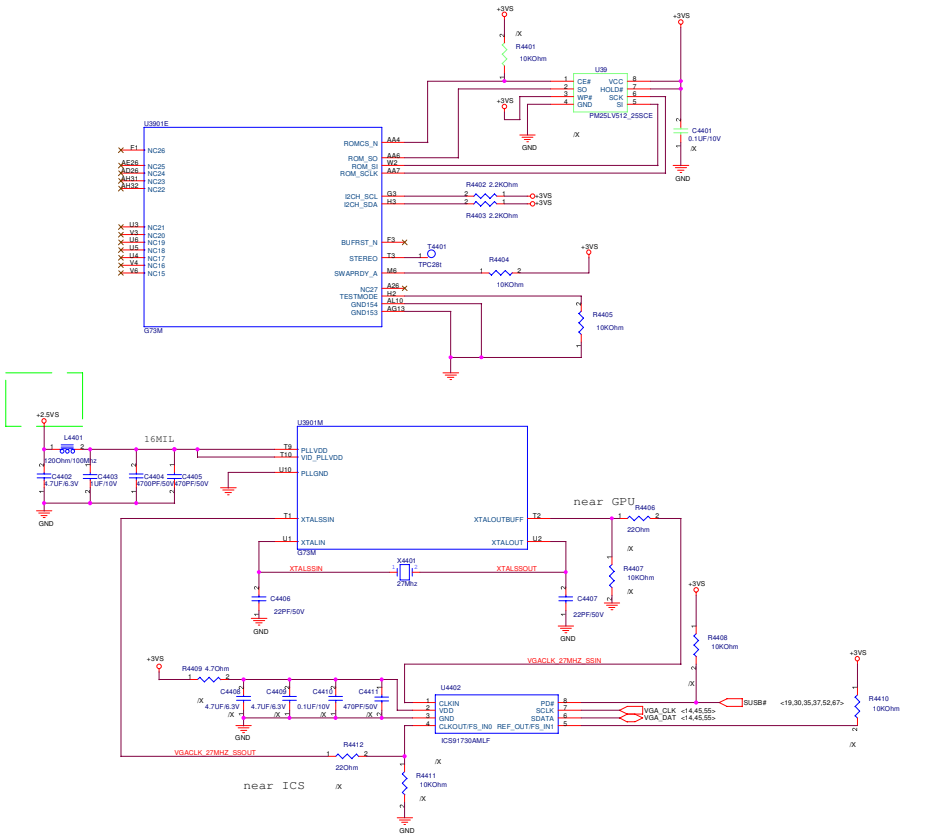
Title : G73M_PCIEX16_1			
ASUSTECH	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 41 of 73		



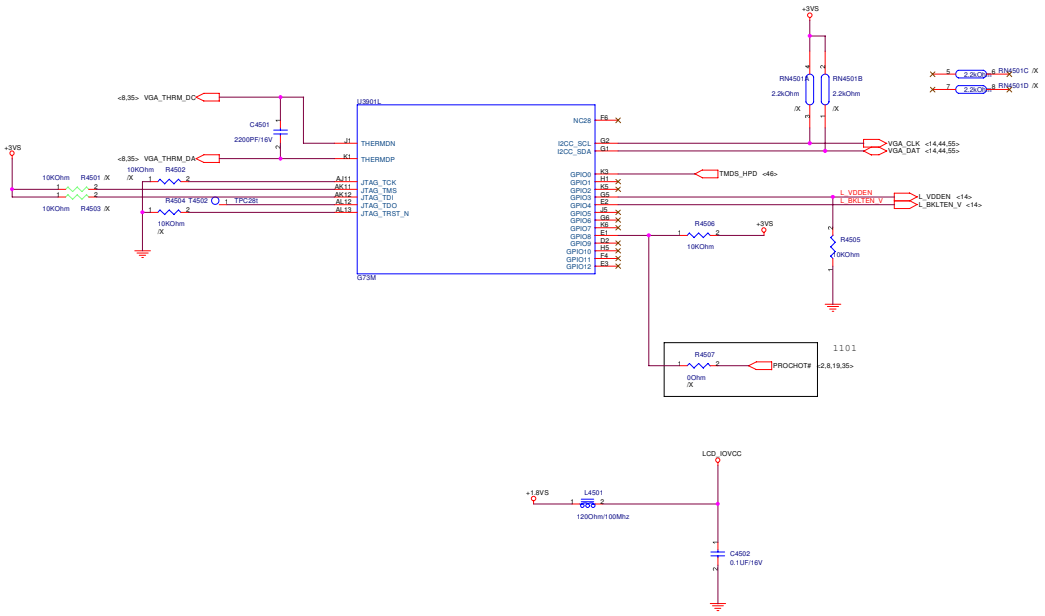
ASUSTeK	Title : G73M_PCIEX16_2	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 42 of 73	



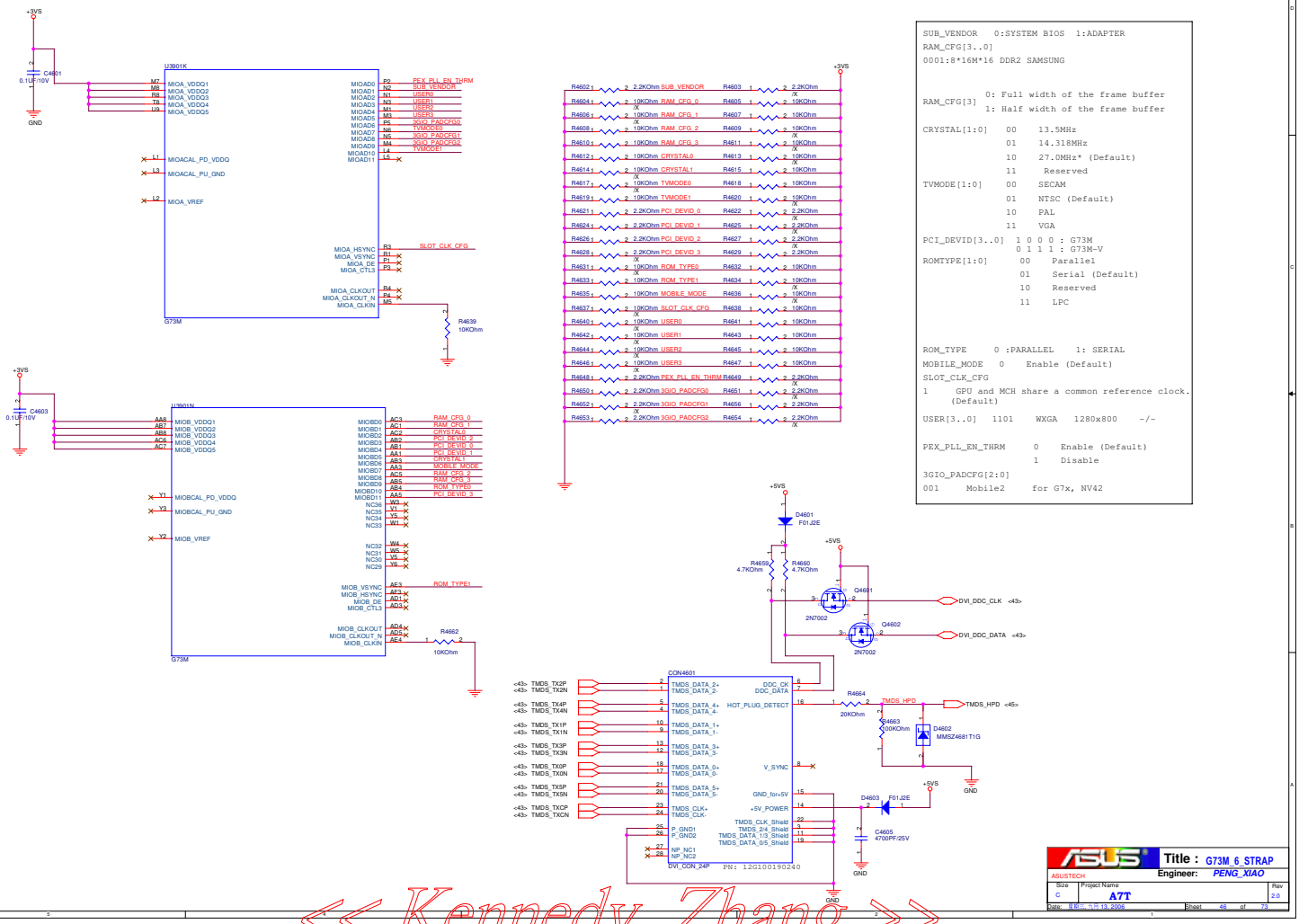
ASUSTeK	Title : G73M_4_DISPLAY	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 43 of 73	

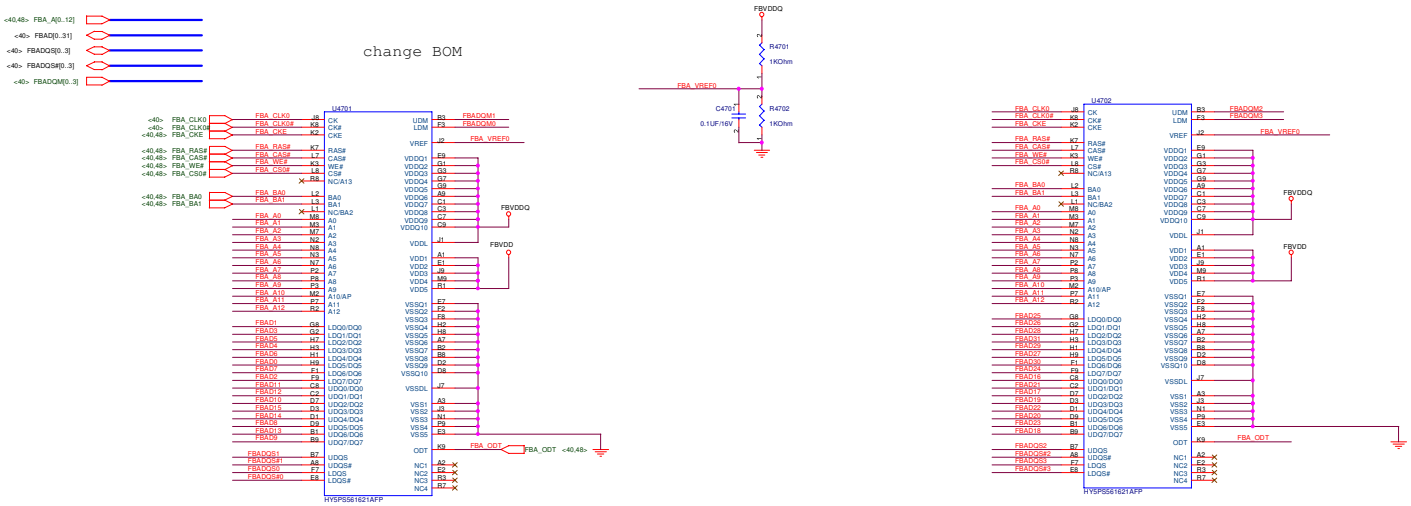


Title : G73M-BIOS&CRY
ASUSTECH
Engineer: PENG_XIAO
Size C | Project Name A7T | Rev 2.0
Date: 星期二, 八月 02, 2006 | Sheet 44 of 73

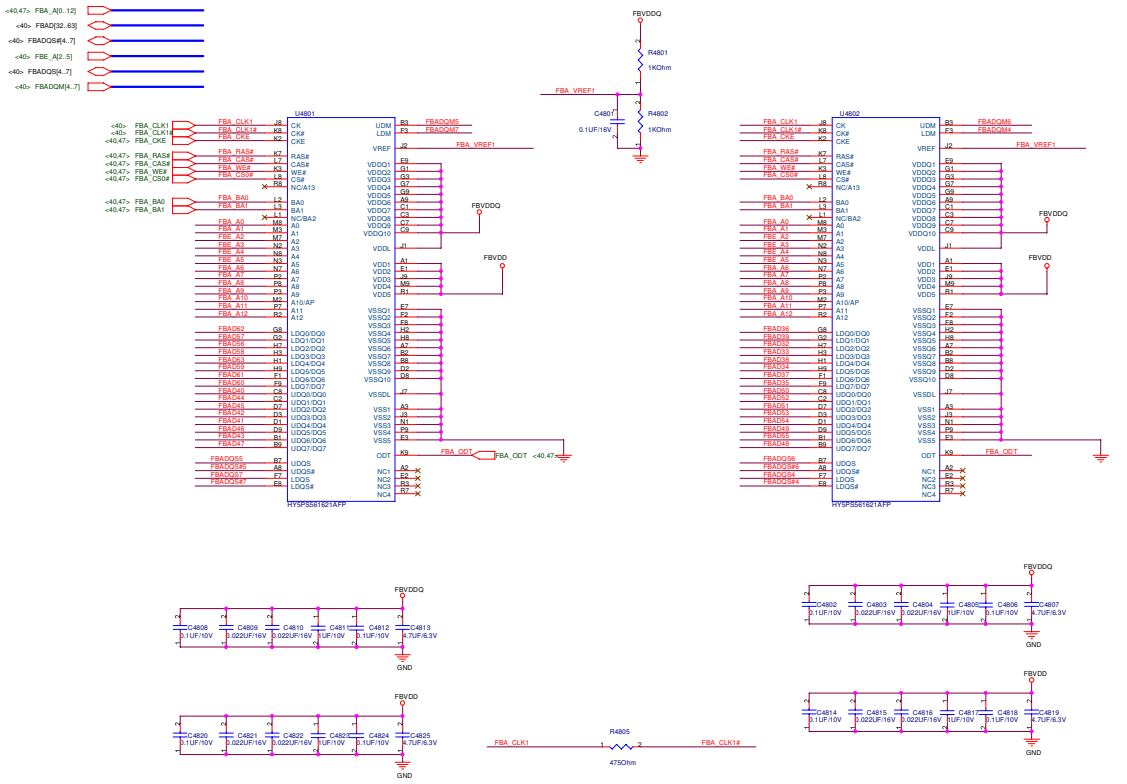


ASUSTeK	Title : G73M_5_GPIO		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 45 of 73		



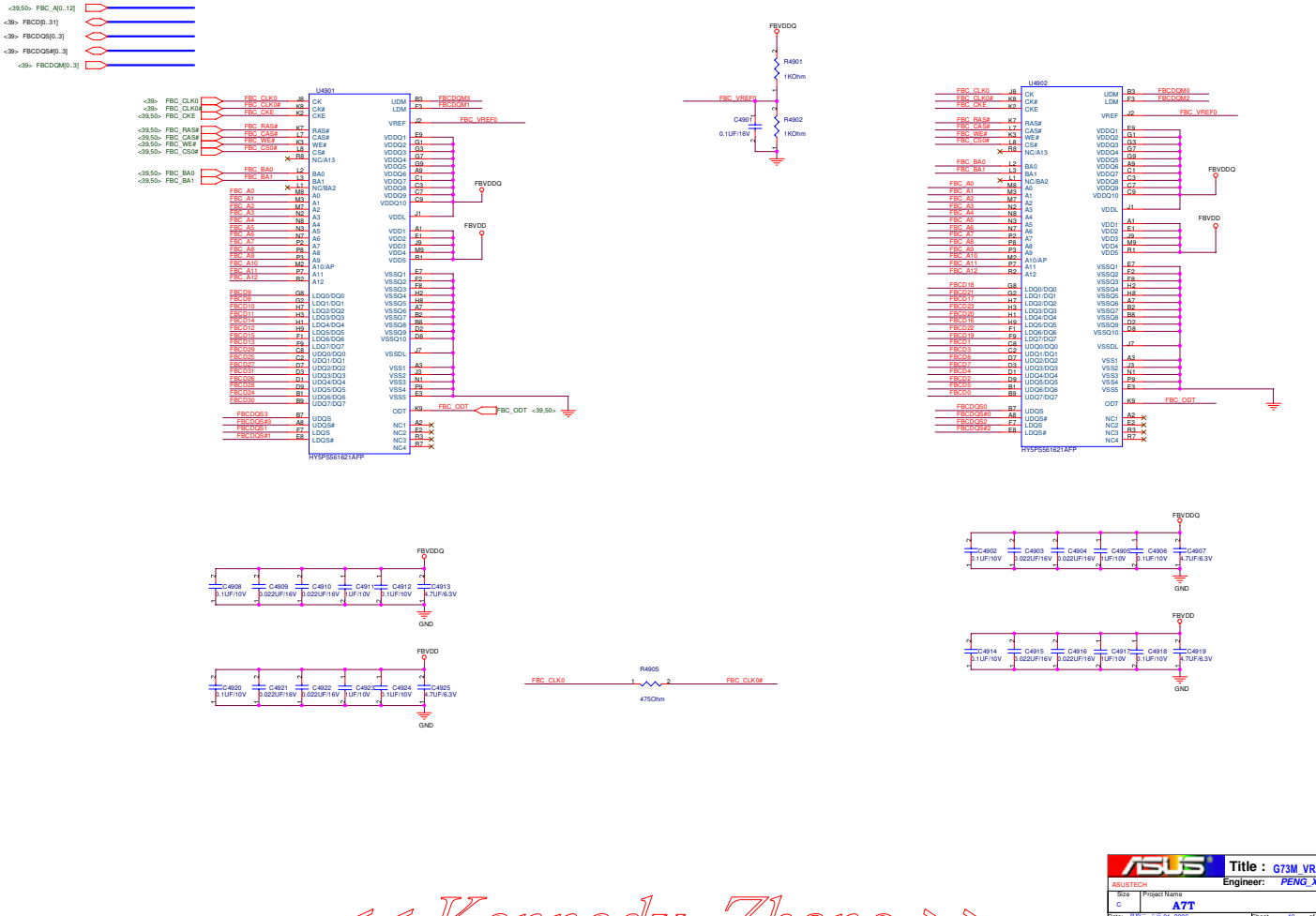


ASUSTeK	Title : G73M_VRAM1		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 01, 2006	Sheet 47 of 73		

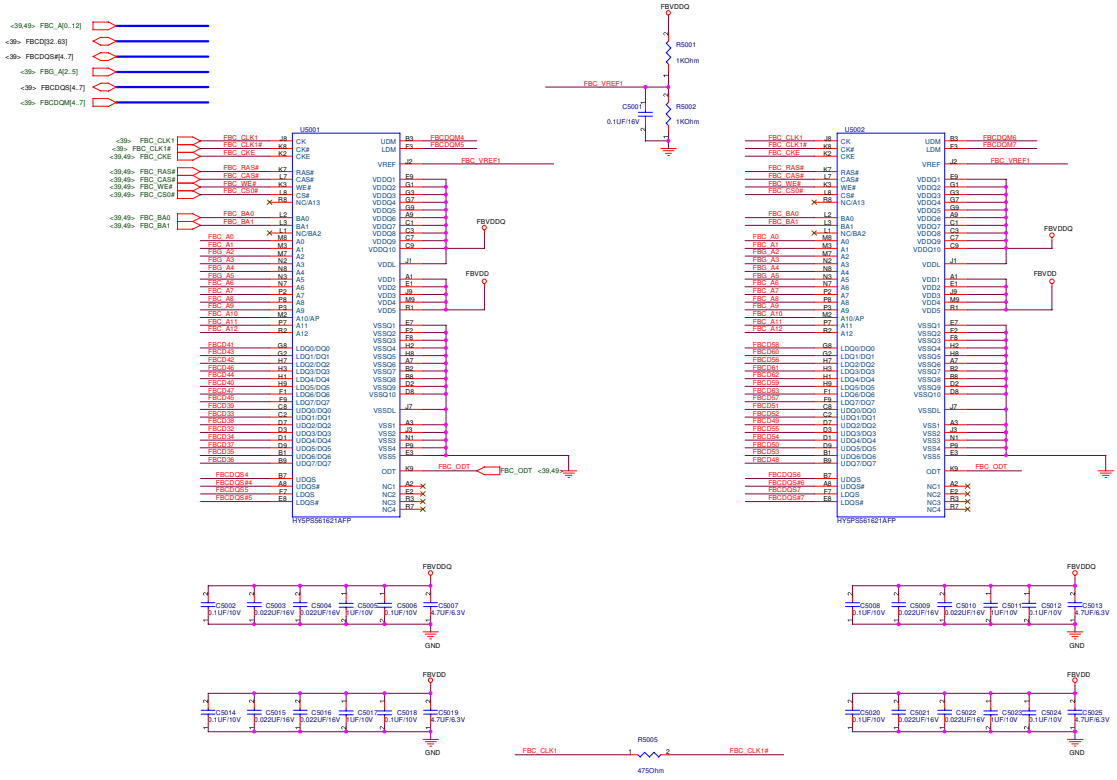


<< Kennedy_Zhang >>

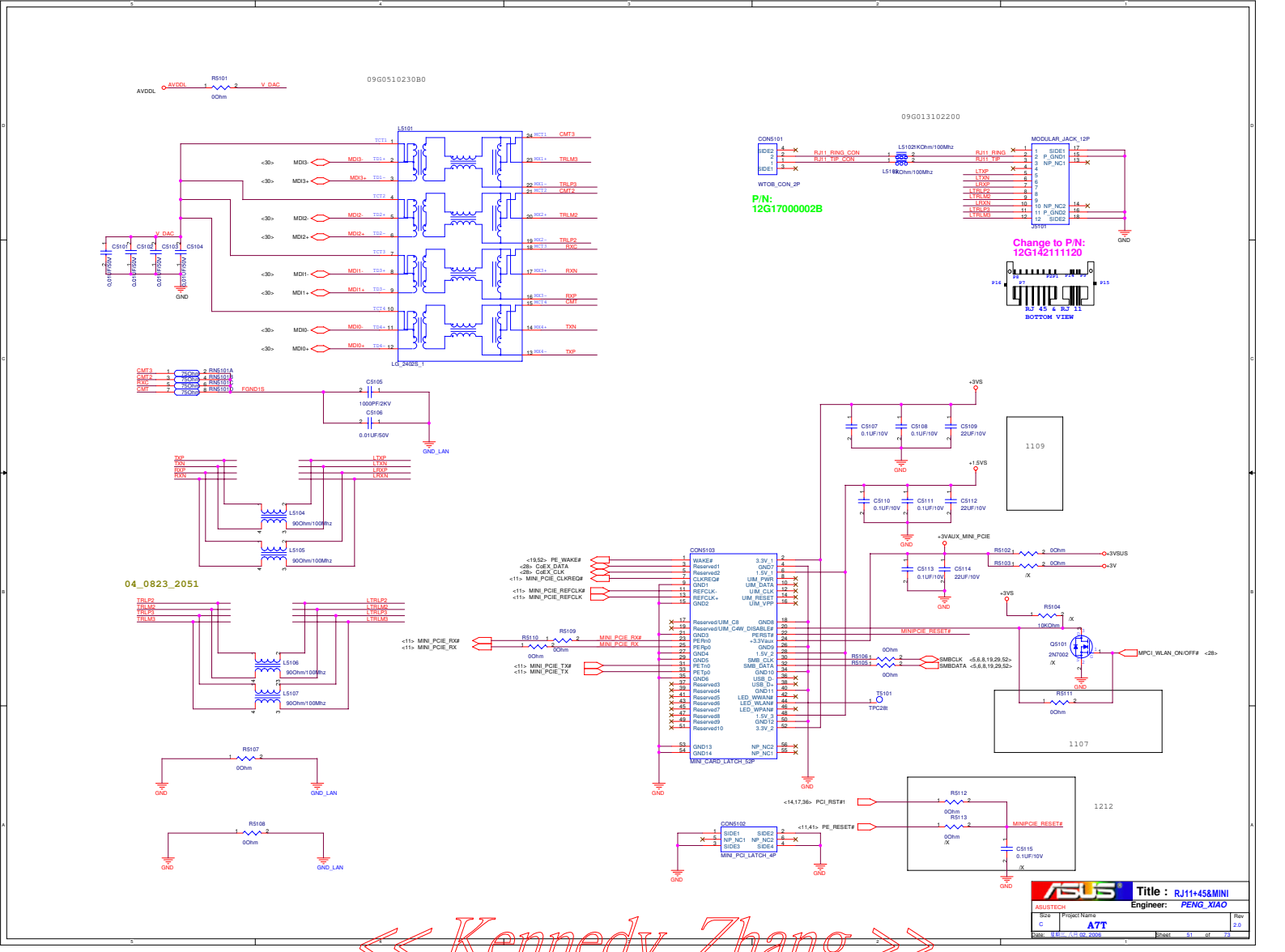
ASUSTeK	Title : G73M_VRAM2		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 01, 2006	Sheet 48 of 73		

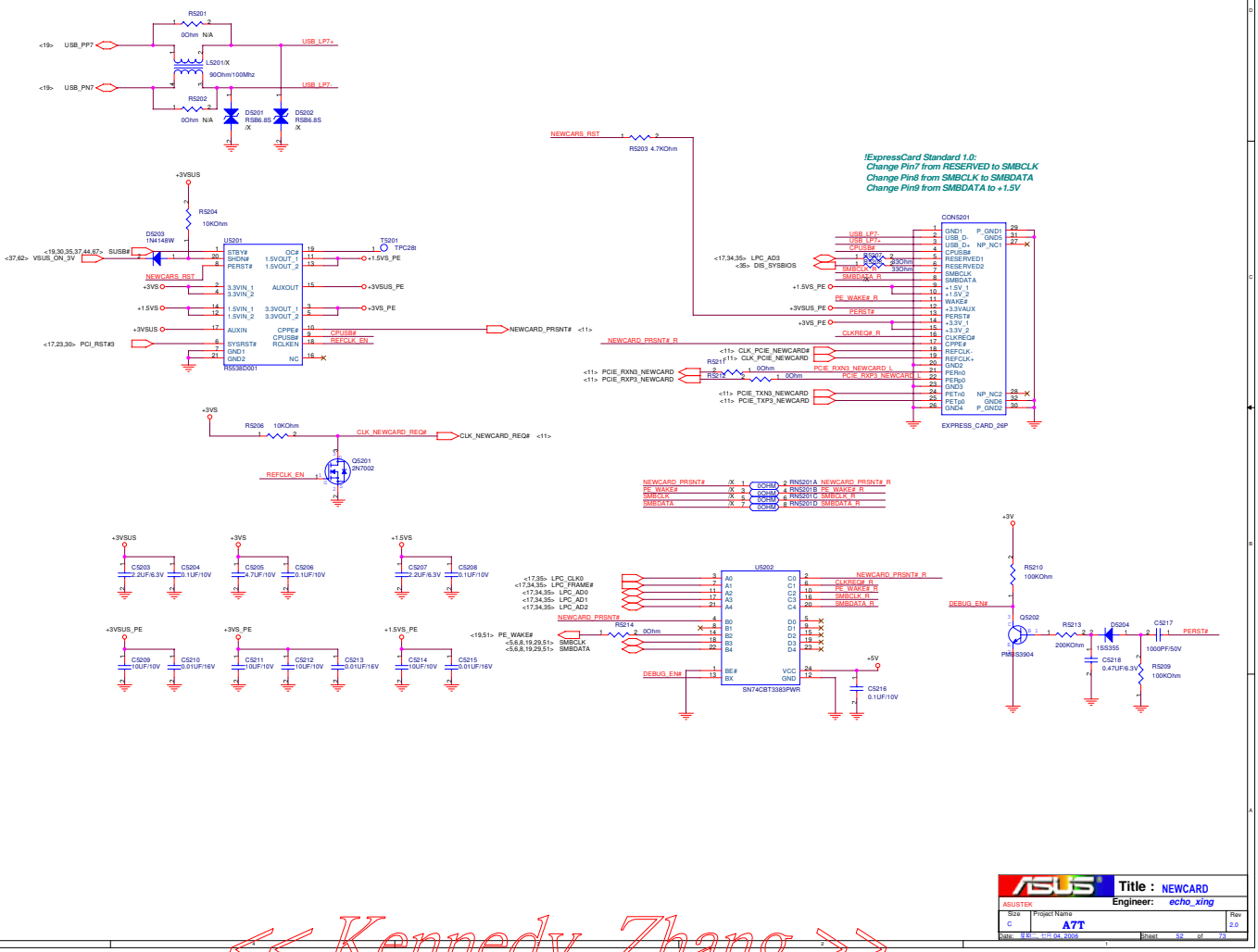


ASUSTeK	Title : G73M_VRAM3		
	Engineer: PENG_XIAO		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 01, 2006	Sheet 49 of 73		



ASUSTeK	Title : G73M-VRAM4	
	Engineer: PENG_XIAO	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期二, 八月 01, 2006	Sheet 50 of 73	





ASUSTEK

Title : NEWCARD

Engineer: echo_xing

Size	Project Name	Rev
C	A7T	2.0

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PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	A
CARD READER	AD17	1	C
1394	AD17	1	B
MINIPCI (802.11a/b/g)	AD19	3	B,C
MINIPCI (TV)	AD18	0	A,D

Host	SM-Bus Device	SM-Bus Address	Device
MCP51	Voice DSP	1100000x (C2H)	VP1010
MCP51	SO-DIMM 0	1010000x (A0H)	DDR SOCKET1
MCP51	SO-DIMM 1	1010010x (A4H)	DDR SOCKET2
MCP51	Thermal Sensor	0101110x (5CH)	ADT7463 (Optinal)
	PIC	1001001x (92H)	Charge IC
	M38857	0001000x (10H)	KBC control IC
	BQ2060	16H-17H	Battery sensor IC

MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 1	INPUT	KB_SCI#				+3VS
GPIO 2	INPUT	SIO_SMI#				+3VS
GPIO 3	OUTPUT	BACK_OFF#	LOW	HIGH	Off	+3VS
GPIO 4	OUTPUT	FWH_WP#	LOW	LOW	Off	+3VS
GPIO 5	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 6						+3VSUS
GPIO 7	OUTPUT	BT_LED_EN#	**LOW**	HIGH	Driven	+3VSUS
GPIO 8						
GPIO 9						
GPIO 10						
GPIO 11	OUTPUT	BT_ON#	LOW	LOW	Off	+3VS
GPIO 12	OUTPUT	WLAN_ON#	LOW	LOW	Off	+3VS
GPIO 13						
GPIO 14						
GPIO 15	INPUT	PROCHOT#	LOW	HIGH	Off	
GPIO 16						
GPIO 17		LID#				+3VSUS
GPIO 18		USB_OC#0				+3VSUS
GPIO 19		USB_OC#1				+3VSUS
GPIO 20		USB_OC#2				+3VSUS
GPIO 21		USB_OC#3				+3VSUS
GPIO 22		ACZ_SDIN0				+3VSUS
GPIO 23		ACZ_SDIN1				+3VSUS
GPIO 24						
GPIO 25						
GPIO 26						
GPIO 27		SMB_CLK				+3VSUS
GPIO 28		SMB_DATA				+3VSUS
GPIO 29		SMB_ALERT#				+3VSUS
GPIO 30		PCI_PME#				+3VSUS
GPIO 31		SIO_PME#				+3VSUS
GPIO 32		EXTSMI#				+3VSUS
GPIO 33		RI#				+3VSUS
GPIO 34		SUS_CLK	PULL-DOWN:Normal mode select			
GPIO 40						
GPIO 41						
GPIO 46		SPDIFO	PULL-HIGH:SIO_CLK select 24MHz			+3VS
GPIO 47	INPUT	RF_OFF_SW#	LOW	HIGH	Off	+3VS
GPIO 61	INPUT	PANEL_ID0			Off	+3VS
GPIO 62	INPUT	PANEL_ID1			Off	+3VS

KBC GPIO	I/O Mode	Signal	Active	S0 Default	S3
P23(Pin 35)					
P22(Pin 36)	OUTPUT	BAT_LEARN	HIGH	LOW	LOW
P21(Pin 37)		KBC_P21			
P20(Pin 38)	OUTPUT	KBCRSM	HIGH	LOW	LOW
P42(Pin 23)	OUTPUT	WATCHDOG	HIGH	LOW	LOW
P43(Pin 22)	INPUT	LID_KBC#			
P44(Pin 21)					
P45(Pin 20)	OUTPUT	KB_GATEA20			
P46(Pin 19)	OUTPUT	KBSCI#			
P47(Pin 18)		PM_CLKRUN#			
P50(Pin 17)	INPUT	BAT_LLOW#_OC			
P51(Pin 16)	INPUT	KB_ID0			
P52(Pin 15)	INPUT	KB_ID1			
P53(Pin 14)	OUTPUT	CLR_DJ#	LOW	LOW	Driven
P54(Pin 13)	INPUT	BAT_SEL#			
P55(Pin 12)	INPUT	BAT1_IN#_OC			
P56(Pin 11)	OUTPUT	FAN_DA1(Optinal)	Analog	Analog	Driven
P57(Pin 10)	OUTPUT	INVTER_DA	Analog	Analog	Driven
P67(Pin 74)	OUTPUT	DJ_LED#	LOW	HIGH	HIGH
P66(Pin 75)	INPUT	SWDJ_EN#			
P65(Pin 76)	INPUT	CHG_FULL_OC			
P64(Pin 77)	INPUT	ACIN_OC			
P63(Pin 78)	INPUT	DISTP_SW#			
P62(Pin 79)	INPUT	P4GEAR_SW#			
P61(Pin 80)	INPUT	**EMAIL_SW#**			
P60(Pin 1)	INPUT	**INTERNET_SW#**			
P75(Pin 4)		KB_CLK			
P74(Pin 5)		MS_CLK			
P73(Pin 6)		TPAD_CLK			
P72(Pin 7)		KB_DAT			
P71(Pin 8)		MS_DAT			
P70(Pin 9)		TPAD_DAT			
P77(Pin 2)		SMC_BAT			
P76(Pin 3)		SMD_BAT			
P27(Pin 31)					
P26(Pin 32)	OUTPUT	NUM_LED#	LOW	Define	HIGH
P25(Pin 33)	OUTPUT	CAP_LED#	LOW	Define	HIGH
P24(Pin 34)	OUTPUT	SET_PLTRSTNS#	LOW		
P40(Pin 27)	OUTPUT	EXT_SMI			
P41(Pin 26)	OUTPUT	EMAIL_LED#	LOW	HIGH	HIGH

MCP51 GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 16	OUTPUT	DSP_SHI_EN	HIGH	HIGH	Off	+5VS
GPIO 53	INPUT	SUSC#	LOW	HIGH	H/L	+5VS
GPIO 45	INPUT	SUSB#	LOW	HIGH	LOW	+5VS
GPIO 11	INPUT	PROCHOT#	LOW	HIGH	Off	+5VS

ASUSTeK

Title : SYS RESOU

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 53 of 73

Rev	Date	Description
1.1		
	1101	add throttle circuit
	1102	add HD and ODD LED control
	1103	change therm sensor
	1104	add de-glitch circuit for NVIDIA suggestion
	1105	add damping resistor for LPC bus
	1106	change C1319,20,29,30,39,40,41,42 package, add C1354,55,56,57 for therm issue
	1107	add R5111 for wireless disable option
	1108	add MCP51 LCD control signal
	1109	modify C5109,12,14,CE2601 P/N for high limit
1.2		
	1201	swap LVDS control signal
	1202	remove Q3608 for charge LED
	1203	change R3609 and R3612's pull high power to +3V
	1204	change R1612 P/N
	1205	swap speaker
	1206	add C2936
	1207	change HDD LED control
	1208	change bead to inductor for SI
	1209	add R1214 for RGB signal
	1210	add R1964 for NVIDIA suggestion
	1211	add C1415 for LCD
	1212	add R5112 R5113 and C5115 for MINIPCIE reset sequence

Rev	Date	Description

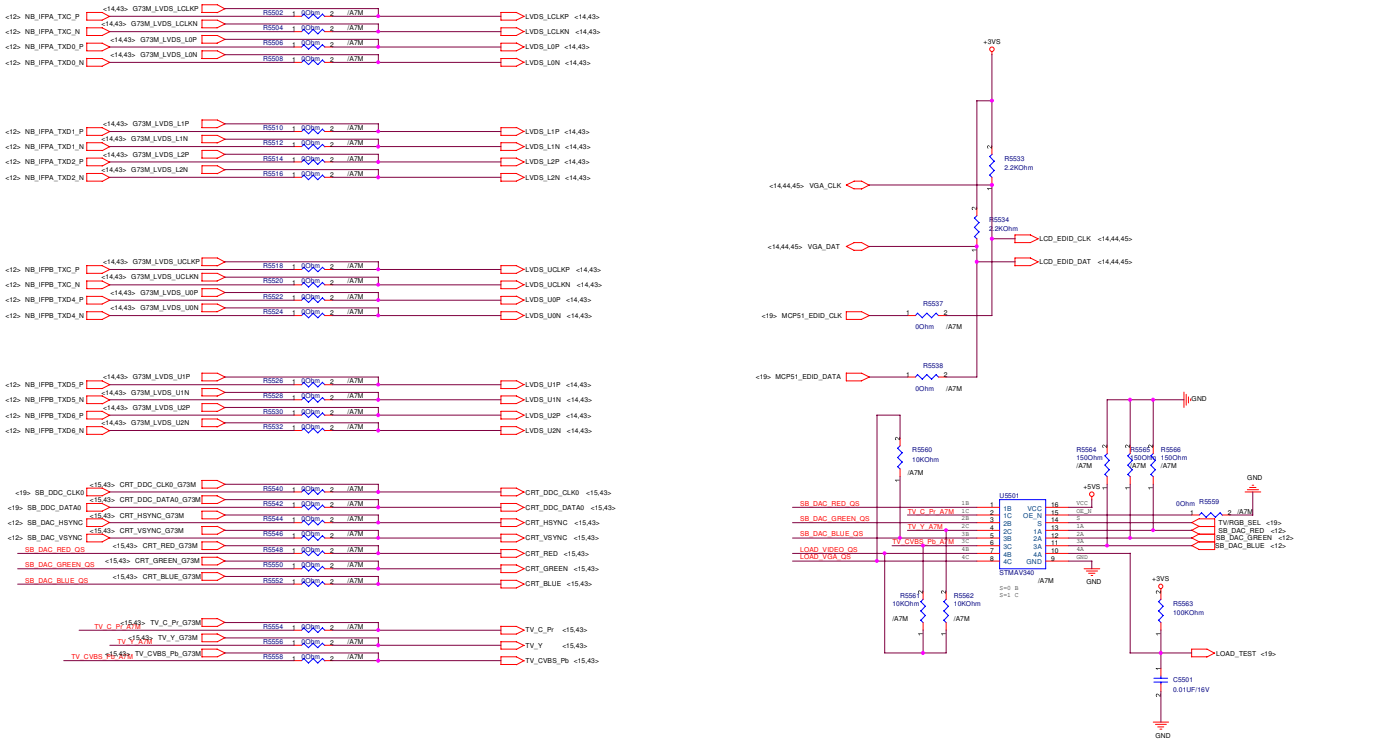
ASUSTECK

Title : HISTORY

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 54 of 73



ASUSTeK	Title : LVDS SWITCH		
	Engineer: DEL_TAN		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 55 of 73		

Title : HISTORY

ASUSTECH

Engineer: DEL_TAN

Size	Project Name	Rev
C	A7T	2.0

Date: 星期日, 四月 29, 2006 Sheet 58 of 73

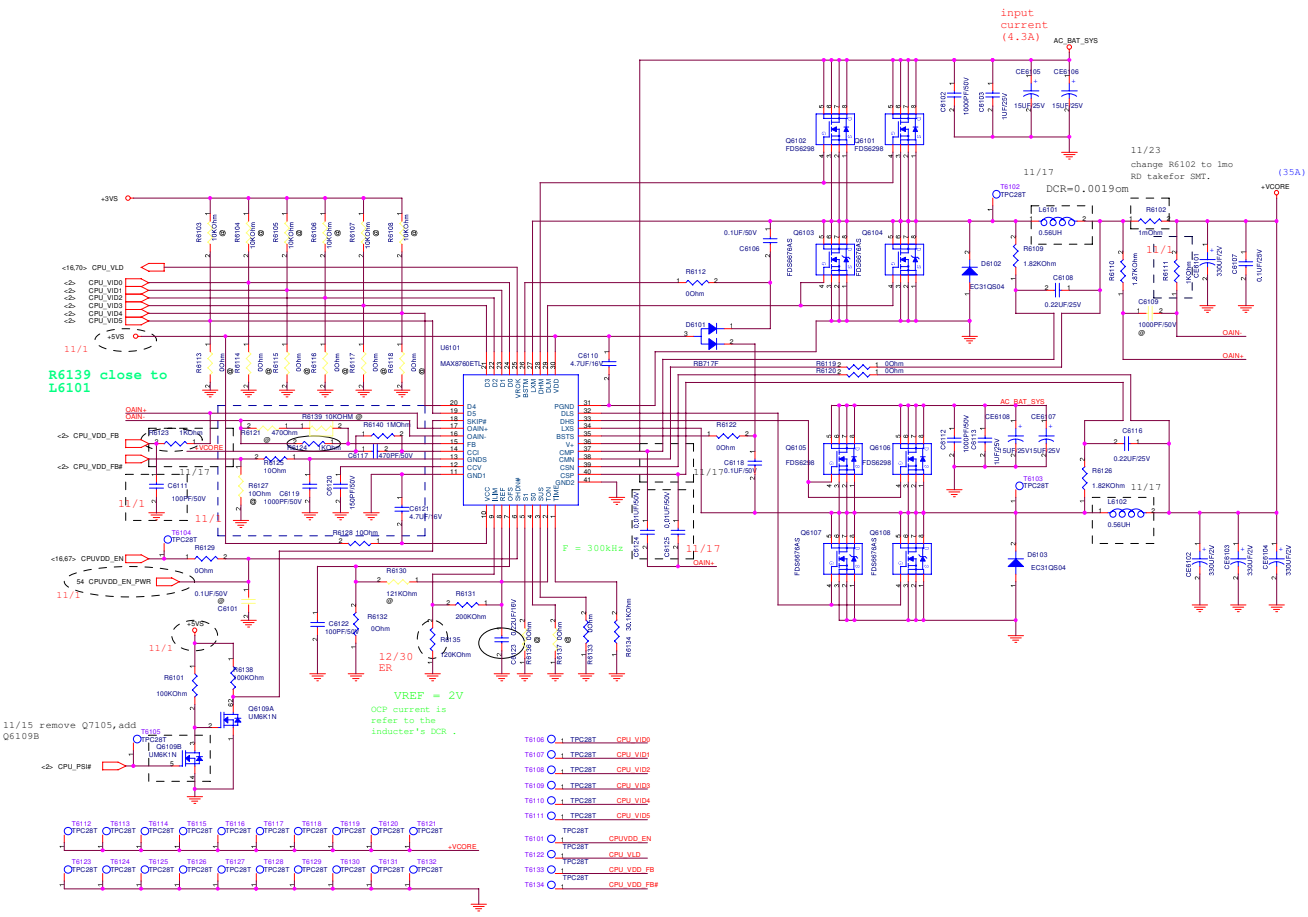
<< Kennedy_Zhang >>

ASUSTECH	Title : HISTORY	
	Engineer: DEL_TAN	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 57 of 73	

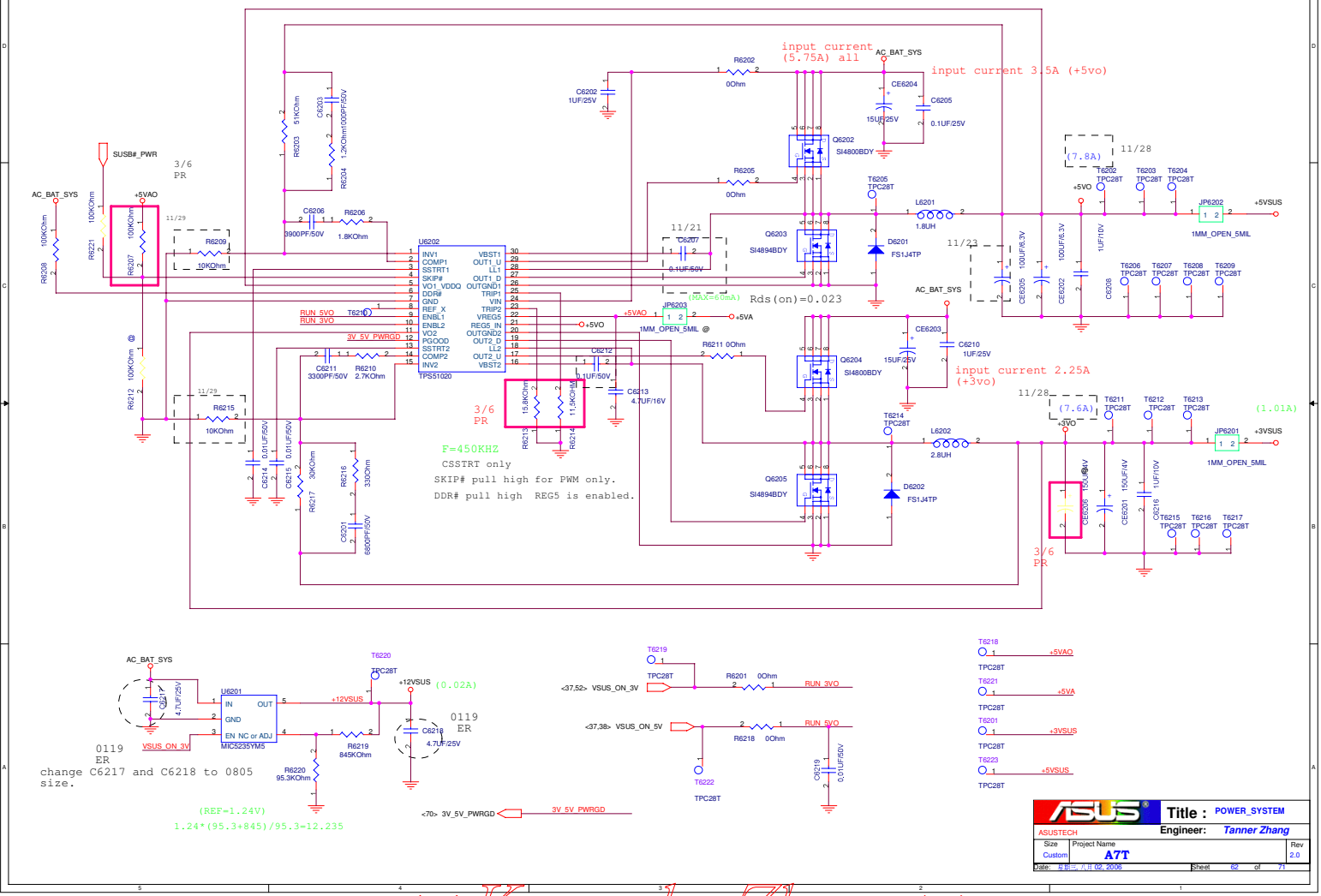
ASUSTECH	Title : HISTORY	
	Engineer: DEL_TAN	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 58 of 73	

ASUSTECH	Title : HISTORY	
	Engineer: DEL_TAN	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 59 of 73	

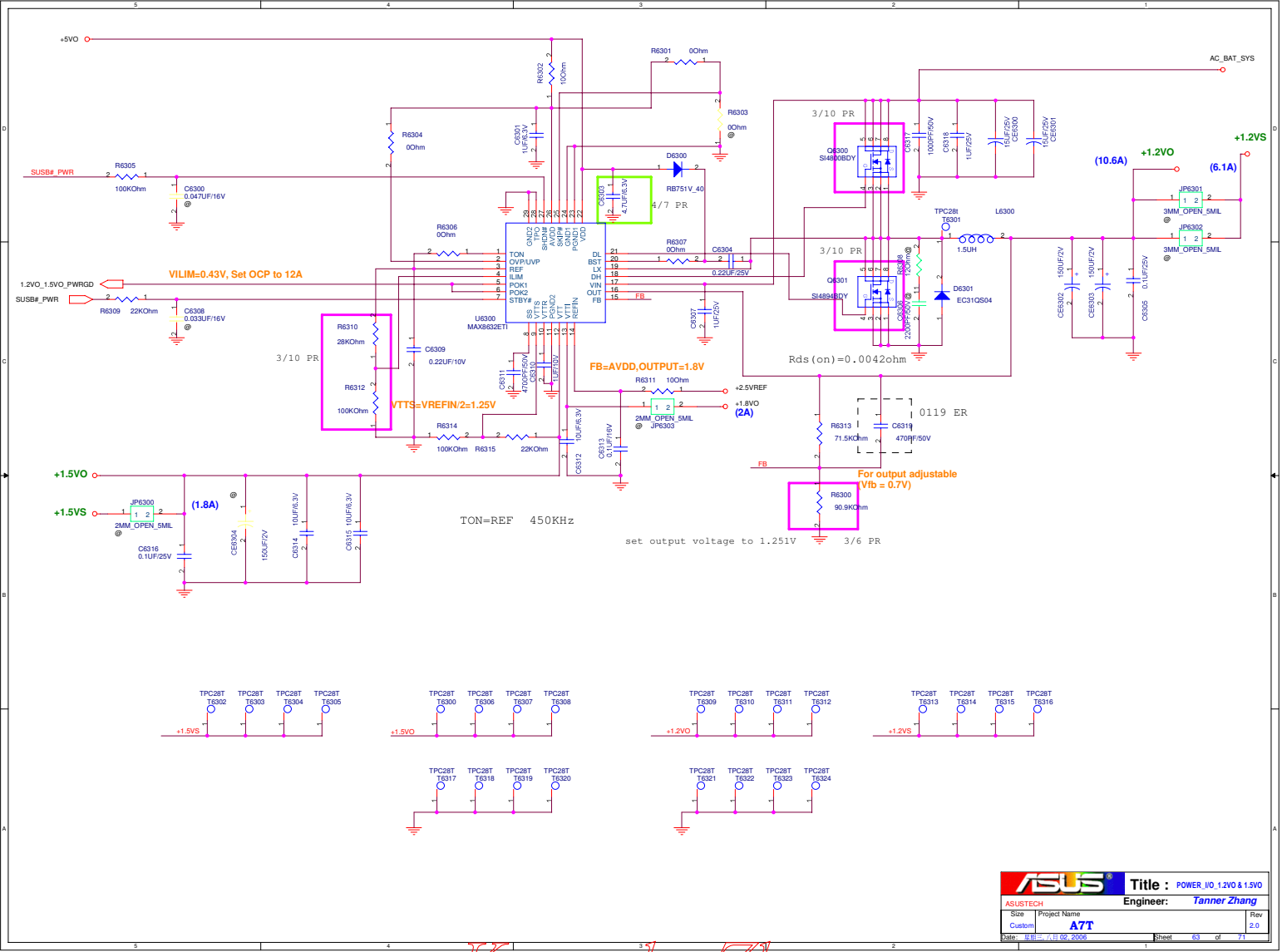
ASUSTECH	Title : HISTORY	
	Engineer: DEL_TAN	
Size: C	Project Name: A7T	Rev: 2.0
Date: 星期日, 四月 29, 2006	Sheet 60 of 73	



ASUSTek	Title : POWER_VCORE		
	Engineer: Tanner Zhang		
Size: C	Project Name: A7T		Rev: 2.0
Date: 星期二, 八月 02, 2006	Sheet 61 of 71		

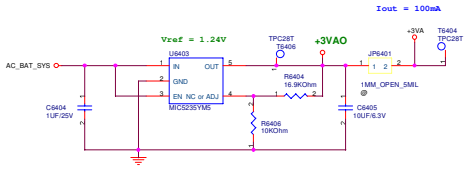


<< Kennedy_Zhang >>



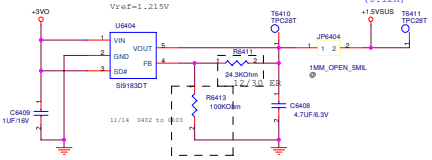
ASUSTECH	Title : POWER_I/O_1.2VO & 1.5VO		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A7T		Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 63 of 71		

<< Kennedy_Zhang >>

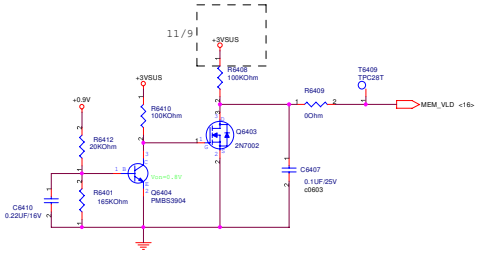


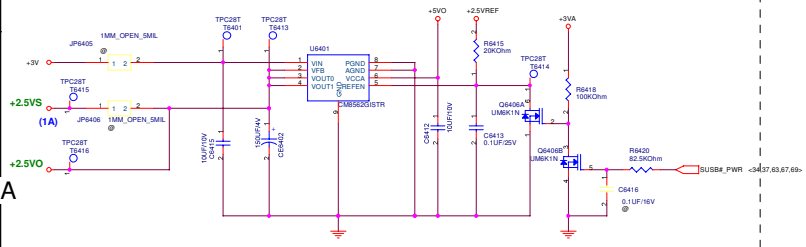
+3VA

+1.5VS

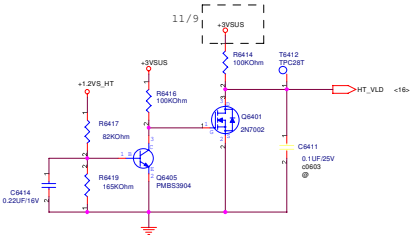


+1.5VSUS

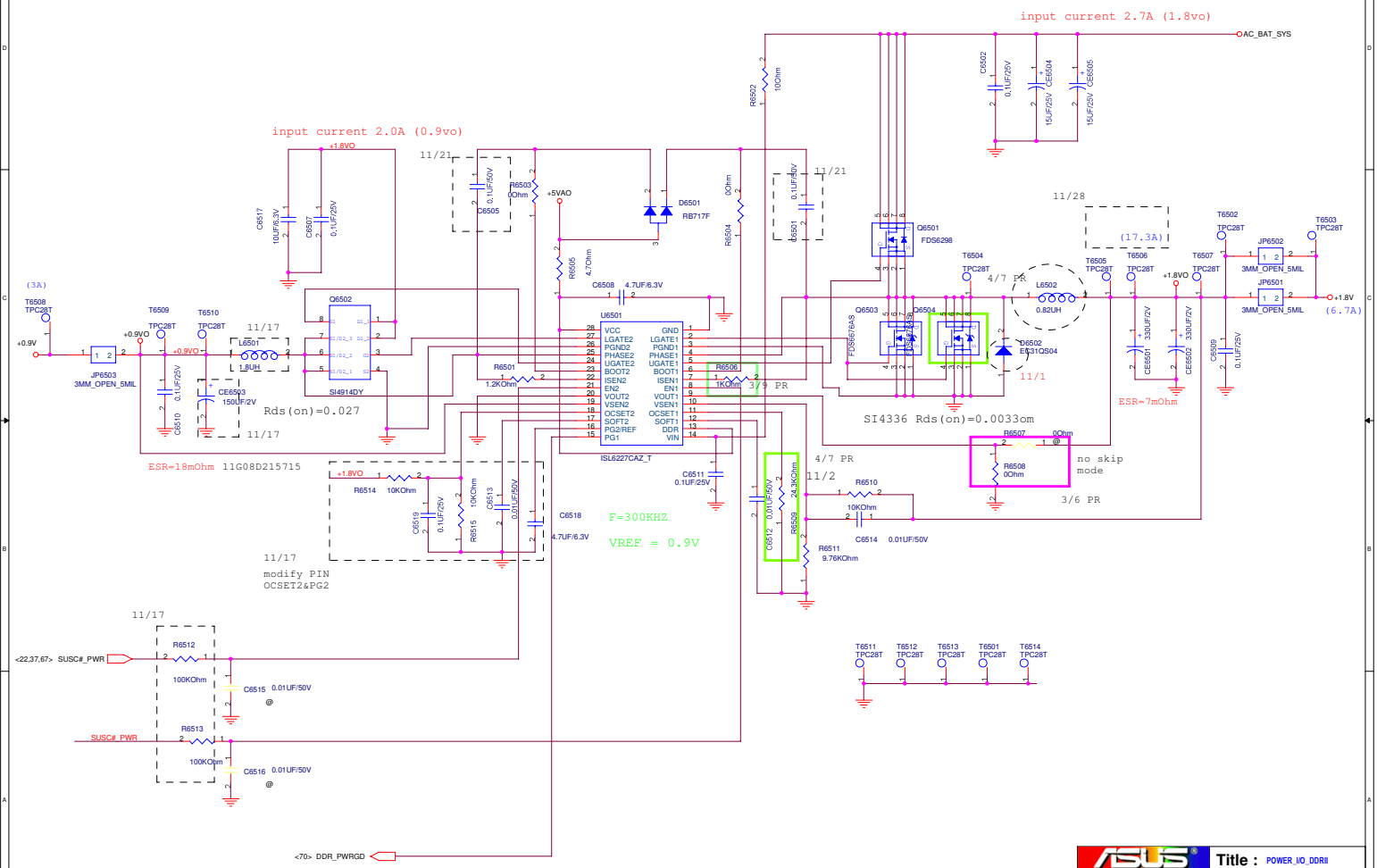




+2.5VS



ASUSTECH	Title : POWER_IO_LDO		
	Engineer: Tanner Zhang		
Size: C	Project Name: A7T		Rev: 2.0
Date: [illegible] 07, 2006	Sheet 64 of 71		



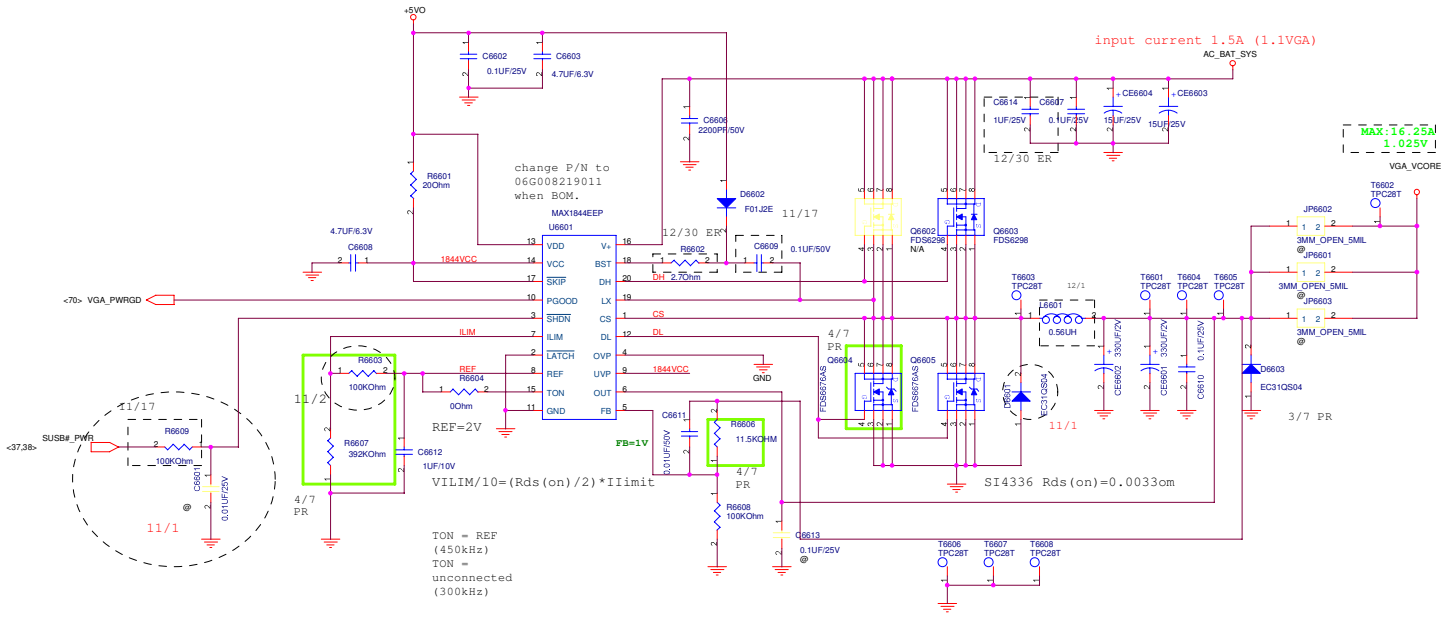
ASUSTECH

Title : POWER_I/O_DDRII

Engineer: Tanner Zhang

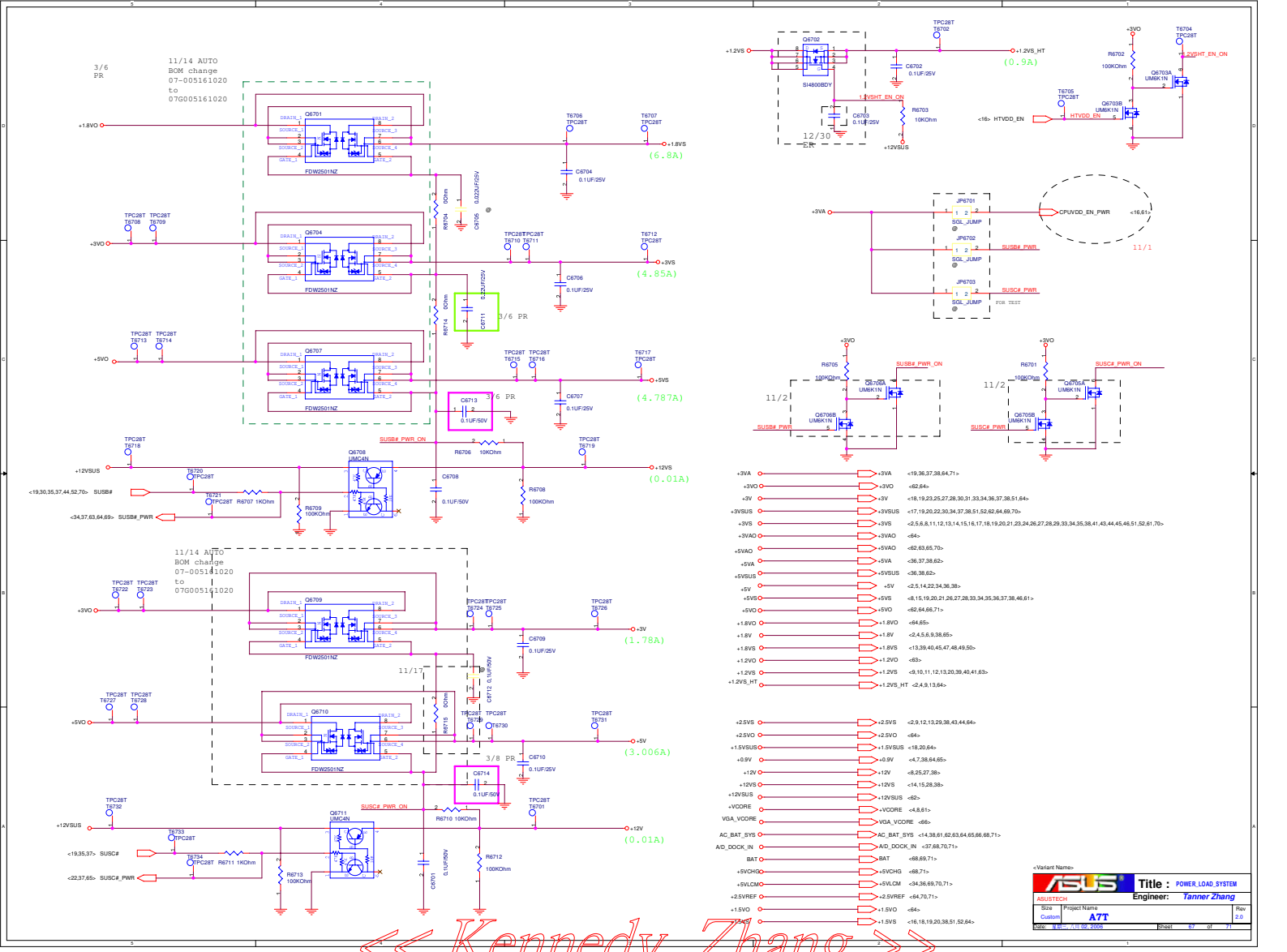
Size	Project Name	Rev
Custom	A7T	2.0

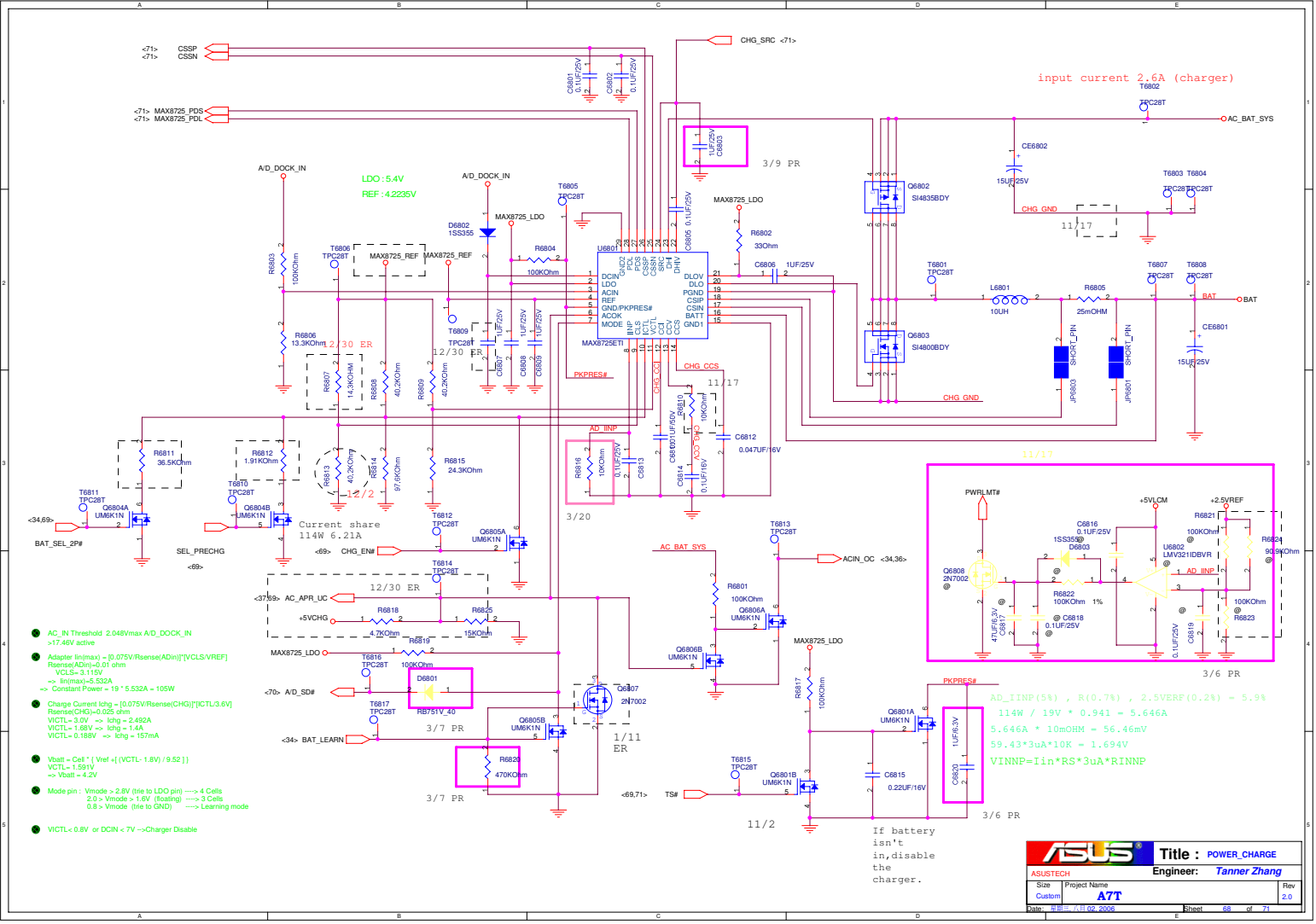
Date: 星期三, 八月 02, 2006 Sheet 65 of 71



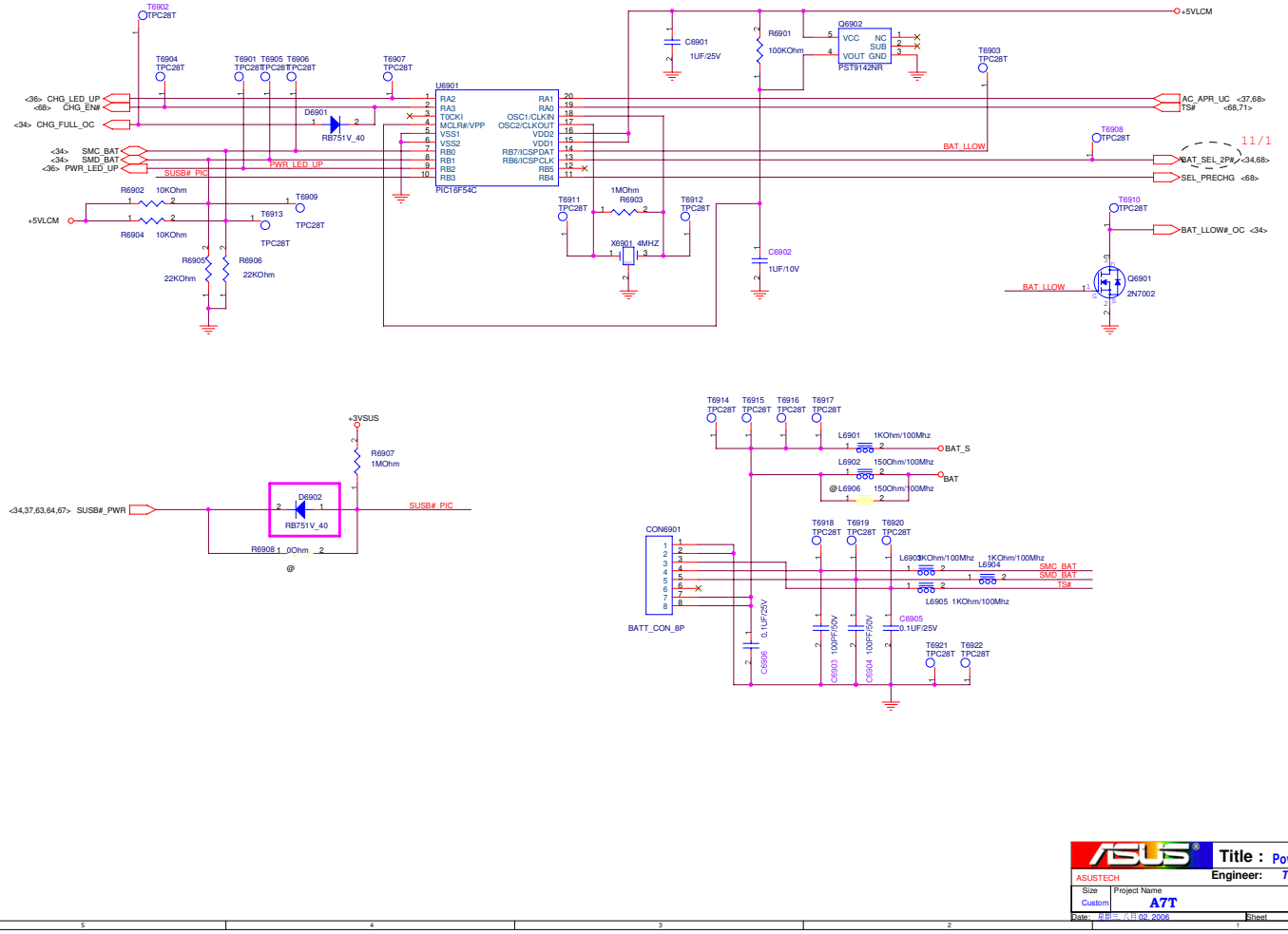
<Variant Name>

ASUSTek	Title : POWER_VGACORE	
	Engineer: Tanner Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 66 of 71	





<< Kennedy_Zhang >>



ASUSTEK	Title : Power_PI		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A7T	Rev: 2.0	
Date: 星期三, 八月 02, 2006	Sheet 69 of 71		

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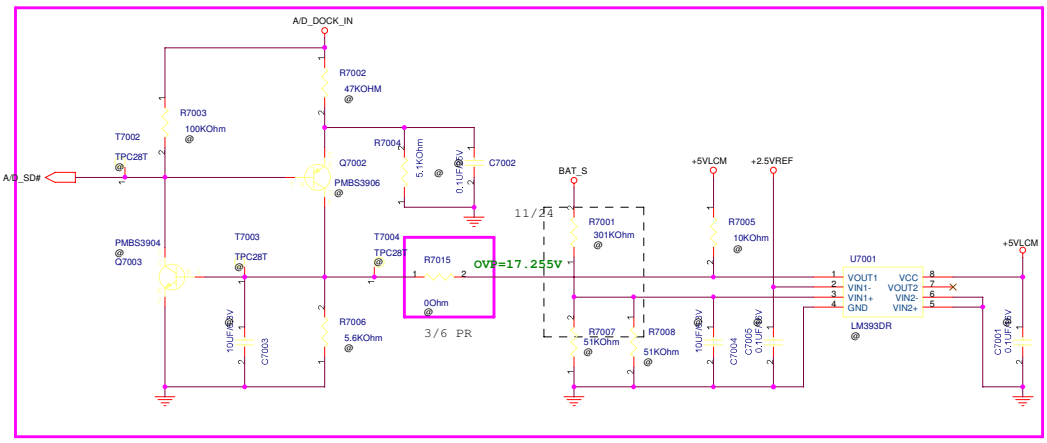
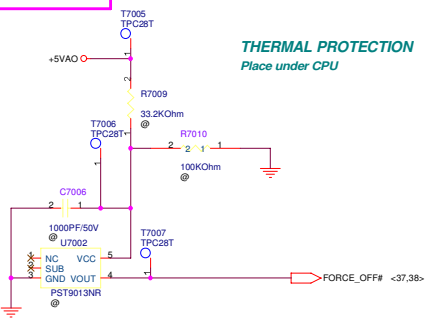
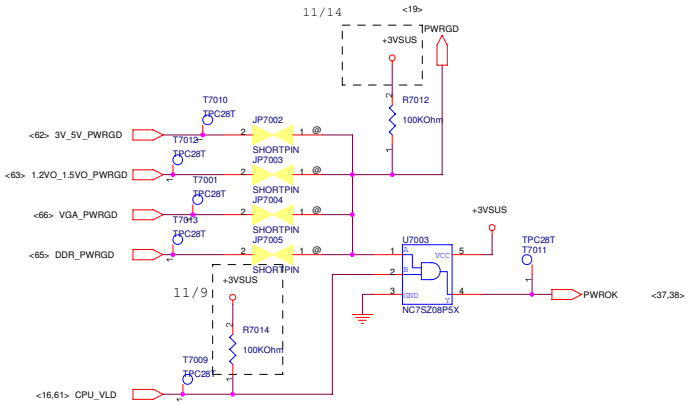


3/7 PR



THERMAL PROTECTION

Place under CPU



ASUSTECH	Title : POWER_PROTECT		
	Engineer: Tanner Zhang		
Size: Custom	Project Name: A7T		Rev: 2.0
Date: 星期十, 八月 02, 2006	Sheet 70 of 71		

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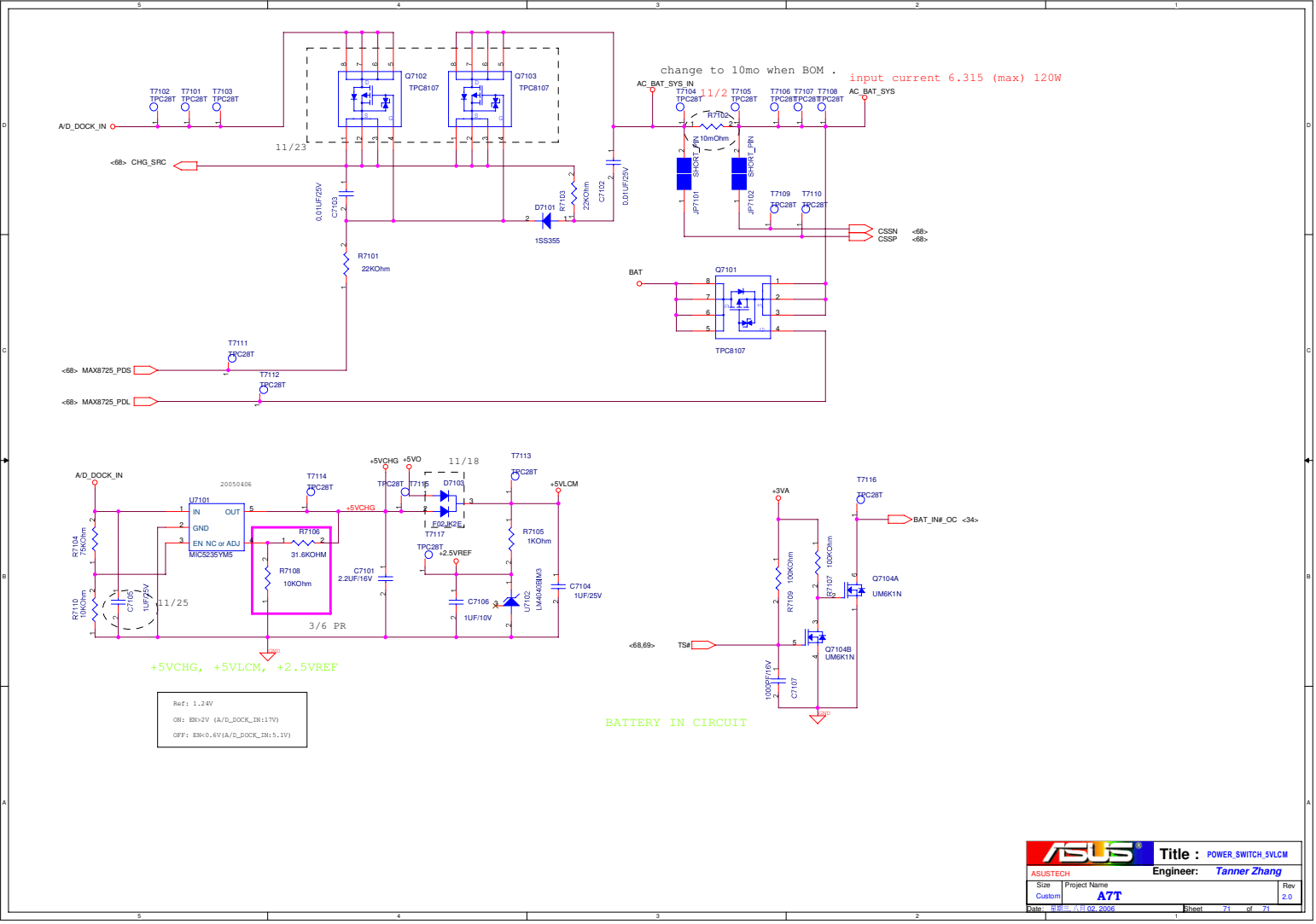

ASUSTECH	Title : POWER_SWITCH_5VLCM	
	Engineer: Tanner Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 71 of 71	

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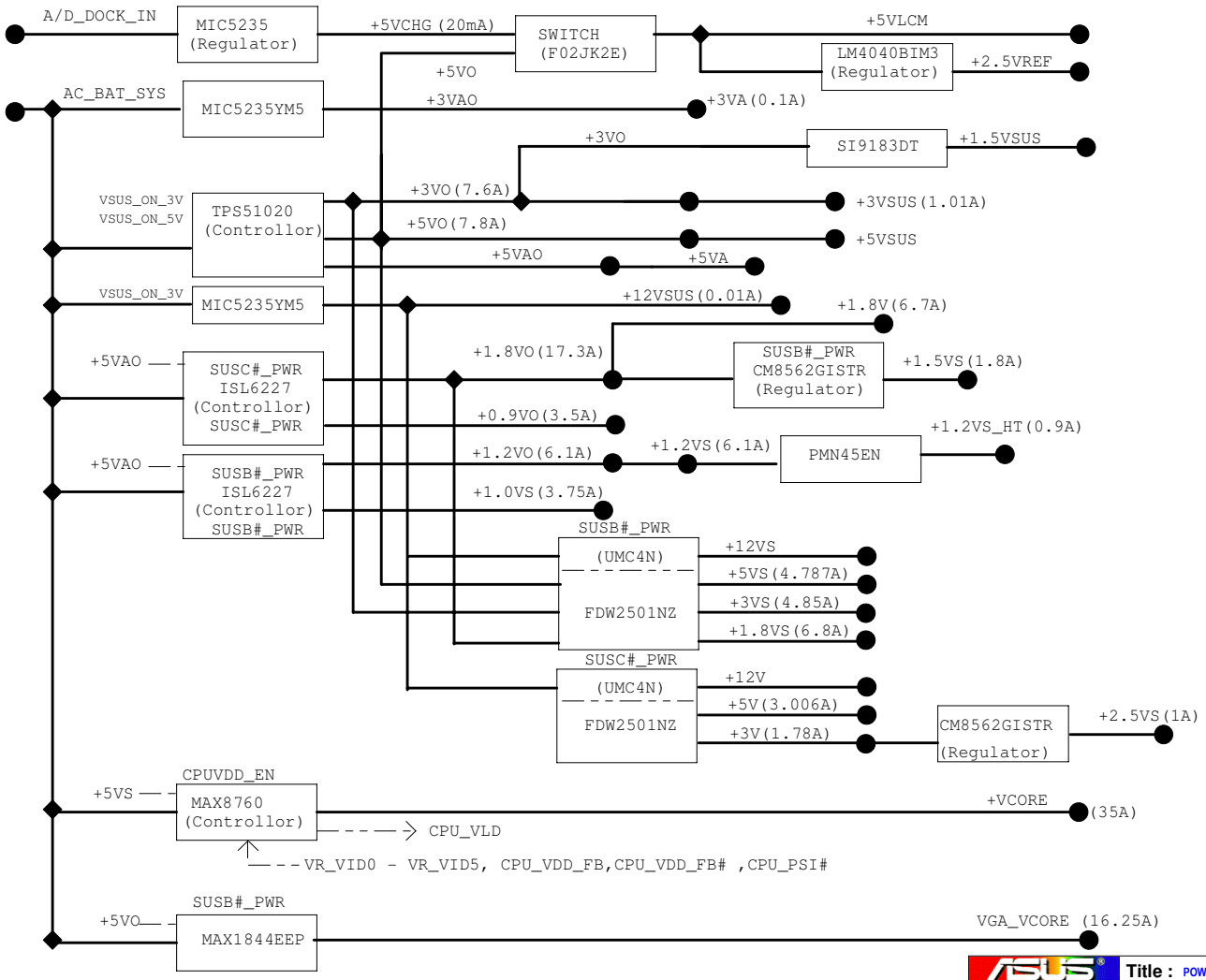

ASUSTECH

Title : POWER FLOWCHART

Engineer: Tanner_Zhang

Size	Project Name	Rev
Custom	A7T	2.0

Date: 星期三, 八月 02, 2006 Sheet 72 of 73

<< Kennedy_Zhang >>

Revision History

Power

R1.0

2006.01.03

1.Add 150UF/4V (15mohm) to +3VO output for the gate Feq. is wrong.
2.change c6708.1 to Q6710.2 for +5vs's gate softstart.
3.change R6135 to 120K for Vcore OCP set
4.Add 1uf/25V to VGACORE input for gate noise.
5.change C6703 to N/A for load switch 1.2VS_HT gate
6.Change R6506 to 470ohm.and R6509 to 100Kohm for 1.8V ocp set
7.add R6825 15Kohm and change R6818 to 4.7Kohm for AC_IN wrong motion.
8.Change C6807 to 4.7uf/25V for AD_IN noise
9.Remove JP6303
10.Change R6602 0ohm to 2.7ohm(0603 5%) for vgacore high side gate noise
11.Change Q6702 to SI4800 for 1.2vs_HT low voltage.
12.Change R6606 to 1K (0603 1%) for VGACORE output 1.02V
13.Change R6807 to 29.4K(0603 1%) for current share point set.
14.For PWRLMT# 114w,change R6823 to 100k(0603 0.1%),and change R6824 to 90.9K(0603 1%)
15.change R6511 to 9.76K(0603 1%) for 1,8vs voltage set.
16.Change R6312 R6314 to 7.5K(0603 1%) for 1.2vs voltage set.
17.Change R6411 to 24.3K.(0603 1%) for 1.5VSUS voltage set.
18.C6411 change to @

2006.01.04

1.change C6217 to 4.7UF/25v(0805)11G235247512320
2.change C6807 to 1uF/25V(0805) 11G235310532360
3.change C7105 to 1UF/25V(1206) 11G236110512320

2006.01.05

1.Change PAGE 68 MAX8725_LDO to MAX8725_REF.
2.change R6814 (49.9K) to 97.6k(1%)10G213976213030
Change R6812(1.5K) to 1.91K(1%) 10G213191113030
Change R6811(22.6K) to 36.5k(1%) 10G213365213010
Change R6809(53.6k) to 40.2K(1%) 10G213402213030
Change R6815(22.6k) to 24.3K(1%) 10G213243213030
Change R6807(40.2k) to 14.3K(1%) 10G213143213030
Change R6813(55.1k) to 40.2K(1%) 10G213402213030

2006.01.06

1.change L6501 to 1.8UH(09G02X183100) for 0.9 transit ripple.
2.for battery OVP 17.25V, change R7001(200k 0.1%) to 301K(0.1%) 10G213301323030
Change R7007(100K 0.1%) to 51K(0.1%) 10G213510223030
Set R7008 to @ When A7M bom
3.change L6202 to 2.8uh. (09G02X183100)
4. add Q6807 for auto battery learning error.

System

R1.0

ASUSTECH	Title : HISTORY	
	Engineer: Tanner_Zhang	
Size: Custom	Project Name: A7T	Rev: 2.0
Date: 星期三, 八月 02, 2006	Sheet 73 of 73	